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HP 12967A
SYNCHRONOUS COMMUNICATIONS INTERFACE DIAGNOSTIC

for

hp-2100 SERIES COMPUTERS

reference manual

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Section I

INTRODUCTION

1-1. GENERAL

This diagnostic checks the operation of the Synchronous Communications Interface. The basic I/O portion of the card, which includes the Flag and Control circuits, will be tested. The interface will be used with skip-on-flag, interrupt, and direct memory access (DMA)*. The status, control, receive, and transmit features will be tested using the "self test" function of the interface in conjunction with the test hood.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. HP 2100 series computer with at least 4K of memory.
b. HP 12967A Synchronous Communication Interface Kit with hooded self-test connector, Part No. 12967-60003 (the self-test connector wiring is shown in Figure 1-1).
c. A paper tape reading device (for loading only).
d. Optional: A console teleprinter device for message reporting.
e. Optional: A DMA/DCPC board for complete testing of the interface.

1-3. REQUIRED SOFTWARE

The following software is required:

a. Diagnostic Configurator Product No. 24296 used for equipment configuration and as a console device driver. The product includes the following part no.:

Binary object tape	Part No. 24296-60001
Manual	Part No. 02100-90157

b. HP 12967A Synchronous Communication Interface Diagnostic binary object tape Part Number 12967-16001.

Note: The diagnostic serial number (DSN) for the synchronous communication interface diagnostic, which resides in memory location 126 (octal), is 103116 (octal).

*Or dual-channel port controller (DCPC).

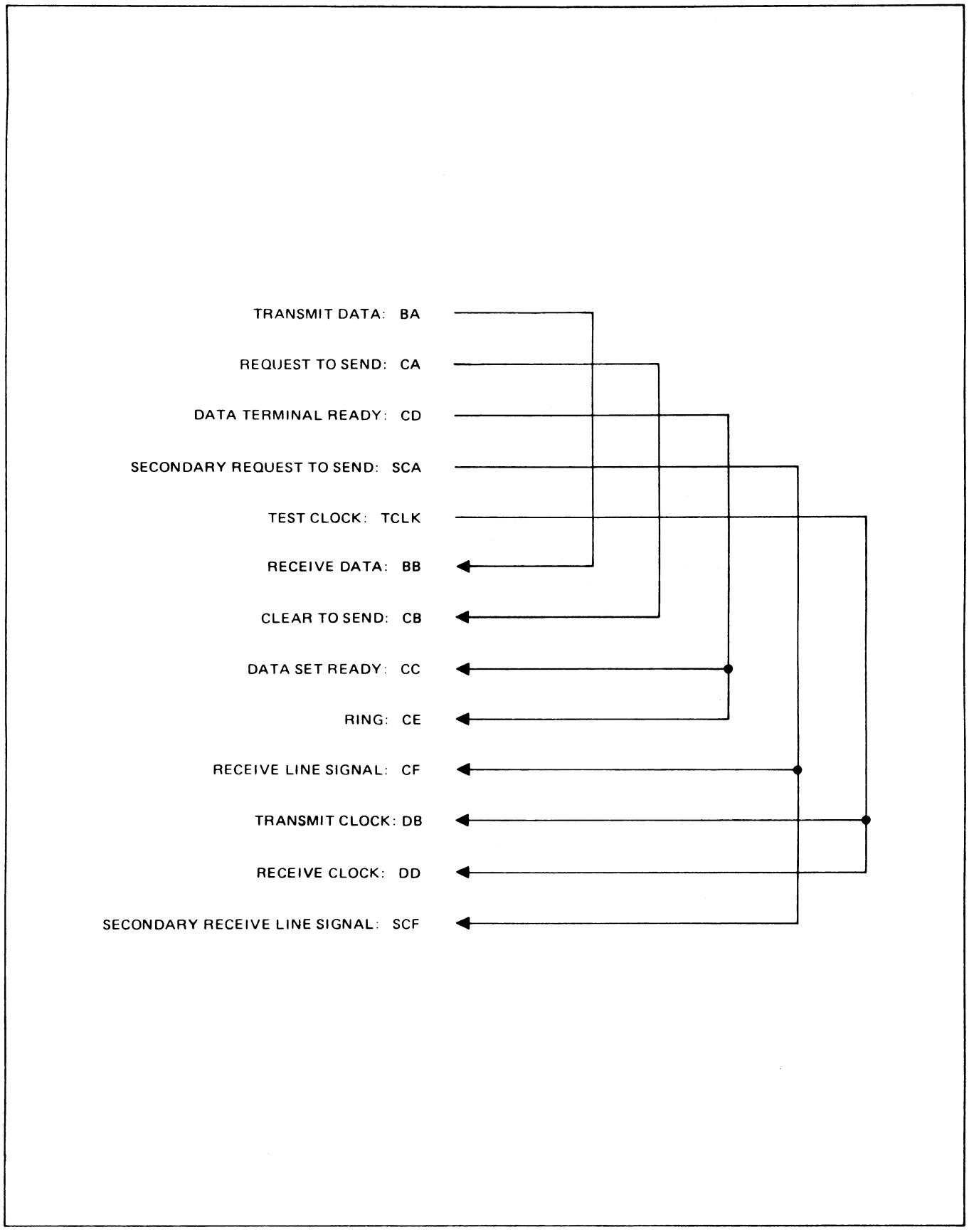


Figure 1-1. Self-Test Connector Wiring

Section II

PROGRAM ORGANIZATION

2-1. ORGANIZATION

This 4K diagnostic program consists of 1Ø tests plus a control and initialization section. The initialization and control sections accept the select code, sync character and options required by the tests. The tests are called into execution by the control section as sequential or selectable subroutines. The following circuits are placed under test by this diagnostic:

1) Flag and Interrupt Circuits (Basic I/O) - TSTØØ
2) Master Reset Circuits - TSTØ1
3) Modem Control and Status Circuits - TSTØ2
4) Arm and Mask Circuits - TSTØ3
*5) Internal Control Circuits - TSTØ4
6) Data Path Circuits - TSTØ5
7) Receive Control Circuits - TSTØ6
8) Transmit Data Circuits - TSTØ7
9) Receive Data Circuits - TST1Ø
10) DMA/DCPC Circuits - TST11

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message to the console device for operator information and then executes the tests according to the options selected on the Switch Register by the operator. The control section mainly checks Switch Register bits 15, 13, and 12.

The program also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if Switch Register bit 10 is clear). The count will be reset only if the program is restarted.

Test sections are executed one after another in each diagnostic pass. User selection or default will determine which test sections will be executed. (Refer to paragraph 2-3.)

2-3. SELECTION OF TESTS BY OPERATOR

The operator has the capability to select his own tests or sequences of tests with the help of bit 9 in the Switch Register. Paragraph 3-4 outlines the test selection.

*Except those unique to receive operations, which are covered in test 6 (TSTØ6).

2-4. MESSAGE REPORTING

There are two types of messages: error and information. Error messages are used to inform the operator when the card fails to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform some operation related to the function of the unit. In this case, an associated halt will occur to allow the operator time to perform the function. The operator must then press RUN. If a console device is used, the printed message will be preceded by an E (error) or H (information) and a number (in octal). The number is also related to the halt code when a console device is not available. Examples of error and information messages are as follows:

Example - Error with halt

Message: E030 FLAG NOT SET BY CLC 0
Halt Code: 102030_8 (T-register or Memory Data register)

Example - Information with halt

Message: H024 PRESS PRESET (EXT & INT), RUN
Halt Code: 102024_8

Example - Information only

Message: H025 BI-O COMP
Halt Code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors. The A-register contains XXXXXX value and the B-register contains the YYYYYY value when an error halt takes place.

Information messages are suppressed by setting Switch Register bit 10.

Operator intervention is suppressed by setting Switch Register bit 8 (i.e., Preset Test in BI-O). When Switch Register bit 12 is set, the tests that are selected will be repeated, all operator intervention will be suppressed.

Excessive reporting of errors E124, E125, E126, E127, E137, E141, E146 and E147 will not take place with Switch Register bit 2 clear. The errors will be reported in full if Switch Register bit 2 is set.

2-5. DIAGNOSTIC LIMITATIONS

2-6. PRIORITY STRING

The capability of the board to receive, pass, and deny priority is not completely checked by this diagnostic. If the board does not receive priority (i.e., PRH from next lower select code) an error E014 NO INT will occur. To check this, remove a board of lower select code and run the Basic I/O Test and the above-mentioned error should occur. Checking the ability of the board to pass or deny priority is beyond the scope of this diagnostic.

2-7. TEST CLOCK

The interface is operated only with the Test Clock (TCLK) which is supplied by the program. This may not totally simulate the real world of Modem-supplied clocks.

Section III

OPERATING PROCEDURE

3-1. LOADING AND CONFIGURING

3-2. LOADING BINARY TAPES

Load Diagnostic Configurator binary object tape. If it is a configured version, proceed with paragraph 3-3; otherwise, configure program according to the Diagnostic Configurator Manual of Diagnostics. Manual No. 02100-90157.

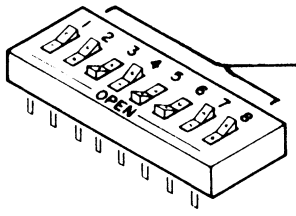
The operator may dump a configured Diagnostic Configurator binary object tape at this point.

Load main diagnostic binary object tape. At this point, a binary tape of the combined configurator and diagnostic may be dumped using the configurator dump routine.

3-3. CONFIGURING THE DIAGNOSTIC

If a preconfigured diagnostic binary tape was loaded, proceed with paragraph 3-4; otherwise, load the P-register with starting address 100_8.

Load the Switch Register with the select code of the card under test. (Bits 0-5 for a single I/O select code.) Load Switch Register bits 6-13 with the SYNC character bit configuration. To determine the SYNC character bit configuration, check the switch settings of SYNC switch assembly U101 on the interface printed-circuit assembly. The switches are numbered 1 through 8 and correspond to SYNC character bits Ø through 7, respectively. An "open" switch is a logic 1 and a "closed" switch is a logic Ø. An all ones SYNC character cannot be used because the idle state of the serial data line is a MARK(1). Press PRESET (INT/EXT) and press RUN. The computer will run and then halt with 102074_8 in the Memory Data register. If halt 102073_8 occurs, the select code input was less than or equal to 7_8; correct the select code and press RUN.



	MSB							LSB
S-REG BIT	13	12	11	10	9	8	7	6
SWITCH NO.	8	7	6	5	4	3	2	1
SYN BYTE BIT NO.	7	6	5	4	3	2	1	0
BINARY BIT VALUE	1	1	0	0	1	0	1	1
SYN BYTE (OCTAL)		3			1		3	

THE SWITCH ILLUSTRATED IS SET FOR A SYN BYTE WITH AN OCTAL CODE OF 313.

At this point the operator may dump to paper tape a copy of the configured program. Refer to the Manual of Diagnostics for the configurator dump routine operation instructions. If this is done, the operator must set the P-register equal to 2000_8 before continuing to the next section.

3-4. RUNNING THE DIAGNOSTIC

If a preconfigured tape was loaded or the dump routine used, set the P-register equal to 2000_8; if not, do not modify the P-Reg.

Make selection of Switch Register options according to table 3-2. Bit 12 is used to loop on the diagnostic if set. Bit 13 is used to loop on a given test that is running at the time. Bit 15, if set, will halt the computer at the completion of a test. After making selection press PRESET (INT/EXT) and press RUN. The program will now execute the diagnostic according to the Switch Register options. At the completion of each pass of the diagnostic the pass count is output to the console for operator information. If Switch Register bit 12 was not selected, the computer will halt with 102077_8 in the Memory Data register. At this point, the A-register contains the pass count. To run another pass, the operator need only press RUN.

3-5. TEST SELECTION BY OPERATOR

The control portion of the program provides for the operator to select his own test or sequence of tests to be run. The operator sets Switch Register bit 9 to indicate that he wants to make a selection. If the computer is halted press RUN. The computer will come to a halt 102075_8 to indicate it is ready for the selection. If the program is running, the test in progress will be completed and then the program will halt. Now the operator loads the A-register with the tests desired. Bit 0 of the A-register represents Test 00, bit 1 represents Test 01, and so on up to bit 9, which represents Test 11. If the operator clears all bits of the A-register, the standard sequence will be run. The operator must then clear Switch Register bit 9 and press RUN. The operator-selected test(s) will then be run.

Table 3-1. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
0	TEST 00
1	TEST 01
2	TEST 02
3	TEST 03
4	TEST 04
5	TEST 05
6	TEST 06
7	TEST 07
8	TEST 10
9	TEST 11
10-15	RESERVED
B-Register	RESERVED

3-6. RESTARTING

The program may be restarted by setting the P-register to 2000_8 and proceeding from paragraph 3-4. To restart and reconfigure, proceed from paragraph 3-3.

If a trap cell halt occurs (106077_8), the user must determine the cause of the interrupt or transfer of control to the location in the M-register. The program may need to be reloaded to continue.

3-7. ADDITIONAL OPERATING INSTRUCTIONS

The diagnostic test hood Part No. 12967-60003 should be placed on the interface 48-pin connector, oriented like the interface cable assembly.

Table 3-2. Switch Register Options

BIT	MEANING IF SET
0	Reserved
1	Reserved
2	All error messages will be reported. If clear excessive error reports are suppressed.
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and halt (102075); the user may specify a new group of tests in the A-register by clearing bit 9 and pressing RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or teletype is not present. Also, those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-register will contain the test number in octal.

Section IV

DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

Figure 4-1 and 4-2 illustrate the command formats, the interface status word and diagnostic status byte. Refer to table 4-2 for additional details on the content of each test.

4-2. BASIC I/O TEST 0 E000-E026

Subtest 1 - Checks the ability to clear, set, and test the interrupt system. The following instruction combinations are tested:

```
CLF 0 - SFC 0
CLF 0 - SFS 0
STF 0 - SFC 0
STF 0 - SFS 0
```

Errors in the above sequences produce error messages E000-E003 as shown in table 4-2.

Subtest 2 - Checks the ability to clear, set, and test the interface card flag. The following instruction combinations are tested:

```
CLF CH - SFC CH
CLF CH - SFS CH
STF CH - SFC CH
STF CH - SFS CH
```

Errors in the above sequences produce error messages E005-E010 as shown in table 4-2.

Subtest 3 - Checks that the test select code does not cause an interrupt with the Flag and Control set on the card and the interrupt system off. The sequence of instructions is shown below:

```
STF 0
STF CH
STC CH
CLF 0
```

The CLF 0 instruction should inhibit an interrupt from occurring. Error message E004 occurs if CLF 0 fails.

Subtest 4 - Checks that the Flag of the card under test is not set when all other select code Flags are set. Error message E011 occurs if a Flag is set incorrectly.

Subtest 5 - Checks the ability of the card to interrupt. With the Flag and Control set and the interrupt system on, there should be an interrupt on the tested channel; if not, error message E014 occurs. Checks that the interrupt occurred where expected. The interrupt should not occur before a string of priority-affecting instructions are executed. The following instructions are used to check the holdoff operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages E012 and E015 will occur if the holdoff fails. Checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message E013 will occur if an interrupt does occur. Checks that no instruction was missed during the interrupt (E026 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the CH Control and Flag set, there is no interrupt following a CLC CH instruction. The following sequence of instructions are used:

```
STC CH
STF CH
STF Ø
CLC CH
```

If the CLC CH fails to inhibit an interrupt, error message E016 will occur.

Subtest 7 - Checks that the CLC 0 instruction inhibits interrupts when the CH Control and Flag are set. The following sequence of instructions is used:

```
CLF CH
STC CH
STF CH
STF 0
CLC 0
```

If the CLC 0 fails to inhibit an interrupt, error message E017 will occur.

Subtest 8 - Checks that the PRESET (EXTERNAL and INTERNAL if applicable) switches on the operator panel performs the following actions:

1. Sets the cards flag (EXTERNAL).
2. Clear the cards control (EXTERNAL).
3. Turns of the interrupt system (INTERNAL).
4. Clears the I/O data lines (EXTERNAL).

4-3. MASTER RESET TEST 1 E030-E033

This test provides additional testing of the I/O portion of the interface. The operation of the CLC 0 instruction and the Master Reset Command is verified.

4-4. MODEM STATUS TEST 2 E034-E043

This test verifies the operation of the three modem control signals (RQS, DTR, and SRQS) and the five modem status line (SRLS, RLS, CLS, RNG, and DSR).

4-5. ARM AND MASK COMMANDS TEST 3 E044-E056

This test verifies the operation of both the Arm and Mask Commands for modem status lines. Included in this test are the Modem Request, check, and status bits.

4-6. INTERNAL CONTROL STATE TEST 4 E057-E117

This test takes advantage of the interfaces self-test feature. The program commands the interface to enter the diagnostic (DIAGN) mode of operation. The following circuits are under test: TSDTA, TRDTA, RQS, DIAGN, RUN, ACTV, HUNT, BYMD, BCOV, DRQ, DERR, and TCLK.

4-7. DATA PATH TEST 5 E120-E126

This test verifies the paths taken by data in the interface. Included in this test are check of the transmit shift register, transmit holding register, and parity generator/checker.

4-8. RECEIVE MODE TEST 6 E127-E135

This test checks those portions of the interface that are unique to the receive operation. Areas under test include: Sync Detect, Hunt mode, Byte mode, Parity Error, Reset Parity Error, and Receive shift register.

4-9. TRANSMIT TEST 7 E136-E137

In this test a sample message is transmitted. The data is accumulated a bit at a time by the program and is verified with the original data.

4-10. RECEIVE TEST 10 E140-E141

In this test a sample message is received. The program outputs the test data a bit at a time. The received data is verified against the original data.

4-11. DMA/DCPC TEST 11 E142-H152

This test performs initial testing on the Service Request circuitry. Then both trans mit and receive operations are performed using the DMA (DCPC). A CHECK condition is created and the channel interrupt is verified. A partial check is made even though DMA is not present in the computer.

4-12. ERROR INFORMATION MESSAGES/HALT CODES

Table 4-1 summarizes the halt codes and table 4-2 provides a complete description of the individual halts.

Table 4-1. Halt Code Summary

HALT	MEANING
TESTS 0_8 to 11_8	
102000-102067	Error (E) & information (H) messages $00\text{-}67_8$.
106000-106056	Error (E) & information (H) messages $100\text{-}156_8$.
CONTROL	
102073	Select code input error.
102074	Select code input complete.
102075	User selection request.
102076	End of test (A = test number).
102077	End of diagnostic run.
106077	Trap cell halts in location $2\text{-}77_8$.

NOTE: See table 4-2 for complete explanation of individual halts.

Table 4-2. Error Information Messages and Halt Codes

HALT CODE	SECTION	MESSAGE	COMMENTS
102073	Configuration	None	I/O select code entered at configuration is invalid. Must be greater than 7_8. Reenter a valid select code and press RUN.
102074	Configuration	None	Select code entered during configuration is valid. Enter program option bits in Switch Register and press RUN.
102075	Test Control	None	Test selection request resulting from Switch Register bit 9 being set. Enter in A register the desired group of tests to be executed and press RUN. (See table 3-1.)
102076	Test Control	None	End-of-test halt resulting from Switch Register bit 15 being set (A-register has the test number). To continue, press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. Switch register options may be changed (A-register has the pass count). To continue press RUN.
106077	Test Control	None	Halt stored in location $2\text{-}77_8$ to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot which interrupted. Diagnostic may be partially destroyed and has to be reloaded if it was caused by a CPU failer; the problem should be corrected before proceeding.
None	Test Control	SYNC COMM INTFC DIAG	Header message. Output at initial start of diagnostic.
None	Test Control	TEXT XX	Information message before error messages (XX = test number). Message occurs only once within a test and is suppressed for any subsequent messages within the same test.
102000	Test 0	E000 CLF0-SFC 0 ERROR	CLF/SFC 0 combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102001	Test 0	E001 CLF SFC 0 ERROR	CLF/SFS 0 combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.

Table 4.2 Error Information Messages and Halt Codes

HALT CODE	SECTION	MESSAGE	COMMENTS
102002	Test 0	E002 STF Ø-SFC Ø ERROR	STF/SFC 0 combination failed. STF did not set Flag or SFC caused skip with Flag set.
102003	Test 0	E003 STF Ø-SFS Ø ERROR	STF/SFS 0 combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102004	Test 0	E004 CLF Ø DID NOT INHIBIT INT	With card Flag and Control set, CLF 0 did not turn off interrupt system.
102005	Test 0	E005 CLC CH-SFC CH ERROR	CLF/SFC CH combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102006	Test 0	E006 CLF CH-SFS CH ERROR	CLF/SFS CH combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.
102007	Test 0	E007 STF CH-SFC CH ERROR	STF/SFC CH combination failed. STF did not set Flag or SFC caused skip with Flag set.
102010	Test 0	E010 STF CH-SFS CH ERROR	STF/SFC CH combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102011	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. A-register contains XX_8, where XX = select code that caused that card Flag to set.
102012	Test 0	E012 INT DURING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURRED	Card interrupted a second time after initial interrupt was processed and interrupt system was turned back on.
102014	Test 0	E014 NO INT	No interrupt occurred with card Flag and Control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not store the correct return address in memory.
102016	Test 0	E016 CLC CH ERROR	CLC CH did not clear interface card Control.
102017	Test 0	E017 CLC Ø ERROR	CLC 0 did not clear interface card Control.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the card Flag.
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear Control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I-O LINES	PRESET (EXT) did not clear I/O data lines. Data lines should be zero.
102024	Test 0	H024 PRESS PRESET (EXT & INT), RUN	Press PRESET (External, Internal) and RUN.
NONE	Test 0	H025 BI-0 COMP	Basic I/O tests completed.
102026	Test 0	E026 INT EXECUTION ERROR	Interrupt was not processed correctly and one or several instructions were processed incorrectly during the interrupt.
102030	Test 1	E030 FLAG NOT SET BY CLC 0	The Flag is reset by the program and then the instruction CLC 0 is executed. The interface Flag should be set.
102031	Test 1	E031 CONTROL NOT RESET BY CLC 0	The Control is set by the program and then the instruction CLC 0 is executed. The interface Control should be reset.
102032	Test 1	E032 FLAG NOT SET BY MRST	The Flag is reset by the program and a Master Reset Command is given. The Flag should be set.
102033	Test 1	E033 CONTROL NOT RESET BY MRST	The Control is set by the program and the Master Reset Command is sent to the interface. The Control is reset by this command.
102034	Test 2	E034 STATUS IS XXXXXX EXP YYYYYY (RQS, CLS)	Using the Control Command to activate then deactivate the Request to Send signal, the program verifies the RQS and CLS circuits. The Clear to Send signal is observed in the status word.
102035	Test 2	E035 STATUS IS XXXXXX EXP YYYYYY (DTR,DSR,RNG)	The Data Terminal Ready signal is activated and deactivated using the Control Command. The program observes the Data Set Ready and Ring bits in the status word.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102036	Test 2	E036 STATUS IS XXXXXX EXP YYYYYY (SRQS, RLS, SRLS)	The Secondary Request to Send signal is activated and deactivated using the Control Command. The program observes the Receive Line Signal and Secondary Receive Line Signal bits in the status word.
102037	Test 2	E037 STATUS NOT RECVD ON 1ST INPUT AFTER CLC CH	A known status response is expected on the first input after a CLC CH instruction has preset the Input Selector to SELS state.
102040	Test 2	E040 STATUS RECVD ON 2ND INPUT AFTER CLC CH	The program is not expecting to receive status on the second input after the CLC CH instruction. The Input Selector should now be in the SELD state.
102041		E041	Reserved.
102042	Test 2	E042 STATUS IS XXXXXX EXP YYYYYY (MRST)	The status is obtained and verified following a Master Reset Command. The modem signals should be zeros.
102043	Test 2	E043 STATUS RECVD AFTER MASTER RESET COMMAND	Following the Master Reset Command a known status response is initialized. The first input should not yield this status because the Input Selector is reset to the SELD state.
102044	Test 3	E044 STATUS IS XXXXXX EXP YYYYYY (RNGI, DSRI)	Modem status lines RNG and DSR are activated. A Mask Command, with the corresponding bits set, is given. The status input should indicate Ring Interrupt or Data Set Ready Interrupt. Also verified are the composites Modem Request (MRQ) and CHECK.
102045	Test 3	E045 STATUS IS XXXXXX EXP YYYYYY (RLSI, SRLSI)	Modem status lines RLS and SRLS are activated. A Mask Command, with the corresponding bits set, is given. The status input should indicate Receive Line Signal Interrupt or Secondary Receive Line Signal Interrupt. Also verified are the composites Modem Request (MRQ) and CHECK.
102046	Test 3	E046 STATUS IS XXXXXX EXP YYYYYY (CLSI)	Modem status line CLS is activated. A Mask Command, with the corresponding bit set, is given. The status input should indicate Clear to Send Interrupt. Also verified are the composites Modem Request (MRQ) and CHECK.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102047	Test 3	E047 STATUS IS XXXXXX EXP YYYYYY (DSRA)	Modem status bit Data Set Ready is activated. The Arm Command is given with the corresponding arming bit equal to zero then one. Then modem status bit DSR is deactivated and the Arm Command testing repeated.
102050	Test 3	E050 STATUS IS XXXXXX EXP YYYYYY (CLSA)	Modem status bit Clear to Send is activated. The Arm Command is given with the corresponding arming bit equal to zero then one. Then modem status bit CLS is deactivated and the Arm Command testing repeated.
102051	Test 3	E051 STATUS IS XXXXXX EXP YYYYYY (RLSA)	Modem status bit Receive Line Signal is activated. The Arm Command is given with the corresponding arming bit equal to zero then one. Then modem status bit RLS is deactivated and the Arm Command testing repeated.
102052	Test 3	E052 STATUS IS XXXXXX EXP YYYYYY (SRLSA)	Modem status bit Secondary Receive Line Signal is activated. The Arm Command is given with the corresponding arming bit equal to zero then one. Then modem status bit SRLS is deactivated and the Arm Command testing repeated.
102053	Test 3	E053 STATUS IS XXXXXX EXP YYYYYY (MASK, MRST)	The Mask is initialized to enable all modem status interrupts. A Master Reset Command follows. Conditions are then established that would otherwise generate a Modem Request that is now prevented by the resetting of the armed bits
102054	Test 3	E054 STATUS IS XXXXXX EXP YYYYYY (ARM, MRST)	The Arm is initialized to all ones. A Master Reset Command (0) follows. Conditions are then established that would otherwise generate a Modem Request that is now prevented by the resetting of the arms.
102055	Test 3	E055 FLAG SET - LOCK INOPERATIVE	A Master Reset Command sets the LOCK. A Modem Request is then generated, which should not allow the Flag to be set.
102056	Test 3	E056 FLAG NOT SET-DEVRQ	A Modem Request results in a Device Request. The LOCK is reset by a CLC CH, which should now allow the Flag to set.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102057	Test 4	E057 DATA IS XXXXXX EXP YYYYYY (TSDTA)	DIAGNostic mode is established by setting bit 3 of a Test command.
102060	Test 4	E060 DATA IS XXXXXX EXP YYYYYY (RQS)	The Request to Send signal is activated.
102061	Test 4	E061 DATA IS XXXXXX EXP YYYYYY (RECVT)	The Receive Test is enabled by a test command with bit 2 = 1.
102062	Test 4	E062 DATA IS XXXXXX EXP YYYYYY (TRDTA)	Test Receive Data along with Receive Test produces Test Serial Data.
102063	Test 4	E063 DATA IS XXXXXX EXP YYYYYY (RUN)	The interface is placed in RUN mode by a START command.
102064	Test 4	E064 DATA IS XXXXXX EXP YYYYYY (RUN, STOP)	The STOP command is given to reset the RUN mode.
102065	Test 4	E065 DATA IS XXXXXX EXP YYYYYY (RUN, MRST)	A Master Reset Command is issued to reset the RUN mode.
102066	Test 4	E066 DATA IS XXXXXX EXP YYYYYY (ACTV)	With the interface in RUN mode the program supplies a test clock. The interface goes to an ACTIVE state.
102067	Test 4	E067 DATA IS XXXXXX EXP YYYYYY (ACTV, STOP)	A STOP command is given to reset the ACTIVE state.
106000	Test 4	E100 DATA IS XXXXXX EXP YYYYYY (HUNT)	With RUN and ACTIVE set and RQS = 0, a Test Clock is supplied by the program to initiate HUNT.
106001	Test 4	E101 DATA IS XXXXXX EXP YYYYYY (HUNT, STOP)	A STOP command is given to reset the HUNT mode.
106002	Test 4	E102 DATA IS XXXXXX EXP YYYYYY (BYMD)	With RUN and ACTIVE set and RQS = 1, a Test Clock is supplied by the program to initiate Byte mode operation.
106003	Test 4	E103 DATA IS XXXXXX EXP YYYYYY (BYMD, STOP)	A STOP command is given to reset the Byte Mode.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
106004	Test 4	E104 DATA IS XXXXXX EXP YYYYYY (BCOV)	Eight clocks are supplied by the program via the Test Clock. The Bit Count Overflow should result.
106005	Test 4	E105 DATA IS XXXXXX EXP YYYYYY (BCOV+1)	One additional clock time past Bit Count Overflow should remove Bit Count Overflow.
106006	Test 4	E106 DATA IS XXXXXX EXP YYYYYY (BCOV+8)	The Bits Count Overflow should occur again after eight clocks.
106007	Test 4	E107 DATA IS XXXXXX EXP YYYYYY (BCOV, STOP)	A STOP command should clear the Bit Count Overflow condition.
106010	Test 4	E110 STATUS IS XXXXXX EXP YYYYYY (DRQ)	With Request to Send, RUN, and ACTIVE high, the Test Clock is presented to the interface to initiate a Data Request.
106011	Test 4	E111 STATUS IS XXXXXX EXP YYYYYY (DRQ, STOP)	A STOP command is given to reset the Data Request.
106012	Test 4	E112 FLAG NOT SET BY DRQ	The Flag was not set by a Data Request.
106013	Test 4	E113 STATUS IS XXXXXX EXP YYYYYY (DRQ, DATA)	An output of data with bit 15 = 0 should reset Data Request.
106014	Test 4	E114 STATUS IS XXXXXX EXP YYYYYY (DRQ, BCOV)	The program supplies additional Test Clocks which should set Data Request.
106015	Test 4	E115 STATUS IS XXXXXX EXP YYYYYY (DRQ, INPUT)	An input instruction is used to reset the Data Request.
106016	Test 4	E116 STATUS IS XXXXXX EXP YYYYYY (DERR)	A data error is generated by obtaining a Data Request and ignoring the request. Additional Test Clocks are supplied, and Data Error set.
106017	Test 4	E117 STATUS IS XXXXXX EXP YYYYYY (DERR, SRSTC)	A Status Reset Command is given to reset the Data Error.
106020	Test 5	E120 DATA IS XXXXXX EXP YYYYYY (MAST)	A Master Reset Command is used to reset the data registers.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
106021	Test 5	E121 DATA IS XXXXXX EXP YYYYYY (SHIFT ONES)	The program supplies Test Clocks to the interface which fills the send shift register with ones.
106022	Test 5	E122 DATA IS XXXXXX EXP YYYYYY (SDOUT)	The ones placed in the send shift register are now presented as send data.
106023	Test 5	E123 DATA IS XXXXXX EXP YYYYYY (SDOUT, MRST)	A Master Reset command resets the send data register.
106024	Test 5	E124 DATA IS XXXXXX EXP YYYYYY (DATA PATH)	Data from the computer is loaded into the transmit holding register and then transferred to the transmit shift register. Test Clocks are supplied by the program. Bit 7 is transferred directly as are the other bits because the parity generator is not enabled.
106025	Test 5	E125 DATA IS XXXXXX EXP YYYYYY (PARITY ODD)	See E126.
106026	Test 5	E126 DATA IS XXXXXX EXP YYYYYY (PARITY EVEN)	Data from the computer is loaded into the transmit holding register. Test Clocks are supplied and the data is loaded into the transmit shift register. The parity bit is generated by the interface and verified by the program.
106027	Test 6	E127 SYND=X DATA=YYY	The receive shift register is loaded with data and the SYNC Detect circuitry is verified by monitoring the SYND bit in the diagnostic status byte. X = SYND bit in diagnostic status byte. YYY = DATA character under test.
106030	Test 6	E130 DATA IS XXXXXX EXP YYYYYY (BYMD, SYND)	A SYNC character is placed in the receive shift register. The Test Clock is activated and the Byte Mode becomes active.
106031	Test 6	E131 DATA IS XXXXXX EXP YYYYYY (BYMD, NOT SYND)	The second character in the receive shift register is not a SYNC. The program provides Test Clocks and the Byte Mode is reset.
106032	Test 6	E132 DATA IS XXXXXX EXP YYYYYY (HUNT, SYND)	The second character in the receive shift register is a SYNC. The program provides Test Clocks and the Hunt mode is reset.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
106033	Test 6	E133 DATA IS XXXXXX EXP YYYYYY (NO PARITY)	A sample three-character message is received. This message consists of two SYNC characters followed by one data character.
106034	Test 6	E134 STATUS IS XXXXXX EXP YYYYYY (PERR)	A sample message containing a parity error is received. The Parity Error status is expected along with CHECK.
106035	Test 6	E135 STATUS IS XXXXXX EXP YYYYYY (RPERR)	A parity error is generated and a Status Reset Command is given to reset the Parity Error condition.
106036	Test 7	E136 STATUS IS XXXXXX EXP YYYYYY (TRANSMIT)	See E137.
106037	Test 7	E137 DATA IS XXXXXX EXP YYYYYY (TRANSMIT)	A sample message is transmitted and verified. This testing is to simulate a typical transmit operation.
106040	Test 10	E140 STATUS IS XXXXXX EXP YYYYYY (RECEIVE)	See E141.
106041	Test 10	E141 DATA IS XXXXXX EXP YYYYYY (RECEIVE)	A sample message is received and verified. This testing is to simulate a typical receive operation.
106042	Test 11	E142 FLAG SET WITH DMA ENABLED (DRQ)	The Control Command for DMA enable is given. The interface is caused to generate a Data Request. The Flag should not get set.
106043	Test 11	E143 FLAG SET BY CHECK WITH (SRQ)	A CHECK condition is created. The interface should not set its Flag because DMA is enabled and a Service Request is present.
106044	Test 11	E144 FLAG NOT SET AFTER CLF CH (SRQ)	The Service Request is reset by a CLF CH. The pending CHECK condition should set the Flag.
106045	Test 11	E145 SRQ SET WHILE LOCK=1	The LOCK is set and a data request is generated to attempt to set SRQ.
106046	Test 11	E146 DATA IS XXXXXX EXP YYYYYY (DMA TRANSMIT)	A data transfer is performed using DMA. The interface is operating in transmit mode.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
106047	Test 11	E147 DATA IS XXXXXX EXP YYYYYY (DMA RECEIVE)	A data transfer is performed using DMA. The interface is operating in receive mode.
106050	Test 11	E150 DMA ABNORMAL COMPLETION	The DMA did not transfer the correct number of characters.
106051	Test 11	E151 STATUS IS XXXXXX EXP YYYYYY (DMA TEST)	An abnormal interface status was detected during the execution of Test 11.
NONE	Test 11	H152 DMA DATA TRANSFER OMITTED - NO DMA	This message is output when test 11 is selected and no DMA is present. Portions of test 11 involving SRQ are executed but no data transfer can take place without DMA.
106053	Tests 7,10,11	E153 MISSING INT. DURING STATUS	Sufficient time was allowed for an interrupt to occur but the interrupt did not take place.
106054	Tests 10,11	E154 INT. WHEN NOT EXPECTED	An interrupt has taken place during SYND or initialization of a receive operation. The A-register contains the current status and the B-register contains the current data.
106055	Test 7	E155 MISSING INT. DURING TRANSMIT	Sufficient time was allowed for an interrupt to occur but the interrupt did not occur.
106056	Test 10	E156 MISSING INT. DURING RECEIVE	Sufficient time was allowed for an interrupt to occur but the interrupt did not take place.

4-13. DICTIONARY OF TERMS

ACTV - Interface Active

BCOV - Bit Counter Overflow
BYMD - Byte Mode

CLS - Clear to Send
CLSA - Clear to Send Arm
CLSI - Clear to Send Interrupt
CLSM - Clear to Send Mask

DERR - Data Error (overflow and underflow)
DIAGN - Diagnose
DMAEN - DMA/DCPC enabled
DRQ - Data Request
DSR - Data Set Ready
DSRA - Data Set Ready Arm
DSRI - Data Set Ready Interrupt
DSRM - Data Set Ready Mask
DTR - Data Terminal Ready

MASK - Interrupt Mask
MRQ - Modem Request
MRST - Master Reset Command (0)

PEN - Parity enabled
PERR - Parity Error
PSNS - Parity Sense

RDATA - Receive Data
RDERR - Reset Data Error
RECVT - Receive Test Mode
RLS - Receive Line Signal
RLSA - Receive Line Signal Arm
RLSI - Receive Line Signal Interrupt
RLSM - Receive Line Signal Mask
RNG - Ring
RNGI - Ring Interrupt
RNGM - Ring Mask
RPERR - Reset Parity Error
RQS - Request to Send

SDOUT - Send Data Output
SELD - Select Data
SRLS - Secondary Receive Line Signal
SRLSM - Secondary Receive Line Signal Mask
SRLSA - Secondary Receive Line Signal Arm
SRLSI - Secondary Receive Line Signal Interrupt
SRQ - Service Request (DMA)
SRQS - Secondary Request to Send
SRSTC - Status Reset Command (1)
SYND - Sync Detect

TCLK - Test Clcok
TRDTA - Test Receive Data

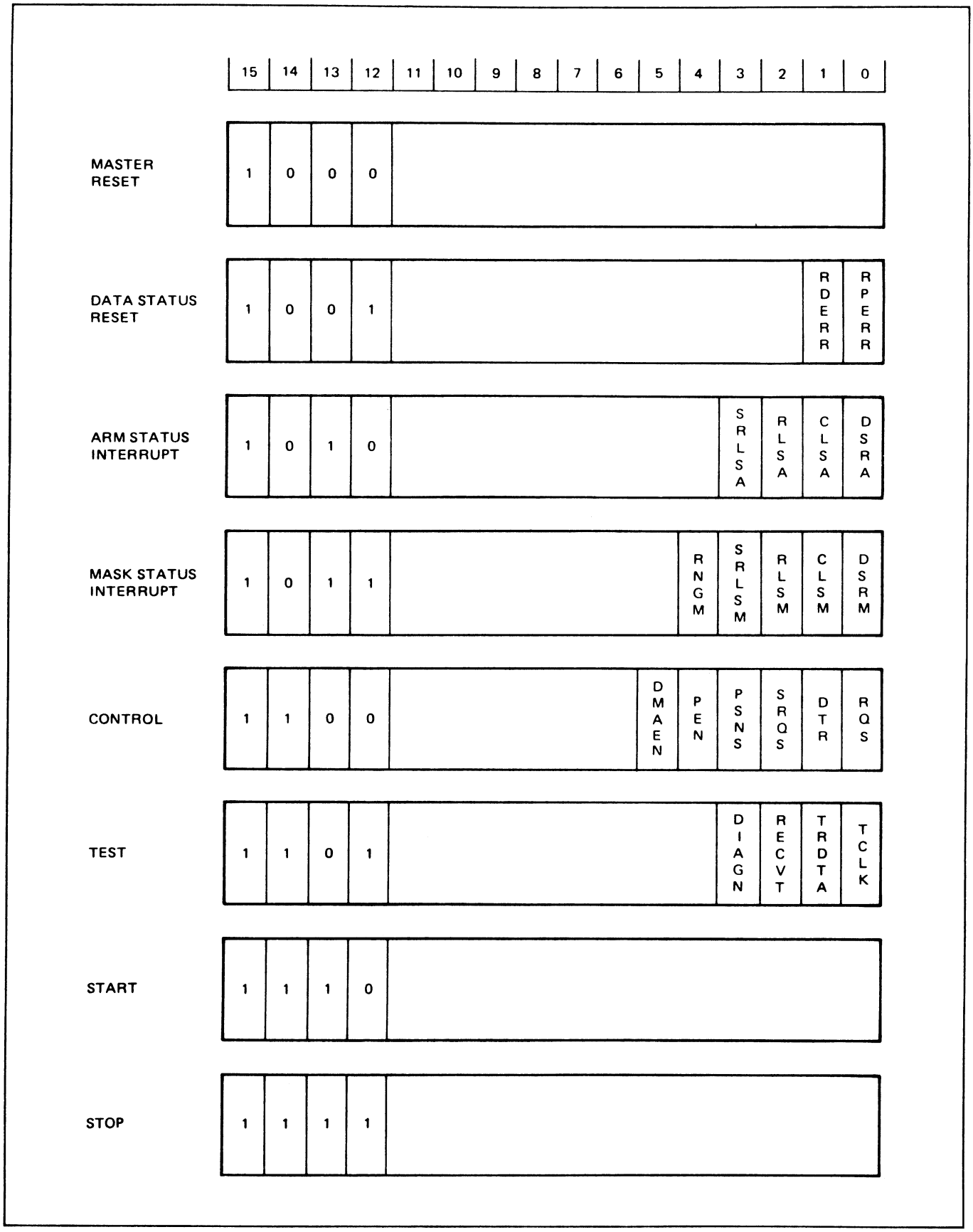
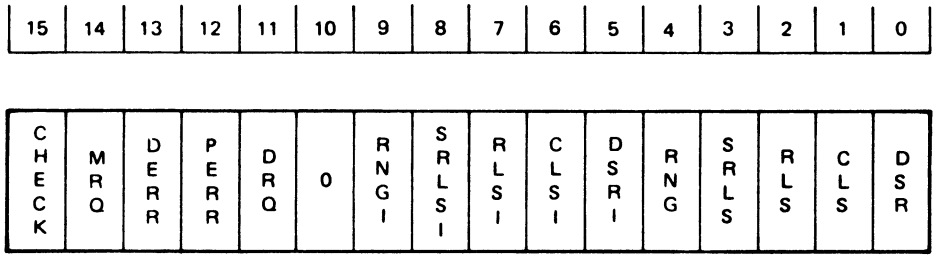
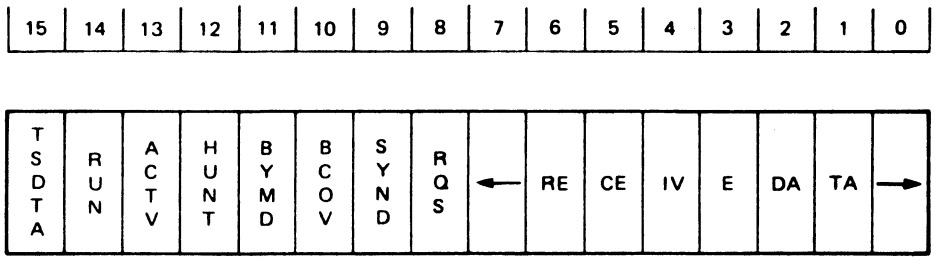


Figure 4-1. Command Formats



INTERFACE STATUS WORD



DIAGNOSTIC STATUS BYTE

Figure 4-2. Interface Status Word and Diagnostic Status Byte