HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

12557A

CARTRIDGE DISC INTERFACE KIT

(FOR 2114, 2115, AND 2116 COMPUTERS)

Card Assemblies

12557-60002, Rev. 1013
12557-60003, Rev. 1013

Note

This manual should be retained with Volume Three of the Hewlett-Packard computer documentation.

12557-90001

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GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the HP 12557A Cartridge Disc Interface Kit.

Note

Since this manual will be used with other manuals for the cartridge disc system, the term "Device Command" used in this manual is synonymous with the term "Encode" used in the other manuals.

1-3. GENERAL DESCRIPTION.

1-4. The HP 12557A Cartridge Disc Interface Kit (figure 1-1) interfaces the Hewlett-Packard 2114, 2115, and 2116 Computers with DMA capability to the HP 2871A Cartridge Disc Controller. If the Disc Operating System (DOS) software is used, the computer also must have central interrupt capability. Two interface cards and a cable are contained in the kit. The cable connects the interface cards to the disc controller. The two interface cards are electronically identical except for the positions of the jumper wires on each card. The signal outputs to the disc controller are inverted from positive-true/ground-false logic to ground-true/positive-false logic to make the signals compatible with the disc controller logic.

1-5. One interface card, used as the data channel, transfers data, status, and addressing information. The other interface card, used as the command channel, transfers commands and drive selection signals. Commands, addressing, and status words are transferred under program control; data words are transferred under direct memory access (DMA) control.

1-6. KIT CONTENTS.

1-7. The HP 12557A Cartridge Disc Interface Kit contains the following:

a. Data Channel Card, part no. 12557-60002.
b. Command Channel Card, part no. 12557-60003.
c. Cable Assembly, part no. 12557-60006.

Note

Early versions of the interface kit contained an unshielded Cable Assembly, part no. 12557-60001. When reordering specify the shielded Cable Assembly, part no. 12557-60006.

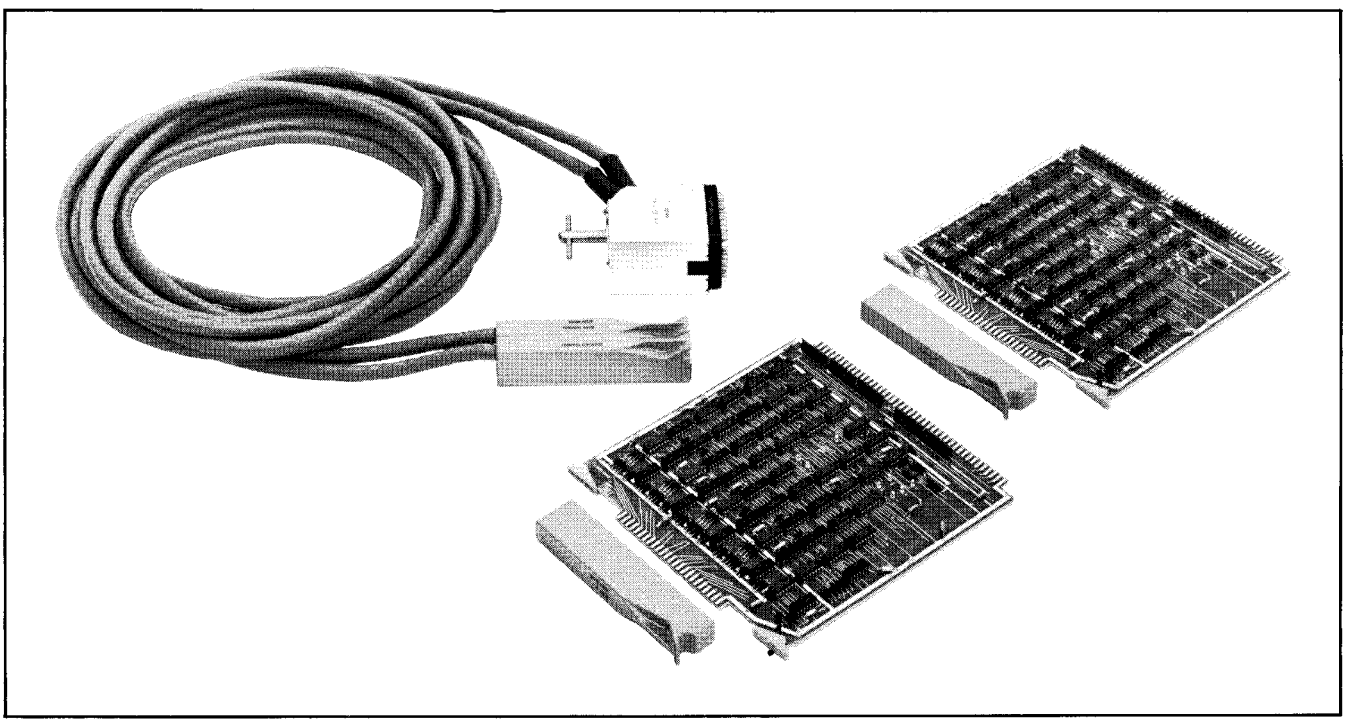

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Figure 1-1. HP 12557A Cartridge Disc Interface Kit

d. 48-Pin Test Connector, part no. 12849-60003.
e. 48-Pin Test Connector, part no. 12849-60004.
f. Operating and Service Manual, part no. 12557-90001.

1-8. IDENTIFICATION.

1-9. Printed-circuit card revisions are identified by a letter, a date code, and a division code stamped on the board (e.g. A-1005-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The data code (four middle digits) refers to the electrical characteristics of the loaded board. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the board. If the date codes stamped on the printed-circuit boards do not agree with the date codes shown on the title page of this manual, there are differences between your boards and the boards described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-10. SPECIFICATIONS.

1-11. Specifications for the data channel card and the command channel card are given in table 1-1.

Table 1-1. Interface Kit Specifications

POWER REQUIREMENTS		VOLTAGE	CURRENT
		-2V dc +4.5V dc	0.17 amperes 3.5 amperes
SIGNAL REQUIREMENTS		**"0" LEVEL**	**"1" LEVEL**
DATA AND FLAG INPUTS	Voltage	+2.4 to +5V dc ①	0 to +0.5V dc
	Open Circuit Voltage and Impedance	+3V dc, Z_{in} = 122 ohms	
	Current Required	–	0.025 amperes
	Minimum Pulse Width	300 nanoseconds	
DATA AND COMMAND OUTPUTS	Voltage	+2.4 to +5V dc ②	0 to +0.5V dc
	Impedance	1K (to +5V dc)	–
	Current Sink (maximum)	–	0.031 amperes

NOTES: ① Or open circuit capable of withstanding +5V dc.
② +5V dc maximum; impedance determined by external circuit.
3 Maximum interface cable length is 15 feet.

SECTION II
INSTALLATION AND PROGRAMMING

2-1. INTRODUCTION.

2-2. This section provides information on unpacking, inspection, installation, and programming for the HP 12557A Cartridge Disc Interface Kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping container is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for contents and damage (cracks in circuit card, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. JUMPER WIRES.

2-7. Table 2-1 lists the jumper wires and their appropriate positions for each interface card. Inspect each card and verify that the jumper wires are in the required positions. See the parts location diagrams in figures 4-1 and 4-2 to determine the physical location of the jumpers.

Table 2-1. Interface Card Jumper Wire Positions

JUMPER WIRE	POSITION	
	COMMAND CHANNEL	DATA CHANNEL
W1	A	A
W2	B	B
W3	B	B
W4	B	B
W5	Out	In
W6 thru W8	In	In
W9	A	B
W10	A	A

2-8. CARD INSTALLATION.

CAUTION

Make certain that power is off at the computer and at the disc controller before installing the interface kit, or damage to the computer or disc controller may result.

2-9. Install the interface cards and the interconnecting cable as follows:

a. Turn computer power and disc controller power off. Open the computer for access to the I/O card slots.

b. Plug the interface cards into the I/O card slots assigned for the particular computer system. (Ensure that the data channel interface card is in the higher priority position.)

c. Pass the interface card connectors of the cable assembly (part no. 12557-60006) through the opening at the rear of the computer. Slide the connectors onto the corresponding cards and close the computer.

d. Pass the disc controller connector of the cable assembly through the opening below the rear door of the disc controller cabinet. Secure the connector to the disc controller by turning the screw handle at the rear of the connector. Remove one of the screws that secure the disc controller power supply cage to the back plate. Secure the ground lug of the cable assembly to the back plate with this screw. If the power supply is not available secure the ground lug to the rack frame.

2-10. Table 2-2 contains a list of cable assembly pin assignments for both interface card connectors and the disc controller connector. The cable assembly contains 72 twisted-pair conductors. Each twisted pair consists of a signal conductor and a signal-ground conductor. The entries in table 2-2 are organized with the signal conductor of a twisted pair listed first and the corresponding signal-ground conductor immediately following. The table also provides a cross-reference of signal names between the disc controller and the interface cards. The minus signs (-) in the SIGNAL NAME column for the disc controller indicate ground-true, positive-false signal levels. The plus (+) sign indicates positive-true, ground-false signal levels.

2-11. PROGRAMMING.

2-12. The following programming information includes disc drive unit characteristics, addressing information, an explanation of command words and format, content of the disc status word, data transfer timing considerations, sample programs, and programming recommendations.

Table 2-2. Interconnecting-Cable Connector-Pin Functions

DISC CONTROLLER CONNECTOR PIN	DATA CHANNEL CARD CONNECTOR PIN	COMMAND CHANNEL CARD CONNECTOR PIN	SIGNAL NAME	
			INTERFACE CARD	DISC CONTROLLER
M8 P3	A BB		Bit 0 Sig Gnd	-Output Data Bit 0
C1 D5	B BB		Bit 1 Sig Gnd	-Output Data Bit 1
K1 K9	C BB		Bit 2 Sig Gnd	-Output Data Bit 2
B5 C9	D BB		Bit 3 Sig Gnd	-Output Data Bit 3
M1 N5	E BB		Bit 4 Sig Gnd	-Output Data Bit 4
B3 C7	F BB		Bit 5 Sig Gnd	-Output Data Bit 5
K4 L5	H BB		Bit 6 Sig Gnd	-Output Data Bit 6
A7 C2	J BB		Bit 7 Sig Gnd	-Output Data Bit 7
M7 P2	K BB		Bit 8 Sig Gnd	-Output Data Bit 8
B9 D4	L BB		Bit 9 Sig Gnd	-Output Data Bit 9
J9 K8	M BB		Bit 10 Sig Gnd	-Output Data Bit 10
B4 C8	N BB		Bit 11 Sig Gnd	-Output Data Bit 11
L9 N4	P BB		Bit 12 Sig Gnd	-Output Data Bit 12
B2 C6	R BB		Bit 13 Sig Gnd	-Output Data Bit 13
J8 K7	S BB		Bit 14 Sig Gnd	-Output Data Bit 14
A2 A5	T BB		Bit 15 Sig Gnd	-Output Data Bit 15
K5 L6	U BB		Flag Sig Gnd	(Not Used)
E3 F7	X BB		Control Sig Gnd	(Not Used)
M6 P1	1 BB		Bit 0 Sig Gnd	-Read Bus 15/-Any Error Status
B8 D3	2 BB		Bit 1 Sig Gnd	-Read Bus 14/-Data Error Status

Table 2-2. Interconnecting-Cable Connector-Pin Functions (Continued)

DISC CONTROLLER CONNECTOR PIN	DATA CHANNEL CARD CONNECTOR PIN	COMMAND CHANNEL CARD CONNECTOR PIN	SIGNAL NAME	
			INTERFACE CARD	DISC CONTROLLER
K3 L2	3 BB		Bit 2 Sig Gnd	-Read Bus 13/-Drive Busy Status
A3 A6	4 BB		Bit 3 Sig Gnd	-Read Bus 12/-Flagged Track Status
L8 N3	5 BB		Bit 4 Sig Gnd	-Read Bus 11/-Address Error Status
B1 C5	6 BB		Bit 5 Sig Gnd	-Read Bus 10/-End of Cylinder
J7 K6	7 BB		Bit 6 Sig Gnd	-Read Bus 9/-Not Ready
A1 A4	8 BB		Bit 7 Sig Gnd	-Read Bus 8
D7 F2	9 BB		Bit 8 Sig Gnd	-Read Bus 7/-Seek Check
H2 J3	10 BB		Bit 9 Sig Gnd	-Read Bus 6/-Seek Incomplete
E4 F8	11 BB		Bit 10 Sig Gnd	-Read Bus 5/-Access Hunting
E9 G9	12 BB		Bit 11 Sig Gnd	-Read Bus 4/-Access Unsafe
B7 D2	13 BB		Bit 12 Sig Gnd	-Read Bus 3/-Read-Write Unsafe
E2 F6	14 BB		Bit 13 Sig Gnd	-Read Bus 2/-Overrun
D6 F1	15 BB		Bit 14 Sig Gnd	-Read Bus 1/-First Seek
E8 G3	16 BB		Bit 15 Sig Gnd	-Read Bus 0/-Attention
A8 C3	22 BB		Device Command Sig Gnd	-Data Encode
T9 V1	23 BB		Device Flag Sig Gnd	-Data Flag
H1 J2		A 24	Bit 0 Sig Gnd	-Control Bit 0
T7 T8		B 24	Bit 1 Sig Gnd	-Control Bit 1
V3 V2		C 24	Bit 2 Sig Gnd	(Not Used)
E1 F5		D 24	Bit 3 Sig Gnd	(Not Used)

Table 2-2. Interconnecting-Cable Connector-Pin Functions (Continued)

DISC CONTROLLER CONNECTOR PIN	DATA CHANNEL CARD CONNECTOR PIN	COMMAND CHANNEL CARD CONNECTOR PIN	SIGNAL NAME	
			INTERFACE CARD	DISC CONTROLLER
R6 T1		E 24	Bit 4 Sig Gnd	(Not Used)
K2 L1		F 24	Bit 5 Sig Gnd	(Not Used)
H3 J4		H 24	Bit 6 Sig Gnd	(Not Used)
P8 S3		J 24	Bit 7 Sig Gnd	(Not Used)
H6 J5		K 24	Bit 8 Sig Gnd	-Control Bit 8
R5 S9		L 24	Bit 9 Sig Gnd	-Control Bit 9
G8 H5		M 24	Bit 10 Sig Gnd	(Not Used)
T5 T6		N 24	Bit 11 Sig Gnd	(Not Used)
G5 H8		P 24	Bit 12 Sig Gnd	-Control Bit 12
P6 S1		R 24	Bit 13 Sig Gnd	-Control Bit 13
D9 F4		S 24	Bit 14 Sig Gnd	-Control Bit 14
R8 T3		T 24	Bit 15 Sig Gnd	-Control Bit 15
R3 S7		W 24	Power On Normal Sig Gnd	+Power On
G7 H4		1 24	Bit 0 Sig Gnd	-Cmd Chnl Input 0
R9 T4		2 24	Bit 1 Sig Gnd	-Cmd Chnl Input 1
G6 H9		3 24	Bit 2 Sig Gnd	-Cmd Chnl Input 2
R4 S8		4 24	Bit 3 Sig Gnd	-Cmd Chnl Input 3
R2 S6		5 24	Bit 4 Sig Gnd	(Not Used)
M9 P4		6 24	Bit 5 Sig Gnd	(Not Used)
M4 N8		7 24	Bit 6 Sig Gnd	(Not Used)

Table 2-2. Interconnecting-Cable Connector-Pin Functions (Continued)

DISC CONTROLLER CONNECTOR PIN	DATA CHANNEL CARD CONNECTOR PIN	COMMAND CHANNEL CARD CONNECTOR PIN	SIGNAL NAME	
			INTERFACE CARD	DISC CONTROLLER
B6		8	Bit 7	(Not Used)
D1		24	Sig Gnd	
M2		9	Bit 8	(Not Used)
N6		24	Sig Gnd	
E5		10	Bit 9	(Not Used)
F9		24	Sig Gnd	
V6		11	Bit 10	(Not Used)
V7		24	Sig Gnd	
R7		12	Bit 11	(Not Used)
T2		24	Sig Gnd	
V5		13	Bit 12	(Not Used)
V4		24	Sig Gnd	
R1		14	Bit 13	(Not Used)
S5		24	Sig Gnd	
P9		15	Bit 14	(Not Used)
S4		24	Sig Gnd	
G9		16	Bit 15	(Not Used)
J1		24	Sig Gnd	
E6		19	POPIO(B)	-POPIO
G1		24	Sig Gnd	
D8		22	Device Command	-Command Encode
F3		24	Sig Gnd	
H7		23	Device Flag	-Command Flag
J6		24	Sig Gnd	

2-13. DISC DRIVE UNIT CHARACTERISTICS.

2-14. The disc drive unit contains two discs (one removable and one fixed) and four read/write heads (one for each disc surface). There are 203 cylinders available for information storage. The cylinder address numbers range from zero to 202. Each cylinder consists of four tracks, one on each disc surface. Also, each track is divided into 12 sectors. Within a cylinder, sectors are addressed by specifying a read/write head number and a sector number. The head numbers range from zero to three (head zero serves the top surface of the removable disc, head three serves the bottom surface of the fixed disc, etc.). Sector numbers range from zero to eleven.

2-15. The smallest addressable data storage area in the disc drive unit is a sector. Addressing is accomplished by specifying the cylinder number (0 to 202), read/write head number (0 to 3), and sector number (0 to 11). More information on addressing is contained in paragraph 2-30.

2-16. Each sector contains a sector address field and a data field. The sector address field contains the cylinder, head, and sector numbers of the sector, as well as indicators for defective and protected cylinder. The data field stores 128 16-bit words of data. Only the data field is transferred to and from the computer; the sector address field is generated and checked in the disc controller. Both fields are cyclic checked by the disc controller.

2-17. The disc system may contain up to four disc drive units, and the disc drive units are numbered from zero to three for addressing commands to a particular disc drive unit. Also, the four least significant bits from the command channel card to the computer are used to indicate the state of attention for each disc drive unit. The state of attention means whether or not a disc drive unit has finished executing a command and is ready to accept another command. Attention for disc drive unit zero is bit 0; attention for disc drive unit one is bit 1, etc. If the corresponding bit is false, either the disc drive unit is busy or the

last operation performed on the unit was a status check; if the bit is true, the disc drive unit is ready. Use of the disc drive unit numbers and the attention bits is explained further at various points in the remainder of this section.

2-18. CHANNEL ADDRESSES.

2-19. The disc system has a data channel and a command channel, each of which can be addressed by the computer program. The data channel is associated with the data channel card and is addressed by using the I/O select code for that card. The command channel is associated with the command channel card and is addressed by using the I/O select code for the command channel interface card.

2-20. COMMAND CHANNEL I/O SELECT CODE. The command channel I/O select code can be used with OTA/B, LIA/B, MIA/B, STF, CLF, STC, CLC, SFS, and SFC instructions. The OTA/B instruction sends a command word to the disc controller which specifies the operation to be performed. An LIA/B or MIA/B instruction transfers the attention bits to the computer. A STF instruction can be used to force an interrupt to a service subroutine for transferring data, checking status of a drive, or analyzing attention bits. The STC and CLF instructions are usually used together to initiate the operation specified in the command word and to ensure that the command channel Flag FF is cleared. The SFS and SFC instructions are used to check command completion (if the Flag FF is set, the command has been executed).

2-21. DATA CHANNEL I/O SELECT CODE. The data channel I/O select code can be used with OTA/B, LIA/B, MIA/B, CLF, STC, CLC, SFS, and SFC instructions. An OTA/B instruction is used to transfer cylinder and head/sector numbers for specifying the location for reading and writing data. The OTA/B instruction also transfers sector count words which are used in data recoverability checks. Either an LIA/B or MIA/B instruction can be used for transferring the disc status word to the computer. The STC and CLF instructions are used together to cause the disc controller to accept the cylinder, head/sector, or sector count number and to ensure that the data channel Flag FF is cleared. The CLC instruction may be used to prevent an interrupt, if the interrupt system is enabled, during cylinder, head/sector, and sector count word transfers. The SFS and SFC instructions are used to check if a word transferred over the data channel by the computer program has been accepted by the disc controller, or if a word has been issued by the disc controller. (If a word has been accepted, or issued, the Flag FF is set.)

2-22. COMMAND WORDS.

2-23. To initiate a disc operation, the computer places a command word in the output register of the command channel card and issues an STC instruction. The disc controller decodes the command word and initiates the operation specified on the drive selected. When the command issued is Status Check, Seek Record, or Address Record, the disc controller will be free to accept another command as soon as the required data information transfer through the data channel has been completed. For all other commands, the command word must remain unchanged on the command channel card until the disc controller sets the Flag FF on the command channel card.

2-24. The command word consists of four bits of command information and two bits of drive select information. The format is shown in figure 2-1. The Initialize Data command requires other information bits in the command word; these are described in paragraph 2-36. The two-bit drive select field contains the number (0 through 3) of the disc drive unit which is to execute the command. (The disc controller has the capability to control up to four disc drive units.) The four-bit command field contains the binary code of the command to be executed. The command codes are shown in table 2-3. An explanation of each command word is discussed in the following paragraphs.

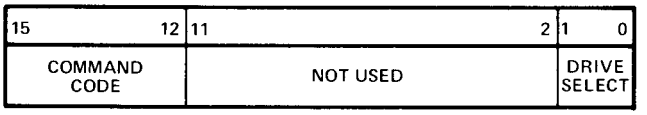

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Figure 2-1. Command Word Format

Table 2-3. Command Codes

CODE BITS 15	14	13	12	COMMAND
0	0	0	0	Status Check
0	0	0	1	Write Data
0	0	1	0	Read Data
0	0	1	1	Seek Record
0	1	0	1	Refine Sector
0	1	1	0	Check Data
1	0	0	1	Initialize Data
1	0	1	1	Address Record

2-25. STATUS CHECK. The Status Check command is used to transfer a word of status information from the disc controller to the computer. When the command is issued, the disc controller selects the disc drive unit specified, assembles the status word, and transfers the word to the computer via the data channel interface card. The word details status of the selected disc drive unit as well as conditions detected by the disc controller during data operations with the disc drive unit. Status word bit definitions are given in paragraph 2-42. Command execution is completed when the disc controller sends the status word to the data channel card and sets the Flag FF on the data channel card. The Flag FF is not set on the command channel card.

2-26. WRITE DATA. Write Data is the normal command used for writing after the disc has been initialized. When the command is issued, the disc controller selects the disc drive unit specified and waits for the addressed sector to come into position. In all cases, the addressed sector is that sector specified by the contents of the disc controller record address register (RAR). When the addressed sector comes into position, the disc controller examines the cylinder condition indicators and address information in the address field, and then cyclic checks the entire sector. If the address compares properly and the cylinder is not protected or defective, the disc controller starts writing in the next sector. The controller assembles and writes the address field, then initiates data transfer from the data channel card. The controller always writes 128 data words in a sector; if the computer sends less than 128 words, the controller fills the remainder of the sector with "0's" before setting the Flag FF on the command channel card. If the computer has more than 128 words to write, the controller adds one to the contents of the record address register and continues writing in the next sector. The maximum number of words that can be written before a new head positioning command is required is 3,072. The maximum number can be written only if the writing starts at sector zero, head zero, or at sector zero, head two of a particular cylinder. In other words, the disc controller will write data in a maximum of 24 sectors before a new Seek Record command or Address Record command is required. Data transfer is suspended as the controller assembles and writes the sector address field. The address information is taken from the record address register; the cylinder indicator information is written as it was read from the first sector. Data transfer resumes with the first data word of the sector. Writing continues until the computer has no more data to transfer, or the controller detects an End of Cylinder signal or other error condition. In either case, the Flag FF is set on the command channel card to signal completion.

2-27. If, during the address checking phase of the command, the address does not compare with the contents of the record address register, the defective cylinder indicator (DCI) is on, or the protected cylinder indicator (PCI) is on with the OVERRIDE switch off, the Flag FF is set on the command channel card and no writing or data transfer occurs. A Status Check command will receive status detailing the cause for termination.

2-28. READ DATA. Read Data is the normal command used for reading. When the command is issued, the disc controller adds one to the contents of the record address register, selects the disc drive unit specified, and waits for the addressed sector to come into position. With the sector in position, the controller examines the flag and address information in the address field and then initiates data transfer to the data channel card. The controller always reads 128 data words from the data field of the sector. If the computer accepts less than 128 words, the controller continues to the end of the sector to complete the cyclic check before signaling completion by setting the Flag FF on the command channel card. If the computer tries to accept more than 128 data words, the controller adds one to the contents of the record address register and continues reading in the next sector. The maximum number of words that can be read before a new head positioning command is required is 3,072. The maximum number can be read only if the reading starts at sector zero, head zero, or at sector zero, head two of a particular cylinder. In other words, the disc controller will read data in a maximum of 24 sectors before a new Seek Record command or Address Record command is required. Data transfer is suspended while the controller examines the address field; data transfer resumes with the first data word of the sector. Reading continues until the computer stops accepting data or the controller detects an End of Cylinder signal or other error condition. In either case, the Flag FF is set on the command channel card to signal completion.

2-29. If the address written in the sector address field does not compare with the contents of the record address register or if the defective cylinder indicator is on during examination of the sector address field, the read operation continues normally to the end of the current sector. At this point, the disc controller halts data transfer and sets the Flag FF on the command channel card. A Status Check command to the disc drive unit being read will produce status information detailing the cause for early termination. If the protected cylinder indicator is encountered, the Read Data operation proceeds normally. Issuing a Status Check command after the Read Data operation is complete will indicate the presence of protected cylinder indicator.

2-30. SEEK RECORD. Seek Record is the command used to initiate a head positioning operation in the disc drive unit. A Seek Record command must precede a Read command or Write command. When the command is issued, the disc controller selects the disc drive unit specified and accepts two words of address information from the data channel card. The first word contains the cylinder number to which the head is to move; the second word contains the head/sector number. (See figure 2-2 for word formats.)

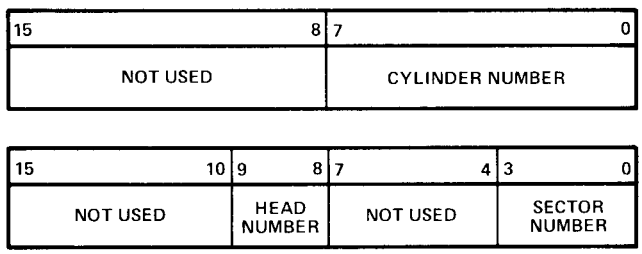


Figure 2-2. Address Word Formats

2-31. As the disc controller accepts each of these words it assembles a new record address in the record address register (previous contents of the register are lost), transfers cylinder and head/sector numbers to the selected disc drive unit, and initiates the head positioning operation in the disc drive unit. The Flag FF on the command channel card is not set until the head positioning operation is complete and the addressed sector is 3.3 milliseconds away from the

read/write head. However, the disc controller is free to perform other operations as soon as the second word of address information has been accepted. Average Seek Record execution time is 35 milliseconds.

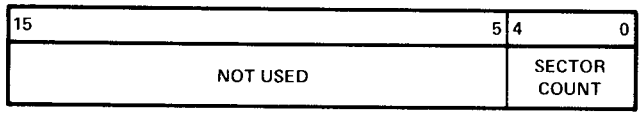
2-32. If the selected disc drive unit has a head positioning operation already in progress when Seek Record command is issued, the disc controller will accept the new command and address words normally, but the new head positioning operation will not be initiated. The seek-check error condition is set in the disc drive unit.

2-33. If the command addresses a cylinder number greater than 202, or the heads are already positioned at the addressed cylinder, the disc controller accepts the Seek Record command and address words normally, but no head positioning operation is initiated in the selected disc drive unit. In the case of a cylinder address greater than 202, the seek-check error condition is also set in the disc drive unit.

2-34. To make maximum use of computer time when two to four disc drive units are used in the disc system, two or more Seek Record commands may be issued before issuing the command to read or write data on a particular disc drive unit. When the Device Flag signal from the disc controller sets the Flag FF on the command channel card, the attention bits must be examined to determine which disc drive unit set the Flag FF and is ready for data transfer. The attention bit corresponding to a particular disc drive unit is true for 2.8 milliseconds when the Device Flag signal is issued. The period of the attention bits is 40 milliseconds. A method for issuing multiple Seek Record commands and examining the attention bits is given in table 2-4. If another command is issued to a disc drive unit (write, read, etc.), the Device Flag signal from any other disc drive unit is inhibited until the command has been executed.

2-35. REFINE SECTOR. Refine Sector is a special recovery command that the disc controller performs on a sector to improve the characteristics of the data. The command should be used only after re-try procedures have failed to recover data. (Error recovery procedures are given in paragraph 2-60.) When the command is issued, the disc controller adds one to the contents of the record address register, selects the disc drive unit specified, and waits for the addressed sector to come into position. When the addressed sector is reached, a tunnel erase is performed on the sector in an attempt to improve the signal-to-noise ratio. (The tunnel erase operation is described in the disc drive unit manual.) No communications occur on the data channel card; the Flag FF is set on the command channel card when the end of the addressed sector is reached. The command operates on one sector at a time; no check is made for address comparison, defective cylinder indicator, or protected cylinder indicator.

2-36. CHECK DATA. The Check Data command performs a cyclic check of file data to verify recoverability of the data. (A Seek Record command must precede the Check Data command to specify the starting address.) The disc controller executes the command in the same manner as the Read Data command; however, no transfer of file data occurs between the computer and the disc controller. When the command is issued, the disc controller accepts a single word of count information from the data channel card. The word contains the positive count of sectors to be checked in the format shown in figure 2-3. The maximum number of sectors that can be checked before a new Seek Record command or Address Record command is required is 24.



2090-15

Figure 2-3. Sector Count Word Format

2-37. The controller adds one to the contents of the record address register, selects the disc drive unit specified, and waits for the addressed sector to come into position. With the sector in position, the disc controller examines the cylinder indicators and address information and cyclic checks the entire sector. The disc controller subtracts one from the sector count. If the count is not zero, the checking operation is repeated in the next sector. This process continues until the sector count reaches zero or the disc controller detects an End of Cylinder signal or other error condition. At this point, the Flag FF is set on the command channel card to signal completion.

2-38. If the address written in the sector address field does not compare with the contents of the record address register or the defective cylinder indicator is on during examination of the sector address field, the disc controller halts the checking operation at the end of the current sector and sets the Flag FF on the command channel card. A Status Check command to the disc drive unit in operation will detail the cause for early termination. If the protected cylinder indicator is encountered, the Check Data operation proceeds normally. Issuing a Status Check command after the Check Data operation is complete will indicate the presence of a protected cylinder indicator.

2-39. INITIALIZE DATA. Initialize Data is the command used to initialize unwritten tracks and to generate the defective cylinder indicator or protected cylinder indicator. (A Seek Record command must precede the Initialize Data command to specify the starting address.) This command is accepted only when the OVERRIDE switch on the disc controller is set to ON. If the OVERRIDE switch is set to OFF, the command channel card Flag FF is set and the disc controller makes no attempt to execute the command. The disc controller executes the command in the same manner as the Write Data Command, except that the controller does not check the first sector for address and cylinder indicator information. When the command is issued, the disc controller adds one to the contents of the record address register, selects the disc drive unit specified, and waits for the addressed sector to come into position. With the sector in position, the disc controller assembles and

Table 2-4. Multiple Seek Record Operations

LABEL	OPCODE	OPERAND	COMMENTS
	CLA		
	STA	VAR 1	Provide locations in memory for temporary storage of variables. Store all zeros in each location.
	STA	UNIT	
	LDA	CYL 1	Load cylinder number for disc drive unit 0 into A-register.
	STA	CYL	Store cylinder number in memory.
	LDA	HDST 1	Load head/sector number for disc drive unit 0 into A-register.
	STA	HDSCT	Store head/sector number in memory.
	JSB	SEEK	Perform Seek Record operation on disc drive unit 0.
	ISZ	UNIT	Increment the memory location used for disc drive unit number. Now specifies disc drive unit 1.
	LDA	CYL 2	Load cylinder number for disc drive unit 1 into A-register.
	STA	CYL	Store cylinder number in memory.
	LDA	HDST 2	Load head/sector number for disc drive unit 1 into register.
	STA	HDSCT	Store head/sector number in memory.
	JSB	SEEK	Perform Seek Record operation on disc drive unit 1.
	ISZ	UNIT	Increment the memory location used for disc drive unit number. Now specifies disc drive unit 2.
	LDA	CYL 3	Load cylinder number for disc drive unit 2 into A-register.
	STA	CYL	Store cylinder number in memory.
	LDA	HDST 3	Load head/sector number for disc drive unit 2 into A-register.
	STA	HDSCT	Store head/sector number in memory.
	JSB	SEEK	Perform Seek Record operation on disc drive unit 2.
SS3	SFS	CC	Has any disc drive unit completed Seek Record operation?
	JMP	*-1	No, wait.
	LIA	CC	Yes, load attention bits into A-register.
	CLB		Clear B-register.

Table 2-4. Multiple Seek Record Operations (Continued)

LABEL	OPCODE	OPERAND	COMMENTS
SS1	SLA		Did disc drive unit 0, 1, or 2 complete Seek Record operation? (First pass examines drive 0, second pass examines drive 1 etc.)
	JMP	SS2	Yes, perform operation assigned to disc drive unit.
	INB		Increment unit number.
	RAR		Position next attention bit.
	CPB	D4	Have all attention bits been examined?
	RSS		Yes, skip next instruction.
	JMP	SS1	No, Loop again.
	LDA	STAT	Load Status Check command into A-register.
	IOR	UNIT	Place last used disc drive unit number into A-register along with Status Check command.
	STC	DC,C	Output Device Command signal to disc controller data channel to indicate that data channel is ready to receive disc status word.
	OTA	CC	Output Status Check command to last used disc drive unit number.
	CLC	CC	Ensure that command channel Device Command FF is cleared so that disc controller will respond to next STC instruction. (See note 1.)
	STC	CC,C	Execute command.
	SFS	DC	Is disc status word available?
	JMP	*-1	No, wait.
	LIA	DC	Yes, transfer disc status word into A-register.
	CLC	DC	Prevent unwanted interrupts on data channel.
	SSA		Skip if attention bit in Status word is zero.
	JMP	SS2A	Attention bit is a "1", therefore unit has completed Seek Record operation. Perform Status Check.
	JMP	SS3	Re-examine attention bits.
SS2	STB	UNIT	Store disc drive unit number performing operation in memory location.
SS2A	EQU	*	Label for entering the following operation.
	—	—	Perform Status Check operation on unit just determined.

Table 2-4. Multiple Seek Record Operations (Continued)

LABEL	OPCODE	OPERAND	COMMENTS
	—	—	Perform Read Data or Write Data operation on ready disc drive unit as a function of unit number.
	—	—	Perform Status Check operation which eliminates this unit's attention bit from being true.
	ISZ	VAR 1	Increment memory location by one each time a Read Data or Write Data operation is performed.
	LDA	VAR 1	Load into A-register the number corresponding to the number of times Read Data or Write Data operations are performed.
	CPA	D3	Have three operations been performed?
	JMP	DONE	Yes, multiple operations complete.
	JMP	SS3	No, find next ready disc drive unit.
VAR 1	BSS	1	Allocates one memory location for temporary storage of variables.
STAT	OCT	0	Specifies Status Check command.
SKCMD	OCT	30000	Specifies Seek Record command.
UNIT	BSS	1	Allocates one memory location for temporary storage of unit numbers.
CYL	BSS	1	Allocates one memory location for temporary storage of cylinder numbers.
HDSCT	BSS	1	Allocates one memory location for temporary storage of head/sector numbers.
CYL 1	DEC	0	Specifies cylinder 0.
CYL 2	DEC	202	Specifies cylinder 202.
CYL 3	DEC	100	Specifies cylinder 100.
HDST 1	OCT	0	Specifies head 0, sector 0.
HDST 2	OCT	1413	Specifies head 3, sector 11.
HDST 3	OCT	405	Specifies head 1, sector 5.
CC	EQU	nn	Where nn is the select code of the command channel card.
DC	EQU	nn	Where nn is the select code of the data channel card.
D4	DEC	4	Specifies decimal 4 for count comparisons.
D3	DEC	3	Specifies decimal 3 for count comparisons.

Table 2-4. Multiple Seek Record Operations (Continued)

LABEL	OPCODE	OPERAND	COMMENTS
			SEEK RECORD SUBROUTINE
SEEK	NOP		
	LDA	CYL	Load cylinder number from memory into A-register.
	OTA	DC	Output cylinder number to data channel.
	STC	DC,C	Output Device Command signal to disc controller data channel to indicate that cylinder number is available.
	LDA	SKCMD	Load Seek Record command into A-register.
	IOR	UNIT	Place disc drive unit number into A-register with Seek Record command.
	OTA	CC	Output Seek Record command and disc drive unit number to command channel.
	CLC	CC	Clear command channel Device Command FF so that disc controller will respond to the next STC instruction. (See note 1.)
	STC	CC,C	Execute command.
	SFS	DC	Has disc controller accepted cylinder number?
	JMP	*-1	No, wait.
	LDA	HDSCT	Yes, load head/sector number from memory into A-register.
	OTA	DC	Output head/sector number to data channel.
	STC	DC,C	Output Device Command signal to disc controller data channel to indicate that head/sector number is available.
	SFS	DC	Has disc controller accepted head/sector number?
	JMP	*-1	No, wait.
	JMP	SEEK,I	Yes, return to program.

NOTE: 1. The disc controller responds only to a true-going Device Command signal. If the STC instruction is issued while the Device Command FF is set, the disc controller will not respond.

writes the address field. The address information is that in the record address register. The cylinder indicator information is written according to the state of bits 8 and 9 of the command word. If bit 8 is a "1," the defective cylinder indicator is set. If bit 9 is a "1," the protected cylinder indicator is set. The controller never sets both indicators; if both bits 8 and 9 are "1's" in the command word, only the defective cylinder indicator is set.

2-40. Data transfer from the computer begins with the first data word. The disc controller always writes 128 data words in a sector. If the computer sends less than 128 words, the disc controller fills the remainder of the sector with "0's" before setting the Flag FF on the command channel card. If the computer has more than 128 words to write, the disc controller adds one to the contents of the record address register and continues writing in the next

sector. Data transfer is suspended as the disc controller assembles and writes the sector address field again using the command word to determine the state of the cylinder indicators. Data transfer resumes with the first data word of the sector. Writing continues until the computer has no more data to transfer, or until the controller detects an End of Cylinder or other error condition. In either case, the Flag FF is set on the command channel interface card to signal completion.

2-41. ADDRESS RECORD. The Address Record command is used to alter the contents of the record address register in the disc controller. The command is executed in the same manner as the Seek Record command, except that no operation is initiated on the disc drive unit specified. (Hence, the disc controller makes no use of the disc drive unit select information in the command word.) When the command is issued, the disc controller accepts two words of address information from the data channel card. The format of the address words is that described in paragraph 2-30. As the disc controller accepts each of these words, it assembles a new record address in the record address register (previous contents of the register are lost). When the second address word has been accepted, command execution terminates, and the Flag FF is set on the command channel card.

2-42. STATUS WORD.

2-43. The disc status word is a 16-bit word which can be initiated by the disc system by a Status Check command word from the computer program. The status word then can be transferred to the computer by a LIA/B instruction to the data channel I/O select code. A sample program to obtain the disc status word is provided in table 2-5. The format and content of the disc status word are given in table 2-6.

2-44. DATA TRANSFER TIMING CONSIDERATIONS.

Note

The restrictions in paragraphs 2-45 and 2-46 apply only to transfer of file data and not to transfers involving address, count, or status information.

Table 2-5. Sample Program to Obtain Status Word

LABEL	OPCODE	OPERAND	COMMENTS
	LDA	STAT	Load Status Check Command into A-register.
	STC	DC,C	Data channel ready to accept status word from disc controller.
	IOR	UNIT	Place disc drive unit number into A-register.
	OTA	CC	Output Status Check Command to command channel.
	CLC	CC	Ensure that Device Command FF is cleared.
	STC	CC,C	Execute Command.
	SFS	DC	Status word received?
	JMP	*-1	No, wait.
	LIA	DC	Transfer Status word into A-register.
	CLC	DC	Prevent unwanted interrupts.
STAT	OCT	000000	Specifies Status Check Command.
UNIT	OCT	000000	Specifies disc drive unit 0.
DC	EQU	nn	Where nn is the select code of the data channel card.
CC	EQU	nn	Where nn is the select code of the command channel card.

Table 2-6. Disc Status Word

BIT	DESCRIPTION
0	ANY ERROR. A "1" indicates that any one or more of the remaining 15 bits (except bits 2, 3, and 7) is a "1." Also, the ANY ERROR bit is a "1" whenever bit 3 (FLAGGED CYLINDER) is a "1" as a result of Write Data or Initialize Data commands. Bit 3 does not generate an ANY ERROR status when it occurs as a result of Read Data or Check Data commands.
1	DATA ERROR. A "1" indicates an error has been detected in the data transfer between the disc controller and the disc drive unit during a read, write, or check operation. The condition is reset with the execution of a Status Check command to the disc drive unit on which the condition occurred.
2	DRIVE BUSY. A "1" indicates the selected drive is busy executing a Seek Record command.
3	FLAGGED CYLINDER. A "1" indicates the cylinder being processed is write-protected or defective or the Initialize Data command has been issued with the OVERRIDE switch on the controller set to OFF. The condition is reset with execution of a Status Check command.
4	ADDRESS ERROR. A "1" indicates the address read from the track does not compare with contents of the record address register in the disc controller, or (when bit 3 (FLAGGED CYLINDER) also is a "1") the cylinder being processed is defective. The condition is reset with the execution of a Status Check command.
5	END OF CYLINDER. A "1" indicates the computer has attempted to extend a data command across a cylinder boundary. This occurs when the computer has more data to write or read and the end of sector 11, head 1 or the end of sector 11, head 3 has been reached.
6	NOT READY. A "1" indicates that the selected disc drive unit is not connected to the disc controller, or is not sequenced up with disc spinning and heads loaded, or is in an unsafe condition. (In the latter case, bits 11 and/or 12 will also be a "1.") Normally, manual intervention is required to bring a disc drive unit from the not-ready to the ready state.
7	Not used.
8	SEEK CHECK. A "1" indicates that the selected disc drive unit has been issued a Seek Record command calling for a cylinder number greater than 202, or a Seek Record command has been issued while a servo positioning operation was still in progress on the selected disc drive unit. The condition is reset by the next properly issued Seek Record command to the disc drive unit in question.
9	SEEK INCOMPLETE. A "1" indicates that a servo positioning operation failed to be completed normally on the selected disc drive unit. The condition is reset by the next Seek Record command issued to the disc drive unit.
10	ACCESS HUNTING. A "1" indicates that checking circuits in the selected disc drive unit have detected misadjustment in the disc drive unit servo system. The condition is reset by the next Seek Record command issued to the disc drive unit.
11	ACCESS UNSAFE. A "1" indicates that checking circuits in the selected disc drive unit have detected an unusual condition in the drive access system. Bit 6 will also be a "1." The condition is reset by recycling power to the disc drive unit in question.
12	READ/WRITE UNSAFE. A "1" indicates that checking circuits in the selected disc drive unit have detected an unusual condition in the drive read/write circuits. Bit 6 will also be a "1." The condition is reset by unlocking the disc cartridge on the disc drive unit in question.

Table 2-6. Disc Status Word (Continued)

BIT	DESCRIPTION
13	OVERRUN. A "1" indicates that checking circuits in the disc controller have detected a late transfer response or a failure in the controller data clocking circuits. During the data transfer portion of Write Data, Read Data, or Initialize Data commands, the condition is generated when the data transfer response from the computer occurs after termination of data transfer but before the disc controller has signaled completion of the operation by setting the Flag FF on the command channel card.
14	FIRST SEEK. A "1" indicates that the selected disc drive unit has gone from the not-ready to the ready state. Bit 15 will also be a "1." The condition is reset with the execution of a Status Check command to the disc drive unit that generated the condition.
15	ATTENTION. A "1" indicates that an operation previously in progress on the selected disc drive unit has terminated either through normal completion or due to occurrence of an error or other unusual condition. During execution of all commands except Status Check, the condition is generated when command execution terminates regardless of the cause for termination. Presence of the attention condition generates a command channel Device Flag signal if the Device Command FF on the command channel card is set. The attention condition is reset with the execution of a Status Check command to the disc drive unit that generated the condition.

2-45. During data transfer to and from the disc controller, the computer must transfer data at an average rate equal to the data rate of the disc drive unit. (The data rate of the disc drive unit is from 40,500 words per second to 49,500 words per second.) This transfer rate is maintained by the request/response nature of the computer/disc controller communication on the data channel card. The disc controller transfers a word of data and sets the Flag FF on the data channel card to request service. The computer, in turn, accepts the data through DMA and sends a Device Command signal (STC instruction) to the disc controller to input another data word.

2-46. In order to maintain data transfers with the disc drive unit, the computer must respond to the request for service within a certain length of time (termed overrun time). (The overrun time of the disc drive unit is from 19.2 microseconds to 25.6 microseconds.) If the computer fails to respond within the overrun time, the disc controller terminates the data transfer with the computer. No further communications occur on the data channel card. The disc controller completes processing of the current sector before setting the Flag FF on the command channel card. If a write operation is in process, "0's" are written in the remainder of the field; if a read operation is in process, the remainder of the field is cyclic checked. If the computer responds with a STC instruction to the data channel card after the termination of data transfer but before the setting of the Flag FF on the command channel card, the disc controller sets a data overrun error latch. This is to warn the program that the computer may have failed to transfer as much data as intended.

2-47. SAMPLE PROGRAMS.

2-48. Sample input and output programs are given in tables 2-7 and 2-8. Table 2-9 gives a summary of device flag responses to command words as an aid in varying a program to suit particular needs.

2-49. PROGRAMMING RECOMMENDATIONS.

2-50. DESIGN CONSIDERATIONS. The cartridge disc system has been designed to function with an interrupt driven program. In most cases, the best level of system performance will be achieved when the program issues one or more disc storage commands and then goes on to other tasks, relying upon the disc controller to generate a command channel interrupt whenever a command is completed. Following each interrupt, the program must issue a Status Check command to the disc drive unit that executed the storage command and verify that the Any Error bit (bit 0) is not a "1" in the disc status word. A new command can then be issued to any of the disc drive units in the system. Although the disc controller has no capability to queue or execute more than one read or write command at a time, provisions have been made to allow overlap of Seek Record commands on multiple disc drive unit systems. (Refer to paragraph 2-34.) In applications where more than one disc drive unit is active, such overlap should be used to minimize the effects of accessing delays.

2-51. DISC CONTROLLER RECORD ADDRESS REGISTER CONTROL. Although the "one ahead" nature of the record address register (RAR) operation seems to imply a need for plus one or minus one addressing, such is not the case. The program need only ensure that whenever a data handling command (Write Data, Read Data, Refine Sector, Check Data, or Initialize Data) is issued the RAR contains the complete address of the first sector to be processed. If the RAR is set to cylinder 6, head 1, sector 3 when a Write Data command is issued, then the same data will be read back if the RAR is set to cylinder 6, head 1, sector 3 and a Read Data command is issued.

Table 2-7. Sample Input Program

LABEL	OPCODE	OPERAND	COMMENTS
			DISC ADDRESSING
	LDA	CYL	Load cylinder number into A-register.
	OTA	DC	Output cylinder number to data channel.
	STC	DC,C	Output Device Command signal to disc controller data channel to indicate that cylinder number is available.
	LDA	SKCMD	Load Seek Record Command into A-register.
	CLC	CC	Ensure that command channel Device Command FF is cleared so that disc controller will respond to next STC instruction.
	OTA	CC	Output Seek Record Command to command channel.
	STC	CC,C	Execute command.
	SFS	DC	Cylinder number accepted by disc controller?
	JMP	*-1	No, wait.
	LDA	HDSCT	Yes, load head/sector number into A-register.
	OTA	DC	Output head/sector number to data channel.
	STC	DC,C	Output Device Command signal to disc controller data channel to indicate that head/sector number is available.
	SFS	CC	Seek Record complete?
	JMP	*-1	No, wait.
			INITIALIZE DMA
	LDA	CW1	Yes, fetch Control Word 1 (CW1) from core memory and load into A-register.
	OTA	6	Output CW1 to DMA.
	CLC	2	Prepare DMA memory address register to receive CW2.
	LDA	CW2	Fetch Control Word 2 (CW2) from core memory and load into A-register.
	OTA	2	Output CW2 to DMA.
	STC	2	Prepare DMA word-count register to receive CW3.
	LDA	CW3	Fetch Control Word 3 (CW3) from core memory and load into A-register.
	OTA	2	Output CW3 to DMA.

Table 2-7. Sample Input Program (Continued)

LABEL	OPCODE	OPERAND	COMMENTS
			START DISC READ OPERATION AND DMA
	LDA	RDCMD	Load Read Command into A-register.
	CLC	CC	Ensure that command channel Device Command FF is cleared so that disc controller will respond to next STC instruction.
	OTA	CC	Output Read Command to command channel.
	STC	DC,C	Data channel ready to accept first data word. Clear data channel flag to prevent erroneous data from being sent to DMA before first data word.
	STC	6,C	Activate DMA.
	STC	CC,C	Execute Read Command.
CYL	OCT	000053	Specifies cylinder number address (43_{10}).
DC	EQU	nn	Where nn is the select code of the data channel card.
CC	EQU	nn	Where nn is the select code of the command channel card.
SKCMD	OCT	030000	Specifies Seek Record Command word for disc drive unit 0.
HDSCT	OCT	001413	Specifies head 3, sector 11_{10}.
CW1	OCT	120010	Assignment for DMA; specifies I/O data channel select code address (10_8), STC after each word is transferred, and CLC after final word is transferred. (See Note 1.)
CW2	OCT	100200	Memory address register control for DMA; specifies memory input operation and starting memory address (200_8).
CW3	OCT	177662	Word count register control for DMA; specifies the two's complement of the number of words in the block to be transferred (78_{10}).
RDCMD	OCT	020000	Specifies Read Data Command word for disc drive unit 0.
NOTE: 1. CLC to the data channel card does not clear the Device Command FF.			

2-52. Use can be made of the fact that the RAR address is updated by the disc controller when multiple sectors are processed (such as reading or writing more than 128 words of data). If the program needs to read sectors 2 and 3 into one core memory block and sectors 4 and 5 into another, two Read Data commands are used. The RAR sector address must be at 2 when the first Read Data command is issued (and a DMA word count of 256). When the command is completed, the program executes a Status Check command to test for errors, modifies the core memory starting address, and issues a second Read Data command. Similar techniques may be used for writing successive sectors from several different core memory locations.

2-53. WRITE CHECKING. When records are written on a disc drive unit, some form of program check should be executed to ensure that the record was written exactly as it existed in core memory and that the record can be recovered without error from the disc. Where data integrity is crucial, each record written should be read back from the disc into core memory and compared word-for-word with the original record transferred during the write operation. This provides a check, not only on the serial data transfer between the disc controller and the disc drive unit, but also on the parallel transfer between the disc controller and the computer. The latter is important since the system provides no hardware check of parallel data transfer.

Table 2-8. Sample Output Program

LABEL	OPCODE	OPERAND	COMMENTS
			DISC ADDRESSING
	LDA	CYL	Load cylinder number into A-register.
	OTA	DC	Output cylinder number to data channel.
	STC	DC,C	Output Device Command signal to disc controller data channel to indicate that cylinder number is available.
	LDA	SKCMD	Load Seek Record Command into A-register.
	CLC	CC	Ensure that command channel Device Command FF is cleared so that disc controller will respond to next STC instruction.
	OTA	CC	Output Seek Record Command to command channel.
	STC	CC,C	Execute command.
	SFS	DC	Cylinder number accepted by disc controller?
	JMP	*-1	No, wait.
	LDA	HDSCT	Load head/sector number into A-register.
	OTA	DC	Output head/sector number to data channel.
	STC	DC,C	Output Device Command signal to disc controller data channel to indicate that head/sector number is available.
	SFS	CC	Seek Record complete?
	JMP	*-1	No, wait.
			INITIALIZE DMA
	LDA	CW1	Yes, fetch CW1 from core memory and load into A-register.
	OTA	6	Output CW1 to DMA.
	CLC	2	Prepare DMA memory address register to receive CW2.
	LDA	CW2	Fetch CW2 from core memory and load into A-register.
	OTA	2	Output CW2 to DMA.
	STC	2	Prepare DMA word-count register to receive CW3.
	LDA	CW3	Fetch CW3 from core memory and load into A-register.
	OTA	2	Output CW3 to DMA.

Table 2-8. Sample Output Program (Continued)

LABEL	OPCODE	OPERAND	COMMENTS
		START DISC WRITE OPERATION AND DMA	
	LDA	WRCMD	Load Write Command into A-register.
	CLC	CC	Ensure that command channel Device Command FF is cleared so that disc controller will respond to next STC instruction.
	OTA	CC	Output Write Command to command channel.
	STF	DC	Ensure that the first word to disc controller data channel is the first data word from core memory and not spurious data.
	STC	6,C	Activate DMA.
	STC	CC,C	Execute Write Command.
CYL	OCT	000224	Specifies cylinder number address (148_{10}).
DC	EQU	nn	Where nn is the select code of the data channel card.
CC	EQU	nn	Where nn is the select code of the command channel card.
SKCMD	OCT	030001	Specifies Seek Record Command word for disc drive unit 1.
HDSCT	OCT	001005	Specifies head 2, sector 5_{10}.
CW1	OCT	120010	Assignment for DMA; specifies I/O data channel select code address (10_8), STC after each word is transferred, and CLC after final word is transferred. (See Note 1.)
CW2	OCT	000300	Memory address register control for DMA; specifies memory output operation and starting memory address (300_8).
CW3	OCT	177644	Word count register control for DMA; specifies the two's complement of the number of words in the block to be transferred (92_{10}).
WRCMD	OCT	010001	Specifies Write Data Command word for disc drive unit 1.

NOTE: 1. CLC to the data channel card does not clear the Device Command FF.

2-54. Where data integrity is less crucial, issuing a Check Data command to the address of each record that is written on the disc is sufficient (refer to paragraph 2-36). This provides a check on the serial data transfer between the disc controller and the disc. Write checking should be eliminated from the program in those situations where data integrity is not crucial.

2-55. CARTRIDGE DISC INITIALIZATION. All cartridge discs have been analyzed for defects by the disc manufacturer according to accepted industry standards. Prior to use in a system, new (unwritten) cartridge discs should be processed by a disc initialization program. The program should initialize all sectors to generate the sector address fields and provide for flagging any cylinders found defective by the disc manufacturer. (Refer to paragraph 2-39.) Also, the program should execute additional data testing to help isolate defects which may have developed after manufacture. The additional data testing should include the following routine executed six times on each cylinder:

a. Write a fixed pattern in all data fields of the cylinder.

b. Execute the Check Data command 10 times to all sectors of the cylinder.

Table 2-9. Device Flag Responses to Command Words

COMMAND	RESPONSE
STATUS CHECK	Device flag is issued to data channel card after the status word is transferred. (See note 1.)
WRITE DATA	Device flag is issued to data channel card after each data word is transferred. Device flag is issued to command channel card after completion.
READ DATA	Device flag is issued to data channel card after each data word is transferred. Device flag is issued to command channel card after completion.
SEEK RECORD	Device flag is issued to data channel card after each address word is transferred. Device flag is issued to command channel card after head positioning is complete. (See note 1.)
REFINE SECTOR	Device flag is issued to command channel card at the end of the addressed sector.
CHECK DATA	Device flag is issued to data channel card after sector count word is transferred. Device flag is issued to command channel card after completion.
INITIALIZE DATA	Device flag is issued to data channel card after each data word is transferred. Device flag is issued to command channel card after completion.
ADDRESS RECORD	Device flag is issued to data channel card after each address word is transferred. Device flag is issued to command channel card after completion.

NOTE: 1. When the last data channel device flag has been issued for a Status Check or a Seek Record, the disc controller is free to process other commands. To issue another command, a CLC is first issued to the command channel. Any command may then be issued normally. If no command is issued after the last data channel device flag for a Status Check or a Seek Record, the disc controller will issue a command channel device flag if any positioner operation completes.

2-56. On each of the six passes, a different data pattern should be used. Below, in octal, are the six words recommended:

a. 000000
b. 101421
c. 125252
d. 052525
e. 162745
f. 170360

2-57. If a data error occurs more than once in executing the routine on a cylinder, the cylinder should be flagged defective.

2-58. CYLINDER FLAGGING AND DEFECTIVE CYLINDER PROCESSING. As discussed earlier, the disc controller provides the program with the ability to flag cylinders as either write-protected or defective. In either case, the entire cylinder (all 24 sectors) must be so flagged to avoid erroneous responses from the disc controller during subsequent operations on the cylinder. The Initialize Data command should be used for the flagging operation.

2-59. There are several workable schemes for handling defective cylinders. Regardless of the method employed, the following recommendations should be considered:

a. The system should allow up to three defective cylinders per disc (leaving 200 cylinders for active data storage).

b. If the system relies on reading an alternate cylinder address from the defective cylinder, the address should be written in several different (preferably in all) sectors of the defective cylinder.

2-60. ERROR RECOVERY PROCEDURES. Certain errors which are detected in the disc status word (see table 2-6) during data storage operations are often correctable through re-try procedures. User programs should include provisions for re-try to reduce the frequency of errors which impact on the application. Listed below are the correctable error conditions and the recommended re-try procedures for each:

a. Data Error During Read Data Operation. Read the same record 16 times. If the error persists after 16 re-tries, issue a Seek Record command to cylinder 0, issue a Seek Record command to cylinder 202, issue a Seek Record command to the failing record address, and re-read up to 16 times. If error persists, issue a Refine Sector command to the failing record address and re-read 16 times. If error persists, terminate re-try.

b. Data Error During Write or Initialize Data Operations. Re-try the write or initialize data operation once. If error persists, terminate re-try.

c. Data Error During Write Check Routine. If data error occurs during the Read Data or Check Data operations used in a write check routine (refer to paragraph 2-53), the complete Write Data operation and write check routine should be re-tried three times or more. If the error persists, the cylinder should be either flagged immediately or logged for future checking and possible flagging. If an error is detected during the word-for-word comparison, the Write Data operation and write check routine should be re-tried once.

d. Address Error, Seek Incomplete, or Access Hunting. Issue a Seek Record command to cylinder 0, issue a Seek Record command to cylinder 202, and issue a Seek Record command to the failing cylinder. If error persists, terminate re-try.

e. Overrun. Re-try the operation once; if error persists, terminate re-try.

2-61. RECORD LENGTH. The maximum number of sectors that can be written or read before a new Seek Record command or Address Record command must be issued is 24. This can occur only if the Read Data or Write Data operation starts at head 0, sector 0 or at head 2, sector 0. The disc controller will automatically switch (when the end of sector 11 is reached) from head 0 to head 1 or from head 2 to head 3. The disc controller does not automatically switch from head 1 to head 2 or from head 3 to head 0. In other words, the disc controller cannot automatically switch from the cartridge disc to the fixed disc or from the fixed disc to the cartridge disc.

SECTION III

THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section contains a brief functional description of the cartridge disc interface kit followed by a detailed circuit description. An overall block diagram of the disc interface is shown in figure 3-1. Signal timing diagrams are given in figures 3-2 and 3-3. Functional flow diagrams for each command operation are provided in figures 3-4 through 3-9. Schematic diagrams of the two interface cards are provided in figures 4-1 and 4-2.

3-3. FUNCTIONAL DESCRIPTION.

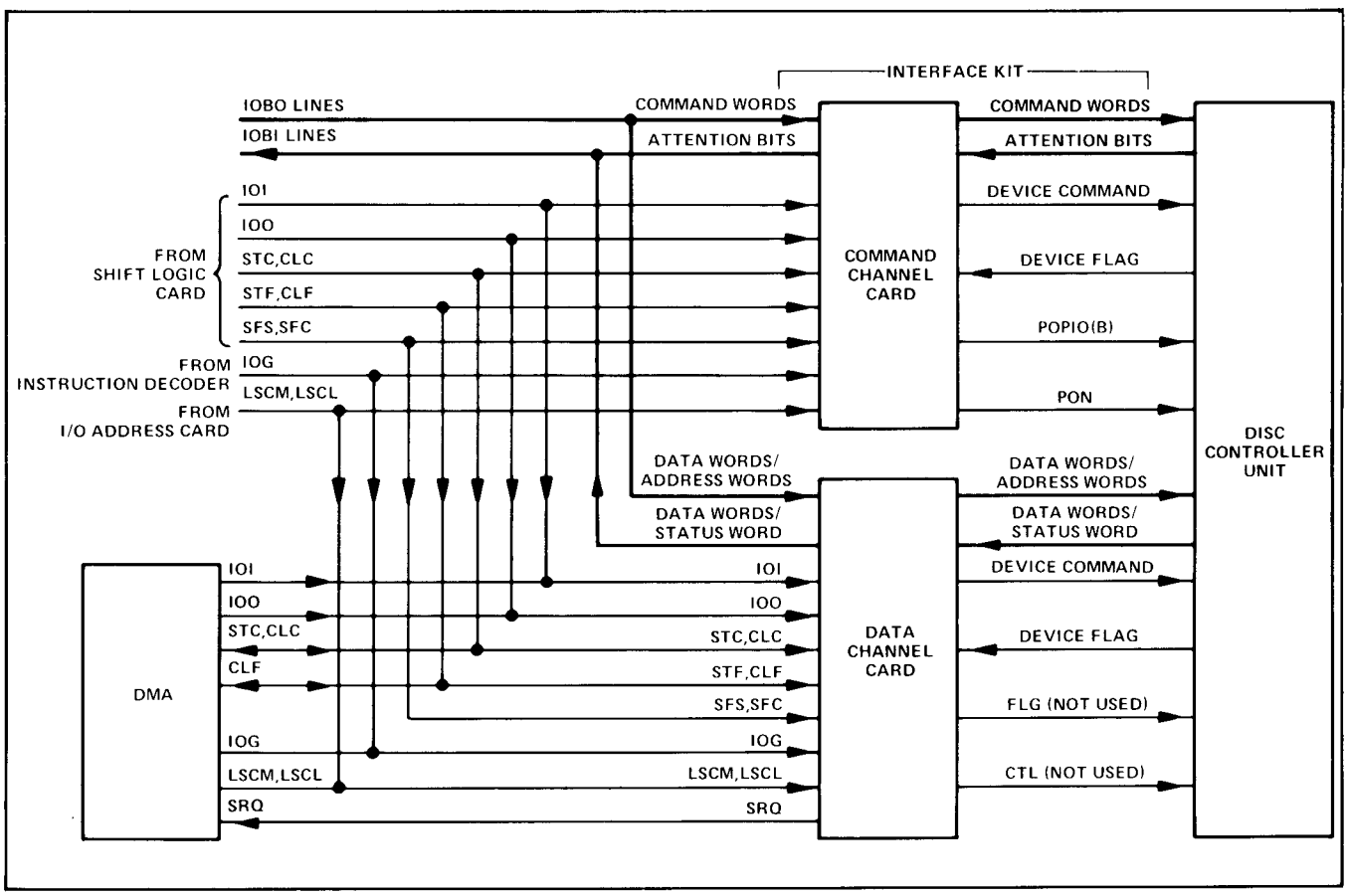
3-4. COMPUTER POWER ON.

3-5. When power is initially applied by the POWER switch on the front panel of the computer, the POPIO(B) and CRS signals are received simultaneously from the I/O control card. These signals establish initial conditions for operation of the command channel and data channel cards. The POPIO(B) signal sets the Flag Buffer FFs on each card and resets the output data and command bit lines from each card to logic 0 (+4.5 volts dc). The POPIO(B) signal from the command channel card is buffered and sent to the disc controller to establish initial conditions for the disc system. The CRS signal resets the Control FF and Device Command FF on each interface card.

3-6. When the dc power supplies in the computer have settled to the proper output voltages, the Power On Normal (PON) signal is applied to the interface cards for buffering. Only the buffered PON signal from the command channel card is applied to the disc controller to indicate that the computer dc power supplies are operating properly.

3-7. DATA OUTPUT OPERATIONS.

3-8. To output data to the disc memory system, address words are sent through the data channel and command words are sent through the command channel to prepare the system for a write operation. Data to be written is then sent through the data channel under DMA control.



2090-1

Figure 3-1. Cartridge Disc Interface Overall Block Diagram

3-9. CYLINDER NUMBER TRANSFER. The cylinder number is placed in the A- or B-register by a load A/B (LDA/B) instruction. An Output from A/B (OTA/B) instruction to the data channel card select code places the cylinder number (bits 0 through 7) on the IOBO lines to the output buffer register on the data channel card. The IOO signal from the computer, as a result of the OTA/B instruction, clocks the cylinder number into the output buffer register. The cylinder number is now present on the data channel lines to the disc controller. The output buffer register still contains the cylinder number until the IOBO lines change state and another IOO signal to the data channel select code is received. The voltage levels of the bits are inverted by the gates at the output of the buffer register to make the buffer register logic compatible with the disc controller logic. A set control, clear flag (STC,C) instruction to the data channel select code sets the Device Command FF and clears the Flag Buffer FF and Flag FF. The set output from the Device Command FF is inverted and sent to the disc controller data channel as a ground-true Device Command signal. The Device Command signal indicates that information is available on the data channel lines to the disc controller.

3-10. SEEK RECORD COMMAND TRANSFER. The Seek Record command word is placed in the A- or B-register by a LDA/B instruction. An OTA/B instruction to the command channel select code places the command word on the IOBO lines to the output buffer register on the command channel card. The IOO signal from the computer, as a result of the OTA/B instruction, clocks the Seek Record command word into the output buffer register. The Seek Record command word is now present on the command channel lines to the disc controller. The voltage levels of the command word bits are inverted by the gates at the output of the buffer register to make the buffer register logic compatible with the disc controller logic. An STC,C instruction to the command channel select code sets the Device Command FF and clears the Flag Buffer FF and Flag FF. The set output from the Device Command FF is inverted and sent to the disc controller command channel as a ground-true Device Command signal. This signal causes the disc controller to decode the command word and initiate write/read head positioning on the selected drive. The disc controller issues a Device Flag signal to the data channel interface card to set the Flag Buffer FF and Flag FF when the cylinder number has been accepted.

3-11. HEAD/SECTOR NUMBER TRANSFER. The head/sector number bits (see figure 2-2) are transferred to the disc controller by the same instructions and in the same manner as the cylinder number. When the disc controller accepts the head/sector number, it issues a Device Flag signal to set the Flag Buffer FF and Flag FF and to clear the Device Command FF on the data channel card. After the head positioning operation is complete, the disc controller issues a Device Flag signal to clear the Device Command FF and to set the Flag Buffer FF and Flag FF on the command channel card.

3-12. WRITE DATA COMMAND TRANSFER. Before the Write Data command is issued, DMA is initialized to prepare DMA to respond with the proper data and assume control of the data transfer when the Write Data Command is accepted by the disc controller. During initialization, the starting address in memory that contains the data is specified along with the number of data words to be transferred.

3-13. The Write Data command word bits (see figure 2-1) are transferred to the disc controller by the same instructions and in the same manner as the Seek Record command. (Refer to paragraph 3-10.) Next, the program issues a STF instruction to the data channel card. The resulting STF signal sets the Flag Buffer FF and Flag FF. The set output from the Flag FF is sent to DMA as a Service Request (SRQ) signal. The disc controller will issue a Device Flag signal to the command channel card when all the data has been transferred and the write operation is complete.

3-14. DATA TRANSFER. When DMA receives the SRQ signal from the data channel card, phase 5 is set on the next machine cycle and DMA provides SCL, SCM, IOG, and IOO signals to transfer data to the disc. The SCL, SCM, and IOG signals enable the IOO signal to clock the first data word into the output buffer register onto the data channel lines to the disc controller. Also, DMA issues a STC instruction to the data channel interface card which generates the Device Command signal to indicate that a data word is present on the data lines to the disc controller. When the data word is accepted, the disc controller issues Device Flag to clear the Device Command FF and set the Flag Buffer FF and Flag FF. The set output from the Flag FF (SRQ signal) is sent to DMA and the process is repeated for each word until all the data words are transferred.

3-15. DATA INPUT OPERATIONS.

3-16. Data is transferred from the disc system to the computer by sending address and read command words through the data and command channels, and receiving data words, under DMA control, through the data channel.

3-17. ADDRESSING. Addressing the disc system to locate the data to be read consists of sending the cylinder number, the Seek Record command, and the head/sector number to the disc controller in the same manner as described in paragraphs 3-9 through 3-11.

3-18. READ DATA COMMAND TRANSFER. Before the Read Data command is issued, DMA is initialized to prepare DMA to assume control of the data transfer when the Read Data command word is accepted by the disc controller. During initialization, the starting address in memory where the first data word will be stored and the number of data words to be transferred are specified. The last step in the initialization process sends a STC,C instruction to the data channel interface card to set the Device Command FF and clear the Flag Buffer FF and Flag FF.

3-19. The Read Data command word bits (see figure 2-1) are transferred to the disc controller by the same instructions and in the same manner as the Seek Record command. (Refer to paragraph 3-10.) When the disc controller has accepted the Read Data command word and has applied the first data word to the input buffer register on the data channel card, it issues a Device Flag signal to the data channel card. This clears the Device Command FF and sets the Flag Buffer FF and Flag FF. The set output from the Flag FF (SRQ signal) is sent to DMA to start the data transfer. Also, the Device Flag signal clocks the data word into the input buffer register.

3-20. DATA TRANSFER. When DMA receives the SRQ signal from the data channel card, phase 5 is set on the next machine cycle and DMA provides LSCL, LSCM, IOG, STC, CLF, and IOI signals to transfer data to the computer. The IOI signal gates the data out of the input buffer register onto the IOBI lines for storage in memory.

3-21. Next, DMA issues STC and CLF signals to the data channel card. The STC signal sets the Device Command FF which in turn sends a Device Command signal to the disc controller. The CLF signal clears the Flag Buffer FF and Flag FF to enable the Device Flag signal to generate another SRQ signal. The disc controller responds with another data word to the input buffer register and a Device Flag signal to clock the data into the input buffer register. The Device Flag signal also clears the Device Command FF and sets the Flag Buffer FF and Flag FF. The set output from the Flag FF sends another SRQ signal to DMA which sets the computer in another phase 5 mode on the next machine cycle. The above process is repeated for each data word until the number of data words specified during initialization of DMA have been transferred.

3-22. On the last phase 5 of the data transfer, the STC signal is not sent to the data channel card to prevent the disc controller from inputing another data word beyond the number specified. A CLC signal from DMA is sent during the last phase 5 to clear the Control FF on the data channel card.

3-23. DETAILED CIRCUIT DESCRIPTION.

3-24. COMPUTER POWER ON.

3-25. When power is initially applied, POPIO(B) and CRS signals are applied simultaneously to both interface cards. The POPIO(B) signal, through "nand" gate U26D, sets the Flag Buffer FF, provides a ground-true POPIO(B) signal to the disc controller through "and" gate U101A on the command channel card (the POPIO(B) from the data channel card is not used), and provides a clock input to the output buffer register FFs through "nand" gate U75A. The true clock input clears the flip-flops since all IOBO lines are false at power turn on. The output gates from the buffer register invert the positive-true/ground-false signal levels to ground-true/positive-false levels to be compatible with the disc controller logic. The Control Reset (CRS) signal resets the Control FF and Device Command FF through "nand" gates U45C, U45B, and U45D on the command channel card. On the data channel card, the Device Command FF is reset through "nand" gate U45C and jumper wire W9 in position B. The CRS signal buffered through "and" gate U101B is not used.

3-26. At time T2, the ENF signal from the I/O control card resets the Interrupt Request (IRQ) FF through "nand" gate U27C. The set output from the Flag Buffer FF and the ENF signal from "nand" gate U27D are "anded" by U26C, setting the Flag FF.

3-27. The Power On Normal (PON) signal applied to pin 66 of the interface cards is buffered through "and" gate U91B and connected through jumper wire W10A to pin W. Only the command channel card PON signal is routed to the disc controller. The positive-true PON signal indicates that the computer power supplies are operating normally, and a ground-false signal indicates a computer power fail.

3-28. OUTPUT OPERATIONS.

3-29. COMMAND CHANNEL CARD. Command words are placed on the IOBO lines to the output buffer register FFs by an OTA/B instruction to the command channel select code. The select code (LSCM, LSCL) from the I/O address card starting at time T1 of phase 1, along with the IOG(B) signal from the I/O control card starting at time T3, enables the instruction logic gates through "nand" gate U35A and U47B. The IOO signal, resulting from the OTA/B instruction, is applied to "nand" gate U35C at time T3T4. The remaining input to U47B is true at time T4 and remains true until time T2 of the following machine cycle. The false output from U35C during T4 is inverted by U75A to clock the command word into the output buffer register FFs. The gates in the output lines from the output buffer register are constantly enabled by jumper wire W4 in position B, which provides a constant true output from "nand" gate U65B. The command word is now present on the command channel lines to the disc controller. The false output from U35C is also applied to the ORL (Output Register Loaded) FF; however, this circuit is not used.

3-30. Next, a Set Control, Clear Flag (STC,C) instruction is issued to the command channel select code from the computer program. Again, the instruction logic gates are enabled by LSCM, LSCL, and IOG(B) signals starting at time T3. The STC and CLF signals are applied simultaneously during time T4. The STC signal sets the Control FF and Device Command FF through "nand" gate U47D. The true set output from pin 11 of the Control FF is applied to "nand" gate U36B to enable the disc controller Device Flag signal to cause an interrupt after the command has been executed. The buffered CTL signal from "nand" gate U94A is not used. The true set output at pin 12 of the Device Command FF is applied through jumper wire W1B and inverted by "nand" gate U65A to provide the ground-true Device Command signal to the disc controller command channel.

3-31. The CLF signal, through "nand" gate U37C, resets the Flag Buffer FF and the Flag FF. The true reset output from the Flag FF is applied to "nand" gate U36C to provide flag status information for the Skip if Flag Clear (SFC) instruction and applied to "nand" gate U77B to allow the Flag Buffer FF to be set when a Device Flag signal is received from the disc controller command channel.

3-32. The Device Flag signal is applied to pins 23 and AA of the command channel card when the addressed drive has executed the command. The negative-going Device Flag signal is inverted by "nand" gate U77A and delayed 100 nanoseconds by R61 and C3. The leading edge of the signal is shaped by schmitt trigger U77C, U77D, R62, R63, and R64. The positive-going output from U77D is applied through jumper wires W2B and W3B to the command reset pulse-shaping network (U76A, U76C, R66, and C5) and to the flag pulse-shaping network (U76B, U76D, R65, and C4). The output from each pulse-shaping network is a negative-going 300-nanosecond pulse. The pulse from U76D is inverted by U75B and applied to "nand" gate U77B which is enabled by the reset condition of the Flag FF. The resulting false output sets the Flag Buffer FF. The output from U75B also clocks the Bit 4 through Bit 15 FFs of the input buffer register through jumper wires W6 through W8; however, these bits are not used in this application.

3-33. The Flag Buffer FF set output sets the Flag FF at time T2 (ENF true) through "nand" gate U26C. The set output from the Flag FF is applied to "nand" gate U36A to provide flag status information for the Skip if Flag Set (SFS) instruction. The Service Request (SRQ) and Flag (FLG) signals generated by the set output of the Flag FF through gates U16B and U94A are not used in command channel operation. If the interrupt method is used with the command channel, the set output is also "anded" with the Interrupt Enable (IEN) signal from the I/O control card and with the Control FF set output by "nand" gate U36B. The false output disables "nand" gate U15A which prevents I/O devices of lower priority from requesting interrupt (PRL false). At time T5 (SIR true) the IRQ FF is set by "nand" gate U25A, providing that an I/O device of higher priority has not requested interrupt (PRH false). The true set output from the IRQ FF generates the FLGL and IRQL signals which are applied to the I/O address card to request the computer for an interrupt phase (phase 4) on the next available machine cycle and to specify the service request address (the memory location corresponding to the address, or select code, of the command channel card). Generally, the memory location will contain a jump to a service subroutine (JSB) instruction.

3-34. At time T1 of the fetch phase (phase 1), directly following the interrupt phase, IAK (interrupt acknowledge) is "anded" with the true set output from the IRQ FF by "nand" gate U45A to reset the Flag Buffer FF. Another command word may now be transferred by an OTA/B instruction followed by an STC,C instruction.

3-35. DATA CHANNEL CARD. Address words (cylinder and head/sector numbers) are transferred to the disc controller in the same manner and by the same instructions as the command words through the command channel. (Refer to paragraphs 3-29 through 3-33). However, the interrupt method is not used in data channel operation.

3-36. Data words are transferred by control signals provided by DMA during phase 5. After DMA has been initialized, the program sends a STF signal to the data channel interface card. The LSCM and LSCL signals from the I/O address card and the IOG(B) signal from the I/O control card enable the instruction logic gates at time T3 of the fetch phase (phase 1). The STF signal, during time T3, sets the Flag Buffer FF which, in turn, sets the Flag FF at time T2 of the next machine cycle.

3-37. The true set output from the Flag FF is applied to "nand" gate U94A and "and" gate U16B. The ground-true FLG signal from U94A is routed to the disc controller, but is not used. The positive-true Service Request (SRQ) signal from U16B is sent to DMA to set phase 5 on the next machine cycle. With phase 5 set, LSCM, LSCL, and IOG(B) signals are true during the entire machine cycle starting at time T0. The IOO and STC signals are applied simultaneously during T3T4. The STC signal sets the Device Command FF; the true set output is inverted by "nand" gate U65A to provide a ground-true Device Command signal to the disc controller data channel. The IOO signal is "anded" with the output from U47B and with the output from U57A, which is true starting at time T4, by "nand" gate U35C. The false output from U35C is inverted by U75A to apply a true clock signal to the output buffer register FFs during T4. The data word is gated onto the IOBO lines to the output buffer register at time T4T5 by DMA, and is present on the data channel lines to the disc controller starting at T4. The gates in the output lines from the output buffer register are constantly enabled by jumper wire W4 in position B at the input to "nand" gate U65B, which provides a constant true output. The output from U35C is also applied to the Output Register Loaded (ORL) FF; however, this circuit is not used.

3-38. The Clear Flag (CLF) signal is sent to the data channel card by DMA during time T4T5 of phase 5 to clear the Flag Buffer FF and the Flag FF. The SRQ signal is false when the Flag FF is cleared at the beginning of T4, which prevents another phase 5 from being set on the next machine cycle.

3-39. When the disc memory system has accepted the data word, the disc controller issues a negative-going Device Flag signal to the data channel card. The positive-going leading edge from U77A is shaped by the schmitt trigger circuit and applied through jumper wires W2B and W3B to the pulse-shaping networks in the same manner as described in paragraph 3-32. The false 300-nanosecond pulse from "nand" gate U76C resets the Device Command FF. The false pulse output from "nand" gate U76D is inverted through U85B and "anded" with the true reset output from the Flag FF to set the Flag Buffer FF. At time T2, the true set output from the Flag Buffer FF is "anded" with ENF

from "nand" gate U27D to set the Flag FF. The set output from the Flag FF generates another SRQ signal to set phase 5 on the next machine cycle.

3-40. The process described in paragraphs 3-37 through 3-39 is repeated for each data word transferred.

3-41. INPUT OPERATIONS.

3-42. COMMAND CHANNEL CARD. When the disc memory system consists of two or more disc drive units (four maximum) and multiple Seek Record command operations are used, attention bit sampling is necessary. (Refer to paragraph 2-31.) When multiple Seek Record commands are issued, the first disc drive unit to complete the execution will cause the disc controller to send a Device Flag signal to the command channel card simultaneously with the corresponding attention bit to the input buffer register. Jumper wire W5 is removed to allow the Bit 0 through Bit 3 FFs of the input buffer register to follow the state of the attention bits.

3-43. When the Device Flag signal is received, the Device Command FF is cleared and the Flag Buffer FF is set. At time T2, the Flag FF is set, and the true set output is "anded" with the SFS signal when the Skip if Flag Set (SFS) instruction is issued by the computer program. The resulting SKF signal at T4 causes the computer to skip the next instruction which may be a JMP *-1. (Refer to table 2-4.) On the next machine cycle, an LIA instruction to the command channel select code will generate a true IOI signal at T4T5. The true IOI signal is "anded" with the true output from U46B by "and" gate U15B. The resulting true output enables the gates in the input lines from the input buffer register during T4T5. The status of the attention bits is then put on the IOBI lines to the computer.

3-44. DATA CHANNEL CARD. The control signals required to transfer the data words to the computer are provided by DMA during phase 5; status words are transferred by control signals resulting from instructions in the computer program.

3-45. When the first data word is placed on the input lines to the input buffer register, a negative-going Device Flag signal is applied to pin 23 of the card. The positive-going leading edge from U77A is shaped by the schmitt trigger circuit and applied through jumper wires W2B and W3B to the pulse-shaping networks. The false 300-nanosecond pulse from U76C clears the Device Command FF. The false pulse output from U76D is inverted through U85B to provide a true clock signal for storing the data word in the input buffer register. The true pulse output from U85B is also "anded" with the true reset output from the Flag FF to set the Flag Buffer FF. At time T2 (ENF true), the set output from the Flag Buffer FF sets the Flag FF.

3-46. The true set output from the Flag FF is buffered through U16B to generate a true SRQ signal. The SRQ signal is sent to DMA to set phase 5 on the next machine cycle. With phase 5 set, LSCM, LSCL, and IOG(B) signals are true during the entire machine cycle. The IOI signal, which is true during T2 of phase 5, is "anded" with the true output from U46B by "and" gate U15B. The resulting true output from U15B gates the data word onto the IOBI lines for storage in computer memory.

3-47. During T3T4 of phase 5, the STC signal is true which sets the Device Command FF. The true set output is inverted by U65A to provide the ground-true Device Command signal to the disc controller. The Device Command signal causes the disc controller to input another data word.

3-48. During T4T5 of phase 5, the CLF signal is true which clears the Flag Buffer FF and the Flag FF. The SRQ signal is false when the Flag FF is cleared at the beginning of T4, which prevents another phase 5 on the next machine cycle.

3-49. The process described in paragraphs 3-45 through 3-48 is repeated for each data word until all the data words are transferred.

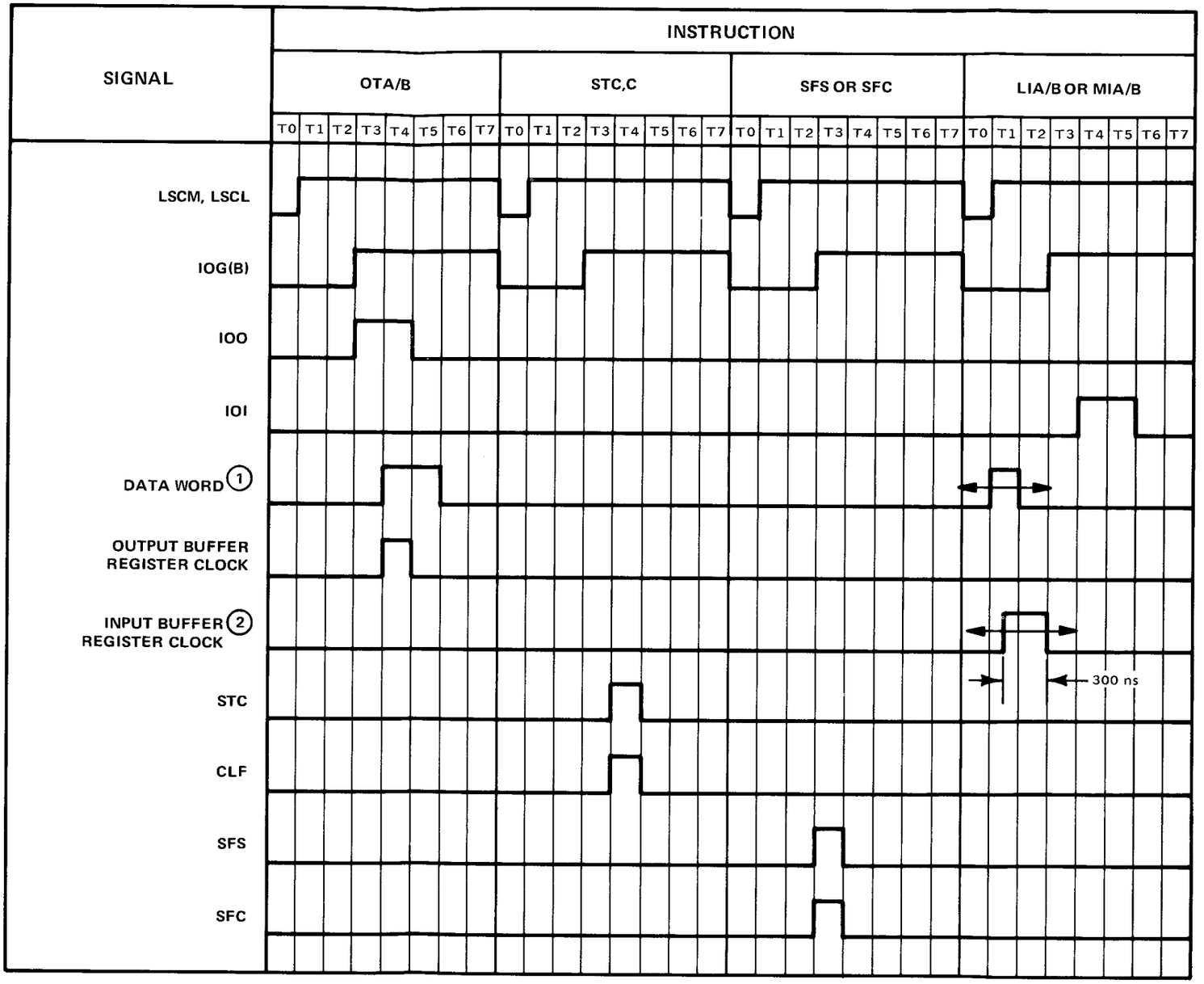
3-50. When the disc status word is placed on the input lines to the input buffer register, a Device Flag signal is sent to the data channel card. The Device Flag signal clears the Device Command FF, clocks the disc status word into the input buffer register, and sets the Flag Buffer FF. At time T2, the Flag FF is set.

3-51. If the Skip Flag method is used by the computer program, a Skip if Flag Set instruction will be issued by the program. The resulting SFS signal, which is true during T3, is "anded" with the true set output from the Flag FF to generate the SKF signal. The computer will skip the next instruction in the program and execute the following instruction. The following instruction may be an LIA/B to the data channel select code to input the disc status word into the A- or B-register. The IOI signal, resulting from the instruction, is true during time T4T5 and enables the gates in the input lines from the input buffer register. The disc status word is now present on the IOBI lines for storage in the A- or B-register.

3-52. If the interrupt method is used, the true set output from the Flag FF is "anded" with the true Interrupt Enable (IEN) signal from the I/O control card and with the true set output from the Control FF by "nand" gate U36B. The false output disables "nand" gate U15A which prevents I/O devices to lower priority from requesting interrupt (PRL false). At time T5 (SIR true), the IRQ FF is set by

"nand" gate U25A, providing that an I/O device of higher priority has not requested interrupt (PRH false). The set output from the IRQ FF generates the FLGL and IRQL signals which are applied to the I/O address card (I/O control card on 2114 Computers) to request the computer for an interrupt phase (phase 4) on the next available machine cycle and to specify the service request address (the memory location corresponding to the address, or select code, of the data channel interface card). Generally, the memory location will contain a jump to a service subroutine (JSB) instruction. The subroutine will contain an LIA/B or MIA/B instruction to gate the disc status word onto the IOBI lines.

3-53. At time T1 of the fetch phase (phase 1) directly following the interrupt phase, IAK (interrupt acknowledge) is "anded" with the true set output from the IRQ FF by "nand" gate U45A to reset the Flag Buffer FF.



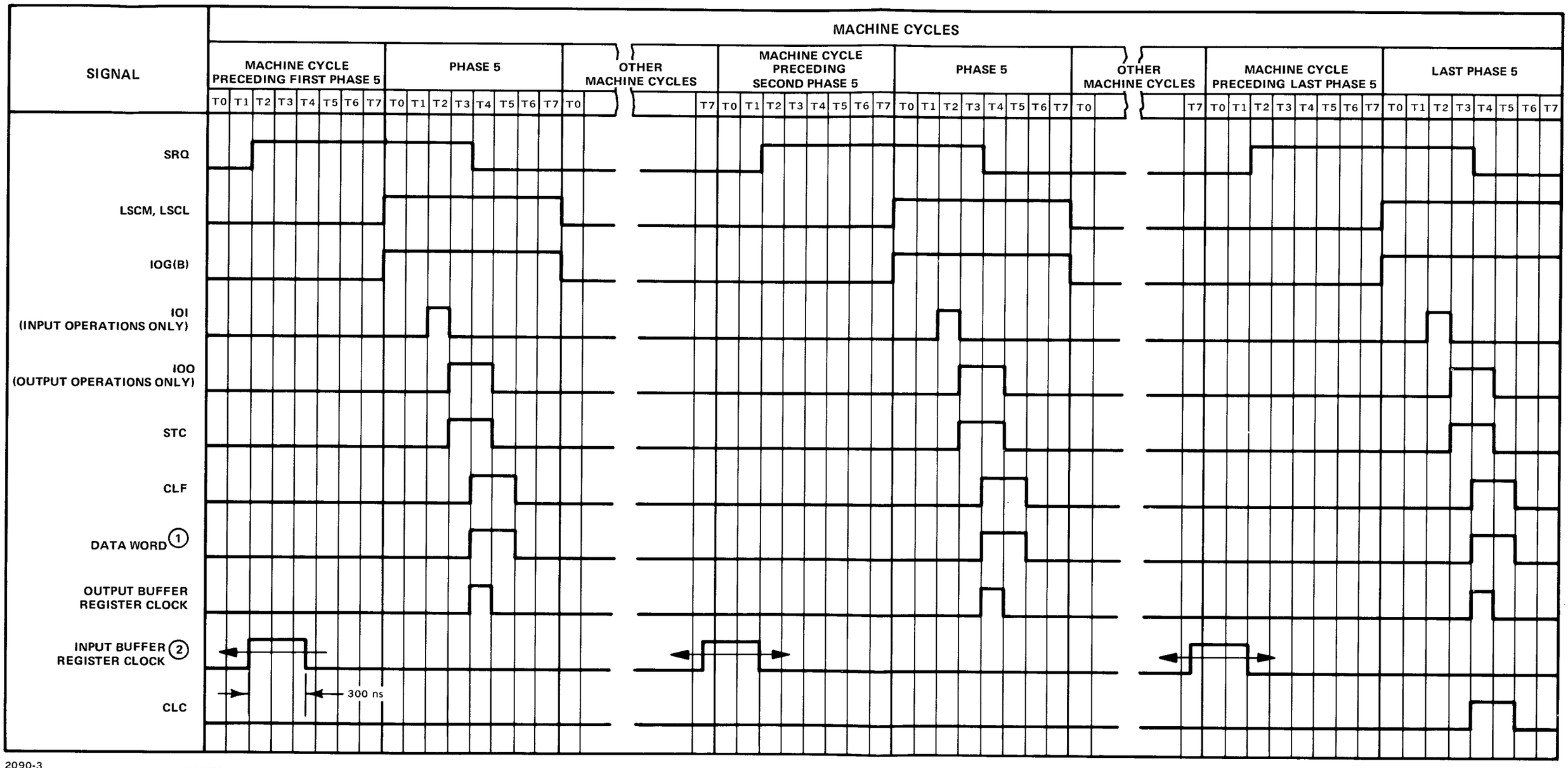
2090-2

NOTES:

(1) DATA WORD MEANS COMMAND WORD, ADDRESS WORD, STATUS WORD, OR ATTENTION BITS. THE STATUS WORD OR ATTENTION BITS WILL BE LOADED ONTO THE DATA LINES FROM THE DISC CONTROLLER SIMULTANEOUSLY WITH THE DEVICE FLAG SIGNAL.

(2) LEADING EDGE TIME OCCURS 100 NANOSECONDS AFTER THE DEVICE FLAG SIGNAL.

Figure 3-2. Signal Timing During Program Control



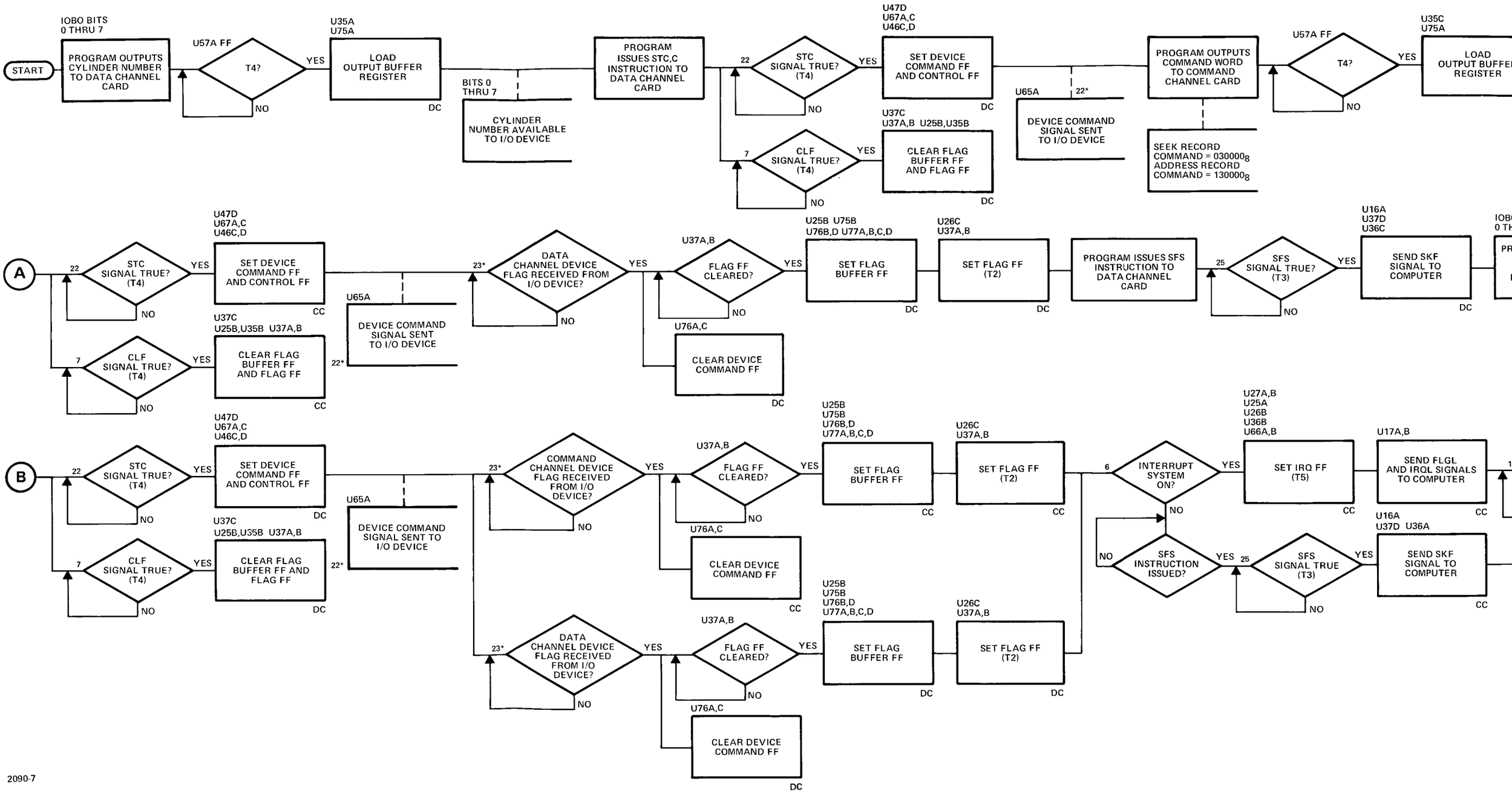
2090-3

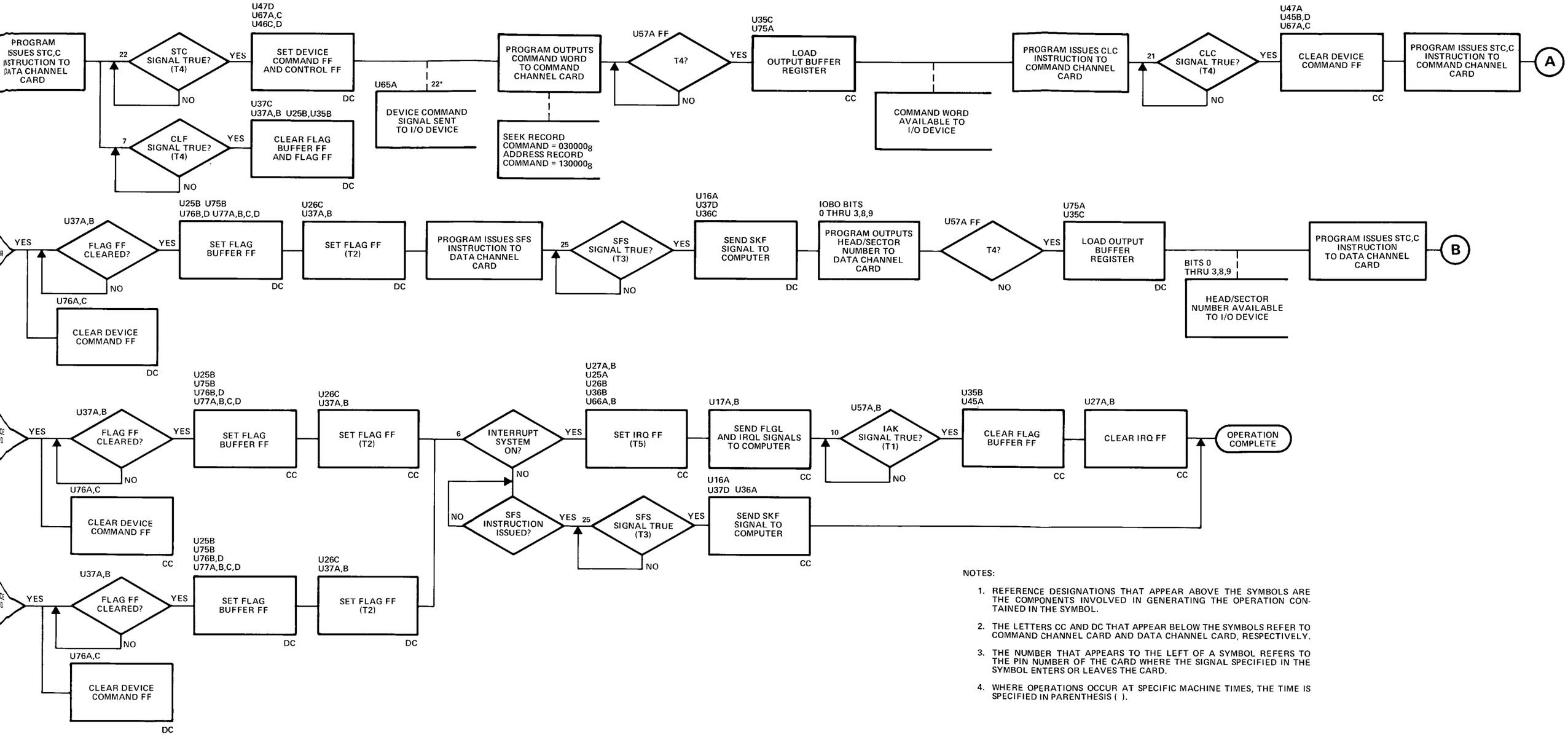
NOTES:

(1) OUTPUT DATA WORD TIMING IS SHOWN. INPUT DATA WORD WILL BE LOADED ONTO THE DATA LINES FROM THE DISC CONTROLLER SIMULTANEOUSLY WITH DEVICE FLAG SIGNAL.

(2) LEADING EDGE TIME OCCURS 100 NANOSECONDS AFTER THE DEVICE FLAG SIGNAL.

Figure 3-3. Signal Timing During DMA Control


START
IOBO BITS 0 THRU 7
PROGRAM OUTPUTS CYLINDER NUMBER TO DATA CHANNEL CARD
U57A FF
T4?
YES
NO
U35A U75A
LOAD OUTPUT BUFFER REGISTER
DC
BITS 0 THRU 7
CYLINDER NUMBER AVAILABLE TO I/O DEVICE
PROGRAM ISSUES STC,C INSTRUCTION TO DATA CHANNEL CARD
22
STC SIGNAL TRUE? (T4)
U47D U67A,C U46C,D
SET DEVICE COMMAND FF AND CONTROL FF
7
CLF SIGNAL TRUE? (T4)
U37C U37A,B U25B,U35B
CLEAR FLAG BUFFER FF AND FLAG FF
U65A
22*
DEVICE COMMAND SIGNAL SENT TO I/O DEVICE
PROGRAM OUTPUTS COMMAND WORD TO COMMAND CHANNEL CARD
SEEK RECORD COMMAND = 030000₈
ADDRESS RECORD COMMAND = 130000₈
U57A FF
T4?
YES
NO
U35C U75A
LOAD OUTPUT BUFFER REGISTER
A
U47D U67A,C U46C,D
22
STC SIGNAL TRUE? (T4)
YES
NO
SET DEVICE COMMAND FF AND CONTROL FF
CC
7
CLF SIGNAL TRUE? (T4)
U37C U25B,U35B U37A,B
CLEAR FLAG BUFFER FF AND FLAG FF
U65A
22*
DEVICE COMMAND SIGNAL SENT TO I/O DEVICE
23*
DATA CHANNEL DEVICE FLAG RECEIVED FROM I/O DEVICE?
U37A,B
FLAG FF CLEARED?
U76A,C
CLEAR DEVICE COMMAND FF
U25B U75B U76B,D U77A,B,C,D
SET FLAG BUFFER FF
U26C U37A,B
SET FLAG FF (T2)
PROGRAM ISSUES SFS INSTRUCTION TO DATA CHANNEL CARD
25
SFS SIGNAL TRUE? (T3)
U16A U37D U36C
SEND SKF SIGNAL TO COMPUTER
B
U47D U67A,C U46C,D
22
STC SIGNAL TRUE? (T4)
SET DEVICE COMMAND FF AND CONTROL FF
DC
7
CLF SIGNAL TRUE? (T4)
U37C U25B,U35B U37A,B
CLEAR FLAG BUFFER FF AND FLAG FF
U65A
22*
DEVICE COMMAND SIGNAL SENT TO I/O DEVICE
23*
COMMAND CHANNEL DEVICE FLAG RECEIVED FROM I/O DEVICE?
U37A,B
FLAG FF CLEARED?
U76A,C
CLEAR DEVICE COMMAND FF
U25B U75B U76B,D U77A,B,C,D
SET FLAG BUFFER FF
U26C U37A,B
SET FLAG FF (T2)
U27A,B U25A U26B U36B U66A,B
6
INTERRUPT SYSTEM ON?
SET IRQ FF (T5)
U17A,B
SEND FLGL AND IRQL SIGNALS TO COMPUTER
SFS INSTRUCTION ISSUED?
SFS SIGNAL TRUE (T3)
U16A U37D U36A
SEND SKF SIGNAL TO COMPUTER
DATA CHANNEL DEVICE FLAG RECEIVED FROM I/O DEVICE?
U37A,B
FLAG FF CLEARED?
U76A,C
CLEAR DEVICE COMMAND FF
U25B U75B U76B,D U77A,B,C,D
SET FLAG BUFFER FF
U26C U37A,B
SET FLAG FF (T2)



NOTES:

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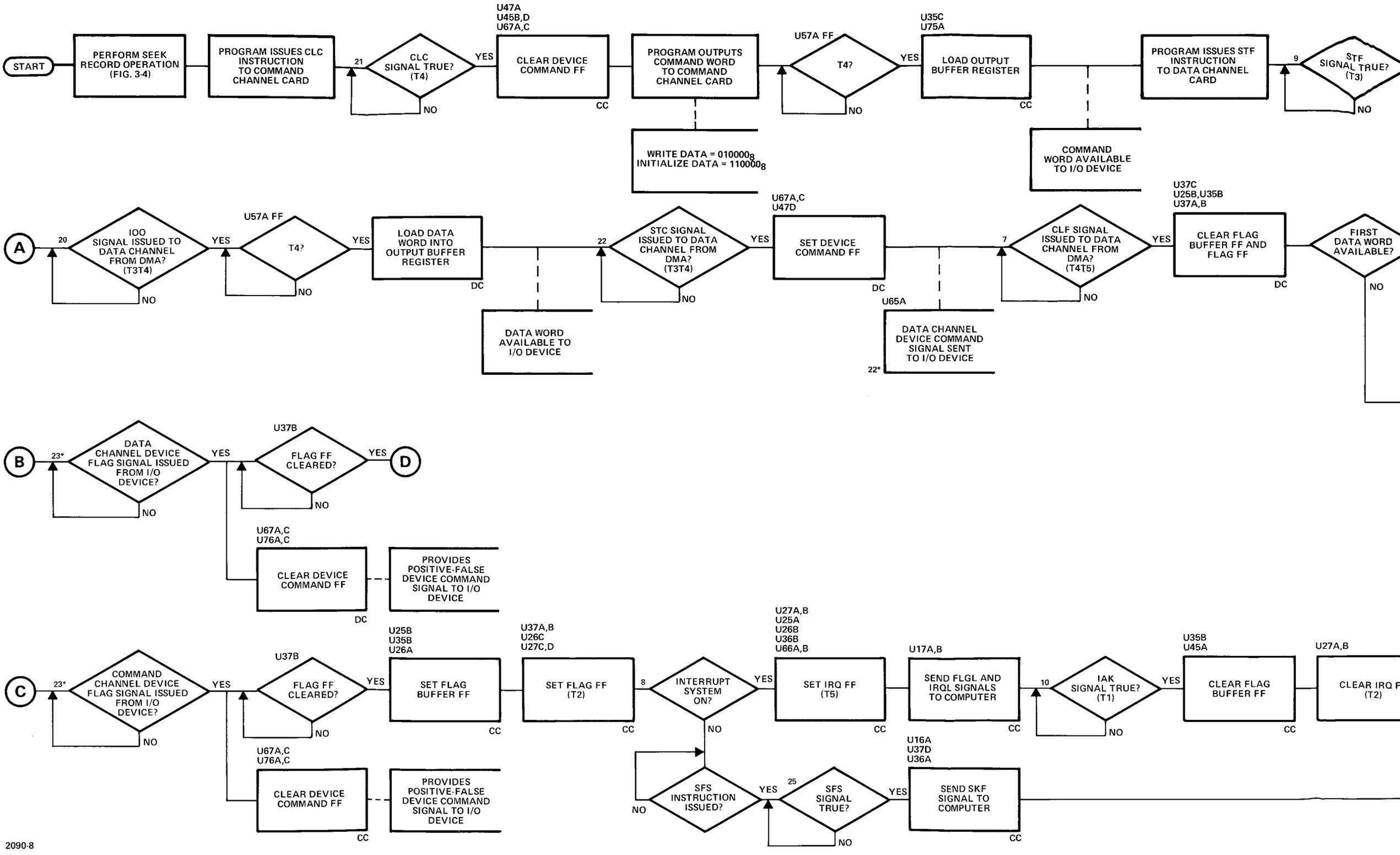
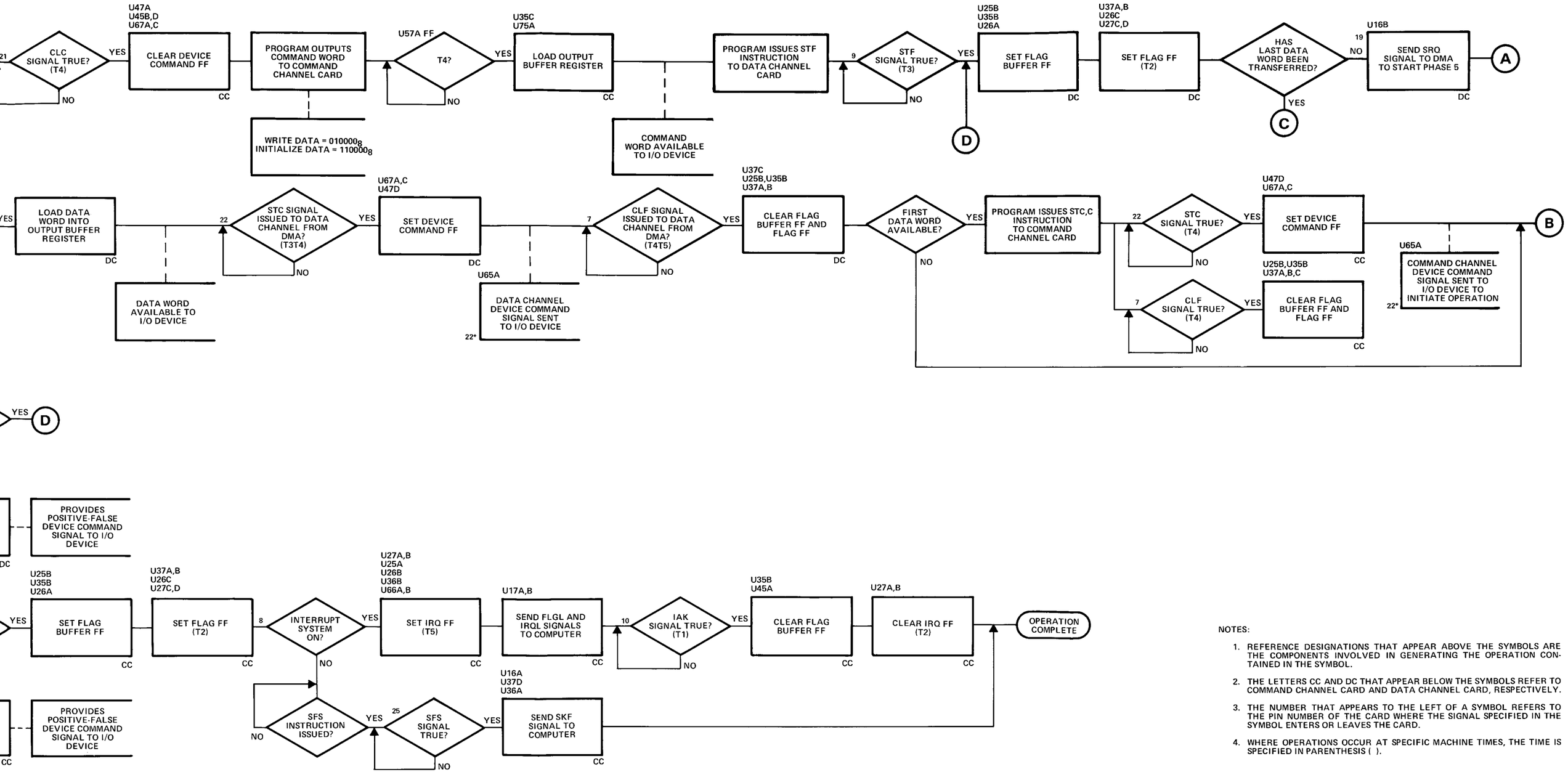
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

Figure 3-4. Seek Record and Address Record Operations Flow Diagram


START
PERFORM SEEK RECORD OPERATION (FIG. 3-4)
PROGRAM ISSUES CLC INSTRUCTION TO COMMAND CHANNEL CARD
21
CLC SIGNAL TRUE? (T4)
NO
YES
U47A
U45B,D
U67A,C
CLEAR DEVICE COMMAND FF
CC
PROGRAM OUTPUTS COMMAND WORD TO COMMAND CHANNEL CARD
WRITE DATA = 010000₈
INITIALIZE DATA = 110000₈
U57A FF
T4?
NO
YES
U35C
U75A
LOAD OUTPUT BUFFER REGISTER
CC
COMMAND WORD AVAILABLE TO I/O DEVICE
PROGRAM ISSUES STF INSTRUCTION TO DATA CHANNEL CARD
9
STF SIGNAL TRUE? (T3)
NO
A
20
IOO SIGNAL ISSUED TO DATA CHANNEL FROM DMA? (T3T4)
NO
YES
U57A FF
T4?
NO
YES
LOAD DATA WORD INTO OUTPUT BUFFER REGISTER
DC
DATA WORD AVAILABLE TO I/O DEVICE
22
STC SIGNAL ISSUED TO DATA CHANNEL FROM DMA? (T3T4)
NO
YES
U67A,C
U47D
SET DEVICE COMMAND FF
DC
U65A
DATA CHANNEL DEVICE COMMAND SIGNAL SENT TO I/O DEVICE
22*
7
CLF SIGNAL ISSUED TO DATA CHANNEL FROM DMA? (T4T5)
NO
YES
U37C
U25B,U35B
U37A,B
CLEAR FLAG BUFFER FF AND FLAG FF
DC
FIRST DATA WORD AVAILABLE?
NO
B
23*
DATA CHANNEL DEVICE FLAG SIGNAL ISSUED FROM I/O DEVICE?
NO
YES
U37B
FLAG FF CLEARED?
NO
YES
D
U67A,C
U76A,C
CLEAR DEVICE COMMAND FF
DC
PROVIDES POSITIVE-FALSE DEVICE COMMAND SIGNAL TO I/O DEVICE
C
23*
COMMAND CHANNEL DEVICE FLAG SIGNAL ISSUED FROM I/O DEVICE?
NO
YES
U37B
FLAG FF CLEARED?
NO
YES
U25B
U35B
U26A
SET FLAG BUFFER FF
CC
U37A,B
U26C
U27C,D
SET FLAG FF (T2)
CC
8
INTERRUPT SYSTEM ON?
NO
YES
U27A,B
U25A
U26B
U36B
U66A,B
SET IRQ FF (T5)
CC
U17A,B
SEND FLGL AND IRQL SIGNALS TO COMPUTER
CC
10
IAK SIGNAL TRUE? (T1)
NO
YES
U35B
U45A
CLEAR FLAG BUFFER FF
CC
U27A,B
CLEAR IRQ F
(T2)
U67A,C
U76A,C
CLEAR DEVICE COMMAND FF
CC
PROVIDES POSITIVE-FALSE DEVICE COMMAND SIGNAL TO I/O DEVICE
NO
SFS INSTRUCTION ISSUED?
YES
25
SFS SIGNAL TRUE?
NO
YES
U16A
U37D
U36A
SEND SKF SIGNAL TO COMPUTER
CC
2090-8



NOTES:

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2. THE LETTERS CC AND DC THAT APPEAR BELOW THE SYMBOLS REFER TO COMMAND CHANNEL CARD AND DATA CHANNEL CARD, RESPECTIVELY.
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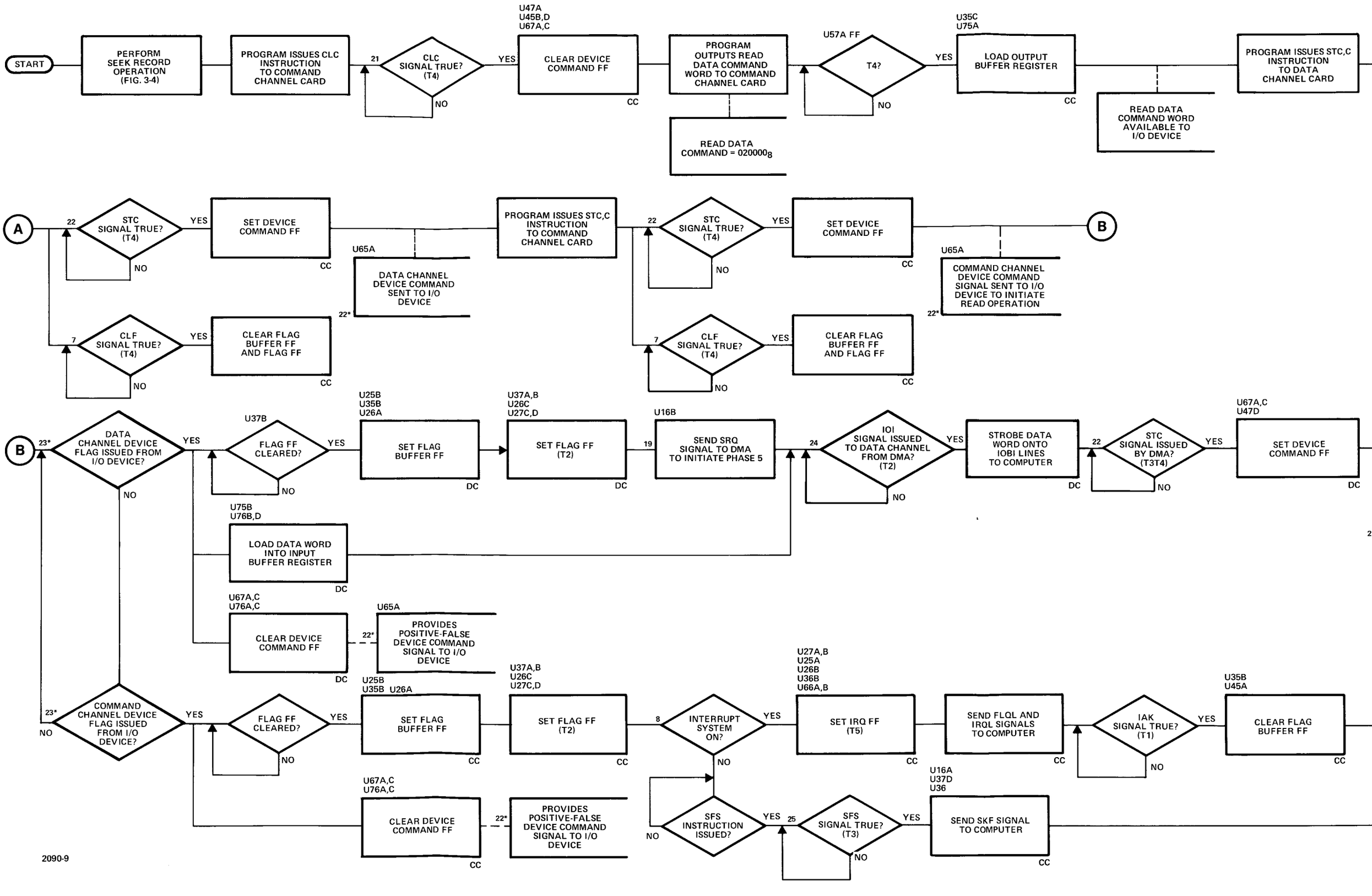
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

Figure 3-5. Write Data and Initialize Data Operations Flow Diagram


START
PERFORM SEEK RECORD OPERATION (FIG. 3-4)
PROGRAM ISSUES CLC INSTRUCTION TO COMMAND CHANNEL CARD
21
CLC SIGNAL TRUE? (T4)
NO
YES
U47A
U45B,D
U67A,C
CLEAR DEVICE COMMAND FF
CC
PROGRAM OUTPUTS READ DATA COMMAND WORD TO COMMAND CHANNEL CARD
READ DATA COMMAND = 020000$_8$
U57A FF
T4?
NO
YES
U35C
U75A
LOAD OUTPUT BUFFER REGISTER
CC
READ DATA COMMAND WORD AVAILABLE TO I/O DEVICE
PROGRAM ISSUES STC,C INSTRUCTION TO DATA CHANNEL CARD
A
22
STC SIGNAL TRUE? (T4)
NO
YES
SET DEVICE COMMAND FF
CC
U65A
DATA CHANNEL DEVICE COMMAND SENT TO I/O DEVICE
22*
7
CLF SIGNAL TRUE? (T4)
NO
YES
CLEAR FLAG BUFFER FF AND FLAG FF
CC
PROGRAM ISSUES STC,C INSTRUCTION TO COMMAND CHANNEL CARD
22
STC SIGNAL TRUE? (T4)
NO
YES
SET DEVICE COMMAND FF
CC
U65A
COMMAND CHANNEL DEVICE COMMAND SIGNAL SENT TO I/O DEVICE TO INITIATE READ OPERATION
22*
7
CLF SIGNAL TRUE? (T4)
NO
YES
CLEAR FLAG BUFFER FF AND FLAG FF
CC
B
U25B
U35B
U37A,B
U26C
U67A,C
B
23*
DATA CHANNEL DEVICE FLAG ISSUED FROM I/O DEVICE?
NO
YES
U37B
FLAG FF CLEARED?
NO
YES
U26A
SET FLAG BUFFER FF
DC
U27C,D
SET FLAG FF (T2)
DC
19
U16B
SEND SRQ SIGNAL TO DMA TO INITIATE PHASE 5
U75B
U76B,D
LOAD DATA WORD INTO INPUT BUFFER REGISTER
DC
U67A,C
U76A,C
CLEAR DEVICE COMMAND FF
DC
22*
U65A
PROVIDES POSITIVE-FALSE DEVICE COMMAND SIGNAL TO I/O DEVICE
24
IOI SIGNAL ISSUED TO DATA CHANNEL FROM DMA? (T2)
NO
YES
STROBE DATA WORD ONTO IOBI LINES TO COMPUTER
DC
22
STC SIGNAL ISSUED BY DMA? (T3T4)
NO
YES
U47D
SET DEVICE COMMAND FF
DC
22*
23*
COMMAND CHANNEL DEVICE FLAG ISSUED FROM I/O DEVICE?
NO
YES
FLAG FF CLEARED?
NO
YES
U25B
U35B
U26A
SET FLAG BUFFER FF
CC
U37A,B
U26C
U27C,D
SET FLAG FF (T2)
CC
8
INTERRUPT SYSTEM ON?
NO
YES
U27A,B
U25A
U26B
U36B
U66A,B
SET IRQ FF (T5)
CC
SEND FLOL AND IROL SIGNALS TO COMPUTER
CC
IAK SIGNAL TRUE? (T1)
NO
YES
U35B
U45A
CLEAR FLAG BUFFER FF
CC
U67A,C
U76A,C
CLEAR DEVICE COMMAND FF
CC
22*
PROVIDES POSITIVE-FALSE DEVICE COMMAND SIGNAL TO I/O DEVICE
NO
SFS INSTRUCTION ISSUED?
YES
25
SFS SIGNAL TRUE? (T3)
NO
YES
U16A
U37D
U36
SEND SKF SIGNAL TO COMPUTER
CC
2090-9

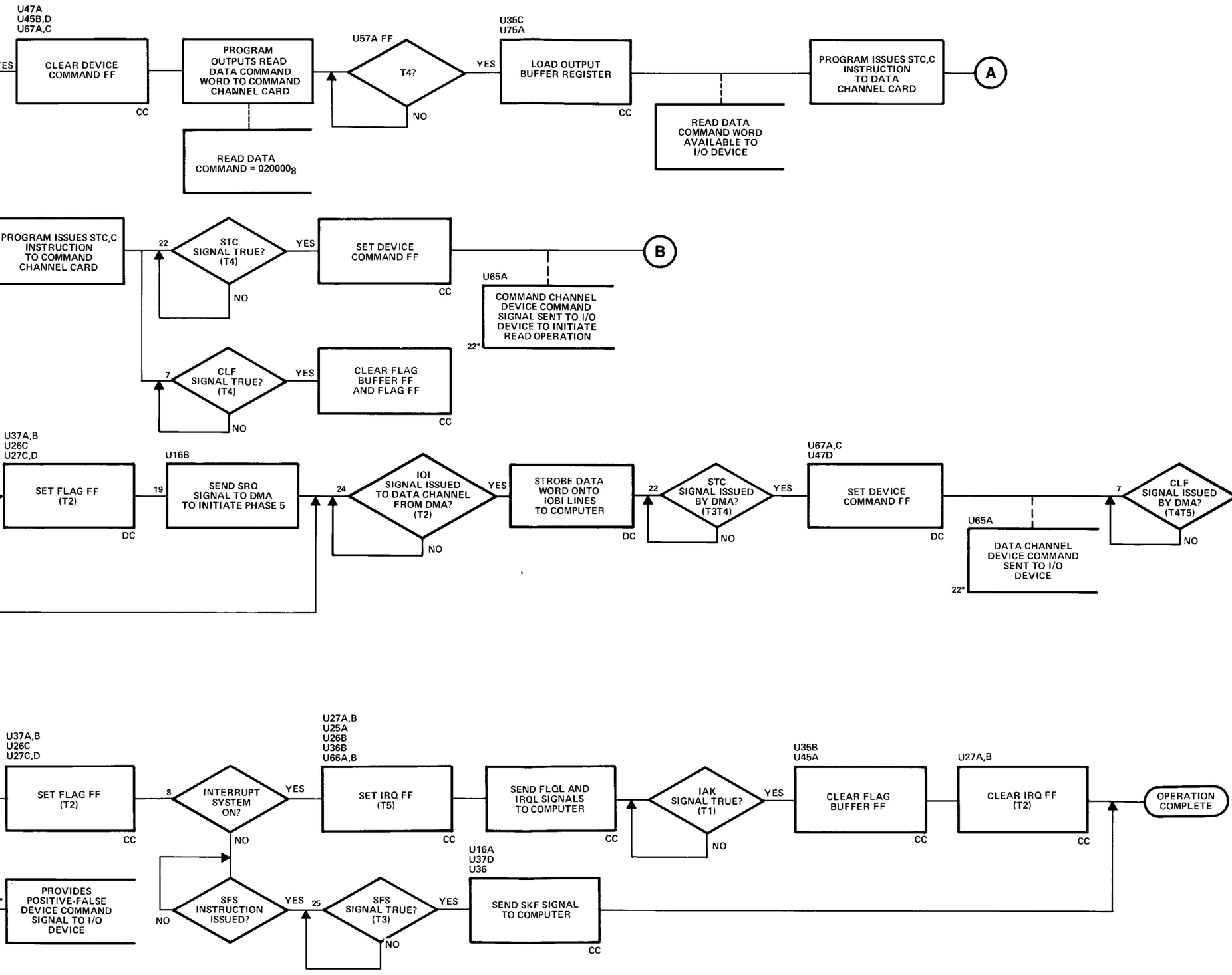


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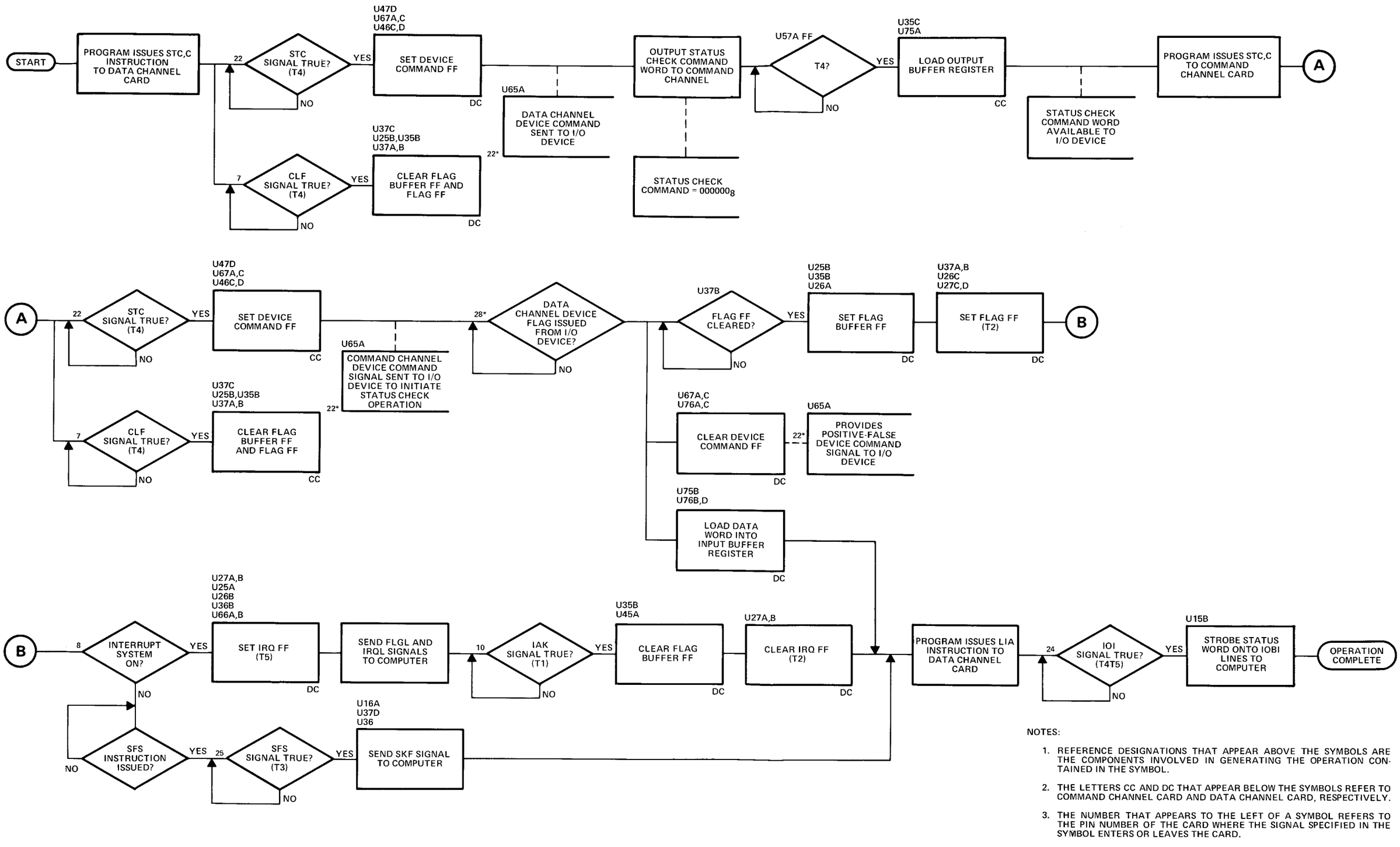
Figure 3-6. Read Data Operation Flow Diagram



2090-10

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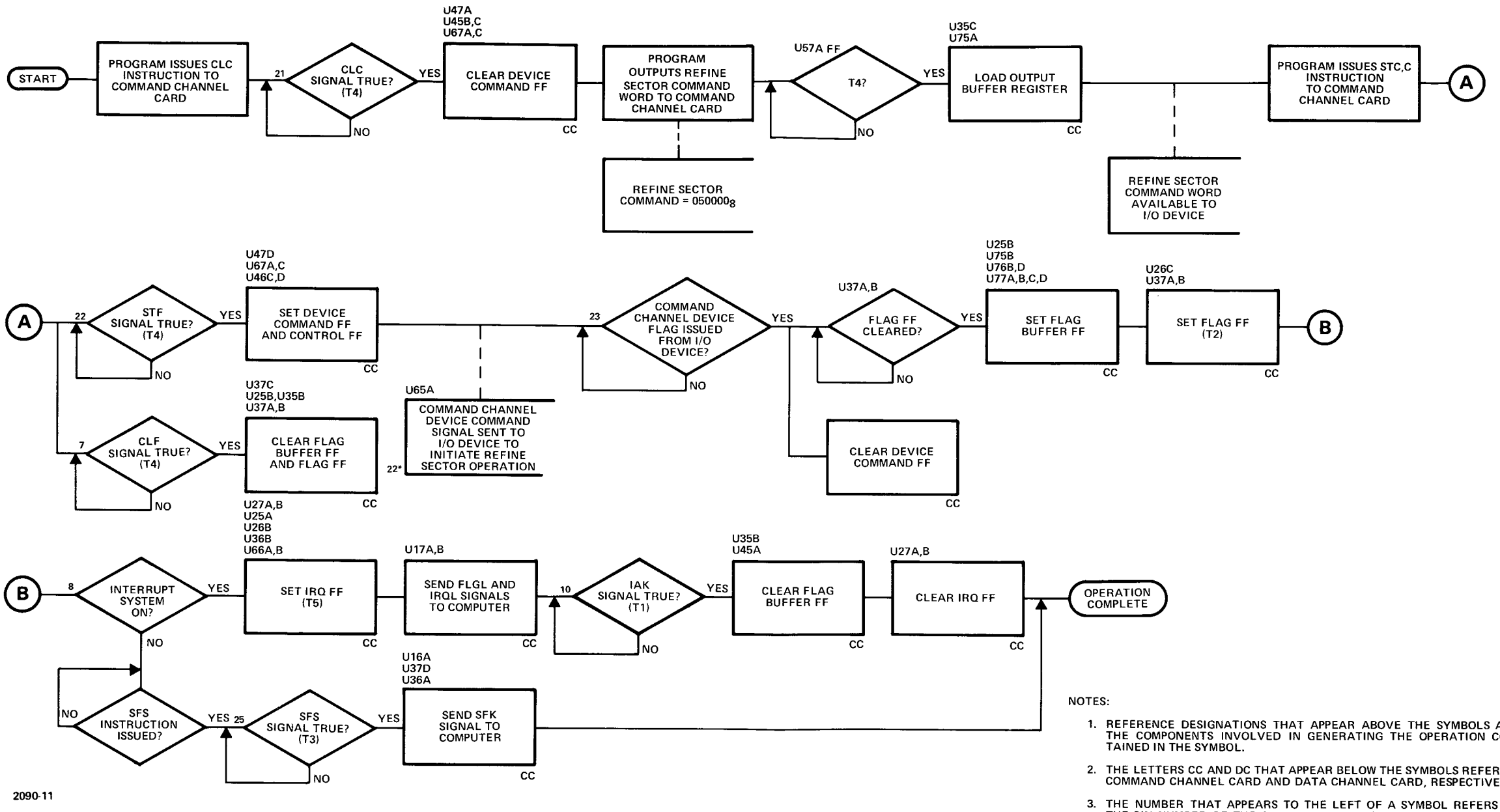
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

Figure 3-7. Status Check Operation Flow Diagram



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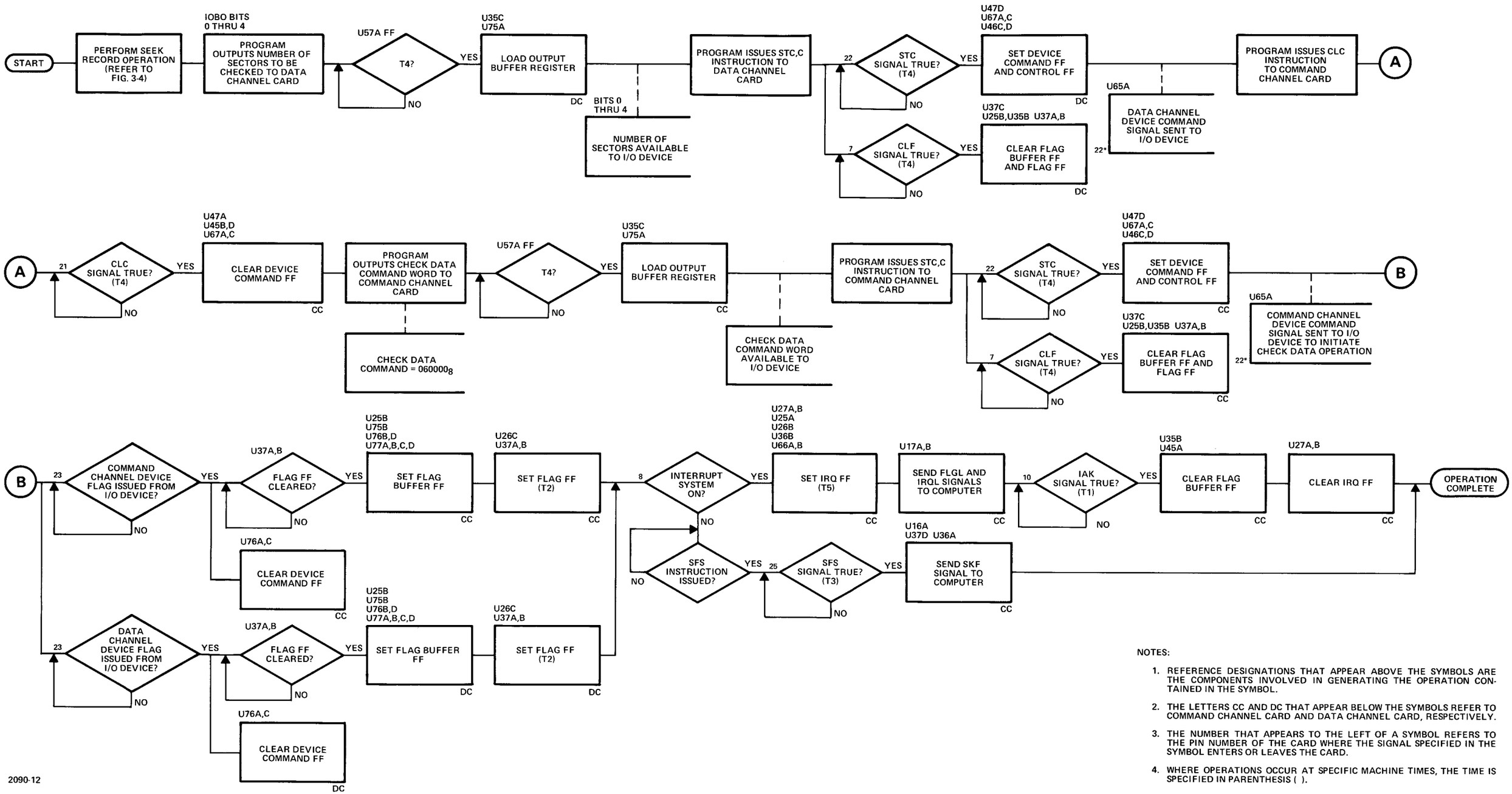
3. THE NUMBER THAT APPEARS TO THE LEFT OF A SYMBOL REFERS TO THE PIN NUMBER OF THE CARD WHERE THE SIGNAL SPECIFIED IN THE SYMBOL ENTERS OR LEAVES THE CARD.

Figure 3-8. Refine Sector Operation Flow Diagram



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4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

Figure 3-9. Check Data Operation Flow Diagram

SECTION IV
MAINTENANCE

4-1 INTRODUCTION.

4-2. This section contains information on diagnostics and troubleshooting for the cartridge disc interface kit.

4-3. PREVENTIVE MAINTENANCE.

4-4. Detailed preventive maintenance procedures and schedules are provided in Volume Two for the computer. There are no separate preventive maintenance procedures to be performed on the interface kit.

4-5. DIAGNOSTICS.

4-6. Each interface card may be checked using the Diagnostic Operating Procedures, part no. 12849-90002, contained in the Manual of Diagnostics. The diagnostic program consists of a general diagnostic covering basic I/O test, data buffer test, and control signals test. Test Connectors A and B, part no. 12849-60003 and 12849-60004, are used during the diagnostic test procedure to couple certain output and input signals of the interface card together. Wire lists for the two test connectors are contained in tables 4-1 and 4-2.

Table 4-1. Test Connector A (12849-60003) Wire List

PINS			PINS		
FROM	TO	SIGNAL	FROM	TO	SIGNAL
A	1	Bit 0 to Bit 0	L	10	Bit 9 to Bit 9
B	2	Bit 1 to Bit 1	M	11	Bit 10 to Bit 10
C	3	Bit 2 to Bit 2	N	12	Bit 11 to Bit 11
D	4	Bit 3 to Bit 3	P	13	Bit 12 to Bit 12
E	5	Bit 4 to Bit 4	R	14	Bit 13 to Bit 13
F	6	Bit 5 to Bit 5	S	15	Bit 14 to Bit 14
H	7	Bit 6 to Bit 6	T	16	Bit 15 to Bit 15
J	8	Bit 7 to Bit 7	Z	23	Device Command to Device Flag
K	9	Bit 8 to Bit 8			

Table 4-2. Test Connector B (12849-60004) Wire List

PINS			PINS		
FROM	TO	SIGNAL	FROM	TO	SIGNAL
17	1	ORL to Bit 0	X	5	CTL to Bit 4
18	2	DIR to Bit 1	V	A	Bit 0 to RORL
U	3	FLG to Bit 2	Y	20	CRS to RDIR
W	4	PON to Bit 3	Z	23	Device Command to Device Flag

4-7. The entire cartridge disc system may be checked using the Cartridge Disc Memory Diagnostic Operating Procedures, part no. 12557-90003, also contained in the Manual of Diagnostics.

4-8. TROUBLESHOOTING.

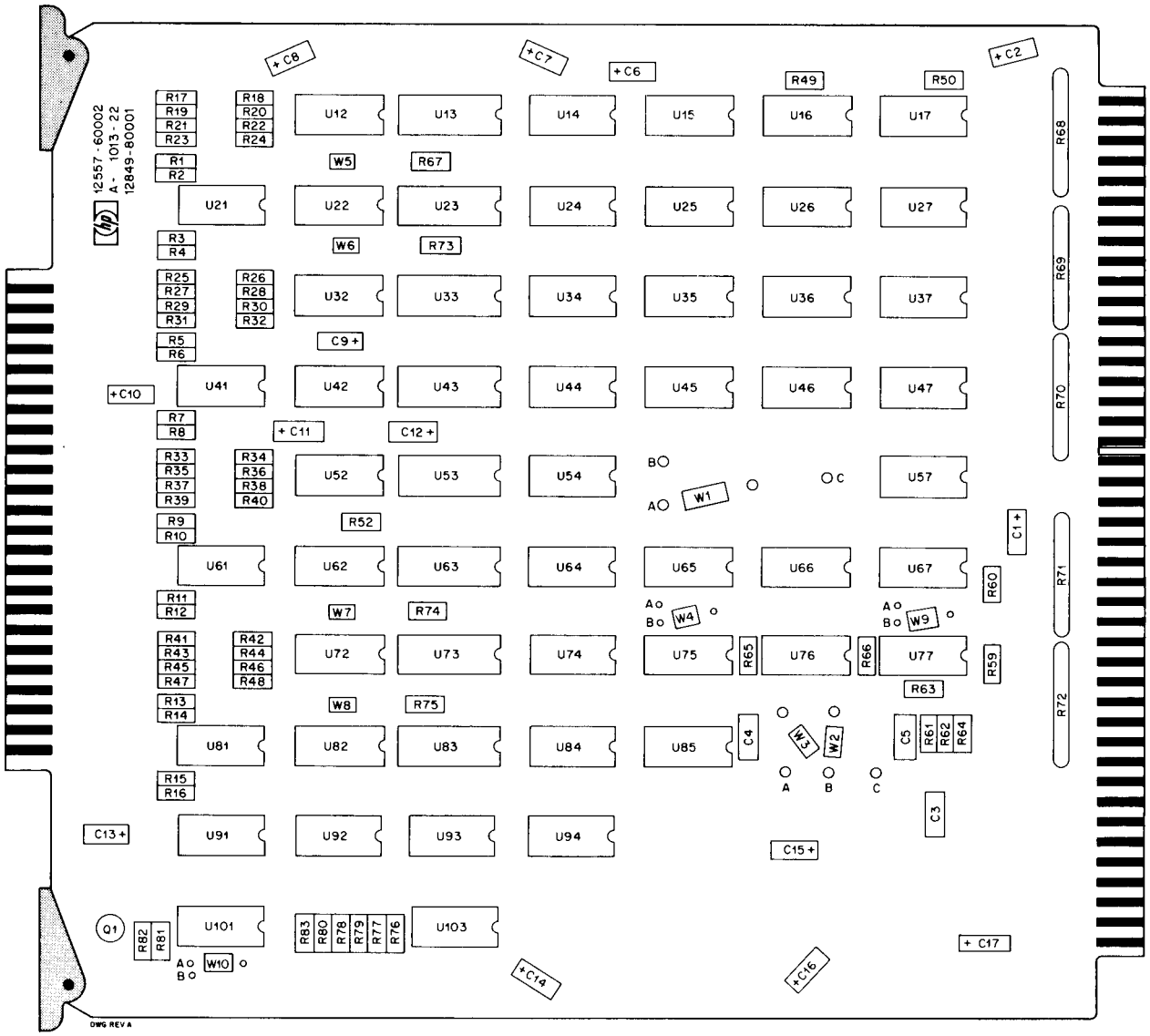
4-9. Troubleshooting for the interface cards is accomplished by performing the diagnostic tests in the diagnostic program and analyzing the error halts that occur as the test is being run. To further isolate the trouble, refer to the schematic and parts location diagrams in figures 4-1 and 4-2.

4-10. Tables 4-3 and 4-4 contain parts lists for the two interface cards with the parts listed in alphanumeric order by reference designation. Figure 4-3 contains logic diagrams and pin locations for the integrated circuits used on the interface cards. Table 4-5 gives the integrated circuit input levels, output levels, and delay times which correspond to the integrated circuit characteristic number shown below each diagram in figure 4-3.

4-11. Table 2-2 contains a list of connector pin functions for the interconnecting cable assembly. Replaceable parts for the cable assembly are contained in table 5-1; an exploded view of the cable assembly is shown in figure 5-1.

Table 4-3. Data Channel Card (12557-60002) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2,C6 thru C17	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	28480	0180-0197
C3	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153
C4,5	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154
Q1	1854-0094	Transistor, Si, NPN	07263	2N3646
R1 thru R16,52,63,80	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F
R17,19,21,23,25,27,29,31,33,35, 37,39,41,43,45,47,49,59,65, 66,76,78	0757-0407	Resistor, Fxd, Flm, 200 ohms, 1%, 1/8W	14674	MF4CD2000F
R18,20,22,24,26,28,30,32,34,36, 38,40,42,44,46,48,50,60, 77,79	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F
R61,62	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	14674	MF4CD1000F
R64	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R67,R73 thru R75	0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	14674	MF4CD1002F
R68 thru R72	1810-0020	Resistor Network, (7 fxd flm resistors)	28480	1810-0020
R81	0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	19701	MF4CD4640F
R82	0757-0418	Resistor, Fxd, Flm, 619 ohms, 1%, 1/8W	14674	MF4CD6190F
R83	0757-0438	Resistor, Fxd, Flm, 5.11k, 1%, 1/8W	14674	MF4CD5111F
U12,26,27,32,37,U45 thru U47, 52,66,72,76,77,85	1820-0054	Integrated Circuit, TTL	01295	SN4343
U13,23,33,43,53,63,73,83	1820-0301	Integrated Circuit, TTL	01295	SN4463
U14 thru U17,34,44,54,64,74, 84,91	1820-0956	Integrated Circuit, CTL	07263	SL3459
U21,22,41,42,61,62,81,82	1820-0348	Integrated Circuit, DTL	01295	SN4506
U25	1820-0069	Integrated Circuit, TTL	56289	USN7420A
U35,36,67	1820-0068	Integrated Circuit, TTL	01295	SN4343
U57,93	1820-0077	Integrated Circuit, TTL	56289	USN7474A
U65,75,92,94	1820-0071	Integrated Circuit, TTL	56289	USN7440A
U101	1820-0140	Integrated Circuit, TTL	04718	SC7513PK
U103	1820-0141	Integrated Circuit, TTL	04713	SC7514PK
W1 thru W10	8159-0005	Jumper Wire	28480	8159-0005


12557-60002
A- 1013-22
12849-80001
+C8
+C7
+C6
+C2
R49
R50
R68
R69
R70
R71
R72
R60
R59
R63
R52
R67
R73
R74
R75
W1
W2
W3
W4
W5
W6
W7
W8
W9
W10
C9+
+C10
+C11
C12+
C13+
C15+
+C14
+C16
+C17
C1+
C3
C4
C5
Q1
DWG REV A

DATA CHANNEL INTERFACE (12557-60002, REV. 1013)

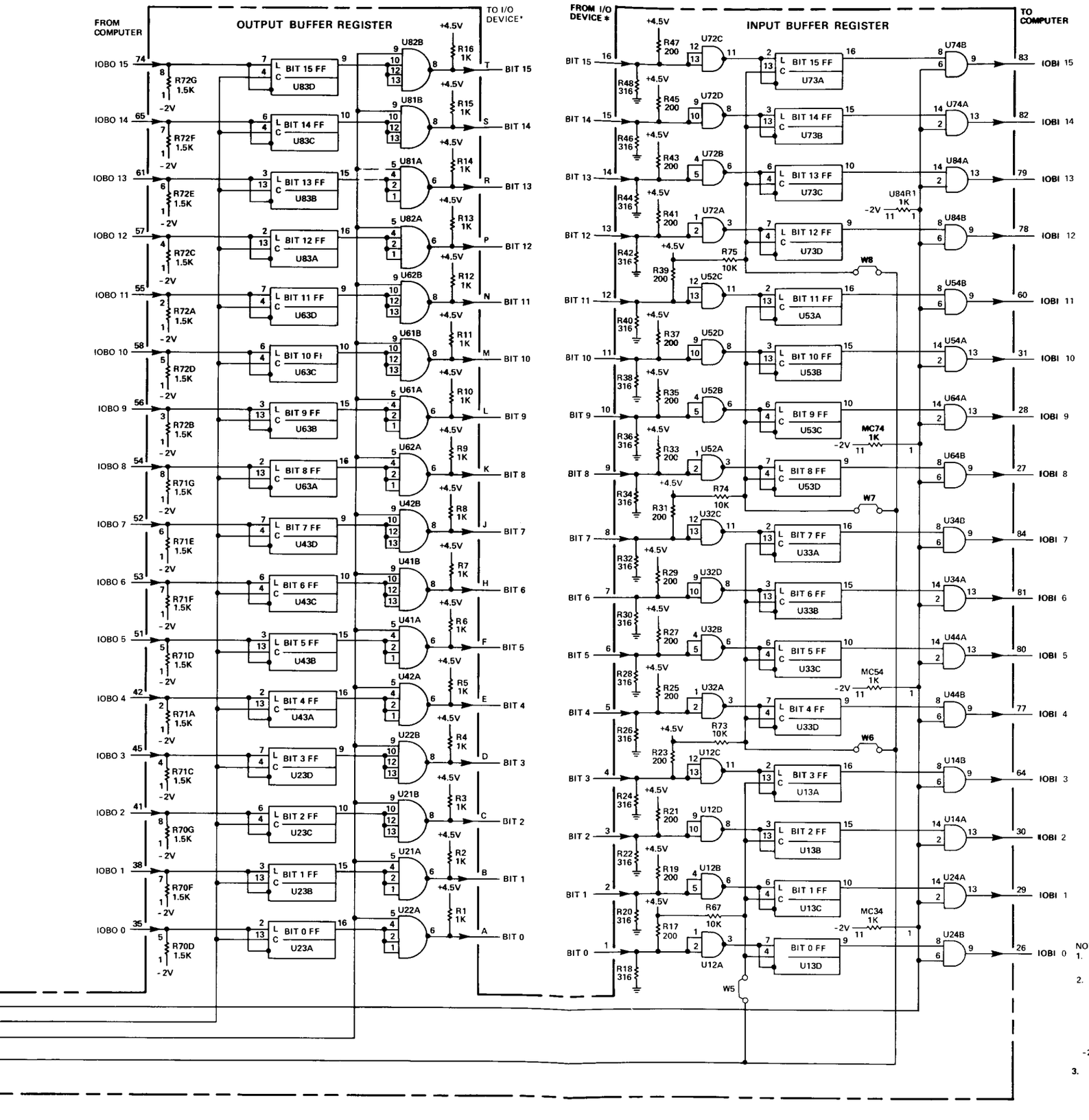
ENF 46 — R71B 1.5K -2V — U27C — U27D
POPIO(B) 17 — R69C 1.5K -2V — U26D
STF 9 — R68D 1.5K -2V — U26A
CLF 7 — R68B 1.5K -2V — U37C
LSCM 14, LSCL 16, IOG(B) 15 — U35A — R68G 1.5K, R69B 1.5K, R69A 1.5K — -2V — U47B, U46B
IEN 8
SFS 25
SFC 5 — R68C 1.5K, R70A 1.5K, R68A 1.5K — -2V
IOO 20 — R69D 1.5K -2V — U35C
STC 22 — R69F 1.5K -2V — U47D
CLC 21 — R69E 1.5K -2V — U47A
CRS 13 — R68F 1.5K -2V — U45C
T3 11 — R70B 1.5K -2V — U47C — +4.5V — U57A (D, C)
+4.5V 39, 40 — C1,C2,C6,C8 THRU C15 2.2 UF
-2V 47, 48 — C7, C16, C17 2.2 UF
GND 85, 86
*DEVICE FLAG 23 AA — R59 200 — U77A — R60 316 — R61 100 — C3 0.001 UF — R62 100 — R64 1.47K

FLAG BUFFER FF: U25B, U35B
FLAG FF: U37A, U37B
U26C
U66A, U66B
U36B, U26B
U25A
IRQ FF: U27A, U27B
U15A
U36A, U36C, U37D
U75A
U77B
U45B, U45D
CONTROL FF: U46C, U46D
PARTY LINE TIMING FF: U66D, U66C
U67B, U85A
U94B
U101A
U101B
DEVICE COMMAND FF: U67A, U67C
W9B, W9A
U76C
W2C PULSE
W4A PULSE +FALSE
W4B NORMAL UNGATED
U65B
U76A — R66 200 — C5 0.0022 UF
U85C — W2A, W2B, W3A, W3B
R63 1K
U77C, U77D
U76B — R65 200 — C4 0.0022 UF
U76D
U75B
W1C PULSE +FALSE
W1A +FALSE
W1B +TRUE
U65A

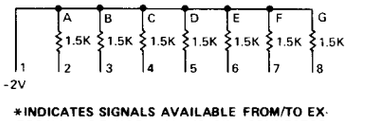
SIR 32 — R70E 1.5K -2V
PRH 23 — R69G 1.5K -2V
IOI 24
IAK 10 — R68E 1.5K -2V
+4.5V — R50 316
+4.5V — R49 200
U45A
U15B
U85A
U15R1 1K -2V
U16R2 1K -2V
U94A
+4.5V — R78 200
R79 316
U103D
U92B
U103C
DIR — U93B
+4.5V — R76 200
R77 316
U92A
U103A
U103B
R80 1K +4.5V
U91B
U91R2 1K -2V
W10A
W10B
R83 5.11K +4.5V
Q1
R81 464 -2V
R82 619
ORL — U93A
+4.5V — R52 1K
U15R2 1K -2V

FLGL 4
IRQL 6
PRL 3
SKF 12
SRQ 19
U* FLG
20* RDIR
18* DIR
V* RORL
17* ORL
66 PON
W* PON
24* GND
BB*
X* CTL
19* POPIO(B)
Y* CRS
22* DEVICE COMMAND
Z*

DWG REV. A



NOTES:
1. ALL LOGIC IS POSITIVE – TRUE
2. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R68 THRU R72:

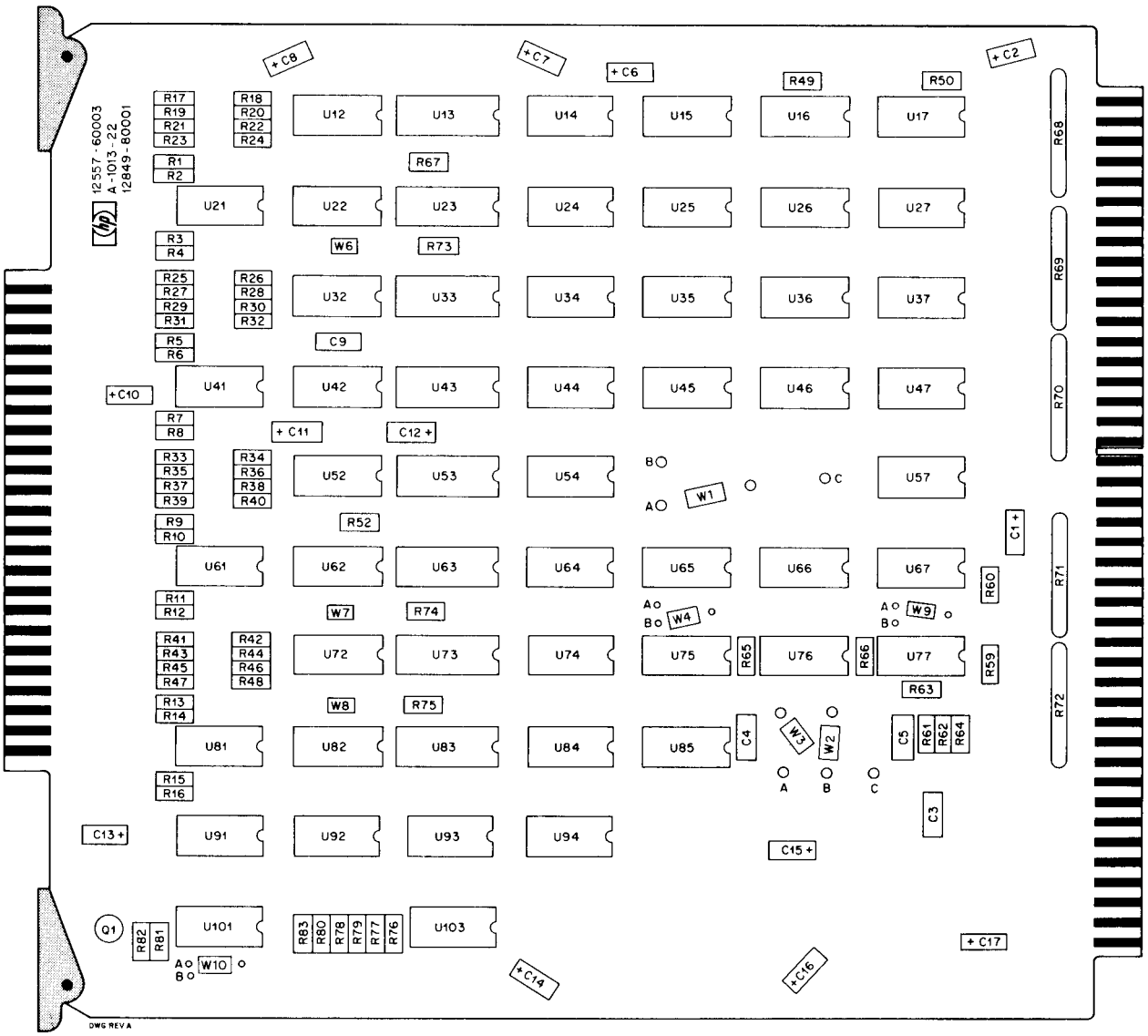


3. *INDICATES SIGNALS AVAILABLE FROM/TO EXTERNAL DEVICE VIA 48-PIN CONNECTOR. ACTUAL SIGNALS USED DEPENDS UPON EXTERNAL DEVICE. ALL OTHER SIGNALS ARE FROM/TO COMPUTER VIA 86-PIN CONNECTOR.

Figure 4-1. Data Channel Card (12557-60002), Schematic and Parts Location Diagrams

Table 4-4. Command Channel Card (12557-60003) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2,C6 thru C17	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	28480	0180-0197
C3	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153
C4,5	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154
Q1	1854-0094	Transistor, Si, NPN	07263	2N3646
R1 thru R16,52,63,80	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F
R17,19,21,23,25,27,29,31,33,35, 37,39,41,43,45,47,49,59,65, 66,67,78	0757-0407	Resistor, Fxd, Flm, 200 ohms, 1%, 1/8W	14674	MF4CD2000F
R18,20,22,24,26,28,30,32,34,36, 38,40,42,44,46,48,50,60, 77,79	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F
R61,62	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	14674	MF4CD1000F
R64	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R67,R73 thru R75	0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	14674	MF4CD1002F
R68 thru R72	1810-0020	Resistor Network, (7 fxd flm resistors)	28480	1810-0020
R81	0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	19701	MF4CD4640F
R82	0757-0418	Resistor, Fxd, Flm, 619 ohms, 1%, 1/8W	14674	MF4CD6190F
R83	0757-0438	Resistor, Fxd, Flm, 5.11k, 1%, 1/8W	14674	MF4CD5111F
U12,26,27,32,37,U45 thru U47, 52,66,72,76,77,85	1820-0054	Integrated Circuit, TTL	01295	SN4343
U13,23,33,43,53,63,73,83	1820-0301	Integrated Circuit, TTL	01295	SN4463
U14 thru U17,34,44,54,64,74, 84,91	1820-0956	Integrated Circuit, CTL	07263	SL3459
U21,22,41,42,61,62,81,82	1820-0348	Integrated Circuit, DTL	01295	SN4506
U25	1820-0069	Integrated Circuit, TTL	56289	USN7420A
U35,36,67	1820-0068	Integrated Circuit, TTL	01295	SN4343
U57,93	1820-0077	Integrated Circuit, TTL	56289	USN7474A
U65,75,92,94	1820-0071	Integrated Circuit, TTL	56289	USN7440A
U101	1820-0140	Integrated Circuit, TTL	04713	SC7513PK
U103	1820-0141	Integrated Circuit, TTL	04713	SC7514PK
W1 thru W10	8159-0005	Jumper Wire	28480	8159-0005


12557 - 60003
A -1013 - 22
12849 - 80001
DWG REV A
+C8
+C7
+C6
+C2
R49
R50
R68
R69
R70
R71
R72
R60
R59
R63
R65
R66
C1 +
C3
C4
C5
C9
C10
C11
C12 +
C13 +
C14
C15 +
C16
C17
R52
R67
R73
R74
R75
W1
W2
W3
W4
W6
W7
W8
W9
W10
Q1
U12
U13
U14
U15
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R1
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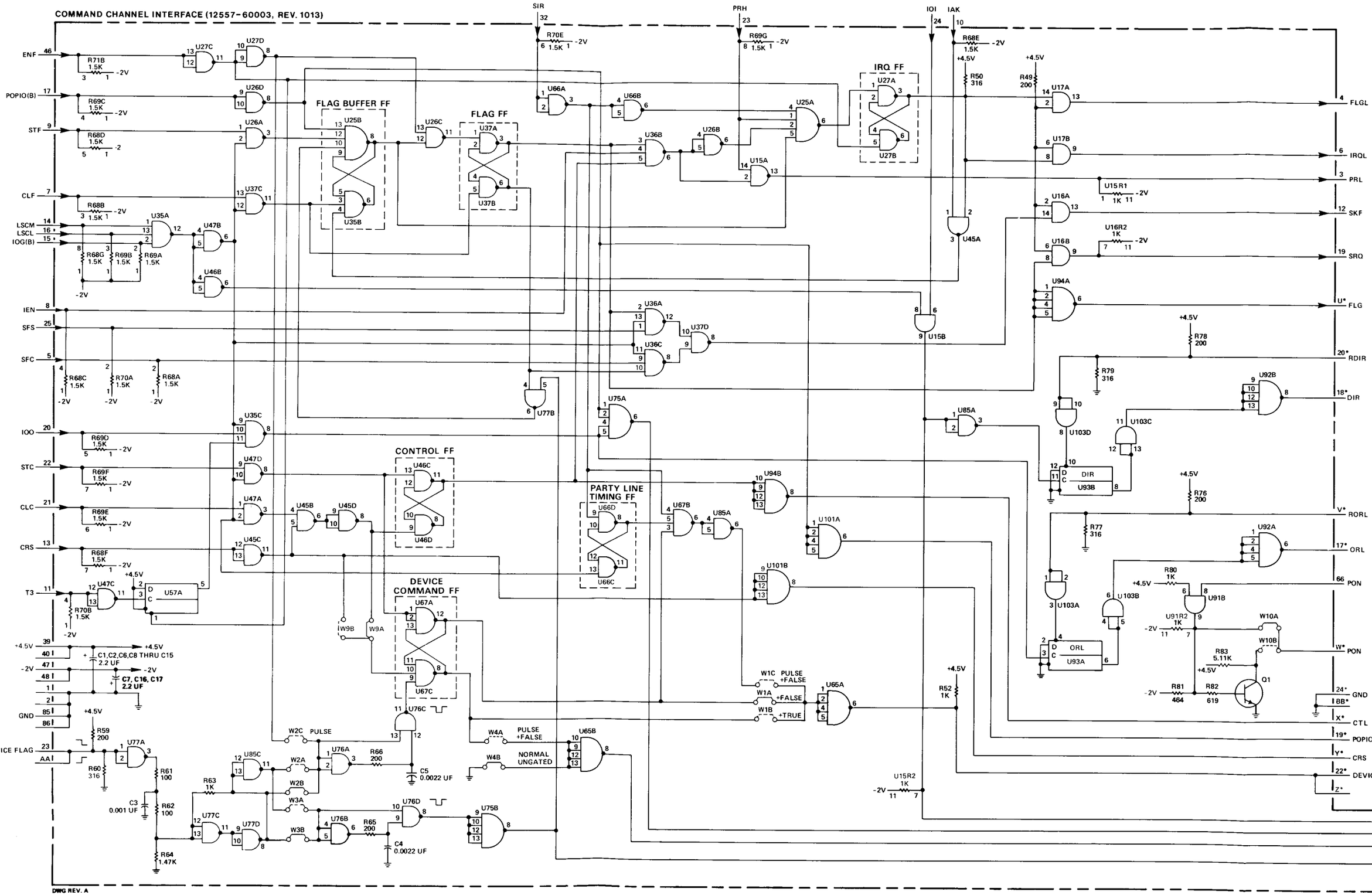
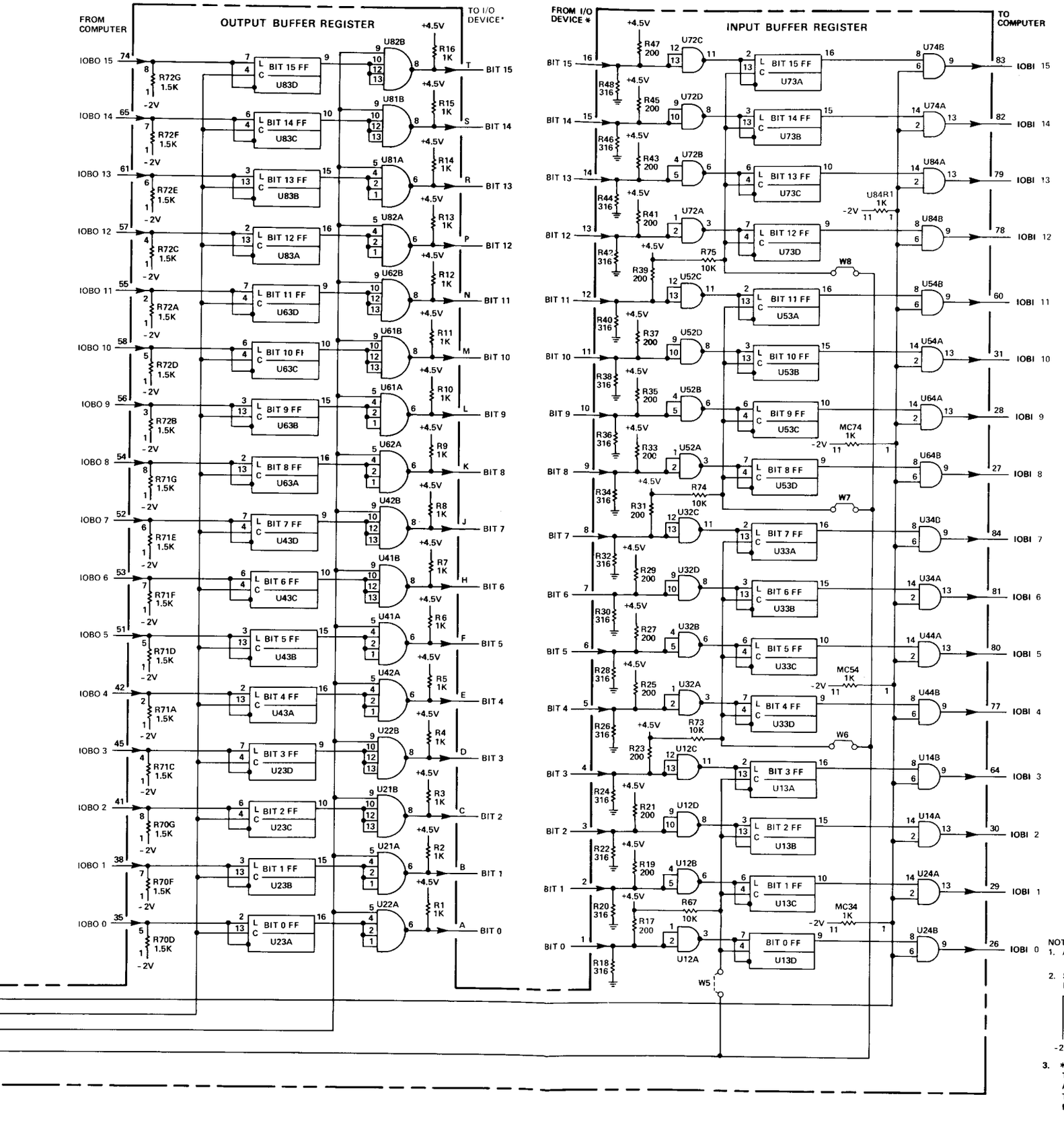
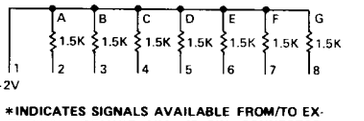
R44
R45
R46
R47
R48
R61
R62
R64
R76
R77
R78
R79
R80
R81
R82
R83
A
B
C

COMMAND CHANNEL INTERFACE (12557-60003, REV. 1013)



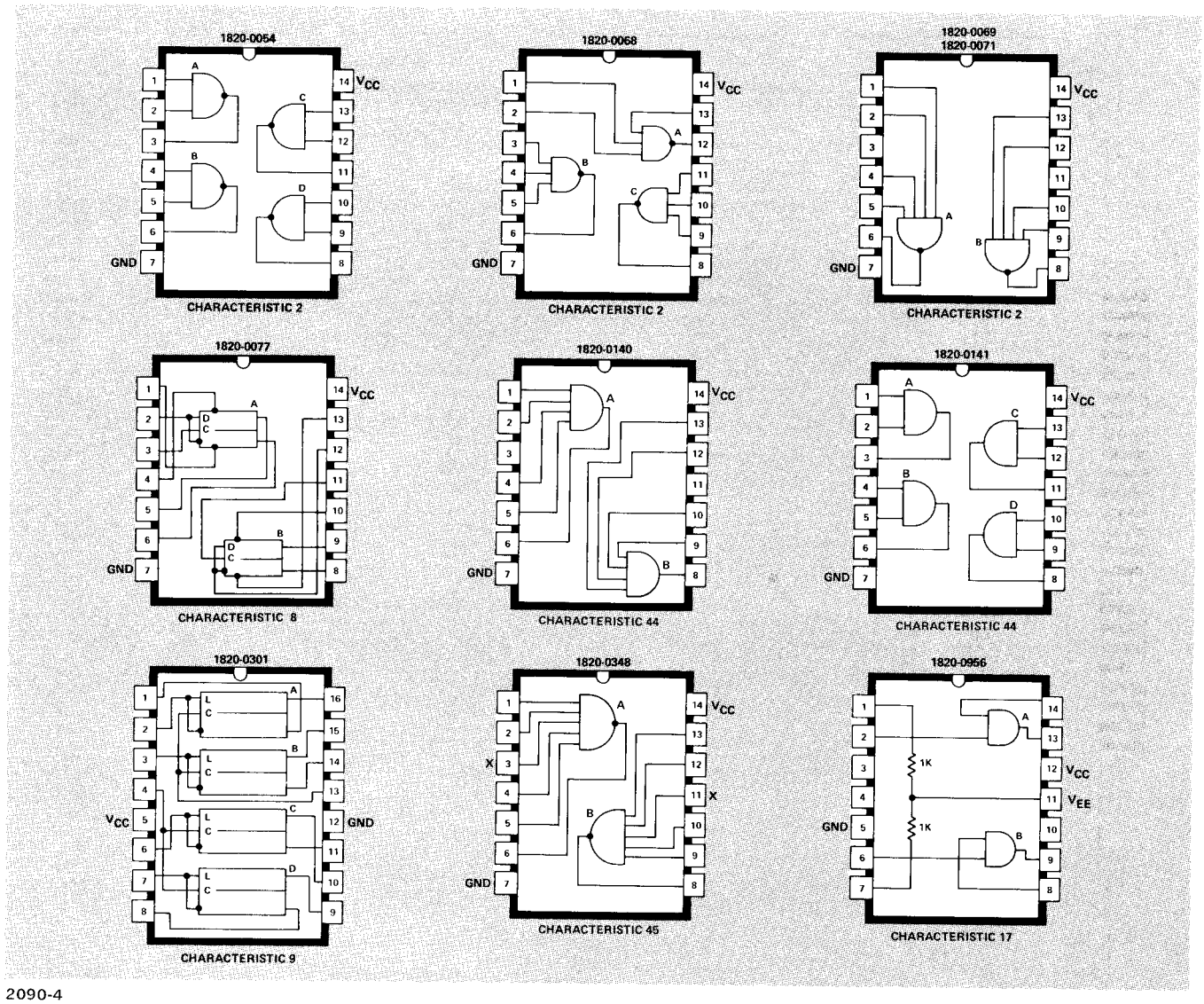


NOTES:
1. ALL LOGIC IS POSITIVE – TRUE
2. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R68 THRU R72:



3. *INDICATES SIGNALS AVAILABLE FROM/TO EXTERNAL DEVICE VIA 48-PIN CONNECTOR. ACTUAL SIGNALS USED DEPENDS UPON EXTERNAL DEVICE. ALL OTHER SIGNALS ARE FROM/TO COMPUTER VIA 68-PIN CONNECTOR.

Figure 4-2. Command Channel Card (12557-60003), Schematic and Parts Location Diagrams



2090-4

Figure 4-3. Integrated Circuit Diagrams

Table 4-5. Integrated Circuit Characteristics

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	PROPAGATION DELAY (MAX)	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
8	+2.0	+0.8	+2.4	+0.4	Logic 1	35	50
9	+2.0	+0.8	+2.4	+0.4	Logic 1	40	25
17	+1.25	+0.5	+2.25	-0.36	Logic 0	18	18
44	+1.8	+1.1	+2.5	+0.4	Logic 1	15	15
45	+2.0	+1.1	Note 1	+0.5	Logic 1	50	35

NOTE:

1. Depends on load.

SECTION V
REPLACEABLE PARTS

5-1. INTRODUCTION.

5-2. This section contains information for ordering replacement parts for the cartridge disc interface kit. Table 5-1 lists the parts of the cable assembly called out in figure 5-1. Table 5-2 is a total quantity listing of all replaceable parts in the interface kit, and the parts are listed in numerical order by HP part number. Tables 5-1 and 5-2 list the following information for each part:

a. Description of the part. (Refer to table 5-3 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to list of manufacturers in table 5-4.

c. Manufacturer's part number.

d. Total quantity of each part used in the interface kit.

5-3. A separate parts list is provided along with the parts location diagram for each cartridge disc interface card in section IV of this manual. These parts lists present the parts in alphanumeric order by reference designation.

5-4. ORDERING INFORMATION.

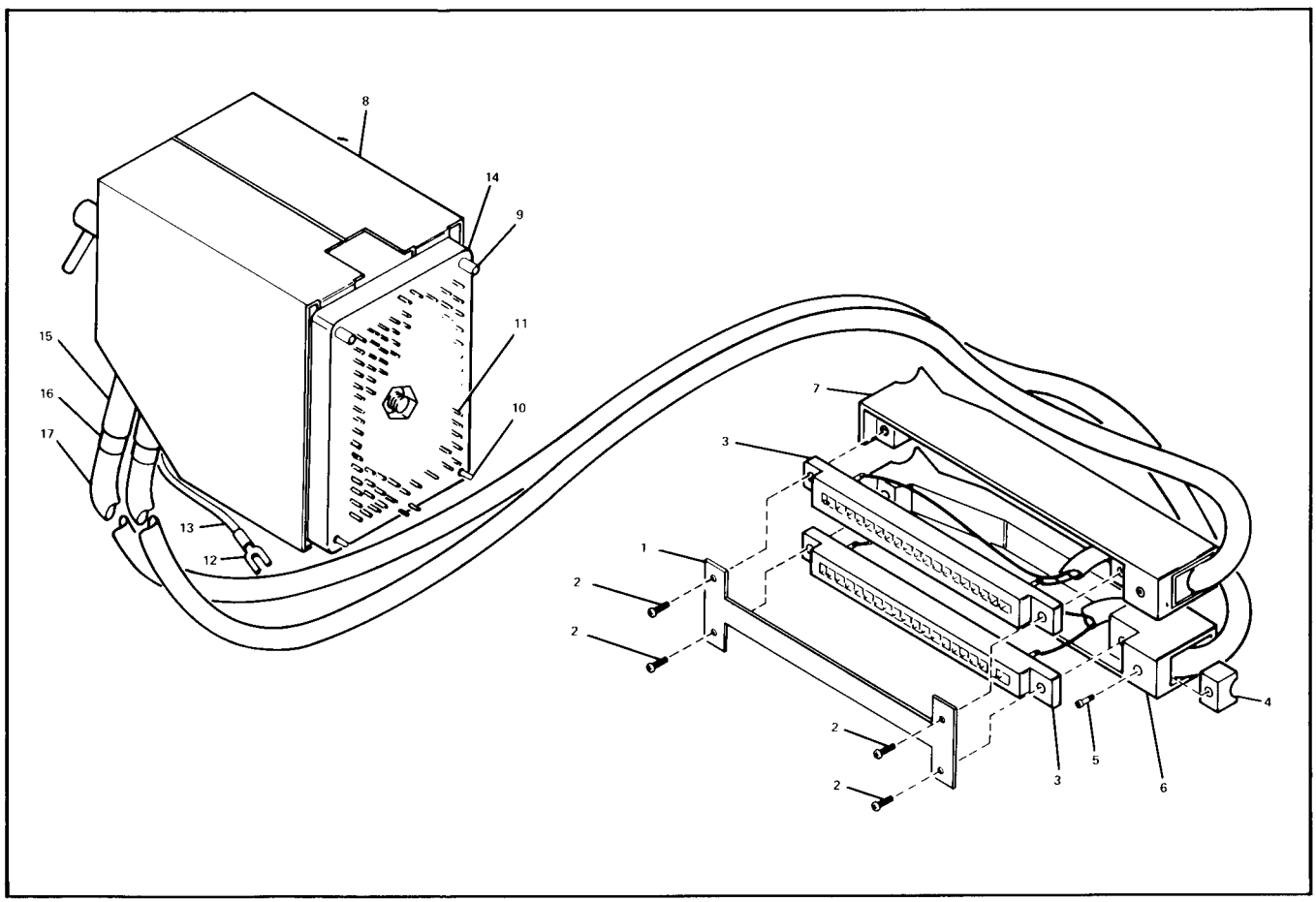
5-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Instrument model and serial number.

b. Hewlett-Packard stock number for each part.

c. Description of each part.

d. Circuit reference designation.



2090-6

Figure 5-1. Cable Assembly, Exploded View

Table 5-1. Cable Assembly Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
5-1-	12557-60006	Cable Assembly (note 1)	28480	12557-60006	1
1	02116-0081	* Brace, Double Connector	28480	02116-0081	1
		(Attaching Parts)			
2	0624-0098	* Screw, Machine, pozi, No. 4-40, 7/16 in.	00000	OBD	4
		– – – x – – –			
3	1251-0335	* Connector, Receptacle, PC, 48 pin	95238	K600-13-PCGD-24	2
4	02116-4003	* Cable Clamp	28480	02116-4003	2
		(Attaching Parts)			
5	3030-0143	* Setscrew, No. 6-32, 1/2 in.	00000	OBD	2
		– – – x – – –			
6	02116-2070	* Hood, Dual, Right	28480	02116-2070	1
7	02116-2071	* Hood, Dual, Left	28480	02116-2071	1
8	1251-2521	* Shield	00779	202798-1	1
9	1251-2524	* Guide Pin, Male	00779	201046-4	2
10	1251-2523	* Guide Pin, Female	00779	201047-4	2
11	1251-2522	* Connector Pin	00779	66106-3	144
12	0362-0127	* Terminal Lug, 12-10 AWG	00000	OBD	1
13	8150-1899	* Wire, 12 AWG	00000	OBD	7-1/2 in.
14	1251-2525	* Block, Pin	00779	202799-2	1
15	1251-0170	* Bushing, rubber, No. 10	98825	18220-10	2
16	1251-0171	* Bushing, rubber, No. 8	98825	18220-1	2
17	8120-1416	* Cable, 36 twisted pair	28480	8120-1416	30 ft.

NOTE:

1. Early versions of the interface kit contained an unshielded cable assembly, part no. 12557-60001. When re-ordering specify the shielded cable assembly, part no. 12557-60006.

Table 5-2. Cartridge Disc Interface Kit Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153	2
0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154	4
0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	28480	0180-0197	28
0362-0127	Terminal Lug, 12-10 AWG	00000	OBD	1
0624-0098	Screw, Machine, pozi, No. 4-40, 7/16 in.	00000	OBD	4
0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	19701	MF4CD4640F	2
0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F	40
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F	38
0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	14674	MF4CD1000F	4
0757-0407	Resistor, Fxd, Flm, 200 ohms, 1%, 1/8W	14674	MF4CD2000F	44
0757-0418	Resistor, Fxd, Flm, 619 ohms, 1%, 1/8W	14674	MF4CD6190F	2
0757-0438	Resistor, Fxd, Flm, 5.1k, 1%, 1/8W	14674	MF4CD5111F	2
0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	14674	MF4CD1002F	8
0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	14674	MF4CD1471F	2
1251-0170	Bushing, rubber, No. 10	98825	18220-10	2
1251-0171	Bushing, rubber, No. 8	98825	18220-1	2
1251-0335	Connector, Receptacle, PC, 48 pin	95238	K600-13-PCGD-24	2
1251-2521	Shield	00779	202798-1	1
1251-2522	Connector Pin	00779	66106-3	144
1251-2523	Guide Pin, Female	00779	201047-4	2
1251-2524	Guide Pin, Male	00779	201046-4	2
1251-2525	Block, Pin	00779	202799-2	1
1480-0116	Extractor Pin, PC Card	28480	1480-0116	4
1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020	10
1820-0054	Integrated Circuit, TTL	01295	SN4342	28
1820-0068	Integrated Circuit, TTL	01295	SN4343	6
1820-0069	Integrated Circuit, TTL	56289	USN7420A	2
1820-0071	Integrated Circuit, TTL	56289	USN7440A	8
1820-0077	Integrated Circuit, TTL	56289	USN7474A	4
1820-0140	Integrated Circuit, TTL	04713	SC7513PK	2
1820-0141	Integrated Circuit, TTL	04713	SC7514PK	2
1820-0301	Integrated Circuit, TTL	01295	SN4463	16
1820-0348	Integrated Circuit, DTL	01295	SN4506	16
1820-0956	Integrated Circuit, CTL	07263	SL3459	24
1854-0094	Transistor, Si, NPN	07263	2N3646	2
3030-0143	Setscrew, No. 6-32, 1/2 in.	00000	OBD	2
5040-1464	Extractor, PC Card	28480	5040-1464	4
8120-1416	Cable, 36 twisted pair	28480	8120-1283	30 ft.
8150-1899	Wire, 12 AWG	00000	OBD	7-1/2 in.
8159-0005	Jumper Wire	08480	8159-0005	20
02116-0081	Brace, Double Connector	28480	02116-0081	1
02116-2070	Hood, Dual, Right	28480	02116-2070	1
02116-2071	Hood, Dual, Left	28480	02116-2071	1
02116-4003	Cable Clamp	28480	02116-4003	2
12557-60002	Circuit Card, Data Channel	28480	12557-60002	1
12557-60003	Circuit Card, Command Channel	28480	12557-60003	1
12557-60006	Cable Assembly	28480	12557-60006	1
12557-90001	12557A Operating and Service Manual	28480	12557-90001	1
12849-60003	PC Connector, Test	28480	12849-60003	1
12849-60004	PC Connector, Test	28480	12849-60004	1

HEWLETT hp PACKARD

12557A

CARTRIDGE DISC INTERFACE KIT

(FOR 2114, 2115, AND 2116 COMPUTERS)

UPDATING SUPPLEMENT FOR OPERATING AND SERVICE MANUAL

1 JANUARY 1971

MANUAL IDENTIFICATION

Manual Serial No. Prefix: NA

Manual Printed: September 1970

Manual Part Number: 12557-90001

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Serial No. Prefix	Change

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes

Changes 1 through 5 dated 1 January 1971.

11000 Wolfe Road, Cupertino, California 95014, Tel. (408) 257-7000, TWX 910-338-0221

Europe: 1217 Meyrin-Geneva, Switzerland • Cable "HEWPACKSA" Tel. (022) 41.54.00

Printed in U.S.A.

CHANGE	DESCRIPTION
1	Page 2-14. Add an asterisk next to number 10 in the BIT column and at the bottom of the page add the following: *If the HP 2870A Disc Drive has a serial number prefix 1050- or subsequent, the Access Hunting signal is not used and bit 10 remains at logic 0.
2	Page 4-3, figure 4-1. Add an inversion dot at the clear-side input to the input buffer register Bit 2 FF (U13B).
3	Page 4-3, figure 4-1. Add an inversion bar (as $\overline{\text{BIT 15}}$) over all signal mnemonics for signals routed between the I/O device and the interface card, except the Power On (PON) signal.
4	Page 4-5, figure 4-2. Add an inversion dot at the clear-side input to the input buffer register Bit 2 FF (U13B).
5	Page 4-3, figure 4-2. Add an inversion bar (as $\overline{\text{BIT 15}}$) over all signal mnemonics for signals routed between the I/O device and the interface card, except the Power On (PON) signal.