HEWLETT PACKARD

Racal - Redac
vs
HP EE DesignCenter

Competitive Report
January, 1989

Electronic Design Division
Fort Collins, Colorado
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Introduction

This report provides business and technical competitive information on Racal-Redac in comparison to HP's EE DesignCenter products. It is intended as a reference tool for EDD's sales organization. This guide is for HP internal use only.

The business section contains both factual information and background material of Racal-Redac. The business information was obtained through Racal-Redac's company press releases, brochures, customer contacts, and a consultant research group. The information is HP's interpretation of information in the public domain and information obtained through outside consultants and has not been verified. HP does not guarantee its completeness, timeliness or accuracy.

The document also contains technical information on products offered by Racal-Redac as compared to EDD's product offerings. Product comparisons are based on technology comparisons, as opposed to product feature comparisons. Product strengths and weaknesses are also included. The technical information was obtained through field systems engineers and factory-based support engineers research.

Executive Summary

Racal-Redac Strengths

Racal-Redac prides itself as being first in the printed circuit board layout industry and is considered a senior vendor, especially in Europe. Racal-Redac had a good period of revenue growth between 1986 and 1987, increasing from $61 million (U.S.) to $84 million on a system that primarily centers around printed circuit board design. Also, Racal-Redac considers itself a leader in the CIM environment.

- Visula runs on industry standard platforms (Sun, DEC VAX, NEC NEWS, & Apollo)
- Good drawing ability and functionality
- INFORMIX database
- Long established history as a player in printed circuit board design

HP Strengths

Racal-Redac is now in a shaky position since companies like Daisy-Cadnetix and Mentor have products that run on the same platforms owned by Racal-Redac customers. Racal-Redac is also vulnerable to companies like Mentor and Hewlett-Packard, whose product offerings have a range of functionality that Racal-Redac can't match.

- DesignCenter, with its wide range of applications
- EDS & PCDS software and HP-UX are more stable software products than Visula
- Hierarchical design support
- Open links to other CAD systems
- Designed for an electrical engineer rather than a data entry operator
- HP's strong world-wide sales force

Company Background

History

Racal Electronics plc Group is a UK multi-divisional electronics company with a product range spanning all areas of electronics. Racal-Redac was founded in 1965 as a research company supplying Racal Electronics with computer-based tools. In 1970 Racal-Redac produced its first interactive computer graphics PCB layout system. During the early 1970's, Recal-Redac quickly built a reputation for PCB layout products with very few competitors. During the latter 1970's, with the advent of more competition, Recal-Redac turned to hardware design and manufacturing. At first, Racal-Redac introduced and began to produce the CADET and MAXI graphics systems as stand-alone and terminal systems. However, Recal-Redac was unable to keep up with the continuous hardware developments in graphics technology and by 1981 had lost leadership of the PCB layout business. In the mid 1980's, Recal-Redac moved from providing software running on their own proprietary hardware to industry-standard platforms. Since this time, Racal-Redac has put most of their resources into software, thus remaining competitive.

General Information

Headquarters

Racal Electronics plc Group
Bracknell, England, UK
CEO: Sir Ernest Harrison

Racal-Redac LTD
Tewkesbury, England, UK
CEO: Gary Vansteen

Number of Employees

Racal Electronics plc Group	approx.	32,500 world-wide
Racal-Redac LTD	"	550 world-wide
Redac R&D	"	180
SRs	"	80
SEs	"	80

Installed Base: Since Recal-Redac was founded in 1965, they have installed almost 8500 seats, nearly half on Personal Computers (PCs). **Table 1** shows the regional segmentations of Racal-Redac's installed base in units shipped. The figures reflect 1987 data with the total shipped to date figures being cumulative and the remaining figures representing the number shipped in that year. The table also lists Racal-Redac's Compounded Annual Growth Rate (CAGR) in the regional segmentations of their markets. N/A represents not applicable.

Table 1: Regional Segmentations of Racal-Redac's Installed Base
(CAE, PCB and IC workstation, units)

	1983	1984	1985	1986	1987	CAGR 83-87
World Wide Workstations	642	639	218	469	199	-25%
North America	156	213	93	115	29	-34%
Europe	480	426	93	310	144	-26%
Far East	6	0	29	32	25	44%
Rest of World	0	0	3	12	1	na
Total Shipped to Date	885	1,518	1,282	963	1,110	6%*
CAE Systems	0	0	12	23	31	na
PCB Systems	642	625	195	443	167	-29%
IC Systems	na	na	10	3	2	na

* figures reflect a move away from host-based systems to workstations & PCs
   source: Dataquest, July 1988

Target Markets

Racal-Redac considers itself a leader in the CIM environment. It stresses integrating the technical information that exists between engineering, design, test and manufacturing. Racal-Redac pride themselves as being the first in the printed circuit board layout industry and are considered a Senior Vendor, especially in Europe.

Racal-Redac's target market areas are:

CAE - Computer Aided Engineering
CAD - Computer Aided Design

CAM - Computer Aided Manufacturing
CAT - Computer Aided Test
CIM - Computer IntegratedManufacturing

Technology Partners

The wide range of products offered by Racal Electronics gives Racal-Redac a large number of existing customers with which to work.

Even though an outside consultant group claims that Racal invented "not invented here", Racal does have the following partners:

- Apollo Computer—joint marketing agreement
- INMOS plc—exclusive marketing and manufacturing agreement for the transputer chip and their IC CAD system
- IBM—value adder remarketer (VAR) for IBM PCs
- HHB Softron—third-party marketing agreement for CADAT
- Relational Database Systems—third-party marketing agreement for INFORMIX

- Various ME Vendors—co-operation to provide an ME solution (Ferranti Infographics and SDRC are two examples)
- Siemens—modification of Visula into Siemens SITEST product
- Praxis—ELLA VHDL
- Analogy—Saber analog simulator
- Interleaf—technical publishing system
- NEC—CMOS4 block libraries for ASIC gate array design

Financial and Market Share Information

Financials

Racal-Redac has shown steady improvement in revenues over the last four years, with an excellent period of revenue growth between 1986 and 1987, increasing from $61 Million to $84 Million. This explosive growth is attributed to Recal-Redac's move in the mid 1980's from providing proprietary hardware to using industry-standard platforms and allocating more money to software development.

Even with increasing revenues, Recal-Redac's CAGR was at negative 25% between 1983 and 1987, responding to their move away from host-based systems toward workstations and PCs.

The majority of Recal-Redac's revenue is generated from printed circuit board products. **Table 2** shows the regional segmentations of revenue for Recal-Redac between 1983 and 1987. The figures in the table represent millions of dollars per year.

Table 2: Regional Segmentations of Racal-Redac's Revenue
(CAE, PCB and IC workstations, millions of dollars)

Racal-Redac	1983	1984	1985	1986	1987	CAGR 83-87
Total Revenues	44.7	32.3	50.5	62.1	89.8	19%
North America	9.9	11.1	14.2	10.9	13.0	7%
Europe	33.8	21.2	32.5	46.1	64.9	18%
Far East	1.0	0	3.4	3.9	11.6	85%
Rest of World	0	0	.5	1.1	.3	na

source: Dataquest, July 1988

Market Share

Market share is typically determined by comparing either units sold by each vendor or dollar revenue earned by each vendor. **Figure 1** shows the comparisons of total revenues of the combined markets of technical workstation platforms of CAE, PCB, & IC. Recal-Redac's third place position with 8% of the market share leads over HP's fifth place position with 5.3%. But when broken down into separate markets, Racal-Redac's lead over HP comes from it's advantage in the PCB market. They are considered experts by virtue of their long history in the market. For instance, in Europe, Recal-Redac is considered the de-facto standard in PCB design systems.
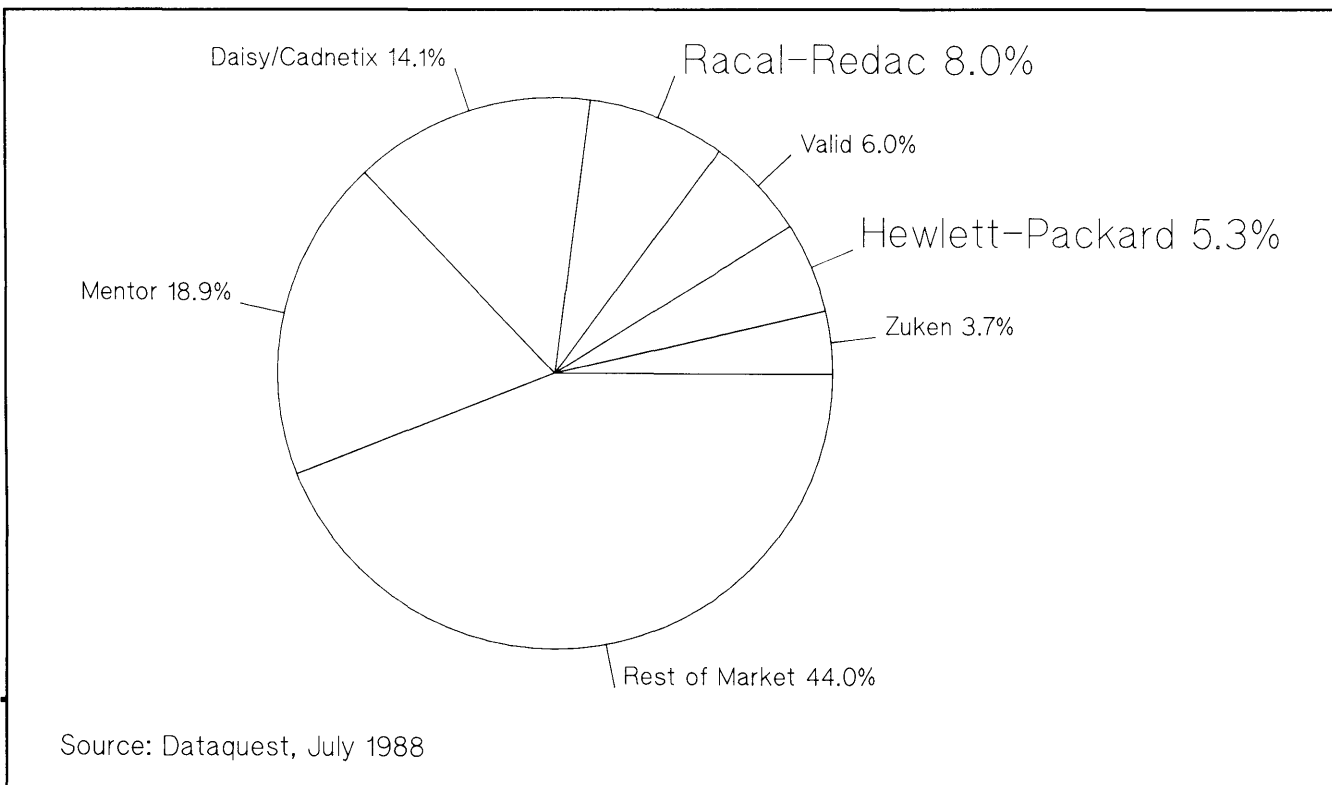

Figure 1: Market Share 1987, Total CAE, PCB, IC Markets

Figures **2, 3** and **4** show the breakdown of revenues in each market, CAE, PCB, and IC respectively. In the CAE and IC markets, Racal-Redac falls behind HP's lead.
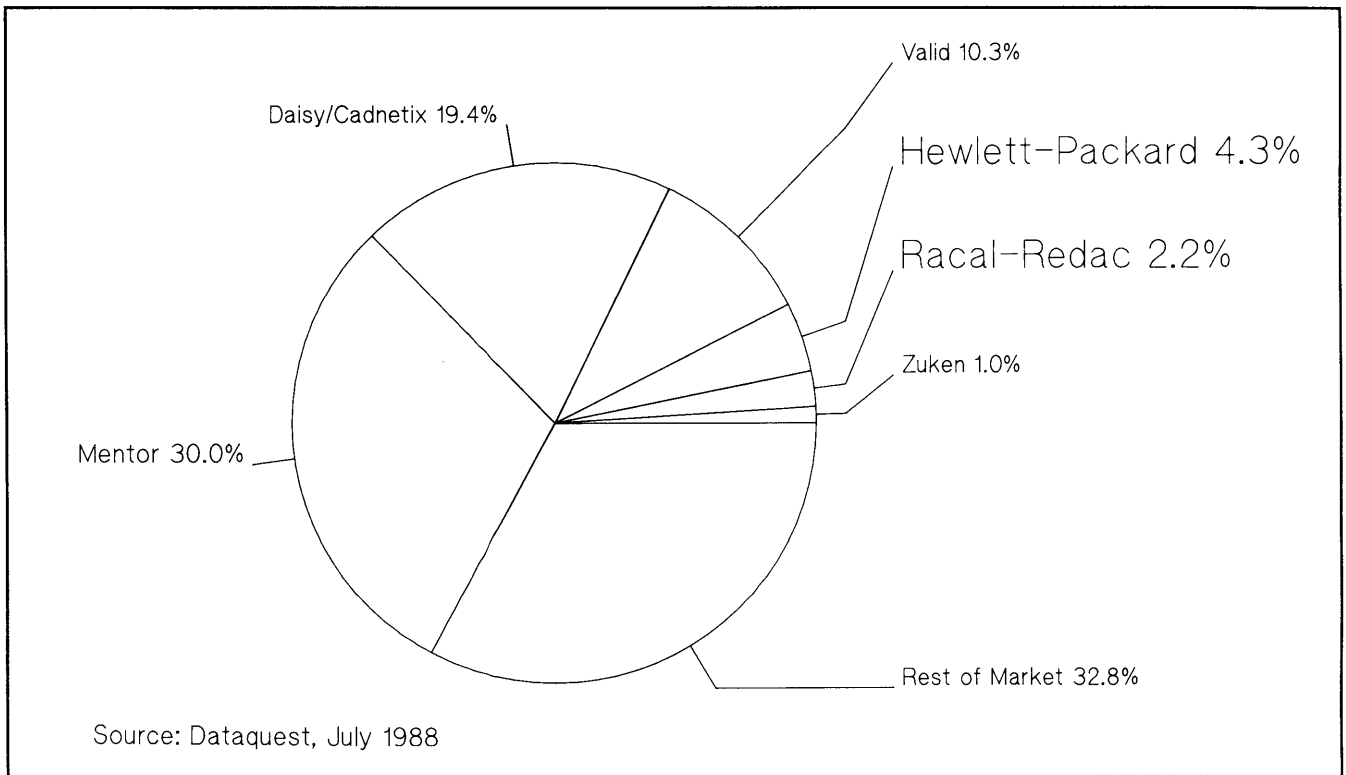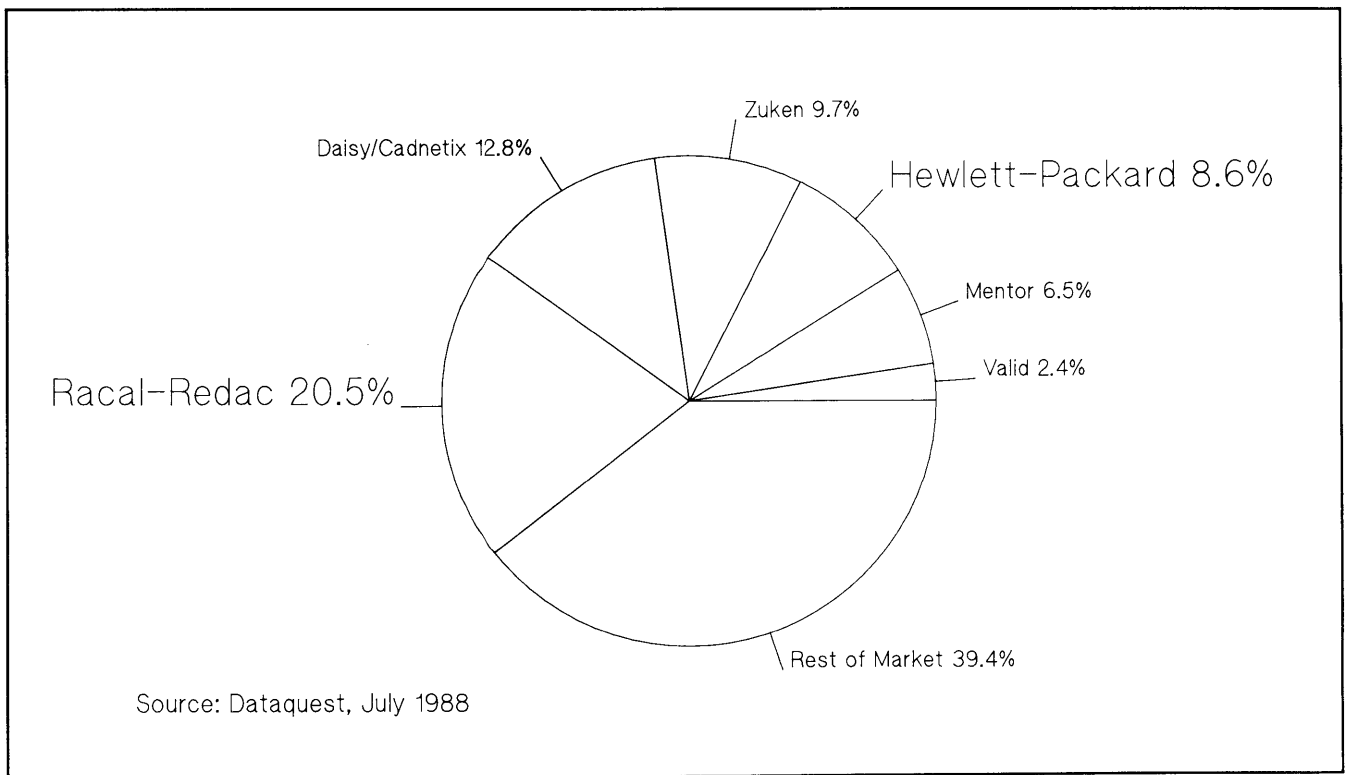
Figure 2: Market Share 1987, CAE Market

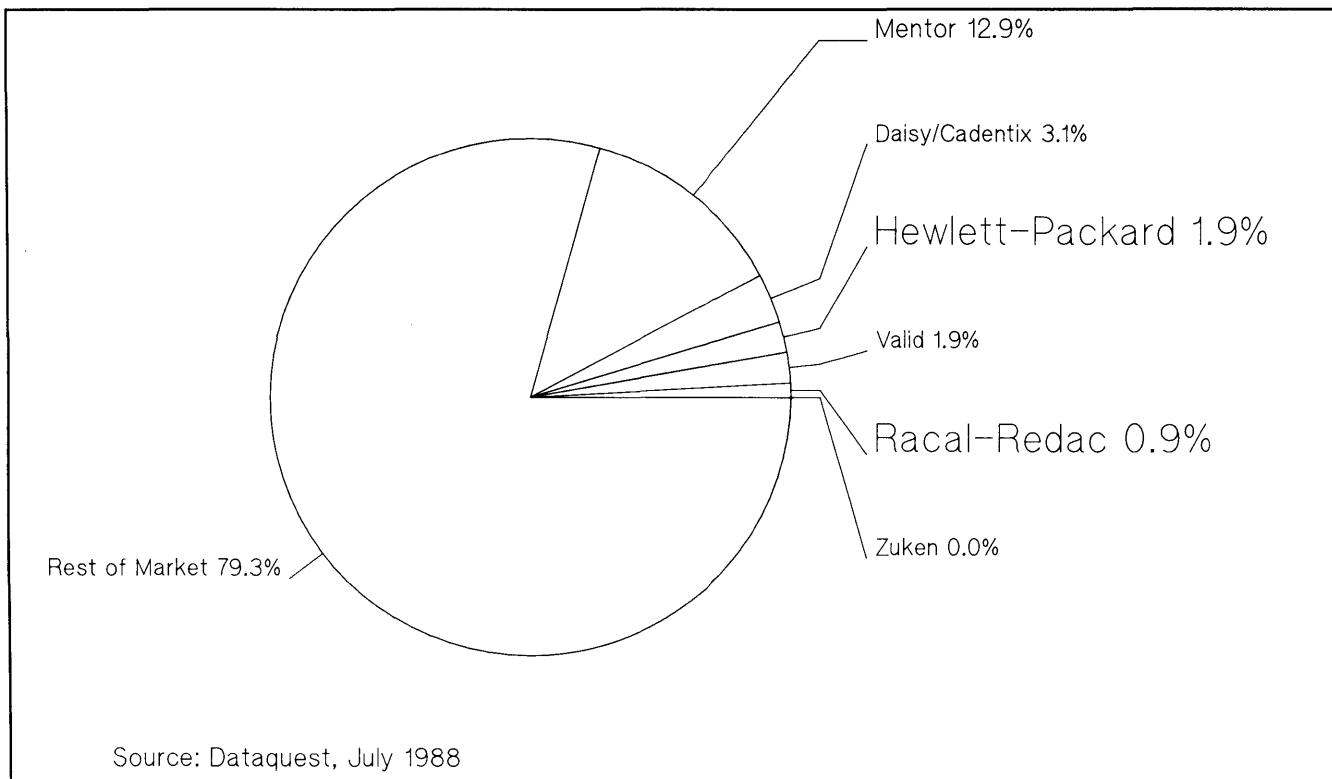**Figure 3: Market Share 1987, PCB Market**

Figure 4: Market Share 1987, IC Market

Product Family

Platforms

Racal-Redac runs on a variety of platforms.
- Apollo DN3000 — 2 MIP, 12 MHz MC68020 with MC68881 floating point processor
- NEC NEWS
- Sun 3/family — 1.5 to 4 MIP platforms, MC68020 based
- Sun 4/family —10 MIP platform
- MIPPER — 10 MIP hardware accelerator for hardware modelling & simulation from HHB
- VAX 11/780 —1 MIP, 32-bit proprietary processor
- VAX 11/750 —1 MIP, 32-bit proprietary processor
- PDP 11/73 —.3 MIP, 16-bit processor
- IBM PC based

Software

Recal-Redac offers the following software:
- Visula — CAE-PCB design system Rev 4.2 is current, and includes new user interface, customization, & hybrid support
- Visula Entry — personal computer based schematic capture system
- ISIS — IC layout product
- CADSTAR — high-end personal computer design (includes 386 based autorouter)
- REDCAD — low-end personal computer design (based on the old MAXI design system
- REDLOG — Schematic capture for REDCAD
- REDBOARD — PCB design for REDCAD
- REDSIM — Simulator for REDCAD

Note: MAXI, MINI and CADET are older systems no longer being sold.

Product coverage charts for Racal-Redac and HP are included in Appendix A.

Pricing Comparison

Figure 5 compares pricing on Racal-Redac's and HP's design capture systems for single seats. HP Design-Center has the competitive edge over Racal-Redac, running approximately 30% to 40% lower in price. Racal-Redac does offer a low-end personal computer entry into the design capture market, whereas HP does not.
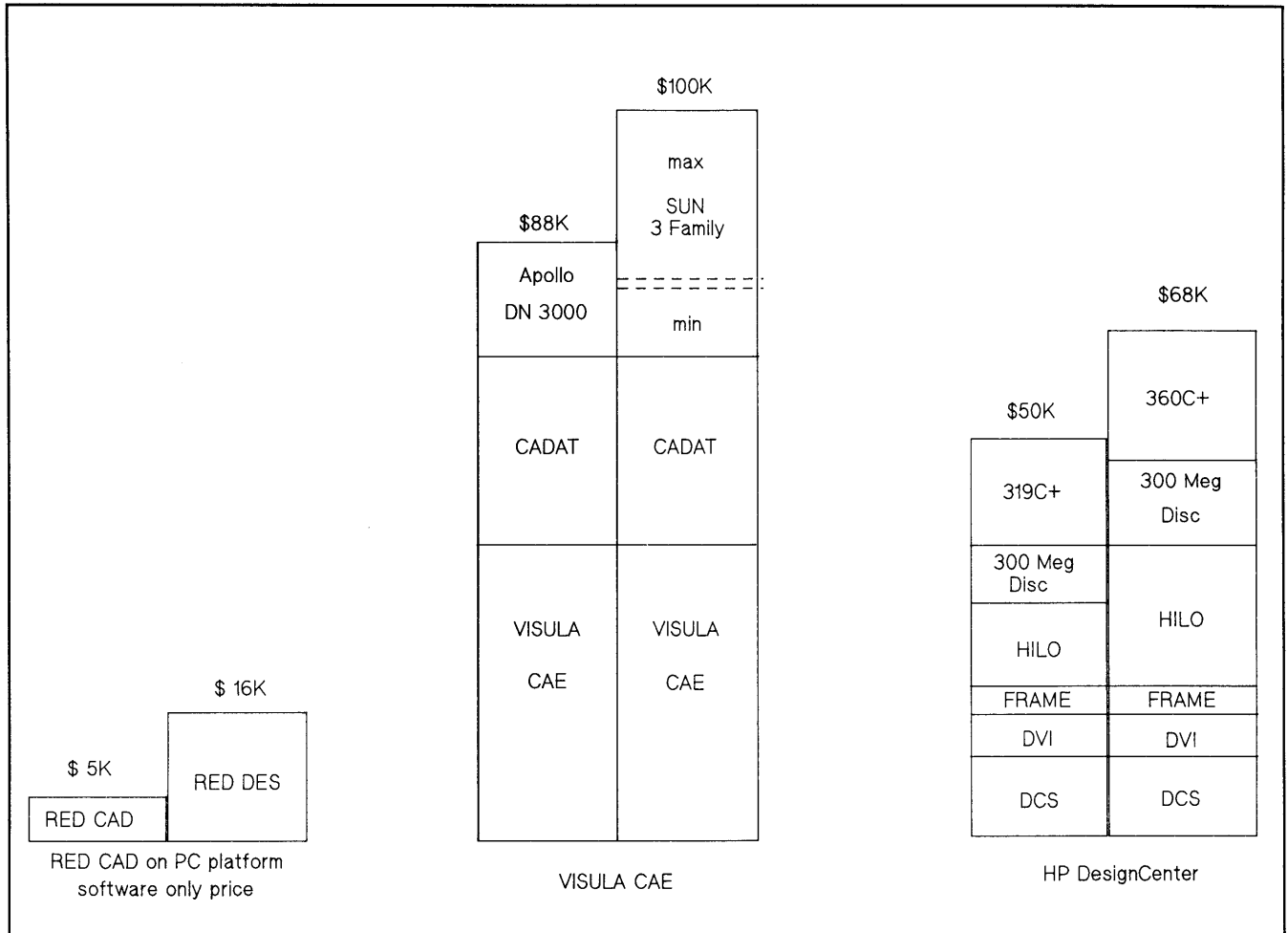
Figure 5: Pricing Comparison, Design Capture, Single Seat

HP Internal Use Only

Figure 6 compares prices on Racal-Redac's and HP's physical design systems for single seats. Again HP has the competitive edge in pricing, running approximately 40% lower in price.
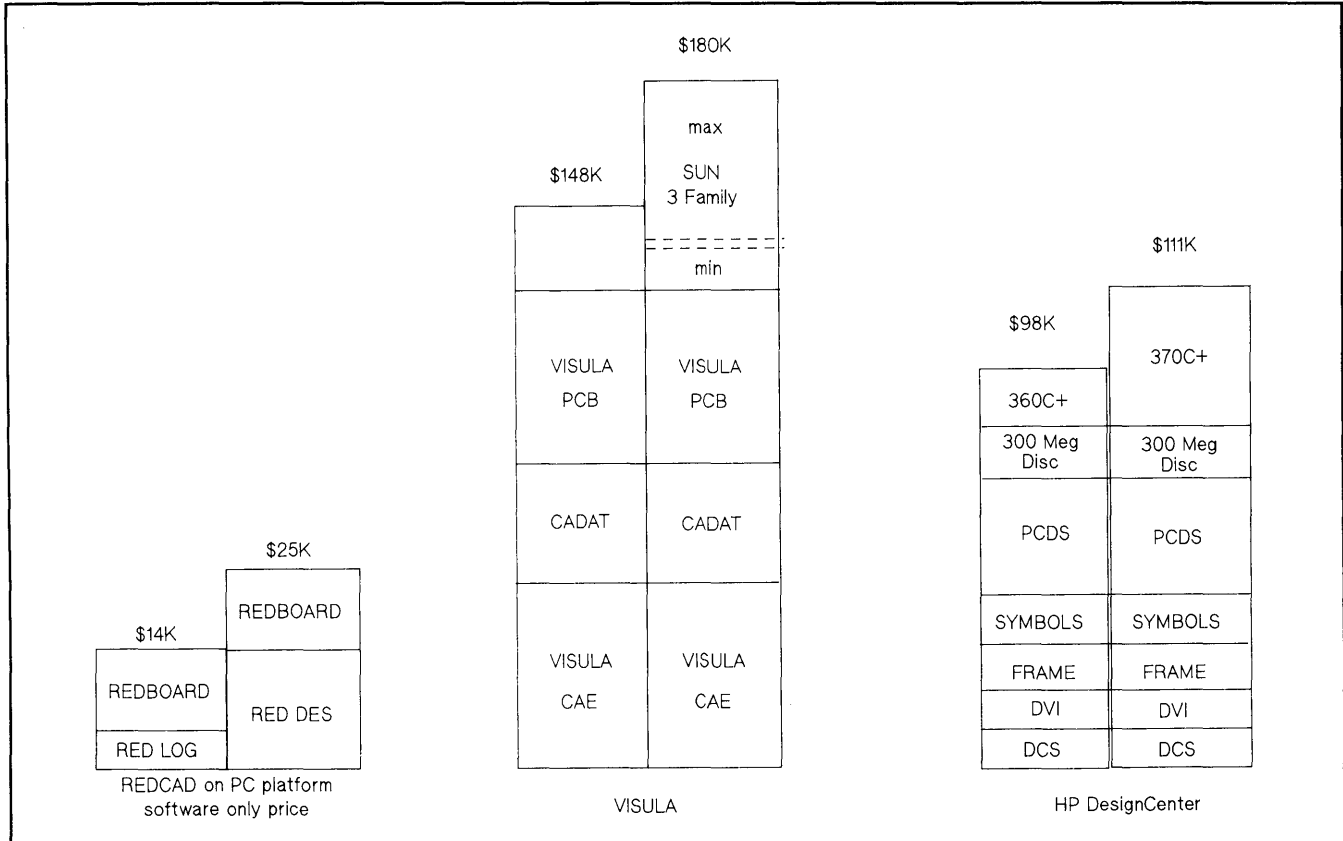
Figure 6: Pricing Comparison, Physical Design , Single Seat

For a listing of Racal-Redac's individual product prices, see Appendix B.

Service and Support

Racal-Redac has approximately 80 SEs to service their installed base and support sales demos. HP has a worldwide sales force that is adapted to each local country. In the 1980's, Racal-Redac moved from providing proprietary hardware to running on industry platforms. The revenue they saved from not having to provide hardware support is now funnelled into software development.

In 1985 Racal-Redac was taking a serious drubbing because their sales reps were selling 'customized links' while their SEs were unable to write and deliver them. Racal-Redac's R&D lab currently writes customized links.

Racal-Redac Future Products and Markets

A very high proportion of Racal-Redac's business comes from 150 major accounts that have been nurtured over their nearly 20 years in the business. However, in the early 1980's, Racal-Redac missed an opportunity to sell schematic and simulation products to these companies. Racal-Redac's future goal is to spot the products and services that these companies will buy in the next decade.

Recal-Redac recently released several major product enhancements in the Visula and CADSTAR range and these will bring in revenue for the next two to three years.* Racal-Redac is also selling CIM consulting to the rest of Racal Electronics. Products addressing the CIM marketplace should be expected in the near future.

Racal-Redac made three different attempts at ME design, failing each time. It is not expected that they will try again in the near future. Racal-Redac's current agreements with mechanical design companies appears to be working well to both side's advantage.

*At the time of this report, we did not have access to these new Racal-Redac systems to evaluate the new enhancements.

Racal-Redac Sales Pitches

At first glance, Racal-Redac appears comparable to HP in product offerings. However, HP Design-Center has the advantage of superior product coverage, running on top of superior workstations. Going head-to-head should allow HP to win, especially if mechanical engineering is a key part of the sale.

Racal-Redac claims to be the leader in CAM for the last 20 years. In reality, Racal-Redac is third in overall CAE, PCB, & IC revenues, with a decreasing market share and a negative CAGR, while, HP is fifth in overall CAM revenues after only 2 years in the market.

Racal-Redac also claims they have 5500 systems installed at over 1500 sites in 25 countries. HP EE DesignCenter can counter with the fact that HP has over 5500 systems installed already (EDS, PCDS, PLDDS & HP EGS). One claim that HP cannot refute is Racal-Redac's assertion that they created the first fully integrated computer electronic engineering system.

Another rising situation is CAD systems that use Mentor CAE linked to Racal-Redac's Visula PCB, running on the same hardware. Countering this will prove difficult for HP. It is easier for Mentor to sell a back-end to the Racal-Redac front-end system, than for HP to sell a complete system including hardware.

HP's design interface for RINF (Redac Interface Neutral Format) should be stressed as a selling point, allowing new accounts with data in a RINF formats to switch to HP systems without sacrificing the data.

Technical Analysis

Introduction

This section contains technical comparisons of Racal-Redac and HP/EDD applications for standard logic design, PLD design and verification, and PCB layout. It is also a presentation of the strengths and weaknesses of both Racal-Redac and HP/EDD products.

Spider diagrams are used for comparing the technical applications. Each application is divided by product components or parameters. The parameters establish the axis of the spider diagrams. In some cases, such as standard logic design entry and board layout, there are several subcategories or attributes for each of the axis.

For each axis, or subcategory, a whole number between 1 and 10 is used by HP field and factory support engineers. The larger the number, the "better" the performance of the application for that measurement axis, or subcategory. A value of 10 indicates the best, or state of the art, for current products on the market. A value of 1 indicates no capability, while a 5 is considered average. Unknown information is left blank and not included in the calculations. The subcategories are averaged and rounded to the nearest integer for plotting on the axis.

All comparisons of the Racal-Redac systems were performed at a service bureau in West Germany. The service bureau ran a set of 3 Apollo systems and a Sun, all networked together. The Apollo hardware included an D4000, DN3000, and DN580T all running Aegis, Domain revision 9.7. The Apollo systems were running Visula revision 4.1. The Sun system was used for the CADAT 6.0 system. Racal-Redac was compared to HP's current EE DesignCenter systems (release 2805) except for PCDS where the revision 2.0 was used as the comparison.

HP Internal Use Only

Standard Logic Design Entry

Visula Design Capture vs. HP EDS

Figure 7 is a design flow diagram showing the design process of both Racal-Redac Visula Design Capture and HP EDS. Racal-Redac's process relies on the use of macros. Macros are rated as a good thing by Visula and the press, but they are not very powerful. However, the macros are needed because of the poor system user interface.
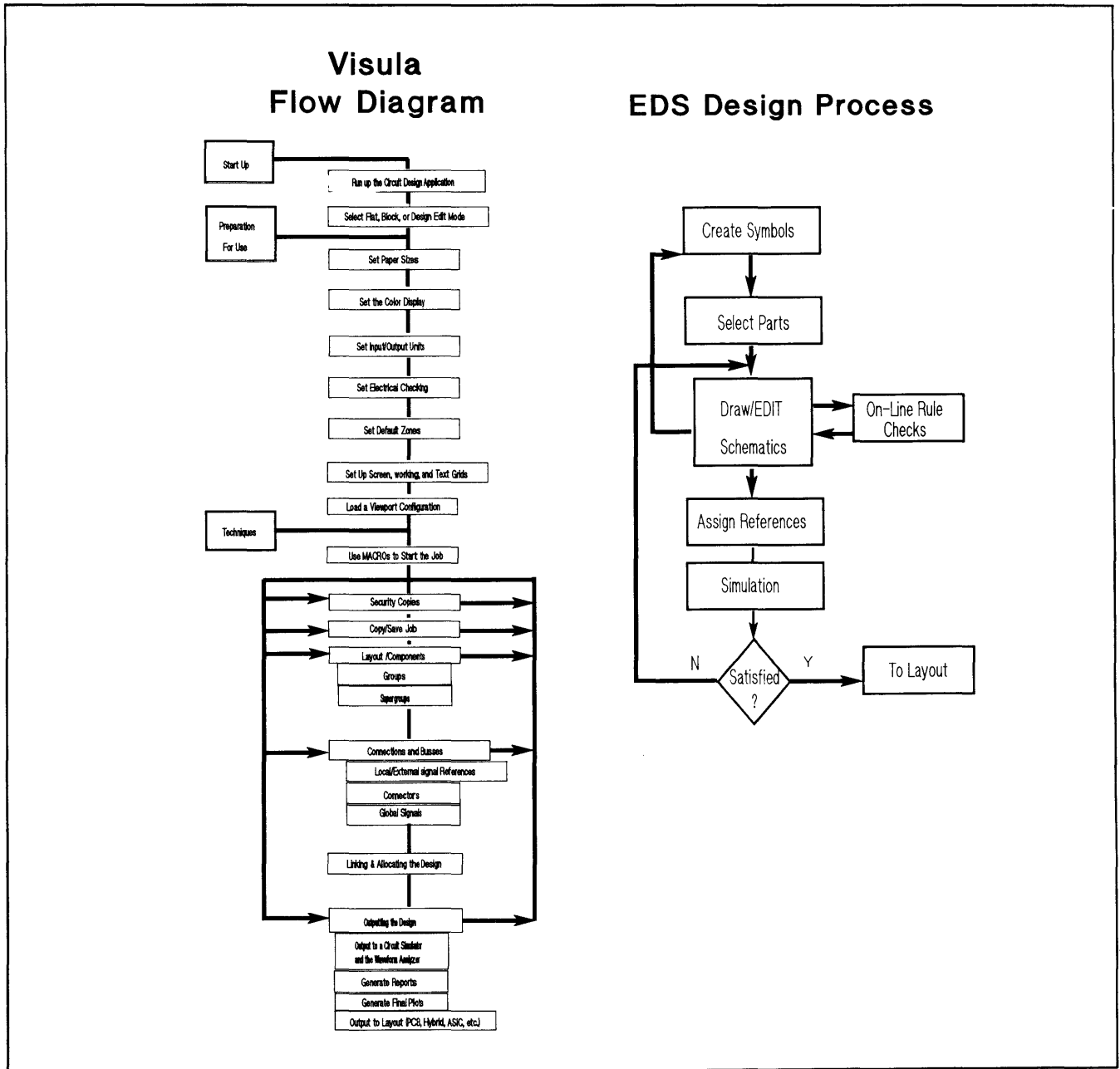
Figure 7: Design Flow Diagram

Figure 8 is a spider diagram comparing the Standard Logic Design Entry systems of Racal-Redac and HP. The parameters and attributes chosen are:

- User Interface
    —flexible command entry
    —operating system access
    —windowing
    —customizability
    —commonality
- Libraries
    —coverage
    —completeness
    —creation
    —standards
- Editor
    —graphics performance
    —speed of design entry
    —part selection
    —design rule checking
    —flat design
    —hierarchical design
- Capacity
    —IC design
    —PCB design

- Data Access
    —industry standarddatabase
    —access language
    —design file access
- Technology
    —PCB
    —IC
- Links
    —EDIF
    —IGES
    —test
    —simulation
    —layout
    —documentation
- General
    —learning tools
    —revision control
    —quality
    —engineering changes
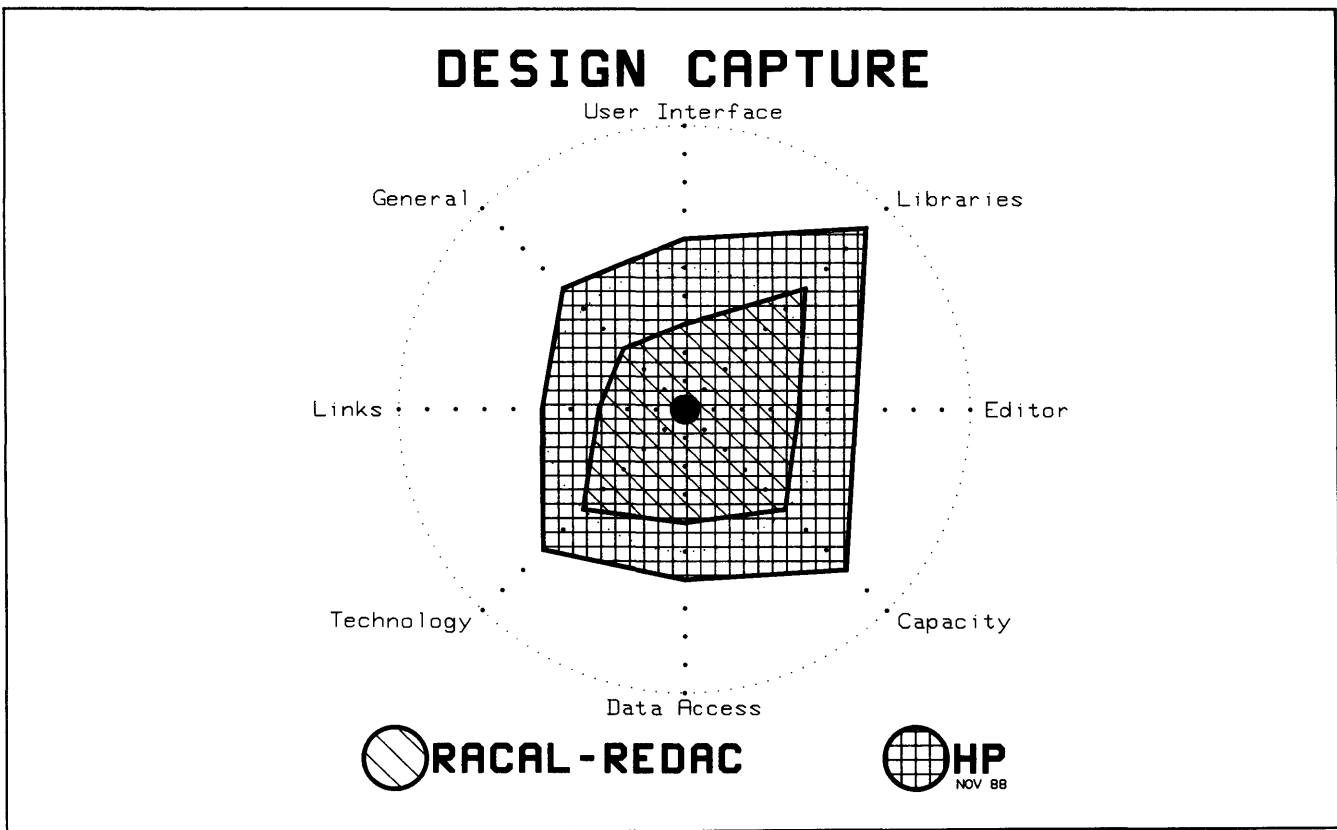
Figure 8: Standard Logic Design Entry

Visula Design Capture Strengths

- **INFORMIX Database** — Visula Design Capture (VDC) uses the standard relational database package INFORMIX for both PCB and schematic library parts storage. This makes a good "buzzword" but is of limited real use since other files (non-relational) are created and used by the PCB and schematic tools. The INFORMIX database coupled with other file structures, is similar to the multiple database structure in HP DesignCenter.

- **Drawing Ability** — Symbols and circuit drawings are easily created using the fundamental drawing (drafting) abilities of the system. VDC is a good artwork system with high resolution.

- **Netlist Capture** — VDC is a good, but limited, netlist capture tool. It is not as good for simulation information capture and interfacing.

- **Forced Design Rules** — All signals must end on connecting points, no "free space" signals are allowed. This results in a more correct circuit drawing.

- **Industry-Standard Platforms** — Visula runs on "industry-standard" hardware (Sun, Apollo and DEC) on the UNIX® operating system.

UNIX® is a registered trademark of AT&T in the U.S. and other countries.

HP EDS Strengths

- **For EEs** — HP EDS is designed to meet the needs of electrical engineers doing total design capture (schematic capture and simulation) as well as linking to physical layout, documentation and ASIC or Hybrid design. Racal-Redac is more of a front-end netlist-capture tool for PCBs with simulation interfacing "tacked on" to the system. Their sales literature states ".. reduces the possibility of error when non-engineering staff are entering designs". With HP EDS, EEs are directly using and benefiting from design capture and simulation tools.

- **Human Interface** — HP EDS is quick and easy to learn, with its mature human interface featuring online help and library access. Racal-Redac VDC is an old style drafting tool that is slower and more difficult to use.

- **Reliable** — HP DCS is stable code with relatively few bugs and infrequent system crashes. Racal-Redac VDC crashes often.

- **Hierarchical Design** — HP DCS is a fully-functional hierarchical design tool, suitable for both ASIC and PCB hierarchical design. Racal-Redac VDC has difficulties with hierarchical design, though their ads imply that it is easily done.

- **Integration with Simulation** — Information flow between HP DCS and the HILO simulator is excellent and also easy to use. The information flow betweenRacal-Redac VDC and HHB CADAT and CATS system is poor.

PLD Design and Verification

Racal-Redac does not offer PLD design and verification. HP offers PLDDS (HP PLD Design System), one of the most advanced PLD design tools available. HP PLDDS is oriented towards the system designer wanting to take full advantage of the latest PLD technology.

HP PLDDS Strengths

- **Human Interface** — Graphical, interactive user interface with pop-up menus for ease of use and fast startup.

- **Integrated Design Editors** — Multiple design editors with tightly integrated debuggers to quickly enter and verify designs at the same level of abstraction.

- **Device Nomination** -- Automatic fitting of designs into the most efficient PLD for device independent design.

- **Automatic Partitioning** -- Automatic partitioning of large designs into multiple PLDs to shorten design time.

- **Bidirectional Link** — Links with the HP Electronic Design System for more thorough system simulation and documentation.

- **Superior Links** — Links to the JEDEC standard for PLD fusemaps to migrate previously designed PLDs into newer devices.

- **Automatic Test Vector Generation** — Assures accurate manufacturing test.

Standard Logic Verification

Figure 9 shows Racal-Redac's Visula design verification design steps compared to HP design verification process. Racal-Redac has added a design capture package and a linker to the "flat" capture package which adds the capability of "hierarchical" design. The Visula documentation only documents their netlist output to simulators. Racal-Redac relies on simulators to document the true verification design cycle.
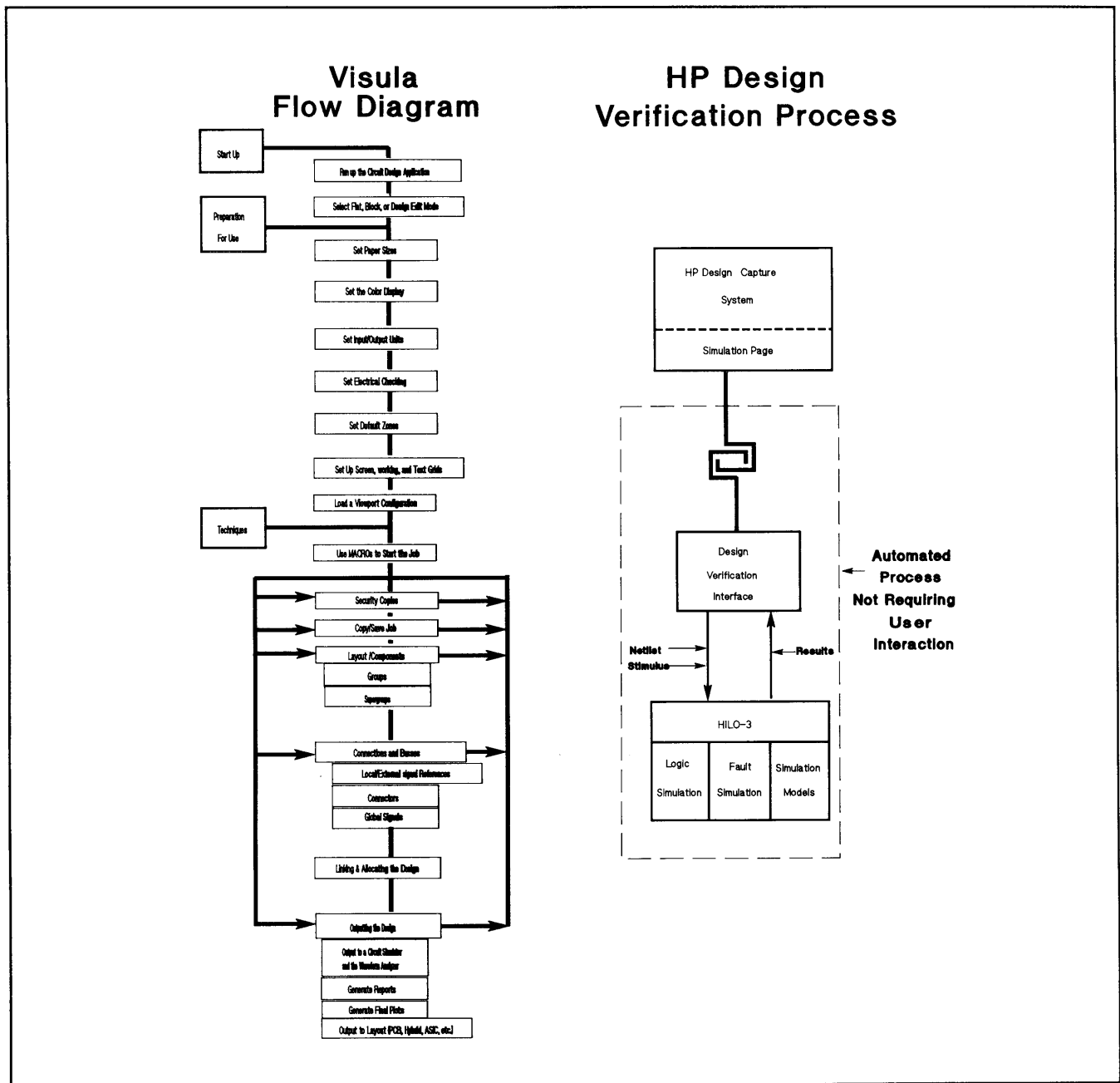

Figure 9: Design Verification Steps

Visula Digital Design Verification Strengths

- **INFORMIX Database** — Visula uses the industry standard INFORMIX database for its schematic and PCB data. INFORMIX is not used for design control, revision control or design data management.

- **Industry Standard Simulators Supported** — Visula links to CADAT, SPICE and Saber. However, these interfaces are at a primitive netlist level.

- **Rule Checking** — On-line rule checking is implemented.

- **Forced-connection Wire Addition** — Requires wires to be terminated at a connection point allowing fewer wiring mistakes to enter a design.

- **Locate Features** — Racal-Redac allows a limited amount of part locate/wire location. Racal-Redac's implementation is not as comprehensive and functional as it is in HP EDS.

- **Flexible Flat Circuit Netlist Extraction** — Part of a flat circuit can be used in a simulation simply by marking components to be included in the netlist.

- **Strong Set of Primitives for Gate-Level Modeling** — A good set of parameterized primitives come with the simulator. These range from MOS gates to ALU units.

- **Correct Dual Delay and Common Mode Ambiguity Analysis** — This feature works very well for Visula.

HP EDS Digital Design Verification Strengths

HP EDS competes extremely well against Visula, as these following points indicate.

- **Application Aimed at EEs** — HP EDS is designed for electrical engineers who desire a highly productive design verification tool. Racal-Redac Visula suite of software is oriented to PCB design with links to simulation and hierarchical design.

- **Quick Verification Loop** — HP EDS has good control of data during the verification process. Visula requires you to control the data.

- **User Interface** — HP EDS has a consistent user interface for design capture and verification. The interface includes the same advanced pop-up menus interface for all stages of verification and is quick to learn and easy to use. Visula uses hierarchical menus which are often confusing and misleading (23 function keys vs. 2 mouse buttons). Also, Visula capture interface is different from the Visula verification interface, which makes transition from one interface to the next difficult.

- **Fast Schematic Capture and Netlist Extraction** -- HP EDS has good circuit capture and circuit modification functionality. Visula has some nice features but overall, Visula is slower than HP EDS due to poor circuit modification functionality and poor software performance. Additionally, Visula requires a hierarchical linking before netlist extraction, while HP EDS does not.

- **Graphical/Textual Stimulus Generation** — HP EDS has a simulation page as part of the model. The simulation page has powerful graphical and textual editing tools where Visula requires the use of vi (UNIX editor) and an understanding of the CADAT textual stimulus language.

- **Easy Access to Simulation Control** — HP EDS grants access to the simulator controls through schematic capture. Visula requires running the simulator and interacting with the menu.

HP EDS Digital Design Verification Strengths, cont'd

- **Good Control of Verification Iteration** —HP EDS controls the generation of modified files for simulation. In HP EDS, complete netlist and stimulus does not have to be extracted when only one level of hierarchy is changed.

- **Simulation Server Access** — HP EDS gives transparent access to simulation servers which reduces the verification iteration time. Visula uses a manual copy of files to remote servers.

- **Link to HP 64000 Development Systems** — HP EDS links code from compilers and partitions the code across multiple memory devices. Visula/ CADAT requires the manual partitioning of memory contents and an addition to the library before simulation.

- **Link to PLDDS** — HP EDS can automatically create a pal symbol and simulation model. How ever, this is not handled (well) in the Visula link to CADAT.

- **HILO Behavioral Modelling Language** — HILO has a flexible behavioral modeling language. The modeling language preferred by Visula/ CADAT is C.

- **Timing Check Parameters Included in Models** — Timing checks are implemented by the HILO simulator and are included in quality models. CADAT implements timing checks, but doesn't have data in its released library.

- **Design Database is Open** — When user defined data extraction is needed, HP DDL provides access. Visula allows access only with RINF for pre-defined reports.

- **ASIC Support** — HP EDS has a growing list of ASIC design kits which are jointly supported by HP and the vendor. The Visula system we inspected, had an NEC symbol library, but lacked the design kit and documentation from either Racal-Redac, HHB or NEC.

- **Simulator Control** — HILO has good stand-alone verification tools. CADAT does not have these features.

- **Links to Prototyping** — HP EDD Vulcan link has no equivalent on Visula.

Documentation

Racal-Redac does not provide tools for documentation, but they do provide standard platforms enabling third-party documentation software to run on their systems. The Visula system does output HPGL (and other graphics formats) for possible inclusion in the documentation system.

HP offers FrameMaker, a professional document publishing software designed for the engineer, scientist or technical professional.

FrameMaker Strengths

- Complete word processor

- Graphics program for importing, formatting, and creating graphics

- Interactive page and document layout

- FrameViewer providing view-only access to FrameMaker

- International FrameMaker providing localization in 5 languages

ASIC Design and Verification

There was little information available about the capabilities or performance of Racal-Redac's ASIC Design applications, therefore no comparisons were possible.

Printed Circuit Board Layout

Figure 10 shows the Diagrammatic Representation of Typical PCD Design Steps for Racal-Redac and HP. Racal-Redac's diagram shows a strong focus on the PCB design and manufacturing process. Racal-Redac make no reference to connecting with (although they do) the schematic capture for back annotation. This is an "older" style concept of PCB creation and not the integrated information sharing available in HP DesignCenter, shown on the right side of the diagram. While it could be argued that Racal-Redac shows a conceptual flow to better help the older technique designer get use to a CAD system, it also shows how outdated their approach can be.

Diagrammatic Representation of Typical PCD Design Steps

- Preparing For Use
- Determining the job parameters
- Bringing a Job into the System
- Laying Out the Board
- Setting Up the System
- Preparing the Board
- Placing the Components
- Tidying up the connections
- Editing the Layout
- Routing Your Design
- Prepare for Routing
- Power Planes
- Manual Routing
- Memory Routing
- Automatic Routing
- Checking your Design
- Preparing For Checking
- Documentation & Mfging Output
- Producing Manufacturing Dwgs
- Outputting Data
- Producing Parts Lists & Reports
- Archive
- Archiving Data

HP PCDS Design Process

- Input Netlist
- Create Board Blank
- Input Logic
- Design Module Autoplace Edit Board, etc. → Back Annotation to EDS
- Routing
- Create Manufacturing Outputs

Figure 10: Design Steps

Figure 11 is a spider diagram comparing board layout systems from Racal-Redac and HP. The parameters and attributes chosen are:

- Manufacturing Outputs
    —panelization
    —photoplotters
    —drill
    —pick and place
    —assembly drawings
    —reports

- Library
    —creation
    —maintenance
    —vendor supplied quantity

- Editing
    —interactive placement
    —interactive routing
    —design rule checking
    —logic information access

- Place & Route
    —automatic placer
    —automatic router

- Technology
    —surface mount
    —through hole
    —hybrid thick film
    —hybrid thin film
    —multi layer
    —metal core
    —ECL

- Links
    —front end
    —mechanical engineering
    —documentation
    —thermal
    —test
    —EDIF
    —IGES
    —open system

- General
    —user interface
    —customizability
    —quality
    —reliability
    —engineering changes

Figure 11: Board Layout

HP Internal Use Only

Visula PCB Design (VPD) Strengths

- **INFORMIX Database** — VPD uses an industry-standard relational database for both PCB and schematic library parts storage. This is a good "buzzword" but of limited real use since other files (not relational) are created by both the PCB and schematic tools. This multiple database structure is similar to the HP DesignCenter concept.

- **Gridless, Ripup Autorouter** — Racal-Redac's VPD autorouter has all the "buzzwords" including gridless, ripup, memory router, sm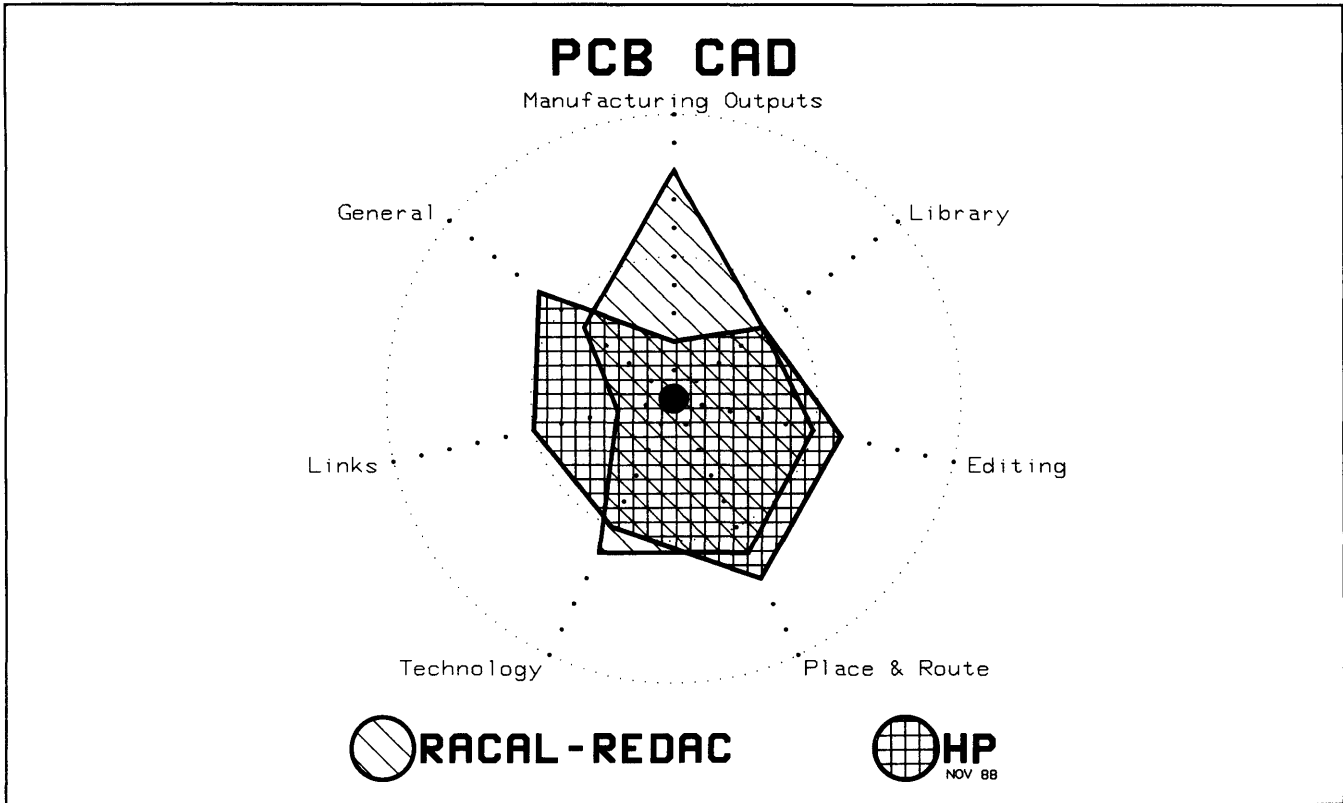oothing, mitering and their "bloodhound" algorithm. This all sounds very good, but the results show that the router is only a little better than the HP router.

- **Manual Tools** — Racal-Redac VPD has strong abilities for moving and drawing parts and traces. Its evolution from a drawing tool shines here, and should not be discounted for its effect on designers.

- **Manufacturing Outputs** — VPD supports output files created for a broad line of tools such as photoplotters, ACI, NC drill, ATE, penplotters and raster plotters. A strong tool is the menu driven configuration processor that creates a reusable process that is tuned to a particular machine at the customer site. HP EDD is currently working on a similar design manufacturing link for PCDS.

HP PCDS Strengths

- **Placement** — HP PCDS placement tools are superior both in scope and execution when compared to Racal-Redac Visula. Our histogram of channel usage and improve device is strong and better than Visula. In Visula, the measure of how good a placement is, is determined by running the autorouter for one pass to see the results! Obviously good placement is required for good routing; in HP PCDS we provide good tools to establish good placement.

- **Reliability** — HP PCDS is stable code with relative few bugs and seldom crashes. Visula PCB design crashes often. Racal-Redac is not known for its quality and designers learn to expect system crashes.

- **Performance** — HP PCDS graphics performance is superior to Racal-Redac's VPD.

- **Human Interface** — HP PCDS has a consistent "heads-up" design interface. Visula requires the operator to constantly look down at the keys, the screen and pick using the 3-button mouse to get the job done. There are too many menus that must be searched to get the job done in Visula. HP PCDS has on-line help, whereas Racal-Redac does not.

- **Integration** — HP PCDS works well with HP DCS for information flow in both directions. HP PCDS also works with mechanical design systems (ME-10/30) for bidirectional data flow. HP PCDS passes pictures into our documentation tool (FrameMaker) while Racal-Redac doesn't provide integrated documentation or ME design tools. HP's DesignCenter offers a larger, better integrated solution.

Racal-Redac Buzz-Word List

12 October, 1988

BDL
    CADAT's Behaviorial Modeling

Bloodhound
    Algorithm used in Visula router

CADET
    Racal-Redac stand-alone PCB product, now
    obsolete

CADAT
    HHB Digital Simulator product

CADSTAR
    High-end, personal computer design product

CATS
    CADAT's hardware modeler

CLASS
    Saber's command language

DSL
    CADAT's digital stimulus language

HSL
    High speed logic module

INFORMIX
    Relational database used by Visula

ISIS
    Racal-Redac's IC design system, licensed from
    INMOS

ISQL
    Interactive structured query language for
    INFORMIX database

LANA
    CADAT's Local area network acceleration

MAST
    Saber's Modeling language

MAXI
    Racal-Redac terminal based design system, now
    obsolete

MDF
    Machine description files

MINCON
    Visula PCB design's airline length summation
    (of traces)

POST
    Saber's interactive post-processor

REDCAD
    Low-end, personal computer design product

REDBOARD
    REDCAD's PCB product

REDLOG
    REDCAD's schematic capture product

REDSIM
    REDCAD's simulator product

Racal-Redac Buzz-Word List , cont'd

RINF
Redac Interface Neutral Format (files)

RMCS
Router Monitor Control System

Saber
Analogic Inc.'s Analog Simulator

VDC
Visula Design Capture

Visula
High end, front to back design system

VPD
Visula Printed Circuit Board Design

VSC
Visula Schematic Capture

V2DD
Visula 2D Drafting

WAVE
Visula Waveform Analyzer

Appendix A: Product Coverage Comparison

Design Step	Conventional PCB		PLD ASIC		Standard Cell ASIC	
	Racal	HP	Racal	HP	Racal	HP

Architecture Design
  Structured Des.
  HW/SW Partition
  Implm. Indep.
				
				PLDDS		

Library Parts
  Sch. Parts Creat
  PCB Parts Creat
  Hardware Models
  Mil Std Parts
	Visula
	
	no
		
		DCS/PCDS
		DCS/PCDS
		yes
		no
						
						DCS

Design Capture
  Behavioral
  Wave/STD/Boa
  Schematic Capt
	VDC
	CADAT BDL
	
	VDC
		DCS
		HILO HDL
		
		DCS
				
				PLDDS
				PLDDS/DCS
						
						DCS

Digital Simulation
 	
  Logic Sim.
  HW Sim.
  Fault Analysis
  Timing Analysis
	CADAT
	
	CADAT
	CATS
	CADAT
	CADAT
		HILO-3/
		System HILO
		
		System-HILO
		HiChip
		HILO FAULT
		System-HILO
		HiTime
				HILO-3/
				SystemHIlO
				
				System-HILO
				HiChip
				HILO FAULT
				System-HILO
				HiTime
						HILO-3/
						System HILO
						
						System-HILO
						HiChip
						HILO FAULT
						System-HILO
						HiTime

Analog Simulation
  SW Analog
  Mixed Mode
  Stress/reliabil
  RF/microwave
	Saber
	
	no
	Saber
	MDS
		AWB/Saber
		
		no
		AWB/Saber
		MDS
				Saber		AWB/Saber
						
						MDS

Physical Layout
  Edit
  Forced Router
  Rip-Up Router
  Random Route
  Other Router
  DRC
  Manuf. Outputs
	Visula VPD
	VPD
	yes
	yes
	no
	no
	batch
	yes
		PCDS
		PCDS
		yes
		yes
		no
		no
		on-line
		Mfg links
					ISIS
					ISIS	

Prototype Testing
  Waveform Cap/Com
  Digital HW Test
  Analog Waveform
  Analog HW Test
		
		HP16500A
		HP16500A
				
				HP16500A
				HP16500A
						
						HP16500A
						HP16500A

System Integr Test						

Mfg. Test Prep.
  Fault Analysis
  Test Generation
  Tester Links
		
		3065/TSSI
		DICE
						
						3065/TSSI
						DICE

Appendix A: Product Coverage Comparison, cont'd

Design Step	Conventional PCB		PLD ASIC		Standard Cell ASIC	
	Racal	HP	Racal	HP	Racal	HP

Mechanical Design
  2D
  3D
  Thermal Analysis
	V2DD	ME-30
		ME-30				

Documentation
  Text & Graph
  Integrated
  Tech. Pub.
	Interleaf
	Interleaf
	Interleaf
		FRAME
		FRAME
		FRAME				

SW Firmware		HP64000				
Engineering Parts						
Project Mgmt.						
Design Mgmt.		DSM				
File Management		DDC				
Misc						
Silicon Compilers						
System Level Sim						

Appendix A: Product Coverage Comparison, con'td

Design Step	Gate Array ASIC		Custom ASIC		Hybrid	
	Racal	HP	Racal	HP	Racal	HP

Architecture Design
  Structured Des.
  HW/SW Partition
  Implm. Indep.						

Library Parts
  Sch. Parts Creat
  PCB Parts Creat
  Harware Models
  Mil Std Parts
		DCS				

Design Capture
  Behavioral
  Wave/STD/Boa
  Schematic Capt
		DCS				

Digital Simulation
 	
  Logic Sim.
  HW Sim.
  Fault Analysis
  Timing Analysis
		HILO-3/
		System HILO
		
		System-HILO
		  HiChip
		HILO FAULT
		System HILO/
		  HiTime
				HILO-3/
				System HILO
				
				  HiChip
				HILO FAULT
				System HILO/
				  HiTime		

Analog Simulation
  SW Analog
  Mixed Mode
  Stress/reliabil
  RF/microwave
	Saber			AWB/Saber
				
				MDS		

Physical Layout
  Edit
  Forced Router
  Rip-Up Router
  Random Router
  Other Router
  DRC
  Manuf. Outputs
			ISIS
			
			ISIS
						EGS/MDS

Prototype Testing
  Waveform Cap/Com
  Digital HW Test
  Analog HW Test
		HP16500A
		HP16500A
				HP16500A
				HP16500A		

System Integr Test						

Mfg. Test Prep.
  Fault Analysis
  Test Generation
  Tester Links
		3065/TSSI		3065/TSSI		

Appendix A: Product Coverage Comparison, con'td

Design Step	Gate Array ASIC		Custom ASIC		Hybrid	
	Racal	HP	Racal	HP	Racal	HP

Mechanical Design
  2D
  3D
  Thermal Analysis						

Documentation
  Text & Graph
  Integrated
  Tech. Pub.						

SW/Firmware						
Engineering Parts						
Project Mgmt.						
Design Mgmt.						
File Management						
Misc						
Silicon Compilers						
System Level Sim						

Appendix B: Racal-Redac List Prices

The following prices are taken from Daratech, 1987's report on Redac, except where noted.

Visula	Priced as CAE/PCB.	
Visula	CAE	$ 6,000*
Visula	PCB	$40,000*
Visula Entry		
	PC based system	no price listed
ISIS		
	IC system	no price listed
REDCAD		
	PC based low-end system	no complete price listed
REDLOG		
	PC based capture	$ 500*
REDSIM		
	PC based simulation	no price listed
REDDES		
	New product, unsure of its composition	$16,000 **
REDBOARD		
	PC based layout	$ 9,000
CADSTAR		
	PC based high-end system	$ 4,500 *
CADAT		
	Simulator	$26,000 *
MAXI/PC		$ 995.00 *

* Source: CAD-CAM Technology, 1988.

** prices based on conversation between M.Haugen (HP) & Daratech, 11/88.