HEWLETT-PACKARD

HP 7936 AND HP 7937 DISC DRIVES

HARDWARE SUPPORT MANUAL

CERTIFICATION

Products, materials, parts, and services furnished on this order have been provided in accordance with all applicable Hewlett-Packard specifications. Actual inspection and test data pertaining to this order is on file and available for examination.

Hewlett-Packard's calibration measurements are traceable to the National Bureau of Standards to the extent allowed by the Bureau's calibration facilities.

The Hewlett-Packard Quality Program satisfies the requirements of FAR 52.246-15.

HP 7936 and HP 7937 Disc Drives Hardware Support Manual

Manual part number: 07937-90903
Microfiche part no. 07937-90803

Printed: JANUARY 1987 Edition 1
Printed in U.S.A. E0187

MODELS COVERED

This manual covers the following models: HP 7936H, 7937H, 7936XP, 7937XP.

OPTIONS COVERED

In addition to the standard model, this manual covers the following options: 015, 017.

HEWLETT-PACKARD
P.O. Box 39, Boise, Idaho 83707-0039

Notice

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance or use of this material.

HEWLETT-PACKARD assumes no responsibility for the use or reliability of its software on equipment that is not furnished by HEWLETT-PACKARD.

FOR U.S.A. ONLY

The Federal Communications Commission (in 47 CFR 15.818) has specified that the following notice be brought to the attention of the users of this product.

FEDERAL COMMUNICATIONS COMMISSION
RADIO FREQUENCY INTERFERENCE
STATEMENT

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition or a new update is published. No information is incorporated into a reprinting unless it appears as a prior update; the edition does not change when an update is incorporated.

A software code may be printed before the date; this indicates the version level of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

Edition 1.....JANUARY 1987

Herstellerbescheinigung

Hiermit wird bescheinigt, daß das Gerät/System HP 7936/7937 in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Manufacturer's Declaration

This is to certify that the product(s) HP 7936/7937 is in accordance with the Radio Interference Requirements of Directive FTZ 1046/1984. The German Bundespost was notified that this equipment was put into circulation; the right to check the series for compliance with the requirements was granted.

Additional Information for Test and Measurement Equipment

If Test and Measurement Equipment is operated with unscreened cables and/or used for measurements on open setups, the user has to assure that under operating conditions the Radio Interference Limits are still met at the border of his premises.

Safety Considerations

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure or practice that, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice that, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source according to the input power configuration instructions provided in this manual.

If this product is to be operated with an autotransformer make sure that the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged after the product has been disconnected from the main power source.

To avoid a fire hazard, fuses with the proper current rating and of the specified type (normal blow, time delay, etc.) must be used for replacement. To install or remove a fuse, first disconnect the power cord from the device. Then, using a small flat-bladed screw driver, turn the fuseholder cap counterclockwise until the cap releases. Install either end of a properly rated fuse into the cap. Next, insert the fuse and fuseholder cap into the fuseholder by pressing the cap inward and then turning it clockwise until it locks in place.

List of Effective Pages

The List of Effective Pages shows the edition or update number of all pages. Within the manual, any page changed since the last edition is indicated by printing the update number on the bottom of the page. Changes are marked with a vertical bar in the margin. If an update is incorporated when an edition is reprinted, these bars are removed. No information is incorporated into a reprinting unless it appears as a prior update. To verify that your manual contains the most current information, check that the version printed at the bottom of the page matches the version listed below for that page.

Effective Pages	Version
all	Edition 1

Contents

Contents (continued)

Contents (continued)

Contents (continued)

Figures and Tables

Figure or Table **Page**

Product Information 1

1-1. INTRODUCTION

This chapter contains product information for the Hewlett-Packard Model 7936 and 7937 Disc Drives. The information provided includes a general description of the HP 7936 and HP 7937, a list of equipment supplied, details of the product structure, test equipment required, and support strategy.

1-2. PRODUCT DESCRIPTION

The HP 7936 and HP 7937 Disc Drives are high-performance, random access, data storage devices designed for use with medium- and large-sized computer systems. In this manual, unless otherwise specified, "drive" refers to both the HP 7936 and HP 7937.

A microprocessor-based controller is factory-installed in the drive to provide an interface to the host computer. Two HP-IB controllers are available for this purpose. In the HP 7936H and HP 7937H Disc Drives, interface to the host is via an Hewlett-Packard Interface Bus (HP-IB) controller. In the HP 7936XP and HP 7937XP, the controller has HP-IB Cache added. Both of the controllers interface with the drive electronics via an HP-developed standard interface (ESI).

A sealed head-disc assembly (HDA) in the drive contains a spindle with a stack of seven non-removable 210-millimetre (8.3-inch) diameter discs. The spindle is belt-driven by a motor mounted adjacent to the sealed HDA. There are seven (HP 7936) or 13 (HP 7937) thin-film surfaces on the discs for data storage. An additional surface is used for dedicated servo code.

The formatted storage capacity of the drive is 307 megabytes (HP 7936) or 571 megabytes (HP 7937). Each data surface uses a movable read/write head to service its data tracks. The bottom surface of the lowest disc in the stack contains prerecorded servo code which is used to position the read/write heads over the desired data track.

Head positioning is performed by a rotary actuator and a dual closed-loop servo positioning system. Control of the servo system is derived from the dedicated servo code on the servo surface and also from servo code embedded between data sectors on all of the data surfaces.

Mechanical and contamination protection for the discs, heads, and rotary actuator is achieved by enclosing these components in the sealed head-disc assembly. The head-disc assembly includes a self-contained air filtration system which supplies clean air and equalizes temperature throughout the HDA.

A self-contained power supply in the drive supplies dc voltages to the controller and the drive electronics. The standard drive is configured for operation from a 90-132V, 60 Hz power source. Options 015 and 017 permit operation from 50 Hz and 180-264V, respectively.

The drive is contained in an enclosed housing and is fitted with removable covers to permit easy access for servicing. A total of two drives can be installed on the rack slides of a desk-height HP 19511A Cabinet. See figure 1-1. An HP 19512A Rack Slide Kit is available for mounting the drive in an EIA 19-inch rack cabinet. A special lifter tool makes it possible for one person to install the 56.7 kg (125 lb) drive in either cabinet.

An upgrade kit is available for the drive: HP 97521A Controller Cache Upgrade.

Self-test diagnostics and a fault-finding system contained within the drive exercise key functions of its operation. Self test is performed automatically at power on and also can be initiated by the host. Drive status is indicated by three light-emitting diodes (LEDs) on the front panel. See figure 3-1. In the event of a self-test failure, the LEDs will identify the failed subassembly in the drive.

1-3. DOCUMENTATION SUPPLIED

The drive is supplied with one each of the following publications:

- *HP 7936 and HP 7937 Disc Drives Operating and Installation Manual*, part no. 07937-90902
- *Site Environmental Requirements for Disc/Tape Drives Manual*, part no. 5955-3456

1-4. SUPPORTING DOCUMENTATION

The following supporting documentation for the drive may be ordered from your nearest Hewlett-Packard Sales and Support Office:

- *HP 7936 and HP 7937 Disc Drives Hardware Support Manual*, part no. 07937-90903
- *CS/80 Instruction Set Programming Manual*, part no. 5955-3442
- *CS/80 External Exerciser Manual*, part no. 5955-3462

1-5. PRODUCT STRUCTURE

The drive product structure is outlined in Table 1-1.

1-6. SPECIFICATIONS

Specifications for the drive are listed in the *Site Environmental Requirements for Disc/Tape Drives Manual*, part no. 5955-3456. This manual is supplied with the drive.

1-7. SERIAL NUMBER

The serial number of the drive is recorded on a serial number label attached to the front cover of the drive, below the front panel. The drive model number and full serial number should be quoted in any communication with Hewlett-Packard regarding the drive.

1-8. SUPPORTED EQUIPMENT

This manual is intended to provide the information needed to support service of the drive and all of its accessories and options.

1-9. TEST EQUIPMENT REQUIRED

No special test equipment is needed for installation and normal maintenance of the drive. However, when using the special diagnostics available for troubleshooting the drive, the following equipment is needed:

- HP 85B Personal Computer
- CS/80 External Exerciser Tapes, part numbers 5010-0566 and 5010-0567.
- *CS/80 External Exerciser Manual*, part no. 5955-3462.

1-10. WARRANTY

The drive is covered by a 90-day Hewlett-Packard warranty. However, this warranty is voided if the sealed head-disc assembly is opened or otherwise tampered with. The warranty does not include installation or rack mounting.

1-11. SUPPORT STRATEGY

The drive may be repaired on site to the field replaceable assembly level. Troubleshooting is aided by firmware controlled self-test diagnostics with the malfunctioning assembly identified on a front-panel display, error codes returned by the drive to the CPU, and diagnostics available through the use of the HP 85B Personal Computer and an external exerciser or a host-supported external exerciser.

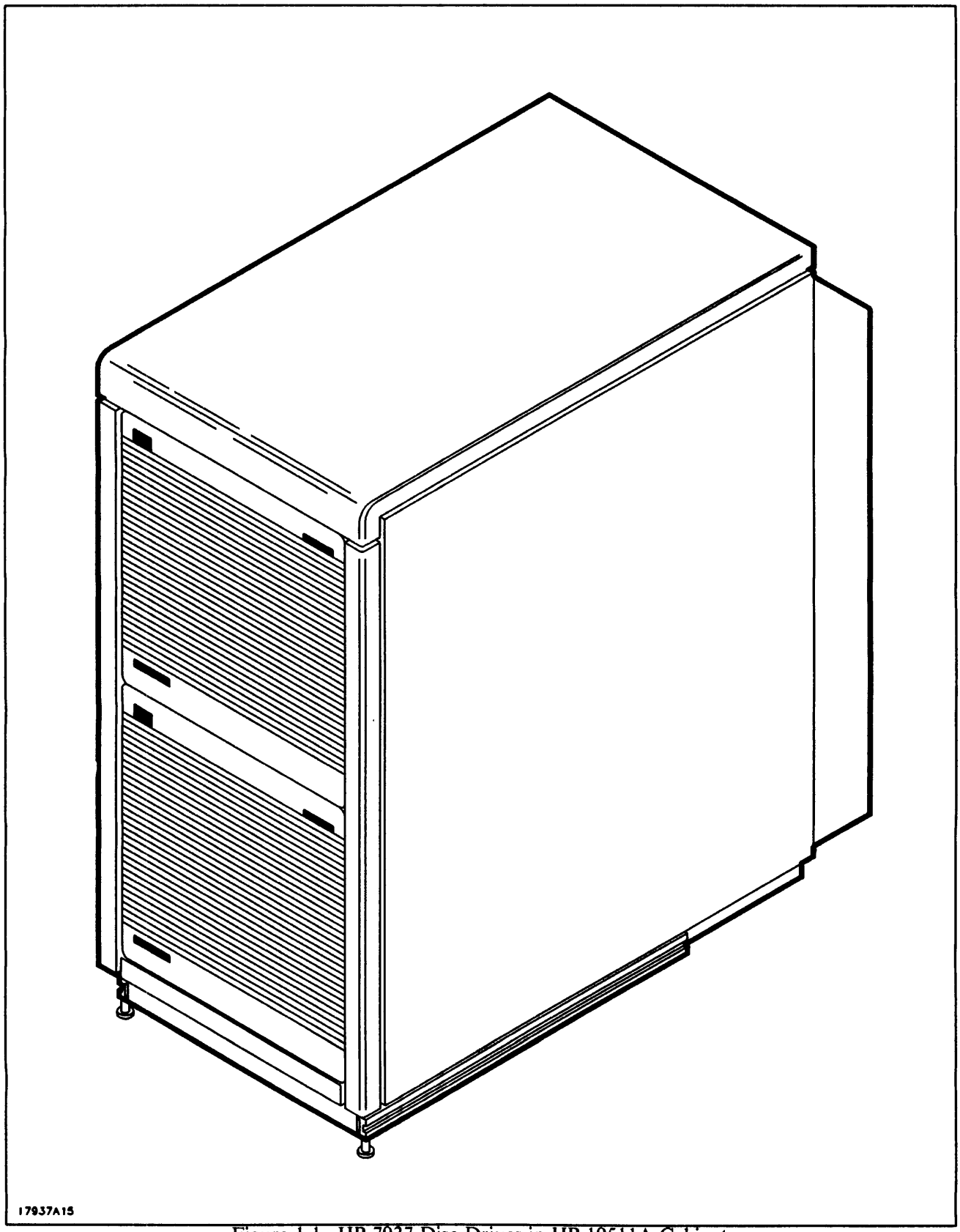


Figure 1-1. HP 7937 Disc Drives in HP 19511A Cabinet

Table 1-1. Disc Drive, Product Structure

DISC DRIVE

HP 7936H/7937H - 307/571 Mbyte Disc Drive, HP-IB Controller

HP 7936XP/7937XP - 307/571 Mbyte Disc Drive, HP-IB Controller with Cache

CABINET

HP 19511A - Desk-height Cabinet for up to two 7936/7937 Disc Drives.

CABINET OPTIONS

208 - Adds 07937-60214 Power Tap to HP 19511A Cabinet. Designed for environments using NEMA 6-30R power receptacles (208 Vac, 60 Hz).

RACK SLIDE KIT

HP 19512A - Rack Slide Kit for mounting a 7936/7937 Disc Drive in an EIA 19-inch rack cabinet

POWER OPTIONS

015 - 50 Hz operation

017 - 180-264 Vac operation

UPGRADE KITS

HP 97521A - HP-IB Cache Controller

Site Planning and Requirements 2

2-1. INTRODUCTION

This chapter defines site preparation and requirements needed to ensure a proper operating environment for the drive.

2-2. SITE PLANNING

No site preparations are required for the drive other than those specified for the host system.

2-3. SPECIFICATIONS

Detailed electrical, environmental, and physical specifications for the drive are provided in the *Site Environmental Requirements for Disc/Tape Drives Manual*, part no. 5944-3456. This publication is supplied with the drive.

NOTE

In order for the drive to operate properly, it must be operated within the environmental specifications given in the above mentioned publication.

Detailed dimensional specifications for the drive are given in figure 12-1. The dimensions of the HP 19511A Cabinet are shown in figure 12-2.

2-4. CABLING LIMITATIONS

The drive adheres to the cabling limitations set forth in the interface documentation applicable to the controller installed in the drive. This documentation is listed in chapter 1.

Installation And Configuration 3

3-1. INTRODUCTION

This chapter contains a summary of drive installation information, compiled for use by service-trained personnel. For detailed installation information, including unpacking instructions, cabinet installation procedures, input voltage and frequency configuration, and initial checkout tests, refer to the *HP 7936 and 7937 Disc Drives Operating and Installation manual*, part no. 07937-90902.

WARNING

The drive does not contain operator-serviceable parts. To prevent electrical shock, refer all maintenance activities to service-trained personnel.

3-2. SHIPPING LATCH

CAUTION

Do not operate the Shipping Latch when the drive LINE~ switch is in the 1 (in) position. The drive must be in a powered-down state before the latch is moved.

Do not attempt to operate the drive with the Shipping Latch in the ■ (Ship) position. If the drive is powered up with the latch in the ■ position, a servo fault will occur (Red and Yellow LEDs illuminated). To recover from this situation, power down the drive, move the latch to the ▌ (Operate) position, and then power up the drive.

The drive shipping latch prevents the drive head-disc assembly from being damaged by vibration and shock during shipment and installation of the drive. The latch is located behind the rear panel and can be activated by a medium-sized flat-blade screwdriver through a rectangular opening in the rear panel. See figure 3-1.

The latch settings are indicated by symbols on the latch, visible through the rectangular opening. The ■ symbol is the "Ship" setting and the ▌ symbol is the "Operate" setting. The latch must remain in the ■ (Ship) position until the drive is installed at its operating location and is ready to be powered on. At this time, the latch should be set to the ▌ (Operate) position and then the drive powered on.

NOTE

If the latch is inadvertently moved to the ■ (Ship) setting after the drive is powered on, the latch may overshoot the ■ (Ship) setting. (The latch is in an overshoot state if the ■ (Ship) symbol moves to the right, past the range of visibility of the rectangular opening.)

If an overshoot occurs, the drive will continue to operate normally as long as power is not turned off. However, to ensure that data is not destroyed, the following procedure should be performed immediately to reset the latch:

1. Power down the drive by setting the LINE~ switch to the 0 (out) position.

2. Disconnect the HP-IB connector.

3. Power up the drive.

4. Wait for the drive to finish its internal self-test diagnostic routine (approximately 10 seconds).

5. Insert the tip of a small flat-blade screwdriver through the round overshoot opening in the rear panel (see

figure 3-1) and return the latch to the | (Operate) position.

6. Power down the drive.

7. Reconnect the HP-IB connector.

8. Power up the drive.

3-3. DRIVE INSTALLATION

WARNING

Anti-tip feet must be in position on the cabinet when the drive is installed and any time the drive is extended out of the cabinet on its rack slides.

A total of two drives can be installed in the HP 19511A Cabinet or up to four drives can be installed in a EIA 19-inch rack cabinet using HP 19512A Rack Slide Adapter Kits. A special lifter tool, part no. 07937-60141, allows one person to install the drive in either cabinet. For instructions on how to install the drive in the HP 19511A Cabinet and EIA rack cabinet, refer to the *HP 7936 and HP 7937 Disc Drive Operating and Installation Manual*, part no. 07937-60602.

3-4. PRIMARY POWER REQUIREMENTS

CAUTION

Do not operate a drive configured for 90-132 Vac on 180-264 Vac, or vice versa. Also, do not operate a drive configured for 60 Hz on 50 Hz, or vice versa. Failure to observe these precautions may result in damage to the drive.

The drive has been factory preset for the proper line voltage and frequency in your area. The standard model is configured for an ac input of 90-132 Vac, 60 Hz and a drive with option 017 is configured for an input of 180-264 Vac, 60 Hz. A drive with option 15 is configured for an input of 50 Hz.

The voltage and frequency for which the drive has been configured at the factory is marked on the ~LINE label attached to the rear panel of the drive. The location of the label is shown in figure 3-2. Make sure that your power source meets the requirements marked on the label.

Voltage configuration (standard/option 017) is accomplished within the drive by moving plug-in connectors in power supply PCA-A4 and primary power PCA-A8.

Frequency configuration (standard/option 015) is accomplished by changing the spindle motor pulley and drive belt.

Details of how to change the drive voltage and/or frequency configuration are provided in the *HP 7936 and HP 7937 Disc Drive Operating and Installation Manual*, part no. 07937-90902.

3-5. CONTROLS, INDICATORS, AND CONNECTORS

The drive front and rear panel controls, indicators, and connectors are identified in figure 3-1. The functions of these components are described in the following paragraphs.

3-6. LINE~ SWITCH

The LINE~ switch controls the application of ac power to the drive. Power is "on" when the switch is in the 1 (in) position and "off" when it is in the 0 (out) position. The 1 and 0 markings correspond to international symbology presently in use.

3-7. CHANNEL ADDRESS/DIAGNOSTIC SWITCH

The Channel Address/Diagnostic switch is a 4-segment switch assembly which selects the system channel address and the drive self-test diagnostics. The switch segments are read by the controller at power-on. The segments can be set with any sharp-pointed tool, such as the tip of a ball point pen.

CHANNEL ADDRESS switch segments S2, S3, and S4 permit the selection of one of eight unique channel addresses. The address settings, 0 through 7, are shown on the Channel Address/Diagnostic Switch label on the rear panel. See figure 3-2. Switches S2, S3, and S4 can also be used to initiate diagnostic tests. (This function is not implemented in the drive at this time.)

DIAGNOSTIC SWITCH segment S1 selects which internal diagnostic routine the drive will execute at power-on. The two diagnostic modes are described in the following paragraphs.

3-8. RUN TIME MODE. When switch S1 is set to the RUN TIME MODE position, a series of hardware tests are performed at power-on. Following successful completion of the hardware diagnostic routines, the drive comes on line. The diagnostic normally takes approximately 10 seconds to complete.

Successful completion of the diagnostic is indicated by the Green LED remaining lit. If the drive fails the hardware diagnostic, the Red LED will remain lit and the Yellow and Green LEDs will be coded to indicate the malfunctioning assembly. A power supply failure or loss of input power is indicated by all LEDs extinguished. The coding for the LEDs is shown on a label on the rear panel. See figure 3-2.

NOTE

A drive fault condition (Red LED lit) does not necessarily mean that the drive controller is incapable of communication with the host. In most cases, details of the fault condition (over and above the information encoded by the LEDs), can still be obtained by commands from the host. Refer to Chapter 8 for details.

3-9. DIAGNOSTIC MODE.

NOTE

The DIAGNOSTIC MODE position is for service purposes and should not be used during normal operation of the drive.

If S1 is set to the DIAGNOSTIC MODE position, the same hardware diagnostic executed in RUN TIME MODE is invoked when power is applied. However, the controller does not bring the drive on line following the completion of the hardware diagnostic routines. Instead, the drive performs a full-volume RO ERT (7.5 minutes) followed by a continuous loop of random RO ERTs.

When the drive successfully completes the hardware diagnostics and begins the RO ERTs, both the Yellow and Green LEDs will be illuminated. If any uncorrectable or marginal data errors occur during the RO ERTs, the Green LED is extinguished leaving only the Yellow LED lit.

A hardware diagnostic failure is indicated by the Red LED remaining lit and the Yellow and Green LEDs coded to indicate the source of the most likely malfunctioning assembly. A power supply failure or loss of input power is indicated by all LEDs extinguished. The coding for the LEDs is listed on a label on the rear panel. See figure 3-2.

When the DIAGNOSTIC MODE position is selected, the drive will not come on line (be capable of communication with the host) until the Power switch is turned off, switch S1 returned to the RUN TIME MODE position, and the drive powered on again.

NOTE

Failure information gathered during this time will be logged in the internal error logs of the drive. Refer to Chapter 8 for details on how to retrieve this data.

3-10. LED DISPLAY

The front panel LED display provides the operator with a visual indication of the operational status of the drive. The LED display consists of single red, green, and yellow LEDs. As explained in the preceding paragraphs, the significance of the LED patterns is determined by the operating mode of the drive (RUN TIME or DIAGNOSTIC). The Front Panel Status label affixed to the rear of the drive indicates the significance of the LED patterns (see figure 3-2).

In addition to its role as a status display, the Green LED also serves as an activity indicator, flashing any time the drive is exchanging data or commands with the host.

3-11. HP-IB CONNECTOR

The HP-IB connector provides the mechanical connection for the HP-IB cable which connects the host and the drive.

3-12. POWER FUSE

WARNING

The power fuse is not an operator-serviceable part and should only be replaced by service-trained personnel.

The power fuse protects the drive from an ac power overload. The same fuse is used regardless of the input operating voltage. The fuse value is listed below.

OPERATING VOLTAGE	FUSE DESCRIPTION	HP PART NO.
All	5AS - 250V	2110-0030

3-13. LINE CONNECTOR

The line connector allows the drive to be connected to an ac power source via a suitable power cord. The input power configuration of the drive is listed on the ~LINE label.

3-14. CPU CONNECTION - HP-IB SYSTEMS

CAUTION

Do not connect or disconnect the HP-IB cable(s) from the drive while the system is in active state.

The interconnection of the drive is dependent on the system configuration. The location of the HP-IB connector for the drive is shown in figure 3-1. The major considerations concerning the connection of the drive to an HP-IB channel are contained in the following paragraphs.

3-15. HP-IB CABLING

The Hewlett-Packard Interface Bus (HP-IB) has certain rules which must be observed or successful installation of the drive. Cabling is limited to 1 metre per HP-IB load. Typically the Central Processing Unit (CPU) is 7 equivalent loads and the drive is 1 equivalent load. See figure 3-3.

The CPU adheres to an HP standard which allows 7 metres of HP-IB cable between the CPU and the nearest device connected to it and 1 metre of cable between each additional device. The maximum configuration is 8 devices (excluding the CPU) per HP-IB channel of a maximum of 15 metres of 10 equivalent loads.

NOTE

The maximum number of devices that can be connected to a single HP-IB channel is host dependent. This information is contained in the appropriate host configuration guide.

3-16. HP-IB DEVICE ADDRESS

The Channel Address switches located on the rear panel of the drive are used to set the HP-IB device address. See figure 3-1. The switches permit setting one of eight unique addresses. The switches can be set with any pointed tool. When setting the HP-IB address, disregard any markings on the switch body. Set the switches according to the information on the Channel Address/Diagnostic switch label. See figure 3-2.

NOTE

Before using the drive, check the address switches to ensure that no two devices in the system have the same address.

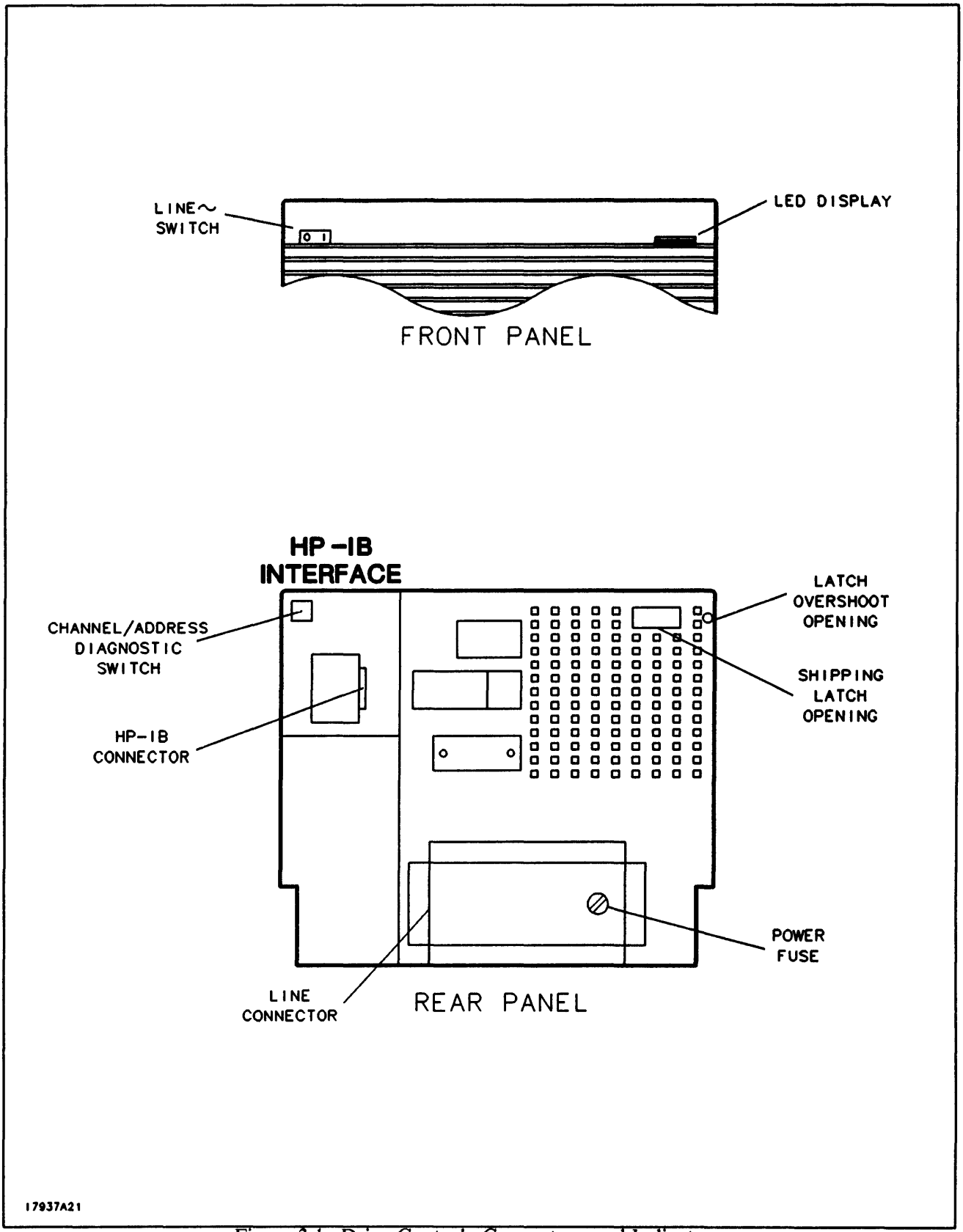


Figure 3-1. Drive Controls, Connectors, and Indicators

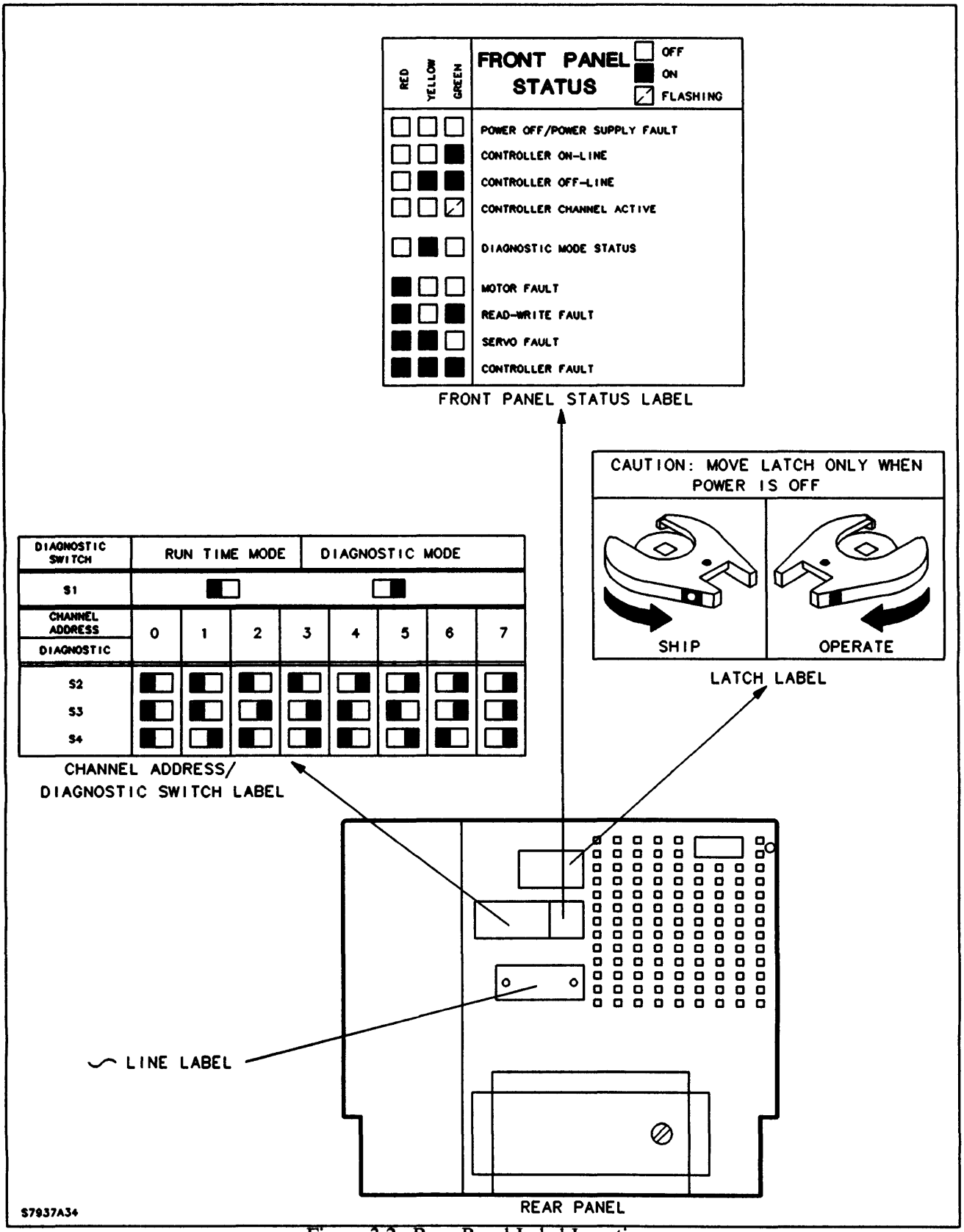
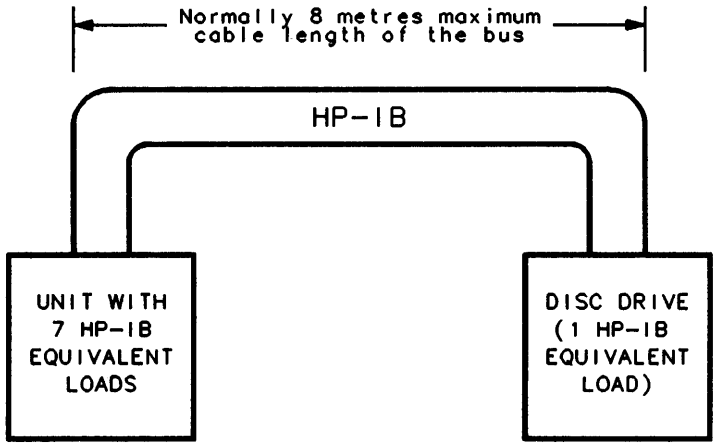
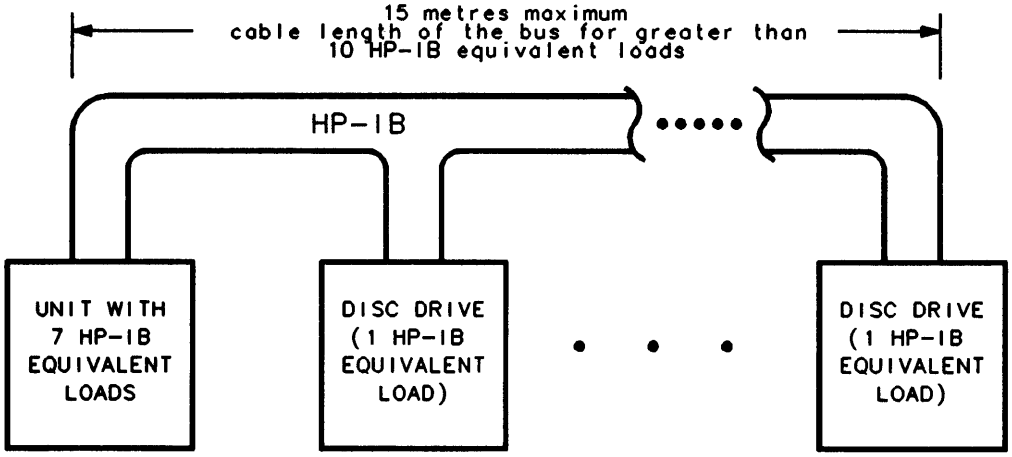


Figure 3-2. Rear Panel Label Locations



SINGLE DRIVE INSTALLATION



1 metre X n loads = cable length in metres (up to 15 metres maximum)

MULTIPLE DRIVE INSTALLATION

NOTES:

1. The maximum number of drives that can be connected to a single HP-IB channel is host dependent. This information is is contained in the appropriate host configuration guide.

17937A11

Figure 3-3. Maximum Cable Length for HP-IB Channel

Preventive Maintenance 4

4-1. INTRODUCTION

WARNING

The drive does not contain operator-serviceable parts. To prevent electrical shock, refer all maintenance activities to service-trained personnel.

No preventive maintenance procedures are required to be scheduled for the drive.

Functional Description 5

5-1. INTRODUCTION

The HP 7936 and HP 7937 Disc Drives are high performance, random access, data storage devices designed for use in medium-and large-sized computer systems. In this chapter, unless otherwise specified, "drive" refers to all models of the HP 7936 and HP 7937.

The drive is housed in a rigid enclosure designed to be mounted on rack slides in a cabinet. Contained within the enclosure is a sealed head-disc assembly (HDA), with spindle and disc stack, read/write heads, servo head, electromagnetic head positioning mechanism (actuator), read preamplifiers, write drivers, head gain reference PROM and DAC, and air filtration system. See figure 5-16. The spindle is belt driven by an ac induction motor mounted adjacent to the sealed HDA. The motor speed is regulated by the line frequency. This motor also drives a squirrel-cage type cooling fan.

The disc stack is composed of seven 210-millimetre (8.3-inch) diameter nonremovable discs. These discs have seven (HP 7936) or 13 (HP 7937) thin-film magnetic surfaces for data storage. (The same number of discs are used in both drives in order to maintain the dynamic design parameters of the head-disc assembly.) The formatted storage capacity of the drive is 307 megabytes (HP 7936) or 571 megabytes (HP 7937). One movable head is used to service each surface. The bottom surface of the lowest disc in the stack contains prerecorded dedicated servo code which is used to generate timing and seeking information. When on track, embedded servo code prerecorded between data sectors on all of the data tracks is sampled to keep the heads on track.

In addition to head-disc assembly A3, a number of printed-circuit assemblies (PCAs) are contained within the enclosure. These include servo PCA-A1, read/write PCA-A2, power supply PCA-A4, power distribution PCA-A5, controller PCA-A6, LED PCA-A7, and primary power PCA-A8.

Servo PCA-A1 contains a servo controller, phase-locked loop (PLL) and servo timing counters, dedicated servo circuit, sampled (embedded) servo circuit, and servo power amplifier. These circuits provide sector timing information, control seeks, and maintain the heads on track.

Read/write PCA-A2 includes a custom-designed read/write controller that, together with associated read chain, write chain, and head select electronics, transfers data to and from the disc media. The PCA also maintains data communication with controller PCA-A6, and performs amplification of the sampled and dedicated servo codes.

Power supply PCA-A4, in addition to supplying DC voltages for the controller and drive electronics, provides power-on reset and power fail signals.

Power distribution PCA-A5 filters and distributes the outputs from power supply PCA-A4 to the controller and drive electronics.

Controller PCA-A6 is a factory-installed microprocessor-based controller which provides an interface to the host computer. Two different HP-IB controllers are available for this purpose. In the HP 7936H and HP 7937H Disc Drives, interface to the host is via an Hewlett-Packard Interface Bus (HP-IB) controller. In the HP 7936XP and HP 7937XP, the controller has HP-IB Cache added. (In this manual, the controllers are identified collectively as PCA-A6.) Both controllers interface with the drive electronics via an HP-developed standard interface (ESI).

Self-test diagnostics and fault-finding firmware contained within the controller PCA-A6 exercise key functions of drive operation. Self test is performed automatically at power on and can also be initiated by the host. Drive status is indicated by three LEDs mounted on the front panel. In the event of a self-test failure, this LED display identifies the most likely failed assembly within the drive.

LED PCA-A7 contains three light-emitting diodes (LEDs) that signal to the user the operating status of the drive.

Primary power PCA-A8 contains the drive LINE~ switch and the spindle motor start capacitor and control relay. Also mounted on PCA-A8 are connectors that facilitate the changeover of the spindle motor wiring when the drive power configuration is changed from 90-132 Vac to 180-264 Vac, or vice versa.

5-2. BLOCK DIAGRAMS

A basic block diagram (figure 5-16) for the controller and drive electronics is provided in this chapter. Functional block diagrams (figures 12-20 through 12-23) for the servo, read/write, spindle, and power supply systems within the drive are located in chapter 12. A functional block diagram for the two HP-IB controllers available for use in the drive is contained in Appendix A at the rear of the manual.

In order to facilitate text and table references to the functional block diagrams in chapter 12 and the appendixes, each diagram is identified by two large characters in the lower right-hand corner of the page. For example, the read/write system diagram is identified with the characters **RW**. These characters are boxed in the text and tables thus: RW.

The diagrams are identified as follows:

CR = Figure A-3, Controller, Functional Block Diagram, in Appendix A.

NOTE

Appendix A describes the two HP-IB controllers available for use in the drive. Refer to figure A-3 when CR is used in this chapter to identify the functional block diagram for controller PCA-A6.

S1 = Figure 12-20. Servo System, Functional Block Diagram (Sheet 1 of 2)

S2 = Figure 12-20. Servo System, Functional Block Diagram (Sheet 2 of 2)

RW = Figure 12-21. Read/Write System, Functional Block Diagram

NOTE

The numbers which identify the test points in the servo and read/write functional block diagrams are the pin numbers on the read/write and servo test PCAs. Refer to chapter 8 for details.

SD = Figure 12-22. Spindle Drive System, Functional Block Diagram

PS = Figure 12-23. Power Supply System, Functional Block Diagram

5-3. SIGNAL NOTATION

In the controller and drive logic circuits, a digital signal is applied to its destination in one of two states: active or inactive. The signal is active when its voltage level (high or low) makes the action occur for which the signal was designed. This action is usually identified by a signal mnemonic. A mnemonic with an "-L" suffix indicates a logic signal with an active low voltage level. A mnemonic with an "-H" suffix indicates a logic signal with an active high voltage level. Signal mnemonics without an "-L" or "-H" suffix usually indicate analog, data bus, or control bus signals.

5-4. LIST OF MNEMONICS

The mnemonics used in the functional block diagrams and accompanying text are defined in table 5-1. The **SOURCE** column of table 5-1 gives the identification characters for the functional block diagram where the signal appears, followed by the number of the assembly where the signal originates.

The following assembly numbers appear in the **SOURCE** column of table 5-1:

A1 = Servo PCA-A1
A2 = Read/Write PCA-A2
A3 = Head-Disc Assembly A3
A4 = Power Supply PCA-A4

A5 = Power Distribution PCA-A5
A6 = Controller PCA-A6
A7 = LED PCA-A7
A8 = Primary Power PCA-A8

Certain of the signals listed in table 5-1 may be monitored with test PCAs that can be connected to servo PCA-A1 and read/write PCA-A2. Refer to chapter 8 for details. In the **SIGNAL** column of table 5-1, the servo test signals are identified with an asterisk (*), and the read/write test signals with a double asterisk (**).

In the **DESCRIPTION** column of table 5-1, the circuits listed in upper case (capital) letters are blocks in the functional diagrams.

5-5. DISC FORMAT

Each data surface is divided into a number of concentric circles called tracks. See figure 5-1. From the outer diameter (OD) of the disc to the inner diameter (ID), there are a number of OD guard band tracks, one OD maintenance track, three spare tracks, 1396 user data tracks, three spare tracks, one ID maintenance track, a number of ID guard band tracks, and a landing zone.

The OD guard band is used for calibration. Both the OD and ID guard band tracks allow for overshooting when seeking to the outermost and the innermost data tracks. The maintenance tracks contain service information including run time error logs, fault log (data surface 0 only), and error rate test logs. See figure 5-2. The maintenance tracks are also used when reading and writing during self test. The data tracks are used for reading and writing host data. The spare tracks are used for sparing out any data tracks containing media defects. The head comes to rest on the landing zone when power is removed from the drive.

Each data track is organized into smaller sequentially-numbered blocks of data called sectors. On each track, there are 124 of these physical sectors, with each sector having 256 bytes of data. See figure 5-3.

In addition to the 256 bytes of data, each sector contains a 14-byte sync field, a 6-byte header, a 2-byte CRC field, a 12-byte ECC field, a data gap, a servo field, and a servo code field.

The 14-byte formatter/separator field and the 6-byte header field comprise a 20-byte preamble. This information is used for synchronization and addressing purposes. The header field specifies status, head, cylinder, and sector addresses, and provides the spare sector information. The head and cylinder are logical addresses and the spare sector and sector bytes are physical addresses. The status byte is used to determine whether a spare is classified as primary (factory) or secondary (field). If bit 6 of the status byte is zero, the sector is spared secondary; if 1, the sector is spared primary. If bit 7 of the status byte is zero, the entire track has been field spared; if 1, the track has been spared primary.

The data field is used to store 256 bytes of data. Only the data field is transferred from the system during most data operations. The preamble and the postamble are checked by controller PCA-A6.

The 2-byte CRC field and 12-byte ECC field form a 14-byte postamble. Controller PCA-A6 generates the CRC and ECC information during a write operation and appends it to the other information written in the sector. The check information itself depends on the value of every bit from the first bit in the header field to the last bit in the data field. During a read operation, this check information is regenerated and compared in such a way that the presence of errors is detected. The controller ECC firmware corrects any data errors detected by the hardware in the background while the hardware is busy transferring subsequent sectors in a multiple-sector transfer. In most cases, this scheme will result in no loss of performance for correctable data errors.

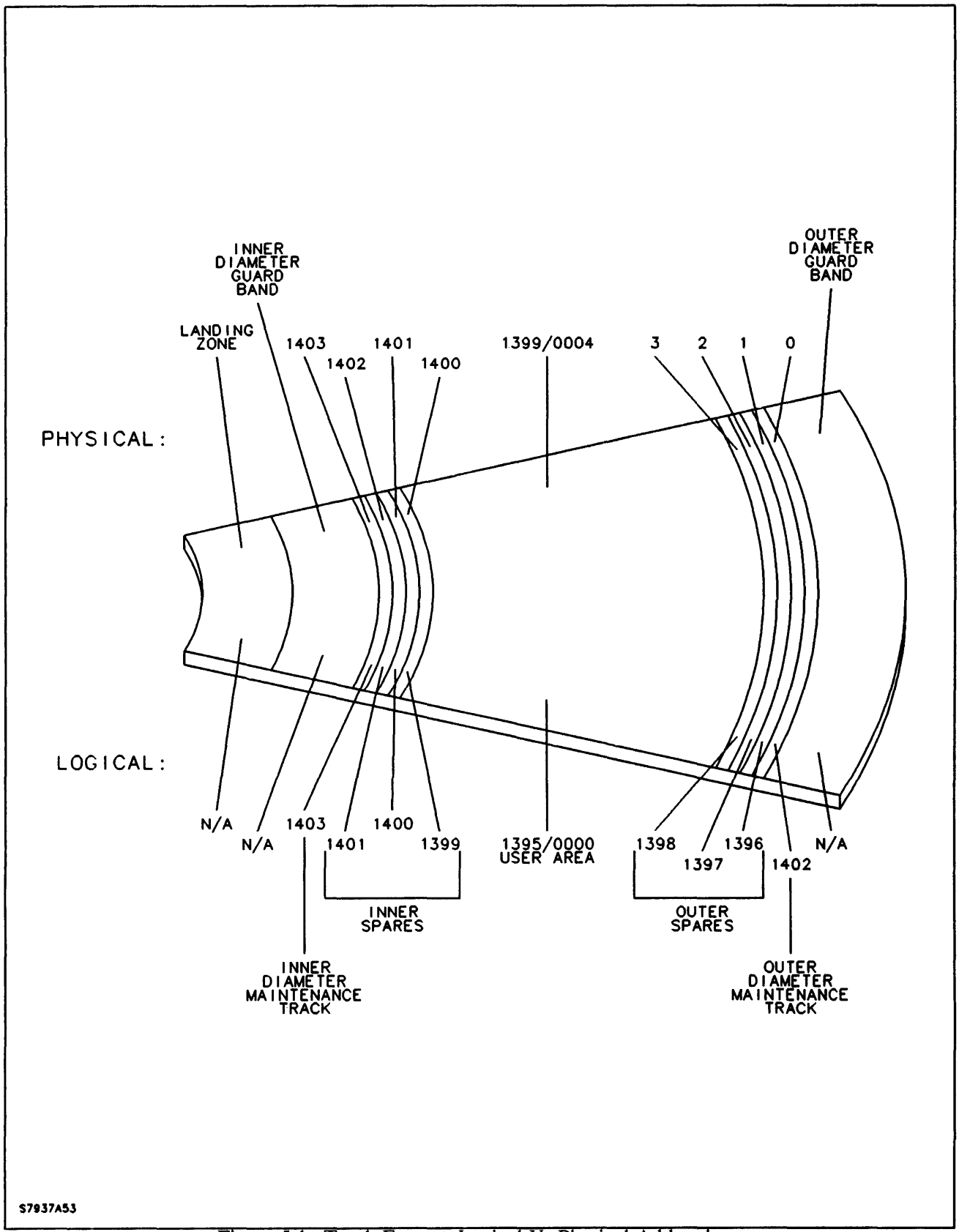


Figure 5-1. Track Format, Logical Vs Physical Addressisng

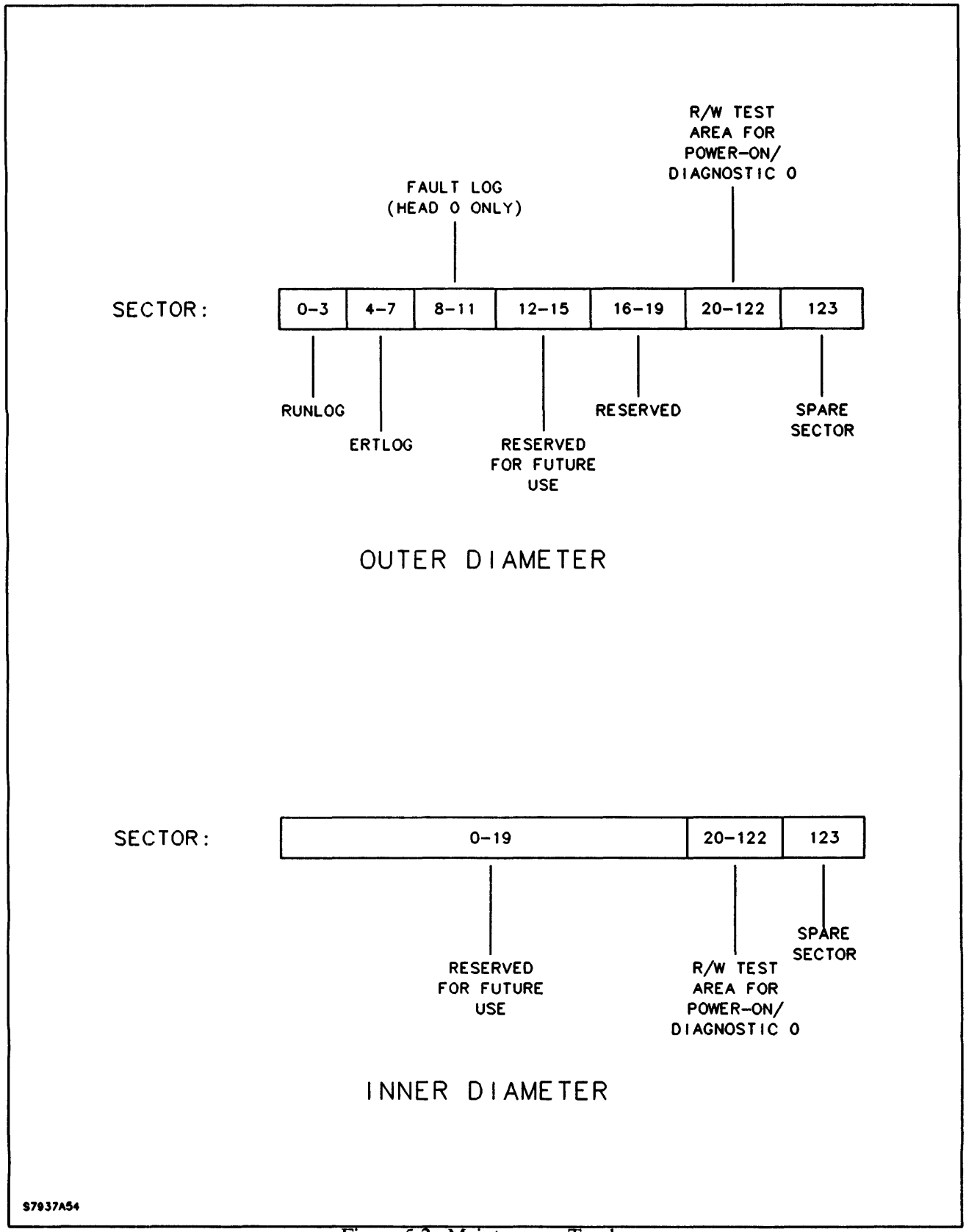
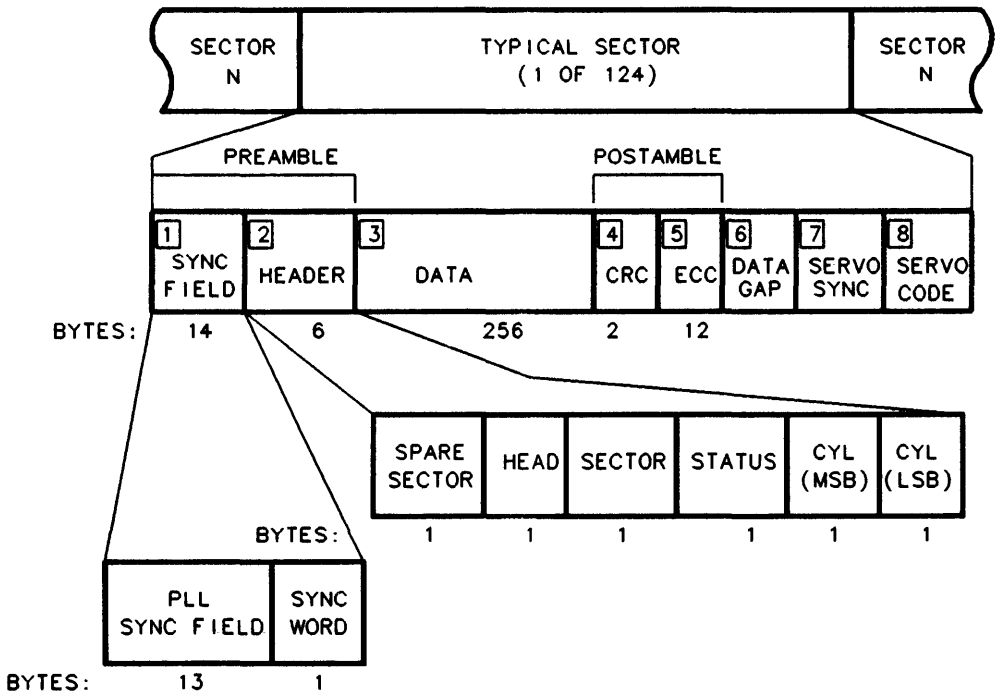


Figure 5-2. Maintenance Tracks



1	SYNC FIELD	FOR SYNCHRONIZATION OF READ CIRCUIT PHASE-LOCKED LOOP (PLL).
	• PPL SYNC FIELD	TO ACHIEVE PHASE LOCK.
	• SYNC WORD	SIGNALS START OF DATA FIELD.
2	HEADER	STATUS AND ADDRESS INFORMATION.
	• SPARE SECTOR	PHYSICAL ADDRESS OF SPARED SECTOR ON TRACK. (WILL BE 123 IF NO SECTOR SPARING DONE.)
	• HEAD	LOGICAL HEAD ADDRESS.
	• SECTOR	PHYSICAL SECTOR ADDRESS.
	• STATUS	TRACK STATUS. BIT 7: 1=PRIMARY TRACK SPARE; 0=SECONDARY TRACK SPARE. BIT 6: 1=PRIMARY SECTOR SPARE; 0=SECONDARY SECTOR SPARE.
	• CYL (MSB)	LOGICAL CYLINDER ADDRESS (MSB).
	• CYL (LSB)	LOGICAL CYLINDER ADDRESS (LSB).
3	DATA	READ/WRITE DATA.
4	CRC	CYCLIC REDUNDANCY CHECK. ERROR CHECKING INFORMATION.
5	ECC	ERROR CORRECTION CODE. ERROR CHECKING AND CORRECTIONS. ECC WILL CORRECT UP TO SIX DATA BYTES PER SECTOR. THE BYTES NEED NOT BE CONTIGUOUS.
6	DATA GAP	ALLOWS TIME TO SWITCH FROM WRITE MODE (DURING A WRITE) TO READ MODE WHILE SEPARATING DATA FROM SERVO INFORMATION.
7	SERVO SYNC	CONTAINS A QUALIFICATION PULSE AND A SYNC PULSE TO TRIGGER THE START OF SAMPLED SERVO READING.
8	SERVO CODE	SAMPLED SERVO CODE.

S7937A13

Figure 5-3. Sector Format

The data gap, servo sync, and servo code fields which follow the postamble comprise the sampled (embedded) servo data. This code is described in more detail in the description of the servo system electronics.

5-6. ADDRESSING STRUCTURE

The head-disc assembly in the HP 7936 contains seven data surfaces, with the data being accessed with seven read/write heads. See figure 5-4. The HDA in the HP 7937 contains 13 data surfaces, with data being accessed with 13 read/write heads.

Head positioning information and sector clocking are derived from the dedicated servo surface through the read-only servo head. There are 1396 ensured cylinder positions available for data storage (HP 7936 and HP 7937). Cylinder addresses range from 0 to 1395. Each cylinder consists of seven (HP 7936) or 13 (HP 7937) data tracks, one for each data surface. Tracks are addressed when both cylinder and head addresses are specified. Each data track is divided into 123 logically addressable physical sectors (HP 7936 and HP 7937). Sectors are addressed when both head and sector addresses are specified for a given cylinder. Head addresses range from zero to 6 (HP 7936) or zero to 12 (HP 7937).

All addressing in the drive is logical. Controller PCA-A6 assigns logical addresses to the physical addresses. Figure 5-1 shows logical versus physical track addressing. When a defective physical track is encountered, a new physical track (spare track) will be assigned to the same logical address. This eliminates dual seeks to obtain the the correct data and reduces system overhead in managing the discs and spare tracks. A total of 1396 tracks are guaranteed as logical tracks through the the use of spares, which the controller assigns as required.

There are 124 physical sectors. Of these, 123 sectors (addressed from 0 to 122) are available for data storage and one sector is reserved for use as a spare in the event that one of the original 123 becomes defective. Sectors are spared by the controller. In the event that the spare sector is already used, the entire logical track will then be assigned a new physical address (one of the spare tracks). This sparing action is transparent to the host CPU, except that the host may note the decision to spare, and issue the spare command.

5-7. ADDRESSING MODE

The drive operates in a cylinder mode to access the data storage areas of the drive. In the cylinder mode, the heads are positioned over a particular cylinder and then data is written or read, starting at the lowest numbered head and continuing to the highest numbered head. A cylinder of information consists of all sectors on all tracks at a given cylinder address. Head switching occurs after the data in sector 123 of the current track has been transferred. Head switching is sequential, that is, head 1 will be selected after head 0, and so on. Data transfers will continue with sector 0 of the next track after the address fields and track status indicators of a sector of that track have been verified by the drive.

5-8. DISC SPARING

One sector per track and six tracks per data surface (head) are allocated for sparing bad sectors discovered during data transfers. When performing a sparing operation, controller PCA-A6 attempts a sector spare on the target address (sector). If the allocated spare sector has been used, the entire data track is spared. When sparing, the host has the option of retaining or not retaining data. If the host chooses not to retain data, all data on the target track is destroyed. If the host chooses to retain data, all data on the target track, excluding the sector being spared, is kept.

5-9. SECTOR SPARING

When performing a sector sparing operation that retains data, controller PCA-A6 copies the entire contents of the target track (excluding the defective sector) to the nearest available spare track for temporary storage. The controller then reformats the original track, placing the spare sector into user accessible area and mapping out the bad sector. The data is then copied from the spare track back to the reformatted track with the bad sector being skipped. This shifts all those sectors with logical addresses greater than the bad sector to the next higher sector address. By reformatting the entire

track in this manner, an additional latency is not incurred when accessing a track containing a spared sector.

When reformatting the target track, the controller writes the physical address of the bad sector in the header of each sector on the track. Using this information, the controller knows which sector to skip in subsequent accesses to the track. On tracks that have not undergone a sparing operation, the field in the sector headers contains the physical address of the spare sector (logical sector 123).

5-10. TRACK SPARING

If the spare sector has been used, controller PCA-A6 must copy the entire track on which the defective sector resides to an available spare track. Each data head has 6 spare tracks allocated for this purpose. Like data tracks, these spare tracks are organized into cylinders and, to improve sparing efficiency, are located in two bands on each data surface. See figure 5-1. A spare track table, which is stored in controller RAM, is generated at power on by reading the ID and OD spare pools sequentially until a track is found that has not been spared out. This table is then searched before a seek begins to determine if a particular logical address has been reallocated and if so the address is pulled from the table. To reduce the amount of controller RAM consumed by the spare track table, scalar values, rather than explicit addresses, are used to record the physical location of each spare track. Figure 5-5 shows the relationship of scalar values to physical spare track locations.

When performing a track sparing operation, the controller first determines the nearest (in terms of seek time) from the spare pool. Then the next sequential scalar in the pool is the track that is used in the spare. If the track to be spared resides at logical cylinder 0-697, then the OD spare pool is used (scalar number 39-77). If the track is at cylinder 698-1395, the the ID spare pool is used (scalar number 0-38).

If all of the spare tracks are used up in one of the spare pools, then the next sequential scalar from the opposite spare pool will be chosen.

Defective maintenance tracks are spared automatically by controller PCA-A6. No host intervention is required when sparing a maintenance track.

5-11. CONTROLLER PCA-A6

Controller PCA-A6 provides an interface between the host computer and the drive electronics. One of two available HP-IB controllers is factory installed in the drive mainframe.

Appendix A at the rear of this manual provides details of the controllers, including a functional block diagram and accompanying circuit description. Refer to Appendix A for details of the controller installed in the drive.

NOTE

In this manual, the controllers are referred to collectively as "PCA-A6".

Each controller includes: host interface, a data buffer for data examination and speed matching, disc memory access (DMA) for control of data transfer, error correction (ECC), firmware in read only memory (ROM) for an on-board microprocessor to execute drive commands and monitor status, a peripheral interface for command and status interface with the drive electronics, and channel address/diagnostic control switches. See figure 5-16.

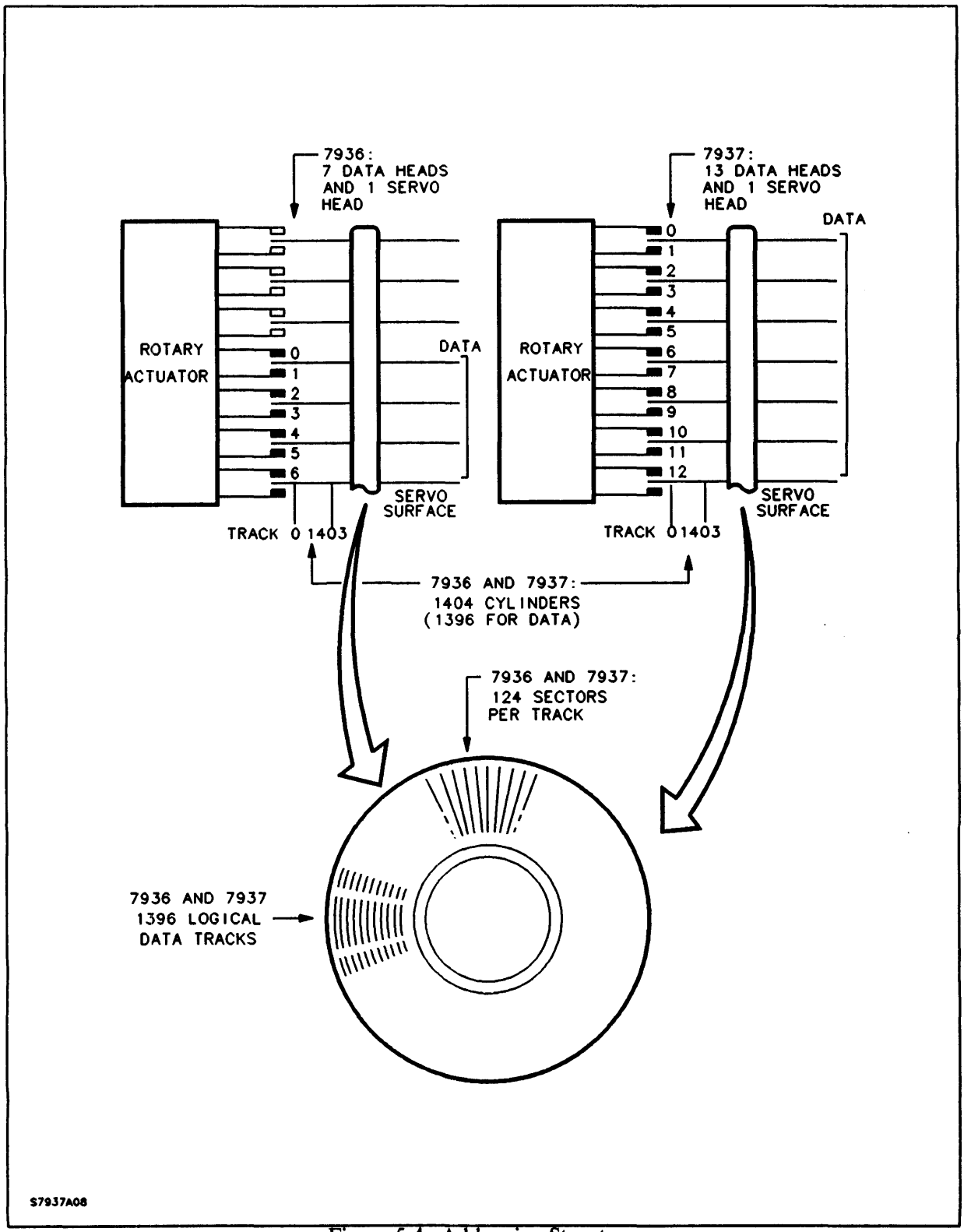


Figure 5-4. Addressing Structure

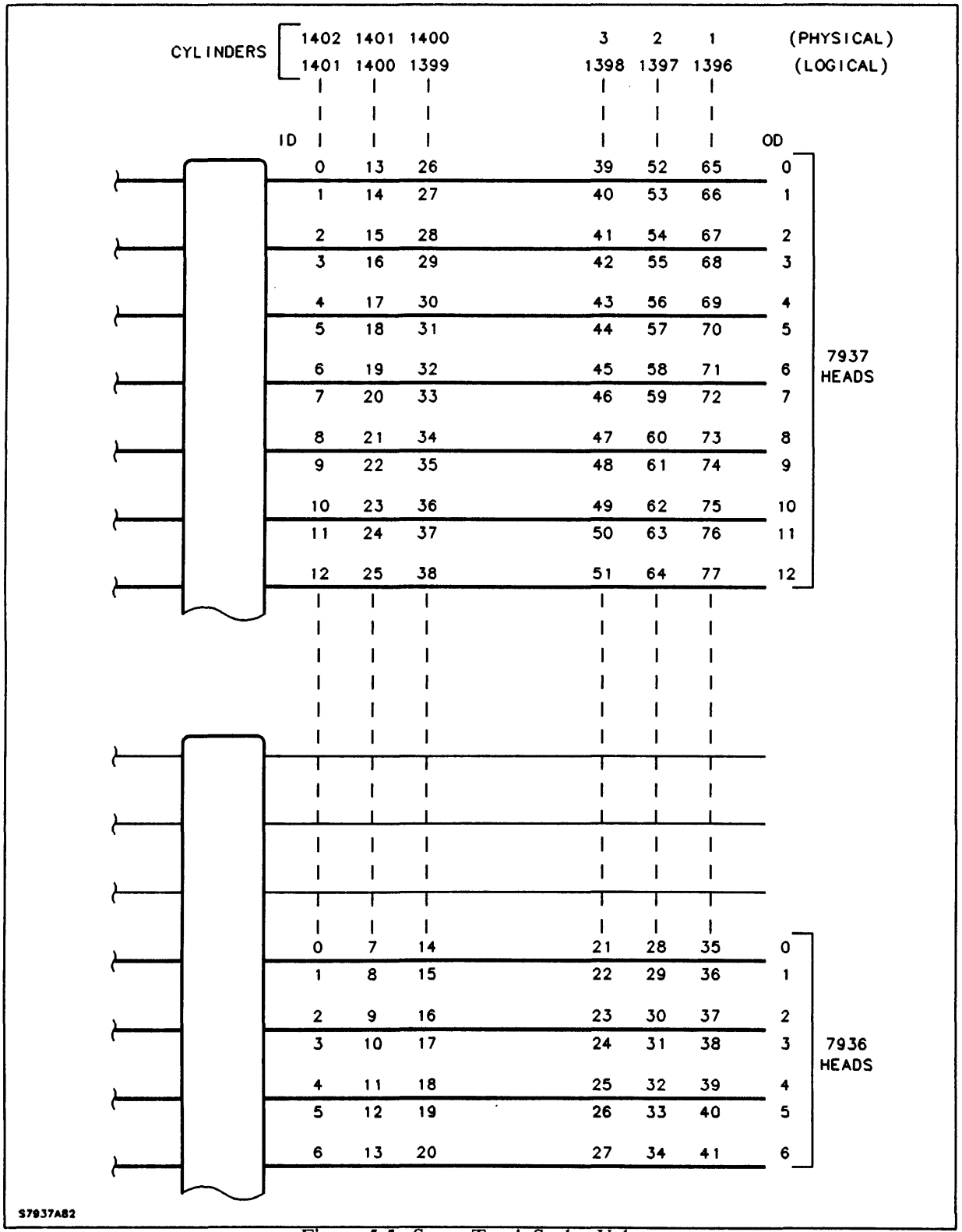


Figure 5-5. Spare Track Scalar Values

Both of the controllers interface to the drive electronics via a standard interface (ESI). This interface consists of a Disc Data Bus, a Data Path Control Bus, and a Servo Control Bus. Each bus is a bidirectional parallel 8-bit bus with associated control and handshake lines. The mnemonics which identify the bus signals are listed below. Refer to table 5-1 for a description of the signal functions.

DISC DATA BUS

DD0-DD7	Disc Data Bus
DDS-H	Disc Data Strobe
SEF-L	Start ECC Field
SOS-L	Start of Sector
WHO-L	Write Hold Off

DATA PATH CONTROL BUS

DPC0-DPC7	Data Path Control Bus
DPA0-H	Data Path Address Zero
DPCS-L	Data Path Control Select
DPIRQ-L	Data Path Interrupt Request
DPRHW-L	Data Path Read High, Write Low

SERVO CONTROL BUS

SD0-SD7	Servo Data Bus
SBF-L	Servo Buffer Full
SDAV-L	Servo Data Available
SPR-L	Servo Processor Reset
SRD-L	Servo Read
SWR-L	Servo Write

The controller also supplies drive signals for the three LEDs in LED PCA-A7 that indicate the operating status of the drive. These signals are labeled Red LED (RLED), Green LED (GLED), and Yellow LED (YLED). The signals reach PCA-A7 via read/write PCA-A2, signal jumper cable W7, power distribution PCA-A5, and power supply output cable W4. See figure PS.

The +5V supply for the LEDs, labeled LED Power (LEDP), originates in read/write PCA-A2, and is connected to PCA-A7 via the same path as the LED drive signals.

5-12. SERVO SYSTEM

Control of the servo system is based on dedicated servo code (prerecorded on the single servo surface) and embedded servo code (prerecorded on all of the data surfaces between data sectors). The servo system follows the specified track while reading or writing and when needed, initiates and controls seeks between cylinders. In addition, the servo system is responsible for determining the type of HDA being addressed (7936 or 7937), monitoring the spindle speed, reporting current servo system status, and interpreting incoming commands from controller PCA-A6.

The servo system makes use of an off-the-shelf microcomputer integrated circuit (servo controller) to provide an interface between the servo system and controller PCA-A6. See figure 5-16. In response to commands passed over the Servo Control Bus, the servo controller interprets incoming commands from PCA-A6 (report HDA type, spin up, recalibrate, seek, report status, report seek time, report present track) and reports servo system information. The servo controller also reports faults in the servo system.

The dedicated servo circuit takes the differential output signal from the servo preamplifier IC, as processed by the dedicated servo AGC amplifier in read/write PCA-A2, and filters the signal to eliminate high-frequency noise. The dedicated servo circuit provides the input to the servo system phase-locked loop (PLL) which supplies the reference timing information needed for writing. The PLL and associated timing circuits also supply timing information needed for position discrimination to allow for the determination of track seeking information during seeking. The dedicated servo circuit also generates an automatic gain control (AGC) voltage which is fed back to the dedicated servo AGC amplifier in read/write PCA-A2. The AGC reference for the dedicated track follower is adjusted by a read-only memory (PROM) and digital-to-analog converter (DAC) on the HDA to compensate for servo gain variations across the disc surface.

The sampled servo circuit takes the differential embedded servo code, as read from the selected read/write head and amplified by the sampled servo AGC amplifier in read/write PCA-A2, to keep the head on track. The sampled servo amplifier is

gated by a switch which allows only sampled servo code to reach the servo circuit. The sampled servo signal is filtered and integrated to create a head position error signal. This signal is fed to the servo power amplifier which in turn supplies drive current to the actuator, to keep the head on track. The sampled servo circuit also generates an AGC voltage for the sampled servo AGC amplifier in read/write PCA-A2. The reference voltage on the AGC amplifier is adjusted by a PROM and DAC on the HDA to compensate for gain variations across the surface of the disc and between different heads.

The position error signal from the sampled servo circuit also drives an off-track detector. If the head is determined to be off track , the servo controller is notified, and takes corrective action. Writing is immediately stopped when an off track condition is detected.

At the request of controller PCA-A6, the servo controller initiates and controls the seek operation that moves the data heads from a known beginning or present head and track location to a desired track location. When the command to seek is received from the controller, the servo controller determines the offset and the appropriate acceleration profile needed to reach the target. The servo controller starts the seek by using the servo power amplifier to move the actuator, at the same time monitoring the movement of the actuator by watching the track crossing information being received from the dedicated servo circuit. The seek profile used is a flattop velocity profile. This implies that the actuator accelerates at a constant rate until it reaches a predetermined maximum velocity, and then coasts at that maximum velocity until the servo power amplifier is again used to decelerate the system. When the heads are within one-half track of target track center, the fine position servo loop is closed. An error position signal from the dedicated servo is used to position the heads on servo track center. Sampled servo from the currently selected head is then used to properly position the head on the data track.

In response to a recalibrate command from controller PCA-A6, the servo controller: a) moves the heads, starting from an unknown velocity and position, to the outer guard band, b) controls the lock up of the servo PLL, c) stops the actuator arm against the crash stop, d) settles on a track in the guard band, e) seeks out of the guard band until track 0 is detected, f) enables Start of Sector SOS-L to the drive electronics, g) enables sampled servo timing acquisition, and h) ends with the drive track following on dedicated track 0.

Parts of the servo system circuitry are located in head-disc assembly A3, read/write PCA-A2, and servo PCA-A1. Details of this circuitry are provided in the following paragraphs.

5-13. HEAD-DISC ASSEMBLY A3

The components of the servo system in head-disc assembly A3 include the dedicated servo code on the dedicated servo surface, sampled (embedded) servo code on all of the data surfaces, servo head, servo read preamplifier/write driver IC, head gain reference PROM and digital-to-analog converter (DAC), drive ID (identification) circuit, speed sensor, and actuator. See figure RW.

5-14. DEDICATED SERVO CODE. The dedicated servo code is used for track-to-track seeking, position recalibrating, as a timing reference for the write clock when writing data, and as a reference when the sampled servo code is written at the factory. In addition, the dedicated servo code contains encoded sector marks, index marks, and guard band marks. The dedicated servo code is divided into three areas: an outer guard band, a data area, and an inner guard band. See figure 5-12.

The servo code in the data area is recorded in 1.7 microsecond "cells", with each cell containing two dibits pairs. The "in-phase" dibit pair (A/B) defines the center of the corresponding data tracks. When track following on the in-phase dibits, the data heads will be on track center.

The cells on each servo track are organized into groups of 80, with each group corresponding to a physical data sector on the data surfaces. The first 16 cells of each sector contain a unique pattern of dibits which identify the beginning of a new sector (sector mark). The in-phase dibits are deleted from selected cells to create the zeros which allow the servo circuitry to decode this mark.

The sector mark pattern is also used to identify the index mark, a mark which occurs once on each

servo track and defines physical sector zero. The index mark is nothing more than one sector mark followed by another recorded in the middle of the sector. This is the only spot on the track where sector marks are separated by only 40 cells, rather than the usual 80.

The second, or "quad", dibit pair (A′/B′) is physically offset one-half track from the in-phase dibits. Thus, when track following on this pair, the data heads will be exactly one-half track from track center. The quad dibits are used when recording sampled servo on the data surfaces.

In addition to being used to record sampled servo code, the quad dibits are also used to generate the track crossing signal during seeks. By using quads, the final track crossing signal occurs when the heads are one-half track from the target, which allows the servo system to turn on the fine positioning loop in time to bring the heads on track.

The outer servo guard band is similar to the data area, but the quad dibits have been deleted from each cell. Only in-phase dibits (A/B) are recorded in this area. The first 8 cells of each sector in the outer guard band contains a unique pattern of dibits, known as the guard band mark. Selected dibits are deleted from each cell to identify the guard band mark. Because the absence of a single dibit within the cell represents a 0, each individual dibit is sensed to detect the guard band mark.

Like the data area, the inner guard band servo area contains four dibits in each cell. However, the inner guard band is distinct from the data area in that no sector marks are recorded at sector boundaries. Servoing is possible in either guard band area.

5-15. SAMPLED SERVO CODE. The sampled servo code is written at the factory with a sampled servo writer, using the dedicated servo code as a timing and physical reference. The servo writer uses the read/write heads in the drive to write and verify the servo code. The sampled servo code is written on all data tracks on all 7 (HP 7936) or 13 (HP 7937) data surfaces.

When writing the sampled servo code, the servo head is track following on the quad dibits; therefore the sampled servo code is physically offset 1/2 track from the center of the adjacent data track (see figure 5-13). When reading the sampled servo code, the data head is physically located midway between the two (odd and even) sampled servo code patterns. This allows the head to detect dibits from both patterns.

The complete window for the sampled servo code is defined by Gap (GAP-L,), which is generated by the servo controller. The first portion of the sampled servo field is occupied by two sets of coincident dibits. The first set of dibits functions as a qualifying pulse, ensuring that any power-on noise is not erroneously identified as a valid sync pulse. The second set of coincident dibits are the servo sync pulse. This pulse, when followed by the requisite number of zeros, synchronizes the sampled servo code to the dedicated servo.

The servo sync pulse is followed approximately 54 Write Clocks (WC) later by six alternating dibits (three odd, three even). It is from these six dibits that the sampled servo circuit determines how far the read/write head is offset from track center.

5-16. SERVO HEAD . The servo head is a Winchester technology head, similar to the data read/write heads. (These heads are described in detail in the read/write system functional description.) When the drive is manufactured, the servo head is used to write the dedicated servo code on the servo surface. Following completion, the servo head is used only to read this servo code.

5-17. SERVO READ PREAMPLIFIER/WRITE DRIVER IC. The servo read preamplifier/write driver IC is similar to the data read preamplifier/write driver ICs. (These ICs are described in detail in the read/write system functional description.) During manufacture of the drive, the write driver section of the IC is used when the dedicated servo information is written on the servo surface. Following completion of the drive, only the read preamplifier section of the IC is used.

5-18. DRIVE ID CIRCUIT. The drive identification (ID) circuit is permanently programmed during manufacture of the head-disc assembly to identify the HDA as having seven (7936) or 13

(7937) data surfaces. The output signals, labeled Drive ID bits (DID0, DID1), are connected via read/write PCA-A2 to the input of the servo controller in servo PCA-A1. See figure S1.

5-19. HEAD GAIN REFERENCE PROM AND DAC. Read-only memory (PROM) and digital-to-analog converter (DAC) ICs in the HDA supply a reference current to servo PCA-A2 that represents the gain characteristics of the read/write heads and servo head installed in the drive. The PROM is programmed with this data during manufacture and checkout of the drive. These gain characteristics are included in the determination of the AGC levels for the sampled and dedicated AGC amplifiers in read/write PCA-A2.

During operation of the drive, the read/write controller supplies read/write head address information to the PROM together with details of where the head is located on the disc. The head address information is supplied by signals Chip 0, 1 (CH0-H, CH1-H) from the head select encoder and Head Select 1, 2 (HD1S-H, HD2S-H) from the read/write controller. Head position information is provided by Write Current Select 1, 2 (WCS1, WSC2), also from the read/write controller. In addition, Buffered Start of Sector (BSOS-L) indicates when to look at the gain of the read/write heads (for sampled servo) or the servo head (for dedicated servo). A 6.25V reference to the DAC, labeled DAR, is supplied from servo PCA-A1.

The DAC converts the 8-bit output from the PROM into a head gain reference current for the selected head. The DAC output is labeled Servo Gain Reference (SGR).

Signal SGR is connected to the dedicated and sampled AGC circuits in servo PCA-A1 where it is converted to a reference voltage and integrated with outputs from the position demodulators to determine the AGC levels for the dedicated and sampled servo AGC amplifiers in read/write PCA-A2.

5-20. ACTUATOR. The read/write heads and servo head are mounted on a rotary arm supported by precision ball bearings. A bobbin-type voice coil, attached to the rotary arm, and mounted between two fixed permanent magnets, comprise a head positioning mechanism (actuator). The actuator provides the driving force needed to move the arm for positioning the heads over the discs. The magnetic field in the gap between the two magnets allows acceleration of the moving arm to be controlled by the current in the voice coil. Drive current for the voice coil is supplied by the servo power amplifier in servo PCA-A1. Crash stops are incorporated in the actuator to prevent damage to the heads in the event that the servo system loses control of the actuator.

When the drive is powered down, the rotary arm is driven to a nondata head landing zone at the inner diameter of the discs. A mechanical latch for the arm prevents damage to the heads during shipment of the drive by immobilizing them in the landing zone.

5-21. SPEED SENSOR. The speed sensor is a Hall-effect device mounted on the head-disc assembly near the spindle pulley. A magnet, embedded in the pulley, triggers the sensor once per revolution of the spindle. The sensor output, labeled Speed Sense (SPDSNS-L), is connected to the servo controller in PCA-A1. See figure SD. This output is used by the controller at power on to determine when the spindle is rotating fast enough to allow the actuator to move the heads away from the landing zone. This action occurs when the speed reaches approximately 3000 rpm.

5-22. READ/WRITE PCA-A2

The servo system components in read/write PCA-A2 include the dedicated servo AGC amplifier, sampled servo switch, and sampled servo AGC amplifier. See figure RW.

5-23. DEDICATED SERVO AGC AMPLIFIER. Differential Servo Data (SDX, SDY), from the servo read preamplifier/write driver IC in head-disc assembly A3, is buffered and gain controlled by the dedicated servo AGC amplifier. The input to the preamplifier section of the IC is the servo code read from the dedicated servo surface. The differential output from the AGC amplifier, labeled Dedicated Servo (DEDN, DEDP), is passed to the input of the dedicated servo filter in servo PCA-A1. Dedicated AGC (DAGC), developed by

the AGC integrator in the dedicated servo circuit, is fed back to the AGC amplifier to control its gain.

5-24. SAMPLED SERVO SWITCH. The sampled servo switch gates differential Read/Write Data (DX, DY), allowing only the sampled servo code prerecorded between data sectors to reach the input of the sampled servo AGC amplifier. The gating action of the circuit is controlled by differential Sampled Servo Enable (SSEN-H, SSEN-L), from the sampled servo timing circuit in servo PCA-A1. See figure S1.

5-25. SAMPLED SERVO AGC AMPLIFIER. The differential output from the sampled servo switch is buffered and gain controlled by the sampled servo AGC amplifier. The differential output from the amplifier, labeled Sampled Servo (SMPN, SMPP), is passed to the input of the sampled servo filter in servo PCA-A1. Sampled AGC (SAGC), developed by the AGC integrator in the sampled servo circuit, is fed back to the AGC amplifier to control its gain.

5-26. SERVO PCA-A1

The servo system components in servo PCA-A1 include the servo controller, AGC circuits, sampled servo circuit, dedicated servo circuit, servo power amplifier, and amplifier control and fault indication logic. See figures S1 and S2.

5-27. SERVO CONTROLLER. The servo controller consists of an 8-bit control-oriented microcomputer IC. Included on the single chip are an 8-bit central processing unit (CPU), 32 input/output (I/O) lines, internal memory of 8k by 8 ROM (program) and 128 by 8 RAM (data), two 16-bit timer/counters, and a full duplex serial port. The IC is clocked by an on-chip clock circuit and external crystal oscillator.

The servo controller receives commands from the microprocessor in controller PCA-A6, provides control for the drive servo system to complete these commands, and returns servo status information to the microprocessor. All communication with controller PCA-A6 is via the Servo Control Bus.

5-28. Controller Intercommunication. Either controller (the microprocessor in PCA-A6 or the servo controller) is capable of initiating communication to the other at any time. To arbitrate such an interface, a dual first-in-first-out (FIFO) register in PCA-A6 is used between the two controllers.

The FIFO contains two bytes for each controller and is clocked separately by each controller. When data is written to the FIFO, an interrupt line to the other controller is asserted. Servo Buffer Full (SBF-L) is used to determine if the controller has read the previous message from the FIFO, making the interface ready for another message from the servo controller.

A transaction in either direction is initiated by the transmitting controller writing two bytes to its write FIFO. (Dual FIFOs allow both controllers to write at the same time.) This write causes the interface interrupt of the receiving controller to be asserted. When the receiver reads both data bytes in its read FIFO, the interrupt is deasserted, and pointer of that FIFO is reset. This allows the transmitter to write again into this FIFO, when necessary.

Typically, controller PCA-A6 initiates transactions by sending the servo controller a 2-byte command, upper byte first. Controller PCA-A6 initiated request servo function commands include seek, recalibrate, and spin up. Request servo status commands initiated by controller PCA-A6 include report HDA type, report status, report seek time, and report present track. It is also possible for the servo controller to initiate a status message to controller PCA-A6. The servo controller always returns a 2-byte immediate status message in response to all servo function commands and a 2-byte detailed status message in response to a controller Report Status command.

5-29. Servo Control Bus. The signals which the servo controller exchanges with the microprocessor in controller PCA-A6 over the Servo Control Bus are detailed below:

SD0-SD7	Servo Data Bus
SBF-L	Servo Buffer Full
SDAV-L	Servo Data Available
SPR-L	Servo Processor Reset
SRD-L	Servo Read
SWR-L	Servo Write

Servo Data Bus (SD0-SD7) is an 8-bit bidirectional bus which interconnects the microprocessor in controller PCA-A6 with the servo controller.

Servo Buffer Full (SBF-L) indicates that the microprocessor in PCA-A6 cannot accept any more status bytes from the servo controller.

Servo Data Available (SDAV-L) indicates that the microprocessor has a command byte ready for the servo controller.

Servo Processor Reset (SPR-L) allows the microprocessor to reset the servo controller.

Servo Read (SRD-L) permits controller PCA-A6 to drive the bus with a byte of command information.

Servo Write (SWR-L) indicates that the servo controller is driving the bus with a byte of servo information.

5-30. Servo Controller Input and Output Signals. The servo controller exchanges the following signals with the drive electronics:

INPUTS

AGCF-L	AGC Fault
AMPFLT-L	Amplifier Fault
DID0, DID1	Drive ID
GBD-H	Guard Band Detect
OFTRK-H	Offtrack Latched
SPDSNS-L	Speed Sense
SRTF-H	Servo Timing Fault
SSGT-L	Sampled Servo Gate
TRKCR-H	Track Crossing

Signal SPDSNS-L is from the spindle drive system (see figure SD) and the remainder of the signals are from components of the servo system (see figures S1 and S2).

OUTPUTS

ACQUIRE-H	Acquire
AMPEN-H	Amplifier Enable
CLER-L	Clear Error
CLSER-L	Clear Servo Error
FSEN-L	Fine Servo Enable
GDBEN-H	Guard Band Enable
LCK-L	Lock
LSB-H	Least Significant Bit
NACC-L	Negative Acceleration
PACC-L	Positive Acceleration
QUAD-H	Quadrature
SCAP-L	Start Capacitor
SOSEN-H	Start of Sector Enable
SSSL-H	Sampled Servo Select

The majority of the outputs from the servo controller are connected to the dedicated servo circuit, sampled servo circuit, and servo power amplifier. Start Capacitor (SCAP-L) is output to the spindle drive system. See figure SD .

The functions of the servo controller input and output signals are described in table 5-1 and related circuit descriptions.

5-31. 2-BIT ADC. The servo controller monitors head shift (dedicated track/sampled track offset) and adjusts for it. The measurement of head shift is done while track following on the sampled servo, after a seek command has been received, but before the seek is begun by the servo controller. The 2-bit analog-to-digital converter (ADC) is continuously monitoring Dedicated Servo Position Error (DPOS) to a sign and a single bit of amplitude. From a DPOS/in-phase versus DPOS/quad dedicated servo code measurement, the servo controller can determine how much head shift the present data head has (relative to the servo head), and can adjust the subsequent seek accordingly.

5-32. DEDICATED SERVO AGC CIRCUIT. Included in this circuit are a dedicated AGC reference circuit and an AGC integrator. In operation, the AGC reference demod(ulator) switch connects Servo Gain Reference (SGR), a current representing the gain of the servo head, to the dedicated AGC reference circuit. The switch is controlled by Gap (GAP-L), which causes SGR to be applied to the dedicated AGC reference circuit during the period between embedded servo gaps on the data surface. In the AGC reference circuit, the current is converted to a reference voltage level. At the AGC integrator, the reference is integrated with Dedicated Level DLVL from the dedicated servo position demodulator and the resulting output from the integrator is Dedicated AGC (DAGC). This voltage is fed back to the dedicated servo AGC amplifier in read/write PCA-A2.

5-33. SAMPLED SERVO AGC CIRCUIT. The sampled servo AGC circuit is similar to the dedicated servo AGC circuit described above. In operation, the AGC reference demod(ulator) switch switches Servo Gain Reference (SGR), a current representing the gain of the selected read/write head to the sampled AGC reference circuit. In this case, GAP-L connects SGR to the sampled reference circuit for the duration of the sampled servo gap. The reference voltage is integrated in the sampled AGC integrator with Sampled Level (SLVL) from the sampled servo position demodulator and the resulting output is Sampled AGC (SAGC). This voltage is fed back to the sampled servo AGC amplifier in read/write PCA-A2.

5-34. SECTOR MARK DECODER. The sector mark decoder identifies two unique dibit patterns on the dedicated servo tracks. These two patterns, sector mark and guard band mark, are used to synchronize the timing functions of the drive to the dedicated servo surface.

The sector mark decoder monitors the Dedicated Servo signal (DSRVP) looking for missing dibits, or zeros. It is the absence of these dibits which identifies the sector and guard band marks. The actual decoding is performed by a zero detector and a 16-bit shift register. The basic timing for the servo mark decoder is generated by the dedicated servo timing circuit.

When the servo head is over the data area, the sector mark decoder is searching for a sector mark. The absence of both in-phase dibits within a cell defines a sector mark zero. The Dibit Gate (DBGT-H) signal gates the in-phase dibits into the zero detector. At the end of each cell, the output of the zero detector is clocked into the shift register by Zero Clock (ZCLK). If both in-phase dibits are missing, a zero is clocked into the register. When the unique 16-bit sequence of ones and zeros which define a sector mark is clocked into the shift register, the decoder generates Sector Mark Detect (SMDT-H), which is clocked out of the decoder by Sector Mark Clock (SMCLK).

When the servo head is over the guard band area, a change in the ZCLK frequency causes the decoder to search for the guard band mark. In the guard band, the absence of either in-phase dibit within a cell defines a zero. Therefore, ZCLK must sample the output of the zero detector twice during each cell. Once again, the output of the zero detector is clocked into the shift register by ZCLK. However, the decoder is now looking for a different 16-bit pattern of ones and zeros. When the guard band mark is detected, the decoder outputs Guard Band Detect (GBD-H) to the dedicated servo timing.

5-35. DEDICATED SERVO CIRCUIT. Components in the dedicated servo circuit include a filter, amplifier, position demodulator, and PLL and timing circuit. See figure 5-14 for circuit timing diagram.

5-36. Dedicated Servo Filter. The input to the dedicated servo low-pass filter is differential Dedicated Servo (DEDP, DEDN) from the dedicated servo AGC amplifier in read/write PCA-A2. The fundamental frequency of DEDP, DEDN is 288 kHz and the filter has a cut-off of 3.5 MHz. The filter is needed for noise suppression.

5-37. Dedicated Servo Amplifier. The dedicated servo amplifier is an integrated circuit operational amplifier connected to operate as a buffer amplifier with a gain of 20. The differential output of the amplifier is labeled Dedicated Servo (DSRVP, DSRVN). The DSRVN line is connected

to the dedicated servo position demodulator and the DSRVP line is coupled to the sector mark decoder and the dedicated servo timing and PLL circuitry.

5-38. Position demodulator. The dedicated servo position demodulator monitors the Dedicated Servo (DSRVN) signal and generates a Dedicated Position (DPOS) analog signal, which represents the current position of the servo head relative to the dedicated servo dibits. This signal is used to generate the track crossing signal during seeks, and also to control actuator positioning at the conclusion of a seek. DPOS is also used to control head positioning when servoing in the guard bands.

The DSRVN signal from the dedicated servo amplifier is input to a dibit peak detector, which creates a voltage proportional to the amplitude of the incoming dibits. The output of the peak detector is fed to a pair of sample-and-hold circuits, which capture the peak values for the appropriate dibit pair. The timing of the sample-and-hold circuits is controlled by two signals, A Sample (ASMPL) and B Sample (BSMPL), from the dedicated servo timing circuit. These signals ensure that the proper dibit pair (in-phase or quad) is sampled at the correct time. A third signal, Dump (DMP-H), discharges the peak detectors in preparation for the next sampling cycle.

The outputs of the two sample-and-hold circuits are input to a position discriminator, which subtracts the two signals. The resultant DPOS signal, which represents the position of the servo head relative to the dibits being sensed, is used by the 2-bit ADC and track crossing detector during seeks. DPOS also controls the position of the actuator at the conclusion of seeks and when servoing in the guard bands.

The sample-and-hold circuit outputs are also used as the input to a level discriminator circuit. This summing amplifier generates a Dedicated Level (DLVL) signal proportional to the sum of the two inputs. DLVL represents the level of the servo signal and is used by the dedicated servo AGC integrator to generate the proper AGC level.

5-39. Dedicated Servo Timing And PLL. This block generates the reference timing signals for servo and write operations.

The PLL circuit generates the 28.2 MHz Differential Write Clock (DWC-L, DWC-H) used when writing data on the disc. The PLL includes a VCO which, through the use of a phase detector, is synchronized to DSVRP. In addition, the PLL generates a Write Clock (WC-H) used by the sampled servo timing, and also provides the timing signals for remainder of the dedicated servo timing. The Lock (LCK-L) signal from the servo controller aids the VCO in locking to the incoming dibit stream by sweeping the output frequency of the VCO until lock is achieved.

The dedicated servo timing circuit controls the operation of the sector mark decoder and the position demodulator. The generation of dedicated servo timing is controlled by three signals from the servo controller: Guard Band Enable (GBDEN-H), Quadrature (QUAD-H), and Least Significant Bit (LSB).

The GBDEN-H signal is used to generate the proper timing signals to allow the sector mark decoder to search for sector marks (GBDEN-H inactive) or guard band marks (GBDEN-H active). The primary timing difference between the two search modes is that when looking for guard band marks the frequency of ZCLK is doubled. This allows the sector mark decoder to sample each servo cell twice when looking for missing guard band dibits; a necessity since each dibit within the guard band mark represents a discrete state. The two additional timing signals (DBGTH, SMCLK) used to control the operation of the sector mark decoder are unchanged by the state of GBDEN-H. When a guard band mark is detected, the Guard Band Detect (GBD) signal from the sector mark decoder is passed by the dedicated servo timing circuit to the servo controller.

The state of QUAD-H determines whether the dedicated servo position demodulator will be configured to process in-phase dibits (QUAD-H inactive) or quad dibits (QUAD-H active). In response to the state of QUAD-H, the dedicated servo timing circuit generates the proper timing signals for the position demodulator. These signals, ASMPL, BSMPL, DMP-H, control the internal sampling

periods of the demodulator, ensuring that the proper dibit pair is being processed.

The LSB signal is also used to control the sampling signals (ASMPL, BSMPL) to the position demodulator. Using LSB, the proper timing is maintained to ensure that the polarity of DPOS is constant, regardless of whether the drive is following an even or odd track.

5-40. SAMPLED SERVO CIRCUIT. The sampled servo circuit processes the sampled servo code embedded between data sectors to obtain position and amplitude information relative to the position of the read/write head with track center. Circuitry in the sampled servo circuit includes a filter, amplifier, timing and fault detection circuit, and a position demodulator. See figure 5-15 for circuit timing diagram.

5-41. Sampled Servo Filter. The input to the sampled servo band-pass filter is differential Sampled Servo (SMPN, SMPP) from the sampled servo AGC amplifier in read/write PCA-A2. The fundamental frequency of SMPN, SMPP is 446 kHz and the filter has a center frequency of 2.5 MHz. The filter is needed for noise suppression.

5-42. Sampled Servo Amplifier. The sampled servo amplifier is an integrated circuit operational amplifier connected to operate as a buffer amplifier with a gain of 20. The differential output is labeled Sampled Servo (SSRVN, SSRVP). The SSRVN line is connected to the sampled servo position demodulator and the SSRVP line is connected to the sampled servo timing and fault detection circuit.

5-43. Sampled Servo Timing and Fault Detection. This block of circuitry generates the timing signals that coordinate the operation of the sampled servo circuits. Timing faults in the sampled servo are also detected by this circuit.

The sampled servo timing circuit uses a group of Programmable Array Logic (PAL) circuits to control the generation of the timing signals. The outputs of the PALs control the operation of a sector counter. The counter outputs serve as address lines for the timing PROM, which generates the sampled servo timing signals.

The WC-H signal from the dedicated servo timing and SMDT-H from the sector mark decoder serve as timing reference inputs to the PALs, synchronizing the sampled servo timing with the dedicated servo. The SSRVN signal from the sampled servo amplifier is input to a comparator which detects the sampled servo sync pulse. The sync pulse indicates the beginning of the sampled servo code.

Inputs from the servo controller are also used to maintain proper sampled servo timing. The Acquire (ACQUIRE-H) signal facilitates synchronization of the sampled servo when switching data heads. Start Of Sector Enable (SOSEN-H) is gated with GAP-L to produce the Differential Start Of Sector signals (DSOS-H, DSOS-L). GAP-L also controls the operation of the AGC reference demod switch. Sampled Servo Select (SSSL-H) is used to generate Read AGC Gate (RAGC-H, RAGC-L) at the proper time.

The sampled servo timing controls the operation of the sampled servo position demodulator through the use of three timing signals: Sampled Servo Demodulation (SSDEMOD-H), Sampled Dump (SDMP-H), and Sampled Servo Gate (SSGT-L). SSGT-L is also output to the servo controller.

The Sampled Servo Enable (SSEN-H, SSEN-L) signals are used by the sampled servo switch on read/write PCA-A2. Good Clock (GDCLK) serves as a timing reference for the Missing Pulse Width Modulation (PWM) clock detector.

The sampled servo timing circuit detects the index mark on the dedicated servo surface. The index mark occurs once every revolution and identifies physical sector zero. The index mark is encoded as an additional sector mark which occurs in the middle of a sector. Midway through each sector, a signal from the timing circuit is gated with SMDT-H from the sector mark decoder. If SMDT-H goes active, the index mark has occurred and controller PCA-A6 is alerted via the INDEX-H signal.

The second function of this block of circuitry is to detect errors in the servo timing. Two timing error signals are output to the fault latches: Timing

Error 1 (TERR1-L) and Timing Error 2 (TERR2-L). The fault detection circuit monitors SMDT-H and GAP-L to ensure that the sampled servo timing is correct relative to the dedicated servo timing. If either signal does not occur at the proper time, TERR1-L is asserted. If three consecutive servo sync pulse are missing, or do not occur within a predefined window, TERR2-L is asserted.

5-44. Position Demodulator. The sampled servo position demodulator monitors the Sampled Servo (SSRVN) signal and generates a Sampled Position (SPOS) analog signal which represents the position of the currently selected data head relative to the sampled servo code. This signal is used to control actuator positioning when track following on a data track.

The SSRVN signal from the sampled servo amplifier is input to a dibit integrator, which is enabled at the proper time by SSGT-L. The integrator processes the sampled servo code by measuring the energy contained in the first half of each dibit, holding it for sampling, then discharging it to a constant value before processing the next dibit.

The output of the dibit integrator is fed to a pair of sample-and-hold circuits, which demultiplex the odd and even dibits into separate channels. The timing of the sample-and-hold circuits is controlled by the SSDEMOD-H signal from the sampled servo timing circuit. A second signal, Sampled Dump (SDMP-H), discharges the sample-and-hold circuits in preparation for the next sampling cycle.

The outputs of the two sample-and-hold circuits are input to a position discriminator, which subtracts the two signals. The resultant SPOS signal represents the position of the data head relative to the sampled servo code. SPOS is used to position the actuator when reading and writing data.

The sample-and-hold circuit outputs are also used as the input to a level discriminator circuit. This summing amplifier generates a Sampled Level (SLVL) signal proportional to the sum of the two inputs. SLVL represents the level of the sampled servo signal and is used by the sampled servo AGC integrator to generate the proper AGC level.

5-45. SAMPLED/DEDICATED SELECT SWITCH. The sampled/dedicated select switch selects either Sampled Servo Position Error signal (SPOS) or Dedicated Servo Position Error signal (DPOS) for connection to the input of the servo power amplifier via the slew rate limit switch. The selection of the desired input signal is controlled by Sampled Servo Select (SSSL-H) from the servo controller. The switch output is labeled Position Error (PES).

5-46. SLEW RATE LIMITER. The function of the slew rate limiter is to prevent single sector dropouts of the sampled servo from disturbing the operation of the sampled servo loop. When a large step in SPOS occurs, caused possibly by a bad sector, the slew rate limiter limits the rate at which SPOS can change, reducing the possibility of the head being driven off track. The limiter output is labeled Slew Position Error (SLPES).

5-47. SLEW RATE LIMIT SWITCH. The purpose of the slew rate limit switch is to disconnect the slew rate limiter from the sampled servo loop when the servo system is in a settling (off-track) mode. The switch is operated by Offtrack Unlatched (OFTU-L) from the off-track detector.

5-48. OFF-TRACK DETECTOR. The function of the off-track detector is to process Position Error (PES) into a digital indication of whether the heads are off track or on track. The output of the detector, labeled Offtrack Unlatched (OFTU-L), is used by the servo controller, together with a track verify, to report to controller PCA-A6 that a head settle on track has occurred.

5-49. TRACK CROSSING DETECTOR. The track crossing detector is a voltage comparator that detects when Dedicated Servo Position Error signal (DPOS) falls below a certain level. At this time, the detector output Track Crossing (TRKCR-H) is enabled to indicate that a dedicated servo track has been crossed.

Also included in the track crossing detector circuitry is a divide-by-five circuit that the servo controller activates at certain times to divide the track crossings by five. This is necessary when the

activator is moving at high speed and the time interval between track crossings is to short for the servo controller to process. For this reason, track crossings are divided by five when the heads are more than 20 tracks from the addressed track.

5-50. FAULT LATCHES. The fault latches retain servo errors detected by the servo system fault detection circuitry for action by the servo controller and read/write controller. Inputs to the latches are Timing Error 1 (TERR1-L) and Timing Error 2 (TERR1-L), from the sampled servo timing block; and Offtrack Unlatched (OFTU-L), from the off-track detector. Latch outputs are Servo Timing Fault (SRTF-L) and Offtrack Latched (OFTRK-H) to the servo controller, and Servo Error (SRVER-L) to the read/write controller. The latches are reset by Clear (CLER-L) and Clear Servo Error (CLSER-L) from the servo controller. Servo system error detection and reporting are discussed in later paragraphs of this chapter.

5-51. SERVO POWER AMPLIFIER. The servo power amplifier and associated circuitry provides the power to move the actuator. See figure S2 . The input to the power amplifier portion of the circuit comes from the output of the low-pass filter and notch filters block. When the actuator is doing a track to track seek, input to this block is from the seek current command generator and when the actuator is track following, the input is derived from Position Error signal (PES). The, selection of the input is performed by the position loop signal switch, which is controlled by Fine Servo Enable (FSEN-L).

The servo power amplifier converts the voltage from the output of the low-pass filter and notch filters block into a current through the actuator. The amplifier generates 1 ampere DC through the actuator for every 2 volt DC input.

The input signal to the amplifier is compared with sensed Actuator Current (ACUR) at the power amplifier compensation and DC offset compensator stage. The sensed current signal comes from the current-sense amplifier block. The resulting error signal from the amplifier compensation circuit is proportional to the difference between the input signal and the sensed current, with the frequency effects from the compensator.

The error signal from the amplifier compensation circuit is input to the pulse-width modulator (PWM) block. Here the error signal is converted into a 100-kHz pulse-width-modulated TTL square wave, labeled Pulse Width Modulation (PWM-L). The square wave is routed through gate logic in the amplifier control and fault indication block. The output from the gating logic goes to the transistor driver stages.

The transistor drivers shift the level of the gated signal to the level required to drive the output transistors and also provide the gate drive voltage needed to switch the output transistors on and off.

The output devices are power field effect transistors (FETs). One FET is connected to the positive power supply and the other is connected the the negative power supply.

The voltage seen at the common connection of the FET (drain) is the same waveform generated at the PWM block, except that the voltage level is shifted from +32/+37V to -32/+37V.

The signal at the common FET connection is filtered by the output filter. This filter removes the high frequency components of the square wave and changes the pulse-width-modulated square wave into a signal resembling a 100-kHz sine wave with a lower frequency component that is proportional to the original error signal from the power amplifier compensation circuit. The filtered voltage is applied to the actuator and the resulting current is sensed through the current-sense resistor using the current sense amplifier.

The combined action of the pulse-width modulator, transistor drivers, output transistors, and output filter is to power amplify the error signal from the power amplifier compensation block. Using pulse-width modulation gives the amplifier a relatively high efficiency of over 80 percent during the high current portion of a track to track seek.

The servo power amplifier is enabled/disabled through the amplifier control and fault indication block. If there are no detector faults, the amplifier is enabled when Amplifier Enable (AMPEN-H) from the servo controller goes high, and is disabled when AMPEN-H goes low. However, if any one of

a number of amplifier faults is detected, the amplifier is disabled and the amplifier crowbar circuit is activated.

Possible amplifier faults are Power On Reset from the power supply, Servo Processor Reset from the controller, Under Voltage from the under voltage detector, Overvelocity fault from the overvelocity detector, or Missing 100-kHz PWM Clock from the missing PWM clock detector. These faults are discussed in more detail in later paragraphs.

The following paragraphs provide a more detailed description of the circuit blocks in the servo power amplifier and associated circuitry.

5-52. Position Loop Compensation. The position loop compensation circuit provides the frequency compensation necessary to achieve the desired phase and gain margins for the position servo loop. The input to the circuit is Slew Position Error (SLPES). The compensator has two zeros at 372 Hz and two poles at 1590 Hz. This, along with the low-pass filter and notch filters stage, gives a phase margin of about 30 degrees for the sampled servo system and 40 degrees for the dedicated servo system.

The output from the position loop compensation block is connected into the circuit via the position loop signal switch when Fine Servo Enable (FSEN-L) is low.

5-53. Low Pass Filter and Notch Filters. Since the sampled servo signal has frequency components that are mirrored about the sampling frequency, a low-pass filter is required in order to remove high frequency components from the signal.

The low-pass filter is also used to control the output signal from the seek current command generator. The servo power amplifier has a limited current slew rate, since it is driving an inductive load. In order to ensure that the amplifier output does not saturate, the rate of change of the input signal must be within the limits that the amplifier can follow. The low-pass filter, in addition to a filter within the seek current command generator, limits the rate of change of the signal input to the amplifier.

Three notch filters in the circuit compensate for mechanical resonances in the drive. Since these resonances can be excited by either the signal derived from Slew Position Error (SLPES) or the seek command current generator output, both signals are routed through the notch filters. The notches are set at frequencies of 1336 Hz, 2200 Hz, and 6596 Hz.

The output of the low-pass filter and notch filters block is connected to the input of the servo power amplifier.

5-54. Seek Current Command Generator. This circuit provides the input signal for the servo power amplifier when the actuator seeks between cylinders. There are three digital inputs to the circuit. When Positive Acceleration (PACC-L) is low, the output from the seek current command generator goes to +6V, which is equivalent to a steady state current of +3 amperes through the actuator. When Negative Acceleration (NACC-L) is low, the output from the seek current command generator goes to -6V, equivalent to -3 amperes through the actuator. Both PACC-L and NACC-L are gated by Fine Servo Enable (FSEN-L), with the result that the output from the generator is at zero volts unless FSEN-L is high. The seek current command generator has a low-pass filter in its output stage. This is part of the filtering which limits the rate of change of the input signal to the servo power amplifier. Refer to the low-pass filter and notch filters circuit description for additional details.

5-55. Position Loop Signal Switch. This analog switch connects either the output of the position loop compensator or the seek current command generator into the input of the low-pass filter and notch filters block (servo power amplifier input.) When Fine Servo Enable (FSEN-L) is low, the position loop compensator output is selected. This occurs when the servo system is following either the dedicated or sampled servo code. When FSEN-L is high, the output from the seek current command generator is used. This occurs when the servo system is in the seek mode.

5-56. Summing Junction No. 1. Here the outputs from the position loop compensation and the seek current command generator stages are summed together. The resulting signal forms the input to the low-pass filter and notch filters stage.

5-57. Summing Junction No. 2. This summing junction sums the sensed actuator current from the current-sense amplifier block and the output from the low-pass filter and notch filters circuit. The result forms the input to the servo power amplifier compensation and DC offset compensation stage.

5-58. Power Amplifier Compensation and DC Offset. This circuit provides the ac compensation necessary to stabilize the servo power amplifier. It also contains a resistor divider network which is used to compensate for DC offset currents in the servo PCA. During factory testing of the servo PCA, the DC offset current is measured and the network adjusted to reduce the actuator offset current to less than ±1 milliampere.

5-59. Pulse Width Modulator. The pulse-width modulator (PWM) section consists of a triangle-wave generator and a comparator. The frequency of the triangle-wave generator is 100 kHz, and the output is coupled to the negative input of the comparator. The positive input of the comparator is connected to the output from the power amplifier compensation and DC offset compensation circuit.

The output from the comparator is a pulse-width-modulated square wave. The duty cycle of the square wave is 50 percent when the error signal input is at 5.18V. This is equivalent to no movement required from the actuator. As the error signal voltage increases, the duty cycle increases (stays high for a longer period), and vice versa. The output from the comparator, labeled Pulse Width Modulation (PWM-L), is gated with a signal from the amplifier control and fault indication section. The gating is required to turn off both output transistors when the servo power amplifier is shut off.

5-60. Transistor Drivers. The transistor driver stages change the PWM-L output from the pulse-width modulator into signals which drive the gates of the output transistors. The drivers have an optical isolator at their inputs, which translates the TTL input signal into a signal which switches relative to the ±45V supply.

Slow turn-on and fast turn-off circuitry incorporated in each driver prevents the two output transistors from being turned on at the same time.

5-61. Output Transistors. The output transistors are power field-effect transistors (FETs) An IRF9530 is used for the P-channel device and an IRF520 for the N-channel device. Power FETs are used because of their fast switching speed, and the relatively low power needed to drive the gate terminal.

5-62. Output Filter. The output filter is basically a 2-pole low-pass filter. The filter has a series inductor, followed by capacitors connected to ground. The resulting voltage seen at the actuator consists mainly of a 100-kHz sine wave, with a lower frequency component which is generated by the signal from the power amplifier compensation circuit. The natural frequency of the output filter is approximately 15 kHz.

5-63. Current-Sense Resistor. This is a 0.1-ohm precision resistor in series with the actuator. All current that flows through the actuator also passes through this resistor. In addition, the current that is shunted around the gate of the bidirectional triode thyristor in the actuator crowbar circuit also flows through this resistor. This offset current is compensated for during factory testing of the servo PCA. Refer to the paragraphs describing the actuator crowbar and power amplifier compensation circuits for additional details.

5-64. Current-Sense Amplifier. The current-sense amplifier senses the voltage drop across the current-sense resistor. The amplifier has a gain of 20, so that the equivalent voltage at the output of the amplifier is 2 volts for every 1 ampere of current in the actuator. The output signal from the amplifier is labeled Actuator Current (ACUR).

5-65. Amplifier Control and Fault Indication. This circuit monitors certain functions of servo power amplifier operation and shuts off the amplifier if a fault condition is detected.

Inputs to the circuit are Power On Reset (POR-L), Servo Processor Reset (SPOR-L), Under Voltage (UNDER VLT-L), Over Velocity (OVER VEL-L), Missing 100-kHz Clock (NO CLK-H), and Amplifier Enable (AMPEN-H).

There are three output signals from the circuit. Two of these signals are digital signals. One digital signal, Amplifier Fault (AMPFLT-L), is latched low if any fault condition occurs (any input active except AMPEN-H). The fault latch is cleared on the rising edge of AMPEN-H, as long as there is not an existing fault.

The other digital signal is the NAND combination of AMPEN-L and AMPFLT-L, and is called Switch On (SWON-L). Signal SWON-L is gated with Pulse Width Modulation (PWM-L), and controls the input signals to the two transistor driver stages. When this signal is low, both FET driver circuits are commanded to turn off their respective output transistor.

Since the SWON-L signal operates from +5V, it can only turn off the FETs as long as the +5V supply is functioning. Because of this, an analog signal is also used to turn the power FETs off. This signal is called Transistor Enable (QEN-H). If there are no fault conditions, QEN-H is connected to +5V through a transistor. Signal QEN-H is connected to the optical isolator of the N-channel transistor driver, the actuator crowbar circuit, and to some circuitry connected to the P-channel transistor driver. When QEN-H is equal to +5V, the optical isolator for the N-channel is operational, the actuator crowbar is disabled, and the P-channel driver operates normally.

When a fault condition exists, QEN-H does not source any current. This causes the N-channel transistor driver to turn off the N-channel FET, the actuator crowbar circuit is activated, and the P-channel circuit is forced to turn off the P-channel FET. All of these functions operate even when any of the +5V, -5.2V, +12V, or -12V supplies are at zero volts. The actuator crowbar circuit requires that the +45V supply to be about 10V in order to operate, and the output FETs will remain turned off for any value of either the +45V or -45V supplies.

5-66. Actuator Crowbar. The actuator crowbar circuit is activated if a fault is detected in the servo power amplifier. The purpose of the circuit is to prevent the actuator from hitting the crash stops at a high speed. The circuit employs a triac which is activated when a fault is detected in the servo power amplifier. When the triac gate control circuit is triggered by Transistor Enable (QEN-H) from the amplifier control and fault indication circuit, the actuator is effectively "shorted" and the output from the servo power amplifier is also shorted. This prevents the amplifier from putting high current into the actuator, in the event that an output transistor shorts to the power supply.

The triac also provided some braking action to the actuator, since the triac looks like a low impedance load, with the actuator acting like a generator. This reduces the velocity of the actuator during a fault condition.

The triac is triggered by its gate control circuit as long as the fault condition continues to exist. Once the fault condition stops, the gate drive to the triac is removed. However, the triac will continue to conduct as long as there is current flowing through it. Once the current flow through the triac ceases, it will turn off.

5-67. AMPLIFIER ERROR DETECTION. There are three error detection circuits in the servo power amplifier. These circuits are required in order to prevent a failure in the electronics from causing damage to the head-disc assembly or causing a safety hazard. The three errors that are detected are: failure of the 100 kHz triangle waveform wave generator (NO CLK-H), either the +45V or -45V supply is too low (UNDER VLT-L), or the actuator velocity is too high (OVER VEL-H).

The errors are reported to the amplifier control and fault indication circuit previously discussed.

5-68. Missing PWM Clock Detector. The two inputs to this circuit are a square wave from the 100-kHz generator in the pulse-width modulator (PWM-L) and a clock from the position detector circuit (GDCLK-H). If the 100 kHz signal quits, the detector output will go high after a maximum of one sector (approximately 125 microseconds). The detector output is labeled No 100 KHz Clock (NO CLK-H).

Failure of the 100-kHz oscillator will cause the servo power amplifier to self-oscillate at about 15 kHz. This causes a high power dissipation in the output filter. As an added precaution, there is a fuse in the output filter.

5-69. Undervoltage Detector. The circuit monitors the +45V and -45V supplies. If either supply should fail, (possibly because of a fuse opening), then the servo power amplifier will be turned off. Trip points for the circuit to indicate a failure are approximately +24V for the +45V supply, and -24V for the -45V supply. The detector output is labeled Undervoltage (UNDER VLT-L).

5-70. Overvelocity Detector. The circuit monitors Actuator Current (ACUR) and is used to indicate if the actuator is moving too fast. The circuit contains a low-pass filter which basically integrates ACUR. The output of the filter gives a relative indication of the velocity of the actuator. The filter output goes to a window comparator which trips if the voltage gets above +9.2V or -9.2V. The output from the comparator section is called Overvelocity (OVER VEL-H). The filter is reset if Fine Servo Enable (FSEN-L) stays low for over 1.5 milliseconds. It is necessary to reset the filter after every seek since the low-pass filter must start at zero volts in order to properly indicate an overvelocity condition.

5-71. SERVO SYSTEM ERRORS

Servo system errors can be divided into three categories: track follower-PLL errors, seek errors, and power amplifier errors. Some of the errors are hard-wire errors, that is, they immediately shut down a data write, whereas others are detected in the servo controller and are communicated only to controller PCA-A6.

The occurrence of most of the errors will cause the servo controller to jump to an abort routine. In this routine, various servo protect routines will be taken, depending on the severity of the error. The severity of the error is indicated by the immediate status message reported to the controller. An immediate status of 0 indicates no error. An immediate status of 1 indicates a soft error for which the servo controller commands a coast with the position loop open (no current to the actuator) and reports the immediate status to the controller. An immediate status of 02H indicates a hard error for which the servo controller does all of the above plus turn off the servo amplifier.

Details of the errors in each category are provided in the following paragraphs. Refer to the flowcharts in figures 5-6 through 5-11 for the control paths taken to derive the errors. The errors appear as "status = xx" blocks in the flowcharts. Drive errors (DERRORs) and test errors (TERRORs) are discussed in detail in chapter 8.

5-72. TRACK FOLLOWER - PLL ERRORS. The errors in this category are: servo timing, AGC error (sampled), off track (OFFTRK), and spindle speed error.

5-73. Servo Timing. There are servo timing errors (STEs) and servo timing faults. Servo timing error is asserted when the fixed amplitude pulse of the sampled servo field on a data surface does not occur within the proper time windows inside the sampled servo gate (generated from the dedicated servo surface). Servo timing error is expected to be true any time the drive is off track.

Either Timing Error 1 (TERR1-L) or Timing Error 2 (TERR2-L) will trigger Servo Timing Fault (SRTF-H), which in turn will cause the servo controller to abort any write operation.

In the sampled servo timing circuit, TERR1-L is asserted when GAP-L and SMDT-H do not occur at the proper time, relative to one another. TERR2-L is asserted when three consecutive sampled servo sync pulses are missing, or do not occur at the proper time.

5-74. AGC Error. AGC error is used to flag a lack of sampled servo dibit amplitude at the sampled servo amplifier in read/write PCA-A2. AGC error is asserted when the gain of this amplifier is at maximum and the AGC loop is no longer functioning. When track following, this error causes an immediate status to be sent to controller PCA-A6 with a request status returning a "sampled servo error" message.

5-75. Off Track. Off-track error is asserted when the low-pass filtered PES signal exceeds the limits of a voltage window detector. The limits on this window are equivalent to a head offset of ±90 microinches from track center. This error generates an immediate status message to the controller PCA-A6 and a request status will return a "off track while track following" or "too many off tracks in settle" message. The off track error is hardwired to the read/write system to disable a data write from taking place.

5-76. Spindle Speed Error. Spindle speed error is reported to controller PCA-A6 only when track following. It is an indication that the time interval between successive sampled servo gates has moved out of the 136 microsecond, ±7.5 percent tolerance. As such, this indicates that either the spindle speed is out of tolerance or the servo PLL is not locked (the former causing the latter). An immediate status is sent to controller PCA-A6, with a request status message returning a "servo timing error" message.

5-77. SEEK ERRORS. All seek errors are detected by the servo controller and are reported to controller PCA-A6. Errors in the seek category are: Too many off tracks in settle, seek timed out, too fast at fine servo closure, attempt to seek off the disc, and recalibrate failure. The figure and status number following each error title indicates the flowchart where the error can be found.

5-78. Too Many Off Tracks In Settle. (Figure 5-9, Status = 6) When the heads are one-half track away from target, a final deceleration current pulse is sent to the actuator and the sampled servo circuit is enabled. When the PES signal passes through track center for the first time, a "seek near complete" is sent to the controller. At the same time, a counter in the servo controller begins to count the number of times OFTRK indicates that the heads have moved from being on-track to off-track. If this count exceeds four, this error is reported to the controller. If the settle is successful, a "seek complete" message is sent to the controller.

5-79. Seek Timed Out. (Figure 5-8, Status = 10) At the initiation of a seek, a timer is loaded with an appropriate timeout for that length of seek. If the timer counts through this timeout, the seek aborts and the error is reported.

5-80. Too Fast At Fine Servo Closure. (Figure 5-8, Status = 11) The time between successive track crossings is a measure of the velocity at which the heads are moving. If the time is greater than 330 microseconds (4000 tracks/second) at the last track, the seek is aborted (it would not settle) and a bad immediate status is reported. A status request would then return a "fast last track" message.

5-81. Attempt to Seek Off the Disc. (Figure 5-8, Status = 12) This error is reported if the servo controller receives a seek command which will cause it to attempt to seek beyond the physical limits of the actuator crash stops. The seek is aborted and the error reported.

5-82. Recalibrate Failure. (Figures 5-7, 5-8, 5-9, Status = 2) During a recalibrate operation, the servo controller tests the spindle speed to determine if the servo PLL has locked up over the guard band servo code. (This is the only place where the PLL can lock up.) If lockup, or the proper spindle speed does not occur within 1.8 seconds during a recalibrate, this error is reported. This error is also reported if the dedicated AGC error occurs before moving on track.

5-83. POWER AMPLIFIER ERROR. Status = 2, Recalibrate, Seek, sheets 1 and 2) A power amplifier error is generated when a current has been flowing into the actuator for more that an allowable time, there is no 100-kHz clock, the +45V or -45V supply is too low, or Servo Processor Reset

(SPR-L) is low. These errors are detected by the servo controller when detailed status is requested.

5-84. ERROR REPORTING. Servo system error reporting is performed by 2-byte immediate status and 2-byte detailed status information exchanged across the Servo Control Bus.

Immediate status is returned by the servo controller in response to all request servo function commands issued by controller PCA-A6. Immediate status reported can be: no error (normal response), soft error, hard error, or interface error. Also reported is the servo function command for which the status is being returned, and a detailed description of the bad status associated with the identified command.

Detailed status is returned by the servo controller in response to a report status command from controller PCA-A6. The 2-byte detailed status contains a bit array in which one of the elements represents the current servo system fault. The fault is not related to any servo command. Detailed status also contains a description of the bad immediate status associated with the function command indicated by immediate status.

5-85. FLOWCHARTS

A number of flowcharts are provided which chart the various operations of the servo system. Figures 5-6 through 5-11 describe servo controller power-on, recalibrate, seek, servo commands, and controller power-on, respectively. These flowcharts also show the activity which the drive goes through to generate certain errors. The status numbers shown in the flowcharts are error codes generated by the servo controller. These codes are sent to controller PCA-A6 where they are converted to a different error code. Refer to chapter 8 for additional details.

5-86. READ/WRITE SYSTEM

The principal component in the read/write system is a custom-designed read/write controller integrated circuit with associated read chain, write chain, and head select encoder electronics. See figure 5-16.

To perform the task of writing or recovering data from the disc media, the read/write controller receives commands from the microprocessor in controller PCA-A6 (passed over the Data Path Control bus), transforms byte-parallel data to or from the DMA/ECC electronics in PCA-A6 (passed over the Disc Data Bus), and obtains timing information from the servo system. Read and write operations are commanded on a sector by sector basis and the operation for every sector is completely independent. When not reading a sector or writing a sector, the read/write system is in an idle state.

When the microprocessor in PCA-A6 sends a write command to the read/write controller, the servo system identifies the start of sector and a driver in the write chain will be enabled and a constant frequency sync field will override any previous pattern on the disc. Following the sync field, a framing word will be written, and then the data to be written will start being clocked from the DMA/ECC in PCA-A6 into the encoder portion of the read/write controller. The encoder takes the byte-parallel data and maps it to serial VLFM code. This code drives the write drivers in the read preamplifier/write driver ICs in head-disc assembly A3. After the second CRC byte is clocked into the encoder, two bytes are clocked in as dummies, allowing the ECC to switch paths and become operable before supplying the ECC bytes. A counter within the encoder will stop clocking the data at the end of the ECC field. Write current will be turned off at the end of the sector. All timing in the read/write system during a write is based on a write clock from the servo system.

When PCA-A6 sends a read sector command to the read/write controller, the controller waits for the start of sector, as defined by the servo system. After a fixed delay following start of sector, a PLL and data separator in the read chain is enabled to lock to the sync field. (The time delay is to allow for start up delays when the sector was written, propagation time through the read circuitry, and time error between the servo head and the data head.) After a time interval adequate for the PLL to obtain lock, the read/write controller switches the PLL from a locking mode to a tracking mode. Timing up to this point is based on the write clock from the servo system. Now, the PLL becomes the timing reference for the read

operation, and the decoder is enabled to look for the framing word in the bit stream. The framing word is a 1000101001 bit sequence, decoded such that no single bit error will impact the proper framing of the following data string. When framing occurs, the bit-serial VLFM data going into the decoder will be mapped to byte-parallel data. A clock generated in the decoder will transfer this to the DMA/ECC electronics in PCA-A6.

Portions of the read/write system circuitry are located in head-disc assembly A3, read/write PCA-A2, servo PCA-A1, and controller PCA-A6. See figure RW . Details of these circuits, with the exception of those in PCA-A6, are provided in the following paragraphs. Refer to Appendix A at the rear of the manual for a description of the PCA-A6 circuitry.

5-87. HEAD-DISC ASSEMBLY A3

The parts of the read/write system in head-disc assembly A3 include the recording medium, read/write heads, and read preamplifier/write driver ICs.

5-88. RECORDING MEDIUM. The recording medium in the drive is a sputtered thin-film metal magnetic coating on either side of a circular 210-millimeter (8.3-inch) diameter aluminum substrate. In the HP 7936, there are seven of these surfaces for data and one surface for dedicated servo code. The dedicated servo code is recorded on the lower surface of the bottom disc in the stack. In the HP 7937, there are 13 surfaces for data and one surface for dedicated servo code. Again, the dedicated servo code is recorded on the lower surface of the bottom disc in the stack.

5-89. READ/WRITE HEADS. The drive employs Winchester technology read/write heads, one for each data surface. When the disc is powered down, the actuator moves the heads to a "landing zone" at the inner diameter of the discs where the heads come to rest on the disc surfaces.

Each head consists of a gapped ferrite core mounted in a ceramic shoe. There are two windings wound around the ferrite core and the windings are connected at a common point and phased in such a way that the common point acts as a center tap. These windings are used for both reading and writing by detecting or producing a magnetic field at the gap in the ferrite core.

In a write operation, data is written by passing a current through the windings of the selected head. The current generates a flux field across the gap and aligns the magnetic particles contained in the surface of the disc. The writing process orients the poles of each magnetized particle to permanently store the direction of the field as the particles pass beneath the head. The direction of the flux field is a function of the write current direction. Erasing is accomplished by writing over data which may have been previously recorded on the disc.

In the read operation, as the data surface passes beneath a head, the magnetically stored flux fields intersect the gap in the ferrite core. Gap motion through the flux field causes a voltage to be induced into the windings wound around the core. This induced voltage is analyzed by the read chain to define the data recorded on the surface of the disc. Each flux reversal, caused by a write current polarity change, generates a readback voltage pulse.

5-90. READ PREAMPLIFIER/WRITE DRIVER ICS. The read preamplifier/write driver ICs are off-the-shelf units designed for disc drive head control. Each IC can select 1 of 4 heads, read from or write to the selected head, and supply a read/write fault signal.

Since the drive has a total of seven (HP 7936) or 13 (HP 7937) read/write heads, four of the ICs are used for head control. The ICs are multiplexed with Chip Enable (CE0-L through CE3-L) from the head select encoder in read/write PCA-A2. Binary Head Select (HS1-H, HS2-H), also from the head select encoder, are decoded by the chosen IC to select the desired head.

Read and write select is controlled by Write Select A (WSA) and Write Select B (WSB) from the write chain in read/write PCA-A2. (Both signals originate at a common point within the write chain.) When WSA and WSB are low, read is selected; and when WSA and WSB are above 3.5V, write is selected.

When the IC is in the write mode, differential

current from input switches in the write chain, applied across differential Read/Write Data lines (DX, DY) switch the current from a current source in the write chain to the selected head. The write current line is labeled Write Current (WC). Head voltage swings, generated by the switching of the write current through the inductive head are monitored by a head transition detect circuit in the IC. Absence of proper voltage swings, caused by an open or short in either half of a head winding or the absence of write current, will cause a current to flow into the Unsafe output line (US). This line is connected to the unsafe detector in read/write PCA-A2, which in turn reports the fact to the read/write controller via Current Unsafe (CURUS-H).

When the IC is in the read mode, data is read from the selected head, amplified, and output on the differential DX, DY lines to a filter and amplifier stage at the input of the read chain in read/write PCA-A2. The same signal is also input to the sampled servo switch in PCA-A2. If a fault condition exists such that write current is applied to the IC when it is in the read mode, the write current will be drawn from the Unsafe line and the fault will be detected by the unsafe detector in read/write PCA-A2 and reported to the read/write controller.

5-91. READ/WRITE PCA-A2

The read/write system circuits contained in PCA-A2 include a custom-designed read/write controller IC, a head select encoder, a write chain, a read chain, and amplifiers for the sampled and dedicated servo code. Details of these circuits are provided in the following paragraphs.

5-92. READ/WRITE CONTROLLER IC. The read/write controller IC is a custom-designed gate array IC which operates with associated read chain and write chain electronics to control the task of reading from or writing to the data surfaces.

The controller consists of two independent sections - a control section and an encoder/decoder section. The control section receives commands and exchanges status information with the microprocessor in controller PCA-A6 over the Data Path Control Bus. The encoder/decoder section exchanges disc data with the DMA/ECC electronics in PCA-A6 via the Disc Data Bus, receives timing information from the servo system, and interfaces with the read chain and write chain circuitry external to the IC.

5-93. Interface Signals. The signals which the read/write controller exchanges with the microprocessor in controller PCA-A6 are detailed below.

DATA PATH CONTROL BUS

DPC0-DPC7	Data Path Control Bus
DPRHW-L	Data Path Read High, Write Low
DPA0-H	Data Path Address Zero
DPCS-L	Data Path Control Select
DPIRQ-L	Data Path Interrupt Request

Commands and status information exchanged between the microprocessor in PCA-A6 and the read/write controller via the Data Path Control Bus are stored in three registers in the control section: an address register (read/write only), a command register (write only), and a status register (read only). The bus signals operate as follows:

Data Path Control Bus (DPC0-DPC7) is an 8-bit bidirectional bus interconnecting the read/write controller and the microprocessor in controller PCA-A6. Transactions can take place at any time provided that the setup and hold times around Start of Sector (SOS-L) are not violated.

Data Path Read High/Write Low (DPRHW-L) when high enables the address or command register to accept data. When low, DPRHW-L enables the status or address registers to be read.

Data Path Address Zero (DPA0-H) when low selects the control or status registers. When high, DPA0-H selects the address register.

During a microprocessor read, a low Data Path Control Select (DPCS-L) enables the read/write controller output buffers; and a high DPCS-L tristates the output buffers. During a microprocessor write, data is strobed into the internal registers by the rising edge.

Data Path Interrupt Request (DPIRQ-L), when asserted, interrupts the microprocessor on a read/write fault condition. DPIRQ-L will be

asserted with the positive-going edge of SOS-L, at the end of the sector in which the fault was detected.

DISC DATA BUS

DD0-DD7	Disc Data Bus
DDS-H	Disc Data Strobe
SEF-L	Start ECC Field
SOS-L	Start of Sector
WHO-L	Write Holdoff

Disc data information exchanged between the read/write controller and the DMA/ECC circuitry in controller PCA-A6 is passed over the Disc Data Bus. The bus signals function as follows:

Disc Data Bus (DD0-DD7) is an 8-bit bidirectional bus interconnecting the read/write controller and the DMA/ECC. The bus output is enabled when the read/write controller is commanded to a read mode and Start of Sector (SOS-L) goes low, until SOS-L goes high again.

Data Strobe (DDS-H), normally low, is generated by the read/write controller. Data is transferred between the read/write controller and the DMA/ECC on the negative-going edge of the DDS-H. During a normal sector of read, there will be 276 low-high-low transitions of DDS-H. During a normal sector of write, there will be 278 low-high-low transitions due to two dummy bytes between the CRC and ECC fields.

Start ECC Field (SEF-L) allows the controller in PCA-A6 to switch data paths from the data source driving the bus to the ECC generator.

Start of Sector (SOS-L), originating in the servo system is used in the Disc Data Bus as a handshake line. SOS-L goes high for the duration of the sampled servo field. The falling and rising edges of the signal determine the beginning and end of the data field.

Write Holdoff (WHO-L) can be asserted by the DMA to inhibit a write sector. If asserted prior to the falling edge of SOS-L, it will override a command from the controller, and no read or write will take place.

5-94. Servo Signals. The read/write controller receives the following signals from the servo system:

SOS-L	Start of Sector
WCLK-L	Write Clock
SVER-L	Servo Error

5-95. Read/Write Control Signals. The signals which the read/write controller exchanges with the read/write system electronics are as detailed below:

INPUTS

CURUS-H	Current Unsafe
PARER-H	Parity Error
RDATA	Read Data
RDCLK-H	Read Clock

OUTPUTS

WDATA-H	Write Data
WGTO-L	Write Gate Open
RDEN-H	Read Enable
PAREN-H	Parity Error Enable
HDS1-H, HDS2-H	Head Select 1, 2
CHIP0-H thru CHIP3-H	Chip Select, 0 thru 3
DQUAL-L	Qualification Level
WCS0, WCS1	Write Current Select 0,1

The functions of the servo and read/write signals noted above are summarized in table 5-1.

5-96. Control Section. The control section of the read/write controller contains four registers: a command register, a operation register, an address register, and a status register (with associated fault detect logic.)

The control section can be commanded at any time by controller PCA-A6 to carry out a read or write. The command from PCA-A6, which can occur at any time in the sector, is stored in the command register and is transferred to the operation register on the rising edge of Start of Sector (SOS-L). Every sector must be commanded independently - the controller cannot be commanded to read or write a number of sectors. Once the sector read or write operation is completed, the controller reverts back to an idle state, unless

another command has been received to read or write the next sector.

In the command register, bit 0 commands a write operation for the next sector, bit 1 commands a read operation for the next sector, bit 3 clears the status register, bit 5 enables detection of a parity error, and bit 6 enables a detection of a servo error during a read.

The read or write command from PCA-A6 includes head address information. This is entered into the address register. The address information is decoded into read preamplifier/write driver IC and head select data.

In the address register, bits 0 through 3 comprise the address of the head being addressed for reading, writing, or sampled servo; bits 4 and 5 are the two most significant bits of the cylinder address; and bits 6 and 7 change the characteristics of the read/write circuitry for diagnostic and error recovery purposes.

Outputs from the operation register provide the appropriate signals to operate the desired portion of the read/write electronics. These outputs include Write Gate Open (WGTO-H) and Parity Error Enable (PAREN-H).

During a read or write operation, status information is entered into the fault detect circuitry. A fault can occur at any time during a read or write. However, in order not to confuse controller PCA-A6, this information is not reported via the status register until the end of the sector, when Data Path Interrupt Request (DPIRQ-L) is activated. If a write fault that could endanger data is detected, the read/write controller immediately stops the write with the Write Gate Open (WGTO-L) line. However, the controller is not informed at this time.

In the status register, bits 0 through 7 contain the read/write system errors reported to controller PCA-A6. These errors are described in later paragraphs.

5-97. **Encoder/Decoder Section.** The encoding scheme used in the encoder/decoder section of the read/write controller is called variable length frequency modulation (VLFM). This scheme produces 1.33 bits per flux reversal. The code algorithm is shown below:

DATA PATTERN	TRANSITION PATTERN
00	X01
01	010
10	X10
1100	010001
1101	X00000
1110	X00001
1111	010000

X = 1 if followed by 0, otherwise 0

The code is structured using data blocks of two- or four-bit length. There are four possible combinations in the two-bit block, but VLFM only uses three of them (00, 01, and 10). If "11" is encountered in a string of data, a four-bit block will be encoded (instead of a two-bit block). Only four of the sixteen possible four-bit combinations are encoded (1100, 1101, 1110, and 1111). These three two-bit patterns and four four-bit patterns cover all possible data sequences.

All two-bit blocks are mapped into three bits, and all four-bit blocks are mapped into six bits. At first glance, this would appear to be more of a disadvantage than an advantage, but design of the data map ensures that the worst case data pattern generates transitions on the disc surface that are further apart than other previously employed codes. This means that the data can be packed tighter on the data surface.

Implementation of the VFLM coding is achieved in the encoder/decoder section with a shift register, pattern detector, and bit generator, together with a clock generator and byte counter. These components are used for both reading and writing and the recognition of the framing word.

When a write is performed, Write Clock (WCLK-L), from the servo system, is fed to the clock generator. This generator supplies two 3-phase clock pulses which are used to control all of the functions on the read/write controller.

The clock generator drives the byte counter and its outputs are decoded to identify all of the operations that occur during a sector. In the case of a write, there are 14 bytes of sync field, followed by the framing word, and then data.

Immediately after the framing word, parallel data is accepted from the Disc Data Bus (DD0-DD7) lines, as clocked in with Disc Data Strobe (DDS-H) from the byte counter. The data, which comes from the DMA/ECC circuitry in controller PCA-A6, is parallel loaded into the shift register. Once a byte is loaded, the contents of the register are examined by the pattern detector, which looks for two-bit and four-bit patterns, as shown in the VLFM code algorithm.

The output of the pattern detector is coupled to the bit generator. For every two bits interrogated, the bit generator outputs three bits of write data on the WDATA line. The write data is RZ encoded. Every transition is a pulse, which drives a toggle in the write chain, causing a change in the direction of the current in the write head.

At a certain point in the sector, Start ECC Field (SEF-L) is generated by the byte counter. This signal changes the data path from the DMA to the ECC. Due to the slowness of the ECC IC, the DMA puts out two dummy bytes after SEF-L is received. These dummy bytes are not written to the disc.

When a read is performed, Write Clock (WCLK-L) is used until the read phase-locked loop is synchronized. At this time, the clock generator switches to Read Clock (RDCLK-L).

After the framing word is recognized, data is passed through the shift register to the pattern detector. The resulting serial decoded data is clocked in bytes to the Disc Data Bus (DD0-DD7) lines with Disc Data Strobe (DDS-H). At the appropriate time, the byte detector enables Start ECC Field (SEF-L) line, causing data to be transferred to the ECC IC.

5-98. HEAD SELECT ENCODER. Due to mechanical layout restrictions, the physical head locations in the head-disc assembly do not match the addresses required to access them. The head select encoder maps address register outputs CHIP0-H through CHIP3-H and HS1-H, HS2-H from the read/write controller to select the proper heads.

The head select encoder outputs are labeled Chip Enable (CE0-L through CE3-L) and Head Select (HS1-L, HS2-L).

Two additional outputs, labeled Channel 0,1 (CH0-H, CH1-H), together with HDS1-H, HDS2-H are used to address the head gain reference PROM in the HDA. This circuit is discussed in the servo system functional description.

5-99. READ CHAIN. Included in the read chain are a filter and amplifier stage, zero-crossing detector, AGC circuit, and PLL and data separator stage. The input to the chain is a stream of VLFM-encoded pulses from the media, labeled Read/Write Data (DX, DY). This differential analog signal is filtered, amplified, and converted to TTL-level NRZ form before being applied to the input of the PLL and data separator stage. From the NRZ data, the PLL and data separator supplies a stream of ones and zeros, accompanied by a synchronous clock, to the encoder/decoder section of the read/write controller IC for further processing.

5-100. Filter and Amplifier. Included in the filter and amplifier stage are a number of filters, an AGC amplifier, and a video amplifier.

The filters attenuate signals at frequencies higher than signal frequencies from the media. The filters also provide the proper group delay of frequency to match the read path and provide the proper timing of the read data.

Automatic gain control of the read data is controlled by the AGC amplifier. The amplifier amplifies the Read/Write Data (DX, DY) signal by a gain proportional to the amplitude of the AGC signal from the AGC circuit.

The video amplifier has a gain of 100 and acts as a buffer amplifier. The differential analog output from the amplifier is fed to the input of the zero-crossing detector and the AGC circuit.

5-101. AGC Circuit. The AGC circuit examines the amplitude of the video amplifier output and determines the amount that the gain of the AGC amplifier has to be increased or decreased in order to keep the amplitude constant. The action of the

AGC circuit is gated by Read AGC Gate (RAGC-H, RAGC-L) from the sampled servo timing circuit and Write Gate Open (WGO-L), from the read/write controller. This gating allows only the data sync field in each sector to determine the amplitude of the AGC signal. The AGC circuit output is labeled Automatic Gain Control (AGC).

5-102. Zero Crossing Detector. The zero-crossing detector converts the differential analog output of the video amplifier into TTL-level pulses. Each data transition, positive or negative, results in a high-true signal at the detector output. The output signal, labeled NRZ Data (NRZ-H), is coupled to the input of the read chain PLL and data separator stage.

5-103. PLL and Data Separator. The function of the phase-locked loop (PLL) and data separator stage is to phase lock a clock source to the read-back data stream from the disc and separate the data transitions into timing windows, thus generating a synchronous clock and a data stream of VLFM-encoded ones and zeros.

The circuit consists of a voltage-controlled oscillator (VCO) clock source which is locked up to one of two input signals, depending on the drive mode of operation. During seeks or writes the VCO is in a frequency hold (locking) mode, where it is locked to Differential Write Clock (DWC-L, DWC-H), derived from the dedicated servo surface. During a read, the VCO is in a phase lock (tracking) mode of operation where the NRZ-H data stream from the zero-crossing detector is fed to the clock source. The changeover between the two modes is controlled by Read Enable (RDEN-L) from the read/write controller IC.

Included in the PLL and data separator are a phase detector, a frequency detector, and a controlled clock source. The phase detector compares the phase of the data source to that of the clock source and outputs a signal proportional to their difference. The frequency detector compares the frequency of the clock source and outputs a signal proportional to their difference. The controller clock source advances, maintains, or delays the phase of the output clock as commanded by a plus, zero, or minus input signal. The outputs from the PLL and data separator are are labeled Read Data (RDATA) and Read Clock (RDCLK). Both signals are fed to the encoder/decoder section of the read/write controller IC.

5-104. Sampled and Dedicated Servo Amplifiers. The sampled and dedicated servo amplifiers contained on read/write PCA-A2 are described in the servo system functional description.

5-105. WRITE CHAIN. Signal Write Gate Open (WGTO-L) to the write chain is clocked true by the falling edge of Start of Sector (SOS-L) when a write command has previously been entered in the command register. When WGTO-L is low, the write chain supplies write current on Write Current (WC) line to the read preamplifier/write driver ICs in the head-disc assembly.

The read preamplifier/write driver ICs are set in a write mode of operation by Write Select A, B (WSA, WSB). A high level (approx 3.5V) on these lines select the write mode.

Each time a positive edge is seen on the Write Data (WDATA) line from the encoder/decoder, a D-type flip-flop in the chain steers current into either the DX or DY line to write data on the disc.

A number of outputs from the write chain are used in the factory to write the dedicated servo code. These signals include Servo Write Select (SWS), Servo Write Current (SWC), and Servo Head Select (SHS-H). After the drive is manufactured, SHS-H is permanently set low, effectively limiting the servo head to read-only operation.

5-106. READ/WRITE SYSTEM ERRORS. Details of the errors detected by the read/write system are provided in the following paragraphs.

5-107. Unsafe Current in Read/Write ICs. This error indicates that an unsafe current has been detected in one of the read preamplifier/write driver ICs. The error could indicate multiple selection of the read preamplifier/write driver ICs or lack of data during a write.

The error can occur any time during the sector.

Write is disabled immediately upon detection of the error and continues to be disabled until status is cleared. Interrupt (RWIRQ-L) is asserted at the end of the sector in which the error occurred. Interrupt and the status register can be cleared by a clear command to the command register.

5-108. Data Overrun Detected. This error indicates that the data transfer has not been completed by the time SOS-L starts to go high. During a write, this indicates that an inconsistency exists between SOS-L and WC from the servo system, or a hardware failure. During a read, the error probably indicates a loss of lock by the read/write system PLL, or the data framing word was not detected. (A data framing word might be detected in random data, leading to a partially transferred erroneous sector.)

The error occurs only at the end of a sector. Interrupt is asserted and write is disabled until the status register is cleared. Interrupt and the status register can be cleared by a clear command to the status register.

5-109. Write Holdoff Command Abort. This error indicates that the write operation was aborted because Write Holdoff (WHO-L) was asserted at the falling edge of SOS-L.

The error will only occur at the beginning of a sector. Write is disabled immediately upon detection, and until the status register is cleared. Interrupt is asserted at the end of the sector. Interrupt and the status register can be cleared by a clear command to the status register.

5-110. Write With Servo Error. This error indicates that a write was aborted because a Servo Error (SVER-L) was detected by the servo system.

5-111. Parity Error During a Read With Mask Set. This error indicates that a parity error was detected in the amplitude qualification circuitry (probably dropout). The error is used primarily for defect location in media test.

Read is not disabled until the next sector. Interrupt is asserted at the end of the sector in which the error occurred. Interrupt and the status register can be cleared by a clear command to the status register. This action occurs if the bit mask is not set.

5-112. Servo Error During a Read with Mask Set. This error indicates that a servo system off-track error or sampled servo error occurred during the previous read operation. This error is used primarily for defect location for sparing.

Read is not disabled until the following sector. Interrupt is enabled at the end of the sector in which the error occurred. Interrupt and the status register can be cleared by a clear command to the command register. No action occurs if the mask bit is set.

5-113. Underrun. This error signals that a underrun was detected in the data operation. This indicates that a read or write completed too soon relative to the rising edge of Start of Sector (SOS-L), which marks the end of the sector.

During a read operation, the error probably indicates a loss of lock by the read/write system PLL, causing the read clock to go to a higher than normal frequency and leading to an early completion of the data transfer.

An underrun in a write operation and in a read operation (not caused by a PLL loss of lock) would indicate a failure to receive SOS-L at the proper time or an out of sync write clock. These problems are probably related to the operation of the servo system.

5-114. ERROR REPORTING. The read/write system errors detailed above are reported to the microprocessor in PCA-A6 via the read/write controller status register.

5-115. SPINDLE DRIVE SYSTEM

The principal component in the spindle drive system is an ac induction motor which transmits its torque to the spindle assembly via a belt drive system. The motor is powered by the ac line voltage input to the drive. In the standard drive (60 Hz),

the spindle speed is 3600 rpm, ±7 percent. The actual speed is controlled by the frequency and voltage of the ac input. In the option 015 drive (50 Hz), a different size of motor pulley and drive belt keep the spindle speed within the same speed range. A squirrel-cage type fan attached to the shaft at the other end of the motor circulates cooling air through the drive.

Also included in the spindle drive system are cable assemblies, primary power PCA-A8, servo PCA-A1, read/write PCA-A2, and power distribution PCA-A5. See figure SD.

The following paragraphs provide a more detailed description of the spindle drive system components. Refer to table 5-1 for a description of the mnemonics used in the text and the functional block diagram. Refer also to table 12-1 for detailed signal distribution information.

5-116. AC INPUT CIRCUIT

Power is applied to spindle motor B1 via the ac input connector, line filter FL1, input power cable W1, and primary power PCA-A8. At PCA-A8, the motor windings can be configured for 90-132 Vac or 180-264 Vac operation by connecting the motor power plug to the appropriate connector on primary power PCA-A8.

5-117. SPINDLE MOTOR B1

Spindle motor B1 is a 2-pole capacitor start/run induction motor with its torque transmitted to the spindle assembly through a belt drive system. The motor windings are split to allow operation from either a 90-132 Vac or 180-264 Vac power source. The motor can operate within a range of 47 to 67 Hz (50 Hz or 60 Hz). To maintain the spindle speed at 3600 rpm, ±7 percent, different drive pulleys and drive belts are used for 50 Hz and 60 Hz operation.

The motor runs/start capacitor is mounted on the motor and start capacitor C1 and associated start relay K1 are mounted on primary power PCA-A8.

Automatic thermal reset protection circuitry incorporated in the motor provides overload protection.

A brake mounted on the shaft of the motor brings the motor to a rapid halt when ac power is removed from the drive.

5-118. PRIMARY POWER PCA-A8

The principal function of primary power PCA-A8 is to facilitate the changeover of the spindle motor windings and the input of the brake voltage source when the drive power configuration is changed from 90-132 Vac to 180-264 Vac, or vice versa. This is achieved by connectors J1 and J2, labeled "115 Vac" (for 90-132 Vac), and "240 Vac" (for 180-264 Vac), respectively. Voltage configuration is achieved by connecting the plug on the motor cable to the appropriate connector. (It should be noted that ac voltage configuration for power supply PCA-A4 is not performed at PCA-A8 -- a jumper on PCA-A4 must be set to the match the ac input voltage range.)

Other components on PCA-A8 include the drive LINE~ switch, spindle motor start capacitor and relay, and DC voltage source for the motor brake.

5-119. LINE~ SWITCH. The drive LINE~ switch is a 2-pole switch mounted on PCA-A8. The switch is activated by a pushbutton on the drive front panel.

5-120. START CAPACITOR AND RELAY. At power on reset, start relay K1 connects start capacitor C1 in parallel with the run/start capacitor on the spindle motor. Start capacitor C1 provides more phase lead in the motor start winding current and thus more torque. The relay is activated by Start Capacitor signal (SCAP-L) from the servo controller in servo PCA-A1. The length of time that SCAP-L is active depends on how long it takes the spindle to reach a speed of greater than 3000 rpm. This is determined by the servo controller monitoring Speed Sense (SPDSNS-L) from the speed sensor.

Control of the start capacitor is part of the servo controller spin-up routine. The servo controller measures the time between SPDSNS-L pulses to determine the speed of the spindle. The start relay is turned on until 3000 rpm is reached or spin up

fails. If the spindle speed does not measure 3000 rpm within approximately 13 seconds, the start relay is turned off and spin up fails. Without a successful spin up, no functional commands (recalibrate, seek, etc.) can be executed.

5-121. BRAKE VOLTAGE SOURCE. The motor brake is an electromechanical device, powered by 24 Vdc from transformer T1 and full-wave rectifier CR1 on PCA-A8. The primary windings of the transformer are connected to the ac input via jumpers in the connector which connects the motor leads to connector J1 ("115 Vac") or J2 ("240 Vac") on PCA-A8. The windings are connected in parallel for a 90-132 Vac input and in series for a 180-264 Vac input. The 24 Vdc output from CR1 holds the brake off when the drive LINE~ switch is in the on position. When power is turned off, the loss of DC voltage immediately causes the brake to be applied.

5-122. SPEED SENSOR

The speed sensor is a Hall-effect device mounted adjacent to the spindle drive pulley. A magnet, embedded in the pulley, triggers the sensor once per revolution of the pulley. The sensor output, labeled Speed Sense (SPDSNS-L), is connected to the servo controller in servo PCA-A1.

5-123. SERVO PCA-A1

The servo controller in servo PCA-A1 generates Start Capacitor (SCAP-L) and monitors Speed Sense (SPDSNS-L) during the drive spin up (start) operation. This operation is discussed in the servo system functional description.

5-124. READ/WRITE PCA-A2

Signals SPDSNS-L and SCAP-L are routed through read/write PCA-A2 and signal jumper cable W7 to power distribution PCA-A5.

5-125. POWER DISTRIBUTION PCA-A5

Power distribution PCA-A5 receives Speed Sense (SPDSNS-L) from the speed sensor via Speed sensor cable W5 and routes the signal to servo controller PCA-A1 via signal jumper cable W7 and read/write PCA-A2. PCA-A5 also supplies +5V to the speed sensor via cable W5.

Signal Start Capacitor (SCAP-L) from servo PCA-A1 is routed through PCA-A5 to the start relay in primary power PCA-A8 via power supply cable W4. PCA-A5 also supplies +5V to the relay via cable W4.

5-126. POWER SUPPLY SYSTEM

The power supply system develops DC operating voltages from the ac line voltage and distributes these voltages throughout the drive. The output voltages are ±45V unregulated; and ±12V, +5V, and -5.2V regulated. The power supply system also includes fault circuitry which shuts down drive operation for over voltage, over current, under voltage, or power supply overheating. Control signals Power On Reset (POR-L) and Power Fail (PF-L) are also generated by the system.

In addition, the signals from controller PCA-A6 which control the operation of the front panel LED display are routed through the power supply system cabling to LED PCA-A7.

The power supply system consists of cable assemblies, mainframe wiring, primary power PCA-A8, power supply PCA-A4, power distribution PCA-A5, and circuits in servo PCA-A1 and read/write PCA-A2. See figure PS.

The following paragraphs provide a more detailed description of the power supply circuitry. Refer to table 5-1 for a description of the mnemonics used in the text and the functional block diagram. Refer also to table 12-2 for detailed voltage distribution information.

5-127. AC INPUT CIRCUIT

The ac line voltage is connected to the input of power supply PCA-A4 via the power cord, line filter FL1, primary power cable W1, the LINE~

switch in primary power PCA-A8, and power supply input cable W3. The rear panel line fuse is part of line filter assembly FL1.

5-128. PRIMARY POWER PCA-A8

The drive LINE~ switch is located on PCA-A8 and is operated by a push button on the drive front panel.

It should be noted that the voltage selection made at PCA-A8 for 90-132 Vac or 180-264 Vac operation is for spindle motor B1. See figure SD . To configure power supply PCA-A4 for 90-132 Vac or 180-264 Vac, a 2-pin plug on PCA-A4 must be placed in the correct position.

5-129. POWER SUPPLY PCA-A4

Power supply PCA-A4 is a self-contained unit which employs switching regulator circuitry. Included in the supply are a primary control circuit, six output sections, and fault detection and protection circuitry.

5-130. PRIMARY POWER SELECTION. Primary voltage selection of 90-132 Vac or 180-264 Vac for power supply PCA-A4 is performed by a 2-pin plug which must be placed in one of two adjacent connectors on PCA-A4. The location of these connectors, labeled "115V" (for 90-132 Vac) and "230V (for 180-264 Vac), is shown in figure 12-16.

5-131. PRIMARY CONTROL CIRCUIT. A control integrated circuit is used to control the output voltages on the ±45, ±12, and +5 Vdc lines. The control IC also provides coarse regulation for the -5.2 Vdc supply. This supply uses a linear regulator for final regulation. The control IC in effect regulates the +5 Vdc output. This is accomplished by varying the ac voltage applied to the primary of the main power transformer.

5-132. OUTPUT SECTION. Each output voltage is derived from a separate secondary winding on the main transformer. The turns ratio for each supply is selected so that the proper voltage appears at the output of a full wave rectifier when the +5 Vdc output is correct. Each supply also has a LC filter to smooth the rectifier output.

5-133. FAULT DETECTION AND PROTECTION. The power supply can detect overcurrent and overvoltage conditions on all outputs. When either condition occurs, the primary is turned off and the supply shuts down. After an overvoltage condition has been detected and its cause removed, the power supply can be returned to normal operation by turning the LINE~ switch off for at least one minute, and then turning it back on again. The supply can be returned to normal operation in a similar fashion following the detection and removal of an overcurrent condition.

Undervoltage is detected on the +5V, -5.2V, +12V, -12V outputs. In each case, when an undervoltage is detected, Power On Reset (POR-L) is asserted. This resets the drive electronics and controller PCA-A6. If the undervoltage is caused by a loss of primary power, Power Fail (PF-L) is asserted to signal that a primary power failure has occurred. Signal PF-L is asserted two milliseconds before any supply goes out of regulation. Signal PF-L is used by controller PCA-A6 to stop operations that would be interrupted by the assertion of POR-L.

5-134. POWER DISTRIBUTION PCA-A5

Power distribution PCA-A5 filters the dc outputs from PCA-A4, and acts as a distribution point for these voltages. Signals Power On Reset (POR-L) and Power Fail (PF-L) are also routed through PCA-A5.

5-135. READ/WRITE PCA-A2

Read/write PCA-A2 contains two IC voltage regulators which supply -4 Vdc and +6 Vdc to the read preamplifier/write driver ICs in head-disc assembly A3. The regulators are powered by +12 Vdc from power supply PCA-A4.

Signals POR-L and PF-L are buffered in read/write PCA-A2 before being sent to servo PCA-A1 and controller PCA-A6.

5-136. SERVO PCA-A1

Servo PCA-A1 contains an undervoltage detector which monitors the -45 Vdc and +45 Vdc outputs from PCA-A4. If either supply drops below approximately 24 Vdc, the servo power amplifier is turned off. The output signal from the detector is labeled Under Voltage (UNDER VLT-L). Refer to the description of the servo system amplifier error detection circuit for additional details.

5-137. LED DISPLAY

The signals from controller PCA-A6 which control operation of the front panel LEDs are labeled Red LED (RLED), Green LED (GLED), and Yellow LED (YLED). From PCA-A6, these signals are coupled to LED PCA-A7 via read/write PCA-A2, signal jumper cable W7, power distribution PCA-A5, and power supply output cable W4. An LED is lit when the controller pulls the appropriate control line low.

The +5v anode voltage for the LEDs, labeled LED Power (LEDP), originates in read/write PCA-A2, and is sent to LED PCA-A7 via the same path as RLED, GLED, and YLED.

5-138. HDA AIR FILTRATION

A recirculating air filtration system within sealed head-disc assembly A3 purges the air in the assembly of particulate contamination. In addition, a chemical filter and desiccant chamber, connected at the intake of a breather filter, removes corrosive gases and moisture from the incoming air. This is to prevent corrosion from occurring on the thin-film surfaces of the discs.

5-139. RECIRCULATING FILTER

The recirculating filter is a 60 percent/0.3 micron filter. The circular shape of the HDA cover and the rotational speed of the discs cause the inlet of the filter to be pressurized. This results in the filtration of approximately seven to eight volumes of HDA air per minute.

5-140. BREATHER FILTER

The breather filter is a 99.9 percent/0.3 micron filter which allows the pressure to equalize within the HDA.

5-141. CHEMICAL FILTER AND DESICCANT CHAMBER

The chemical filter and desiccant chamber remove corrosive chemicals and moisture from the incoming air to the HDA. The chemical filter is composed of multiple layers of carbon, copper, and nickel foam which react with incoming gases. The desiccant chamber dries the incoming air to less than 5 percent relative humidity.

5-142. DRIVE AIR FLOW

Air is circulated through the drive by a squirrel-cage type fan driven by the induction motor used to rotate the spindle assembly. The impeller of the fan is attached to the motor shaft at the end opposite the spindle pulley. See figure 12-3. Air is drawn into the drive at a rate of 38.7 litres/second (82 cubic feet/minute) through slots in the front panel and exhausted through openings in the rear panel. The air circulation pattern through the fan and the interior of the drive is shown in figure 12-3.

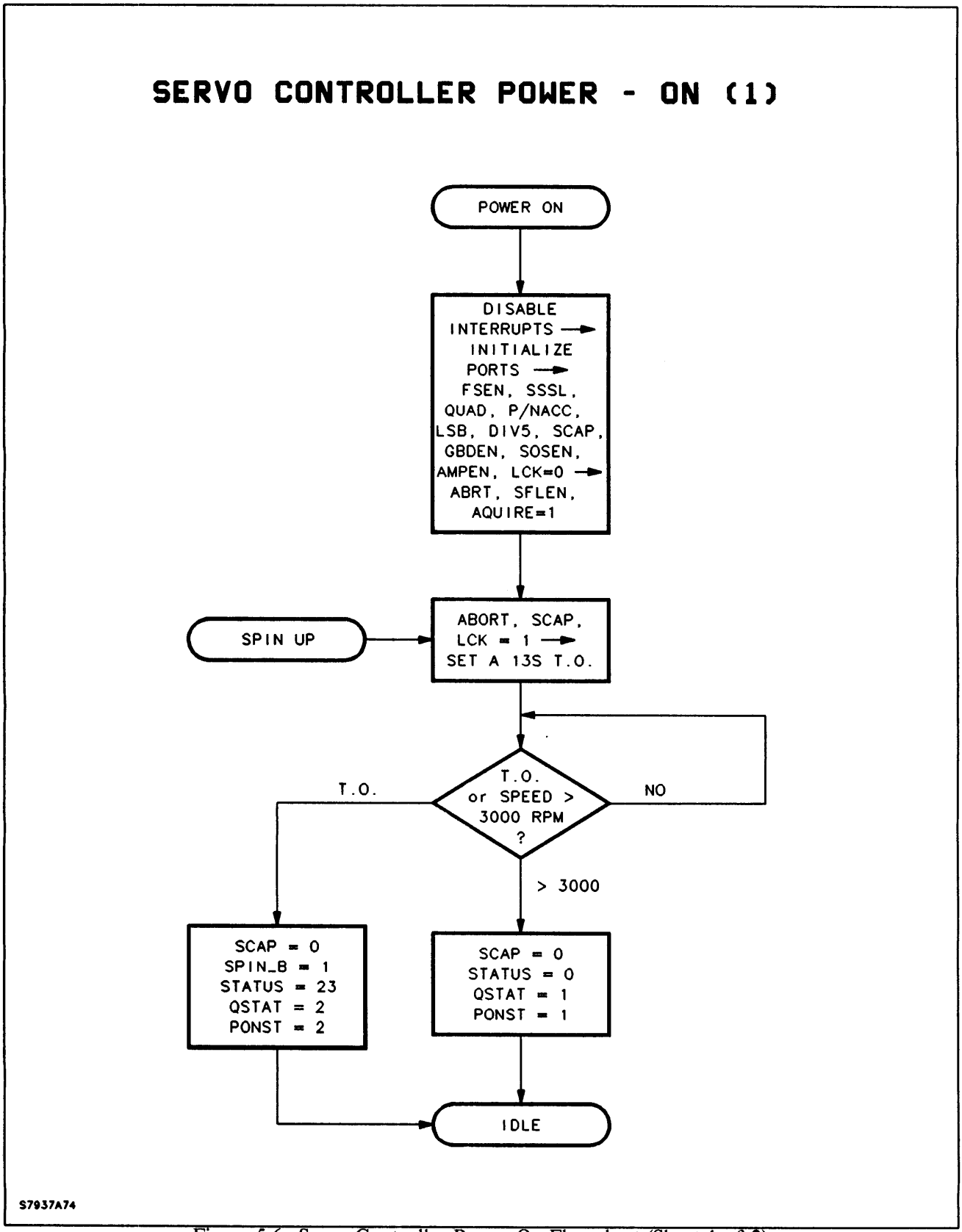


Figure 5-6. Servo Controller Power On Flowchart (Sheet 1 of 2)

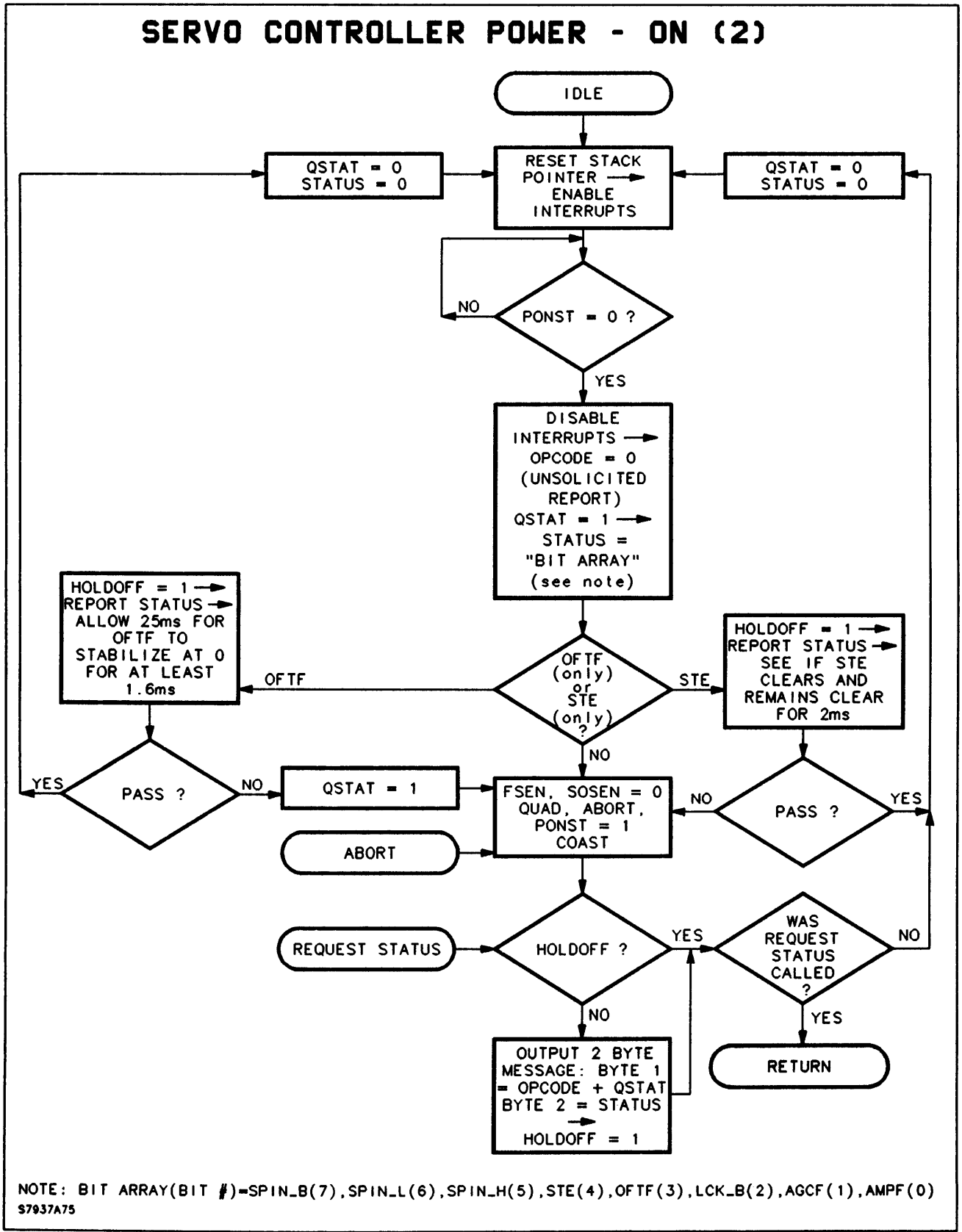


Figure 5-6. Servo Controller Power On Flowchart (Sheet 2 of 2)

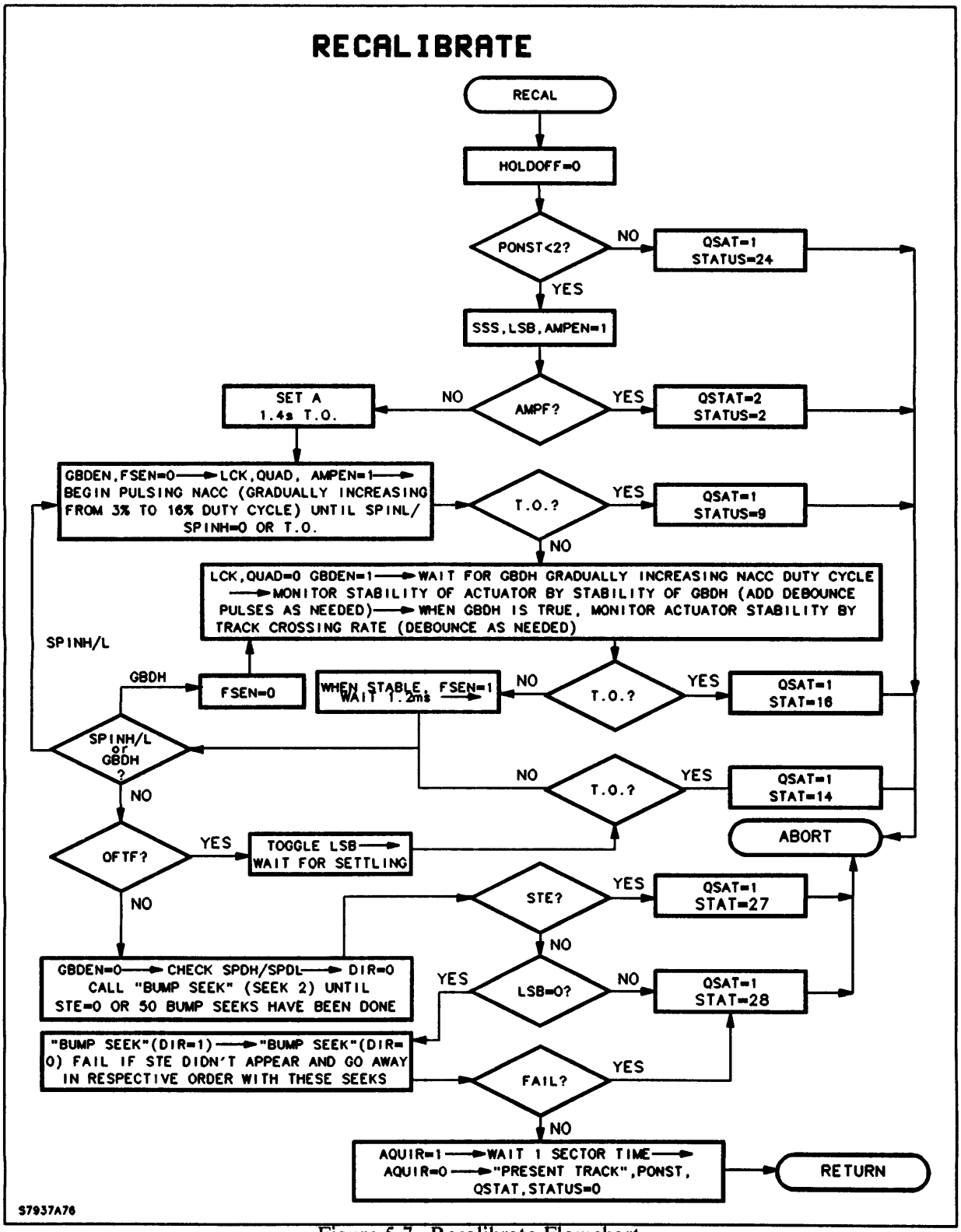


Figure 5-7. Recalibrate Flowchart

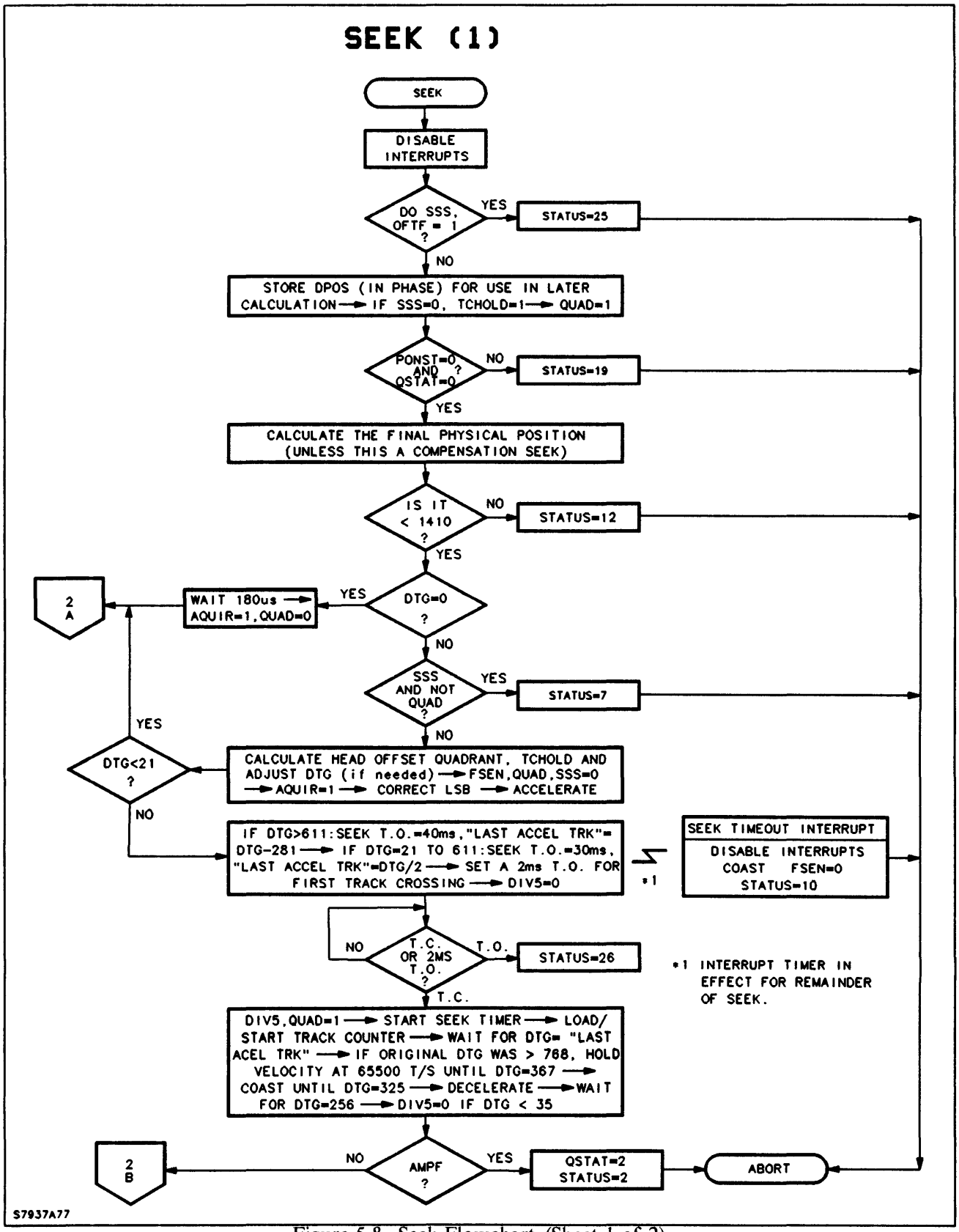


Figure 5-8. Seek Flowchart, (Sheet 1 of 2)

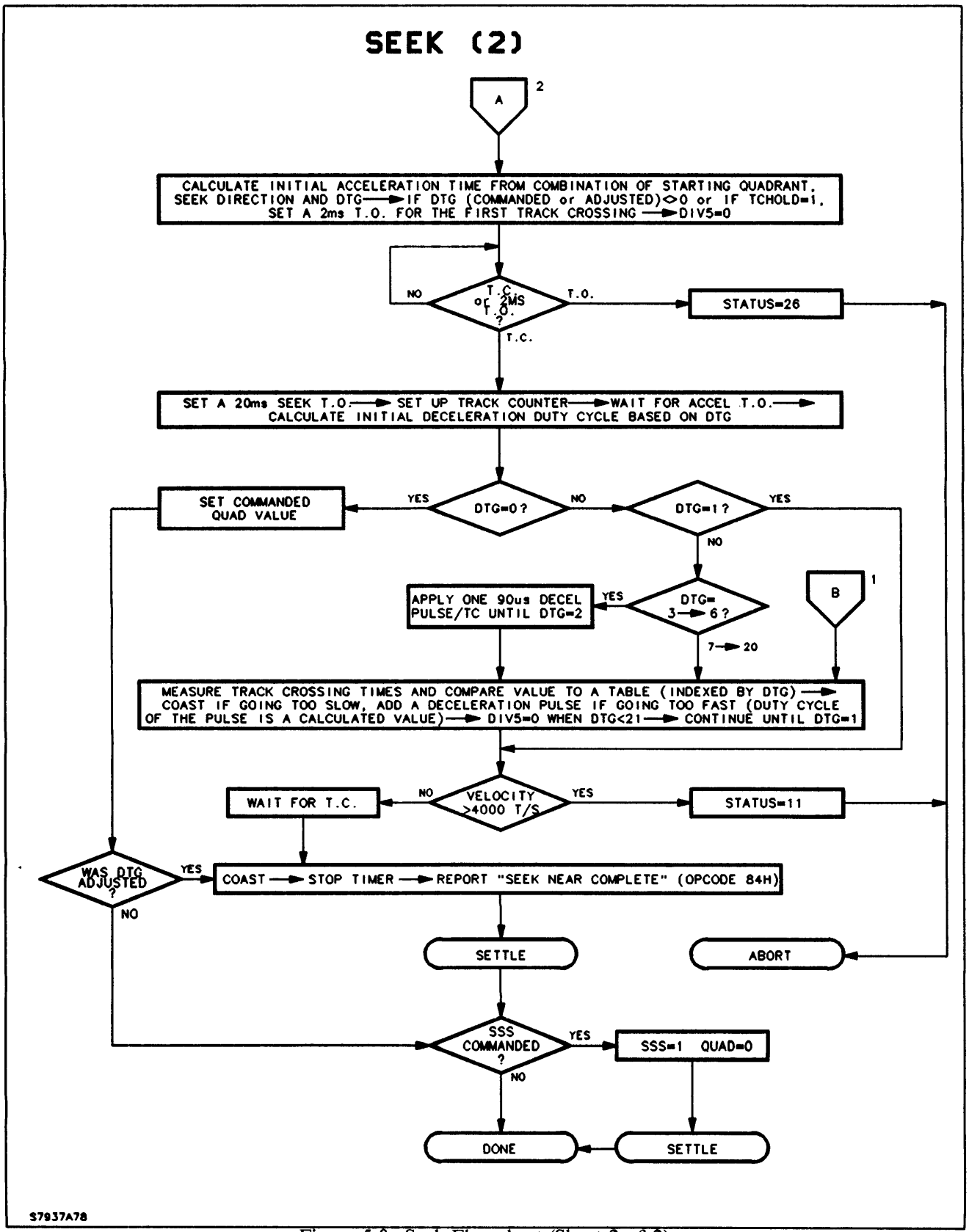


Figure 5-8. Seek Flowchart (Sheet 2 of 2)

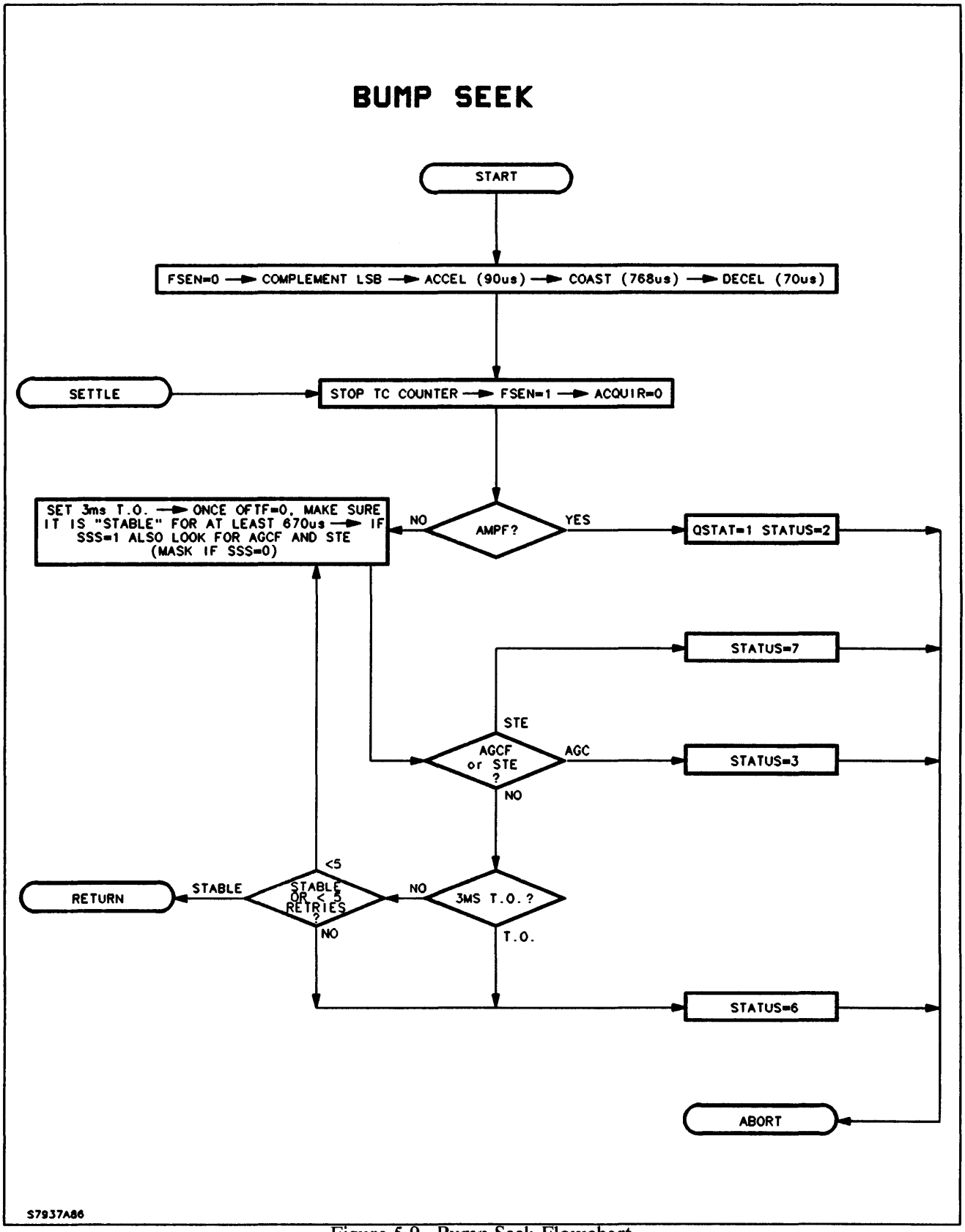


Figure 5-9. Bump Seek Flowchart

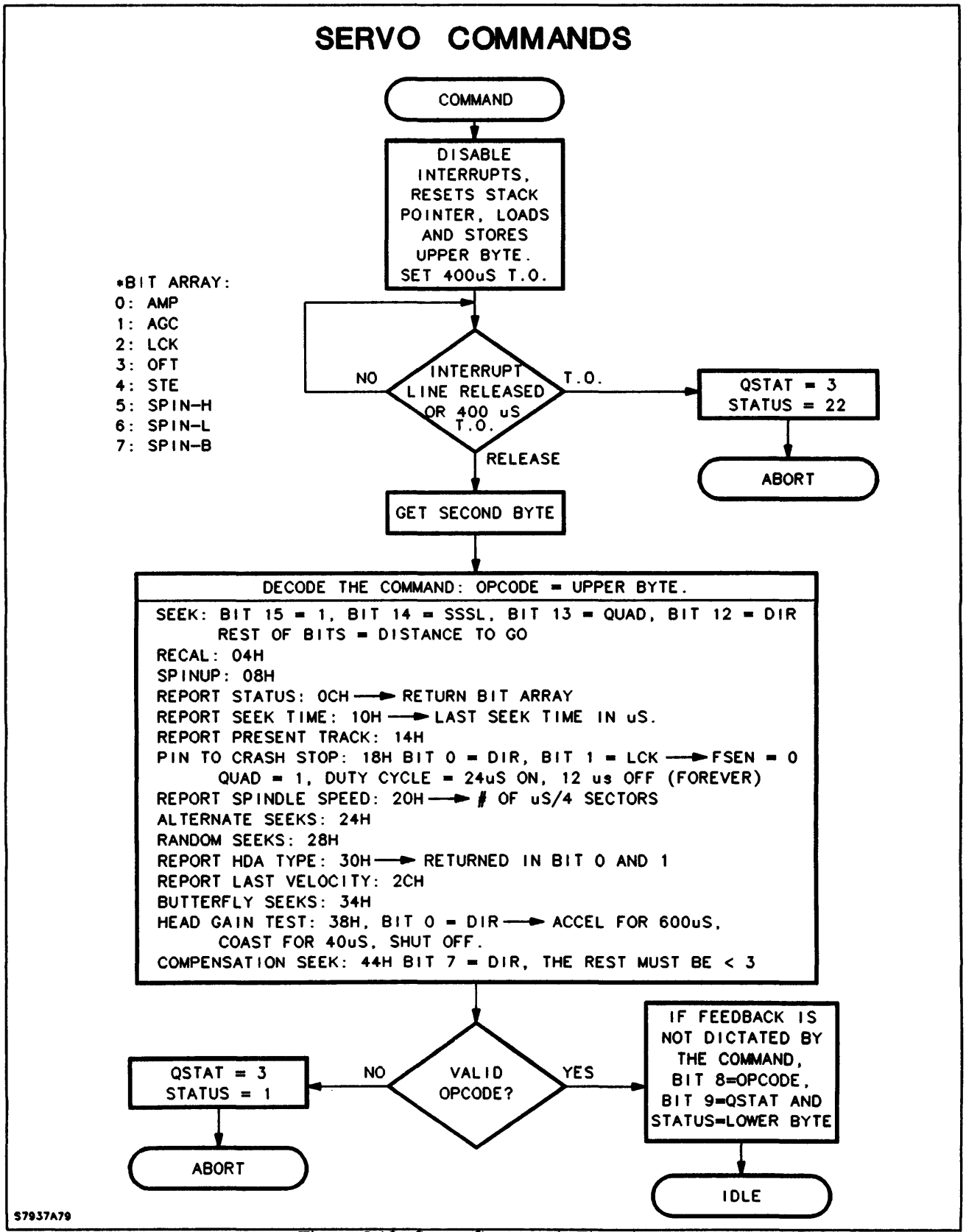


Figure 5-10. Servo Commands Flowchart

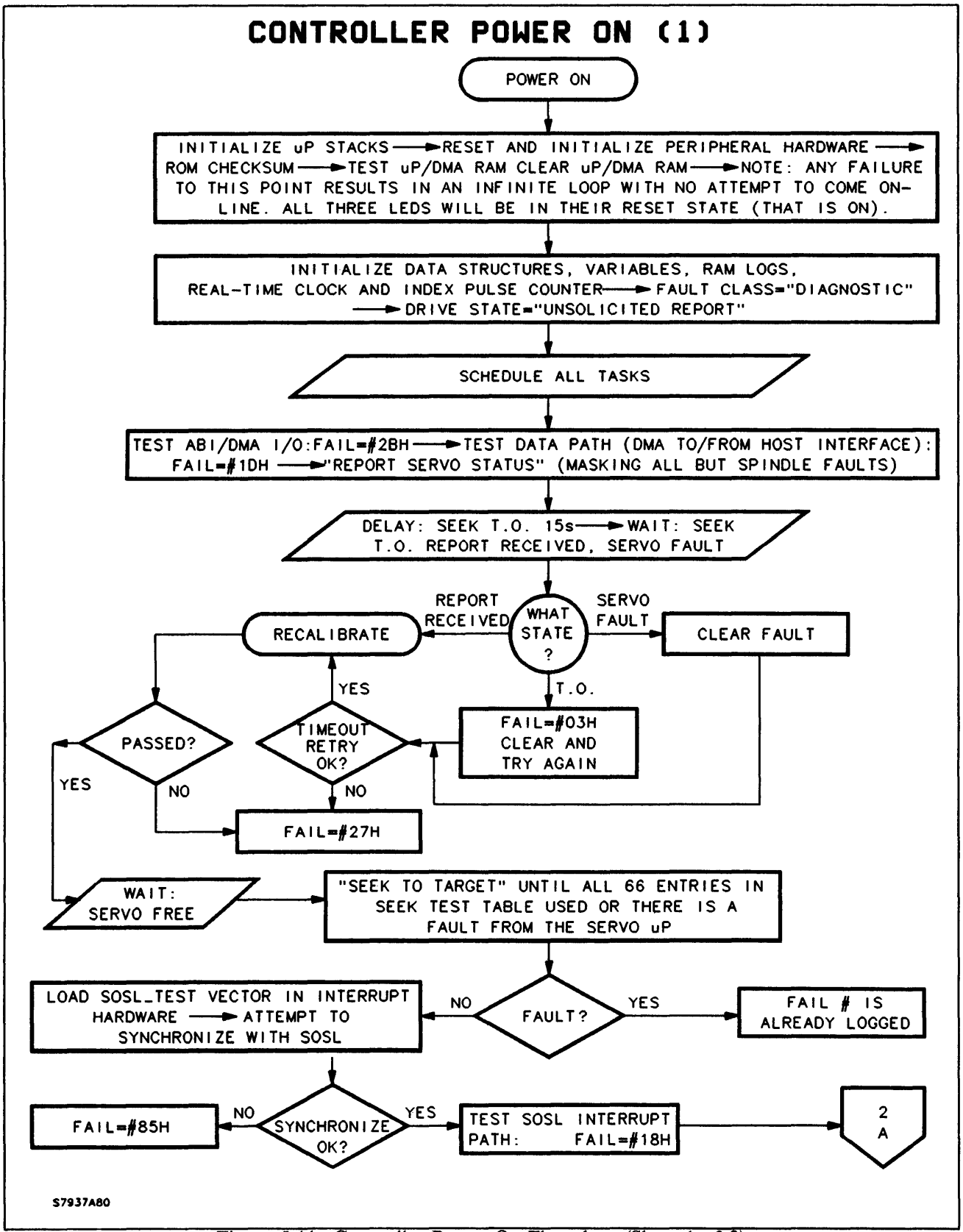


Figure 5-11. Controller Power On Flowchart (Sheet 1 of 2)

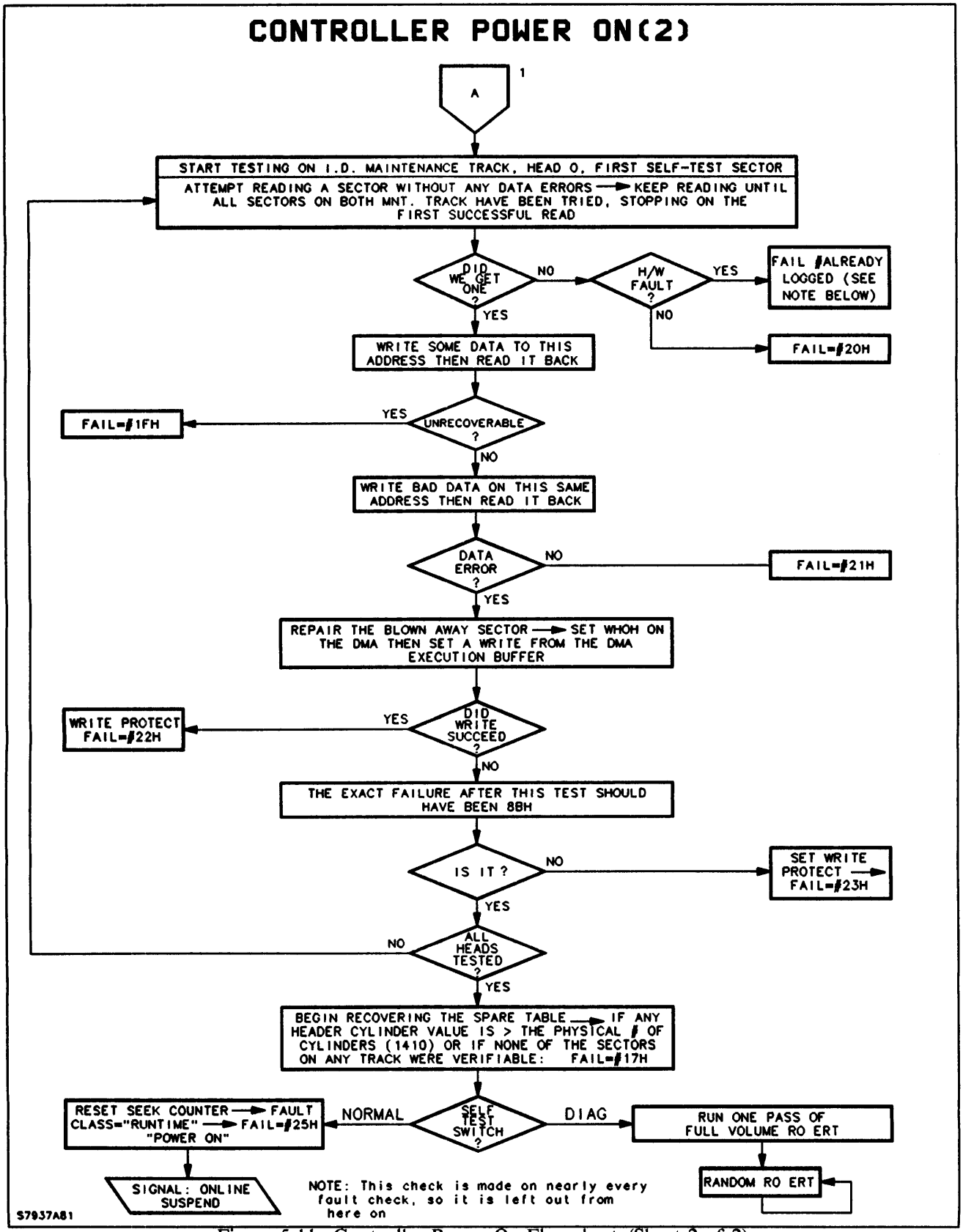


Figure 5-11. Controller Power On Flowchart, (Sheet 2 of 2)

Table 5-1. List of Mnemonics (1 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
ACQUIRE-H	Acquire	S1 A1	SERVO CONTROLLER output to SAMPLED SERVO TIMING circuit. ACQUIRE-H is used to synchronize the timing of the dedicated and sampled servo circuits.
ACUR	Actuator Current*	S2 A1	Output of CURRENT SENSE AMPLIFIER. Equivalent voltage is 2 volts for every 1 ampere of current in actuator. ACUR can be monitored at pin 4 of the servo test point PCA.
AGC	Automatic Gain Control	RW A2	AGC CIRCUIT analog output that controls the gain of the AGC amplifier in the read chain FILTER and AMPLIFIER stage.
AGCF-L	AGC Fault*	S1 A1	AGC INTEGRATOR output to SERVO CONTROLLER. AGCF-L is active when level of sampled servo is too far above or below a reference. AGCF-L can be monitored at pin 40 of the servo test point PCA.
AMPEN-H	Amplifier Enable	S1 A1	SERVO CONTROLLER output to AMPLIFIER CONTROL and FAULT INDICATION circuit. See figure S2 . The servo power amplifier is off when AMPEN-H is low and is turned on by the rising edge of AMPEN-H (assuming that there are no amplifier faults.)
AMPFLT-L	Amplifier Fault*	S2 A1	AMPLIFIER CONTROL and FAULT INDICATION output to SERVO CONTROLLER. See figure S1 . AMPFLT-L is latched low if any one of the following servo fault conditions occurs: Servo Processor Reset SPR-L goes low, an under voltage (+45V or -45V) condition is detected, an overvoltage condition is detected, or the 100-KHz clock in the PWM fails. The fault is cleared on the rising edge of AMPEN-H. AMPFLT-L can be monitored at pin 32 of the servo test point PCA.

Table 5-1. List of Mnemonics (2 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
ASMP-L	A Sample	S1 A1	DEDICATED SERVO TIMING and PLL output to POSITION DEMODULATOR. ASMP-L is a timing signal used to sample dedicated servo bits.
BSMP-L	B Sample	S1 A1	DEDICATED SERVO TIMING and PLL output to POSITION DEMODULATOR. BSMP-L is a timing signal used to sample dedicated servo bits.
BSOS-L	Buffered Start of Sector	RW A2	BSOS-L is an address line to the HEAD GAIN REFERENCE PROM in HDA A3. BSOS-L switches the head gain PROM address from read/write heads to servo head. BSOS-L is connected to the PROM in HDA A3 via HDA cable W8.
CE0-L thru CE3-L	Chip Enable, bits 0 thru 3	RW A2	HEAD SELECT ENCODER outputs which, together with Head Select bits HS1-H, HS2-H, are decoded by the READ PREAMP/WRITE DRIVER ICs to select the desired read/write head. CE0-L thru CE3-L are connected to the READ PREAMP/WRITE DRIVER ICs in HDA A3 via HDA cable W8.
CH0-H, CH1-H	Chip 0,1	RW A2	HEAD SELECT ENCODER address lines to the HEAD GAIN REFERENCE PROM in HDA A3. CH0-H, CH1-H are connected to the PROM in HDA A3 via HDA cable W8.
CHIP0-H thru CHIP3-H	Chip Select, bits 0 thru 3	RW A2	The four most significant bits of the READ/WRITE CONTROLLER address register. Output to the HEAD SELECT ENCODER.
CLER-L	Clear	S1 A1	SERVO CONTROLLER output to FAULT LATCHES and other circuits in the servo system.

Table 5-1. List of Mnemonics (3 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
CLSER-L	Clear Servo Error	S1 A1	SERVO CONTROLLER output to FAULT LATCHES. CLSER-L resets a servo controller error condition.
CURUS-H	Current Unsafe	RW A2	UNSAFE DETECTOR output which informs the READ/WRITE CONTROLLER that an unsafe write condition has been detected in the READ PREAMP/ WRITE DRIVER ICs in the HDA. Recognition of CURUS-H by the READ/WRITE CONTROLLER is limited to a window starting one microsecond after Start of Sector (SOS-L) goes low and continuing until SOS-L goes high at the end of a write sector.
DAGC	Dedicated AGC*	S1 A1	Dedicated servo AGC INTEGRATOR analog voltage output which controls the gain of the DEDICATED SERVO AGC AMPLIFIER. DAGC can be monitored at pin 46 of the servo test point PCA. DAGC is connected to the DEDICATED SERVO AGC AMPLIFIER in read/write PCA-A2. See figure RW.
DAR	DAC Reference	S1 A1	6.25V reference for the DAC in HDA A3. (Part of head gain reference circuit.) DAR is connected to the DAC in HDA A3 via read/write PCA-A2 and HDA cable W8.
DD0 thru DD7	Disc Data, bits 0 thru 7	CR A6 RW A2	Bidirectional 8-bit parallel bus in Disc Data Bus which carries all data read from or written to the media. Data is transferred across the bus by Disc Data Strobe (DDS-H). Transfer takes place during the low state of Start of Sector (SOS-L). Other handshake lines associated with the bus are Disc Data Strobe (DDS-H), Start ECC Field (SEF-L), and Write Hold Off (WHO-L). DD0 thru DD7 are connected between the DMA/ECC in controller PCA-A6 and the READ/WRITE CONTROLLER in read/write PCA-A2 via connectors A6P1 and A2J1.

Table 5-1. List of Mnemonics (4 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
DDS-H	Disc Data Strobe	RW A2	Disc Data Bus handshake line. The rising edge of DDS-H from the READ/WRITE CONTROLLER causes the driver of the bus to output the next data byte, and the falling edge causes the receiver on the bus to latch the data byte. DDS-H is connected to the DMA/ECC circuitry in controller PCA-A6 via connectors A2J1 and A6P1.
DEDP, DEDN	Dedicated Servo	RW A2	DEDICATED SERVO AGC AMPLIFIER differential output. The amplifier input is differential Servo Data (SDX, SDY), from the SERVO READ PREAMP/WRITE DRIVER IC. DEDP and DEDN are connected to the input of the DEDICATED SERVO FILTER in servo PCA-A1. See figure S1.
DID0, DID1	Drive ID bits 0, 1	S1 A3	DRIVE ID outputs to SERVO CONTROLLER. Signals identify the HDA type (7936 or 7937). When requested, the SERVO CONTROLLER reports this information to controller PCA-A6. DID0, DID1 are connected to the SERVO CONTROLLER in servo PCA-A1 via HDA cable W8 and read/write PCA-A2.
DLVL	Dedicated Level*	S1 A1	Dedicated servo POSITION DEMODULATOR output to the AGC INTEGRATOR. DLVL represents the sum of the sampled servo code A and B dibits. DLVL can be monitored at pin 9 of the servo test point PCA.
DMP-H	Dump	S1 A1	DEDICATED SERVO TIMING and PLL output to POSITION DEMODULATOR. DMP-H controls the discharge of the position demodulator sample-and-hold circuit.

Table 5-1. List of Mnemonics (5 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
DPA0-H	Data Path Address Zero	CR A6	Data Path Control Bus handshake line from the DATA PATH CONTROL INTERFACE. Low state selects the READ/WRITE CONTROLLER control or status registers; high state selects the address register. DPA0-H is connected to the READ/WRITE CONTROLLER in read/write PCA-A2 via connectors A6P1 and A2P1.
DPC0 thru DPC7	Data Path Control, bits 0 thru 7	CR A6 RW A2	Bidirectional parallel 8-bit bus in the Data Path Control Bus which carries data path control commands and status information. Signals which control addressing and handshaking are Data Path Read High Write Low (DPRHW-L), Data Path Address Zero (DPA0-H), Data Path Control Select (DPCS-L), and Data Path Interrupt Request (DPIRQ-L). DPC0 thru DPC7 are connected between the DATA PATH CONTROL INTERFACE in controller PCA-A6 and the READ/WRITE CONTROLLER in read/write PCA-A2 via connectors A6P1 and A2J1.
DPCS-L	Data Path Control Select	CR A6	Data Path Control Bus handshake line from DATA PATH CONTROL INTERFACE. During a read, a low state enables the output buffers and a high state tristates the output buffers. During a microprocessor write, data is strobed into the internal registers on the rising edge. DPCS-L is connected to the READ/WRITE CONTROLLER in read/write PCA-A2 via connectors A6P1 and A2J1.

Table 5-1. List of Mnemonics (6 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
DPIRQ-L	Data Path Interrupt Request**	RW A2	READ/WRITE CONTROLLER Data Path Control Bus handshake line to INTERRUPT CONTROLLER in controller PCA-A6. When activated by the READ/WRITE CONTROLLER, DPIRQ-L interrupts the controller on a fault condition. The line is asserted with the rising edge of Start of Sector (SOS-L), at the end of the sector in which a fault is detected. DPIRQ-L can be monitored at pin 6 of the read/write test point PCA. DPIRQ-L is connected to controller PCA-A6 via connectors A2J1 and A6P1.
DPOS	Dedicated Servo Position Error*	S1 A1	Dedicated servo POSITION DEMODULATOR output. DPOS is dedicated servo code A dibits minus dedicated servo code B dibits. DPOS can be monitored at pin 47 of the servo test point PCA.
DPRHW-L	Data Path Read High, Write Low	CR A6	Data Path Control Bus handshake line from the DATA PATH CONTROL INTERFACE. The low state enables address or control registers in the READ/WRITE CONTROLLER to accept data. The high state enables status or address registers to be read. DPRHW-L is connected to the READ/WRITE CONTROLLER in read/write PCA-A2 via connectors A6P1 and A2J1 .
DQAL-L	Decrease Qualification Level**	RW A2	Bit 6 of the READ/WRITE CONTROLLER address register. Signal is used for diagnostic testing only. DQAL-L can be monitored at pin 15 of the read/write test point PCA.

Table 5-1. List of Mnemonics (7 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
DSOS-H, DSOS-L	Differential Start of Sector	S1 A1	SAMPLED SERVO TIMING differential output representing start of sector. Signal becomes single-ended Start of Sector (SOS-L) in read/write PCA-A2. See SOS-L. DSOS-H and DSOS-L are connected to a buffer in read/write PCA-A2. See figure RW.
DSRVN, DSRVP	Dedicated Servo, Positive and Negative	S1 A1	Differential output of DEDICATED SERVO AMPLIFIER. DSRVN is connected to the POSITION DEMODULATOR. DSRVP is connected to the SECTOR MARK DECODER and the DEDICATED SERVO TIMING and PLL.
DSRVPT	Dedicated Servo, Positive, Test*	S1 A1	Measurement point for DSRVP. DSRVPT can be monitored at pin 13 of the servo test point PCA.
DWC-L DWC-H	Differential Write Clock	S1 A1	DEDICATED SERVO TIMING AND PLL differential output to read/write PCA-A2. This signal, which becomes single-ended Write Clock WCLK-L in PCA-A2, is the write clock used by the read/write controller. DWC-L and DWC-H are connected to a buffer in read/write PCA-A2. See figure RW.
DX, DY	Read/Write Data	RW A2 RW A3	During a read, DX, DY, is the differential read data signal sent by the preamplifier section of the READ PREAMP/WRITE DRIVER ICs to the read chain and sampled servo circuitry in read/write PCA-A2. During a write, DX, DY, is the differential write data signal sent by the WRITE CHAIN to the write driver section of the READ PREAMP/WRITE DRIVER ICs in HDA A3. DX and DY are connected between read/write PCA-A2 and head-disc assembly HDA A3 via HDA cable W8.

Table 5-1. List of Mnemonics (8 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
FSEN-L	Fine Servo Enable*	S1 A1	SERVO CONTROLLER output to the POSITION LOOP SERVO switch. SEEK CURRENT COMMAND GENERATOR, and OVERVELOCITY DETECTOR. See figure S2 . FSEN-L changes the servo system from a dedicated (seek) to a sampled (track follow) mode of operation. FSEN-L can be monitored at pin 44 of the servo test point PCA.
GAP-L	Gap*	S1 A1	SAMPLED SERVO TIMING output to AGC REF DEMOD SWITCH. GAP-L is gated with SOSEN-H to create DSOS-L, DSOS-H. GAP-L is the complete window for the sampled servo code. GAP-L can be monitored at pin 26 of the servo test point PCA.
GBD-H	Guard Band Detect	S1 A1	DEDICATED SERVO TIMING output to SERVO CONTROLLER. GBD-H is activated when the guard band mark is detected by the sector mark decoder. The signal is used during calibration to indicate when the heads are on the guard band.
GBDEN-H	Guard Band Enable*	S1 A1	SERVO CONTROLLER output to DEDICATED SERVO TIMING and PLL. GBDEN-H determines whether the sector mark decoder will search for sector marks or guard band marks. GBDEN-H can be monitored at pin 42 of the servo test point PCA.
GDCLK	Good Clock	S1 A1	Output from SAMPLED SERVO TIMING to MISSING PWM CLOCK DETECTOR. GDCLK is a reference used to ensure that the 100-kHz clock in the servo power amplifier is present. (The absence of the clock will signal a servo fault).

Table 5-1. List of Mnemonics (9 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
GLED	Green LED	CR A6	LED DRIVER output to green LED in front panel LED display. GLED is connected to LED PCA-A7 via read/write PCA-A2, power distribution PCA-A5, and power supply output cable W4.
HD1S-H, HD2S-H	Head Select 1, 2	RW A2	Two least significant bits of head address from the address register in the READ/WRITE CONTROLLER. Output to the HEAD SELECT ENCODER and the HEAD GAIN REFERENCE PROM in HDA-A3. HDS1-H and HDS2-H are connected to the PROM in HDA A3 via HDA cable W8.
HS1-H, HS2-H	Head Select, bits 1,2	RW A2	HEAD SELECT ENCODER outputs which, together with Chip Enable bits CE0-L through CE3-L, are decoded by the READ PREAMP/WRITE DRIVER ICs to select the desired read/write head. HS1-H and HS2-H are connected to the READ PREAMP/WRITE DRIVER ICs in HDA A3 via HDA cable W8.
INDEX-H	Index*	S1 A1	SAMPLED SERVO TIMING output to controller PCA-A6. INDEX-H represents one rotation of the spindle. INDEX-H can be monitored at pin 48 of the servo test point PCA. INDEX-H is connected to controller PCA-A6 via read/write PCA-A2.
LCK-L	Lock	S1 A1	SERVO CONTROLLER output to DEDICATED SERVO TIMING and PLL. LCK-L facilitates lock-up of the dedicated servo PLL.

Table 5-1. List of Mnemonics (10 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
LEDP	LED Power	PS A2	+5V power for three LEDs in front panel LED display. LEDP is connected to LED PCA-A7 via signal jumper cable W7, power distribution PCA-A5, and power supply output cable W4.
LSB-H	Least Significant Bit	S1 A1	SERVO CONTROLLER output to DEDICATED SERVO TIMING and PLL. LSB-H is used by the servo system to indicate when the heads are over odd or even tracks.
MOTOR+, MOTOR-	Actuator Drive +,-	S2 A1	Servo power amplifier OUTPUT FILTER lines which supply drive current to the actuator voice coil. MOTOR+ and MOTOR- are connected to the ACTUATOR in HDA A3 via read/write PCA-A2 and HDA cable W8.
NACC-L	Negative Acceleration	S1 A1	SERVO CONTROLLER output to SEEK CURRENT COMMAND GENERATOR. See figure S2 . NACC-L causes the servo power amplifier to drive the actuator with -2.90 amperes.
NO CLK-H	No 100-kHz Clock	S2 A1	Output from MISSING PWM CLOCK DETECTOR. NO CLK-H signals to the amplifier CONTROL AND FAULT INDICATION circuit that the 100-kHz oscillator in the PULSE WIDTH MODULATOR has failed.
NRZ-H	NRZ Data	RW A2	ZERO-CROSSING DETECTOR output to read chain PLL and DATA SEPARATOR. NRZ-H goes high each time a flux reversal occurs in the data path.
OFTU-L	Offtrack Unlatched*	S1 A1	OFFTRACK DETECTOR output to FAULT LATCHES and SLEW RATE LIMIT SWITCH. OFTU-L is a pulse that indicates the start of an offtrack condition. OFTU-L can be monitored at pin 45 of the servo test point PCA.

Table 5-1. List of Mnemonics (11 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
OFTRK-H	Offtrack Latched	S1 A1	FAULT LATCHES output to SERVO CONTROLLER. OFTRK-H denotes an off-track condition, which occurs during a normal seek. The signal is a fault when on-track condition is desired.
OVER VEL-L	Over Velocity	S2 A1	Output from OVERVELOCITY DETECTOR. OVER VEL-L signals to the amplifier CONTROL AND FAULT INDICATION circuit that the actuator is moving too fast.
PACC-L	Positive Acceleration	S1 A1	SERVO CONTROLLER output to SEEK CURRENT COMMAND GENERATOR. See figure S2 . PACC-L causes the servo power amplifier to drive the actuator with +2.90 amperes.
PAREN-H	Parity Error Enable	RW A2	READ/WRITE CONTROLLER output which enables the PARITY ERROR DETECTOR in the read chain.
PARER	Parity Error	RW A2	PARITY DETECTOR output which informs the READ/WRITE CONTROLLER that a parity error has been detected.
PES	Position Error*	S1 A1	SAMPLED/DEDICATED SELECT SW output. PES is either the dedicated or sampled position signal, depending on whether the servo system is presently in the dedicated (seek) or sampled (track follow) mode of operation. PES can be monitored at pin 21 of the servo test point PCA.

Table 5-1. List of Mnemonics (12 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
PF-L	Power Fail	PS A4	POWER FAIL/RESET output which goes low 2 milliseconds before any output voltage from the power supply drops out of regulation. The timing is valid only when primary power to the supply is removed. If an output voltage from the power supply loses regulation because of a load fault or a component failure, PF-L will go low an unspecified time later. PF-L goes high 1 millisecond before Power On Reset POR-L. PF-L is connected to controller PCA-A6 via power supply output cable W4, power distribution PCA-A5, and read/write PCA-A2.
POR-L	Power On Reset	PS A4	POWER FAIL/RESET output used to reset circuits in the drive at power on. POR-L goes high a minimum of 100 milliseconds after all output voltages from the power supply are in regulation, following application of primary power to the power supply. During operation of the drive, POR-L will go low when any output voltage from the power supply loses regulation. POR-L is connected to PCAs A1, A2, and A6 via power supply output cable W4 and power distribution PCA-A5.
PWM-L	Pulse Width Modulation*	S2 A1	PULSE WIDTH MODULATOR 100-kHz pulse-width-modulated square wave output. Used in servo power amplifier. PWM-L can be monitored at pin 12 of the servo test point PCA.
QEN-H	Transistor Enable	S2 A1	AMPLIFIER CONTROL AND FAULT INDICATION output to TRANSISTOR DRIVERS and ACTUATOR CROWBAR. QEN-H shuts down servo power amplifier operation when a servo fault is detected.
QUAD-H	Quadrature	S1 A1	SERVO CONTROLLER output to DEDICATED SERVO TIMING AND PLL. QUAD-H causes the dedicated position demodulator to process quad dibits.

Table 5-1. List of Mnemonics (13 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
RAGC-H, RAGC-L	Read AGC Gate	S1 A1	SAMPLED SERVO TIMING differential output which defines the time that the read chain AGC CIRCUIT is active. RAGCC-H and RAGCC-L are connected to the read chain AGC Circuit in read/write PCA-A1. See figure RW.
RDATA	Read Data	RW A2	NRZ data from the read chain PLL and DATA SEPARATOR. The data is clocked on the positive-going edge of Read Clock (RDCLK-H) into the encoder/decoder section of the READ/WRITE CONTROLLER.
RDCLK-H	Read Clock	RW A2	Read data clock from the read chain PLL and DATA SEPARTOR. RDCLK-H is input to the encoder/decoder section of the READ/WRITE CONTROLLER.
RDEN-H	Read Enable**	RW A2	An output from the encoder/decoder section of the READ/WRITE CONTROLLER to the PLL and DATA SEPARATOR. RDEN-H changes the PLL from a frequency mode to a phase mode when a read begins. RDEN-H can be monitored at pin 11 of the read/write test point PCA.
REF-L	Reference	S1 A1	DEDICATED SERVO TIMING and PLL output to POSITION DEMODULATOR. REF-L is a reference level which gates the positive dedicated servo pulse level of acceptance. Used in the creation of write clock.
RLED	Red LED	CR A6	LED DRIVER output to red LED in front panel LED display. GLED is connected to LED PCA-A7 via read/write PCA-A2, power distribution PCA-A5, and power supply output cable W4.

Table 5-1. List of Mnemonics (14 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
SAGC	Sampled AGC*	S1 A1	Sampled servo AGC INTEGRATOR analog voltage output which controls the gain of the SAMPLED SERVO AGC AMPLIFIER. SAGC can be monitored at pin 43 of the servo test point PCA. SAGC is connected to the SAMPLED SERVO AGC AMPLIFIER in read/write PCA-A2. See figure R4.
SBF-L	Servo Buffer Full	CR A6	Servo Control Bus handshake line from the SERVO CONTROL INTERFACE. When active, SBF-L indicates that controller PCA-A6 cannot accept any more status bytes from the SERVO CONTROLLER. SBF-L is connected to the SERVO CONTROLLER in servo PCA-A1 via read/write PCA-A2.
SCAP-L	Start Capacitor	SD A1	SERVO CONTROLLER output to spindle system. SCAP-L controls a relay which connects a start capacitor in parallel with the spindle motor run capacitor at power on. SCAP-L is connected to the start relay via read/write PCA-A2, power distribution PCA-A5, and power supply output cable W4.
SDAV-L	Servo Data Available	CR A6	Servo Control Bus handshake line from the SERVO CONTROL INTERFACE. When active, SDAV-L indicates that controller PCA-A6 has a command byte ready for the SERVO CONTROLLER. SDAV-L is connected to the SERVO CONTROLLER in servo PCA-A1 via read/write PCA-A2.

Table 5-1. List of Mnemonics (15 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
SDMP-H	Sampled Dump	S1 A1	SAMPLED SERVO TIMING output to POSITION DEMODULATOR. SDMP-H controls the discharge of the position demodulator sample-and-hold circuits.
SDX, SDY	Servo Data	RW A3	Differential output from the preamplifier section of the SERVO READ PREAMP/WRITE DRIVER IC. SDX and SDY are connected to the DEDICATED SERVO AMPLIFIER in read/write PCA-A2 via HDA cable W8.
SD0 thru SD7	Servo Data, bits 0 thru 7	CR A6 S1 A1	Bidirectional parallel 8-bit bus in Servo Control Bus which carries commands and status information between the SERVO CONTROL INTERFACE in controller PCA-A6 and the SERVO CONTROLLER in PCA-A1. All command and status messages are two bytes in length, so it requires two operations to complete a message. These transfer operations are fully handshaked by four lines associated with the bus. These lines are Servo Read (SRD-L), Servo Write (SWR-L), Servo Data Available (SDAV-L), and Servo Buffer Full (SBF-L). SD0 thru SD7 are connected between controller PCA-A6 and servo PCA-A1 via read/write PCA-A2.
SEF-L	Start ECC Field	RW A2	READ/WRITE CONTROLLER Disc Data Bus handshake line. SEF-L goes low during the 264th data byte of a transfer. During a read operation, 12 more bytes are sent to the controller. During a write operation, 14 more DDS-H clocks occur. The first two clocks after the falling edge of SEF-L are ignored by the data path control system, and only the last 12 bytes are written to the disc. This allows the controller to switch data paths from the data source driving the bus to the ECC generator driving the bus. SEF-L is connected from the READ/WRITE CONTROLLER to the DMA/ECC in controller PCA-A6 via connectors A2J1 and A6P1.

Table 5-1. List of Mnemonics (16 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
SGR	Servo Gain Reference	RW A3	Analog current from the HDA DAC which represents the gain of the heads installed in the drive. Included in the determination of DAGC and SAGC. SGR is connected to the AGC REF DEMOD SWITCH in servo PCA-A1 via HDA cable W8 and read/write PCA-A2.
SHS-H	Servo Head Select	RW A2	WRITE CHAIN output to SERVO READ PREAMP/WRITE DRIVER IC. SHS-H is set high to write the dedicated servo code; thereafter is always low. SHS-H is connected to the SERVO READ PREAMP/WRITE DRIVER IC in HDA A3 via HDA cable W8.
SLPES	Slew Position Error*	S1 A1	Output from SLEW RATE LIMIT switch to POSITION LOOP COMPENSATION block. See S2. The switch is controlled by OFTU-L. SLPES can be monitored at pin 17 of the servo test point PCA.
SLVL	Sampled Level*	S1 A1	Sampled servo POSITION DEMODULATOR output to the AGC INTEGRATOR. SLVL represents the addition of the sampled servo code odd and even dibits. SLVL can be monitored at pin 25 of the servo test point PCA.
SMCLK	Sector Mark Clock	S1 A1	DEDICATED SERVO TIMING and PLL output to SECTOR MARK DECODER. SMCLK clocks Sector Mark Detect (SMDT-H) out of the SECTOR MARK DECODER.
SMDT-H	Sector Mark Detect*	S1 A1	SERVO MARK DECODER output to DEDICATED SERVO TIMING and PLL. SMDT-H is asserted when the sector mark decoder detects a sector mark on the dedicated servo. SMDT-H can be monitored at pin 14 of the servo test point PCA.

Table 5-1. List of Mnemonics (17 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
SMPN, SMPP	Sampled Servo, Negative, Positive	RW A2	SAMPLED SERVO AGC AMPLIFIER differential output. The amplifier input is Read/Write Data signal DX, DY, gated by the SAMPLED SERVO SWITCH to allow only the sampled servo information prerecorded between data sectors to reach the amplifier. SMPN and SMPP are connected to the input of the SAMPLED SERVO FILTER in servo PCA-A1.
SOS-L	Start of Sector**	RW A2	BUFFER output to READ/WRITE CONTROLLER. SOS-L, derived from servo system DSOS-L, DSOS-H, goes high for the duration of the sampled servo field. The falling and rising edges of the signal determine the beginning and end of the writeable data field. The signal is used in the write chain as a Disc Data Bus handshake line. The controller uses SOS-L to initiate a data transfer across the bus. Since SOS-L is generated, not only for sectors which will be transferred, but for all sectors, the controller also uses SOS-L to count sectors and keep track of rotational position. SOS-L can be monitored at pin 13 of the read/write test point PCA. SOS-L is connected to the READ/WRITE CONTROLLER in read/write PCA-A2 and the DMA/ECC in controller PCA-A6.
SOSEN-H	Start of Sector Enable	S1 A1	SERVO CONTROLLER output to SAMPLED SERVO TIMING. SOSEN-H controls the generation of Start of Sector SOS-L.
SPDSNS-L	Speed Sense	SD A3	Speed sensor output to SERVO CONTROLLER. SPDSNS is used at power on to determine when the spindle is rotating fast enough to allow the heads to be moved away from the landing zone. SPDSNS is connected to the SERVO CONTROLLER in servo PCA-A1 via power power distribution PCA-A5 and read/write PCA-A1.

Table 5-1. List of Mnemonics (18 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
SPOS	Sampled Servo Position Error*	S1 A1	Sampled servo POSITION DEMODULATOR output to SAMPLED/DEDICATED SELECT SW. SPOS represents odd sampled servo code dibits minus even sampled servo code dibits. Signal is used for track following. SPOS can be monitored at pin 37 of the servo test point PCA.
SPR-L	Servo Processor Reset	CR A6	Servo Control Bus signal from controller PCA-A6 which resets the servo system. SPR-L is connected to the SERVO CONTROLLER and the SERVO POWER AMPLIFIER in servo PCA-A1 via read/write PCA-A2.
SRD-L	Servo Read	S1 A1	SERVO CONTROLLER Servo Control Bus handshake line to SERVO CONTROL INTERFACE in controller PCA-A6. When active, SRD-L enables controller PCA-A6 to drive the bus with a byte of command information. SRD-L is connected to controller PCA-A6 via read/write PCA-A2.
SRTF-H	Servo Timing Fault*	S1 A1	FAULT LATCHES output to SERVO CONTROLLER. SRFT-H is a combination of Timing Errors TERR1 and TERR2. SRTF-H can be monitored at pin 49 of the servo test point PCA.
SRVER-L	Servo Error*	S1 A1	FAULT LATCHES output to read/write controller. SRVER-L is a combination of off-track or timing errors. SRVER-L can be monitored at pin 29 of the servo test point PCA. SRVER-L is connected to the READ/WRITE CONTROLLER in read/write PCA-A1. See figure RW.

Table 5-1. List of Mnemonics (19 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
SSDEMOD-H	Sampled Servo Demodulation*	S1 A1	SAMPLED SERVO TIMING output to POSITION DEMODULATOR. SSDEMOD-H gates the demodulation of the A versus B dibits in the sampled servo circuit. SSDEMOD-H can be monitored at pin 2 of the servo test point PCA.
SSEN-H, SSEN-L	Sampled Servo Enable	S1 A1	SAMPLED SERVO TIMING differential output which controls the operation of the SAMPLED SERVO SWITCH. This switch allows only the sampled servo information prerecorded between data sectors to reach the SAMPLED SERVO AMPLIFIER. See SMPN, SMPP. SSEN-L and SSEN-H are connected to the SAMPLED SERVO SWITCH in read/write PCA-A2. See figure RW.
SSGT-L	Sampled Servo Gate*	S1 A1	SAMPLED SERVO TIMING output to POSITION DEMODULATOR and SERVO CONTROLLER. SSGT-L is a window of the sampled servo code dibits. SSGT-L can be monitored at pin 34 of the servo test point PCA.
SSRVN, SSRVP	Sampled Servo, Negative, Positive	S1 A1	Differential output from SAMPLED SERVO AMPLIFIER. SSRVN is connected to the POSITION DEMODULATOR and SSRVP is connected to the SAMPLED SERVO TIMING circuit.
SSRVPT	Sampled Servo, Positive, Test*	S1 A1	Measurement point for SSRVP. SSRVPT can be monitored at pin 1 of the servo test point PCA.
SSSL-L	Sampled Servo Select	S1 A1	SERVO CONTROLLER output to SAMPLED/DEDICATED SELECT switch and the SAMPLED SERVO TIMING. SSSL-L controls the selection of the sampled or dedicated servo error signal (SPOS or DPOS.)

Table 5-1. List of Mnemonics (20 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
SWC	Servo Write Current	RW A2	WRITE CHAIN output which sends current to the SERVO READ PREAMP/ WRITE DRIVER IC when dedicated servo code is written on the dedicated servo surface. (Factory use only.) SWC is connected to the SERVO READ PREAMP/WRITE DRIVER IC in HDA A3 via HDA cable W8.
SWR-L	Servo Write	S1 A1	SERVO CONTROLLER Servo Control Bus handshake line to SERVO CONTROL INTERFACE in controller PCA-A6. When active, SWR-L indicates that the SERVO CONTROLLER is driving the bus with a byte of status information. SWR-L is connected to controller PCA-A6 via read/write PVA-A2.
SWON-L	Switch On	S2 A1	AMPLIFIER CONTROL and FAULT INDICATION output. SWON-L controls the input signals to the servo power amplifier input stages.
SWS	Servo Write Select	RW A2	WRITE CHAIN output which selects the operating mode of the SERVO PREAMP/WRITE DRIVER IC. SWS is low when read is selected, and approx. 3.5V when write is selected. (Write mode is only used when the dedicated servo code is written at the factory.) SWS is connected to the SERVO READ PREAMP/WRITE DRIVER IC in HDA A3 via HDA cable W8.
TERR1-L	Timing Error 1*	S1 A1	DEDICATED SERVO TIMING and PLL output to FAULT LATCHES. TERR1-L represents an overall timing error caused by Start of Sector gap not occurring at the proper time relative to SMDT-H. TERR1-L can be monitored at pin 5 of the servo test point PCA.

Table 5-1. List of Mnemonics (21 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
TERR2-L	Timing Error 2*	S1 A1	DEDICATED SERVO TIMING AND PLL output to FAULT LATCHES. TERR2-L is the output of a circuit that monitors the sync bit to make sure that it falls within a specified window and is followed by a specified gap. TERR2-L can be monitored at pin 35 of the servo test point PCA.
TRKCR-H	Track Crossing*	S1 A1	TRACK CROSSING DETECTOR output to SERVO CONTROLLER. TRKCR-H goes high when a dedicated servo code track is crossed. TRKCR-H can be monitored at pin 50 of the servo test point PCA.
UNDER VLT-L	Under Voltage	S2 A1	Output from UNDERVOLTAGE DETECTOR. UNDER VLT-L signals to the servo power amplifier CONTROL AND FAULT INDICATION circuit that a failure has occurred in either the +45V or -45V supply to the amplifier.
US	Unsafe	RW A3	READ PREAMP/WRITE DRIVER IC output line in which current flows whenever writing is enabled and there is an absence of write current or data transitions. Possible causes include: • One or both sides of selected head open • One or both sides of selected head shorted • Insufficient write current to heads • Failure to select write mode. US is connected to the UNSAFE DETECTOR in read/write PCA-A2 via HDA cable W8.
WC	Write Current	RW A2	WRITE CHAIN output line which sends current to the READ PREAMP/WRITE DRIVER ICs during a write. WC is connected to the READ PREAMP/WRITE DRIVER ICs in HDA A3 via HDA cable W8.

Table 5-1. List of Mnemonics (22 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
WC-H	Write Clock	S1 A1	DEDICATED SERVO TIMING output to SAMPLED SERVO TIMING circuit. WC-H serves as the timing signal for the SAMPLED SERVO TIMING logic.
WCLK-H	Write Clock	RW A2	BUFFER output to WRITE CHAIN. WCLK-H is the single-ended version of differential Write Clock DWC-L, DWC-H.
WCS0, WCS1	Write Current Select 0,1	RW A2	Address lines for HEAD GAIN REFERENCE PROM in HDA A3. WCS0, WCS1 are connected to the PROM in HDA A3 via HDA cable W8.
WDATA-H	Write Data**	RW A2	A READ/WRITE CONTROLLER output. Signal is VLFM-encoded data in NRZ form, clocked by the write clock supplied by the servo system. A negative transition of WDATA-H maps to a transition on the magnetic media. WDATA-H can be monitored at pin 12 of the read/write test point PCA.
WGTO-L	Write Gate Open**	RW A2	READ/WRITE CONTROLLER output to WRITE CHAIN. WGTO-L is clocked true (low) by the the falling edge of Start of Sector SOS-L when a write command has previously been entered into the READ/WRITE CONTROLLER command register. When WGTO-L is low, write current is supplied to the write drivers in HDA A3 and write current in the head is toggled each time a positive edge is seen at Write Data WDATA-H. WGTO-L is normally deactivated by the positive-going edge of SOS-L. However, it can also be deactivated by the detection of a fault condition by the READ/WRITE CONTROLLER. WGTO-L can be monitored at pin 10 of the read/write test point PCA.

Table 5-1. List of Mnemonics (23 of 23)

MNEMONIC	SIGNAL	SOURCE	DESCRIPTION
WHO-L	Write Hold Off	CR A6	Disc Data Bus handshake signal from DMA. If WHO-L goes low before the falling edge of Start of Sector SOS-L, it will cause the read/write system to abort any data transfer which may have been set in its command register. This signal allows the controller a "last chance" to abort a write to the disc, in case of some failure such as a buffer under-run, or verify failure. WHO-L is connected to the READ/WRITE CONTROLLER in read/write PCA-A2 via connectors A6P1 and A2J1.
WSA, WSB	Write Select A, B	RW A2	WRITE CHAIN outputs which select the operating mode of the READ PREAMP/WRITE DRIVER ICs in HDA A3. Signals are low when read is selected, and approx. 3.5V when write is selected. WSA and WSB are connected to the READ PREAMP/WRITE DRIVER ICs in HDA A3 via HDA cable W8.
YLED	Yellow LED	CR A6	LED DRIVER output to yellow LED in front panel LED display. YLED is connected to LED PCA-A7 via read/write PCA-A2, power distribution PCA-A5, and power supply output cable W4.
ZCLK	Zero Clock	S1 A1	DEDICATED SERVO TIMING and PLL output to SECTOR MARK DECODER. ZCLK serves as the sample clock for the SECTOR MARK DECODER zero detector. The frequency of this signal is determined by whether the decoder is searching for sector marks or guard band marks.
ZDT	Zero Detect*	S1 A1	ZDT changes state for each missing dibit so sector marks or guard band marks can be decoded. ZDT can be monitored at pin 16 of the servo test point PCA.

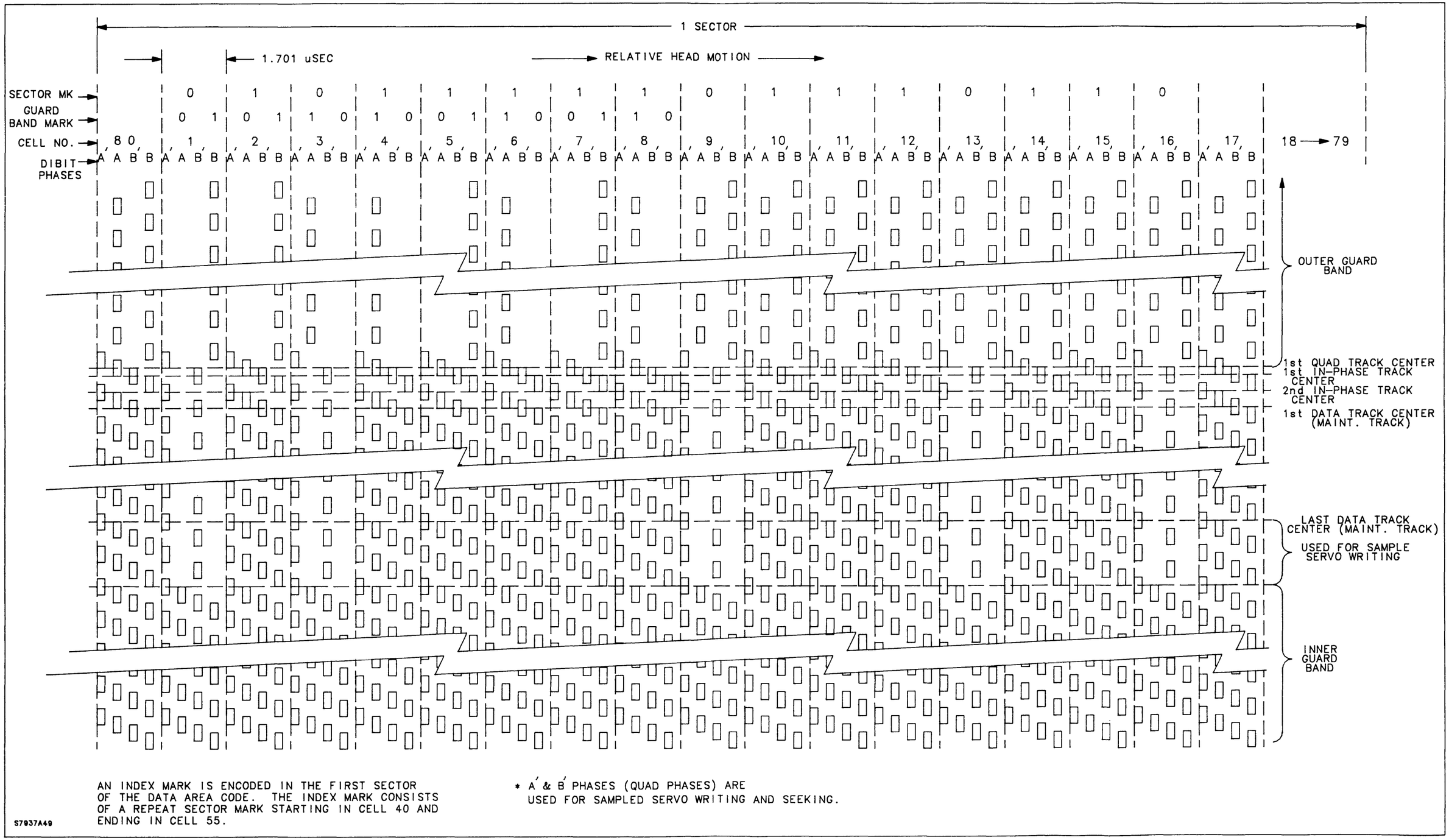


Figure 5-12. Dedicated Servo Code

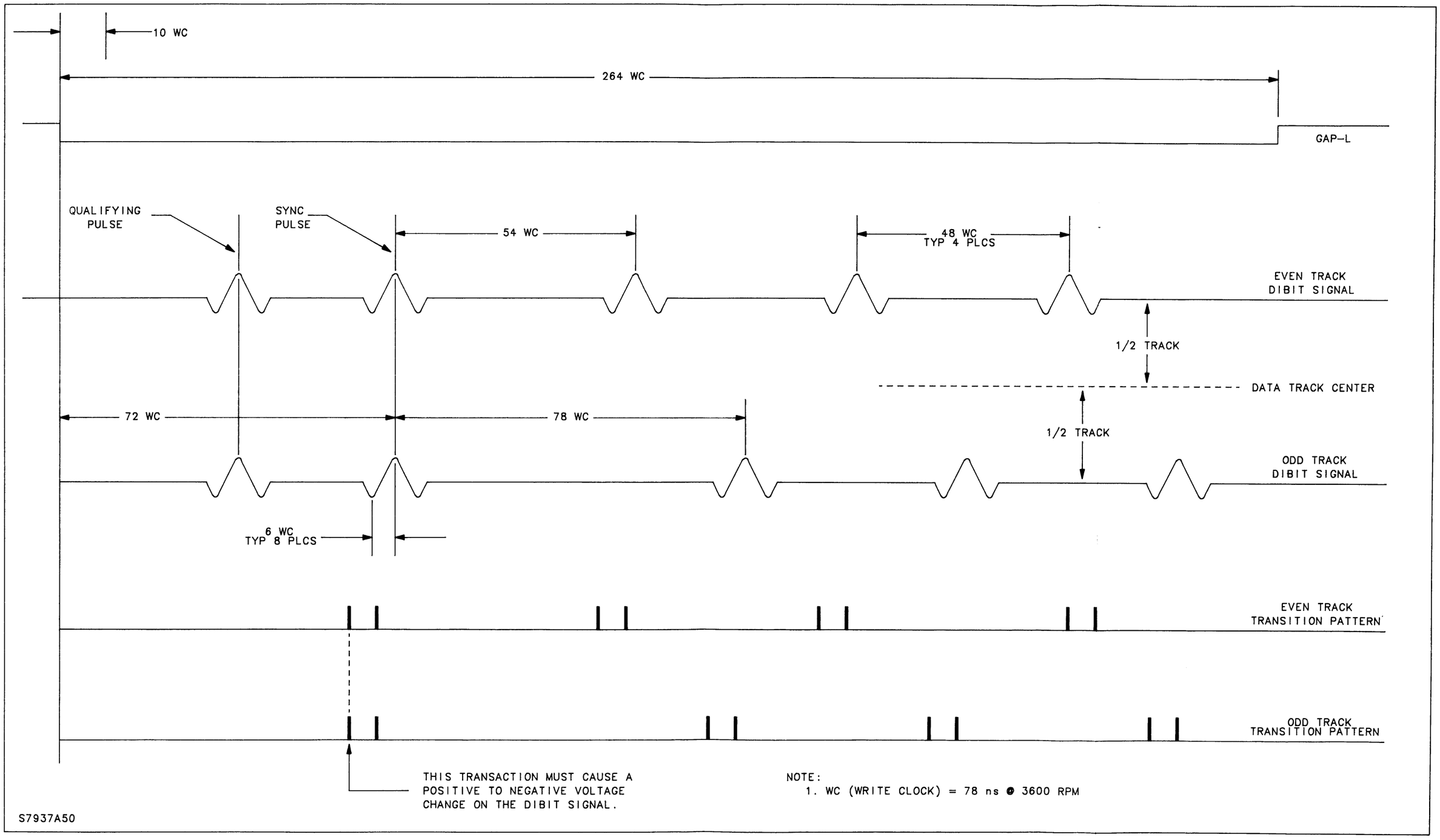


Figure 5-13. Sampled Servo Code

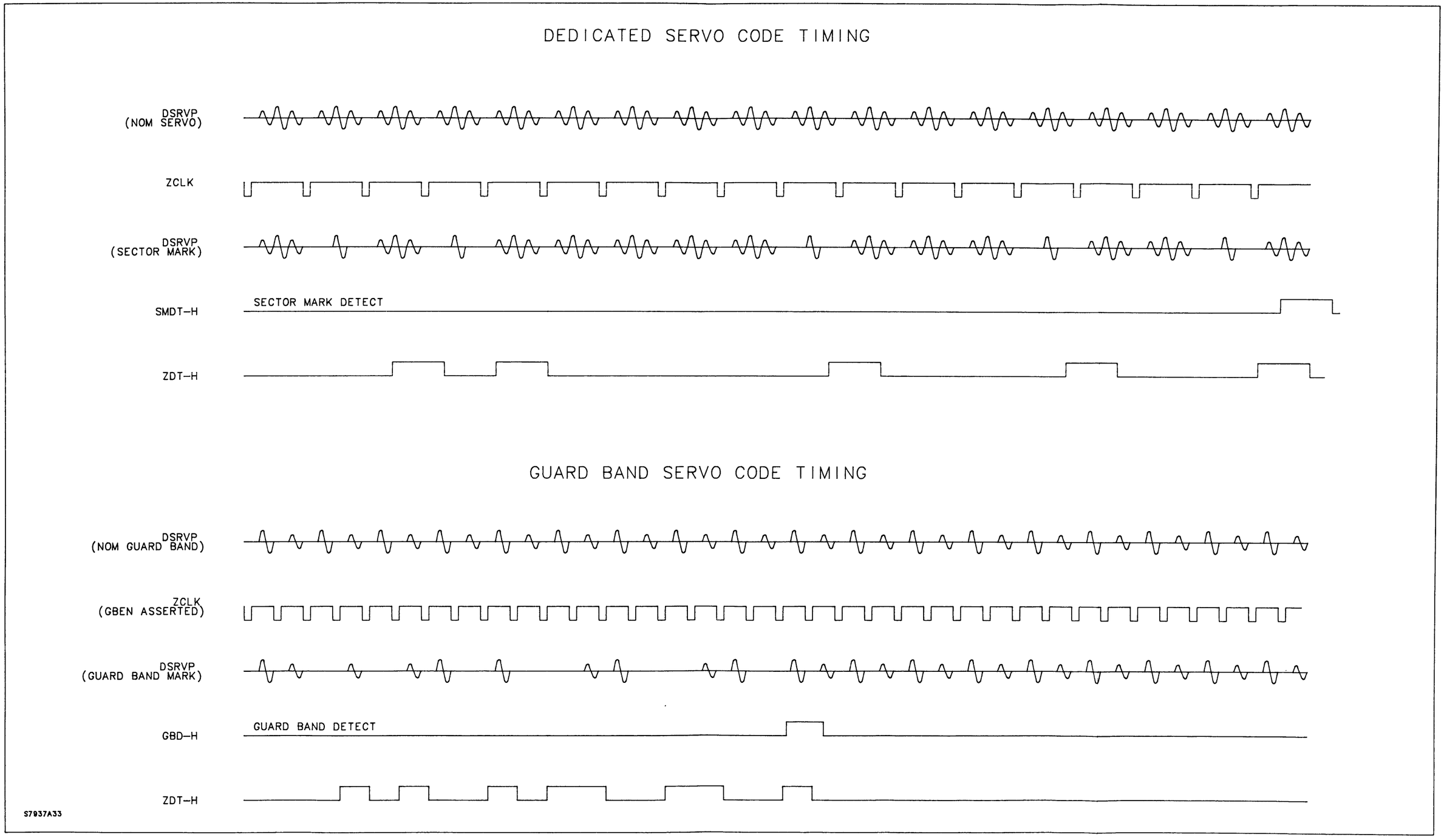


Figure 5-14. Dedicated Servo Circuit Timing

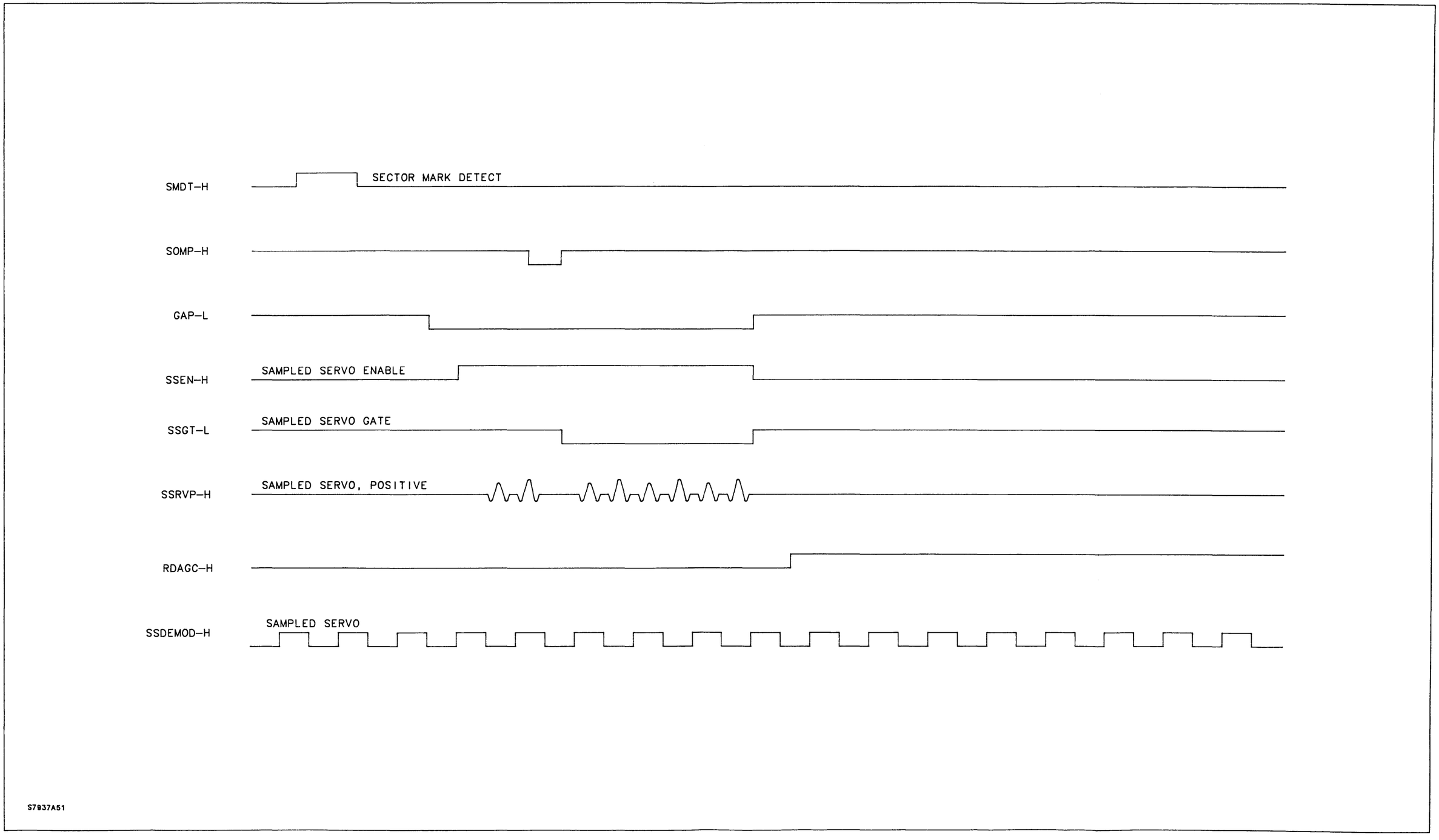


Figure 5-15. Sampled Servo Circuit Timing

HP 7937 DISC DRIVE

CONTROLLER PCA–A6

ECC

HOST

HOST INTERFACE

DMA

DATA

MICRO–PROCESSOR

ROM, RAM MEMORY

PERIPHERAL INTERFACE

ADDRESS

DATA BUFFER

CHANNEL ADDRESS/ DIAGNOSTIC SWITCHES

DISC DATA BUS

DATA PATH CONTROL BUS

SERVO CONTROL BUS

STANDARD INTERFACE (ESI)

DISC DATA BUS

DATA PATH CONTRO

SERVO CONTROL BUS

LED DISPLAY

LED PCA–A7

SERVO PCA–A1

SERVO CONTROLLER

PLL AND SERVO TIMING

SAMPLED SERVO CKT

SAMPLED POSITION ERROR

SERVO POWER AMP

POSITION ERROR SWITCH

DEDICATED SERVO CKT

DEDICATED POSITION ERROR

ACTUATOR DRIVE

PRIMARY POWER PCA–A8

AC INPUT

POWER SWITCH

MOTOR–BRAKE POWER CONFIG. CKTS

DC (BRAKE)

AC (MOTOR)

POWER SUPPLY PCA–A4

DC POWER SUPPLIES

POWER–ON RESET AND POWER FAIL CKTS

POWER DISTRIBUTION PCA–A5

±45V, ±12V, +5V, –5.2V

POWER–ON RESET

POWER FAIL

TO ALL CIRCUITS

S7937A22

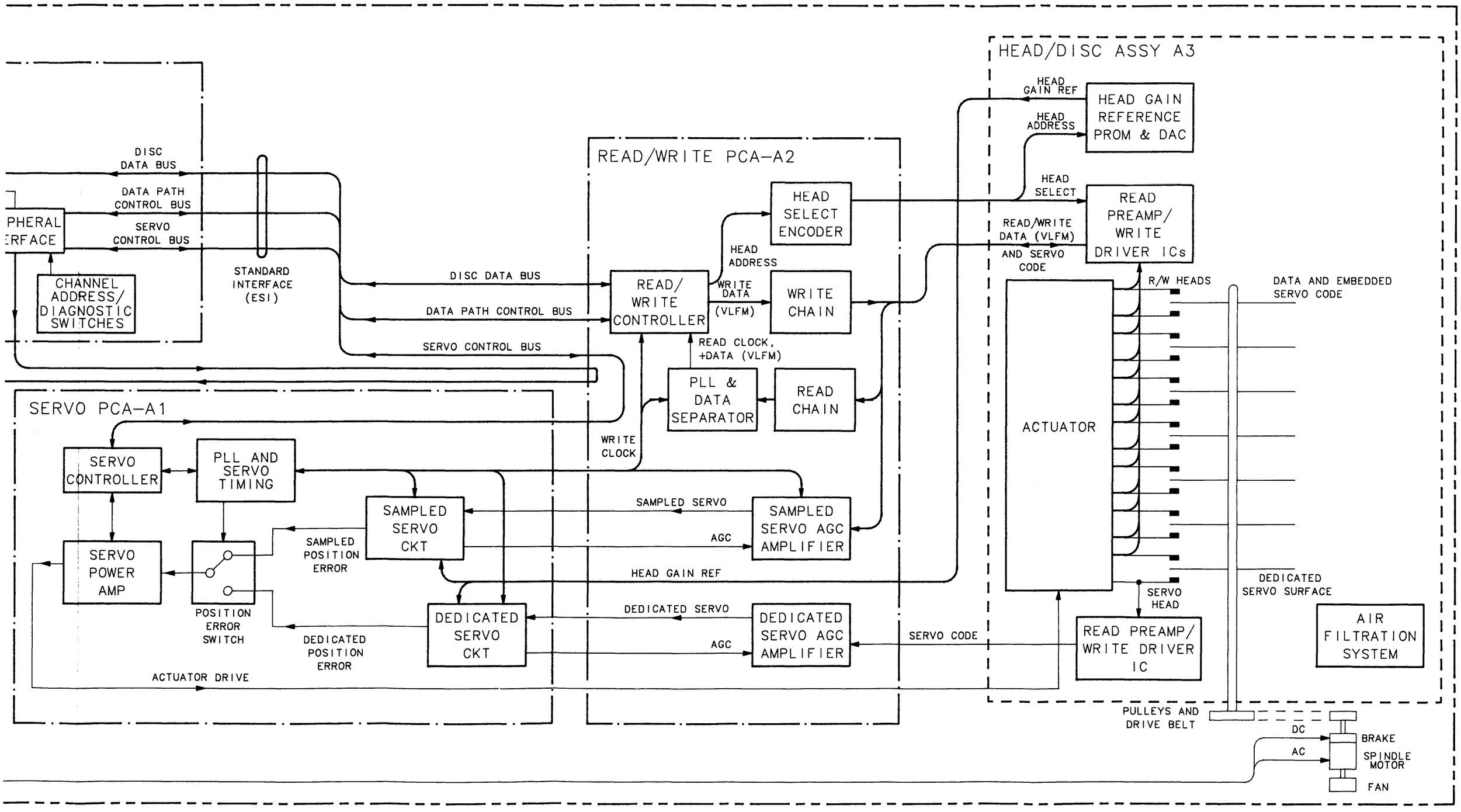


Figure 5-16. Disc Drive Basic Block Diagram

Removal And Replacement 6

6-1. INTRODUCTION

WARNING

The drive does not contain operator-serviceable parts. To prevent electrical shock, refer all maintenance activities to service-trained personnel.

WARNING

The anti-tip feet on the HP 19511A cabinet must be extended before the drive is pulled out of the cabinet on its rack slides. Similar anti-tip devices must be in place on a rack cabinet.

CAUTION

Set the rear panel Shipping Latch to the ■ (Ship) position immediately after the drive has been powered down for service. Refer to chapter 3 for details.

Electrostatic-sensitive devices within the drive require special care if damage is to be avoided. Take appropriate precautions when removing components from the drive. Ground the drive and use a grounding wrist strap. When components are removed from the drive, they should be stored in anti-static, conductive plastic bags.

Do not turn ac power to the drive on or off when the system is in an active state.

Do not connect or disconnect the HP-IB cable when the system is in an active state.

This chapter contains removal and replacement procedures for field replaceable assemblies and parts in the drive. Also provided are a list of tools required, illustrations available, and instructions on how to prepare the drive for service.

The removal and replacement procedures are given in the order in which disassembly normally occurs. Thus, each assembly or part needed to be removed before access to another assembly or part, is listed first, followed by the next assembly or part that can be removed. Unless otherwise stated, all procedures assume that the drive is extended out of the cabinet on its rack slides.

6-2. TOOLS REQUIRED

Standard hand tools only are required for removal and replacement of assemblies and parts in the drive and cabinet. The following hand tools are required:

- TORX® driver, with T9, T10, and T15 bits
- flat-blade screwdriver, 3/16 by 9 in.
- 1/2-in. nut driver

NOTE

TORX® hardware is used extensively in the drive and cabinet. Removal and installation of this hardware requires the use of TORX® drivers. Any reference to this type of hardware will be accompanied by the appropriate driver size, for example T15.

TORX® is a registered trademark of the Camcar Division of Textron, Inc.

6-3. ILLUSTRATIONS

The following illustrations facilitate identification of the field replaceable assemblies and parts in the drive and cabinet:

- Figure 12-4. A drawing which shows the location of the principal assemblies and components in the drive.
- Figure 9-1. An exploded view of the drive which shows the location of all field replaceable assemblies, parts, and attaching parts. The index numbers assigned to the components follow the order of disassembly outlined in the removal and replacement procedures. Refer to table 9-1 for a description of the items shown in figure 9-1.
- Figure 9-2. An exploded view of the HP 19511A Cabinet which shows the location of all field replaceable parts. Refer to table 9-2 for a description of the parts shown in figure 9-2.

6-4. DRIVE PREPARATION FOR SERVICE

Before starting any drive removal or replacement procedure, perform the following steps:

a. Set the drive LINE~ switch to the 0 (out) position.

b. Disconnect the drive power cord from the ac power source.

c. Set the drive Shipping Latch to the ■ (Ship) position. Refer to chapter 3 for details.

d. Disconnect the HP-IB cable from the drive interface connector.

6-5. DRIVE REMOVAL AND REPLACEMENT PROCEDURES

Removal and replacement procedures for field replaceable assemblies and parts in the drive are provided in the following paragraphs. Unless otherwise specified, replacement is a reversal of the removal procedure.

NOTE

The parenthetically enclosed numbers in the removal and replacement procedures refer to the index numbers used in figure 9-1.

6-6. REAR COVER

To remove the rear cover (1, figure 9-1), proceed as follows:

a. Perform the drive preparation for service procedure outlined in paragraph 6-4.

b. Remove the four T15 screws (2) which secure the rear cover (1) to the drive.

c. Remove the rear cover (1) from the drive.

Reinstallation is a reversal of the removal procedure.

NOTE

The rear cover must be in place and all four of its attaching screws tight, in order for the drive to meet its electromagnetic compatibility and data reliability standards.

6-7. HP-IB ASSEMBLY

To remove the HP-IB assembly (3, figure 9-1), proceed as follows:

a. Remove the rear cover (refer to paragraph 6-6) from the drive.

b. Remove the two T15 screws (4) which secure the HP-IB assembly to the drive.

c. Disconnect the HP-IB assembly from connector J1 on controller PCA-A6 (9).

Reinstallation is a reversal of the removal procedure.

6-8. FRONT PANEL

To remove the front panel (41, figure 9-1), proceed as follows:

a. Perform the drive preparation for service procedure outlined in paragraph 6-4.

b. Pull forward on the front panel (41), to release it from the two snap-in studs (50) on the front cover (49) and the two studs (89) on the drive mainframe (90).

c. Remove the front panel (41) from the drive.

Reinstallation is a reversal of the removal procedure.

6-9. FRONT COVER

To remove the front cover (49, figure 9-1), proceed as follows:

a. Perform the drive preparation for service procedure outlined in paragraph 6-4.

b. Remove the front panel (refer to paragraph 6-8) from the drive.

c. Remove the twelve T15 screws (47) and two T10 screws (48) which secure the front cover (49) with prefilter (53) attached, to the drive.

d. Remove the front cover (49) and prefilter (53) from the drive.

Reinstallation is a reversal of the removal procedure.

6-10. CONTROLLER PCA-A6

To remove controller PCA-A6 (9, figure 9-1), proceed as follows:

a. Remove the rear cover (refer to paragraph 6-6) and the HP-IB assembly (refer to paragraph 6-7) from the drive.

b. Remove power jumper cable W6 (5) and signal jumper cable W7 (6) from the drive.

c. Disconnect connector P2 on HDA cable W8 (7) from connector J7 on read/write PCA-A2 (16).

d. While holding cable W8 (7) out of the way, press down on the PCA guide (78) latch and withdraw PCA-A6 (9), with servo PCA-A1 (11) and read/write PCA-A2 (16) attached, until servo PCA-A1 latches.

e. Disconnect read/write PCA-A2 (with controller PCA-A6 attached) from servo PCA-A1.

f. Remove the four T10 screws (8) which secure HP-IB PCA-A6 (9) to the PCA shield (15).

g. Disconnect controller PCA-A6 (9) from read/write PCA-A2 (16).

Reinstallation is a reversal of the removal procedure.

6-11. EPROM KIT, CONTROLLER PCA-A6

To remove the EPROM kit (10, figure 9-1) from controller PCA-A6, proceed as follows:

a. Remove controller PCA-A6 (refer to paragraph 6-10) from the drive.

b. Remove the four EPROMs (10) from their 28-pin sockets on PCA-A6. See figure A-4 for the location of the EPROMs.

c. Place the EPROMs a piece of anti-static foam.

Reinstallation is a reversal of the removal process.

NOTE

Ensure that the EPROMs are inserted in their proper sockets, with the notches on the EPROMs facing towards connectors P1 and P2 on the PCA.

6-12. READ/WRITE PCA-A2

To remove read/write PCA-A2 (16), proceed as follows:

a. Remove read/write PCA-A2 from the drive as described in steps a through e of the controller PCA-A6 removal procedure (refer to paragraph 6-10).

b. Remove the four T10 screws (14) which secure read/write PCA-A2 (16) to the PCA shield (15).

c. Disconnect read/write PCA-A2 (16) from controller PCA-A6 (9).

d. Remove the two T10 screws (12) which secure the ground assembly (13) to PCA-A2 (16) and remove the ground assembly (13).

Reinstallation is a reversal of the removal procedure.

6-13. SERVO PCA-A1

To remove servo PCA-A1 (11), proceed as follows:

a. Remove read/write PCA-A2 from the drive as described in steps a through e of controller PCA-A6 removal procedure (refer to paragraph 6-10).

b. While holding cable W8 (7) out of the way, press down on the PCA guide (78) latch and slide servo PCA-A1 out of the drive.

Reinstallation is a reversal of the removal process.

6-14. POWER DISTRIBUTION PCA-A5

To remove power distribution PCA-A5 (28, figure 9-1), proceed as follows:

a. Remove controller PCA-A6 (refer to paragraph 6-10), read/write PCA-A2 (refer to paragraph 6-12), and servo PCA-A1 (refer to paragraph 6-13).

b. Disconnect connectors P2 and P3 on power supply output cable W4 (88) from connectors J2 and J1, respectively, on power distribution PCA-A5 (28).

c. Disconnect connector P1 on speed sensor cable W5 (34) from connector J3 on PCA-A5 (28).

d. Disconnect connector P1 on primary power cable W1 (87) from connector J1 on filter FL1 (24).

e. Remove the four T15 screws (20) and four T10 screws (21) which secure the rear panel (22) to the drive.

NOTE

The three T15 screws which secure the line filter (24) to the rear panel need not be removed.

f. Remove the rear panel (22) from the drive.

g. Remove the four T10 screws (27) which secure power distribution PCA-A5 (28) to the rear panel (22) and remove the PCA.

Reinstallation is a reversal of the removal procedure.

6-15. LINE FILTER ASSEMBLY FL1

To remove line filter assembly FL1 (24, figure 9-1), proceed as follows:

a. Remove the rear panel (22) as described in steps a through f of the power distribution PCA-A5 removal procedure (refer to paragraph 6-14).

b. Remove the three 15 screws (23) securing the line filter (24) to the rear panel (22).

c. Disengage the line filter connector from its

support bracket.

d. Pull the line filter away from he rear panel until the two ground terminal mounting screws are accessible.

e. Remove the two ground terminal mounting screws and remove the line filter.

WARNING

When reinstalling the line filter assembly (22), tighten the two ground terminal mounting screws securely. This ensures that a good ground connection is established.

Reinstallation is a reversal of the removal procedure.

6-16. DRIVE BELT, MOTOR PULLEY

To remove the drive belt (55, figure 9-1) and motor pulley (58), proceed as follows:

a. Remove the front panel (refer to paragraph 6-8) and front cover (refer to paragraph 6-9) from the drive.

b. Pull the belt cover (54) forward and out of the drive.

CAUTION

Do not turn the spindle pulley on head-disc assembly A3 (35) during removal and replacement of the drive belt. Failure to observe this precaution could result in damage to the HDA.

c. Remove the five T9 screws (65) which secure the top cover (66) to the drive.

d. Remove the fan scroll cover clip (67) and fan scroll cover (79) by loosening the T10 mounting screw (68).

e. Remove the 1/2-inch nut (56) which secures the belt guard (57) and motor pulley (58) to the motor (74) shaft. Hold the fan rotor (71) to keep the shaft from turning while removing the nut.

f. Remove the belt guard (57), drive belt (55), and motor pulley (58) from the motor (74) shaft.

CAUTION

When the top cover (66) is reinstalled, make sure that the PCA guide on the cover fits freely between the edge of power supply PCA-A4 (60) and its metal base plate.

Reinstallation is a reversal of the removal procedure.

NOTE

1. The drive belt should be installed with its smooth (shiny) side in contact with the two pulleys.

2. Different drive belts are used for 60 Hz and 50 Hz operation. Ensure that the proper belt is reinstalled. The belts are identified by part number as follows:

07937-80033 - 60 Hz
07937-80034 - 50 Hz

3. Different motor pulleys are used for 60 Hz and 50 Hz operation. Ensure that the proper pulley is reinstalled. The pulleys are identified by part number as follows:

07936-20005 - 60 Hz
07937-20006 - 50 Hz

6-17. POWER SUPPLY PCA-A4

To remove power supply PCA-A4 (60, figure 9-1), proceed as follows:

a. Remove the front panel (refer to paragraph

6-8) and front cover (refer to paragraph 6-9) from the drive.

b. Disconnect connector P1 on power supply output cable W4 (88) from connector J2 on power supply PCA-A4 (60).

c. Partially withdraw PCA-A4 (60) from the drive mainframe (90) and disconnect connector P1 on power supply input cable W3 (59) from connector J1 on PCA-A4 (60).

d. Remove PCA-A4 (60) from the drive.

CAUTION

Ensure that the 2-pin connector on PCA-A4 is plugged into the proper voltage configuration connector ("115V" for 90-132 Vac; "230V" for 180-264 Vac) on PCA-A4. (Details of drive voltage configuration are provided in Section II of the *HP 7936 and HP 7937 Disc Drive Operating and Installation Manual*, part no. 07937-90902.

Reinstallation is a reversal of the removal procedure.

6-18. PRIMARY POWER PCA-A8

To remove primary power PCA-A8 (61, figure 9-1), proceed as follows:

a. Remove the front panel (refer to paragraph 6-8) and front cover (refer to paragraph 6-9) from the drive.

b. Disconnect connector P2 on primary power cable W1 (87) from connector J4 on PCA-A8 (61).

c. Disconnect connector B1P1 on the motor (74) brake cable from connector J3 on PCA-A8 (61).

d. Disconnect connector P5 on power supply output cable W4 (88) from connector J5 on PCA-A8 (61).

e. Disconnect connector P2 on power supply input cable W3 (59) from connector J7 on PCA-A8 (61).

f. Disconnect connector B1P2 on the motor B1 (74) power cable from connector J1/J2 on PCA-A8 (61).

g. Detach power supply input cable W3 (59) from the cable retainer on PCA-A8 (61).

h. Partially withdraw power supply PCA-A4 (60) from the drive.

i. Disconnect connector P1 on power supply output cable W4 (88) from connector J2 on power supply PCA-A4 (60).

j. Remove primary power PCA-A8 (61) from the drive.

CAUTION

Ensure that the motor (74) power connector is plugged into the proper voltage configuration connector ("J1-115V" for 90-132 Vac; "J2-240V" for 180-264 Vac) on PCA-A8. (Details of drive voltage configuration are provided in Section II of the *HP 7936 and HP 7937 Disc Drive Operating and Installation Manual*, part no. 07937-90902.

Reinstallation is a reversal of the removal process.

6-19. START CAPACITOR C1

To remove start capacitor C1 (62, figure 9-1), proceed as follows:

a. Remove primary power PCA-A8 (refer to paragraph 6-18) from the drive.

b. Remove capacitor C1 (62) and cap (63) from the retainer on PCA-A8 (61). Disconnect the wire assembly (64) from the capacitor (62).

Reinstallation is a reversal of the removal process.

6-20. MOTOR B1

To remove motor (74, figure 9-1), proceed as follows:

a. Remove the drive belt (55) and motor pulley (58) (refer to paragraph 6-16).

b. Remove the 1/2-inch nut (70) which secures the fan rotor (71) to the motor (74) shaft and remove the fan rotor (71).

c. Disconnect connector P1 on power supply output cable W4 (88) from connector J2 on power supply PCA-A4 (60).

d. Disconnect connector P5 on power supply output cable W4 (88) from connector J5 on primary power PCA-A8 (61).

e. Remove the two T10 screws (72) which secure the fan scroll (73) to the drive mainframe (90).

f. Being careful not to bend LED PCA-A7 (46), pull the LED PCA cable wires out of the cable clamp attached to the fan scroll (73). Remove the fan scroll.

g. Disconnect connector B1P2 on the motor (74) power cable from connector J1/J2 on primary power PCA-A8 (61).

h. Disconnect connector B1P1 on the motor (74) brake cable from connector J3 on PCA-A8 (61).

i. Release the spring (91) from the motor (74).

j. Turn the motor (74) on its hinged mounting bracket until it clears the drive mainframe (90) and then lift the motor out of the drive.

CAUTION

Ensure that the motor (74) power connector is plugged into the proper voltage configuration connector ("J1-115V" for 90-132 Vac; "J2-240V" for 180-264 Vac) on PCA-A8 (60).

CAUTION

When the fan scroll (73) is reinstalled, ensure that the PCA guide on the scroll fits between the edge of primary power PCA-A8 (60) and its plastic base plate.

CAUTION

When the top cover (66) is reinstalled, make sure that the PCA guide on the cover fits between the edge of power supply PCA-A4 (59) and its metal base plate.

Reinstallation is a reversal of the removal procedure.

6-21. HEAD-DISC ASSEMBLY A3

To remove head-disc assembly (HDA) A3 (35, figure 9-1), proceed as follows:

a. Remove the drive belt (55) and pulley (58) (refer to paragraph 6-16).

b. Remove the rear panel (22) as described in steps a through f of the power distribution PCA-A5 removal procedure (refer to paragraph 6-14).

c. Remove the two T9 screws (29) which secure the cover (25) and shock mount (32) to the drive mainframe (90).

d. Remove the T15 screw (31) which secures shock mount (32) to the top of the HDA (35).

e. Remove the shock mount (32) from the drive.

CAUTION

The head-disc assembly weighs approximately 34 kg (75 lb). Exercise caution when removing it from the drive.

f. Carefully slide the HDA (35) out of the drive and place it on a firm work surface.

NOTE

If the HDA is not being replaced, skip steps q through t.

g. Remove the shunt connector from J1 of the new HDA and place it on connector J1 of the old HDA.

NOTE

A spindle lock is installed on replacement HDAs to protect them during shipment. During installation, the lock must be removed from the new HDA and installed on the old HDA to protect it during shipment back to the factory. Two different types of locks are used: spring-type (see figure 6-1) and bracket-type (see figure 6-2).

h. Carefully tilt the new HDA until it is resting on its side and the spindle lock is accessible. Identify the type of spindle lock installed on the HDA (see figures 6-1 and 6-2).

i. To remove a spring-type spindle lock (figure 6-1), push down on the lock and disengage it from the base plate. Remove the lock and install it on the old HDA.

j. To remove a bracket-type spindle lock (see figure 6-2), proceed as follows:

1) On the new HDA, remove the two T15 screws (39, figure 9-1) securing the spindle ground spring assembly (40) to the HDA. Remove the ground spring assembly.

2) Remove the two T15 screws securing the spindle lock to the new HDA and remove the lock.

3) Reinstall the spindle ground spring assembly on the new HDA.

4) Install the spindle lock on the old HDA by reversing the previous three steps.

Reinstallation of the HDA is a reversal of steps a through p of the removal procedure.

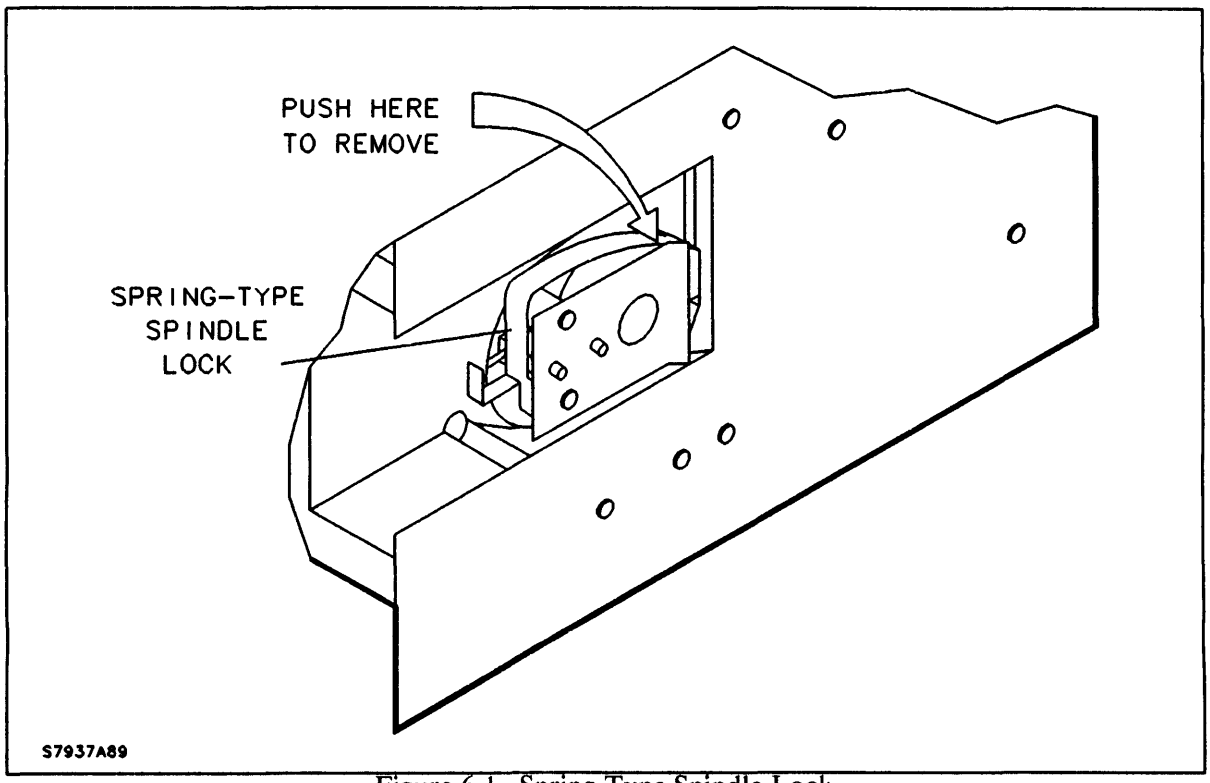


Figure 6-1. Spring-Type Spindle Lock

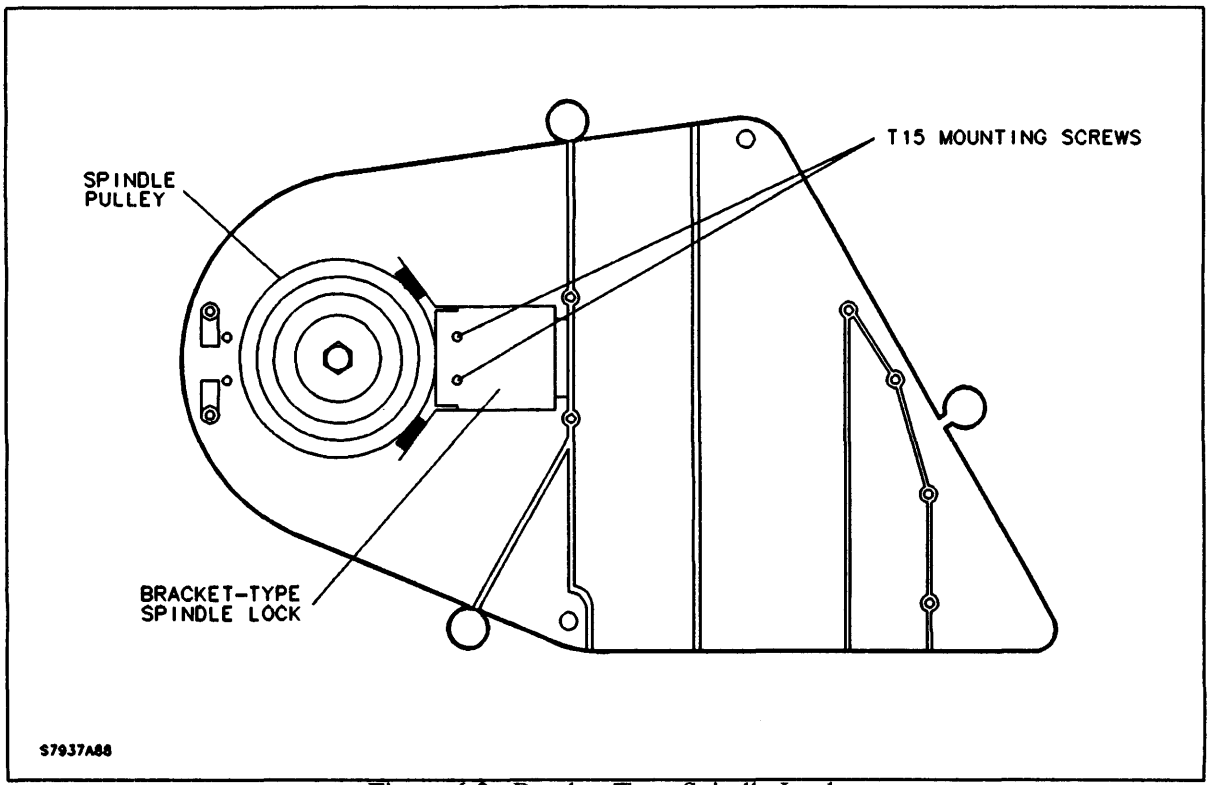


Figure 6-2. Bracket-Type Spindle Lock

Adjustments 7

7-1. INTRODUCTION

WARNING

The drive does not contain operator-serviceable parts. To prevent electrical shock, refer all maintenance procedures to service-trained personnel.

Troubleshooting and Diagnostics 8

8-1. INTRODUCTION

This chapter contains troubleshooting information for the drive. Included are safety considerations, trouble shooting strategy, details of the diagnostic test switch and LED display, a description of the servo and read/write test fixtures, and an introduction to the external exerciser.

8-2. SAFETY CONSIDERATIONS

WARNING

The drive does not contain operator-serviceable parts. To prevent electrical shock, refer all maintenance activities to service-trained personnel.

WARNING

The anti-tip feet on the cabinet or equipment rack in which the drive is installed must be extended before the drive is pulled out on its rack slides.

CAUTION

Electrostatic-sensitive devices within the drive require special care if damage is to be avoided. Take appropriate precautions when removing components from the drive. Make sure that the drive is properly grounded and a grounding strap should be worn by service personnel. Upon removal, store the components in anti-static, conductive plastic bags.

Do not turn ac power to the drive on or off when the system is in an active state.

Do not connect or disconnect the interface cable to the host when the system is in an active state.

8-3. TROUBLESHOOTING STRATEGY

The drive is designed to be repaired quickly on site by the replacement of field-replaceable assemblies. To aid in diagnosing drive malfunctions, several important service tools are available. The first of these is the self-test diagnostic routine which is initiated each time the drive is powered on. Hardware malfunctions discovered during the self-test diagnostics are identified by the front panel LED display.

The second service tool used for troubleshooting the drive is the external exerciser program. The exerciser provides expanded capability for selectively testing the drive and retrieving more detailed error and status information.

Two hardware test PCAs are also available for use in troubleshooting the drive. These fixtures allow a number of digital and analog signals in the servo and read/write circuits to be monitored while the drive is in operation.

Details of these troubleshooting aids are provided in the following paragraphs.

8-4. SELF TEST DIAGNOSTICS

Resident in the drive controller's firmware are self-test diagnostics which are invoked at power-on. These diagnostics perform a series of subtests which verify operation of the drive. The subtests perform many hardware checks, first by micro-diagnostics and then by higher level macrodiagnostics such as seeks, reads, and writes.

A rear panel Diagnostic switch allows the selection of the normal hardware diagnostic sequence (Run

Time Mode) or a Diagnostic Mode which adds Read-Only Error Rate Tests (RO ERT) to the sequence. The results of the diagnostics are passed to the front panel LED display, providing a visual indication of the operational status of the drive.

The external exerciser program can also be used to initiate the self-test diagnostics and retrieve the resultant status/error information.

8-5. DIAGNOSTIC SWITCH

Diagnostic switch S1 is one segment of the 4-segment Channel Address/Diagnostic switch assembly, located on the rear panel of the drive. See figure 3-2. Two diagnostics can be selected by the switch: RUN TIME MODE and DIAGNOSTIC MODE. The selected switch position is read each time the drive is powered on.

8-6. RUN TIME MODE. When switch S1 is set to the RUN TIME MODE position, a series of hardware tests are performed at power-on. Following successful completion of the hardware diagnostic routines, the drive comes on line. The diagnostic normally takes approximately 10 seconds to complete. During this time the front panel LEDs sequence through the following display:

RED	YELLOW	GREEN	DURATION
ON	ON	ON	8 seconds
OFF	ON	ON	2 seconds
OFF	OFF	ON	continuous

Successful completion of the diagnostic is indicated by the Green LED remaining lit at the end of the sequence. If the drive fails the hardware diagnostic, the Red LED will remain lit and the Yellow and Green LEDs will be coded to indicate the malfunctioning assembly. A power supply failure or loss of input power is indicated by all LEDs extinguished.

The coding for the LEDs is shown on a label on the rear panel. See figure 3-2.

NOTE

A drive fault condition (Red LED illuminated) does not necessarily mean that the controller is incapable of communication with the host. In most cases, details of the fault condition (over and above the information encoded by the LEDs), can still be obtained by using the external exerciser to retrieve status and error information.

8-7. DIAGNOSTIC MODE. If S1 is set to the DIAGNOSTIC MODE position, the same hardware diagnostic executed in RUN TIME MODE is invoked when power is applied. However, the controller does not bring the drive on line following the completion of the hardware diagnostic routines. Instead, the drive performs a full-volume RO ERT (7.5 minutes) followed by a continuous loop of random RO ERTs.

When the drive successfully completes the hardware diagnostics and begins the RO ERTs, both the Yellow and Green LEDs will be illuminated. If any uncorrectable or marginal data errors occur during the RO ERT, the Green LED is extinguished leaving only the Yellow LED lit.

A hardware diagnostic failure will be indicated by the Red LED remaining lit and the Yellow and Green LEDs coded to indicate the source of the most likely malfunctioning assembly. A power supply failure or loss of input power is indicated by all LEDs extinguished.

The coding for the LEDs is listed on a label on the rear panel. See figure 3-2.

NOTE

Failure information gathered during this time will be logged in the internal error logs. To retrieve this failure information, Diagnostic switch S1 must be returned to the RUN TIME MODE position and the power cycled. After this, the information can be obtained by using the appropriate external exerciser command.

8-8. LED DISPLAY

The front panel LED display provides the operator with a visual indication of the operational status of the drive. The LED display consists of single red, green, and yellow LEDs. As explained in the preceding paragraphs, the significance of the LED patterns is determined by the operating mode of the drive (RUN TIME or DIAGNOSTIC). The Front Panel Status label affixed to the rear of the drive indicates the pattern coding of the LEDs (see figure 3-2).

In addition to its role as a status display, the Green LED also serves as an activity indicator, flashing any time the drive is exchanging data or commands with the host.

8-9. ASSEMBLY IDENTIFICATION

The assemblies in the drive associated with the faults indicated by the LED display are:

FAULT	ASSEMBLY
Power Supply	Power Supply PCA-A4
	Power Distribution PCA-A5
	Primary Power PCA-A8
Motor	Motor B1
Read/Write	Read/Write PCA-A2
Servo	Servo PCA-A1
	Read/Write PCA-A2
Controller	Controller PCA-A6

Removal and replacement procedures for all of the assemblies listed above are provided in Chapter 6.

NOTE

1. There is no LED readout identifying a head-disc assembly (A3) fault. This is to discourage the early replacement of the HDA in the troubleshooting process, before it is established that one of the other assemblies is defective. Refer to paragraph 8-24 for further details.

2. There is no LED readout identifying a cabling fault (cable assemblies W1 through W8). Check that the cable connectors are properly seated in their mating connectors before considering the replacement of a PCA. The following cables are associated with faults indicated by the LEDs:

FAULT	CABLE
Power Supply	W1, W3, W4, W6
Motor	Motor B1 cables
Read/Write	W8
Servo	W5, W7, W8

3. A portion of the servo system circuitry is located on read/write PCA-A2. A servo fault may require the replacement of servo PCA-A1 and/or read/write PCA-A2.

8-10. CS/80 EXTERNAL EXERCISER

Additional capability for troubleshooting and isolating drive failures is provided by the CS/80 External Exerciser program. The external exerciser is an interpreter which links the drive's internal diagnostic utilities to a service-trained person.

The operation of the exerciser program is detailed in the *CS/80 External Exerciser Reference Manual*, part no. 5955-3462.

This document provides detailed information regarding the use and operation of the exerciser. All exerciser commands supported by the drive, including any product-specific information, are listed in table 8-1.

The external exerciser can be used to test the drive hardware by initiating the self-test diagnostics. The diagnostic results can then be retrieved and examined to aid in isolating the fault.

The exerciser is also used to establish and maintain media integrity. Error Rate Tests (ERT) are used to isolate defective media locations. Media maintenance is accomplished through the use of sparing operations for defective sectors and initialize routines for reformatting the entire disc media.

In addition to retrieving drive status, the exerciser also provides access to the various fault and error logs maintained by the drive. This log information can be invaluable in isolating drive problems.

8-11. ERROR LOGS

In addition to the LED display and the drive status, the drive also maintains several internal logs to record error information. The contents of these logs can be accessed using the appropriate external exerciser command. Details of these logs are provided in the following paragraphs.

8-12. ERROR RATE TEST (ERT) LOG

This log contains read data errors detected during an Error Rate Test (ERT). Data errors are initially logged in controller RAM, which holds a maximum of 5 entries. Periodically, the drive transfers the log entries from RAM to the ERT log on the disc maintenance tracks. There is a separate ERT log for each data head. The ERT log is located on the OD maintenance track and can hold a maximum of 101 log entries. The drive returns both RAM and disc entries when the fault log is read; therefore, a total of 106 ERT log entries can be returned for each head.

The log header includes the following information:

- Total number of data error entries
- Number of sectors transferred (by corresponding head)
- Number of correctable (by ECC) data errors
- Number of uncorrectable (by ECC) data errors

After the header information, there is an entry for each unique sector address that experienced one or more errors during the ERT. If there were multiple errors on the same sector, the information in the Error Code Byte represents all the errors that occurred. The counters in the log header are incremented for each error.

Each data error entry includes the following information:

- Logical address (cylinder, head, and sector) of the error
- Error Code Byte. This byte is defined in figure 8-1.
- Error type
- Occurrence count

8-13. RUN TIME LOG

The run time log contains data errors detected during operation of the drive, excluding those that occur during an ERT. The structure of the run time log is identical to that of the ERT log. However, there are important differences in the significance of some of the data fields. These differences are summarized below:

- The "number of correctable data errors" field in the run time log header indicates the number of times a single retry was required to recover data in a sector. Data errors corrected solely by ECC (no retry required) are ignored. Although counted, correctable errors are *not* entered in the run time log.
- The "number of uncorrectable data errors" field in the run time log header indicates the number of times two or more retries were required to recover data. Whether or not the data was ultimately recovered is indicated by the Error Code Byte for the sector. The drive uses a default retry time of 800 milliseconds, which equates to roughly 40 read attempts before the data is declared unrecoverable. All uncorrectable data errors are entered in the run time log.
- The run time log data error entries include only *uncorrectable* errors. The significance of the Error Code Byte returned with each run time log entry is shown in figure 8-2.

8-14. FAULT LOG

The fault log contains events and faults that have occurred during operation of the drive. These two types of entries cover all situations except data errors, which are recorded in the ERT log and run time log, as previously described. The fault log physically resides on the OD maintenance track on data surface 0.

The distinction between a fault and an event is related to their impact on command execution. An occurrence from which the drive can recover and still complete the current transaction is classified as an event. Events are retried by the drive in an attempt to continue the transaction. An occurrence that causes termination of a transaction is classified as a fault. A fault represents a situation from which the drive cannot recover, consequently the failed operation is not retried.

During routine operation of the drive, all faults are logged in the fault log. In addition, any event(s) associated with each fault are also logged. Events that are retried successfully and do not lead to a fault are not logged in the fault log. For example, if an offtrack condition (an event) is detected, the drive will try to reposition the heads back on track. If the attempt is successful, the offtrack event is not logged in the fault log. However, if the drive tries repeatedly without success to properly position the heads, the operation is terminated and a servo fault is logged in the fault log. All offtrack events associated with the fault are also logged.

During an ERT, *all* events and faults that occur are logged in the fault log. An event does not have to be associated with a fault to be logged during an ERT.

Faults and any related events are initially logged in controller RAM, which holds a maximum of 30 entries. Periodically, the drive transfers the log entries from RAM to the fault log on the disc maintenance tracks. The disc fault log can hold a maximum of 44 log entries. The drive returns both RAM and disc entries when the fault log is read; therefore, a total of 74 fault log entries can be returned.

Each entry in the log contains the following information:

- Current address (cylinder, head, and sector). This is the last address at which the servo system was successfully positioned.
- Target address (cylinder, head, and sector). This is the address the servo system was attempting to access when the error occurred.
- Hardware Fault Register. This byte is a collection of bits from the servo register and the read/write controller register. The purpose of this register is to provide additional information about the servo and read/write systems when a fault in the data path occurs. The significance of the individual register bits is defined in table 8-1.
- Error Code. This is the TERROR/DERROR (see table 8-2).
- Activity Number. This is a number which represents the number of seeks within a range that occurred between faults. The ranges are listed in table 8-1. The numbers given are approximations of the time that would have elapsed between faults if the drive was placed on a "typical" system and under "normal" activity.

8-15. ERROR CODES

The drive encodes internal error conditions into two-digit error codes. These codes, which are logged in the drive status and fault log, are retrieved using the appropriate external exerciser commands.

A complete list of the error codes is contained in table 8-2. The table includes the error code, the applicable controller interface, and a brief description of the error. The description identifies the errors as Faults, Events, or Status Only errors. This last category includes those errors which affect the status of the current transaction, but are not recorded in any logs.

Table 8-2 also includes a list of assemblies most likely to cause the associated error. The suspect assemblies are listed in order of descending probability.

NOTE

It is very important to note that when HDA A3 is called out as one of the most likely failing components in the drive, care should be taken to prove that the actual media, electronics, or mechanics is defective in the HDA. The HDA is the most expensive assembly in the drive and the most difficult assembly to replace. Be sure it requires replacement before doing so. In many cases, simple magnetic recording problems on the disc surface may be the problem. For example, a defective read/write PCA may have caused data destruction on the surface of the disc, which appears as a hard fault when reading. Simply replacing the R/W PCA and rewriting the suspect sectors will correct the problem. Refer to paragraph 8-19 for more details regarding data error related faults.

The drive errors are divided into two classifications: Test Errors (TERROR) and Drive Errors (DERROR). The classification of each error is determined by when the error occurred.

8-16. TERRORS

A TERROR is defined as an error that occurred during execution of the drive's self-test diagnostics, regardless of whether the diagnostics were invoked at power-on or by the host. When retrieving drive status following a diagnostic failure, each TERROR will be accompanied by a Field Replaceable Unit (FRU) code. The FRU identifies the most likely cause of the failure. In the DESCRIPTION column of table 8-2, the failing assembly is identified for those error codes which may be returned as TERRORS. If no assembly is indicated, the drive is unable to accurately isolate the malfunctioning hardware (FRU code = 0). TERRORs are also logged in the fault log; however, the accompanying FRU code is not recorded.

It should be understood that the FRU numbers do not necessarily correspond to the drive assembly numbers documented in this manual. The following matrix shows the relationship of the FRU numbers to the assembly numbers and the assembly names. Note that four of the drive assemblies, including head-disc assembly A3, do not have FRU numbers.

FRU	DRIVE ASSEMBLY
0	None - unable to isolate malfunctioning hardware
1	Controller PCA-A6
2	Read/Write PCA-A2
3	Servo PCA-A1
4	Power Supply PCA-A4
5	Spindle Motor B1
-	Head-Disc Assembly A3
-	Power Distribution PCA-A5
-	LED PCA-A7
-	Primary Power PCA-A8

8-17. DERRORS

Errors that occur during any drive activity other than self-test diagnostics are classified as DERRORs. The DERRORs, which are logged in both the drive status and the fault log, can be accessed using the appropriate external exerciser command.

The DERROR codes define a specific drive malfunction that occurred during routine drive operation. If the same malfunction occurred during self-test diagnostics, it would classified as a TERROR; therefore, certain error codes may fall into either category.

8-18. SERVO CONTROLLER ERROR CODES

Errors that are generated by the servo controller (see the servo flowcharts in chapter 5) are mapped into different error codes by controller PCA-A6 before being logged in the fault log. The following matrix allows the servo controller error codes to be converted to their corresponding TERROR/DERROR codes.

SERVO CONTROLLER ERROR (hex/dec)	TERROR/DERROR (hex/dec)
1/1	AC/172
2/2	72/114
3/3	73/115
6/6	76/118
7/7	78/120
9/9	B9/185
A/10	79/121
B/11	7A/122
C/12	7B/123
E/14	7D/125
10/16	7F/127
13/19	80/128
16/22	AD/173
17/23	1C/28
18/24	66/102
19/25	BA/186
1A/26	BB/187
1B/27	BC/188
1C/28	BD/189

8-19. DATA ERROR TROUBLESHOOTING

To date, there is little empirical data regarding detailed troubleshooting hints for data errors. Refer to the *HP 7936 and HP 7937 Disc Drive CE Handbook,* part no. 07937-90905, for the latest troubleshooting information as it becomes available.

The first step in the determination of the cause of data errors is to identify the nature of the data error. This is done most effectively by reading the ERT log and/or the run time log and analyzing the information provided. The formats for the ERT log and the run time log are described in paragraphs 8-12 and 8-13, respectively. The bits in the error code bytes for the logs are shown in figures 8-1 and 8-2. Care must be taken to remember which of the logs is being read as the definition of the data errors is different in each case.

The next step is to determine whether the error is "hard" or "soft". A hard error is repeatable at a certain address and indicates that the sector was written improperly by the electronics, or the media is defective. Soft errors are much less severe (they do not cause the loss of data) and may in fact be totally ignored if they occur infrequently.

After noting the error entries, a Read Only Error Rate Test (RO ERT) should be executed on (and possibly around) the offending sector(s). The results of this test should then be compared with the first log entries to determine if the error is hard, soft, or gone.

If the error is hard, there may be a media defect that should be spared. The only way to determine this is to perform a a Write-Then-Read Error Rate Test (WTR ERT) on the suspect sector(s). If the sector(s) being tested contains important data, then care should be taken to back up the data (if possible) before any write operation is performed. If after performing a WTR ERT on the suspect area, there is still an error in this sector, then the media is most likely at fault and a sparing operation is in order. However, before making a decision to spare, other areas should also be tested in order to prove that this is not just a random occurrence.

If the hard error disappears after being rewritten, the media is unlikely to be at fault and the blame shifts to the electronics.

If the error is soft to begin with, the electronics will initially be suspect. There is one test that can be used to differentiate between errors caused by the servo system and the read/write system. First, execute a full volume RO ERT and see if there are any soft errors. Next, execute several random RO ERT passes (10 or more) and see if the error rate changes for the worse. If it does, the servo system may be at fault. If there is no change, then the read/write system is more suspect.

Another source of soft errors is problems with the drive environment. Do not overlook the "cleanliness" of the primary power input, and RFI and ESD levels.

8-20. CHECKING POWER SUPPLY VOLTAGES

There are no test points on power supply PCA-A4; however, the power supply output voltages can be measured at connector P2 on power jumper cable W6. See figure 8-3. To reach W6, it is necessary to remove the rear cover from the drive. Cable W6

need not be disconnected from power distribution PCA-A5 and read/write PCA-A2. A voltmeter probe can be inserted into the openings on the rear of the connector. Figure 8-3 lists the voltage and ripple limits for the power supply output voltages.

NOTE

There are no adjustments for the power supply output voltages.

Power supply output signals Power On Reset POR-L and Power Fail PF-L can be monitored at pins 1 and 2, respectively, of connector J5 on PCA-A5. See figure 8-3.

8-21. SERVO TEST POINT PCA

Servo test point PCA, part no. 07937-60208, allows a number of servo system digital and analog signals to be monitored with suitable test equipment, while the drive is in operation. See figure 8-4. To install the PCA in the drive, proceed as follows:

a. Extend the anti-tip feet on the cabinet.

b. Extend the drive out of the cabinet on its rack slides.

c. Remove the two T9 screws which secure the access cover for servo PCA-A1 to the top of the drive and remove the cover. The location of the cover is shown in figure 9-1, item 81.

d. Plug the servo test point PCA into the 50-pin connector on PCA-A1, visible through the opening in the top of the drive.

The mnemonics used in figure 8-4 to identify the test PCA signals are described in table 8-3. The test points are identified by number in the servo system functional diagrams S1 and S2 in chapter 12.

8-22. READ/WRITE TEST POINT PCA

Read/write test point PCA, part no. 07937-60209, allows a number of read/write system digital and analog signals to be monitored with suitable test equipment, while the drive is in operation. See figure 8-5. To install the PCA in the drive, proceed as follows:

a. Extend the anti-tip feet on the cabinet.

b. Extend the drive out of the cabinet on its rack slides.

c. Remove the two T9 screws which secure the access cover for read/write PCA-A1 and controller PCA-A6 to the top of the drive and remove the cover. The location of the cover is shown in figure 9-1, item 81.

d. Plug the PCA into the 16-pin connector on PCA-A2, visible through the opening in the top of the drive.

The mnemonics used in figure 8-5 to identify the test PCA signals are described in table 8-4. The test points are identified by number in the read/write system functional diagram R1 in chapter 12.

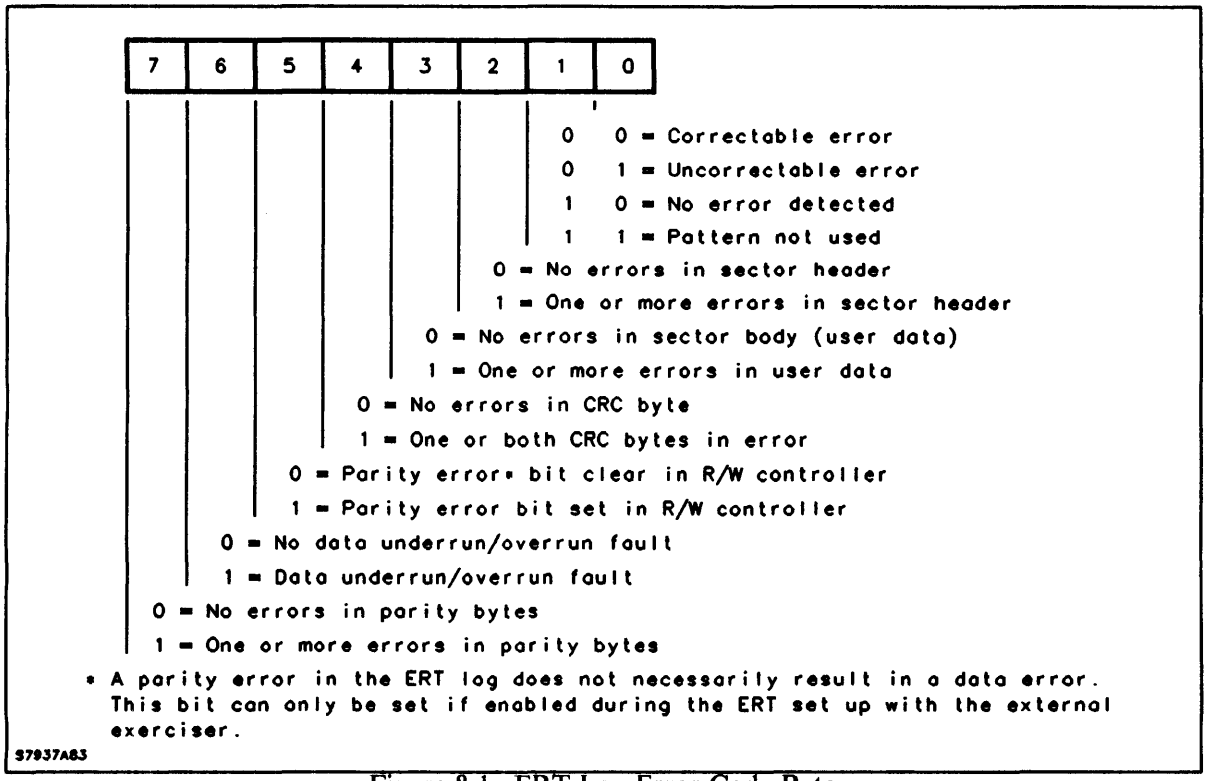


Figure 8-1. ERT Log Error Code Byte

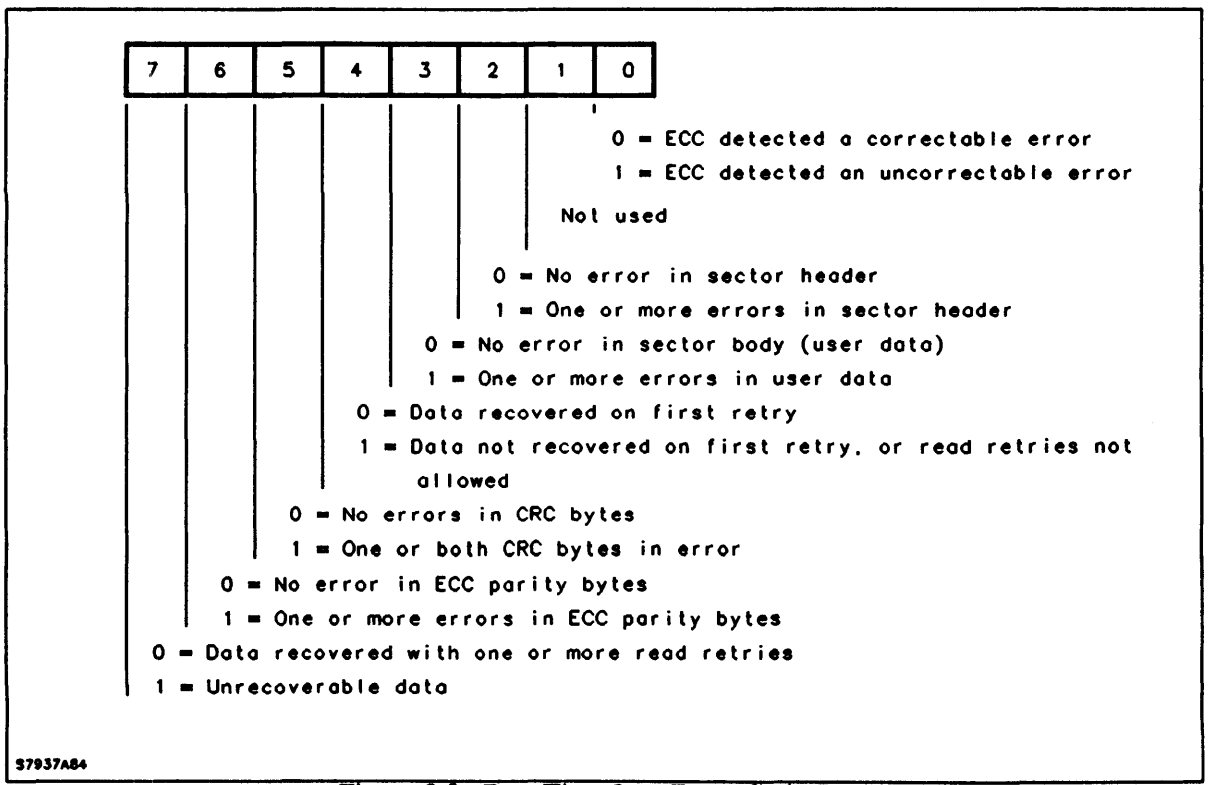
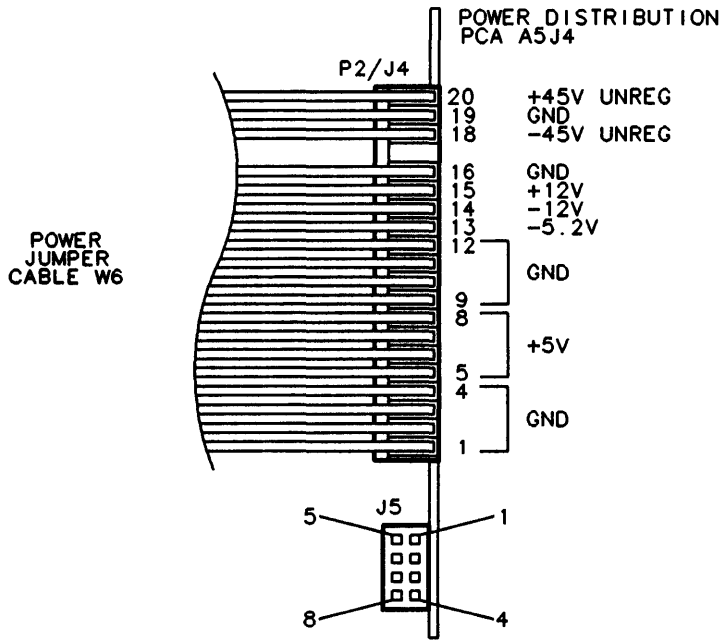


Figure 8-2. Run Time Log Error Code Byte



POWER SUPPLY PCA-A4 OUTPUT VOLTAGES:

W6P2	OUTPUT	RANGE (V)	MAX RIPPLE (P-P)
5-8	+5V	4.75 TO 5.25	100 mV
13	-5.2V	-4.9 TO -5.40	100 mV
14	-12V	-10.8 TO -13.2	200 mV
15	+12V	10.8 TO 13.2	200 mV
18	-45V	-30 TO -45*	1V
20	+45V	30 TO 45*	1V
1-4, 9-12, 16, 19	GND	—	—

*Typical values for the 45V outputs are: 32V when seeking, 37V when not seeking.

S7937A23

Figure 8-3. Power Supply PCA-A4 Outputs

Table 8-1. External Exerciser Commands (1 of 4)

COMMAND	DETAILS
CACHEOFF	7936XP/7937XP drives only.
CACHEON	7936XP/7937XP drives only.
CACHE LOG	7936XP/7937XP drives only. Correctable errors are defined as a single-bit error in a byte of the cache memory. An uncorrectable error is a double-bit error in a single byte of cache memory.
CACHE STATUS	7936XP/7937XP drives only.
CANCEL	No device-specific information.
CHANNEL	No device-specific information.
CICLEAR	No device-specific information.
CLEAR LOGS	When clearing disc logs, all associated entries currently in RAM are also cleared. Used to clear the cache log on 7936XP/7937XP drives.

DESCRIBE	The drive returns the following information:
	`MODEL: 7937 or 7936`
	`UNIT: 0`
	`TYPE: DISC`
	`Max Cylinder Address: 1395`
	`Max Head Address: 12 (7937) or 6 (7936)`
	`Max Sector Address: 122`
	`Max Block Address: 2,232,203 (7937) or 1,202,816 (7936)`
	`Current Interleave: 1`

DIAG	The only diagnostic executed by the drive is the power-on diagnostic (number 0). The duration of the diagnostic is approximately 10 seconds.
ERT LOG	Each head returns up to 106 entries. The format for the Error Code Byte returned with each log entry is shown in figure 8-1. (Refer to paragraph 8-12 for more information concerning the ERT log.)
EXIT	No device-specific information.

Table 8-1. External Exerciser Commands (2 of 4)

FAULT LOG

The disc fault log contains up to 44 entries, is not read destructive, and upon being read may include up to 30 entries contained in controller RAM. (Refer to paragraph 8-14 for more information concerning the fault log.)

TERROR/DERROR codes returned can be decoded using table 8-2. The Hardware Fault Register (HFR) bits are decoded as follows:

BIT	ERROR	SYSTEM
0	Spin-up failed	Servo
1	Servo timing error	Servo
2	Heads off-track	Servo
3	AGC error	Servo
4	Sector timing error	Servo
5	Data overrun	Read/Write
6	Undefined	
7	Undefined	

The significance of the Activity Number field is defined as follows:

ACTIVITY NUMBER	NUMBER OF SEEKS
0	none
1	1
2	2
3	3
4	4
5	5 to 7 (1 second)
6	8 to 200 (1-30 seconds)
7	201 to 2,000 (30 seconds-5 minutes)
8	2,001 to 12,000 (5-30 minutes)
9	12,001 to 25,000 (30-60 minutes)
10	25,000 to 150,000 (1-6 hours)
11	150,000 to 600,000 (6-24 hours)
12	600,000 to 4,000,000 (1-7 days)
13	4,000,000 to 16,000,000 (1-4 weeks)
14	16,000,000 to 100,000,000 (1-6 months)
15	>100,000,000 (>6 months)

Table 8-1. External Exerciser Commands (3 of 4)

HELP	No device-specific information.
INIT MEDIA	This utility destroys all user data. When executed, a worst case data pattern (22 hex) is written in the data field of all of the user sectors, and header information is recorded in the first six bytes of each sector. The postamble is also rewritten to reflect an ECC pattern matching the data. Options allow the user to retain only primary spares (P), retain primary and secondary spares (A), or initialize only the maintenance tracks (M). All disc logs are cleared when performing an INIT MEDIA operation.
OPER	No device-specific information.
PRESET	No device-specific information.
READ FULL SECTOR	Returns all of the data in a sector including the 6 header bytes, 2 CRC bytes, and 12 ECC bytes. The sector address value used when executing this command represents a *physical* sector address. If the track on which the specified sector resides has undergone a sparing operation, the logical and physical sector addresses may not correspond.
REQSTAT	No device-specific information.
RESET STATS	Clears cache table on 7936XP/7937XP drives.
REV	No device-specific information.
RO ERT	During an ERT the ECC circuit is functioning, but no data correction takes place. Retrys are not performed during an ERT. No offset is allowed when performing an ERT. The format for the printed error information is defined in the details for the ERT LOG command.

Table 8-1. External Exerciser Commands (4 of 4)

RUN LOG	Each head returns up to 106 entries. The format for the Error Code Byte returned with each log entry is shown in figure 8-2. (Refer to paragraph 8-13 for more information concerning the run time log.)
SDCLEAR	No device-specific information.
SERVO	The drive performs a "butterfly" seek on the specified head(s). This test performs all possible length seeks in both directions (2808 seeks). The test can be run on an individual head or all heads. If all heads are selected, each head (starting with 0) completes a butterfly seek before the next sequential head begins its seeks. If a fault occurs during the test, the drive logs the fault and continues with the next length seek. Drive status and the fault log provide information concerning the results of the test. The test takes approximately 1 minute for each head tested.
SPARE	No device-specific information.
SPARE TABLE	The spare table is generated at power-on and stored in controller RAM. Any spares added since power-on are included in the table. Because the spare table is volatile, the drive always returns zero as the "number of secondary spares" value.
TABLES	The only tables supported are the spare track table and the cache table (7936XP/7937XP drives).
UNIT	The drive is addressed as unit 0. The controller is individually addressable as unit 15.
WRITECACHEOFF	7936XP/7937XP drives only.
WRITECACHEON	7936XP/7937XP drives only.
WRITE LOG	7936XP/7937XP drives only
WRT ERT	No offset is allowed when performing an WTR ERT. The format for the printed error information is defined in the details for the ERT LOG command.

Table 8-2. List of DERROR/TERROR's (1 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
1/1	HP-IB	END OF VOLUME. (Status Only). The host attempted to access data across a volume boundary.	1. Host hard/software 2. Cabling 3. Controller PCA-A6
3/3	HP-IB	SERVO TIMEOUT. (Event; FRU = servo). The servo system did not respond to a command before the expiration of the watchdog timer.	1. Servo PCA-A1 2. Controller PCA-A6
4/4	HP-IB	INVALID CONTROLLER EVENT. (Fault; FRU = controller). An invalid executive program event value was detected during the execution of a controller program task.	1. Controller PCA-A6
5/5	HP-IB	CHANNEL TIMEOUT. (Fault; FRU = controller). The channel program has aborted a transaction because the channel byte timer has expired.	1. Controller PCA-A6
7/7	HP-IB	MARGINAL DATA. (Status Only). The requested data was read from the disc with some difficulty (at least one read retry).	Refer to data error troubleshooting hints in paragraph 8-19.
8/8	HP-IB	UNRECOVERABLE DATA. (Fault). Data was unrecoverable at the specified block address.	Refer to data error troubleshooting hints in paragraph 8-19.

Table 8-2. List of DERROR/TERROR's (2 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
9/9	HP-IB	UNRECOVERABLE DATA OVERFLOW. (Fault). The previous transaction contained more than one unrecoverable data block.	Undetermined or parts not required.
B/11	HP-IB	UNRECOVERABLE DATA DURING VERIFY. (Fault). During the previous Locate And Verify command at least one block of data was unrecoverable.	Undetermined or parts not required.
D/13	HP-IB	NO AVAILABLE SPARES. (Status Only). All spare tracks have been allocated, indicating media degradation.	Most likely caused by a very high error rate problem. Refer to data error troubleshooting hints in paragraph 8-19.
10/16	HP-IB	MEDIA WEAR. (Status Only). The last available spare track was just used.	Most likely caused by a very high error rate problem. Refer to data error troubleshooting hints in paragraph 8-19.
11/17	HP-IB	ILLEGAL OPCODE. (Status Only). An unrecognized opcode was received.	1. Host hard/software 2. Cabling 3. Controller PCA-A6
12/18	HP-IB	ADDRESS BOUNDS. (Status Only). The target address specified exceeds the address boundary for this device.	1. Host hard/software 2. Cabling 3. Controller PCA-A6

Table 8-2. List of DERROR/TERROR's (3 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
13/19	HP-IB	ILLEGAL PARAMETER. (Status Only). A parameter field was the wrong length for the opcode preceding it.	1. Host hard/software 2. Cabling 3. Controller PCA-A6
14/20	HP-IB	UTILITY PARAMETER. (Status Only). The utility opcode received is not supported for this device, or the utility parameter received is out of range for the specified utility opcode.	1. Host hard/software 2. Cabling 3. Controller PCA-A6
15/21	HP-IB	REQUEST RELEASE. (Status Only). The drive needs to make a nonvolatile copy of its RAM logs in the disc logs.	None
16/22	HP-IB	MAINTENANCE TRACK OVERFLOW. (Status Only The error and fault log areas of the disc are full.	None
17/23	HP-IB	BAD SPARE AT POWER-ON. (Fault). During the power-on sequence, the mapping of a spare track could not be determined.	1. Read/Write PCA-A2 2. HDA A3
18/24	HP-IB	BAD SECTOR MARK TIMER. (Fault; FRU = controller). During power-on diagnostics, the SOS-L signal timer in the controller was unable to interrupt or count correctly.	1. Servo PCA-A1 2. Controller PCA-A6

Table 8-2. List of DERROR/TERROR's (4 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
19/25	HP-IB	SERVO RECALIBRATE TIMEOUT. (Event; FRU = servo). The controller watchdog timer monitoring a servo recalibration command expired prior to response from the servo system.	1. Servo PCA-A1 2. Read/Write PCA-A2 3. HDA A3
1A/26	HP-IB	SERVO RECALIBRATE FAULT. (Event; FRU = servo). Too many error events occurred during attempts to recalibrate the servo, or insufficient channel time was available to start servo recalibration.	1. Shipping Latch 2. Servo PCA-A1 3. Read/write PCA-A2 4. HDA A3
1B/27	HP-IB	SERVO RESYNC TIMEOUT. (Fault; FRU = servo). The servo system did not respond after attempting to resynchronize the servo/controller communication interface.	1. Servo PCA-A1 2. Controller PCA-A6
1D/29	HP-IB	DATA PATH CONTROL INTERFACE FAULT. (Fault; FRU = read/write). During diagnostic functional testing, the data path control bus interface between the read/write and controller showed a data miscompare.	1. Read/Write PCA-A2 2. Controller PCA-A6
1F/31	HP-IB	WRITE FAILURE (Fault; FRU = read/write). During diagnostic functional testing, a disc write was not successfully completed on a reserved selftest data track.	1. Read/Write PCA-A2 2. Controller PCA-A6 3. HDA A3

Table 8-2. List of DERROR/TERROR's (5 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
20/32	HP-IB	READ FAILURE (Fault; FRU = read/write). During diagnostic functional testing, a disc read was not successfully completed on a reserved selftest data track.	1. Read/Write PCA-A2 2. Controller PCA-A2 3. HDA A3
21/33	HP-IB	CAN'T DETECT DATA ERROR (Fault; FRU = controller). During diagnostic function testing, an uncorrectable data error could not be detected by the controller ECC circuit during a disc read of the reserved selftest data track.	1. Controller PCA-A6 2. Read/Write PCA-A2
23/35	HP-IB	EMPTY DATA BUFFER NOT DETECTED. (Fault; FRU = controller). The controller DMA circuit did not interrupt indicating a DMA RAM buffer empty condition.	1. Controller PCA-A6 2. Read/Write PCA-A2
25/37	HP-IB	POWER ON. (Status Only). The drive has completed power-on initialization following power disruption.	None
26/38	HP-IB	UTILITY END. (Fault). This fault is logged at the end of a utility as a dummy error. The action of logging this fault will cause any events which occurred during the utility to be copied from the event log into the fault log.	None

Table 8-2. List of DERROR/TERROR's (6 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
27/39	HP-IB	TOO MANY SERVO EVENTS. (Fault). Insufficient fault recovery time exists or the maximum number of allowable hardware events has occurred during recovery.	1. Servo PCA-A1 2. Shipping Latch 3. Read/Write PCA-A2 4. HDA A3
28/40	HP-IB	TOO MANY DISC EVENTS. (Fault). Insufficient fault recovery time exists or the maximum number of allowable hardware events has occurred during fault recovery.	1. Read/Write PCA-A2 2. Controller PCA-A6 3. HDA A3
29/41	HP-IB	NO INDEX PULSE. (Fault; FRU = servo). The once-around, or Index Mark signal could not be detected during a format operation.	1. Servo PCA-A1 2. HDA A3
2A/42	HP-IB	MODULE ADDRESSING. (Status Only). An illegal volume or unit number was specified for this device.	1. Host hard/software 2. Cabling 3. Controller PCA-A6
2B/43	HP-IB	CHANNEL INTERFACE FAULT. (Fault; FRU = controller). A diagnostic test of the host channel interface circuit in the controller failed.	1. Controller PCA-A6
2C/44	HP-IB	PARAMETER BOUNDS. (Status Only). A parameter, other than unit, volume, or target address, is not allowed for this device.	1. Host hard/software 2. Cabling 3. Controller PCA-A6

Table 8-2. List of DERROR/TERROR's (7 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
2D/45	HP-IB	VERIFY FAILURE DURING SPARE. (Fault). Unrecoverable data, other than the target block address, was detected during a sparing operation.	1. Read/Write PCA-A2 2. Controller PCA-A6 3. HDA
2E/46	HP-IB	FAULT DURING SPARE. (Fault). A hardware fault occurred while verifying data track containing the target address.	1. Servo PCA-A1 2. Read/Write PCA-A2 3. Controller PCA-A6 4. HDA A3
2F/47	HP-IB	FAULT DURING AVAILABLE SPARE SEARCH (Fault). A hardware fault occurred while verifying the next available spare data track for use in sparing.	1. Servo PCA-A1 2. Read/Write PCA-A2 3. Controller PCA-A6 4. HDA A3
30/48	HP-IB	FAULT IN SPARE OR MAINTENANCE TRACK FORMAT (Fault). A hardware fault occurred while formatting the spare data tracks or the maintenance tracks.	1. HDA A3
31/49	HP-IB	READ DISC LOGS FAULT. (Event). The disc logs were not readable during a Read Logs command. The returned data is only the contents of the RAM logs.	Undetermined or parts not required.
32/50	HP-IB	RAM BUFFER EMPTY FAULT. (Fault; FRU = controller). The controller did not detect a RAM buffer empty condition during a disc write diagnostic test.	1. Controller PCA-A6

Table 8-2. List of DERROR/TERROR's (8 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
41/65	HP-IB	LOOPBACK PARITY ERROR. (Fault). A parity error occurred during a channel loopback command.	1. Controller PCA-A6 2. Cabling 3. Host Interface
45/69	HP-IB	CHANNEL PARITY ERROR. (Fault; FRU = controller). HP-IB interface circuit detected a parity error.	1. Controller PCA-A6 2. Host Interface 3. Cabling
46/70	HP-IB	INBOUND BYTE FAULT. (Fault; FRU = controller). The controller detected a bad hardware state of the HP-IB channel interface circuit while decoding a received message byte.	1. Controller PCA-A6
47/71	HP-IB	MESSAGE SEQUENCE ERROR. (Status Only). The sequence of the message is incorrect.	1. Controller PCA-A6 2. Host Interface 3. Cabling
48/72	HP-IB	RETRANSMIT COMMAND. (Status Only). The drive is currently in the release state and unable to complete the last command. Retransmit the last command.	None
4A/74	HP-IB	UNRECOGNIZED SECONDARY. (Status Only). An unknown secondary message byte was received from the host.	1. Controller PCA-A6 2. Host Interface 3. Cabling

Table 8-2. List of DERROR/TERROR's (9 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
4C/76	HP-IB	MESSAGE LENGTH ERROR. (Status Only). Channel message was the wrong length.	1. Host Interface 2. Cabling
4D/77	HP-IB	HP-IB INTERFACE FAULT. (Fault; FRU = controller). A hardware fault was detected in the HP-IB interface circuit of the controller.	1. Controller PCA-A6
4E/78	HP-IB	COMPLETION FAULT. (Fault; FRU = controller). The channel message did not complete.	1. Controller PCA-A6
52/82	HP-IB	TRANSPARENT MESSAGE LENGTH ERROR. (Status Only). The received transparent message was the wrong length.	1. Host 2. Controller PCA-A6
55/85	HP-IB	UNRECOGNIZED TRANSPARENT COMMAND. (Status Only). An unknown transparent command was received.	1. Controller PCA-A6
56/86	HP-IB	READ LOOPBACK ERROR. (Status Only). Controller fault detected during Read Loopback command.	1. Controller PCA-A6

Table 8-2. List of DERROR/TERROR's (10 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
5F/95	HP-IB	DEFAULT HDA CONFIGURATION. (Fault; FRU = servo). The default HDA configuration table has been used for specifying the drive description parameters. The default table specifies a 7937 HDA.	1. Servo PCA-A1
60/96	HP-IB	CATASTROPHIC CONTROLLER FAULT. (Fault; FRU = controller). A controller fault condition was detected which required resetting the drive.	1. Controller PCA-A6
61/97	HP-IB	POSITION VERIFY ERROR. (Event; FRU = servo). A verify of the track header address indicates that the heads are positioned incorrectly.	1. Servo PCA-A1 2. Controller PCA-A6 3. HDA A3
62/98	HP-IB	WRITE SERVO AMPLIFIER FAULT. (Fault; FRU = servo). The servo system reported an amplifier fault during a disc write.	1. Servo PCA-A1
63/99	HP-IB	WRITE SERVO AGC ERROR. (Fault; FRU = servo). The servo system reported an AGC error during a disc write.	1. Servo PCA-A1
64/100	HP-IB	WRITE SECTOR TIMING HIGH. (Fault; FRU = servo). The sector timing was higher than the specified limit during a disc write.	1. Servo PCA-A1

Table 8-2. List of DERROR/TERROR's (11 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
65/101	HP-IB	WRITE SECTOR TIMING LOW. (Fault; FRU = servo). The sector timing was higher than the specified limit during a disc write.	1. Servo PCA-A1
66/102	HP-IB	RECALIBRATE COMMAND IGNORED. (Fault; FRU = spindle). The servo has ignored a command to recalibrate the servo system because the spindle is not spinning sufficiently.	1. Spindle Motor B1
67/103	HP-IB	UNRESOLVED VERIFY FAILURE. (Event; FRU = controller). The compensation seek algorithm was unable to resolve the occurrence of a position verify error.	1. Controller PCA-A6
68/104	HP-IB	CORRECTABLE SEEK ERROR. (Event; FRU = servo). A position verify error has occurred because of head mispositioning, correctable using a compensatory seek.	1. Servo PCA-A1
69/105	HP-IB	UNCORRECTABLE SEEK ERROR. (Event: FRU = servo). A position verify error has occurred because of head mispositioning, uncorrectable using a compensatory seek.	1. Servo PCA-A1

Table 8-2. List of DERROR/TERROR's (12 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
6A/106	HP-IB	INVALID HEADER. (Fault). A position verify error has occurred because at least one sector on the current track has invalid header information.	Undetermined or parts not required.
6B/107	HP-IB	ADDRESS MISCOMPARE. (Event; FRU = servo). A position verify error has occurred because the servo system and controller cylinder position address do not agree.	1. Servo PCA-A1
6C/108	HP-IB	FORMAT FAULT. (Fault). Examination of the headers on the current track indicates that one or more sectors have headers which are not consistently formatted.	Undetermined or parts not required.
6D/109	HP-IB	POSITION ERROR. (Event). A position verify error has occurred because the physical cylinder address field of the header does not match the current target physical address.	Undetermined or parts not required.
6F/111	HP-IB	READ SERVO MESSAGE TIMEOUT. (Event; FRU = servo). A complete servo message was not received in the servo communication port after receiving a servo system interrupt.	1. Servo PCA-A1

Table 8-2. List of DERROR/TERROR's (13 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
70/112	HP-IB	WRITE SERVO MESSAGE TIMEOUT. (Event; FRU = servo). A timeout occurred while attempting to write a complete servo message to the servo system interface port.	1. Servo PCA-A1
71/113	HP-IB	ILLEGAL SERVO MESSAGE. (Event; FRU = servo). The servo message received was not recognized.	1. Servo PCA-A1
72/114	HP-IB	SERVO AMPLIFIER FAULT. (Event; FRU = servo). The servo system reported a servo amplifier fault.	1. Servo PCA-A1
73/115	HP-IB	SERVO AGC FAULT. (Event; FRU = servo). The servo system reported a sampled servo AGC fault.	1. Servo PCA-A1
74/116	HP-IB	SERVO RESETTLE TIMING ERROR. (Event; FRU = servo). The servo system reported a sampled servo timing error during resettling on track.	1. Servo PCA-A1
76/118	HP-IB	SERVO SETTLE TIMEOUT. (Event; FRU = servo). The servo system was unable to settle on track after a head switch or seek.	1. Servo PCA-A1

Table 8-2. List of DERROR/TERROR's (14 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
77/119	HP-IB	SERVO TIMING ERROR. (Event; FRU = servo). The sampled servo timing marks between sectors was outside acceptable time window.	1. Servo PCA-A1
78/120	HP-IB	SERVO SETTLE TIMING ERROR. (Event; FRU = servo). The sampled servo timing marks between sectors was outside the acceptable time window during head settling.	1. Servo PCA-A1
79/121	HP-IB	SEEK TIMEOUT (Event; FRU = servo). The requested seek took too long to complete.	1. Servo PCA-A1
7A/122	HP-IB	FAST SERVO TRACK CROSSING. (Event; FRU = servo). The heads were moving too fast at the last track crossing to settle on track correctly.	1. Servo PCA-A1
7B/123	HP-IB	SEEK BOUNDARY VIOLATION. (Event; FRU = servo). The last seek command would cause the heads to move beyond the usable boundaries of the disc media.	1. Servo PCA-A1

Table 8-2. List of DERROR/TERROR's (15 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
7D/125	HP-IB	TRACK FOLLOW IN GUARD BAND FAULT. (Event; FRU = servo). Servo was unable to track follow in the guard band area of the disc, or no guard band was detected.	1. Servo PCA-A1
7F/127	HP-IB	GUARD BAND FAULT. (Event; FRU = servo). Servo system was unable to complete guard band verification, or no guard band was detected.	1. Servo PCA-A1
80/128	HP-IB	SERVO FAULT STATUS PENDING. (Event; FRU = servo). The requested seek command was not processed because of pending servo fault status.	1. Servo PCA-A1
81/129	HP-IB	SECTOR TIMING HIGH. (Event; FRU = servo). The servo system reported the Sector Timing Mark rate exceeded the upper specified limit while track following. The read/write system was idle.	1. Servo PCA-A1
82/130	HP-IB	SECTOR TIMING LOW. (Event; FRU = servo). The servo system reported the Sector Timing Mark rate exceeded the lower specified limit while track following. The read/write system was idle.	1. Servo PCA-A1

Table 8-2. List of DERROR/TERROR's (16 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
84/132	HP-IB	SPINDLE FAULT. (Fault; FRU = servo). Disc spindle is not spinning, or not spinning at correct speed.	1. Servo PCA-A1
85/133	HP-IB	SECTOR WINDOW FAULT. (Event; FRU = servo). The sector timing counter in the controller timed out while attempting to synchronize the controller with the sector timing mark.	1. Servo PCA-A1
86/134	HP-IB	MISSING HEADER AVAILABLE. (Event; FRU = controller). The Header Available status bit in the controller was not set during a position verify.	1. Controller PCA-A6
88/136	HP-IB	DATA ERROR QUEUE FULL. (Event). The queue for the data error correction was full, preventing the start of a disc read. A rotational latency has been induced.	Undetermined or parts not required.
89/137	HP-IB	CONTROLLER COUNTER FAULT. (Event; FRU = controller). The diagnostic which tests the sector timing mark counter in the controller failed.	1. Controller PCA-A6
8C/140	HP-IB	DATA ERROR QUEUE OVERFLOW. (Event). A disc read has been shut off because the data error buffer queue has filled. A rotational latency has been induced.	Undetermined or parts not required.

Table 8-2. List of DERROR/TERROR's (17 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
8D/141	HP-IB	VERIFY FAILED. (Event). A position verification has failed due to ECC data errors.	1. Read/Write PCA-A2
8E/142	HP-IB	VERIFY FAULT. (Fault). The controller has detected a head miscompare with no ECC data errors while reading from a track on which a successful verify has already completed.	1. Controller PCA-A6
8F/143	HP-IB	CONTROLLER FAULT. (Fault; FRU = controller). The controller has detected an illegal program state or hardware condition within itself.	1. Controller PCA-A6
90/144	HP-IB	READ DMA DISC ERROR. (Event). The controller disc DMA has the disc error status bit set. No other hardware status is indicated.	Undetermined or parts not required.
91/145	HP-IB	READ ECC TIMING FAULT. (Event). During a read, the ECC circuit in the controller had the Timing Fault status bit set. No other hardware status indicated.	Undetermined or parts not required.
92/146	HP-IB	OFFTRACK WRITE. (Fault). A disc write operation has failed because of a servo offtrack error.	1. Servo PCA-A1

Table 8-2. List of DERROR/TERROR's (18 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
93/147	HP-IB	OFFTRACK READ. (Event; FRU = servo). The servo system reported an offtrack error during a disc read or a position verify.	1. Servo PCA-A1 2. HDA A3
94/148	HP-IB	OFFTRACK. (Event; FRU = servo). The servo system reported an offtrack error while the disc system was idle.	1. Servo PCA-A1 2. Spindle Motor B1
95/149	HP-IB	ILLEGAL SERVO ERROR. (Fault). The read/write system reported a servo error condition and the servo system reported no error.	1. Read/Write PCA-A2 2. Servo PCA-A1
96/150	HP-IB	READ HDA OVERCURRENT. (Event; FRU = read/write). The read/write system reported an overcurrent condition in the head amplifier circuit during a read or position verify.	1. Read/Write PCA-A2
97/151	HP-IB	WRITE DMA DISC ERROR. (Event). The controller DMA circuit has the Disc Error status set during a disc write.	Undetermined or parts not required.
98/152	HP-IB	WRITE ECC TIMING FAULT. (Fault). The controller ECC circuit has the Timing Fault status bit set during a disc write. No other hardware error status set.	1. Controller PCA-A6 2. Read/Write PCA-A2

Table 8-2. List of DERROR/TERROR's (19 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
99/153	HP-IB	HEADER MISCOMPARE FAULT. (Fault; FRU = controller). The Header Miscompare error status is set in the controller DMA. No other hardware error status is set.	1. Controller PCA-A6
9A/154	HP-IB	MISMATCHED DATA ERROR STATUS. (Fault; FRU = controller). The controller ECC circuit status and DMA circuit status indicating a detected ECC data error is inconsistent.	1. Controller PCA-A6
9B/155	HP-IB	READ DATA OVERRUN. (Event). The read/write system reported a data overrun error during a disc read or position verify.	Undetermined or parts not required.
9C/156	HP-IB	WRITE DATA OVERRUN. (Fault). The read/write system has reported a data overrun error during a disc write.	Undetermined or parts not required.
9D/157	HP-IB	PARITY DATA ERROR. (Event). The read/write system detected a parity data error in the sync field of a sector during a disc read or position verify.	Undetermined or parts not required.

Table 8-2. List of DERROR/TERROR's (20 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
9E/158	HP-IB	READ DATA UNDERRUN. (Event). The read/write system detected a data underrun error during a disc read or position verify.	Undetermined or parts not required.
9F/159	HP-IB	WRITE DATA UNDERRUN. (Fault). The read/write system detected a data underrun error during a disc write.	Undetermined or parts not required.
A0/160	HP-IB	READ/WRITE FAULT. (Fault; FRU = read/write). The read/write system has indicated an illegal fault status.	1. Read/Write PCA-A2
A2/162	HP-IB	EMINENT POWER FAIL. (Fault; FRU = power supply). The power supply indicated an impending power failure.	1.Power Supply PCA-A4
A3/163	HP-IB	READ SIGNAL FAULT. (Event; FRU = read/write). The controller circuits indicated an error during a disc read. No error is indicated by the read/write system.	1. Read/Write PCA-A2
A4/164	HP-IB	WRITE HOLD OFF (WHO). FAULT. (Fault; FRU = controller). The read/write system did not respond correctly to the controller assertion of the WHO signal.	1. Controller PCA-A6

Table 8-2. List of DERROR/TERROR's (21 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
A5/165	HP-IB	UNRECOGNIZED DISC FAULT. (Fault; FRU = controller). A disc hardware control interrupt could not be decoded.	1. Controller PCA-A6
A6/166	HP-IB	WRITE PROTECT. (Fault; FRU = controller). The controller has write protected the drive because of a previously detected fault condition.	1. Controller PCA-A6
A7/167	HP-IB	UNSUPPORTED HDA. (Fault; FRU = servo). The installed controller circuit and program firmware does not support or does not recognize this version of disc device.	1. Servo PCA-A1
A8/168	HP-IB	WRITE SIGNAL FAULT. (Fault; FRU = read/write). The controller circuit indicates a fault condition during a disc write. The read/write system indicates no fault status.	1. Read/Write PCA-A2
A9/169	HP-IB	WRITE SECTOR ADDRESS FAULT. (Fault; FRU = controller). The controller sector address counter had the wrong value during a disc write.	1. Controller PCA-A6

Table 8-2. List of DERROR/TERROR's (22 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
AA/170	HP-IB	COMMAND ABORT FAULT. (Fault; FRU = read/write). A discrepancy exists in the correct status for assertion of the Write Hold Off (WHO) signal between the controller and read/write system.	1. Read/Write PCA-A2
AB/171	HP-IB	SERVO OFFTRACK. (Event; FRU = servo). The servo system was offtrack after a system clear, or was unable to resettle on track after a previous servo error condition.	1. Servo PCA-A1
AC/172	HP-IB	ILLEGAL SERVO COMMAND. (Event; FRU = servo). The servo system did not recognize the last servo command issued by the controller.	1. Servo PCA-A1
AD/173	HP-IB	SERVO/CONTROLLER INTERFACE FAULT. (Event; FRU = servo). The servo system did not recognize the last servo command issued by the controller.	1. Servo PCA-A1
AE/174	HP-IB	WRITE SERVO TIMING ERROR. (Fault; FRU = servo). The servo system reported a sampled servo timing error during a disc write.	1. Servo PCA-A1 2. HDA A3

Table 8-2. List of DERROR/TERROR's (23 of 25)

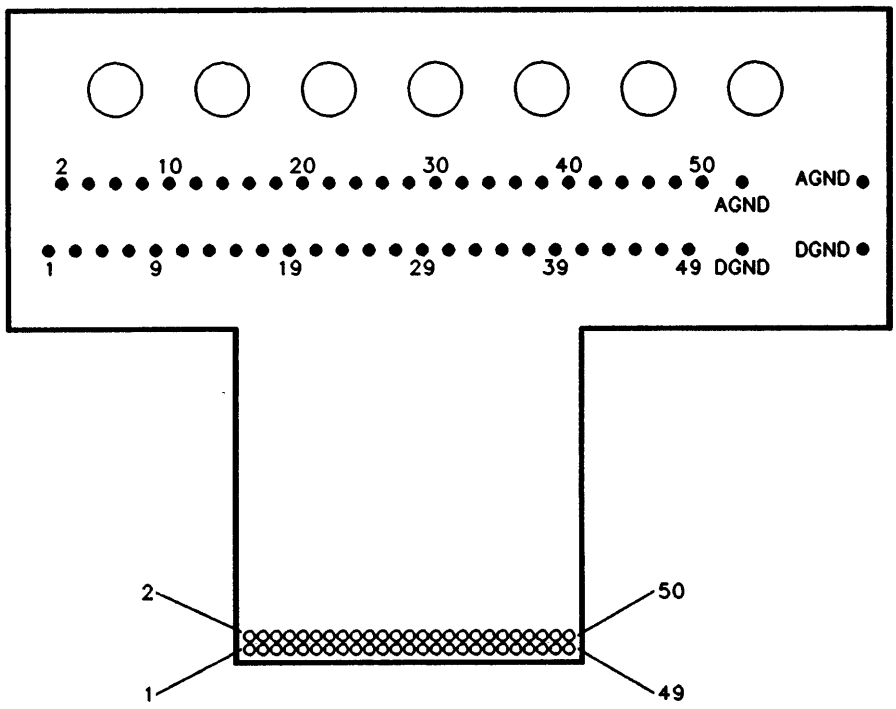
NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
AF/175	HP-IB	READ SERVO TIMING ERROR. (Event; FRU = servo). Servo timing error occurred during disc read or verify.	1. Servo PCA-A1
B0/176	HP-IB	SERVO COMMAND CANCELED. (Event). The controller has canceled the last servo command and will ignore its completion status.	None
B1/177	HP-IB	SERVO RECALIBRATION REQUIRED. (Event). The servo system requires calibration prior to accessing the disc.	None
B2/178	HP-IB	DATA ERROR OVERFLOW MISMATCH. (Fault; FRU = controller). The DMA and ECC circuits of the controller have mismatched data error overflow status.	1. Controller PCA-A6
B3/179	HP-IB	WRITE HDA OVERCURRENT. (Fault; FRU = read/write). The read/write system detected an overcurrent condition in the head amplifier circuit of the HDA during a disc write.	1. Read/Write PCA-A2

Table 8-2. List of DERROR/TERROR's (24 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
B5/181	HP-IB	READ SECTOR ADDRESS FAULT. (Fault; FRU = controller). The controller sector address counter had the wrong value during a disc read.	1. Controller PCA-A6
B7/183	HP-IB	READ DMA BUFFER POINTER FAULT. (Fault; FRU = controller). The controller DMA RAM address pointer had the wrong value at completion of a segment of a disc read.	1. Controller PCA-A6
B8/184	HP-IB	WRITE DMA BUFFER POINTER FAULT. (Fault; FRU = controller). The controller DMA RAM address pointer had the wrong value at completion of a segment of a disc write.	1. Controller PCA-A6
B9/185	HP-IB	SAMPLED SERVO GATE (SSG). TIMING ERROR. (Event; FRU = servo). Sampled servo gate timing was outside specified limits during servo recalibration.	1. Servo PCA-A1
BA/186	HP-IB	BAD SERVO MEASURE STATUS. (Event; FRU = servo). Servo status was bad at start of seek. Position measurement for seek not done.	1. Servo PCA-A1

Table 8-2. List of DERROR/TERROR's (25 of 25)

NUMBER (hex/dec)	INTER-FACE	ERROR DESCRIPTION	SUSPECT ASSEMBLY
BB/187	HP-IB	MISSING FIRST SERVO RACK CROSSING. (Event; FRU = servo). First servo track crossing was not detected during seek.	1. Servo PCA-A1
BC/188	HP-IB	SERVO TRACK 0 MISSING. (Event; FRU = servo). Servo information at track 0 not detected during recalibration.	1. Servo PCA-A1
BD/189	HP-IB	TRACK 0 LSB INCORRECT. (Event; FRU = servo). Servo could not verify positioning at track 0 during recalibration.	1. Servo PCA-A1
DO/208	HP-IB	ERROR CORRECTION HEADER MISCOMPARE. (Fault; FRU = controller). After successful data error correction, the header field read from the disc did not match the target header.	1. Controller PCA-A6



TEST PCA PIN ASSIGNMENTS:

PIN	SIGNAL	PIN	SIGNAL
1	SSRVPT	26	GAP-L
2	DEMOD-L	27	VCOV
3	TEST1	28	PHDET
4	ACUR	29	SRVER-L
5	TERI-L	30	-12UF
6	EXT-INPUT	31	OTEN-H
7	IDB	32	AMPFLT-L
8	SEEK CC	33	TFOUT
9	DLVL	34	SSGT-L
10	ERRSIG	35	TER2
11	TF-INPUT	36	DTO-L
12	PWM-L	37	SPOS
13	DSRVPT	38	TCRS/S
14	SMDT-H	39	TESTEN-L
15	AGND	40	AGCF-L
16	ZDT	41	ABORT
17	SLPES	42	GBDEN-H
18	DGND	43	SAGC
19	+12UF	44	FSEN-L
20	+5V	45	OFTU-L
21	PES	46	DAGC
22	AMFU-H	47	DPOS
23	OPOS	48	INDEX-H
24	DC OFST	49	SRTF-H
25	SLVL	50	TRKCR-H

S7937A72

Figure 8-4. Servo System Test Point PCA

Table 8-3. Servo System Test Connector A1J3, Mnemonics (1 of 4)

PIN NO.	MNEMONIC	SIGNAL	DESCRIPTION
1	SSRVPT	Sampled Servo, Positive, Test	Amplified sampled servo code A and B dibits.
2	DEMOD-L	Sampled Servo Demodulation Pulse	A versus B pulse clock (Write clock divided by 24).
3	TEST1	Test 1	High input disables transistor enable; low input enables transistor enable. CAUTION: Can damage actuator/servo PCA-A1 if other faults exist.
4	ACUR	Actuator Current	Voltage indication of current flow through the actuator. Scale is 0.5A/volt.
5	TER1-L	Timing Error 1	Overall timing error caused by SOS-L gap not occurring at a designated time.
6	EXT INPUT	External Input	Used to increase/decrease level to triangle wave comparator. CAUTION: If this level is too high/low, it can pin the actuator to a crash stop and cause HDA damage.
7	IDB	Integrated Dibits	Dibits which are integrated.
8	SEEK CC	Seek Current Control	Test point for examining output of negative and positive acceleration pulses, integrated. Does not include external input or internal feedback.
9	DLVL	Dedicated Level	Sum of dedicated servo code A & B dibits. Used for dedicated AGC.
10	ERRSIG	Error Signal	Test point for looking at level into amplifier drive triangle wave comparator. CAUTION: Not an input - can cause fuse/FET damage on servo PCA-A1.
11	TF INPUT	Transfer Function Input	Test point where an external noise source can be connected in order to measure the transfer function of the servo system.

Table 8-3. Servo System Test Connector A1J3, Mnemonics (2 of 4)

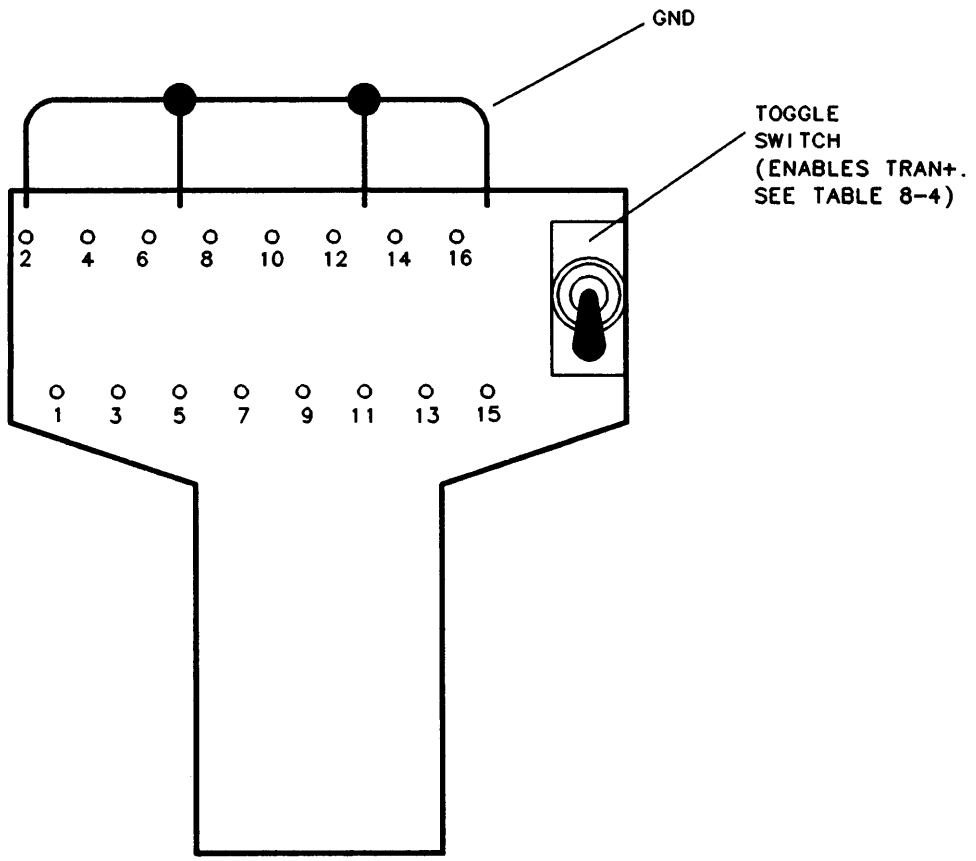
PIN NO.	MNEMONIC	SIGNAL	DESCRIPTION
12	PWM-L	Pulse Width Modulation	Digital signal which shows the duty cycle of the switching transistors.
13	DSRVPT	Dedicated Servo, Positive, Test	Amplified signal from dedicated servo head.
14	SMDT-H	Sector Mark Detect	Asserted by the servo system when the dedicated servo code sector mark pattern is detected.
15	AGND	Analog Ground	Analog Ground
16	ZDT	Zero Detection	Changes state when missing dibits in the sector mark or guard band mark are detected.
17	SLPES	Slew Position Error Signal	When track following, system switches to slew PES to be less sensitive to changes in position glitches.
18	DGND	Digital Ground	Digital Ground
19	+12UF	+12 Vdc, Unfiltered	+12 Vdc power supply output, before PI filters.
20	+5V	+5 Vdc, Unfiltered	+5 Vdc power supply output, before PI filters.
21	PES	Position Error Signal	Either the dedicated or sampled position signal, depending on whether the system is presently in the dedicated or sampled mode of operation.
22	AMFU-H	Amplifier Unlatched	Asserted when the actuator power amp is disabled because of a fault.
23	OPOS	Offset Position Error Signal	PES signal plus any external DC offset added to it. Also includes any transfer function input.

Table 8-3. Servo System Test Connector A1J3, Mnemonics (3 of 4)

PIN NO.	MNEMONIC	SIGNAL	DESCRIPTION
24	DC OFST	DC Offset	An external signal can be introduced at this point to provide a dc offset to signal PES during track following, to be able to read/write with no offset.
25	SLVL	Sampled Level	Addition of A sampled dibits and B sampled dibits used for sampled servo AGC.
26	GAP-L	Sector Gap	Complete window for entire sampled servo code.
27	VCOV	VCO Voltage	Integrated sum of all positive dedicated servo peaks to control VCO, which creates read clock.
28	PHDET	Phase Detection	Dedicated servo positive, scaled for input to VCO integrator.
29	SRVER-L	Servo Error	Combination of off-track or timing error 1 and 2.
30	-12UF	-12 Vdc, Unfiltered	-12 Vdc output of power supply before the PI filters.
31	OTEN-H	Off Track Enable	Tie this point low to disable off-track faults. CAUTION: This means that writing may occur off track without the disc drive stopping.
32	AMPFLT-L	Amplifier Fault	This signal goes low if an over velocity, under voltage, missing 100 KHz clock, or SPR-L is detected. This will shut off amplifier enable.
33	TFOUT	Transfer Function	Output signal used when measuring the transfer function of the servo system.
34	SSGT-L	Sampled Servo Gate	Window of A dibits and B dibits of sampled servo code.
35	TER2	Timing Error 2	Monitors sync bit to make sure that it falls within a specified window and is followed by a specified gap.

Table 8-3. Servo System Test Connector A1J3, Mnemonics (4 of 4)

PIN NO.	MNEMONIC	SIGNAL	DESCRIPTION
36	DTO-L	Dedicated Timing Only	Tie low to servo from dedicated surface only. Used to measure runout and skew.
37	SPOS	Sampled Position	Sampled B dibits minus sampled A dibits to give sampled track following.
38	TRCS/S	Track Crossing	Track crossing divided by 5 when seeking fast; track crossing when seeking slow.
39	TESTEN-L	Diagnostic Mode Enable	Comes from diagnostic mode switch at rear of drive. See chapter 3 for details.
40	AGCF-L	AGC Fault	Active when sampled AGC level falls too far below or above a reference.
41	ABORT	Abort	Output for test only.
42	GBDEN-H	Guard Band Enable	Switches between guard band detection and sector mark detection.
43	SAGC	Sampled AGC	Clocked and integrated SLVL used for AGC of sampled servo.
44	FSEN-L	Fine Servo Enable	Output of servo controller indicating that the servo system is in fine servo (track following) mode.
45	OFTU-L	Off Track Unlatched	Goes low when offtrack, and high when ontrack.
46	DAGC	Dedicated AGC	Clocked and integrated DLVL used for AGC of dedicated servo.
47	DPOS	Dedicated Position	Dedicated A bits minus dedicated B bits.
48	INDEX-H	Index	Indicates that the Index mark has been detected. Index is two sector marks occurring during one sector.
49	SRTF-H	Servo Timing Fault	Combination of TER1-L and TER2-L.
50	TRKCR-H	Track Crossing	Goes high when crossing a dedicated track.



TEST PCA PIN ASSIGNMENTS:

PIN	SIGNAL	PIN	SIGNAL
1	BIT8	9	TRAN+
2	FRAME	10	WGTO-L
3	RDGT-H	11	RDEN-H
4	DATAEN	12	WDATA-H
5	AGND	13	SOS-L
6	DPIRQ-L	14	DMARG
7	-5.2	15	DQAL-L
8	FIL	16	DGND

S7937A73

Figure 8-5. Read/Write Test Point PCA

Table 8-4. Read/Write System Test Fixture, Mnemonics (1 of 2)

PIN NO.	MNEMONIC	SIGNAL	DESCRIPTION
1	BIT 8	Bit 8	A count during a sector. A convenient trigger for viewing other read/write wave forms.
2	FRAME	Frame	Bit word in sync field to begin start of header. Only looked for approximately half-way through sync field. Triggered by sector read.
3	RDGT-H	Read Gate	Internal to read/write controller. Not used.
4	DATAEN	Data Enable	Frame asserts data enable (header included). This is the first sync bit out of the read/write controller.
5	AGND	Analog Ground	Analog ground
6	DPIRQ-L	Data Proc Interrupt Request	Read/write controller has received fault condition, for example write holdoff. For development only.
7	-5.2V	-5.2V	-5.2V
8	FIL	Fault Ignore	Read/write controller will ignore all fault conditions. CAUTION: allows writing in the sampled servo area.
9	TRAN+	Read Transition	Rises each time a flux reversal is detected in the read/write path. The toggle switch on the test PCA must be set to the ON position to monitor this signal.
10	WGTO-L	Write Gate Output	Active when a write operation is occurring. Gates write current to the data heads.
11	RDEN-H	Read Enable	Tells PLL to lock onto data instead of WC.
12	WDATA-H	Write	The actual data being written to the heads. (Leading edge creates flux reversal.) Signal is not precompensated.
13	SOS-L	Start of Sector	Alerts the read/write controller to begin a read or write.

Table 8-4. Read/Write System Test Fixture, Mnemonics (2 of 2)

PIN NO.	MNEMONIC	SIGNAL	DESCRIPTION
14	DMARG	Decrease Margin	Decreases timing margin to read path. An input to the read/write PCA used to test margins. +10V gives no reading to good reading range. For safety, do not exceed +/- 10V
15	DQUALL-L	Dequalification Low	Decreases amplitude qualification duty cycle. Normal = 72% in system field. Not used at this time except for factory testing. Grounding produces more errors. Small defects become "large".
16	DGND	Digital Ground	Digital ground

Replaceable Parts 9

9-1. INTRODUCTION

This chapter contains listings of all field-replaceable parts and illustrated parts breakdowns for the drive, HP 19511A Cabinet, and HP 19512A Rack Slide Kit. Parts lists for recommended electronic and mechanical spares kits for the drive are also provided.

Replaceable parts for the drive are listed in order of disassembly in table 9-1 and illustrated in figure 9-1. Replaceable parts for the cabinet and rack slide kit are similarly documented in tables 9-2, 9-3 and figures 9-2, 9-3. In each listing, attaching parts are listed immediately after the item they attach. Items in the DESCRIPTION column are indented to indicate their relationship to the next higher assembly. In addition, the symbol "- - - x - - -" follows the last attaching part for the item. Identification of the items and the labels is as follows:

Major Assembly
*Replaceable Assembly
*Attaching Part for Replacement Assembly
**Subassembly or Component Part
**Attaching Part for Subassembly or Component Part
***Sub-subassembly or Component Part
***Attaching Parts for Sub-subassembly or Component Part

The replaceable parts listings provide the following information for each part:

a. FIG & INDEX NO. The figure and index number which indicates where the replaceable part is illustrated.

b. HP PART NO. The Hewlett-Packard number for each replaceable part.

c. DESCRIPTION. The description of each replaceable part. (Refer to table 9-5 for an explanation of the abbreviations used the DESCRIPTION column.)

d. MFR CODE. The 5-digit code that denotes a typical manufacturer of a part. Refer to table 9-6 for a listing of manufacturers that corresponds to the codes.

e. MFR PART NO. The manufacturer's part number for each replaceable part.

f. UNITS PER ASSEMBLY. The total quantity of each part used in the major assembly.

g. The MFR CODE and MFR PART NO. for common hardware are listed as 00000 and OBD (order by description), respectively, because these items can usually be purchased locally.

NOTE

TORX® hardware is used in the assembly of the drive. This hardware requires the use of special drivers. In this manual, any reference to this type of hardware will be accompanied by the required driver size (for example, "T15").

9-2. ORDERING INFORMATION

To order replaceable parts for the drive, cabinet, and rack slide kit, address the order to your local Hewlett-Packard Sales and Support Office. For the address of the nearest HP Sales and Support Office, contact a Hewlett-Packard Headquarters Office. Headquarters Offices are listed at the rear of this manual. Specify the following information in each order:

a. Model number and full serial number.

b. Complete Hewlett-Packard part number.

c. Complete description of each part, as provided

TORX is a registered trademark of the Camcar Division of Textron, Inc.

in the replaceable parts listing.

9-3. SERVICE KIT CONTENTS

Certain items are recommended for field service inventory and for product support of the drive. The field stocking inventory should consist of the following:

07937-60202	Power Supply PCA-A4
07936-69001	Exchange Head-Disc Assembly A3
07937-60038	Speed Sense Cable Assembly W5
07937-60061	Power Distribution PCA-A5
07937-60064	Power Jumper Cable Assembly W6
07937-60065	Signal Jumper Cable Assembly W7
07937-60068	HDA Cable Assembly W8
07937-60074	Line Filter Assembly FL1
07937-60099	Ground Spring Assembly
07937-60140	Primary Power PCA-A8
07937-60150	LED PCA-A7
07937-60163	Power Supply Output Cable Assembly W4
07937-60164	Power Supply Input Cable Assembly W3
07937-60051	Motor Assembly (B1)
07937-60173	Primary Power Cable Assembly W1
07937-80033	Drive Belt, 60 Hz
07937-80034	Drive Belt, 50 Hz
07937-10104	EPROM Kit, HP-IB
07937-10201	EPROM Kit, HP-IB W/Cache
07937-69001	Exchange Head-Disc Assembly A3
07937-69018	Exchange Servo PCA-A1
07937-69035	Exchange Controller PCA-A6, HP-IB
07937-69037	Exchange Controller PCA-A6, HP-IB Cache
07937-69073	Exchange R/W PCA-A2

The following support items should also be stocked:

5955-3462	CS/80 External Exerciser Reference Manual
07937-90903	Hardware Support Manual
07937-90905	CE Handbook
5010-0566	Tape 1, External Exerciser
5010-0567	Tape 2, External Exerciser

Table 9-1. Disc Drive, Replaceable Parts

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
9-1-					
	7936H	DISC DRIVE, HP-IB	28480	7936H	REF
	7937H	DISC DRIVE, HP-IB	28480	7937H	REF
	7936XP	DISC DRIVE, HP-IB CACHE	28480	7936XP	REF
	7937XP	DISC DRIVE, HP-IB CACHE	28480	7937XP	REF
1	07937-00110	* COVER, rear	28480	07937-00110	1
		(Attaching Parts)			
2	0515-0380	* SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	4
		- - - X - - -			
3	07937-60212	* HP-IB ASSEMBLY	28480	07937-60212	1
		(Attaching Parts)			
4	0515-0380	* SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	2
		- - - x - - -			
5	07937-60064	* CABLE ASSEMBLY, power jumper (W6)	28480	07937-60064	1
6	07937-60065	* CABLE ASSEMBLY, signal jumper (W7)	28480	07937-60065	1
7	07937-60068	* CABLE ASSEMBLY, HDA (W8)	28480	07937-60068	1
8	0515-0665	* SCREW, machine, pnh, T10, M3.0 by 0.5, 14 mm long, w/scw	00000	OBD	4
9	07937-60035	* HP-IB CONTROLLER PCA (PCA-A6) (7936H, 7937H only)	28480	07937-60035	1
	07937-60137	* HP-IB CACHE CONTROLLER (PCA-A6) (7936XP, 7937XP only)	28480	07937-60137	REF
10	07937-10104	** EPROM KIT (7936H, 7937H only)	28480	07937-10104	1
	07937-10201	** EPROM KIT (7936XP, 7937XP only)	28480	07937-10201	REF
11	07937-60018	* SERVO PCA (PCA-A1)	28480	07937-60018	1
12	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	1
13	07937-00055	* GROUND ASSEMBLY, R/W	28480	07937-00055	1
14	0515-0665	* SCREW, machine, pnh, T10, M3.0 by 0.5, 14 mm long, w/scw	00000	OBD	4
15	07937-00107	* PCA SHIELD	28480	07937-00107	1
16	07937-60073	* READ/WRITE PCA (PCA-A2)	28480	07937-60073	1
17	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	2
18	07937-00079	* LABEL, power, 240/220/208/200V, 50/60 Hz	28480	07937-00079	1
19	07937-00080	* LABEL, power, 120/100V, 50/60 Hz	28480	07937-00080	1
20	0515-0380	* SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	4
21	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	4
22	07937-00088	* PANEL ASSEMBLY, rear	28480	07937-00088	1
23	0515-0380	* SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	5

Table 9-1. Disc Drive, Replaceable Parts (continued)

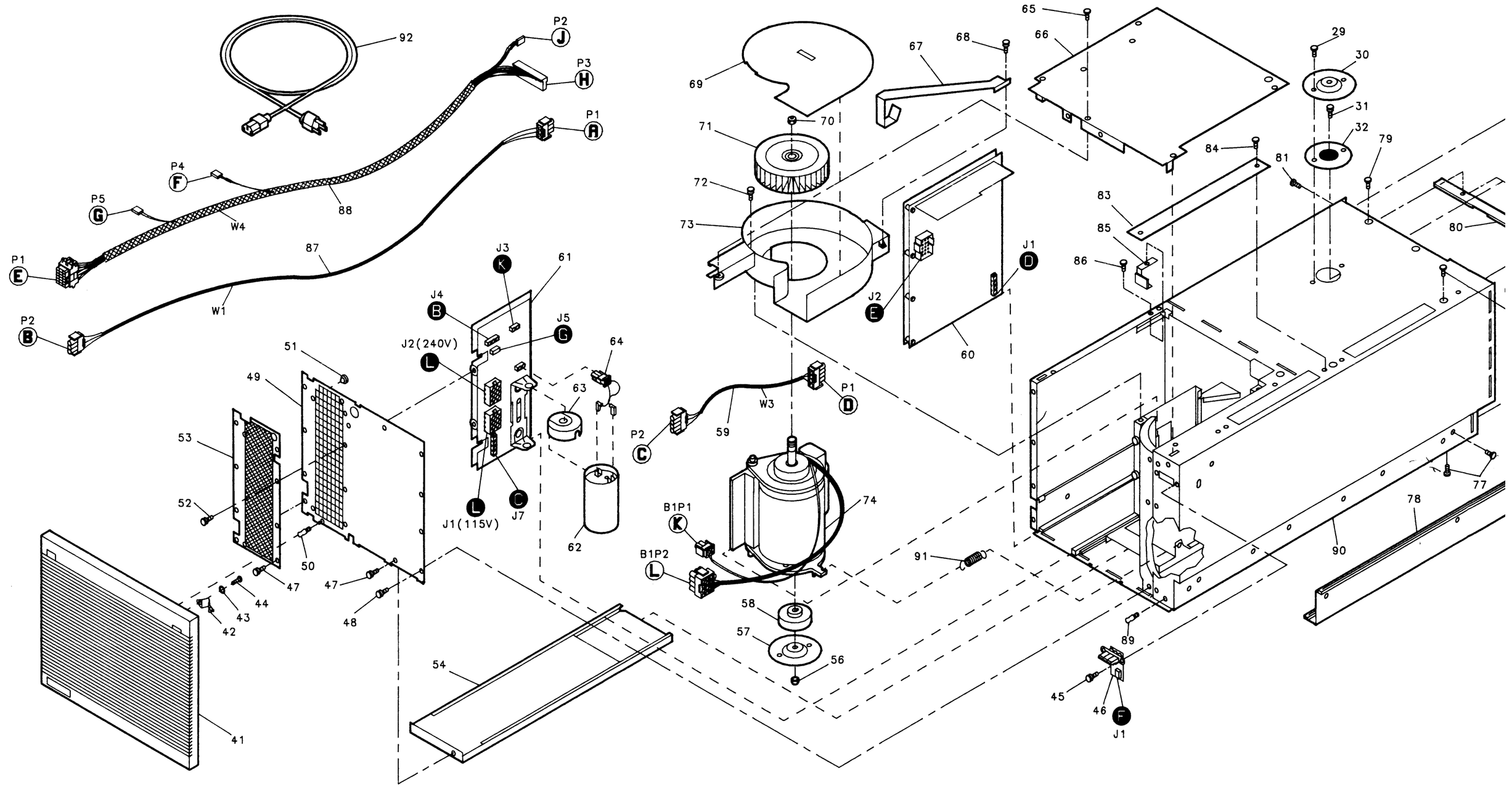
FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
24	07937-60175	** LINE FILTER ASSEMBLY (FL1)	28480	07937-60175	1
25	2110-0565	***CAP, fuse	28480	2110-0565	1
26	2110-0030	***FUSE, 5A, SB	75915	313005	1
27	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	4
28	07937-60061	* POWER DISTRIBUTION ASSEMBLY (PCA-A5)	28480	07937-60061	1
29	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	2
30	07937-00058	* GUARD, belt	28480	07937-00058	1
31	0515-0433	* SCREW, machine, pnh, T15, M4.0 by 0.7, 8 mm long, w/scw	00000	OBD	1
32	07937-80125	* SHOCK MOUNT	28480	07937-80125	1
33	0515-0380	* SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	2
34	07937-60038	* CABLE ASSEMBLY, speed sense (W5)	28480	07937-60038	1
35	07936-60001	* HEAD-DISC ASSEMBLY, (A3) (7936 only)	28480	07936-60001	1
	07937-60001	* HEAD-DISC ASSEMBLY (A3) (7937 only)	28480	07937-60001	REF
36	07937-20113	** SPRING	28480	07937-20113	1
37	0510-0083	** CLIP, retaining	00000	OBD	2
38	07937-40110	** BUTTON	28480	07937-40110	1
39	0515-0380	** SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	2
40	07937-60099	** GROUND SPRING ASSEMBLY, spindle	28480	07937-60099	1
41	07937-60027	* FRONT PANEL ASSEMBLY	28480	07937-60027	1
42	1390-0675	** RECEIVER, stud, snap-in (Attaching Parts)	28480	1390-0675	4
43	2190-0584	** WASHER, lock, helical, 3.0 mm	00000	OBD	2
44	0624-0629	** SCREW, tapping, pnh, pozi, 3-24, 0.250 in. long	00000	OBD	2
		- - - X - - -			
45	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	2
46	07937-60150	* LED DISPLAY ASSEMBLY (PCA-A7)	28480	07937-60150	1
47	0515-0380	* SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	11
48	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	2
49	07937-00085	* COVER ASSEMBLY, top	28480	07937-00085	1
50	1390-0740	** STUD, snap-in	28480	1390-0740	2
51	0403-0086	** BUMPER, rubber	00000	0403-0086	1
52	0515-0380	* SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	2
53	07937-80181	* PREFILTER	28480	07937-80181	1
54	07937-60184	* COVER, belt	28480	07937-60184	1
55	07937-80033	* BELT, 60 Hz	28480	07937-80033	1
	07937-80034	* BELT, drive, 50 Hz	28480	07937-80034	REF

Table 9-1. Disc Drive, Replaceable Parts (continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
56	0590-1395	* NUT, hex, 5/16-18, 1/2 in., plastic locking	00000	OBD	1
57	07937-00058	* GUARD, belt	28480	07937-00058	1
58	07937-20005	* PULLEY, 60 Hz	28480	07937-20005	1
	07937-20006	* PULLEY, 50 Hz	28480	07937-20006	REF
59	07937-60164	* CABLE ASSEMBLY, power supply input (W3)	28480	07937-60164	1
60	07937-60202	* POWER SUPPLY ASSEMBLY (PCA-A4)	28480	07937-60202	1
61	07937-60140	* PRIMARY POWER PCA (PCA-A8)	28480	07937-60140	1
62	0180-3762	** CAPACITOR, 39.5 uF, +/-8.9%, 330 WVAC	28480	0180-3762	1
63	1400-1396	** CAP, capacitor	28480	1400-1396	1
64	07937-60170	** WIRE ASSEMBLY	28480	07937-60170	1
65	0515-0369	* SCREW, machine, 90-deg fh, T9, M3.0 by 0.5, 6 mm long	00000	OBD	5
66	07937-00086	* COVER ASSEMBLY, top	28480	07937-00086	1
67	07937-00105	* CLIP, fan scroll cover	28480	07937-00105	1
		(Attaching Parts)			
68	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	1
		- - - X - - -			
69	07937-00078	* COVER, fan scroll	28480	07937-00078	1
70	0590-1395	* NUT, hex, 5/16-18, 1/2 in., plastic locking	00000	OBD	1
71	3160-0480	* ROTOR, fan	28480	3160-0480	1
72	0515-0372	* SCREW, machine, pnh, T10, M3.0 by 0.5, 8 mm long, w/scw	00000	OBD	2
73	07937-40152	* SCROLL, fan	28480	07937-40152	1
74	07937-60051	* MOTOR ASSEMBLY (B1)	28480	07937-60051	1
75	0515-0369	* SCREW, machine, 90-deg fh, T9, M3.0 by 0.5, 6 mm long	00000	OBD	3
76	07937-40075	* PCA GUIDE, upper	28480	07937-40075	1
77	0515-0369	* SCREW, machine, 90-deg fh, T9, M3.0 by 0.5, 6 mm long	00000	OBD	4
78	07937-40072	* PCA GUIDE, lower	28480	07937-40072	1
79	0515-0369	* SCREW, machine, 90-deg fh, T9, M3.0 by 0.5, 6 mm long	00000	OBD	2
80	07937-20105	* BLOCK, HDA	28480	07937-20105	1
81	0515-0369	* SCREW, machine, 90-deg fh, T9, M3.0 by 0.5, 6 mm long	00000	OBD	2
82	07937-20126	* BLOCK, HDA, side	28480	07937-20126	1
83	07937-00013	* COVER, access	28480	07937-00013	2
		(Attaching Parts)			
84	0515-0369	* SCREW, machine, 90-deg fh, T9, M3.0 by 0.5, 6 mm long	00000	OBD	2
		- - - X - - -			

Table 9-1. Disc Drive, Replaceable Parts (continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
85	07937-60082	* STOP, power supply	28480	07937-60082	1
		(Attaching Parts)			
86	0515-0369	* SCREW, machine, 90-deg fh, T9, M3.0 by 0.5, 6 mm long	00000	OBD	2
		- - - X - - -			
87	07937-60173	* CABLE ASSEMBLY, primary power (W1)	28480	07937-60173	1
88	07937-60163	* CABLE ASSEMBLY, PWR SUPPLY OUTPUT (W4)	28480	07937-60163	1
89	1390-0740	* STUD, snap-in	28480	1390-0740	2
90	07937-60149	* ENCLOSURE ASEMBLY	28480	07937-60149	1
91	1460-2109	** SPRING, belt	28480	1460-2109	1
92	8120-1378	* POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-1378	1
	8120-0698	* POWER CORD ASSEMBLY, NEMA5A/CEE	28480	8120-0698	REF
	8120-1351	* POWER CORD ASSEMBLY, BS 1363/CEE	28480	8120-1351	REF
	8120-1369	* POWER CORD ASSEMBLY, ASC 112/CEE	28480	8120-1369	REF
	8120-1689	* POWER CORD ASSEMBLY, GMBH/CEE	28480	8120-1689	REF
	8120-1860	* POWER CORD ASSEMBLY, CEE/CEE	28480	8120-1860	REF
	8120-2104	* POWER CORD ASSEMBLY, SEV/CEE	28480	8120-2104	REF
	8120-2956	* POWER CORD ASSEMBLY, MDPP/CEE	28480	8120-2956	REF
	8120-4211	* POWER CORD ASSEMBLY, SABS/CEE	28480	8120-4211	REF
93	8120-3445	* HP-IB CABLE ASSEMBLY, 1m, (Model 10833A)	28480	8120-3445	1
94	07937-80170	* LABEL, address switch/LED display	28480	07937-80170	1


92
P2
J
P3
H
P1
A
P4
F
P5
G
W4
88
87
P1
E
W1
P2
B
J3
K
61
J4
B
J5
G
J2(240V)
L
64
51
49
63
53
52
J1(115V)
L
J7
C
62
50
47
47
44
43
42
48
41
54
69
70
71
72
73
67
68
65
66
29
30
31
32
79
84
81
83
85
86
80
J1
D
J2
E
60
P1
D
W3
59
P2
C
74
B1P1
K
B1P2
L
58
57
56
91
78
90
77
89
45
46
F
J1

S7937A71

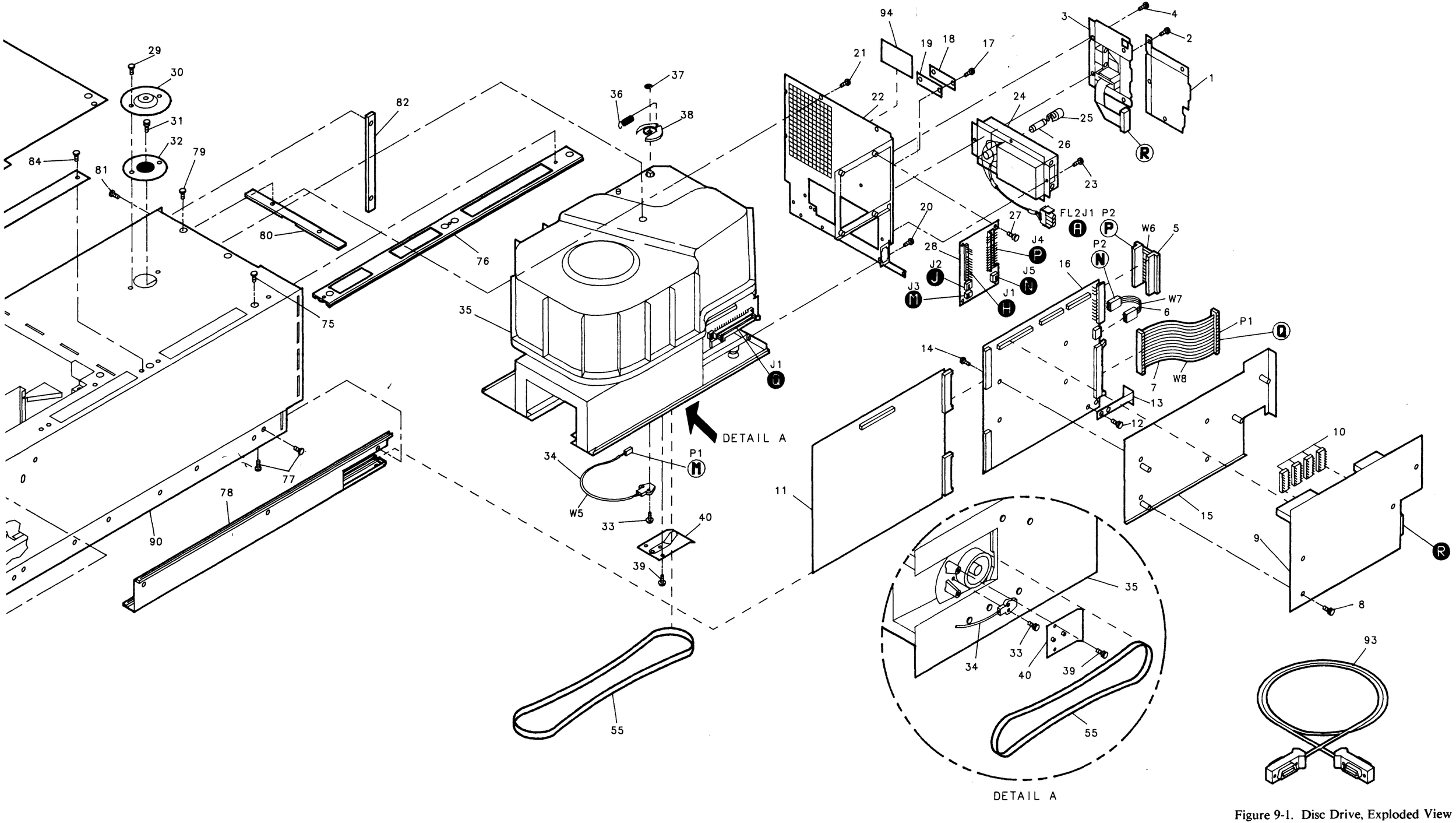


Figure 9-1. Disc Drive, Exploded View

Table 9-2. HP 19511A Cabinet, Replaceable Parts

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
9-2-					
	19511A	CABINET	28480	19511A	REF
1	5061-3136	* PANEL ASSEMBLY, top	28480	5061-3136	1
2	1390-0573	** STUD, ball	28480	1390-0573	2
3	3050-0407	** WASHER, flat, no. 6	00000	OBD	2
4	5061-3137	* PANEL ASSEMBLY, side	28480	5061-3137	2
5	19511-60001	* PANEL ASSEMBLY, rear	28480	19511-60001	1
6	1390-0573	** STUD, ball	28480	1390-0573	2
7	2190-0581	** WASHER, lock, helical, no. 6	00000	OBD	2
8	0400-0248	** GROMMET, U-channel, length 355 mm	28480	0400-0248	1
9	19511-60007	* ANTI-TIP FOOT ASSEMBLY, right	28480	19511-60007	1
		(Attaching Parts)			
10	0515-1726	* SCREW, cap, slotted, M6 by 1.0, 14 mm long	28480	0515-1726	2
		- - - X - - -			
11	0403-0484	** PAD, leveling	28480	0403-0484	1
12	19511-60002	* ANTI-TIP FOOT ASSEMBLY, left	28480	19511-60002	1
		(Attaching Parts)			
13	0515-1726	* SCREW, cap, slotted, M6 by 1.0, 14 mm long	28480	0515-1726	2
		- - - X - - -			
14	0403-0484	** PAD, leveling	28480	0403-0484	1
15	5061-3139	* TRIM PANEL ASSEMBLY	28480	5061-3139	1
16	0515-0390	* SCREW, machine, pnh, T15, M4.0 by 0.7 6 mm long, w/scw	00000	OBD	8
17	19511-00005	* CLAMP	28480	19511-00005	4
18	19511-00006	* BAR, locking	28480	19511-00006	2
19	19511-20002	* PIN, locking	28480	19511-20002	4
20	19511-20003	* NUT, locking	28480	19511-20003	4
21	0403-0419	* LEVELING PAD	28480	0403-0419	4
22	1492-0112	* CASTER	28480	1492-0112	4
		(Attaching Parts)			
23	0535-0096	* NUT, hex, M8 by 1.25, 13 mm	00000	0535-0096	4
24	0515-0238	* SCREW, machine, M8 by 1.25, 16 mm long	00000	OBD	4
		- - - X - - -			
25	0541-1307	* PANEL, filler	28480	0541-1307	11
	07937-80114	* RACK SLIDE PAIR	28480	07937-80114	1
26	07937-80098	** RACK SLIDE, right	28480	07937-80098	1
		(Attaching Parts)			
27	0515-1745	* SCREW, machine, pnh, T15, M4.05 by 0.7, 6 mm long, w/scw	00000	OBD	2
		- - - X - - -			
28	07937-80083	** RACK SLIDE, left	28480	07937-80083	1
		(Attaching Parts)			
29	0515-1745	* SCREW, machine, pnh, T15, M4.05 by 0.7, 6 mm long, w/scw	00000	OBD	2
		- - - X - - -			
30	19511-60003	* FRAME ASSEMBLY	28480	19511-60003	1

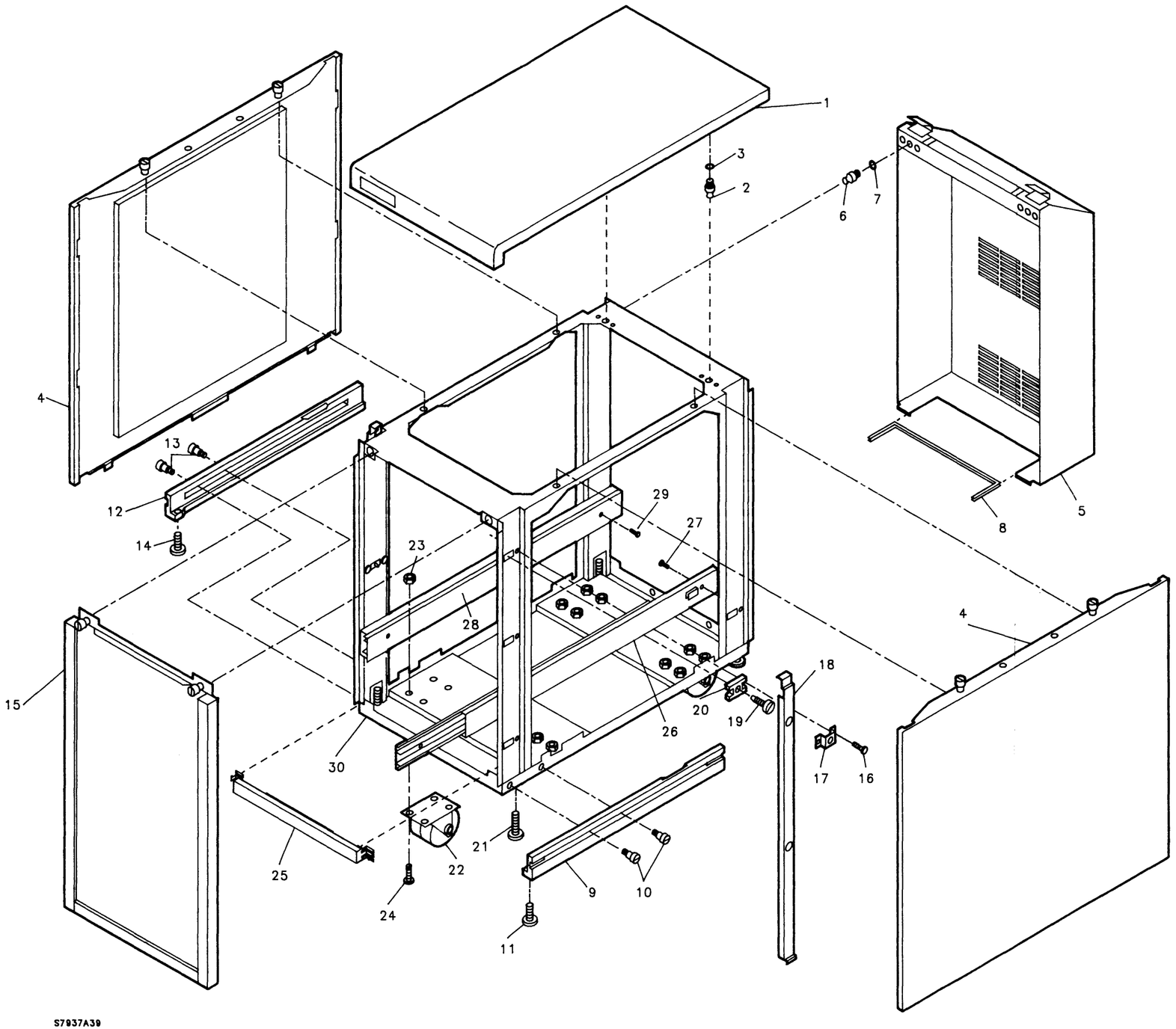


Figure 9-2. HP 19511A Cabinet, Exploded View

Table 9-3. HP 19512A Rack Slide Kit, Replaceable Parts

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
9-3-					
	19512A	RACK SLIDE KIT	28480	19512A	REF
1	19512-00001	* EIA RACK ADAPTER	28480	19512-00001	2
		(Attaching Parts)			
2	0590-0804	* NUT, sheetmetal, 10-32	00000	OBD	4
3	2680-0278	* SCREW, machine, pnh, T25, 10-32, 0.5 in. long, w/scw	00000	OBD	4
		- - - X - - -			
4	19512-00002	* RETAINER	28480	19512-00002	2
		(Attaching Parts)			
5	0515-0380	* SCREW, machine, pnh, T15, M4.0 by 0.7, 10 mm long, w/scw	00000	OBD	2
		- - - X - - -			
	07937-80114	* RACK SLIDE PAIR	28480	07937-80114	1
6	07937-80083	** RACK SLIDE, left	28480	07937-80083	1
		(Attaching Parts)			
7	0515-1745	* SCREW, machine, pnh, T15, M4.05 by 0.7, 6 mm long, w/scw	00000	OBD	2
		- - - X - - -			
8	07937-80098	** RACK SLIDE, right	28480	07937-80098	1
		(Attaching Parts)			
9	0515-1745	* SCREW, machine, pnh, T15, M4.05 by 0.7, 6 mm long, w/scw	00000	OBD	2
		- - - x - - -			
10	19512-00003	* TRIM PANEL	28480	19512-00003	1
		(Attaching Parts)			
11	0590-0804	* NUT, sheetmetal, 10-32	00000	OBD	4
12	2680-0278	* SCREW, machine, pnh, T25, 10-32, 0.5 in. long, w/scw	00000	OBD	4
		- - - x - - -			

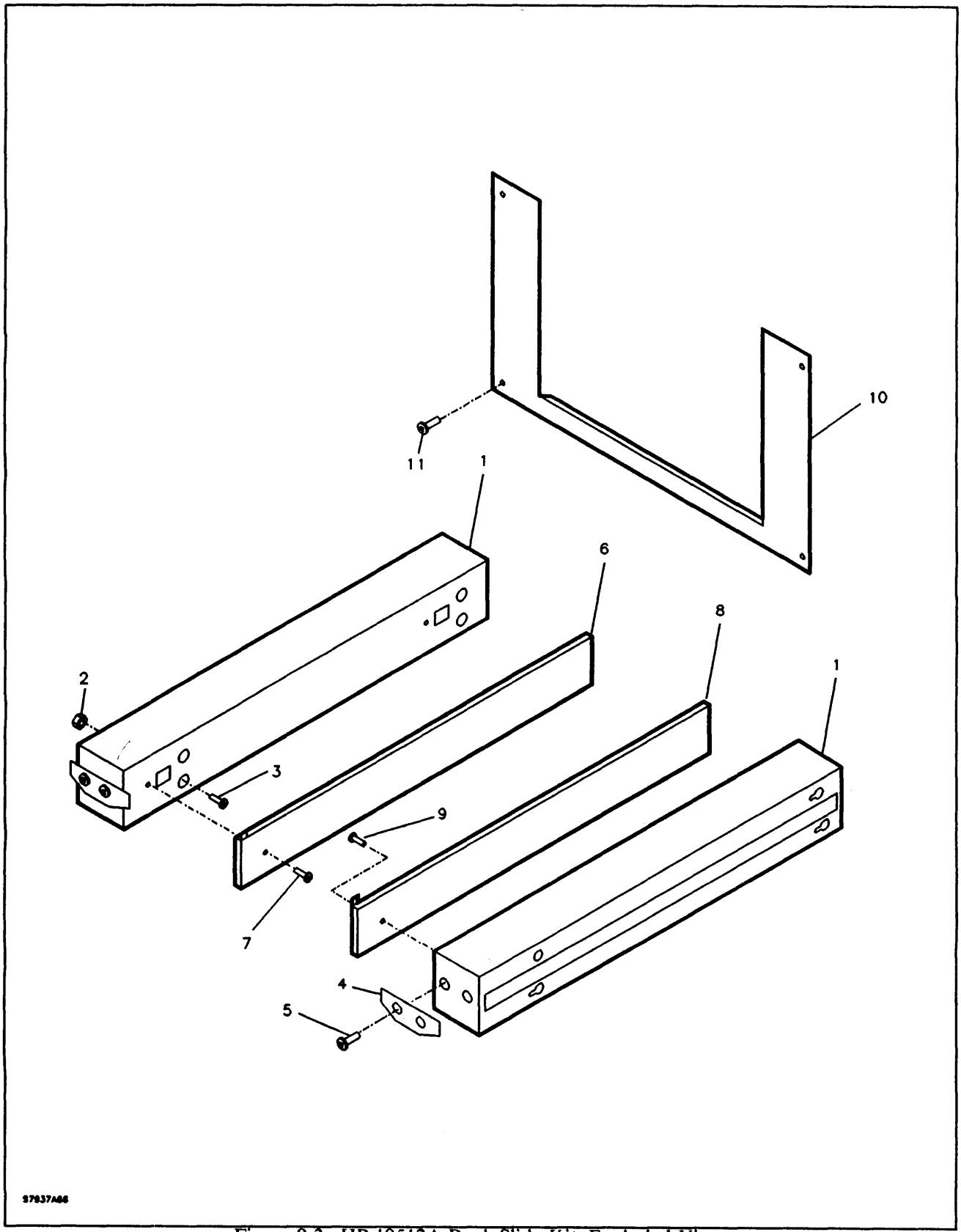


Figure 9-3. HP 19512A Rack Slide Kit, Exploded View

Table 9-4. Abbreviations

A	= ampere(s)	incand	= incandescent	qty	= quantity
ac	= alternating current	incl	= include(s)		
		intl	= internal	rdh	= round head
AR	= as required	I/O	= input/output	rect	= rectifier
assy	= assembly			ref	= reference
		k	= kilo (10^{3}), kilohm	rf	= radio frequency
brkt	= bracket			rfi	= radio frequency interference
		kg	= kilogram		
c	= centi (10^{-2})			rh	= right hand
C	= Celsius, centigrade	lb	= pound	rpm	= revolutions per minute
		LED	= light-emitting diode		
cer	= ceramic			rwv	= reverse working voltage
cm	= centimetre	lh	= left hand		
comp	= composition				
conn	= connector	M	= mega (10^{6}), megohm	sb	= slow blow
				SCR	= semiconductor-controlled rectifier
d	= deci (10^{-1})	m	= milli (10^{-3})		
dc	= direct current	mach	= machine		
deg	= degree(s)	mb	= medium blow	scw	= square cone washer
dia	= diameter	met oxd	= metal oxide		
dpdt	= double-pole, double-throw	mfr	= manufacturer	Se	= selenium
		misc	= miscellaneous	Si	= silicon
dpst	= double-pole, single throw	mm	= millimetre	slftpg	= self-tapping
		mtg	= mounting	spdt	= single-pole, double throw
		My	= Mylar		
elctlt	= electrolytic			spst	= single pole, single throw
encap	= encapsulated	n	= nano (10^{-9})		
ext	= external	n.c.	= normally closed	sst	= stainless steel
		no.	= number	stl	= steel
F	= Fahrenheit, farad	NSR	= not separately replaceable	sw	= switch
				T	= TORX(R) screw
fb	= fast blow	ntd	= no time delay	Ta	= tantalum
fh	= flat head			tgl	= toggle
fig.	= figure	OBD	= order by description	thd	= thread
filh	= fillister head			Ti	= titanium
flm	= film	OD	= outside diameter	tol	= tolerance
fw	= full wave				
fxd	= fixed	ovh	= oval head		
		oxd	= oxide	U (μ)	= micro (10^{-6})
G	= giga (10^{9})				
Ge	= germanium	p	= pico (10^{-12})	V	= volt(s)
		PCA	= printed-circuit assembly	var	= variable
H	= Henry, Henries			Vdcw	= direct current working volts
hd	= head	phh	= phillips head		
hex	= hexagon, hexagonal	pnh	= pan head		
		P/O	= part of	W	= watt(s)
hlcl	= helical	pot	= potentiometer	w/	= with
Hz	= Hertz	pozi	= Pozidriv	WIV	= inverse working volts
ID	= inside diameter				
in.	= inch, inches			ww	= wire-wound

TORX(R) is a registered trademark of the Camcar Division of Textron, Inc. (abbrev-8/83)

Table 9-5. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
28480	Hewlett-Packard Co.	Palo Alto, CA
60016	Littlefuse Inc.	Des Plaines, IL

Reference 10

10-1. CONTROLLER PCA-A6

Appendix A at the rear of this manual describes the controller PCA installed in the drive. This appendix describes HP-IB Controller, part no. 07937-60035 and HP-IB Cache Controller, part no. 07937-60037. These controllers are installed in the HP 7936H/7937H Disc Drive and and HP 7936XP/7937XP Disc Drive, respectively.

NOTE

In this manual, the controllers are designated collectively as PCA-A6.

Product History 11

11-1. INTRODUCTION

This chapter documents, by means of backdating information for other chapters of the manual, earlier versions of the drive. At present, no such backdating information is needed.

Diagrams 12

12-1. INTRODUCTION

This chapter contains electrical and mechanical diagrams for the drive. These provide details of drive dimensions, air circulation, the location of components within the drive, signal and power distribution, and functional block diagrams.

12-2. DIMENSIONS

The dimensions of the drive and the HP 19511A Cabinet are shown in figures 12-1 and 12-2, respectively.

12-3. AIR CIRCULATION

The path of the cooling air circulated by the squirrel-cage fan in the drive is shown in figure 12-3.

12-4. ASSEMBLY LOCATION

Figure 12-4 shows the locations of the major electronic assemblies and parts in the drive. These include:

servo PCA-A1
read/write PCA-A2
head-disc assembly A3
power supply PCA-A4
power distribution PCA-A5
controller PCA-A6
LED PCA-A7
primary power PCA-A8
spindle motor B1
line filter FL1

12-5. SIGNAL DISTRIBUTION

Due to the number of assemblies, multi-pin connectors, and interconnecting cables in the drive, it is impractical to provide a detailed signal distribution drawing for the drive in a single diagram. Instead, a simplified overall cabling diagram for the drive is supplied, followed by separate drawings which show the input and output signals at the connectors of each assembly in the drive and details of the interconnecting cables. Two tables also provide additional signal distribution information.

This signal distribution documentation consists of the following tables and figures:

- Table 12-1. An alphabetical listing of the signal mnemonics used in the parts location and connector pinout drawings, together with the source and destination for each signal. Refer to table 5-1 for a description of the signal functions.

- Table 12-2. A listing of the dc voltages shown in the parts location and connector pinout drawings, together with the source and destination of the voltages. Output specifications for the voltages are also given.

NOTE

In tables 12-1 and 12-2, where a multiple destination is given for a signal, this indicates that the signal is routed through a number of assemblies before it reaches its final destination. The destinations are listed in order, from the one nearest the source (first) to the final destination (last). In both tables:

A1 = servo PCA-A1
A2 = read/write PCA-A2
A3 = head-disc assembly A3
A4 = power supply PCA-A4
A5 = power distribution PCA-A5
A6 = controller PCA-A6
A7 = LED PCA-A7
A8 = primary power PCA-A8

- Figures 12-5 through 12-11. Drawings which provide details of cable assemblies W1

through W8, respectively. Information given includes:

description of connectors
connector pinout information
wire color code and gauge

- Figure 9-1. An exploded view of the drive where the connectors on cable assemblies W1 through W8 are identified and the locations of the mating connectors on the assemblies and parts are shown.

- Figure 12-12. A cabling diagram which illustrates how the assemblies and parts shown in figure 12-4 are interconnected together by connectors, cable assemblies, and wiring.

- Figures 12-13 through 12-19. Parts location and connector pinout drawings for assemblies A1 through A8, excluding controller PCA-A6 (see figure A-4). These drawings show:

location of connectors
mating cable connectors
connector pinout information
directional of signal flow
other parts

- Figure A-4. This figure contains the parts location and connector pinout for controller PCA-A6.

12-6. FUNCTIONAL BLOCK DIAGRAMS

The following functional block diagrams are contained in this chapter:

- Figure 12-20. Servo System
- Figure 12-21. Read/Write System
- Figure 12-22. Spindle Drive System
- Figure 12-23. Power Supply System

The functional block diagram for controller PCA-A6 is included in Appendix A (figure A-3).

Table 12-1. Signal Distribution List (1 of 6)

MNEMONIC	SIGNAL	SOURCE	DESTINATION	REMARKS
CE0-L	Chip Enable,	A2J7-43	A3J1-43	
CE1-L	bits 0 thru	A2J7-52	A3J1-52	
CE2-L	3	A2J7-50	A3J1-50	
CE3-L		A2J7-46	A3J1-46	
CH0-H	Chip 0	A2J7-5	A3J1-5	
CH1-H	Chip 1	A2J7-3	A3J1-3	
DAGC	Dedicated AGC	A1J2-19,20	A2P2-19,20	
DAR	DAC Reference	A1J2-8	A2P2-8 A2J7-4 A3J1-4	
DD0	Disc Data,	A6P1-46	A2J1-46	Disc Data
DD1	bits 0	A6P1-45	A2J1-45	Bus
DD2	thru 7	A6P1-48	A2J1-48	
DD3		A6P1-47	A2J1-47	
DD4		A6P1-50	A2J1-50	
DD5		A6P1-49	A2J1-49	
DD6		A6P1-52	A2J1-52	
DD7		A6P1-51	A2J1-51	
DDS-H	Disc Data Strobe	A2J1-41	A6P1-41	Disc Data Bus
DEDP	Dedicated	A2P2-13,14	A1J2-13,14	Differential
DEDN	Servo	A2P2-15,16	A1J2-15,16	signal
DID0	Drive Ident, bit 0	A3J1-25	A2J7-25 A2P2-5 A1J2-5	
DID1	Drive Ident, bit 1	A3J1-42	A2J7-42 A2P2-6 A1J2-6	
DPA0-H	Data Path Address Zero	A6P1-38	A2J1-38	Data Path Control Bus

Table 12-1. Signal Distribution List (2 of 6)

MNEMONIC	SIGNAL	SOURCE	DESTINATION	REMARKS
DPC0	Data Path	A6P1-24	A2J1-24	Bidirectional
DPC1	Control,	A6P1-23	A2J1-23	Data Path
DPC2	bits 0	A6P1-26	A2J1-26	Control bus
DPC3	thru 7	A6P1-25	A2J1-25	
DPC4		A6P1-28	A2J1-28	
DPC5		A6P1-27	A2J1-27	
DPC6		A6P1-30	A2J1-30	
DPC7		A6P1-29	A2J1-29	
DPCS-L	Data Path Control Select	A6P1-33	A2J1-33	Data Path Control Bus
DPIRQ-L	Data Path Interrupt Request	A2J1-36	A6P1-36	Data Path control Bus
DPRHW-L	Data Path Read High Write Low	A6P1-35	A2J1-35	Data Path Control Bus
DSOS-H, DSOS-L	Differential Start of Sector	A1J1-47 A1J1-48	A2P1-47 A2P1-48	
DWC-H, DWC-L	Differential Write Clock	A1J1-49 A1J1-50	A2P1-49 A2P1-50	
DX, DY	Read/Write Data	A2J7-57 A2J7-60	A3J1-57 A3J1-60	Bidirectional differential signal
GLED	Green LED	A6P2-3	A2J4-3 A2J6-4 A5J5-8 A5J2-5 A7J1-1	
HD1S-H	Head Select 1	A2J7-9	A3J1-9	
HDS2S-H	Head Select 2	A2J7-7	A3J1-7	
HS1-L, HS2-L	Head Select, bits 1,2	A2J7-47 A2J7-56	A3J1-47 A3J1-56	

Table 12-1. Signal Distribution List (3 of 6)

MNEMONIC	SIGNAL	SOURCE	DESTINATION	REMARKS
INDEX-H	Index	A1J1-39	A2P1-39 A2J1-15 A6P1-16	Servo Control Bus
LEDP	LED Power	A2J6-1	A5J5-5 A5J2-8 A7J1-4	
MOTOR+	Actuator Drive +	A1J2-42,43	A2P2-42,43 A2J7-33 thru 36,38 A3J1-33 thru 36,38	
MOTOR-	Actuator Drive -	A1J2-46,47	A2P2-46,47 A2J7-28 thru 32 A3J1-28 thru 32	
PF-L	Power Fail	A4J2-1	A5J2-2 A5J5-2 A2J6-6 A2J1-20 A6P1-20	
POR-L	Power On Reset	A4J2-2	A5J2-3 A5J5-1 A2J6-5 A2J1-18 A6P1-18 A2P1-43 A1J1-43	
RAGC-H, RAGC-L	Read AGC Gate	A1J2-2 A1J2-1	A2P2-2 A2P2-1	Differential signal
RLED	Red LED	A6P2-2	A2J4-2 A2J6-2 A5J5-6 A5J2-7 A7J1-3	
SAGC	Sampled AGC	A1J2-25,26	A2P2-25,26	

Table 12-1. Signal Distribution List (4 of 6)

MNEMONIC	SIGNAL	SOURCE	DESTINATION	REMARKS
SBF-L	Servo Buffer Full	A6P1-13	A2J1-13 A2P1-38 A1J1-38	Servo Control Bus
SCAP-L	Start Capacitor	A1J1-42	A2P1-42 A2J6-8 A5J5-4 A5J2-1 A8J5-2	
SDAV-L	Servo Data Available	A6P1-14	A2J1-14 A2P1-37 A1J1-37	Servo Control Bus
SDX, SDY	Servo Data	A3J1-12 A3J1-14	A2J7-12 A2J7-14	Differential signal
SD0	Servo Data, bit 0	A6P1-2	A2J1-2 A2P1-25 A1J1-25	Bidirectional Servo Control Bus (SD0 thru SD7)
SD1	Servo Data, bit 1	A6P1-1	A2J1-1 A2P1-26 A1J1-26	
SD2	Servo Data, bit 2	A6P1-4	A2J1-4 A2P1-27 A1J1-27	
SD3	Servo Data, bit 3	A6P1-3	A2J1-3 A2P1-28 A1J1-28	
SD4	Servo Data, bit 4	A6P1-6	A2J1-6 A2P1-29 A1J1-29	
SD5	Servo Data, bit 5	A6P1-5	A2J1-5 A2P1-30 A1J1-30	
SD6	Servo Data, bit 6	A6P1-8	A2J1-8 A2P1-31 A1J1-31	

Table 12-1. Signal Distribution List (5 of 6)

MNEMONIC	SIGNAL	SOURCE	DESTINATION	REMARKS
SD7	Servo Data, bit 7	A6P1-7	A2J1-7 A2P1-32 A1J1-32	
SEF-L	Start ECC Field	A2J1-40	A6P1-40	
SGR	Servo Gain Reference	A3J1-8	A2J7-8 A2J2-7	
SMPN, SMPP	Sampled Servo	A2P2-31,32 A2P2-29,30	A1J2-31,32 A1J2-29,30	Differential signal
SHS-H	Servo Head Select	A2J7-18	A3J1-18	
SOS-L	Start of Sector	A2J1-19	A6P1-19	Disc Data Bus
SPDSNS-L	Speed Sense	W5	A5J3-1 A5J5-3 A2J6-7 A2P1-40 A1J1-40	
SPR-L	Servo Processor Reset	A6P1-16	A2J1-16 A2P1-44 A1J1-44	Servo Control Bus
SRD-L	Servo Read	A1J1-35	A2P1-35 A2J1-12 A6P1-12	Servo Control Bus
SRVER-L	Servo Error	A1J1-45	A2P1-45	
SSEN-H SSEN-L	Sampled Servo Enable	A1J2-4 A1J2-3	A2P2-4 A2P2-3	Differential signal
SWC	Servo Write Current	A2J7-19	A3J1-19	Factory use only
SWR-L	Servo Write	A1J1-36	A2P1-36 A2J1-11 A6P1-11	Servo Control Bus

Table 12-1. Signal Distribution List (6 of 6)

MNEMONIC	SIGNAL	SOURCE	DESTINATION	REMARKS
SWS	Servo Write Select	A2J7-22	A3J1-22	Factory use only
US	Unsafe	A3J1-51	A2J7-51	
WC	Write Current	A2J7-53	A3J1-53	
WCS0	Write Current Select 0	A2J7-1	A3J1-1	
WCS1	Write Current Select 1	A2J7-17	A3J1-17	
WHO-L	Write Hold Off	A6P1-37	A2J1-37	Disc Data Bus
WSA	Write Select A	A2J7-45	A3J1-45	
WSB	Write Select B	A2J7-48	A3J1-48	
YLED	Yellow LED	A6P2-4	A2J4-4 A2J6-3 A5J5-7 A5J2-6 A7J1-2	

Table 12-2. Voltage Distribution List (1 of 1)

VOLTAGE	SOURCE	DESTINATION	OUTPUT SPECIFICATIONS
+45V	A4J2-15	A5J1-17 A5J4-20 A2J5-1 A2P1-4,5 A1J1-4,5	+30V to +45V, ripple 1V pp max. Typical values are 32V when seeking, and 37V when not seeking.
+12V	A4J2-13	A5J1-12 A5J4-15 A2J5-6 A2P1-13 A1J1-13 A2J7-2 A3J1-2	+10.8V to +13.2V, ripple 200 mV pp max.
+6V	A2J7-21,49	A3J1-21,49	
+5V	A4J2-4, 5, 8	A5J1-2,4,6 A5J4-5 thru 8 A2J5-13 thru 16 A2P1-19 thru 21 A1J1-19 thru 21 A2J4-5 thru 16 A6P2-5 thru 16 A2J7-13 A3J1-13	+4.75V to +5.25V, ripple 100 mV pp max.
-45V	A4J2-18	A5J1-15 A5J4-18 A2J5-3 A2P1-8,9 A1J1-8,9	-30V to -45V, ripple 1V pp max. Typical values are -32V when seeking, and -37V when not seeking.
-12V	A4J2-7	A5J1-10 A5J4-14 A2J5-7 A2P1-15 A1J1-15 A2J7-6 A3J1-6	-10.8V to -13.2V, ripple 200 mV pp max.
-5.2V	A4J2-16	A5J1-8 A5J4-13 A2J5-8 A2P1-14 A1J1-14 A2J4-1 A6P2-1	-4.94V to -5.46V, ripple 100 mV pp max.
-4V	A2J7-20,54	A3J1-20,54	

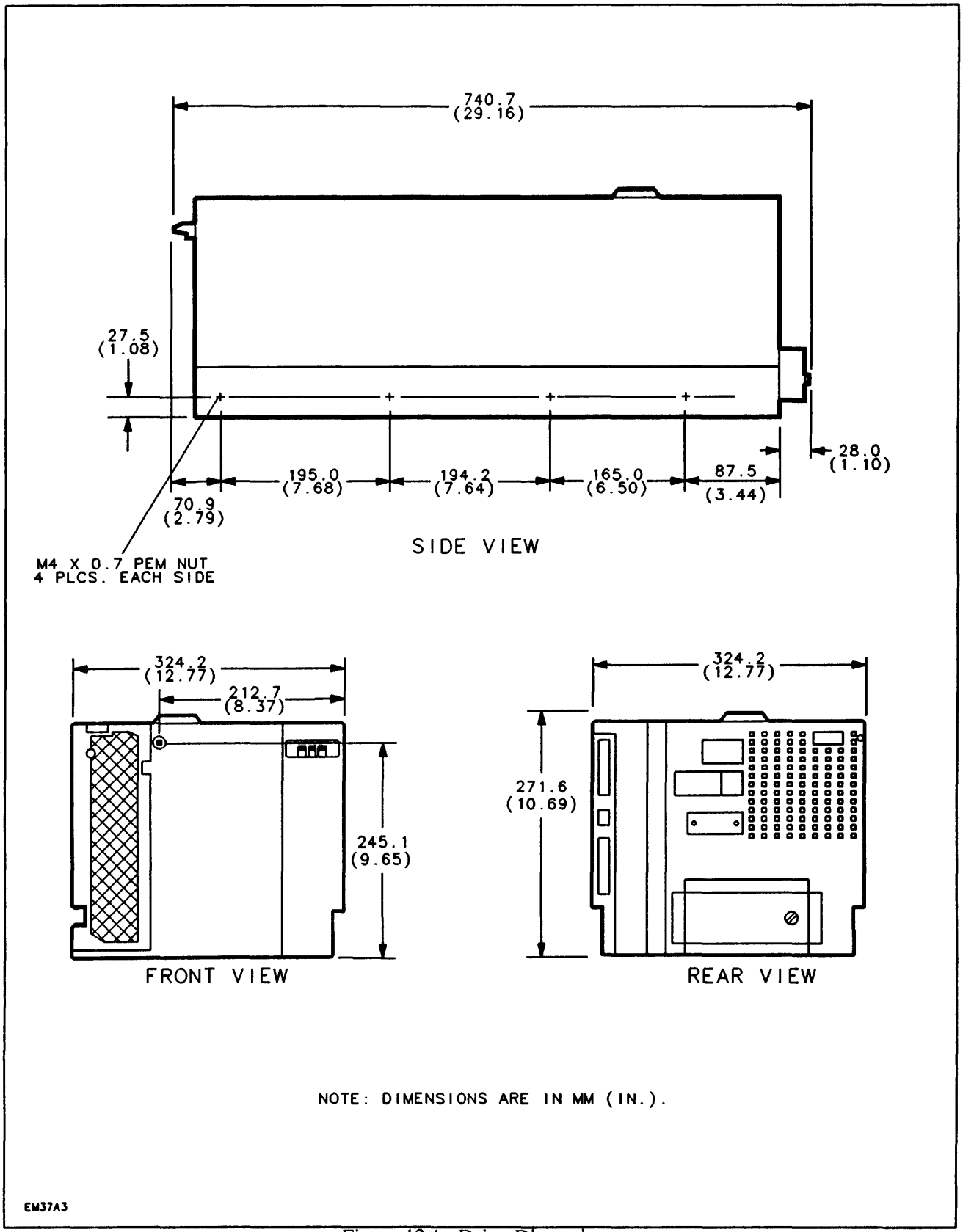
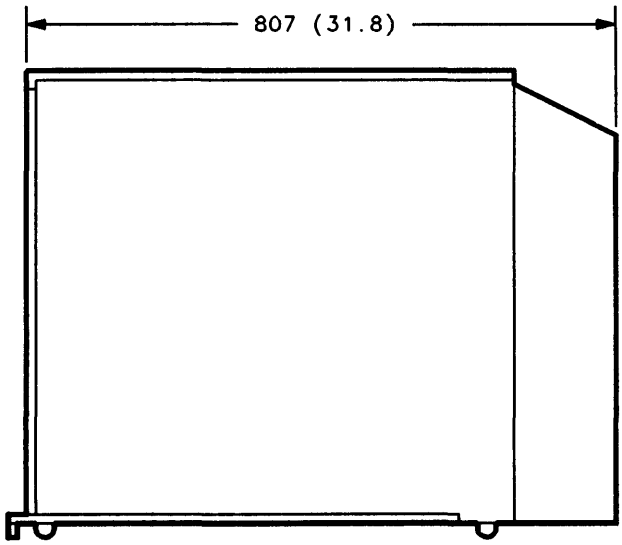
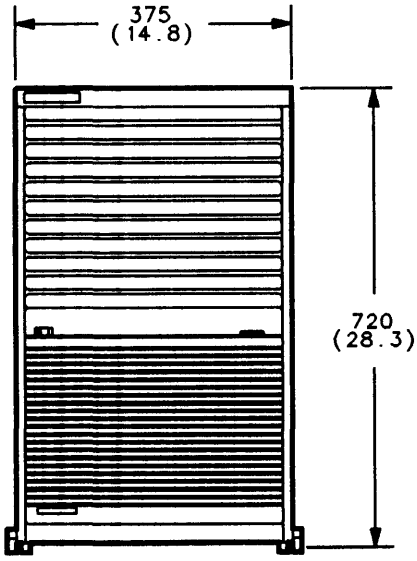


Figure 12-1. Drive Dimensions



SIDE VIEW



FRONT VIEW

NOTE: DIMENSIONS ARE IN MM (IN.)

17937A14

Figure 12-2. HP 19511A Cabinet Dimensions

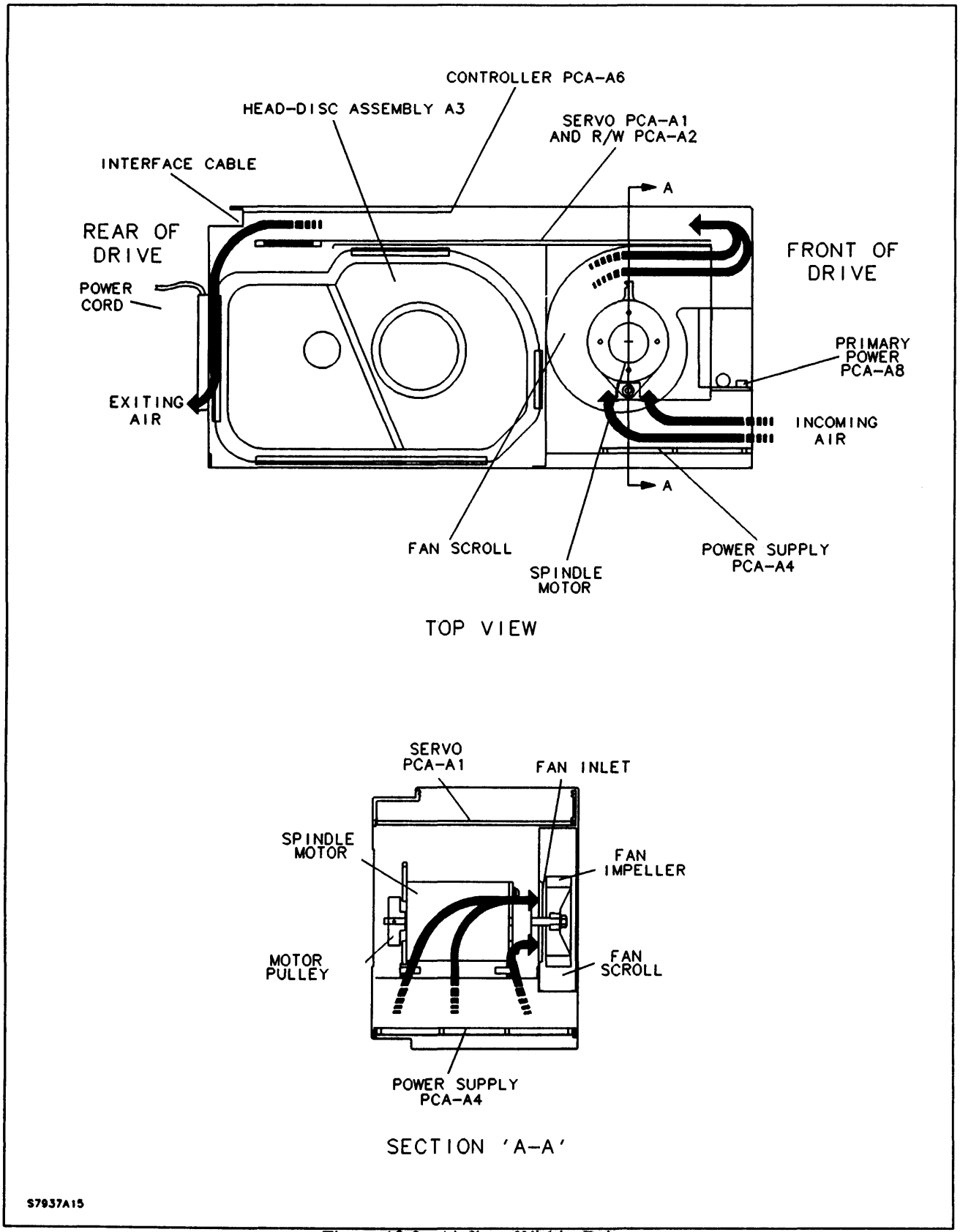


Figure 12-3. Airflow Within Drive

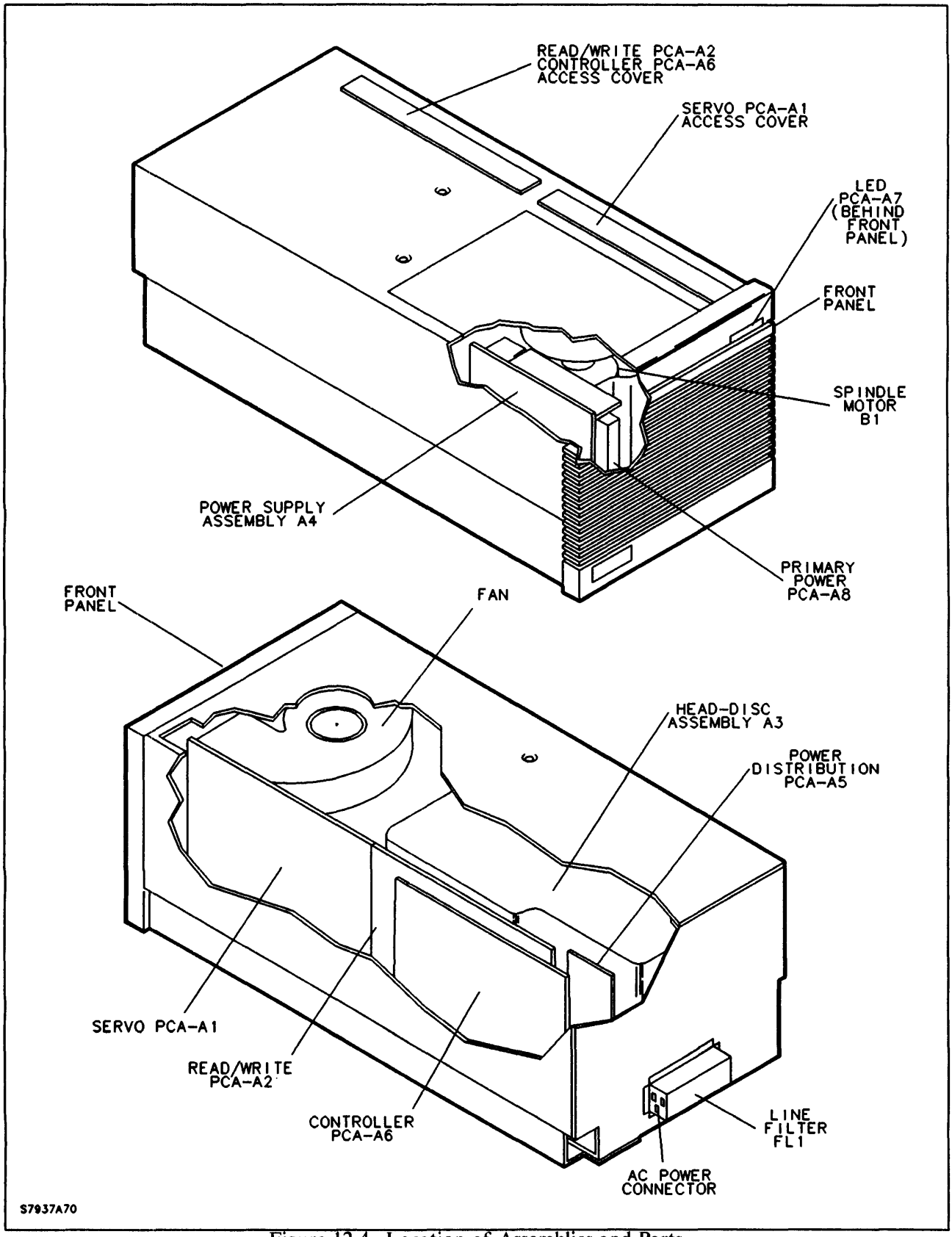
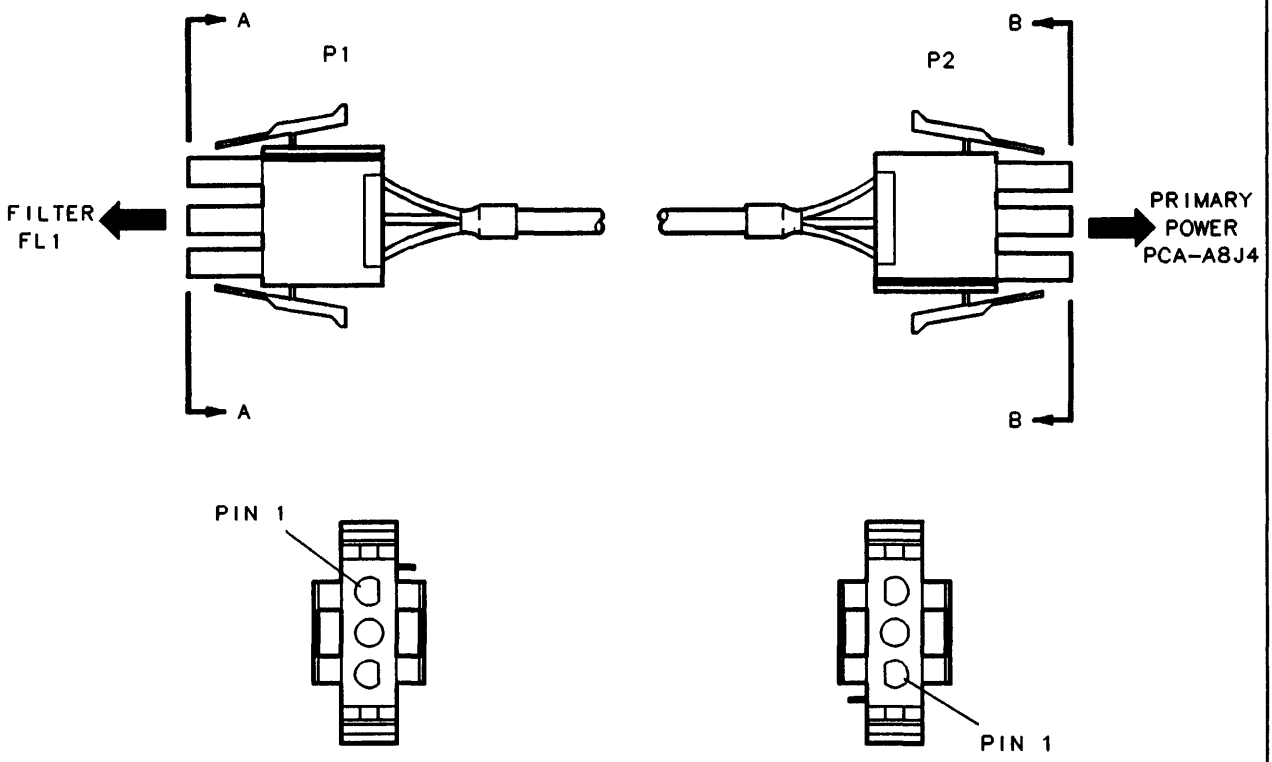


Figure 12-4. Location of Assemblies and Parts



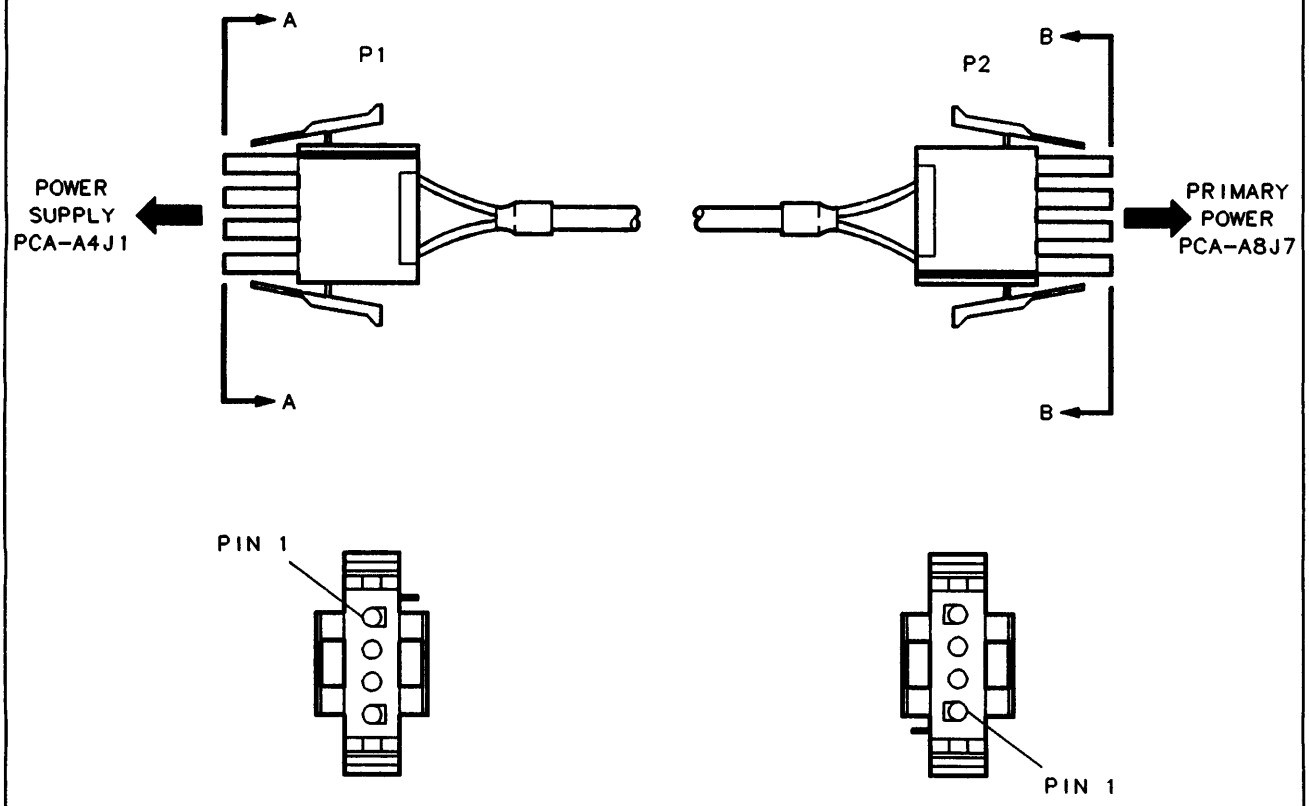
PIN ASSIGNMENTS:

SIGNAL	P1	P2	WIRE	
NEUTRAL	1	1	BLU	SEE NOTE 2
EARTH	2	2	GRN/YEL	
LINE	3	3	BRN	

NOTES:
1. CABLE PART NO. 07937-60173
2. 3-CONDUCTOR CABLE, 18 AWG

S7937A67

Figure 12-5. Primary Power Cable Assembly W1



PIN ASSIGNMENTS:

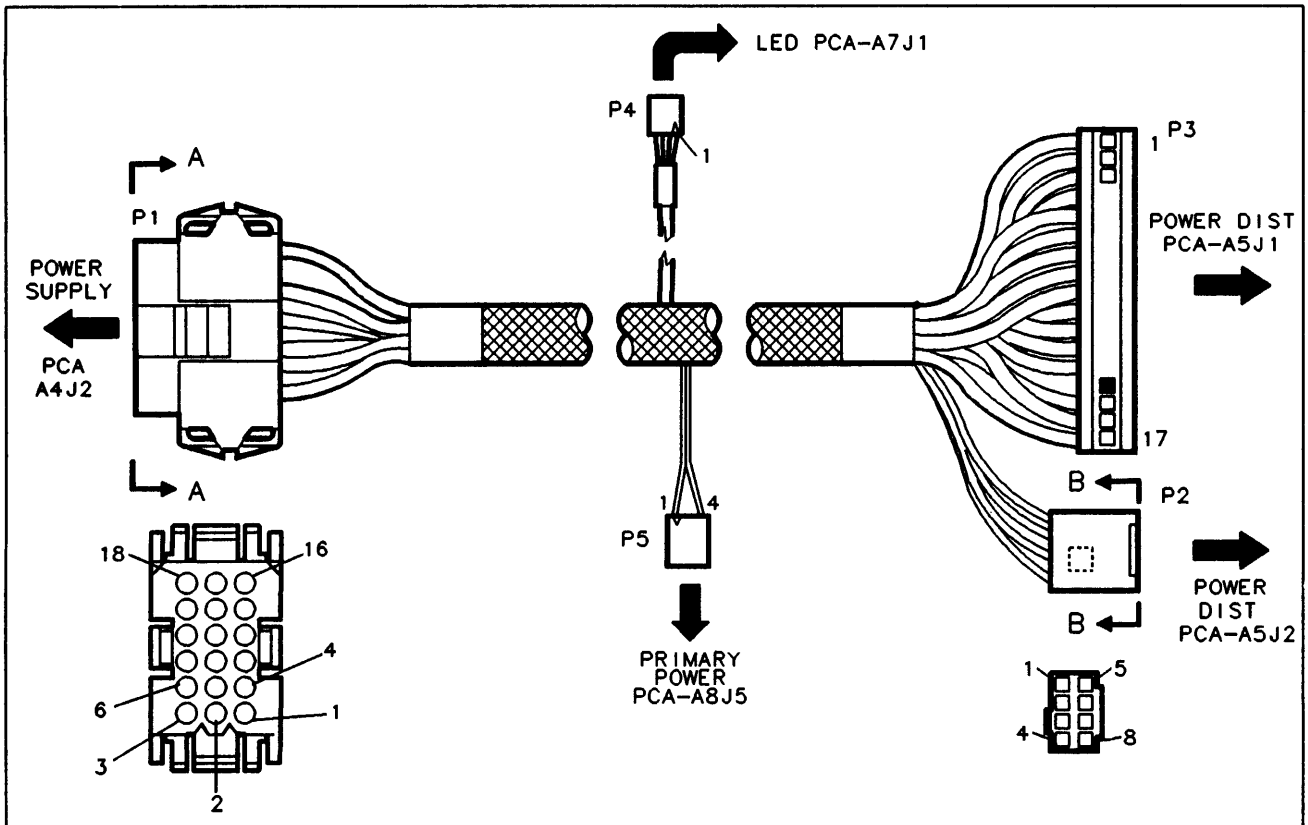
SIGNAL	P1	P2	WIRE	
NEUTRAL	1	1	BRN	SEE NOTE 2
EARTH	2	2	BLU	
LINE	4	4	GRN/YEL	

NOTES:

1. CABLE PART NO. 07937-60164
2. 3-CONDUCTOR CABLE, 18 AWG

S7937A68

Figure 12-6. Power Supply Input Cable Assembly W3



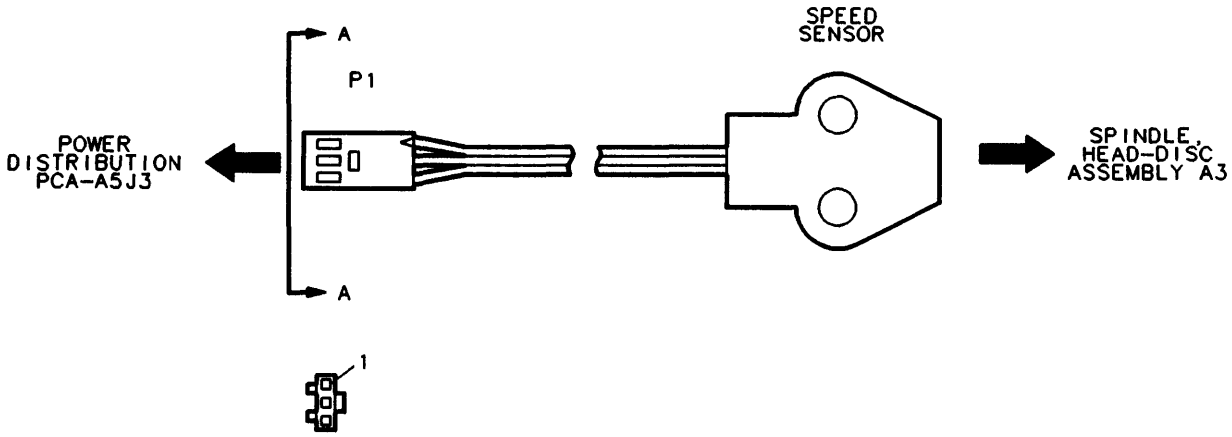
PIN ASSIGNMENTS:

SIGNAL	P1	P2	P3	P4	P5	WIRE	
PF-L	1	2				GRN	22 AWG
POR-L	2	3				WHT/RED	
GND	3		1			BLK	
+5V	4		2			WHT	
+5V	5		4			WHT	
GND	6		3			BLK	
-12V	7		10			RED	
+5V	8		6			WHT	
GND	9		5			BLK	
GND	10		7			BLK	18 AWG
GND	11		9			BLK	
GND	12		11			BLK	
+12V	13		12			ORN	
GND	14		13			BLK	
+45V	15		17			VIO	
-5.2V	16		8			GRA	
GND	17		16			BLK	
-45V	18		15			WHT/BLK	
GLED		5		1		YEL	
YLED		6		2		ORN	
SCAP-L		1			2	BLK	
+5V		4			4	WHT	22 AWG
RLED		7		3		RED	
+5V		8		4		WHT/GRN	

NOTE: CABLE PART NO. 07937-60163

S7937A69

Figure 12-7. Power Supply Output Cable Assembly W4



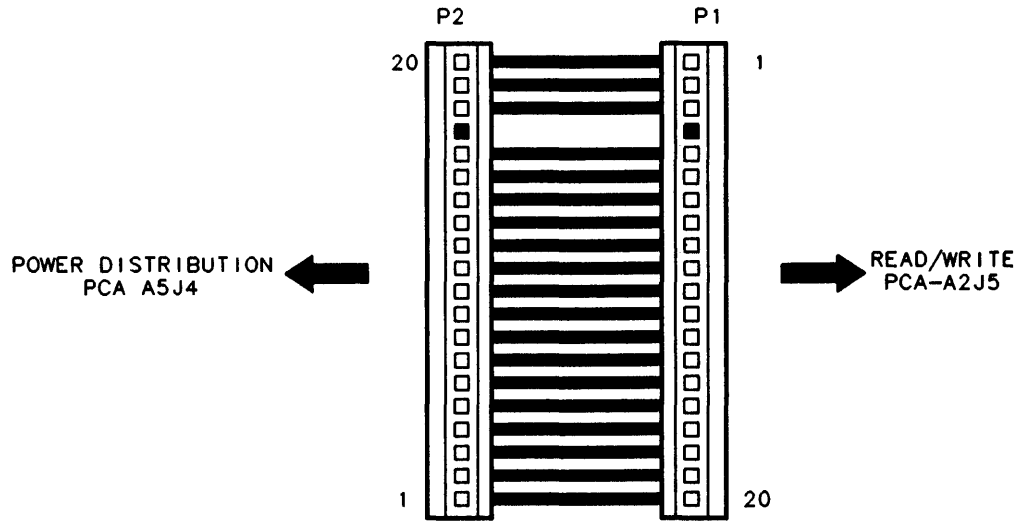
PIN ASSIGNMENTS:

SIGNAL	P1	SPEED SENSOR	WIRE
GND	1		WHT
SPD SNS	2		BLK
+5V	3		RED

NOTES: 1. Cable part no. 07937-60038

S7937A17

Figure 12-8. Speed Sensor Cable Assembly W5



PIN ASSIGNMENTS:

SIGNAL	P1	P2	WIRE	SIGNAL	P1	P2	WIRE
+45V	1	20	NOTE 2	GND	11	10	NOTE 2
GND	2	19		GND	12	9	
−45V	3	18		+5V	13	8	
KEY	4	17		+5V	14	7	
GND	5	16		+5V	15	6	
+12V	6	15		+5V	16	5	
−12V	7	14		GND	17	4	
−5.2V	8	13		GND	18	3	
GND	9	12		GND	19	2	
GND	10	11		GND	20	1	

NOTES: 1. Cable part no. 07937-60064
2. Wire: ORN, 18 AWG

S7937A18

Figure 12-9. Power Jumper Cable Assembly W6

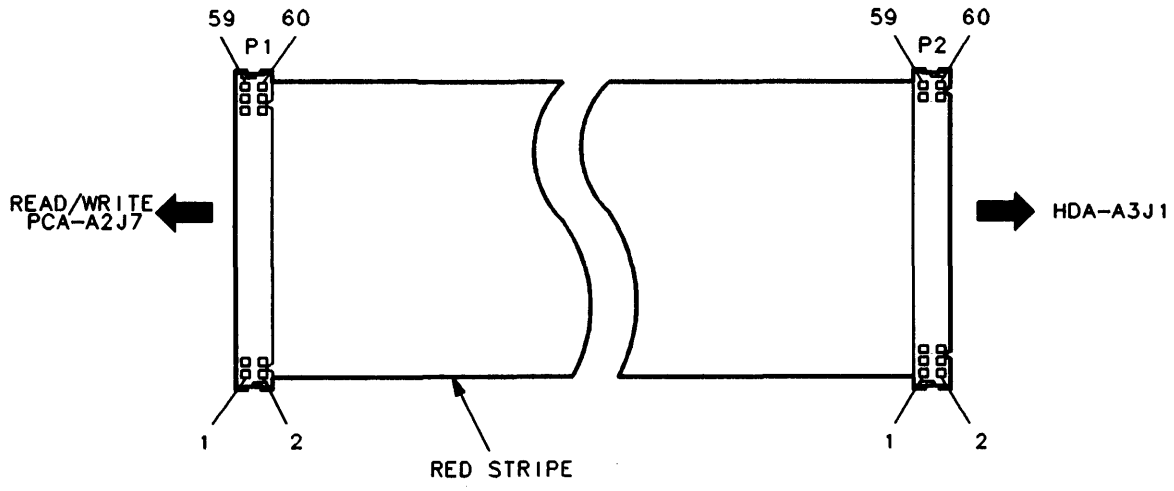
PIN ASSIGNMENTS:

SIGNAL	P1	P2	WIRE
POR-L	5	1	NOTE 2
PF-L	6	2	
SCAP-L	8	4	
SPD SNS-L	7	3	
LEDP +5V	1	5	
RLED	2	6	
YLED	3	7	
GLED	4	8	

NOTES: 1. Cable part no. 07937-60065
2. All wires BLK, 22 AWG

S7937A19

Figure 12-10. Signal Jumper Cable Assembly W7



PIN ASSIGNMENTS:

SIGNAL	P1	P2	WIRE	SIGNAL	P1	P2	WIRE
WCS0	1	1	NOTE 2		31	31	
+12V	2	2		MOTOR-	32	32	
CH1-H	3	3			33	33	
DAR	4	4			34	34	
CH0-H	5	5		MOTOR+	35	35	
-12V	6	6			36	36	
HD2S-H	7	7		GND	37	37	
SGR	8	8		MOTOR+	38	38	
HD1S-H	9	9			39	39	
BSOS-H	10	10		GND	40	40	
GND	11	11			41	41	
SDX	12	12		D1D1	42	42	
+5V	13	13		CE0-L	43	43	
SDY	14	14		GND	44	44	
GND	15	15		WSA	45	45	
GND	16	16		CE3-L	46	46	
WCS1	17	17		HS1-L	47	47	
SHS-H	18	18		WSB	48	48	
SWC	19	19		+6V	49	49	
-4V	20	20		CE2-L	50	50	
+6V	21	21		US	51	51	
SWS	22	22		CE1-L	52	52	
GND	23	23		WC	53	53	
GND	24	24		-4V	54	54	
D1D0	25	25		GND	55	55	
GND	26	26		HS2-L	56	56	
GND	27	27		DX	57	57	
	28	28		GND	58	58	
MOTOR-	29	29		GND	59	59	
	30	30		DY	60	60	

NOTES: 1. Cable, part no. 07937-60068
2. 60-conducter ribbon cable, 28 AWG

S7937A20

Figure 12-11. HDA Cable Assembly W8

NOTES:

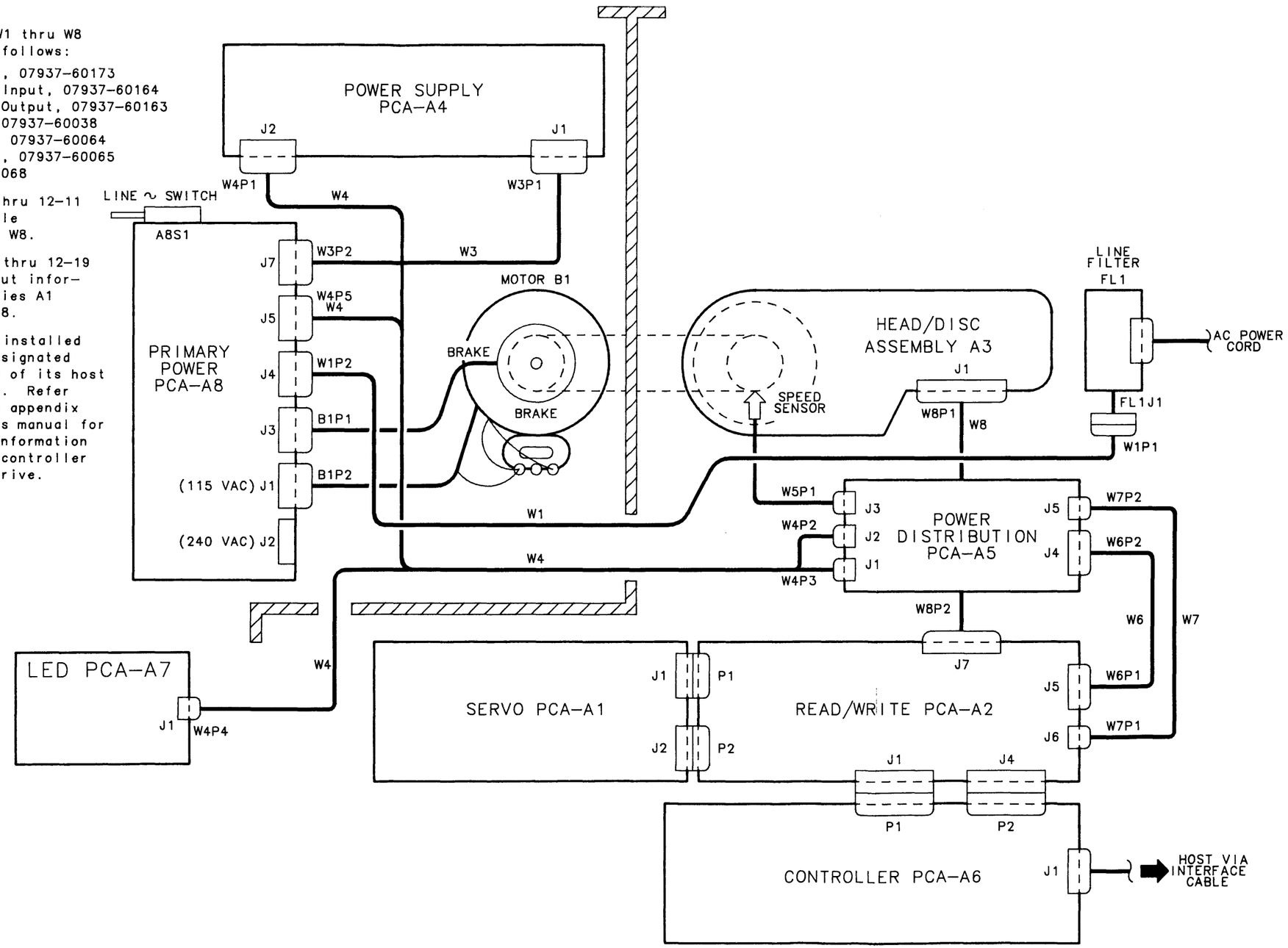
1. Cable assemblies W1 thru W8 are identified as follows:

   W1 – Primary Power, 07937-60173
   W3 – Power Supply Input, 07937-60164
   W4 – Power Supply Output, 07937-60163
   W5 – Speed Sense, 07937-60038
   W6 – Power Jumper, 07937-60064
   W7 – Signal Jumper, 07937-60065
   W8 – HDA, 07937-60068

2. See figures 12-5 thru 12-11 for details of cable assemblies W1 thru W8.

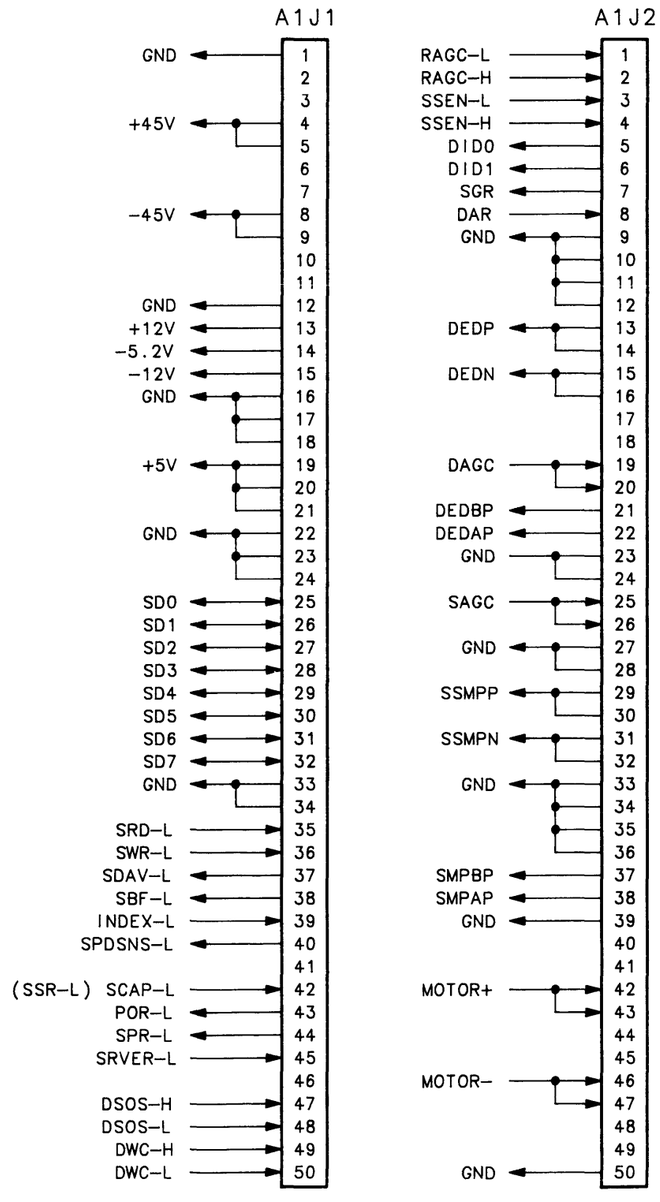
3. See figures 12-13 thru 12-19 for connector pinout information for assemblies A1 thru A5, A7, and A8.

4. Controller PCA-A6 installed in the drive is designated PCA-A6, regardless of its host interface function. Refer to the appropriate appendix at the rear of this manual for connector pinout information applicable to the controller installed in the drive.

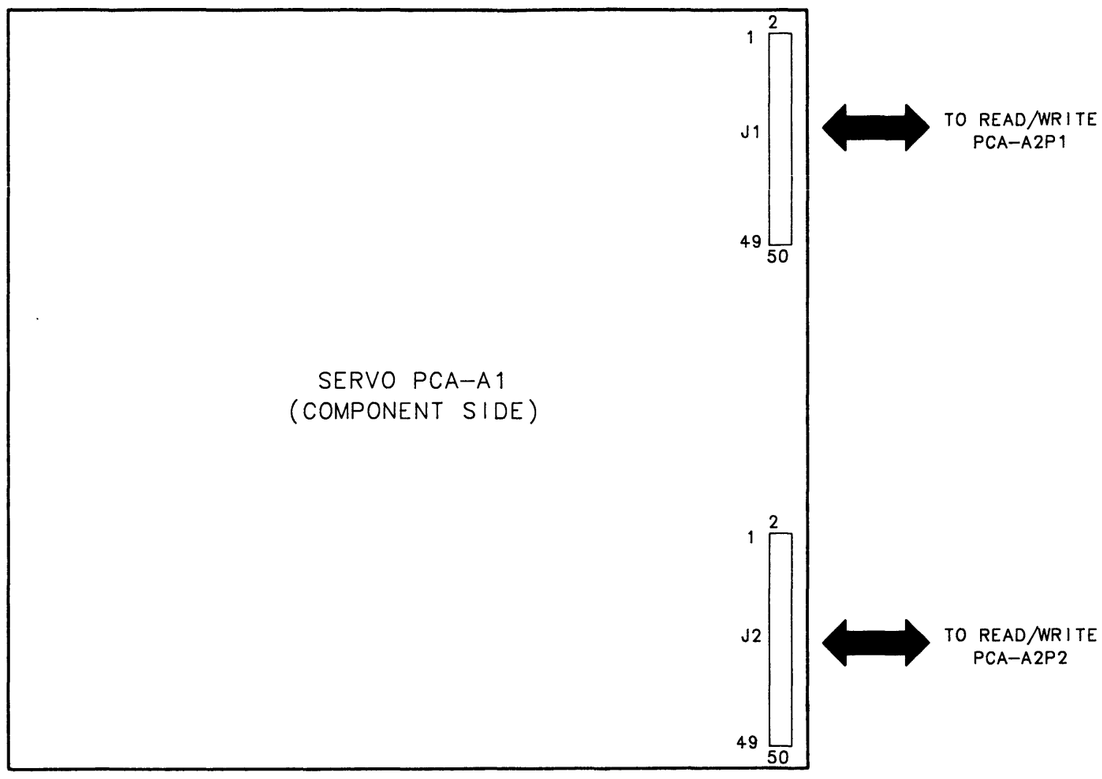


S7937A57

Figure 12-12. Cabling Diagram



S7937A02



NOTE: Direction of signal flow in and out of PCA-A1 is indicated as follows:

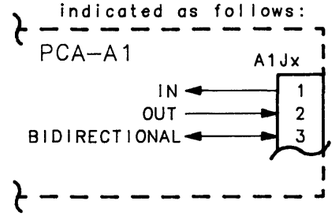
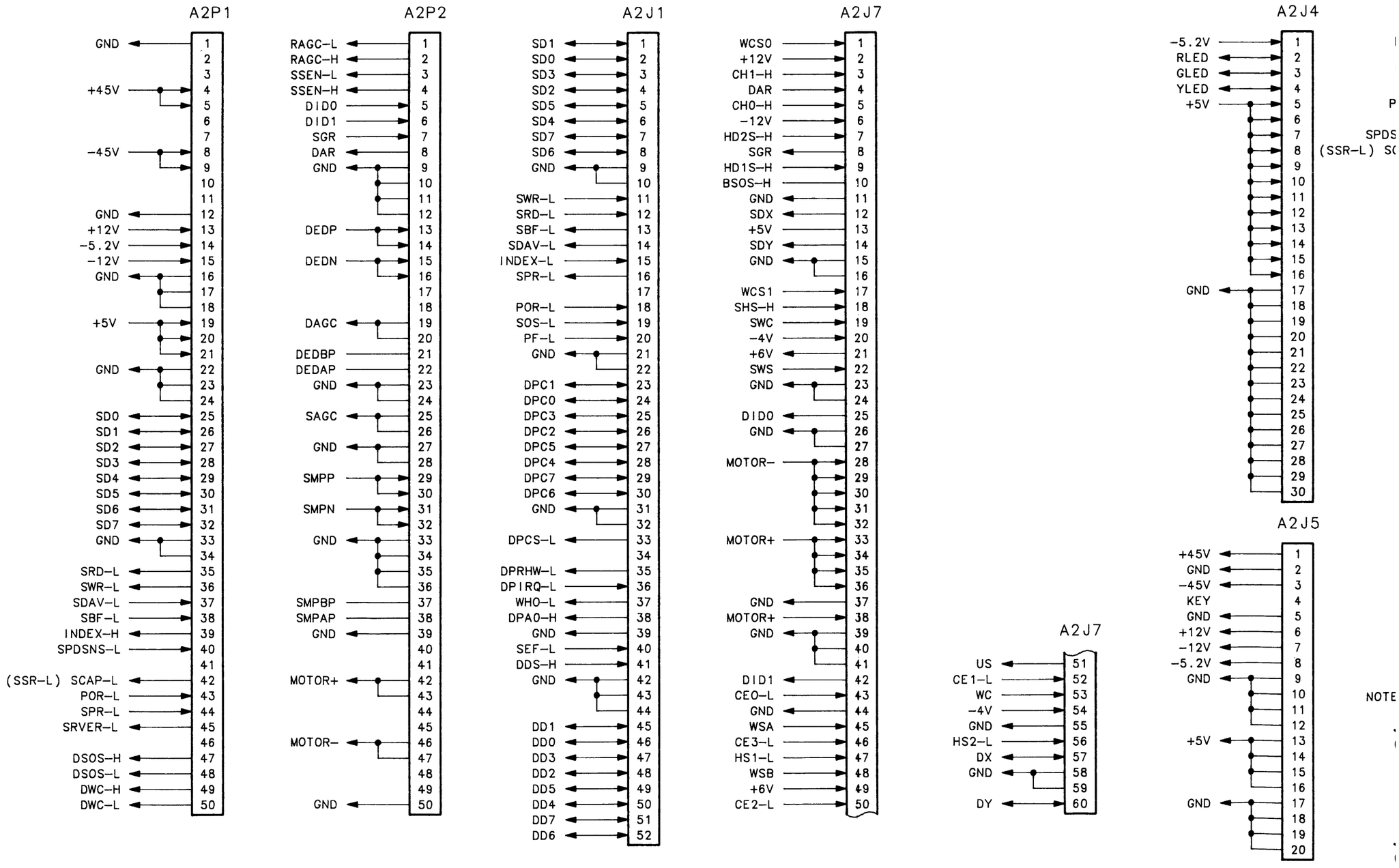


Figure 12-13. Servo PCA-A1, Parts Location and Connector Pinout


A2P1
GND 1
2
3
+45V 4
5
6
7
-45V 8
9
10
11
GND 12
+12V 13
-5.2V 14
-12V 15
GND 16
17
18
+5V 19
20
21
GND 22
23
24
SD0 25
SD1 26
SD2 27
SD3 28
SD4 29
SD5 30
SD6 31
SD7 32
GND 33
34
SRD-L 35
SWR-L 36
SDAV-L 37
SBF-L 38
INDEX-H 39
SPDSNS-L 40
41
(SSR-L) SCAP-L 42
POR-L 43
SPR-L 44
SRVER-L 45
46
DSOS-H 47
DSOS-L 48
DWC-H 49
DWC-L 50
A2P2
RAGC-L 1
RAGC-H 2
SSEN-L 3
SSEN-H 4
DID0 5
DID1 6
SGR 7
DAR 8
GND 9
10
11
12
DEDP 13
14
DEDN 15
16
17
18
DAGC 19
20
DEDBP 21
DEDAP 22
GND 23
24
SAGC 25
26
GND 27
28
SMPP 29
30
SMPN 31
32
GND 33
34
35
36
SMPBP 37
SMPAP 38
GND 39
40
41
MOTOR+ 42
43
44
45
MOTOR- 46
47
48
49
GND 50
A2J1
SD1 1
SD0 2
SD3 3
SD2 4
SD5 5
SD4 6
SD7 7
SD6 8
GND 9
10
SWR-L 11
SRD-L 12
SBF-L 13
SDAV-L 14
INDEX-L 15
SPR-L 16
17
POR-L 18
SOS-L 19
PF-L 20
GND 21
22
DPC1 23
DPC0 24
DPC3 25
DPC2 26
DPC5 27
DPC4 28
DPC7 29
DPC6 30
GND 31
32
DPCS-L 33
34
DPRHW-L 35
DPIRQ-L 36
WHO-L 37
DPA0-H 38
GND 39
SEF-L 40
DDS-H 41
GND 42
43
44
DD1 45
DD0 46
DD3 47
DD2 48
DD5 49
DD4 50
DD7 51
DD6 52
A2J7
WCS0 1
+12V 2
CH1-H 3
DAR 4
CH0-H 5
-12V 6
HD2S-H 7
SGR 8
HD1S-H 9
BSOS-H 10
GND 11
SDX 12
+5V 13
SDY 14
GND 15
16
WCS1 17
SHS-H 18
SWC 19
-4V 20
+6V 21
SWS 22
GND 23
24
DID0 25
GND 26
27
MOTOR- 28
29
30
31
32
MOTOR+ 33
34
35
36
GND 37
MOTOR+ 38
GND 39
40
41
DID1 42
CE0-L 43
GND 44
WSA 45
CE3-L 46
HS1-L 47
WSB 48
+6V 49
CE2-L 50
A2J4
-5.2V 1
RLED 2
GLED 3
YLED 4
+5V 5
6
7
8
9
10
11
12
13
14
15
16
GND 17
18
19
20
21
22
23
24
25
26
27
28
29
30
A2J5
+45V 1
GND 2
-45V 3
KEY 4
GND 5
+12V 6
-12V 7
-5.2V 8
GND 9
10
11
12
+5V 13
14
15
16
GND 17
18
19
20
A2J7
US 51
CE1-L 52
WC 53
-4V 54
GND 55
HS2-L 56
DX 57
GND 58
59
DY 60

S7937A03

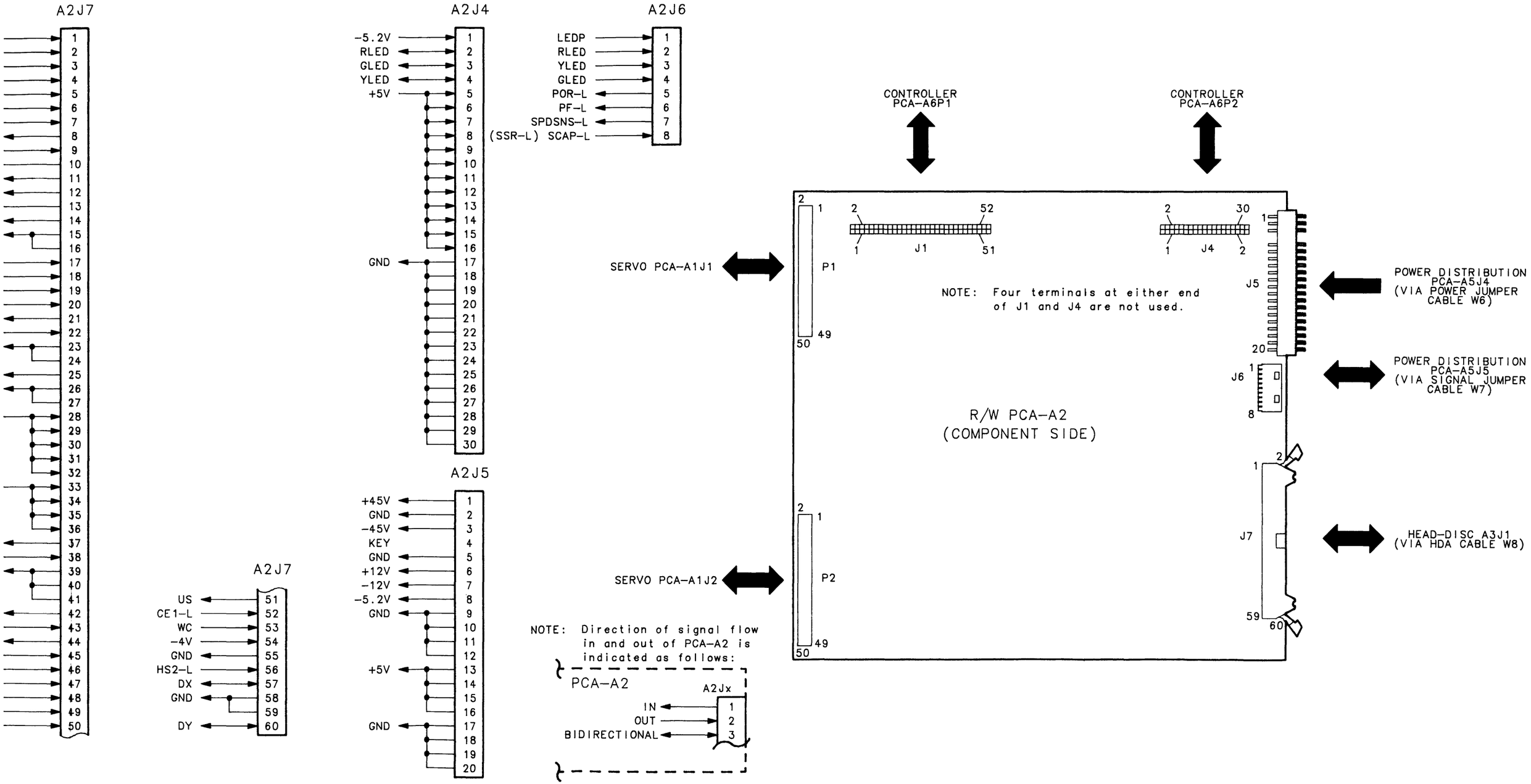
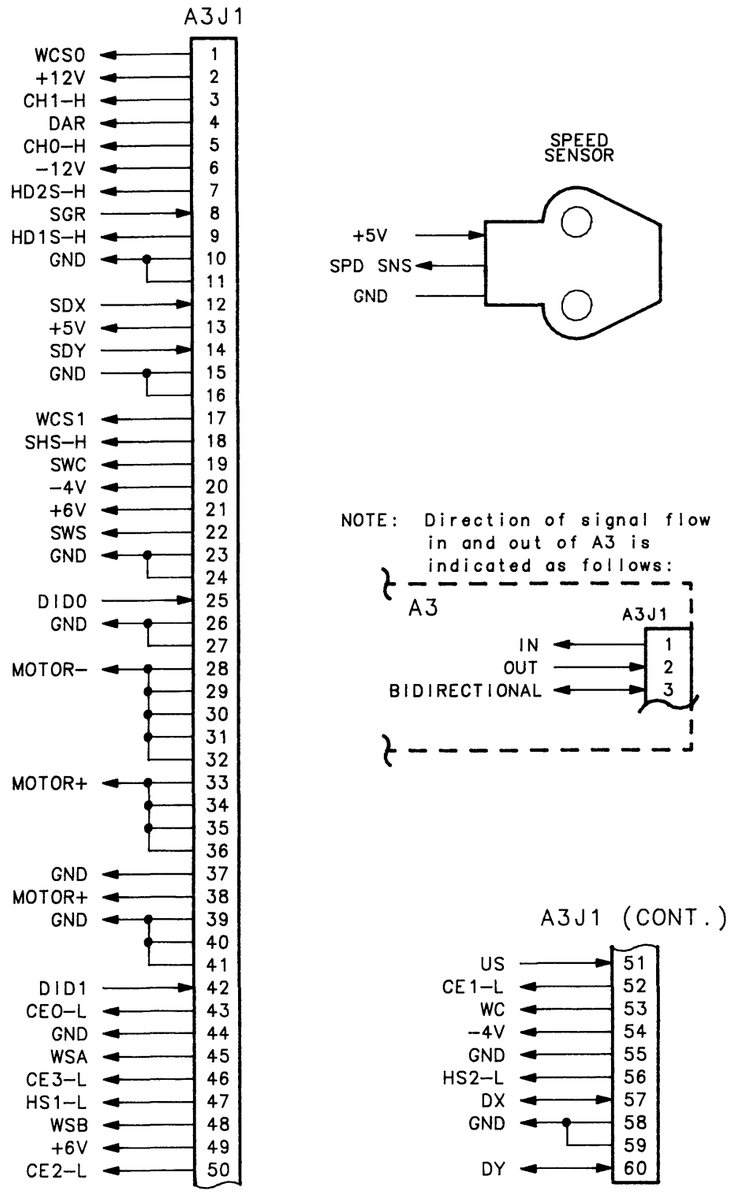


Figure 12-14. R/W PCA-A2, Parts Location and Connector Pinout



NOTE: Direction of signal flow in and out of A3 is indicated as follows:

S7937A04

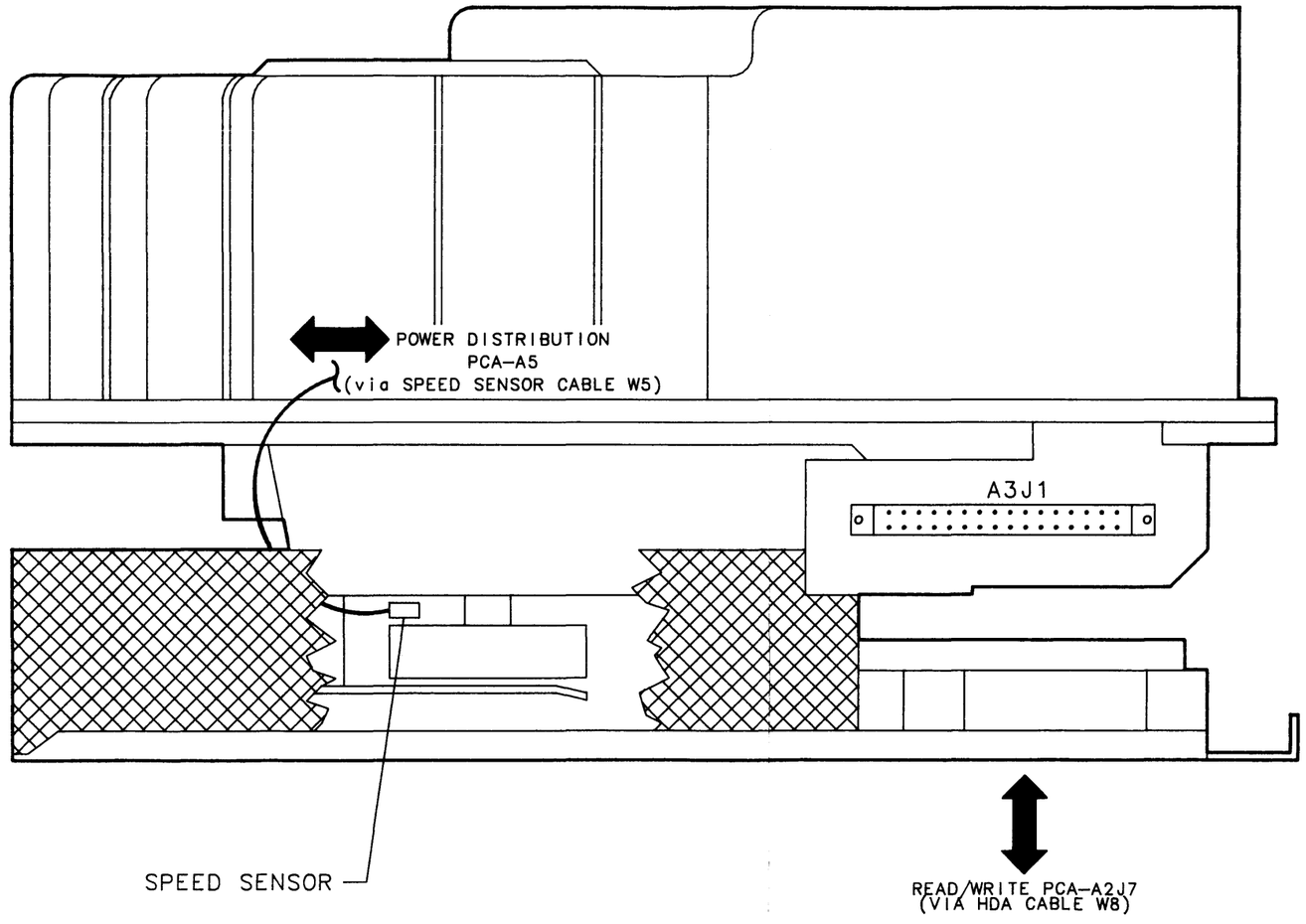
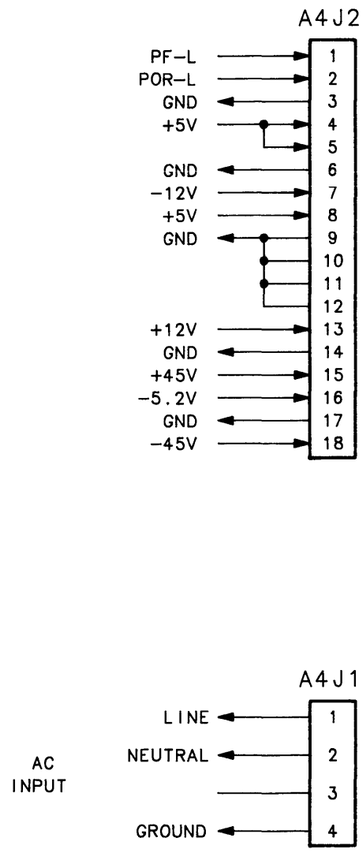
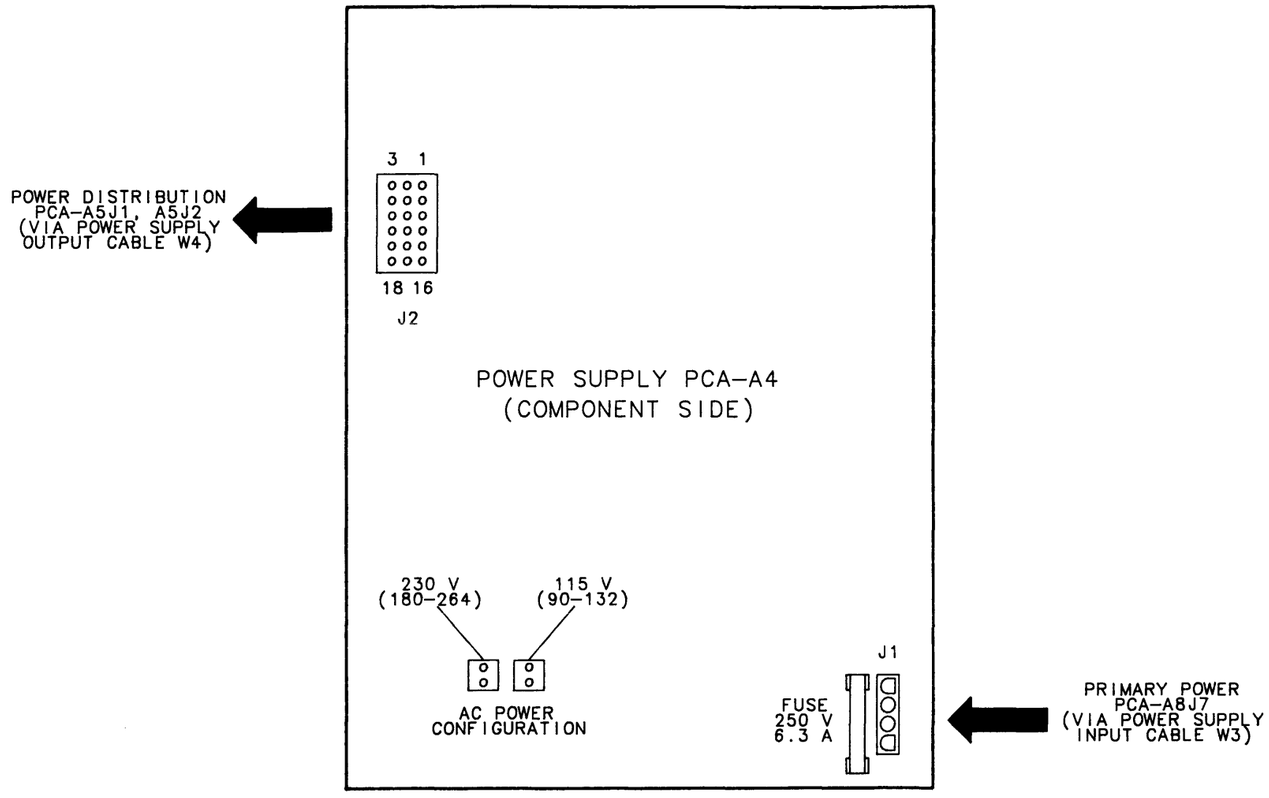
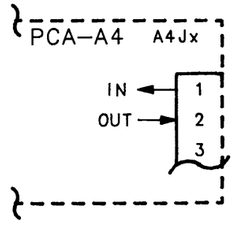


Figure 12-15. HDA Assembly A3, Parts Location and Connector Pinout





NOTE:
DIRECTION OF SIGNAL FLOW IN AND OUT OF PCA–A4 IS INDICATED AS FOLLOWS:



S7937A05

Figure 12-16. Power Supply PCA-A4, Parts Location and Connector Pinout

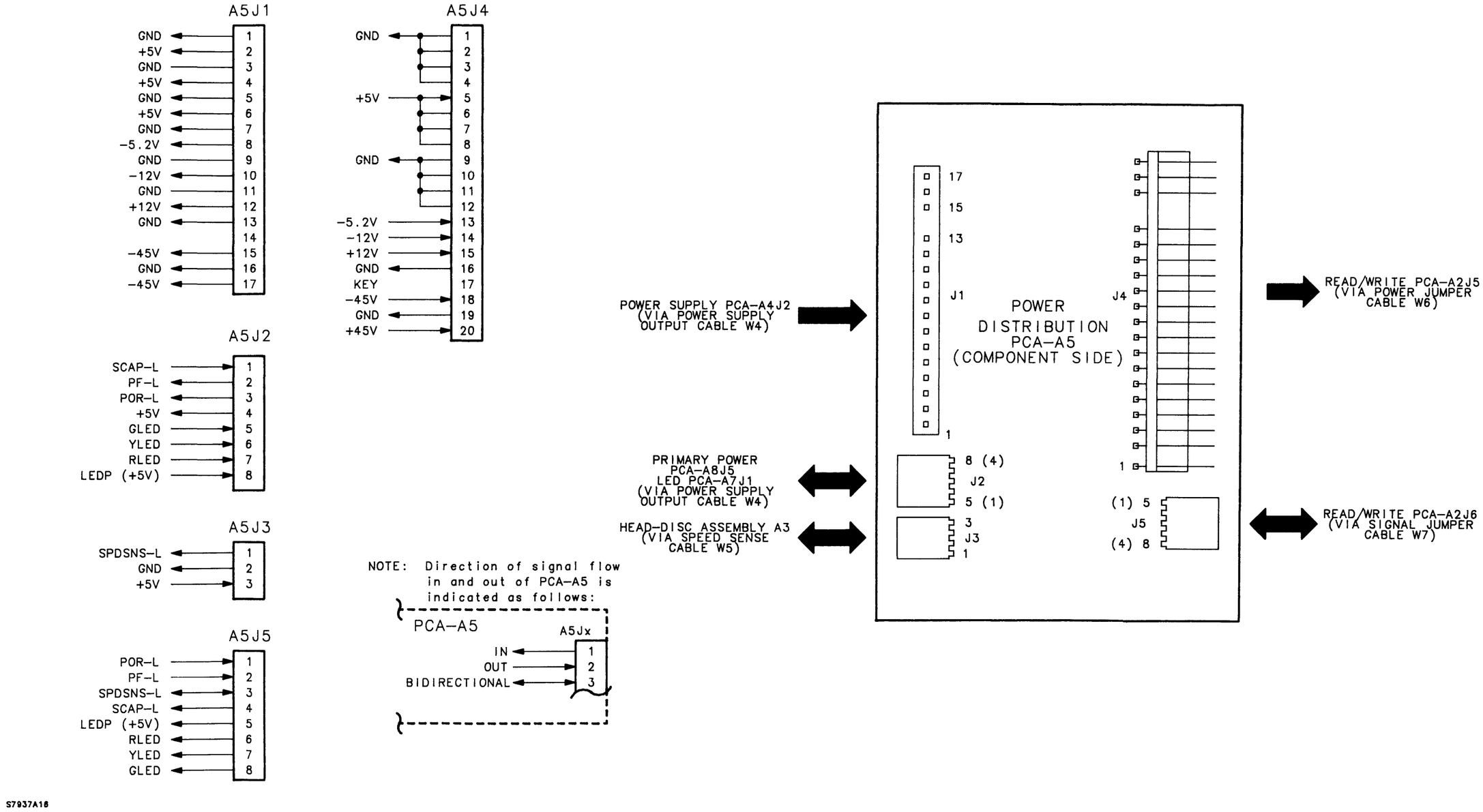


Figure 12-17. Power Distribution PCA-A5. Parts Location and Connector Pinout

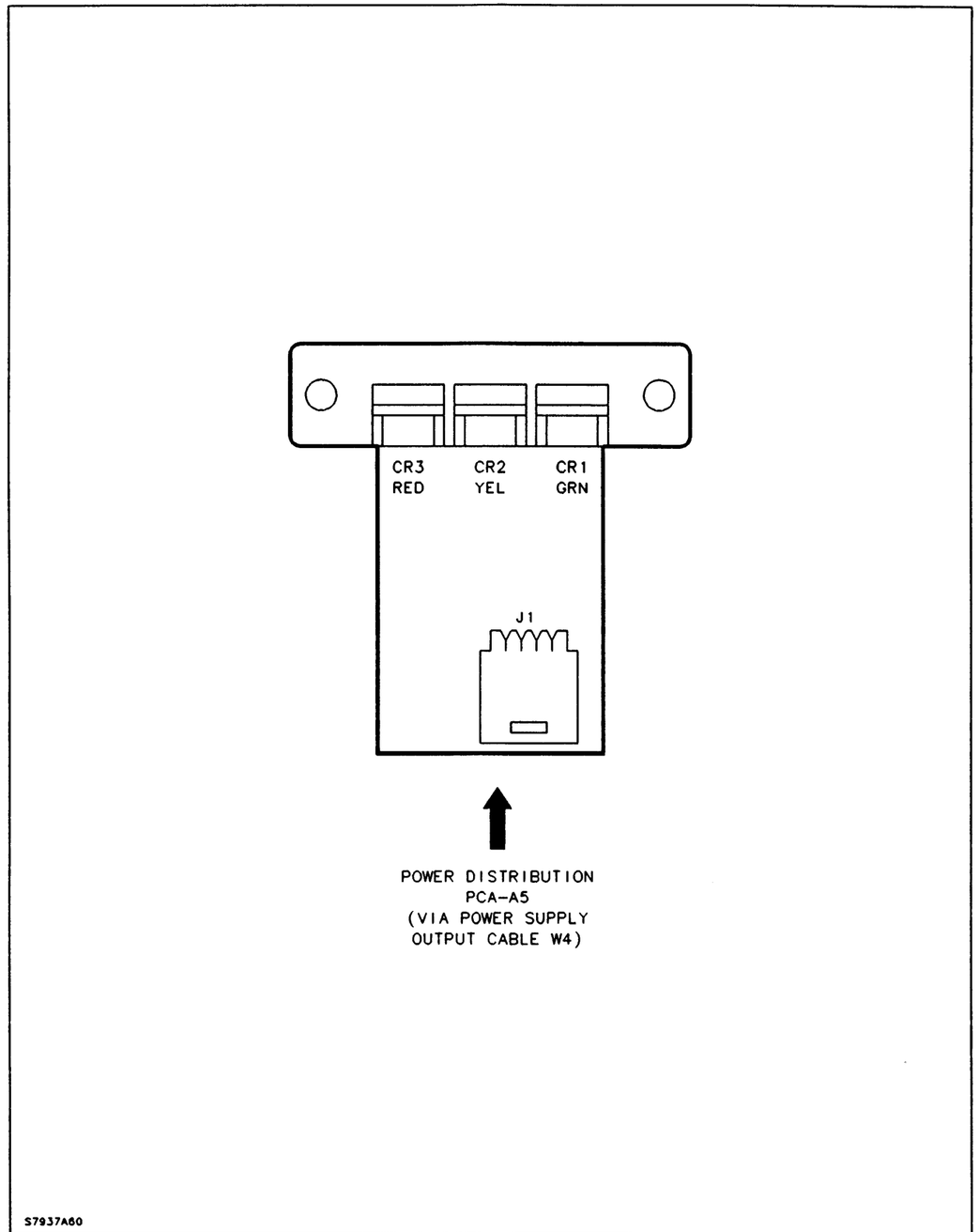
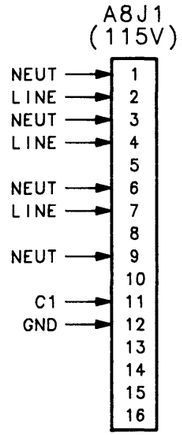
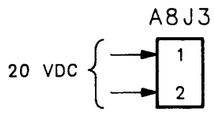
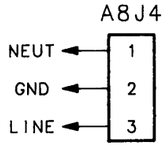
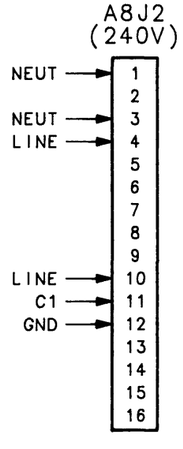


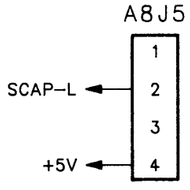
Figure 12-18. LED PCA-A7 Parts Location and Connector Pinout

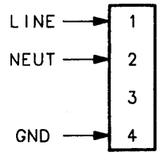


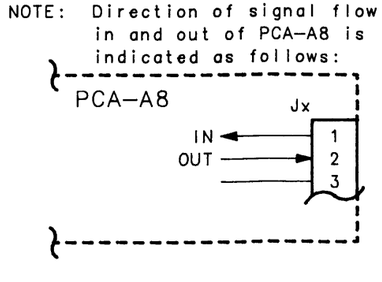












S7937A61

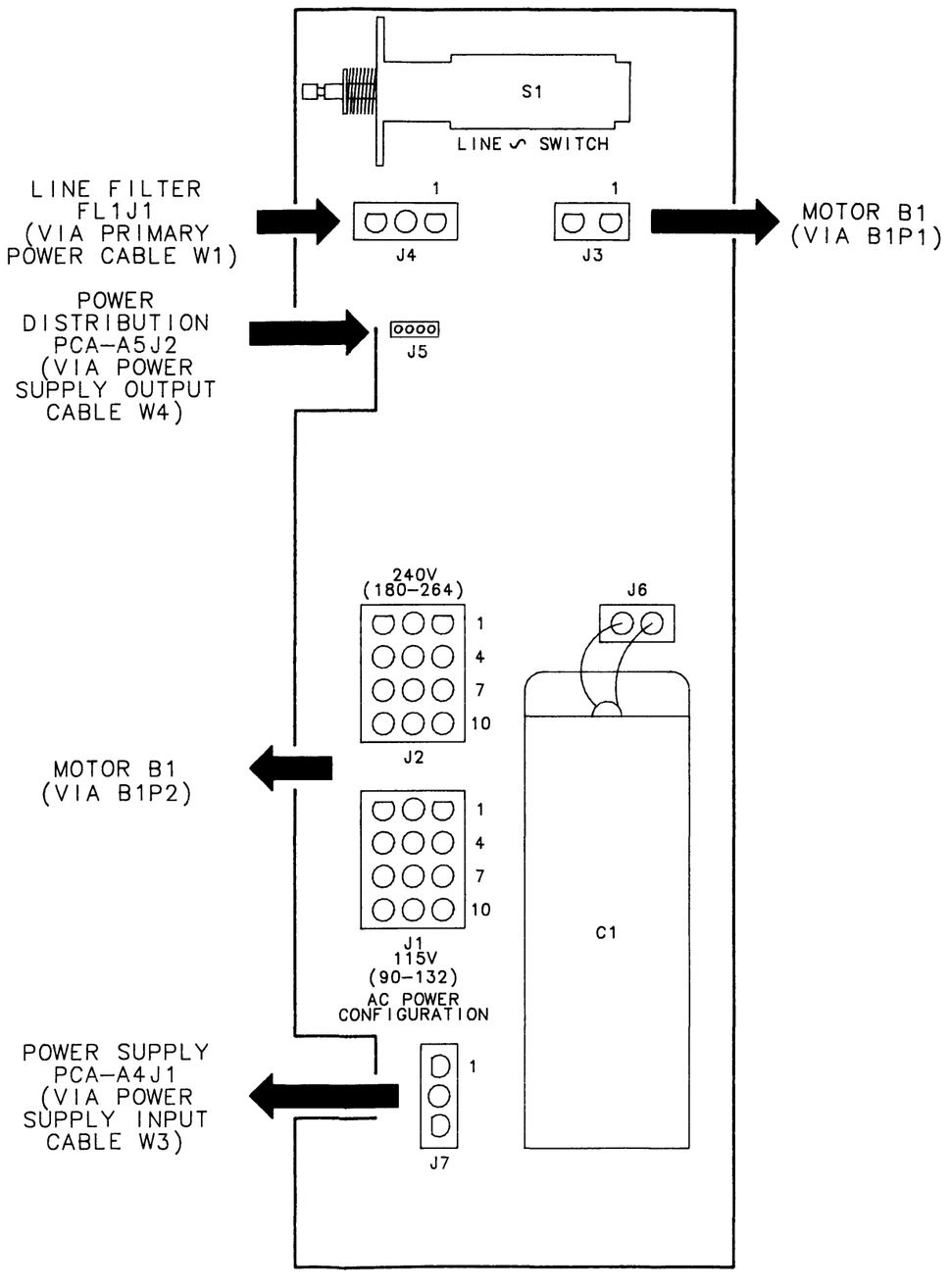


Figure 12-19. Primary Power PCA-A8, Parts Location and Connector Pinout

HEAD–DISC ASSY A3
(SEE **RW**)

DAC

HEAD GAIN REFERENCE PROM

DAR A3J1 4
SGR 8

W8P2 W8 W8P1

R/W PCA–A2
(SEE **RW**)

SAMPLED SERVO AGC AMPLIFIER

SMPN A2P2 31,32
SMPP 29,30
SAGC 25,26
DAR 8
SGR 7

A2J7

BUFFER

DWC–H 49
DSOS–L 48
DWC–L 50
DSOS–H 47

R/W CONTROLLER IC

SRVER–L 45

SAMPLED SERVO SWITCH

SSEN–L 3
SSEN–H 4

READ CHAIN AGC CKT

RAGC–L 1
RAGC–H 2

DEDICATED SERVO AGC AMPLIFIER

DEDP 13,14
DEDN 15,16
DAGC 19,20
DIDO 5
DID1 6

DRIVE ID CIRCUIT

DIDO A3J1 25
DID1 42

W8P2 W8 W8P1 36 19

SERVO PCA–A1

A1J2
SMPN
SMPP
SAMPLED SERVO FILTER
SAMPLED SERVO AMP
SSRVN
SSRVP
43
SAGC
AGC INTEGRATOR
SLVL
AGCF–L
1
25
40
26
DAR
6.25V REF
AGC REF DEMOD SWITCH
SGR
GAP–L
SRG
SAMPLED AGC REF CKT

A1J1

SRG
DEDICATED AGC REF CKT

DEDICATED SERVO CIRCUIT

DEDICATED SERVO FILTER
DEDICATED SERVO AMP
13
DSRVN
DAGC
46
AGC INTEGRATOR
DLVL
9
POSITION DEMODULATOR
DPOS
ASMP
TERR1–L
TERR2–L
7
2–BIT ADC
OFTU–L
SRVER–L
29
FAULT LATCHES
SRTF–H, OFTRK–H
49
CLSER–L
CLER–L

5,35
TERR1–L,TE
SECTOR MARK DECODER
14
16
DB

SDO–SD7
SRD–L
SWR–L
SBF–L
SDAV–L
SPR–L
DIDO
DID1
39
TEST ENABLE (FROM REAR PANEL SW)

CONTROLLER PCA–A6
(SEE **CR**)

SERVO CONTROL BUS

A6P1 A2J1 A2P1 A1J1

SDO–SD7 1–8 SDO–SD7 8 25–32
SRD–L 12 SRD–L 35
SWR–L 11 SWR–L 36
INDEX–H 15 INDEX–H 39
SBF–L 13 SBF–L 38
SDAV–L 14 SDAV–L 37
SPR–L 16 SPR–L 44

S7937A25

) PCA–A1

SAMPLED SERVO CIRCUIT

SMPN
SMPP
SAMPLED SERVO FILTER
SAMPLED SERVO AMP
SSRVN
SSRVP
POSITION DEMODULATOR
SPOS
37
2
SSDEMOD–H
SSGT–L
SDMP–H
1
25
SAGC
SLVL
AGC INTEGRATOR
AGCF–L
40
26
DAR
6.25V REF
AGC REF DEMOD SWITCH
SGR
GAP–L
SSRVP
GAP–L
RAGC–H
RAGC–L
SSEN–H
SSEN–L
DSOS–H
DSOS–L
INDEX–H
SAMPLED SERVO TIMING/ FAULT DETECTION
ACQUIRE–H
SOSEN–L
GDCLK
SSGT–L
34
36
SSSL–H
SRG
SAMPLED AGC REF CKT
SRG
DEDICATED AGC REF CKT
5,35
48
TERR1–L, TERR2–L
SMDT–H
SECTOR MARK DECODER
14
16
WC–H
DWC–L
DWC–H
DBGT–H, SMCLK, ZCLK
GBD
DSRVP
ASMP–L, BSMP–L, DMP–H
DEDICATED SERVO TIMING & PLL
GBDEN–H
LCK–L
QUAD–H
LSB–H
GBD–H
SAMPLED/ DEDICATED SELECT SWITCH
SPOS
SSSL–H
PES
21
DPOS
SLEW RATE LIMIT AMP
SLEW RATE LIMIT SWITCH
SLPES
17
OFTU–L
OFF TRACK DETECTOR
23
24
DC OFFSET
31
OFTU–L
45
FILTER
DPOS
GDCLK
TO SHEET 2 (S2)

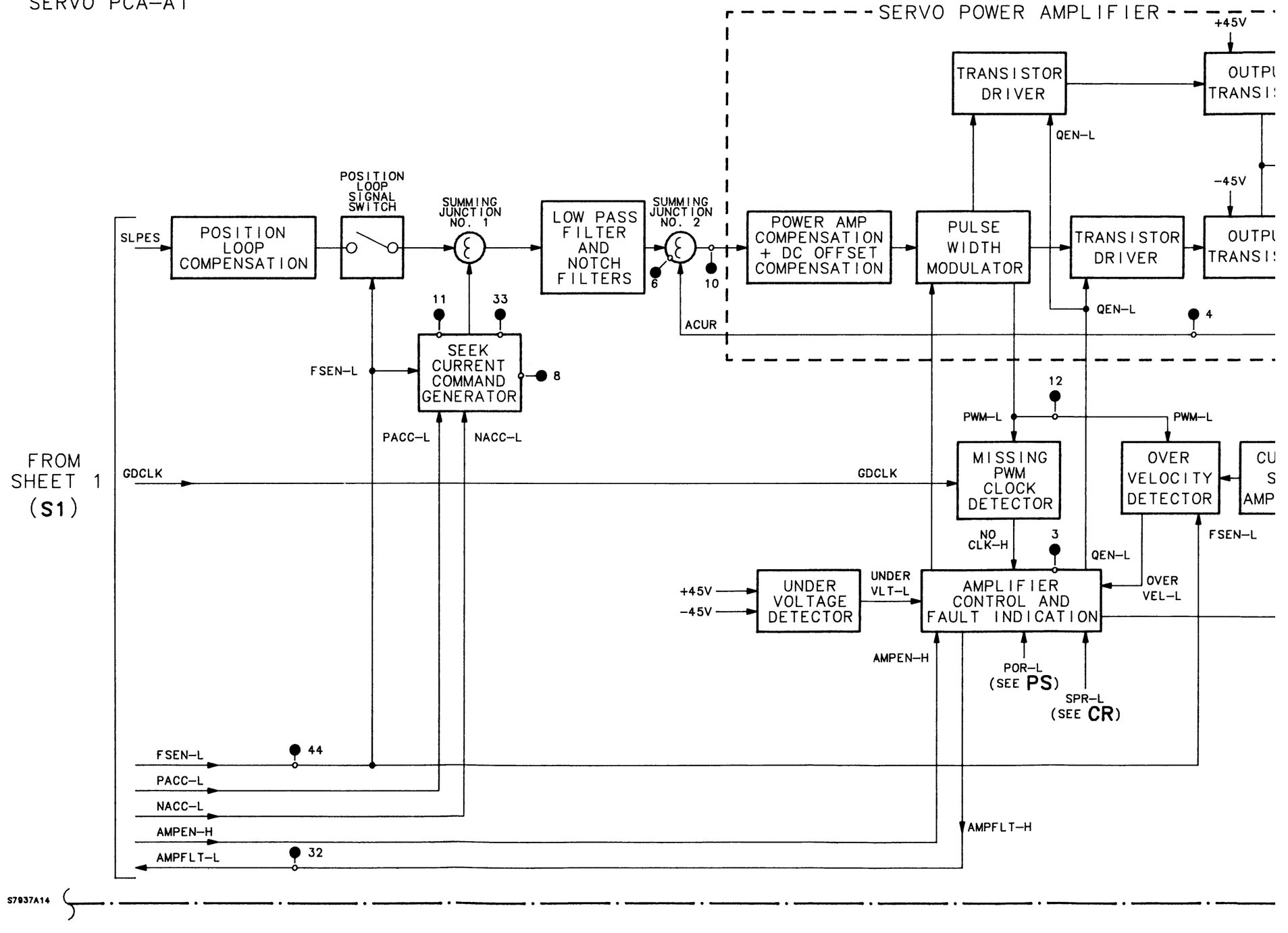
DEDICATED SERVO CIRCUIT

DEDICATED SERVO FILTER
DEDICATED SERVO AMP
13
DSRVN
DAGC
46
AGC INTEGRATOR
DLVL
9
POSITION DEMODULATOR
DPOS
7
TERR1–L
TERR2–L
DPOS
2–BIT ADC
DPOS
TRACK CROSSING DETECTOR
38
27
28
47
OFTU–L
SRVER–L
29
FAULT LATCHES
SRTF–H, OFTRK–H
49
CLSER–L
CLER–L
TRKCR–H
50
SSSL–H
GBDEN–H
ACQUIRE–H
42
SOSEN–H
LCK–L
QUAD–H
LSB–H
GBD–H
SSGT–L
AGCF–L
SD0–SD7
SRD–L
SWR–L
SBF–L
SDAV–L
SPR–L
DID0
DID1
SERVO CONTROLLER
41
44
32,22
FSEN–L
PACC–L
NACC–L
AMPEN–H
AMPFLT–L
39
TEST ENABLE (FROM REAR PANEL SW)

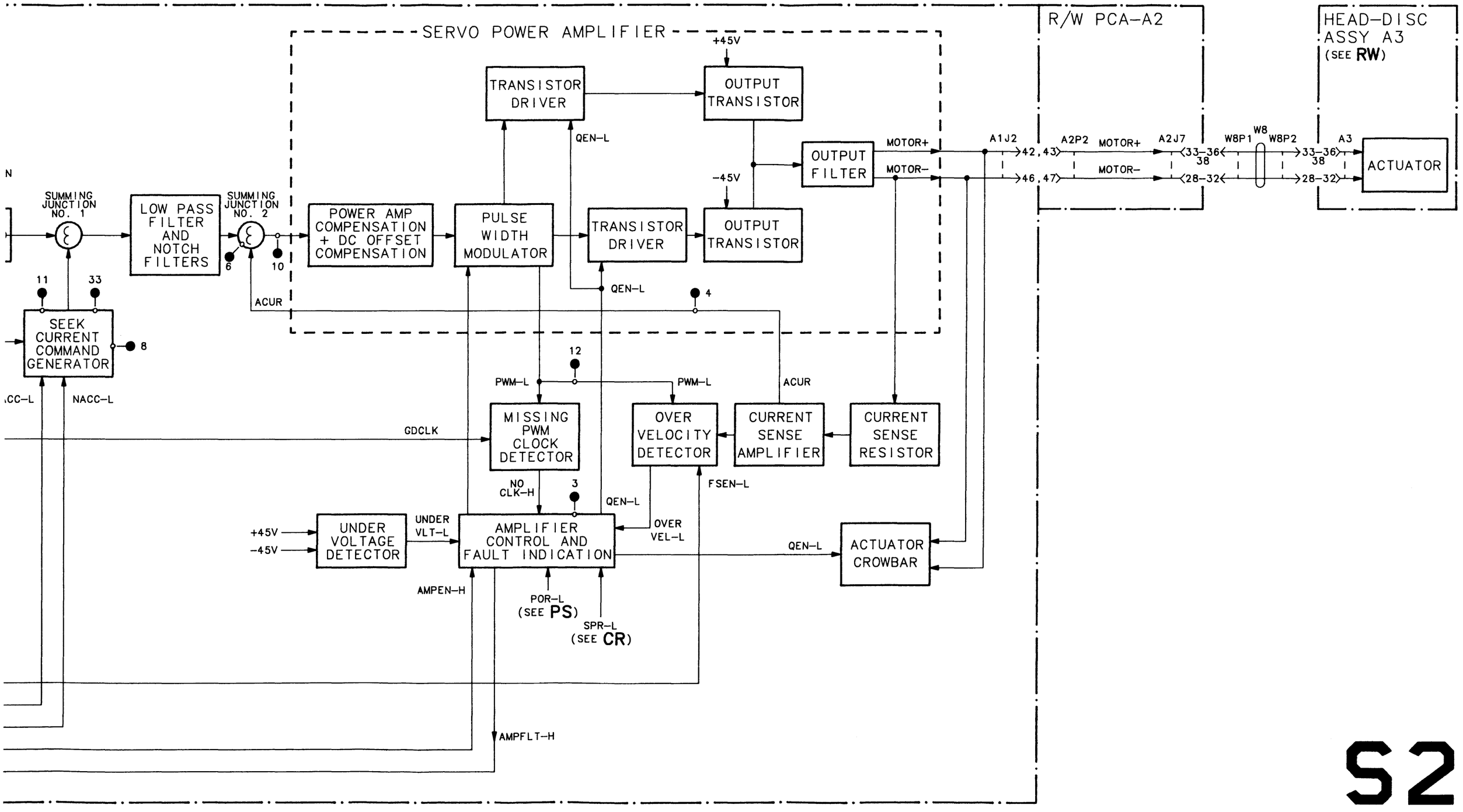
S1

Figure 12-20. Servo System, Functional Block Diagram (Sheet 1 of 2)

SERVO PCA–A1



S7937A14



S2

Figure 12-20. Servo System, Functional Block Diagram (Sheet 2 of 2)

CONTROLLER PCA–A6
(SEE **CR**)

R/W PCA–A2

SERVO PCA–A1
(SEE **S1**)

DATA PATH CONTROL BUS
DPC0–DPC7 8 A6P1 23–30 A2J1 8
DPRHW–L 35
DPA0–H 38
DPCS–L 33
DPIRQ–L 36 6

DISC DATA BUS
DD0–DD7 8 45–52
DDS–H 41
SEF–L 40
WHO–L 37
SOS–L 19 13

FAULT LATCHES
DEDICATED SERVO TIMING
SAMPLED SERVO TIMING
SRVER–L A1J1 45 A2P1 SRVER–L
DWC–H 49
DWC–L 50
DSOS–H 47
DSOS–L 48
BUFFER
SOS–L
WCLK–L
BSOS–L

+6.25V REF.
AGC REF DEMOD SWITCH
SAMPLED SERVO TIMING
SAMPLED SERVO FILTER
SAMPLED AGC INT.
DEDICATED SERVO FILTER
DEDICATED AGC INT.
DAR A1J2 8 A2P2
SGR 7
RAGCG–L 1
RAGCG–H 2
SSEN–L 4
SSEN–H 3
SSMPP 29,30
SSMPN 31,32
SAGC 25,26
DEDN 15,16
DEDP 13,14
DAGC 19,20

R/W CONTROLLER IC

CONTROL SECTION
ADDRESS REGISTER
STATUS REGISTER
FAULT DETECT
COMMAND REGISTER
OPERATION REGISTER

ENCODER/DECODER SECTION
SHIFT REGISTER
PATTERN DETECTOR
BIT GENERATOR
CLOCK GENERATOR
BYTE COUNTER

DPC0–DPC7
DPRHW–L
DPA0–H
DPIRQ–L
DPCS–L
DPC0–DPC7
SRVER–L
WHO–L
SOS–L
SOS–L
DPC0–DPC7
DD0–DD7
SEF–L
DDS–H
WCLK–L
RDCLK–H
2
1

CHIP0–H/CHIP3–H 4
HDS1–H,HDS2–H 2
WCS0,WCS1 2
DPIRQ–L 8
3
CURUS–H
4
SOS–L
WGTO–L 10
RDATA
WDATA–H 12
RDEN–H 11
–5.2V 7
AGND 5
DGND 16

CURUS–H
UNSAFE DETECTOR
US

CHIP0–H
CHIP1–H
CHIP2–H
CHIP3–H
HDS1–H
HDS2–H
HEAD SELECT ENCODER
HS1–L
HS2–L
CE0–L
CE1–L
CE2–L
CE3–L
CH0–H
CH1–H
HDS2–H
HDS1–H

WCS0
WCS1
WDATA–H
WGTO–L
WRITE CHAIN
WS
WC
SHS–
DX
DY

READ CHAIN
RDATA
RDCLK–H
DWC–H, DWC–L
PLL + DATA SEPARATOR
9
NRZ–H
ZERO CROSSING DETECTOR
RDEN–H
15
RAGC–L
RAGC–H
WGTO–L
AGC CIRCUIT
14
FILTER + AMPLIFIER
DX
DY
AGC

SMPN
SMPP
SAGC
SAMPLED SERVO AGC AMPLIFIER
SAMPLED SERVO SWITCH
DX
DY
SSEN–L
SSEN–H

SERVO AMPLIFIERS
DEDP
DEDN
DAGC
DEDICATED SERVO AGC AMPLIFIER

S7937A28

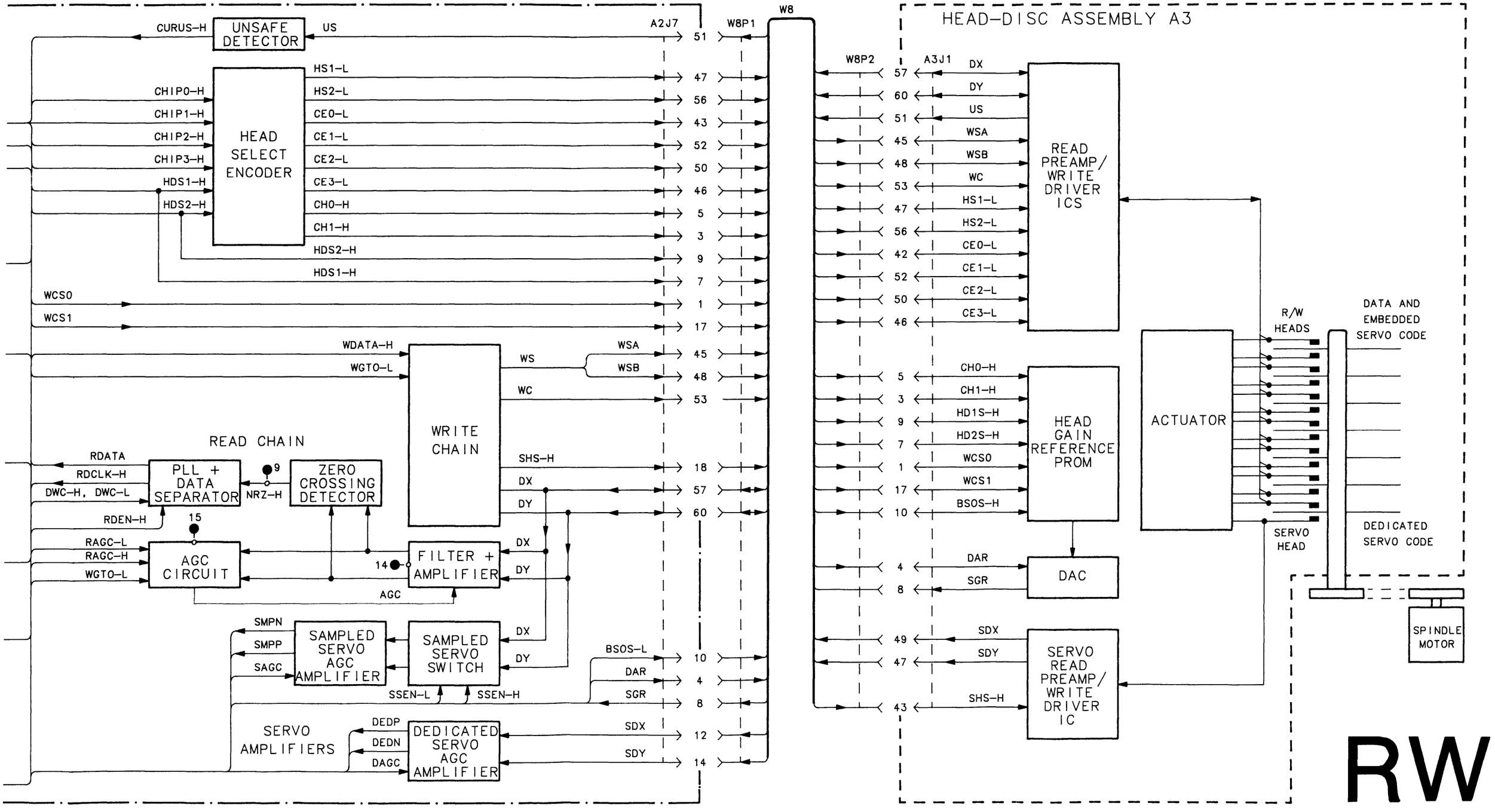
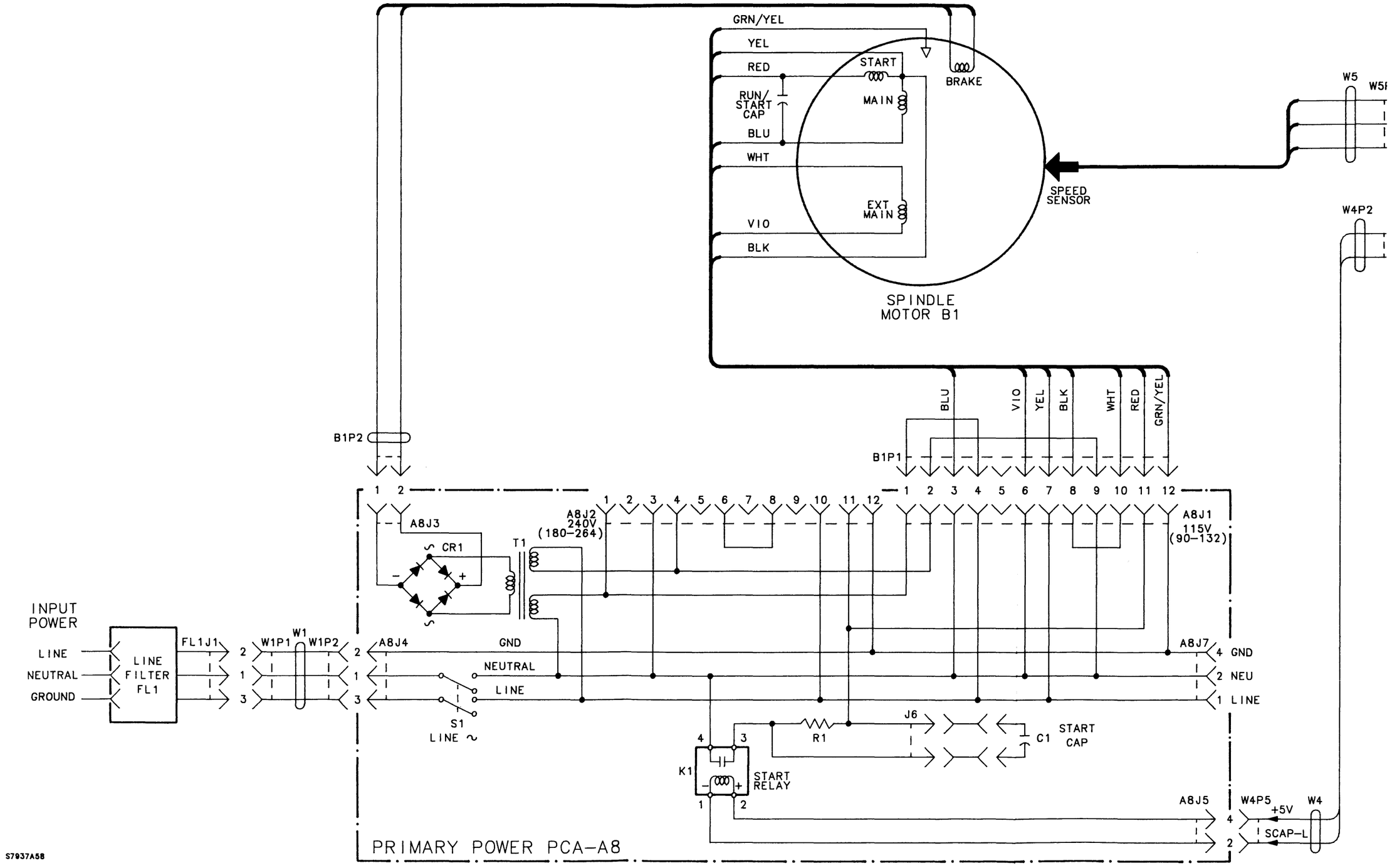
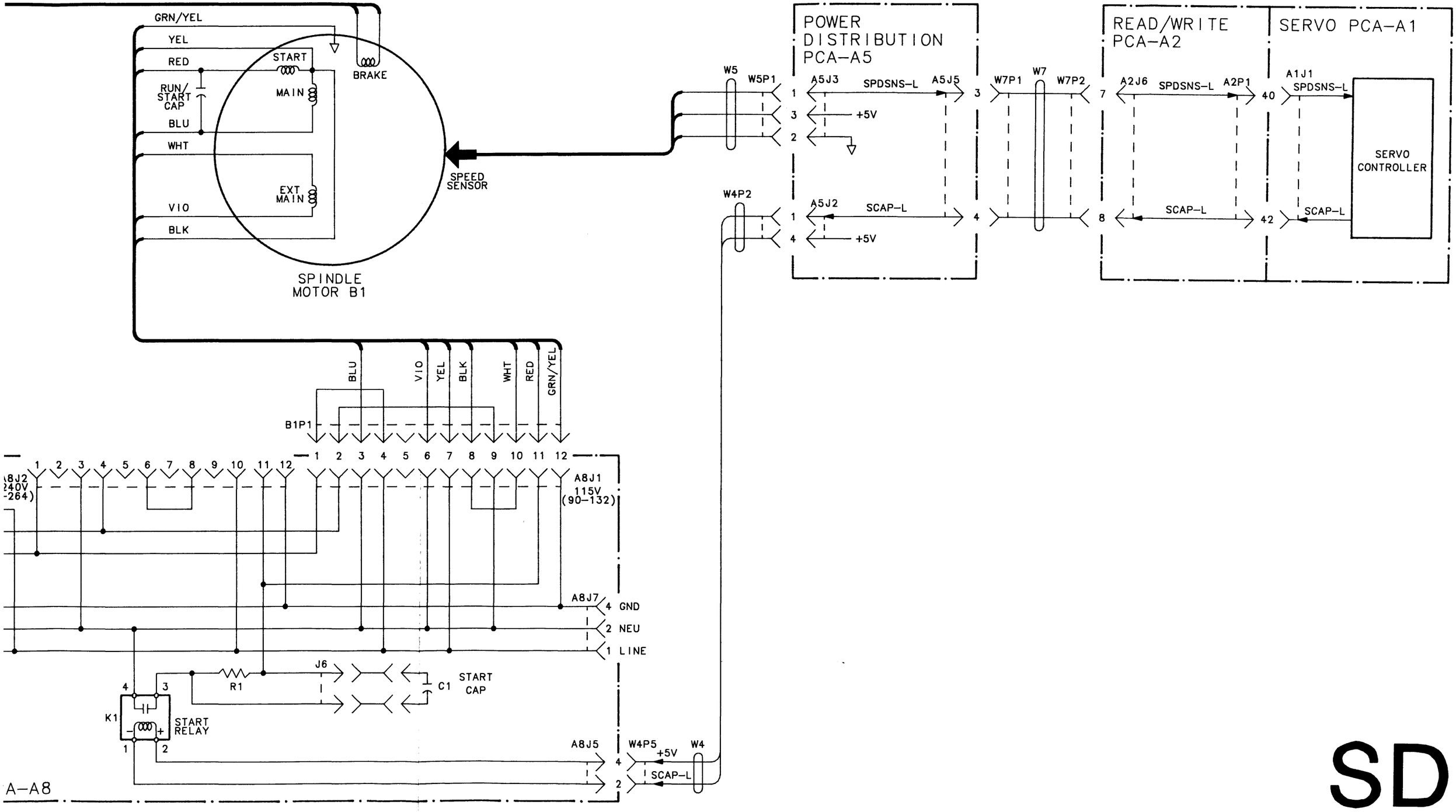


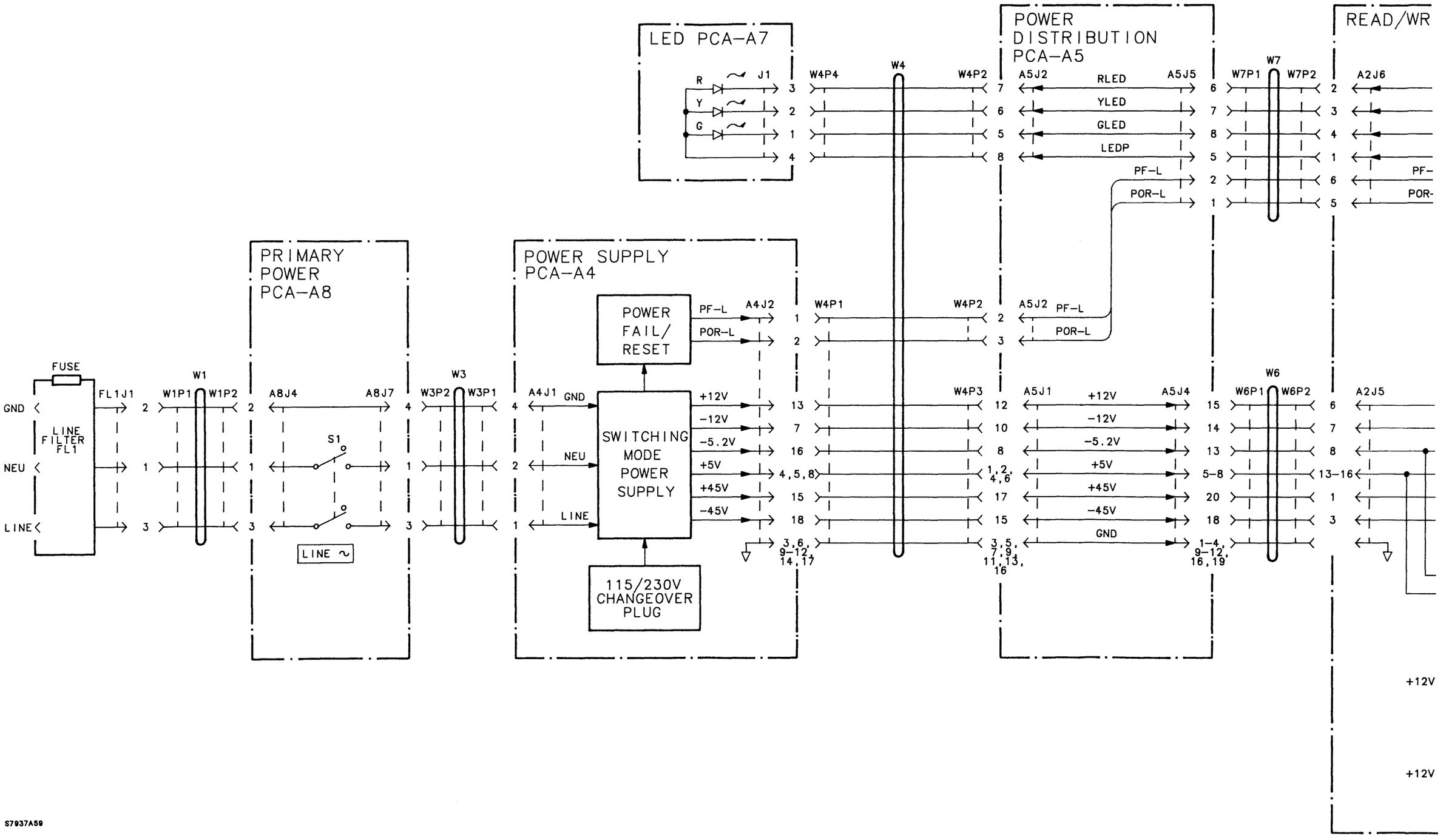
Figure 12-21. Read/Write System, Functional Block Diagram


GRN/YEL
YEL
RED
RUN/
START
CAP
BLU
WHT
VIO
BLK
START
MAIN
EXT
MAIN
BRAKE
SPEED
SENSOR
W5
W5P1
SPINDLE
MOTOR B1
W4P2
BLU
VIO
YEL
BLK
WHT
RED
GRN/YEL
B1P2
B1P1
A8J3
CR1
T1
A8J2
240V
(180-264)
A8J1
115V
(90-132)
INPUT
POWER
LINE
NEUTRAL
GROUND
LINE
FILTER
FL1
FL1J1
W1
W1P1
W1P2
A8J4
GND
NEUTRAL
LINE
S1
LINE ~
A8J7
GND
NEU
LINE
J6
R1
C1
START
CAP
K1
START
RELAY
A8J5
W4P5
+5V
SCAP-L
W4
PRIMARY POWER PCA-A8
S7937A58



SD

Figure 12-22. Spindle Drive System, Functional Block Diagram


LED PCA-A7
R
Y
G
J1
POWER DISTRIBUTION PCA-A5
READ/WR
W4
W7
W6
W4P4
W4P2
W7P1
W7P2
A2J6
A5J2
A5J5
RLED
YLED
GLED
LEDP
PF-L
POR-L
PF-
POR-
PRIMARY POWER PCA-A8
POWER SUPPLY PCA-A4
FUSE
GND
NEU
LINE
LINE FILTER FL1
FL1J1
W1
W1P1
W1P2
A8J4
A8J7
S1
LINE ~
W3
W3P2
W3P1
A4J1
POWER FAIL/ RESET
A4J2
SWITCHING MODE POWER SUPPLY
115/230V CHANGEOVER PLUG
+12V
-12V
-5.2V
+5V
+45V
-45V
W4P1
W4P3
A5J1
A5J4
W6P1
W6P2
A2J5
GND
3,6, 9-12, 14,17
1,2, 4,6
3,5, 7,9, 11,13, 16
1-4, 9-12, 16,19
13-16
5-8
+12V
+12V

S7937A59

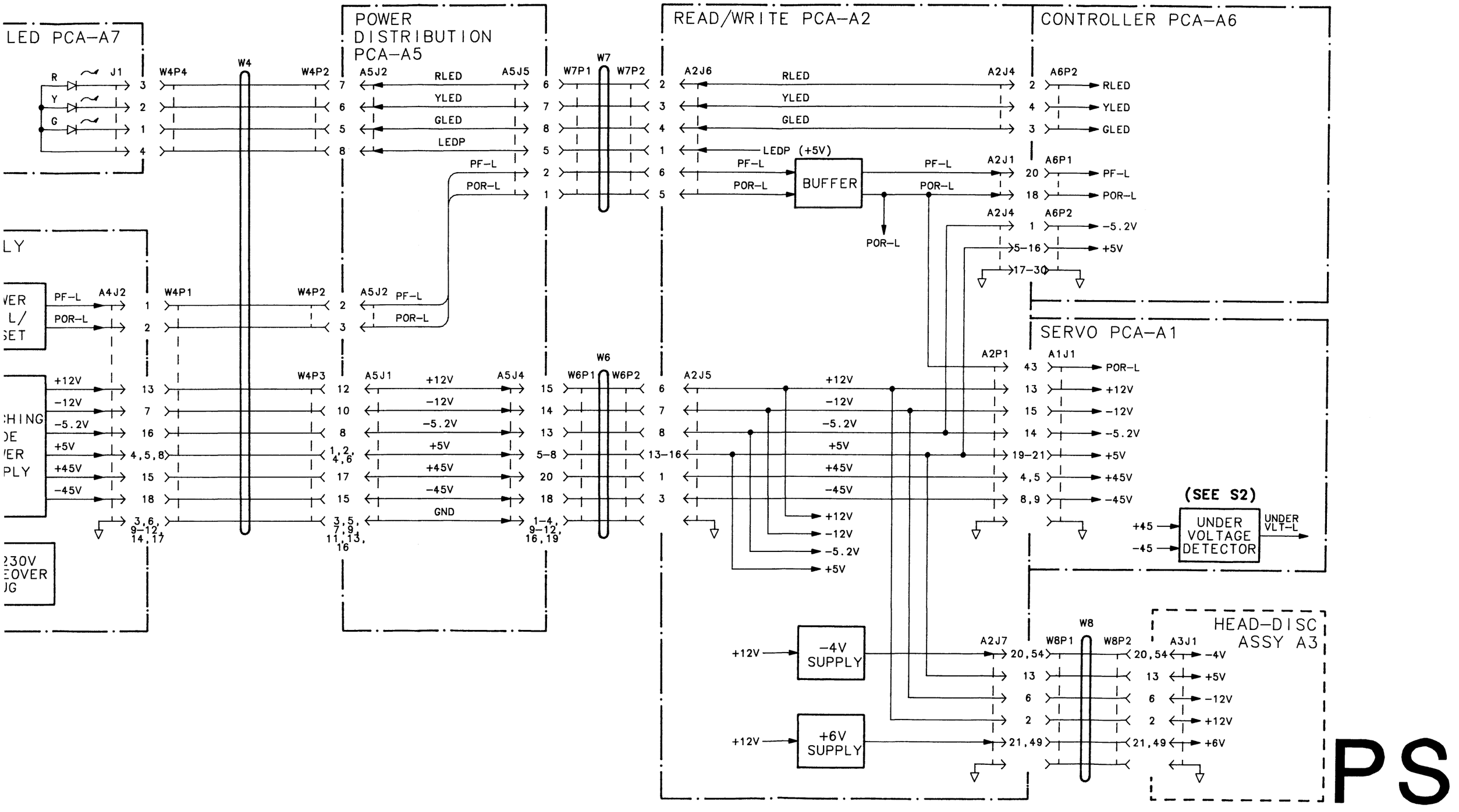


Figure 12-23. Power Supply System, Functional Block Diagram

HP-IB Controller A

A-1. INTRODUCTION

The HP 7936H, HP 7937H, HP 7936XP, and HP 7937XP Disc Drives are configured for use on an HP-IB channel. These drives are equipped with an HP-IB Controller PCA-A6 which provides the electrical and mechanical interface between the HP-IB channel and the drive. The host system communicates with the controller using the CS/80 Instruction Set, a command set created for mass storage devices. The controller translates the CS/80 protocol into the necessary format for communication with the drive over an HP-developed standard interface (ESI).

This appendix begins with an overview of the controller interfaces, followed by a functional description of the controller PCA. The controller description includes information on both the hardware and firmware architecture. Functionally, the H-model controller and the XP-model controller are similar. The main difference between the two is the addition of 2 megabytes of cache RAM on the XP's controller PCA. All functional information, except that concerning caching, applies to both controller PCAs.

A-2. CONTROLLER INTERFACES

Host/controller communication takes place over the HP-IB channel; controller/drive communication is conducted over the ESI. A third interface, the human interface, transfers signals between the controller and various drive switches and the front panel LEDs.

A-3. HP-IB

The Hewlett-Packard Interface Bus (HP-IB) provides a standardized method of connecting separate devices. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cable connects all controllers and other devices of the system in parallel.

The Hewlett-Packard Interface Bus (HP-IB) has certain rules which must be followed for successful installation of the disc drive. Cabling is limited to 1 metre per HP-IB load. Typically the Central Processing Unit (CPU) is 7 equivalent loads and the disc drive is 1 equivalent load.

The CPU adheres to an HP standard which allows 7 metres of HP-IB cable between the CPU and the nearest device connected to it and 1 metre of cable between each additional device. The maximum configuration is eight devices (not including CPU) per HP-IB channel or a maximum of 15 metres or 15 equivalent loads.

The HP-IB permits transfer of commands and data between the components of a system on 16 signal lines (see figure A-1). The eight Data I/O lines are reserved for the transfer of commands, data, and other messages in a byte-serial, bit-parallel manner. Data and message transfers are asynchronous, coordinated by three handshake lines: Data Valid (DAV-L), Not Ready For Data (NRFD-L), and Not Data Accepted (NDAC-L). The other five lines are for bus management.

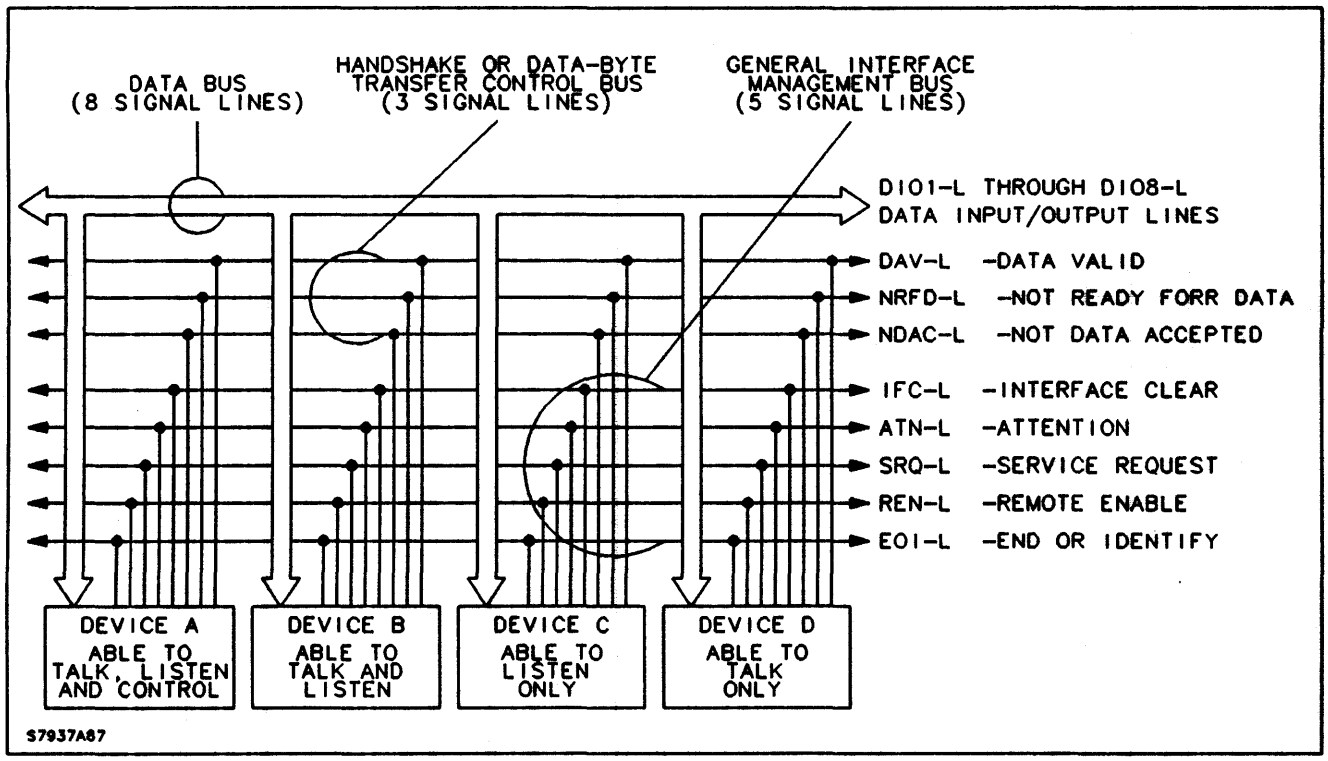


Figure A-1. HP-IB Signal Lines

Information is transmitted on the data lines under sequential control of the three handshake lines (DAV-L, NRFD-L and NDAC-L). No step in the sequence can be initiated until the previous step has been completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed. This permits several devices to receive the same message byte concurrently.

Devices connected to the bus may be talkers, listeners, or controllers (refer to table A-1). The Controller-In-Charge (CIC) dictates the role of each of the other devices by setting the Attention (ATN-L) line low and sending talk or listen addresses on the data lines. Addresses are set for each device at the time of system configuration. While the ATN-L line is low, all devices must listen to the data lines. When the ATN-L line is high, devices that have been addressed will send or receive data; all others ignore the data lines. Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN-L is low), all other talkers will be automatically unaddressed.

The Interface Clear (IFC-L) line places the interface system in a known quiescent state. The Remote Enable (REN-L) line is used to select between two alternate sources of device programming data such as the front panel or the HP-IB. The End Or Identify (EOI-L) line is used to indicate the end of a multiple-byte transfer sequence. In addition, when a CIC sets both the ATN-L and EOI-L lines low, each device capable of a parallel poll responds on the DIO line assigned to it.

Table A-1. HP-IB Definitions

HP-IB TERM	DEFINITION	CONSIDERATIONS
TALKER	Any device which sends information over the HP-IB.	There can be only one TALKER sending information over the HP-IB at a time.
LISTENER	Any device which receives information over the HP-IB. Some devices can function as LISTENERS or TALKERS.	In a parallel poll system, there can be up to 8 LISTENERS receiving information over the HP-IB at the same time.
CONTROLLER	Any device that has been programmed to manage data flow between the TALKER and the LISTENER(s) in addition to being a TALKER and a LISTENER.	The CONTROLLER manages data flow by addressing one device as a TALKER and one or more devices as LISTENERS. There can be only one active CONTROLLER on the HP-IB at at any time. The active CONTROLLER is called the CONTROLLER-IN-CHARGE (CIC).
SYSTEM CONTROLLER	Any device that functions as a CONTROLLER and is able to gain absolute control of the HP-IB with the Interface Clear (IFC) signal.	There can be only one SYSTEM CONTROLLER connected to the HP-IB.

A-4. HP-IB COMMUNICATIONS. This section describes the formats and sequences for the HP-IB commands, messages, and transactions that occur between the CIC and the disc drive. The following list explains the terms used in this section.

COMMAND -- A parcel of information transmitted over the channel (HP-IB) relating to a specific operation. Channel commands (usually a single byte) are used to manage operations on the interface channel. Device commands (usually more than one byte) are used to control the operation and are contained within the text of a command message.

UNIVERSAL COMMAND -- A channel command that causes all devices on the bus to perform a predetermined interface function. Refer to table A-2.

PRIMARY COMMAND -- The primary I command is a channel command that begins the message sequence (refer to table A-3). It contains the command to listen or talk and the address of a particular device. The primary II command terminates the message with an unlisten or untalk command.

Table A-2. Universal Command Formats

UNIVERSAL COMMAND	UNIVERSAL DEVICE CLEAR
ATN [P001CCCC] P=Parity Bit CCCC=Command Code	ATN [P0010100] P=Parity Bit

SECONDARY COMMAND -- The secondary command sets up the action required of the disc drive in the text of the message.

TEXT -- The text of the message can be 1 to n bytes depending on the required action. The required action can be to receive further qualifying information or instructions (such as a device command), to receive write data, to send read or status data, or to perform a specific operation such as a CLEAR.

MESSAGE -- A unique sequence of command and text bytes transmitted over the channel during which the communication link between the devices (for example, CIC and the disc drive) remains unbroken.

COMMAND MESSAGE -- A single message containing all the information required to address a device and initiate an operation, set up a programmable parameter, or set up an operation to be executed by an execution message.

EXECUTION MESSAGE -- A single message containing all the information required to carry out an operation previously set up by a command message.

TRANSACTION -- A complete process or operation carried out over the channel. Some transactions are completed with only a command/reporting message, and some require a command, execution, and a reporting message.

A-5. CHANNEL MANAGEMENT. The following techniques are used by the CIC to manage the HP-IB: Parallel Poll and Universal Device Clear.

A-6. Parallel Poll. The CIC conducts a parallel poll on the HP-IB by asserting ATN-L and EOI-L simultaneously. Each device requiring service can then respond by asserting the DIO line corresponding to its address. The CIC then addresses only the device requiring service. If more than one device requires service, the CIC addresses the device with the highest priority (lowest address) first. Parallel Poll Enable (PPE) and Parallel Poll Disable (PPD) are internal states of the disc drive controller. PPE occurs when the disc drive requires service from the CIC. PPD is the opposite state and occurs whenever the disc drive is active (for example, busy executing a command) or idle. A Parallel Poll Response (PPR) from the disc drive will occur if the CIC asserts both ATN-L and EOI-L and if the disc drive is in the PPE state.

A-7. Universal Device Clear. A universal command is a channel command that causes all devices on the HP-IB to perform a pre-determined interface function. Universal Device Clear erases information stored in the disc drive controller and places the disc drive in a known reset state. The universal device clear format is shown in table A-2.

A-8. MESSAGE STRUCTURE. Each message contains the following components (refer to table A-3).

- Primary I Command (unidirectional from CIC to device)
- Secondary Command (unidirectional from CIC to device)
- Text (bidirectional)
- Primary II Command (unidirectional from CIC to device)

The CIC asserts ATN-L during primary and secondary commands to distinguish them from text information. The disc drive decodes the information contained in both the primary I and secondary commands to prepare for action specified in the text.

A-9. CS/80 INSTRUCTION SET. The host uses the CS/80 Instruction Set to communicate with the drive. This instruction set increases the efficiency and speed of channel operations between disc memories and their associated host computers. Table A-4 provides a list of the CS/80 instructions supported by the drive. For details on CS/80, refer to the *CS/80 Instruction Set Programming Manual*, part no. 5955-3442.

The CS/80 Instruction Set allows the host to initiate special utilities resident within the disc drive. These utilities routines, which are stored in controller firmware, are used for diagnosing and

servicing the drive. The utilities supported by the drive are enumerated in Chapter 8.

A-10. ESI

The ESI provides the communication link between the controller and the disc drive. This communication includes disc data, control signals, and status information. The ESI also includes the operating voltages for the controller PCA.

The ESI comprises three eight-bit parallel data busses with associated control signal for each bus. The three data busses are for disc data, data path control, and servo control. The ESI also includes several additional miscellaneous signals.

Physically, the ESI consists of a 60-pin connector for the signal lines and a 30-pin connector for controller power. The controller layout and connector pin assignments are shown in figure A-4. A complete description of each ESI signal is provided in Chapter 5.

A-11. DISC DATA BUS. The disc data bus includes the following data and control lines:

- DD0-DD7 - Bi-directional 8-bit disc data bus
- DDS-H - Disc Data Strobe
- SEF-L - Start ECC Field
- SOS-L - Start Of Sector
- WHO-L - Write Hold Off

All data written to or read from the disc media is transferred over the disc data bus. Disc data is clocked over the 8-bit parallel data bus by DDS-H from the R/W PCA.

Table A-3. HP-IB Message Structure

HEADER		TEXT	TRAILER
PRIMARY I	SECONDARY	DEVICE COMMAND OR DATA	PRIMARY II
(ATN) <One Byte> Unidirectional -CIC To Device Begins Message -Addresses Device To Talk Or Listen -Universal	(ATN) <One Byte> Unidirectional -CIC To Device Set Up Device For Further Action	<One To n Bytes> Bidirectional Qualifying Instructions To Device Write Data To Device Read Data To CIC Status Data To CIC	(ATN) <One Byte> Unidirectional -CIC To Device Terminates Message Unaddresses Device -Unlisten -Untalk

Table A-4. Supported CS/80 Commands

COMMAND	TYPE	COMMAND	TYPE
LOCATE AND READ	RT	DESCRIBE	GP
LOCATE AND WRITE	RT	INITIALIZE MEDIA	GP
SET UNIT	C	SPARE BLOCK	GP
SET VOLUME	C	LOCATE AND VERIFY	GP
SET ADDRESS	C	RELEASE	GP
SET BLOCK DISPLACEMENT	C	RELEASE DENIED	GP
SET LENGTH	C	INITIATE UTILITY	GP
SET BURST	C	INITIATE DIAGNOSTIC	GP
SET RPS	C	REQUEST STATUS	GP
SET RETRY TIME	C	UNIVERSAL DEVICE CLEAR	T
SET STATUS MASK	C	SELECTED DEVICE CLEAR	T
SET RELEASE	C	CHANNEL INDEPENDENT CLEAR	T
SET RETURN		CANCEL	T
ADDRESSING MODE	C	LOOPBACK	T
NO OP	C	HP-IB PARITY CHECKING	T
		IDENTIFY	T

RT = REAL TIME; C = COMPLEMENTARY; GP = GENERAL PURPOSE;
T = TRANSPARENT

SOS-L is a timing signal from the servo PCA-A1 which defines the beginning and end of the sector data field. The SEF-L signal, generated by the drive R/W system, indicates when a sector's ECC field is about to begin. WHO-L is used by the controller to abort an impending data transfer.

A-12. DATA PATH CONTROL BUS. The data path control bus includes the following signals:

- DP0-DP7 - Bi-directional 8-bit control data bus
- DPRHW-L - Data Path Read/Write
- DPA0 - Data Path Address Zero
- DPCS-L - Data Path Control Select
- DPIRQ-L - Data Path Interrupt Request

The data path control bus is used to transfer control and status information between the controller and the R/W PCA. The controller sends command data to the R/W PCA over the 8-bit control data bus. Each sector of disc data to be transferred must be preceded by a command establishing the appropriate operation (read or write) for that sector.

The controller uses the data path control system to communicate with three registers on the R/W PCA. The appropriate register is selected by the controller using DPA0. When DPA0 is high, the R/W address register is selected. This register is loaded with head address and cylinder address information. The controller can also read this register (DPRHW-L high) to verify its operation.

When the controller performs a write operation (DPRHW-L low) with DPA0 low, a byte of command data is latched into the R/W PCA command register. The contents of this register define

whether a read or write operation will be performed. When the controller performs a read operation with DPA0 low, the R/W PCA returns the contents of its status register, which contains information about error conditions which may have occurred during data transfer operations. Bits set in the status register cause the DPIRQ-L signal to go true at the end of the sector in which the fault occurred. DPIRQ-L is an interrupt input to the controller microprocessor.

The controller enables the output of the R/W PCA registers by asserting DPCS-L.

A-13. SERVO CONTROL BUS. The servo control bus includes the following signals:

- SD0-SD7 -Bidirectional 8-bit servo data bus
- SRD-L - Servo Read
- SWR-L - Servo Write
- SDAV-L - Servo Data Available
- SBF-L - Servo Buffer Full
- SPR-L - Servo Processor Reset

The servo control bus is used to transfer command and status information between the controller and the Servo PCA. Servo commands and status are transferred over the 8-bit servo data bus. The Servo PCA controls the transfer of data over this bus through the use of the associated control signals.

The controller indicates that it has a command for the servo system by asserting SDAV-L. The servo PCA responds by toggling SRD-L to read the two command bytes from the controller's servo interface buffer. When the servo operation is complete, the servo PCA loads two bytes of status information into the controller interface buffer by toggling SRW-L. If the servo interface buffer is full, the controller asserts SBF-L, indicating to the Servo PCA that no additional status bytes can be accepted.

The SPR-L signal resets the servo system microprocessor.

A-14. MISCELLANEOUS SIGNALS. Included in the ESI architecture are three miscellaneous signals:

- INDX-L - Index
- POR-L - Power On Reset
- PF-L - Power Fail

INDX-L is a timing signal generated by the servo PCA-A1 that defines the beginning of the track (physical sector 0). This signal is used by the controller when formatting the disc media.

The remaining two signals indicate the status of the drive power supply: POR-L is used to reset hardware circuits at power-on. In addition, POR-L will also go low if any power supply voltage drops out of regulation. The PF-L signal indicates that the input power has been removed and that the power supply will soon lose regulation.

A-15. HUMAN INTERFACE

The human interface includes inputs to the controller from four drive switches, and outputs to the drive front panel LEDs. The switches include three used to set the HP-IB address and one used to force a selftest at power-on. The outputs to the LEDs provide the operator with a visual indication of the current status of the drive. The significance of the LED patterns is described in Chapter 8.

A-16. FUNCTIONAL OPERATION

The following paragraphs describe how the controller performs its primary functions. These functions include power-on, head positioning, writing and reading data, and error correction. The descriptions include the involvement of both the hardware and firmware (refer to figures A-2 and A-3).

NOTE

The controller recognizes "optimized" Read and Write command sequences from the host. Optimized commands are decoded by the channel module; all other commands are decoded by the the command preprocessor (refer to paragraph A-44). The following functional descriptions assume the optimized command case.

A-17. POWER-UP

At power-on, the drive power supply asserts Power-On Reset (POR-L). This signal causes the starting address of the drive initialization routine to be loaded into the controller microprocessor's program counter. The processor begins executing the initialization routine, which performs the following sequence of operations:

1) Initialize all drive hardware, including the controller PCA hardware.

2) Test the controller PCA. This includes the processor hardware (e.g., clocks, timers, ROM, RAM) and all interface hardware. If a controller hardware test fails, the front panel LEDs indicate the fault (all illuminated) and the controller firmware enters an infinite loop.

3) Configure the multi-tasking executive operating system. This includes setting up the executive data structures and initializing variables.

The initialization firmware routine now transfers control to the multi-tasking executive. The first task scheduled by the executive is the initialize task, which continues the drive initialization:

4) Perform functional tests of drive systems. This includes the servo system, the read/write system, and the data transfer path from the disc to the HP-IB Interface, including the DMA hardware.

5) Recover the spare table. Even if the functional tests failed, the controller will still try to recover the spare table.

Following completion of drive initialization, the controller checks the selftest switch. If the switch is in the RUN TIME MODE, the controller brings the drive on line. If all hardware functional tests were successful, the drive is ready to process commands from the host. If a functional test failed, the controller reports the failure to the host. The appropriate failure code is also passed to the front panel LEDs.

If the selftest switch is in the DIAGNOSTIC MODE, the controller does not bring the drive on line following the hardware functional tests. Instead, the drive performs a full-volume Read-Only Error Rate Test (RO ERT) followed by a continuous loop of random RO ERTs as described in Chapter 8.

A-18. HEAD POSITIONING

An integral part of any data transfer operation involves locating the desired data on the disc. The address of the target data may be included in the command message from the host. This "logical" address is converted to a "physical" address by the channel module (optimized case). Using the physical target address, the channel module calculates the direction and distance of the seek. This information is included in a two-byte seek command which the channel module loads into the servo control interface. The servo system reads the command and begins the seek.

When the seek operation is complete, the servo system returns two bytes of status to the servo control interface. The CS/80 module reads and interprets this status. If the seek was successful, the data transfer operation begins. If the status indicates a fault, the CS/80 module requests two additional bytes of status. This status gives a more detailed indication of the exact cause of the failure. Based upon the detailed status, the controller will take action to correct or report the fault.

A-19. WRITE

Under control of the channel module, the incoming optimized Write command is transferred from the HP-IB interface to the DMA buffer RAM. The command is passed to the channel module's flash decoder for decoding. Using the address included with the command, the channel module initiates a seek to the target area. The channel

module then passes the decoded command to the CS/80 module, which continues execution of the command.

While the seek is being performed, the CS/80 module informs the channel module that the execution message can begin. The channel module programs the DMA for a data transfer from the host, and prompts the host for an execution secondary. The host begins transferring data, which is stored in the DMA buffer RAM, ready for transfer to the disc once the seek is complete. The CS/80 module also programs the drive hardware to perform a read and verify operation once the target track is reached.

When the seek operation is complete and the target track has been verified, the CS/80 module programs the read/write system to perform the write by sending two bytes of data over the data path control bus. The control byte contains head address and write current information; the command byte specifies that a write operation will be performed. The CS/80 module also programs the DMA to begin the data transfer to the disc.

Data flows from the host to the disc under control of the CS/80 module. The CS/80 module must send a new Write command to the read/write system for each sector transferred. As each sector is transferred to the disc, the ECC circuit appends 12 bytes of ECC to the data. When the data transfer to the disc is complete, the DMA interrupts the CS/80 module, which then moves to the reporting state.

In the reporting state, the CS/80 module generates the status report message (QSTAT). This message is derived from status information returned from the drive servo and R/W systems. The CS/80 module sends the QSTAT to the channel module, which prompts the host for a reporting secondary. When the host accepts the reporting message, the channel module informs the CS/80 module, which enters an idle state waiting for the next command.

A-20. READ

The incoming optimized Read command is transferred by the channel module from the HP-IB interface to the DMA buffer RAM. The command is passed to the channel module's flash decoder for decoding. Using the address included with the command, the channel module initiates a seek to the desired data. The channel module then passes the decoded command to the CS/80 module, which continues execution of the command.

While the seek is being performed, the CS/80 module prepares the read/write system for the impending read by sending two bytes of data over the data path control bus. The control byte contains head address information; the command byte specifies that a read operation will be performed.

As the target data is being located, the RPS task determines when the data will be available for transfer to the host. This time is calculated from the current RPS value and the position of the heads relative to the target data. At the proper time, the RPS task alerts the CS/80 module, which in turn tells the channel module to notify the host that the execution phase of the transaction may begin. By the time the host responds with the execution secondary, the data is in the DMA buffer, ready for transfer.

When the seek operation is complete, the drive immediately begins reading data. The data is transferred to the DMA buffer RAM and verified. As the data is being read from the disc, the ECC checks the data for errors. Once valid target data is in the buffer RAM, the CS/80 module informs the channel module that the channel transfer can begin.

Data continues to flow from the disc to the host under control of the CS/80 module. The CS/80 module must send a new Read command to the read/write system for each sector transferred. When the data transfer to the host is complete, the channel module informs the CS/80 module, which then moves to the reporting state.

In the reporting state, the CS/80 module generates the status report message (QSTAT). This message is derived from status information returned from the drive servo and R/W systems. The CS/80 module sends the QSTAT to the channel module which prompts the host for a reporting secondary. When the reporting message is complete, the channel module informs the CS/80 module, which enters an idle state waiting for the next command.

A-21. ERROR CORRECTION

All data transferred between the controller and the disc is monitored by the ECC. During a write the ECC generates the 12-byte ECC field. During reads, the ECC uses these 12 bytes to detect the presence of data errors.

When an error is detected, the ECC signals the DMA that an error has occurred. The DMA logs the location of the defective sector and flags the sector as containing bad data. As long as the sector is flagged defective, it cannot be transferred to the host. The ECC also generates an interrupt which causes the executive operating system to start the error correction task.

The ECC syndromes are passed to the error correction task which uses them to perform the data correction. The defective sector is read from the DMA buffer RAM, corrected (if possible), and then returned to the buffer RAM. The error correction task then clears the sector for transfer to the host and informs the CS/80 module that the data has been corrected. The error correction task runs in parallel with the data transfer in progress; therefore, if the data is corrected before the DMA is ready to send it to the host, the flow of data to the host will not be interrupted.

If the error correction task cannot correct the data, it initiates read retrys in an attempt to recover the data. If the retrys are unsuccessful in recovering the data, the error correction task declares the sector uncorrectable and clears the defective sector for transfer to the host. The exact data read from the disc is sent to the host. The data transfer then continues to completion, but the transaction terminates with status indicating that uncorrectable data was included in the transfer.

A-22. HARDWARE ARCHITECTURE

The heart of the HP-IB controller PCA is the 68000 microprocessor, which implements the logical command set of the controller. The microprocessor circuits include memory (ROM and RAM), clocks, timers, and interrupt control. The remainder of the controller hardware supports the PCA's external interfaces: HP-IB, ESI, and the human interface. The functional blocks of the hardware architecture are shown in figure A-3.

A-23. HP-IB CIRCUITRY

The HP-IB circuits are responsible for transferring data over the host HP-IB channel. These circuits include the HP-IB Interface and a portion of the DMA.

A-24. HP-IB INTERFACE. The HP-IB interface provides the necessary electrical interface to properly transfer data over the HP-IB channel. This includes detection of all primary commands, parallel poll and identify response, and the protocol to handshake bytes on and off the bus.

All data is transferred between the interface and the DMA over a 10-bit data bus. Control signals coordinate the flow of data over this bus, and allow access to internal interface registers. The microprocessor accesses the interface through the DMA.

The HP-IB interface also provides an interrupt output which alerts the processor of conditions such as an inbound message or a Clear command.

A-25. DMA. The DMA controls the transfer of data between the host and the disc media. The DMA includes 32 kbytes of buffer RAM to allow for the different operating speeds of the HP-IB channel and the disc data bus. The buffer RAM is supported by 8 kbytes of overhead RAM which contains header and status information for each sector stored in the DMA buffer.

The DMA is divided into two independent state machines: the I/O state machine controls data transfers between the HP-IB channel and DMA buffer RAM; the disc state machine controls data transfers between DMA buffer RAM and the disc media. (The DMA disc state machine is included in the discussion of the ESI disc data interface.)

The DMA properly coordinates the HP-IB channel transfers with the disc transfers, interleaving buffer RAM accesses between the disc and the I/O state machines. Processor access control circuits allow the microprocessor access to the DMA buffer RAM to read incoming host commands, store status for output to the host, and perform error

correction. Processor accesses are allowed while disc and/or I/O operations are in progress. All internal DMA status, interrupt, and control registers are accessible to the processor. A 32 MHz input from the clock generator provides the clock for the DMA.

The DMA I/O state machine handles all transfers to and from the HP-IB interface, including both host data and processor accesses. To initiate an HP-IB channel data transfer, the processor loads internal DMA control registers with command data indicating the type of operation to perform (read or write), the length of the data transfer, and the buffer RAM location of the data. The DMA acknowledges receipt of the data from the processor and begins the HP-IB transfer. When the transfer is complete, the DMA generates an interrupt to inform the processor. If an error condition occurs during a data transfer, the I/O state machine generates a channel interrupt to alert the processor.

To maximize data integrity, the DMA I/O state machine generates a 2-byte CRC checksum for every 256 bytes of data received from the host. These bytes are appended to the data and recorded on the disc. When a read is performed, the DMA monitors the data as it is being sent to the host and again generates CRC. This CRC is compared to that generated when the sector was written to determine if an error occurred. If a CRC error is detected, the DMA interrupts the processor.

A-26. ESI CIRCUITRY

The ESI circuitry is divided into three functional groups, with each group responsible for one of the ESI busses. These groups are the disc data interface, the data path control interface, and the servo control interface.

A-27. DISC DATA INTERFACE. The disc data interface controls all data transfers between the controller and the drive read/write system. This interface includes two circuits: a portion of the DMA and the ECC.

A-28. DMA. A major portion of the ESI disc data interface is made up of part of the DMA. The DMA disc state machine handles all data transfers between the DMA buffer RAM and the ESI disc data bus, except for ECC data. The transfer of each data sector is synchronized to the SOS-L signal from the drive servo system. The data is clocked over the bus by the data strobe (DDS-H) from the R/W system.

To initiate a data transfer over the disc data bus, the microprocessor loads registers in the disc channel state machine indicating the type of operation to perform (read or write), the buffer RAM location of the data, and header information for the first sector to be transferred. The DMA acknowledges receipt of the data from the processor and begins the disc transfer.

All data is transferred over the disc data bus in full sectors, which include a 256-byte data field, 6-byte header address field, 2 bytes of CRC, and 12 ECC parity bytes. When writing data, the DMA disc state machine is responsible for generating the header address field. The header address register in the DMA is loaded by the processor at the beginning of a transfer, and then updated automatically by the DMA as each sector is written on the disc. During reads, the contents of the header address register is used to check the header read from the disc. If the header read from the disc sector does not match the header information in the register, the DMA interrupts the processor to indicate the error condition.

Additional registers in the DMA are used to keep track of which areas of the buffer RAM contain valid data. These registers are used to log the locations of sectors which require error correction. When an error occurs, the ECC alerts the DMA which logs the location of the defective sector, thus allowing the processor to locate and correct the data. The overhead RAM for the defective sector is used to flag the sector as bad. Until this flag is cleared, the sector cannot be transferred to the host.

If an error condition is detected just prior to beginning a data transfer, the DMA can abort the impending operation by asserting WHO-L. This signal also disables the ECC circuit.

A-29. ECC. The ECC generates the 12-byte ECC field which is used to correct data errors that occur when a sector is read. The ECC can correct up to six bytes (contiguous or noncontiguous) in a sector before the processor must use read retries.

While a write operation is in progress, the ECC monitors the data being transferred to the disc. The ECC performs a mathematical algorithm on this data and generates 12 ECC parity bytes, which are appended to the data field and recorded on the disc. When the sector is read, the ECC again monitors the data bus and performs the algorithm on the entire data sector, including the ECC field. The resulting 12 bytes, referred to as syndromes, indicate whether an error has occurred. When an error occurs, the ECC interrupts the microprocessor, which reads the syndromes and uses them to correct the data. The ECC also alerts the DMA when an error has occurred so the location of the defective sector can be flagged.

When the sector ECC field is about to begin, the R/W PCA asserts SEF-L, indicating that the next 12 bytes of data will be ECC information. During a write, SEF-L disables the output of the DMA, giving the ECC exclusive control of the ESI disc data bus. The ECC data is clocked over the bus by DDS-H. The WHO-L signal from the DMA disables the ECC when a data transfer operation must be aborted.

All internal ECC data, control, and status registers are accessible to the processor via its data bus. The ECC is clocked by a 4 MHz signal from the clock generator.

A-30. DATA PATH CONTROL INTERFACE. The data path control interface hardware consists of a single buffer isolating the controller microprocessor data bus from the ESI data path control bus. This configuration allows the data path control bus to operate at the full speed of the processor data bus, a necessity since the processor must send the R/W PCA a command for every sector transferred.

The additional control signals associated with the data path control system (DPA0, DPRHW-L, DPCS-L) are generated by the processor and output to the R/W PCA through the data path control interface.

A-31. SERVO CONTROL INTERFACE. The servo control interface provides the link between the controller microprocessor and the servo PCA. The servo system is operated by its own microprocessor, so this interface serves as the communication port between the two processors.

The servo control interface acts as a double-buffered, bidirectional, 8-bit parallel I/O port. Because all servo commands and status are two bytes in length, the double buffering allows either processor to load two bytes into the buffer without having to wait for a response from the other processor. The handshake mechanism of the I/O port alerts the processor on the other side of the port when two bytes of data are available.

Four handshake signals control the transfer of data across the servo control bus. When the controller processor loads a servo command into the buffer, the servo interface asserts SDAV-L. The servo microprocessor responds by asserting SRD-L and reading the contents of the I/O port's buffer. When the servo PCA is ready to return status to the controller, the servo processor checks to see if SBF-L is deasserted, indicating that there is room in the interface buffer for the status bytes. If there is room, the servo processor writes the status into the interface buffer using SWR-L. The presence of the status bytes in the buffer causes the servo interface to interrupt the controller processor, which then reads the status bytes.

Five lines from the controller processor's address bus allow the processor to access the servo control interface internal registers. The servo control interface is driven by an 8 MHz clock input from the clock generator.

A-32. MICROPROCESSOR CIRCUITS

The microprocessor and its related support circuits coordinate all activities on the controller PCA. These activities include transferring and correcting disc data, controlling the drive R/W and servo systems, and monitoring drive status.

A-33. MICROPROCESSOR. The microprocessor used on the controller PCA is a 68000 operating at 12.5 MHz. This is a 16-bit processor with an addressable memory space of 16 Megabytes. The processor communicates with the other devices on the PCA via its 16-bit data bus. The 24-line address bus accesses the processor memory and registers in the interface hardware circuits.

The processor initiates the various drive activities by addressing the appropriate interface circuit and transferring command information over the data bus to that device. All devices must respond to processor access within a predefined amount of time. Failure to respond in time causes the bus error timer to generate a Bus Error (BERR) to the processor.

The processor uses interrupts to determine when certain events take place. This relieves the processor of the responsibility of polling for hardware status to determine if an event has occurred. The processor supports seven levels of interrupt priority. When a hardware circuit generates an interrupt, the inputs from the interrupt controller indicate the priority of the interrupt.

The Index (INDX-L) signal from the servo PCA-A1 is a timing signal indicating the beginning of each track (physical sector 0). This signal is used by the processor when formatting the disc media. The Power-On Reset (POR-L) signal from the power supply serves as the reset input to the processor. When asserted, this signal invokes the drive initialization routine.

A-34. MICROPROCESSOR MEMORY. The processor memory includes ROM and RAM organized into 16-bit words. The memory consists of 64 kilowords of ROM and 8 kilowords of RAM. The ROM contains the firmware for implementing the CS/80 command set and for running internal diagnostics. The RAM provides temporary data and stack space for the processor.

A-35. CLOCK GENERATORS. The clock generators provide the necessary timing signals for the controller PCA. A 25 MHz oscillator develops the 12.5 MHz clock for the microprocessor. A separate 32 MHz oscillator provides the clock signals for the remainder of the PCA, including 32 MHz for the DMA, 8 MHz for the servo control interface, 4 MHz for the ECC, and 500 KHz for the bus error timer.

A-36. INTERRUPT CONTROLLER. The interrupt controller prioritizes the interrupts generated by the controller hardware. The processor supports seven levels of interrupt priority, with level seven being the highest.

The interrupt controller monitors the interrupt lines from the various hardware circuits, each of which has been assigned an interrupt priority. These circuits include the DMA, ECC, HP-IB interface, and servo control interface. There are also interrupt inputs from the power supply (PF-L) and the R/W PCA (DPIRQ-L).

When an interrupt occurs, the interrupt controller outputs to the processor a three-bit value representing the encoded priority level of the device requesting the interrupt. The processor always services the interrupt from the device with the highest unmasked priority. Lower priority interrupts must wait until higher priority interrupts are serviced.

A-37. BUS ERROR TIMER. The bus error timer detects non-responding controller hardware circuits. This timer is required to avoid a situation where the processor might wait indefinitely for malfunctioning hardware to respond to a data transfer.

The processor initiates a data transfer with other controller hardware circuits by placing the device's address on the address bus and asserting Address Strobe (AS-L), which resets the bus error timer. A counter in the timer begins counting, clocked by the 500 kHz clock input. The processor then waits for a response from the addressed device. If the device does not respond before the counter reaches its timeout value, the bus error timer outputs Bus Error (BERR) to the processor. If the peripheral responds in time, the processor deasserts AS-L, disabling the bus error timer until the next bus cycle begins.

A-38. HUMAN INTERFACE CIRCUITRY

The human interface circuits provide the interface between the controller processor data bus and various drive switches and the front panel LEDs.

A-39. HP-IB ADDRESS/SELFTEST SWITCH. This four-segment switch mounted on the rear of the controller PCA is used to set the drive's HP-IB address (3 segments) and enable the drive selftest (1 segment). The outputs of the switch are buffered onto the processor data bus.

During the drive's initialization procedure, the processor reads the values of the three HP-IB switch segments and loads this binary data into the address register in the HP-IB interface. The value of the fourth switch segment is also read: if this segment is set, the drive will automatically enter a selftest mode at power-on.

A-40. LED DRIVERS. This circuit serves as the driver for the drive's three front-panel LEDs. Binary data from the processor data bus is latched into the drivers. This data is output to the LEDs, which provide a visual indication of the current operational status of the drive. The significance of the LED patterns is described in Chapter 8.

A-41. FIRMWARE ARCHITECTURE

The controller firmware is structured as a multi-tasking executive-based operating system. The firmware is organized into modules called "tasks", with each task responsible for a particular function (see figure A-2). The multi-tasking architecture allows the execution of several tasks simultaneously. The responsibility for coordinating the execution of the various tasks lies with the executive firmware, which controls the interaction between concurrent tasks and the hardware resources they need. The executive operating system is configured at power-on by the drive initialization firmware.

A-42. DRIVE INITIALIZATION FIRMWARE

The initialization firmware is responsible for taking the drive from its power-down state to a state ready to process commands from the host. This includes functionally testing all drive hardware to ensure that the drive is operating properly before allowing the host access to the drive. The drive initialization firmware is divided into two segments: a non-task initialization routine invoked at power-on, and an initialization task scheduled by the executive to complete the drive initialization.

At power-on, the non-task portion of the initialization firmware begins execution. This program performs the following sequence of operations:

1) Initialize all drive hardware

2) Test controller PCA hardware

3) Configure the executive operating system

Following the successful completion of these operations, the initialization program passes control to the multi-tasking executive. The first task scheduled by the executive is the initialize task, which performs a complete functional test of the drive hardware. When the functional tests are complete, the initialize task schedules the other firmware tasks, returns control to the executive, and then suspends itself. The initialization firmware remains idle until the next power-on condition occurs.

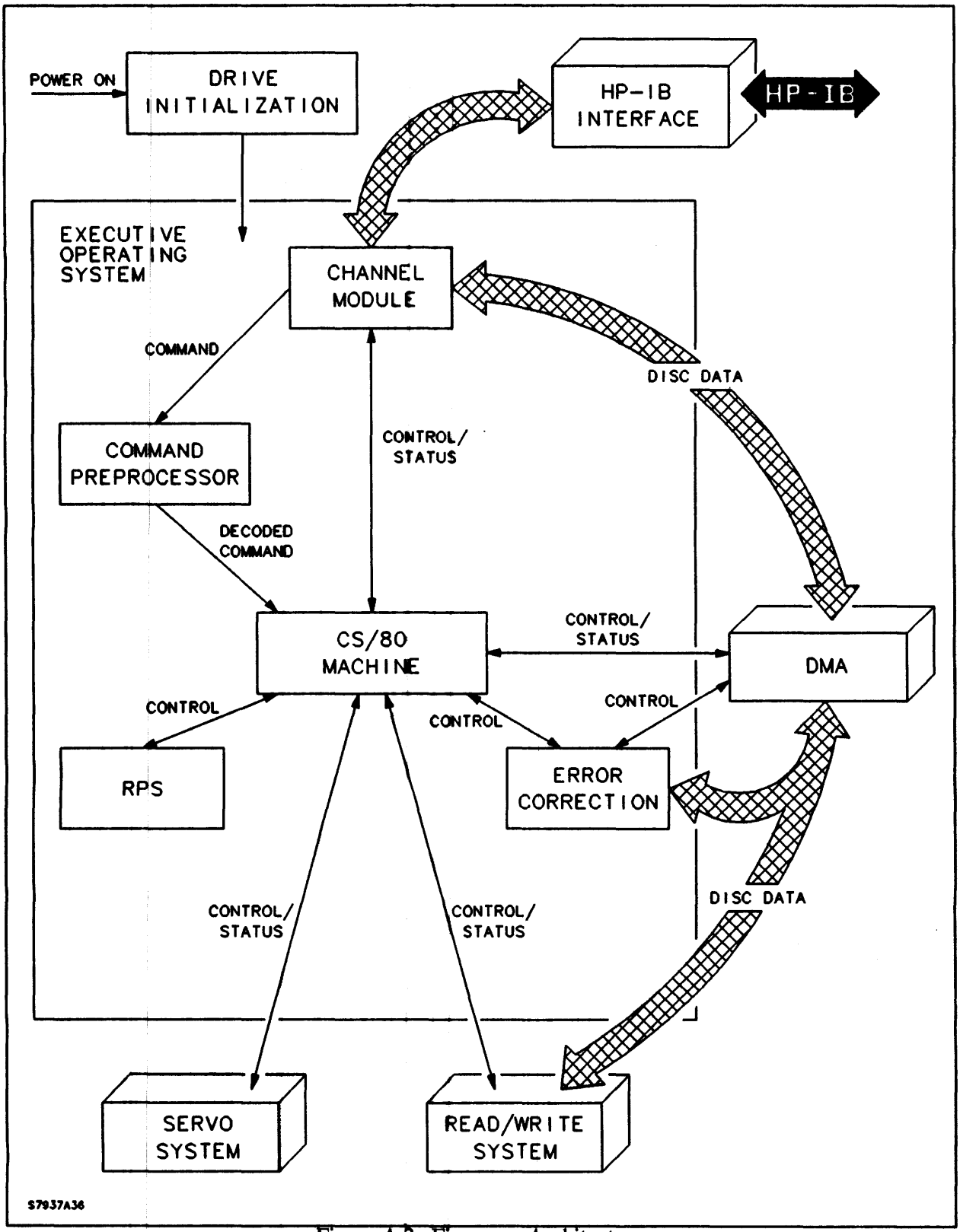


Figure A-2. Firmware Architecture

A-43. MULTI-TASKING EXECUTIVE

The executive module of the firmware is the key to the controller's multi-tasking operating system. The executive schedules the execution of the tasks, manages the hardware resources shared by the tasks, and passes information between tasks. In addition, the executive forms the connecting link between the drive's interrupt system and the firmware tasks, allowing interrupts to communicate with and influence the execution of the tasks.

In the controller's multi-tasking firmware architecture several tasks may execute simultaneously; however, these tasks must all share the controller microprocessor. It is the responsibility of the executive to control which task has possession of the processor at any one time. The executive accomplishes this by assigning priority and readiness levels to each task, then using these levels to ensure that the highest priority task requiring the processor is serviced. If, while one task is executing, a higher priority task requires service, the executive suspends the executing task and allows the higher priority task to run. When the task completes, the suspended task resumes its execution. Although a task may be suspended many times before it completes, it produces the same result as if it had run uninterrupted.

In addition to allocating the microprocessor, the executive also manages the other drive hardware resources. These include the HP-IB channel interface, the DMA, the servo system, and the read/write system. The executive must ensure that two tasks do not have simultaneous possession of the same hardware resource. For example, if one task is granted use of the servo system, that task must be allowed to finish before the executive can give the servo system to another task.

The executive controls the flow of information between tasks. This information includes messages passed from one task to another to control the operation of the tasks. The executive also controls the flow of disc data through the drive, ensuring that data integrity is maintained.

The executive also serves as the interface to the drive interrupt system. The interrupt system is the primary means for synchronizing firmware operations with hardware events. These hardware events communicate to the firmware the status of the separate functional hardware blocks. When an interrupt occurs, the executive suspends the task currently executing and services the interrupt.

A-44. CHANNEL MODULE

All information transferred between the host and the drive flows through the channel module. The channel module ensures that the protocol requirements of the HP-IB channel are maintained for all information transfers, thus making the HP-IB protocol requirements invisible to the rest of the controller. The channel module decodes channel addressing and recovers from channel errors. The channel module also contains a flash decoder used to decode optimized read and write commands.

The information transferred between the channel module and the host includes commands, status, and disc data. Incoming commands fall into one of three categories: optimized reads and writes, transparent, and all other commands. Optimized read and write commands are decoded by the channel module's flash decoder. Transparent commands are decoded and executed by the channel module. All other commands from the host are passed to the preprocessor task for decoding.

The channel module flash decoder is designed to quickly process optimized read and write sequences. An optimized sequence consists of valid combinations of Set Unit, Set Volume, Set Address, Set Length, and Read or Write commands. By giving the flash decoder the first opportunity to decode the command message, read and write commands are processed as quickly as possible. If the command message is not an optimized sequence, or if it contains an error, the command is passed to the preprocessor task for decoding.

The channel module initiates any seek operation associated with an optimized Read or Write command. This includes performing the logical-to-physical address conversion and passing the resultant two-byte command to the servo system. Once the seek operation has begun, the channel module passes the decoded command information to the CS/80 machine, which continues the command execution.

The channel module communicates with the CS/80 module to coordinate the transfer of execution and reporting messages between the drive and the host. When the CS/80 module indicates that a message transfer may begin, the channel module enables Parallel Poll Response (PPR). When the host responds with the appropriate message secondary, the transfer begins. During the execution phase, disc data is transferred directly between the channel module and the drive hardware. In the reporting phase, status information is passed from the CS/80 module to the channel module for output to the host.

A-45. COMMAND PREPROCESSOR

Host commands are passed from the channel module to the command preprocessor for decoding. In addition to decoding, the command preprocessor executes all complementary commands included in the command sequence, and sets the drive state variables according to these commands. Once the command has been fully decoded, the preprocessor passes the results to the CS/80 module, which executes the command. If the command message consists solely of complementary commands, no hardware resources are required and the entire command message will be executed by the command preprocessor.

The command preprocessor decodes all CS/80 command sequences not decoded by the channel module's flash decoder. This includes command sequences not recognized by the flash decoder, and erroneous or illegal parameter and opcode combinations. The general nature of this module results in slower execution speed than the flash decoder. If the general decoder detects an illegal command sequence, it initiates the proper error handling procedure.

A-46. CS/80 MODULE

The CS/80 module executes all commands requiring hardware resources. It synchronizes the movement of disc data between the HP-IB interface and the drive hardware, and generates the status reporting message (QSTAT).

The CS/80 module is idle until passed a decoded command by the preprocessor or, in the case of an optimized Read or Write command, the channel module. When a command is received, the CS/80 module obtains the hardware resources necessary to execute the command. The hardware remains under the control of the CS/80 module until command execution is complete. When a command requiring a seek is passed from the preprocessor (nonoptimized), the CS/80 module performs the logical-to-physical address conversion and initiates the seek operation.

The transfer of execution and reporting messages over the HP-IB channel is controlled by the CS/80 module. When the CS/80 module is ready to transfer an execution or reporting message, it informs the channel module. The channel module alerts the host, which responds with the appropriate message secondary, initiating the transfer. When the transfer is complete, the channel module informs the CS/80 module.

The CS/80 module uses inputs from the RPS and error correction tasks to coordinate command execution. When executing read commands, the CS/80 module uses input from the RPS task to determine the proper time to initiate the execution phase of the transaction. When an error is detected in data being read from the disc, the error correction task alerts the CS/80 module if the data cannot be corrected. In this case, the CS/80 module must initiate read retrys in an attempt to recover the data.

A-47. RPS TASK

To maximize channel efficiency, the RPS task initiates the execution phase of a Read command before the target data is physically located by the drive. This task executes only during read commands when RPS is enabled by the host.

Using the RPS value defined by the host, and the current location of the data head relative to the target data, the RPS task determines when the target data is within range. When this time arrives, the RPS task tells the CS/80 module to initiate the execution message. By the time the host responds with an execution secondary, the data is in the DMA buffer RAM, ready for transfer to the host.

A-48. ERROR CORRECTION TASK

The error correction task detects and, if possible, corrects errors in the data read from the disc. This task is idle until the ECC detects a data error in the data being read from the disc. When an error is detected, the task enters its error correction routine which includes the following sequence of operations:

1) Alert the DMA that an error has been detected. The DMA logs the buffer RAM location of the defective sector. The DMA also flags the sector as bad, thus preventing that sector from being transferred to the host.

2) Read the data from the DMA buffer RAM and, if possible, correct it.

3) Rewrite the corrected data into the buffer RAM and clear the defect flag for that sector. This informs the DMA that the data may now be transferred to the host.

4) Inform the CS/80 module that the correction is complete.

If the error correction task is unable to correct the data error, it informs the CS/80 module, which initiates read retrys in an effort to recover the data. If the data still cannot be corrected, the error correction task clears the sector for transfer to the host and informs the CS/80 module that the transfer included bad data. When the data transfer is complete, the CS/80 module generates a status report indicating the uncorrectable data condition.

A-49. DIAGNOSTICS

Both controllers implement the power-on diagnostic described in paragraph A-17. In addition, the controllers implement the CS/80 External Exerciser commands listed in table 8-1. The XP-model controller supports several additional cache-related exerciser commands, which are identified in table 8-1. For detailed instructions on using the exerciser, refer to the *CS/80 External Exerciser Reference Manual*, part number 5955-3462.

A-50. DISC CACHING

The HP-IB Controller PCA-A6 included in XP-model disc drives supports disc caching. The cache improves system performance by decreasing disc response time during reads and writes. The response time is decreased during reads by reducing the number of physical seeks needed to locate data. During writes, disc response is improved through the use of an "immediate write" feature.

The disc cache is implemented using 2 megabytes of dynamic RAM. The cache RAM is logically organized as 440 blocks (or domains) of 4 kbytes (16 sectors) each. The controller stores the last 440 accessed areas of the disc in the cache RAM. Subsequent reads to any of these areas will not require a physical seek.

A-51. CACHE FUNCTIONAL OPERATION

Disc caching is enabled by the drive during its power-on sequence. The entire cache RAM is tested during the power-on diagnostic. If any area of the cache RAM fails, the caching is disabled. The disc cache is also enabled following a Device Clear command from the host.

The cache is disabled if a power-on diagnostic failure or a DMA diagnostic failure occurs. The host can also disable (or enable) cache using the CACHEON/CACHEOFF external exerciser commands (see table 8-1).

When disc caching is enabled, it is used during all host reads and writes.

A-52. READ WITH DISC CACHING. When the host issues a Read command with a transfer length of 4 kbytes or less, the CS/80 module searches cache RAM to determine if the entire data request can be satisfied from one domain. If it can, the data is transferred from the cache RAM to the host. If the request cannot be satisfied from a single domain, a physical seek to the target sector is performed, and a full 4-kbyte block of data is read from the disc and stored in cache. Simultaneously, the requested data is transferred to the host. If cache RAM is full, the least recently used block will be used to store the new data. In

this way, infrequently accessed data is removed from the cache to make way for new data.

If a Read command specifies a transfer length greater than 4 kbytes, a cache search is not performed. The controller executes the Read command as if cache were not present.

A-53. WRITE WITH DISC CACHING. When the host issues a Write command with a transfer length of 4 kbytes or less, the CS/80 module searches cache for all domains which include any of the sectors to be updated. If the entire range of target sectors is contained in one of these "overlapping" domains, that domain is updated with the new data and retained. All other domains that overlap the target sectors are flushed from the cache RAM. If the range of target sectors is not contained in any single domain, the write data is not retained in cache.

If the Write command transfer length exceeds 4 kbytes, all domains that overlap the target sectors are flushed and the data is not retained in cache RAM.

Disc caching allows the drive to perform "immediate writes" for any Write command with a transfer length of 4 kbytes or less. When a Write command is received, the drive enters the execution phase and prompts the host for the data. Once the data transfer has completed successfully, the drive proceeds immediately to the report phase and reports successful completion (QSTAT=0). Although the data has not yet been written to the disc, the host is free to perform another disc access. The drive then proceeds to write the data to the disc.

While the drive is updating the disc, the host may perform another disc access. If the access is a read that can be satisfied from cache, the drive will perform the read concurrently with the disc update in progress. A read that requires a physical seek, or another write, must wait until the drive completes the write operation in progress. Both these operations require drive resources that will not be available until the write is complete.

A-54. CACHE FLUSHING. There are certain conditions and events which will cause the controller to "flush" the entire contents of the cache RAM. These conditions include the following:

- Power-On
- Device Clear command from the host
- Initialize Media command from the host
- Self-test (DMA diagnostic)
- An Error Rate Test (ERT)
- A spare operation
- A cache disable command from the host

A-55. CACHE HARDWARE

The cache hardware contains the memory necessary to implement disc caching. Also included in this hardware are the control, addressing, and error correction circuits required to support the cache. The functional relationship of the cache to rest of the controller hardware is shown in figure A-3.

The heart of the cache is two megabytes of dynamic RAM. This RAM expands the size of the DMA buffer from its normal 32 kbytes to 64 pages of 32 kbytes each. Each 32 kbyte page is supported by 2 kbytes of overhead RAM. Cache addressing is accomplished by a combination of lines from the DMA and the microprocessor. Fifteen address lines from the DMA provide access to an entire 32 kbyte page of RAM. Page registers in the cache hardware select one of the 64 pages. The page registers are loaded by the processor from its data bus. The entire cache RAM is accessible to both DMA state machines and the processor. All cache data transfers pass through the DMA.

The cache also includes 8 kbytes of non-volatile RAM (NV RAM), which performs an "eavesdrop" function during write operations. When host data is loaded into cache RAM for writing to the disc, a copy of the data is also stored in the NVRAM. If a power failure occurs before the disc is updated, the cache still retains a copy of the data. When

power is restored, the data is still available for writing to the disc.

Additional control circuits in the cache hardware provide support for the proper operation of the cache RAM. This includes memory addressing, timing, refresh, and error correction.

A-56. CACHE DIAGNOSTICS

In addition to the cache test performed as part of the power-on diagnostic, the XP-model controller implements several CS/80 External Exerciser commands used to support disc caching. These commands are listed in table 8-1. A detailed description of these commands and how to initiate them is included in the *CS/80 External Exerciser Reference Manual*, part number 5955-3462.

CONTROLLER PCA–A6

HP-IB

A6J1

ATN → 11
SRQ → 10
IFC → 9
NDAC → 8
NRFD → 7
DAV → 6
REN → 17
EOI → 5
DIO1 → 1
DIO2 → 2
DIO3 → 3
DIO4 → 4
DIO5 → 13
DIO6 → 14
DIO7 → 15
DIO8 → 16

HP–IB INTERFACE

CONTROL
DATA 10
INTERFACE INTERRUPT
CHANNEL INTERRUPT
32 MHz

DMA

BUFFER RAM
I/O STATE MACHINE
DISC STATE MACHINE
I/O CONTROL
BUFFER CONTROL
CRC
HEAD ADR. REG.
DISC CONTROL
PROCESSOR ACCESS CONTROL

ECC ERROR
ECC INTERRUPT
4 MHz
ECC ERROR
WHO–L
SOS–L
SEF–L
DDS–H
DD7–DD0
DISC INTERRUPT

CACHE (97521A ONLY)

CONTROL
NV RAM
PAGE REG.
CACHE RAM

8
ADDRESS
DATA
5
16
24

500 KHz
BUS ERROR TIMER
AS–L
BERR
12.5 MHz
MICROPROCESSOR
INDX–L
POR–L

PROCESSOR MEMORY
ROM–64K X 16
RAM–8K X 16

SWITCHES/ BUFFER

3
INTERRUPT PRIORITY

INTERFACE INTERRUPT
CHANNEL INTERRUPT
DISC INTERRUPT
ECC INTERRUPT
SERVO INTERRUPT
INTERRUPT CONTROLLER
DPIRQ–L
PF–L

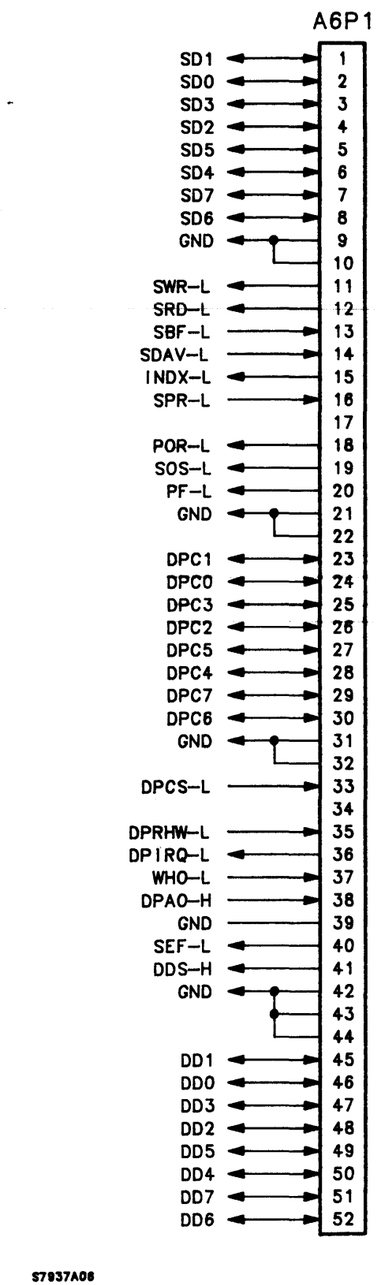
CLOCK GENERATORS
32 MHz
12.5 MHz
8 MHz
4 MHz
500 KHz

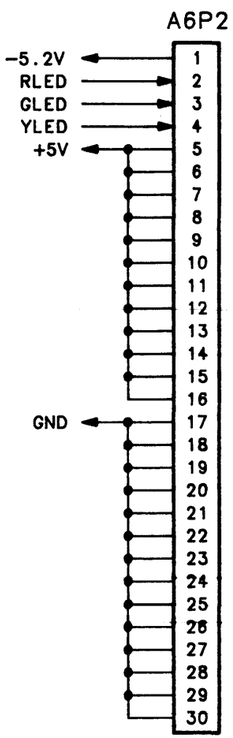
S7937A35

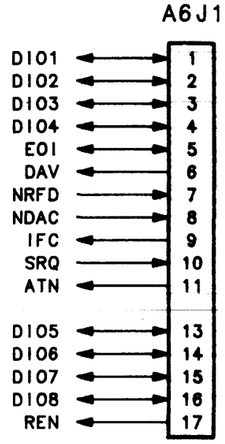
R/W PCA–A2

DMA
BUFFER RAM
I/O STATE MACHINE
DISC STATE MACHINE
BUFFER CONTROL
I/O CONTROL
CRC
HEAD ADR. REG.
DISC CONTROL
PROCESSOR ACCESS CONTROL
INTERRUPT
32 MHz
A ONLY)
NV RAM
CACHE RAM
8
5
16
24
ADDRESS
DATA
ECC ERROR
ECC INTERRUPT
4 MHz
ECC
WHO–L
SOS–L
SEF–L
DDS–H
DD7–DD0
DISC INTERRUPT
8
A6P1
A2J1
37 WHO–L
19 SOS–L
40 SEF–L
41 DDS–H
ESI DISC DATA BUS (SEE RW)
8
45–52 DDO–DD7
8
DATA PATH CONTROL INTERFACE
CONTROL
23–30 DP0–DP7
38 DPA0
35 DPRHW–L
33 DPCS–L
36 DPIRQ–L
ESI DATA PATH CONTROL BUS (SEE RW)
A1–A5
5
8
8 MHz
SERVO INTERRUPT
SERVO CONTROL INTERFACE
8
1–8 SD0–SD7
16 SPR–L
12 SRD–L
11 SWR–L
14 SDAV–L
13 SBF–L
ESI SERVO CONTROL BUS (SEE S1)
500 KHz
BUS ERROR TIMER
AS–L
BERR
12.5 MHz
MICROPROCESSOR
INDX–L
POR–L
PROCESSOR MEMORY ROM–64K X 16 RAM–8K X 16
3
INTERRUPT PRIORITY
INTERFACE INTERRUPT
CHANNEL INTERRUPT
DISC INTERRUPT
ECC INTERRUPT
SERVO INTERRUPT
INTERRUPT CONTROLLER
DPIRQ–L
PF–L
SWITCHES/ BUFFER
4
3
LED DRIVERS
A6P2
A2J4
2 RLED
3 YLED
4 GLED
FRONT PANEL LED SIGNALS (SEE R/W)
15 INDX–L
18 POR–L
20 PF–L
POWER SUPPLY STATUS (SEE PS)

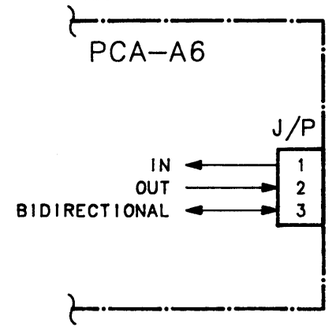
Figure A-3. HP-IB Controller PCA-A6 Functional Block Diagram







NOTE:
SIGNAL DIRECTION IN AND OUT OF THE PCA IS INDICATED AS FOLLOWS:



S7937A08

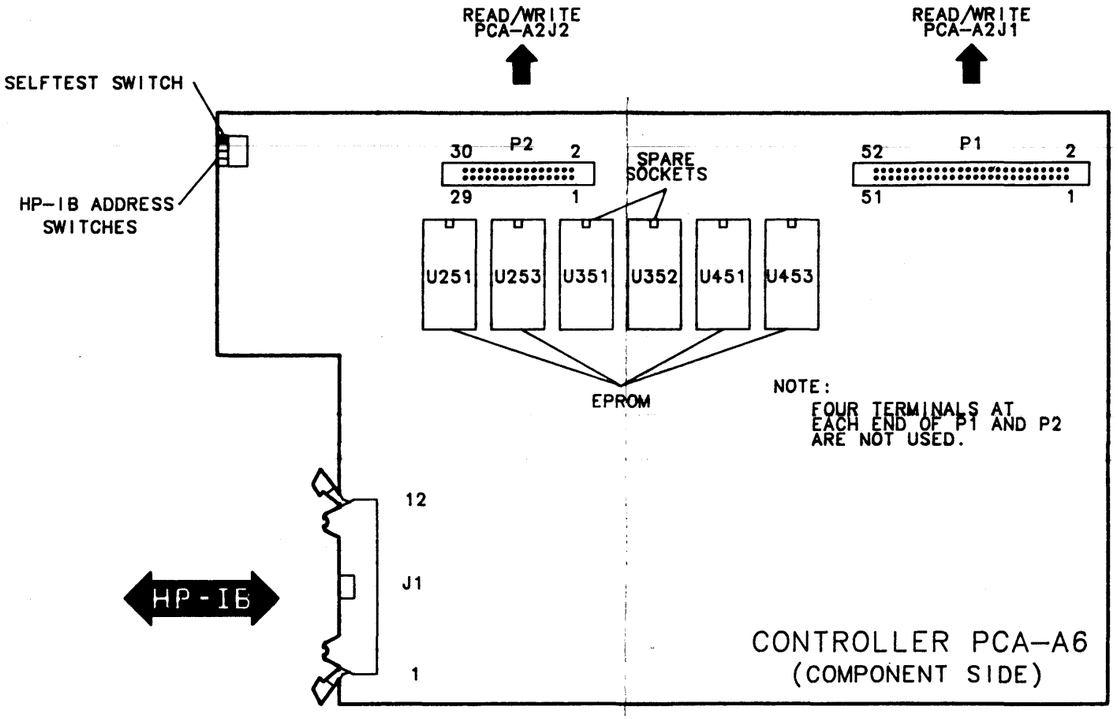


Figure A-4. HP-IB Controller PCA-A6, Parts Location and Connector Pinout

Manual Part Number: 07937-90903
Printed in U.S.A., JANUARY 1987
Edition 1
E0187

HEWLETT PACKARD