HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

13012B

PROGRAMMABLE READ PARITY ACCESSORY KIT

(FOR THE 7970 SERIES DIGITAL MAGNETIC TAPE UNITS)

Printed-Circuit Assembly:
07970-60954, Series ~~1122~~ 1841

Note

This manual should be retained with the 7970 Digital Magnetic Tape Unit Operating and Service Manual.

13012-90003

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PRINTED: AUG 1976

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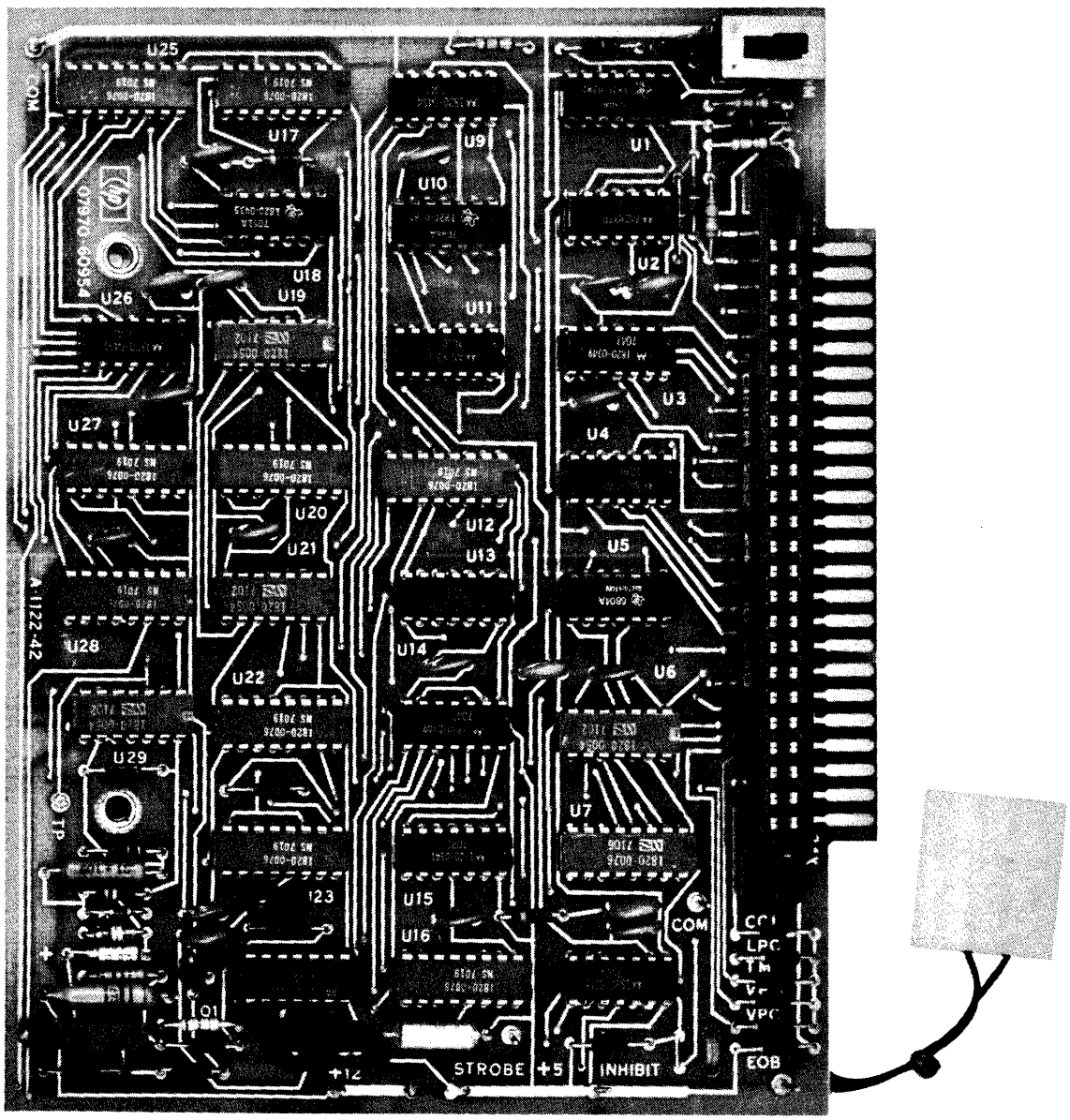


Figure 1-1. HP 13012B Programmable Read Parity Accessory Kit

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides general information, installation, interfacing, principles of operation, maintenance, and replaceable parts information for the HP 13012B Programmable Read Parity Accessory Kit. (See figure 1-1.)

1-3. GENERAL DESCRIPTION.

1-4. The programmable read parity accessory kit is a single plug-in printed-circuit assembly (07970-60954) that checks for data errors when reading seven- or nine-track, NRZI format magnetic tape records. The read parity accessory can detect data errors when reading tape records recorded at densities of 200, 556, or 800 characters per inch and at speeds of 10 to 45 inches per second.

1-5. Parity checking of seven- or nine-track records can be selected directly on the printed-circuit assembly or remotely with an appropriate signal input. When checking nine-track tape records, the read parity accessory operates in the odd-parity mode; for seven-track tape records, the odd- or even-parity mode can be remotely selected with an appropriate signal input. Parity-checking operations can be disabled, if desired, with an appropriate signal input.

1-6. A single read parity accessory can check for read-data errors on as many as one master and three slave tape units.

1-7. IDENTIFICATION.

1-8. Hewlett-Packard uses five digits and a letter (00000A) to identify standard accessories. If the designation of the accessory received does not agree with the designation on the title page of this manual, there are differences between the accessory received and the accessory described in this manual. The differences are described in manual supplements available at HP Sales and Service Offices. (Addresses of these offices are listed at the back of this manual.)

1-9. Printed-circuit assembly revisions are identified by a letter, a series code, and a division code marked below the part number on the printed-circuit assembly (PCA). The letter identifies the revision of the etched trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical characteristics of the loaded PCA and the positions of the components. If the series code number does not correspond with the number on the title page of this manual, the PCA differs from the one described in this manual. These differences are explained in manual supplements available at the nearest HP Sales and Service Office.

1-10. SPECIFICATIONS.

1-11. Specifications for the accessory are listed in table 1-1.

Table 1-1. HP 13012B Programmable Read Parity Accessory Kit Specifications

POWER REQUIREMENTS

+12 Vdc ±3% @ 60 mA

+ 5 Vdc ±1% @500 mA

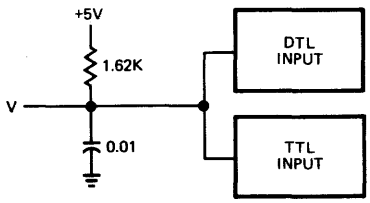
LOGIC LEVELS

Line Receivers

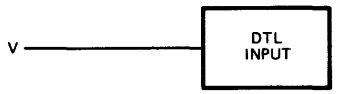
Assertion: ⩽ +0.4V

Negation: ⩾ +2.4V

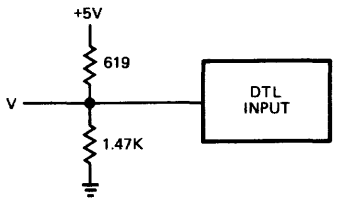
INHIBIT



RC, RDP, RD0 THROUGH RD7



CSD2, CSD5, PSL

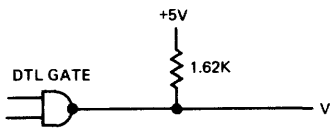


Line Transmitters

Assertion: ⩽ +0.4V

Negation: ⩾ +2.4V

VP, VPC, CCI, EOB, LPC, AND TM



SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides unpacking, initial inspection, and interfacing information for the HP 13012B Programmable Read Parity Accessory Kit.

2-3. UNPACKING AND INITIAL INSPECTION.

2-4. If the read parity accessory is received separately from the tape unit, inspect the shipping carton before opening. If there is external evidence of damage or if the box rattles, request that the carrier's agent be present when the carton is opened.

2-5. Inspect the accessory as it is unpacked. If the PCA is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Offices will arrange for repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-6. INSTALLATION.

2-7. Install the read parity PCA as follows:

a. Set computer and master tape unit power switches to off.

b. Open tape unit for access to read data module assembly.

c. Set 9/REM-7 switch S1 to the 9/REM position to locally select nine-track operation or to allow remote selection of seven- or nine-track operation; set S1 to 7 position to locally select seven-track operation.

d. Install read parity PCA P1 into tape unit connector RJ11.

e. Connect read parity PCA power connector P2 to RJ12 in the tape unit.

* NOTE: Perform adjustment procedure per paragraph 4-5, page 4-1.

f. Thread two number 6-32, 0.75-inch screws with number 6 lockwashers through the holes provided in the read parity PCA and into the read data module assembly.

g. Close tape unit and set computer and tape unit power switches to on.

2-8. PARALLELING TAPE UNITS.

2-9. A single read parity accessory can check for read-data errors in as many as one master and three slave tape units. Information for connecting tape units for parallel operation is contained in the HP 13194A Multiunit Cable Accessory Kit Operating and Service Manual.

2-10. INTERFACING CONSIDERATIONS.

2-11. READ PARITY SIGNAL DEFINITIONS.

2-12. The controller or interface of the system in which the read parity accessory and associated tape unit(s) are employed must be compatible with the read parity signals as described in paragraphs 2-13 through 2-22.

2-13. COMMAND SELECT DENSITY 2 AND COMMAND SELECT DENSITY 5 (CSD2/CSD5). When asserted (low), the CSD2 signal modifies the read parity timing circuits for 200 cpi operation. When CSD5 is asserted (low), the read parity timing circuits are modified for 556 cpi operation. When both CSD2 and CSD5 signals are negated (high), read parity timing circuits are modified for 800 cpi operation. Command Select Density signals must be maintained at the desired level for the duration of the operation.

2-14. PARITY SELECT (PSL). The Parity Select signal modifies read parity circuits for the even-parity configuration when asserted (low), and for the odd-parity configuration when negated (high). The Parity Select line should only be used during seven-track operation, and must be held at the desired level for the duration of the operation.

2-15. SELECT SEVEN-TRACK (S7T). If 9/REM-7 switch S1 is in the 9/REM position, the S7T signal modifies the read parity circuits for seven-track operation when asserted (low). Nine-track operation is remotely selected when S7T is negated (high). The S7T signal must be held at the desired level for the duration of the operation.

2-16. INHIBIT. When asserted (low), the Inhibit signal disables all read parity circuits; all read parity output signals will be negated (high). (Jumper W1 may be removed if the inhibit feature will not be used.)

2-17. VERTICAL PARITY CHECK (VPC). The VPC signal indicates whether any character of the record being read contains an incorrect number of "1" bits. (Vertical parity of the check characters at the end of the record is not checked.) If an incorrect number of "1" bits in a record character is detected, the VPC signal will be asserted (low) and remain asserted until one character period after the End-of-Block signal has been asserted (low).

2-18. LONGITUDINAL PARITY CHECK (LPC). The LPC signal indicates whether any data track of the record

just read contained an incorrect number of "1" bits. If an incorrect number of "1" bits in a data track is detected, the LPC signal will be asserted (low) until one character period after the End-of-Block signal is asserted (low). Longitudinal parity checking is performed during both forward and reverse normal speed operations. Longitudinal parity error indications are valid only after the last record character is read.

2-19. TAPE MARK (TM). The TM signal indicates whether the record just read was a tape or file mark. If a tape mark is detected, the TM signal will be asserted (low) until one character period after the End-of-Block signal is asserted. Tape mark indications are valid only after the last record character is read.

2-20. CHECK CHARACTER INHIBIT (CCI). The CCI signal can be used to distinguish record data characters from the check characters at the end of the records. The CCI signal will be asserted low approximately two character periods after the last data character has been read and remain asserted until the End-of-Block signal is asserted (low). The CCI signal is valid only during normal speed, forward operations.

2-21. VERTICAL PARITY ERROR (VP). The VP signal provides an instantaneous indication of the number of "1" bits in each data character as it is read from the tape. During nine-track operations, the VP signal will be asserted (low) if the number of "1" bits is even. During seven-track operation, the VP signal is asserted when the number of "1" bits is even and the odd-parity mode has been selected; the VP signal is asserted if the number of "1" bits is odd and the even-parity mode has been selected.

2-22. END-OF-BLOCK (EOB). The End-of-Block signal indicates when the last character of a record has been read. The EOB signal will be asserted (low) for 10 ± 2 microseconds at six character periods ±2% (for 200 and 800 cpi; +4% -0% for 556 cpi) after the last character of the record has been read. End-of-block indications are valid only during normal-speed operations.

2-23. READ PARITY PCA CONNECTOR.

2-24. The controller or interface cable of the system in which the read parity accessory and the associated tape unit(s) are used must be compatible with the read parity PCA connector pin assignments listed in table 2-1.

Table 2-1. Programmable Read Parity PCA Connector P1 Pin Assignments

SIGNAL NAME	MNEMONIC	ACTIVE PIN	GROUND PIN
Parity Select	PSL	1X	1
Command Select Density 2	CSD2	3X	3
Command Select Density 5	CSD5	4X	4
Select Seven-Track	S7T	5X	5
Read Clock	RC	8X	8
Read Data Parity Bit	RDP	9X	9
Read Data 0 Bit	RD0	10X	10
Read Data 1 Bit	RD1	11X	11
Read Data 2 Bit	RD2	12X	12
Read Data 3 Bit	RD3	13X	13
Read Data 4 Bit	RD4	14X	14
Read Data 5 Bit	RD5	15X	15
Read Data 6 Bit	RD6	16X	16
Read Data 7 Bit	RD7	17X	17
Inhibit	Inhibit	18X	18
Vertical Parity Error	VP	19X	19
Vertical Parity Check	VPC	20X	20
Tape Mark	TM	21X	21
Longitudinal Parity Check	LPC	22X	22
Check Character Inhibit	CCI	23X	23
End-of-Block	EOB	24X	24

SECTION III
THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section describes the theory of operation of the HP 13012B Programmable Read Parity Accessory Kit.

3-3. FUNCTIONAL DESCRIPTION.

3-4. Parity information is added to magnetic tape records during write operations to aid in detecting errors during subsequent read operations. A single bit is added to each data character and to each data track at the end of the record as required to make the sum of the "1" bits odd or even.

3-5. The programmable read parity accessory checks for read data errors by monitoring the number of "1" bits in each data character (vertical parity) and each data track of the record (longitudinal parity) during read operations. By assuring that the sum of "1" bits is odd or even, most data errors can be detected. Odd- or even-parity checking is selected according to the parity mode used during the write operation.

3-6. If a parity error is detected, the read parity accessory signals the tape unit interface or controller. Additional circuits are included for signaling detection of an end-of-block or tape mark signal.

3-7. DETAILED CIRCUIT DESCRIPTIONS.

3-8. LONGITUDINAL PARITY CHECK CIRCUIT.

3-9. The longitudinal parity check circuit (figure 4-2) monitors the read data signals from the tape unit to check for the proper number of ''1'' bits in each data track of the record. At quiescence, Read Data FFs U17A and B, U20A and B, U25A and B, U27A and B, and U12A are cleared. Each time a data character ''1'' bit is read, the corresponding Read Data FF will toggle. If an even number of ''1'' bits is read in each data track of a record block, the inputs of ''nand'' gate U26 will be high. As a result, the ''not'' LPC signal to the controller will be high, indicating no longitudinal parity error. If an odd number of ''1'' bits is read in any data track of a record block, the corresponding Read Data FF will be set. As a result, the output of ''nand'' gate U26 will be high and the ''not'' LPC signal to the controller will be low, indicating that a longitudinal parity error was detected. If seven-track operation is selected, the ''not'' S7T signal applied through ''exclusive or'' gates U10D, U10B, and U1C will disable the RD0 FF and the RD1 FF.

3-10. VERTICAL PARITY CHECK CIRCUIT.

3-11. The vertical parity check circuit (figure 4-2) monitors the read data signals from the tape unit to check for the proper number of "1" bits in each data character read. Vertical parity errors are detected by Parity Checker U18.

3-12. During seven-track operation, when odd parity is selected, the ''Not'' PSL signal from the controller will be applied through ''nand'' gate U3A, inverter U4A, and ''exclusive or'' gate U10C as a low signal to the pin 3 input of U18. Inverter U11C will apply a high signal to the pin 4 input of U18. If the sum of ''1'' bits in a data character is even, the pin 6 output of U18 will be high to indicate a vertical parity error. If the sum of ''1'' bits is odd, the U18 pin 6 output will be low.

3-13. During seven-track operation when even parity is selected, a high signal will be applied to the pin 3 input of U18 and a low signal will be applied to the pin 4 input. If the sum of the "1" bits in a data character is odd, the pin 6 output of U18 will be high, indicating a vertical parity error. If the sum of "1" bits is even, U18 pin 6 will be low. During nine-track operation, when only odd parity is used, parity checking is the same except the pin 3 input of U18 is the read data zero bit.

3-14. The U18 output signal is applied to the Vertical Parity Check FFs through "nand" gate U19C. Since CCI FF U7A will be set two character periods after the last data character has been read, the "not" CCI FF signal at the pin 10 input of "nand" gate U19C will inhibit any vertical parity errors detected in data record check character(s). Refer to paragraph 3-17 for a detailed description of the CCI FF operation.

3-15. When data characters are being read, however, detected vertical parity errors will be applied through ''nand'' gate U19C and ''nand'' gate U 21C to the set-side input of Vertical Parity Check FF2 U12B. The read clock pulse corresponding to the data character in which a vertical parity error was detected will set VPC FF2. The VPC FF2 will remain set until cleared by the Reset pulse issued at the end of the data record.

3-16. The ''not'' VPC signal will also be asserted (low) if more than one read clock pulse is received after the EOB FF has been set (only the LRC character clock pulse should be present). When the EOB FF is set, a read clock pulse will also set VPC FF1. The low ''not'' VPC FF1 signal applied through ''nand'' gate U21C will make the set-side input of VPC FF2 high. If a second clock occurs before the end of the data record, the VPC FF2 will be set indicating a vertical parity error to the controller (assuming a detected vertical parity error has not already set VPC FF2). Since issuance of

the "not" EOB pulse to the controller is dependent on the last read clock of a record, this technique signals a vertical parity error if an invalid character alters the normal timing of the "not" EOB signal.

3-17. READ PARITY CONTROL CIRCIUTS.

3-18. Issuance of the Vertical Parity Check, End-of-Block, and Check Character Inhibit signals is controlled by the read parity control circuits (figure 4-2). Timing for the control circuit is provided by one-shot multivibrator U24. The one-shot multivibrator toggles Strobe FF U16A via density select timing FFs U23A, U23B, and U22A. The density select timing FFs frequency-divide the multivibrator output by an amount that corresponds to the timing requirements for the various recording densities. The Strobe FF clocks Check Character Inhibit FF U7A and End-of-Block FF U7B through the control cycle. By using the "not" Read Clock signal from the tape unit as the trigger for the multivibrator, the read parity control circuits can distinguish read data from the longitudinal redundancy check character and, during nine-track operation, the cyclic redundancy check character.

3-19. One-shot multivibrator U24 can be triggered by (1) making input pins 3 and 4 high and clocking input pin 1 or 2 low or (2) making input pin 1 or 2 low and clocking input pins 3 and 4 high. At quiescence, U24 is cleared making the pin 3 and 4 inputs high; Strobe FF U16A is cleared making the pin 1 input of U24 high; and the CCI FF U7A and EOB FF U7B are cleared making the pin 2 input of U24 high.

3-20. The first read clock pulse applied through "nand" gate U14A will set Strobe FF U16A and thus trigger U24 by making the pin 1 input low. U24 will be set and timing capacitor C6 will quickly discharge and begin charging toward +5 volts. (The charge time of C6 is adjusted during 800 cpi operation, for one character period by variable resistor R23.) With U24 set, the pin 3 and 4 inputs will be low

3-21. When data is being read during forward tape motion, read clock pulses will be received at one-character period intervals. Read clock pulses corresponding to read data characters will be applied through "nand" gate U6B, capacitor C9, and "nand" gate U14C to U24 pins 3 and 4 to immediately retrigger the multivibrator. Read clock pulses will also be continuously applied through "nand" gate U14A to U16A, keeping the Strobe FF set and thus inhibiting any clocking of the CCI FF and EOB FF.

3-22. During the four-character period interval between the read clock pulse that corresponds to the last data character and the read clock pulse that corresponds to the first check character, capacitor C6 will be allowed to charge. Each time C6 charges, U24 will be cleared by internal circuits. As a result, input pins 3 and 4 will be clocked high and the multivibrator will be retriggered, producing "not" Clock 1 output pulses.

3-23. Since no read clock pulses are received through "nand" gate U14A, "not" Clock 1 pulses generated by U24 during the four-character period interval will be applied through "and" gate U15D to clock the Strobe FF at a rate determined by the density select timing circuits. For example, during 800 cpi operation a divide-by-two function is performed by DST FF3. (Refer to paragraph 3-32 for detailed circuit description of density select timing circuits.) The Strobe FF will be cleared by a "not" Clock 1 pulse two character periods after the last data character read clock pulse is received.

3-24. The high-to-low transition of the Strobe FF signal will set CCI FF U7A and the "not" Check Character Inhibit signal will be low. If seven-track operation is selected, the S7T signal will be applied through "nand" gate U14D to the set-side input of the EOB FF. Therefore, the high-to-low transition of the Strobe FF signal will also set the EOB FF. If nine-track operation is selected, only the clear-side input of U7B will be high, and the EOB FF will remain cleared.

3-25. Four character periods after the last data character read clock pulse is received, the read clock pulse that corresponds to a check character will be received. If seven-track operation is selected, the check character read clock pulse will be applied through "nand" gate U14A and set the Strobe FF. The high-to-low transition of the "not" Strobe FF signal will set U24. Since no more read clock pulses will be received, U24 will free-run and generate "not" Clock 1 pulses. Because of the divide-by-two function of DST FF3, the Strobe FF will be cleared when two "not" Clock 1 pulses have been generated. The high-to-low transition of the Strobe FF signal will clear the CCI FF. After two more "not" Clock 1 pulses, the Strobe FF will be set. After two more "not" Clock 1 pulses, the Strobe FF will again be cleared. The high-to-low transition of the Strobe FF will clear the EOB FF. The high-to-low transition of the EOB FF signal will be applied through diode CR1 to resistor-capacitor (RC) network R19, C4, R17, and R18. The RC network will convert the negative-going signal to a 10-microsecond pulse. As a result, the "not" EOB pulse will be issued to the controller six character periods after the LRC character read clock pulse is received.

3-26. If nine-track operation is selected, "nand" gate U6B will inhibit any read clock pulses received because only the CCI FF will be set after the last data character read clock is received. As a result, U24 will free-run and generate "not" Clock 1 pulses. Because of the divide-by-two function of DST FF3, the Strobe FF will be set after two "not" Clock 1 pulses. After two more "not" Clock 1 pulses, the Strobe FF will again be cleared. The high-to-low transition will set the EOB FF. With the EOB FF set, "nand" gate U6B will no longer inhibit read clock pulses.

3-27. As a result of the four-character period delay before setting the EOB FF, the CRC character read clock pulse will not affect the EOB FF. The next signal to be received will be the read clock pulse that corresponds to the longitudinal redundancy check character. The LRC character read clock pulse will set the Strobe FF. Two character periods later, the Strobe FF will be cleared and the CCI FF will be cleared; after two more character periods, the Strobe FF will set. The Strobe FF will be cleared after two more

character periods, the EOB FF will also be cleared, and the "not" EOB pulse will be generated as described for seven-track operation. Figure 3-1 shows the relationship of read parity control events during forward tape motion operations.

3-28. When data is being read during reverse tape motion, the read clock pulse(s) that correspond to the check character(s) of a record will be received before data character read clock pulses. The first check character read clock pulse received when U24 is at quiescence will be applied through "nand" gate U6B, capacitor C19, and "nand" gate U14C to trigger U24. Since no more read clock pulses will be received within one character period, U24 will free-run and generate "not" Clock 1 pulses, and the Strobe FF will be toggled every two character periods.

3-29. If seven-track operation is selected, the Strobe FF will be cleared two character periods after the LRC check character read clock pulse. The high-to-low transition of the Strobe FF signal will set the CCI FF and EOB FF. The first data character read clock pulse will again set the Strobe FF. Data character read clock pulses will be received at one-character period intervals and applied through "nand" gate U14A to keep the Strobe FF set. When no more data character read clock pulses are received, U24 will begin to free-run. After two "not" Clock 1 pulses, the Strobe FF will be cleared, which will clear the CCI FF. After two more "not" Clock 1 pulses, the Strobe FF will again be set. The Strobe FF will be cleared two "not" Clock 1 pulses later and the negative-going transition will produce the "not" EOB pulse as described in paragraph 3-25.

3-30. If nine-track operation is selected, the Strobe FF will be cleared after two character periods and the high-to-low transition of the Strobe FF signal will set only the CCI FF. "Nand" gate U6B will inhibit any read clock pulses received and, as a result, the CRC character read clock pulse will not affect the read parity control circuits. One-shot multivibrator U24 will free-run and generate "not" Clock 1 pulses. After four "not" Clock 1 pulses, the Strobe FF will be cleared. The high-to-low transition of the Strobe FF signal will set the EOB FF and "nand" gate U6B will no longer inhibit read clock pulses.

3-31. Eight character periods after the LRC character read clock is received, the first data character read clock pulse will set the Strobe FF. The data character read clock pulses received at one-character period intervals will keep the Strobe FF set. The "not" EOB pulse will be generated six character periods after the last data character read clock pulse is received. Figure 3-2 shows the relationship of read parity control events during reverse tape motion operations.

3-32. DENSITY SELECT TIMING CIRCUIT.

3-33. Although the read parity control circuit timing is adjusted for 800 cpi operation, the density select timing circuit modifies control circuit timing to permit compatible operation at 200 cpi and 556 cpi. (figure 4-2).

3-34. When 800 cpi operation is selected both the "not" Character Density Select 2 (CSD 2) and "not" Character Density Select 5 (CSD 5) signals from the controller will be high. As a result DST FF1 U23A and DST FF2 U23B will be held set. The DST FF1 and DST FF2 signals, applied through "and" gate U15C will make the set- and clear-side inputs of DST FF3 high. The "not" Clock 1 pulses generated by one-shot multivibrator U24 will toggle DST FF3 thus providing a divide-by-two function during 800 cpi operation.

3-35. When 556 cpi operation is selected the "not" CSD 5 signal from the controller will be low and DST FF1 will no longer be held set. Since the "not" DST FF3 signal is applied through "nand" gate U29D to the clear-side input of DST FF1, the reset-side input will be low each time the "not" DST FF3 signal is high. Thus DST FF1 will remain set every third "not" Clock 1 pulse, providing a divide-by-three function for 556 cpi operation.

3-36. When 200 cpi operation is selected, the "not" CSD 2 signal from the controller will be low and DST FF2 and DST FF1 will no longer be held set. As a result, all three FFs will be clocked by "not" Clock 1 pulses, providing a divide-by-eight function during 200 cpi operation.

3-37. TAPE MARK DETECTION CIRCUIT.

3-38. On nine-track magnetic tape records the tape mark format is a single character with "1" bits in tracks 3, 6, and 7 and "0" bits in tracks 0, 1, 2, 4, 5, and 8 (figure 4-2). At quiescence, Tape Mark FF1 U28B will be cleared, Tape Mark FF2 will be set, and the pin 5 input of "nand" gate U21B will be high. When a tape mark is read, the "1" bits of the tape mark character and "0" bits applied through appropriate inverters and "exclusive or" gates will make all inputs of "nand" gate U9 high and the output of "nand" gate U21A will be high. As a result, the pin 4 input of "nand" gate U21B will be high and will make the set-side input of TM FF1 low.

3-39. The read clock pulse that corresponds to the tape mark character will clear TM FF2 and the "not" Tape Mark signal to the controller will be asserted (low). The Reset pulse generated at the end of each data record will clear TM FF1 and set TM FF2.

3-40. However, if a second read clock pulse is received the low signal at the pin 5 input of "nand" gate U21B will make the set-side input of TM FF1 high, TM FF1 will be set, and the set-side input of TM FF2 will still be high when the second read clock pulse is received, TM FF2 will remain cleared and the "not" Tape Mark signal will remain asserted.

3-41. If a third read clock pulse is received, the set-side input of TM FF2 will be high and the read clock pulse will set TM FF2, which will negate the "not" Tape Mark signal at EOB time if a data character in the record is detected as a tape mark.

3-42. Figures 3-3 and 3-4 show overall event timing for seven-track and nine-track operations, respectively.

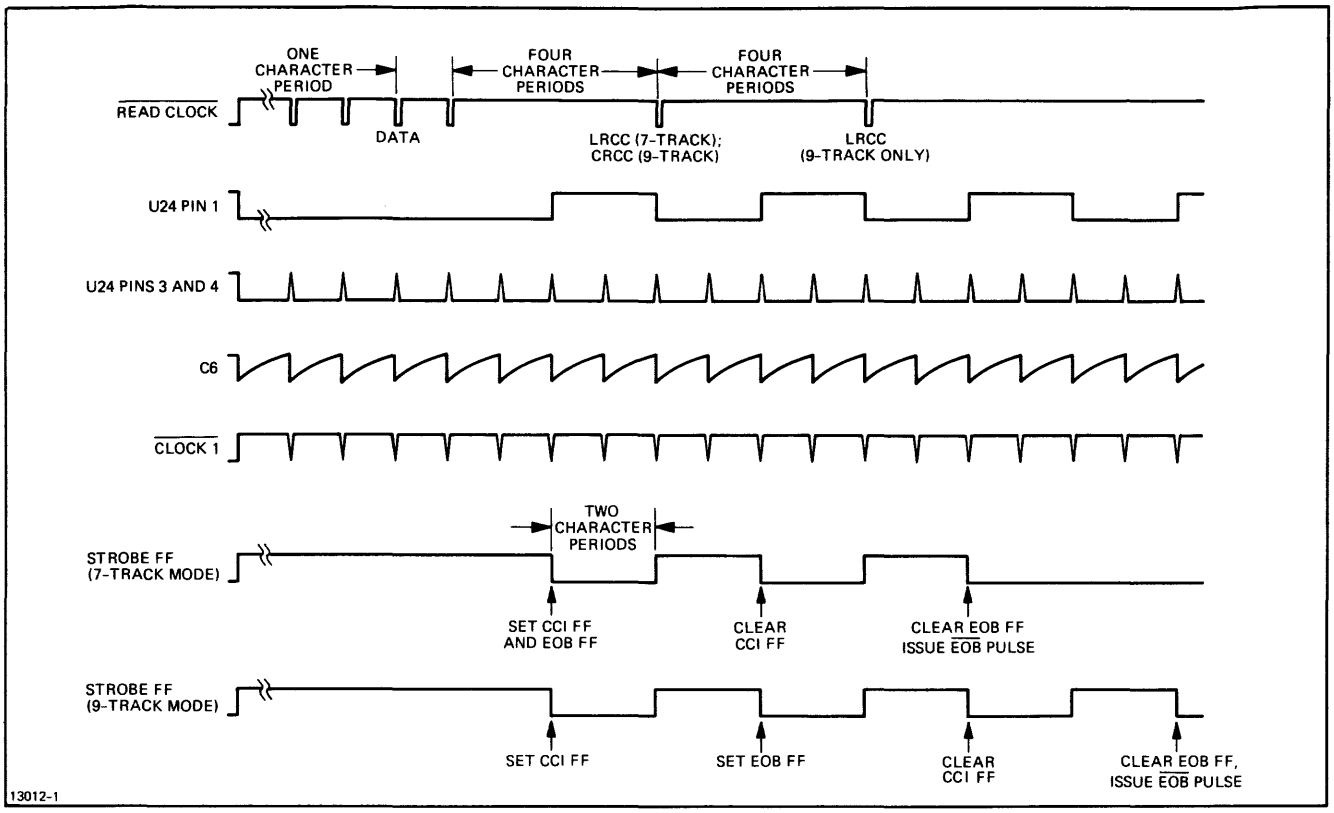


Figure 3-1. Control Circuit Timing, Forward Tape Motion

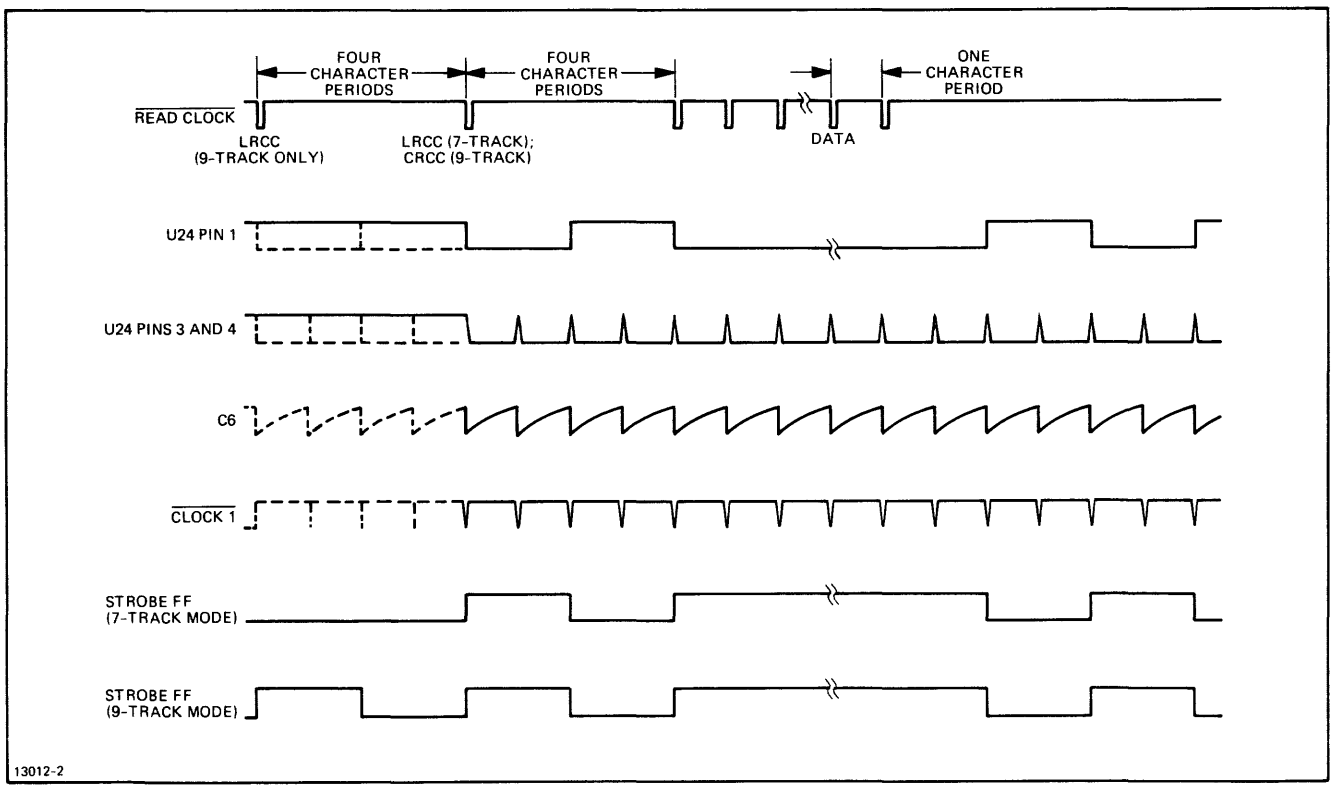


Figure 3-2. Control Circuit Timing, Reverse Tape Motion

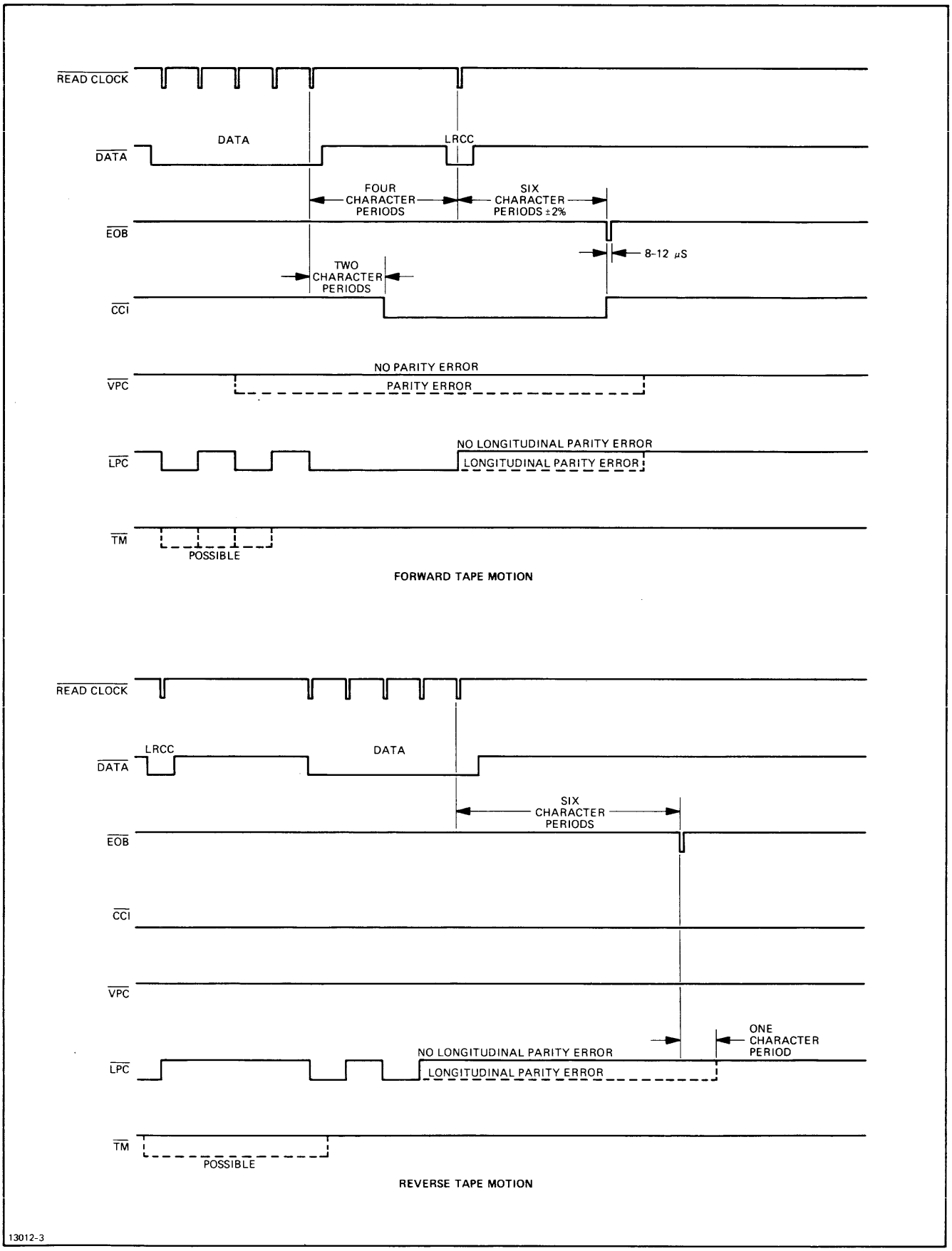


Figure 3-3. Read Parity Event Timing, Seven-Track Operation

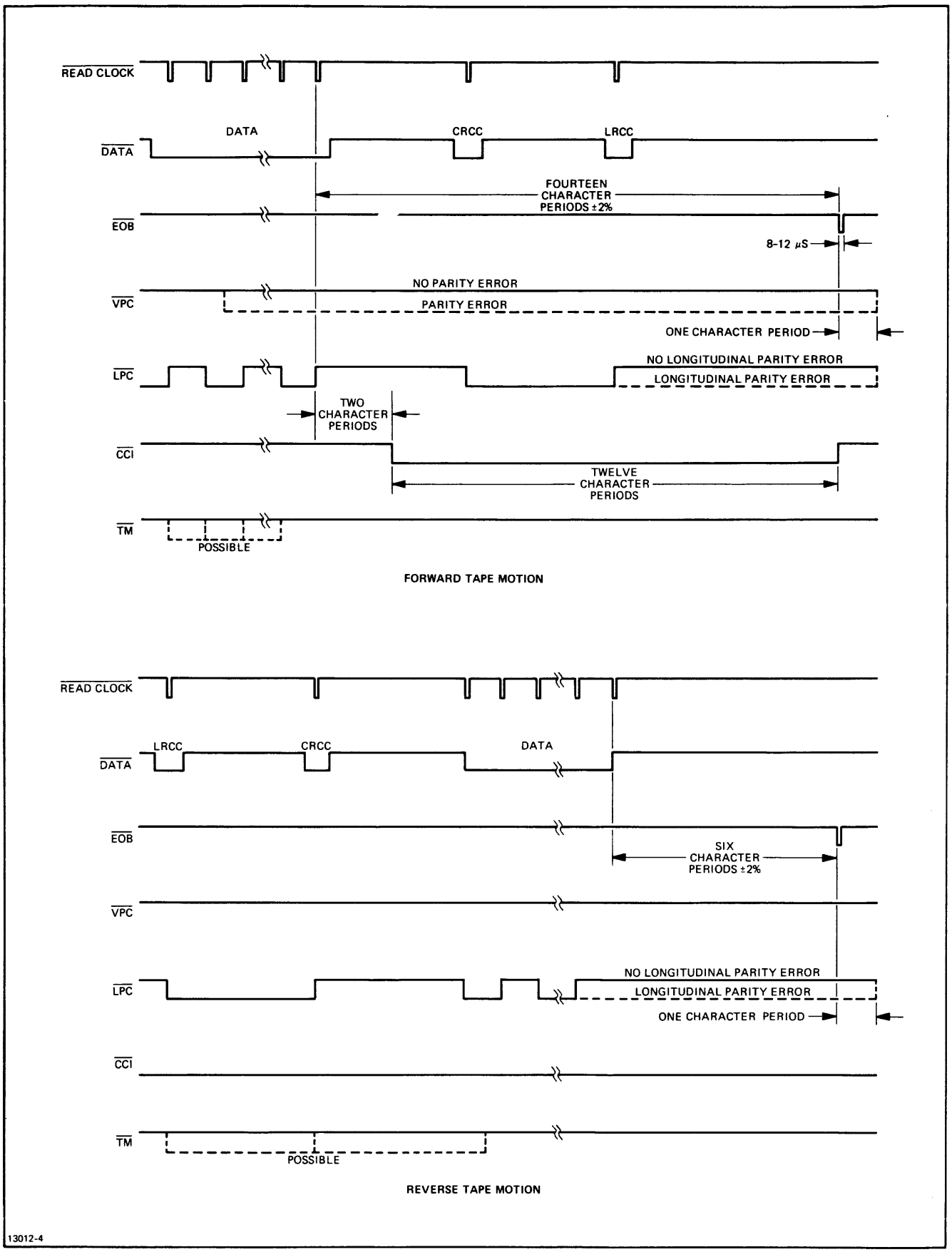


Figure 3-4. Read Parity Event Timing, Nine-Track Operation

SECTION IV
MAINTENANCE

4-1. INTRODUCTION.

4-2. This section provides maintenance information for the HP 13012B Programmable Read Parity Accessory Kit. Included are preventive maintenance, adjustment, troubleshooting, replaceable parts and ordering information, and parts location and schematic diagrams.

4-3. PREVENTIVE MAINTENANCE.

4-4. Detailed preventive maintenance procedures and schedules are provided in the tape unit documentation. There are no separate preventive maintenance procedures to be performed on the read parity accessory.

4-5. ADJUSTMENTS.

4-6. A single frequency adjustment is required to adjust the read parity timing circuits for compatibility with the tape-speed of the tape unit(s) in which the accessory is used. The adjustable component, R23, is shown in figure 4-1.

4-7. REQUIRED TEST EQUIPMENT.

4-8. The following test equipment and tools are required to perform the adjustment procedure:

a. Electronic counter with ±1 count ±0.1% accuracy and 1 Hertz resolution (HP 5221A Frequency Counter or equivalent).

b. A timmmer adjusting tool.

4-9. ADJUSTMENT PROCEDURE.

4-10. Perform the adjustment procedure as follows:

a. With power applied and the read parity accessory installed in the master tape unit, connect a jumper between the TP and GND test points on the read parity PCA.

b. Connect the counter input to the STROBE test point on the read parity PCA.

c. Set the tape unit power switch to on. Select 800 cpi density.

d. Adjust resistor R23 to obtain counter reading listed in table 4-1 according to tape-speed of the tape unit.

e. Set tape unit power switch to off and remove test equipment.

Table 4-1. Read Parity Timing Frequencies for Various Tape Speeds

SPEED (IPS)	TIMING FREQUENCY (kHz)
10	2.000 ± 0.010
12.5	2.500 ± 0.013
20	4.000 ± 0.020
25	5.000 ± 0.025
30	6.000 ± 0.030
37.5	7.500 ± 0.038
45	9.000 ± 0.045

4-11. TROUBLESHOOTING.

4-12. Troubleshooting the read parity accessory is accomplished by performing the tape unit read module performance tests given in the tape unit documentation and analyzing any performance deficiencies. If the malfunction is isolated to the read parity accessory, further isolation of a trouble can be accomplished by referring to the theory of operation given in section III, the parts location and schematic diagrams in figures 4-1 and 4-2, and integrated circuit details in figure 4-3 and table 4-3.

4-13. REPLACEABLE PARTS.

4-14. Table 4-2 lists replaceable parts for the read parity PCA in alphanumeric order by reference designation. Table 4-4 lists explanations of abbreviations used in the part descriptions. Table 4-5 lists manufacturers that correspond to the codes used to identify part manufacturers.

4-15. To order replacement parts, address the order or inquiry to the local HP Sales and Service Office. (Refer to the list at the back of this manual.) Specify the following information.

a. Accessory model number.

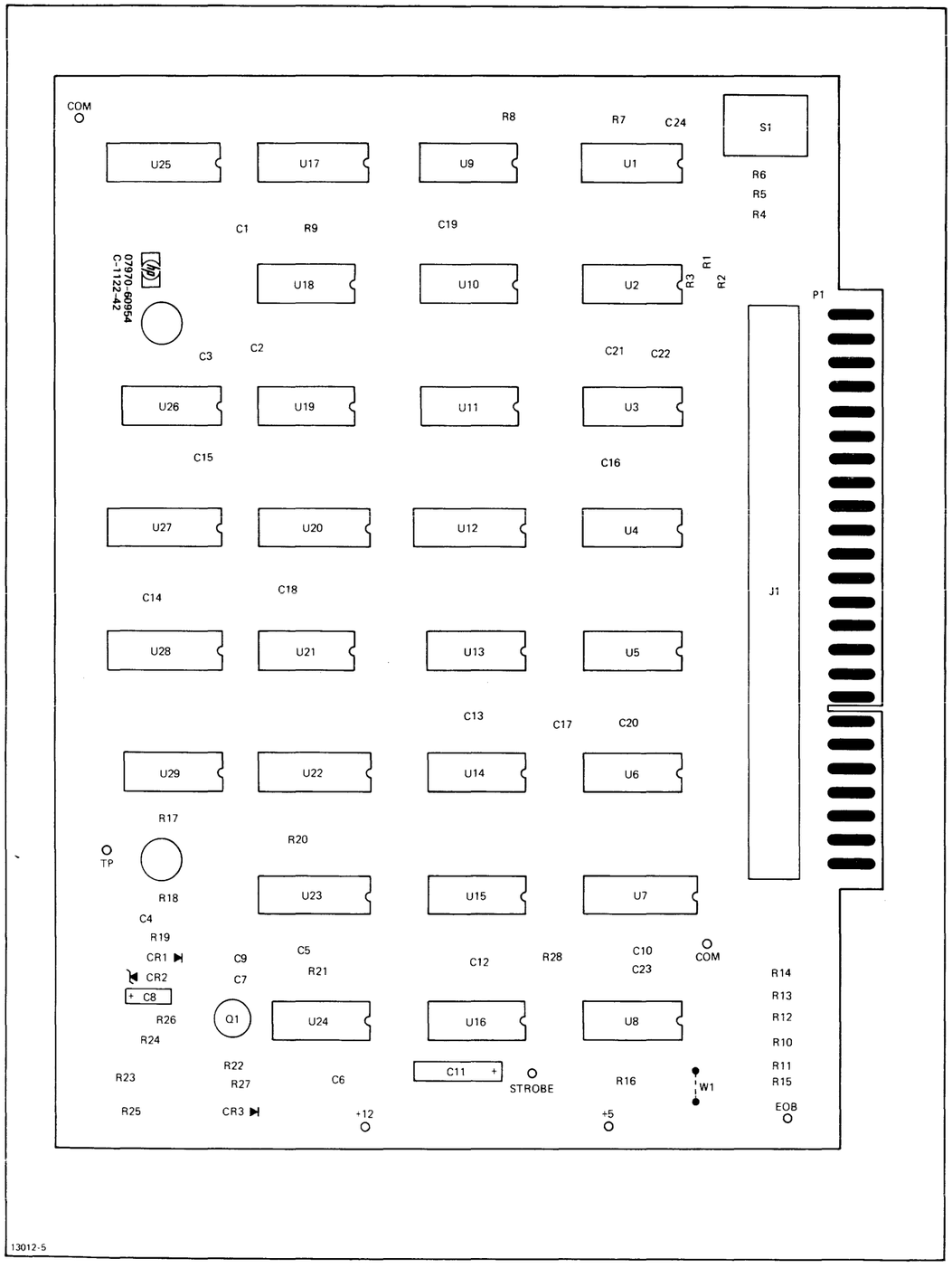
b. HP part number for each part.

c. Description of each part.

d. Circuit reference designation (if applicable).

Table 4-2. Programmable Read Parity PCA (07970-60954) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 2, 3, 7, 10, 12-19, 21-24	0160-2055	CAPACITOR, fxd, cer, 0.01 μF	56289	C023F101F103ZS22-CDH
C4	0160-0161	CAPACITOR, fxd, My, 0.01 μF	56289	192P10392-PTS
C5	0140-0198	CAPACITOR, fxd, mica, 200 pF	72136	RDM15F201J3C
C6	0160-2277	CAPACITOR, fxd, mica, 0.015 μF	72136	RDM30F152G3C
C8	0180-1701	CAPACITOR, fxd, Ta, 6.8 μF, 20%, 6 VDCW	56289	150D658X0006A2-DYS
C9, 20	0160-3449	CAPACITOR, fxd, 0.002 μF, 10%, 250 VDCW	56289	C067B251F202KS25-CDH
C11	0180-0106	CAPACITOR, fxd, Ta, 60 μF, 20%, 6 VDCW	56289	150D606X0006B2-DYS
CR1	1901-0040	DIODE, 30V, 30 mA	07263	FDG1088
CR2	1902-3094	DIODE, breakdown, 5.11V	07910	CD35623
CR3	1901-0025	DIODE, 100V, 200 mA	12065	SG817
Q1	1853-0020	TRANSISTOR	01295	SKA 1123
R1, 3, 5, 7	0757-0418	RESISTOR, fxd, met flm, 619 ohms, 1%, 1/8W	19701	MF4C T-O
R2, 4, 6, 8	0757-1094	RESISTOR, fxd, met flm, 1.47k	19701	MF4C T-O
R9, 28	0683-1025	RESISTOR, fxd, comp, 1k, 1/4W	01121	CB 1025
R10-16	0757-0428	RESISTOR, fxd, met flm, 1.62k, 1%, 1/8W	19701	MF4C T-O
R17	0757-0279	RESISTOR, fxd, met flm, 3.16k, 1%, 1/8W	75042	CEA T-O
R18, 22	0698-3155	RESISTOR, fxd, met flm, 4.64k, 1%, 1/8W	19701	MF4C T-O
R19	0683-1035	RESISTOR, fxd, comp, 10k, 1/4W	01121	CB 1035
R20	0698-3150	RESISTOR, fxd, met flm, 2.37k, 1%, 1/8W	19701	MF4C T-O
R21	0698-0085	RESISTOR, fxd, met flm, 2.61k, 1%, 1/8W	19701	MF4C T-O
R23	2100-3138	RESISTOR, var, 25k	32991	3005P-1-253
R24	0698-3400	RESISTOR, fxd, met flm, 147 ohms, 1/2W	19701	MF4C T-O
R25	0757-0317	RESISTOR, fxd, met flm, 1.33k, 1%, 1/8W	75042	CEA T-O
R26	0757-0420	RESISTOR, fxd, met flm, 750 ohms, 1%, 1/8W	19701	MF4C T-O
R27	0757-0278	RESISTOR, fxd, met flm, 1.78k, 1%, 1/8W	75042	CEA T-O
S1	3101-0973	SWITCH, slide, dpdt	79727	GF126-0018A
U1, 10	1820-0282	INTEGRATED CIRCUIT	01295	SN 13603
U2, 4, 11	1820-0128	INTEGRATED CIRCUIT DTL	04713	MC 837P
U2, 4, 11	1820-0894	IC TTL		
U3, 14	1820-0349	INTEGRATED CIRCUIT DTL	07263	SL 16216
U3, 14	1820-2054	IC TTL		
U5	1820-0376	INTEGRATED CIRCUIT	01295	SN 4484
U6, 19, 21, 29	1820-0054	INTEGRATED CIRCUIT	01295	SN 4342
U7, 12, 16, 17, 20, 22, 23, 25, 27, 28	1820-0076	INTEGRATED CIRCUIT	01295	SN 7476
U8	1820-0256	INTEGRATED CIRCUIT	04713	SC 8161PK
U9, 26	1820-0454	INTEGRATED CIRCUIT	04713	SC 8968PK
U13	1820-0348	INTEGRATED CIRCUIT DTL	07263	SL 16215
U13	1820-1256	IC TTL		
U15	1820-0141	INTEGRATED CIRCUIT DTL	04713	SC 7514PK
U15	1820-0891	IC TTL		
U18	1820-0435	INTEGRATED CIRCUIT	01295	SN 14656
U24	1820-0207	INTEGRATED CIRCUIT	07263	SL 12895
*U29	1820-0344	" "		



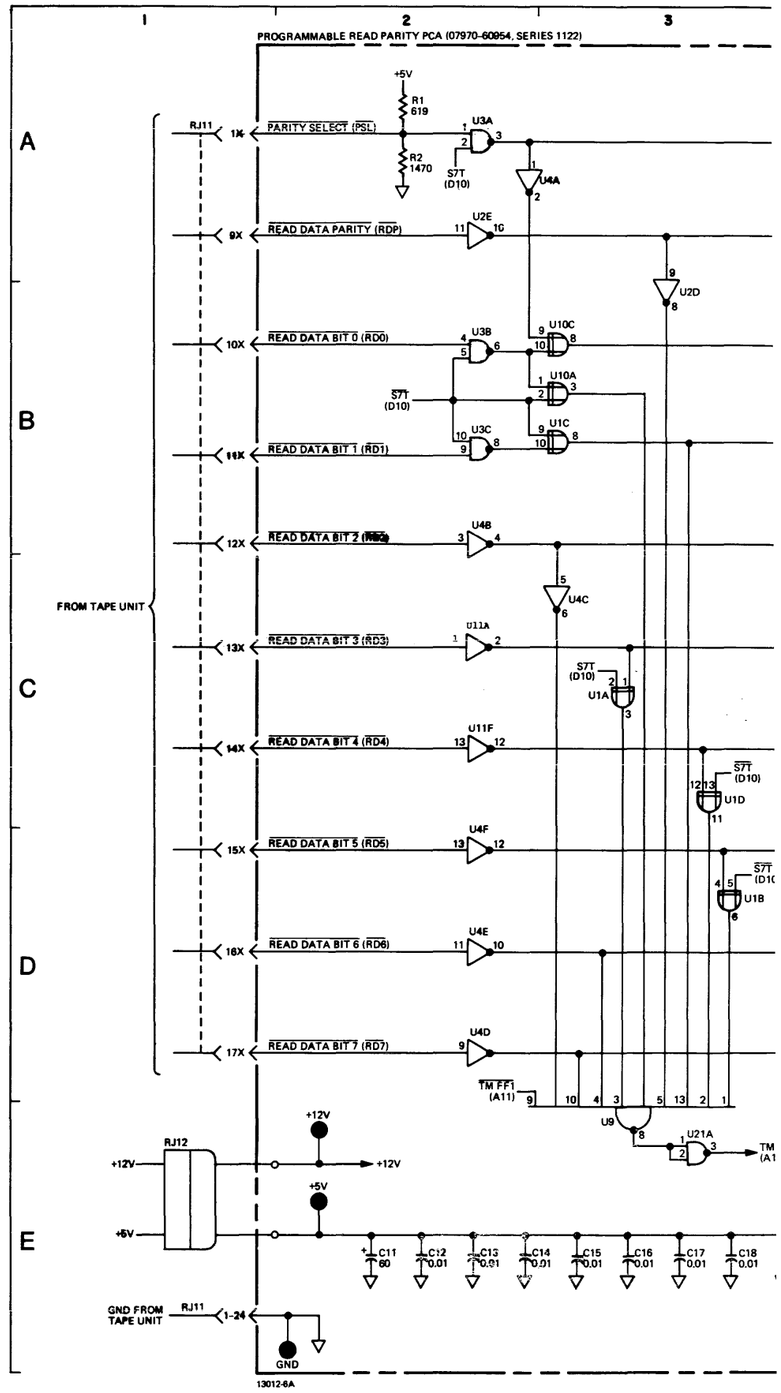
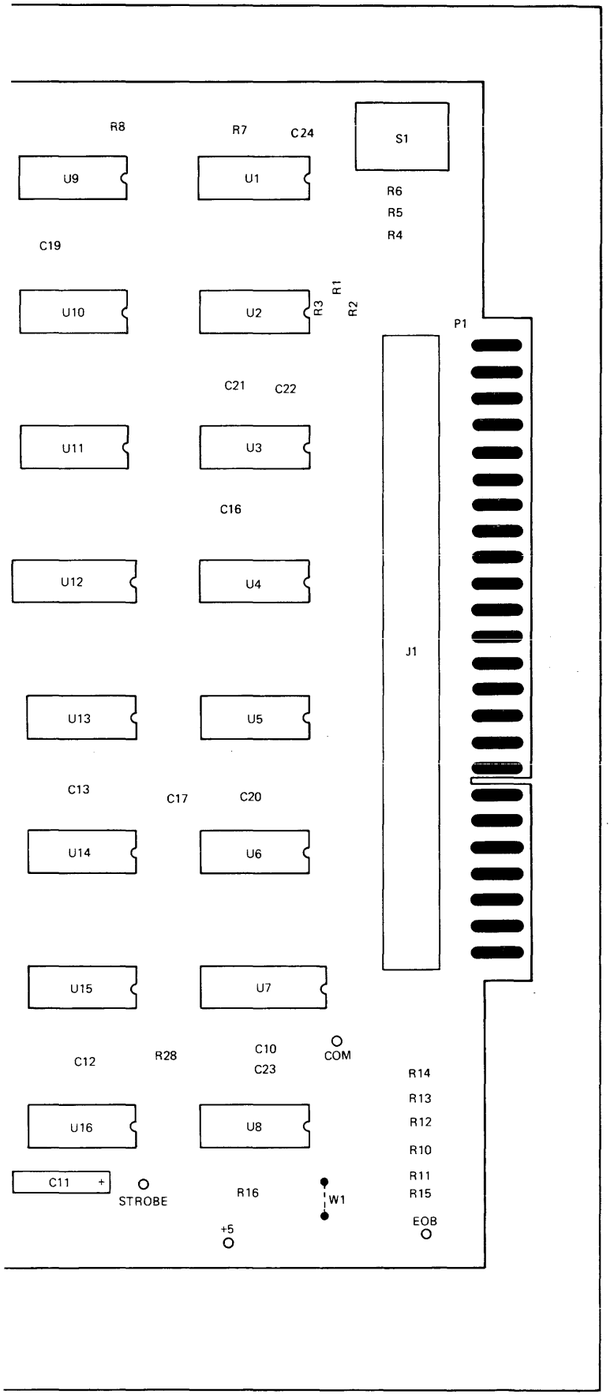
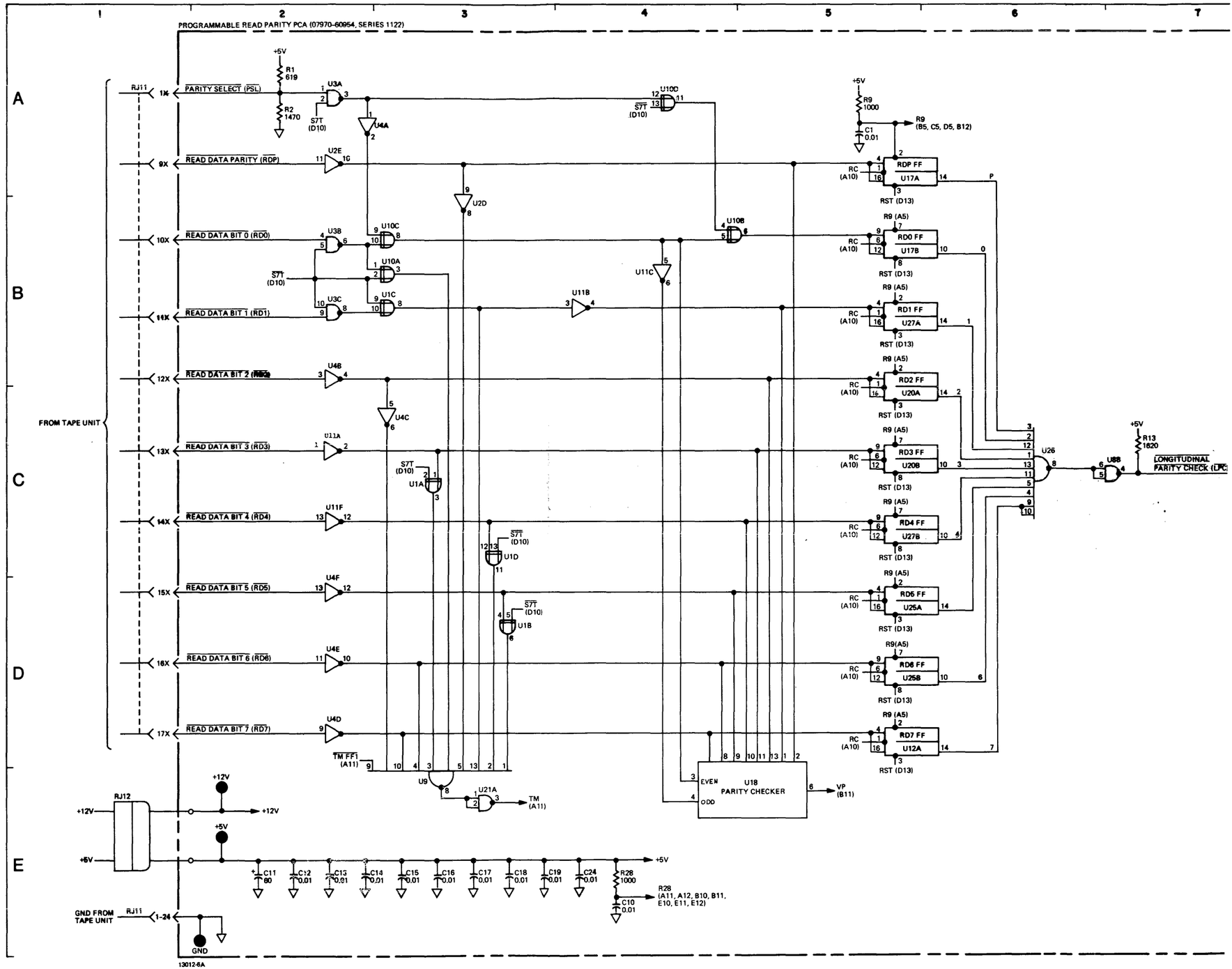


Figure 4-1. Programmable Read Parity PCA Parts Location Diagram





le Read Parity PCA Parts Location Diagram

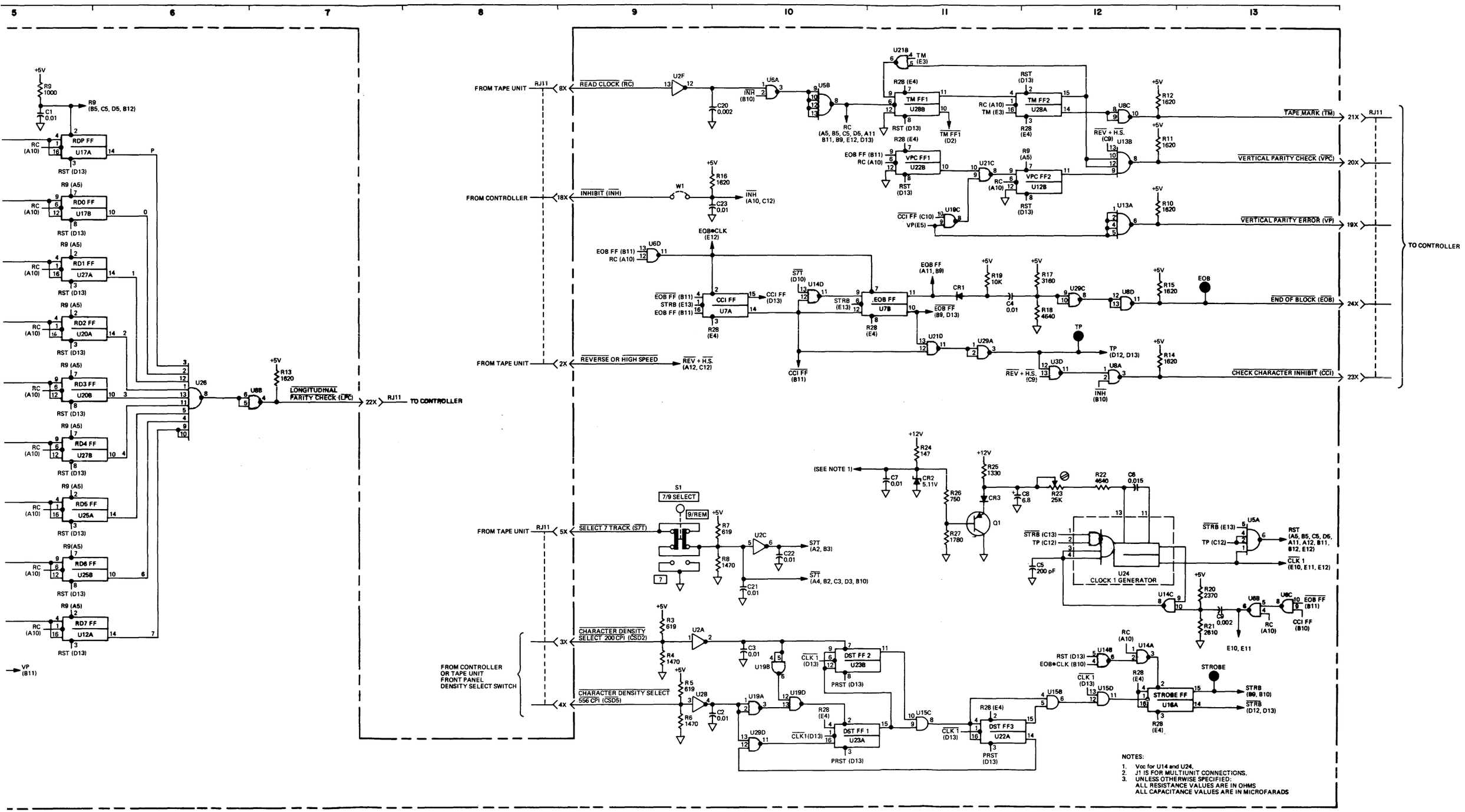


Figure 4-2. Programmable Read Parity Schematic Diagram

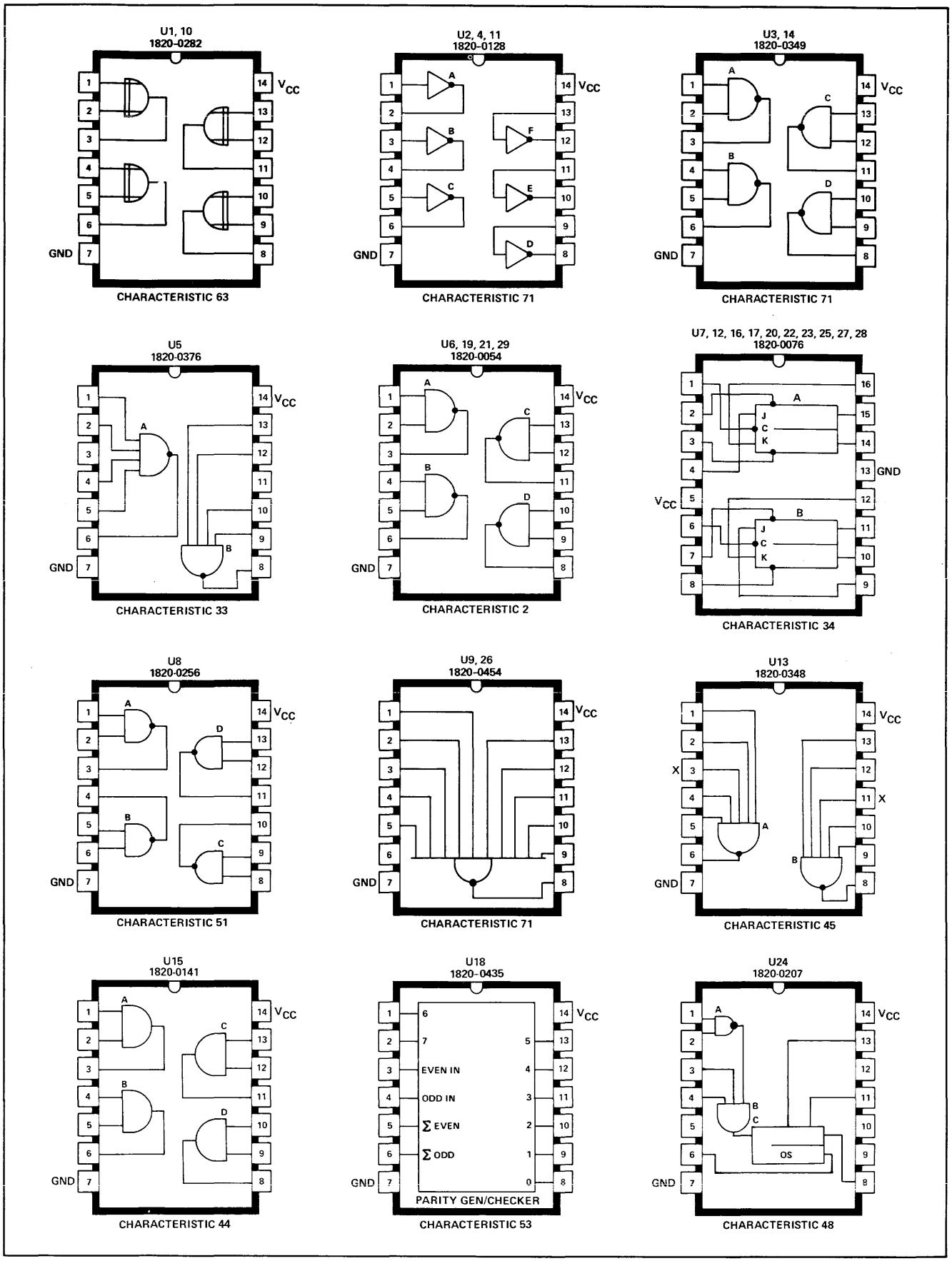


Figure 4-3. Integrated-Circuit Pack Diagrams

Table 4-3. Integrated Circuit Characteristics

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
2	2.0	0.8	2.4	0.4	Logic 1	15	15
33	2.0	0.8	2.4	0.4	Logic 1	11	11
34	2.0(1)	0.8	2.4	0.4	Logic 1	30	45
44	1.8	1.1	2.5	0.4	Logic 1	15	15
45	2.0	1.1	(2)	0.5	Logic 1	50	35
48	1.9	0.85	2.4	0.45	Logic 1	40	—
51	1.8	1.1	(2)	0.45	Logic 1	50	35
63	2.0	0.8	2.4	0.4	Logic 1	23 and 30	17 and 22
71	2.0	0.8	2.4	0.4	Logic 1	30	22

NOTES:

1. Required clock pulse widths 20 ns min.
2. Level depends on load.

Table 4-4. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor, synchro	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit, non-repairable assembly
C	= capacitor	P	= plug connector	V	= vacuum tube, photocell, etc.
CB	= circuit breaker	Q	= semiconductor device other than diode or integrated circuit	VR	= voltage regulator
CR	= diode	R	= resistor	W	= jumper wire
DL	= delay line	RT	= thermistor	X	= socket
DS	= indicator	S	= switch	Y	= crystal
E	= Misc electrical parts	T	= transformer	Z	= tuned cavity, network
F	= fuse				
FL	= filter				
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gra	= gray	PCA	= printed-circuit assembly
ac	= alternating current	grn	= green	PWB	= printed-wiring board
Ag	= silver			phh	= phillips head
Al	= aluminum	H	= henries	pk	= peak
ar	= as required	Hg	= mercury	p-p	= peak-to-peak
adj	= adjust	hr	= hour(s)	pt	= point
assy	= assembly	Hz	= hertz	prv	= peak inverse voltage
		hdw	= hardware	PNP	= positive-negative-positive
b	= base	hex	= hexagon, hexagonal	pwv	= peak working voltage
bp	= bandpass			porc	= porcelain
bpi	= bits per inch	ID	= inside diameter	posn	= position(s)
blk	= black	IF	= intermediate frequency	pozi	= pozidrive
blu	= blue	in.	= inch, inches		
brn	= brown	I/O	= input/output	rf	= radio frequency
brs	= brass	int	= internal	rdh	= round head
Btu	= British thermal unit	incl	= include(s)	rms	= root-mean-square
Be Cu	= beryllium copper	insul	= insulation, insulated	rwv	= reverse working voltage
		impgrg	= impregnated	rect	= rectifier
cpi	= characters per inch	incand	= incandescent	r/min	= revolutions per minute
coll	= collector	ips	= inches per second	RTL	= resistor-transistor logic
cw	= clockwise				
ccw	= counterclockwise	k	= kilo (10^3), kilohm	s	= second
cer	= ceramic			SB, TT	= slow blow
com	= common	lp	= low pass	Se	= selenium
crt	= cathode-ray tube			Si	= silicon
CTL	= complementary-transistor logic	m	= milli (10^{-3})	scr	= silicon controlled rectifier
		M	= mega (10^6), megohm	sst	= stainless steel
cath	= cathode	My	= Mylar	stl	= steel
Cd pl	= cadmium plate	mfr	= manufacturer	spcl	= special
comp	= composition	mom	= momentary	spdt	= single-pole, double-throw
conn	= connector	mtg	= mounting	spst	= single-pole, single-throw
compl	= complete	misc	= miscellaneous		
		met. ox.	= metal oxide		
dc	= direct current	mintr	= miniature		
dr	= drive			Ta	= tantalum
DTL	= diode-transistor logic	n	= nano (10^{-9})	td	= time delay
depc	= deposited carbon	nc	= normally closed or no connection	Ti	= titanium
dpdt	= double-pole, double-throw			tgl	= toggle
dpst	= double-pole, single-throw	Ne	= neon	thd	= thread
		no.	= number	tol	= tolerance
em	= emitter	n.o.	= normally open	TTL	= transistor transistor logic
ECL	= emitter-coupled logic	np	= nickel plated		
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative-positive zero (zero temperature coefficient)	U(μ)	= micro (10^{-6})
elctlt	= electrolytic	NSR	= not separately replaceable		
		NRFR	= not recommended for field replacement	V	= volt(s)
F	= farads			var	= variable
FF	= flip-flop			vio	= violet
flh	= flat head	OD	= outside diameter	Vdcw	= direct current working volts
flm	= film	OBD	= order by description		
fxd	= fixed	orn	= orange	W	= watts
filh	= fillister head	ovh	= oval head	ww	= wirewound
		oxd	= oxide	wht	= white
G	= giga (10^9)			WIV	= working inverse voltage
Ge	= germanium	p	= pico (10^{-12})		
gl	= glass	PC	= printed circuit	yel	= yellow
gnd	= ground(ed)				

Table 4-5. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
01121	Allen-Bradley Company	Milwaukee, Wisconsin
01295	Texas Instruments Inc., Semiconductor Components Division	Dallas, Texas
04713	Motorola Semiconductor Products Inc.	Phoenix, Arizona
07263	Fairchild Camera, Inst. Corp., Semiconductor Division	Mountain View, California
07910	Continental Device	Hawthorne, California
12065	Transitron Electronic Corporation	Boston, Massachusetts
19701	Electra Mfg. Co.	Independence, Kansas
32997	Bourns, Inc. Trimpot Products Division	Riverside, California
56289	Sprague Electric Company	N. Adams, Massachusetts
72136	Electro Motive Mfg. Co., Inc.	Willimantic, Connecticut
75042	IRC Division of TRW Inc.	Philadelphia, Pennsylvania
79727	Continentalwirt Electronics Corporation	Philadelphia, Pennsylvania

13012-90003

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