HP 13220A

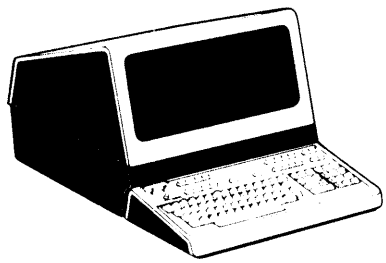
02620-60175 MEMORY EXTENDER MODULE

Manual Part No. 13220-91175

PRINTED

DECEMBER 8, 1981

DATA TERMINAL
TECHNICAL INFORMATION



HEWLETT hp PACKARD

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1.0 INTRODUCTION.

The 2626W Memory Extender PCA provides memory that can be programmed to overlay user-selected portions of the 02620-60093 processor's 64K memory address space. The Memory Extender's 64K words of RAM may be assigned to the processor's address space in chunks of 1K words, and they may be optionally designated as Read Only, Write Only, or Read-Write. Allocation of memory and the assigning of options is done by writing into a static RAM register file.

A more detailed description of the functionality of the Memory Extender and the information necessary to configure the board is contained in Section 3.1.

The 02620-60093 processor PCA uses the MC5, an HP custom microprocessor. An understanding of the operation of the MC5 is necessary for the use of this document.

2.0 OPERATING PARAMETERS.

A summary of operating parameters of the Memory Extender Module is contained in tables 1.0 through 4.0.

Table 1.0 Physical Parameters

PART NUMBER	NOMENCLATURE	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02620-60175	Memory Extender PCA	204 x 158 x 11	N/A

NUMBER OF BACKPLANE SLOTS REQUIRED: N/A

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NOTE: This document is part of the 262XX DATA TERMINAL product series Technical Information Package (HP 13220).

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Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	2.5 (percent per 100 hours)

Table 3.0 Power Supply and Clock Requirements — Measured
(At +/−5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	−12 Volt Supply	−42 Volt Supply
@ 1.5 A	@ mA N/A	@ mA N/A	@ mA N/A

115 volts ac	220 volts ac
@ A N/A	@ A N/A

Clock Frequency: N/A MHz

Table 4.0 Connector Information (Memory Extender PCA)

CONNECTOR AND PIN NO.	SIGNAL NAME	SIGNAL DESCRIPTION
J1		
-1	+12v	Power (not used)
-2		
-3	NEND	Negative true, END signal to MC5
-4	D15	Data (LSB)
-5	NXDI	Negative true, External device interrupt
-6	D13	Data
-7	D14	.
-8	D11	.
-9	D12	.
-10	D09	.
-11	D10	.
-12	+5v	Power
-13	D08	Data
-14	+5v	Power
-15		
-16	D07	Data
-17	PON	Power on.
-18	D06	Data
-19	BMEM	Processor board Memory Go
-20	D05	Data
-21		
-22	D04	Data
-23	GND	Ground
-24	D03	Data
-25	GND	Ground
-26	D02	Data
-27	GND	Ground
-28	D01	Data
-29	GND	Ground
-30	D00	Data (MSB)
-31	A03	Address
-32	A01	.
-33	A05	.
-34	A00	. (MSB)
-35	A07	.
-36	A02	.
-37	A09	.
-38	A04	.
-39	A11	.
-40	A06	.
-41	A13	.
-42	A08	.
-43	A15	. (LSB)
-44	A10	.
-45	A14	.
-46	A12	.
-47	NCLK	System Clock (Negative True)
-48	NMGO	Memory Go (Negative True)
-49	NIOGO	IO GO (Negative True)
-50	WH/RDL	Write/Not Read (Negative True)

3.0 FUNCTIONAL DESCRIPTION

Refer to the block diagram (FIGURE 1), schematic diagram (FIGURE 2) timing diagram (FIGURE 4,5,6), component location diagram (FIGURE 3), and parts list (02620-60175) located in the appendix.

The Memory Extender is logically divided into three sections: the Memory Array and Refresh circuitry section, Configuration RAM section, and the State-machine section. These are described in sections 3.1, 3.2, and 3.3 respectively. Section 3.4 describes how the board is turned on and off and how that affects the control of the bus.

3.1 Memory Array and Refresh Circuitry

The 64K words of dynamic RAM have been organized as follows: there are two "environments", E0 and E1, of 32K words each, and each environment has been further divided into two banks, B0 and B1, of 16K words each. This is illustrated in Figure 3.1-1.

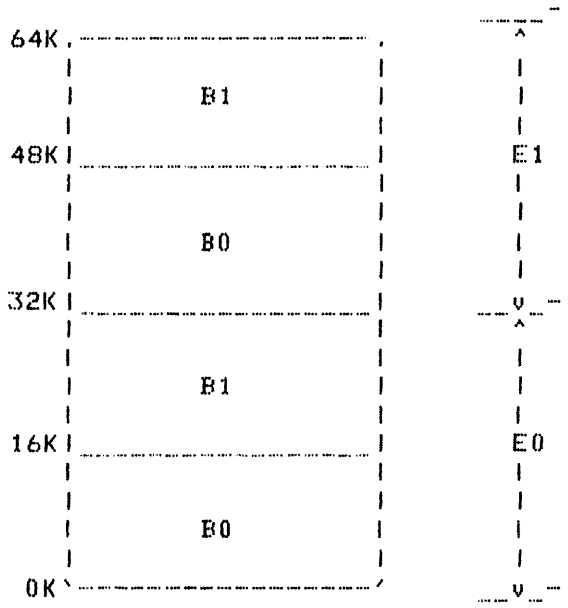
The two most significant address bits, A0 and A1, have been replaced by the two signals FLOP and BSEL at the inputs to U93, the address multiplexor. These two signals control the selection of environment and bank, respectively.

Each 16K word bank of memory is arranged as shown in Figure 3.1-2. Note that the two address bits A0 and A1 are not used. Because of this, each word in each bank may be located in any of four places in the MC5 memory address space. For example, location !1000 in either bank maps into all of the following memory locations: !1000, !5000, !9000, and !D000. Conversely, each memory location in the MC5 memory address space may be overlayed with one word of RAM in either bank.

Additionally, address bit A02 has been exclusive-nored with a signal called NSWAP which is under the control of the user. When NSWAP has been asserted, the value of the address line that goes to the RAMs in place of A02 is the inverse of A02. This gives the user the ability to programmatically select either the upper half or the lower half of either memory bank, B0 or B1.

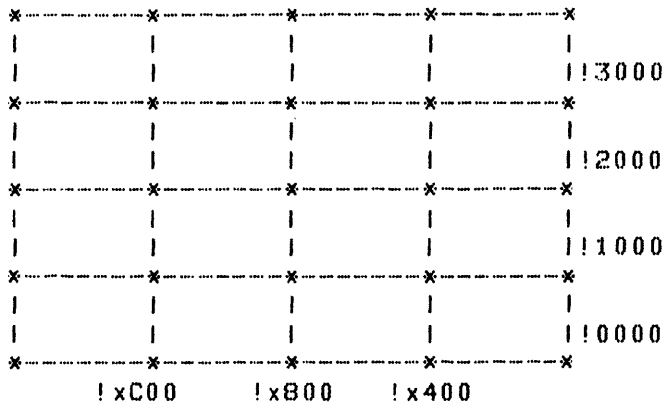
The timing diagram for memory read and write operations, (FIGURE 4) can be found in the appendix.

The refresh circuitry is shown on page two of the schematic in the lower left quadrant. It consists of an LS161 4-bit counter, an LS393 dual 4-bit counter, an LS244 octal buffer, some D flip flops, and two nand gates. The LS161 is enabled and clocked every four clock periods so that the carry-out line of the counter (RFCO) initiates a refresh cycle every sixty clock periods. This is accomplished with the control of the state machine. With this system, 128 row addresses have RAS-only cycles performed every 1.5 milliseconds, well within the requirements of the 64K RAMs. The timing of the refresh cycle is shown in (FIGURE 5) in the appendix.



Memory Array Organization

Figure 3.1-1



Memory Bank Organization

Figure 3.1-2

3.2 Configuration RAM

The memory address space of the MC5 is 64K words. For the purposes of the Memory Extender it has been organized as follows: sixteen rows of four 1K blocks. This is illustrated in Figure 3.2-1.

The configuration RAMs are organized as shown in Figure 3.2-2. There are sixteen registers of eight bits each. The lower eight registers are addressed through register base RB!40, and the upper eight registers are addressed through register base RB!41.

The four least significant bits in each register, D12, D13, D14, and D15, correspond to the four 1K blocks in each row of Figure 3.2-1. For example, bit D14 in xr7 of register base !40 corresponds to the 1K chunk of memory starting at location !7400.

The four most significant bits in each register, D8, D9, D10, and D11, are used to assign the following options: Read, Write, Bank Select, and Swap. These options, when assigned, will apply only to the four 1K blocks which are represented by that particular register.

The bits D12 through D15 and the Read and Write bits determine whether the Memory Extender will respond to a particular operation at a given memory address. Writing a one to any of the bits D12 through D15 turns on the Memory Extender for the corresponding 1K chunks of memory. Writing a one to either or both of the Read and Write bits enables either or both of those operations for any of the turned-on 1K chunks in that row.

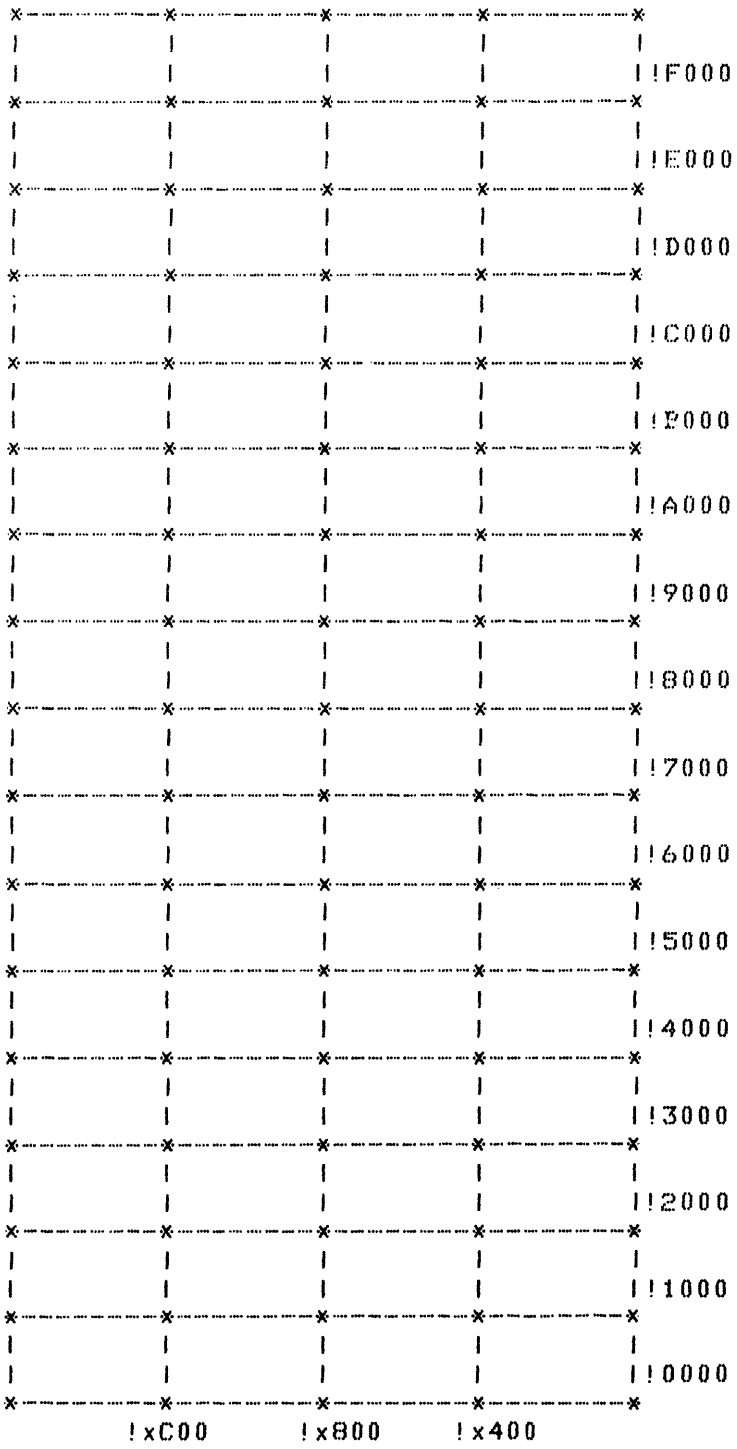
The functions of the Bank Select bit (D10) and the Swap bit (D11) are dictated by the organization of the 64K memory array. This organization is illustrated in Figures 3.2-1 and 3.2-2. and has been described in section 3.1.

Note that only 16K words may be allocated to any one bank. These words need not be contiguous, and they need not be limited by 16K boundaries. But, in allocating memory locations to either Bank 1 or Bank 0, which are identical, the programmer must take into account the system of mapping between the banks and the MC5 memory address space.

For example, the 8K block of words located at !6000 to !7FFF maps into the upper half of either bank. The 8K block located at !A000 to !BFFF also maps into the upper half of the bank. Since both of these 8K blocks of words map into the same half of the bank they cannot both be assigned to the same memory bank without disaster unless the Swap option is employed. Assigning the Swap option to one of the 8K blocks of words inverts address line A02 every time a word in that block is addressed and therefore maps that 8K block into the lower half of the bank.

The choice of environment, E0 or E1, is made by writing to bit 14 of any external register in register base RB!45. For this reason, at any one time only one environment of 32K words may be allocated. When more than one environment is allocated, then bit 14 must be changed and new configuration information relevant to the second environment must be written to the configuration RAM.

The timing diagram for read and write operations with the configuration RAMs, FIGURE 6, can be found in the appendix.



MC5 Memory Address Space

Figure 3.2-1

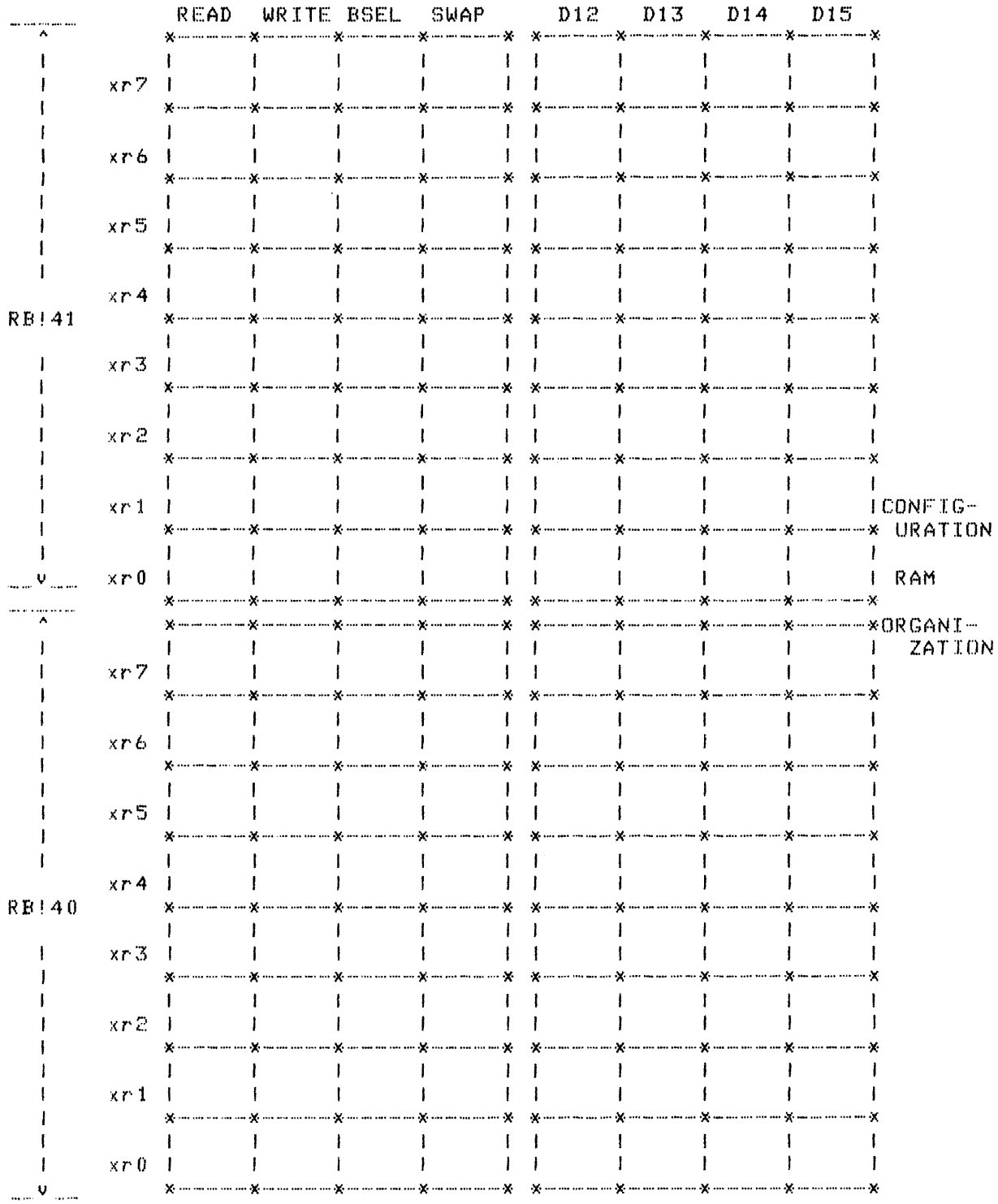

READ
WRITE
BSEL
SWAP
D12
D13
D14
D15
xr7
xr6
xr5
xr4
xr3
xr2
xr1
xr0
RB!41
RB!40
CONFIG-
URATION
RAM
ORGANI-
ZATION

Figure 3.2-2

3.3 State Machine

All functions of the Memory Extender are controlled by the state machine which consists of U84 (a field programmable logic array), U54 (a 32-word by 8-bit PROM), U44 (an eight-to-one multiplexor), U64 (an eight bit latch), and U85 (an eight-to one multiplexor.) It handles the refresh cycle, IO cycles (reading from and writing to the configuration RAMs), determines whether or not the memory word addressed has been allocated to the RAM on the board, and handles the memory operations with the RAM on the board.

The flow chart for the state machine is shown in drawing number B-13220-91175-4 (FIGURE 7) in the appendix, and the contents of the state machine PROM is shown in drawing number A-13220-91175-5 (FIGURE 7). Essentially, the state machine continually samples the signals Refresh Go (RFGO), Configuration Cycle (CONFIG), and Dynamic Memory Go (DMGO). When a signal is found to be true, the appropriate section of the state machine PROM code is jumped to and executed. Then, sampling of the three signals is resumed. Note the timing diagram located in the appendix.

The function of determining whether or not the addressed memory location has been allocated to the Memory Extender is performed by the state machine using the information stored in the configuration static RAMs. First, note that the configuration RAMs may be addressed in two different ways depending on the state of the signal End Configuration (ENDC). When that signal is true (during an IO operation, either read or write, to the configuration RAMs) then the RAMs are addressed by address lines A7, A13, A14, and A15. This makes the configuration RAM words available to the programmer as external registers as explained in section 3.2.

When ENDC is false then the RAMs are addressed by address lines A00, A01, A02, and A03. These address lines will then address the register corresponding to the correct row in the memory address map. Note the correspondence between the map of the memory address space in Figure 3.2-1 and the organization of the configuration RAMs. In other words, when each memory operation is initiated, the most significant four address bits address the configuration RAM word which contains the answer to the question: Is this word allocated for this operation?

The allocation information is transmitted via the signal MEMALL (Memory Allocated) to the FPLA. There, if the state of the signals NREAD and NWRITE are compatible with the state of the signal WH/RDL, then the signal DMGO (Dynamic Memory Go) is generated. If not, (if, for example, a write operation is attempted and the word addressed has been configured as Read Only) then DMGO is not generated and instead the signal NROMGO is generated and becomes the signal BMEM on the processor board.

In the state machine, random logic has been combined into the field programmable logic array (FPLA). The contents of this device are shown in HP document number A-1820-2615-1.

3.4 On/Off Switch

The Memory Extender may be turned on or off by writing either a one or a zero, respectively, to bit 15 of any external register in register base RB!45. When the board has been turned off none of the memory on the board may be accessed by the processor regardless of whether it has been allocated (ie. regardless of the information stored in the configuration RAMs.) Upon power-on, the Memory Extender is off.

When the Memory Extender is on, it claims priority over the ROMs and RAMs on the processor board. In this case, every time Memory Go (MGO) is asserted by the MC5, the Memory Extender intercepts the signal and sends it to the state machine. Then, the decision is made as to whether the memory transaction should take place. (Is the word allocated to the Memory Extender? Is the word optioned for the operation requested?)

If the decision is made that the memory transaction "belongs" to the Memory Extender then it takes place and the End signal (NEND) is sent to the MC5 as an indication that the transaction is complete. If the decision is made that the memory transaction does not "belong" to the Memory Extender, then the signal Rom Go (NROMGO) is generated and sent to the memory on the processor board. From the time that the MC5 initiates MGO to the time that the processor's memory sees the signal Board Memory Go (BMEM) (which is essentially NROMGO) there is a delay of approximately one clock cycle.

When the board has been turned off, or upon power-on, the Memory Extender remains passive on the MC5 bus, and the decision-making process described above is circumvented. The signal Memory Allocated (MEMALL) is gated by the ON/OFF signal, therefore, when the board is off, no memory cycles are initiated. Also, when the signal ON/OFF is false (the board is off) the signal Board Memory Go (BMEM) is held high, allowing immediate MC5 interaction with the processor's ROM and RAM.

4.0 Glossary of Signal Names

An	MC5 address lines (A00 to A15 where A00 is the MSB)
BMEM	Board Memory Go. Rom Go signal gated by On/Off signal.
BSEL	Bank Select. Chooses between Bank0 and Bank1 for a particular 4K block of memory locations.
CAS	Column Address Strobe.
CONFIG	Signals an eligible IO transaction (ie. correct RB)
DMGO	Dynamic Memory Go. Starts a memory cycle with Memory Extender RAM.
Dn	MC5 data lines (D0 to D15 where D0 is the MSB)
ENDC	End Configuration. Signals the MC5 that data transfer during an IO operation has been completed.
ENDINIT	Signals the end of the init cycle on the 32K word version. Not currently used.
FLOP	Indicates environment. 0 is E0, 1 is E1.
INT	Interrupt line from the HP-IB controller. Not used currently.
MEMALL	Memory Allocated. Indicates that the word addressed has been allocated to the Memory Extender.
NADDREN	Address Enable. Enables the address multiplexor for the 64K RAMs.
NCLK	MC5 system clock.
NEND	End. Signals the MC5 that the data has been taken (write) or that the data is available (read).
NERFEN	Early Refresh Enable. Refresh Enable Signal taken before the latch.
NIOGO	Go signal for MC5 IO transactions.
NMEMEN	Memory Enable. Advances state machine program and enables the enable for the memory address.
NMGO	Go signal for MC5 memory transactions.
NMGODLY	Memory Go Delayed. Clocked Memory Go signal.
NREAD	Indicates whether read operations are enabled for a particular 4K block of memory locations.
NRFEN	Refresh Enable. Enables the refresh address buffer.
NRFEND	Refresh End. Initiates the end of the refresh cycle and resets the refresh counter.
NROMGO	ROM Go. Memory Go signal to the memory on the processor board.
NRSRAM	Read Static RAM. Allows data read from configuration RAMs access to the data bus.
NSWAP	Indicates whether the Swap option has been chosen (and A02 inverted) for a particular 4K block of memory location

NWDRAM	Write Dynamic RAM. Write signal to the 64K RAMs.
NWINIT	Used only on 32K version of Memory Extender.
NWRITE	Indicates whether write operations are enabled for a particular 4K block of memory locations.
NWSRAM	Write Static RAM. Write signal to the configuration RAMs.
NWSRAMDLY	Write Static RAM Delayed. Clocked Write Static RAM signal.
NXDI	External Device Interrupt. Interrupt line to the processor board.
ON/OFF	Indicates whether Memory Extender is enabled.
PHIEND	Phi End. HP-IB controller end signal. Not currently used.
PON	Power On reset signal.
RAS	Row Address Strobe.
RDn	Data read from configuration RAMs. (RD12 to RD15)
RFGO	Refresh Go. Output from refresh circuit initiates the refresh cycle.
RSL/CSH	Row Select Low/Column Select High. Selects between column and row addresses.
WEN	Write Enable. Precedes data transfer in either direction.
WH/RDL	Write High/Read Low signal. Indicates read or write operation.

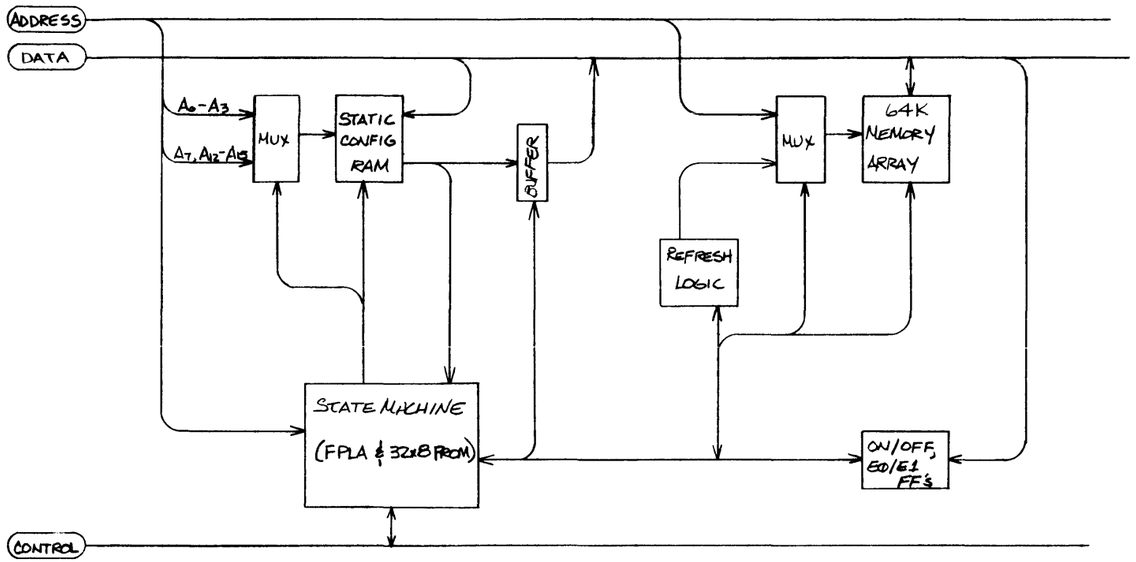


FIGURE 1
MEMORY EXTENDER BLOCK DIAGRAM
DEC-08-81 13220-91175

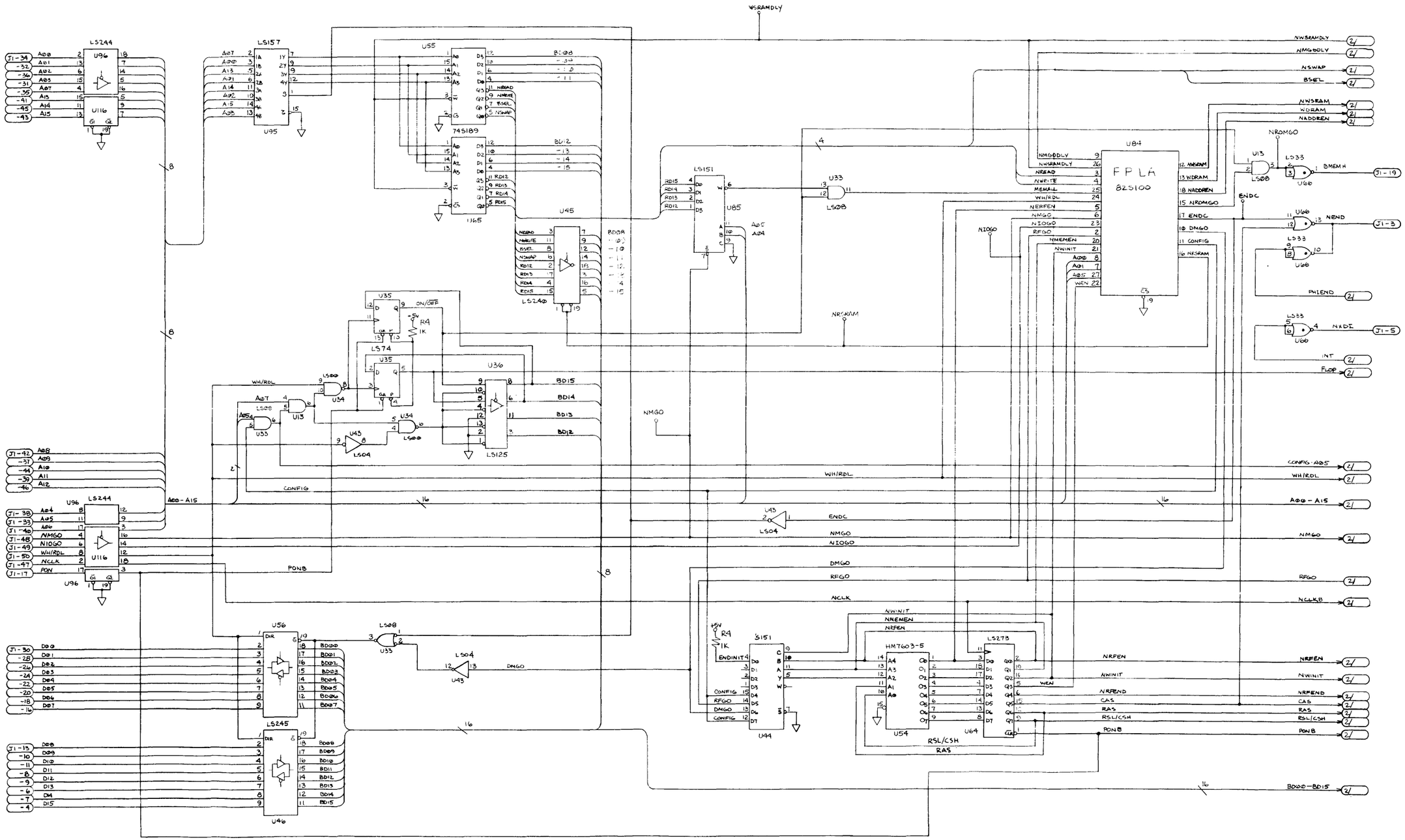
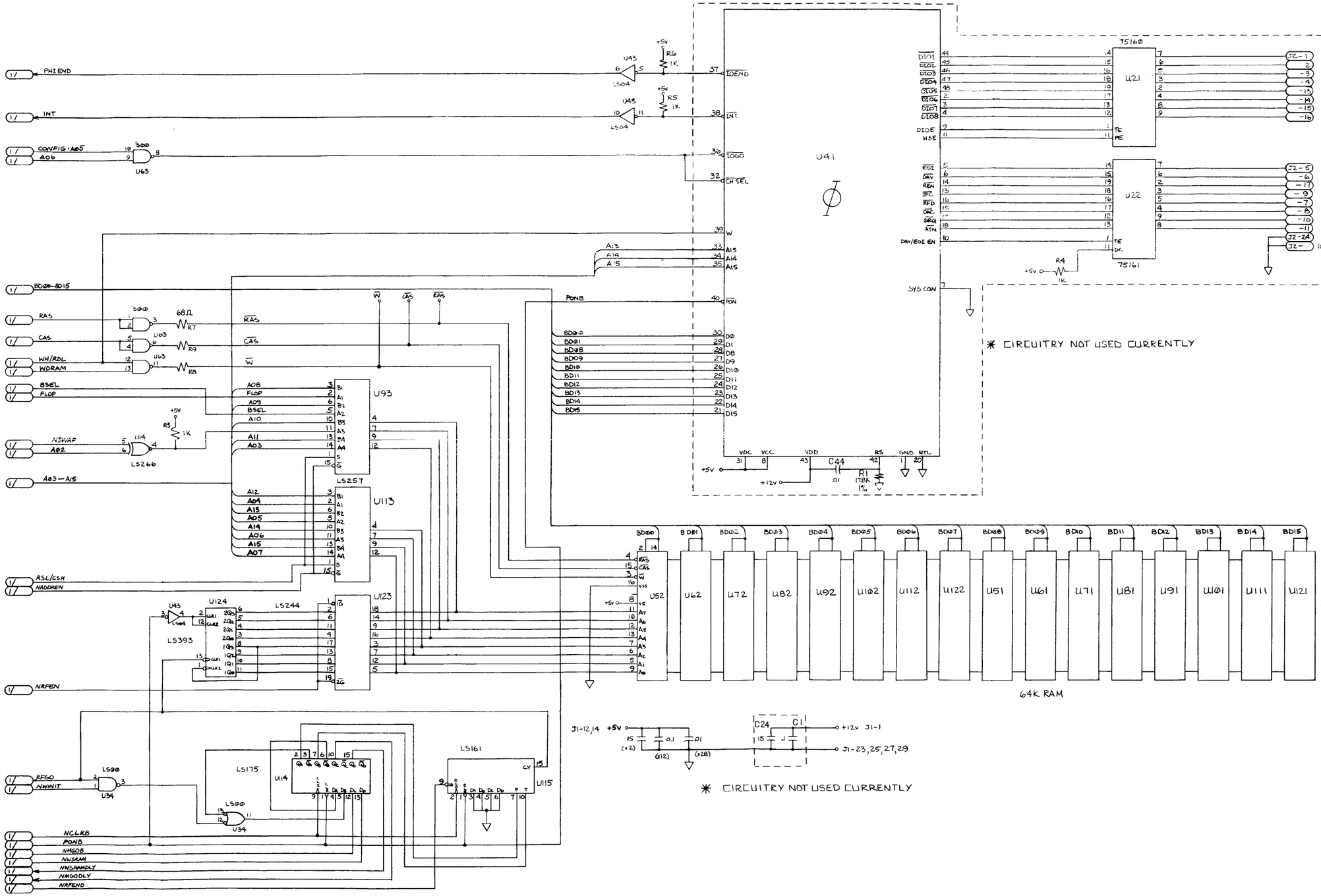


FIGURE 2
MEMORY EXTENDER SCHEMATIC DIAGRAM
DEC-08-81 13220-91175



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DEC-08-81 13220-91175

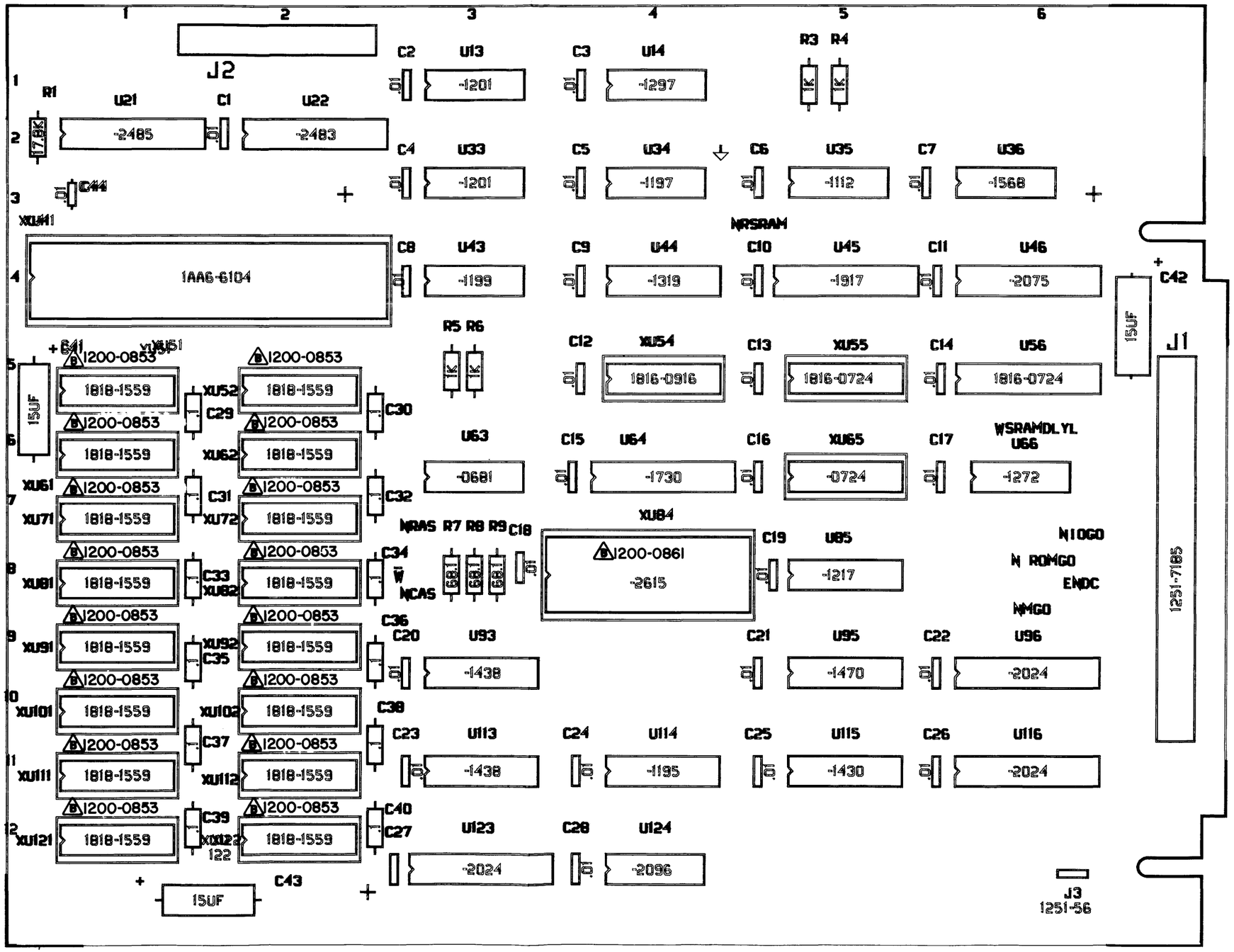
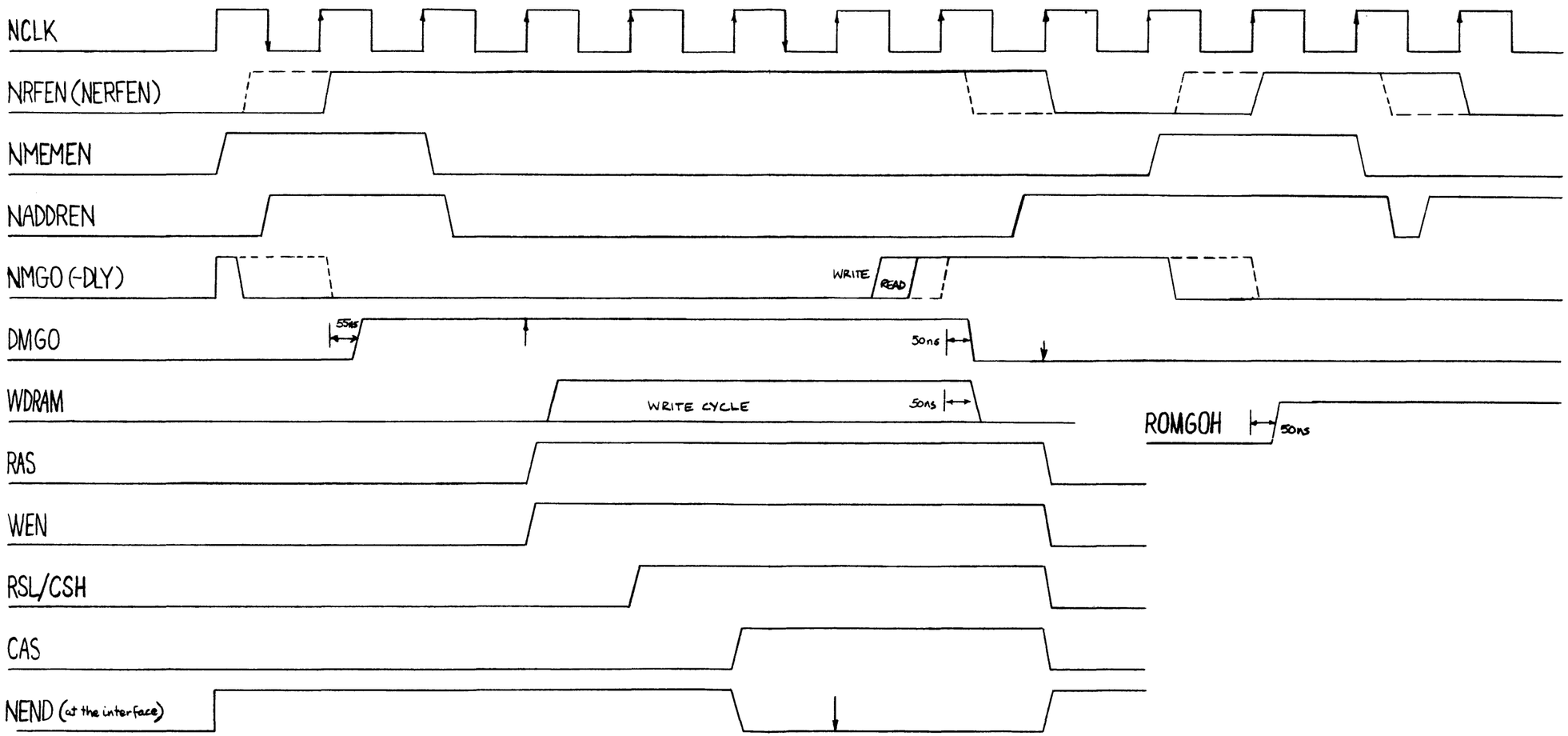
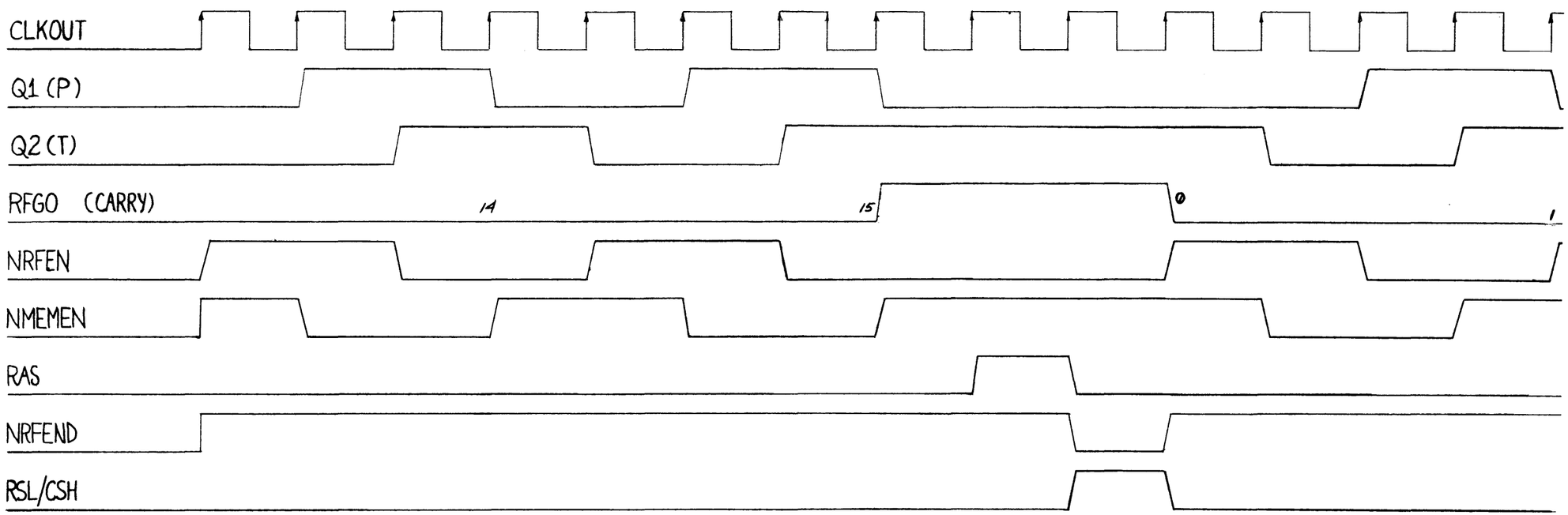


FIGURE 3
MEMORY EXTENDER COMPONENT LOCATION DIAGRAM
DEC-08-81 13220-91175



NOTE: THE SECOND ASSERTION OF MGOL IS NOT FOLLOWED BY THE ASSERTION OF DMGOH. THIS INDICATES A ROM TRANSACTION.

FIGURE 4
MEMORY EXT DYNAMIC RAM TIMING DIAGRAM
DEC-08-81 13220-91175



NOTE: RFENL AND MEMENL DETERMINE WHICH STATE MACHINE INPUT HAS PRIORITY AS SHOWN BELOW

	RFENL	MEMENL	WINITL
ENDINITH*	0	0	0
CONFIG	0	0	1
RFGO	0	1	1
CONFIG	1	1	1
DMGC	1	0	1

* NOT SHOWN FOR REFRESH CYCLE.

FIGURE 5
MEMORY EXT REFRESH CYCLE TIMING DIAGRAM
DEC-08-81 13220-91175

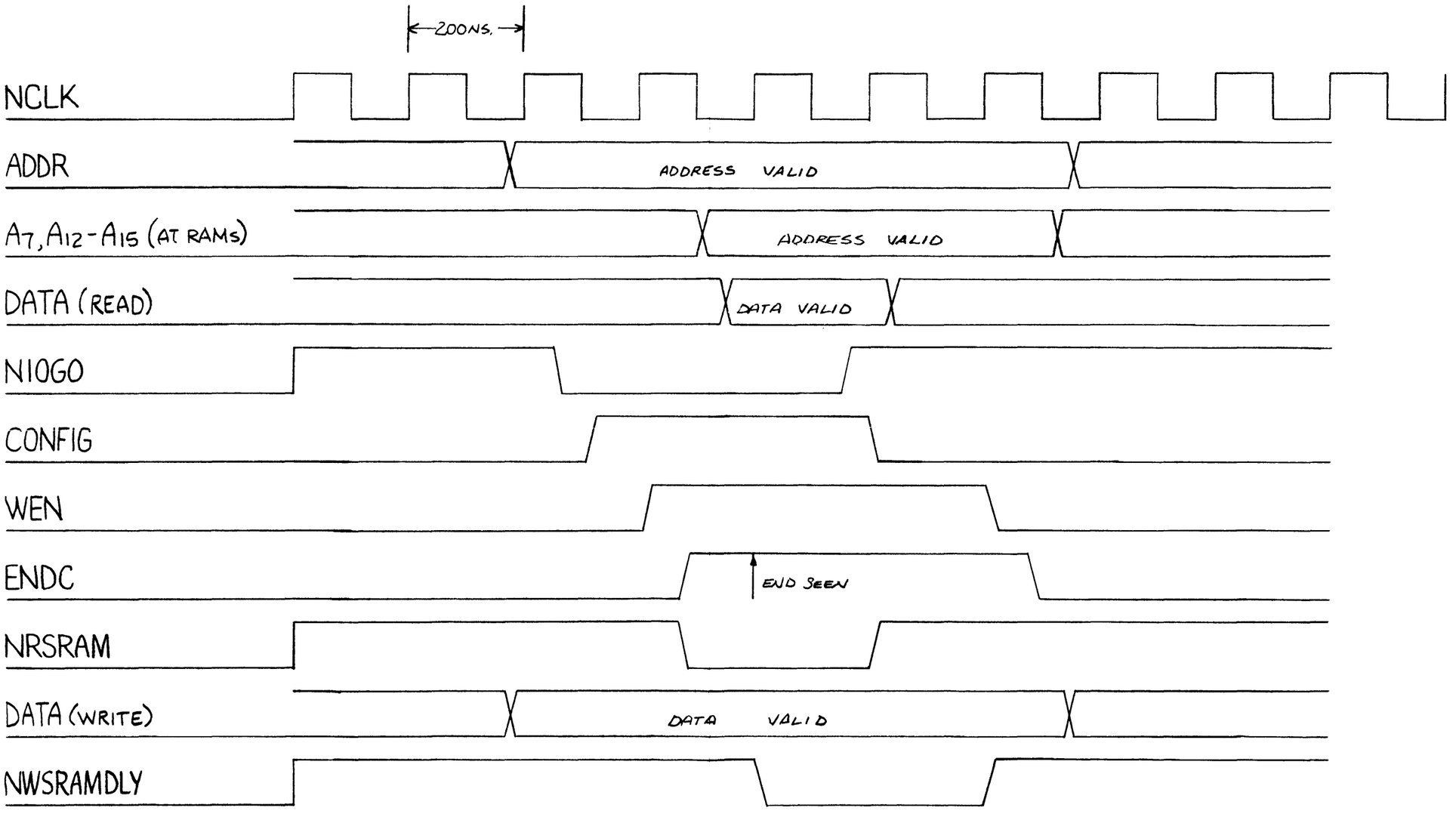
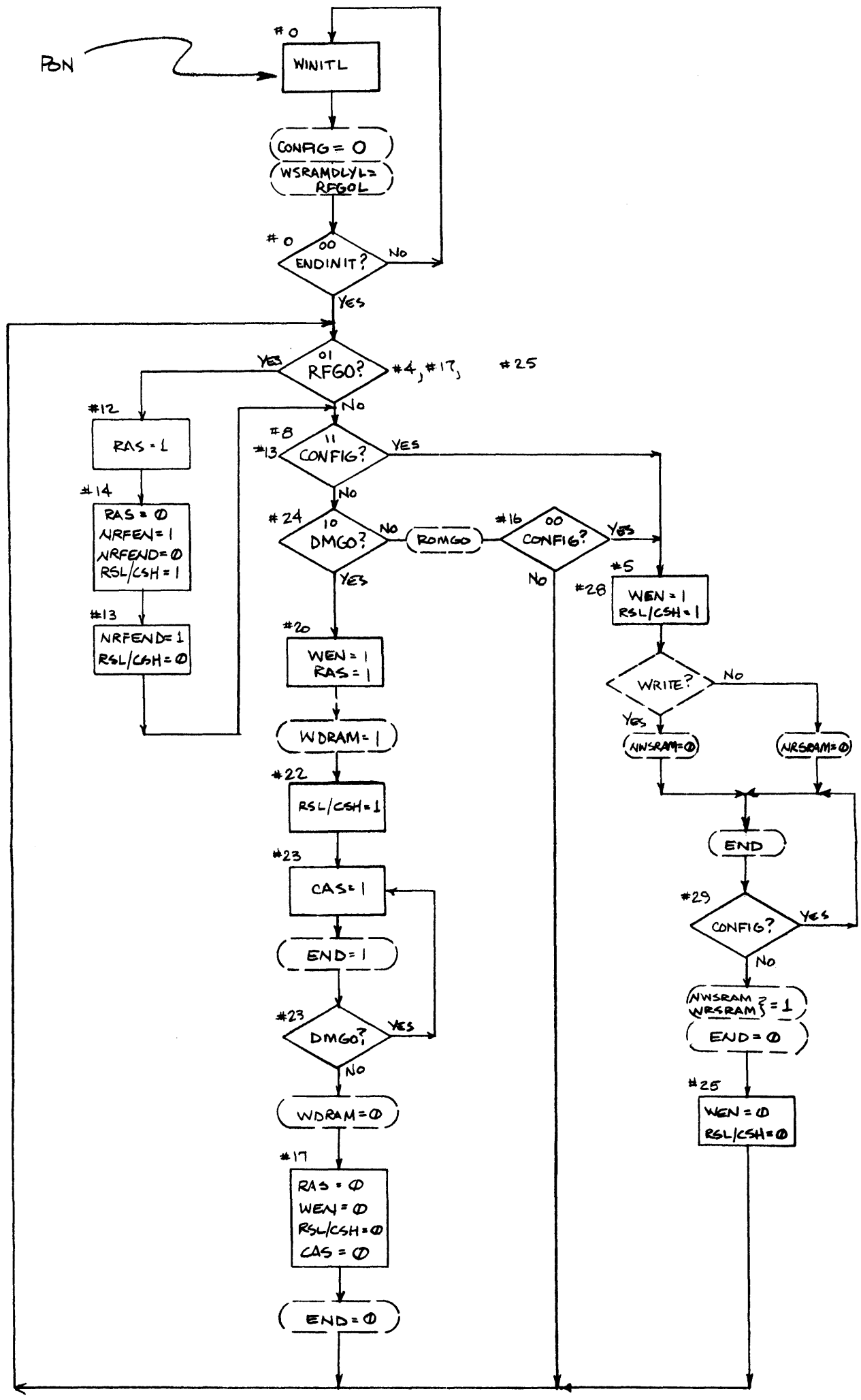


FIGURE 6
MEMORY EXT CONFIGURATION RAM TIMING DIAGRAM
DEC-08-81 13220-91175



2626W MEMORY EXTENDER STATE MACHINE

( ) THIS SYMBOL INDICATES AN FPLA OUTPUT.

FIGURE 7
MEMORY EXT STATE MACHINE FLOW CHART
DEC-08-81 13220-91175

A_4	A_3	A_2	A_1	A_0		NRFEN	NMEMEN	CONDITIONAL INPUT	RAS	RSL/CSH	RSL/CSH (MSB)	RAS	CAS	NRFEND	WEN	NWINIT	NMEMEN	NRFEN	NEXT ADDRESS	YES	NO	COMMENTS
0	0	0	0	0	INIT						0	0	0	0	0	0	0	0	0000	4	0	0
0	0	0	0	1							0	0	0	1	0	1	1	0	0100	12	8	1 RFGO?
0	0	0	1	0							0	0	0	0	0	0	0	0	0000			2
0	0	0	1	1							0	0	0	0	0	0	0	0	0000			3
0	0	1	0	0							0	0	0	1	0	1	1	0	0100	12	8	4 RFGO?
0	0	1	0	1							1	0	0	1	0	1	1	1	1101			5 YES CONFIG, GOTO 29
0	0	1	1	0							0	0	0	0	0	0	0	0	0000			6
0	0	1	1	1							0	0	0	0	0	0	0	0	0000			7
0	1	0	0	0	RFGO						0	0	0	1	0	1	1	1	1100	28	24	8 NO RFGO. CONFIG?
0	1	0	0	1							0	0	0	1	0	1	1	0	0100	12	8	9 RFGO?
0	1	0	1	0							1	0	0	1	0	1	1	0	0101			10 DEASSERT RAS, NRFEND RSL/CSH. GOTO 9
0	1	0	1	1							0	0	0	0	0	0	0	0	0000			11
0	1	1	0	0							0	1	0	1	0	1	1	0	0110			12 YES RFGO. RAS. GOTO 14
0	1	1	0	1							0	0	0	1	0	1	1	1	1100	28	24	13 NRFEN. CONFIG?.
0	1	1	1	0							1	0	0	0	0	1	1	0	0101			14 DEASSERT RAS, NRFEND, RSL/CSH, GOTO 13
0	1	1	1	1							0	0	0	0	0	0	0	0	0000			15
1	0	0	0	0	DMGO						1	0	0	1	0	1	0	0	0001	5	1	16 NO DMGO. CONFIG?
1	0	0	0	1							0	0	0	1	0	1	1	0	0100	12	8	17 RFGO?
1	0	0	1	0							0	0	0	0	0	0	0	0	0000			18
1	0	0	1	1							1	0	0	1	0	1	0	0	0001			19 GOTO 1
1	0	1	0	0							0	1	0	1	1	1	0	1	1010			20 YES DMGO. WEN. RAS GOTO 22
1	0	1	0	1							1	0	0	1	1	1	0	1	1001			21 DEASSERT CAS. GOTO 17
1	0	1	1	0							1	1	0	1	1	1	0	1	1011			22 RSL/CSH. GOTO 23
1	0	1	1	1							1	1	1	1	1	1	0	1	1011			23 CAS. GOTO 19
1	1	0	0	0	CONFIG						0	0	0	1	0	1	0	1	1000	16		24 NO CONFG. DMGO?
1	1	0	0	1							0	0	0	1	0	1	1	0	0100	12	8	25 RFGO?
1	1	0	1	0							0	0	0	0	0	0	0	0	0000			26
1	1	0	1	1							0	0	0	0	0	0	0	0	0000			27
1	1	1	0	0							1	0	0	1	1	1	1	1	1101			28 YES CONFG. GOTO 29
1	1	1	0	1							0	0	0	1	1	1	1	1	1100			29 GOTO 24
1	1	1	1	0							0	0	0	0	0	0	0	0	0000			30
1	1	1	1	1							0	0	0	0	0	0	0	0	0000			31

PROM IS HP PART NO. 1816-1503

FIGURE 7
MEMORY EXT STATE MACHINE FLOW CHART
DEC-08-81 13220-91175

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As issued	3-9-81	DH

Model No.		Stock No.	1820-2615
Title	SPECIFICATION CONTROL DRAWING		
Description	IC- Programmable Logic Array	Date	3-9-81
By	Susan Hayase	Sheet No.	1 of 5
Supersedes		Drawing No.	A-1820-2615-1

1. GENERAL:

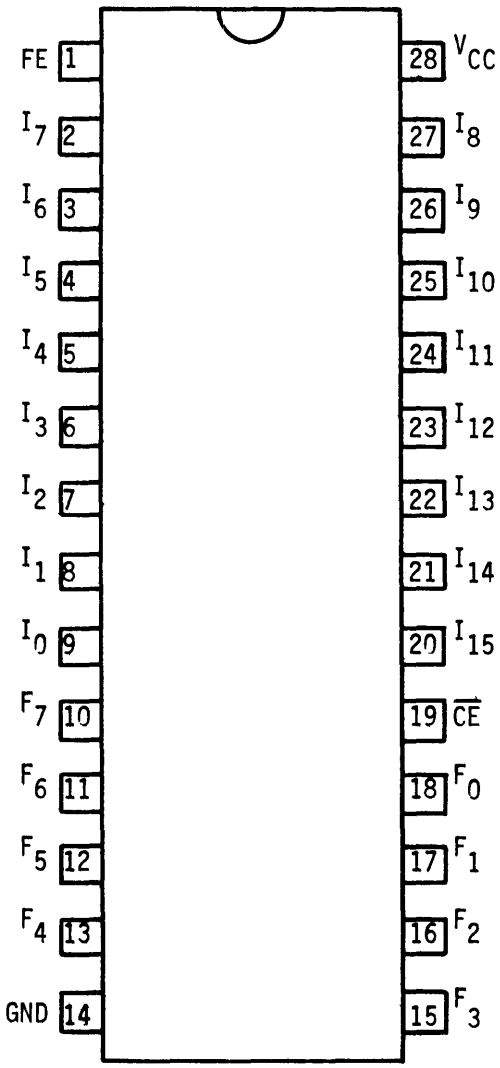
This document contains specifications for a TTL-compatible bipolar Logic Array intergrated ciruit with tri-state outputs. This part can be made from a Signetics 82S100 Field Programmable Logic Array.

2. MECHANICAL:

The device shall be packaged in a 28-pin dual-in-line package with the connections shown figure 1. The package shall be marked with the manufacturer's name or symbol, date code and the HP part number (1820-2615). Marking shall be legible and shall withstand a dish-washer cycle using Calgonite or equivalent.

				MODEL	STK. NO. 1820-2615
				IC-PROGRAMMABLE LOGIC ARRAY	
				BY SUSAN HAYASE	DATE 3-9-81
LTR	P.C. NO.	APPROVED	DATE	APPD.	SHEET NO. 2 OF 5
PPP0360S	REVISIONS			SUPERSEDES	DWG. NO. A-1820-2615-1

HEWLETT-PACKARD CO.



LTR	P.C. NO.	APPROVED	DATE
	REVISIONS		

MODEL	STK. NO. 1820-2615
Programmable Logic Array	
BY Jim Hunt	DATE 3-31-81
APPD.	SHEET NO. 3 OF 5
SUPERSEDES	DWG. NO. A-1820-2615-1

3. ELECTRICAL:

The Logic Array circuit is bipolar TTL with tri-state outputs. The third state (outputs OFF) is enabled when pin 19 ($\overline{CE}$) is high. Electrical and switching characteristics for this device are per Signetics 82S100 as specified in Signetics Bipolar & MOS Memory Data Manual, 1980.

Supply Voltage	5 volts ± 5%
Operating Temperature Range	0 deg C to +70 deg C.

4. TRUTH TABLE:

The state of an output pin is a function of its associated output function within the logic array and the state of $\overline{CE}$ pin.

$\overline{CE}$	OUTPUT FUNCTION	OUTPUT PIN
Low	True	High
Low	False	Low
High	Don't Care	Off

An output functions is TRUE if and only if at least one of its product terms is TRUE. Product terms belonging to the output function are identified by the presence of an "A" in the output function half of the accompanying Program Table.

A product term is True if and only if the state of each input pin matches the value specified in the product term half of the program Table.

				MODEL	STK. NO. 1820-2615
				IC-PROGRAMMABLE LOGIC ARRAY	
				BY SUSAN HAYASE	DATE 3-9-81
LTR	P.C. NO.	APPROVED	DATE	APPD.	SHEET NO. 4 OF 5
PPP0360S	REVISIONS			SUPERSEDES	DWG. NO. A-1820-2615-1

HEWLETT-PACKARD CO.

16X48X8 FPLA PROGRAM TABLE

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	$\overline{Im}$	Don't Care	Prod. Term Present in F_P	Prod. Term Not Present in F_P	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L
NOTE Enter (—) for unused inputs of used P-terms.			NOTES 1. Entries independent of output polarity. 2. Enter (A) for unused outputs of used P-terms.		NOTES 1. Polarity programmed once only. 2. Enter (H) for all unused outputs.	

PRODUCT TERM[1]																ACTIVE LEVEL[1]							
	INPUT VARIABLE[1]															H	H	L	H	L	L	L	H	L
NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OUTPUT FUNCTION[1]							
																	7	6	5	4	3	2	1	0
0	L	H	-	-	-	-	-	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	-	A
1	-	H	H	L	-	-	-	-	-	-	-	-	-	H	L	-	-	-	-	-	-	-	A	-
2	H	H	H	-	L	-	-	-	-	-	-	-	H	-	H	L	-	-	-	-	-	-	A	-
3	L	H	H	-	L	-	-	-	-	-	-	-	L	-	H	L	-	-	-	-	-	-	A	-
4	-	H	H	-	-	-	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A	-
5	-	H	H	L	L	-	-	L	-	-	-	-	-	H	L	-	-	-	-	-	-	A	-	-
6	-	H	-	-	H	H	-	-	-	-	-	H	-	-	-	L	-	-	-	-	A	-	-	-
7	-	H	-	-	L	H	-	-	-	-	H	-	-	-	-	L	-	-	-	-	A	-	-	-
8	-	H	-	-	-	L	-	-	-	-	-	-	-	-	-	L	-	-	-	-	A	-	-	-
9	-	-	H	-	H	H	-	-	-	-	-	L	-	L	-	L	-	-	-	A	-	-	-	-
10	-	H	H	L	H	-	-	-	L	-	-	-	-	H	L	-	-	-	A	-	-	-	-	-
11	-	L	H	-	-	-	-	-	H	-	-	-	-	-	-	-	-	-	A	-	-	-	-	-
12	-	H	-	L	-	-	-	-	-	-	-	-	-	H	L	-	-	A	-	-	-	-	-	-
13	-	-	-	-	L	H	-	-	-	L	-	-	L	-	-	L	A	-	-	-	-	-	-	-
14	-	-	-	-	H	H	-	-	-	L	-	-	L	-	-	L	A	-	-	-	-	-	-	-
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LTR	P C NO	APPROVED	DATE
	REVISIONS		

BY S. Hayase	DATE 3-9-81
APPD.	SHEET NO 5 OF 5
SUPERSEDES	DWG NO A-1820-2615-1

9320-3767

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02620-60175	6	1	MEMORY EXTENDER DATE CODE: B-2120-42	28480	02620-60175
C2	0160-4554	7	27	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C4	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C5	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C12	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C22	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C23	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C24	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C25	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C26	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C27	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C28	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C29	0160-4557	0	12	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C30	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C31	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C32	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C33	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C34	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C35	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C36	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C37	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C38	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C39	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C40	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C41	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C43	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
R3	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R6	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R7	0757-0397	3	3	RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
R8	0757-0397	3		RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
R9	0757-0397	3		RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
U13	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U14	1820-1297	0	1	IC GATE TTL LS EXCL-NOR QUAD 2-INP	01295	SN74LS266N
U33	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U34	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U35	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U36	1820-1568	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U43	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U44	1820-1319	7	1	IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S151N
U45	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U46	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U51	5180-0133	7	16	IC-64K RAM 200NS	28480	5180-0133
U52	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U54	1816-1503	2	1	IC-ROM 32 X 8	01295	TBP18S030N PROGRAMMED
U55	1816-0724	7	2	IC TTL S 64-BIT STAT RAM 35-NS 3-S	01295	SN74S189N
U56	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U61	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U62	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U63	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U64	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U65	1816-0724	7		IC TTL S 64-BIT STAT RAM 35-NS 3-S	01295	SN74S189N

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U66	1820-1272	1	1	IC BFR TTL LS NOR QUAD 2-INP	01295	SN74LS33N
U71	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U72	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U81	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U82	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U84	1820-2615	8	1	IC MISC TTL S	18324	82S100N PROGRAMMED
U85	1820-1217	4	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS151N
U91	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U92	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U93	1820-1438	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U95	1820-1470	1	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U96	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U101	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U102	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U111	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U112	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U113	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U114	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U115	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U116	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U121	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U122	5180-0133	7		IC-64K RAM 200NS	28480	5180-0133
U123	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U124	1820-2096	9	1	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
XU51	1200-0853	8	17	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU52	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU54	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU61	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU62	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU71	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU72	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU81	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU82	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU84	1200-0861	8	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0861
XU91	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU92	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU101	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU102	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU111	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU112	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU121	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU122	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
				MISCELLANEOUS		
	0360-1682	0	10	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
	1251-5613	5	1	TERMINAL-PCB TAB	28480	1251-5613
	1251-7185	0	1	CONNECTOR 50-PIN M POST TYPE	28480	1251-7185
	02620-80175	8	1	ETCHED BOARD	28480	02620-80175

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
S0545	NIPPON ELECTRIC CO	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
03508	GE CO SEMICONDUCTOR PROD DEPT	AUBURN	NY	13201
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11961	SEMICON INC	BURLINGTON	MA	01803
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH	NC	27604
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34371	HARRIS SEMICON DIV HARRIS-INTERTYPE	MELBOURNE	FL	32901
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247