HP 13255

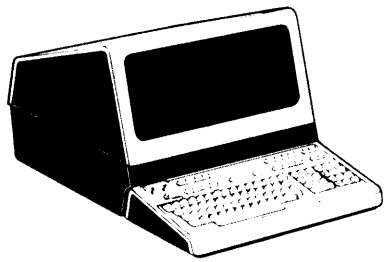
EXTENDED KEYBOARD INTERFACE MODULE

Manual Part No. 13255-91123

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Extended Keyboard Interface Module replaces the standard Keyboard Interface PCA (02640-60019) described in module section 13255-91018. The Product/Module Cross-Reference Table indicates the products in which the replacement is applicable. Parts lists for 02640-60018, 02640-60041, and 02640-60081 are contained in module section 13255-91018.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Extended Keyboard Interface Module is contained in tables 1.0 through 6.7.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60018	Keyboard PCA	16.8 x 7.1 x 2.1	2.75
02640-60041	Speaker Cable Assembly	N/A	N/A
02640-60081	Keyboard Cable Assembly	N/A	N/A
02640-60123	Keyboard Interface PCA	12.9 x 4.0 x 0.5	0.38

Number of Backplane Slots Required: 1

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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02640-60123	Keyboard Interface PCA	12.9 x 4.0 x 0.5	0.38

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 0.629 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
@ 600 mA	@ 100 mA	@ 80 mA	@ mA
			NOT APPLICABLE
115 volts ac		220 volts ac	
@ A		@ A	
NOT APPLICABLE		NOT APPLICABLE	
Clock Frequency: 4.915 MHz			

Table 4.0 Switch Definitions

PCA Designation	Function	
	In	Out
Switch A B C D E F G H J K L M N P Q R S T U V W X Y Z	Data Bit = 0	Data Bit = 1
	The switches are located on the Extended Keyboard Interface PCA and are read by firmware to determine the operating mode of the terminal. (Refer to tables 6.0, 6.1, and 6.2 for accessing these bits.)	

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
- 2	GND	Ground Common Return (Power and Signal)
- 3	SYS CLOCK	4.915 MHz System Clock
- 4	-12V	-12 Volt Power Supply
- 5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
- 6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
- 7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
- 8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
- 9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11		Not Used
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13		Not Used
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17		Not Used
-18		Not Used
-19		Not Used
-20		Not Used
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector Pin Number	Signal Name	Signal
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not Used
-S		
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W	$\overline{\text{BUSY}}$	Negative True, Bus Currently Busy (Controlling Bus)
-X		Not Used
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not Used

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	+5V	+5 Volt Power Supply
- 2	$\overline{\text{BBUS0}}$	Negative True, Buffered Data Bus Bit 0
- 3	$\overline{\text{BBUS1}}$	Negative True, Buffered Data Bus Bit 1
- 4	$\overline{\text{BBUS2}}$	Negative True, Buffered Data Bus Bit 2
- 5	$\overline{\text{BBUS3}}$	Negative True, Buffered Data Bus Bit 3
- 6	$\overline{\text{BBUS4}}$	Negative True, Buffered Data Bus Bit 4
- 7	$\overline{\text{BBUS5}}$	Negative True, Buffered Data Bus Bit 5
- 8	$\overline{\text{BBUS6}}$	Negative True, Buffered Data Bus Bit 6
- 9	$\overline{\text{BBUS7}}$	Negative True, Buffered Data Bus Bit 7
-10	BADDR0	Positive True, Column Address Bit 0
-11	BADDR1	Positive True, Column Address Bit 1
-12	BADDR2	Positive True, Column Address Bit 2
-13	BADDR3	Positive True, Column Address Bit 3
-14	$\overline{\text{READ . COL15}}$	Negative True. Enables Reading Columns 0-13. Not Asserted for Columns 14 & 15
-15	COM	Common Return

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	COM	Common Return
-B	BEEP	Triggers Beeper Circuit
-C	-12V	-12 Volt Power Supply
-D	CHASSIS GND	Grounds the Switchplate
-E		Not Used
-F		
-H		
-J	COL OUT EN	Strobes Column's Previous State Into Input Register
-K	LED EN	Strobes Data Into LED Latches
-L		Not Used
-M	PwR ON	Resets the Terminal
-N	+5V	+5 Volt Power Supply
-P		Not Used
-R		
-S	+12V	+12 Volt Power Supply

Table 6.0 Module Bus Pin Assignments

Function Performed: Read Switches A through H on Extended Keyboard Interface PCA

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0011)

Function Specifier: ADDR 0,1,2,3, = (0111)
ADDR 7 = 0

Data Bus Bit Interpretation:

B7
When set to 1, Switch H is open

B6
When set to 1, Switch G is open

B5
When set to 1, Switch F is open

B4
When set to 1, Switch E is open

B3
When set to 1, Switch D is open

B2
When set to 1, Switch C is open

B1
When set to 1, Switch B is open

B0
When set to 1, Switch A is open

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
X	ADDR 5
1	ADDR 4
1	ADDR 3
1	ADDR 2
1	ADDR 1
0	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.1 Module Bus Pin Assignments

Function Performed: Read Switches J through R on Extended Keyboard Interface PCA	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (0011)	X	ADDR 12
	0	ADDR 11
	0	ADDR 10
	1	ADDR 9
Function Specifier: ADDR 5 = 0	X	ADDR 8
ADDR 7 = 1	1	ADDR 7
	X	ADDR 6
	0	ADDR 5
	1	ADDR 4
	X	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation:	X	ADDR 1
	X	ADDR 0
B7		
When set to 1, Switch R is open	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
B6	B4	BUS 4
When set to 1, Switch Q is open	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B5	B0	BUS 0
When set to 1, Switch P is open		
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B4	X=Don't Care	
When set to 1, Switch N is open		
B3		
When set to 1, Switch M is open		
B2		
When set to 1, Switch L is open		
B1		
When set to 1, Switch K is open		
B0		
When set to 1, Switch J is open		

Table 6.2 Module Bus Pin Assignments

Function Performed: Read Switches S through Z on Extended Keyboard Interface PCA	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (0011)	X	ADDR 12
	0	ADDR 11
	0	ADDR 10
	1	ADDR 9
Function Specifier: ADDR 7 = 1	X	ADDR 8
ADDR 5 = 1	1	ADDR 7
	X	ADDR 6
	1	ADDR 5
	1	ADDR 4
	X	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation:	X	ADDR 1
	X	ADDR 0
B7	B7	BUS 7
When set to 1, Switch Z is open	B6	BUS 6
	B5	BUS 5
B6	B4	BUS 4
When set to 1, Switch Y is open	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
B5	B0	BUS 0
When set to 1, Switch X is open	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B4	X=Don't Care	
When set to 1, Switch W is open		
B3		
When set to 1, Switch V is open		
B2		
When set to 1, Switch U is open		
B1		
When set to 1, Switch T is open		
B0		
When set to 1, Switch S is open		

Table 6.3 Module Bus Pin Assignments

Function Performed: Read data comm switches on Keyboard PCA (Refer to figure 1 in module section 13255-91018 for physical location of data comm switches and their positions.)

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0011)

Function Specifier: ADDR 0,1,2,3 = (1111)
ADDR 7 = 0

Data Bus Bit Interpretation:

Switch 1

Position	0	1
B7	1	0

B6 Not assigned, always 0

Switch 2

Position	0	1	2
B5	0	0	1
B4	0	1	0

Switch 3

Position	0	1	2	3	4	5	6	7
B3	0	0	0	0	1	1	1	1
B2	0	0	1	1	0	0	1	1
B1	0	1	0	1	0	1	0	1

B0 Not assigned, always 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
X	ADDR 5
1	ADDR 4
1	ADDR 3
1	ADDR 2
1	ADDR 1
1	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.4 Module Bus Pin Assignments

Function Performed: Output a column's previous state into the Keyboard PCA's input register

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0011)

Function Specifier: ADDR 5 = 1
ADDR 7 = 0

Data Bus Bit Interpretation: Each data bit is associated with a switch in a column. If the bit is set to 1, it indicates that the switch was previously depressed. The column to which the value is applied is specified by a subsequent switch read as indicated in table 6.5.

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.5 Module Bus Pin Assignments

Function Performed: Read switches in column "n" as determined by A3, A2, A1, and A0

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0011)

Function Specifier: ADDR 0,1,2,3 are used to specify which keyboard column is to be read. The column number specified by these bits must be less than 14 (decimal). ADDR 7 = 0

Data Bus Bit Interpretation: Each data bit is associated with a switch in a column. If the switch is depressed, the data bit is 1. (Refer to figure 1 of module section 13255-91018 for a cross-reference of key numbers to the physical switches on the keyboard.)

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
X	ADDR 5
1	ADDR 4
A3	ADDR 3
A2	ADDR 2
A1	ADDR 1
A0	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Column Address				DATA BUS BIT							
A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	007	006	005	004	003	002	001	000
0	0	0	1	017	016	015	014	013	012	011	010
0	0	1	0	027	026	025	024	023	022	021	020
0	0	1	1	037	036	035	034	033	032	031	030
0	1	0	0	047	046	045	044	043	042	041	040
0	1	0	1	057	056	055	054	053	052	051	050
0	1	1	0	067	066	065	064	063	062	061	-
0	1	1	1	077	076	075	074	073	072	071	070
1	0	0	0	107	106	105	104	103	102	101	100
1	0	0	1	117	116	115	114	113	112	111	110
1	0	1	0	127	126	125	124	123	122	121	120
1	0	1	1	137	136	-	134	133	132	131	130
1	1	0	0	147	-	-	144	-	142	141	140
1	1	0	1	157	-	-	154	-	152	151	150

Table 6.6 Module Bus Pin Assignments

Function Performed: Write LED latch and trigger alarm generator (Beep)

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0011)

Function Specifier: ADDR 5 = 0
ADDR 7 = 0

Data Bus Bit Interpretation:

B7
when Set, Beeper is triggered

B6
when Set, LED #7 is turned on

B5
when Set, LED #6 is turned on

B4
when Set, LED #5 is turned on

B3
when Set, LED #4 is turned on

B2
when Set, LED #3 is turned on

B1
when Set, LED #2 is turned on

B0
when Set, LED #1 is turned on

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.7 Module Bus Pin Assignments

Function Performed: Output Reset key control

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0011)

Function Specifier: ADDR 7 = 1

Data Bus Bit Interpretation:

B7 Not Used

B6 Not Used

B5 Not Used

B4 Not Used

B3 Not Used

B2 when set to 1, the RESET TERMINAL key is "disabled, preventing" hardware reset of the terminal

B1 when set to 1, the RESET TERMINAL key is "enabled, allowing" hardware reset of the terminal

B0 Not Used

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
1	ADDR 7
X	ADDR 6
X	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagram (figure 3), component location diagram (figure 4), and parts list 02640-60123 located in the appendix.

As shown in the block diagram, the Extended Keyboard Interface Module consists of address decoding logic, option switches, beep generator, reset enable/disable, and bus synchronization circuits. (Refer also to module section 13255-91018 for discussion of the Keyboard PCA).

3.1 ADDRESS DECODING LOGIC.

3.1.1 This logic decodes the bus address lines to recognize selection of the Extended Keyboard Interface Module as determined by $\overline{\text{ADDR4}}$, $\overline{\text{ADDR9}}$, $\overline{\text{ADDR10}}$, and $\overline{\text{ADDR11}}$.

3.1.2 $\overline{\text{REQ}}$ serves as a strobe to initiate action only when the address and data lines on the bus are valid, thus avoiding false module selection as bus addresses are changing.

The $\overline{\text{WRITE}}$ signal is combined with $\overline{\text{REQ}}$, $\overline{\text{I/O}}$, and MODULE SELECTED to generate DATA IN ENABLE and WRITE on output to the keyboard, and DATA OUT ENABLE and READ on input from the keyboard.

3.1.2.1 During a read, if $\overline{\text{ADDR7}}$ is "1", $\overline{\text{ADDR0}}$ through $\overline{\text{ADDR4}}$ determine which column of the key switch matrix is to be read. Special logic determines if column 16 (octal) is being read and gates Switches A through H onto the bus. Special logic is also necessary to detect a column in the range 0 to 15 (octal) in order to trigger the ramp generator and other circuitry on the Keyboard PCA by lowering $\overline{\text{RD}} \cdot \overline{\text{COL15}}$. If $\overline{\text{ADDR7}}$ is "0" then $\overline{\text{ADDR5}}$ determines whether to read switch group J through R or S through Z.

3.1.2.2 During writes, $\overline{\text{ADDR5}}$ and $\overline{\text{ADDR7}}$ are used to decode LED EN, COL OUT EN, or MODE SELECT. LED EN causes $\overline{\text{BUS0}}$ through $\overline{\text{BUS6}}$ to be latched into a register on the keyboard, lighting the LEDs. $\overline{\text{BUS7}}$ low combined with LED ON produces BEEP TRIGGER to set off the beep generator. COL OUT EN is a command to the keyboard to use the bus data to provide hysteresis for key depression. MODE SELECT high and $\overline{\text{ADDR7}}$ low select the reset enable/disable function which is controlled by $\overline{\text{BUS1}}$ and $\overline{\text{BUS2}}$.

3.2 OPTION SWITCHES. Twenty-four option Switches (A through H, J through R, and S through Z) are located on the Keyboard Interface PCA. When open, they are at logic 1 and when closed are at logic 0. Their data is gated onto the data bus by a signal from the address decoding logic.

3.3 BEEP GENERATOR. The generator is a dual-timer, the first of which is a monostable generating a 100-millisecond pulse. The second timer is an astable with a free running frequency of 650 hertz, and is enabled by the pulse from the first timer. The astable drives a speaker on the Keyboard PCA through a current limiting resistor.

3.4 RESET ENABLE/DISABLE. The firmware synchronizes itself with the $\overline{\text{RESET}}$ line by disabling and enabling the reset function before and after critical sections of code. This is done when $\overline{\text{ADDR7}}$ is "1" (on a write) and $\overline{\text{BUS1}}$ is "1" (enable reset) or $\overline{\text{BUS2}}$ is "1" (disable reset).

3.5 BUS SYNCHRONIZATION. The PWR ON signal is synchronized with the bus so that it is only asserted at the end of a bus cycle when the bus is available. A monostable ensures complete system reset by holding PWR ON low for 40 microseconds.

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60123	1	EXTENDED KEYBOARD INTERFACE ASSEMBLY DATE CODE: D-1636-42 REVISION DATE: 11-13-76	28480	02640-60123
C1	0180-0393	2	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0160-2055	12	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C3	0150-0121	1	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C4	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C5	0160-0161	1	CAPACITOR-FXD .01UF +-10% 200WVDC POLYE	56289	292P10392
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1901-0050	1	DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
E1	0360-0124	1	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
J1	1251-1126	1	CONNECTOR-SGL CONT SKT .08-IN-BSC-SZ RND	74970	105-0754-001
R1	1810-0125	4	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R3	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R4	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R5	0683-1025	7	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R6	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R7	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R8	0683-1035	1	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R9	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R10	0683-4745	1	RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
R11	0683-2235	1	RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
R12	0683-1045	1	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R13	0683-4705	1	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R14	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R15	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R16	0683-1015	1	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R17	0683-1025		RESISTOR 1K 5% .25W FC TC=400/+600	01121	CB1025
S1	3101-2094	3	SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392	3	COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
S2	3101-2094		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392		COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
S3	3101-2094		SWITCH-TGL DIP ROCKER ASSEMBLY 8-1A NS	28480	3101-2094
	3131-0392		COV-RKR 0.922 IN LG; 0.422 IN W; 0.217	28480	3131-0392
U19	1820-1199	2	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U22	1820-1209	12	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U23	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U24	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U25	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U26	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U27	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U28	1820-1201	3	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U29	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U33	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U34	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U35	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U36	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U37	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U39	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U46	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U44	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U45	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U411	1820-1200	1	IC-DIGITAL SN74LS05N TTL LS HEX 1	01295	SN74LS05N
U47	1820-1215	1	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U48	1820-1422	1	IC-DIGITAL SN74LS122N TTL LS	01295	SN74LS122N
U49	1820-1821	1	IC-DIGITAL 74LS113		
U210	1820-0618	1	IC-SN7417N		SN7417N
U310	1826-0205	1	IC NE 556 TIMER	18324	NE556A
R18	0686-4715	1	RESISTOR 470 5% .5		
Q1	1854-0019	1	TRANSISTOR 2N2369 TO18		
C10	0160-2055		CAPACITOR - FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR - FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR - FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR - FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR - FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR - FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR - FXD .01UF +80-20% 100WVDC CER	28480	0160-2055

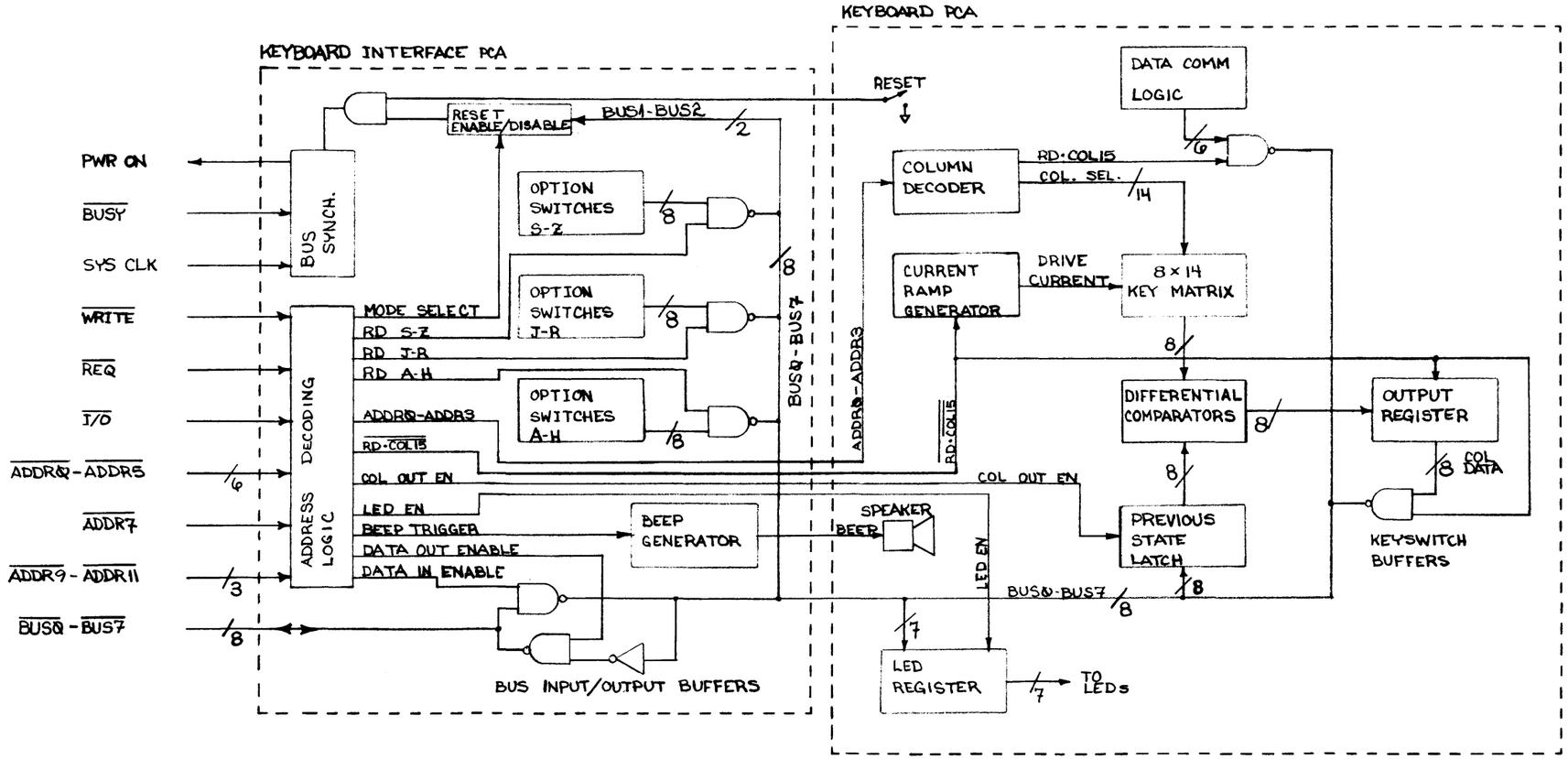

Figure 1
Extended Keyboard Interface Module Block Diagram
AUG-01-76 13255-91123

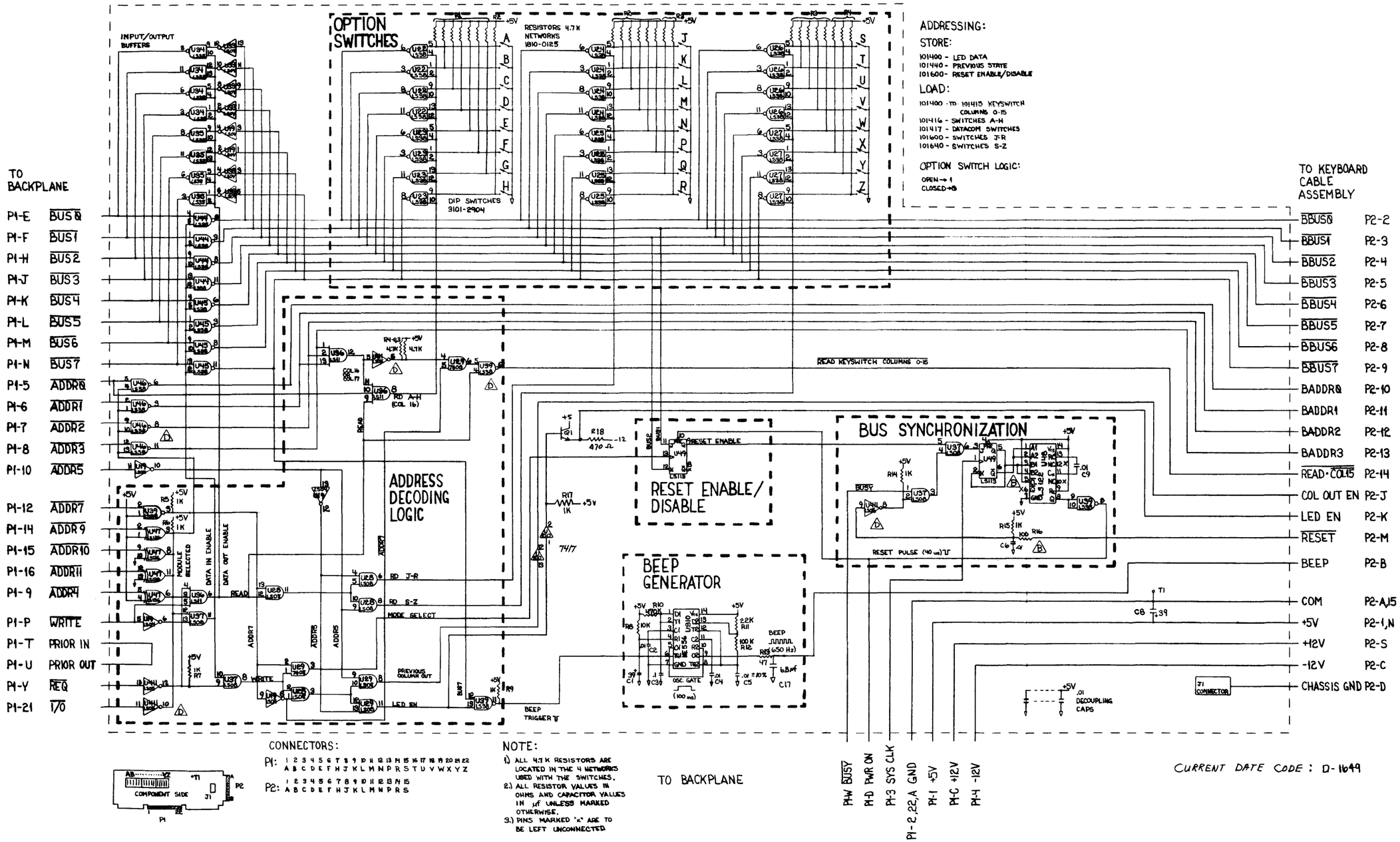

Figure 2
Keyboard Interface PCA Schematic Diagram
AUG-01-76 13255-91123

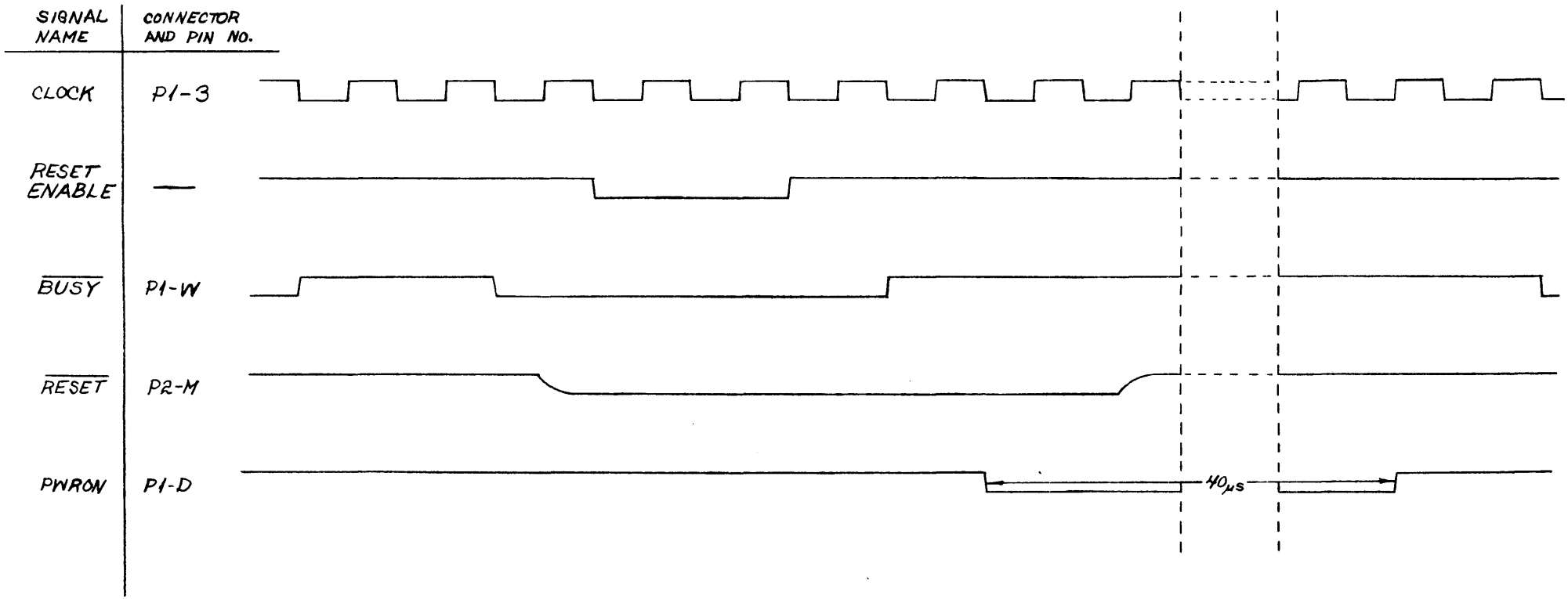

Figure 3
Reset Synchronization Timing Diagram
AUG-01-76 13255-91123

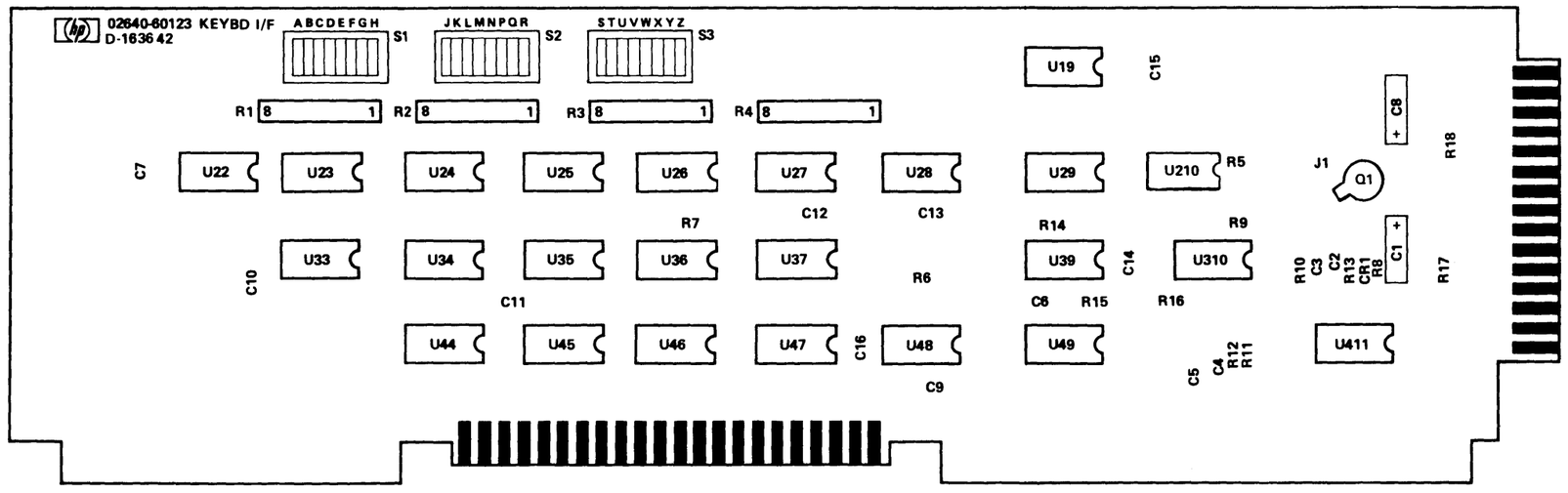

Figure 4
Keyboard Interface PCA Component Location Diagram
AUG-01-76 13255-91123

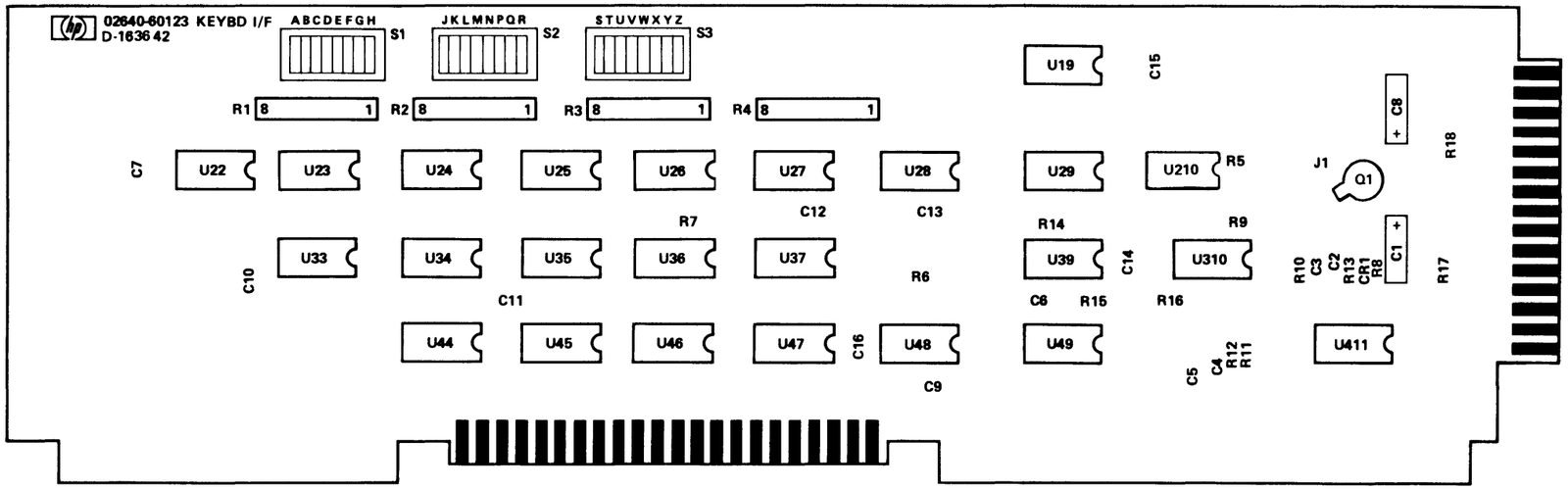

Figure 4
Keyboard Interface PCA Component Location Diagram
AUG-01-76 13255-91123