HP 13255

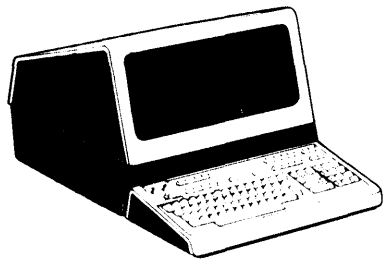
ROM (EA) MODULE

Manual Part No. 13255-91150

REVISED

APR-07-78

DATA TERMINAL
TECHNICAL INFORMATION



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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

The ROM (EA) Module contains space for up to 12K of ROM for storing the operating system firmware.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the ROM (EA) Module is contained in tables 1.0 through 5.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60150	ROM (EA) PCA	12.5 x 4.0 x 0.5	0.44

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.169 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 200 mA (With 6 ROMs loaded)	@ mA	@ 150 mA (With 6 ROMs loaded)	@ mA
	NOT APPLICABLE		NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz +/-0.1%

Table 4.0 Jumper Definitions

PCA Designation		Function In	Function Out
START ADDR		If all START ADDRESS Jumpers are IN, then START ADDR=0	
	16K	Add 0 to START ADDR	Add 16K to START ADDR
	32K	Add 0 to START ADDR	Add 32K to START ADDR
ROM ENABLE ROM	0- 2	0- 2K ROM Enabled	0- 2K ROM Disabled
	2- 4	2- 4K ROM Enabled	2- 4K ROM Disabled
	4- 6	4- 6K ROM Enabled	4- 6K ROM Disabled
	6- 8	6- 8K ROM Enabled	6- 8K ROM Disabled
	8-10	8-10K ROM Enabled	8-10K ROM Disabled
	10-12	10-12K ROM Enabled	10-12K ROM Disabled

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		
-C		Not used
-D		
-E	$\overline{BUS0}$	Negative True, Data Bus Bit 0
-F	$\overline{BUS1}$	Negative True, Data Bus Bit 1
-H	$\overline{BUS2}$	Negative True, Data Bus Bit 2
-J	$\overline{BUS3}$	Negative True, Data Bus Bit 3
-K	$\overline{BUS4}$	Negative True, Data Bus Bit 4
-L	$\overline{BUS5}$	Negative True, Data Bus Bit 5
-M	$\overline{BUS6}$	Negative True, Data Bus Bit 6
-N	$\overline{BUS7}$	Negative True, Data Bus Bit 7
-P	$\overline{WRITE}$	Negative True, Write/Read Type Cycle
-R		Not used
-S	$\overline{WAIT}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		
-W		Not used
-X		
-Y	$\overline{REQ}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not used

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagram (figure 3), component location diagram (figure 4), and parts list (02640-60150) located in the appendix.

The ROM (EA) Module has the capacity of storing from 0 to 12K bytes of firmware. As shown on the block diagram, the ROM (EA) Module consists of a ROM block, start decoder, ROM selector and jumpers, timing logic, and an output buffer.

3.1 ROM. The ROM block can contain up to six chips (EA 4900 or equivalent) with each chip containing 2K bytes. Any combination of chips can be inserted.

3.2 START DECODER. The start decoder applies a SELECT ENABLE (U410, Pin 3) to the ROM Selector and Enable Jumpers. This signal is determined by the configuration of the START ADDR Jumpers and address bits $\overline{\text{ADDR14}}$ and $\overline{\text{ADDR15}}$.

3.3 ROM SELECTOR AND ENABLE JUMPERS. The ROM selector decodes $\overline{\text{ADDR11}}$, $\overline{\text{ADDR12}}$, and $\overline{\text{ADDR13}}$ into six select signals if the SELECT ENABLE, $\overline{\text{I/O}}$, and $\overline{\text{WRITE}}$ signals are high. In order to propagate the select signals to the ROM chips, the proper ROM ENABLE Jumper must be plugged in.

3.4 TIMING LOGIC. If any 2K of ROM is selected and the proper ROM ENABLE Jumper is inserted, then the CLOCK ENABLE (U58, Pin 8) signal is generated and the timing logic is enabled. This results in $\overline{\text{WAIT}}$ and $\overline{\text{READ ADDR}}$ signals being generated and a byte from ROM is read. The

signals $\overline{REQ}$, $\overline{I/O}$, $\overline{WRITE}$ and ADDR11 through $\overline{ADDR15}$ generate the CLOCK ENABLE signal that enables the 93L1059 counter (U48). The counter advances to the states labeled in the timing diagram in figure 3 on the clock edges indicated by arrows. When $\overline{REQ}$ is asserted, $\overline{READ\ ADDR}$ and $\overline{WAIT}$ go low. State 2 of the counter and the positive half of SYS CLK terminate the $\overline{READ\ ADDR}$ signal. On the sixth clock, the counter is preset to state 8 and $\overline{WAIT}$ is terminated. By that time ROM data byte ($\overline{BUS0}$ through $\overline{BUS7}$) is valid. When $\overline{REQ}$ is dropped, CLOCK ENABLE is terminated and the output buffer is disabled.

3.5 OUTPUT BUFFER. The ouput buffer enables a ROM byte on the bus when the CLOCK ENABLE signal is generated.

4.0 ROM ORDERING INFORMATION.

4.1 VENDOR. The ROM used is Electronic Arrays' EA4900. It is a 16,384 bit static read-only-memory chip organized as 2,048 words, 8 bits per word.

4.2 SPECIFICATION. Refer to Electronic Arrays' EA 4900 specification sheet.

4.3 DATA CARD FORMATTING. Electronic Arrays' requires that the ROM data be supplied on a deck of standard 80-column computer cards. Each card is to be punched as follows: Note that for the EA4900, a 3-digit octal number is used for representing the 8 ROM outputs for each byte.

Card Column No.	Card Contents
EA 4900	
1-4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card. (This is the initial address.)
5-7	Punch a 3-digit octal number representing the outputs for the initial input address.
8-10	Punch a 3-digit octal number representing the outputs for the initial input address +1.
11-13	Punch a 3-digit octal number representing the outputs for the initial input address +2.
-	-
-	-
-	-
50-52	Punch a 3-digit octal number representing the outputs for the initial input address +15.
69-80	The unique number assigned to this ROM pattern by EA must be punched in this field enclosed by blank spaces. This number can be obtained by contacting your local EA salesman, representative, or the marketing department at the factory directly.

Each card, therefore carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The cards must be provided for all possible sequential address locations (in blocks of 16). A 2048 word ROM, therefore, requires 128 cards, with all 16 output words defined on each card.

4.4 ROM PULL-UPS. The ROM has programmable input resistors. To provide minimum high level input voltage (3.5V) at least one ROM chip must be programmed with internal pull-ups.

With regard to the sinking capability of the address driver (74LS04) only four ROM chips can have the internal input resistors.

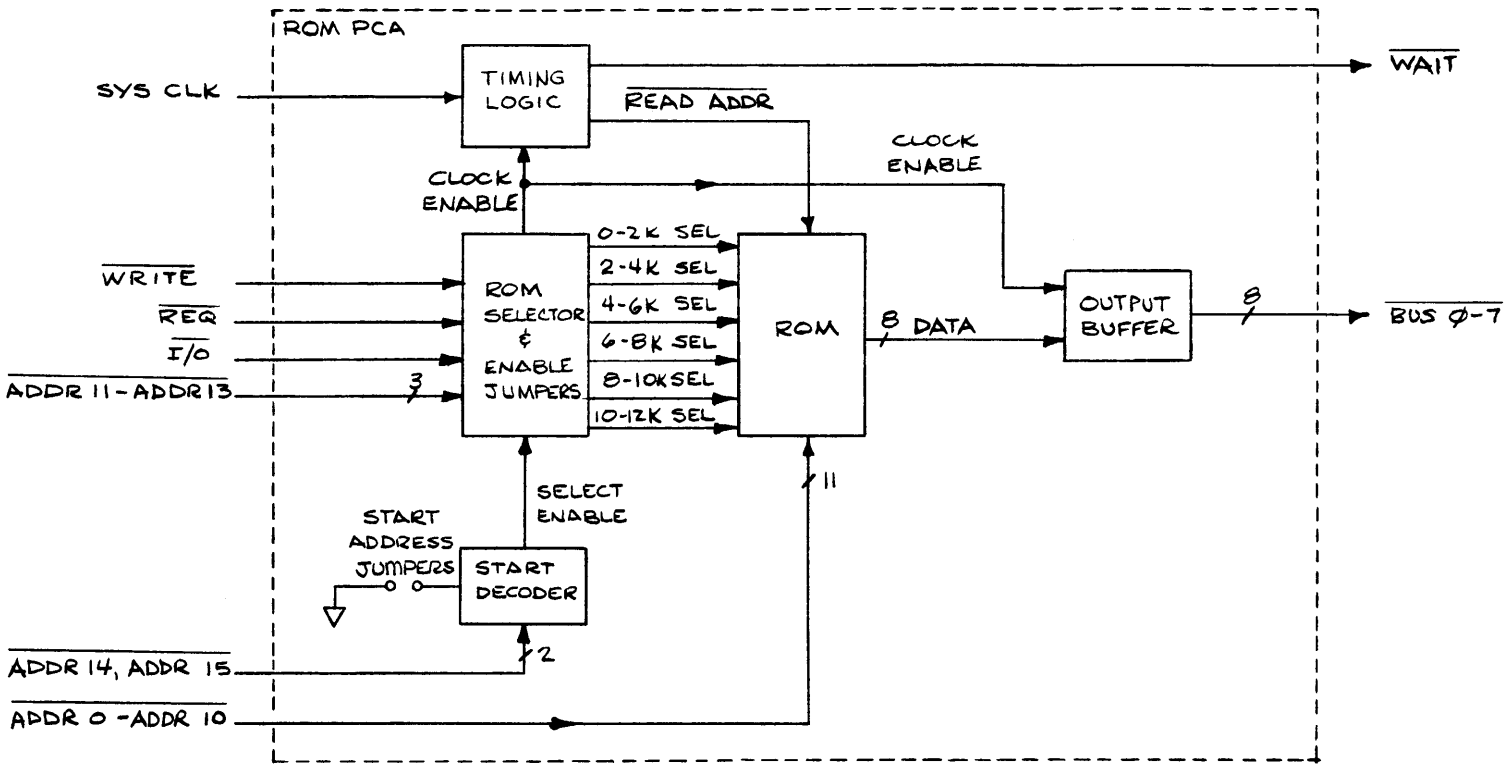

Figure 1
ROM (FA) Module Block Diagram
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BACKPLANE

TIMING LOGIC

WAIT P1-S

SYS CLK P1-3

REQ P1-Y

I/O P1-21

WRITE P1-P

PRIOR IN P1-T

PRIOR OUT P1-U

CLOCK ENABLE

READ ADDR

START DECODER

7x4.7K +5V 1810-0125

START ADDR

32K	16K	START ADDR
IN	IN	0
IN	OUT	16K
OUT	IN	32K
OUT	OUT	48K

SELECT ENABLE

ENABLE ROM

6xLS04

JUMPER	ROM
IN	ENABLED
OUT	DISABLED

ROM SELECTOR & ENABLE JUMPERS

R2 1810-125 7x4.7K +5V

R3-8 4.7k +5V

EA 4900 : PIN 1 = +5V
PIN 9 = -12V

ROM

XU21 0-2K

XU22 2-4K

XU23 4-6K

XU24 6-8K

XU25 8-10K EA 4900

XU26 10-12K

CLOCK ENABLE

OUTPUT BUFFER

8xLS38

R1 +5V 1810-0164 8x4.7K

11xLS04

C19-23 0.01

C3-8 0.1

C11-16 0.1

C2 15µF

C1 39µF

TO BACKPLANE

P1-20 P1-19 ADDR15 ADDR14

P1-18 P1-17 P1-16 ADDR13 ADDR12 ADDR11

P1-4 -12V

P1-A, 22 GND

P1-1 +5V

P1-E P1-F P1-H P1-J P1-K P1-L P1-M P1-N BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7

P1-15 P1-14 P1-13 P1-12 P1-11 P1-10 P1-9 P1-8 P1-7 P1-6 P1-5 ADDR10 ADDR9 ADDR8 ADDR7 ADDR6 ADDR5 ADDR4 ADDR3 ADDR2 ADDR1 ADDR0

P1

Figure 2
ROM (FA) PCA Schematic Diagram
APR-07-78 13255-91150

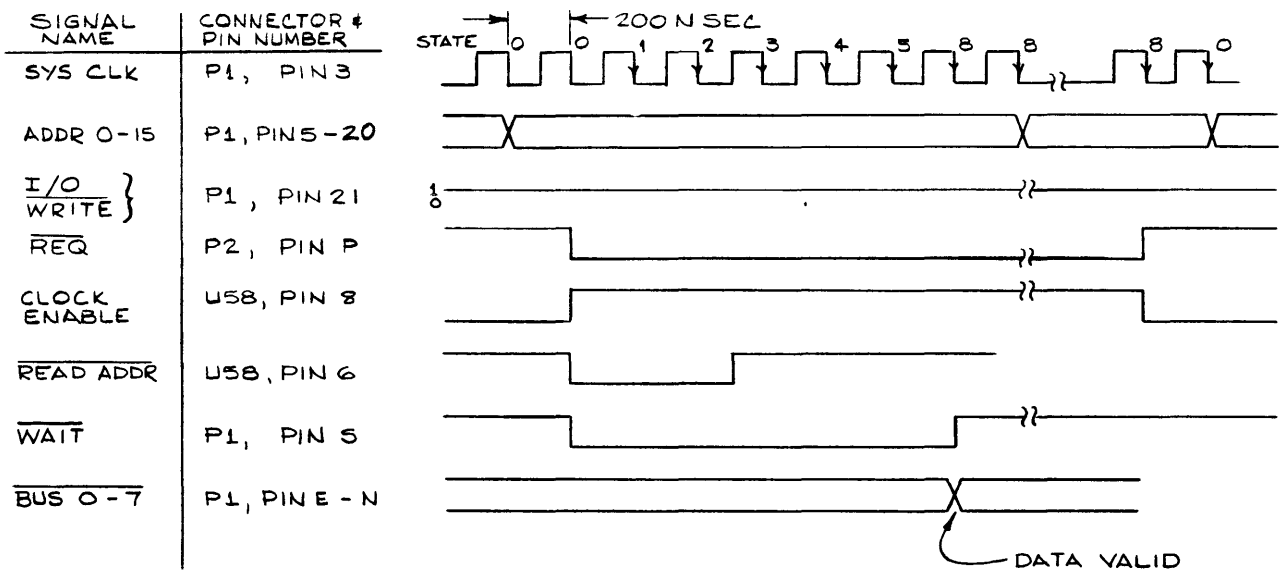

Figure 3
ROM (FA) Module Timing Diagram
APR-07-78 13255-91150

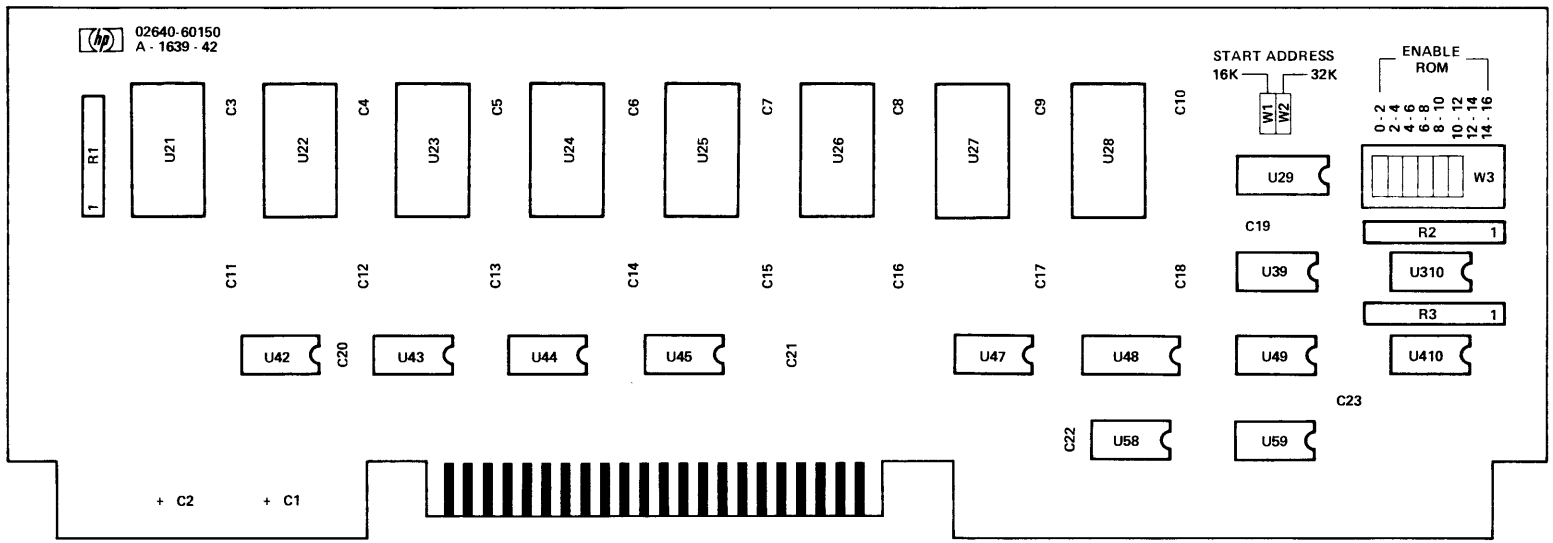

Figure 4
ROM (FA) PCA Component Location Diagram
APR-07-78 13255-91150

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60150	1	1	ASSEMBLY, CONTROL, STORE	28480	02640-60150
C1	0180-0393	6	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C3	0150-0121	5	16	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C4	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C5	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C6	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C7	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C8	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C9	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C10	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C11	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C12	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C13	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C14	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C15	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C16	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C17	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C18	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C19	0160-2055	9	5	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
R1	1810-0055	5	1	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0055
R2	1810-0125	0	2	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	28480	1810-0125
R3	1810-0125	0		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	28480	1810-0125
U29	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U39	1820-1199	1	3	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U42	1820-1209	4	2	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U43	1820-1209	4		IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U44	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U45	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U47	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U48	1820-0669	8	1	IC CNTR TTL L BCD SYNCHRO POS-EDGE-TRIG	07263	93L10PC
U49	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U58	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U59	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U310	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
U410	1820-1215	2	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS136N
W1	8159-0005	0	2	WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
W2	8159-0005	0		WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
XU21	1200-0541	1	8	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU22	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU23	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU24	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU25	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU26	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU27	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU28	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
				MISCELLANEOUS PARTS		
	0360-0124	3	1	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
	1200-0482	9	1	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0482
	1258-0124	7	6	PIN-PROGRAMING DUMPER .30 CONTACT	91506	8136-475G1