HP 13255

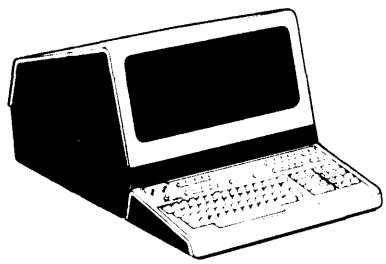
UNIVERSAL MEMORY MODULE

Manual Part No. 13255-91171

REVISED

DEC-26-78

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

1.0.1 The Universal Memory Module is used in the 264XX Terminals for Display Memory or Program Memory. This read-write memory is normally only accessible through the terminal bus (BOT). If it is connected to the Processor Module top plane it is then only accessible through the top plane bus (TOP).

1.0.2 The Universal Memory Module consists of two completely independant memory modules which each use 8 16-Pin socketed MOS RAMS. The modules may be configured with 16K RAMS organized as 16,384 X 1 bit or 4K RAMS organized as 4,096 X 1 bit giving the following Universal Memory Module standard sizes.

8K o 2 4K modules
16K o 1 16K module, 1 vacant module
32K o 2 16K modules

1.0.3 The memory mapping of the Universal Memory Module is unrestricted with the following exceptions:

o In BOT or TOP mode the memory in the memory mapped I/O space I/O space (32K-36K) can only be used with an enhanced version of the Processor Module.

o In BOT mode the module can overlay the 0-64K space occupied by TOP Read only memory (ROM) or Random access memory (RAM) in which case the BOT access is obtained by firmware inhibiting the TOP memory -this can only be done if the TOP memory is addressable as all RAM or all ROM.

o In TOP mode the module can occupy the same 0-64K space as TOP ROM, if none is present a second Universal Memory Module addressed as ROM (but functioning as RAM) may also be used.

o In TOP mode Bank Switching is possible using an enhanced version of the Processor Module and the 16K or 32K configurations of Universal Memory module. This permits up to 4 memory modules to the overlay the 0-64K TOP memory space. Bank Switching can only be used with an enhanced version of the Processor Module.

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

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1.1 OPERATION.

The Universal Memory Module is configured by loading the Ram sockets with the appropriate RAMS as follows :

Memory size	Left Bank (Module 0)	Right Bank (Module 1)
8K	4K RAMs	4K RAMs
16K	16K RAMS	none
32K	16K RAMS	16K RAMS

The HP Part Numbers are 5090-0109 (4K RAMS)
5090-0114 (16K RAMS)
-no other parts may be used.

The remaining part of the configuration is to set the jumper plugs J1-3 positions, set the switches S1-2,and connect the Top Plane connector if TOP access is required. The S1-2 switches are also programmable from the P2 connector.

1.2 PROCESSOR MODULE TOP PLANE INTERFACE.

In top plane mode, the Universal Memory Module interfaces to the Processor Module through the Top Plane Connector Assembly (02640-60012, 02640-60016, or 02640-60022).

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Universal Memory is contained in tables 1.0 through 5.0

Table 1.0 Physical Parameters.

Number	Nomenclature	+/-0.100 Inches	(Pounds)
02640-60171	Universal Memory PCA	12.5 x 4.00 x 0.5	0.5

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:

Restrictions: Type tested at product level

Failure Rate: 8K-3.61 (percent per 1000 hours)
16K-2.74 (percent per 1000 hours)
32K-4.04 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 910 mA	@ 30 mA	@ 20 mA	NOT APPLICABLE
115 volts ac		220 volts ac	
NOT APPLICABLE		NOT APPLICABLE	
Clock Frequency: 4.9150 MHz +/- 0.1%			

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
TOP PLANE CONNECTOR	Connects Universal Memory module to Processor Module via Top Plane	
	When present selects TOP access	When absent selects BOT access
J1	(Note: This jumper must always be installed for proper operation of the PCA, located in the center of the RAM memory array)	
	Applies -5V to the RAM array.	Disconnects -5V generated on the PCA. Permits an external supply to be connected.
J2-3	Bank Selector: Located in top center below P3	
	'B' Position enables Bank Select mode	$\overline{B}$' Position enables normal mode

Table 4.1 Switch Definitions

PCA Designation	Function	
	Closed	Open
S1	Mode Configurator: 0 is Blank Background (Left Module)	
INH 0	Inhibits Module 0, this must be selected if no RAMs are loaded.	Enables Module 0
32K 0	Adds 32K to Module 0 Start Address	Adds 0 to Module 0 Start Address
16K 0	Adds 16K to Module 0 Start Address	Adds 0 to Module 0 Start Address
8K 0	Adds 8K to Module 0 Start Address if $\overline{M1}.\overline{M2}.M3.\overline{B}$ Adds 2 to Bank Select Address of Module 0 if M1.M2.M3.B.TOP	Adds 0 to Module 0 Start Address if $\overline{M1}.\overline{M2}.M3.\overline{B}$ Adds 0 to Bank Select Address of Module 0 if M1.M2.M3.B.TOP
4K 0	Adds 4K to Module 0 Start Address if $\overline{M1}.\overline{M2}.M3.\overline{B}$ Adds 1 to Bank Select Address of Module 0 if M1.M2.M3.B.TOP	Adds 0 to Module 0 Start Address if $\overline{M1}.\overline{M2}.M3.\overline{B}$ Adds 0 to Bank Select Address of Module 0 if M1.M2.M3.B.TOP

Table 4.2 Switch Definitions

PCA Designation	Function	
	Closed	Open
S1	Mode Configurator: 1 is Solid Background (Right Module)	
INH 1	Inhibits Module 1, this must be selected if no RAMs are loaded.	Enables Module 1
32K 1	Adds 32K to Module 1 Start Address	Adds 0 to Module 1 Start Address
16K 1	Adds 16K to Module 1 Start Address	Adds 0 to Module 1 Start Address
8K 1	Adds 8K to Module 1 Start Address if $\overline{M1}.\overline{M2}.M3.\overline{B}$ Adds 2 to Bank Select Address of Module 1 if M1.M2.M3.B.TOP	Adds 0 to Module 1 Start Address if $\overline{M1}.\overline{M2}.M3.\overline{B}$ Adds 0 to Bank Select Address of Module 1 if M1.M2.M3.B.TOP
4K 1	Adds 4K to Module 1 Start Address if $\overline{M1}.\overline{M2}.M3.\overline{B}$ Adds 1 to Bank Select Address of Module 1 if M1.M2.M3.B.TOP	Adds 0 to Module 1 Start Address if $\overline{M1}.\overline{M2}.M3.\overline{B}$ Adds 0 to Bank Select Address of Module 1 if M1.M2.M3.B.TOP

Table 4.3 Switch Definitions

PCA Designation	Function	
	Closed	Open
S2	Mode Configurator: 0 is Blank Background (Left Module) 1 is Solid Background (Right Module)	
R.M 0	Enables RAM/ROM mode for Module 0 if TOP	Module 0 responds as Memory unconditionally
RAM 0	Module 0 responds as RAM if R.M 0.TOP	Module 0 responds as ROM (Addressing only) if R.M 0 . TOP
R.M 1	Enables RAM/ROM mode for Module 1 if TOP	Module 1 responds as Memory unconditionally
RAM 1	Module 1 responds as RAM if R.M 1.TOP	Module 1 responds as ROM (Addressing only) if R.M 1 . TOP
M1	0 and 1 are 16K Modules	0 and 1 are 4K Modules
M2-3	0 and 1 are 4K Modules or Bank Select Enabled.	0 and 1 are 16K Modules
FST	TOP 400nSec Memory Cycle (This is the normal mode).	TOP 500nSec Memory Cycle
RPT	Inhibits TOP Read to Processor when Inhibit Rom is clear.	TOP Read is unconditional.
WPT	Inhibits TOP Write	Enables TOP Write

Table 5.0 Connector Information for Universal Memory PCA

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information for Universal Memory PCA(Cont'd).

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
-D		Not Used
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not Used
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W		
-X		Not Used
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not Used

Table 5.1 Connector Information for Universal Memory PCA

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	GND	Ground
-2	ADDR0	Address Bit 0
-3	ADDR1	Address Bit 1
-4	ADDR2	Address Bit 2
-5	ADDR3	Address Bit 3
-6	ADDR4	Address Bit 4
-7	ADDR5	Address Bit 5
-8	ADDR6	Address Bit 6
-9	ADDR7	Address Bit 7
-10	ADDR8	Address Bit 8
-11	ADDR9	Address Bit 9
-12	ADDR10	Address Bit 10
-13	ADDR11	Address Bit 11
-14	ADDR12	Address Bit 12
-15	ADDR13	Address Bit 13
-16	ADDR14	Address Bit 14
-17	ADDR15	Address Bit 15
-18	$\overline{\text{TOP ACTIVE}}$	Negative True, (Low Indicates Top Plane Module Address Recognition. (High Causes a Bottom Plane Bus Cycle)
-19	READ	High Indicates Top Plane Bus Data Should Be Gated On
-20		Not Used
-21	SYNC.PHASE1	Positive Pulse of 100nSEC at Beginning of Processor Major Cycle
-22	GND	Ground

Table 5.1 Connector Information for Universal Memory PCA (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	GND	Ground
-B	DBIT0	Data Bit 0
-C	DBIT1	Data Bit 1
-D	DBIT2	Data Bit 2
-E	DBIT3	Data Bit 3
-F	DBIT4	Data Bit 4
-H	DBIT5	Data Bit 5
-J	DBIT6	Data Bit 6
-K	DBIT7	Data Bit 7
-L	B0	Bank Select Bit 0 (Enhanced Processor)
-M	B1	Bank Select Bit 1 (Module Only.)
-N	$\overline{\text{TOP WAIT}}$	Negative True, (Low) Causes Processor Wait States to Synchronise Processor with Slow Memories.
-P	$\overline{\text{I/O}}$	Negative True, (Low) Indicates Memory Mapped I/O Area (A15 A14 A13 A12) = (1000)

Table 5.1 Connector Information for Universal Memory PCA (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
-R		Not Used
-S		Not Used
-T		Not Used
-U	DISABLE ROM	High Indicates Future Memory Access Cycles should be Acknowledged by RAM not ROM
-V		Not Used
-W		Not Used
-X		Not Used
-Y	$\overline{\text{TOP GO SLOW}}$	Negative True, (Low) Causes Current Processor Clock Cycle to be 500nsec Instead of the Usual 400nsec
-Z	$\overline{\text{TOP}}$	Negative True, (Low) Selects Top Plane Access (TOP), (High) Selects Bottom Plane Access (BOT).

Table 5.2 Connector Information for Universal Memory PCA

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	M1SWOUT	M1 Switch Output
-2	M1SWIN	M1 Switch Input
-3	$\overline{\text{4K1SWIN}}$	Negative True, 4K Module 1 Switch Input
-4	$\overline{\text{32K0SWIN}}$	Negative True, 32K Module 0 Switch Input
-5	$\overline{\text{16K1SWIN}}$	Negative True, 16K Module 1 Switch Input
-6	$\overline{\text{RPTSWIN}}$	Negative True, Read Protect Switch Input
-7	R.M1SWOUT	Negative True, Ram/Rom Module 1 Switch Input
-8	REFA	Refresh Input A
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{RAM0SWIN}}$	Negative True, RAM 0 Switch Input
-11	$\overline{\text{8K0SWIN}}$	Negative True, 8K Module 0 Switch Input
-12	$\overline{\text{4K0SWIN}}$	Negative True, 4K Module 0 Switch Input
-13	+5RS	+5V With 1K Source Impedance, Reset Input
-14	REFB	Refresh Input B
-15	GND	Ground Common Return (Power and Signal)

Table 5.2 Connector Information for Universal Memory PCA (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	M2SWOUT	Ground Common Return (Power and Signal)
-B	FSTSWIN	Negative True, Fast Switch Input
-C	M3SWOUT	Negative True, M3 Switch Output
-D	8K1SWIN	Negative True, 8K Module 1 Switch Input
-E	16K0SWIN	Negative True, 16K Module 0 Switch Input
-F	32K1SWIN	Negative True, 32K Module 1 Switch Input
-H	R.M0SWIN	Negative True, Ram/Rom Module0 Switch Input
-J	RAM1SWIN	Negative True, Ram Module 1 Switch Input
-K	LOAD REFRESH	Negative True, Load Refresh Counter Value
-L	R.M0SWIN	Negative True, Ram/Rom Module0 Switch Input
-M	R.M0SWOUT	Negative True, Ram/Rom Module0Switch Output
-N		Not Used
-P		Not Used
-R		Not Used
-S	WPTSWIN	Negative True, WPT Switch Input

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figures 2 and 3), the timing diagram (figure 4),the component location diagram (figure 5) and the parts list (02640-60171) located in the appendix.

The Universal Memory PCA is the display or program memory for the terminal. It consists of memory drivers and series termination resistors, memory receivers, top data port, bottom data port, memory array, transparent data latch, top-bottom address multiplexer, refresh-memory multiplexer, bank select switch, mode configurator, top-bottom control multiplexer, clock driver, memory access control, memory timing ,delay line and test connector, top-bottom interface control, memory request generator, refresh request generator, refresh counter, and data port selector.

3.1 MEMORY DRIVERS AND SERIES TERMINATION RESISTORS.

3.1.1 The memory drivers (with integral receivers) drive the memory array bus inputs consisting of column address strobe, row address strobe data in, write enable, and address inputs.

3.1.2 The drivers have a specified propagation delay for a capacitive load 1.5X the worst case memory array input capacitance.

3.1.3 The series termination resistors minimize undershoot by terminating the bus lines with the line impedance. This approximates to 200hms since it consists of an 800hm line with distributed, lumped, capacitive loads. Current limit protection is provided free which limits the memory driver output to 75mA if two or more array inputs are shorted together.

3.2 MEMORY RECEIVERS.

The integral memory receivers are used in diagnostic mode; they allow the the memory array inputs and outputs to be tested.

3.3 TOP DATA PORT.

The top data port consists of a transceiver (U34,U44).The receiver section output corresponding to the port input is enabled in top mode only and connects the processor top plane data bus to the to the memory array input data bus.
The driver section output corresponding to the port output is enabled by the port selector (TDO) and connects the transparent data latch output to the processor top plane data bus.

3.4 BOTTOM DATA PORT.

The bottom data port consists of a transceiver (U54,U64).The receiver section output corresponding to the port input is enabled in bottom mode only and connects the bottom plane data bus to the memory array input data bus.
The driver section output corresponding to the port output is enabled by the port selector (BDO) and connects the transparent data latch output (BDO) to the bottom plane data bus.

3.5 MEMORY ARRAY.

3.5.1 The memory array consists of eight or sixteen 4K or 16K RAMS in ceramic DIP packages. Any Mostek MK4116-4 (16K) MK4027-3 (4K) or equivalent RAM with a demonstrated reliability of < 0.3% failures per 1000 hrs may be used.

The RAMS are used with sockets to allow field upgrade and repair; however, only HP 5090 prefix RAMS should be used (these have been subjected to a burn in, functional and parametric tests at HP incoming inspection).

3.5.2 Each RAM is organized as 128 X 128 cell array (16K) or a 64 X 64 cell array (4K) addressable by row and column. The 14-bit (16K) or 12-bit (4K) address is therefore multiplexed and strobed into the internal row and column latches with the row and column strobes.

3.5.3 The power distribution is via a low impedance 4-layer PC board structure. The ceramic capacitors which supply the transient current are organized so that some redundancy exists. This allows reliable operation with one open circuit component.

3.5.4 The memory array is organized as two modules of equal size (if both are loaded). They are both addressed identically;the RAS or row address strobe determines which module is selected for a write or read.

3.6 TRANSPARENT DATA LATCH.

3.6.1 The transparent data latch (U33) allows the data to propagate through the latch prior to being latched. This means the RAM access time is optimized and if a higher speed RAM is used, the memory will appear to be correspondingly higher in speed. The data is latched so that the completion of a memory cycle does not depend on the completion of the processor-memory handshake. Therefore, a diagnostic tool attached to the terminal bus cannot prevent the memory from being refreshed.

3.6.2 The pull-up resistor array (R10) is required because in the case of the 16K RAM, the data output is not latched internally and when the output is in the tri-state condition, the indeterminate logic levels which result can propagate through the latch causing potential oscillation problems.

3.7 TOP-BOTTOM ADDRESS MULTIPLEXER.

The top-bottom address multiplexer (U35,U65) selects the memory address bus from the top or bottom plane. In bottom plane mode the top connector (and therefore the top plane address bus) is disconnected and the memory address at the output (U35,65) will come from the bottom plane address bus. In top plane mode the multiplexer output is off and the memory address at the output (U35,65) will come from the the top plane address bus.

3.8 REFRESH-MEMORY MULTIPLEXER.

3.8.1 The refresh-memory multiplexer selects the row or column address (U45,55) from the top-bottom address multiplexer for memory cycles and selects the refresh counter (U46) address for refresh cycles.

$\overline{\text{MEMORY MODE}}$ enables the refresh driver output (U46, Pins1 and 19).

$\overline{\text{REFRESH MODE}}$ enables the row column driver output (U45,55 Pin 15) ,

COL selects the column address and $\overline{\text{COL}}$ selects the row address (U45,55 Pin 1).

3.8.2 The memory array address for diagnostic purposes is the same for bottom or top plane mode and the address bit mapping is as follows:

o 16K Modules

Memory Address

ADDR	15	14	13	11	10	9	8	7	6	12	5	4	3	2	1	0
Module Address	A6	A5	A4	A3	A2	A1	A0			A6	A5	A4	A3	A2	A1	A0
		Memory Array Column Address									Memory Array Row Address					

o 4K Modules

Memory Address

ADDR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Module Address				A5	A4	A3	A2	A1	A0		A5	A4	A3	A2	A1	A0
				Memory Array Column Address							Memory Array Row Address					

3.9 BANK SELECT SWITCH.

The bank select switch (J2 J3) is used to select bank select mode (8-position) in which the top plane bank select address is output to the bank select address decoder section of the mode configurator(U310 and U39, Pin 3 and 6). In normal mode this is used as part of the module address decoder for 4K modules and connects to the top-bottom address multiplexer.

3.10 MODE CONFIGURATOR.

The mode configurator consists of two identical comparators for the two memory array modules 0 and 1, and an enable for the most significant memory driver.

3.10.1 The inputs to the configurator are DISABLE ROM (P3,Pin U), BA14 and 15 outputs of the top-bottom address multiplexer, the output of the bank select switch (J2,and J3), the switch bank S1, the $\overline{A6}$ output of the refresh-memory multiplexer (U55, Pin 7),and the I/O output of the top-bottom control multiplexer (U37, Pin 4).

3.10.2 The outputs of the configurator are MODULE 0 SELECT (U410, Pin 8), MODULE 1 SELECT (U410, Pin 6), BOARD SELECT (U69, Pin 4), and the input to memory driver A6 (U53, Pin 4).

3.10.3 The comparators operate as follows:
(only one will be described)

- The $\overline{I/O}$ input from the top-bottom control multiplexer enables the comparator. If the memory address is in the memory mapped I/O space (32K to 36K), the memory module will be inhibited in BOT mode and may be enabled in TOP mode only with an enhanced version of Processor Module (13255-91209).

- The INH switch disables the comparator when closed. This is the normal mode if the RAMS are not loaded or the memory array has to be turned off.

- The 32K,16K,8K,and 4K switches specify the starting address of the module in normal mode. If the memory array contains 4K RAMs the M1 switch would be set open, this means the A6 input of the memory array is low and the memory array chip select is enabled. Also the M2 and M3 switches would be closed enabling the comparator to start on 4K boundaries.
  If 16K RAMS are used the M1 switch would be closed connecting the A6 memory address driver to the refresh-memory multiplexer, and the M2 and M3 switches would be open enabling the comparator to start on 16K boundaries.

- The R.M switch is used to enable the comparator to respond to the DISABLE ROM line (P3, Pin U). When the R.M switch is closed, the comparator will be enabled if the state of the DISABLE ROM line is set and the RAM switch is closed, or if the state of the DISABLE ROM line is cleared and the RAM switch is open (ROM selected).

- In bank select mode the memory array has to be loaded with 16K RAMs and the M2 and M3 switches closed. This is necessary because in bank select mode the section of the comparator used to decode the module address in a 4K RAM configuration is used to decode the bank select address. Therefore, if the bank select address is 3, the 8K and 4K switches would be closed and the comparator would be enabled when the state of the B0 and B1 lines is set.

3.11 TOP-BOTTOM CONTROL MULTIPLEXER.

3.11.1 The top-bottom control multiplexer (U37) selects the principle control lines from the top or bottom plane which control the memory operation. The WPT or write protect switch enables the TOP write (U66, Pin 4) when open and inhibits TOP write into the memory module when closed. It is clear that the WPT switch has to be open when the memory module is being loaded, and cannot be used if any part of the module is used as read-write memory.

3.11.2 The I/O decoder(U37, Pin 4) selects the top or bottom plane $\overline{I/O}$ lines which decode the memory mapped I/O area corresponding to 32K to 36K.

3.11.3 The memory request enable (U37,Pin 12) is unconditional from the bottom plane, the top memory request is enabled if the status for a halt instruction is absent .

3.11.4 The memory request strobe (U37, Pin 9) positive edge is the earliest a memory cycle can begin. REQUEST is used in bottom plane mode, and SYNC.PHASE1 in top plane mode.

3.11.5 The memory write enable (U37, Pin 7) enables a write into memory, in bottom plane mode it is enabled by WRITE and in top plane mode by decoding MEMORY WRITE.$\overline{OUTPUT}$ status.

3.12 CLOCK DRIVER.

The clock driver section buffers the system clock and produces $\overline{CLK}$ (U66, Pin 11) , CLK 1 (U57, Pin 8) , and CLK 2 (U78, Pin 6) which drive the parts of the module which are synchronous with the system clock.

3.13 MEMORY ACCESS CONTROL.

The memory access control initiates the memory cycle timing (RAS and-or RAS 1 set) from the output state of the refresh and memory request generator outputs REFRESH REQUEST ,MEMORY REQUEST, and MEMORY WRITE.

3.13.1 The philosophy for resolving the conflicts between the normal memory requests and the refresh requests required to refresh the dynamic RAM array is as follows:

3.13.1.1 The 'normal' mode of the module is MEMORY MODE and the row address from the memory-refresh multiplexer is set up at the memory drivers prior to the memory request being received. The memory cycle then begins as soon as memory request is set. when the memory timing has been initiated, MEMORY READY is cleared and the refresh request is inhibited until the memory cycle (MEMORY REQUEST is cleared) and the precharge time is completed (MEMORY READY set).
The pending refresh request, if any, is processed next.

3.13.1.2 When a refresh request is received REFRESH MODE is selected which enables the refresh address to the output of the refresh-memory multiplexer and the actual refresh cycle begins 200nsec later when REFRESH sets (U48, Pin 9). The memory module cycle time is therefore optimum for normal operation, and a longer cycle is used for refresh. When the memory timing has been initiated, MEMORY READY is cleared and the memory request is inhibited until the memory cycle (MEMORY REQUEST is cleared) and the precharge time is completed (MEMORY READY is set).
The pending memory cycle, if any, is processed next.

3.13.1.3 If a memory and refresh request occur simultaneously, the hardware is designed such that the refresh cycle will always occur first since the REFRESH REQUEST (U58, Pin 5) will set a maximum of 7 nsec after the buffered system clock. The pending memory request is processed (see 3.13.1.1) after the refresh request (see 3.13.1.2).

3.13.2 The mechanism for memory access is as follows:

3.13.2.1 In BOT mode for a write access MEMORY REQUEST and MEMORY WRITE are set. If MEMORY READY is set and the REFRESH REQUEST is cleared the memory request is enabled (RAS 0 or RAS 1 is set) and the memory is write enabled (WE is enabled) . The memory timing then continues to completion. A BOT read access is identical except that MEMORY WRITE will be cleared therefore the memory write will be inhibited (WE is inhibited).

3.13.2.2 In TOP mode the operation is identical except that for a write access the write data is not available at the same time as the memory request therefore the memory timing is not enabled (RAS 0 or RAS 1 set) until WRITE (P3-20) is asserted. Since the refresh request is inhibited a refresh request which occurs during this period will not interfere with the memory access.

3.13.3 The mechanism for a refresh access is as follows:

REFRESH REQUEST is set and if MEMORY READY is set, REFRESH MODE will set which enables the refresh address out of the refresh-memory multiplexer,inhibits the WE to memory and the memory request. REFRESH sets 200nsec later which sets RAS 0 and RAS 1 (U59, Pin 4 and 10) the memory timing then continues to completion.

3.14 MEMORY TIMING (see figure 4 Memory Timing Diagram)

The memory timing is initiated when a row address strobe is set (RAS 0 and-or RAS 1) and ends when MEMORY READY is set indicating a new cycle may begin. The memory timing controls the column address selection (COL), the transparent data latch clock (DATA CLOCK), the initialization of MEMORY MODE ready for the next cycle, the clearing of RAS which initiated the memory timing and the clearing of the request which caused the access (MEMORY REQUEST or REFRESH REQUEST).

3.14.1 RAS 0 or RAS 1 causes the state of the delay line input to be set, the positive input edge propagates along the delay line and each output will go positive after a fixed time in relation to the input. The output tap 3 (U79, Pin 11) @ 260nsec clears RAS 0 and RAS 1 and hence clears the state of the delay line input , the negative edge then propagates along the delay line. The delay line outputs therefore appear as a a series of 260nsec wide pulses each delayed a different time with respect to the input.

3.14.2 CAS is set by output 3 (75nsec) which clocks U77, Pin 9. If the access is a memory cycle the state of the input (U77, Pin 2) will be set and the CAS output at U78, Pin 8 will be asserted. At the same time DATA CLOCK which is logically the same as CAS is asserted which enables the transparent data latch. CAS is cleared by output 4 (320nsec) and at the same time the transparent data latch is inhibited causing the RAM output data to be held in the latch. In the case of a refresh access the CAS flip-flop will be inhibited therefore neither CAS or DATA CLOCK will be asserted.

3.14.3 SET MEMORY MODE is decoded from REFRESH (U78, Pin 2) and output 5 (415nsec) and output 3 (260 nsec).

CLEAR REFRESH REQUEST is decoded from REFRESH (U78, Pin 2) and output 3(260nsec).

CLEAR MEMORY REQUEST is decoded from MEMORY MODE (U48, Pin 6) and output 1(45nsec) and output 3(260nsec) this gives a nominal cycle time of 600nsec.

MEMORY READY is cleared by RAS 0 + RAS 1 + $\overline{\text{(output 5 and output 3)}}$ at U77 Pin 13 and is set synchronously at the next clock giving the minimum required precharge time following the row address strobe

3.15 DELAY LINE and TEST SOCKET.

3.15.1 The delay line (U79) is a hybrid circuit containing an L-C delay line and a 3-state output buffer used to generate the memory timing. The delay line is packaged in a 16 or 32 Pin DIP package ,and either one may be used on the Universal Memory Module.

3.15.2 The delay line timing is as follows:

FUNCTION	DELAY FROM INPUT	DELAY LINE PIN	TEST CONNECTOR PIN
OUT1	45nsec	Pin 13	Pin 7
OUT2	75nsec	Pin 5	Pin 2
OUT3	260nsec	Pin 11	Pin 8
OUT4	320nsec	Pin 7	Pin 1
OUT5	415nsec	Pin 9	Pin 5
Ground		Pin 8,7a	Pin 4
+5V		Pin 16,14a	
$\overline{\text{Enable}}$ Input		Pin 1 Pin 1a	 Pin 3
$\overline{\text{Enable}}$ Input			Pin 6

3.15.3 The outputs and the output enable control are accessible from the test connector for DTS 70 pretest and for servicing. Note that if an external delay line is wired to a test plug it can be used in repair to substitute for the one on the memory board. The enable delay line input on the test socket and the enable on the external delay line must be grounded and +5V connected to the external delay line.

3.16 TOP-BOTTOM INTERFACE CONTROL.

3.16.1 The top-bottom control logic provides the feedback or handshake response to memory requests received by the memory request generator.

3.16.2 In TOP mode, $\overline{\text{TOP ACTIVE}}$ (P3, Pin-18) is asserted by BOARD SELECT (U78, Pin 4) meaning the memory module will respond to a top plane memory access request. The processor module will then inhibit the bottom plane request sequence and complete a top plane memory cycle.

At the same time $\overline{\text{GO SLOW}}$ (P3,Pin Y)is enabled if the FST switch is open will be asserted indicating the memory cycle will be 500nsec instead of the normal 500nsec cycle.

$\overline{\text{TOP WAIT}}$ (P3, Pin-N) is asserted if a top plane memory request is initiated while a refresh cycle is in progress.

3.16.3 In BOT mode, $\overline{\text{WAIT}}$ (P1,Pin-S) is asserted when the memory request is initiated and cleared when the data is ready. The intervening time may include a refresh cycle in which case the data is ready after the refresh and the memory cycles are completed.

3.17 MEMORY REQUEST GENERATOR.

The memory request generator consists of the MEMORY REQUEST and MEMORY WRITE flip-flops (U38). These are set if a strobe (U38 Pins 3 and 11) is input from the top-bottom control multiplexer when the enables (U38,Pins 2 and 12) are asserted and the board select(U38,Pin 4 and 10) is asserted. MEMORY WRITE is set for a write operation, and clear for a read operation.
When the memory operation is completed, the MEMORY REQUEST and MEMORY WRITE flip-flops are cleared.

3.18 REFRESH REQUEST GENERATOR.

3.18.1 The refresh request generator consists of a refresh counter (U27, U28) and a refresh request JK flip-flop (U58, Pin 5).

3.18.2 The refresh counter is synchronous with the system clock and is used to time out the interval between refresh requests. The modulus of the counter is 74 this gives a carry output (U27, Pin 15) every 15.27 usec or each memory row address is refreshed at 15.27 x 128 usec = 1.96msec (4K RAMS are refreshed at twice this rate). The carry is latched by the Refresh request flip-flop which is cleared after the refresh memory cycle is completed.

3.18.2 The modules of the refresh request generator counter can be cnanged as follows:

REFA	REFB	Modulus	Purpose
1	1	74	Normal refresh @ 2msec
1	0	1	DTS 70 Pretest
0	1	256	Memory Tester extended refresh

3.19 REFRESH COUNTER.

The refresh counter (U36, U56) contains the row refresh address. It is incremented at the end of a refresh cycle.

3.20 DATA PORT SELECTOR

The data port selector controls the TOP and BOTTOM DATA PORT. In TOP mode the TOP DATA PORT output is enabled by TDO, which is asserted by READ (P3,Pin-19) and BOARD SELECT and RPT switch.
The RPT or read protect switch is used to prevent the module from responding to memory reads when the state of the DISABLE Line is clear. When the current loader ROM is used, during the loading process the state of the DISABLE ROM line is initially clear and instructions are read from the loader ROM while the data is written into the RAM on memory module. This requires the ROM to be read only and the RAM on the memory module to be write only during the load sequence. After the load operation is complete the state of the DISABLE ROM line is high, the ROM is inhibited and the RAM on the memory module operates in read or write mode.

4.0 FUTURE ENHANCEMENTS.

When 64K RAMs are available,(with design modifications) the Universal Memory Module standard sizes would be as follows:

64K o 1 64K module , 1 vacant module
128K o 2 64K modules

Based on the assumption that the 64K RAM will be the same as a 16K RAM except that the +12V supply pin will be replaced by the additional address pin the design changes required would be minor and are therefore documented as follows:

1. Connect the TOP-BOT address multiplexer outputs (U35,Pins 18-16) to the unused inputs of the refresh-memory address multiplexer (U45,Pin 5 and 6).
2. Connect the output (U45, Pin 7) to the refresh buffer (U46, Pin11), and the refresh buffer input (U46, Pin 17) to the refresh counter (U56, Pin 11).
3. Change the constant at the preset inputs of the refresh counter (2msec - 1 memory cycle time) apart for the same row address.
4. Remove U310 and U410 in the mode configurator ,since the address would always start at 0K. Bank select mode would have to be used with two 64K modules.
5. Reconnect the memory driver (U63) so that one driver is used for CAS and one used for A7 for the memory array .The A7 driver input would connect to the refresh-memory multiplexer (U45, Pin 7).

5.0 SERVICE GUIDE.

5.1 In the event of problems the most likely causes are:

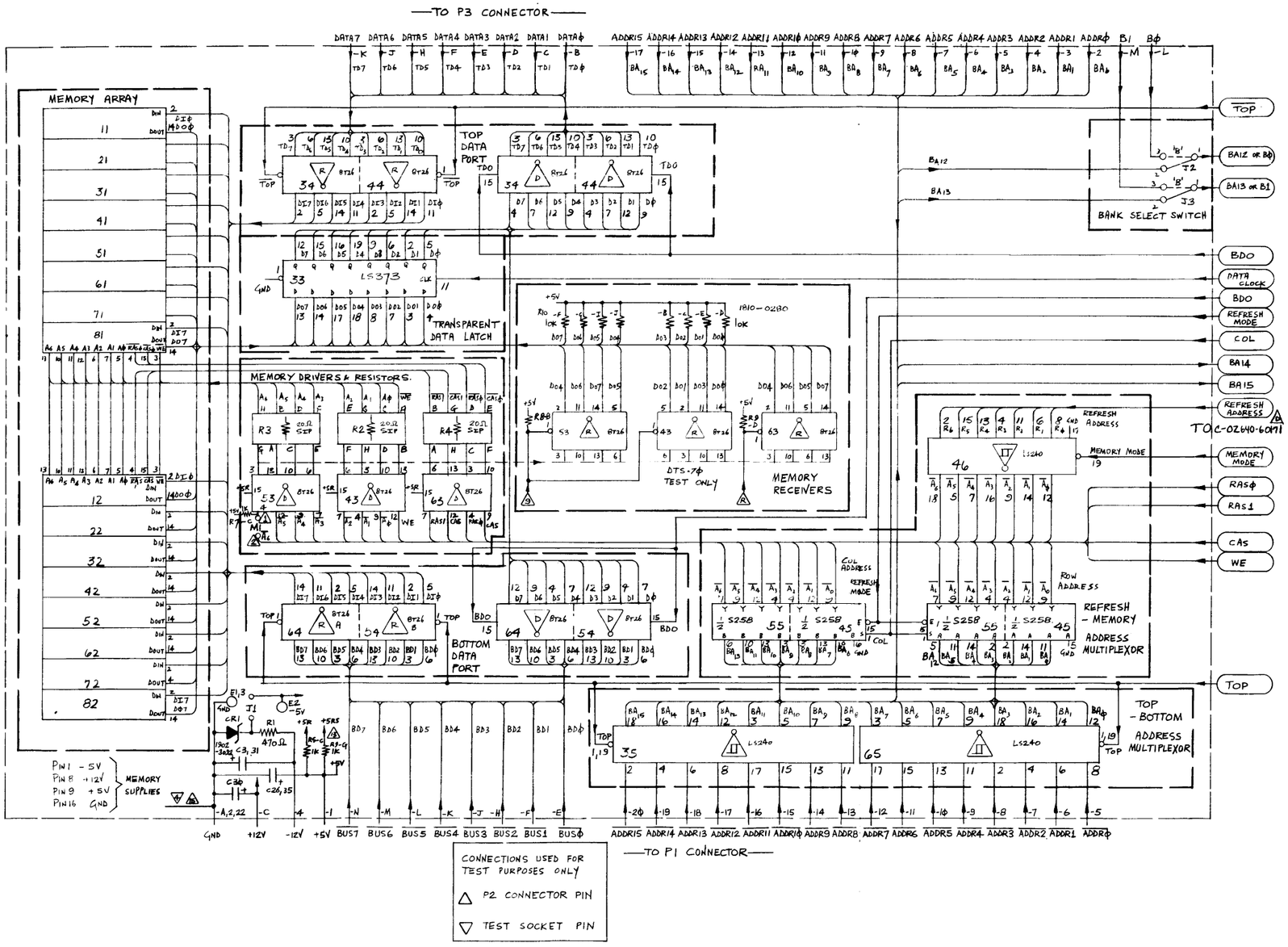
1. Incorrect configuration.

2. Power supply voltages incorrectly set.

3. Bad RAMS

4. Other hardware problems which require board replacement.

5.2 The performance can be verified by configuring the module as display memory and doing bottom and top plane self test several times. The top plane test will not provide diagnostic messages (since the DMA module does not have a top plane interface mode). However, the terminal will beep each time the test is passed successfully and the lights will go off after the last test.



TOC-02640-6091

Figure 3
Universal Memory Schematic Diagram Sheet 2
DEC-26-78 13255-91171

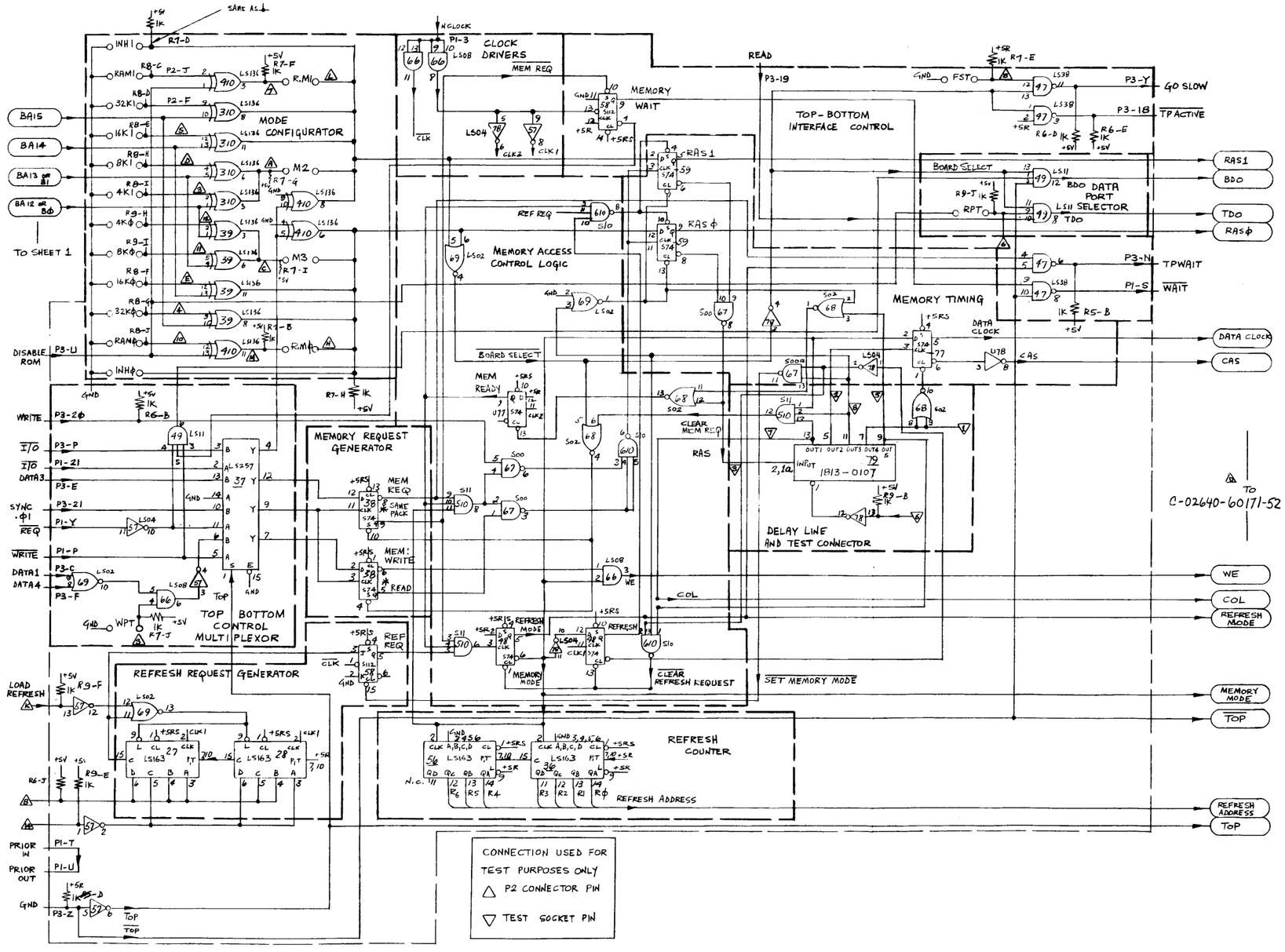
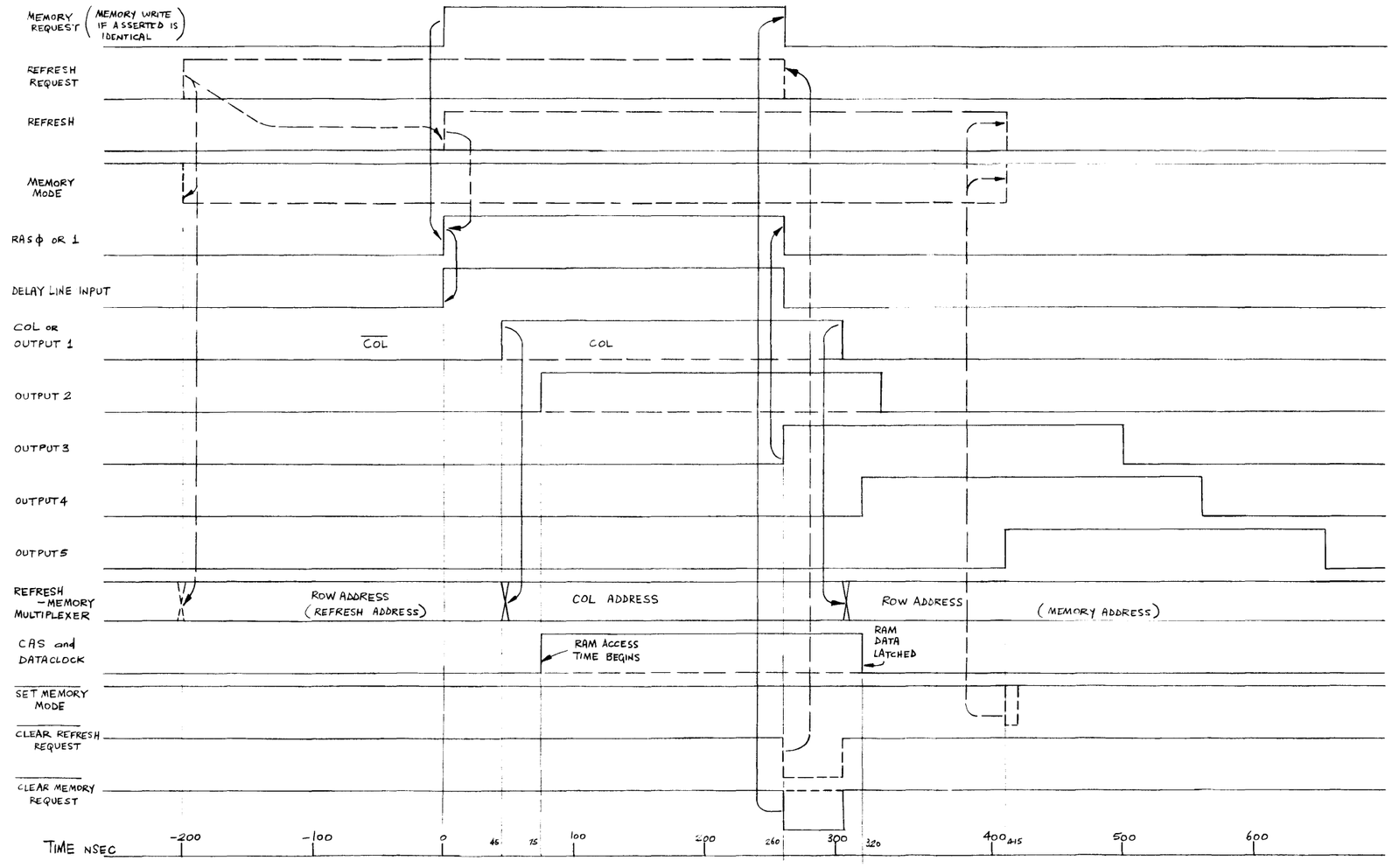


Figure 2
Universal Memory Schematic Diagram Sheet 1
DEC-26-78 13255-91171



THIS DIAGRAM SHOWS THE MEMORY TIMING OPERATION.
FOR A MEMORY AND REFRESH ACCESS

(____)MEANS REFRESH CYCLE ONLY

Figure 4
Universal Memory Memory Timing Diagram
DEC-26-78 13255-91171

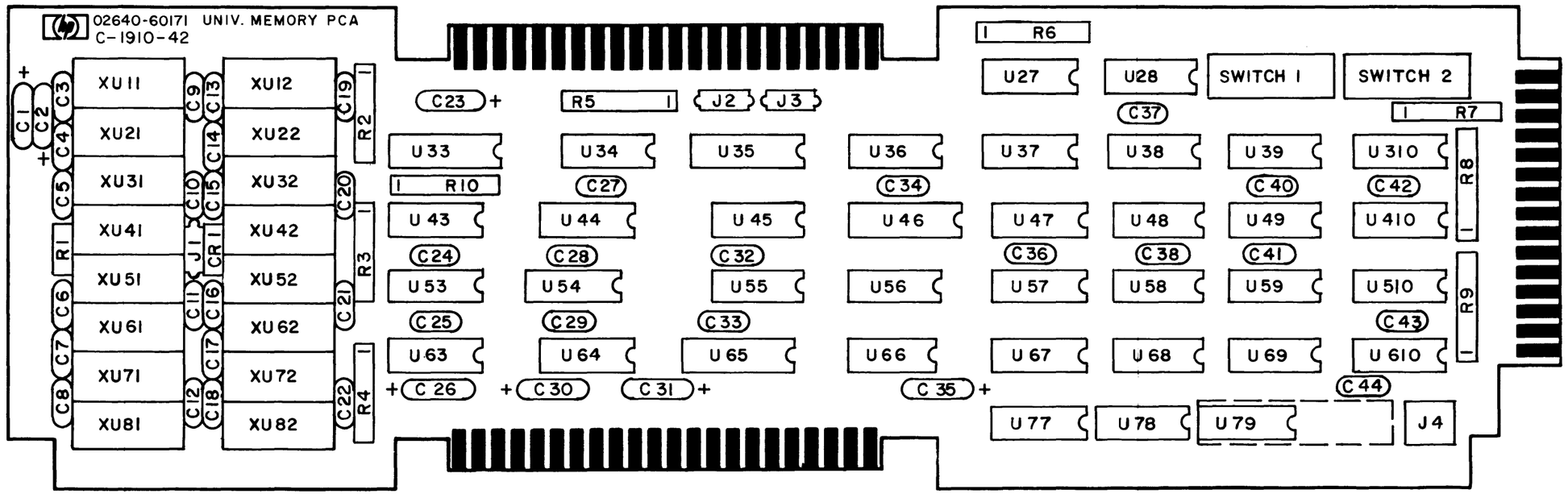


Figure 5
Universal Memory PCA Component Location Diagram
DEC-26-78 13255-91171

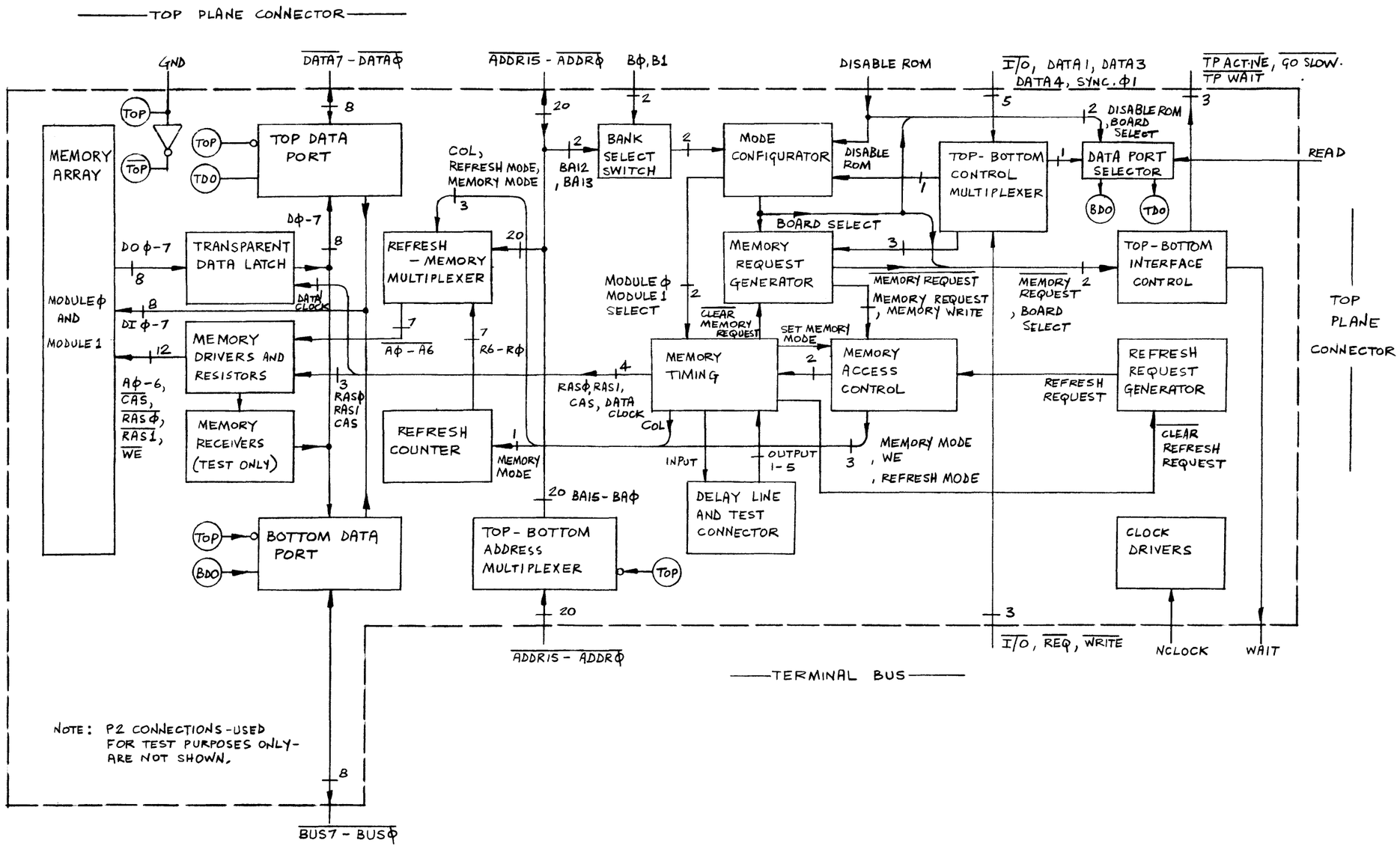


Figure 1
Universal Memory Module Block Diagram
DEC-26-78 13255-91171

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60171	6	1	UNIVERSAL MEMORY ASSEMBLY DATE CODE: C=1910-42	28480	02640-60171
C1	0180-1746	5	3	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C2	0180-0393	6	4	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C3	0160-4892	6	20	CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C4	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C5	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C6	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C7	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C8	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C9	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C10	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C11	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C12	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C13	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C14	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C15	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C16	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C17	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C18	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C19	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C20	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C21	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C22	0160-4892	6		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-4892
C23	0180-0393	6		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C24	0150-0121	5	16	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C25	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C26	0180-0393	6		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C27	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C28	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C29	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C30	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C31	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C32	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C33	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C34	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C35	0180-0393	6		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C36	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C37	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C38	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C40	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C41	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C42	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C43	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
C44	0150-0121	5		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0150-0121
CR1	1902-3092	1	1	DIODE-ZNR 4.99V 2% DO-7 PD=.4W TC=-.012%	28480	1902-3092
E1	0360-0124	3	3	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
E2	0360-0124	3		CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
E3	0360-0124	3		CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
J1	1251-0697	5	3	CONNECTOR-SGL CONT SKT .022-IN-BSC-SZ	28480	1251-0697
J2	1251-0697	5		CONNECTOR-SGL CONT SKT .022-IN-BSC-SZ	28480	1251-0697
J3	1251-0697	5		CONNECTOR-SGL CONT SKT .022-IN-BSC-SZ	28480	1251-0697
J4	1200-0455	6	1	SOCKET-IC 8-CONT DIP-SLDR	28480	1200-0455
R1	0683-4715	0	1	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R2	1810-0322	9	3	NETWORK-RES 8-SIP20.0 OHM X 4	01121	4088200J
R3	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	4088200J
R4	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	4088200J
R5	1810-0275	1	5	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R6	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R7	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R8	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R9	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R10	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
SW1	3101-2102	6	2	SWITCH-RKR DIP-RKR-ASSY 10-1A .05A 30VDC	28480	3101-2102
SW2	3101-2102	6		SWITCH-RKR DIP-RKR-ASSY 10-1A .05A 30VDC	28480	3101-2102
U27	1820-1432	5	4	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U28	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U33	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U34	1820-1081	0	7	IC DRVR TTL BUS DRVR QUAD 1-INP	04713	MC8T26AP
U35	1820-1917	1	3	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U36	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U37	1820-1438	1	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U38	1820-0693	8	4	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U39	1820-1215	2	3	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS136N
U43	1820-1081	0		IC DRVR TTL BUS DRVR QUAD 1-INP	04713	MC8T26AP
U44	1820-1081	0		IC DRVR TTL BUS DRVR QUAD 1-INP	04713	MC8T26AP
U45	1820-1309	5	2	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
U46	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U47	1820-1209	4	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U48	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U49	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
U53	1820-1081	0		IC DRVR TTL BUS DRVR QUAD 1-INP	04713	MC8T26AP
U54	1820-1081	0		IC DRVR TTL BUS DRVR QUAD 1-INP	04713	MC8T26AP
U55	1820-1309	5		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
U56	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U57	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U58	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U59	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U63	1820-1081	0		IC DRVR TTL BUS DRVR QUAD 1-INP	04713	MC8T26AP
U64	1820-1081	0		IC DRVR TTL BUS DRVR QUAD 1-INP	04713	MC8T26AP
U65	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U66	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U67	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U68	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U69	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U77	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U78	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U79	1813-0107	4	1	IC MISC TTL 1-INP	28480	1813-0107
U310	1820-1215	2		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS136N
U410	1820-1215	2		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS136N
U510	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U610	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
W1	1258-0124	7	3	PIN-PROGRAMING JUMPER .30 CONTACT	91506	8136-475G1
W2	1258-0124	7		PIN-PROGRAMING JUMPER .30 CONTACT	91506	8136-475G1
W3	1258-0124	7		PIN-PROGRAMING JUMPER .30 CONTACT	91506	8136-475G1
XU11	1200-0607	0	16	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU12	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU21	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU22	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU31	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU32	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU41	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU42	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU51	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU52	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU61	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU62	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU71	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU72	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU81	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU82	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
	7124-2099	2	1	LABEL	28480	7124-2099