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IBM 1130 Special Feature Description – High Speed Binary Synchronous Communications Adapter

This manual describes the operation and programming of the IBM high speed binary synchronous communications adapter as it relates to the 1130 system. A general description of the channel and information concerning the machine interface are also included.

PREFACE

This manual describes the high speed binary synchronous communications adapter for the 1130 system. It lists the communication facility requirements, transmission speeds, and transmission codes. A definition of each of the control characters and a description of their use in message blocks are contained in this manual. A general description of the basic circuitry contained in the adapter is included.

Programming instruction formats are illustrated and explained. In addition, a section is devoted to programming considerations and limitations and to each of the modes and conditions of operation. Error detection, by program and hardware, is also described.

This manual contains flow charts of typical transmit and receive operations and an illustration of a binary synchronous (bi-sync) message exchange. The reader should have a prior knowledge of the IBM 1130 computing system and should be familiar with the following publications:

IBM 1130 Functional Characteristics, Form A26-5881
IBM Binary Synchronous Communications, Form A27-3004

Second Edition

This is a major revision of, and makes obsolete, A26-1575-0.

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest SRL Newsletter for revisions or contact the local IBM branch office.

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CONTENTS

Transmitting digital data over communications lines is a fundamental requirement in a growing variety of data processing applications. As the kinds of applications have grown, so has the variety of terminal devices, data codes, and communication facilities.

Existing data communication links use control procedures and formats that have been optimized for particular devices, systems, and applications. For example, different control procedures are used in the IBM synchronous transmitter receiver (STR) family of transmission devices as compared to the various teletypewriter systems. Because these procedures were optimized for each system, their suitability for other devices and applications is limited.

Special-purpose digital data communication systems have real advantages in terms of efficiency and cost. But the growth in kinds of applications and device types has dictated the requirement for a unified and consistent set of procedures for a broad class of digital data communication. Binary synchronous communication (BSC) is a set of conventions developed to satisfy that need.

The BSC conventions have been established separately for the elements of data transmission, including transmission codes, synchronizing procedures, start of transmission, message blocking, error detection and correction, acknowledgement signals, and ending of transmission. For each element, specific procedures have been established to carry out the function and relate it to other elements of the communications operation. However, all BSC conventions do not apply to all data links. A basic set of conventions applies to all data communications links. Some additional conventions apply only to particular types of links. Finally, some conventions apply only to optional capabilities if they have been incorporated into the system.

The high speed binary synchronous communications adapter (BSCA) provides the 1130 system with operational capability for binary synchronous communication.

GENERAL DESCRIPTION

The BSCA enables the 1130 system to exchange digital data on a point-to-point, contention phase communication link. The communication adapter (CA) operates over permanently connected lines and can communicate with other devices that use common controls, such as a System/360 equipped with a 2701 that has the following features:

- 7697 (SDA II).
- 9060 (EBCDIC).

Data is transmitted serially by bit and by character. (Both the character and the bits of which they are comprised are sent sequentially.)

A character frame is eight bits. Character codes as well as control codes are in extended binary coded decimal interchange code (EBCDIC). The CA is capable of non-transparent, transparent, and header operation.

The following features are not included in the adapter.

- ASCII line control procedures and data codes.
- VRC/LRC checking.
- Multipoint operation.
- Switched circuit links.
- Synchronous transmit receive.
- Universal code synchronous transmit receive (UCSTR).
- Intermediate Block Check (ITB)

The adapter uses cyclic redundancy checking (CRC) for message blocks.

Implementation

The adapter is designed with SLT components and requires three SLT boards. The boards are installed in the 1133 Multiplex Control Enclosure on a second SLT gate provided by RPQ 831551.

The adapter provides for the transfer of data between the 1130 and remote stations. The adapter has been designed to communicate with remote stations, using the data sets listed in the communication facilities section of this manual.

Physical Planning Information

The external cable which connects to the data set is provided by this RPQ feature. It has a maximum length of 40 feet. The cable is supplied at 25 feet if the length is not specified on the order form.

Data Set Strapping

For 301B data set or equivalent:

a. 40.8K bits per second
b. Data set clocking

For 303B data set or equivalent:

a. Synchronous
b. Data set clocking
c. Unbalanced
d. Scrambler
e. Mark hold when send request off
f. 50% roll off filter

For 303C and 303D or equivalent:

Same as 303B except item f which is 100% roll off filter.

System Prerequisites

Prerequisites for the addition of the bi-sync communications adapter to the 1130 system are:

1. 1133 Multiplex Control Enclosure.
2. Feature Code -- 1865 Channel Multiplexer
3. RPQ 831551 -- 1133 expansion.

COMMUNICATION FACILITIES

The communication facilities should be permanently connected private or leased lines and must provide for four-wire half-duplex message transmission (alternate transmission in either way in a non-simultaneous manner). The line should have broad band communication channels to handle the transmission rates.

The following is a list of the approved data sets and operating speeds. Equivalent data sets may be substituted.

19,200 baud	Western Electric* 303B
40,800 baud	Western Electric 301B
50,000 baud	Western Electric 303C
230,400 baud	Western Electric 303D

Baud = bits/second

Data Rates

The maximum data rate is a function of the data set attached, the overlapping CPU operation, and higher priority cycle stealing. The maximum instantaneous data rates are:

KBS (kilobytes/sec)	Baud
2.4	19,200
5.1	40,800
6.25	50,000
28.8	230,400

These rates are based on worst case with the following conditions:

a. A machine cycle has just been started when a cycle steal request occurs.
b. No higher priority cycle steal devices are making demands upon the system.

Data is transferred two 8-bit characters (two bytes or one word) at a time between 1131 main storage and the CA. When transmitting, total record throughput is also a function of the time required to service interrupt level 3 and send end sequence.

Point-to-Point Network

All message exchanges for the CA occur on a point-to-point network. (All messages are between two stations.) All lines are permanently connected, whether or not the stations are active. The network may be comprised of a number of point-to-point stations, all of which must be connected to a central station to handle traffic between the different stations.

TRANSMISSION CODE

The extended binary coded decimal interchange code (EBCDIC) is used by the CA to transmit and receive data. Several unique characters are reserved for control characters and cannot be used as data. However, in full transparent text mode, these restrictions are removed. In transparent text mode, control characters are designated by preceding them with the DLE (data link escape) character. Any code translation required must be performed by the program.

Characters are transmitted and received low-order bit first; that is EBCDIC bit position 7, main storage position 7 or 15, as the word resides in main storage. (See Figure 1, EBCDIC Code Chart.)

* Trademark of Western Electric Company, Incorporated.

Control Characters

Control of message formats transmitted by the CA is maintained through the use of control characters.

SYN -- Synchronous Idle

Used to establish synchronism and as a time fill in the absence of any data or control character from main storage.

SOH -- Start of Heading

Precedes a block of heading data. A heading consists of auxiliary information necessary to process the text portion of the message.

STX -- Start of Text

Precedes a block of text characters. Text is that portion of a message treated as an entity to be transmitted to the remote station without change. STX also terminates a heading.

ETB -- End of Transmission Block

Indicates the end of a group (block) of characters started with SOH or STX. The blocking structure is not necessarily related to the processing format. The block check characters are sent following ETB. ETB requires a reply indicating the receiving station's status (ACK 0, ACK 1 or NAK).

ETX -- End of Text

Terminates a block of characters started with STX. The block check characters are sent following ETX. A reply is required from the receive station indicating the status.

EOT -- End of Transmission

Indicates the conclusion of message transmission, which may contain one or more blocks, including text and associated headings. It causes a reset of the stations on the line (unless it erroneously occurs within a text or heading block).

ENQ -- Enquiry

Used as a request for a response, to obtain an indication of station status (ACK 0, NAK, etc.). It can also be used to obtain a repeat transmission of a reply, if a transmission was not received when expected or was in error.

ACK 0, ACK 1 -- Affirmative Acknowledgement

These replies indicate the previous block was accepted and the receiver is ready to accept the next block of the transmission. ACK 0 and ACK 1 are used alternately as affirmative replies and provide a sequential checking control for a series of transmissions. Thus it is possible to maintain a running check to ensure that each reply corresponds to the immediately preceding message block.

NAK -- Negative Acknowledgement

Indicates that the previous block was unacceptable and the receiver is ready to accept a retransmission of the erroneous block. It is also the not-ready reply to a station selection.

DLE -- Data Link Escape

A control character used exclusively to provide supplementary line-control signals for transparent text. The sequences DLE STX and DLE ETX initiate and terminate transparent text. In addition, other control sequences using DLE are available to provide active control characters within transparent text as required. (See control character decode section.)

Pad Character

To insure that the entire message or control signal is properly transmitted to the data set, the communications adapter sends an extra character (pad character) following each turnaround character (NAK, EOT, ENQ). When ETX and ETB cause the line turnaround, the pad character follows the block check characters. This character is necessary to ensure that the last significant character is sent before the data set transmitter turns off.

The pad character generated by the adapter consists of all 1-bits (11111111).

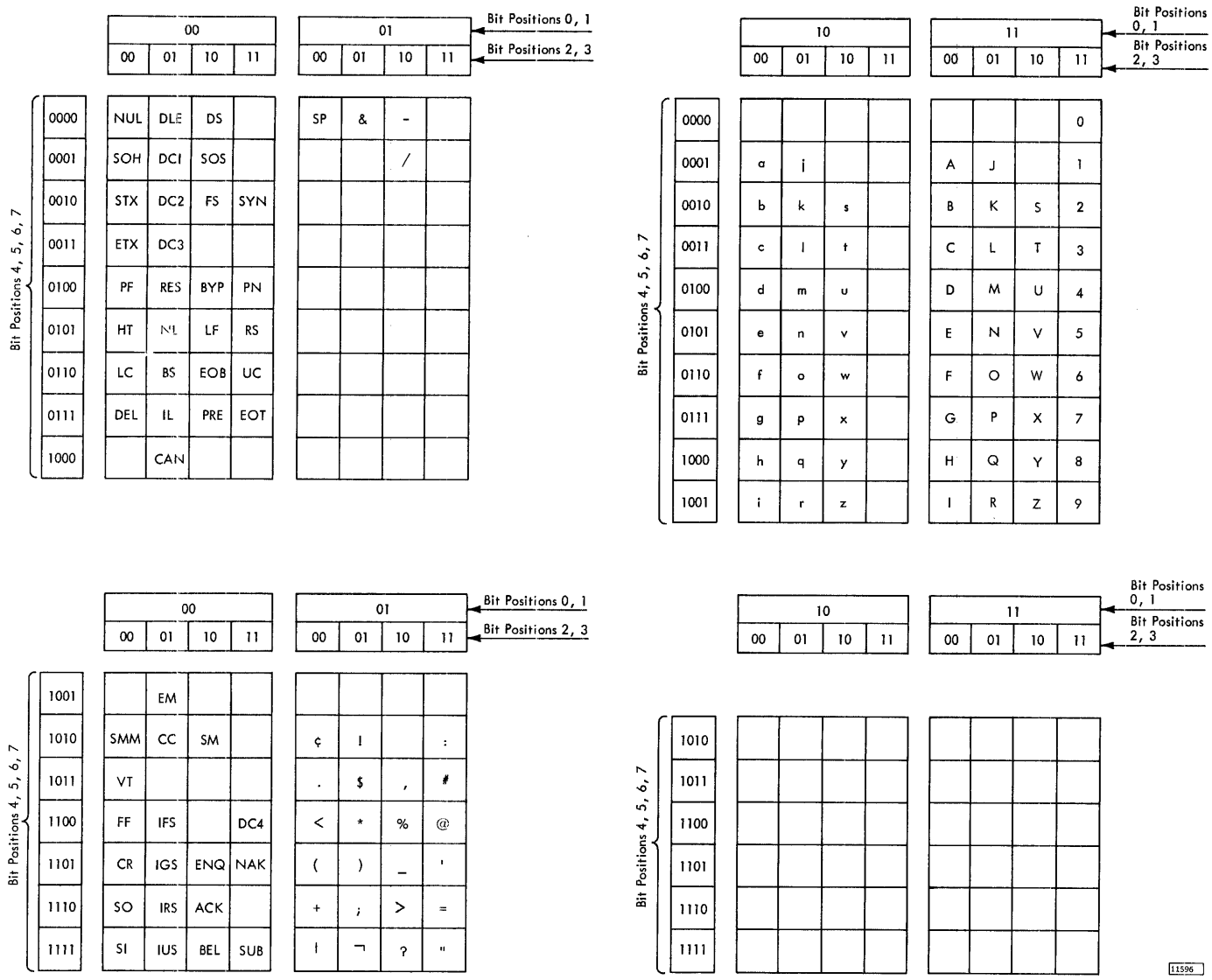


Figure 1. Extended Binary - Coded-Decimal Interchange Code (EBCDIC)

The communications adapter (CA) functions as an input/output control between the 1130 system and transmission line. All data transfers are character synchronous. In receive mode, once character phase has been established, each subsequent character is recognized as a group of data bits. The bits are "framed" by an internal bit counter.

Incoming data from the transmission line is serial by bit and by character. As the data comes in, it is shifted one bit at a time through the deserializer. When a complete character (eight bits) has been assembled, the character is transferred, in parallel, to the upper data register (bit positions 0-7). The next character shifted into the deserializer, is transferred to the lower data register (bit positions 8-15). The two assembled bytes (16 bits) of data are transferred to main storage by a cycle steal. The byte counter determines the record length, and the cyclic redundancy check register maintains a running check of message validity.

Outgoing data is transferred, in parallel, two bytes at a time to the CA data register on cycle steal basis. The CA then starts transmitting data. First the high-order bit positions (0-7), then the low-order bit positions (8-15), of the data register are transferred in parallel to the serializer, which shifts the bits serially onto the transmission line (low-order bit first). At the end of a block of data, an end op interrupt is generated to the CPU to signal for an end of transmission. The CPU services the interrupt by initiating an end sequence operation which results in the transmission of the ending character followed by the cyclic redundancy check characters.

Address Registers

The CA attachment provides two address registers along with associated controls: a write address register (WAR) and a read address register (RAR).

Write Address Register: When the CA is in transmit mode, this register is used to address the area in main storage which contains the transmit data table. The first address of the transmit data table is contained in the effective address of the initiate write instruction and it is during the execution of this instruction that WAR is loaded with the contents of the effective address.

Transfer of data to the CA occurs on a cycle steal basis, and WAR is incremented by 1 at the end of each cycle steal data transfer.

Read Address Register: When the CA is in receive mode, this register is used to address the area in main storage that will receive data transmitted by the remote station. The first address of the receive data table is contained in the effective address of the initiate read instruction and is loaded into RAR during the execution of this instruction.

Data is transferred to main storage on cycle steals, with RAR being incremented by 1 at the end of each cycle steal data transfer.

Also, the first cycle steal occurring just after an initiate write IOCC will load RAR with the first word of the transmit data table. Since the first word of the transmit data table contains the address of the receive data table, the CA, if chaining has been specified by the initiate write IOCC, can start receiving data at the end of the transmission without issuing an initiate read IOCC.

Byte Counter Register (BCR)

On the second cycle steal after an initiate write IOCC, this 14-bit register is loaded with the 1's complement of the contents of the second word of the transmit data table. The second word contains a binary number equal to the number of bytes (characters) to be transmitted (excluding end characters).

In the case of an initiate read IOCC, the first word of the receive data table is loaded, in complement form, into the BCR by the first cycle steal. This word contains the maximum expected message length to be received.

The BCR is incremented by 1 each time a byte is transferred between the data register and the serializer-deserializer (SERDES). Data transfer ceases when all bit positions of the register are 1; that is, when the number is 0. In receive mode, if data continues to be received after the BCR reaches 0, the register continues to be incremented. However, data transfers to main storage will not occur, and the wrong length indicator bit will be set in the sense status DSW. (See Figure 2.)

Data Register

This 16-bit (two-byte) register is loaded from main storage, under cycle steal control, with data to be

transmitted. The data is then transferred to the serializer-deserializer one byte at a time for transmission.

In receive mode, the data register is loaded from the serializer-deserializer and then transferred to main storage under cycle steal control or when the byte counter goes to 0.

Serializer-Deserializer (SERDES)

This section provides circuitry for receiving serial data from the data set, forming the serial data into eight-bit characters, and sending these characters, in parallel, to the data register. In transmit mode, eight-bit characters are received in parallel from the data register and serialized for transmission.

Cyclic Redundancy Check Register

This section provides a two-byte register for hardware computation of the block check characters (BCC). These characters are accumulated in the CRC register, low-order bit first, during a transmit or receive mode operation. The BCC's are transmitted at the end of a block of text in transmit mode, or are compared with the received block characters in receive mode. The compare between the accumulated BCC's in the receiver and the received BCC's should result in the CRC register being zero.

Test SERDES

This register functions the same as SERDES in transmit mode. It is used to check the proper operation of SERDES and the data set during a loop test.

Sequence Counter

This eight-position counter is used to count and keep track of a series of routines that are performed by the CA in the initiate sequence, and the end sequence, for receive and transmit modes of operation.

Bit Counter

This eight-position counter is used to frame the serial data received from the line into eight-bit characters and to control parallel data transfers to and from the serializer-deserializer.

Real-Time Counter

This six-position counter is used to count real elapsed time and to provide checks for a variety of conditions necessary to insure proper bi-sync operation. It is also used to start the insertion of timefill characters, at the proper time, during transmit mode.

Control Character Decode

The CA provides circuit hardware to decode the following control characters:

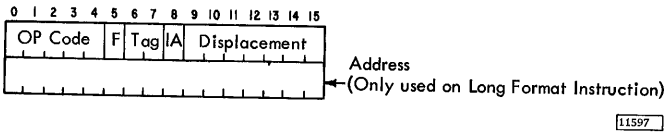
Normal Text Mode	Transparent Text Mode
DLE	DLE DLE
SYN	DLE SYN
SOH	DLE SOH
STX	DLE STX
ETX	DLE ETX
ETB	DLE ETB
ENQ	DLE ENQ

In normal text mode, these characters are restricted for control purposes only. In transparent text mode, they may be used as data or control characters. When they appear in transparent text they must be preceded with a DLE, to be decoded as a control character; otherwise they will be accepted as data.

The decode circuits are used in transmit and receive operations.

Program Character Decode: All turnaround characters, bit structure 011xxxxx, must be decoded by programming (ACK-0, ACK-1, etc.).

The execute I/O (XIO) instruction initiates all input/output operations for the communications adapter and the 1131 via the 1133 multiplex channel. Refer to SRL manual, IBM 1130 Functional Characteristics, Form A26-5881. The XIO can be either short (16 bits) format or long (32 bits) format and is used to specify an input/output control command, (IOCC) which is required for each desired operation.



EXECUTE I/O INSTRUCTION

OP (Operation) Code

Specifies operation to be performed: execute I/O.

F (Format)

Format control bit. A 0 indicates short instruction. A 1 designates a long instruction.

Tag

These two bits designate the register to be used for address modification.

IA (Indirect Address)

A 0 indicates a direct address. A 1 specifies indirect addressing.

Displacement

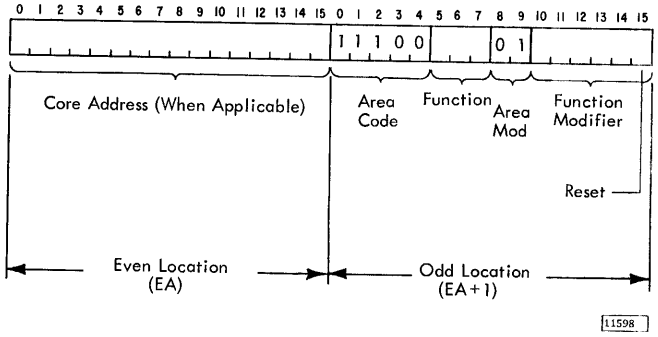
In short format bits 9-15 are used to develop the effective address of the IOCC. The bits are ignored in long-format instructions.

Address

These 16 bits contain the address of the IOCC if a long instruction format is used.

INPUT/OUTPUT CONTROL COMMAND

The IOCC specified by the XIO instruction is a 32-bit word used to define an I/O operation for the communications adapter (CA). The effective address generated by the XIO instruction is the core storage location containing the first word of the IOCC. The second word of the IOCC is at EA+1. The following illustration shows the general format of the IOCC word.



ADDRESS

Specifies the address location of the first word of either the transmit or receive data tables. The first word contains the record length to be transmitted or received. If the command address contains main storage location 1000 and the record length found at this location is 50, then the data table occupies locations 1001 through 1025.

The address field is used only for initiate write, XIO write or initiate read operations.

AREA CODE AND MODIFIERS

Bits 0 through 4 plus modifier bits 8 and 9 are used to address the CA. Area code 28-1 (11100-01) signifies that the CA is to execute a specific XIO command.

FUNCTIONS

The primary I/O functions are specified by the three-bit function code (bits 5, 6, and 7). In addition bits

10 through 14 are used to modify or expand the function. Bit 15 is used to reset certain indicators when it is on.

Function 000

Not a legal function for the communications adapter. Will cause a program check condition.

Function 001 -- XIO Write

This function should be used only to service an end sequence request interrupt when the CA is in transmit mode. It is used to send the ending control character for transmit text or header operation. The only normal ending control character sequences are:

Nontransparent Text	Header	Transparent Text
SYN/ETX	SYN/ETB	DLE/ETX
SYN/ETB		DLE/ETB
SYN/ENQ		DLE/ENQ

Function 010

Not a legal function for the communications adapter. Will cause a program check condition.

Function 011 -- Sense Interrupt Level

This function is used to sense the communications adapter when an interrupt level 3 occurs. There are three conditions in the CA which cause interrupt level 3 to occur: end op, end seq request, and any error. A bit 10 is stored in the ILSW if the interrupt was caused by the CA.

Function 100 -- Control

The control command conditions the CA to accomplish the operations specified by modifier bits 12 through 14. This command is always used with modifier bits.

Modifiers (Control Command):

000 -- Not used.

001 -- The CA is set to test mode.

010 -- Sets the CA for loop test mode. If bit 15 is on (1), the loop DS test is conditioned. If bit 15 is off (0), the loop CA test is conditioned.

011 -- Resets the CA. In addition, if bit 15 is on, the CA is disabled and is set to reset mode. If bit 15 is off, the CA is enabled and is set to control mode.

Programming Note: The CA must be in control mode before it can transmit or receive.

100 -- Used in conjunction with test mode to advance the test clock. Bit 10 is used to simulate data from the receive line of the data set. Bit 10 on (1) simulates a "mark"; off (0) simulates a "space".

101 through 111 -- Not used.

Function 101 -- Initiate Write

This function is used to start all transmit operations. During execution of this IOCC, the address of the first word of the transmit data table is transferred to the write address register (WAR), and data is transferred from main storage to the CA data register on a cycle steal basis.

If bit 15 is on, the CA will chain to a receive operation at the completion of the transmit operation. If bit 15 is off, the CA will generate an end op interrupt and return to control mode at the end of the transmit operation.

During transmission, if text mode is entered, the byte counter going to zero will cause an end sequence interrupt request to be generated by the CA. An XIO write command is used to send the desired end control code and upon completion of this command, the chain condition (bit 15), set during the initiate write, will be checked.

Function 110 -- Initiate Read

This function is used to start a receive operation. During execution of this IOCC, the address of the first location of the receive data table is transferred to the read address register (RAR), and the CA is placed in receive mode. The incoming data is monitored for character phase (three consecutive SYN's) and text. Data transfers to main storage will take place on a cycle steal basis via the CA data register. If the adapter does not enter text or header mode operation within 3 seconds, a 3-second error interrupt will occur.

The receive operation can also be entered automatically, after completion of a transmit operation, if chaining was indicated by the previous initiate write command.

Function 111 -- Sense Device

This function is used to sense the device status word (DSW). When this IOCC is executed, any one

of eight 16-bit DSW's is placed in the accumulator. The eight DSW's are:

- Sense status.
- Sense cyclic redundancy check register (CRC).
- Sense read address register (RAR).
- Sense test status.
- Sense write address register (WAR).
- Sense byte counter.
- Sense serializer/deserializer (SERDES) and sequence counter.
- Sense data register.

The particular DSW to be sensed is determined by modifier bits 12 through 14 of the IOCC. Bit 15, if it is on, is used to reset certain status conditions in the sense status DSW. It has no effect when used with any other sense DSW.

Modifiers (Sense Device Command)

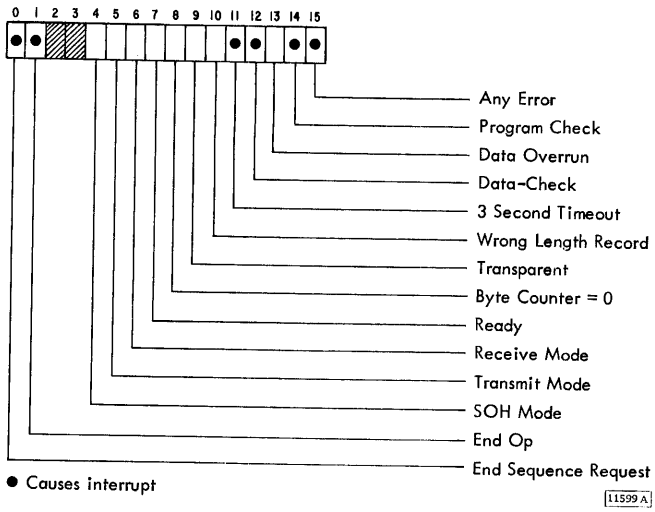
(000) -- Sense Status: Figure 2 illustrates the sense status DSW. A description of the bit conditions follows.

End Sequence Request (Bit 0): When this bit is on, an interrupt is caused, indicating that the CA is in text or header mode and the byte counter is at zero. An XIO write operation must occur within 3 seconds to provide the desired control character for ending transmission, or the 3-second error interrupt will be generated. Bit 0 is reset by modifier Bit 15.

End Op (Bit 1): This bit is turned on and an interrupt is generated when the CA completes a receive mode operation or exits from a transmit operation and no chaining was specified. Can be reset by modifier Bit 15.

SOH (Bit 4): This bit indicates that the CA is performing a header operation. Cannot be reset by modifier Bit 15.

Transmit Mode (Bit 5): When the CA is in transmit mode, bit 5 is on. When the CA is not in transmit mode the bit is off. Cannot be reset by modifier Bit 15.



• Figure 2. Sense Status DSW

Receive Mode (Bit 6): When the CA is in receive mode, bit 6 is on. When the CA is not in receive mode, the bit is off. Cannot be reset by modifier Bit 15.

Ready (Bit 7): When the data set is ready and the CA is in control mode, bit 7 is on. Cannot be reset by modifier Bit 15.

Byte Count Zero (Bit 8): Bit 8 indicates that the byte counter has gone to zero during a transmit or receive operation. Cannot be reset by modifier Bit 15.

Transparent (Bit 9): This bit indicates that the CA is in transparent text mode. Cannot be reset by modifier bit 15. Normal reset state is on (1).

Wrong Length Record (Bit 10): Indicates that the message block received by the CA was too long. Cannot be reset by modifier Bit 15. This bit is reset when receive mode is reset.

Three-Second Time-Out (Bit 11): Indicates that the 3-second time-out has occurred. Examining the bit conditions of the test status DSW will aid in determining which of the following error conditions is present.

1. With receive mode bit on and the text mode bit off, the CA did not enter text mode operation within 3 seconds after beginning a receive operation.

2. With the receive and text mode bits on, and the timefill bit off, the CA did not receive the DLE/SYN sequence within 3 seconds of the previous DLE/SYN while in transparent mode. In nontransparent mode SYN characters must be received within 3 seconds.
3. With the receive mode, text or header mode, and timefill bits on, the CA received more than 3 seconds of timefills.
4. With transmit mode, text or header mode, and timefill bits on, indicates that the end sequence request interrupt did not get serviced and that 3 seconds of timefills has been transmitted. (The XIO write command services the end sequence interrupt.)

Bit 11 can be reset by modifier Bit 15.

Data Check (Bit 12): Indicates that the CA received an end sequence request outside of text mode or that a single DLE, not followed by a control character, was received while the CA was in receive transparent text mode. Bit 12 can be reset by program.

A data check during loop DS test indicates that the data to the data set is different from the data leaving the data set. A data check during loop CA test indicates a problem with SERDES or test SERDES.

Data Overrun (Bit 13): Indicates that a received character was lost within the CA because the CPU did not maintain the speed of the incoming data. Can be reset by modifier Bit 15.

Program Check (Bit 14): Indicates that a programming error has been made. Any of the following errors causes bit 14 to be set on.

1. If WAR or RAR contains an address greater than the size of main storage.
2. If an invalid function code is specified in an IOCC issued to the CA.
3. If an initiate write or initiate read command is issued when the CA is not in control mode.
4. If an initiate read command is issued when the CA is in loop test.
5. If the chain flag bit is set by an initiate write command when the CA is in Loop test. Bit 14 will be set when chaining is attempted to be executed during loop test.
6. If an XIO write instruction is issued when the CA is not in transmit mode or the byte counter is not zero.

Bit 14 can be reset by modifier Bit 15.

Any Error (Bit 15): Bit 15 causes a program interrupt to be generated. It is set by the 3-second timeout, data check, or program check condition. Can be reset by modifier Bit 15.

(001) Sense Cyclic Redundancy Check Register (CRC): Sensing this DSW loads the contents of the CRC register into the accumulator. After receiving a block of text or header, the register should be checked. It will be zero (no error) if the received block check characters are equal to the accumulated block check characters.

(010) Sense Read Address Register (RAR): The contents of the 15-bit RAR are placed into the accumulator, positions 1 through 15. Bit 0 indicates the status of the A/B trigger associated with RAR. If bit 0 is on (1), the last character received is stored in bits 0-7 of the last word transferred to main storage. If bit 0 is off (0), the last character received is stored in bits 8-15 of the last word transferred to main storage.

At the end of a receive operation, RAR is one higher than the main storage address of the last word transferred to storage.

(011) Sense Test Status: This DSW contains various status indicators to be used along with the sense status DSW or for testing the CA operation. The status will not be reset by bit 15 if it is on in the IOCC.

Figure 3 illustrates the test status DSW. Bits have significance only when they are in the on (1) condition. A description of each bit follows.

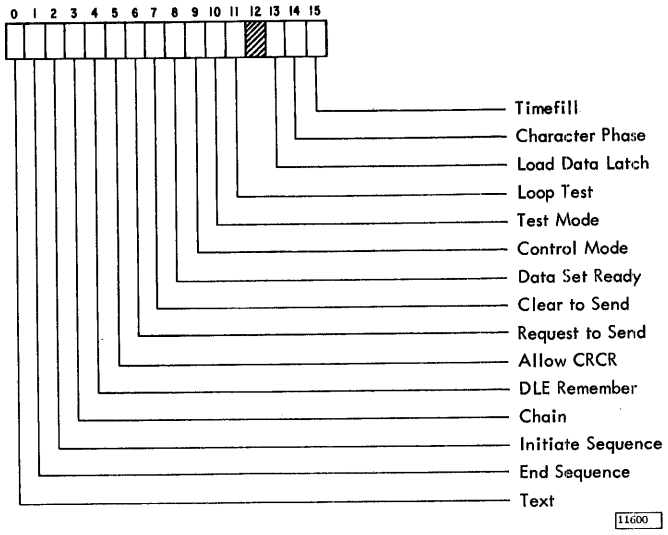


Figure 3. Test Status DSW

Text Mode (Bit 0): The CA is in text mode.

End Sequence (Bit 1): The CA is executing an end sequence operation.

Initiate Sequence (Bit 2): The CA is executing an initiate sequence operation.

Chain (Bit 3): An initiate write command specified chaining and the actual chaining has not taken place.

DLE Remember (Bit 4): Indicates that the previous character received or transmitted was a DLE.

Allow CRCR (Bit 5): The CRCR has been allowed to accumulate.

Request to Send (Bit 6): A request to send signal has been sent to the data station, and the CA is ready to start transmitting.

Clear to Send (Bit 7): The clear-to-send signal has been received from the data station, indicating the station is ready for data transmission. It is the reply to the request-to-send signal.

Data Set Ready (Bit 8): A ready signal has been received from the data station, indicating that the station can receive data from the communications line and, if clear-to-send is also on, can transmit data.

Control Mode (Bit 9): The CA is in control mode.

Test Mode (Bit 10): The CA is in test mode.

Loop Test (Bit 11): The CA is performing a loop test, either loop CA or loop DS.

Load Data Latch (Bit 13): During transmit mode, indicates that the CA data register contains data which has not been sent. In receive mode, indicates that the CA data register contains data which has not been transferred to main storage.

Character Phase (Bit 14): The CA has received two consecutive sync characters in receive mode.

Timefill (Bit 15): The CA is either transmitting or receiving timefills.

(100) Sense Write Address Register (WAR): The contents of the 15-bit WAR are placed into the accumulator, positions 1 through 15. Bit 0 indicates the status of the A/B trigger associated with WAR. If bit 0 is on (1), the last character transmitted came from bit positions 0-7 of the last word transferred from core. If bit 0 is off the last character came from positions 8-15.

(101) Sense Byte Counter Register (BCR):

The contents of the 14-bit BCR are loaded into the accumulator, positions 2 through 15.

(110) Sense Serializer/Deserializer (SERDES) and Sequence Counter: Sensing this DSW places the eight-bit SERDES into accumulator positions 0-7 and the sequence counter into accumulator positions 8-15.

(111) Sense Data Register: The contents of the 16-bit data register are placed into the accumulator.

PROGRAMMING CONSIDERATIONS

General Limitation

The processor and its program control and initiate all operations within the CA and are responsible for:

- Proper sequencing of commands.
- Translation to and from data codes.
- Interpreting sense and status information.
- Initiating and terminating operations.
- Proper message and control format.
- Recognizing all control characters.
- Generating, in the proper sequence, all control characters except sync patterns and additions/deletions of DLE's during a data transfer.

Programming Limitation

These restrictions of the program must also be taken into account.

- When transmitting nontransparent text, a SYN must not be sent from main storage.
- A maximum of 16k bytes may be transmitted or received in any one message block.
- The DLE/STX character must be located in the same main storage data table of a transmit data

block. This character is the start of text for transparent mode transmit message.

Note: When a header message immediately preceeds a DLE/STX sequence, the SOH must be located such that the DLE/STX is located in the same word.

- The receive table should be one word longer than expected by the byte count to provide fail safe protection.

Interrupts

There are three types of interrupts associated with the CA.

- End of operation (end op).
- End of sequence.
- Error.

These interrupts cause bit 10 to set in the interrupt level status (ILSW) on interrupt level 3. The type of interrupt will be stored in the device status word (DSW) (see Figure 2) and occur at the following times:

1. At the completion of an initiate read operation. The end op bit is set in the DSW.
2. At the completion of an initiate write operation if text or header modes were not entered and chaining is not indicated by the initiate write command. The end op bit is set in the DSW.
3. At the completion of an initiate write operation (when the byte counter goes to zero) if text or header modes were not entered. The end op bit will be set in the DSW.
4. At the completion of the XIO write operation, if chaining was not indicated by the initiate write command. An end op bit is set in the DSW.
5. At the completion of a receive operation entered by chaining. The end op bit is set in the DSW.
6. When an error occurs the error interrupt bit associated with the specific error is set in the DSW.

Error Detection

The exposure to errors in a communication network requires adequate error detection and recovery routines. Error detection can be separated into two sections: those detected by circuitry and those detected by program.

Circuit detected errors include:

- Wrong length record.
- Time-out.
- Data check.
- Data overrun.
- Program check.

Program Detected Errors

If program detection of errors is desired, it must be incorporated into the customer program.

Cyclic Redundancy Check

A two-byte (16-bit) checking character is generated by the CRC register, in both transmit and receive modes. These two bytes are the block check characters (BCC) for a transmit text block. Characters outside of text or header modes are not checked.

The cyclic redundancy check uses an arithmetic accumulation that is reset with the first STX or SOH in a transmission block and restarted with the next character in line. Thereafter, any STX or SOH characters received before a line turnaround are included in and do not reset the accumulation. The BCC's are transmitted, automatically, by the CA at the end of a transmit block. The receive station makes a hardware compare with its accumulated BCC's in the CRC register. If the transmit and receive CRC registers agree, a 0 will be in the receive station CRC register.

Sync and timefill characters are not accumulated. Also, within blocks of transparent text (following DLE/STX), the first DLE (data link escape) character in all two-character DLE sequences is excluded from the block check character.

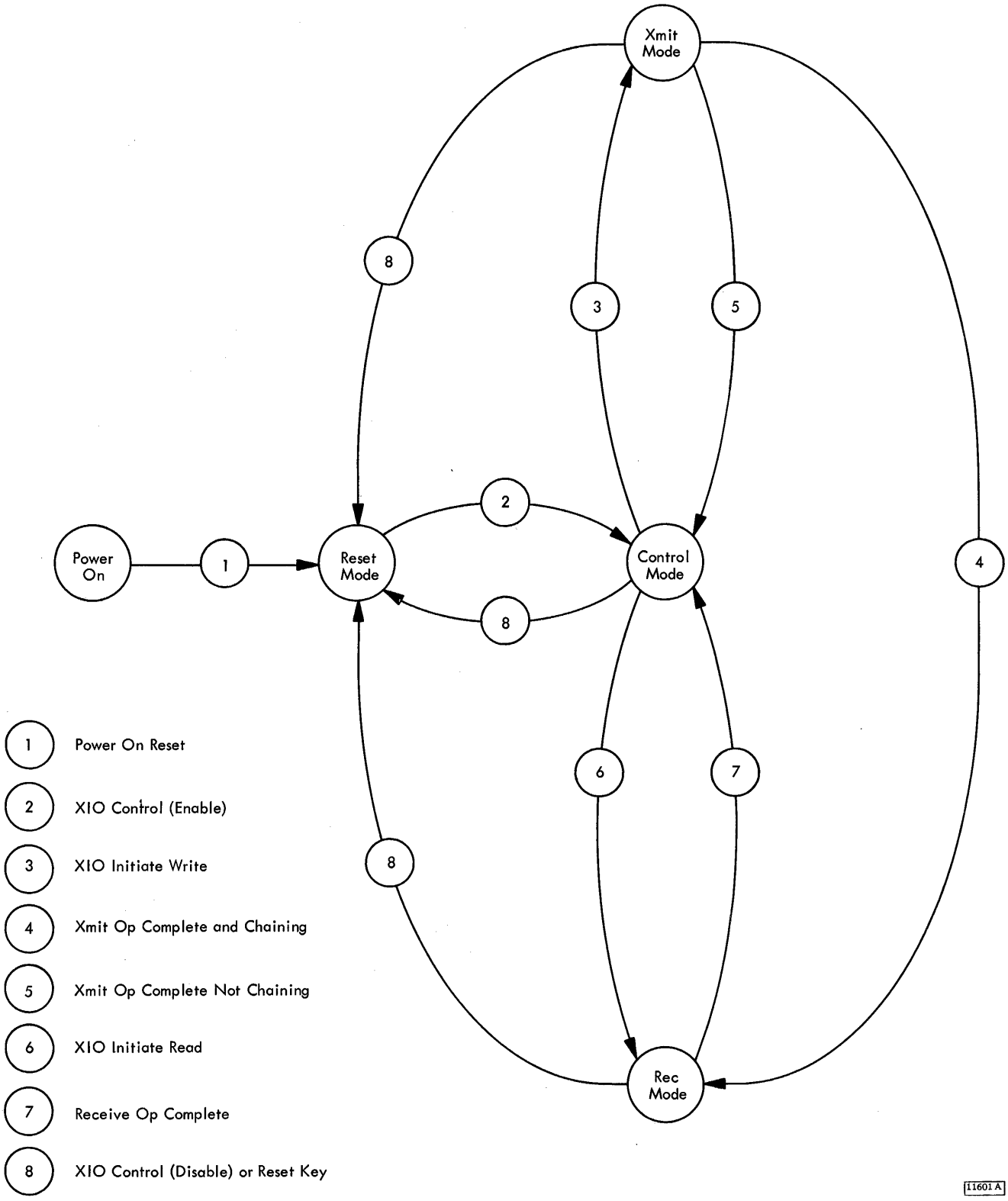
Since this check is made by hardware, it remains a programming responsibility to check the CRC register at the completion of a received block of data to determine if the CRC registers (transmit and receive) agree.

Record Phase Check

The primary responsibility for carrying on a transmission rests with the transmit station. The receive station is responsible for checking the validity of the data it receives and for signaling its status from time to time. The IBM Binary Synchronous Communications, Form A27-3004, defines the proper responses that are required to maintain synchronization and control data transmissions.

MODE AND CONDITION DESCRIPTIONS

The CA is a reciprocating device and operates in a variety of modes. Each mode is conditioned by an XIO command (Refer to Figure 4).



• **Figure 4.** Operational Modes

Reset Mode

When in this mode the CA is disabled and cannot operate. It is entered in any one of three ways:

1. Initial power on of the system, controlled from the 1131 or the 1133.
2. The reset key on the 1131 console.
3. Programming an XIO disable command.

Reset mode is exited by programming an XIO enable command.

Control Mode

The CA is placed in control mode with the execution of an enable XIO command. In this mode, the CA is ready to transmit or receive data, but neither is in progress.

> Note: Although the CA may be ready to transmit or receive, these actions cannot be started if the data set is not ready.

Control mode is exited when the CA enters transmit or receive mode. Reentry to control mode is either of two ways: at the end of the receive mode or at the end of a transmit mode if chaining to a receive operation was not specified. Control mode is also exited by programming a disable (reset) XIO command.

Transmit Mode

Transmit mode is entered by an XIO initiate write command after the CA has been placed in control mode. Transmit mode may be exited in any one of three ways:

1. When chaining occurs.
2. When the end op interrupt occurs, following an initiate write command with no chaining.
3. When the CA is set to reset mode.

When in transmit mode the CA is in the act of transmitting to the data set, initiating a transmit to the data set, or stopped in an error situation which occurred in transmit mode. Also, the CA enters loop tests to check the transmit mode after an XIO initiate write command is issued.

Receive Mode

Receive mode is entered by an XIO initiate read command or by chaining from a transmit operation. Receive mode may be exited in one of two ways:

1. When an end op interrupt occurs following an initiate write command with chaining, or following an initiate read command.
2. When the CA is set to reset mode.

When in receive mode, the CA is either in the act of receiving from the data set, initiating a receive from the data set, or stopped in an error situation which occurred in receive mode.

Test Mode

Test mode allows the CPU to test the CA without transmitting or receiving messages from the remote station. It is used in conjunction with the diagnostic function tests (DFT's) for the CA to aid in maintaining the adapter.

Test mode is entered with an XIO control command and can only be exited by placing the CA in reset mode.

Loop Test

Loop tests allow for testing and checking transmitted data to and from the data set. Loop test is entered with an XIO control Command. The CA exits loop test when it is placed in reset mode.

The data set loop test only tests the data set. It does not verify proper transmission lines.

Initiate Sequence Condition

The CA starts an initiate sequence during an initiate write or initiate read or when chaining occurs at the end of transmit. In the initiate sequence condition, the CA performs a routine or checks to see that a sequence of events occurs to either start transmitting or receiving data.

Transmit Mode: The initiate sequence condition will be exited after a minimum of three SYN characters have been sent and the data register is loaded with the first data to be transmitted.

Receive Mode: The initiate sequence condition will be exited with the decode of the first non-SYN character after two consecutive SYN's have been received and decoded.

Initiate sequence condition can also be exited by the CA being set to reset mode.

Transmit Initiate Sequence

The CA is conditioned to start transmission. The data set must be checked for the "clear to send" signal; then three SYN characters must be transmitted to the data set. The data register is loaded with two bytes of data, and the byte count is placed in the

BCR to indicate how many cycle steals will be required. The read address register is loaded with the first address of the receive data table. This loading stores the answer to the transmission without the need of an initiate read command since the CA is able to chain directly to receive mode.

Receive Initiate Sequence

The expected byte count is placed in the byte counter register, and character phase must be established during the receive initiate sequence.

End Sequence Condition

The end sequence condition can occur for either the transmit or receive modes. When the CA is in transmit mode, an XIO write command causes the CA to start an end sequence which will result in the transmission of the ending control character. The block check characters are then sent, provided the end control character was not a ENQ or DLE/ENQ if in transparent text mode. The exit from the end sequence is by two different ways:

1. If the XIO write command specifies ENQ or DLE/ENQ for transparent text mode, the end sequence exit will occur when the transmission of ENQ, to the data set, is almost completed and just before the pad character is sent.
2. If the XIO write command specifies ETB or ETX (DLE/ETB or DLE/ETX for transparent text mode), the end sequence exit will occur when the transmission of the second BCC, to the data set, is almost completed and just before the pad character is sent.

   Note: If the XIO write instruction does not specify an end character, the end sequence will still be exited as though a ETB or ETX (DLE/ETB or DLE/ETX for transparent text mode) were sent.

In receive mode, the end sequence is entered when ETX or ETB (DLE/ETX or DLE/ETB for transparent text mode) has been decoded and will be exited when the block check characters are received.

Chaining

When chaining is specified by an initiate write command, the CA automatically enters receive mode immediately after a transmit mode. This is necessary because of the rapid turnaround times possible with the available data rates.

Header and Text Modes

Message blocks handled by the CA may be comprised of header and/or text information. In addition, text data may be in nontransparent or transparent form. The CA is conditioned for header and text modes when control characters for these modes are decoded in the data stream.

Text Mode -- Nontransparent

Text mode may be entered when the CA is in receive or transmit mode, after an STX (start of text) is decoded. It indicates that the CA is in the act of receiving or sending a block of text. All control characters decoded in the data stream will be treated as control characters except the DLE (data link escape). In this mode, the DLE character will not be stripped from data when transmitting or receiving. Timefills in this mode are the SYN character, and this will be stripped from the data when the CA is in receive mode.

An end control character received in the receive mode will cause the CA to leave text mode and end the operation after the BCC's are received. The execution of the XIO write command (send end sequence) controls the exit from text mode during transmission.

Text Mode -- Transparent

The CA enters transparent text mode following a DLE/STX sequence. Control characters may be used as data in this mode and are only recognized as control characters when they are prefixed with the DLE character. Normally, when the CA is in transmit mode, the DLE character is placed with the data in the transmit data table except for the following:

- When there is no character (data or control) to be transmitted, the CA will insert the timefill sequence. DLE/SYN is used as a timefill for transparent text mode.
- The CA automatically inserts a timefill into the data stream. Therefore, the DLE/SYN sequence must not be placed in transparent text by the program as a timefill.
- A DLE/SYN will be inserted, by the CA, between the completion of an initiate write command and the XIO write command.
- The CA will insert a DLE into the data stream following each transparent text DLE received from main storage.

The XIO write command (send end sequence) controls the exit from transparent text mode during transmission.

In receive mode, the CA will remove and prevent the transfer to storage of each of the DLE/SYN sequences inserted as timefills and the DLE that follows a transparent text DLE. A DLE followed by and end control character will cause the CA to leave transparent text mode and end the operation after the BCC's have been received.

An exit from transparent text mode will also occur when the CA is set to reset mode.

Header Mode

The CA enters header mode following the decode of SOH (start of header), if the CA is not already in text mode. In this mode the DLE is treated as any other data character except when it is immediately followed with an STX. The DLE/STX sequence will cause the CA to leave header mode and enter transparent text mode. If STX alone is decoded, when the CA is in header mode, the CA then enters text mode (nontransparent).

The SYN character is used as a timefill during header mode. If the CA is in transmit mode, timefills will be inserted; if the CA is in receive mode, timefills will be stripped from the data stream.

Time-Out

Time-outs establish a time for each operation, within which certain operations are required or expected to occur. Because of bi-sync requirements in different situations, two time-outs have been established for transmit and receive modes:

- 1 (-0.25; + 0.25) second
- 3 (-0.40; + 0.90) second

Transmit Time-Out

There are two types of time-outs in transmit mode:

One-Second Time-Out: During transmission, the CA will generate a timefill every second as a result of this timeout.

Three-Second Time-Out: After the transmission of a block of text, the byte counter goes to zero, timefills are generated by the CA, and this time-out begins. The XIO write command to send the end sequence must be accepted within 3 seconds or a 3-second error will occur.

Receive Time-Out

If a normal operation does not take place for the following conditions, the 3 second time-out will occur.

1. After receive mode has been entered, the CA must either enter text or header mode or end the operation within 3 seconds.
2. During receive mode, text or header, no more than 3 seconds of timefills may be received without receiving a data character.

Timefill

The CA provides for the insertion of timefills to maintain character phase and continuity with the receive station. The SYN character is used as a timefill for text and header modes, but for transparent text the DLE/SYN sequence is used. The timefill character is separate from data and is not accumulated in the CRC register.

In addition to the timefills generated by the 1-second timeout, other timefills are generated by the CA.

Transmit Timefill

Outside of text mode, the CA inserts a timefill in the transmitted data when the CPU does not supply a character for transmission. In text mode, a timefill is inserted when the CPU does not supply a character for transmission and between the completion of the initiate write and the beginning of the XIO write commands.

Receive Mode Timefills

All SYN and timefill characters will be stripped from the received message and will not be transferred to main storage. No programming is required.

TRANSMIT OPERATION

A typical transmit operation is illustrated in Figure 5. This could be a "bid" for the line or transmission of a block of data or even an acknowledgment to a transmission of a remote station.

① During the execution of the XIO initiate write, the CA is set to transmit mode and the write address register is loaded with the first address of the transmit data table.

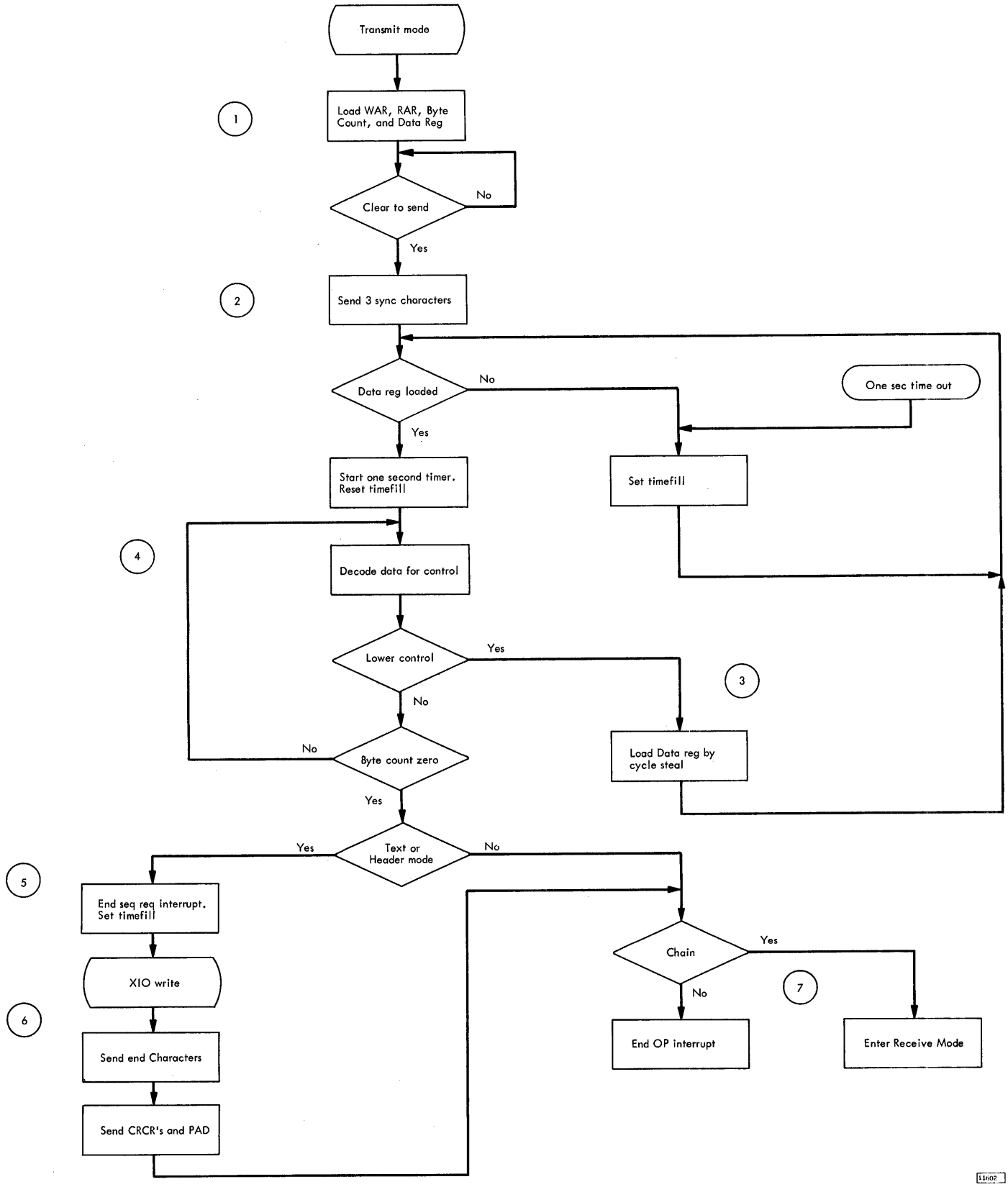


Figure 5. Transmit Operation

② The read address register and the byte counter are loaded by cycle steals from the transmit data table in main storage. The third cycle steal loads the data register with two bytes of data, and the CA generates and transmits three SYN characters.

③ Data is brought from core by cycle steals and transmission continues as long as the byte count is not zero. The data determines when the CA enters header, text, or transparent text modes.

④ The accumulation of the CRC register is determined for each block of data transmitted. The CRC register is reset by the first SOH or STX in a transmission block and restarted with the following character. Control characters, if they occur before line turnaround, are considered data and included in the CRC accumulation. Timefills are not included in the CRC count.

⑤ If text mode is entered, when the byte count goes to zero the CA will start sending timefills and set an end sequence interrupt. If text mode is not entered, the byte count going to zero causes the pad to be sent and the transmit operation to end.

⑥ The end sequence interrupt must be serviced before the 3-second time-out. An XIO sense DSW determines the type of interrupt, and the XIO write command will then cause the CA to end the transmit operation by transmitting the end character, the block check characters, and the pad.

⑦ With the transmit operation ended, the CA either chains to a receive operation or sets a program interrupt (end op) and returns to control mode.

RECEIVE OPERATION

The illustration of a receive operation is shown in Figure 6. Once the CA is placed in control mode the receive operation can be entered by an XIO initiate read command or when chaining from a previous transmit operation.

① When receive mode is entered, the CA will cycle steal the byte count from the receive data table and start monitoring the incoming data for two consecutive SYN characters to establish character phase. (All SYN characters received outside of text mode are deleted from data transferred to main storage.)

② After character phase has been established, the incoming data is decoded and the CA enters the mode of operation determined by the decode. An SOH will place the CA in header mode, and an STX will place the CA in text mode. If text or header modes is not entered and the byte count goes to zero, an end operation interrupt is generated and the CA returns to control mode. The decode of a ENQ also generates an end operation interrupt and causes the CA to return to control mode.

③ In text mode the CA will transfer data to core by cycle steals. Data transfers occur as long as the byte count does not equal zero or until an end character is received. The receive CRC accumulation is reset by the first SOH or STX in a receive block of data and restarted with the following character. Any control characters that follow, if they occur before line turnaround, are included in the CRC accumulation except for timefills. In transparent text the first DLE of a double DLE sequence (DLE DLE) is not accumulated in the CRC count or transferred to main storage.

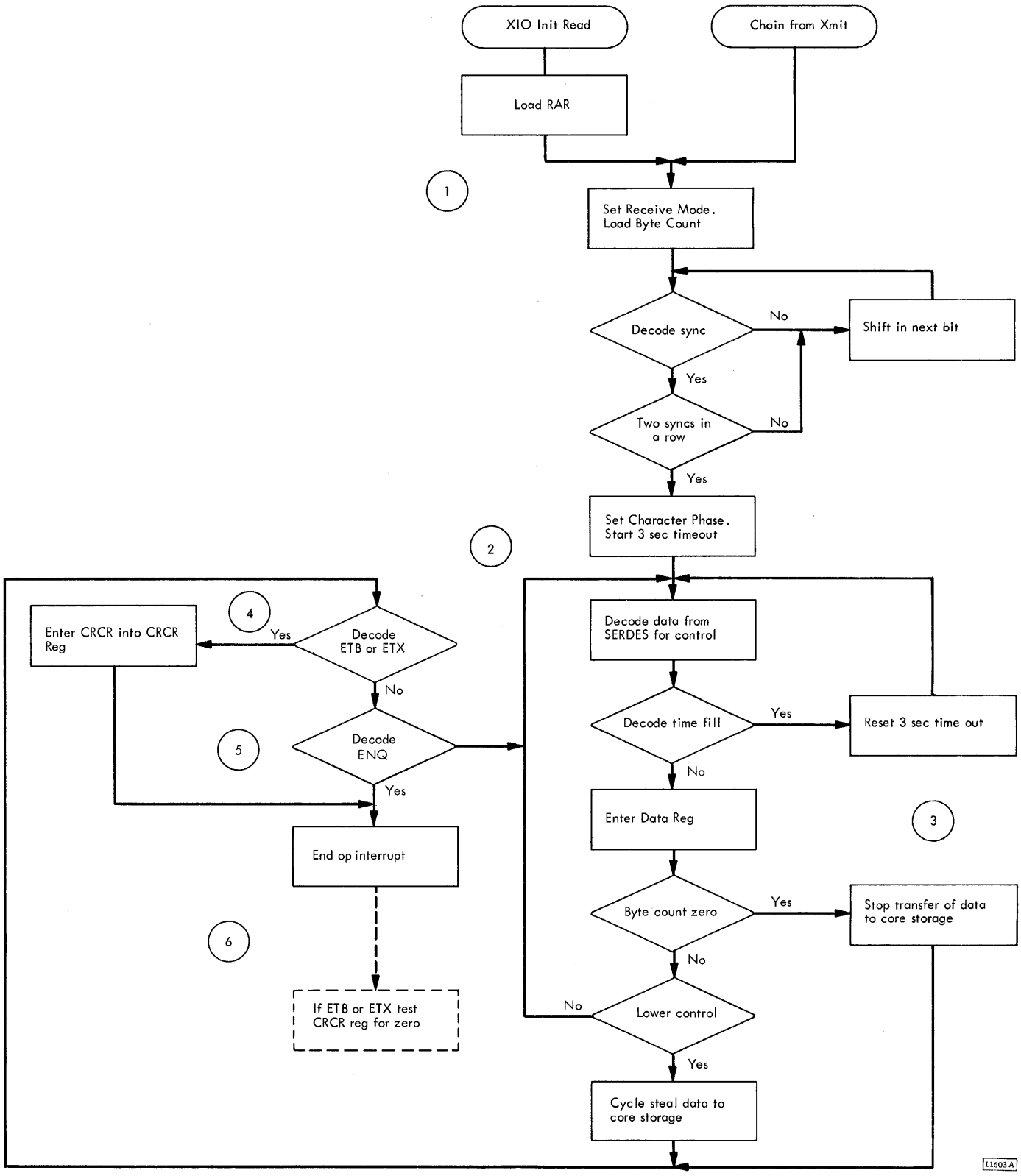
④ A normal end sequence for text mode is the ETX or ETB and signifies that the next two characters are the block check characters. The CA receives the BCC's and ends the operation.

⑤ A ENQ received in text mode will end the operation without receiving the BCC's. This indicates a "disregard this block of data" to the program.

⑥ With the receive operation ended, the CA sets a program interrupt (end op) and returns to control mode.

BI-SYNC MESSAGE EVENTS

A general "talk and listen" session for two stations appears in Figure 7. Station A has data to send so it bids for the line. Station B acknowledges that it is ready to receive, and the link is established. Data transfers take place, and A receives assurances from B that the data has been received correctly except for one instance. Station B rejects one



• Figure 6. Receive Operation

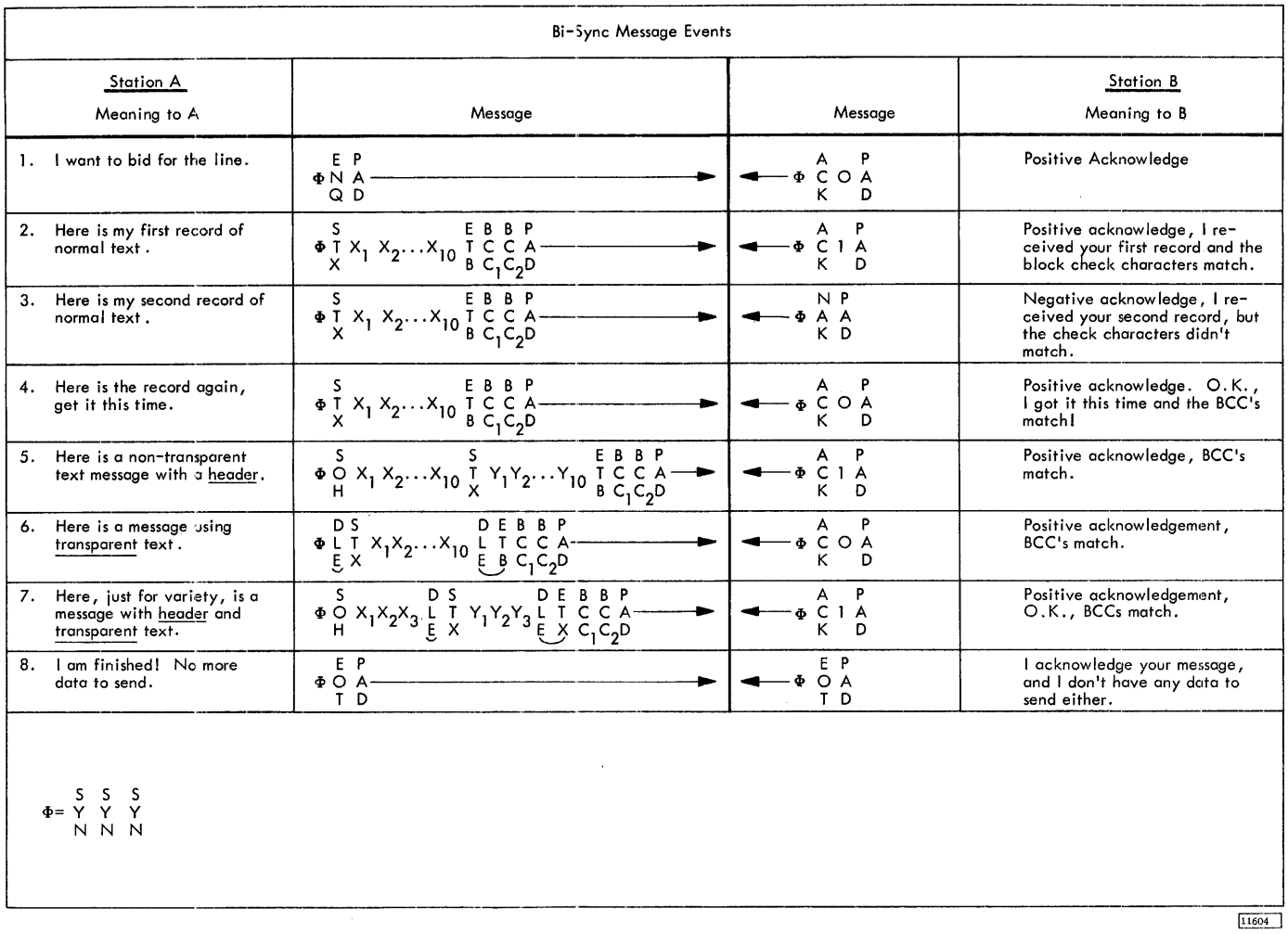


Figure 7. Bi-sync Message Events

message because of unequal cyclic redundancy check characters. Station A then retransmits the message to B.

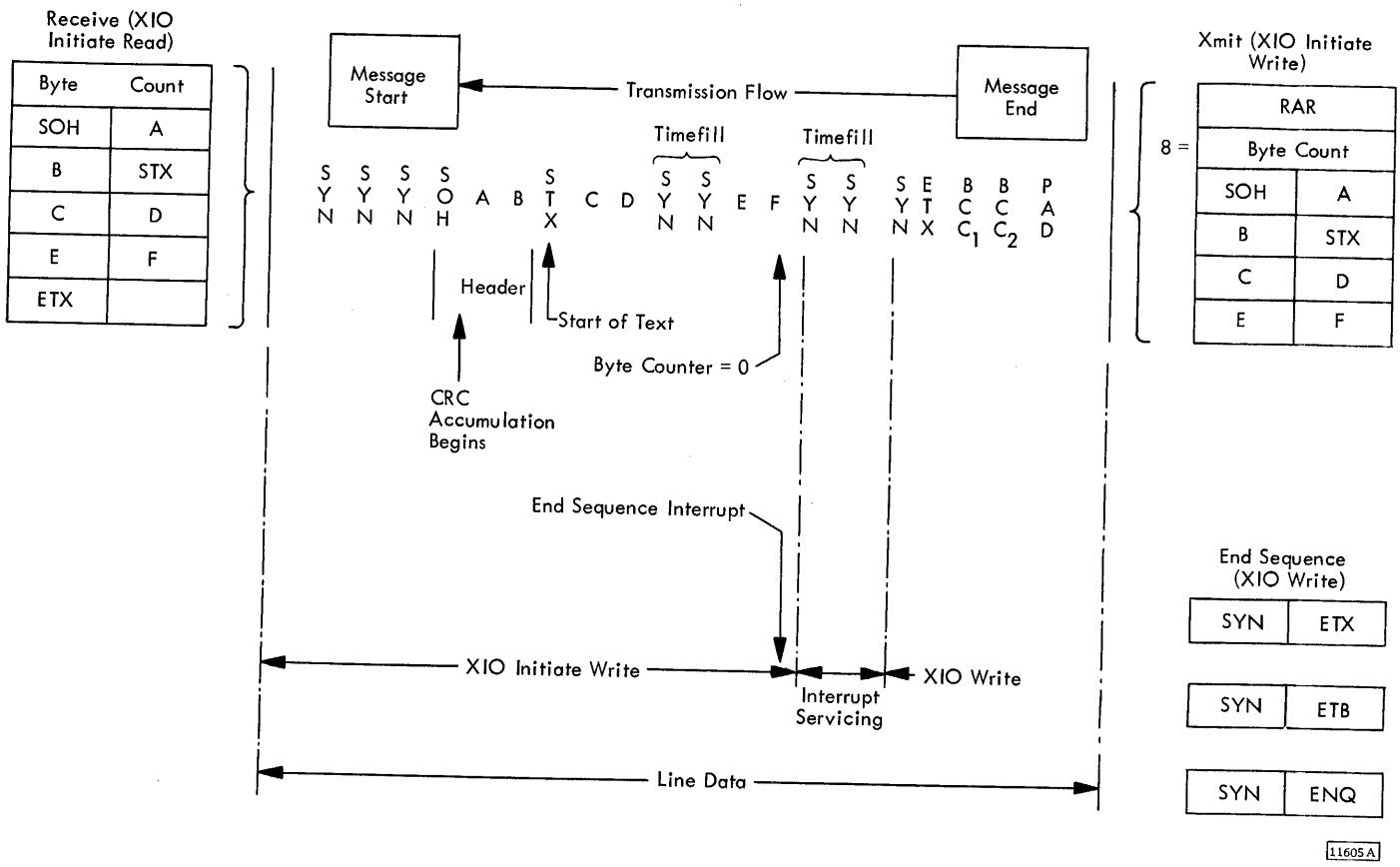
An end is signaled by station A. Since station B has no data for A, it concludes the link by responding with an end character also.

MAIN STORAGE DATA TABLES

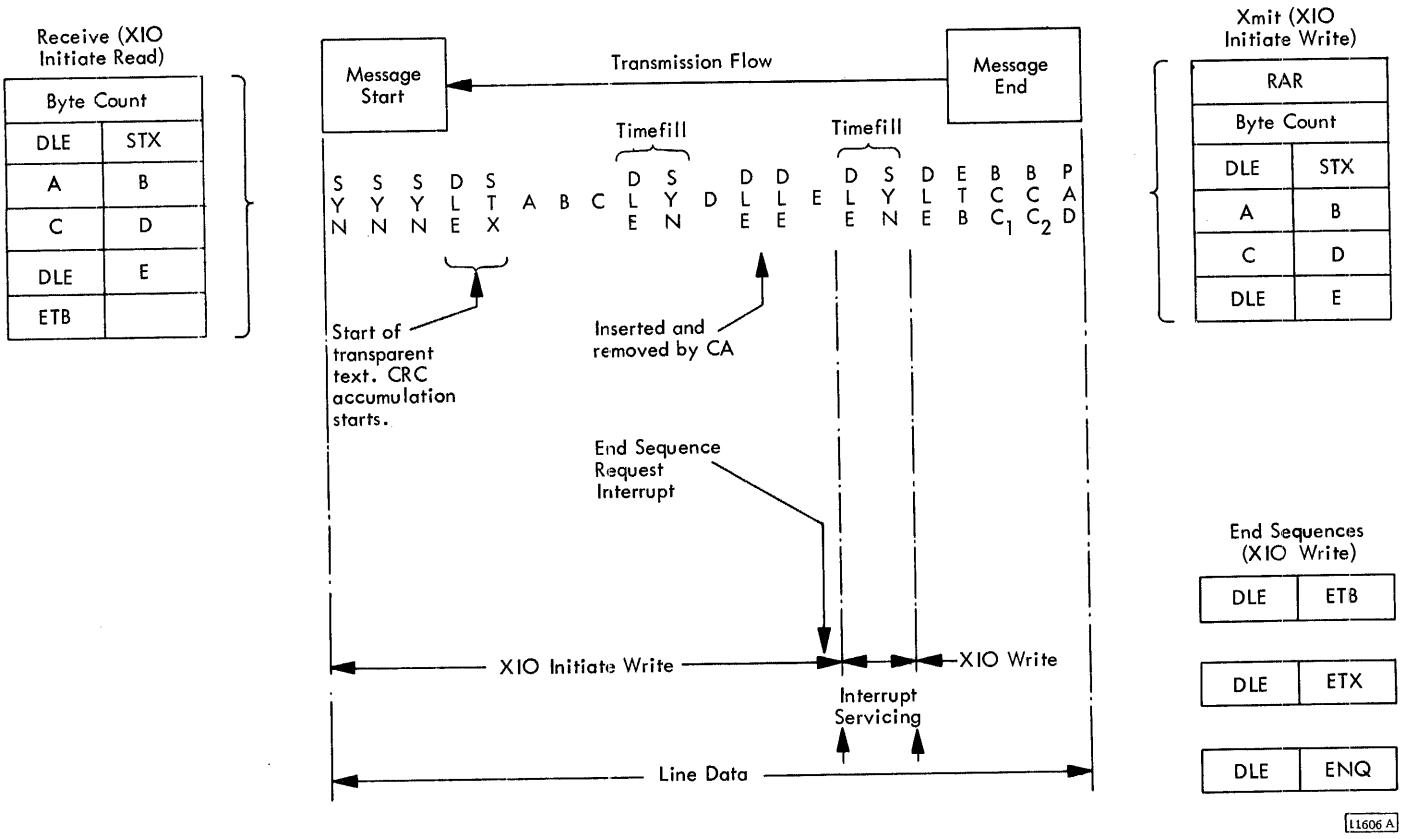
The transmit and receive data tables, as they are constructed in main storage, are shown in Figures 8 and 9. Figure 8 illustrates the data tables for a message containing header and normal text. The data is presented to the line in serialized format, character by character, as it is sent to the receive station.

Figure 9 illustrates the data tables of a message composed for transparent text.

The end sequence characters also reside in main storage and are sent by the XIO write command.



• Figure 8. Main Storage Tables: Normal Text Mode



• Figure 9. Main Storage Tables: Transparent Text Mode

Input/Output - Control Commands (IOCC)	Device Code	Function Code	Modifier Bits	Hexadecimal Value
	0 1 2 3 4	5 6 7	8 9 10 11 12 13 14 15	
High Speed CA	1 1 1 0 0		0 1	
XIO Write		0 0 1		XXXXE140
Initiate Write				
Without Chaining		1 0 1	0	XXXXE540
With Chaining		1 0 1	1	XXXXE541
Initiate Read		1 1 0		XXXXE640
Control				
Test Mode		1 0 0	0 0 1	E442
Loop CA Test		1 0 0	0 1 0 0	E444
Loop DS Test		1 0 0	0 1 0 1	E445
Disable		1 0 0	0 1 1	E446
Advance Test Clock				
SPACE Simulation		1 0 0	0 1 0 0	E448
MARK Simulation		1 0 0	1 1 0 0	E468
Sense Device (DSW)				
Sense Status				
Without Reset		1 1 1	0 0 0 0	E740
With Reset		1 1 1	0 0 0 1	E741
Sense CRCR		1 1 1	0 0 1	E742
Sense RAR		1 1 1	0 1 0	E744
Sense Test Status		1 1 1	0 1 1	E746
Sense WAR		1 1 1	1 0 0	E748
Sense Byte Counter		1 1 1	1 0 1	E74A
Sense SERDES/Sequence Ctr.		1 1 1	1 1 0	E74C
Sense Data Register		1 1 1	1 1 1	E74E
Sense Interrupt (ILSW)		0 1 1		0300

Shaded areas are reserved. Hexadecimal values were developed assuming all reserved modifiers to be zero.

X - Address word not shown. Contains the address of first main storage location used by the Command.

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