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# 1620 Data Processing System, Model 1

## 1620 Central Processing Unit, Model 1

This edition, Form 227-5751-1 is a merge of Form 227-5751-0 and its supplement, Form S27-5850-0.

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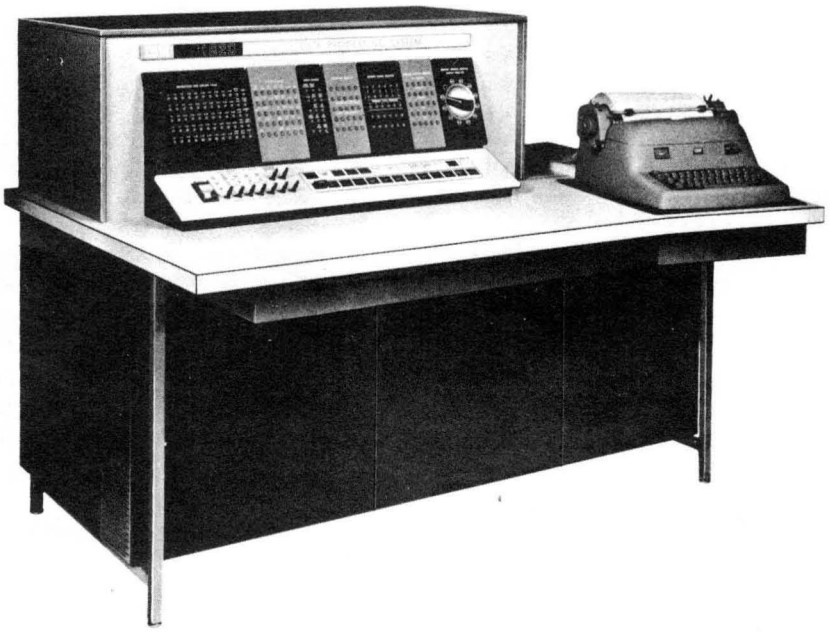
CONTENTS

## PREFACE

This manual, Form 227-5751, describes the IBM 1620 Data Processing System, Model 1 (1620-1), Serial 11550 and up. This manual replaces but does not make obsolete, Form 227-5647-0. Form 227-5647-0 describes the 1620-1 Data Processing System, Serial 10701 to 11550. Additional features associated with the 1620-1 are described in separate Customer Engineering Manuals of Instruction. See Appendix H, Bibliography.

Customer Engineering Instructional System Diagrams for the 1620-1 Data Processing System (including additional features) are in three volumes, (Forms 227-5769, 227-5770, and 227-5771). In addition to the system diagrams, Form 227-5769 contains function charts for the basic 1620-1 features. Form 227-5771 contains function charts of the additional features as well as the system diagrams. Form 227-5770 contains system diagrams only.



## DESCRIPTION OF SYSTEM

The IBM 1620 Data Processing System is an electronic computer system designed for scientific and technological applications. The use of solid state circuit components and the availability of an additional 20,000 or 40,000 positions of core storage to augment the 20,000 positions in the 1620 Model 1 Processing Unit, provides the 1620 System with the capacity, reliability, and speed to solve problems that heretofore have required larger and more expensive data processing systems.

This manual, Form 227-5751, describes the 1620 Model 1 Central Processing Unit with no additional features attached or installed. Additional features available for installation in, or attachment to, the 1620 Central Processing Unit are described in separate Customer Engineering Manuals of Instruction. See Appendix H, Bibliography.

Data and instructions entered into the system are placed in memory as decimal digits. Each of the 20,000 positions of core storage (memory) can be addressed individually by a 5-digit address and can store one digit of information. Memory addresses extend from 00000 to 19999. The addressing system provides for the selection of any digit or group of digits within memory. The 1620 Computer processes numerical, alphabetic and special characters.

The computer is capable of performing more than 30 different standard operations with over 14 special feature operations available. Each operation is specified by a 12-digit instruction which contains a 2-digit operation code and two 5-digit addresses. Instructions comprising a program are normally stored in consecutive locations in memory and executed sequentially. However, the sequence of operations may be altered at any point in the program by conditional branch instructions. Conditional branch instructions make logical decisions by performing tests on indicators or switches set by the computer or the operator.

Arithmetic operations are accomplished by a table addressing method. There are 320 positions of memory assigned for use in arithmetic operations. Of these, 20 positions, 00080 through 00099, are used to store products or quotients, and 200 positions, 00100 through 00299, are assigned for the storage of a Multiply Table. The Multiply Table contains all possible 2-digit products. The remaining 100 positions, 00300 through 00399, are assigned for storage of an Add Table used in all arithmetic operations. The Add Table contains all possible 2-digit sums, with carries indicated. The memory positions containing the table data are addressable.

The 1620 is a variable field length computer. The shortest admissible field is two digits; the longest can be any number of digits within the capacity of memory. Accuracy of data is ensured by the parity check which is made when the data enters, exits, or is manipulated inside the system.

The Console of the 1620 consists of control keys, switches, an indicator panel, and a typewriter. The control keys and switches are used to control operation of the system. The console panel provides a visual indication of the contents of various registers and the status of control circuitry within the computer. The typewriter keyboard is used for manual entry of data and instructions into memory.

Information is entered into the system by the typewriter or by additional feature input or input-output devices. Output data is recorded by the typewriter or by additional feature output or input-output devices.

When the computer is reading from or writing on an input-output device and is in the numerical mode, each character received from or sent to the input-output device is represented in memory as a single digit and occupies one memory position. In the numerical mode, data must consist of numerical characters only. When the computer is reading from or writing on an input-output device and is in the alphameric mode, each character received from or sent to the input-output device is represented in memory as two digits occupying two adjacent memory positions. In the alphameric mode, data may consist of numerical, alphabetic, and special characters. The digits for numerical characters, in the alphameric mode, consist of an arbitrarily assigned digit (zone digit) and a second digit (numerical digit) represented by two arbitrarily assigned digits.

Figures 1-1 and 1-2 illustrate all characters and their assigned digital values for both numerical and alphameric modes.

| Character | Input | Core Storage | | Output |
|---|---|---|---|---|
| | Typewriter | Zone | Num | Typewriter |
| (Blank) | (Space) | | C | 0 |
| 0 (+) | 0 | | C | 0 |
| 0 (-) | $\bar{0}$ | | F | 0 |
| 1-9 (+) | 1-9 | | 1-9 | 1-9 |
| 1-9 (-) | $\bar{1}$-$\bar{9}$ | | F, 1-9 | 1-9 |
| ≠ | ≠ | | C82 | ≠ (Stop, WN) (DN) |
| $\bar{\neq}$ | $\bar{\neq}$ | | F82 | $\bar{\neq}$ |
| Num Blank | @ | | C84 | @ |

Figure 1-1. Character Coding, Numerical

| Character | Input | Core Storage | | Output |
|---|---|---|---|---|
| | Typewriter | Zone | Num | Typewriter |
| (Blank) | (Space) | C | C | (Space) |
| . (Period) | . | C | 3 | . |
| ) | ) | C | 4 | ) |
| + | + | 1 | C | + |
| $ | $ | 1 | 3 | $ |
| * | * | 1 | 4 | * |
| - (Hyphen) | - | 2 | C | - |
| / | / | 2 | 1 | / |
| , (Comma) | , | 2 | 3 | , |
| ( | ( | 2 | 4 | ( |
| = | = | 3 | 3 | = |
| @ | @ | 3 | 4 | @ |
| A-I | A-I | 4 | 1-9 | A-I |
| 0 (—) | (None) | 5 | C | - (Hyphen) |
| J-R | J-R | 5 | 1-9 | J-R |
| 1-9 (—) | J-R | 5 | 1-9 | J-R |
| S-Z | S-Z | 6 | 2-9 | S-Z |
| 0 (+) | 0 | 7 | C | 0 |
| 1-9 (+) | 1-9 | 7 | 1-9 | 1-9 |
| ≠ | ≠ | C | C82 | (Stop) |

Figure 1-2. Character Coding, Alphamerical

## MACHINE LANGUAGE

### Character Code

All data stored, transferred, and processed within the computer is represented as decimal digits in Binary Coded Decimal (BCD) form. A digit is represented by a particular combination of bits. The bit positions of each digit consist of four numerical bits (8, 4, 2, and 1), one flag (F) bit, and one check (C) bit (Figure 1-3). The value of a significant digit is the sum represented by the bits present in the 8, 4, 2, and 1 numerical bit positions. A zero is represented by a C-bit alone. Only bit combinations whose sum is nine or less are used. Considering only the numerical bit positions, the digit-6 is represented by a 4-bit and a 2-bit; the digit-7 by a 4-bit, a 2-bit, and a 1-bit; and the digit-8 by an 8-bit alone (Figure 1-4).

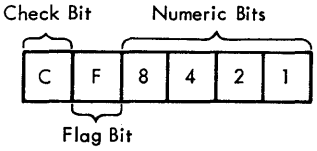



Figure 1-3. Bit Positions

| | C | F | 8 | 4 | 2 | 1 |
|---|---|---|---|---|---|---|
| 0 | X | | | | | |
| 1 | | | | | | X |
| 2 | | | | | X | |
| 3 | X | | | | X | X |
| 4 | | | | X | | |
| 5 | X | | | X | | X |
| 6 | X | | | X | X | |
| 7 | | | | X | X | X |
| 8 | | | X | | | |
| 9 | X | | X | | | X |

Figure 1-4. Bit Configuration - Decimal Digits 0-9

The flag (F) bit is used in three ways. The presence or absence of the flag bit in the units position of a numerical field determines the sign of the field. Absence of the flag bit is interpreted as a

field signed plus. The presence of the flag bit is interpreted as a field signed minus. The flag bit is also used as a field mark defining the high-order position of a numerical field. A flag bit with a digit of the Add Table indicates a carry in arithmetic operations.

The C-bit is used for parity checking purposes. Each digit within the computer must consist of an odd total number of bits, or a parity error will be indicated. The C-bit will be present in a digit when the number of bits present in the numerical bit positions and the F-bit position consists of an even number of bits.

A special combination consisting of the C-bit, 8-bit, and 2-bit is used as a record mark.

## Instruction Format

The IBM 1620 uses a 12-digit instruction divided into three parts; a 2-digit operation code, a 5-digit "P-part," and a 5-digit "Q-part" (Figure 1-5).

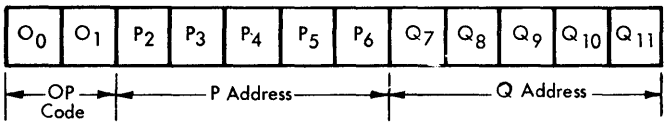



Figure 1-5. Instruction Format

The operation codes consist of two digits (00 through 99) which specify the operation to be performed. Figure 1-6 is a chart of operation codes and their associated mnemonics.

The functions of the P and Q-parts of an instruction are dependent upon the particular operation to be performed. The P-part of an instruction can represent the address in memory of a digit, a field, a record, or another instruction. The Q-part can represent the address in memory of a digit, field, or record; a data field itself; the "address" of an input-output device; the control function to be performed by an input-output device together with the "address" of the device; or the code for a switch or indicator. The specific use of the P and Q-parts will be described with each operation.

## Data Format

Data is stored in memory to form fields or records that can be of any length within the capacity of memory. Data can be classified as digits, fields or records depending upon how they are addressed and the limiting factor of the data.

A digit occupies one memory position and is addressed individually.

Fields in memory consist of a number of consecutive digits and are composed of data related to arithmetic operations and internal field transmission. A field is addressed by its rightmost (low-order) position which occupies the highest numbered memory position of the field. Fields are processed from right to left into successively lower memory positions until a digit with a flag bit is sensed. The shortest admissible field consists of two digits, the addressed digit and the adjacent digit containing the field definition flag bit. Numerical fields are signed minus by a flag bit present in the units position. The absence of a

| Arithmetic Instructions: | MNEMONIC | CODE |
|---|---|---|
| Add | A | 21 |
| Add Immediate | AM | 11 |
| Subtract | S | 22 |
| Subtract Immediate | SM | 12 |
| Compare | C | 24 |
| Compare Immediate | CM | 14 |
| Multiply | M | 23 |
| Multiply Immediate | MM | 13 |
| **Internal Data Transmission Instructions:** | | |
| Transmit Digit | TD | 25 |
| Transmit Digit Immediate | TDM | 15 |
| Transmit Field | TF | 26 |
| Transmit Field Immediate | TFM | 16 |
| Transmit Record | TR | 31 |
| **Branch Instructions:** | | |
| Branch | B | 49 |
| Branch No Flag | BNF | 44 |
| Branch No Record Mark | BNR | 45 |
| Branch On Digit | BD | 43 |
| Branch Indicator | BI | 46 |
| Branch No Indicator | BNI | 47 |
| Branch and Transmit | BT | 27 |
| Branch and Transmit Immediate | BTM | 17 |
| Branch Back | BB | 42 |
| **Input-Output Instructions:** | | |
| Read Numerically | RN | 36 |
| Write Numerically | WN | 38 |
| Dump Numerically | DN | 35 |
| Read Alphamerically | RA | 37 |
| Write Alphamerically | WA | 39 |
| Control | K | 34 |
| **Miscellaneous Instructions:** | | |
| Set Flag | SF | 32 |
| Clear Flag | CF | 33 |
| Halt | H | 48 |
| No Operation | NOP | 41 |

Figure 1-6. Operation Codes and Mnemonics

flag bit in the units position is interpreted as a field signed plus.

A record in memory consists of a field or fields of data related to input-output operations and internal record transmission. A record in memory is addressed at the leftmost (high-order) position, which occupies the lowest numbered memory position of the record. Records are processed serially from left to right into successively higher memory positions. Output and internal record transmission operations are terminated whenever a record mark is sensed. For memory to receive a record, data is entered starting at the addressed position and continuing from left to right into successively higher memory locations until terminated by an end-of-record signal from the input unit.

## STORED PROGRAM CONCEPT

To solve a problem or to process data, a programmer selects from the different operations which the system is capable of performing, those which are required to accomplish the desired results. The series of instructions which designate the operations to be performed is called a program. Because the instructions comprising a program are written into memory from an input device and read from memory for interpretation and execution, the 1620 is called a stored program computer.

For interpretation by the computer, an instruction must be read from memory to registers, starting with the high-order digit and continuing through successively higher memory locations until all 12 digits have been read.

Instructions within a program are normally interpreted and executed sequentially; that is, execution of the first instruction is followed by interpretation and execution of the second instruction, etc. (Figure 1-7). However, this sequence can be altered by the use of conditional branch instructions that direct the computer to an instruction located at other than the next sequential position.

Additional instructions and/or data may be inserted into memory from an input device during the solution of a problem.

The only distinction between instructions and data, in memory, is the manner in which they are interpreted by the computer. If for any reason data was placed in memory locations assigned to instructions, the data would be acted upon as instructions. Conversely, the operation code or either address part of an instruction may be modified by treating the instruction parts as data. Flag bits may be stored with the digits of an instruction to permit operation on the instruction as data. The flag bits are ignored during interpretation of the instruction except when Indirect Addressing, an additional feature, is installed in the 1620.

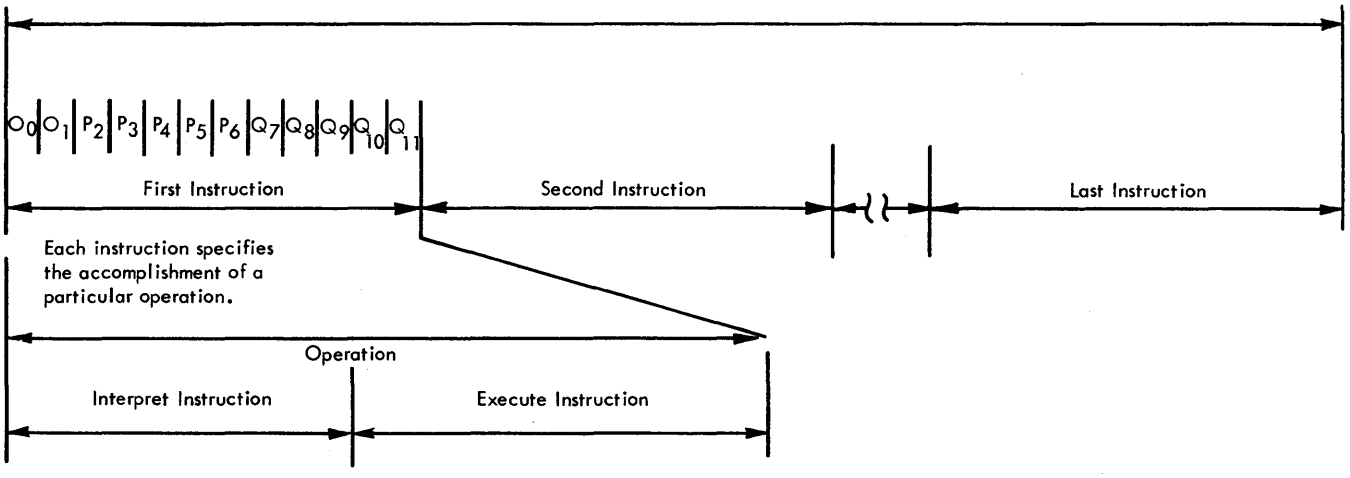



Figure 1-7. Program

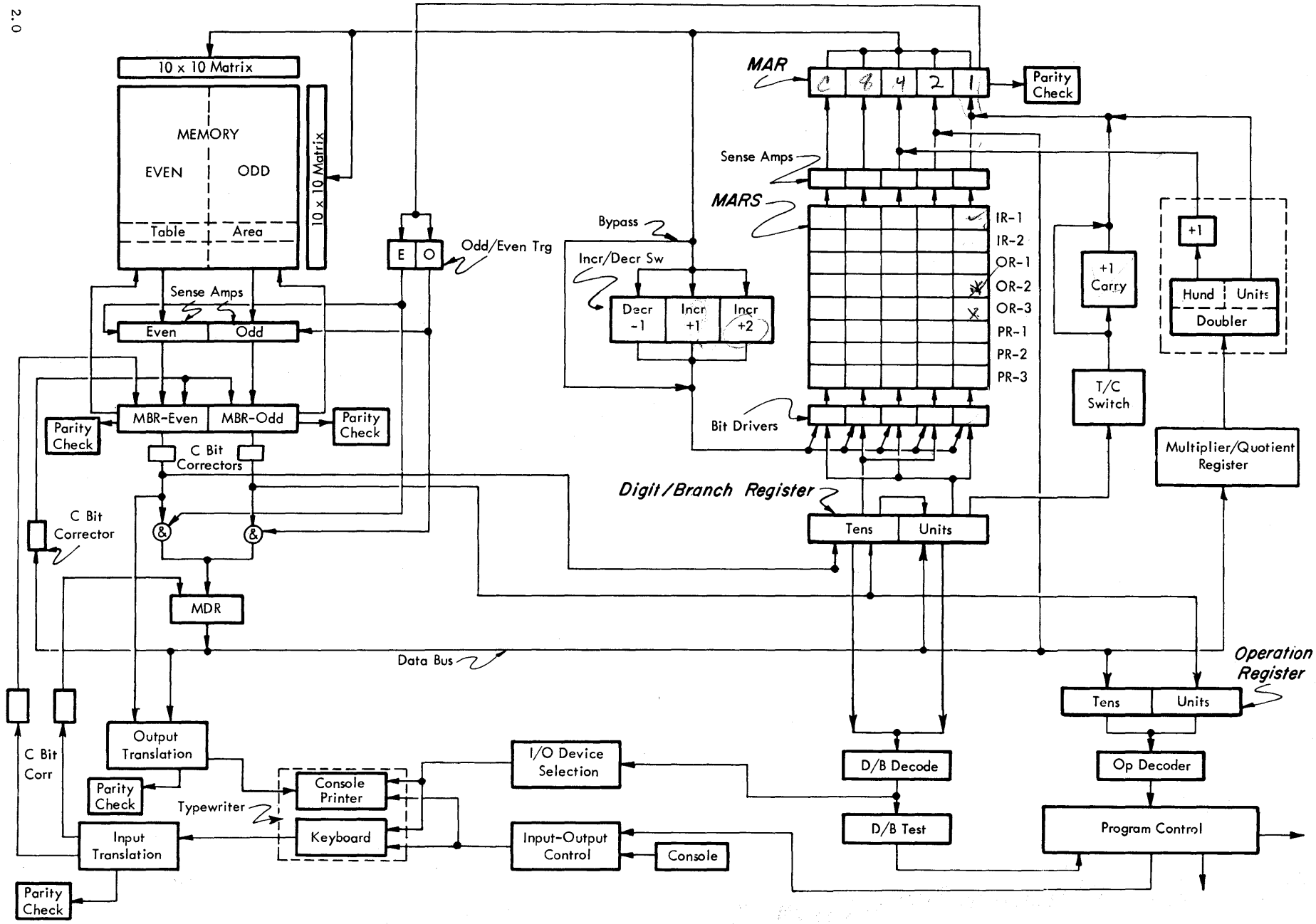



Figure 2-1. Data Flow

## INTRODUCTION

The IBM 1620 Computer normally processes data serially-by-digit, parallel-by-bit. However, the two digits which are read from memory for each address, are processed simultaneously under certain conditions.

Data, as such, is confined to Memory, Memory Buffer Register (MBR), Memory Data Register (MDR), and Input-Output areas. Digits of data which are presented to other registers by MBR and/or MDR are used to develop memory addresses or to control program execution.

Each instruction of a program is interpreted and executed by a series of machine cycles. A machine cycle consists essentially of: addressing memory, reading out of a memory location, and writing into a memory location. Digits read from memory, that are to be used for addressing or control purposes, are set into registers from MBR and/or MDR within the cycle. Digits are presented to an output device or received from an input device within the machine cycle.

NOTE: The original design concepts of this system made extensive use of triggers. Therefore the functional nomenclature chosen included the term trigger (Trigger 21, First Cycle trigger, I-cycle trigger). Subsequent engineering changes have replaced all triggers with latches except in three cases. The True/Complement, High/Plus, and Clock Drive triggers are still binary connected triggers. The system diagrams still maintain the original "trigger" designation for many of the latches and line names. For this reason the terms trigger and latch are generally used synonymously throughout this manual. These terms are not intended to designate the actual type of component used. The functions of SMS card types used in the 1620 System are given in Section 4 of this manual.

Refer to Figure 2-1 for the following discussion of data flow.

## MEMORY

Memory is addressed by means of two matrix switches which select one "column" of 12 cores (one core in the same position in each plane). Since each digit position in memory consists of six bits (C, F, 8, 4, 2, 1), it follows that in selecting one column of 12 cores, two digits will be read out each time memory is addressed. Addressing is in the form of five digits (00000 to 19999) and is from a single register, Memory Address Register (MAR). Memory is divided into two sections, even and odd, by the wiring scheme. If memory is addressed per 00000, the digit at 00000 and at 00001 will be read out (Figure 2-2). If the address is 00001 the digit at 00001 and the digit at 00000 will be read out (Figure 2-3).

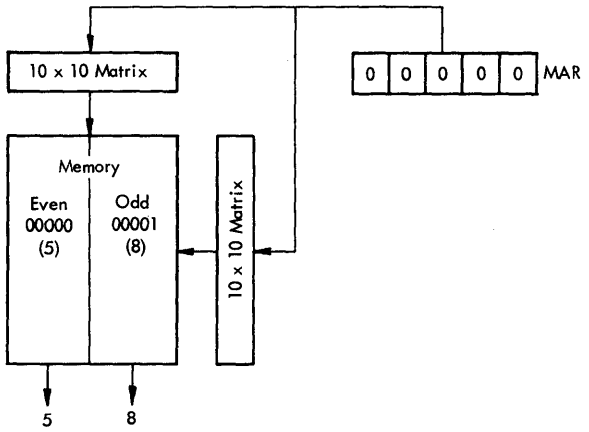



Figure 2-2. Memory Addressed per 00000

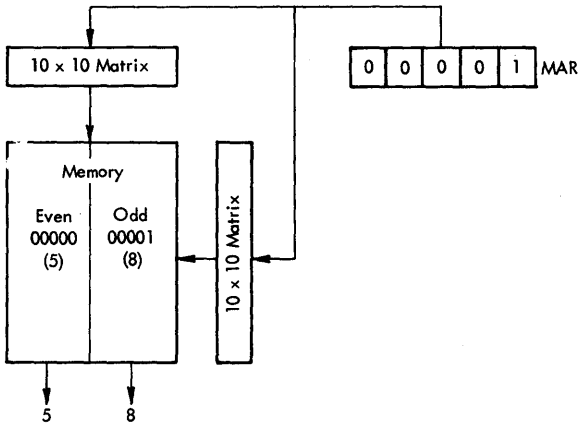



Figure 2-3. Memory Addressed per 00001

## SENSE AMPLIFIERS AND MEMORY BUFFER REGISTER (MBR)

Digits which are read out of memory are sensed by sense amplifiers which in turn set latches in the MBR. The MBR is designated even (MBR-even) and odd (MBR-odd) and will receive the corresponding digit from memory (Figure 2-4).

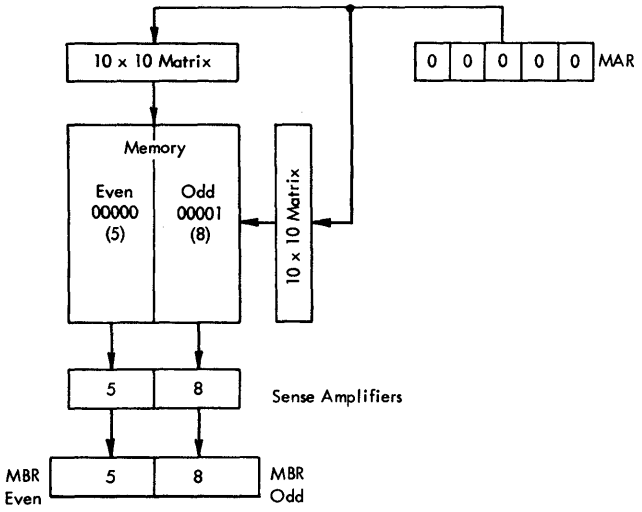



Figure 2-4. Reading Out of Memory

The readout of cores is destructive and therefore to retain the digits they must be written back into memory. The latches in MBR control inhibit lines which in turn permit the digits to be written back into memory (Figure 2-5).

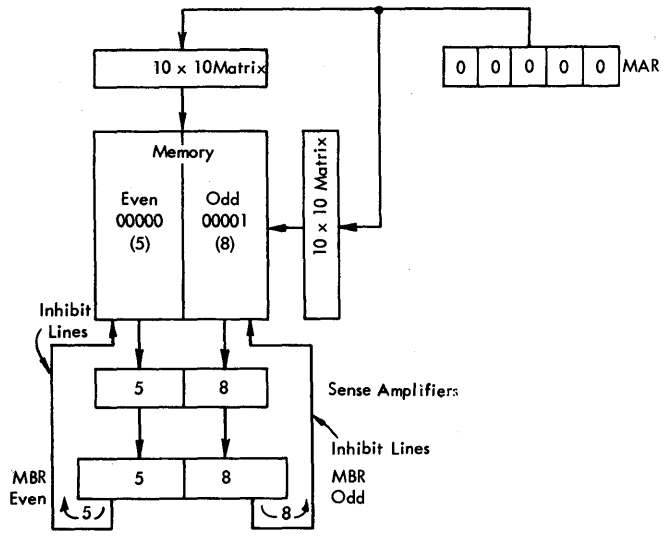



Figure 2-5. Writing Into Memory

## MEMORY DATA REGISTER (MDR)

Generally the 1620 System will use only the specific digit addressed. Therefore, a single digit register called Memory Data Register is provided to receive and store the digit. Controls are provided to determine which digit in MBR (odd or even) is transferred to MDR. To accomplish this, the output of MBR-odd and -even is controlled by an Odd/Even trigger which in turn is controlled by the units position of MAR. Figure 2-6 shows Odd/Even trigger control of the data path for the digit-5 from memory to MDR. The digit is available to the data bus from MDR.

There are times when it is necessary to clear a location in memory. At this time, the Odd/Even trigger exercises control, as to which specific location (odd or even) is to be cleared, by blocking the odd or even sense amplifiers (Figure 2-7). There are functions requiring the clearing of two memory locations, both odd and even, at the same time. This is done by blocking both the odd and the even sense amplifiers without regard to the status of the Odd/Even trigger. The objective of clearing a memory location is to reset the cores at that address so that

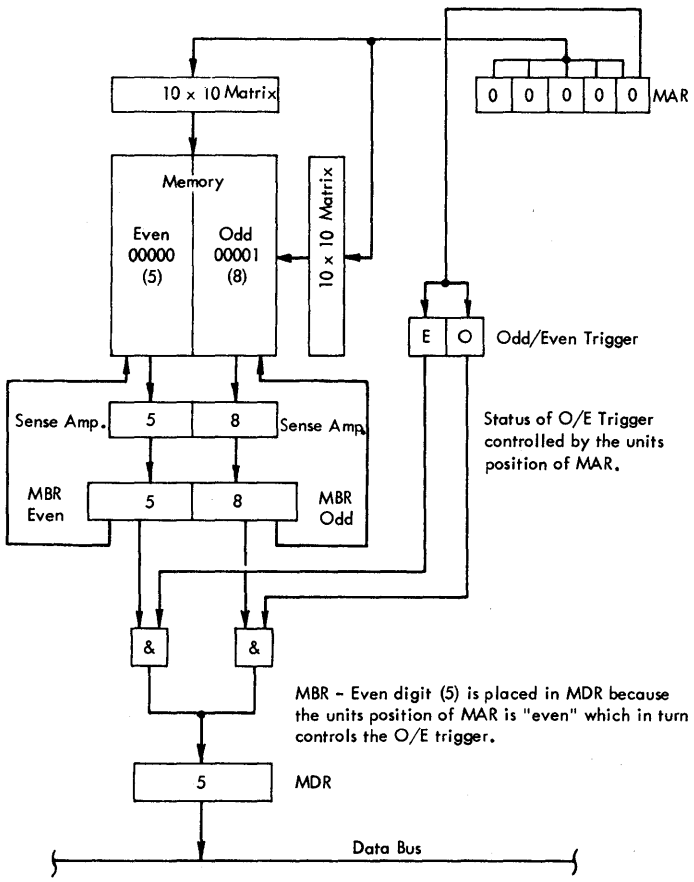



Figure 2-6. MBR to MDR Data Flow with Odd/Even Trigger Control

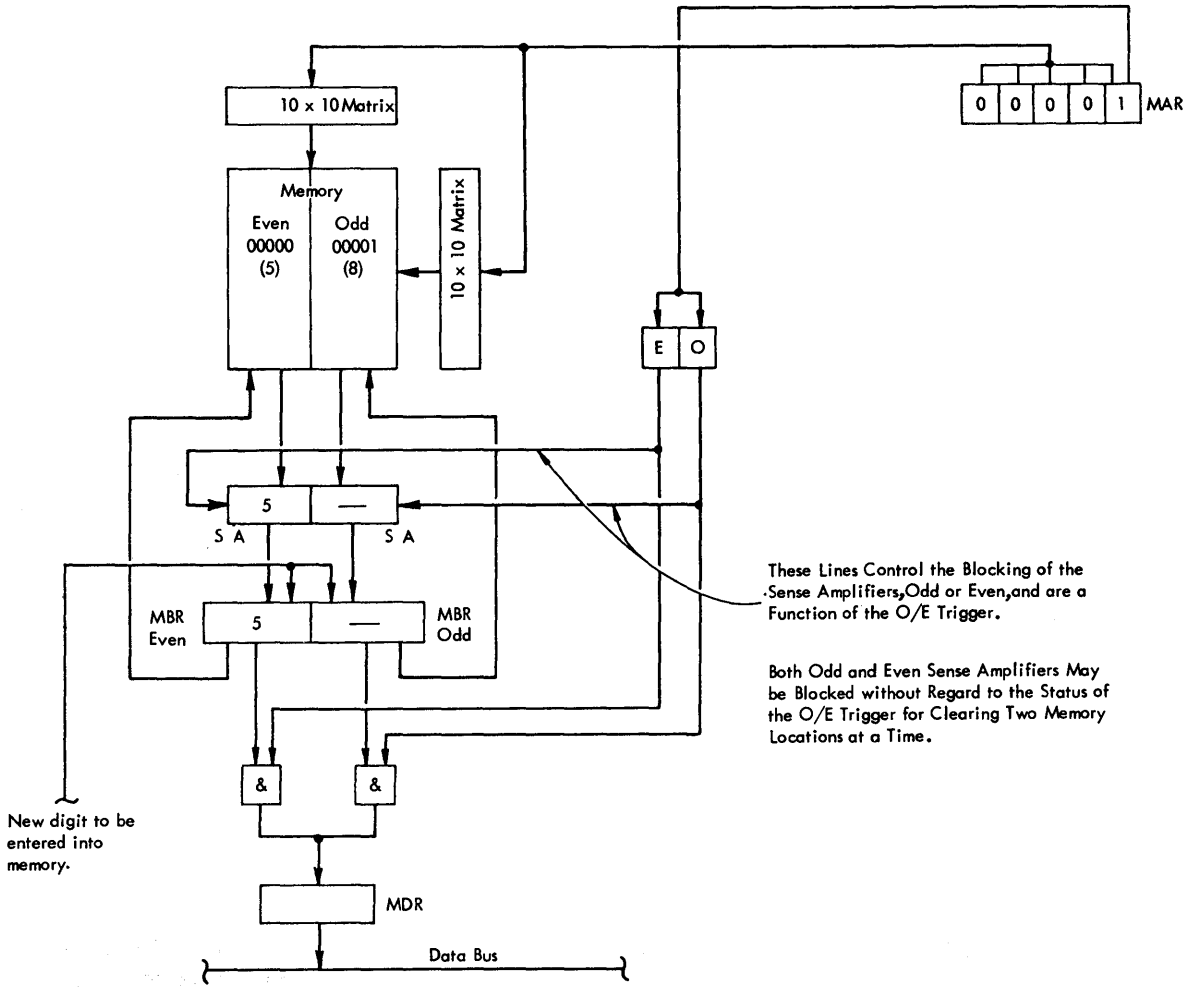



Figure 2-7. Clearing Memory Locations

a new digit may be entered. The new digit will be placed in MBR. MBR controls the inhibit lines which permit writing the new digit into memory.

## MEMORY ADDRESS REGISTER STORAGE (MARS)

Memory Address Register Storage (MARS) is a single-plane core array in a 24 x 16 matrix. The basic 1620 System makes use of only a part of the available storage, using a 24 x 8 matrix. MARS is divided into eight sections, each section capable of storing a 5-digit address. Each section or register has its own read and write drivers so that selection may be made as to which register is to read into MAR and which MARS register (one or more) will be written into (Figure 2-8).

In order to address memory, an address must be placed in MAR. This is done by causing the read drivers of a particular MARS register to be operative. The read drivers cause the address stored in that MARS register to read out, through sense amplifiers, to MAR.

To reset a MARS register the read drivers for that register are made operative at a time when the sense amplifiers are not conditioned to function.

In order to write into a MARS register, coincidence of the MARS write drivers for that register and the bit drivers is required.

The bit drivers can be gated so that a complete 5-digit address is written into MARS at one time. Another gate can cause one or two digits, as needed, to be written into MARS.

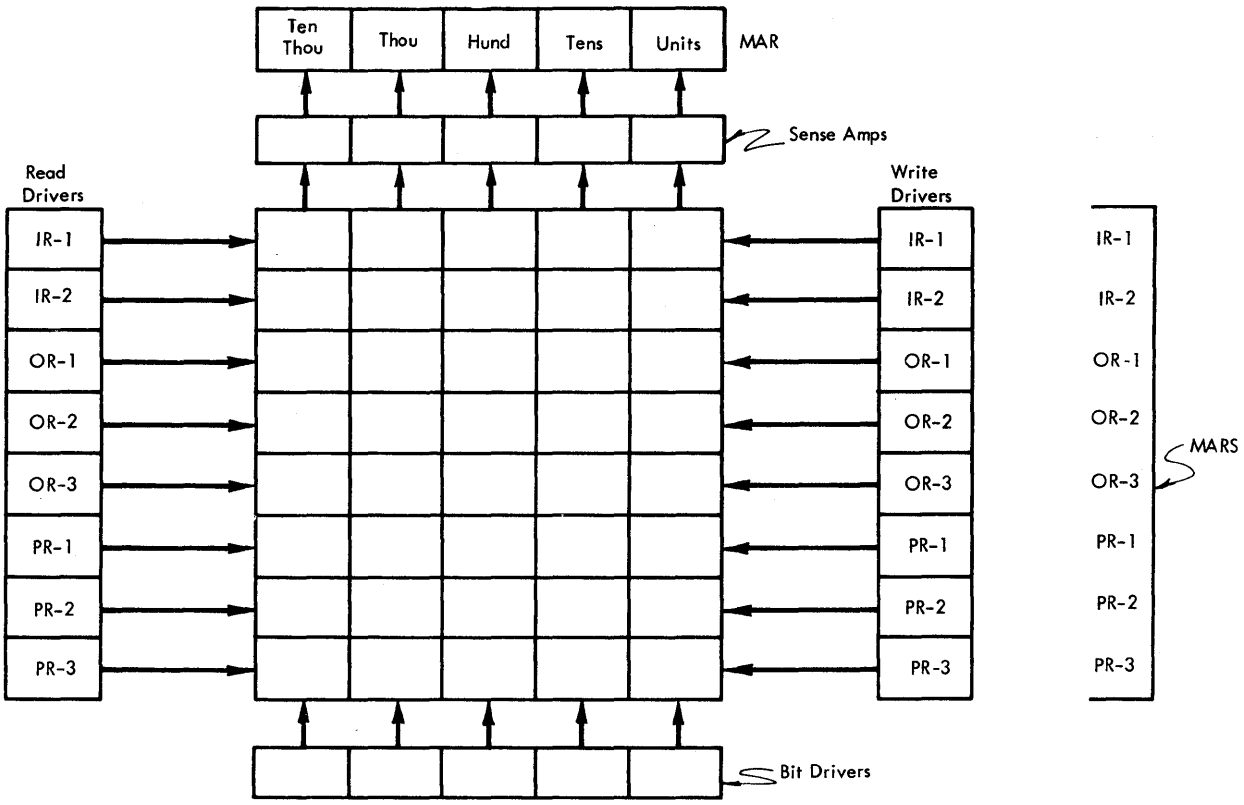



Figure 2-8. Memory Address Register Storage (MARS)

## INCREMENT/DECREMENT SWITCH

Each address read into MAR from MARS is the address of a single location in memory. Since a field or record consists of more than one digit, a means is provided to increase the address by one (increment +1) or decrease the address by one (decrement − 1) depending upon the requirements of the operation being performed. There are operations which make use of two digits at a time for which an increment +2 is provided. A decrement of −2 is provided with the Indirect Addressing feature. The Increment/Decrement switch (Incr/Decr switch) consisting of a network of AND switches and OR switches performs these functions. The Decrement trigger exercises control over the Incr/Decr switch. The status of the Decrement trigger is determined by the instruction to be executed. The output of all MAR bit triggers are connected to the inputs of the Incr/Decr switch. The outputs of the Incr/Decr switch are connected to the bit drivers. The coincidence of the bit drivers and the write drivers for a particular MARS register will write the MAR address (as altered by the Incr/Decr switch) into the MARS register.

There are operations requiring the readout of MARS to MAR where it is desired to write the address back into MARS unchanged. A bypass around the Incr/Decr switch accomplishes this function (Figure 2-9).

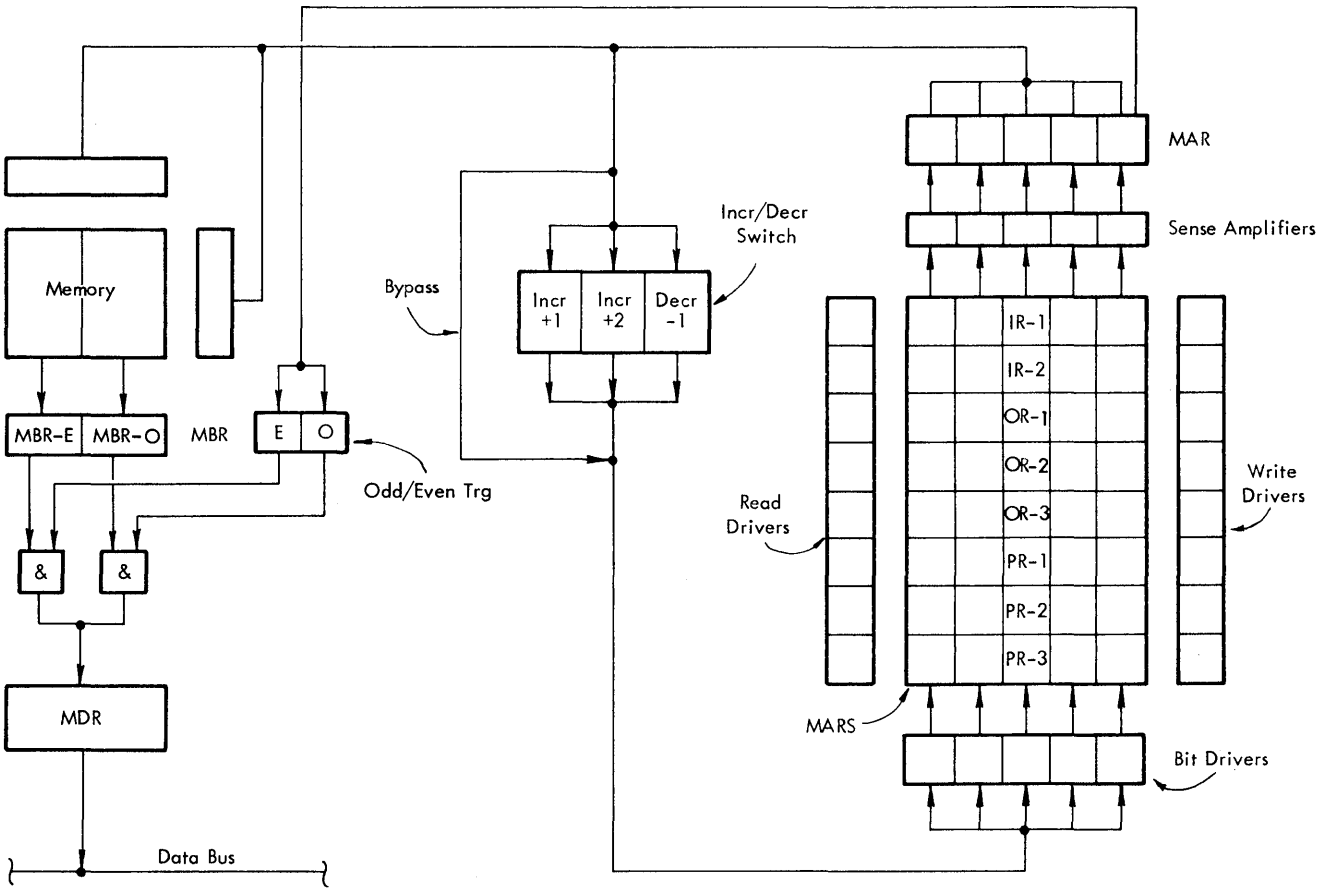



Figure 2-9. Increment/Decrement Switch

## DEVELOPMENT OF A PROGRAM

Programming consists of defining the steps required to receive data, process data, and record results in terms of the operations which the computer system is capable of performing. Each step must be written as an instruction to the computer, with the series of instructions pertaining to an entire procedure constituting a program.

A program to accomplish entry of factors, solution of a simple problem, and printing of the result is presented to illustrate 1620 Computer programming (Figure 3-1).

Compute A + B = C

Specifications:

1. Enter factors A and B into memory by means of the typewriter keyboard.
2. Store the units position of factor A at memory location 00500. (If the assigned field length for factor A is assumed to be five digits, the high-order position will be stored at location 00496.)
3. Store a record mark character at memory location 00501. (This record mark will be used to terminate the write operation demanded by Specification 5.)
4. Store the units position of factor B at memory location 00800. (If the assigned field length for factor B is assumed to be four digits, the high-order position will be stored at location 00797.)
5. Record the sum, C, on the paper form in the typewriter. (The developed sum will replace factor A and assume its location in memory.)
6. Stop the computer upon completion of the program.

## INSERTION OF A PROGRAM INTO MEMORY (TYPEWRITER KEYBOARD)

Because the IBM 1620 is a stored program computer the instructions comprising a program must be written into memory for availability to the computer in the accomplishment of the program objectives.

The program is stored in memory by pressing Insert on the console and then by typing each digit of the five instructions consecutively.

Pressing Insert places the typewriter in numerical shift; activates the typewriter keyboard; and prepares the computer to receive the high-order digit of the first 12-digit instruction at memory location 00000. By consecutively pressing the 3, 6, 0, 0, 4, 9, 6, 0, 0, 1, 0, 0, 3, 6, 0, 0, 7, 9, 7, 0, 0, 1, 0, 0, 2, 1, 0, etc. keys on the typewriter keyboard, the program is stored in memory locations 00000 through 00059. (In the program chart where the letters "P" or "Q" appear in the five instructions, any numerical key may be pressed. Those digit positions must be filled, but they are not used in the execution of the particular instruction.)

After entry of the low-order digit of the fifth instruction, pressing Release on the console terminates the insert operation. Pressing Start then initiates execution of the stored program. Pressing the R-S key on the typewriter keyboard performs the functions of Release followed by Start.

## EXECUTION OF A PROGRAM

Instructions within a program are normally interpreted and executed sequentially: that is, if the first 12-digit instruction is stored in memory locations 00000 through 00011, the execution of that instruction is followed by the interpretation and execution of the instruction stored in locations 00012 through 00023, etc.

Each instruction is read from memory and stored in registers for interpretation, starting with the high-order digit and continuing through successively higher memory locations until all twelve digits have been read.

Because execution of the first instruction, 36 00496 00100, requires that factor A and a record mark character be entered into memory manually from the typewriter keyboard, the ¯ (flag), 0, 0, 3, 2, 1, and record mark keys are pressed consecutively by the operator. Pressing Release then terminates execution of the first instruction.

Pressing Start directs the computer to proceed with the program and the second instruction is interpreted.

| Instruction Number | Memory Location for Instruction | Instruction | | | Function to be Executed |
|---|---|---|---|---|---|
| | | Op Code | P-Part | Q-Part | |
| One | 00000 | 36 | 00496 | Q01QQ | Enter Factor A (0̄0321) at Memory Location 00496 - 00500. Enter Record Mark Character at 00501 |
| Two | 00012 | 36 | 00797 | Q01QQ | Enter Factor B (0̄0067) at Memory Locations 00797 - 00800. |
| Three | 00024 | 21 | 00500 | 00800 | Add A + B and Store Sum, C, at Memory Locations 00496 - 00500. |
| Four | 00036 | 38 | 00496 | Q01QQ | Type Sum, C, (0̄0388) on Paper Form in Typewriter from Memory Locations 00496 - 00500. |
| Five | 00048 | 48 | PPPPP | QQQQQ | Stop Computer |

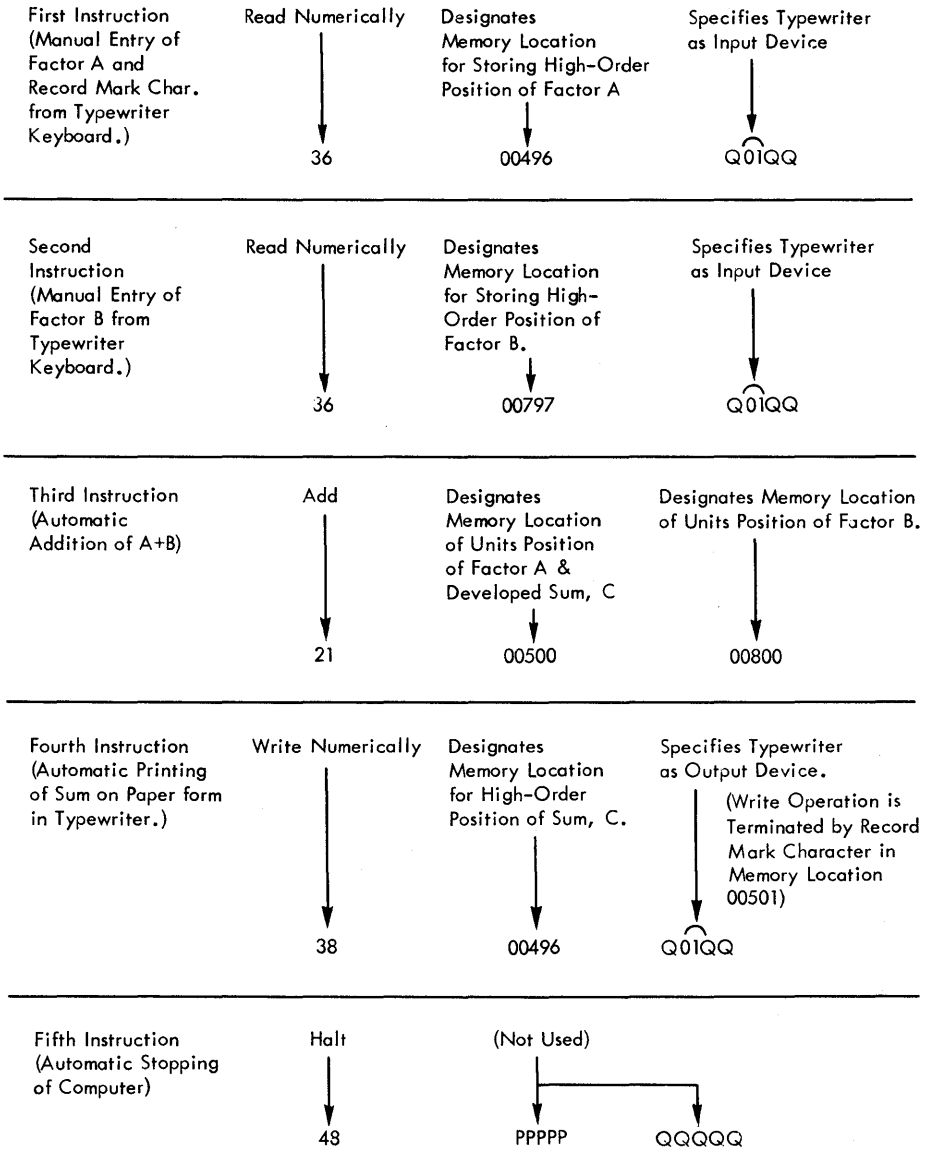



Figure 3-1. Manual Insertion of a Program into Memory

Execution of the second instruction, 36 00797 00100, requires that factor B be entered into memory manually from the typewriter keyboard. The (flag), 0, 0, 6, and 7 keys are depressed consecutively by the operator. Pressing Release terminates execution of the second instruction.

Pressing Start again directs the computer to proceed with the program and the third instruction is interpreted. No further manual entry of data is required by the program, so the third instruction is executed and the two remaining instructions are interpreted and executed automatically. The computer halts upon completion of the program.

## AUTOMATIC PROGRAM REPETITION (PROGRAM LOOP)

The program shown in Figure 3-1 computes the sum for only one problem, but by returning to the first instruction of the program and repeating the program as a loop, the sums for any number of problems can be computed. A program loop will be initiated if the halt instruction, 48 PPPPP QQQQQ, is replaced by the branch instruction, 49 00000 QQQQQ. The branch instruction directs the computer to the instruction located at its P-address, 00000, which is the address of the first instruction in the program. (A typewriter control instruction, 34 PPPPP Q01Q1 or 34 PPPPP Q01Q2, could be inserted into the program to cause the typewriter to line space and carriage return or simply space between sums.)

## MAGNETIC CORES

### Memory Cores

A magnetic core is a small doughnut-shaped ring that is uniformly constructed of ferrite particles bonded together by a ceramic material. The ferrite particles have good magnetic properties and the core has a high retentivity of the magnetic flux lines after the magnetizing force is removed. It is this property of retentivity that makes a memory core useful as a storage device.

The operation of a memory core can best be described by reference to the hysteresis curve, Figure 4-1. This curve is a plot of the relationship between a magnetizing current ($I_m$) and the flux density.

A memory core is capable of maintaining indefinitely one of two stable magnetic states, either at point A or at point D on the hysteresis curve. Because the core has two stable states, it can be used as a binary storage device. At point A the core has a residual flux in a negative direction, and at point D a residual flux in the positive direction. These two directions can be arbitrarily assigned as binary "zero" and binary "one," respectively.

$I_m$ is the amount of current necessary to change the state of the core. Plus $I_m$ is that amount of current flowing in one direction, and minus $I_m$ the same amount of current flowing in the opposite direction.

On the hysteresis curve, it can be observed that a magnetizing current of plus $I_m$ will change the magnetism of the core from point A, a binary zero, to the magnetic saturation value in the positive direction at point C. When the current is removed, the total amount of magnetization drops back to point D (binary one). If, instead of full plus $I_m$, a current of plus $I_m/2$ were applied, the flux would change only the small amount from point A to point B on the curve, and when the current returned to zero, the flux would return to its original value at point A.

A reverse current, minus $I_m$, develops flux of opposite polarity and changes the magnetic field of the core from point D to the magnetic saturation value in the negative direction at point F. The total amount of magnetization drops back to point A (binary zero) when the driving current is removed.

When a matrix of memory cores is constructed to store multiple bits of information, a specific core is selected (addressed) by the coincidence of $I_m/2$ flowing through each of two wires threaded through the core, with a total effective current of full $I_m$. The state of the core is determined by the direction of the current flowing through these wires. A current $I_m$ is passed to store a "1" in the core; this is called "writing" into cores. A current $I_m$ is passed in the opposite direction to change a stored value of "1" to a "0" and can be considered a current of minus $I_m$; this is called "reading" a core.

Reading a memory core depends on a system of sensing the state of the flux field within the core.

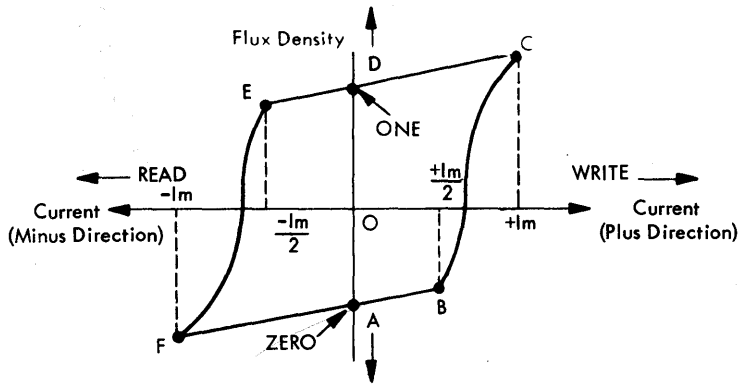



Figure 4-1. Hysteresis Curve

When the core contains a "0" and a current of minus $I_m$ read current is passed through the core, the field changes from point A to point F on the hysteresis curve, which is a very small change in total flux density. If the core contains a "1" and a minus $I_m$ read current is passed through the core, the field changes from point D to point F and a large change in the flux field occurs. A third wire, called the "sense" wire, is threaded through the core to recognize these changes in the magnetic field. Circuits are used to discriminate against low value "0" signals and amplify the large signal that results when a "1" is read from a core.

## Switch Cores

The construction of the switch cores is similar to memory cores, but the switch cores are physically larger. Switch cores, however, are not used to store or retain information, but are used as transformers, making use of the induced current pulses when the core is flipped. The induced current pulses are used to read into or write from memory cores.

The memory addressing scheme selects two specific switch cores. The outputs of the two switch cores are used to establish X and Y coordinate lines for addressing a memory location.

## COMPONENT CIRCUITS

Discussion of electronic or transistor theory is not intended in this manual. Other IBM manuals have been written to provide such information. Samples of the various types of SMS cards including Multiple Use Package (MUP) cards are described to provide the Customer Engineer with sufficient information to interpret System Diagrams and understand machine functions.

The SMS Card Index, Figure 4-2a, 4-2b, and 4-2c, lists the card types, used by the basic 1620 Computer System, by card code. Circuit schematics, part numbers, and associated logic block symbols for the cards are shown in the 1620 System Diagrams.

| Card Code | Symbol | Systems Diagrams | Description |
|---|---|---|---|
| AFR | LD or ID | C.00.05.1 | Lamp Driver. A -S input level causes a +S output level. Example on 01.06.10.1. |
| AHK | A, O, or I | C.00.05.1 | Two-way alloy type extender for AND or OR latches. Example on 01.06.10.1 |
| *AHU | Vor V | C.00.07.1 | See AYX. |
| ALY | DP | C.00.07.1 | Constant current source for matrix switches. Example on 01.30.10.1. |
| ARW | SWD | C.00.08.1 | Decode Switch. Four -S inputs are required to cause conduction. Example on 01.30.16.1. |
| AYX | V or V | C.00.08.1 | Exclusive OR. Like inputs produce a +S output and unlike inputs produce a -S output. Example on 01.40.20.1. |
| CAB | E | C.00.10.1 | Three-way alloy extender card. The collectors are not internally connected to a load resistor. Example on 01.06.11.1. |
| CAU | AL | C.00.10.1 | AND Latch-alloy type (MUP-15). Example on 01.06.11.1. |
| CD | A, O, or E | C.00.12.1 | Three-way alloy AND, OR, or Extender. Example on 01.06.11.1. |
| CEYB (CE) | DE | C.00.12.1 | Emitter follower-alloy type. Example on 01.06.20.1. |
| DAW | E | C.00.17.1 | Three-way drift extender card. Example on 01.40.03.1 |
| DEQ | I, IP, A, or O | C.00.22.1 | Three-way drift A, O, or I with a power inverter (MUP-3). Example on 01.10.05.1. |

* See System Diagram Page 01.00.05.1, Interchangeable Cards.

Figure 4-2a. SMS Card Index

| Card Code | Symbol | Systems Diagrams | Description |
|---|---|---|---|
| DES | A or O | C.00.23.1 | A three-way, two 2-ways feeding a 3-way, and a 2-way drift type AND or OR blocks (MUP-5). Example on 01.40.50.1. |
| DEV | A or O | C.00.23.1 | Two-way drift type AND or OR circuits (MUP-7). Example on 01.30.65.1. |
| DEW | A, IP, I or O | C.00.24.1 | Five 2-way, drift type, AND or OR circuits with one input common, and a power inverter (MUP-8). Example on 01.55.55.1. |
| DFB | A or O | C.00.25.1 | A 3-way feeding a 2-way and two 2-ways feeding two 2-ways, drift type, AND or OR circuits (MUP-13). Example 01.55.15.1 |
| DFC | A or O | C.00.25.1 | Four 3-way drift type AND or OR circuits uits with one input common (MUP-14). Example on 01.55.03.1. |
| DFD | AL | C.00.30.1 | AND latch, drift type. Example on 01.45.05.1. |
| DFE | A, O, or E | C.00.30.1 | A six-way and two 2-way drift type And or OR circuits (MUP-16). Example on 01.40.03.1. |
| DFG | A or O | C.00.33.1 | Two 3-way feeding a 2-way and two separate 2-way drift type AND or OR circuits (MUP-18). Example on 01.55.06.1. |
| DFP | A, O, or IP | C.00.33.1 | Three 3-way feeding a 3-way drift type AND or OR circuits and a separate power inverter (MUP-20). Example on 01.55.06.1. |
| *FL | SWD | C.00.35.1 | See ARW. |
| *FM | D | C.00.38.1 | Current driver, alloy type. Used with ARW card to provide matrix switch input currents. Example on 01.30.10.1. |
| *FQ | DP | C.00.07.1 | See ALY. |
| MH | I | C.00.40.1 | Power inverter. Example on 01.06.20.1. |
| MX | A,O, or I | C.00.40.1 | Two-way alloy type AND, OR, Extender or Inverter. Example on 01.06.10.1. |
| NN | AMP, AM or R | C.00.41.1 | Sense amplifier. Used with MARS. Example on 01.57.01.1. |
| NP | DP | C.00.41.1 | Relay and light driver. Used with typewriter relays and console lights. Example on 01.82.52.1. |
| *QF | LD or ID | | See AFR. |
| QU | | | Differential amplifier card for SMS Power Supplies in some 1620's. |
| RE | THER | C.00.45.1 | Thermoswitch. Used for checking gate temperature. Example on 01.90.42.1. |
| TAF | OSC | C.00.46.1 | Oscillator, one megacycle. Used as basic timer for 1620 clock circuits. Example on 01.10.05.1. |
| TAG | A, O, or I | C.00.47.1 | Two-way AND, OR, or Inverter, drift type. Example on 01.59.10.1. |

Figure 4-2b. SMS Card Index

* See System Diagram Page 01.00.05.1, Interchangeable Cards.

| Card Code | Symbol | Systems Diagrams | Description |
|---|---|---|---|
| TAH | A,O, or E | C.00.47.1 | Three-way AND, Or, or extender, drift type. Example on 01.55.45.1 |
| TAJ | TB | C.00.48.1 | Binary trigger. Example on 01.63.20.1 |
| TAK | I | C.00.60.1 | See TFC. |
| TAL | DSP | C.00.48.1 | Sample pulse generator. Used to provide the rapid rise time required to change the state of a binary trigger. Example on 01.63.20.1. |
| TCZ | L, LI | C.00.55.1 | Latch, inverting drift type (MUP - 12) |
| TFC | I | C.00.60.1 | Power inverter, drift type. Example on 01.10.30.1 |
| *TTX | CP | C.00.61.1 | See NP. |
| *VE | A, O, or I | C.00.47.1 | See TAG. |
| *VF | A, O, or E | C.00.47.1 | See TAH. |
| *VG | OSC | C.00.46.1 | See TAF. |
| *VJ | TB | C.00.48.1 | See TAJ. |
| *VL | DSP | C.00.48.1 | See TAL. |
| *VM | I | C.00.60.1 | See TFC. |
| WF | SWD | C.00.35.1 | See ARW. |
| *WG | D | C.00.61.1 | See FM. |
| WJ | D | C.00.63.1 | Current driver, alloy type. Example on 01.55.55.1. |
| WM | AMP | C.00.63.1 | Single shot sense amplifier, alloy type. Input from memory presense amplifier. Provides a 1 sec pulse to MBR latches. Example on 01.30.50.1. |
| WY | AMP | C.00.65.1 | Pre-sense amplifier, alloy type. Used to amplify a nominal 40 mv signal. Example on 01.30.50.1. |
| YGB | | C.00.69.1 | Overvoltage protection, 12 volt power supply. Example on 01.90.23.1. |
| YGC | | C.00.69.1 | Overvoltage protection, 36 volt power supply. Example on 01.90.22.1. |
| YGH | | C.00.71.1 | Differential amplifier, 36 volt power supply. Example on 01.90.22.1. |
| YGJ | | C.00.71.1 | Differential amplifier, 12 volt power supply. Example on 01.90.23.1 |
| YGN | | C.00.75.1 | Differential amplifier, 30 volt power supply. Example on 01.90.25.1. |
| YJA and YJB | R | C.00.77.1 | Load resistors. Example on 01.55.55.1. |

Figure 4-2c. SMS Card Index

* See System Diagram Page 01.00.05.1, Interchangeable Cards.

The 1620 Computer uses a type of circuitry known as Transistor Resistor Logic (TRL). This type of circuit uses resistors in voltage dividing networks to control the functions of transistors. TRL is also called NOR, Negative OR.

There are two types of transistors used in the 1620: alloy and drift. The drift type is also called saturating drift. The term SDTRL, used with an SMS card, means Saturating Drift Transistor Resistor Logic and indicates that the transistor or transistors used in that card are of the drift type. The difference between alloy and drift transistors is in transition times. The drift is faster than the alloy and is used in areas where speeds are critical.

The term CTRL means Complementary Transistor Resistor Logic which indicates that inputs and outputs can be of a different level. For example a ±S level input can result in a ±R level output. R levels are +R = +12v and — R = 0v. The relay thyratron drivers, DP cards, are an example, having +48v on the output. CTRL cards are not necessarily used with the complementary function.

Figure 4-3 depicts a typical "block," as shown in 1620 System Diagrams, with symbols defined. If the additional features line is blank, the block is a basic 1620 logic block. If a code appears in the line, the block is associated with the additional feature specified by the code. The logic block coding for additional features is as follows:

| Code | Feature |
|---|---|
| DV | Divide |
| IA or IF | Indirect Addressing |
| DI | DV or IA or Both |
| CRP | Card Read-Punch - Card I/O-IBM 1622 |
| TN | Special Instructions - TNS, TNF, MF |
| M1 | Additional Core Storage - 20 or 40 K IBM 1623 |
| M2 | Additional Core Storage - 40 K only IBM 1623 |
| M1N2 | Additional Core Storage - 20 K only IBM 1623 |
| FP | Floating Point |
| RAM | Disk Storage Drive - IBM 1311 |
| CF | CRP and RAM |
| C/F | CRP or RAM or Both |
| FP/F | FP or RAM or Both |
| M1/F | M1 or RAM or Both |
| M2/F | M2 or RAM or Both |
| NM1 | Not M1 |
| FNM1 | RAM Not M1 |
| PT | Paper Tape - IBM 1621 - 1624 |
| PR | Printer - IBM 1443 |

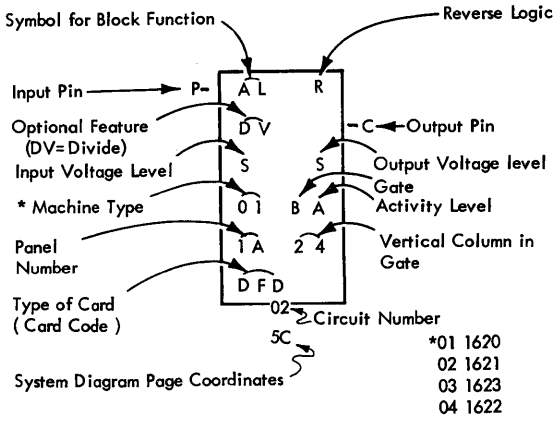



Figure 4-3. 1620 System Diagram (Logic) "Block"

The following logic block codes are associated with the IBM 1710 Control System:

| Code | Feature |
|---|---|
| INT | Interrupt |
| F1 | 1710 Attachment |
| F2 | 1710 Additional Features |
| F3 | 1711 Compatibility |
| SIOC | Serial Input/Output Channel |
| SI/P | SIOC or Pulse Duration |
| HSA | High Speed ADC |

## AFR Card

This block provides a current source for the 12v indicator lamps on the console (Figure 4-4).

A —S level applied to pin A causes T2 to conduct, supplying a low resistance path to ground for the current through the lamp. When T2 is cut off the 1.8K resistor to ground does not pass enough current to light the lamp.

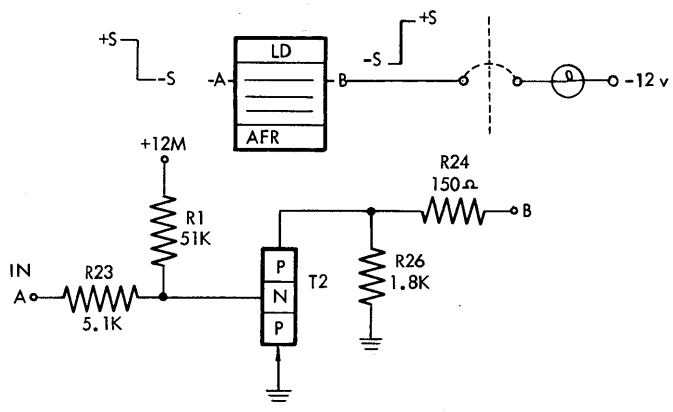



Figure 4-4. CTRL Light Driver

AHK, CAB, CD, DAW, DAX, MX, TAG, TAH, VE, and VF Cards

These cards consist of NOR circuits which are similar in function and operation. The following description of one of the three circuits on a type VF 3-way inverter card (Figure 4-5) will serve to explain the function and operation for the group.

As an Inverter, this block has a +S output level if any one of its inputs is at a –S level.

As an AND switch, this block has a —S output level if all inputs are at +S level.

As an OR switch, this block has a +S output level if any one or more of its inputs is at —S level.

The transistor is conducting when any one or more of the inputs is at —S level.

## Extenders

When additional inputs are necessary to perform a particular logical function, NOR blocks are connected in parallel. One and only one of the logic blocks has a collector load resistor. This configuration merely "extends" the logical function (Figure 4-6). All input lines to extender logic blocks as well as the basic logic block must be at +S level to obtain a —S output level. One or more —S input levels to an extender block as well as to the basic logic block will give a +S output level.

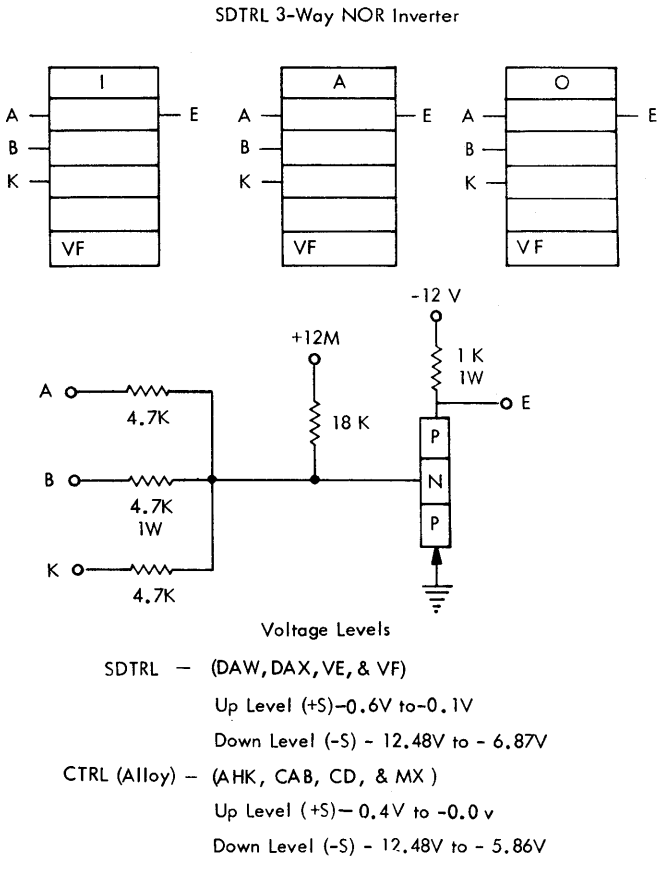



Figure 4-5. SDTRL 3 Way NOR Inverter

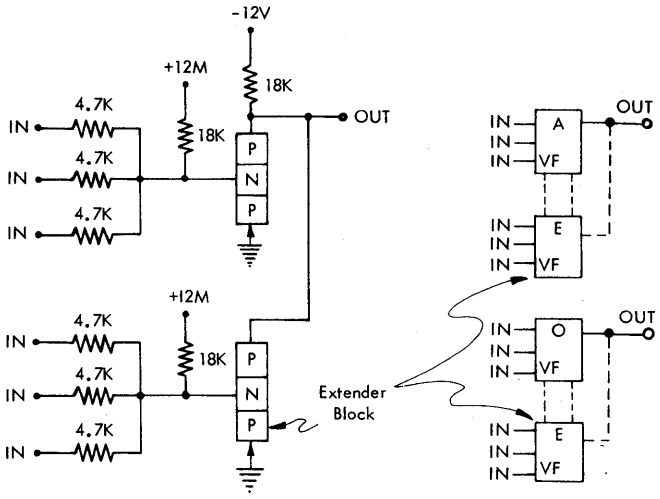



Figure 4-6. Extenders

## NOR Latch

A common method of storing a bit of information in NOR logic is by means of a "latch" (Figure 4-7).

A shift to the —S level at point F or point G places the OFF side transistor into conduction, which puts point CL at +S level. If points A and B are at +S level, the ON side transistor is cut off,

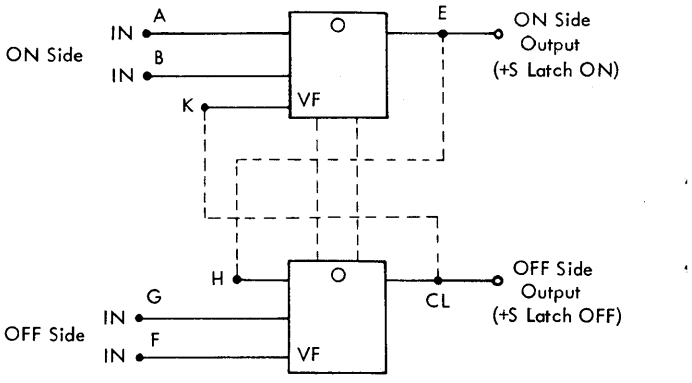



Figure 4-7. NOR Latch

which drops point E to the −S level. A −S level at point E reinforces the −S level introduced at point F or point G and holds point CL at a +S level even if the negative signal at point F or point G is removed. This latches the circuit in an OFF state until a negative (−S) signal occurs at either point A or point B.

## ALY, ARW and FM Cards

These cards are associated with the addressing of memory and will be discussed in terms of that application (Figure 4-8).

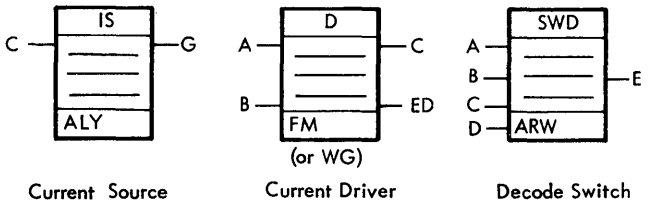



Figure 4-8. SMS Cards Associated with Matrix Switch

The ALY card provides a constant current source for use with the switch cores (packaged one circuit per card).

The ARW card (decode switch) provides a means for selecting a particular switch core coordinate according to the addressing scheme. The decode switch provides a path to ground, through the switch core, for the current source when the gate to the FM card blocks the path through the FM card circuits (packaged two circuits per card with Circuit 1 shown).

The FM (or WG) card provides: (1) A path for the current source during the time when a switch core is not selected and the control gate is not present. This path maintains current flow through the bias winding. (2) A timed control (gate) causing the current path to be directed through the axes of switch cores to a selected decode switch (ARW card). The current through the bias winding is maintained, during the time a switch core is selected, by a path, through the selected core, to the decode switch (packaged 1 circuit per card).

The bias winding is wound with four turns around every switch core, in series, of matrix switches A and D (refer to Figures 4-9 and 4-10). This winding carries a current in such a direction and of such a magnitude that it tends to retain all switch cores in a "zero" state. The bias winding current (1 amp) supplies current for the Y'Y" and X'X" axes of the switch cores. Note that the bias winding current is divided through four circuits; units and tens (Y'Y") of matrix switch A and hundreds and thousands (X'X") of matrix switch D. One ampere in the bias winding times 4 turns equals 4 ampere turns of magneto-motive force (MMF). The Y'Y" and X'X" axes are wired with 12 turns around their respective switch cores. These 12 turns are wound in such a manner that their MMF opposes the bias winding MMF. Because the bias current divides equally through the Y'Y" and X'X" wiring, there will be 250 ma flowing through each coordinate wire. The 250 ma's times 12 turns equals 3 ampere turns of magneto-motive force. It requires 2 ampere turns to flip a switch core. When one coordinate of a matrix switch is carrying current (3 ampere turns) in opposition to the bias current (4 ampere turns), the effect of the bias current is nearly cancelled. When both coordinates are carrying current (3 + 3 = 6 ampere turns), the effect of bias current is cancelled and the core will flip to its "one" state. If the current through one coordinate is removed, the core cannot flip back to its "zero" state because 3 ampere turns from the remaining coordinate are opposing the 4 ampere turns of the bias winding. Four minus three equals one turn which is not enough to flip the switch core to "zero." When the second coordinate current is removed, the 4 ampere turns of MMF in the bias winding will flip the core to its "zero" state.

### Circuit Operation with Switch Core Not Selected

Starting at +30 v, (① Figure 4-10) the bias current passes through all switch cores in series to pin C of the current source (ALY) cards. From pin C, the current passes through a noise elimination inductor, two 90Ω 5W resistors in parallel, T1, noise elimination inductor, and resistor in parallel, to pin G of the ALY card. The +30 v through the 4.7K resistor is for level setting. Pin G is wired to pin A of the FM card.

The current then flows through T2, which is conducting, to the −12 v supply to complete the circuit.

### Selecting a Switch Core

Prior to the selection of a switch core, the status of the transistors in the decode switch (ARW) are as follows: (1) T4 conducting which places a minus potential on the base of T5. (2) T5 cut off by the action of T4. The addressing circuits place −S (− 12 v) on pins A, B, C, and D. This reverse

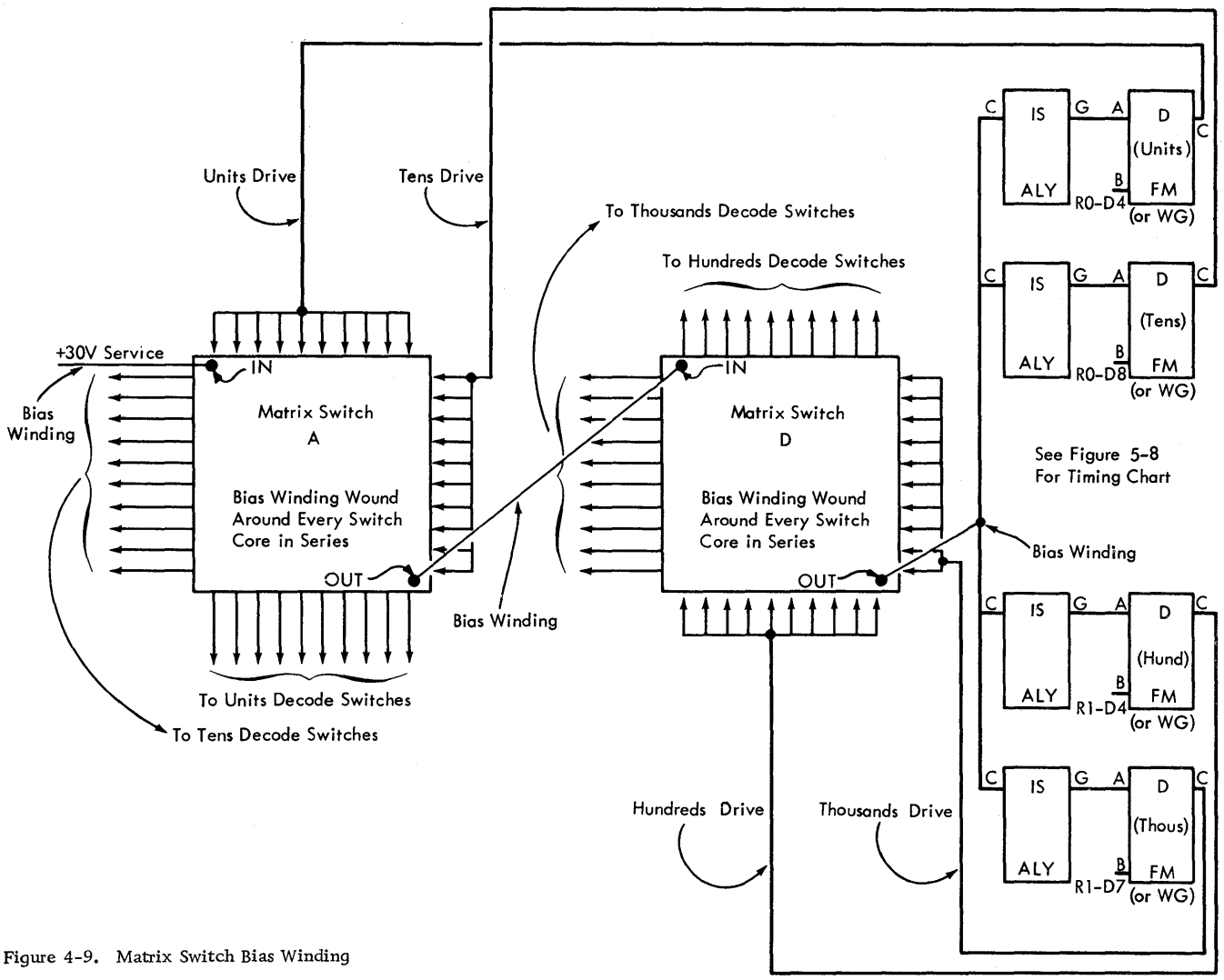



Figure 4-9. Matrix Switch Bias Winding

biases T4 and cuts it off, raising the potential at its collector to +30 v which is placed on the base of T5 to bring it into conduction.

With T5 in conduction, the ground at its emitter is available at pin E of the ARW card, through the selected switch core to pin C of the FM card. However, current will not flow through this circuit until T2 is cut off thereby blocking the current path to −12 v.

Circuit Operation with Switch Core Selected

As long as pin B of T3 is at +S, T3 will conduct, causing a forward bias to be applied to the base of T2 which in turn stays in conduction. When the −S gate (R0-D4 for units of matrix switch A) is placed on pin B of T3, T3 is cut off. This removes the forward bias from T2 which in turn is cut off. With T2 cut off, the current seeks a new path which it finds by passing through the diodes of the FM card, through the switch core, to ground through T5.

NOTE: The direction of this coordinate current flow through the switch core is in opposition to the bias winding current flow.

When a switch core in matrix switch A flips to the "one" state, it induces a current pulse in the winding connected to the memory array. This induced current produces the Y coordinate for a "read" out of memory. Matrix switch D provides the X coordinate.

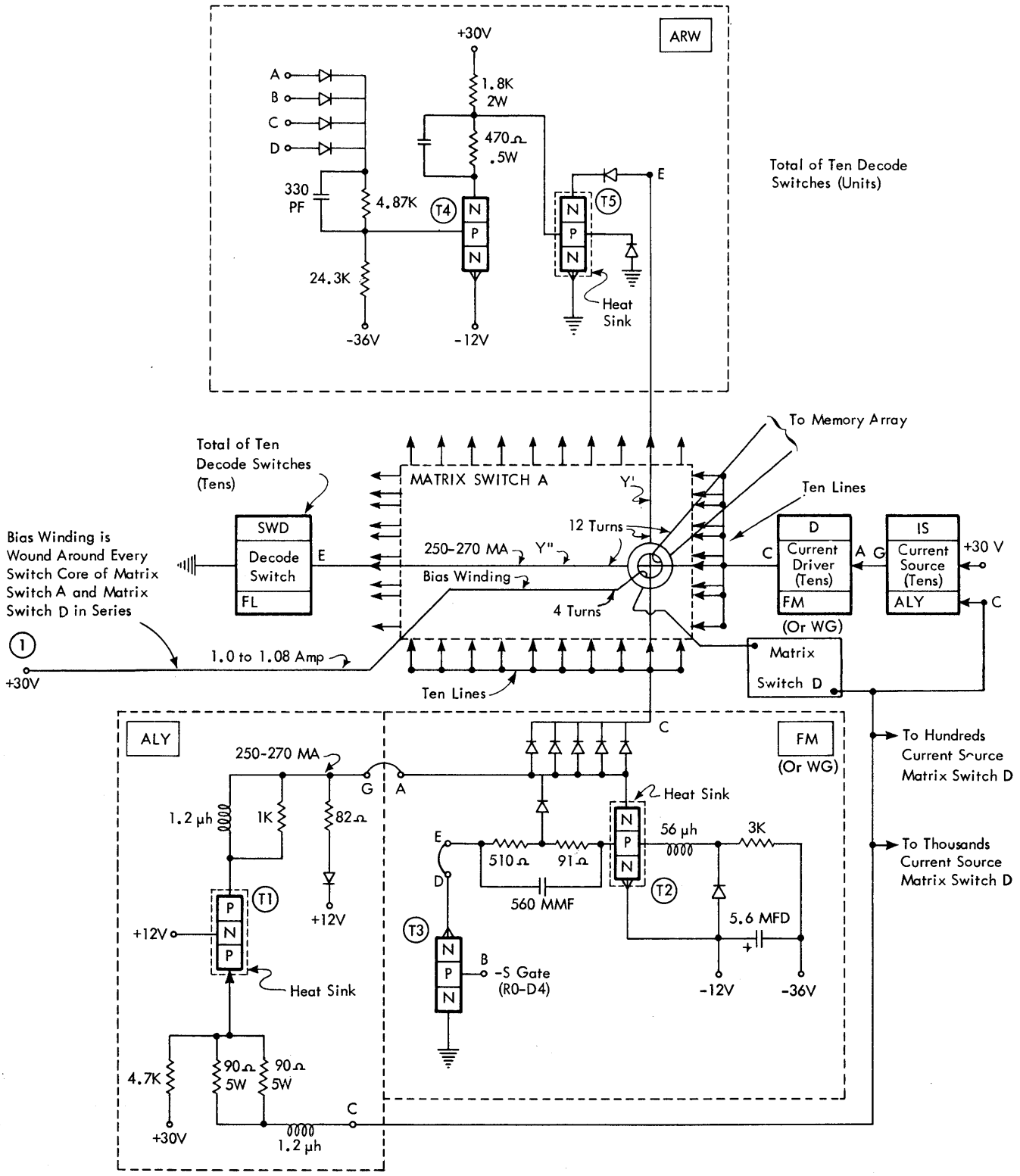



Figure 4-10. Matrix Switch Operation

When the gate at pin B of T3 is removed (returns to +S), T3 will conduct which in turn forward biases the base of T2 causing T2 to conduct and provide a path for the current flow to −12 v. Current will no longer flow from the current source (ALY) to the ground through T5. As soon as the Y' and Y" current flow is cut off, the effect of the bias current, which is still present, will flip the selected switch core back to the "zero" state. When a switch core in matrix switch A flips to its "zero" state, it induces a current pulse in the winding connected to the memory array. This current pulse is induced in the opposite direction to that induced when a switch core was flipped to the "one" state. This current produces the Y coordinate for a "write" into memory. Matrix switch D provides the X coordinate.

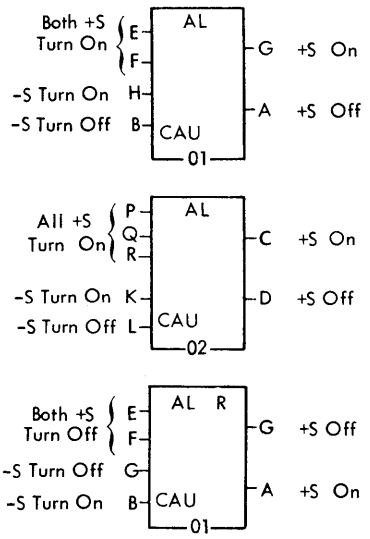



Figure 4-11. AND Latch

## AYX Cards

These Exclusive OR cards are used in the various checking circuits (Read, Write, MBR, MAR) found in the 1620. Like inputs (both +S or both −S) produce a +S output and unlike inputs produce a −S output (packaged 3 to a card).

## CAU and DFD Cards

Each latch circuit contains three transistors. One transistor is used as a 2-way or 3-way AND circuit which feeds an input to the other two transistors. The second two transistors are connected as an OR latch. The AND latch is turned on with a +S input to all legs of the AND portion of the circuit (+S on E and F pins for circuit 1 or +S on P, Q, and R pins for circuit 2) as shown in Figure 4-11. The latch may also be turned on with a −S input to pin H for circuit 1 or to pin K for circuit 2. Output pin G for circuit 1 or pin C for circuit 2 is +S when the latch is on and is −S when the latch is off. Output pin A for circuit 1 or pin D for circuit 2 is −S when the latch is on and is +S when the latch is off. The input and output functions of the logic block are reversed if an "R" is in the upper right corner of the logic block. This reversed logic is used when an AND condition is needed to turn off a latch.

## CEYB Card

This card is an emitter follower used for impedance matching and to provide powering (current) to drive succeeding logic blocks.

## DEQ Card

This MUP card (Figure 4-12) contains three separate 3-way AND or OR circuits connected to three separate power inverter circuits (IP). Pin H is the non-inverted output of one of the 3-way AND or OR circuits. The 3-way circuits are similar to TAH and VF circuits, and the power inverters are similar to TFC circuits. Note the absence of pin designations between the 3-way blocks and the inverters.

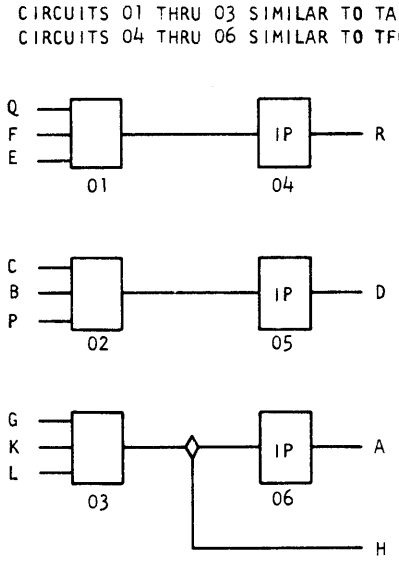



Figure 4-12. DEQ MUP Card

## DES Card

This MUP card (Figure 4-13) contains two 2-way AND or OR circuits connected to a 3-way AND or OR circuit. The card also contains separate 3-way AND or OR circuits and a separate 2-way AND or OR circuit. The 2-way circuits are similar to TAG and VE circuits and the 3-way circuits are similar to TAH and VF circuits.

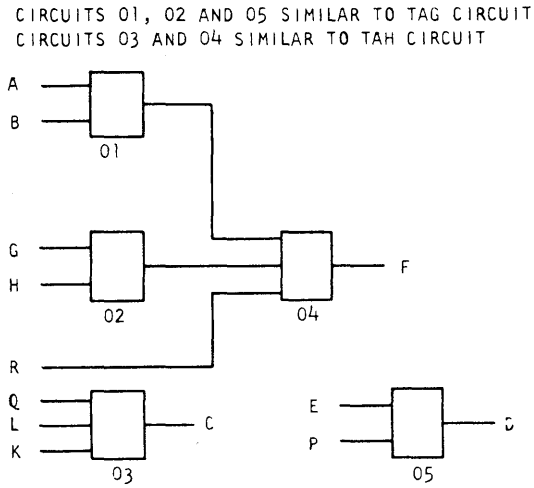



Figure 4-13. DES MUP Card

## DEV Card

This MUP card (Figure 4-14) contains two separate circuits with each having two 2-way AND or OR circuits connected to a 2-way AND or OR circuit. The card also contains a separate, single, 2-way AND or OR circuit. All of the circuits are similar to TAG and VE circuits.

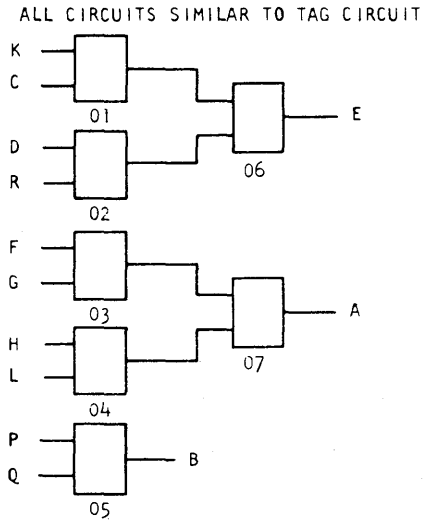



Figure 4-14. DEV MUP Card

## DEW Card

This MUP card (Figure 4-15) contains five 2-way AND or OR circuits with pin L common to each of the five. These five circuits are similar to TAG and VE circuits. The card also contains a power inverter circuit (IP) that is similar to TFC, TAK, and VM circuits.

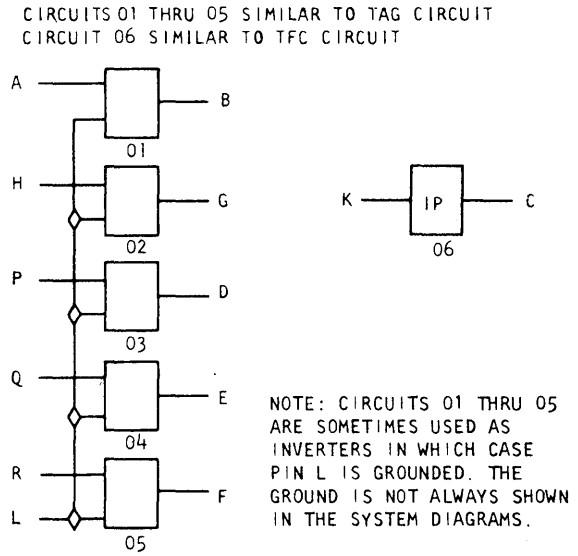



Figure 4-15. DEW MUP Card

## DFB Card

This MUP card (Figure 4-16) contains a 3-way AND or OR connected to a 2-way AND or OR circuit. The 3-way circuit is similar to TAH and VF circuits and the 2-way circuit is similar to TAG and VE circuits. The card also contains two 2-way AND or OR circuits, each connected to a 2-way AND or OR circuit. These four 2-way circuits are similar to TAG and VE circuits.

## DFC Card

This MUP card (Figure 4-17) contains four 3-way AND or OR circuits with pin G being common to all four. These circuits are similar to TAH and VF circuits.

CIRCUIT 01 SIMILAR TO TAH CIRCUIT
CIRCUITS 02 THRU 06 SIMILAR TO TAG CIRCUITS

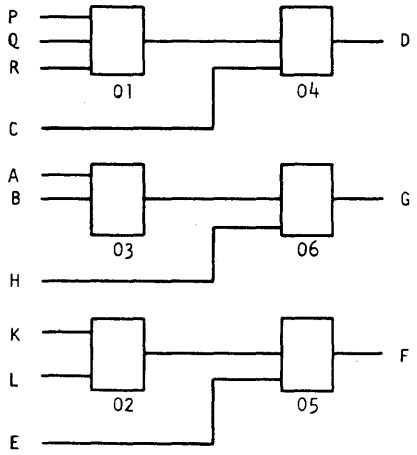



Figure 4-16. DFB MUP Card

ALL CIRCUITS SIMILAR TO TAH CIRCUIT

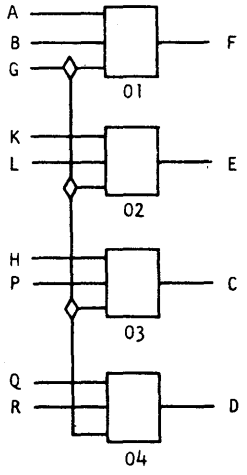



Figure 4-17. DFC MUP Card

## DFE Card

This MUP card (Figure 4-18) contains two 3-way AND or OR circuits connected to a common load resistor thus making up a 6-way AND or OR circuit. The 3-way circuits are similar to TAH and VF circuits. The card also contains two separate 2-way AND or OR circuits, these being similar to TAG and VE circuits.

CIRCUITS 01 AND 02 SIMILAR TO TAH CIRCUIT
CIRCUITS 03 AND 04 SIMILAR TO TAG CIRCUIT

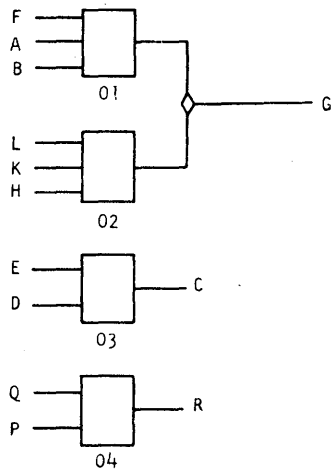



Figure 4-18. DFE MUP Card

## DFG Card

This MUP card (Figure 4-19) contains two 3-way AND or OR circuits connected to a 2-way AND or OR circuit and two separate 2-way AND or OR circuits. The 3-way circuits are similar to TAH and VF circuits. The 2-way circuits are similar to TAG and VE circuits.

CIRCUITS 01 AND 02 SIMILAR TO TAH CIRCUIT
CIRCUITS 03 AND 05 SIMILAR TO TAG CIRCUIT

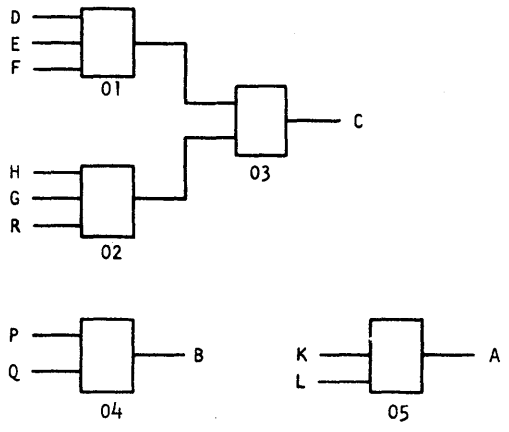



Figure 4-19. DFG MUP Card

## DFP Card

This MUP card (Figure 4-20) contains three 3-way AND or OR circuits connected to a 3-way AND or OR circuit. The 3-way circuits are similar to TAH and VF circuits. The card also contains a power inverter circuit similar to TFC, TAK, and VM circuits.

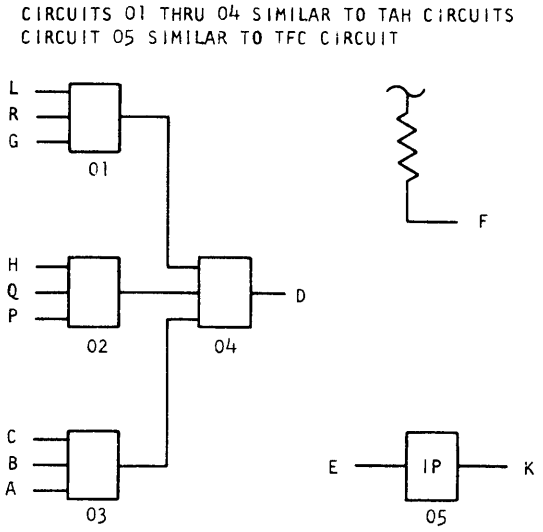



Figure 4-20. DFP MUP Card

## MH Card

This card provides power for driving succeeding logic blocks. The input signal (+S or −S) is inverted in passing through the block.

## NN Card

This card provides a bipolar amplifier to detect and amplify a signal on a sense winding of the MARS core plane (Figure 4-21). The NN card wired in this manner functions as an extender to the TCZ card and turns on the latch by collector pullover.

Because of the physical position of the cores with respect to the "X" and "Y" wires, a unipolar pulse will be generated in the sense winding when a core is flipped. A "MARS Sense Amp Sample" (Strobe) is used to discriminate between read and write pulses, being timed so that only a read pulse is detected. The output waveforms and voltage levels are shown in Figures 4-22, 4-23, and 4-24.

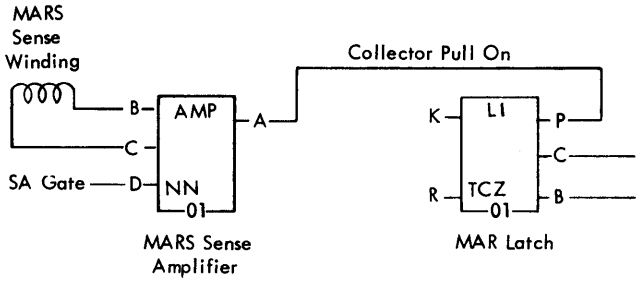



Figure 4-21. CTDL - Sense Amplifier and Load

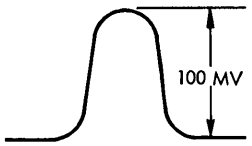



Figure 4-22. Output of MARS Core

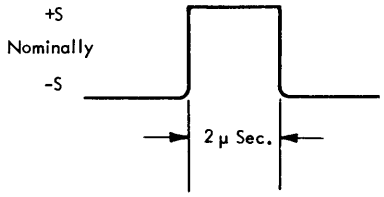



Figure 4-23. MARS Sense Amplifier Output Waveform

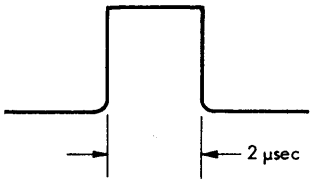



Figure 4-24. Strobe, MARS Sense Amp Sample

NOTE: When the output of the sense amplifier is connected to the collector of a latch which is turned ON by collector pullover, the waveform as seen by a scope at pin A or AF will therefore be the output of the latch (Figure 4-25).

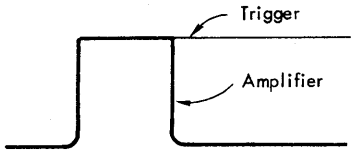



Figure 4-25. Amplifier Output Connected to Trigger (Collector Pullover)

## NP Card

This card provides the control and current source for operation of 48v relays, magnets, and signal lights (Figure 4-26).

A +S potential applied to pins A and B (see note) will cause T4 to go into conduction when a 48 v potential is applied to pin C. Once conduction is started, the current drawn from the base of T4 to the emitter will cause T4 to remain in conduction regardless of the potential at pins A and B. Conduction is cut off only by removing the 48 v supply to pin C. The diagram shows the usual configuration for the output of this circuit. When the CB opens conduction ceases.

NOTE: As generally used in the 1620, one input pin is not connected to any potential (Floating). In this case a +S level to the other pin will cause conduction as described above.

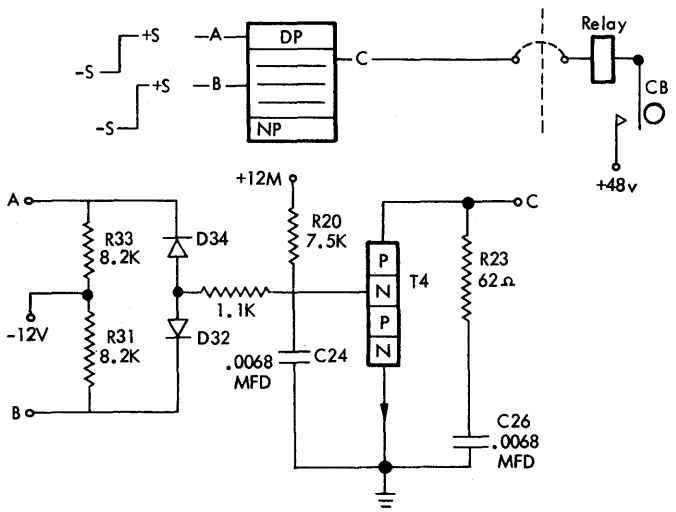


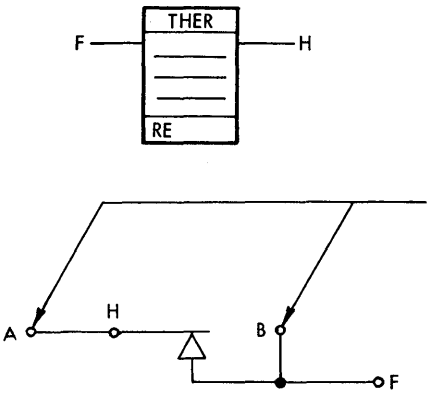

Figure 4-26. CTRL Driver, Relay, Thyratron

## QU Cards

These differential amplifier cards are used in some power supply regulators. All SMS power supplies in the 1620 are referenced to ground. Refer to IBM Customer Engineering Manual of Instruction, 60-Cycle SMS Power Supply (Form 225-6478).

## RE Card

This card is used in the SMS gates to check temperature. The thermal switch opens at 122°F, causing the power supply to sequence OFF (Figure 4-27).




Pins A and B are not Inputs or Outputs
They Insure Positive Identification
When This Card is Accidently
Substituted for 371696, 371697 and
371698

Figure 4-27. Thermal Switch

## TAF Card

This one megacycle oscillator card provides the basic timing pulses for the 1620 clock.

## TAJ Card

There are two AC set inputs per state (OFF or ON) with each input single gated. There is also a provision for DC set and reset (Figure 4-28).

Operation (Figure 4-29)

Assume T3 is OFF and T1 is ON. Then the output of T3 is about — 10 v (driving no external loads) and the output of T1 is ground (+S). The anode of D23 is at — 12 v because of R22 and the anode of D4 is at ground because of R2.

T3 is held OFF by R32 and T1 is held ON by R30 and R28. A 6-v positive shift at the input is passed through C24 and C3 causing the anode of

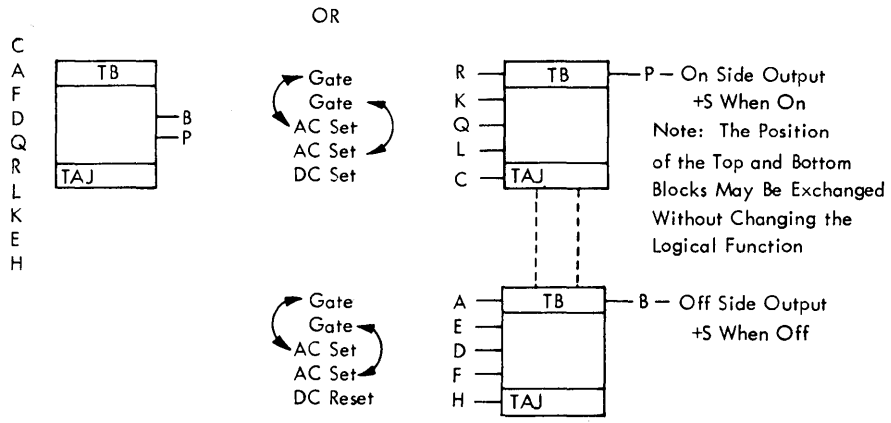
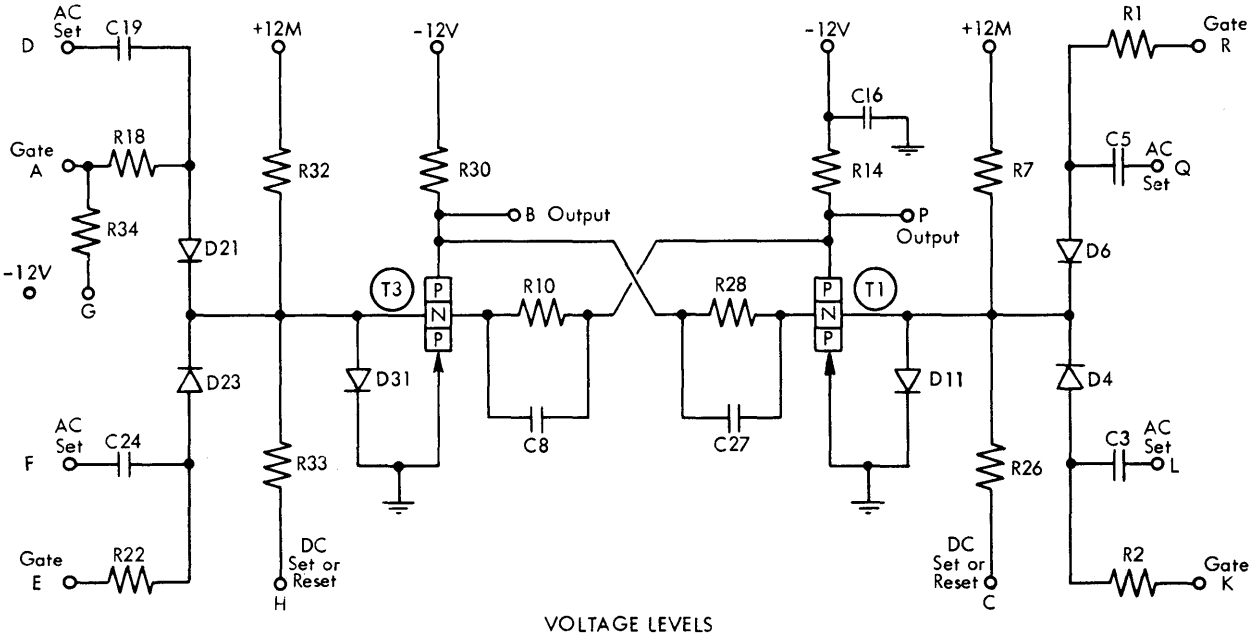



Figure 4-28. SDTRL Trigger, Binary (Block)




VOLTAGE LEVELS

| | | | | | |
|---|---|---|---|---|---|
| AC Set: | | Min. 4.5V Shift (Positive)<br>Max. 5V Shift (Positive) | DC Set or Reset | Up Level: | Max. 0V<br>Min. -0.65V |
| DC Gate | Up Level: | Max. 0V.<br>Min. -0.6V | | Down Level: | Max. 6.87V<br>Min. -12.48V |
| | Down Level: | Max. -6.87V<br>Min. -12.48V | Output Levels DC | Up Level: | Max. -0.1V<br>Min. -0.6V |
| | | | | Down Level: | Max. Depends on Load<br>Min. -9.96V |

Figure 4-29. SDTRL Trigger, Binary (Schematic)

both D23 and D4 to shift positive. Since D23 is back biased by 12 v, the 6-v shift does not get through to the base of T-3. However, since D4 was zero biased the 6-v shift causes the base of T1 to go positive, turning off T1. When T1 goes OFF, R14 and R10 cause T3 to go ON, which in turn holds T1 OFF by nature of the voltage divider formed by R7 and R28. The voltage conditions at the anode of D23 and D4 are now reversed and the trigger is ready for the next positive shift.

By applying a negative level to either R33 or R26 (DC set or reset), the corresponding side of the trigger may be turned on.

The additional AC set and gates are provided to increase the logical flexibility of the trigger.

A +S applied to pin P will turn on the trigger by "collector pull-on."

A +S level applied to pin B will turn off the trigger by "collector pull-off."

## TAL Card

This sample pulse generator card provides a positive going pulse of a definite duration suitable for driving several SDTRL binary triggers (Figure 4-30).

The sample pulse generator requires a +S gate applied to pin C and a positive shift (AC set) applied to pin BA or BE to obtain a +S pulse output at pin D. Pin C can be tied to ground, thereby supplying a continuous gate. The +S gate must be applied a minimum of 0.7 μsec prior to the AC set or shift pulse. The output waveform is shown in Figure 4-31.

## TCZ Cards

Each card contains two latches which are logically and functionally independent. Each latch is shown on the system diagrams as one block. Therefore,

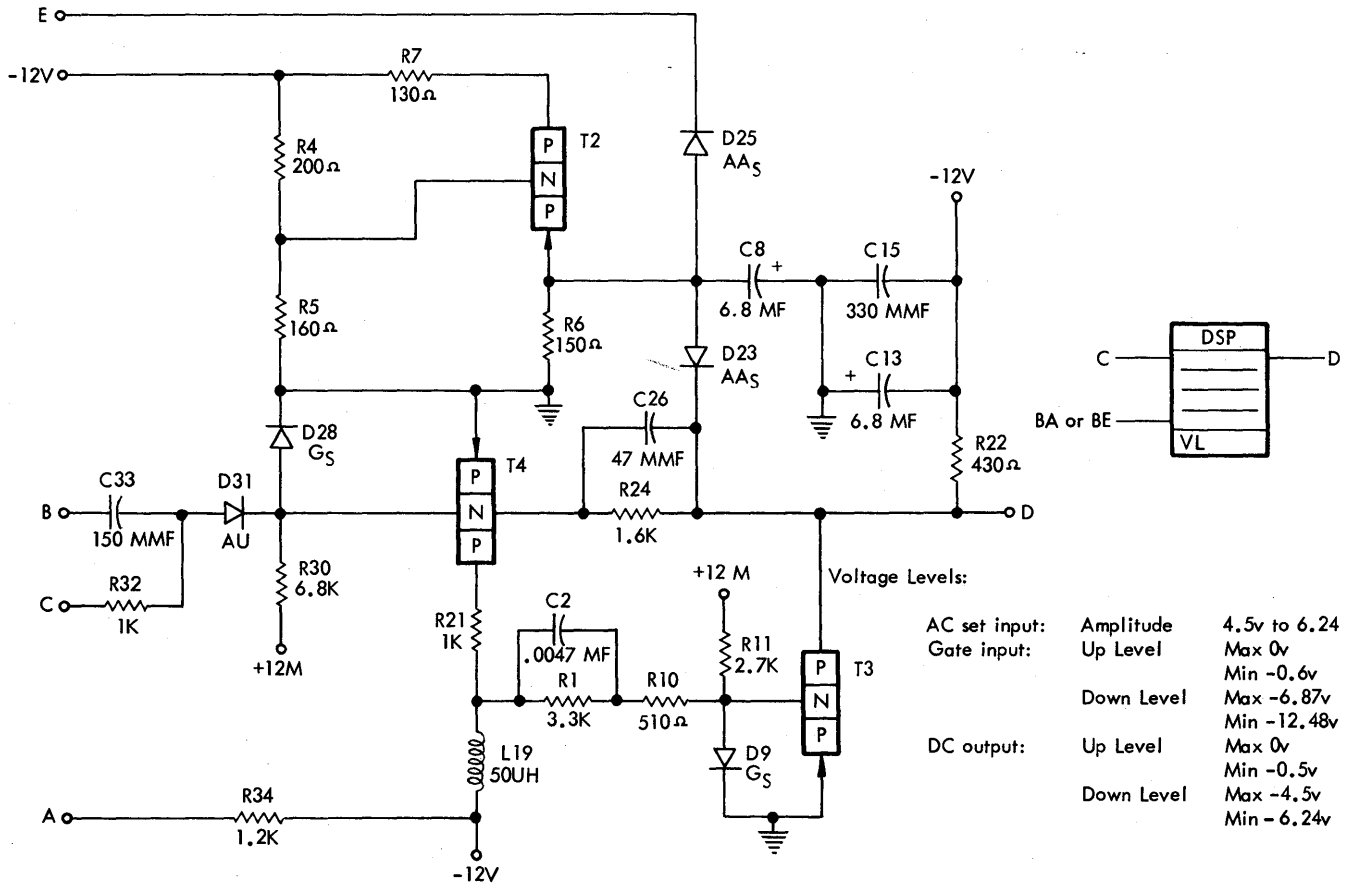



Figure 4-30. SDTRL Sample Pulse Generator

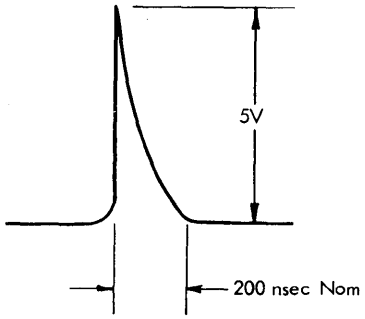



Figure 4-31. Sample Pulse Generator Output Waveform

one TCZ card is represented as two separate blocks on the system diagrams (see Figure 4-32). A — S input to pin K or pin L will turn on latch No. 1. A +S input to pin P will turn on latch No. 1. by collector pullover. Pin C is at a +S level when latch No. 1 is off and is at a — S level when the latch is on. Pin B is at a — S level when latch No. 1 is off and is at a +S level when the latch is on.

Latch No. 2 is turned on by a — S input to the A or G pin. A +S input to pin F will turn on latch No. 2 by collector pullover. Output pin D is at — S when latch No. 2 is on and is at +S when the latch is off. Output pin E is at +S when the latch is on and is at — S when the latch is off. The latches are turned off as follows:

TCZ — S applied to pin Q turns off circuit 1.
— S applied to pin H turns off circuit 2.
— S applied to pin R turns off circuits 1 and 2.

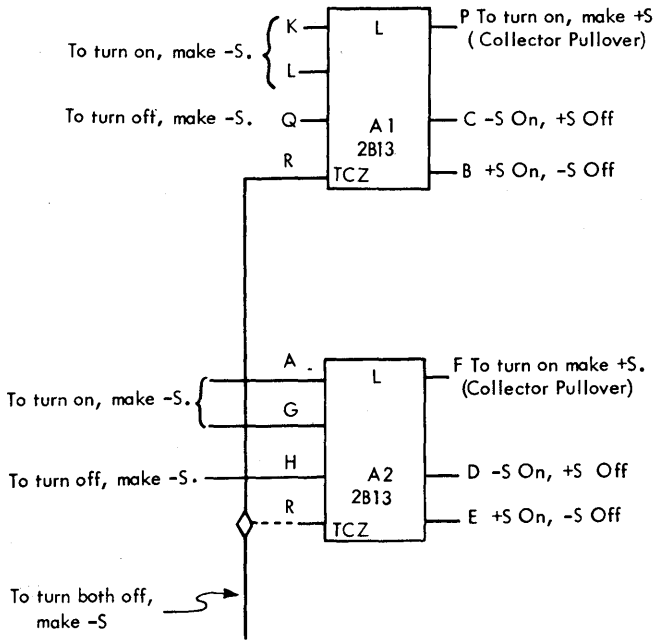



Figure 4-32. TCZ Latch

## TFC Card

This is a power inverter similar to an MH card.

## WJ Cards

These alloy drivers are used as memory inhibit (Z) drivers, MARS bit drivers, MARS read drivers, and MARS write drivers (see Figure 4-33). When the inputs are at +S, a +R level is at the output. When the inputs are at -S, the output goes to a -R level.

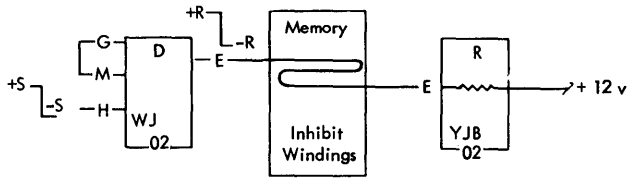



Figure 4-33. Alloy Driver

## WM Card

These cards accept the output of the pre-sense amplifiers, reinforce it, and provide a 1 μsec pulse output to turn on latches in the memory buffer registers (Figure 4-34).

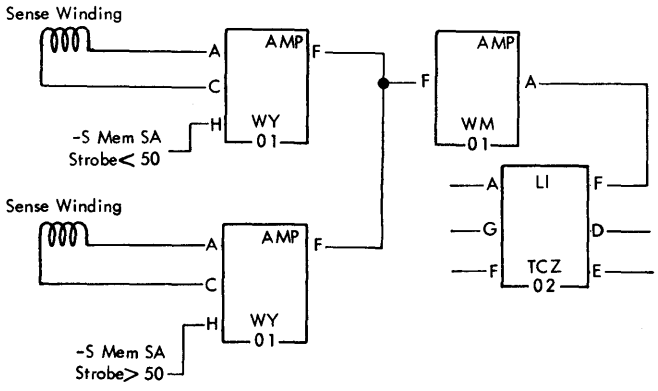



Figure 4-34. Sense Amplifier, Alloy

Typical Voltage Levels and Waveforms
(Figures 4-35 and 4-36)

For input waveform and potentials, see pre-sense amplifier output.

Output waveform and potential of sense amplifier single shot as illustrated in Figure 4-35.

NOTE: When the output of this single shot is connected so as to cause collector pull on of a latch, the waveform as seen on a scope will show the output of the trigger.

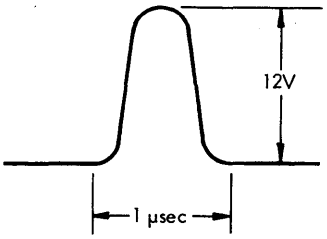



Figure 4-35. Sense Amplifier Output

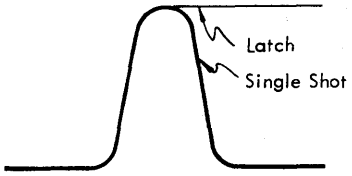



Figure 4-36. Sense Amplifier Connected to Trigger (Collector Pullover)

## WY Card

This card provides a bipolar amplifier to detect and amplify a signal on a sense winding of a memory core plane (Figure 4-37).

Due to the physical position of memory cores, a core flipping to the "zero" state or "one" state can induce a positive going pulse or a negative going pulse in the sense winding. The bipolar pre-sense amplifier detects either type of pulse. The memory sense amp strobe discriminates between a read and a write pulse and is timed to select the read pulse only.

Typical Voltage Levels and Waveforms
(Figures 4-38, 4-39, and 4-40)

Figure 4-38 shows the waveforms and potential for pulse generated when a core is flipped. i.e., the

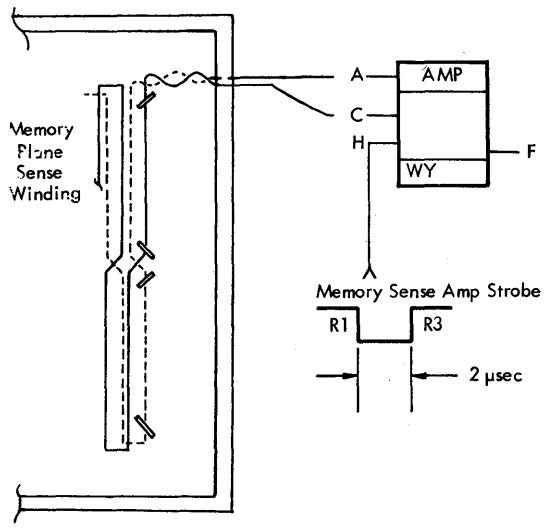



Figure 4-37. Pre-Sense Amplifier, Alloy

selected core is on the "one" state and flips to the "zero" state.

Figure 4-39 shows the waveform and potential for pulse generated when a core is selected but does not flip, i.e., the selected core is in the "zero" state and the currents applied are in a direction such as to try to flip the core to the "zero" state.

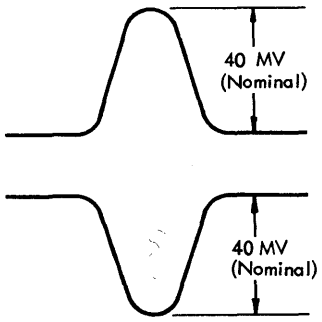



Figure 4-38. Memory Core Output - Flip

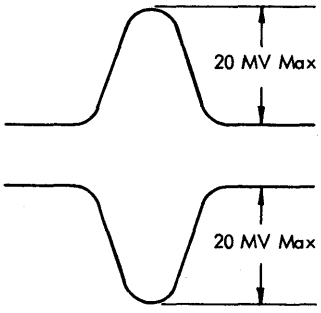



Figure 4-39. Memory Core Output - No Flip

NOTE: These waveforms and potentials apply at "write" time also. However, the memory sense amp strobe is not present at write time and there is no output from the pre-sense amplifier (Figure 4-40).

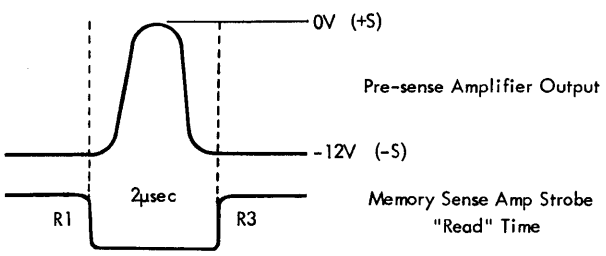



Figure 4-40. "Read" Time

YGB and YGC Cards

These cards provide overvoltage protection for the 12 v and 36 v SMS power supplies in the 1620. Refer to IBM Customer Engineering Manual of Instruction, 60-Cycle SMS Power Supply (Form 225-6478).

YGH, YGJ, and YGN Cards

These differential amplifier cards are used in the SMS power supplies. All SMS power supplies in the 1620 are referenced to ground. Refer to IBM Customer Engineering Manual of Instruction, 60-Cycle SMS Power Supply (Form 225-6478).

YJA and YJB Cards

These resistor cards are used for loading or terminating circuits.

POWER SUPPLIES

The 1620 requires an input voltage at 208 v AC or 230 v AC. The 208 v supply can vary between the limits of 187 v and 228 v and the 230 v supply can vary between 207 v and 253 v.

SMS Power Supplies

The internal functions of the individual SMS power supplies and the theory of ferroresonant regulator transformers are discussed in the IBM Customer Engineering Manual of Instruction, 60-Cycle SMS Power Supply (Form 225-6478). For normal operation, the 1620 SMS power supply DC output voltages must be maintained within the following levels:

| | | |
|---|---|---|
| +12 | from +11.52 to +12.48 | |
| +48 | from +43.20 to +52.80 | (Measured at power supply) |
| −36 | from −34.56 to −37.44 | |
| −12 | from −11.52 to −12.48 | |
| + 3 | from + 2.94 to + 3.06 | |

All machine functions must operate correctly when the +12M DC supply is set between +10.2 and +13.8 (marginal test).

Power-On Sequence (Figure 4-41)

The following describes the sequence, objectives, and functions of operations necessary to place the 1620 in a ready status.

Power Circuit Breaker (PCB) On

Objectives:

1. Apply voltage to convenience outlets.
2. Put the "Normal" relay, R105, under control of:
   a) R104 which in turn is controlled by the gate and memory overtemp thermal trips
   b) SMS power supply overload trip CB contacts
3. Supply 24v DC for power-on sequence control circuits and DC monitor circuits.

Turning on the PCB develops 24 and 48v AC. This voltage turns on the thermal light and picks K1. The points of K1 make, supplying voltage to the convenience outlets and to the rectifier which develops 24 v DC for sequencing. The sequencing voltage supplies potential to the console power switch (01.05.03.1). Pressing Reset picks R104 which remains up until the PCB is turned off or a thermal switch opens. When R104 is picked the thermal light goes off and R105 is picked. Relay 104 is under control of the n/c contacts of the over-temp thermostats. Normal power-on and power-off operation does not affect the operation of R104. Therefore, under normal conditions, Reset need be operated only once after the PCB is turned on.

Console Power Switch On

Objectives:

1. Bring DC voltages up to operating levels. These voltages are: −36, −12, +12, +48, ±3, +30. The +30 v, used with memory

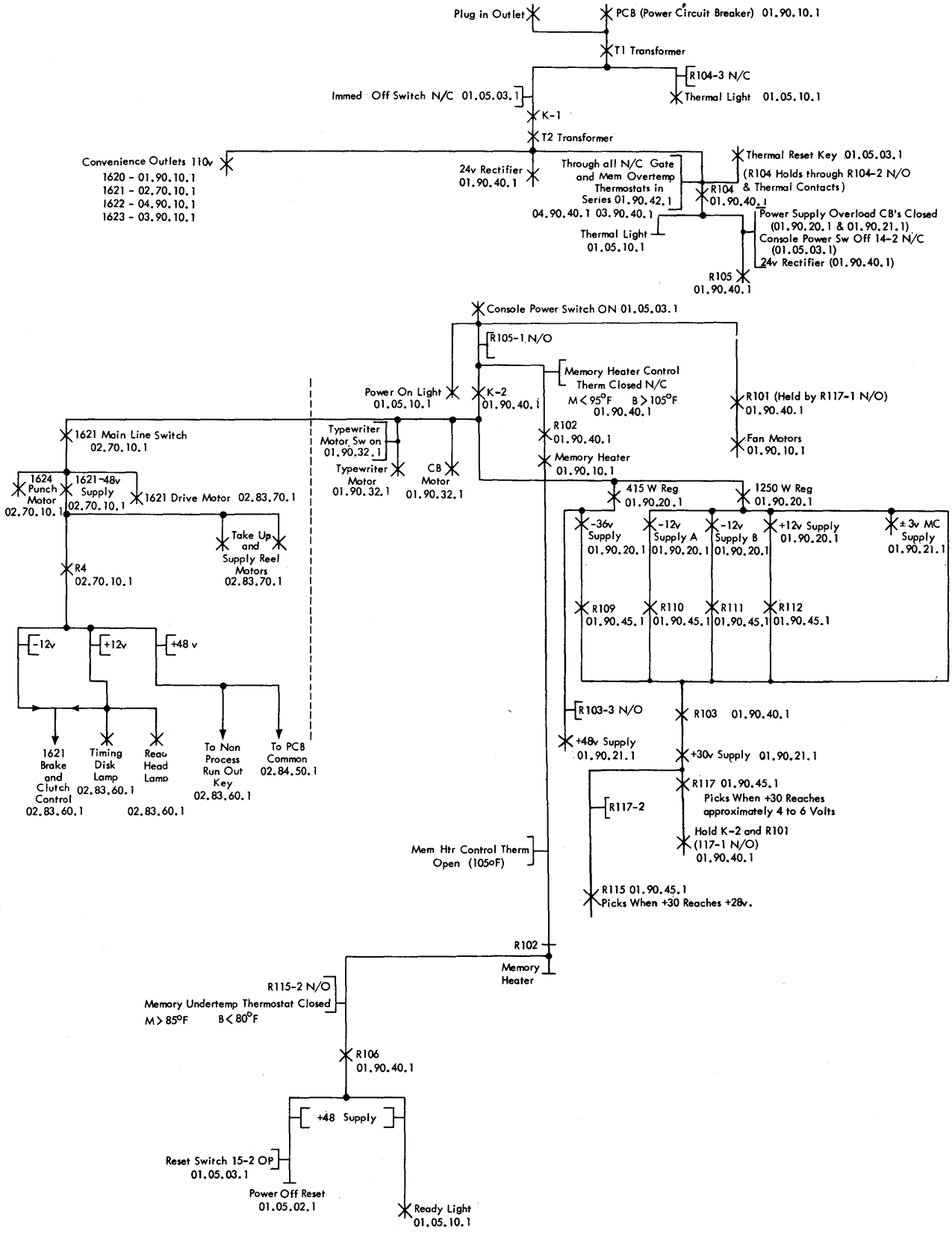



Figure 4-41. Power ON Sequence

addressing circuits, is brought up last to allow all biasing and level setting potentials to be up before the +30 is applied. This prevents the +30 from disturbing memory when it is brought up. The +30 supply is dropped first in a power-off sequence for the same purpose

2. Develop a power-on reset to reset all functional units to their initial condition.
3. Turn on blower fans and CB drive motor.
4. Provide operating potentials to additional feature units as required.
5. Place the memory heater and heater control relay (R102) in operation.
6. Provide a computer ready indication, the "Ready" light.

Operation of R105, R102, and the Memory Heater

Relay 105 is picked through R104-1 n/o, all SMS power supply overload trip contacts n/c, and the console power switch n/c. A circuit through R105-2 n/o parallels the power switch n/c points to hold R105 when the power switch is turned on. Turning on the console power switch picks R101, R102, and K2. Closing the R102-3 n/o causes the memory heater to operate. The heater will continue to function until the temperature rises to 105°. At that time, the heater control thermostat will open to drop R102. The dropping of R102 turns off the heater and permits the pick of Ready R106 through the R115-2 n/o points and the memory undertemp thermostat. This puts the machine in a ready status and assures proper functioning of the cores.

The memory heater will now maintain a core temperature of 95° to 105°F as controlled by the memory heater control thermostat and Relay 102.

Power-On Reset

When the – 12 v supply "B" is established, the machine reset lines become operative and reset all machine units. This reset will remain in operation until the Ready relay (R106) is picked indicating the machine is ready for functioning.

Power-Off Sequence

The following gives the status of the power supplies and control circuitry prior to, and after, a power-off sequence. Turning off the console power switch is the normal way to cause a power-off sequence. The other power-off sequences are for machine failure conditions and immediate off switch operation.

Console Power Switch Turned Off (Figure 4-42)

The 1620 is in a normal ready status prior to turning off the console power switch.

Relays picked: 101, 102 (depending on memory temperature), 103, 104, 105, 106, 109, 110, 111, 112, 115, 117, and K1, K2
All voltages are at operating level.
CB motor and blower motors operating.
Potential supplied to any attached special feature units as applicable.
Power-on light ON.

Status after power off sequence:

Relays picked: 104, 105, and K1.
24 v sequencing remains up.
Convenience outlet voltage remains up.

Thermal Overtemp Trip (Figure 4-43)

The 1620 is in a normal ready status prior to thermal overtemp trip.

Status after power-off sequence:

Relays picked: 101 and K1.
24 v sequencing remains up.
Fan motor operating.
Thermal light ON.
Power on light ON.
Convenience outlet voltage remains up.

Restoring Procedure. Procedure for restoring 1620 to the ready condition after thermal trip is as follows:

1. Clear condition causing thermal trip.
2. Press Reset key (picks R104).
3. Turn off console power switch then on to get normal power-on sequence. Turning off the console power switch completes a circuit through R104-1 n/o and the DC monitor network to pick R105.

SMS DC Power Supply Overload Trip (Figure 4-44)

The 1620 is in a normal ready status prior to power supply overload trip.

Status after power-off sequence:

Relays picked: 104, 101, and K1.
24 v sequencing remains up.
Convenience outlet voltage remains up.
Fan motors operating.

NOTE: If the overload should trip on one of the 12 v supplies, it can cause data in memory to be disturbed due to the +30 supply dropping after the 12 v supply.

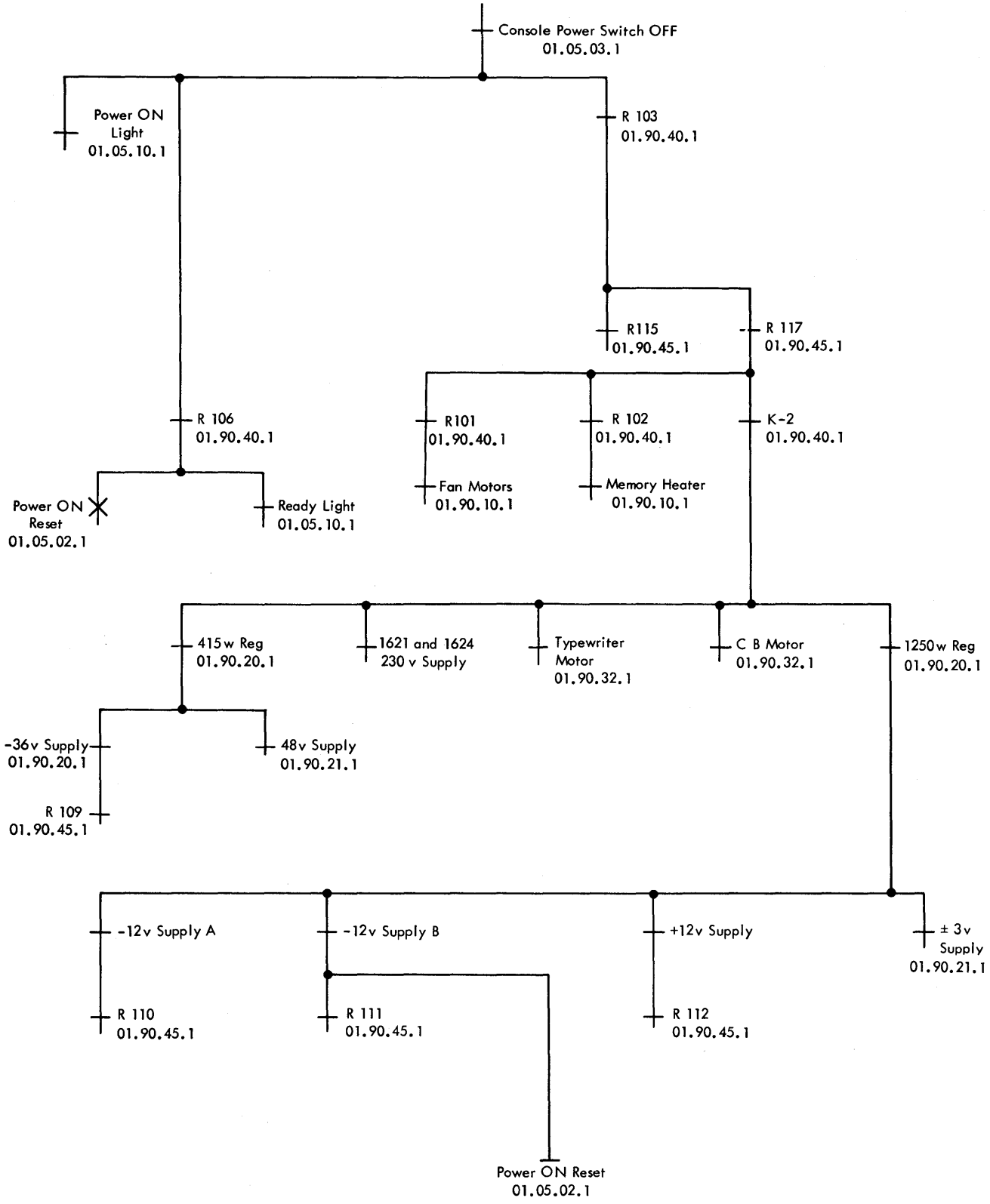



Figure 4-42. Console Power Switch OFF

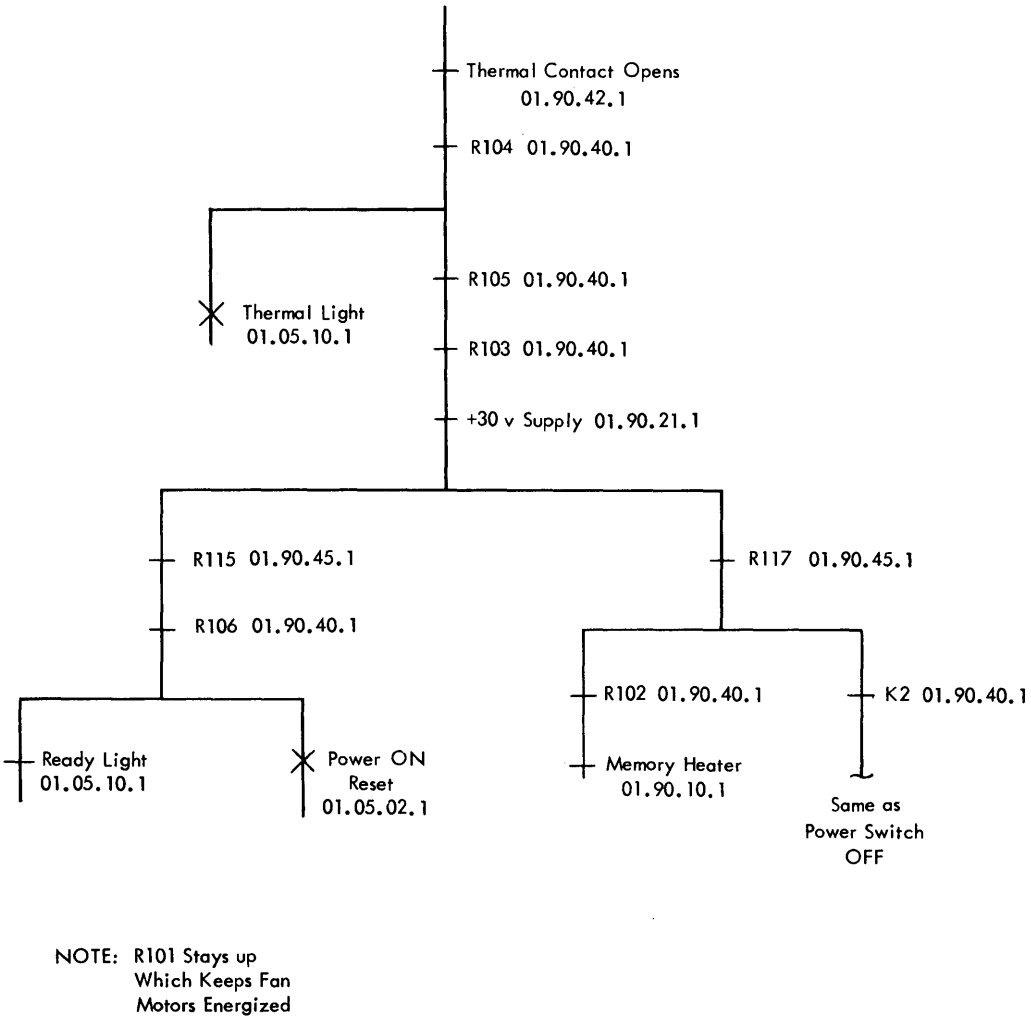



Figure 4-43. Thermal Overtemperature Trip

Restoring Procedure. Procedure for restoring 1620 to the ready condition after an overload trip is as follows:

1. Remove cause of overload.
2. Restore power supply circuit breaker.
3. Turn off console power switch then turn it back to get normal power-on sequence.

Loss of 24 v DC Sequencing Control

This allows random dropout of relays. Data in memory could be disturbed. The thermal light is turned on and convenience outlets remain up.

"Immediate Off" Switch Activated

This allows random dropout of relays which could disturb data in memory. The power-on light remains on and the thermal light is turned on.

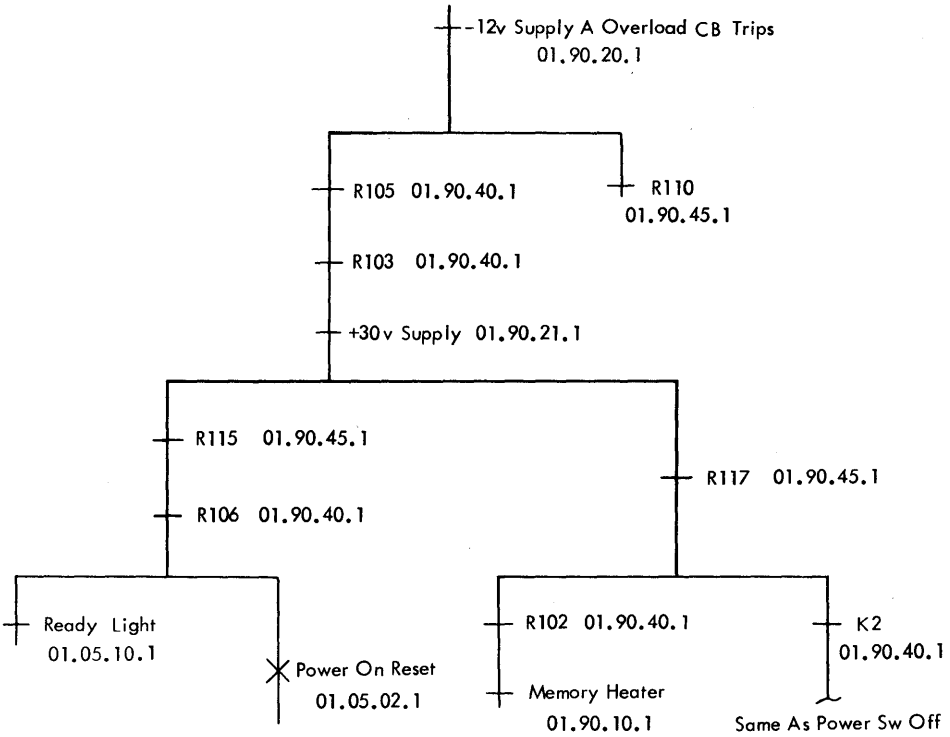



Figure 4-44. SMS DC Power Supply Overload Trip

## CLOCK AND TIMING CHART

A one-megacycle free running crystal oscillator is the basic pulse generator for the machine.

The output of the crystal oscillator is connected to both the ON and the OFF side inputs of a binary trigger for the development of clock drive pulses. When the trigger is turned on, a clock drive "A" pulse is developed. One microsecond later when the trigger is turned off, a clock drive "B" pulse is developed. Clock drive A and B pulses are developed alternately in this manner as long as the Run trigger is ON and the Hold trigger is OFF. (The Hold trigger is used in input-output operations to synchronize the input-output device with the computer.) See Figure 5-1.

The clock ring is composed of ten triggers which are turned on at 1-$\mu$sec intervals and remain on for 10-$\mu$sec each. The ten triggers are turned off at 1-$\mu$sec intervals and remain off for 10-$\mu$sec each. The odd-numbered Clock triggers (C-1, C-3, C-5, C-7, and C-9) are turned on and off by clock drive B pulses "ANDed" with the outputs of even-numbered Clock triggers. The even-numbered Clock triggers (C-2, C-4, C-6, C-8, and C-10) are turned on and off by clock drive A pulses ANDed with the outputs of odd-numbered Clock triggers. The time required to complete a clock ring cycle is 20-$\mu$sec.

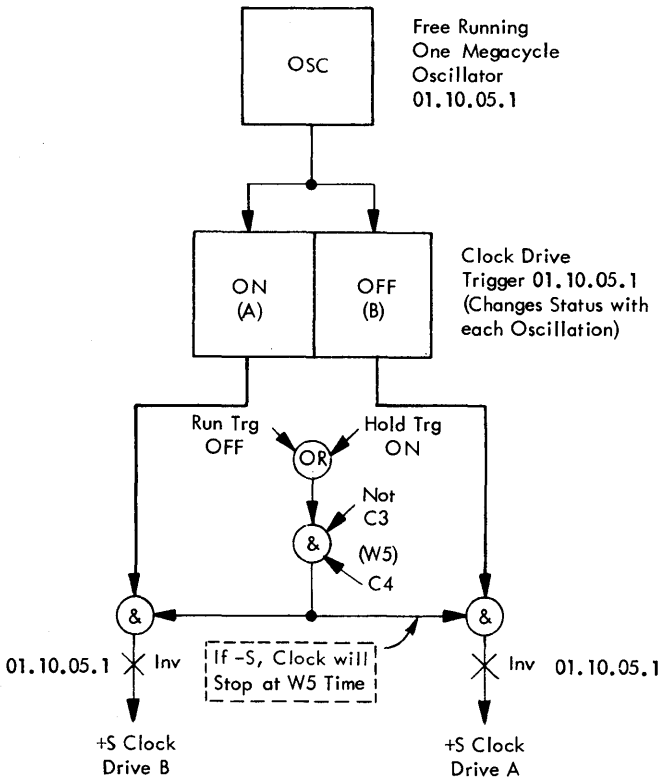



Figure 5-1. Clock Drive

Beginning with the clock drive B pulse which turns on Clock trigger C-1, the start of consecutive microsecond intervals are designated $R_0$ through $R_6$, $W_0$ through $W_6$, and $T_0$ through $T_5$. $T_5$ is followed by $R_0$.

Figure 5-2 shows a function chart and Figure 5-5 a sequence chart for the Clock triggers.

The outputs of two of the ten Clock triggers are ANDed to develop required pulses and gates from 1-$\mu$sec to 19-$\mu$sec in duration. Three examples are shown in Figure 5-3.

A machine cycle has a duration of 20-$\mu$sec and consists of one clock ring cycle. The functional cycle in the computer is defined as a memory cycle and consists of a machine cycle which begins at $W_6$ clock time under control of the A/B trigger. Each memory cycle is a complete operation with respect to memory: that is, memory is addressed, read out of, and written into within the cycle.

The ON-OFF status of the A/B trigger is changed each memory cycle when the C-7 Clock trigger is turned on ($R_6$ clock time) for the development of "A-advance" and "B-advance" pulses (Figure 5-4). When the A/B trigger is turned on at $R_6$ time of a particular memory cycle, an "A-advance" pulse is developed at $W_6$ time and the A/B Auxiliary latch is turned on. On the following memory cycle, the A/B trigger is turned off at $R_6$ time (ANDed with the A/B Auxiliary latch ON). With the A/B trigger off, a "B-advance" pulse is developed at $W_6$ time and the A/B Auxiliary latch is turned off. The next $R_6$ time turns on the A/B trigger to restart the sequence. "A-advance" and "B-advance" pulses are developed in this manner on alternate memory cycles as long as the clock continues to run, or until CE Switch 10 or the Display Address trigger is turned on thus blocking the turn on of the A/B trigger. The line labeled TR30 NOT RA OPR 80 is used with a special

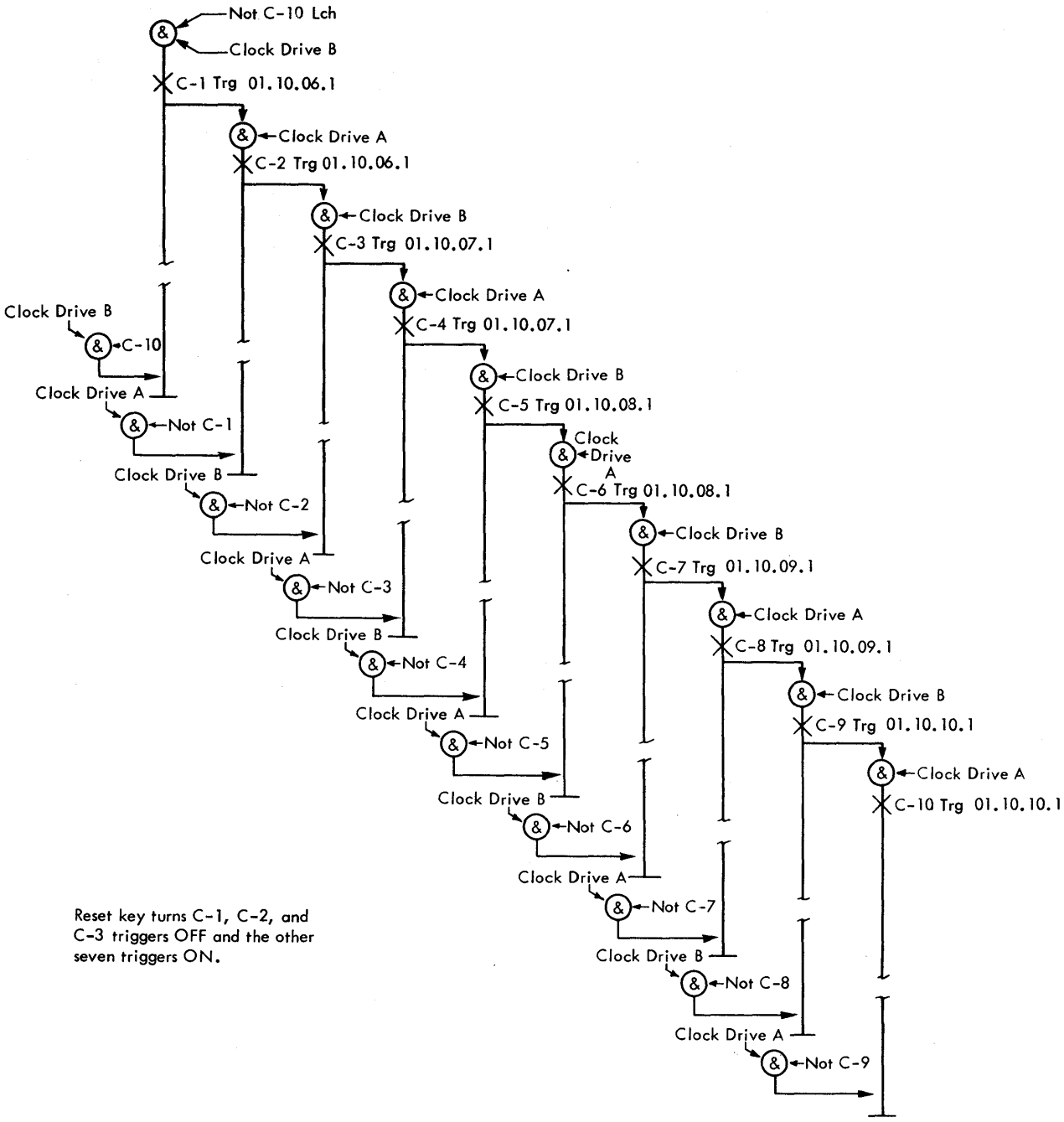



Figure 5-2. Clock Trigger Sequence

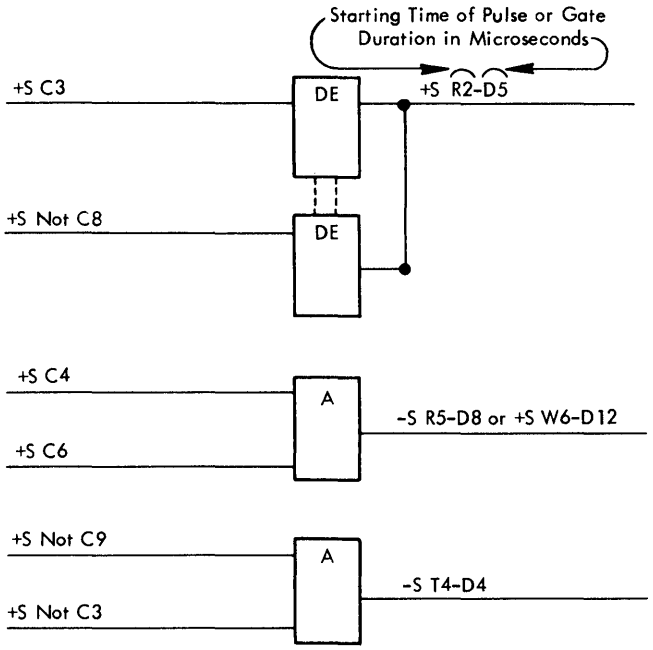



Figure 5-3. Development of Timing Gates

feature (1710-F2). The "A-advance" and "B-advance" pulses are used to initiate alternate memory cycles (Figure 5-5).

Figure 5-6 shows the timing chart for machine operation.

Figure 5-7 illustrates the functions and timings for the reading of a memory address from MARS into MAR and the writing of the address from MAR back into MARS incremented or decremented.

Figure 5-8 illustrates the functions and timings for reading from memory, setting MBR and MDR, and writing back into memory.

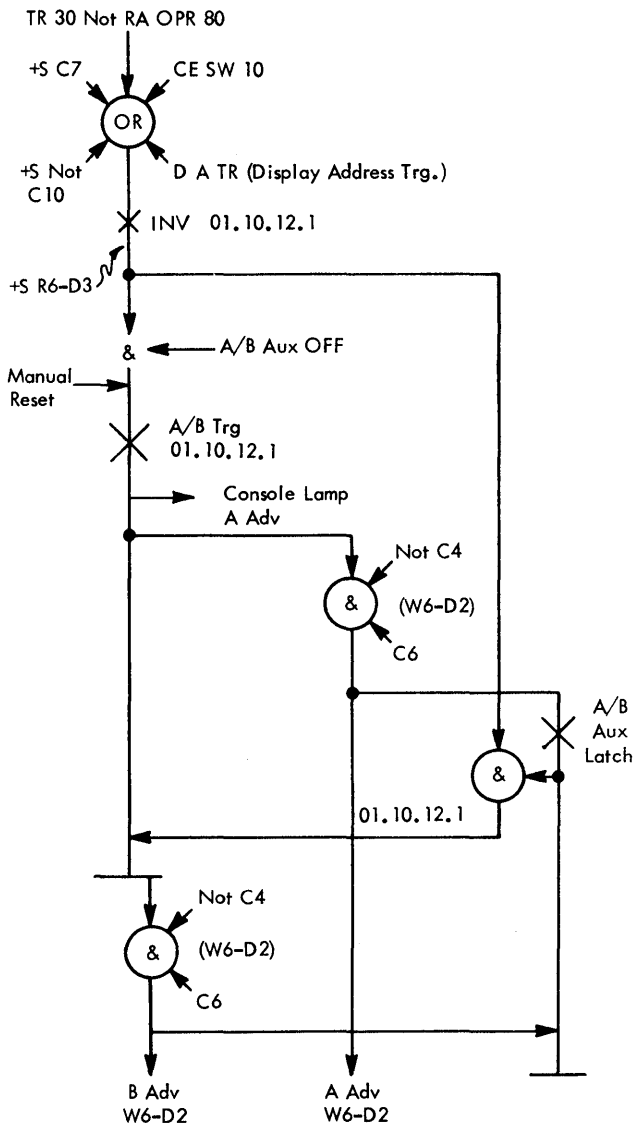



Figure 5-4. A/B and A/B Auxilliary Triggers (Latches)

## MEMORY

Memory (Core Storage) is a three-dimensional, coincident-current core storage system using ferrite core. It consists of 12 planes of 10,000 cores each in a 100 x 100 square matrix. From front to back of the IBM 1620 machine, the planes are arranged as follows (Figure 5-9):

| | |
|---|---|
| Plane 1 | 1-bit odd addresses |
| Plane 2 | 1-bit even addresses |
| Plane 3 | 2-bit odd addresses |
| Plane 4 | 2-bit even addresses |
| Plane 5 | 4-bit odd addresses |
| Plane 6 | 4-bit even addresses |
| Plane 7 | 8-bit odd addresses |
| Plane 8 | 8-bit even addresses |
| Plane 9 | F-bit odd addresses |
| Plane 10 | F-bit even addresses |
| Plane 11 | C-bit odd addresses |
| Plane 12 | C-bit even addresses |

Each memory core is threaded by an X and a Y-address wire, a sense wire, and an inhibit wire. The X and Y-wires form a rectangular coordinate system so that a particular pair of X and Y-wires in one plane will intersect at just one core (Figure 5-10). The core is selected by driving a half-select current ($1/2\ I_m$) along each of the two wires. Corresponding X and Y-wires for each of the 12 planes are connected in series (Figure 5-11).

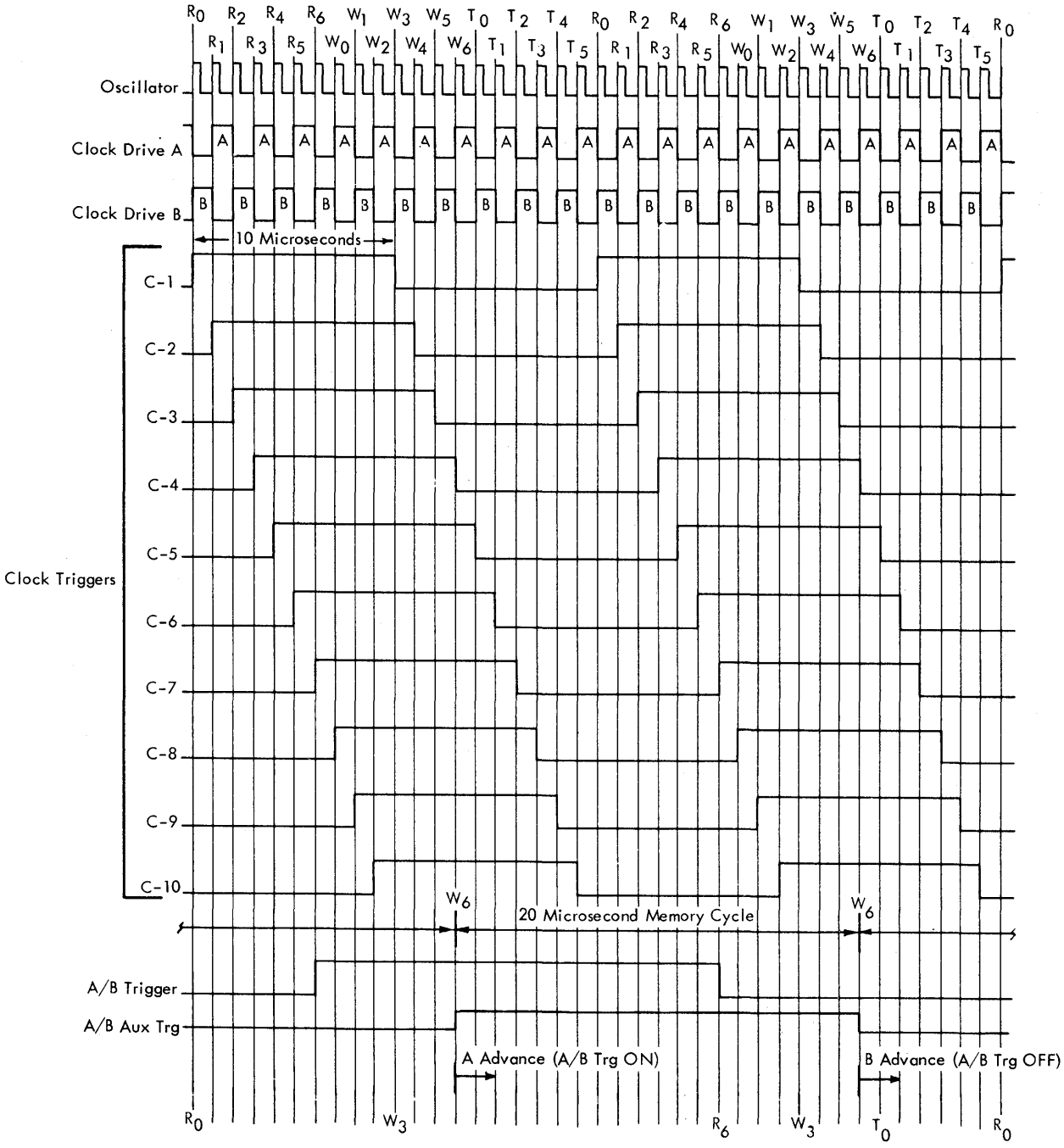



Figure 5-5. Clock Sequence and Timing Chart

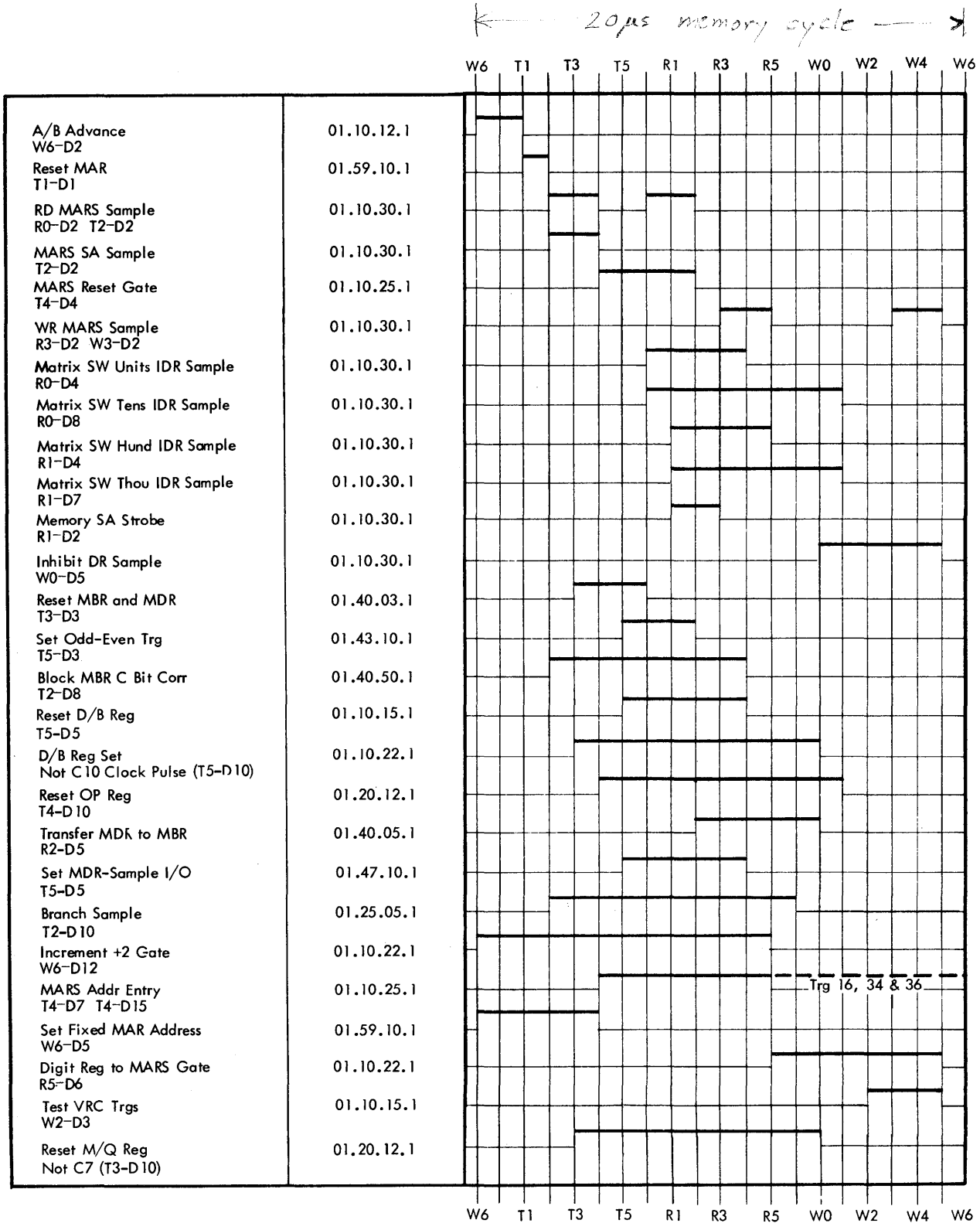



Figure 5-6. Timing Chart, System Memory Cycle

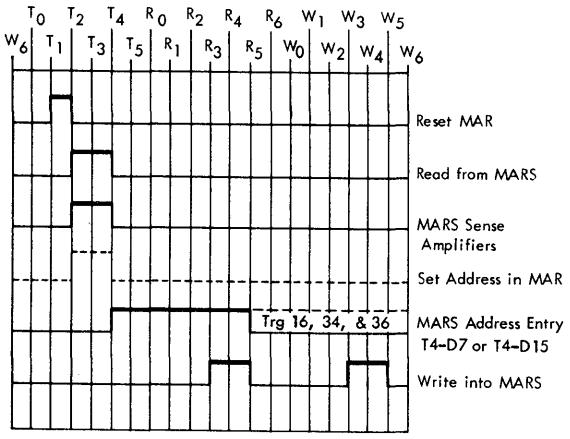



Figure 5-7. MARS-MAR - Increment/Decrement MARS Timing

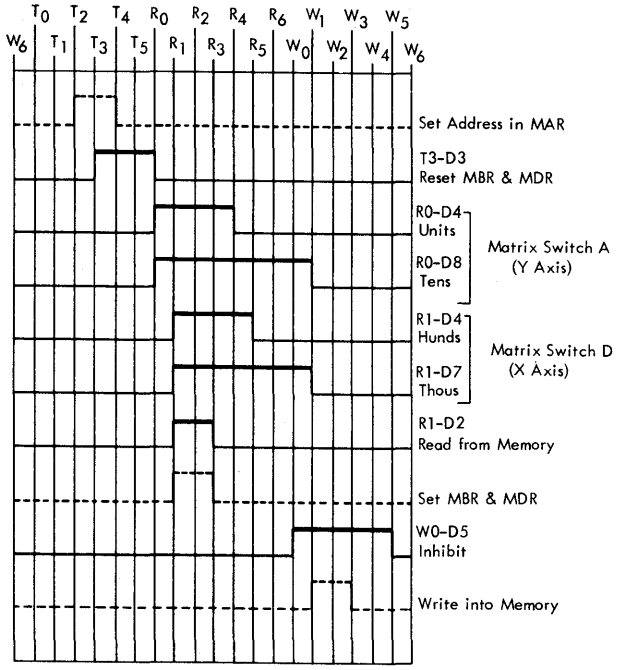



Figure 5-8. Memory Read and Write Timing

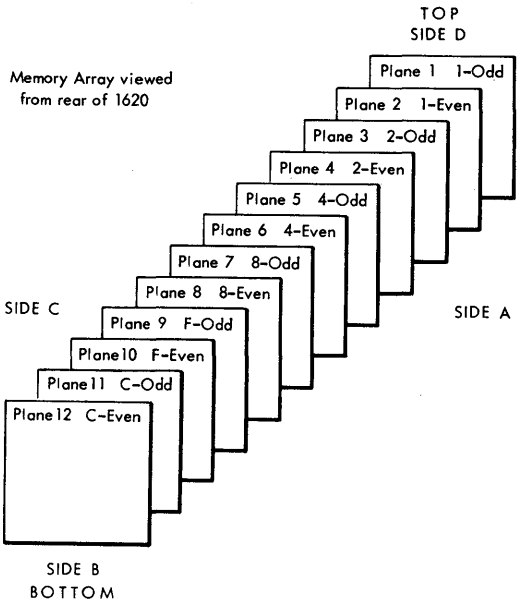



Figure 5-9. Memory Array

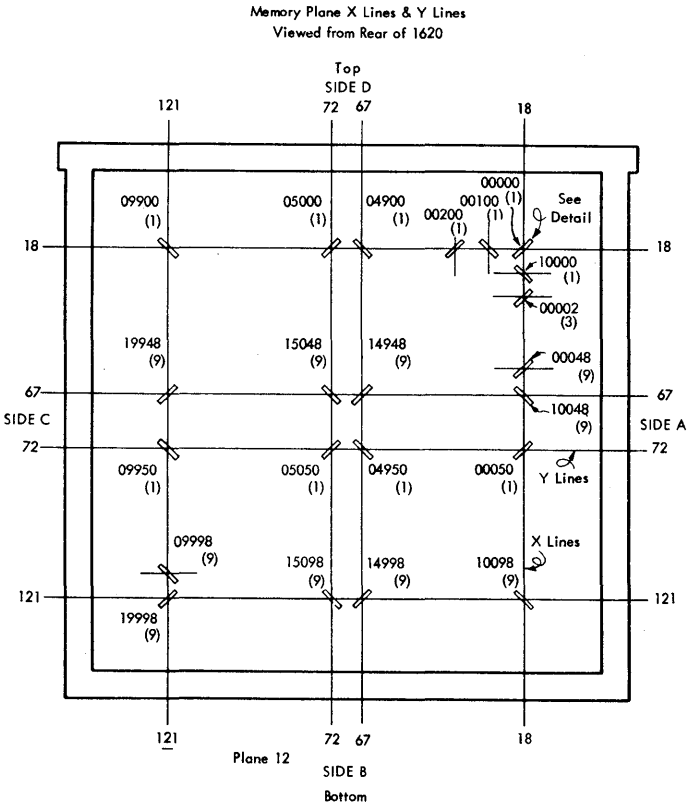



Figure 5-10. Memory Plane

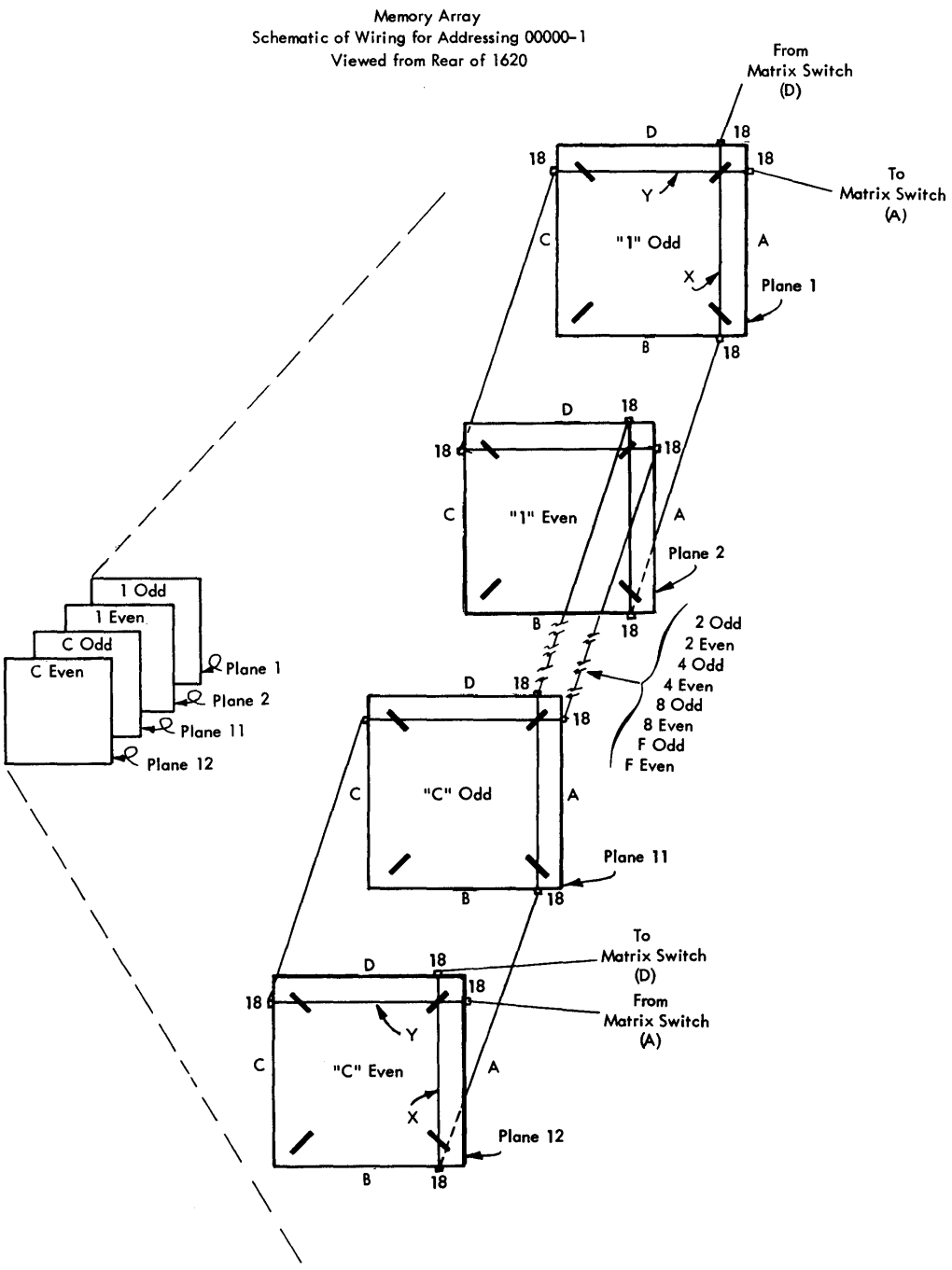



Figure 5-11. Memory Array - Schematic of Wiring

Each of the 12 planes has a sense winding that in effect passes through every core in that plane. The sense winding of each plane is wound in a figure eight pattern and is physically divided into two parts, above 50 ($>50$) and below 50 ($<50$), resulting in two windings per plane. The output of each of these 24 sense windings is connected to a bipolar pre-sense amplifier. Each pair of pre-sense amplifiers associated with a given plane is then connected to a sense amplifier. The output of the sense amplifier is used to set a latch in MBR. Figure 5-12 shows the detail of a single memory core with all windings in place.

The output of a sense winding at "read" time can be either a positive going pulse or a negative going pulse depending upon the physical positioning of the cores in relation to the X and Y-lines. The output of a sense winding is connected to a bipolar pre-sense amplifier which can accept pulses of either polarity. The sense winding will also have a positive going or negative-going pulse induced in it at "write" time. Discrimination between "read" and "write" is accomplished by gating the pre-sense amplifier with a "memory sense amp-strobe," so that pulses during "read" time only will be amplified and used to set an MBR latch.

To clear a location in memory, the memory sense amp-strobe is blocked from reaching the pre-sense amplifiers. Under this condition an MBR latch will not be set. Control of the memory sense amp-strobe is exercised by the "Read-Y Point" or "Block Memory SA" (Read Z). When the machine function calls for clearing a single location, odd or even, the "Read Y Point" is used. "Read-Y Point" blocks the sense amp-strobe, either odd or even, depending on whether the address in MAR is odd or even. "Block Memory SA" blocks the sense amp-strobe to all pre-sense amplifiers (odd and even), regardless of the address in MAR. This effectively clears two locations in memory at one time (Figure 5-15).

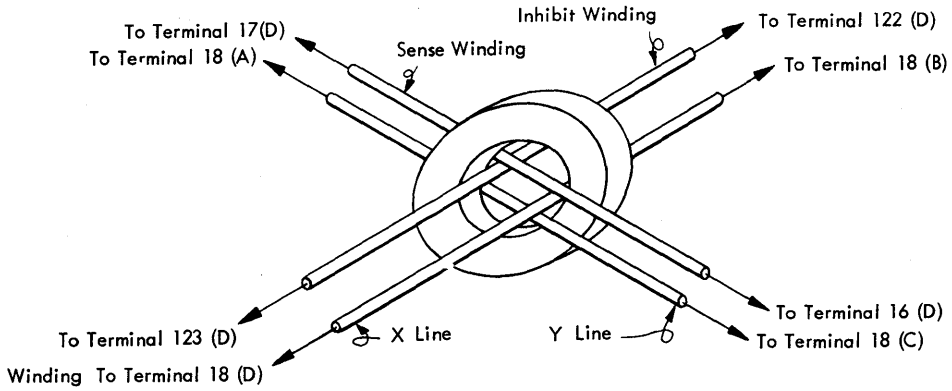
See Figures 5-13 and 5-15 for sense winding configuration and control of pre-sense amplifiers.

Each of the 12 planes also has an inhibit winding that in effect passes through every core in that plane. The inhibit winding of each plane is physically divided into two parts, resulting in two windings per plane. The two windings are wired in series and act as one. Both are controlled by one of the 12 latches in the Memory Buffer Register. See Figure 5-14.

During the "read" part of the memory cycle, a current is sent along an X and a Y-line which intersect at the selected core in each of the 12 planes. Each line carries $1/2\ I_m$ current.

The combined field of the X and Y-lines reverses the magnetic polarity of the core if a "one" is stored but does not affect the polarity if a "zero" is stored. When a "one" is read out, the change in polarity induces a voltage pulse in the sense winding which is rectified, amplified, and used to set a latch in MBR. The contents of 12 selected cores are thus stored in the 12 latches comprising MBR. The outputs of the MBR latches condition the inhibit drivers.

During the "write" portion of the memory cycle, a "one" is written back into all the selected cores unless prevented by the inhibit winding. "Writing" is accomplished by sending a $1/2\ I_m$ current along the selected X and Y-lines in the opposite direction from the read currents. If it is not desired to write a "one" in the selected core of a particular plane, a $1/2\ I_m$ current is sent through the inhibit winding of




The Terminals Indicated Apply to the Twelve (12) Cores at Address 00000 and 00001

Figure 5-12. Detail of Core

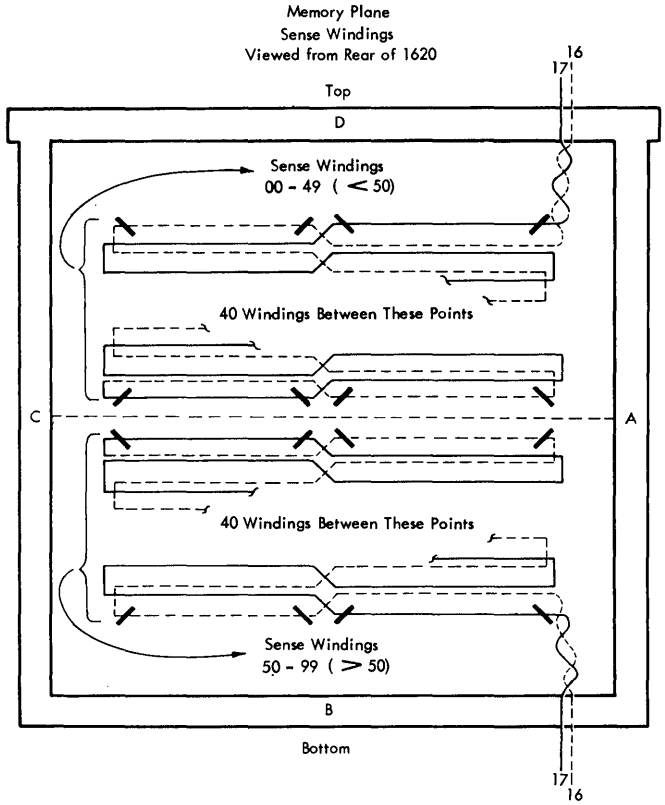



Figure 5-13. Memory Plane - Sense Winding

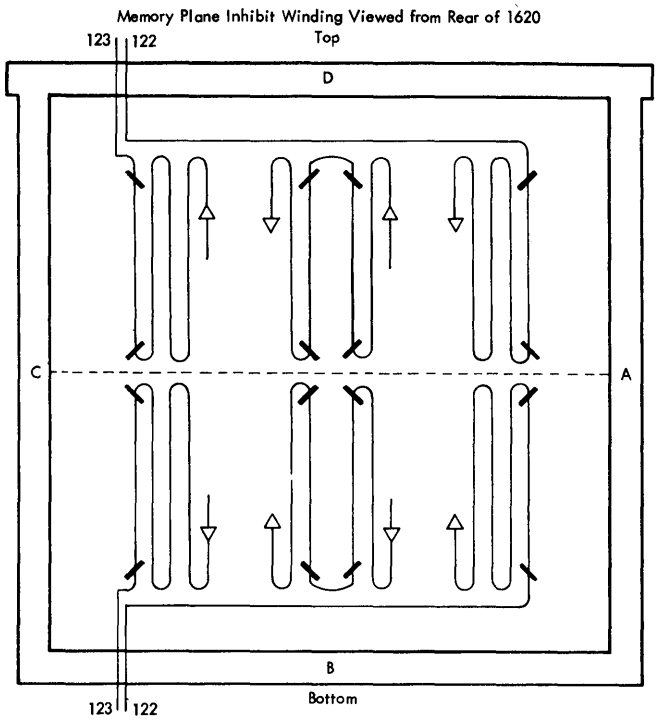



Figure 5-14. Memory Plane - Inhibit Winding

that plane in such a direction as to oppose the write current. The core will therefore remain in its "zero" magnetic state.

The circuitry for selecting memory cores consists of a Memory Address Register (MAR), decoding switches, and a magnetic core matrix switch. Each memory plane has 100 X-lines and 100 Y-lines and it is necessary to select one line of each coordinate. This is accomplished by using two matrix switches, each of which has 100 switch cores arranged in 10 x 10 matrices. Here, as in the memory plane, it is necessary to select one line of each coordinate to select one switch core which in turn is connected to one line serving memory. Thus, by selecting four lines (two per matrix switch), it is possible to select any X and Y-line in memory (Figure 5-16).

The Y' lines of matrix switch A are addressed by the units position of MAR and the Y" lines are addressed by the tens position of MAR. The 1-bit trigger in the units position of MAR is not used for addressing the matrix switches. The 1-bit latch in the ten thousand (10K) portion of MAR is combined with the 8-, 4-, and 2-bit latches in the units position, to distinguish addresses above 10,000 from those below 10,000.

An address in MAR causes the decode switches to present a ground (zero volts) to one end of the Y' - Y", X' - X" lines in the matrix switch. The current source and current drivers under control of a gate will provide +30-v to the other end. The current that flows in each line is capable of reversing the polarity of the switch core ($I_m$). A bias winding carrying $I_m$ is wound on every switch core and is connected in such a manner as to try to maintain the "zero" condition of each switch core. When the Y' and Y" or X' and X" lines are energized (see Figure 5-8 for timing), one line overcomes the effect of the bias winding while the other causes the switch core to reverse its magnetic polarity, or flip, to the "one" state. When the switch core flips to the "one" state, it induces a current pulse by transformer action into the Y or X-lines threading memory. This is the "read" current in memory as previously described. At "write" time for memory the Y' - Y" and X' - X" current is cut off. The bias winding then flips the switch core to its "zero" status. The return of the switch core to its "zero" status induces a current pulse into the X and Y-lines in memory in a direction opposite to that of the "read" current. This current is the "write" current in memory as previously described.

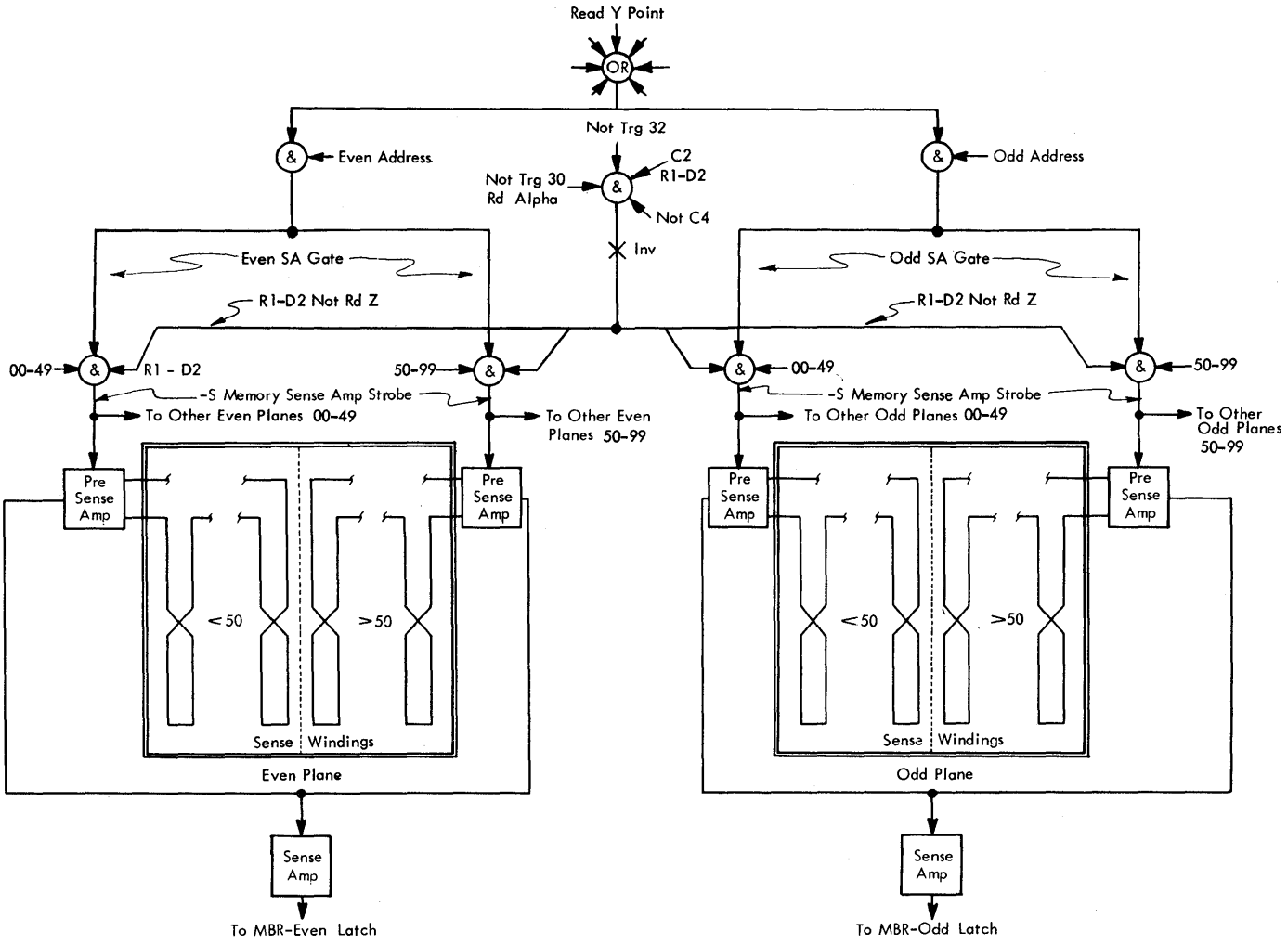



Figure 5-15. Readout Control of Memory Plane

Each odd memory address differs only from the next lower even address by having a 1-bit in the units position. Because the output of the 1-bit latch in the units position of MAR is not used for addressing memory, addresses 00000 and 00001 in MAR actually select the same X and Y-lines in memory. The same thing is true of all even-odd addresses. Due to the 12-plane (2-digit) wiring scheme of memory, an even address will cause the readout of the digit at that specific address and the digit at the next higher odd address. Conversely, an odd address will read out the digit at that specific address and the digit at the next lower even address.

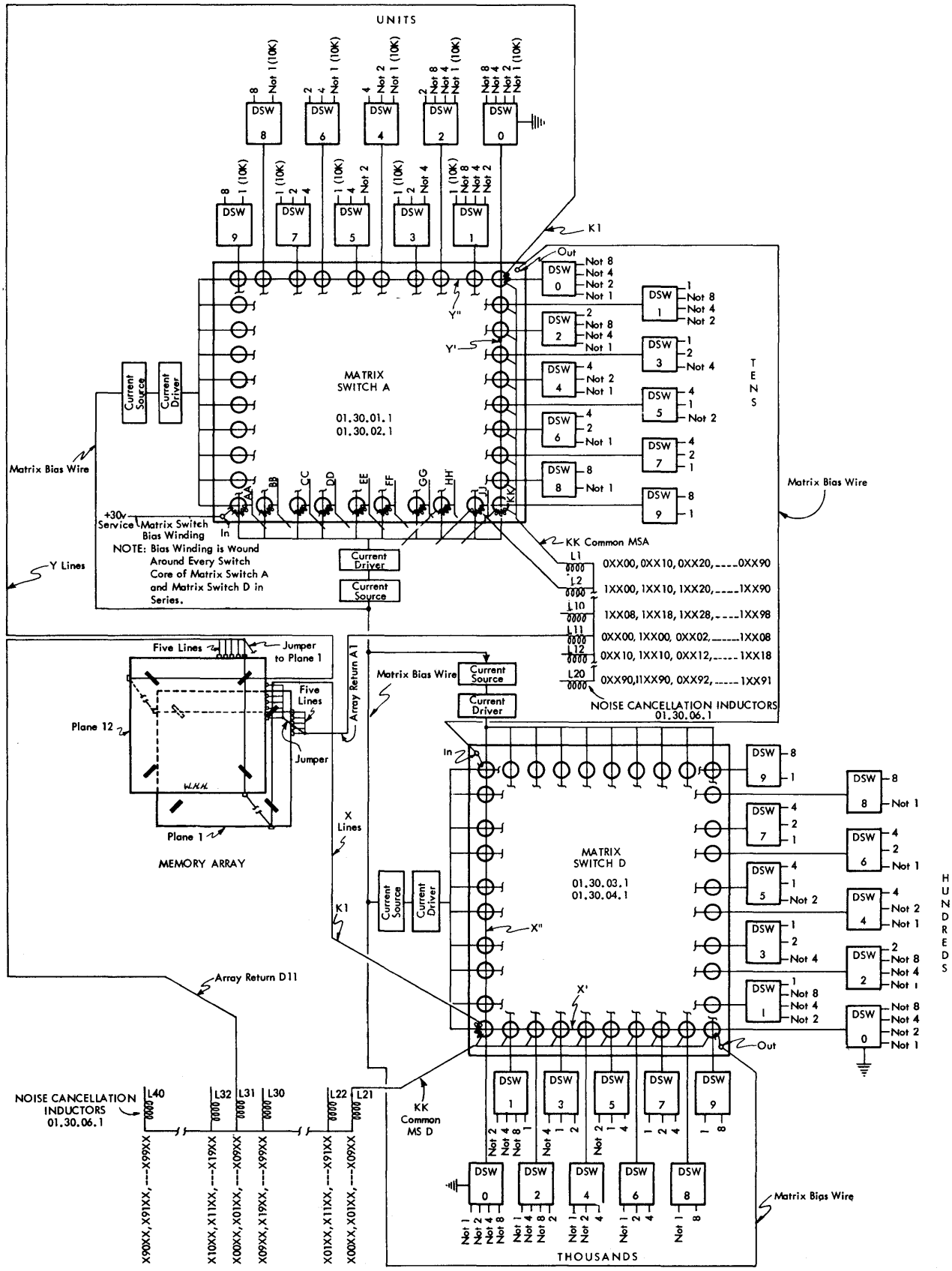



Figure 5-16. Selecting Memory Cores

MEMORY BUFFER REGISTER (MBR)

The Memory Buffer Register is a 2-digit storage unit which is used as follows: (1) to store data that is read from memory for availability to other registers; (2) to store data that is to be written into memory; and (3) to control the entry (writing) of data into memory by exercising control over memory plane inhibit lines.

Memory Buffer Register is divided into MBR-odd (01.40.17.1 to 01.40.09.1) and MBR-even (01.40.17.1 to 01.40.19.1), each of which is capable of storing a single digit. Each is composed of six latches (C, F, 8, 4, 2, and 1). When memory is addressed to read out, the digit at the even address is stored in MBR-even and the digit at the odd address in MBR-odd.

Early in each memory cycle MBR is normally reset to nothing (C, F, 8, 4, 2, and 1 latches OFF) so that new data may be stored later in the cycle. Near the end of each cycle the two halves of MBR are checked independently for odd parity.

Figure 5-17 indicates data paths to and from MBR.

Figure 5-18 shows an example of MBR latch control of inhibit function.

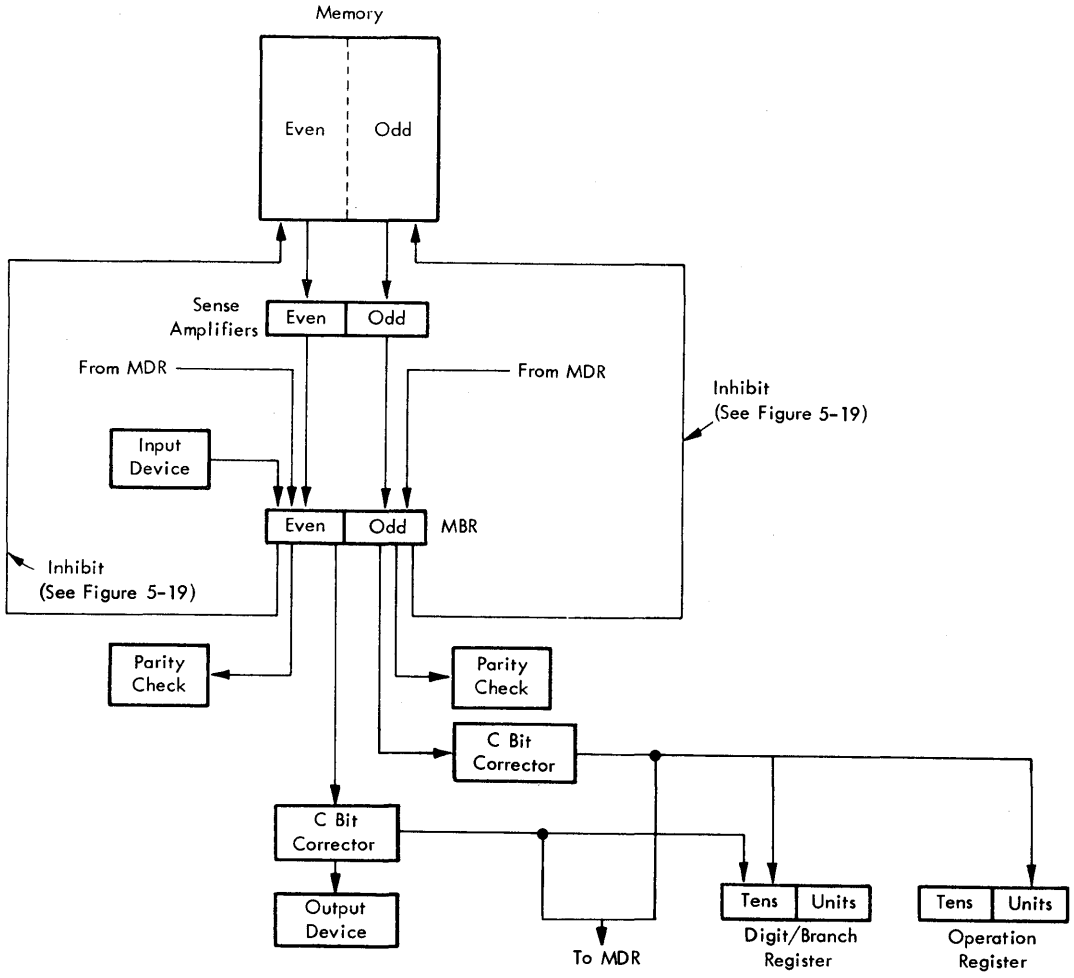



Figure 5-17. Data Paths To and From MBR

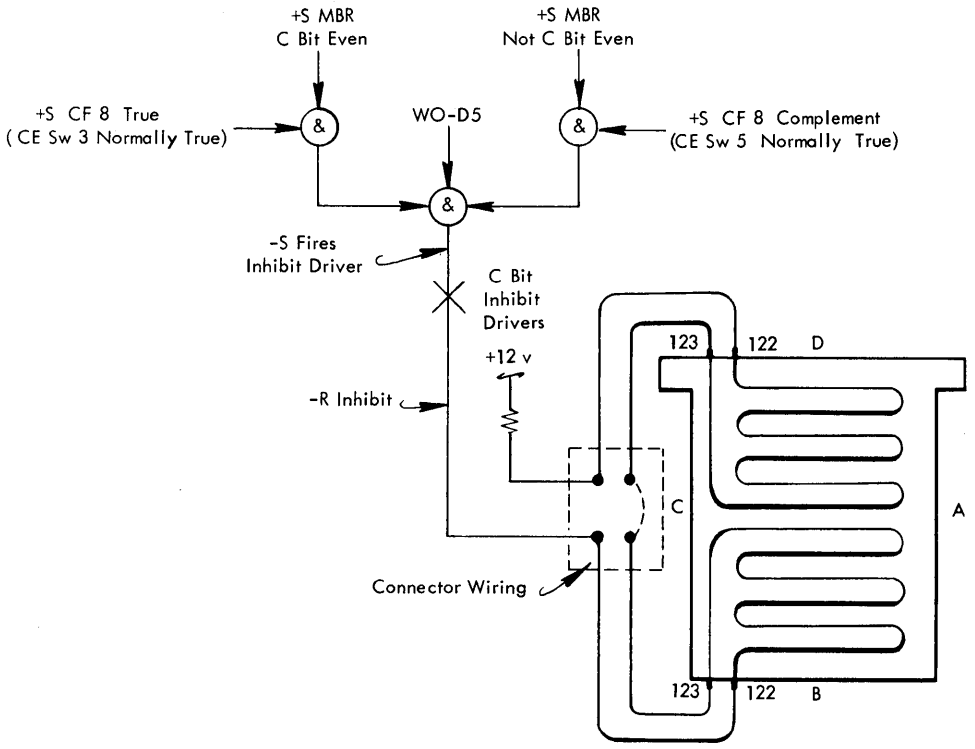



Figure 5-18. MBR Control of Inhibit (Z Driver) Function

## MEMORY DATA REGISTER (MDR)

The Memory Data Register is a single-digit storage unit which is used as follows: (1) to store the specific even or odd digit, that is designated to be read from memory by the address in MAR, for availability to other registers; and (2) to store data that is to be written into memory via MBR-even or MBR-odd.

Memory Data Register (01.45.05.1 to 01.45.07.1) consists of six latches, one for each of the C, F, 8, 4, 2, and 1 bits.

Memory Data Register is normally reset to nothing (C, F, 8, 4, 2, and 1 latches OFF) early in each memory cycle so that new data may be stored later in the cycle.

Figure 5-19 shows data paths to and from MDR.

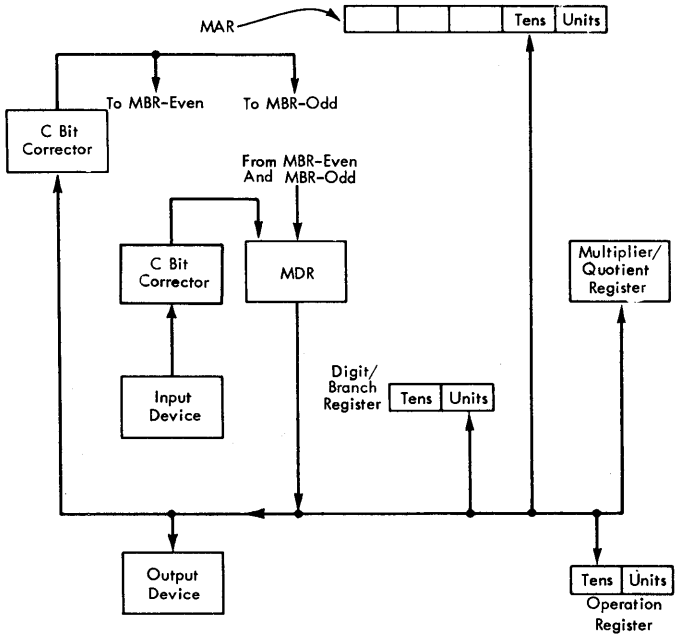



Figure 5-19. Data Paths To and From MDR

## MEMORY ADDRESS REGISTER STORAGE (MARS)

Memory Address Register Storage is a coincident-current core system consisting of a single plane in a 24 x 16 rectangular matrix (System Diagrams 01.57.05.1 to 01.57.32.1). The basic 1620 machine uses only a part (24 x 8) of the available storage.

Figure 5-20 shows the "read" winding. The "read" winding is threaded through each core twice, each traverse supplying 1/2 $I_m$. The two turns supply full $I_m$ which will flip the core to its "zero" state if a "one" was stored in it.

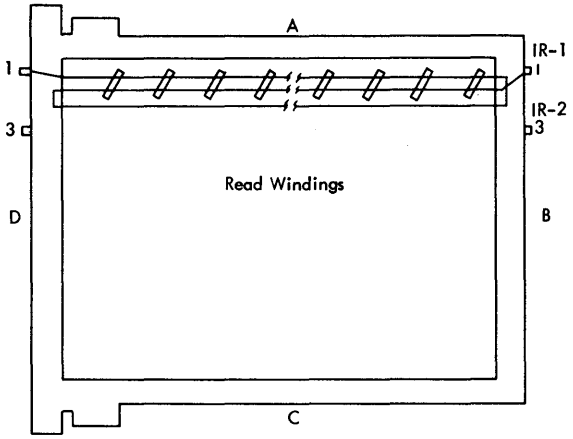



Figure 5-20. MARS Plane - Read Winding

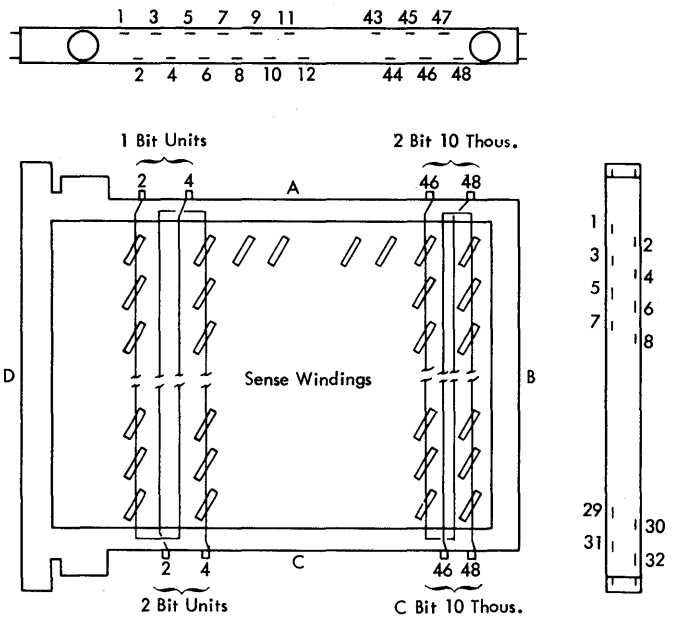



Figure 5-21. MARS Plane - Sense Winding

and the "bit" lines is required. The bit drivers for each position (units, tens, hundreds, etc.) are controlled separately to permit writing into one or two positions of a MARS register without affecting the other positions.

Figure 5-23 shows the "read," "write," "bit," and "sense" windings with associated circuitry for a single core. The 4-bit core in the hundreds position of OR-2 is shown.

Figure 5-21 shows the sense winding. The two ends of the sense winding are connected to a bipolar sense amplifier which will accept positive or negative pulses. The output of the sense amplifier sets a trigger in MAR. At "read" time any cores that flip from "one" to "zero" will induce a pulse in the sense winding. A core that is flipped from "zero" to "one" during "write" time will also induce a pulse in the sense winding. To discriminate between "read" and "write" time, the sense amplifier is gated by the MARS sense amplifier gate. To reset a MARS register, the read winding for that register can be energized at a time when the MAR sense amp gate is not available. An induced pulse in the sense winding at this time is not detected.

Figure 5-22 shows the "write" lines and "bit" lines which form the coordinates for writing into a core. To write into a specific MARS register, coincidence of the "write" lines for that register

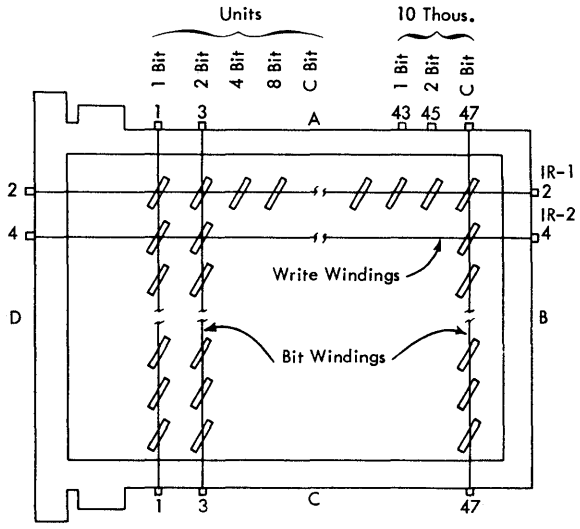



Figure 5-22. MARS Plane - Bit Winding and Write Windings

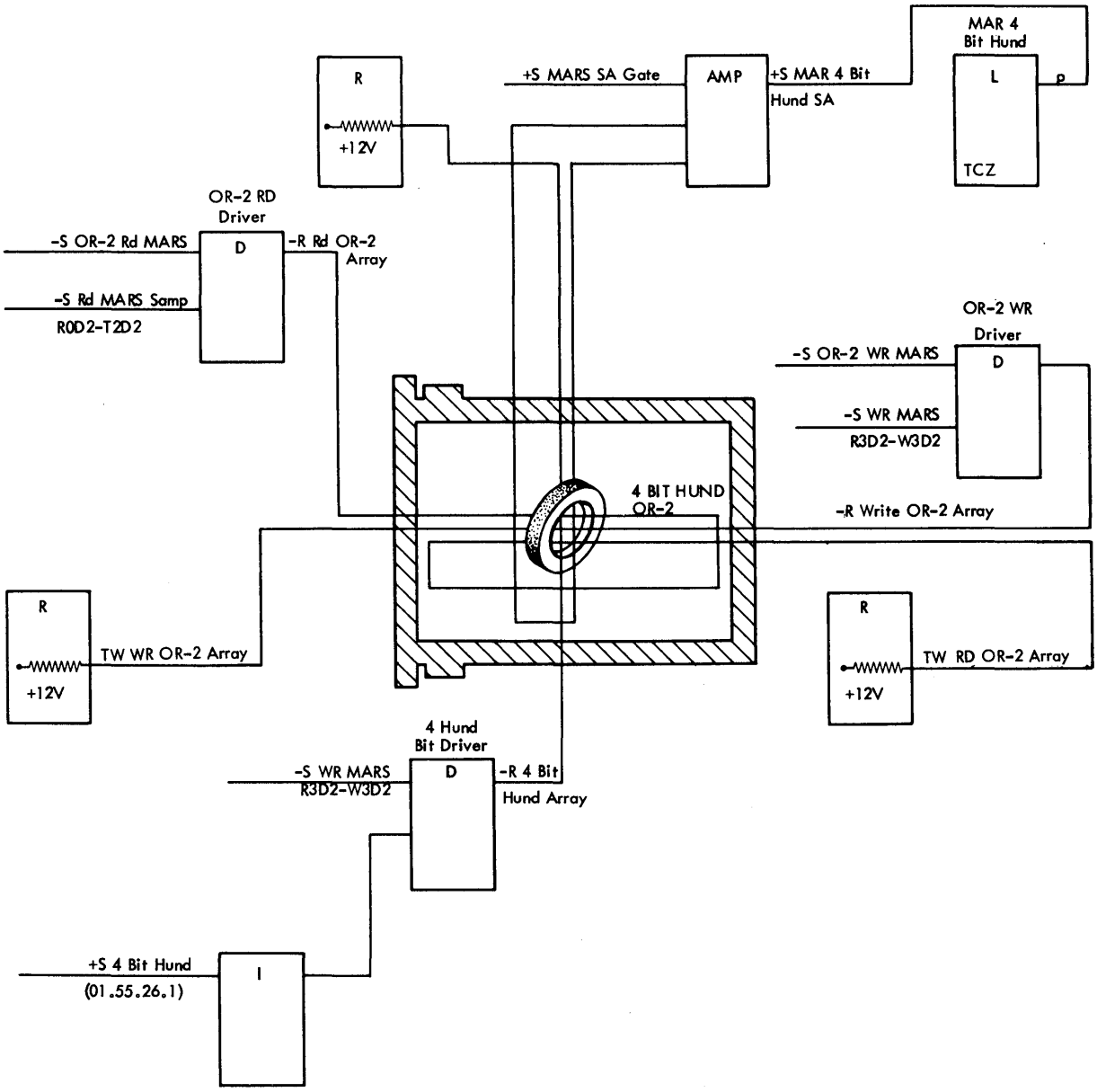



Figure 5-23. MARS Plane - Read/Write and Control Circuits

## MEMORY ADDRESS REGISTER (MAR)

The Memory Address Register (01.57.05.1 to 01.57.32.1) is a 5-digit storage unit which is used to address memory (locate X and Y-axes) for reading from memory or writing into memory. The 1-bit latch in the units position controls the Odd-Even trigger. The Odd-Even trigger has two functions: (1) to determine whether the content of MBR-odd or MBR-even is transferred to MDR to place the specific digit addressed by MAR in MDR; (2) to determine which memory sense amplifier (odd or even) is blocked for clearing a specific memory location if a "Read-Y" function is enabled.

The units, tens, hundreds and thousands positions of MAR each consist of five latches (C, 8, 4, 2, and 1). The ten-thousands position consists of four latches (C, 4, 2, and 1). The 1-bit latch in the ten-thousands position is used in addressing memory, and all four latches in the ten-thousands position are used in the detection of invalid memory addresses.

The ten-thousands position of MAR contains either a "one" or a "zero" for all valid memory addresses unless a 1623 (Special Feature) is attached. Near the end of each memory cycle, MAR is checked for invalid digits in the ten-thousands position and for odd parity in each of the five positions.

Memory Address Register is normally reset to nothing (all latches OFF) at the beginning of each memory cycle, so that a new address may be entered from MARS for addressing memory.

In operations using the Add Table, 0, 0, 3 is set in the ten-thousands, thousands, and hundreds position, respectively, to define the Add Table area in memory. In operations using the Multiply Table, 0, 0 is set in the ten-thousands and thousands positions to complete the multiply table address. At the beginning of multiply (and load dividend, a part of the Automatic Divide, Special Feature) operations, "00080" is set in MAR to define the starting address for clearing the product (or quotient) area in memory. Pressing the Insert key on the console sets "00000" in MAR to define the starting address for manual insertion of instructions.

Figure 5-24 shows data paths to and from MAR.

## INCREMENT/DECREMENT SWITCH

The status of the Decrement latch (01.60.05.1 OFF-Increment, ON-Decrement)determines whether addresses in MAR are incremented or decremented before they are written in MARS by controlling the Increment/Decrement (Incr/Decr) switch.

The Incr/Decr switch (System Diagrams 01.55.02.1 to 01.55.45.1) is a network of AND and OR switches which provide increment +1, increment +2, or decrement -1 functions. (A decrement -2 is supplied with Indirect Addressing, a Special Feature).

Increment +1 and decrement -1 are the normal functions of the Incr/Decr switch, depending on the status of the Decrement latch.

Where it is required to read out to MAR and return an address unchanged to MARS, a bypass around the Incr/Decr switch is available.

Where it is required that an address in MAR be increased by 2 before placing it in a MARS register, an increment +2 function is available.

Figure 5-25 shows the data paths to, from, and bypassing the Incr/Decr switch.

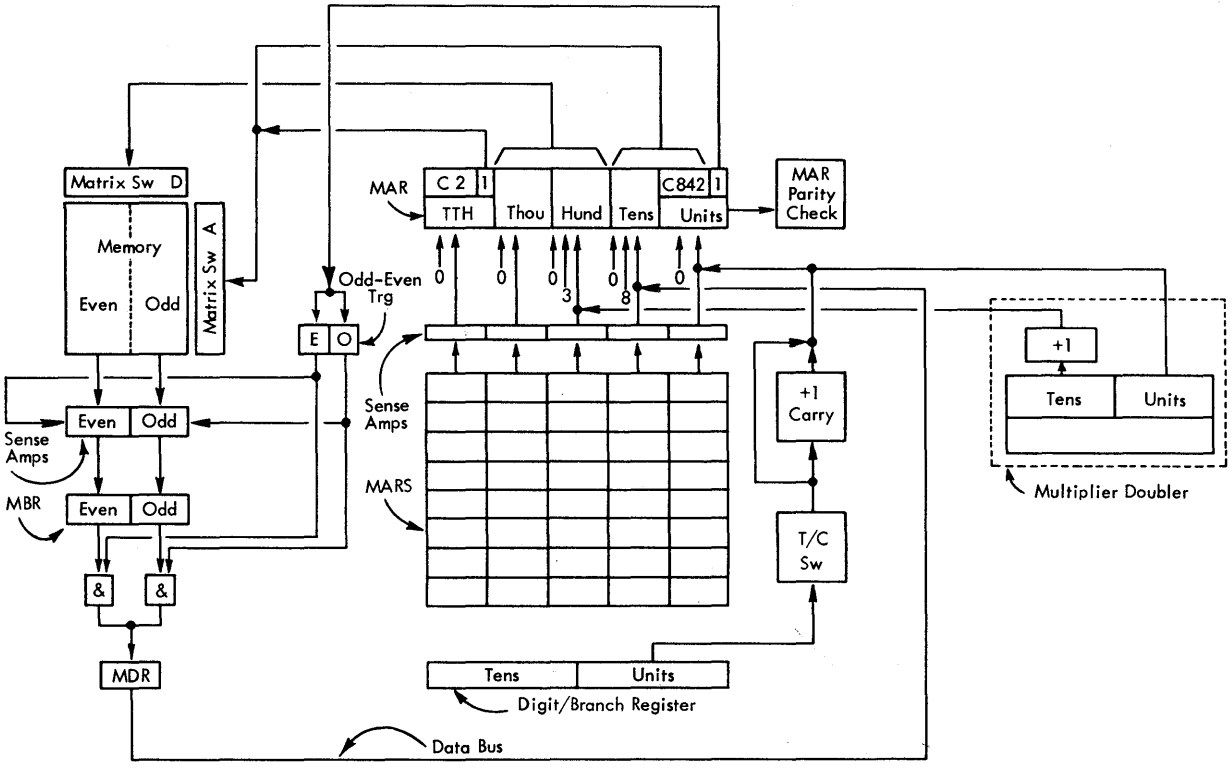



Figure 5-24. Data Paths To and From MAR

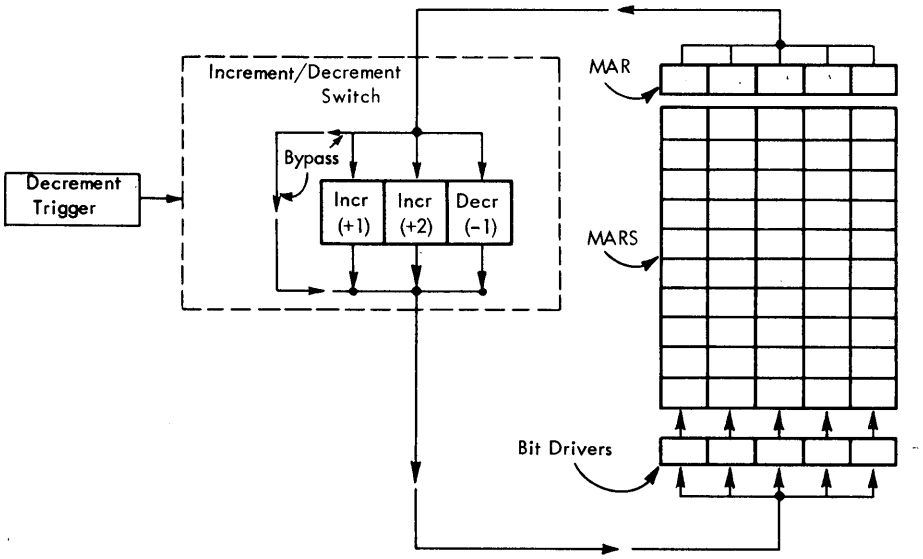



Figure 5-25. Data Paths To, From, and Bypassing the Incr/Decr Switch

The Incr/Decr switch must propagate any carries that are generated when incrementing (adding to) an address. It must also "borrow", as necessary when decrementing (subtracting from) an address. For example, if MAR contains 09999 which is to be incremented +1, the output of the Incr/Decr switch must be 10000. Figure 5-26 is a function chart showing the Incr/Decr switch circuitry that propagates the carries generated when 09999 is incremented by 1 to 10000. Figure 5-27 is a function chart of the Incr/Decr switch circuitry that accomplishes "borrowing" when 10000 is decremented by 1 to 09999.

## OPERATION REGISTER AND DECODER

The operation register (System Diagrams 01.20.07.1 to 01.20.12.1) is a 2-digit storage unit which is used to store the operation code (digits $O_0$ and $O_1$) of each instruction for the duration of the operation specified by the instruction. The contents of the Operation register are decoded to determine the operation to be performed. The output of the decode network controls circuits to accomplish the operation objectives.

The units position of the operation register consists of five latches (C, 8, 4, 2, and 1 bits) and the tens position of the operation register consists of four latches (C, 4, 2, and 1 bits). The decoder (System Diagrams 01.20.13.1 to 01.20.72.1) is composed of a network of AND and OR switches connected to the outputs of the latches comprising the operation register.

The operation register is reset to zeros (C-bit latches on; 8, 4, 2, and 1-bit latches off) prior to entry of a new operation code. The C-bit latches remain on or are turned off as required by the bit combinations of the new operation code.

Figure 5-28 shows data paths to and from the operation register and decoder.

## DIGIT/BRANCH (D/B) REGISTER AND DECODER

The Digit/Branch (D/B) register (System Diagrams 01.50.07.1 to 01.50.19.1) is a 2-digit storage unit which is used for: (1) loading of P and Q-addresses in MARS during the instruction cycle; (2) storing factors in arithmetic operations for use in the development of add table and multiply table addresses; (3) storing the $Q_8$ and $Q_9$ digits of read, write, control, branch indicator, and branch no indicator instructions.

Each position (units and tens) of the D/B register consists of five latches (C, 8, 4, 2, and 1-bits).

Each D/B register position is controlled to store data or to reset to nothing (that is, C, 8, 4, 2, and 1 latches OFF), independent of the other position.

In multiply operations, it is required that the multiply table digit in the tens position of the D/B register be transferred to the units position for processing; therefore, a data flow path is provided

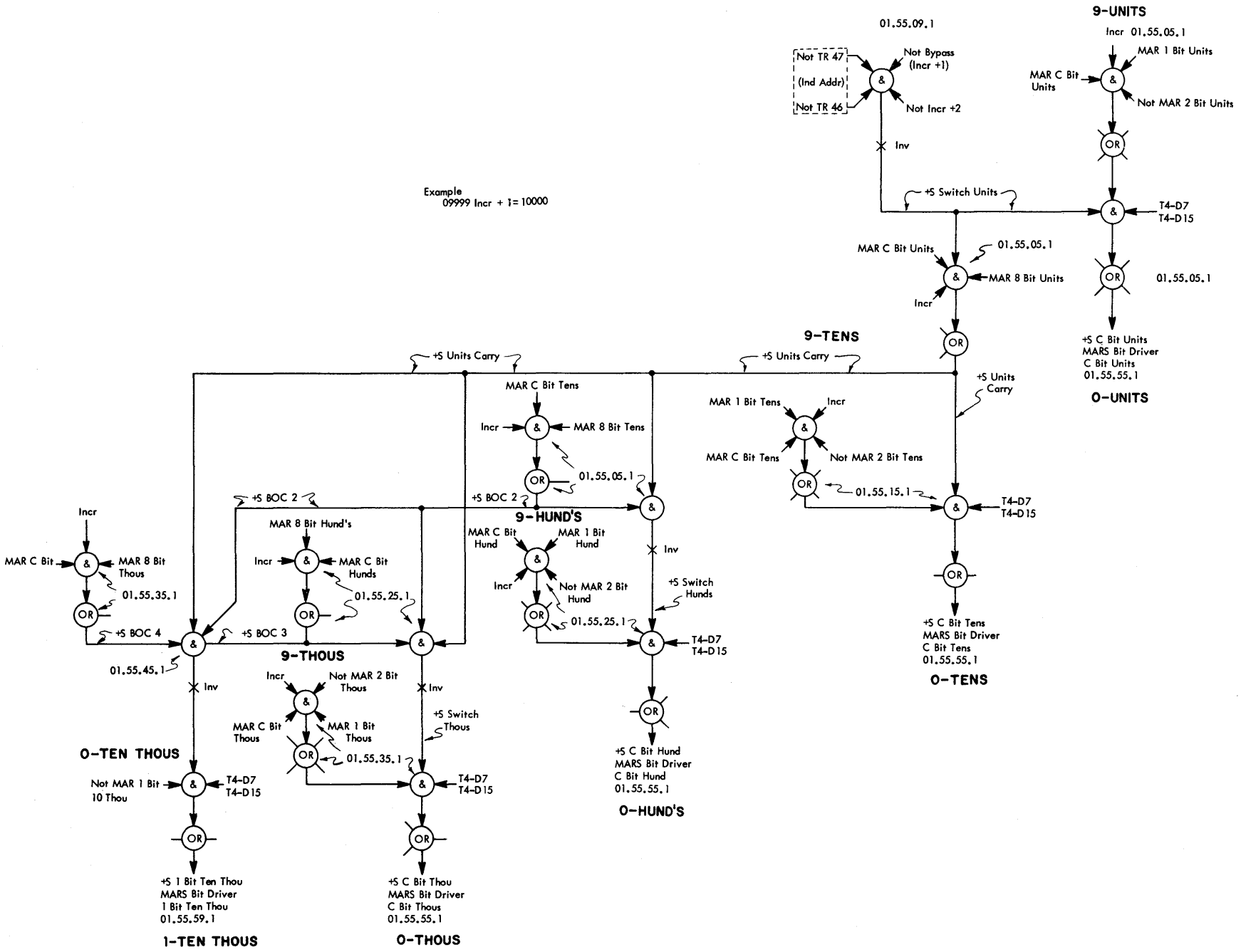



Figure 5-26. "Carries" in the Increment/Decrement Switch

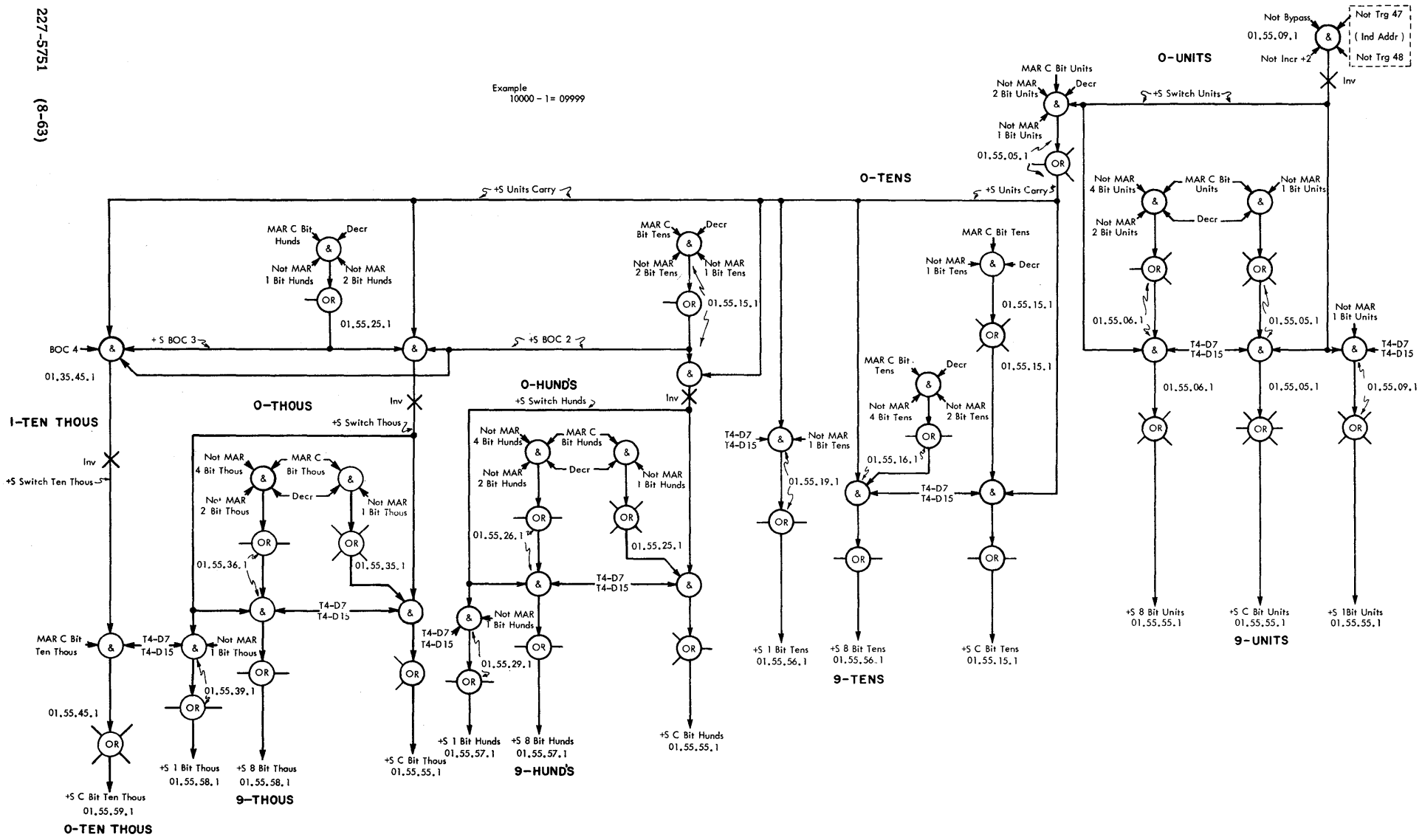



Figure 5-27. "Borrowing" in the Increment/Decrement Switch

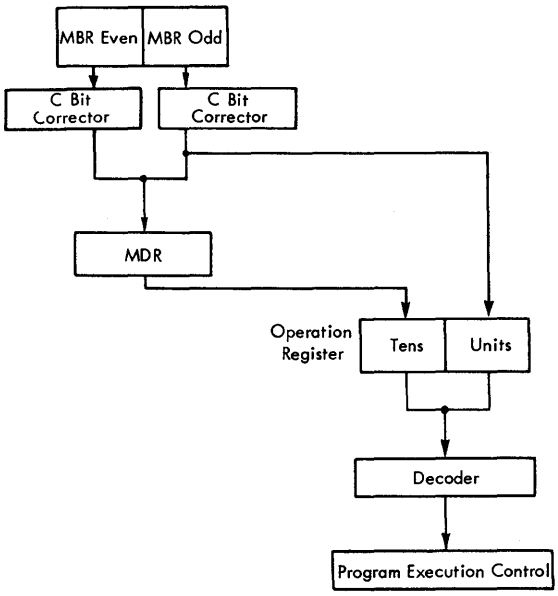



Figure 5-28. Data Paths To and From the Operation Register and Decoder

to accomplish this transfer. The contents of the D/B register are decoded to determine: (1) the input or output unit to be used in read, write, and control instructions; and (2) the program sense switch or indicator to be interrogated in branch indicator and branch no indicator instructions. The decoder is composed of a network of AND and OR switches connected to the outputs of the latches comprising the D/B register.

Figure 5-29 shows the data paths to and from the D/B register positions.

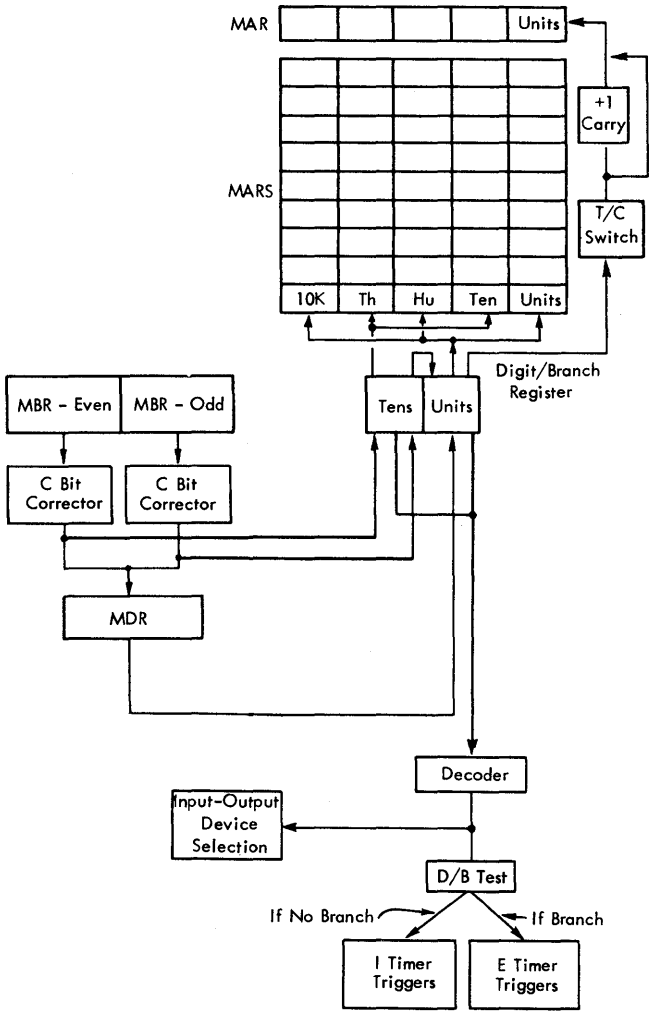



Figure 5-29. Data Paths To and From the Digit/Branch Register

## TRUE/COMPLEMENT (T/C) SWITCH

The True/Complement (T/C) switch (01.60.34.1 to 01.60.38.1) is used with arithmetic operations in the development of add table addresses to be set in MAR.

The T/C switch consists of a network of AND and OR switches connected to the outputs of the latches comprising the units position of the digit register. Control of the T/C switch is exercised by the status of the T/C trigger (01.63.20.1). With the T/C trigger ON, "true" control exists and digits presented to the T/C switch appear unchanged at the output of the switch. With the T/C trigger OFF, "complement" control exists and the 9's complement of digits presented to the T/C switch appear at the output of the switch.

Digits at the output of the T/C switch bypass the carry switch if the Carry In trigger is off. Digits (true or complement) at the output of the T/C switch are increased in value by one by the carry switch if the Carry In trigger is on, denoting: (1) a carry from addition of the two previous digits, or (2) the add table address for the units position of a sum or difference is being developed on a complement operation. (If the output from the T/C switch is a "9" and the Carry In trigger is on resulting in a zero (9 + carry) output from the carry switch, the Carry Out trigger will be turned on to provide for increasing the value of the next digit to the left by one.)

Figure 5-30 shows the data paths to and from the T/C switch and carry switch.

## MULTIPLIER/QUOTIENT (M/Q) REGISTER

The Multiplier/Quotient (M/Q) register (01.62.50.1 to 01.62.52.1) is a single-digit storage unit which is used in multiply operations to store each digit of

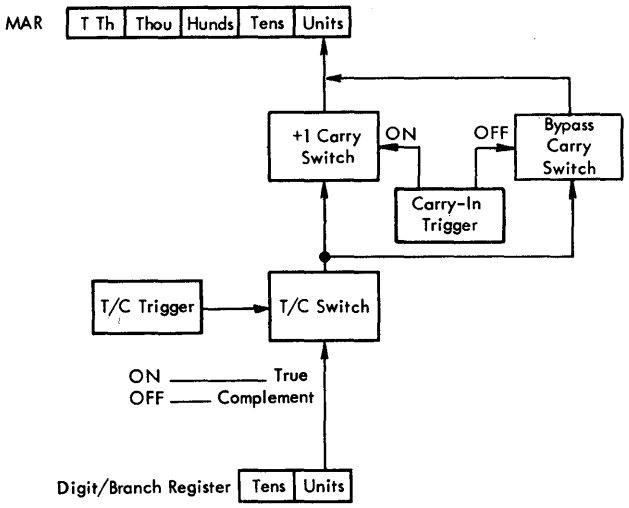



Figure 5-30. Data Paths To and From the True/Complement Switch and Carry Switch

the multiplier until it has been used with each digit of the multiplicand. (It is also used to store the quotient digit developed during an Automatic Divide-operation a Special Feature). The M/Q register consists of five AND latches, one for each bit (C, 8, 4, 2, and 1).

The M/Q register is reset to zero (C-bit latch on; 8, 4, 2, and 1-bit latches off) early in the memory cycle in which a new multiplier digit is to be stored. The C-bit latch remains ON or is turned off as required by the bit combinations of the new multiplier digit.

Figure 5-31 shows data paths to and from the M/Q register.

## MULTIPLIER-DOUBLER

The multiplier-doubler (01.62.55.1 to 01.62.60.1) is used on multiply operations in the development of multiply table addresses to be set in MAR. The doubler consists of an AND network gated by Trigger 35 and connected to the outputs of the triggers comprising the M/Q register. Its function is to double the value of the multiplier digit and increase the value of the resulting tens position digit by one.

Figure 5-32 shows data paths to and from the doubler and gives examples for specific multiplier digits.

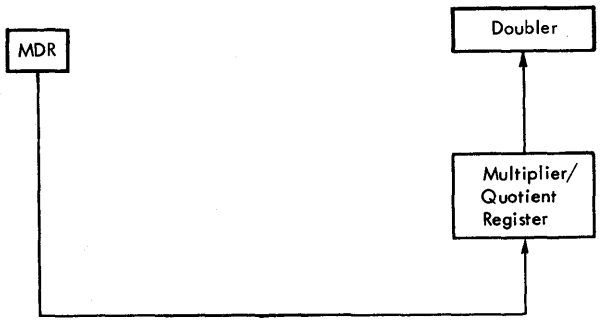



Figure 5-31. Data Paths To and From the Multiplier/Quotient Register

## C-BIT CORRECTORS

C-bit correctors (01.40.50.1 and 01.45.50.1) perform the function of maintaining correct parity where it is desired to clear an F-bit from a digit or set an F-bit with a digit. Any digit in MDR will be correct, exclusive of the F-bit. Although an even number of bits may exist in the MDR latches, the console lights will always display an odd number of bits.

F-bits are not used in the Operation register, the D/B register, the Memory Address Register, or the M/Q register. Data is routed from memory to these registers through MBR-even, MBR-odd, or MDR.

### MBR to MDR

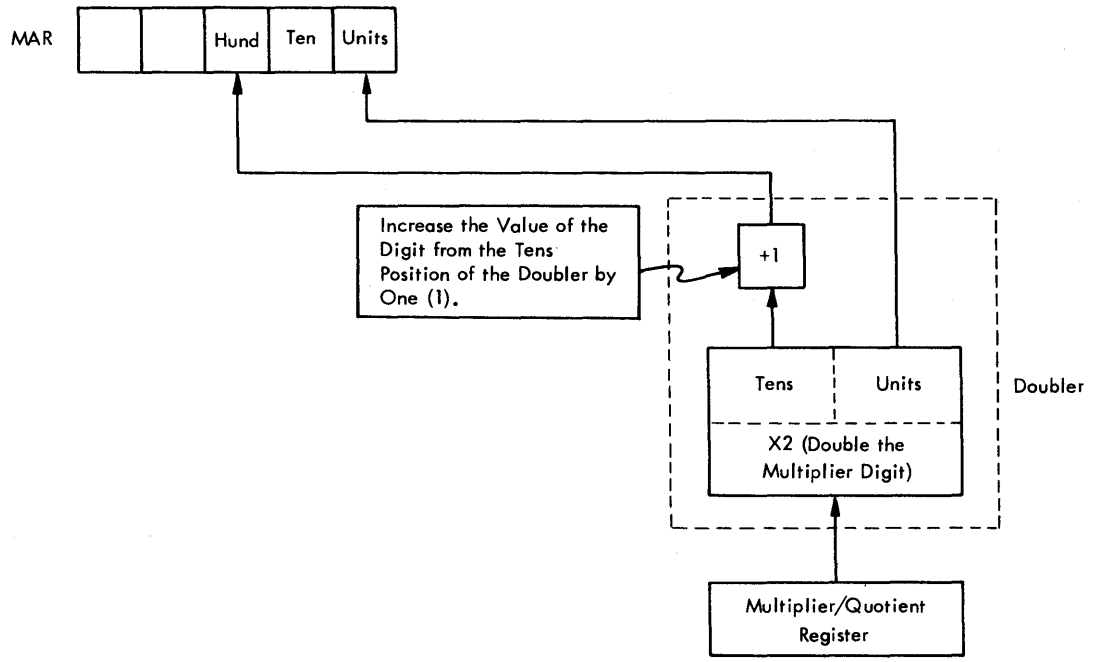
A digit will have odd parity in MBR but a C-bit corrector may change the C-bit to maintain odd parity "exclusive" of the F-bit in MDR (Figure 5-33). The F-bit and C-bit corrector network between MBR-even or MBR-odd and MDR functions as follows:

1. An F-bit in MBR will turn on the MDR F-bit latch.
2. An 8, 4, 2, or 1-bit in MBR will turn on the respective MDR latch.
3. The MBR F-bit and C-bit latches are analyzed by the "exclusive OR" network.
   a. If they are both on or both off, no C-bit will be set into MDR.
   b. If either one is on and the other off, a C-bit will be set into MDR.

Because digits in MDR have correct parity exclusive of the F-bit, these digits may be transmitted from MDR to the Operation register, D/B register, MAR, and the M/Q register without additional C-bit correction.

### MDR to MBR

Because the F-bit does not enter into the parity of MDR, the C-bit must be corrected in the process of transferring data from MDR to MBR. Data flow from MDR to MBR is shown in Figure 5-34. Note




| Multiplier Digit | Doubler | | | MAR | | | | |
|---|---|---|---|---|---|---|---|---|
| | Tens | Tens +1 | Units | T Th | Thous | Hunds | Tens | Units |
| 1 | 0 | 1 | 2 | | | 1 | | 2 |
| 4 | 0 | 1 | 8 | | | 1 | | 8 |
| 5 | 1 | 2 | 0 | | | 2 | | 0 |
| 8 | 1 | 2 | 6 | | | 2 | | 6 |

Figure 5-32. Multiplier Doubler

that the MDR C-bit console lamp operates from the output of the C-bit corrector, thus indicating odd parity in MDR although an even number of latches may be on. The C-bit is corrected through an exclusive OR circuit as follows:

1. If the MDR F-bit and C-bit latches are both on or both off, no C-bit will be set into MBR.
2. If either one (F-bit or C-bit latch) is on and the other is off, a C-bit will be set into MBR.

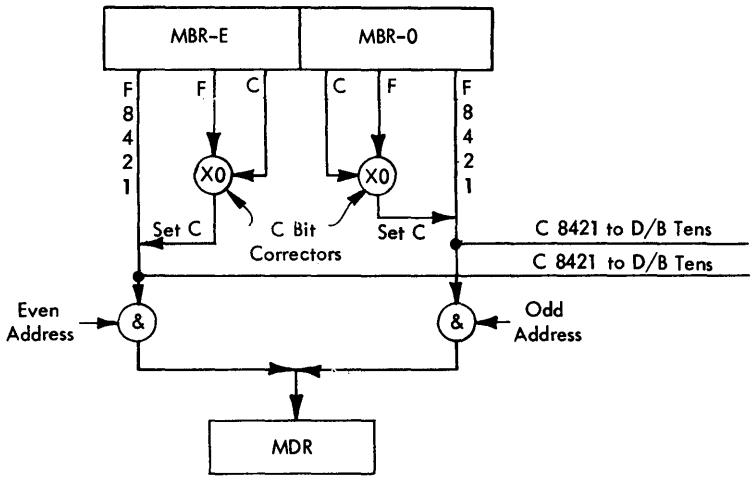



Figure 5-33. C Bit Corrector - From MBR-Odd and MBR-Even

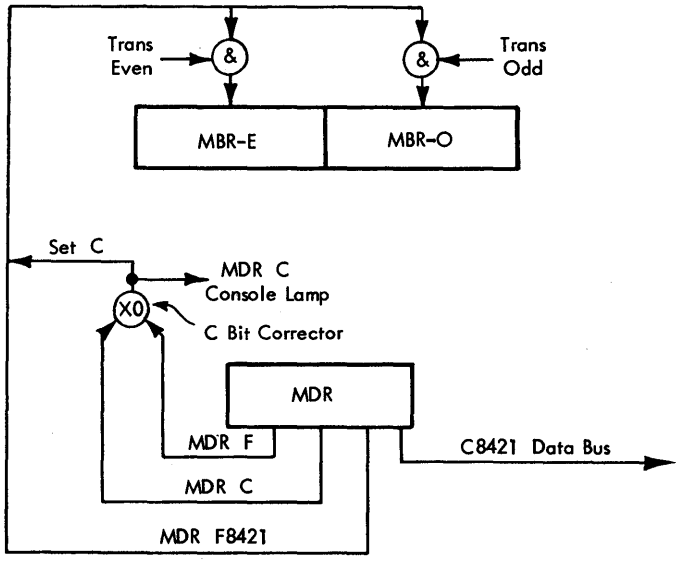



Figure 5-34. C Bit Corrector - From MDR

## CONSOLE

The console is an integral part of the 1620 Computer Unit and consists of the typewriter and the console panel with its indicator lights, switches, control keys, and signal lights.

The typewriter is both an input and an output device. As an input device, the typewriter keyboard is used to enter instructions and data into memory. As an output device, the typewriter is used to print information from memory. Typewriter functions are described in Section 11, Input-Output Operations.

The console panel is shown in Figure 6-1 and the functions of its lights, switches and keys are described in this Section. The greyed areas in Figure 6-1 are associated with special features which are not described in this manual. Special features are described in separate Customer Engineering Manuals of Instruction. See Appendix H, Bibliography.

### Register Displays

The contents of the registers within the computer are displayed on the console panel by means of small incandescent lights. Each bit in each register position is represented by a light, and the light is ON when the bit which it represents is present in the digit displayed. The following registers are displayed:

Memory Address Register (MAR). Five rows of five indicator lights each display the bit configuration of the 5-digit address that is placed in MAR.

Memory Buffer Register (MBR). Two rows of six indicator lights display the bit configuration of the addressed digit and its associated digit. The digit in the even-numbered memory location is displayed in the row of lights labeled "E" (MBR-even); the digit in the next higher numbered memory location is displayed in the row of lights labeled "O" (MBR-odd).

Memory Data Register (MDR). One row of six indicator lights displays the bit configuration of the specific digit that is addressed. The digit displayed in the MDR lights is duplicated in the MBR-even or MBR-odd lights, depending on whether the address in MAR is even or odd.

Digit/Branch Register. Two rows of five indicator lights display the bit configuration of digits placed in the units and tens position of the D/B register.

Operation Register. Two rows of five indicator lights display the bit configuration of the 2-digit operation code placed in the Operation register during an instruction cycle.

Multiplier/Quotient Register. One row of five indicator lights displays the bit configuration of each successive Multiplier or Quotient digit while it is present in the register.

### Machine Check Trigger Lights

The ON and OFF status of Check triggers within the computer is represented by small incandescent lights on the console panel. The indicator light associated with a Check trigger is ON when the Check trigger is ON and OFF when the trigger is OFF.

When a Check trigger is turned on, the computer continues to operate or stops, depending on the setting of the console check switch associated with the Check trigger. If the check switch is set to Stop, the computer stops after detection of the error condition. If the check switch is set to Program, the computer continues to operate and the status of the Check trigger can be interrogated by branch indicator or branch no indicator instructions. If a Check trigger that is ON is interrogated, the trigger is turned off as a result of the interrogation. Pressing the Console Reset key turns off all Check triggers.

The functions of the various Check triggers are described as follows:

#### Overflow Check

The Overflow Check trigger and console indicator light are turned on when an overflow condition occurs in an add, subtract, or compare (or divide)

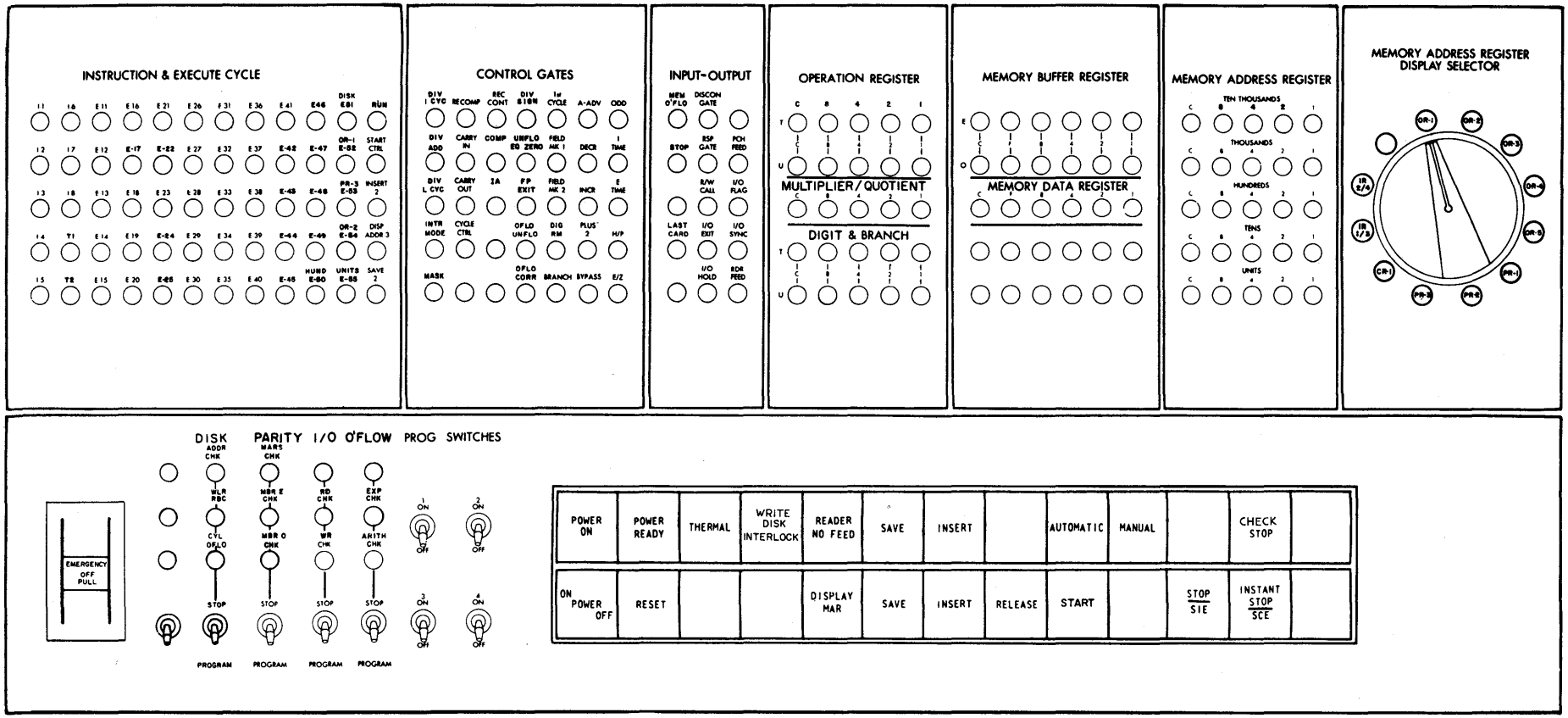



Figure 6-1. Console Panel

operation. The overflow check switch on the console is associated with the Overflow Check trigger.

Memory Address Register Check

The MAR Check trigger and console indicator light are turned on when a digit with incorrect parity or an invalid address is present in MAR. A MAR check will stop the computer at the end of the memory cycle in which the error occurs unless CE Switch 9, MAR stop bypass, is operated. The console switch has no Stop or Program function with a MAR check.

NOTE: Each of the four lights in the following group is associated with triggers which check parity at points in the system data flow. MBR-even and MBR-odd checks are associated with a console check switch. Read and write checks are associated with a console check switch.

Memory Buffer Register—Even Check

The MBR-even Check trigger and console indicator light are turned on when the digit in MBR-even has incorrect parity.

Memory Buffer Register—Odd Check

The MBR-odd Check trigger and console indicator light are turned on when the digit in MBR-odd has incorrect parity.

Read (RD) Check

The RD Check trigger and console indicator light are turned on when a character with incorrect parity is presented to the input translator.

Write (WR) Check

The WR Check trigger and console indicator light are turned on if a character with incorrect parity is presented to an output device, an even number of typewriter bit relays are energized, (an even number of holes are punched by the paper tape punch) or the output device fails to return a response signal to the computer.

Machine Timer Trigger, Auxiliary Trigger, and Control Gate Lights

The ON and OFF status of Instruction Cycle Timer triggers (I-timers), Execution Cycle Timer triggers (E-timers), certain auxiliary triggers, and certain control gates within the computer is represented by small incandescent lights on the console panel. The indicator light is ON when the trigger or control gate is on, and OFF when the trigger or control gate is off.

These lights are grouped in the three upper-left sections of the console panel and are titled "Instruction and Execute Cycle," "Control Gates," and "Input-Output." They are individually labeled for identification and are primarily intended for use by the Customer Engineer in machine trouble analysis. However, some of the indicator lights such as the High/Plus (H/P) and the Equal/Zero (E/Z) in the Control Gates section, may have significance to the machine operator as well as to the Customer Engineer.

Switches

MAR Display Selector Switch (01.05.05.1)

This 12-position rotary switch (8 basic and 5 special feature positions) is used to select one of the 13 MARS registers for display in the MAR indicator lights. When selection of the particular MARS register has been made by means of the switch, pressing Display MAR causes the contents of the selected register to be displayed in the MAR display lights. This switch is also used in conjunction with CE Switch 7 (increment). Also see IR Select switch.

Check Switches

The parity check, overflow check, and I/O check switches are associated with Check triggers within the computer and provide a means of directing the computer to stop or continue with the program when a Check trigger is turned on. If the Check trigger is turned on with the associated check switch set to Stop, the computer stops after detection of the error condition. If the check switch is set to Program, the computer continues to operate, and the status of the Check trigger can be interrogated by branch indicator or branch no indicator instructions.

Parity Check Switch (01.05.02.1). This switch determines the function of the MBR-odd and/or

MBR-even Parity Check triggers. When the parity check switch is set to Stop and either the MBR-even or MBR-odd Check trigger is turned on, the computer stops at the end of the memory cycle in which the parity error is detected, unless the execution cycle of an input-output operation is in progress. If one or both of the triggers is turned on during an input-output operation, the computer stops only upon completion of the read or write operation.

I/O Check Switch (01.05.02.1). When the I/O check switch is set to Stop and either the Read (RD) or Write (WR) Check trigger is turned on, the computer stops only upon completion of the read or write operation. (If a parity error is detected when punching paper tape, the computer remains in the automatic mode but suspends operation with the incorrect character still under the tape punches, without regard to the setting of the I/O check switch.)

Overflow Check Switch (01.05.02.1). When the overflow check switch is set to Stop and the Overflow Check trigger is turned on, the computer stops upon completion of the operation during which the overflow condition is detected.

Program Switches (01.05.02.1)

The four program (console sense) switches, numbered 1 through 4, are toggle switches with ON and OFF settings for use with branch indicator and branch no indicator instructions. When a switch is set to ON and interrogated by a branch indicator instruction, the branch occurs. If the switch is set to OFF, the branch does not occur and the next instruction in sequence is executed.

If a branch no indicator instruction is used to interrogate one of the switches, the branch occurs when the switch is set to OFF.

Console Power Switch (01.05.03.1)

The power switch on the console is a double-pole, single-throw toggle switch. When turned on, AC voltages are applied to the power supplies and DC voltages are properly sequenced.

When the power switch is set to OFF, AC voltages are removed from the power supplies and DC voltages are sequenced OFF.

Console Immediate Off Switch (01.05.03.1)

When the immediate off switch on the console is operated, all power is immediately removed from the machine. IT IS TO BE OPERATED ONLY IN CASE OF AN EMERGENCY. If operated, the switch must be reset by the Customer Engineer after pivoting the console panel forward to permit access to the back of the switch.

IR Select Switch

This switch, when in the Normal position, selects IR-1 and IR-2 (in conjunction with the MAR display selector switch) for display in the MAR display lights. When in the Int (Interrupt — a 1710 Special Feature) position, IR-3 or IR-4 are selected for display.

Control Keys

Reset (01.05.03.1)

Pressing the Reset key restores all triggers, indicator lights, and signal lights to their initial or reset condition. The Reset key is operative only when the computer is in the manual mode. For a description of the manual mode see Signal Lights, Manual Light.

NOTE: Simultaneous depression of the Reset key and the Release key causes a reset operation regardless of whether the computer is in the manual mode or the automatic mode.

Display MAR (01.05.01.1)

The objective of the display MARS operation is to read into MAR the address contained in a selected MARS register for display in the MAR indicator lights. The operation can be performed only when the computer is in the manual mode. Depression of the Stop/SIE key places the computer in the manual mode.

To display a MARS register, the MAR display selector switch is set to the desired register and the display MAR key is depressed. See IR Select Switch.

The address in a second MARS register may be displayed by turning the switch to select the desired register and by again depressing the display MAR key.

Each address that is displayed during a display MARS operation is written back unchanged into the MARS register from which it came.

NOTE: When the Instant Stop/SCE key is used to stop the machine, both the manual mode and the

automatic mode lights will be on, except when the stop occurs on the last E-timer trigger of the cycle. prior to entering I-cycles (I-cycle entry status). With the computer stopped in the I-cycle entry status, only the manual light will be on. When both lights are on, the Reset key must be pressed before pressing the Display MAR key. Pressing the Reset key causes any timer trigger left on from the previous execution cycle to be turned off. The automatic mode light is turned off because the Start 1 trigger is reset OFF.

Figure 6-2 shows a function chart for the display MARS operation.

Save (01.05.01.1)

The machine operator can interrupt the execution of a program to enter instructions for another routine and execute that routine. When the objectives of the interruption have been accomplished, execution of the program can be resumed.

The objective of the save operation is to retain the address of the next instruction to be executed when the program is interrupted.

The save operation can be performed only when the computer is in the manual mode. Execution of the program is interrupted and the computer is placed in the manual mode by pressing the Stop/SIE key.

Pressing the Save key then stores the address of the next instruction to be executed in the PR-1 MARS register and turns on the save signal light.

The last instruction entered into the computer for the routine must be a branch back instruction. Execution of that instruction turns off the save light and directs the computer to resume execution of the program, beginning with the instruction at the saved address.

Instructions entered and executed for the routine should not demand multiply or multiply immediate (also divide, divide immediate, load dividend, load dividend immediate, or floating divide (special features) operations. The execution of such an instruction would destroy the saved address in PR-1.

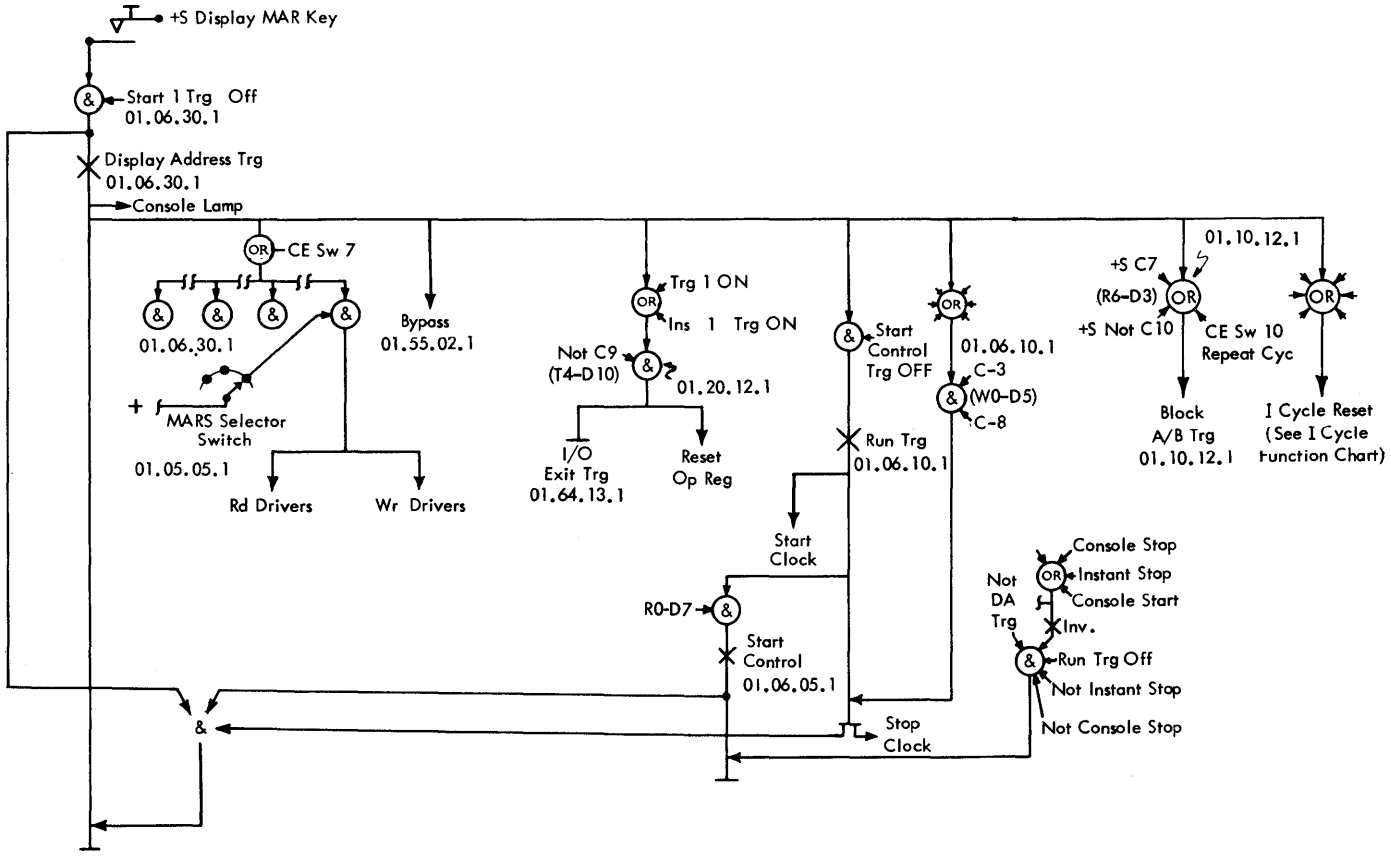



Figure 6-2. Display MAR

The Reset key should not be pressed between the time that the Save key is pressed and the first branch back instruction is executed because pressing the Reset key turns off the Save Control trigger. The saved address in PR-1 would not then be used in resumption of the program. (See Branch Back — Code 42, Section 10.)

Figure 6-3 shows a function chart for the save operation.

Insert (01.05.01.1)

The objective of the insert operation is to activate the typewriter keyboard for direct entry of instructions into memory. Instruction digits are stored at memory location 00000 and succesively higher locations. The operation can be performed only when the computer is in the manual mode.

Pressing the Insert key sets zeros into the IR-1 and OR-2 MARS registers and activates the typewriter keyboard. The OR-2 register is incremented +1 for each entry of an instruction digit into memory to provide the address for storing the following digit. The IR-1 register retains the 00000 address throughout the insert operation.

The last instruction in the sequence should be either a branch back or branch (unconditional) instruction, depending upon whether or not the Save key was used prior to entering the insert operation.

The typewriter keyboard remains activated until the Release key is depressed or the 100th digit is entered into memory. If the Release key is not used to terminate the insert operation before the 100th digit is entered, the simulated read numerically operation is terminated, the I/O Exit and Stop 1 triggers are turned on, and the computer stops in the manual mode. Operation of the Start key is required to restart the computer which will then execute the instruction starting in location 00000 (IR-1).

Figure 6-4 shows a function chart for the insert operations.

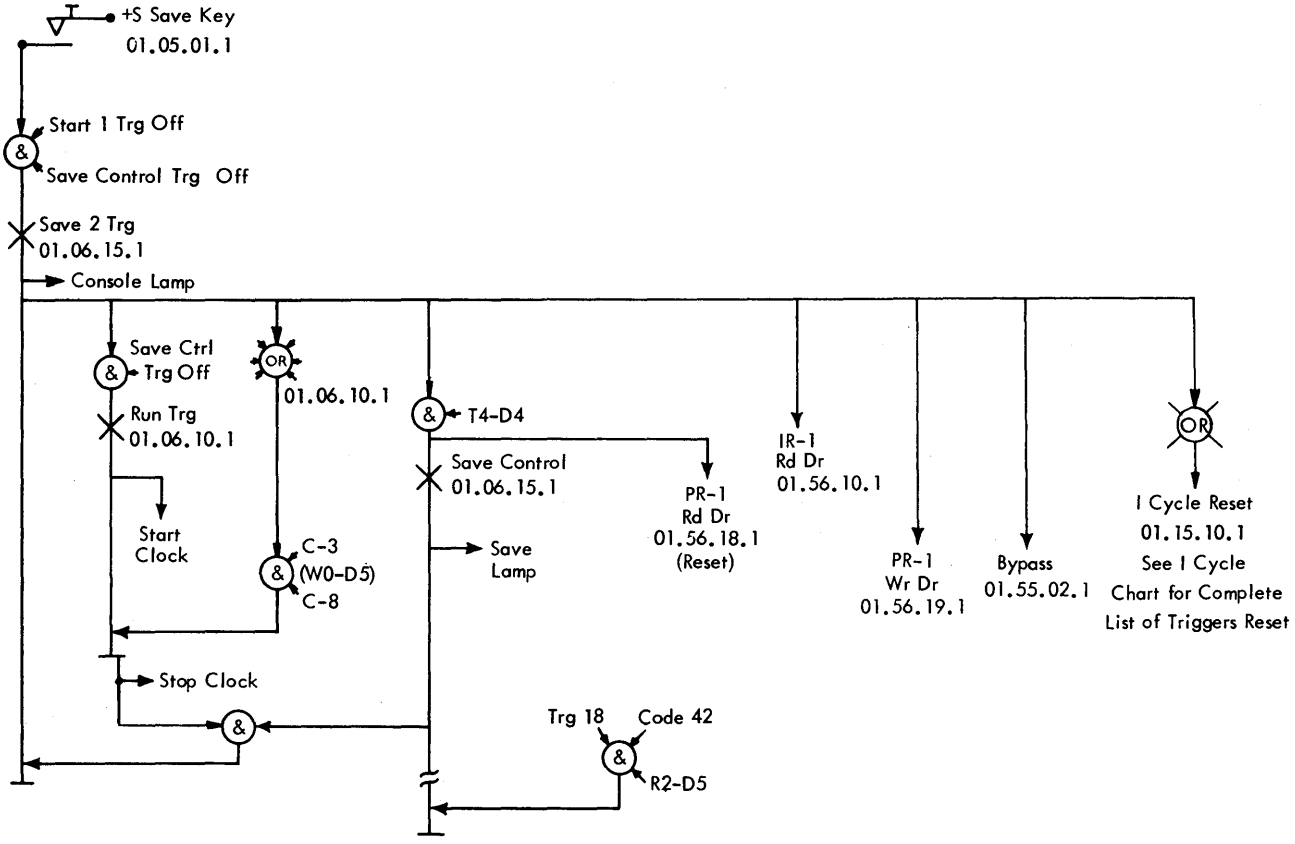



Figure 6-3. Save

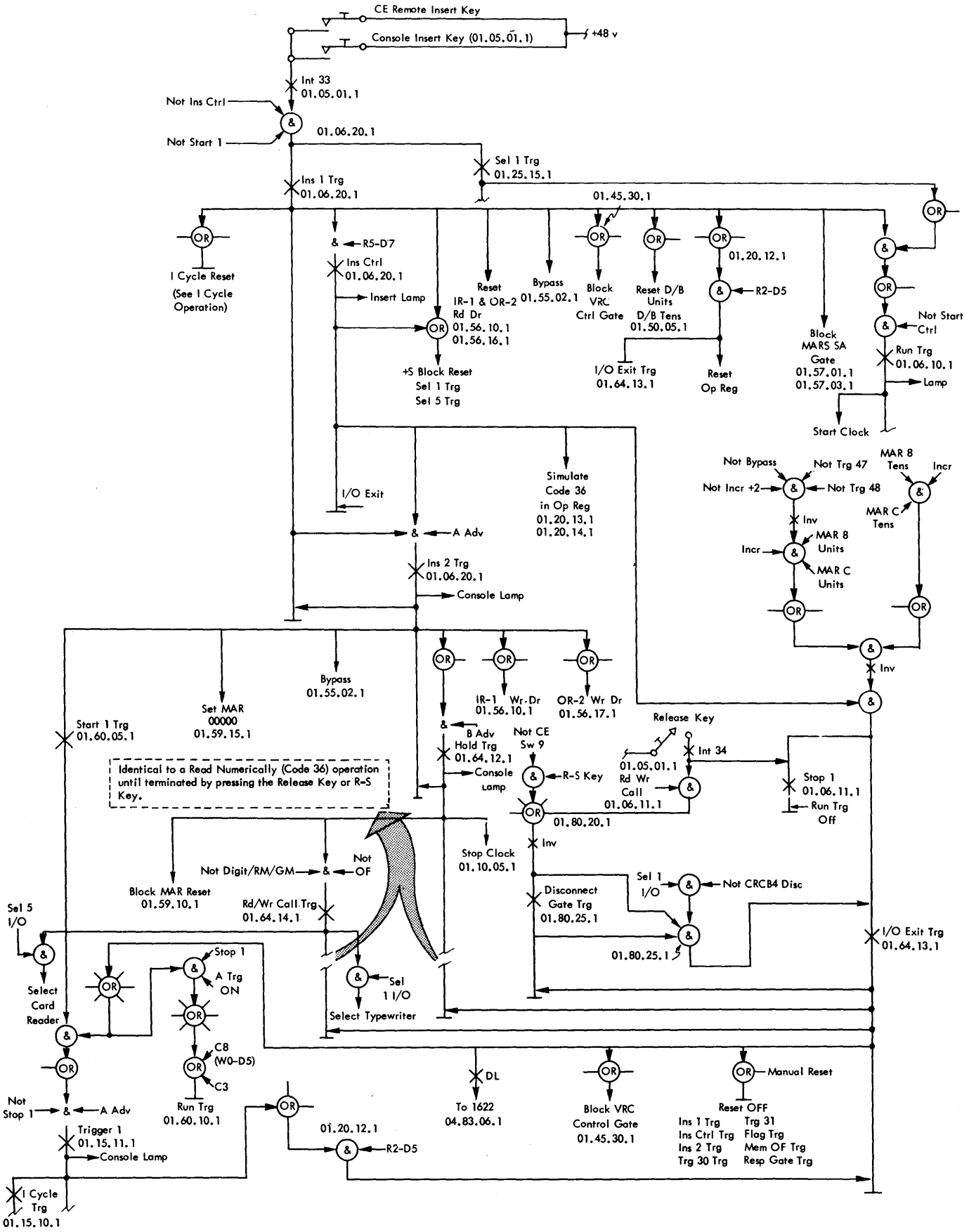



Figure 6-4. Insert

Release (01.05.01.1)

The primary function of the Release key is to terminate an input operation where the input device is the typewriter keyboard. If the input operation was initiated by the insert key, the insert light is turned off by pressing the Release key.

The Release key can be used to immediately stop the computer during any input-output operation. The Release key is used in conjuction with the Reset key to cause a machine reset. See the Note under Reset key.

Figure 6-5 shows a function chart for the release operation.

Start (01.05.01.1)

Pressing the Start key causes the computer to begin execution of a program. The address of the first instruction to be executed is contained in the IR-1 MARS register.

The Start key is operative only when the computer is in the manual mode. Pressing the Start key places the computer in the automatic mode; turns on the automatic light; and turns off the manual light.

Figure 6-6 shows a combined function chart for Start key, Stop/Single Instruction Execute key, and Instant Stop/Single Cycle Execute key operations.

Stop/Single Instruction Execute (SIE) (01.05.01.1)

Pressing the Stop/SIE key with the computer in the automatic mode, terminates the automatic mode and places the computer in the manual mode. The automatic light is turned off and the manual light is turned on.

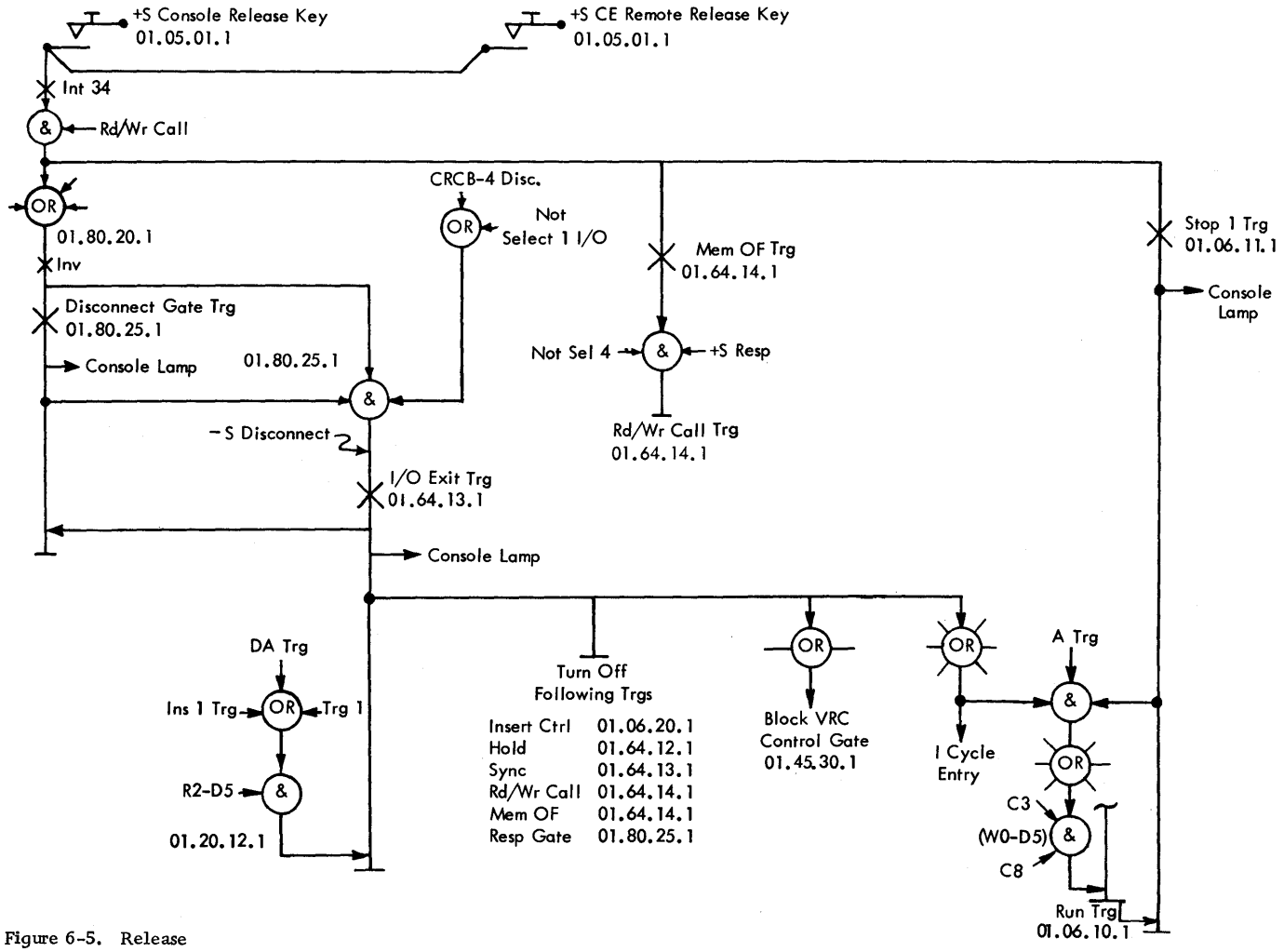



Figure 6-5. Release

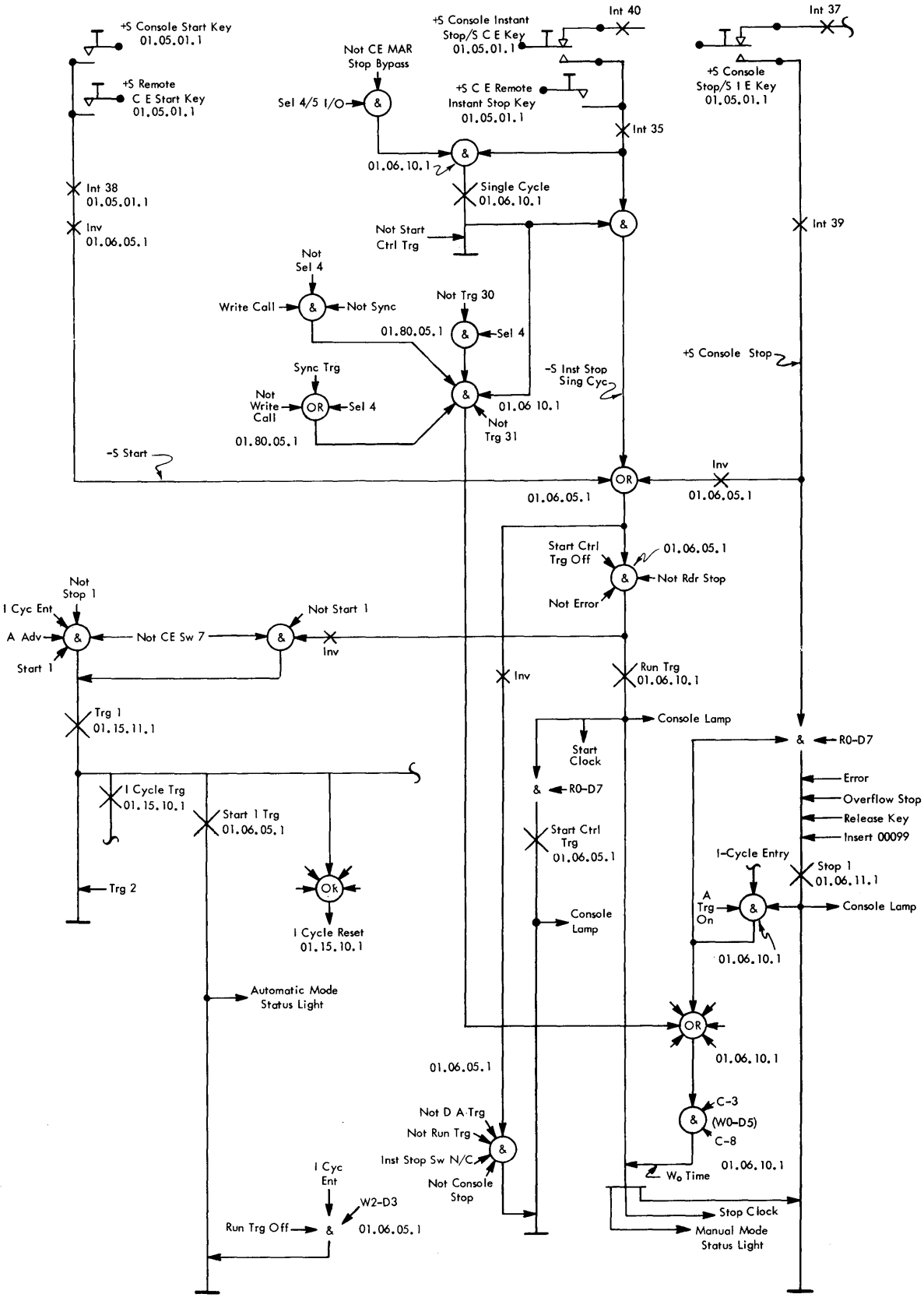



Figure 6-6. Start - Stop

Successive depressions of the Stop/SIE key with the computer in the manual mode cause one instruction to be executed for each depression.

Figure 6-6 shows a combined function chart including the Stop/SIE key.

### Instant Stop/Single Cycle Execute (SCE) (01.05.01.1)

Pressing the Instant Stop/SCE key with the computer in the automatic mode, stops the computer. The cycle in which the computer stops depends upon the operation being performed. The function of the Instant Stop/SCE key differs between I/O operation codes and other operation codes.

For I/O operation codes:

1. Pressing this key during a read operation stops the computer at the end of Trigger 30 time. Successive depressions cause a complete character input cycle, which is completed when the end of Trigger 30 time is again reached.
2. Pressing this key during a write operation stops the computer with the Sync trigger on. Successive depressions cause a complete character output cycle which is completed when the Sync trigger is turned on again.

For other operation codes:

1. Pressing this key stops the computer at the end of the memory cycle in which the key is pressed. Successive depressions cause the computer to execute a single 20-$\mu$sec memory cycle for each depression.

The manual light and the automatic light are both ON, except when the computer is stopped in an I-cycle entry status. In an I-cycle entry status only the manual light is ON.

Figure 6-6 shows a combined function chart including the Instant Stop/SCE key.

### R-S Key

The R-S key (Release-Start) is installed on the typewriter, but is described here because it performs the functions of two console keys. Pressing this key during an Insert, Code 36, or Code 37, operation performs the same function as is performed by pressing the Release key and then the Start key.

### Signal Lights (01.05.10.1)

Signal lights on the console panel provide the machine operator with a visual indication of computer operating and error conditions.

#### Power On Light

The power-on light is turned on when power is applied to the machine through the power-on switch. It is turned off only when power is turned off.

#### Power Ready Light

The power-ready light is turned on when all power supplies have been properly sequenced. It is turned off in the event of any power-supply failure, any over-temperature condition within the machine, or when the power switch is turned off.

#### Manual Light

The manual light is ON when the computer has terminated all operation and is prepared to accept operator intervention. It is turned on as a result of executing a halt instruction; depressing the Release key, Stop key, or Instant Stop key; or detecting an error condition (if the associated check switch is set to Stop).

The computer is normally in the manual mode when the manual light is on. However, during single-cycle execution of an instruction, both the manual and the automatic lights are on, and the computer is in the automatic mode. Both lights are also on, and the computer is in the automatic mode, if the Instant Stop key is pressed during the execution of an instruction at normal speed. In both of these instances, the computer enters the manual mode and the automatic light is turned off if the computer is stopped at the end of the last memory cycle required for the execution of an instruction.

#### Automatic Light

The automatic light is ON when the computer is executing a stored program instruction. It is turned on by pressing the Start key, the Insert key, the SIE key, or the SCE key. The machine is stopped and the automatic light is turned off upon entry into the instruction cycle for the next instruction in sequence, if a halt instruction has been executed; the Release key or Stop key has been pressed; an overflow condition occurs (with the

overflow check switch set to Stop); or a parity error on a read or write operation (with the data check switch set to Stop).

Save Light

The save light is turned on when the Save key is pressed It is turned off by the execution of the next branch back instruction.

Insert Light

The insert light is turned on when the Insert key or 1622 Load key is pressed. It is turned off when the insert or load operation is terminated or when the Reset key is pressed.

Check Stop Light

The check stop light is ON if the machine stops as a result of detecting a parity error in the system data flow or an invalid address in MAR. (A CE switch is provided to bypass the MAR error stop for testing purposes.)

Thermal Light

The thermal light is turned on and the power is removed from the machine if an over-temperature condition is detected within the machine. When the thermal light goes off, power can again be applied.

Reader No Feed Light (Used with Special Features)

The reader no feed light is turned on if the computer attempts to execute a read instruction which specifies the paper tape reader or card reader as the input device and the reader is not in a ready condition. The computer tests for the ready condition of the selected output device. The paper tape ready condition exists when the paper tape main line switch is on and the paper tape is properly loaded. The card reader ready condition exists when the card reader power switch is on, cards have been run in, and the buffer is ready.

Write Disk (Punch/Disk) Interlock Light (Used with Special Features)

The write/disk (punch/disk) interlock light is turned on if the computer attempts to execute a write instruction which specifies the paper tape punch or card punch as an output device and the selected device is not properly loaded. The light is also turned on if a parity check error occurs while punching paper tape. The write/disk (punch/disk) interlock light is also turned on if the computer attempts to execute either a read or write instruction which specifies the disk storage drive as the input-output device and the selected unit is not ready to operate or an illegal operation is specified.

When one of the above conditions occurs, the computer hangs up in the automatic mode and the automatic light remains on.

## CUSTOMER ENGINEERING PANEL

The CE panel (Figure 6-7) contains switches and circuits for checking the operation of memory and associated circuits, operating the clock without a program, and repeating a specific cycle. The panel light, when on, indicates the clock is running.

### CE Switch Functions

CE Switch 7 (Increment MAR + 1)

Transferring this switch (01.05.50.1) suppresses instruction cycles and allows MAR to increment by one when the clock is running. This switch may be used to start the computer cycling, beginning with any address stored in the MARS register selected by the MAR Display Selector switch. Pressing the Insert key with the MAR INC switch ON will set the selected MARS register to zero.

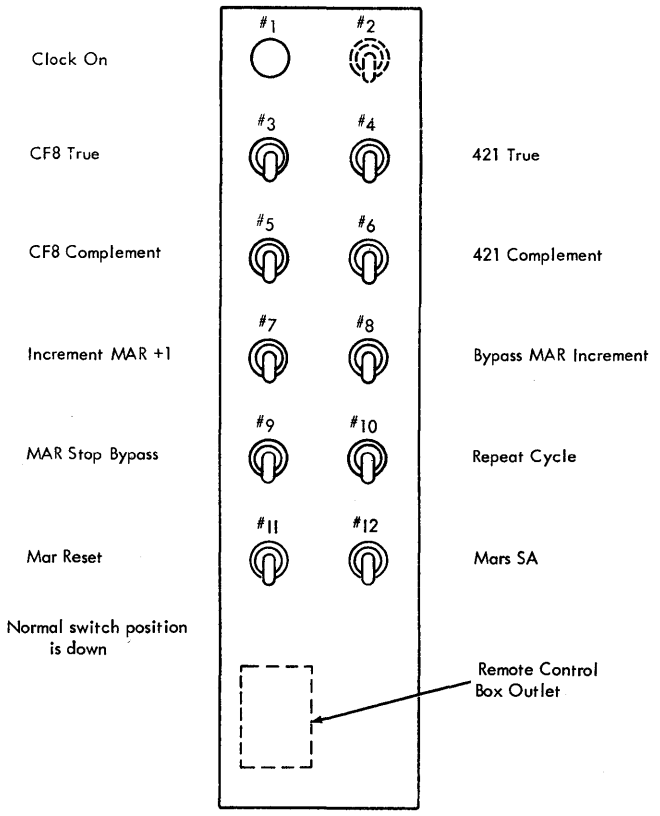



Figure 6-7. Customer Engineering Panel

CE Switch 8 (Bypass MAR Increment)

This switch, CE SW 8 on 01.05.50.1, when transferred, causes MAR to remain at the address which is stored in the MARS register selected by the display MARS switch. With CE Switch 8 and CE Switch 7 transferred and the clock running, the 1620 will continually read and write at the same memory address, the address in the selected register.

True/Complement (T/C) Switches

The T/C switches (CE Switches 3, 4, 5, and 6) are seen on 01.05.50.1. These four switches are used in various combinations. They allow a CE to perform the operations described below.

True Operation. All four T/C switches are set normal (down). At read time, data in memory is placed in MBR. At write time, the data in MBR is written into memory. The data in MBR controls the Z (inhibit) drivers.

Complement Operation. All four T/C switches are placed in the transferred (up) position. At read time the data in memory is placed in MBR. At write time the data in MBR is passed through the inhibit control logic. The bit complement of the data is then written in memory. For example, the C, F, and 1-bits are read from memory at read time. The 8, 4, and 2-bits are written back into memory.

Force Operation. The T/C switches are set to control what is written into memory. The T/C switches may be set to cause data to be stored in every bit position of a memory address and this is called "forcing all bits." If they are set to cause no data to be stored in each of the six positions, the operation is called "blanking memory." If they are set to cause data to be stored in the C, F, and 8-bit positions, this is called "forcing flag eights." If they are set to cause data to be stored in the 4, 2, and 1-bit positions, this is called "forcing sevens."

When forcing, data is read from memory into MBR at read time. At write time, MBR has no control over what is to be written back into memory. The T/C switches control writing. The table below shows the proper switch settings for forcing operations.

| | True | | Complement | |
|---|---|---|---|---|
| CE Switches | 3 | 4 | 5 | 6 |
| Normal Operation | ↓ | ↓ | ↓ | ↓ |
| Force 7 | ↑ | ↑ | ↑ | ↑ |
| Force $\bar{8}$ | ↓ | ↓ | ↑ | ↑ |
| Force Blank | ↑ | ↑ | ↓ | ↓ |
| Force All Bits | ↓ | ↓ | ↑ | ↑ |
| Force Comp Bits | ↑ | ↑ | ↑ | ↑ |

WARNING: Set CE Switches 3, 4, 5, and 6 to true (down) before returning computer to customer.

CE Switch 9 (MAR Stop Bypass)

Transferring this switch allows the clock to run during a MAR check. Transferring it also cripples the console start switch. With this switch transferred, the clock may be started (1) by the CE remote control box or (2) by depressing the console SIE or SCE key. (Transferring CE Switch 7 allows the console SIE key to substitute for the console Start key).

This switch should be used to diagnose trouble in the clock, MAR, MARS, and increment/decrement circuitry. It is not recommended for use in analyzing memory troubles, because a MAR error adversely affects memory operation.

CE Switch 10 (Repeat Cycle)

When this switch is transferred, it prevents the A/B trigger from changing. It should be used when it is desired to repeat a particular cycle during machine analysis. The switch must be transferred in the cycle preceding the one to be repeated. For example, to repeat cycle E14:

1. Single-cycle to the E13 cycle known to precede it.
2. Transfer (up) CE Switch 10.
3. Start clock.

NOTE: During this operation, address will change unless bypass MAR increment, CE Switch 8, is transferred. Also, certain logic conditions may have to be grounded to give a complete repeat cycle.

CE Switch 11 (MAR Reset)

Transferring this switch blocks MAR reset to retain the address in MAR.

CE Switch 12 (MARS SA)

Transferring this switch blocks the MARS SA (sense amp) gate. Blocking MAR reset and MARS sense amp gate, using CE Switches 11 and 12, permit the exercising of MAR and associated circuitry in one specific address without regenerating MAR errors. CE Switches 11 and 12 are usually used together and in conjunction with other CE Switches.

In the performance of stored program instructions, the computer proceeds through an Instruction cycle (I-cycle), and generally an Execution cycle (E-cycle) for each operation (Figure 7-1). The function of the I-cycle is to read the 12-digit instruction from memory and interpret it by storing and decoding the operation code; by placing the P-field and Q-field addresses in MARS storage registers; and by storing and decoding specific digits of the Q part of the instruction for branch and input-output operations, where it is required. A sequence block diagram for the I-cycle is shown in Figure 7-2. A table of function chart symbols and the I-cycle function charts are shown on pages 1, 2, 3, and 4 in the IBM Customer Engineering Instructional System Diagrams, 1620, Model 1, Data Processing System, Form 227-5769.

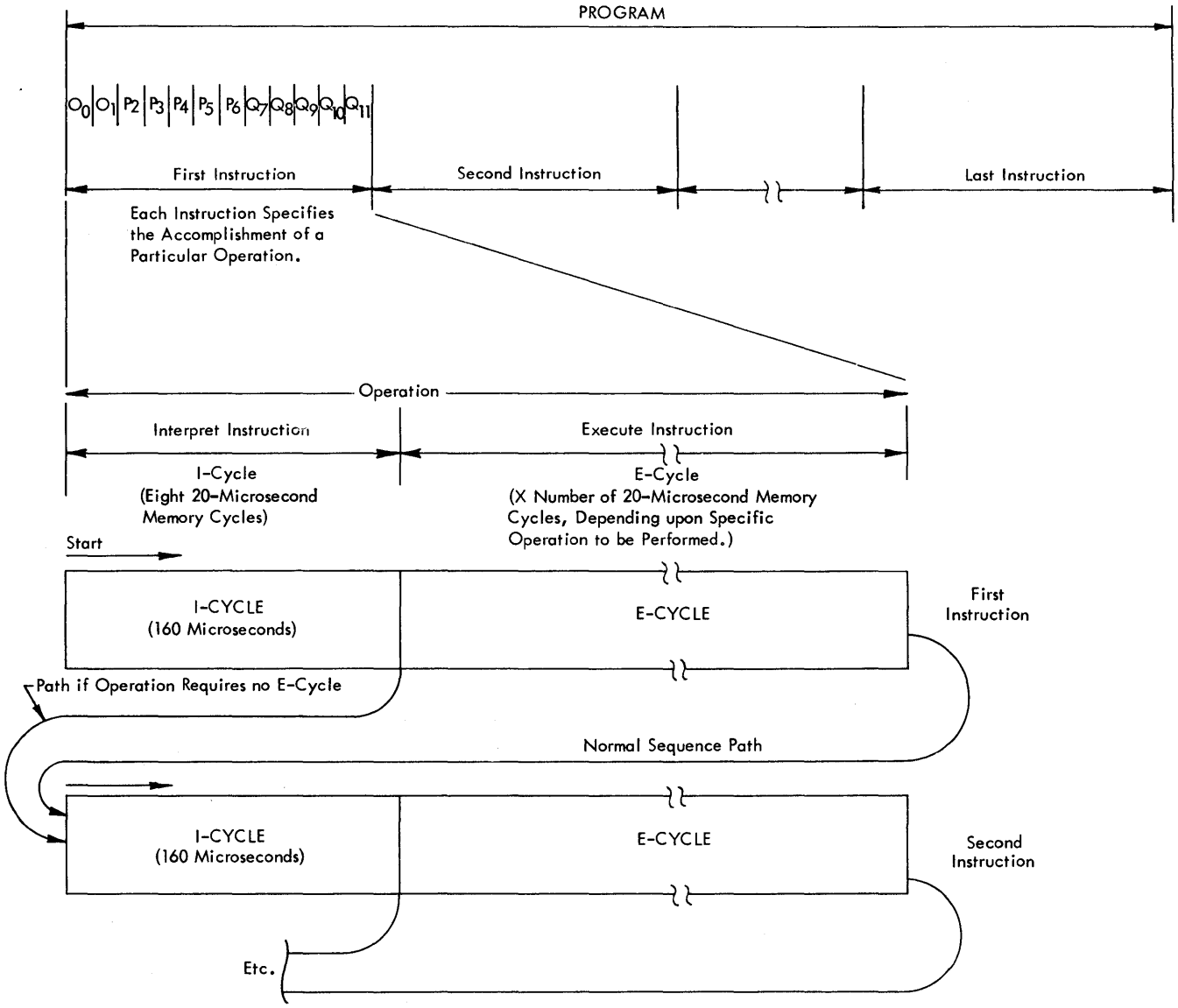



Figure 7-1. Program - I Cycle and E Cycle

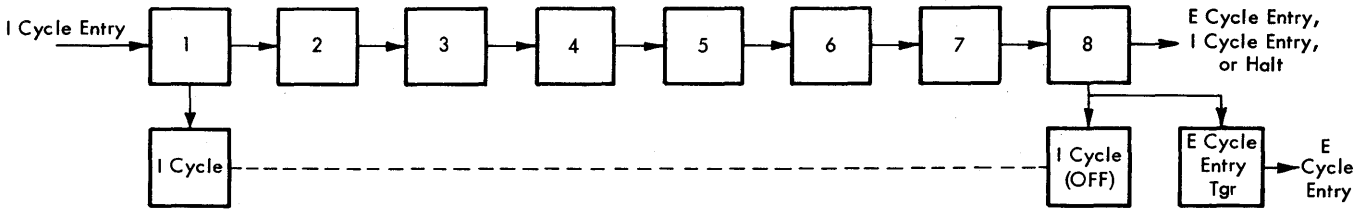



Figure 7-2. Instruction Cycle

## OBJECTIVES

1. Read the 12 digits of the instruction from the memory location specified by IR-1 and successively higher memory locations.
2. Store the digits in registers as follows:

| DIGITS | REGISTER |
|---|---|
| $O_0$ and $O_1$ | Operation (Op Reg) |
| $P_2$, $P_3$, $P_4$, $P_5$ and $P_6$ (P-Field) | Operand (OR-2 and OR-3) |
| $Q_7$, $Q_8$, $Q_9$, $Q_{10}$ and $Q_{11}$ (Q-Field) | *Operand (OR-1) |
| $Q_8$ and $Q_9$ | **Digit/Branch (D/B) |
| $Q_{11}$ | MDR |

*Q-part of an instruction is not entered into the OR-1 register if the operation is immediate. (See Objective No. 7.)

**The $Q_8$ and $Q_9$ digits are retained in the D/B register if the operation to be performed is control, read, write, dump, branch indicator, or branch no indicator.

3. Decode the Op Reg contents to determine the operation to be performed.
4. Decode the D/B register contents to determine the specific input-output device if the operation is control, read, write, or dump.
5. Decode the D/B register contents to determine the indicator or sense switch to be interrogated if the operation is branch indicator or branch no indicator.
6. Decode the $Q_{11}$ digit in MDR to determine the control function to be performed if the operation is control.
7. Store the memory address of the $Q_{11}$ digit of the instruction in the OR-1 MARS operand register if the operation is immediate.

## FUNCTIONS

The I-cycle for each instruction consists of eight 20-$\mu$sec memory (machine) cycles during which the 12-digit instruction is read from memory and stored in registers as indicated under Objective No. 2. The content of the operation register is decoded to determine the desired operation. The contents of the D/B register and MDR are decoded where applicable for the purposes stated in Objective 4, 5, and 6. The P-address of an instruction is always entered into the OR-2 and OR-3 MARS registers by Triggers 2, 3, and 4 of the I-cycle. The Q-address is entered into the OR-1 MARS register by Triggers 5, 6, and 7 of the I-cycle, except in the case of immediate operations. Certain of the non-immediate operations do not use the stored P- or Q-address because the objectives of the operation do not require it.

Immediate operations require the use of digits of the instruction as data. The five Q-part digits of the instruction are not placed in OR-1 by Triggers 5, 6, and 7 of the I-cycle. During Trigger 8 time, the normal memory cycle reset of MAR is blocked and the memory address which was placed in MAR during Trigger 7 time, is transferred to OR-1. This address is the location in memory for the $Q_{11}$ digit of the instruction. Therefore, the address in OR-1 at the end of the I-cycle designates the location in memory of a field whose units position is the $Q_{11}$ digit of the instruction itself. The field can contain as few as two digits ($Q_{10}$ and $Q_{11}$) or more than five, depending upon the location of the flag bit marking its high-order position.

Figure 7-3 illustrates the cycle-by-cycle storage of instruction digits in the operation register and MARS for the non-immediate instruction, 25 01357 02468. This instruction is assumed to be in memory at locations 00000 through 00011, and address 00000 is assumed to be in IR-1 at the beginning of the I-cycle.

Figure 7-4 illustrates the cycle-by-cycle storage for the immediate instruction 15 01357 02468, under the same conditions as in Figure 7-3.

| Memory Cycle | Triggers | IR-1 at Beginning of Memory Cycle | MAR | Increment | IR-1 at End of Memory Cycle | OP Reg | OR-2 & OR-3 | OR-1 |
|---|---|---|---|---|---|---|---|---|
| 1 | I Cycle & 1 | 00000 | 00000 | +2 | 00002 | 25 | | |
| 2 | I Cycle & 2 | 00002 | 00002 | +2 | 00004 | 25 | 01 | |
| 3 | I Cycle & 3 | 00004 | 00004 | +2 | 00006 | 25 | 01 35 | |
| 4 | I Cycle & 4 | 00006 | 00006 | +1 | 00007 | 25 | 01 35 7 | |
| 5 | I Cycle & 5 | 00007 | 00007 | +2 | 00009 | 25 | 01 35 7 | 0 |
| 6 | I Cycle & 6 | 00009 | 00009 | +2 | 00011 | 25 | 01 35 7 | 0 24 |
| 7 | I Cycle & 7 | 00011 | 00011 | +1 | 00012 | 25 | 01 35 7 | 0 24 68 * |
| 8 | 8 | ----- | 00011 | -- | 00012 | 25 | 01 35 7 | 0 24 68 |

* If the operation to be performed is control, read, write, dump, branch indicator, or branch no indicator the Digit/Branch register is not reset during Trigger 7 time. However, the contents of the Digit/Branch register is entered into OR-1 tens. With the example used in this figure, OR-1 will contain 02424 at the end of Trigger 7 time.

Figure 7-3. Instruction Cycle - Non Immediate

| Memory Cycle | I Cycle Triggers | IR-1 at Beginning of Memory Cycle | MAR | Incr | IR-1 at End of Memory Cycle | OP Reg | OR-2 & OR-3 | OR-1 |
|---|---|---|---|---|---|---|---|---|
| 1 | I Cycle & 1 | 00000 | 00000 | +2 | 00002 | 15 | | |
| 2 | I Cycle & 2 | 00002 | 00002 | +2 | 00004 | 15 | 01 | |
| 3 | I Cycle & 3 | 00004 | 00004 | +2 | 00006 | 15 | 01 35 | |
| 4 | I Cycle & 4 | 00006 | 00006 | +1 | 00007 | 15 | 01 35 7 | |
| 5 | I Cycle & 5 | 00007 | 00007 | +2 | 00009 | 15 | 01 35 7 | ----- |
| 6 | I Cycle & 6 | 00009 | 00009 | +2 | 00011 | 15 | 01 35 7 | ----- |
| 7 | I Cycle & 7 | 00011 | 00011 | +1 | 00012 | 15 | 01 35 7 | ----- |
| 8 | 8 | ----- | 00011 | -- | 00012 | 15 | 01 35 7 | *00011 |

* Trigger 8, OR-1 Write Drivers (From MAR through Incr/Decr bypassed)

Figure 7-4. Instruction Cycle - Immediate

## Auxiliary Triggers

### Status

I-Cycle Trigger (01.15.10.1).

1. Turned on by Trigger 1 and remains on through Trigger 7 time.
2. Turned off by Trigger 8.

Decrement Trigger (01.60.05.1).

1. Turned off (increment) by the Trigger 1 and remains off for the entire I-cycle.

E-Cycle Entry Trigger.

1. Turned on by Trigger 8.
2. Turned off at T5 time of the first memory cycle after Trigger 8 time.

### Objectives

I-Cycle Trigger.

1. Reset the units position of the D/B register for each of the memory cycles controlled by Triggers 1 through 7. (See Item 4.)
2. Read out of memory per IR-1 and store the digit in the units position of the D/B register for each of the memory cycles controlled by Triggers 1 through 7. (See Item 4.)
3. Write back into IR-1 from MAR incremented for each of the memory cycles controlled by Triggers 1 through 7. (Increment +1 or +2 is controlled by the individual Triggers 1 through 7.)
4. Block reset of D/B register units at Trigger 7 time of Op Codes 34, 35, 36, 37, 38, 39, 46 and 47.

E-Cycle Entry Trigger (01.15.18.1).

1. Turn off the T/C trigger to change the initial status set by Trigger 1 if the operation to be performed is subtract or compare.
2. Enter I-cycle for the next instruction in sequence if this instruction is No Operation — Code 41.
3. Enter E-cycle (turn on Trigger 18) if this instruction is Branch Indicator — Code 46 and the Branch Test trigger is on.
4. Enter I-cycle for the next instruction in sequence if this instruction is Branch Indicator — Code 46 and the Branch Test trigger is off.
5. Enter E-cycle (turn on Trigger 18) if this instruction is Branch No Indicator — Code 47 and the Branch Test trigger is off.
6. Enter I-cycle for the next instruction in sequence if this instruction is Branch No Indicator — Code 47 and the Branch Test trigger is on.

## I-Timer Triggers

### Objectives of I-Timer Triggers

Trigger 1 (01.15.11.1).

1. Reset OFF (I-cycle reset) the following triggers for use during the execution cycle.
   a. Digit/Record Mark/Group Mark
   b. Recomplement
   c. Recomplement control
   d. Field mark No. 1
   e. Field mark No. 2
   f. Dividend and remainder sign*
   g. Divide add*
   h. First divide cycle*
   i. Last divide cycle*
   j. Decrement
   k. Trigger No. 12
   l. Trigger No. 13
   m. M/Q register
   n. First cycle
   o. Carry in
   p. Carry out
   q. Indirect Address (IA)*

*Special Feature

2. Turn on the I-cycle trigger.
3. Energize the A-trigger reset and B-trigger reset lines to turn off various I, E, and auxiliary triggers that are required to be reset for the start of a new instruction and that are not reset by the I-cycle reset (Item 1).
4. Read out of memory per IR-1 (function of I-cycle trigger) and store the even digit ($O_0$) in Op Reg tens (via MDR). Store the odd digit ($O_1$) in Op Reg units (via MBR-odd).
5. Write back IR-1 (function of I-cycle trigger) incremented +2.

6. Reset OR-1, OR-2, and OR-3 to permit setting of addresses later in the I-cycle.
7. Turn on the True/Complement (T/C) trigger to set initial status for add, subtract, and compare operations.
8. Turn off the I/O Exit trigger.
9. Turn on the Start 1 trigger.

Trigger 2 (01.15.12.1).

1. Read out of memory per IR-1 (function of I-cycle trigger) and write the even digit ($P_2$) into OR-2 and OR-3 ten-thousands position (via MDR and D/B Reg units). Write the odd digit ($P_3$) into OR-2 and OR-3 thousands positions (via MBR-odd and D/B Reg tens).
2. Write back IR-1 (function of I-cycle trigger) incremented +2.
3. Reset OFF the Branch Test trigger to permit setting the trigger during Trigger 7 time of the I-cycle for branch operations.

Trigger 3 (01.15.13.1).

1. Read out of memory per IR-1 (function of I-cycle trigger) and write the even digit ($P_4$) into OR-2 and OR-3 hundreds position (via MDR and D/B Reg units). Write the odd digit ($P_5$) into OR-2 and OR-3 tens position (via MBR-odd and D/B Reg tens).
2. Write back IR-1 (function of I-cycle trigger) incremented +2.

Trigger 4 (01.15.14.1).

1. Read out of memory per IR-1 (function of I-cycle trigger) and write the even digit ($P_6$) into OR-2 and OR-3 units position (via MDR and D/B Reg units).
2. Write back IR-1 incremented +1 (function of I-cycle trigger).

Trigger 5 (01.15.15.1).

1. Read out of memory per IR-1 (function of I-cycle trigger) and write the odd digit ($Q_7$) into OR-1 ten-thousands position (via MDR and D/B Reg units). An immediate instruction prevents this digit from being written into OR-1. (See Trigger 8, Objective 3 following.)
2. Write back IR-1 (function of I-cycle trigger)incremented +2.

Trigger 6 (01.15.16.1).

1. Read out of memory per IR-1 (function of I-cycle trigger) and write the even digit ($Q_8$) into OR-1 thousands position (via MBR-even and D/B Reg tens). Write the odd digit ($Q_9$) into OR-1 hundreds position (via MDR and D/B Reg units). An immediate instruction prevents these digits from being written into OR-1. (See Trigger 8, Objective 3 following.)
2. Write back IR-1 (function of I-cycle trigger) incremented +2.

Trigger 7 (01.15.17.1).

1. For codes other than 34, 35, 36, 37, 38, 39, 46 and 47, read out of memory per IR-1 (function of I-cycle trigger) and write the even digit ($Q_{10}$) into OR-1 tens position (via MBR-even and D/B Reg tens. Write the odd digit ($Q_{11}$) into OR-1 units position (via MDR and D/B Reg units). An immediate instruction prevents these digits from being written into OR-1. (See Trigger 8, Objective 3 following).
2. Write back IR-1 incremented +1 (function of I-cycle trigger).
3. For Codes 34, 35, 36, 37, 38, 39, 46, and 47, block the reset of D/B register tens. The reset of D/B units and tens is blocked for Codes 34 through 39 thus preserving the I/O device code or branch indicator code for later use.
4. For Codes 46 and 47, turn on the Branch Test trigger if the indicator or sense switch designated by the D/B Register is on.

Trigger 8 (01.15.18.1).

1. Turn off the I-cycle trigger.
2. Block reset of MAR to retain the address of the $Q_{11}$ digit of the instruction for use by immediate instructions.
3. For immediate instructions, write the address of the $Q_{11}$ digit of the instruction into OR-1 from MAR.
4. Stop the computer if this instruction is Halt — Code 48.
5. Turn on the E-cycle Entry trigger.
6. Turn on the Decrement trigger if the operation code to be performed requires a decrement function.

The performance of a computer operation is normally divided into two parts, an instruction cycle (I-cycle) and an execution cycle (E-cycle). (See Figure 7-1).

Each E-cycle is immediately preceded by its associated I-cycle during which the instruction is read from memory and interpreted. The I-cycle is described in Section 7.

The function of the E-cycle is to accomplish the objectives of the particular operation specified by the instruction.

## OBJECTIVE

Execute the instruction read from memory and interpreted during the associated I-cycle.

## FUNCTIONS

An E-cycle consists of an even number of 20-$\mu$sec memory cycles under the control of E-timer triggers. The required number of memory cycles depends upon the specific operation to be performed and also upon the length of fields and records in arithmetic, transmit, and input-output operations.

The following instructions are complete at the end of their I-cycle and require no E-cycle for their execution:

1. Branch indicator, if no branch occurs
2. Branch no indicator, if no branch occurs
3. No operation
4. Halt.

Generally, when the E-cycle for an operation is complete, the computer is directed to enter the I-cycle for the next instruction in sequence. In the case of a halt instruction, operator intervention (press Start key) is required to cause the computer to enter the I-cycle for the next instruction in sequence.

## E-TIMER TRIGGERS

The trigger directory in the Appendix lists the E-timer triggers and indicates their location in the System Diagrams.

In general, each E-timer trigger controls all of the functions which must be accomplished during the memory cycle for which it is on. At the beginning of the following memory cycle it serves to turn on the E-timer trigger which is to assume control and is turned off (A or B trigger reset) by the new E-timer trigger (Figure 8-1).

Because identical or similar functions are accomplished during the execution of two or more different computer operations, many of the E-timer triggers are used with more than one operation. For example, the Branch (Code 49) operation is executed in two memory cycles, using E-timer Triggers 18 and 19. The Branch On Digit (Code 43) operation is executed in four memory cycles, using E-timer Triggers 28, 29, 18, and 19. Triggers 18 and 19 are used with both operations to accomplish identical functions. The E-timer trigger chart in the Appendix shows the E-timer triggers that are used with each computer operation.

In arithmetic, transmit, and input-output operations where fields or records are processed, a series of E-timer triggers is used to process the first digit (or character) of the field or record and then the series of or parts of the series are looped as many times as required to process each subsequent digit (or character). (See Figure 8-2).

The functions of individual E-timer triggers are described in Sections 9, through 13 of this manual as they are used to accomplish the objectives of the various computer operations.

## AUXILIARY TRIGGERS

Auxiliary triggers are used to establish or recognize conditions within the computer which must be considered to properly accomplish the execution of an instruction.

The auxiliary trigger chart in the Appendix shows the auxiliary triggers that are used with each computer operation. Auxiliary trigger locations on the System Diagrams are indicated in the trigger directory in the Appendix, under "Named" Triggers.

### Functions of Auxiliary Triggers

Functions of the most commonly used auxiliary triggers are described below. The status of all auxiliary triggers is described in Sections 9, through 13 of

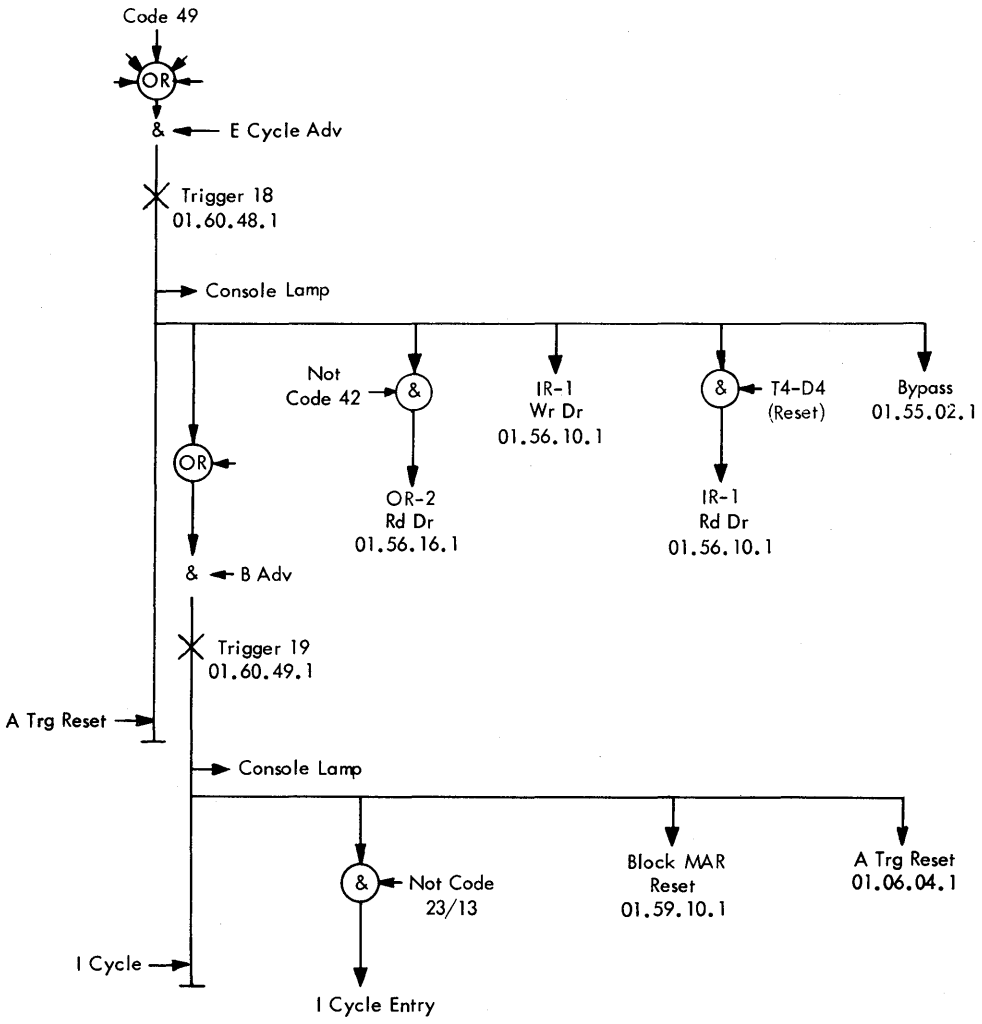



Figure 8-1. E Timer Functions

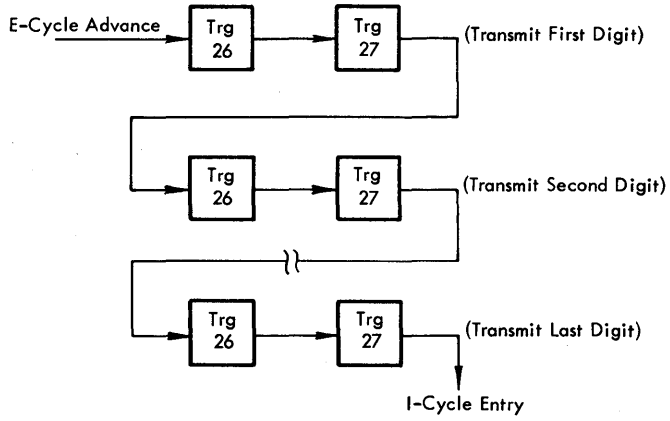
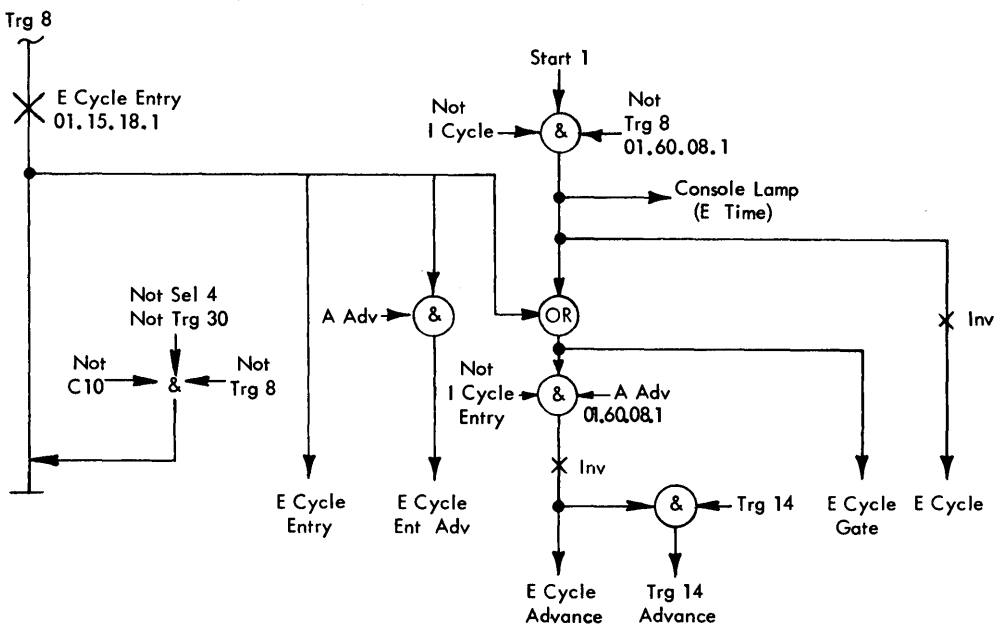



Figure 8-2. Transmit Field

this manual as these triggers are used in the various computer operations.

E-Cycle Entry (01.15.18.1). The output of the E-cycle Entry trigger is used to develop several E-cycle timed gates. These gates are used to control the turn-on of various E-timmer triggers. They are developed as shown on the function chart, Figure 8-3. Note that the E-cycle advance signal and the Trigger 14 advance signal are developed only at A-advance time.

Decrement (Decr) (01.60.05.1). The Decrement trigger is turned on (decrement) or off (increment) as necessitated by the requirements of each computer operation. All basic instruction cycles require



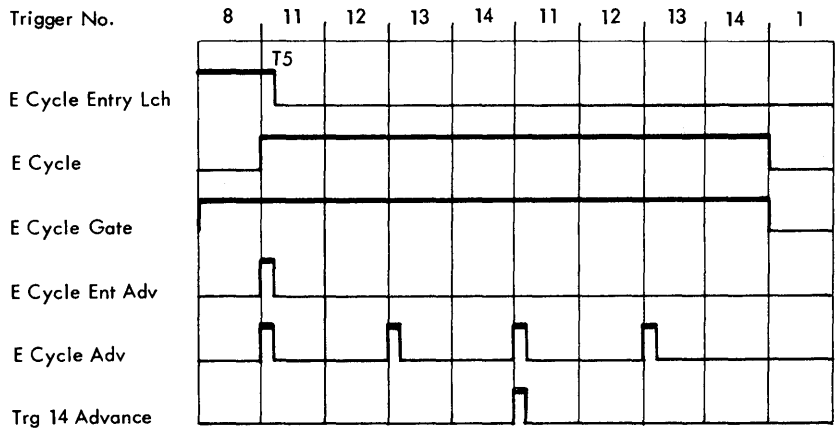




Figure 8-3. E Cycle Gates

increment operation. The increment/decrement requirements of the execution cycle for each operation are indicated on the auxiliary trigger chart in the Appendix. The function of the Decrement trigger is to determine by means of its ON or OFF status whether an address in MAR is to be decremented or incremented before it is written into MARS. This function is accomplished by control of the increment/decrement switch.

First Cycle (01.63.10.1). The primary function of the First Cycle trigger is to permit a flag bit in the units position of a field to be interpreted as denoting the sign of the field rather than the high-order position of the field. The First Cycle trigger is ON only during the memory cycle (or cycles) in which the units position of fields is being processed in arithmetic and transmit field operations.

Field Mark No. 1 (01.63.30.1). Field Mark No. 1 trigger is turned on during arithmetic and transmit field operations when the high-order position of the Q-field is read from memory to indicate that the entire Q-field has been processed. In a branch no flag operation, Field Mark No. 1 trigger is turned on to recognize the presence of a flag bit in the memory location which is interrogated.

Field Mark No. 2 (01.63.30.1). Field Mark No. 2 trigger is turned on during add, subtract, compare, and multiply operations when the high-order position of the P-field is read from memory to indicate that the entire P-field has been processed.

True/Complement (01.63.20.1). The T/C trigger is manipulated during add, subtract, and compare operations to establish an initial condition and alter that condition according to the signs of the factors involved in the particular add, subtract, or compare operation. The function of the T/C trigger is to determine by means of its ON (true) or OFF (complement) status whether digits presented to the T/C switch appear at its output unchanged (true) or complemented (complement).

High/Plus (01.60.40.1). The H/P trigger is manipulated during arithmetic operations to cause the trigger to indicate the sign of the result by means of its status at the end of the particular arithmetic operation. ON indicates plus; OFF indicates minus. In compare operations, the status of the H/P trigger indicates which of two fields is algebraically higher. A zero result of arithmetic or compare operations will turn off the H/P trigger. trigger.

Equal/Zero (01.60.41.1). The E/Z trigger is turned on at the beginning of arithmetic operations and turned off during the particular arithmetic operation if the result is not zero. In compare operations, if two fields are equal, the E/Z trigger remains ON to indicate an equal condition. If a comparison is made of two fields having unlike signs and containing a significant digit, the E/Z trigger is turned off.

Carry Out (01.63.40.1). The Carry Out trigger is turned on during arithmetic operations if a digit with a flag bit is read into MDR from the add table in memory or if a carry occurs in one position that will carry into a position which contains a "9."

Carry In (01.63.40.1). The Carry In trigger is turned on during arithmetic operations if the addition of the two previous digits resulted in a carry out or if the add table address for the units position of a sum is being developed on a complement operation (to obtain 10's complement in units position).

Recomplement Control (01.60.24.1). The Recomplement Control trigger is turned on near the end of an add or subtract operation if the developed sum or difference is in a complement form. The primary function of the Recomplement Control trigger is to initiate recomplement of the complement sum or difference to the true form.

Recomplement (01.60.32.1). The Recomplement trigger is turned on at the beginning of recomplement. Its functions are to continue recomplement until all digits of the complement sum or difference have been recomplemented and then to direct the computer to enter the I-cycle for the next instruction in sequence.

Overflow (01.60.40.1). The Overflow trigger is turned on in add, subtract, and compare operations if the length of the P-field is inadequate.

Digit/Record Mark/Group Mark (01.63.50.1). The Digit/Record Mark/Group Mark (D/RM/GM) trigger is used during add, subtract, and compare operations to detect a digit in MDR. The D/RM/GM trigger is turned on to terminate a transmit record operation or a write operation when the record mark character is read from memory into MDR. The D/RM/GM trigger is turned on if a record mark is decoded during a branch no record mark operation or if a digit is decoded during a branch on digit operation. The group mark function is associated with a special feature, the IBM 1311.

Branch Test (01.25.35.1). The Branch Test trigger is turned on during Trigger 7 time of the I-cycle for branch indicator and branch no indicator instructions if the program switch or indicator interrogated by the instruction is ON. The status of the Branch Test trigger is then used to determine whether the computer proceeds to the next instruction in sequence or branches to another instruction.

READ-Y POINT

During the execution of certain computer operations, it is required that in one memory cycle a particular memory location be cleared, and to write into it, a digit which was stored in MDR during the previous memory cycle. A "Read-Y Point" function is available to satisy that requirement by accomplishing the following:

1. The reset of MDR is blocked to preserve the new digit.
2. Either the even or the odd sense amplifiers are blocked when the memory location designated by the address in MAR is read out. (The memory location is thus cleared and its content is prevented from reaching MBR.)

3. The digit in MDR is transferred to MBR-even or MBR-odd, depending upon whether the address in MAR is even or odd. The new digit is then written into the memory location designated by the address in MAR when the normal "write-back" into memory function is performed. The function chart shown in Figure 8-4 includes the Read-Y Point function.

## BLOCK MEMORY SENSE AMPLIFIERS

Where it is required, during computer operations, that new information be placed into two adjacent memory locations in the same memory cycle, a "Block Mem SA" function is available to block both the even and odd memory sense amplifiers. Clearing the product area to zeros during multiply operations and storing alphameric information during read alphamerically operations requires the use of the Block Mem SA function.

The function chart shown in Figure 8-4 includes the Block Mem SA function.

## SIGNIFICANCE OF P & Q PARTS OF INSTRUCTIONS

Figures 8-5a and 8-5b indicate the significance of the P and Q parts of instructions for each of the operations that the computer is capable of performing.

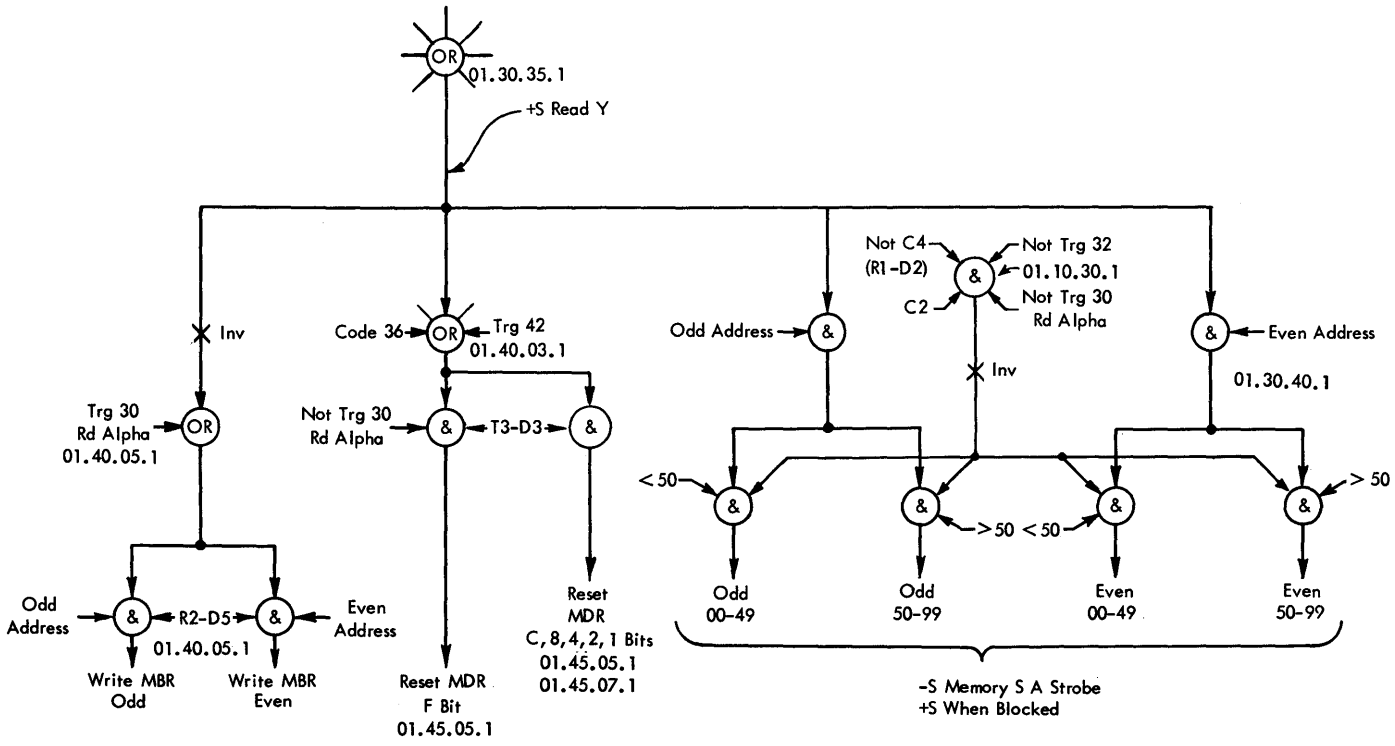



Figure 8-4. Read-Y and Block Memory Sense Amplifiers

| OP Code | Instruction | P Address | Q Address |
|---|---|---|---|
| 11 | Add (I) | Location of units position of Augend and Result. | $Q_{11}$ is units position of Addend. |
| 21 | Add | Same as Code 11. | Location of units position of Addend. |
| 12 | Subtract (I) | Location of units position of Minuend and Result. | $Q_{11}$ is units position of Subtrahend. |
| 22 | Subtract | Same as Code 12. | Location of units position of Subtrahend. |
| 13 | Multiply (I) | Location of units position of Multiplicand. | $Q_{11}$ is units position of Multiplier. |
| 23 | Multiply | Same as Code 13. | Location of units position of Multiplier. |
| 14 | Compare (I) | Location of units position of field compared with Q field. | $Q_{11}$ is units position of field compared with P field. |
| 24 | Compare | Same as Code 14. | Location of units position of field compared with P field. |
| 15 | Transmit Digit (I) | Location to which digit is transmitted. | $Q_{11}$ is digit transmitted. |
| 25 | Transmit Digit | Same as Code 15. | Location of digit transmitted. |
| 16 | Transmit Field (I) | Location to which units position of field is transmitted. | $Q_{11}$ is units position of field transmitted. |
| 26 | Transmit Field | Same as Code 16. | Location of units position of field transmitted. |
| 17 | Branch and Transmit (I) | "P minus one" is the memory address to which the units position of field is to be transmitted. The P address is the memory address of the high-order digit of the next instruction to be interpreted and executed. | $Q_{11}$ is units position of field transmitted. |
| 27 | Branch and Transmit | Same as Code 17. | Location of units position of field transmitted. |
| 31 | Transmit Record | Location to which high-order position of record is transmitted. | Location of high-order position of record transmitted. |
| 32 | Set Flag | Location at which flag is set. | Not used. |
| 33 | Clear Flag | Location at which flag is cleared. | Not used. |
| 34 | Control | Not used. | $Q_8$ and $Q_9$ specify I/O device.<br>$Q_{11}$ specifies control function performed. |
| 35 | Dump Numerically | Location of first character written. | $Q_8$ and $Q_9$ specify output device. |
| 36 | Read Numerically | Location where first character is stored or address of Disk Control Field. | $Q_8$ and $Q_9$ specify disk storage or input device.<br>$Q_{11}$ specifies function performed. |
| 37 | Read Alphamerically | P—1: location where zone digit of first character is stored.<br>P: location where numerical digit of first character is stored. | $Q_8$ and $Q_9$ specify input device. |
| 38 | Write Numerically | Location of first character written or address of Disk Control Field. | $Q_8$ and $Q_9$ specify output device or disk storage.<br>$Q_{11}$ specifies function performed. |
| (I) Immediate | | | |

Figure 8-5a. Significance of P & Q Parts of an Instruction

| OP Code | Instruction | P Address | Q Address |
|---|---|---|---|
| 39 | Write Alphamerically | P—1: location of zone digit of first character written.<br>P: location of numerical digit of first character written. | Same as Code 35. |
| 41 | No OP | Not used. | Not used. |
| 42 | Branch Back | Not used. | Not used. |
| 43 | Branch on Digit | Branch: location of next instruction executed.<br>No Branch: Not used. | Location tested for digit other than zero. |
| 44 | Branch No Flag | Same as Code 43 | Location tested for flag bit. |
| 45 | Branch No Record Mark | Same as Code 43. | Location tested for Record Mark character. |
| 46 | Branch On Indicator | Same as Code 43. | $Q_8$ and $Q_9$ specify program switch or indicator tested. |
| 47 | Branch No Indicator | Same as Code 43. | Same as Code 46 |
| 48 | Halt | Not used. | Not used. |
| 49 | Branch | Location of next instruction executed. | Not used. |

Figure 8-5b. Significance of P & Q Parts of an Instruction

Internal transmission operations accomplish the transfer of a digit, a field, or a record from one memory location to another. Two memory cycles are required for processing each digit. During the first memory cycle, the digit to be transmitted is read out of memory and stored in MDR. During the second memory cycle, the digit in MDR is transferred to the desired memory location.

Function charts for 1620 operation codes are located in the IBM Customer Engineering Instructional System Diagrams, 1620 Model 1, Data Processing System, (Form 227-5769).

## TRANSMIT DIGIT (CODE 25 - TD)

The sequence block diagram for this operation is shown in Figure 9-1. The function chart for this operation is shown in the Instructional System Diagrams on page 5.

### Objective

Replace the single digit at the P-address (OR-2) with the digit and its F-bit, if any, at the Q-address (OR-1).

### Functions

The digit, including its F-bit, if any, at the P-address (OR-2) prior to the transmission is obliterated. The digit at the Q-address (OR-1) remains unchanged. The operation is terminated when the single digit has been transmitted.

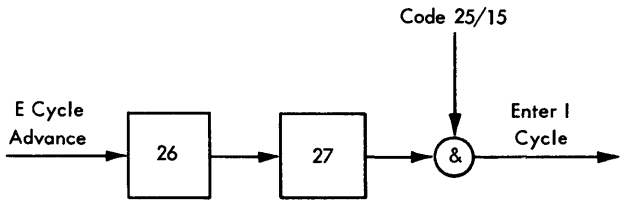



Figure 9-1. Transmit Digit - Code 25/15

### Auxiliary Triggers

None are used.

### E-Timer Trigger Objectives

Trigger 26 (01.60.57.1).

1. Read out of memory per OR-1 and store the digit in MDR.

Trigger 27 (01.60.57.1).

1. Block reset of MDR (Read-Y).
2. Read out memory per OR-2 with either the odd or even sense amplifiers blocked (Read-Y), depending on whether the OR-2 address is odd or even, to clear the memory location.
3. Transfer MDR to MBR.
4. Write into memory per OR-2 from MBR.
5. End operation and enter I-cycle for the next instruction in sequence.

## TRANSMIT DIGIT IMMEDIATE (CODE 15 - TDM)

The sequence block diagram for this operation is shown in Figure 9-1. The function chart for this operation is shown in the Instructional System Diagrams on page 5.

### Objective

Replace the single digit at the P-address (OR-2) with the digit and its F-bit, if any, in the units position ($Q_{11}$) of the transmit digit immediate instruction.

### Functions

The digit including its F-bit, if any, at the P-address (OR-2) prior to transmission, is obliterated. The digit at the Q-address (OR-1) remains unchanged. The operation is terminated when the single digit has been transmitted.

Auxiliary Triggers

None are used.

E-Timer Trigger Objectives

See Transmit Digit - Code 25.

TRANSMIT FIELD (CODE 26 - TF)

The sequence block diagram for this operation is shown in Figure 9-2. The function chart for this operation is shown in the Instructional System Diagrams on page 5.

Objective

Transfer the field, including F-bits for sign and field definition, at the Q-address (OR-1) to the memory location designated by the P-address (OR-2) and successively lower memory locations.

Functions

Transmission proceeds serially, one digit at a time, from low-order to high-order digit of the transmitted field until the operation is terminated by a flag bit (Field Mark No. 1) in the high-order position of the transmitted field. The flag bits in the high-order and units position of the transmitted field are duplicated in the field at P. The digits in the field at P, prior to transmission are obliterated, including their flag bits, if any.

Auxiliary Trigger Status

First Cycle Trigger (01.63.10.1).

1. Turned on by Trigger 26 ANDed with E-cycle entry.
2. Turned off by Trigger 27 on first transmit cycle.

Decrement Trigger (01.60.05.1).

1. Turned on (decrement) during Trigger 8 time of the preceding I-cycle.
2. Remains ON until the next I-cycle is entered.

Field Mark No. 1 Trigger (01.63.30.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be OFF when E-cycle is entered.

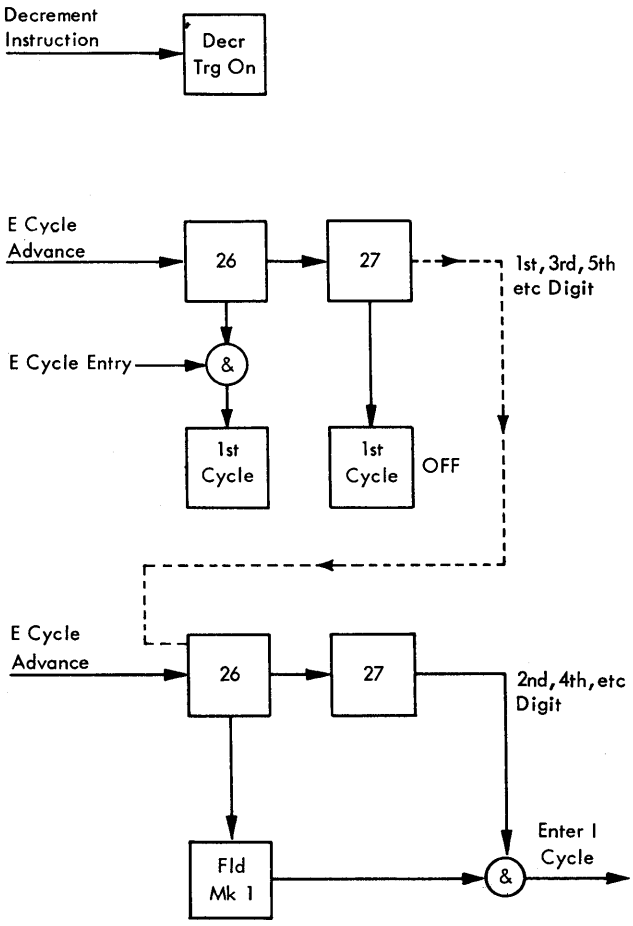



Figure 9-2. Transmit Field - Code 26/16

2. Cannot be turned on during first transmit cycle (Q-field must be a minimum of two digits).
3. Turned on during Trigger 26 time of the transmit cycle in which the high-order digit of the Q-field is read out of memory.

E-Timer Trigger Objectives

Trigger 26 (01.60.57.1).

1. Read out of memory per OR-1 and store the digit in MDR.
2. Write back OR-1 decremented.

Trigger 27 (01.60.57.1).

1. Block reset of MDR (Read-Y).
2. Read out of memory per OR-2 with either the odd or even sense amplifiers blocked (Read-Y), to clear the memory location, depending on whether the OR-2 address is odd or even.

3. Write back OR-2 decremented.
4. Transfer MDR to MBR.
5. Write into memory per OR-2 from MBR. (Repeat Trigger 26 and Trigger 27, Objectives 1, 2, 3, 4, and 5 for each digit of the field.)
6. End operation when all digits of the field have been transferred and enter I-cycle for the next instruction in sequence.

## TRANSMIT FIELD IMMEDIATE ( CODE 16-TFM)

The sequence block diagram for this operation is shown in Figure 9-2. The function chart for this operation is shown in the Instructional System Diagrams on page 5.

### Objective

Transfer the field, including F-bits for sign and field definition, whose units position is the $Q_{11}$ digit of the transmit field immediate instruction to the memory location designated by the P-address (OR-2) and successively lower memory locations.

### Functions

See Transmit Field - Code 26.

### Auxiliary Triggers Status

See Transmit Field - Code 26.

### E-Timer Triggers

See Transmit Field - Code 26

## TRANSMIT RECORD ( CODE 31 - TR)

The sequence block diagram for this operation is shown in Figure 9-3. The function chart for this operation is shown in the Instructional System Diagrams on page 5.

### Objective

Transfer the record, including F-bits for sign and field definition, at the Q-address (OR-1) to the memory location designated by the P-address (OR-2) and successively higher memory locations.

### Functions

Transmission proceeds serially, one digit at a time, from high-order to low-order digit of the transmitted record until the operation is terminated by a record mark in the low-order position of the transmitted record. All flag bits in the record at Q are duplicated in the record at P. The digits in the record at P prior to the transmission are obliterated, including their flag bits, if any. The record mark is duplicated in the low-order positions of the record at P.

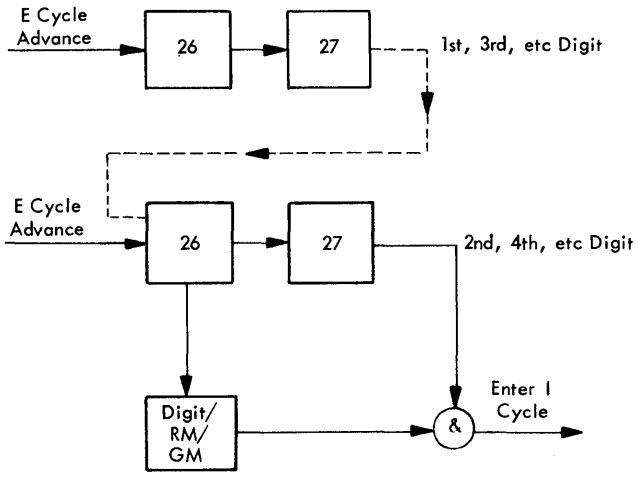



Figure 9-3. Transmit Record - Code 31

### Auxiliary Trigger Status

Decrement Trigger (01.60.05.1).
1. OFF (increment) during the I-cycle.
2. Remains OFF throughout the E-cycle.

Digit/Record Mark/Group Mark Trigger (01.63.50.1).
1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Turned on during Trigger 26 time of the transmit cycle in which the record mark at the Q-address (OR-1) is read out of memory.

E-Timer Trigger Objectives

Trigger 26 (01.60.57.1).

1. Read out of memory per OR-1 and store the digit in MDR.
2. Write back OR-1 incremented +1.

Trigger 27 (01.60.57.1)

1. Block reset of MDR (Read-Y).
2. Read out of memory per OR-2 with either the odd or the even sense amplifiers blocked (Read-Y), depending on whether the OR-2 address is odd or even, to clear the memory location.
3. Write back OR-2 incremented +1.
4. Transfer MDR to MBR.
5. Write into memory from MBR. (Repeat Trigger 26 and 27, Objectives 1, 2, 3, 4, and 5 for each digit of the record.)
6. End operation when all digits of the record and the record mark have been transferred and enter I-cycle for the next instruction in sequence.

Branch instructions are used in a program to permit alteration of the sequential execution of the program. These instructions may be classified into two categories as follows:

1. Unconditional branch instructions:
   a. Branch
   b. Branch and transmit
   c. Branch back
2. Conditional branch instructions:
   a. Branch on digit
   b. Branch no flag
   c. Branch no record mark
   d. Branch indicator
   e. Branch no indicator

Unconditional branch instructions always alter the sequential execution of a program when they are executed. Whether branching occurs as a result of conditional branch instructions is dependent upon the status of a sense switch on the console or an indicator within the computer.

The P-address in every branch instruction must be even because it designates the address of another instruction.

Function charts for 1620 operation codes are located in the IBM Customer Engineering Instructional System Diagrams, 1620 Model 1, Data Processing System (Form 227-5769).

## BRANCH (CODE 49 - B)

The sequence block diagram for this operation is shown in Figure 10-1. The function chart for this operation is shown in the Instructional System Diagrams on page 6.

### Objective

Branch (unconditionally) to the instruction at the P-address (OR-2).


Figure 10-1. Branch - Code 49

### Functions

The content of OR-2 is placed in IR-1. The address of the next instruction to be executed is then specified by IR-1.

The Q-address of this instruction is placed in OR-1 but is not used in the execution of this operation.

### Auxiliary Triggers

None are used.

### E-Timer Trigger Objectives

Trigger 18 (01.60.48.1).

1. Read OR-2 into MAR.
2. Write from MAR into IR-1 bypassed.

Trigger 19 (01.60.49.1).
(Dummy E-Timer)

1. Block MAR reset to prevent VRC error.
2. End operation and enter I-cycle for the instruction at the P-address of the branch instruction (now stored in IR-1).

## BRANCH AND TRANSMIT (CODE 27—BT)

The sequence block diagram for this operation is shown in Figure 10-2. The function chart for this operation is shown in the Instructional System Diagrams on page 7.

### Objective

1. Save the address of the next instruction in sequence. Execution of the next branch back instruction directs the computer to resume the program beginning with the instruction at the saved address.
2. Transmit the field at the Q-address (OR-1) to the memory location designated by the P-address minus 1 and successively lower memory locations.
3. Branch to the instruction at the P-address.

## Functions

The address of the next instruction in sequence is saved by storing the content of IR-1 in IR-2.

The P-address (OR-2) is transferred into IR-1 so that when the computer enters the next I-cycle it will execute the instruction at the P-address.

Transmission of the Q-field proceeds serially, one digit at a time, from low-order to high-order digit of the transmitted field until the operation is terminated by a flag bit (Field Mark No. 1) in the high-order position of the transmitted field. The flag bits in the High-order and units position of the transmitted field are duplicated in the field at P minus 1. The digits in the field at P minus 1 prior to transmission are obliterated, including their flag bits, if any. When transmission is completed, enter I-cycle for the instruction at the P-address now stored in IR-1.

## Auxiliary Trigger Status

First Cycle Trigger (01.63.10.1).

1. Turned on by Trigger 15.
2. Turned off by Trigger 27 on first transmit cycle.

Decrement Trigger (01.60.05.1).

1. Turned on (decrement) during Trigger 8 time of the preceding I-cycle.
2. Remains ON until the next I-cycle is entered.

Field Mark No. 1 Trigger (01.63.30.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be OFF when E-cycle is entered.
2. Cannot be turned on during first transmit cycle. (Q-field must be a minimum of two digits.)
3. Turned on during Trigger 26 time of the transmit cycle in which the high-order digit of the Q-field is read out of memory.

## E-Timer Trigger Objectives

Trigger 15 (01.60.45.1).

1. Read IR-1 into MAR.
2. Write from MAR into IR-2 bypassed.

Trigger 16 (01.60.45.1).

1. Read OR-2 into MAR.
2. Write from MAR into IR-1 bypassed.
3. Write from MAR into OR-2 decremented (P-address minus 1).

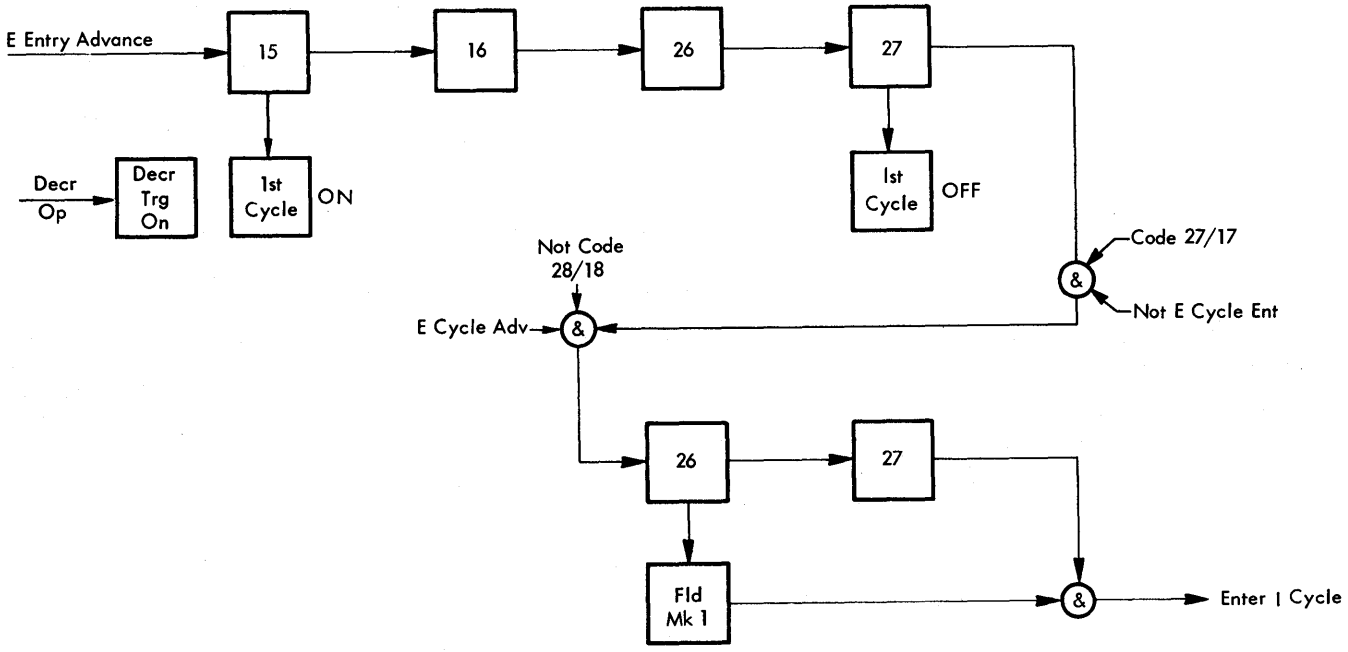



Figure 10-2. Branch and Transmit - Code 27/17

Trigger 26 (01.60.56.1).

1. Read out of memory per OR-1 and store the digit in MDR.
2. Write back OR-1 decremented.

Trigger 27 (01.60.57.1).

1. Block reset of MDR (Read-Y).
2. Read out of memory per OR-2 with either the odd or even sense amplifiers blocked (Read-Y), depending on whether the OR-2 address is odd or even, to clear the memory location.
3. Write back OR-2 decremented.
4. Transfer MDR to MBR.
5. Write into memory per OR-2 from MBR. (Repeat Trigger 26 and Trigger 27, Objectives 1, 2, 3, 4, and 5 for each digit of the field.)
6. End operation when all digits of the field have been transferred and enter I-cycle for the instruction at the P-address of the branch and transmit instruction (now stored in IR-1).

## BRANCH AND TRANSMIT IMMEDIATE (CODE 17—BTM)

The sequence block diagram for this operation is shown in Figure 10-2. The function chart for this operation is shown in the Instructional System Diagrams on page 7.

### Objectives

1. Save the address of the next instruction in sequence for use with the next branch back instruction.
2. Transmit the field whose units position is the $Q_{11}$ digit of the branch and transmit (immediate) instruction to the memory location designated by the P-address minus 1 and successively lower memory locations.
3. Branch to the instruction at the P-address.

### Functions

The branch and transmit immediate operation differs from the Branch and Transmit - Code 27 operation only in the method of setting the OR-1 address during the I-cycle. See Branch and Transmit - Code 27.

### Auxiliary Triggers

See Branch and Transmit - Code 27.

### E-Timer Triggers

See Branch and Transmit - Code 27.

## BRANCH BACK ( CODE 42 - BB)

The sequence block diagram for this operation is shown in Figure 10-3. The function chart for this operation is shown in the Instructional System Diagrams on page 8.

### Objectives

1. Interrogate the status of the Save Control trigger.
2. If the Save Control trigger is ON, proceed to the instruction at the address designated by PR-1. (Address was saved by storing it in PR-1 due to a previous depression of the Save key.)
3. If the Save Control trigger is OFF, proceed to the instruction at the address designated by IR-2. (Address was saved by storing it in IR-2 when the last branch and transmit or branch and transmit immediate instruction was executed.)

### Functions

The address in PR-1 or IR-2, depending upon the status of the Save Control trigger, is transferred to IR-1.

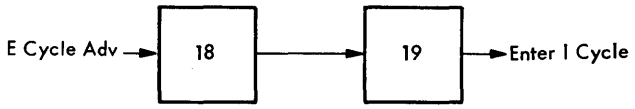



Figure 10-3. Branch Back - Code 42

### Auxiliary Trigger Status

Save Control Trigger (01.06.15.1).

1. Reset OFF by manual reset.

2. Turned on by depressing the Save key on the console.
3. Turned off when status is interrogated by a branch back operation.

E -Timer Trigger Objectives

Trigger 18 (01.60.48.1).

1. Read either PR-1 or IR-2 into MAR depending upon the status of the Save Control trigger.
2. Write from MAR into IR-1 bypassed.

Trigger 19 (01.60.49.1)
(Dummy E-Timer)

1. Block MAR reset to prevent VRC error.
2. End operation and enter I-cycle for the instruction at the saved address (now stored in IR-1).

BRANCH ON DIGIT (CODE 43 - BD)

The sequence block diagram for this operation is shown in Figure 10-4. The function chart for this operation is shown in the Instructional System Diagrams on page 9.

Objectives

1. Interrogate the single digit located at the Q-address (OR-1).
2. If the digit is not a zero, branch to the instruction at the P-address (OR-2).
3. If the digit is a zero, proceed to the next instruction in sequence (address in IR-1).

Functions

The digit at the Q-address per OR-1 is read out of memory to MDR and is interrogated by the Digit/Record Mark/Group Mark trigger. The D/RM/GM trigger will be turned on by a digit other than zero.

If the digit is zero (D/RM/GM trigger OFF), the computer proceeds to the next instruction in sequence.

If the digit is not a zero (D/RM/GM trigger ON), the address in OR-2 is transferred into IR-1 and I-cycle is entered for the instruction at the P-address (now in IR-1).

Auxiliary Trigger Status

D/RM/GM Trigger (01.63.30.1).

1. Turned off by Trigger 1 of the I-cycle and therefore is off when E-cycle is entered.
2. Turned on by a digit other than zero in MDR during Trigger 28 time.

E-Timer Trigger Objectives

Triggers 28 and 29 are always used. Triggers 18 and 19 are also used if the digit is not zero.

Trigger 28 (01.60.58.1).

1. Read out of memory per OR-1 and store the digit in MDR.
2. Turn on the D/ RM/GM trigger if the digit in MDR is not a zero.

Trigger 29 (01.60.59.1).

1. Interrogate status of D/RM/GM trigger. (If ON, proceed to Trigger 18. If OFF, end operation and enter I-cycle for the next instruction in sequence.)

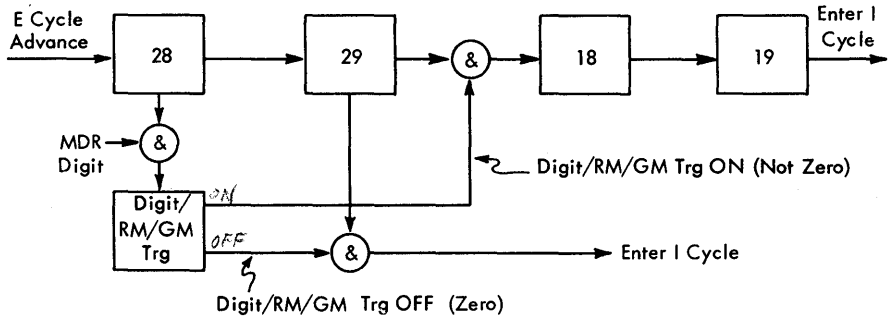



Figure 10-4. Branch On Digit - Code 43

Trigger 18 (01.60.48.1).

1. Read OR-2 into MAR.
2. Write from MAR into IR-1 bypassed.

Trigger 19 (01.60.49.1).
(Dummy E-Timer)

1. Block MAR reset to prevent VRC error.
2. End operation and enter I-cycle for the instruction at the P-address of the branch on digit instruction (now stored in IR-1).

## BRANCH NO FLAG (CODE 44 - BNF)

The sequence block diagram for this operation is shown in Figure 10-5. The function chart for this operation is shown in the Instructional System Diagrams on page 10.

### Objectives

1. Interrogate the single memory position designated by the Q-address (OR-1) for the presence of a flag bit.
2. If a flag bit is not present, branch to the instruction at the P-address (OR-2).
3. If a flag bit is present, proceed to the next instruction in sequence (address in IR-1).

### Functions

The memory location designated by OR-1 is read out to MDR and is interrogated for the presence of a flag bit. The Field Mark No. 1 trigger will be turned on if a flag bit is present.

If a flag bit is present (Field Mark No. 1 ON), the computer proceeds to the next instruction in sequence.

If a flag bit is not present (Field Mark No. 1 OFF), the address in OR-2 is transferred into IR-1 and I-cycle is entered for the instruction at the P-address (now in IR-1).

### Auxiliary Trigger Status

Field Mark No. 1 (01.63.30.1).

1. Turned off by Trigger 1 of the I-cycle and therefore will be OFF when E-cycle is entered.
2. Turned on during Trigger 28 time by the presence of an F-bit in MDR.

### E-Timer Trigger Objectives

Triggers 28 and 29 are always used. Triggers 18 and 19 are also used if a flag bit is not present.

Trigger 28 (01.60.58.1).

1. Read out of memory per OR-1 and store the digit in MDR.
2. Turn on Field Mark No. 1 trigger if an F-bit is present in MDR.

Trigger 29 (01.60.59.1).

1. Interrogate the status of Field Mark No. 1 trigger. (If OFF, proceed to Trigger 18.

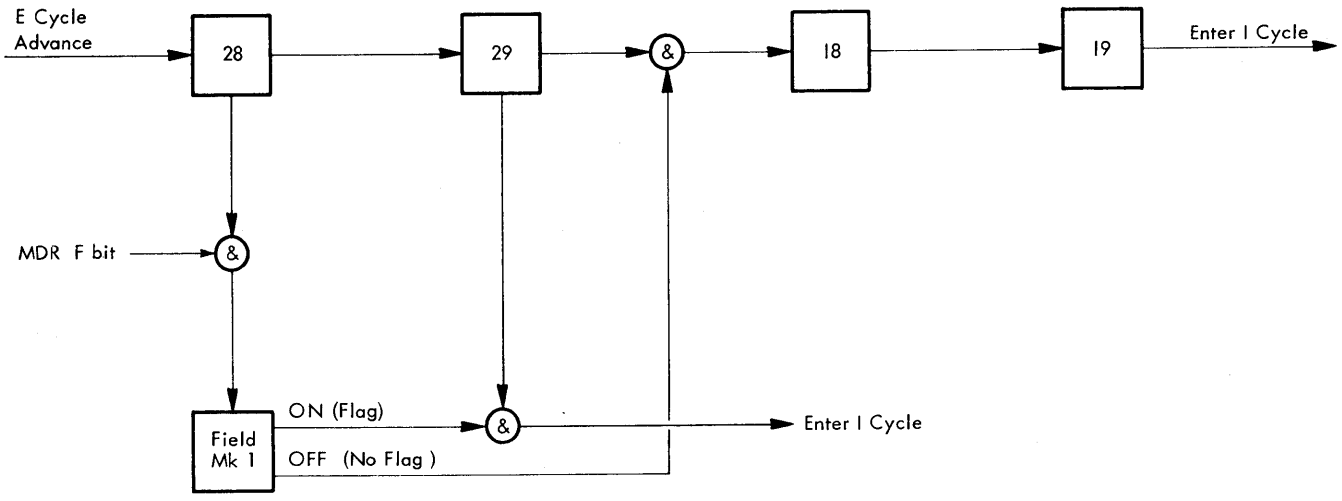



Figure 10-5. Branch No Flag - Code 44

If ON, end operation and enter I-cycle for the next instruction in sequence.)

Trigger 18 (01.60.48.1).

1. Read OR-2 into MAR.
2. Write from MAR into IR-1 bypassed.

Trigger 19 (01.60.49.1).
(Dummy E-Timer)

1. Block MAR reset to prevent VRC error.
2. End operation and enter I-cycle for the instruction at the P-address of the branch no flag instruction (now stored in IR-1).

## BRANCH NO RECORD MARK (CODE 45 - BRN)

The sequence block diagram for this operation is shown in Figure 10-6. The function chart for this operation is shown in the Instructional System Diagrams on page 11.

### Objectives

1. Interrogate the single memory position designated by the Q-address (OR-1) for the presence of a record mark character.
2. If a record mark character is not present, branch to the instruction at the P-address (OR-2).
3. If a record mark character is present, proceed to the next instruction in sequence (address in IR-1).

### Functions

The memory location designated by OR-1 is read out to MDR and is interrogated for the presence of a record mark (C-8-2). The D/RM/GM trigger will be turned on if a record mark is present.

If a record mark is present (D/RM/GM trigger ON), the computer proceeds to the next instruction in sequence.

If a record mark is not present (D/RM/GM trigger OFF), the address in OR-2 is transferred into IR-1 and I-cycle is entered for the instruction at the P-address (now in IR-1).

### Auxiliary Trigger Status

D/RM/GM Trigger (01.63.50.1).

1. Turned off by Trigger 1 of the I-cycle and therefore will be OFF when E-cycle is entered.
2. Turned on during Trigger 28 time by the presence of a record mark (C-8-2) in MDR.

### E-Timer Trigger Objectives

Triggers 28 and 29 are always used. Triggers 18 and 19 are also used if a record mark is not present.

Trigger 28 (01.60.58.1).

1. Read out of memory per OR-1 and store the digit in MDR.
2. Turn on the D/RM/GM trigger if a record mark is present in MDR.

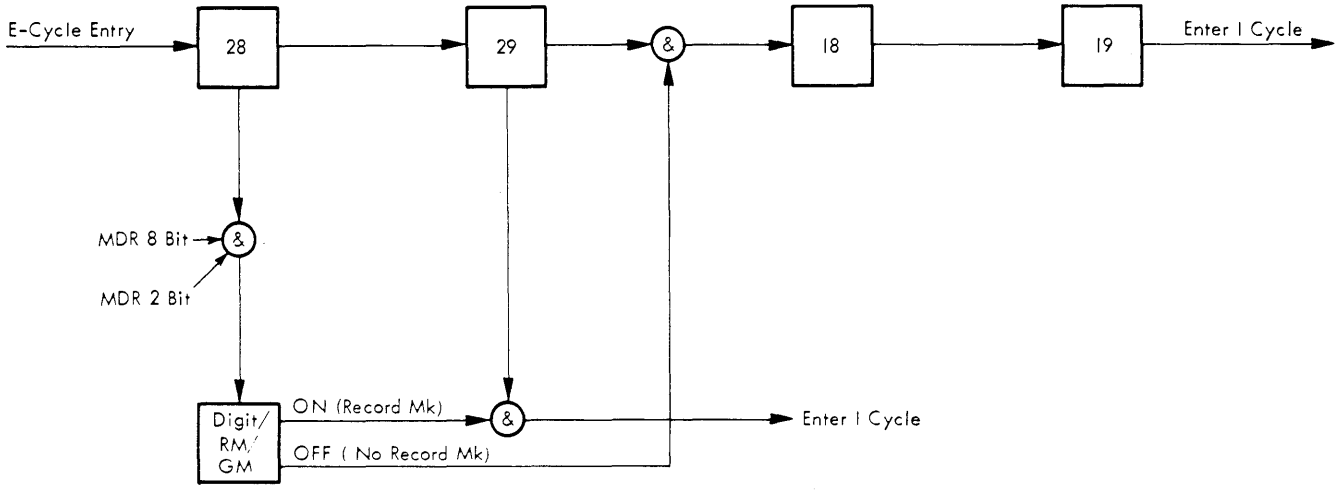



Figure 10-6. Branch No Record Mark - Code 45

Trigger 29 (01.60.59.1).

1. Interrogate the status of the D/RM/GM trigger. (If OFF, proceed to Trigger 18. If ON, end operation and enter I-cycle for the next instruction in sequence.)

Trigger 18 (01.60.48.1).

1. Read OR-2 into MAR.
2. Write from MAR into IR-1 bypassed.

Trigger 19 (01.60.49.1).
(Dummy E-Timer)

1. Block MAR reset to prevent VRC error.
2. End operation and enter I-cycle for the instruction at the P-address of the branch no record mark instruction (now stored in IR-1).

## BRANCH INDICATOR (CODE 46 - BI)

The sequence block diagram for this operation is shown in Figure 10-8. Function charts for this operation are shown in Figures 10-9, 10-10, 10-11 and on page 12 in the Instructional System Diagrams.

### Objectives

1. Interrogate the status of the indicator or program switch designated by the $Q_8$ and $Q_9$ digits of the instruction.
2. If the indicator or program switch is ON, branch to the instruction at the P-address (OR-2).
3. If the indicator or program switch is OFF, proceed to the next instruction in sequence (address in IR-1).

### Functions

During Trigger 6 time of the I-cycle, the $Q_8$ and $Q_9$ digits of the instruction are placed in the D/B register where they are decoded to determine which indicator or program switch is to be interrogated. Examination of the status of the particular indicator or program switch is conducted during Trigger 7 time to determine whether the indicator or program switch is ON or OFF. The Branch Test trigger will be turned on if the indicator or program switch is ON.

If the Branch Test trigger is ON, the P-address in OR-2 is transferred into IR 1 and I-cycle is entered for the instruction at the P-address (now in IR-1).

If the Branch Test trigger is OFF, the computer proceeds to the next instruction in sequence.

The codes which appear in the $Q_8$ and $Q_9$ digits of this instruction for interrogation of program switches and indicators are assigned as follows:

01 - Program switch 1
02 - Program switch 2
03 - Program switch 3
04 - Program switch 4
*06 - Read check indicator
*07 - Write check indicator
08 - MAR check indicator (for CE use only)
11 - High/Plus (H/P) indicator
12 - Equal/Zero (E/Z) indicator
13 - H/P or E/Z indicator
14 - Overflow indicator
*16 - MBR-even check indicator
*17 - MBR-odd check indicator
19 - ANY data check indicator line

* Will cause 19 to be on.

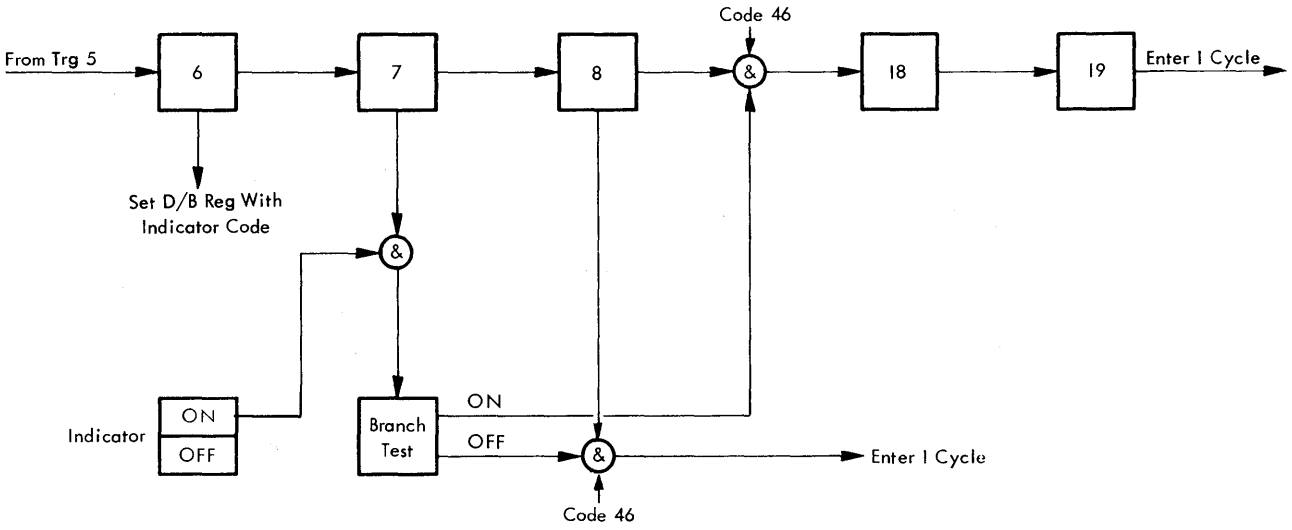



Figure 10-7. Branch Indicator - Code 46

All indicators except the H/P, E/Z, and the ANY line, are turned OFF, if ON, when interrogated by this instruction. Interrogation of a program switch has no effect upon its state, because the program switches are operated manually.

Interrogation of the H/P indicator or the E/Z indicator has no effect upon its state; they are automatically turned on only at the start of arithmetic and compare operations.

Interrogation of ANY data check indicator line has no effect upon its state. The ANY data check indicator line is ON when one or more of the four data check indicators (read, write, MBR-even, and MBR-odd) is ON, and OFF when all four of the data check indicators are OFF.

Auxiliary Trigger Status

Branch Test Trigger (01.25.35.1).

1. Turned off during the I-cycle by Trigger 2.
2. Turned on during Trigger 7 time of the I-cycle if the indicator or program switch that is designated for interrogation is ON.

E-Timer Trigger Objectives

Triggers 18 and 19 are used if a branch occurs. Only I-cycle triggers are used if no branch occurs.

Trigger 18 (01.60.48.1).

1. Read OR-2 into MAR.
2. Write from MAR into IR-1 bypassed.

Trigger 19 (01.60.49.1).
(Dummy E-Timer)

1. Block MAR reset to prevent VRC error.
2. End operation and enter I-cycle for the instruction at the P-address of the branch indicator instruction (now stored in IR-1).

BRANCH NO INDICATOR (CODE 47 - BNI)

The sequence block diagram for this operation is shown in Figure 10-7. Function charts for this operation are shown in Figure 10-9, 10-10, 10-11 and on page 12 in the Instructional System Diagrams.

Objectives

1. Interrogate the status of the indicator or program switch designated by the $Q_8$ and $Q_9$ digits of the instruction.
2. If the indicator or program switch is OFF, branch to the instruction at the P-address (OR-2).
3. If the indicator or program switch is ON, proceed to the next instruction in sequence (address in IR-1).

Functions

During Trigger 6 time of the I-cycle, the $Q_8$ and $Q_9$ digits of the instruction are placed in the D/B register where they are decoded to determine which indicator or program switch is to be interrogated. Examination of the status of the particular indicator or program switch is conducted during Trigger 7 time to determine whether it is OFF or ON. The Branch Test trigger will be turned on if the indicator or program switch is ON.

If the Branch Test trigger is OFF, the address in OR-2 is transferred into IR-1 and I-cycle is entered for the instruction at the P-address (now in IR-1).

If the Branch Test trigger is ON, the computer proceeds to the next instruction in sequence.

The codes which appear in the $Q_8$ and $Q_9$ digits of this instruction for interrogation of program switches and indicators are assigned as follows:

01 - Program switch 1
02 - Program switch 2
03 - Program switch 3
04 - Program switch 4
*06 - Read check indicator
*07 - Write check indicator
08 - MAR check indicator (for CE use only)
11 - H/P indicator
12 - E/Z indicator
13 - H/P and E/Z indicators
14 - Overflow indicator
*16 - MBR-even check indicator
*17 - MBR-odd check indicator
19 - ANY data check indicator line

*Will cause 19 to be on.

All indicators, except the H/P, E/Z, and the ANY line, are turned off, if on, when interrogated by this instruction. Interrogation of a program switch has no effect upon its state, because the program switches are operated manually.

Interrogation of the H/P indicator or the E/Z indicator has no effect upon its state; they are automatically reset OFF only at the start of arithmetic and compare operations.

Interrogation of the ANY data check indicator line has no effect upon its state. The ANY data check

indicator line is ON when one or more of the four data check indicators (read, write, MBR-even, and MBR-odd) is ON, and OFF when all four of the data check indicators are OFF.

Auxiliary Trigger Status

Branch Test Trigger (01.25.35.1).

1. Turned off during the I-cycle by Trigger 2.
2. Turned on during Trigger 7 time of the I-cycle if the indicator or program switch that is designated for interrogation is ON.

E-Timer Trigger Objectives

Triggers 18 and 19 are used if a branch occurs. Only I-cycle triggers are used if no branch occurs.

Trigger 18 (01.60.48.1).

1. Read OR-2 into MAR.
2. Write from MAR into IR-1 bypassed.

Trigger 19 (01.60.49.1).

1. Block MAR reset to prevent VRC error.
2. End operation and enter I-cycle for the instruction at the P-address of the branch no indicator instruction (now stored in IR-1).

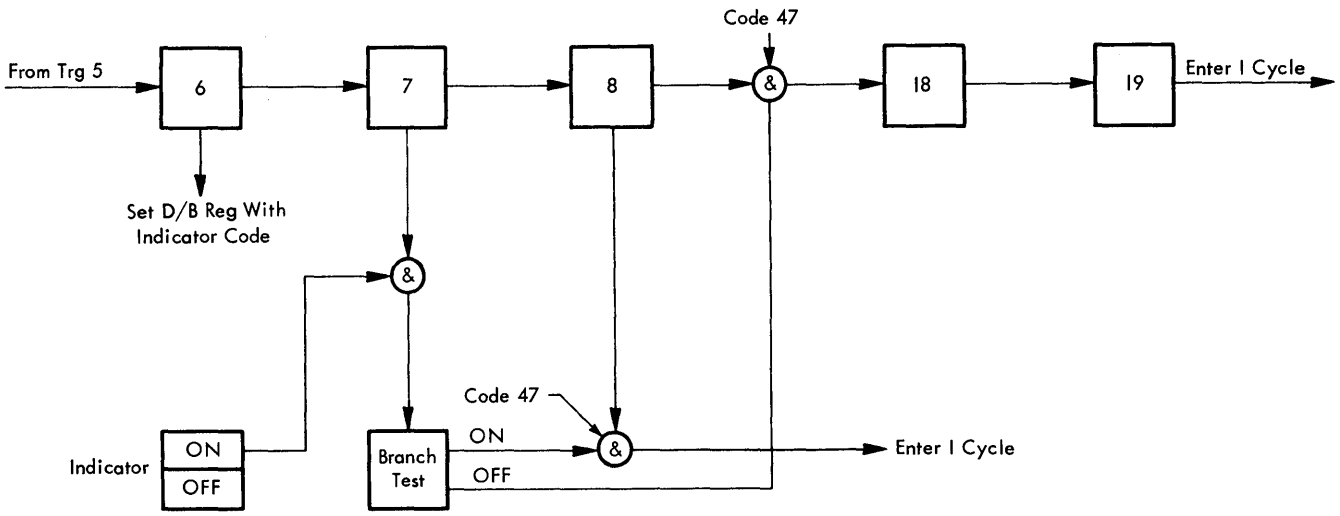
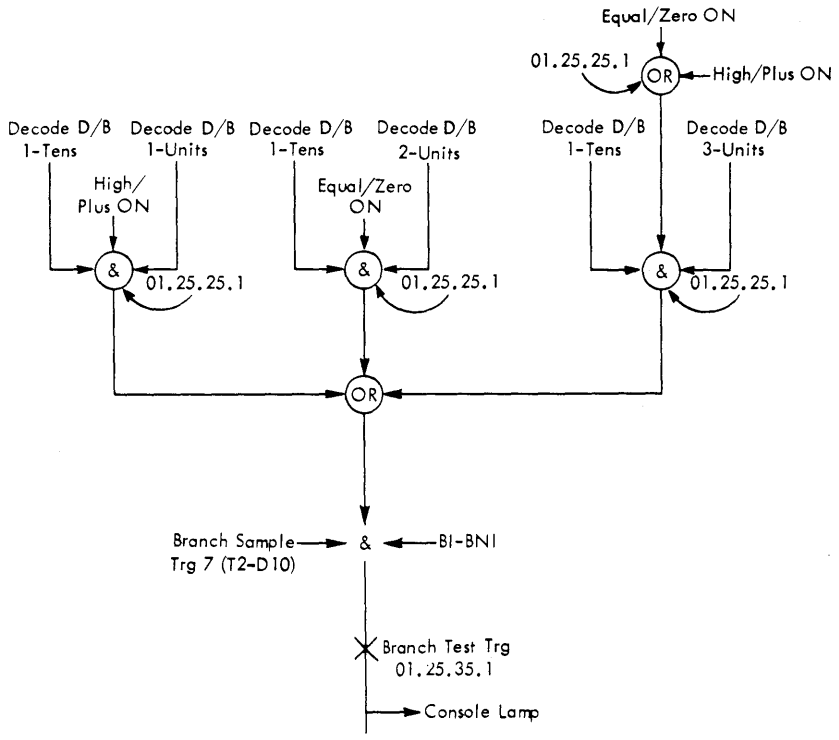
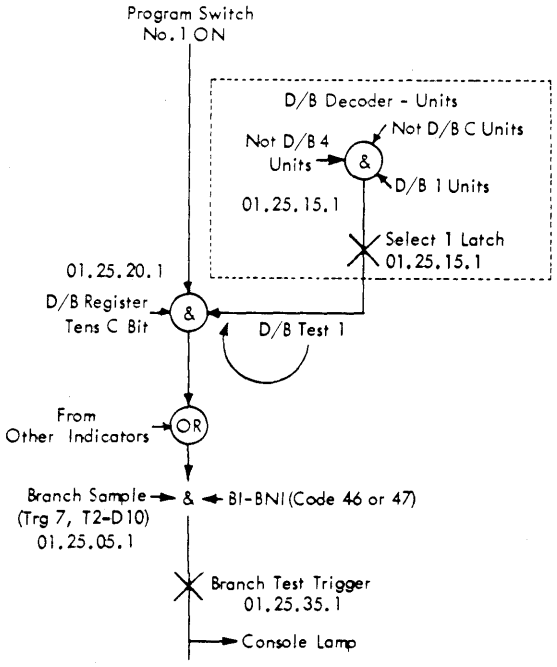



Figure 10-8. Branch No Indicator - Code 47.




Code 46: Branch Can Occur if Either High/Plus OR Equal/Zero Trigger is ON.
Code 47: Branch Can Occur Only if Both High/Plus AND Equal/Zero Triggers are OFF.

Figure 10-9. Branch Indicator - Branch No Indicator - Indicator Codes 11, 12, and 13




NOTE: For Program Switches 2, 3, & 4 the D/B Decoder Units Will Decode a 2, 3, or 4. Remainder of Function is Identical.

Figure 10-10. Branch Indicator - Branch No Indicator - Program Switch Indicator Code 01

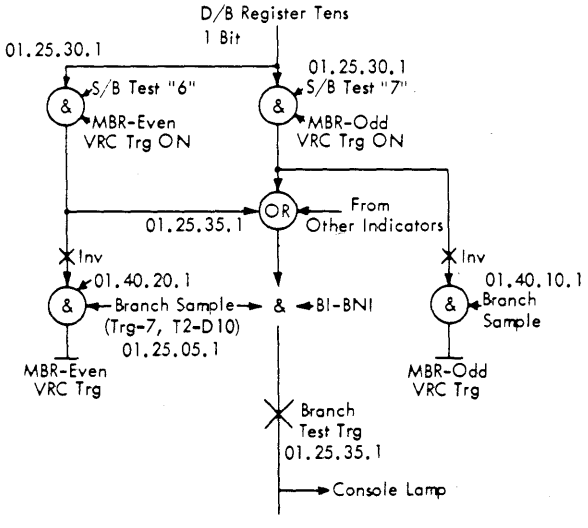



Figure 10-11. Branch Indicator - Branch Indicator - MBR VRC Triggers, Indicator Codes 16 and 17

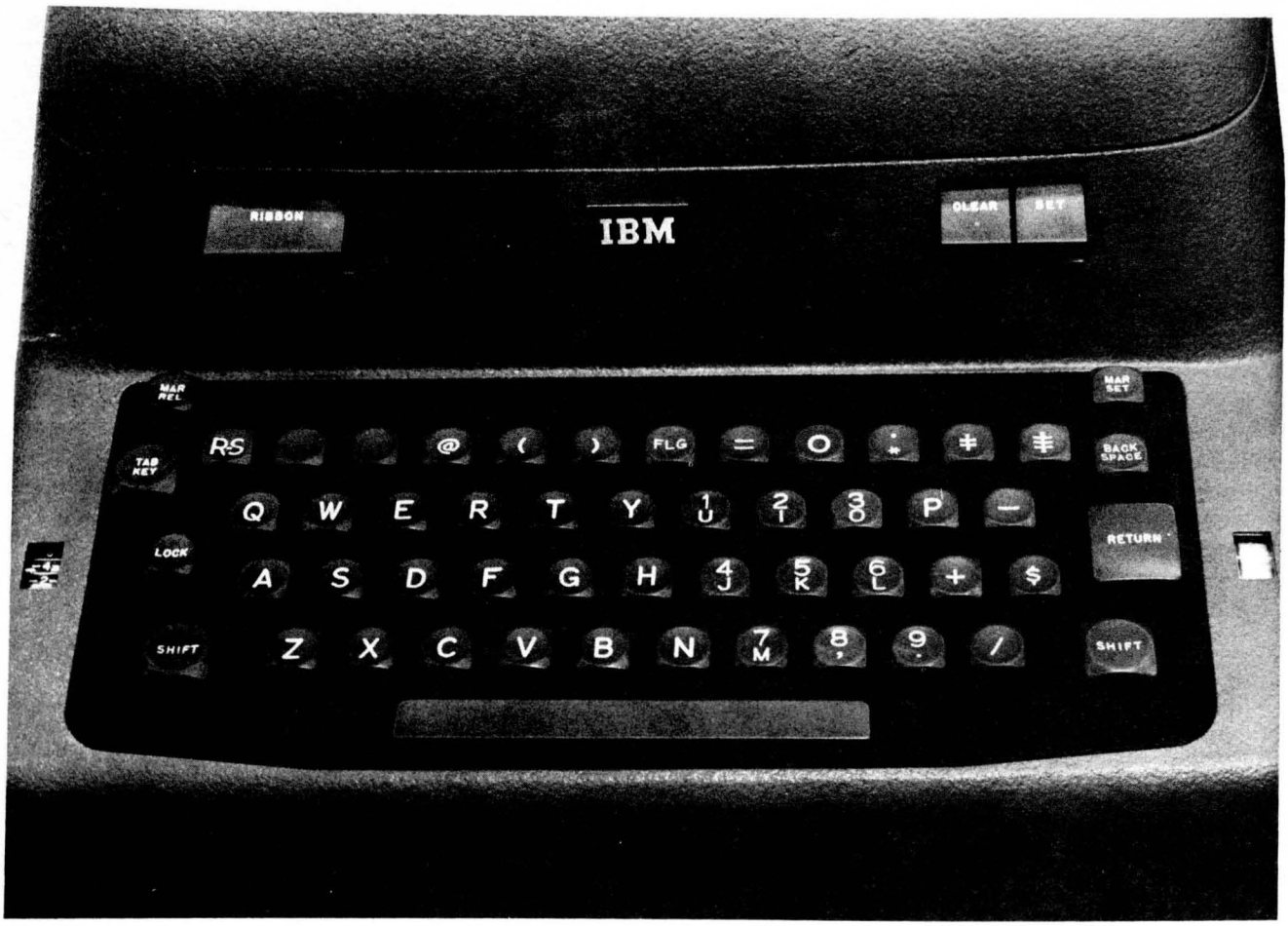



Figure 11-2. Typewriter Keyboard

The console typewriter can be used to enter (read) instructions and data into memory or to print out (write) data from memory. A record of input data is obtained as a byproduct of an input operation. The rate of entry of information from the typewriter keyboard depends upon the speed of the operator; the rate of automatic print out of data is 10 characters per second. The typewriter cannot be used off-line because the keyboard is locked when not in use to enter data into memory.

Pressing Insert on the console activates the typewriter keyboard to permit the direct entry of instructions into memory, starting at location 00000. Each depression of a typewriter key enters that character into memory one location higher than the previous character. The keyboard remains activated until the Release key on the console or the R-S key on the typewriter is pressed.

Flags for sign and field definition in numerical data are indicated on the typewriter by pressing the flag key, before pressing the digit key to which the flag refers.

During an input operation, characters are presented to computer input translator circuitry from the keyboard for conversion to the 6-bit digit code (see Appendix B). If a character with incorrect parity is presented to the translator, the read check indicator is turned on; however, the computer remains in the automatic mode and continues to accept data from the keyboard until Release or the R-S key is pressed. The computer then enters the manual mode. The read check indicator can be interrogated by a branch indicator or branch no indicator instruction and will be turned off, if on, by the execution of that instruction.

During an output operation, characters from memory in the 6-digit code are presented to computer output translator circuitry for conversion to typewriter code. (See Appendix B.) If an invalid character is presented to the typewriter from the

translator, an invalid character symbol ⊁ is printed. If a character with incorrect parity is presented to the typewriter, the write check indicator is turned on and the character is centerscored. The write check indicator is turned on if a typebar fails to mechanically respond to a character in the typewriter encoding (bit) relays. The setting of the I/O check switch on the console to Stop or Program determines whether the computer stops upon completion of writing the record in which the parity error was detected or continues with the program. The write check indicator can be interrogated by a branch indicator or branch no indicator instruction and is turned off, if on, by the execution of that instruction.

Space, carriage return, and tabulate are typewriter functions that may be inserted in a program by means of Control-Code 34 instructions.

## READ NUMERICALLY (CODE 36 - RN)

A sequence block diagram for this operation is shown in Figure 11-3. Function charts for this operation and for the input translator are shown on pages 13, 14, and 15 in the Instructional System Diagrams. A timing chart of the typewriter used as the input device (numerical) is shown in Figure 11-4.

### Objectives

1. Read numerical information, including flag bits, into memory from the input device specified by the $Q_8$ and $Q_9$ digits of the instruction.
2. Store the information at the memory location designated by the P-address (OR-2) and successively higher memory locations.

### Functions

During the I-cycle, the $Q_8$ and $Q_9$ digits of the instruction are placed in the D/B register and decoded to specify the input device. The typewriter keyboard is specified by 01.

The digits of input data are transmitted serially to memory at the location designated by the P-address (OR-2) and successively higher memory locations. Flag bits with digits of input data are duplicated in memory with the digits.

Transmission of a numerical character of input data from the typewriter keyboard requires energization of the coding relay (or relays) corresponding to the typewriter character code for the specific digit. Coding relays are assigned as follows:

| Bit | Coding Relay |
|---|---|
| 0 | R56 |
| 1 | R57 |
| 2 | R58 |
| 4 | R59 |
| 8 | R60 |

Pressing the typewriter keyboard flag key turns on the Flag trigger, which privides for storage of an F-bit with the digit that follows. C-bits are developed as needed for odd parity.

The Read Check trigger is turned on if:

1. A character with even parity is presented to the input translator.
2. The Response Check latch is on because the input device failed to return a response signal to the computer.

However, the computer remains in the automatic mode and continues to accept input data until the read operation is terminated. Termination of the read operation directs the computer to enter the I-cycle for the next instruction in sequence.

When the input device is the typewriter keyboard, the read operation is terminated by one of the following:

1. Pressing Release on the console. The computer stops when the I-cycle is entered. Pressing Start on the console is then required to restart the computer
2. Pressing the R-S key on the typewriter keyboard.
   This performs the same function as Release followed by Start.
3. The address in MAR reaching 00099.
   This performs the same function as Release. A record mark is not automatically placed in memory if any of the three preceding items terminate the read operation. If a record mark is wanted, the Record Mark key must be pressed before Release or the R-S key is used to terminate the read opera tion. In the case of MAR reaching 00099, a record mark cannot be placed in memory because the typewriter keyboard is inactivated.

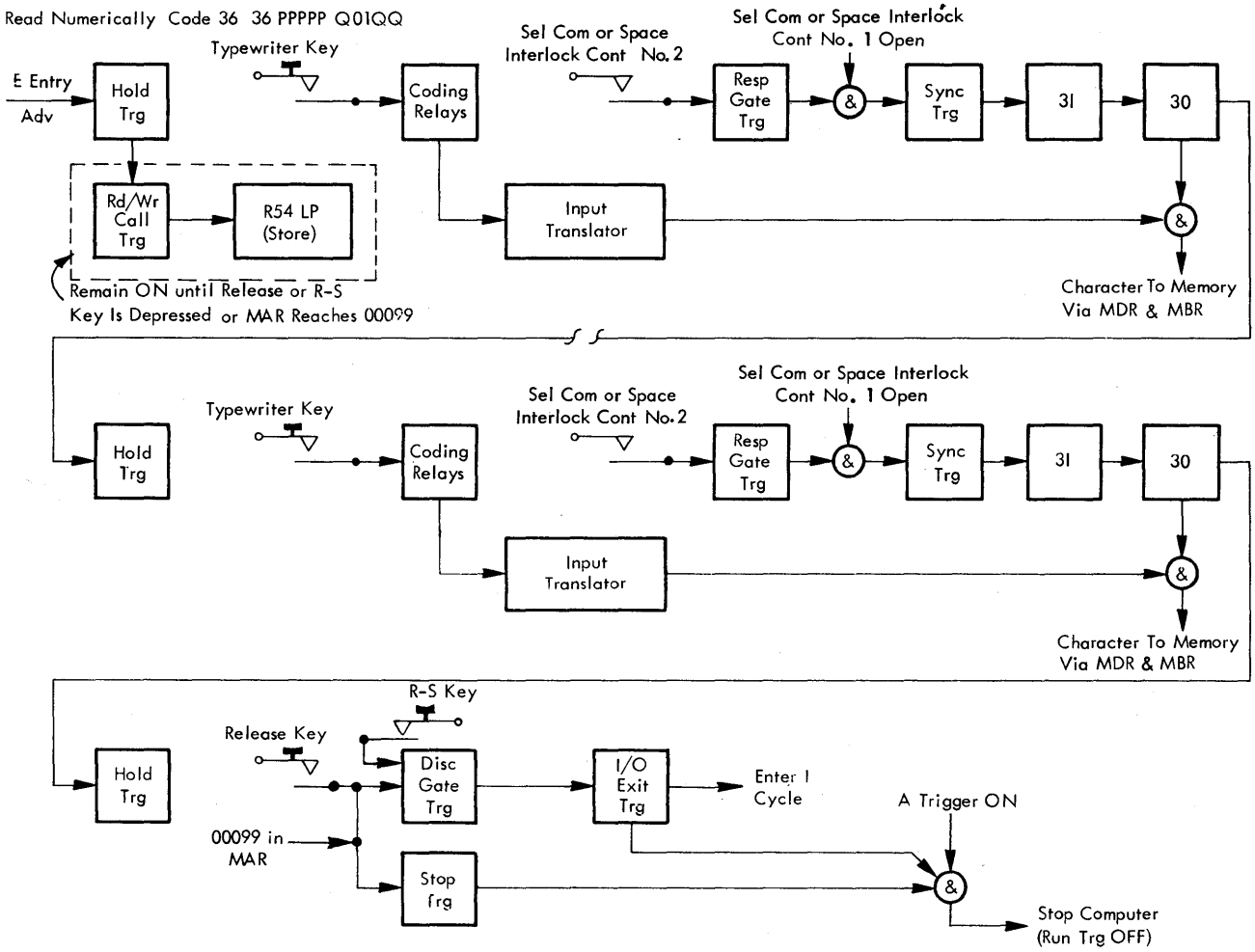



Figure 11-3. Read Numerically - Code 36 (36 PPPPP Q01QQ)

NOTE: Pressing the R-S key blocks the Response Gate trigger to prevent the computer from cycling. The Flag trigger is turned on when the R-S key is depressed; however, it has no function and is turned off by the I/O Exit trigger.

## Auxiliary Trigger Status

Decrement Trigger (01.60.05.1).

1. Turned off (increment) when I-cycle is entered.
2. Remains OFF throughout E-cycle.

Read-Write Call Trigger (01.64.14.1).

1. OFF when E-cycle is entered.
2. Turned on by the Hold trigger and remains ON until the read operation is terminated.
   a. Unlocks typewriter keyboard
   b. Picks R54, the store relay.
3. Turned off by I/O Exit trigger.

Response Gate Trigger (01.80.25.1).

1. OFF when E-cycle is entered.
2. Turned on by a signal from the input device that a character is available to the computer.
3. Turned off by a Clock pulse (T3-D10) or the I/O Exit trigger.

Sync Trigger (01.64.13.1).

1. OFF when E-cycle is entered.
2. Turned on during Hold trigger time, when the input device response signal terminates to signal the computer to proceed with storing the character in memory.
3. Turned off during Trigger 30 time or by the I/O Exit trigger.

Disconnect Gate Trigger (01.80.25.1).

1. OFF when E-cycle is entered.
2. Turned on by Release key or R-S depression, MAR reaching 00099, or a tape level -8

(end-of-line) indication to signal termination of read operation.
3. Turned off by I/O Exit trigger.

I/O Exit Trigger (01.64.13.1).
1. OFF when E-cycle is entered.
2. Turned on when termination of read operation has been signalled by Release key or R-S key depression or MAR reaching 00099.
3. Turned off during Trigger 1 time of following I-cycle.

Stop 1 Trigger (01.06.11.1).
1. OFF when E-cycle is entered.
2. Turned on by pressing the Release key or MAR reaching 00099.

Response Check Latch (01.82.30.1).
1. Turned on during Trigger 31 time.
2. Turned off on the next input cycle after having been turned on by a response signal from the input device. The response signal indicates that a character is available to the computer.
3. Turned off by the I/O Exit trigger ANDed with Read Call gate. When selector common contact No. 2 or space interlock contact No. 2 makes, it turns off the Response Check latch and turns on the Response Gate trigger. When selector common contact No. 1 or space interlock contact No. 1 breaks, the Sync trigger is turned on and, in parallel, a test is made of the status of the Response Check latch. If the latch is on, the Read-Check trigger is turned on.

NOTE: The Response Check latch and its circuits are primarily designed for checking a write operation with the typewriter designated as the output device. It is included here because it is turned on and off each cycle and will detect extra com puter cycles during the read operation. Extra computer cycles could be caused by an extraneous noise spike turning on the Response Gate trigger, the Sync trigger, Trigger 31, Trigger 30, and Hold trigger. In this case the Response Check latch is on from the previous cycle and causes the Read-Check trigger to be turned on in parallel with the Sync trigger, thereby indicating a read error.

Read Check Trigger (01.81.45.1).
1. Turned on during Hold trigger time in parallel with the Sync trigger if the Response Check latch is on.
2. Turned on during Trigger 30 time if a character with incorrect parity is presented to the input translator.
3. Turned off when interrogated by a branch indicator or branch no indicator instruction or when manually reset.

NOTE: The test for parity on the input translator is made by a combination of exclusive OR circuits (01.81.20.1). This read code check circuit tests for an odd number of bits being presented to the input translator. If an even number of bits (incorrect parity) is present, the Read-Check trigger is turned on. The read code check circuit does not check the validity of an input character.

Flag Trigger (01.81.10.1).
1. OFF when E-cycle is entered.
2. Turned on by pressing the Flag key (or R-S key) on the typewriter.
3. Turned off during Trigger 30 time.

E-Timer Trigger Objectives

Hold Trigger (01.64.12.1).
1. Turn on Read-Write Call trigger.
2. Block MAR reset to prevent VRC error.
3. Stop the computer clock to prevent unnecessary cycling of memory.

Trigger 31. (01.64.11.1).
1. Read out of memory per OR-2.
2. Write back OR-2 bypassed.
3. Turn on the Response Check latch. (Trigger 31 is used as a dummy E-timer trigger in Code 36 - Read Numerically operation. See Code 37 - Read Alphamerically for Trigger 31 function.)

Trigger 30 (01.64.10.1).
1. Read out of memory per OR-2 with either the odd or even sense amplifiers blocked, (Read-Y), depending on whether the OR-2 address is odd or even, to clear the memory location.
2. Write back OR-2 incremented +1.
3. Set input character into MDR.
4. Transfer MDR to MBR (Read-Y).
5. Write into memory per OR-2 from MBR.
6. Turn on Hold trigger.

Relay Functions

Objective: Shift the typewriter into the numerical shift (basket up) position and unlock the keyboard.

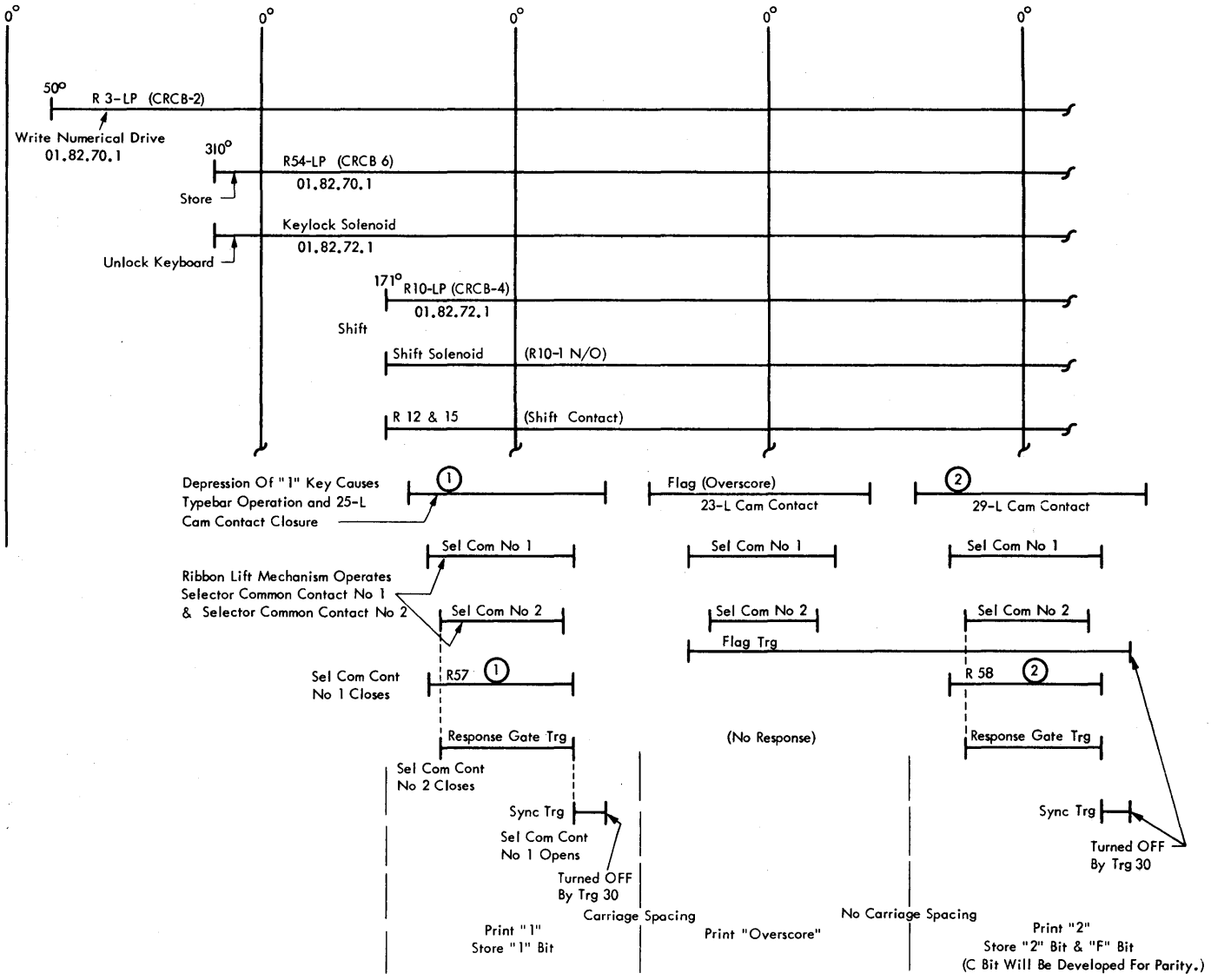



Figure 11-4. Typewriter Used as Input Device (Numerically)

Relay 3LP, Write Numerical (01.82.70.1). This relay is picked at CRCB-2 time when WR NUM DR (01.82.62.1) is enabled by SEL 1 I/O ANDed with OP 36 RN. SEL 1 I/O is enabled by (1) E-Cycle Gate which comes up at the beginning of Trigger 8 time or (2) operating the Insert key.

1. The R3-1 points are not used.
2. The R3-2 points (01.82.72.1) perform no function during read (store) operations.
3. The R3-3 n/o points (01.81.50.1) enable WR NUM INTLK which, when the Op register is reset at the start of the next I-cycle, enables NOT WR NUM DR to latch trip R3 LT (01.82.70.1).
4. The R3-4 n/o points provide a circuit to latch pick R10 LP and pick R11 (01.82.72.1) at CRCB-4 time after R54 is latch picked. The R3-4 n/c points provide a circuit to latch trip R10 (and pick R11) if R3 is latch tripped (NOT WR NUM DR enabled) before R54 is latch tripped (NOT STORE DR enabled).

Relay 54 LP, Store (01.82.70.1). Relay 54 is picked at CRCB-6 time when STORE DR is enabled. STORE DR is enabled when the Read-Write Call trigger is turned on by a Read Numerically - Code 36 operation or by operation of the Insert key.

1. The R54-1 n/o points (01.81.60.1) provide 48v to:
   a. Selector common contact No. 1 and space interlock contact No. 1 which in turn provide 48v to pick encoding relays and to cause -S TPWR RESP to go to +S to inhibit turning on the Sync trigger (01.64.13.1) until the contacts open.
   b. Energize the keylock solenoid (01.82.72.1) thus unlocking the keyboard.
   c. Enable +S STORE INTLK which, when the read operation is terminated, enables NOT STORE DR to latch trip R54 LT (01.82.70.1).
2. The R54-2 n/o points (01.82.72.1) provide a path (through R3-4 and R16-2) to latch pick R10 LP and pick R11 (01.82.72.1). When the read operation is terminated, the R54-2 n/c points provide a circuit to latch trip R10 and enable +S CRCB-4 DISCONN which turns on the I/O Exit trigger.
3. The R54-3 n/c points (01.82.72.1) prevent a back circuit during read numerical (store) operations.
4. The R54-4 n/o points (01.81.50.1) place +S TPWR RESP under control of space interlock contact No. 2 and selector common contact No. 2. +S TPWR RESP ANDed with not FLAG R-S (01.81.10.1) turns on the Response Gate trigger (01.80.25.1).

Relay 10 LP, Shift (01.82.72.1). This relay is picked at CRCB-4 time via R3-4 n/o and R54-2 n/o.

1. The R10-1 n/o points (01.82.70.1) energize the shift solenoid causing the basket to shift to the numerical (up) position.
2. The n/o shift contact (01.82.72.1) closes picking R12 (P and H in series) and R15 (P and H in series).

The typewriter remains in numerical shift until R10 is latch tripped at CRCB-4 time via R54-2 n/c after R54 is latch tripped.

Relay 11, Shift Delay (01.82.72.1). This relay is picked in parallel with R10 LP at CRCB-4 time but performs no function for a read (store) operation. R11 hold is not energized because R1-3 n/o points (WR STATUS) are not closed. R11 drops when R16 is picked.

Relay 12 (01.82.72.1). Relay 12 is picked (P and H in series) by a shift contact closing when the shift solenoid is energized. It remains up until the shift contact opens when the shift solenoid is de-energized. The R12-1 through R12-12 points are in the encoding relay network and their open or closed status determines whether a numerical, special or alphabetic, character is encoded and placed on the input translator when a typewriter key is pressed. Numerical characters are encoded when R12 (and R15) is picked and alphabetic or special characters are encoded when R12 (or R15) is not picked.

Relay 15, Manual Shift (01.82.72.1). This relay is picked (P and H in series) and held in parallel with R12.

1. The R15 1 n/o points (01.82.72.1) provide a path to pick the manual shift delay relay, R16, at CRCB-2 time.
2. The R15 2 n/c points (01.82.70.1) open the pick circuit to the write status relay R1 to prevent R1 LP (01.82.70.1) from being latch picked by the system (after a Release-Start) until the basket has returned to its normal status, that is, shifted to the alphabetic (down) position.
3. The R15-3 and R15-4 points are in the encoding relay network and perform the same type of functions as the R12 points.

Relay 16, Manual Shift Delay (01.82.72.1). Relay 16 is picked by Relay 15 at CRCB-2 time via the R15-1 n/o points.

1. The R16 1 n/o points (01.82.72.1) hold R16 during CRCB-3 time.
2. The R16-2 n/o points (01.82.72.1) perform no function during read (store) operations.
3. The R16-3 n/o points (01.82.72.1) provide a path (during CRCB-2 and -3 time) to latch trip R10 at CRCB-4 time when the store relay R54 is latch tripped.

Numerical Key Operation

Objective: Print a numerical character and store the character in memory.

When a numerical key button is pressed, (for example the 3) the associated cam lever, in operating, causes: (1) the 3 typebar to be driven toward the platen, (2) the associated cam contacts (33U and 33L) to close, and (3) the ribbon lift bail to be operated.

The ribbon lift bail first closes selector common contact No. 1 (01.81.60.1) which, through cam contact 33L on 01.81.62.1 (33U is not used for numerical operations) picks coding relays 57 (1) and 58 (2).

The R57-1 n/c points (01.80.50.1), in operating, enable -S KBRD 1 BIT. The R58-1 n/c points (01.81.55.1) in opening, enable -S KBRD 2-BIT. The +S KBRD C-BIT is enabled by R57-3 n/o and R58-2 n/o points (01.81.55.1). Enabling KBRD 1, 2, and C-bits, place these bits on the input translator.

NOTE: If the Flag key (overscore) had been previously operated, the Flag trigger would be on and a flag bit would be available on the input translator.

The ribbon left bail closes selector common contact No. 2 after No. 1 is closed. Selector common contact No. 2 turns on the Response Gate trigger to signal the system that an input character is available on the input translator.

When selector common contact No. 1 opens, the Sync trigger is turned on and the system proceeds with placing the character (including a flag bit if the Flag trigger is ON) into memory.

Flag Key Operation

Objective: Print an overscore (flag) and prevent spacing. A subsequent depression of a Numerical key prints the number under the overscore and stores the number and its associated flag bit in memory.

When the Flag key is pressed, the associated cam lever, in operating, causes: (1) the overscore (flag) typebar to be driven toward the platen, (2) the associated cam contacts (23U and 23L) to close, and (3) the ribbon lift bail to be operated. Note that the flag typebar has cutaway portion which prevents the typebar from contacting the universal bar and therefore no spacing occurs.

Cam contacts 23U (01.81.60.1) and 23L (01.81.64.1) are in parallel to enable +S FLAG/R-S when selector common contact No. 1 closes. The Flag trigger (01.81.10.1) is turned on and the turn-on of the Response Gate trigger is inhibited, thus preventing the computer from cycling and attempting to place only a flag bit in memory.

No other action takes place until the next key (not a flag) is pressed and, at that time, the system functions as explained in Numerical Key Operation.

## READ ALPHAMERICALLY (CODE 37 - RA)

A sequence block diagram for this operation is shown in Figure 11-3. Sequence block diagrams for Read Numerically - Code 36 and Read Alphamerically - Code 37 differ only in that, for Code 37 operations, the input translator supplies a digit (zone) to MBR-even as well as a digit to MDR. The function charts for this operation and for the input translator are shown in the Instructional System Diagrams on pages 13, 14, 15, and 16.

### Objectives

1. With the computer in alphameric mode, read information into memory from the input device specified by the $Q_8$ and $Q_9$ digits of the instruction.
2. Store the information as two adjacent digits at the memory locations designated by the P-address minus 1 and the P-address (OR-2) and successively higher pairs of memory locations.

### Functions

During the I-cycle, the $Q_8$ and $Q_9$ digits of the instruction are placed in the D/B register and decoded to specify the input device. The typewriter keyboard is specified by 01.

Characters of input data are transmitted serially. Each character is stored in memory as two adjacent digits beginning at the memory locations designated by the P-address minus 1 and the P-address (OR-2) and continuing with successively higher pairs of memory locations. The P-address must designate an odd-numbered memory location for storage of the numerical digit of the first character. The zone digit of the first character is placed at the next lower memory address (P minus 1) which is an even address. Increment +2 is used to provide memory addresses for successive characters.

If an even-numbered memory location is erroneously designated by the P-address, input data is not correctly placed in memory and parity errors may occur.

All flag bits existing in memory locations to which input data is being transmitted remain unchanged; flag bits are not allowed on the input data. Data from the input device may consist of a random mixture of numerical, alphabetic, and special characters.

Transmission of a character of input data from the typewriter keyboard requires energization of the coding relay (or relays) corresponding to the typewriter character code for the specific character.

Coding relays are assigned as follows:

| Bit | Coding Relay |
|---|---|
| X | R55 |
| 0 | R56 |
| 1 | R57 |
| 2 | R58 |
| 4 | R59 |
| 8 | R60 |

C-bits are developed as needed for odd parity.

The Read Check trigger is turned on if:

1. A character with incorrect parity is presented to the input translator.
2. The Response Check latch is on because the input device failed to return a response signal to the computer.

However, the computer remains in the automatic mode and continues to accept input data until the read operation is terminated. Termination of the read operation directs the computer to enter the I-cycle for the next instruction in sequence.

If the input device is the typewriter keyboard, the read operation is terminated by one of the following:

1. Pressing Release on the console. The computer stops when the I-cycle is entered. Pressing Start on the console is then required to restart the computer.
2. Pressing the R-S key on the typewriter keyboard. This performs the same function as pressing Release followed by Start.
3. The address in MAR reaching 00099. This performs the same function as pressing Release.

A record mark is not automatically placed in memory if any of the three preceding items terminate the read operation. If a record mark is wanted, the Record Mark key must be pressed before Release or the R-S key is used to terminate the read operation. In the case of MAR reaching 00099, a record mark cannot be placed in memory because the typewriter keyboard is inactivated.

NOTE: Pressing the R-S key blocks the Response Gate trigger to prevent the computer from cycling. The Flag trigger is turned on when the R-S key is depressed; however, it has no function and is turned off by the I/O Exit trigger.

Auxiliary Trigger Status

See Read Numerically - Code 36.

E-Timer Trigger Objectives

Hold Trigger (01.64.12.1).

1. Turn on Read-Write Call trigger.
2. Block MAR reset to prevent VRC error.
3. Stop the clock to prevent unnecessary cycling of memory.

Trigger 31 (01.64.11.1).

1. Read out of memory per OR-2 to set F-bit triggers in MBR and MDR for retention of any F-bits in the memory locations receiving input data.
2. Write back OR-2 bypassed to retain the address for clearing and writing into the memory locations during Trigger 30 time.

Trigger 30 (01.64.10.1).

1. Read out of memory per OR-2 with both the odd and even sense amplifiers blocked to clear the memory locations (Block Memory SA).
2. Write back OR-2 incremented +2.
3. Block reset of F-bit triggers in MBR-even, MBR-odd, and MDR.
4. Set MBR-even and MDR triggers per character from input device.
5. Transfer MDR to MBR-odd.
6. Write into memory per OR-2 from MBR.
7. Turn on Hold trigger.

Relay Functions

Objective: Unlock the keyboard.

Relay 54 LP, Store (01.82.70.1). This relay is picked at CRCB-6 time when STORE DR is enabled. STORE DR is enabled when the Read-Write Call trigger is turned on by the Read Alphamerically - Code 37 operation.

1. The R54-1 n/o points (01.81.60.1) provide 48v to selector common contact No. 1, space interlock contact No. 1, and energizes the keylock solenoid to unlock the keyboard. For a description of the function of selector common and space interlock contacts see Relay Functions for Read Numerically.
2. The R54-2 n/o and n/c (01.82.72.1) provides a path to latch trip R10 (and pick R11) if the typebar basket was left in the numerical (up) position from the last operation. The R54-2 n/c points provide a path to enable +S CRCB-4 DISCONN to turn on the I/O Exit trigger (01.64.13.1).

3. The R54-3 n/c points (01.82.72.1) perform no function during read alphameric (store) operations.
4. The R54-4 n/o points (01.81.50.1) place +S TPWR RESP under control of space interlock contact No. 2 and selector common contact No. 2 to turn on the Response Gate trigger (01.80.25.1).

The typewriter is now ready to present alphabetic information to the input translator. Note that R12 and R15 are not picked.

The operator may manually shift (press Shift keybutton) to the numerical (up) shift position when it is desired to print and store numerical or special characters interspersed with the alphabetic or special characters. Note that the mechanical shift does not change the alphabetic mode of the input translator; the mode being a function of the operation code only. Numerical characters are stored in memory in the two digit mode (zone and numerical) when the operation code is 37 - read alphamerically. Manually shifting the typewriter will close the shift contact and pick R12 abd R15.

Relay 12 (01.82.72.1). This relay is picked (P and H in series) by the shift contact closing when the Shift key is manually operated, and remains up until the Shift key is released. All points of Relay 12 are in the coding relay network and their open or closed status determines whether a numerical, special, or alphabetic character is coded (7 BCD) and placed on the input translator when a typewriter key is depressed. The input translator codes the 7 BCD character into two parts, zone and numerical, for storing into memory.

Relay 15, Manual Shift (01.82.72.1). This relay is picked (P and H in series) and held in parallel with R12.

1. The R15-1 n/o points (01.82.72.1) provide a path to pick the manual shift delay relay, R16, at CRCB-2 time. However, R16 performs no functions for a manually initiated shift.
2. The R15-2 n/c points (01.82.70.1) open the pick circuit to the write status relay, R1 to prevent R1 LP (01.82.70.1) from being latch picked by the system (after a Release-Start) until the basket has returned to the alphabetic (down) position.
3. The R15-3 and R15-4 points are in the coding relay network and perform the same type of function as the R12 points.

## WRITE NUMERICALLY (CODE 38 - WN)

A sequence block diagram for this operation is shown in Figure 11-5. Function charts for this operation and for the output translator are shown in the Instructional System Diagrams, pages 17, 18, and 19. A timing chart of the typewriter used as the output device (numerical) is shown in Figure 11-6.

### Objective

Transmit numerical information, including flag bits, from the memory location designated by the P-address (OR-2) and successively higher memory locations to the output device specified by the $Q_8$ and $Q_9$ digits of the instruction.

### Functions

During the I-cycle, the $Q_8$ and $Q_9$ digits of the instruction are placed in the D/B register and decoded to specify the output device. The typewriter is specified by 01.

The digits of the output data are transmitted serially from the memory location designated by the P-address (OR-2) and successively higher memory locations to the selected output device. Flag bits in memory with digits of output data are recorded with the digits by the output device.

Alphabetic characters, special characters, and numerical characters, which have been stored in memory as two adjacent digits because the computer was in alphameric mode, are recorded by the output device as two numerical digits.

The write operation leaves output data unchanged in memory.

Transmission of a numerical character of output data to the typewriter requires energization of the typewriter bit relay (or relays) corresponding to the typewriter character code for the specific digit. Bit relays are assigned as follows:

| Bit | Relay |
|---|---|
| C | R21 |
| F (X) | R22 and R25 |
| 0 | R28 and R31 |
| 1 | R41 |
| 2 | R42 and R45 |
| 4 | R46 and R49 |
| 8 | R50 |

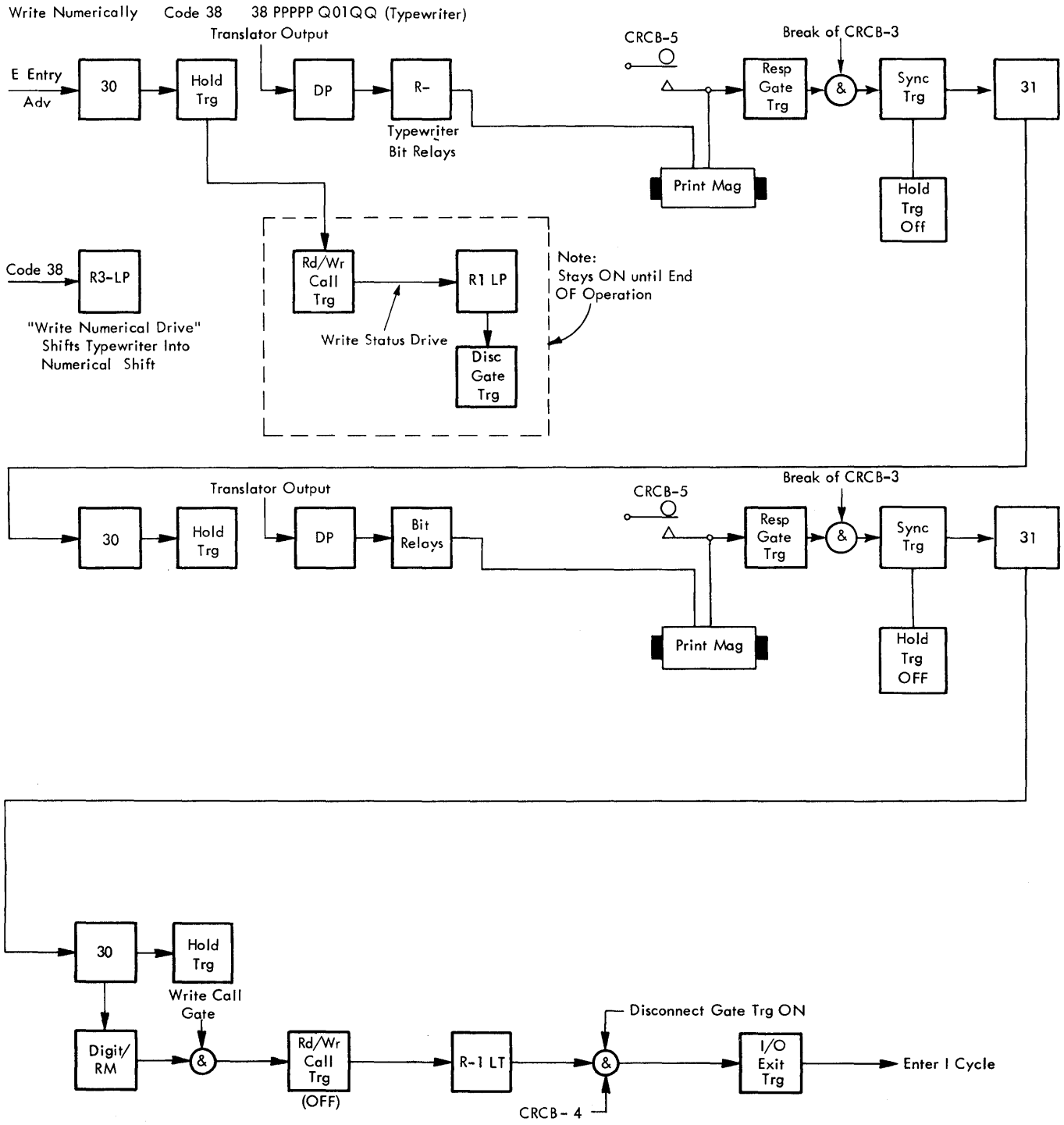



Figure 11-5. Write Numerically - Code 38 (38 PPPPP Q01QQ)

The presence of an F-bit with a digit of output data causes the energization of R22 and R25, which provides for printing an overscore. When a C-bit exists with only an F-bit (FC in MDR), R28 and R31 will be picked along with R22 and R25 and this will cause an overscored zero ($\bar{0}$) to be printed. A C-bit, when accompanied by other bits to comprise a digit, causes energization of R21, which is used only for parity checking purposes.

The Write-Check trigger is turned on when any one or more of the following conditions exist.

1. A character with incorrect parity is presented to the output device by the output translator.
2. Typewriter bit relays are energized for an even number of bits.
3. The Response Check latch is on because the output device failed to return a response signal to the computer.

If the Write-Check trigger is turned on with the typewriter as the output device, the computer remains in the automatic mode and continues to supply data to the typewriter until the write operation is terminated.

With the typewriter as the output device, the write operation is terminated by one of the following:

1. Sensing a record mark from memory. Termination of the write operation directs the computer to enter the I-cycle for the next instruction in sequence. (The record mark is not printed.)
2. Pressing Release on the console. The write operation is terminated immediately, and the computer stops. Pressing Start on the console is required to restart the computer.

Auxiliary Trigger Status

Decrement Trigger (01.60.05.1).

1. Turned off (increment) when I-cycle is entered.
2. Remains OFF throughout E-cycle.

Read-Write Call Trigger (01.64.14.1).

1. OFF when E-cycle is entered.
2. Turned on by the Hold trigger and remains ON until the write operation is terminated.
3. Turned off during Trigger 30 time when MDR contains a record mark.
4. Turned off by the MEM-OF trigger ANDed with the Response Gate trigger if Release is pressed during a write operation and the typewriter is the output device.

Response Gate Trigger (01.80.25.1).

1. OFF when E-cycle is entered.
2. Turned on by a signal from the output device that a character has been received from the computer.
3. Turned off by the Sync trigger.
4. Turned off by the I/O Exit trigger when the write operation is terminated.

Sync Trigger (01.64.13.1).

1. OFF when E-cycle is entered.
2. Turned on during Hold trigger time when CRCB-3 breaks to signal the computer to proceed with presenting the next character to the typewriter.
3. Turned off during Trigger 30 time.
4. Turned off by the I/O Exit trigger when the write operation is terminated.

Digit/Record Mark/Group Mark Trigger (01.63.50.1).

1. OFF when E-cycle is entered.
2. Turned on during Trigger 30 time if MDR contains a record mark (C-8-2).
3. Turned off by Trigger 1 of the I-cycle.

Memory Overflow Trigger (01.64.14.1).

1. OFF when E-cycle is entered.
2. Turned on by pressing the Release key.
3. Turned off by I/O Exit trigger.

Disconnect Gate Trigger (01.80.25.1).

1. OFF when E-cycle is entered.
2. Turned on by R4-1 n/o points closed ANDed with the Sync trigger when it is turned on by a response for the first output character when the output device is the typewriter.
3. Turned off by the I/O Exit trigger.

I/O Exit Trigger (01.64.13.1).

1. OFF when E-cycle is entered.
2. Turned on when the circuit to turn on the Disconnect Gate trigger is terminated and CRCB-4 makes.
3. Turned off during Trigger 1 time of the following I-cycle.

Response Check Latch (01.82.30.1).

1. Turned on during Trigger 31 time.
2. Turned off during Hold trigger time when selector common contact No. 2 or space interlock contact No. 2 makes.

NOTE: The status of the Response Check latch is tested at the same time the Sync trigger is turned on. The on/off status of the Response Check latch at this test time was determined by the previous character. If the previous character failed to turn off the Response Check latch, the Write-Check trigger is turned on. (See Figure 11-11.)

Write-Check Trigger (01.81.45.1).

1. Turned on (in parallel with the Sync trigger) by the Response Gate trigger, if:
   a. The output translator presents a character with incorrect parity to the output device.
   b. The Response Check latch is on.
2. Turned on when CRCB-5 makes, if an even number of typewriter coding relays are picked. (Relay 38 will not pick if an even number of coding relays are picked.)
3. Turned on by Trigger 1 of the I-cycle following a write operation, using the typewriter as the output device, if the response check latch is on. This circuit is functional only if the response failure occurs on the last character prior to sensing the record mark from memory.
4. Turned off when interrogated by a branch indicator or branch no indicator instruction or when manually reset.

NOTE: The write code check circuitry (01.82.30.1) checks for parity only and does not test the validity of an output character.

E-Timer Trigger Objectives

Trigger 30 (01.64.10.1).

1. Read out of memory per OR-2 and store the digit in MDR.
2. Write back OR-2 incremented +1.
3. Turn on Digit/Record Mark/Group Mark trigger when a record mark appears in MDR.

Hold Trigger (01.64.12.1).

1. Block MAR reset to retain output character in MDR.
2. Turn on Read-Write Call trigger.
3. Stop the computer clock to prevent unnecessary cycling of memory.

Trigger 31 (01.64.11.1).

1. Read out of memory per OR-2.
2. Write back OR-2 bypassed.
3. Turn on the Response Check latch. (Trigger 31 is used as a dummy E-timer trigger in Write Numerically - Code 38 operations. See Read Alphamerically - Code 37 for Trigger 31 functions.)

Relay Functions

Objectives:

1. Shift the typewriter into the numerical shift (basket up) position.
2. Prepare the typewriter bit relays to receive characters on the output translator.
3. Prepare the typewriter key magnets to be energized via the coding network set up by the bit relays.

Figure 11-6 is a timing chart of this operation.

Relay 1 LP, Write Status, (01.82.70.1). This relay is picked at CRCB-6 time when WR STATUS DR is enabled by +S WRITE CALL ANDed with +S SEL 1 I/O.

NOTE: Whether R1 or R3 is picked first depends upon the relative CB time when the computer initiates the write operation.

1. The R1-1 n/o points (01.82.72.1) provide a path to: (a) Pick R10, the Shift relay, and (b) pick R38 (Check) or R39 (Error 1) through the parity check network (01.81.55.1).
2. The R1-1 n/c points will, when R1 is latch tripped at the end of the write operation, provide: (a) a path to latch trip R10 and pick R11 to release the type basket so that it shifts down (alpha) and (b) enables +S CRCB-4 DISCONN to turn on the I/O Exit trigger (01.64.13.1).
3. The R1-2 n/o points (01.82.75.1): (a) provide a path to allow the bit relays to be picked at CRCB-3 time according to the character on the output translator, (b) put the -S TPWR RESP line (01.81.60.1) under control of CRCB-3. The -S TPWR RESP line is at +S while CRCB-3 is made ($99^{o}$ to $309^{o}$). When CRCB-3 breaks -S TPWR RESP goes to -S and turns on the Sync trigger. The Sync trigger is inhibited from being turned on (CRCB-3 made) to ensure that the typewriter bit relays and key magnets have time to pick and settle down before the response causes the computer to cycle and present the next output character to the typewriter.

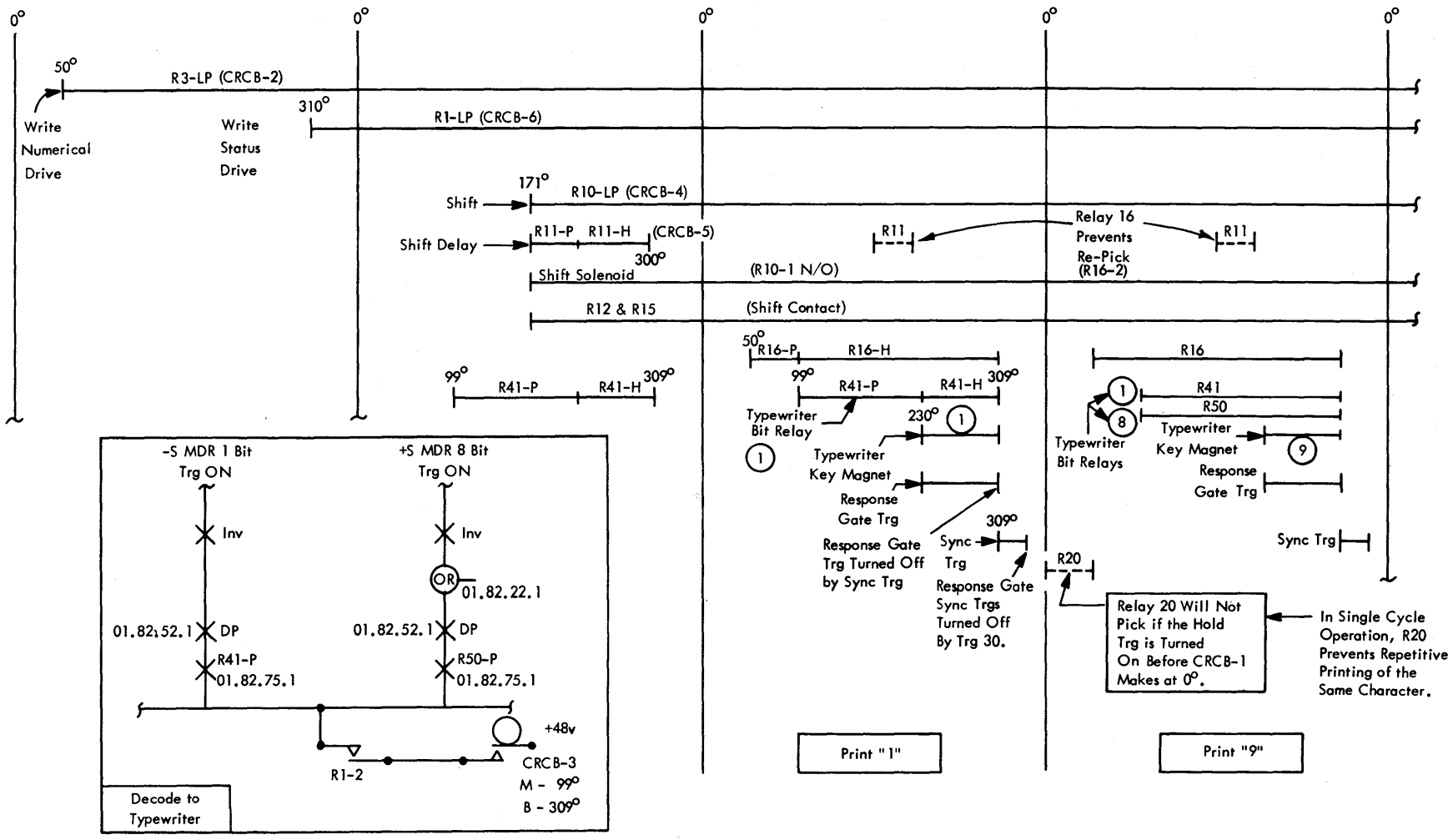



Figure 11-6. Typewriter Used as Output Device (Numerical)

4. The R1-3 n/o points (01.82.80.1) provide a path for energizing key magnets at CRCB-5 time.
5. The R1-4 n/c points (01.81.50.1) cause +S NOT WR STATUS INTLK to go to -S thus inhibiting WR STATUS DR so that R1-4 cannot be latch picked until it has been latch tripped.

Relay 3 LP, Write Numerical (01.82.70.1). This relay is picked at CRCB-2 time when WR NUM DR (01.82.62.1) is enabled by SEL 1 I/O ANDed with OP 38 WN. SEL 1 I/O is enabled by E-cycle gate which comes up at the beginning of Trigger 8 time.

NOTE: Whether R3 or R1 is picked first depends upon the relative CB time when the computer initiates the write operation.

1. The R3-1 points are not used.
2. The R3-2 n/o points (01.82.72.1) provide a path to latch pick R10 (Shift) and pick R11 (Shift Delay).
3. The R3-3 n/o points (01.81.50.1) enable +S WR NUM INTLK which, when the Op register is reset at the start of the next I-cycle, enables NOT WR NUM DR to latch trip R3 LT (01.82.70.1).
4. The R3-4 points (01.82.72.1) perform no function during numerical write operations.

Relay 10 LP, Shift, (01.82.72.1). This relay is picked at CRCB-4 time via R3-2 n/o and R1-1 n/o.

1. The R10-1 n/o points (01.82.70.1) energize the shift solenoid causing the basket to shift to the numerical (up) position.
2. The n/o shift contact (01.82.72.1) closes picking R12 (P and H in series) and R15 (P and H in series).

The typewriter remains in numerical shift until R10 is latch tripped at CRCB-4 time via R1-1 n/c and R54-2 n/c, after R1-1 is latch tripped.

Relay 11, Shift Delay, (01.82.72.1). This relay is picked in parallel with R10 LP at CRCB-4 time.

1. The R11-2 n/o points (01.82.80.1) hold R11 (01.82.72.1) during CRCB-5 time. R11 is picked at 171° and held until 300°
2. The R11-2 n/c points (01.82.80.1) open the 48v circuit to all key magnets thus preventing (delaying) the operation of a key magnet and preventing a response (+S TPWR RESP on 01.81.50.1) from cycling the computer.

Relay 11, Shift Delay, is dropped at 300° by CRCB-4 (R16-2 prevents re-pick of R11) and, when CRCB-5 makes at 220° of the next CB cycle (provided R38 is picked and R20 is not picked), the appropriate key magnet is picked and +S TPWR RESP (01.81.50.1) is enabled to turn on the Response Gate trigger. When CRCB-3 breaks (309°) -S TPWR RESP (01.81.60.1) goes to -S and turns on the Sync trigger which initiates a computer I/O cycle to present the next character to the typewriter.

## DUMP NUMERICALLY (CODE 35 - DN)

A sequence block diagram for this operation is shown in Figure 11-7. Function charts for this operation are shown in the Instructional System Diagrams, pages 17, 18, and 19. A timing chart for the typewriter, used as the output device, is shown in Figure 11-6.

### Objectives

1. Transmit numerical information, including flag bits and record marks, from memory starting at the location designated by the P-address (OR-2) and continuing through location 19999.
2. Record the information on the output device specified by the $Q_8$ and $Q_9$ digits of the instruction.

### Functions

The Dump Numerically - Code 35 operation differs from Write Numerically - Code 38, operation only as follows:

1. Sensing of a record mark from memory does not terminate the dump operation. (Record marks in memory are recorded by the output device as characters of output data.)
2. The dump operation is terminated when the digit in memory location 19999 has been transmitted to the output device.

Termination of the dump operation directs the computer to enter the I-cycle for the next instruction in sequence.

The content of every memory location is recorded by the output device if the P-address of the dump instruction is 00000.

Code 35 Dump Numerically 35 PPPPP Q01QQ

(See Write Numerically - Code 38 Sequence Block Diagram, Figure 11-5, for Sequence Other Than Termination Of Operation.)

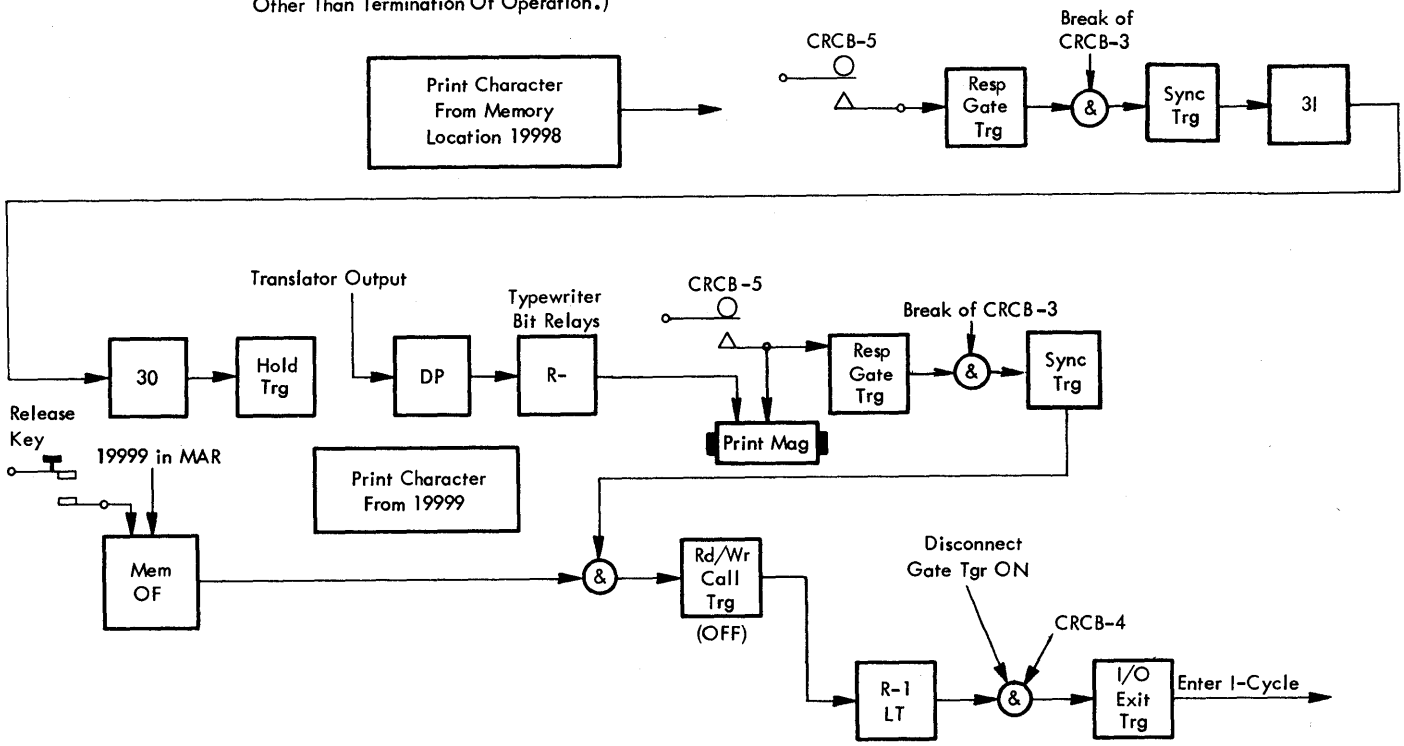



Figure 11-7. Dump Numerically - Code 35 (35 PPPPP Q01QQ)

Auxiliary Trigger Status

Decrement Trigger (01.60.05.1).

1. Turned off (increment) when I-cycle is entered.
2. Remains OFF throughout E-cycle.

Read-Write Call Trigger (01.64.14.1).

1. OFF when E-cycle is entered.
2. Turned on by the Hold trigger and remains ON until the dump operation is terminated.
3. Turned off by the MEM-OF trigger to terminate the dump operation.
4. Turned off by the I/O Exit trigger if Release is pressed during the dump operation.

Response Gate Trigger (01.80.25.1).

1. OFF when E-cycle is entered.
2. Turned on by a signal from the output device that a character has been received from the computer.
3. Turned off by the Sync trigger.
4. Turned off by the I/O Exit trigger when the dump operation is terminated.

Sync Trigger (01.64.13.1).

1. OFF when E-cycle is entered.
2. Turned on during Hold trigger time when CRCB-3 breaks to signal the computer to proceed with presenting the next character to the typewriter.
3. Turned off during Trigger 30 time.
4. Turned off by the I/O Exit trigger when the write operation is terminated.

Memory Overflow (01.64.14.1).

1. OFF when E-cycle is entered.
2. Turned on during memory cycle in which 19999 is placed in MAR.
3. Turned on by pressing the Release key.
4. Turned off by I/O Exit trigger.

Disconnect Gate Trigger (01.80.25.1).

1. OFF when E-cycle is entered.
2. Turned on by Relay 1-4 n/o point closed ANDed with the Sync trigger when it is turned on by a response for the first output character if the output device is the typewriter.
3. Turned off by the I/O Exit trigger.

I/O Exit Trigger (01.64.13.1).

1. OFF when E-cycle is entered.
2. Turned on when the circuit to turn on the Disconnect Gate trigger is terminated and CRCB-4 makes.
3. Turned off during Trigger 1 time of the following I-cycle.

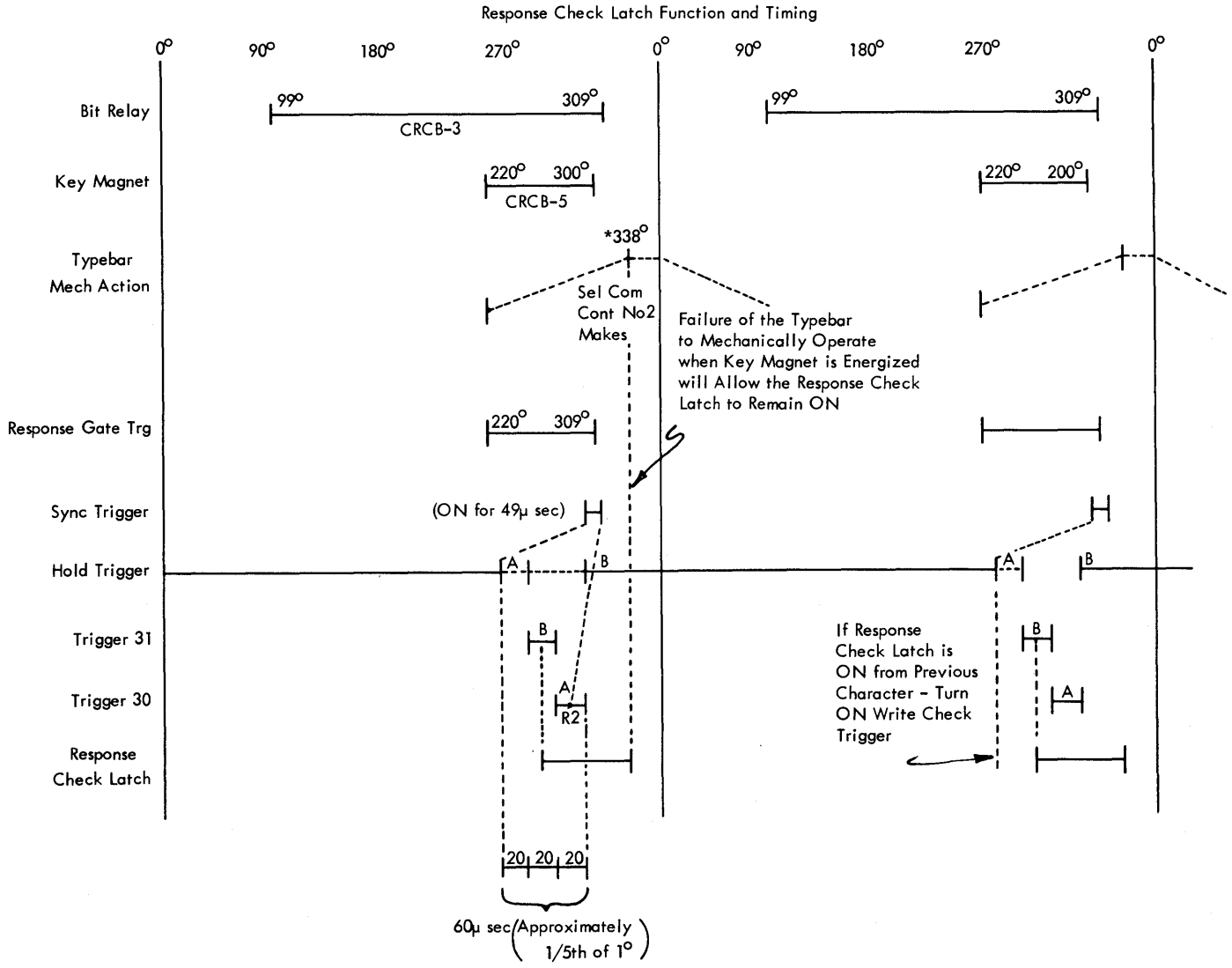
Response Check Latch (01.82.30.1).

1. Turned on during Trigger 31 time.
2. Turned off during Hold trigger time when when selector common contact No. 2 or space interlock contact No. 2 makes.

NOTE: The status of the Response Check latch is tested at the same time the Sync trigger is turned on. The on/off status of the Response Check latch at this test time was determined by the previous character. If the previous character failed to turn off the Response Check latch, the Write-Check trigger is turned on (Figure 11-8).

Write-Check Trigger (01.81.45.1).

1. Turned on (in parallel with the Sync trigger) by the Response Gate trigger, if:
   a. The output translator presents a character with incorrect parity to the output device.




*This is an approximate timing and will vary a few degrees between machines.

Figure 11-8. Response Check Latch Function and Timing

b. The Response Check latch is on

2. Turned on when CRCB-5 makes, if an even number of typewriter coding relays are picked. (Relay 38 will not pick if an even number of coding relays are picked.)
3. Turned on by Trigger 1 of the I-cycle following a write operation, using the typewriter as the output device, if the Response Check latch is on. This circuit is functional only if the response failure occurs on the last character prior to sensing the record mark from memory.
4. Turned off when interrogated by a branch indicator or branch no indicator instruction or when manually reset.

E-Timer Trigger Objectives

Trigger 30 (01.64.10.1).

1. Read out of memory per OR-2 and store the digit in MDR.
2. Write back OR-2 incremented +1.

Hold Trigger (01.64.12.1).

1. Block MAR reset to retain output character in MDR.
2. Turn on Read-Write Call trigger.
3. Stop the computer clock to prevent unnecessary cycling of memory.

Trigger 31 (01.64.11.1).

1. Read out of memory per OR-2.
2. Write back OR-2 bypassed.
3. Turn on the Response Check latch. (Trigger 31 is used as a dummy E-timer trigger in Dump Numerically - Code 35 operations. See Read Alphamerically - Code 37 for Trigger 31 function.)

## WRITE ALPHAMERICALLY (CODE 39 - WA)

A sequence block diagram for this operation is shown in Figure 11-5. Sequence block diagrams for Write Numerically - Code 38 and Write Alphamerically - code 39 differ only in that, for Code 39 operations, the output translator receives a digit (zone) from MBR-even as well as from MDR. Function charts for this operation are shown in the Instructional System Diagrams, pages 17, 18, and 19.

Objectives

1. With the computer in alphameric mode, transmit characters stored as two adjacent digits from the memory locations designated by the P-address minus 1 and the P-address (OR-2) and successively higher pairs of memory locations.
2. Decode each "2-digit" memory character into the proper numerical, alphabetic, or special character.
3. Record the information on the output device specified by the $Q_8$ and $Q_9$ digits of the instruction.

Functions

During the I-cycle, the $Q_8$ and $Q_9$ digits of the instruction are placed in the D/B register and decoded to specify the output device. The typewriter is specified by 01.

Output characters are transmitted serially from memory as two adjacent digits beginning at the memory location designated by the P-address minus 1 and the P-address (OR-2) and continuing with successively higher pairs of memory locations. Each "2-digit" memory character is coded into the proper numerical, alphabetic, or special character by the output translator and presented to the selected output device.

The P-address of the instruction must designate the odd-numbered memory location at which the numerical digit of the first character to be transmitted is stored. The zone digit of the first character is located at the next lower memory address (P minus 1), which is an even address. Increment +2 is used to provide memory addresses for successive characters.

If an even-numbered memory location is erroneously designated by the P-address, data presented to the output device is incorrect and parity errors may occur.

Output data may consist of a random mixture of numerical, alphabetic, and special characters which exist in memory as "2-digit" characters. If an attempt is made to write a record containing single-digit numerical characters by means of this instruction, invalid combinations of disassociated numerical digits are the result and parity errors may occur.

Flag bits existing in memory locations from which an output record is written are not transmitted

to the output device. The write operation leaves output data unchanged in memory.

Transmission of a character of output data to the typewriter requires energization of the typewriter bit relay (or relays) corresponding to the typewriter character code for the specific character. Bit relays are assigned as follows:

| Bit | Relay |
|---|---|
| C | R21 |
| X | R22 and R25 |
| 0 | R28 and R31 |
| 1 | R41 |
| 2 | R42 and R45 |
| 4 | R46 and R49 |
| 8 | R50 |

Relay 21, the C-bit relay, is used for parity checking purposes only. If no bit relay other than R21 is energized on an output character cycle, the typewriter performs a spacing operation.

The Write-Check trigger is turned on when any one or more of the following conditions exist:

1. A character with incorrect parity is presented to the output device by the output translator.
2. Typewriter bit relays are energized for an even number of bits.
3. The Response Check latch is on because the output device failed to return a response signal to the computer.

If the Write-Check trigger is turned on with the typewriter as the output device, the computer remains in the automatic mode and continues to supply data to the typewriter until the write operation is terminated.

With the typewriter as the output device, the write operation is terminated by one of the following:

1. Sensing a record mark at an odd memory address. Termination of the write operation directs the computer to enter the I-cycle for the next instruction in sequence.
2. Pressing the Release key on the console. The write operation is terminated immediately and the computer stops. Pressing Start on the console is then required to restart the computer.

## Auxiliary Trigger Status

See Write Numerically - Code 38.

## E-Timer Trigger Objectives

Trigger 30 (01.64.10.1).

1. Read out of memory per OR-2.
2. Write back OR-2 incremented +2.
3. Turn on D/RM/GM trigger when record mark appears in MDR.

Hold Trigger (01.64.12.1).

1. Block MAR reset to retain the zone digit of the output character in MBR-even and the numerical digit of the output character in MDR.
2. Turn on Read-Write Call trigger.
3. Stop the computer clock to prevent unnecessary cycling of memory.

Trigger 31 (01.64.11.1).

1. Read out of memory per OR-2.
2. Write back OR-2 bypassed.
3. Turn on Response Check latch. (Trigger 31 is used as a dummy E-timer trigger in Write Alphamerically - Code 39 operations. See Read Alphamerically - Code 37 for Trigger 31 function.)

## Relay Functions

Objectives

1. Prepare the typewriter bit relays to receive characters on the output translator.
2. Prepare the typewriter key magnets to be energized via the coding network set up by the bit relays.

Relay 1, Write Status (01.82.70.1). Relay 1 is picked at CRCB-6 time when WR STATUS DR is enabled by +S WRITE CALL ANDed with +S SEL 1 I/O.

1. The R1-1 n/o points (01.82.72.1) provide a path to pick R10, the Shift relay, when the character on the output translator does not have a zone bit, that is, the character is a number (1-9) interspersed in an alphabetic field. In this case the typewriter must shift in order to print the number. This shift is purely a mechanical shift of the typewriter and in no way changes the mode (write alphamerically) of the computer. The mode is a function of the operation code.

When the 1, 2, 4, or 8-bit relays are picked, the R41-1, R42-1, R46-1, and/or R50-1 n/o points (01.82.72.1) provide a path to pick R10 and R11 at CRCB-4 time if R28 and R25, the 0-bit and X-bit relays are not picked. Once R10 is picked and the typewriter is shifted into the numerical (up) position, this position will be maintained until a character containing a zone bit is presented to the bit relays, or Relay 1 is latch tripped at the end of the write alphamerically operation.

The shift operation, shift delay, and remaining relay point functions are essentially the same as given for Write Numerically.

## Parity Checking Write Operations

### Write Operation with No Error

A check is made (01.81.55.1) of the typewriter bit relays at CRCB-4 time ($171^{o}$) via the R1-1 n/o points (01.82.72.1) and before CRCB-5 makes ($200^{o}$) to pick a key magnet. If no error exists (odd number of bit relays picked), R38 (Check - 01.81.55.1) is picked. Figures 11-9 and 11-10 are timing charts of this operation.

Relay 38, Check 01.81.55.1). Picked at CRCB-4 time ($171^{o}$ - $221^{o}$) if an odd number of bit relays (odd parity) are picked.

1. The R38-1 n/o points (01.81.55.1) provide a circuit to hold R38 during CRCB-5 time ($220^{o}$ - $300^{o}$).
2. The R38-2 n/o points (01.82.72.1) provide a path to latch trip R40 (error 2) during an error operation.
3. The R38-3 points are not used.
4. The R38-4 n/o points (01.82.80.1) provide a path for CRCB-5 to energize any key magnet (depending upon bit relay network) except centerscore. Energization of the key magnet causes the selected (bit relay coded) character to be printed.
5. During an operation with an error the R38-4 n/c points (01.82.80.1) provide a path to energize the centerscore key magnet and enable +S I/O PR CH (01.81.55.1) which turns on the Write-Check trigger (01.81.45.1).

### Write Operation with an Error

A check is made (01.81.55.1) of the typewriter bit relays at CRCB-4 time ($171^{o}$) via the R1-1 n/o points (01.82.72.1) and before CRCB-5 makes ($200^{o}$) to pick a key magnet. If an error exists (even number of bit relays picked) R39 (Error-1 on 01.81.55.1) is latch picked and the centerscore is printed to identify the error character.

When an error occurs involving a character without a flag (overscore), two typewriter CB cycles are required to complete the operation before the computer is cycled to present the next character to the typewriter. The centerscore is printed on the first cycle and a character is printed on the second cycle. The character printed depends upon which typewriter bit relays are picked. (Figure 11-11 is a timing chart of this operation.

When an error occurs that involves a character having an associated flag (overscore), three typewriter CB cycles are required to complete the operation before the computer is cycled to present the

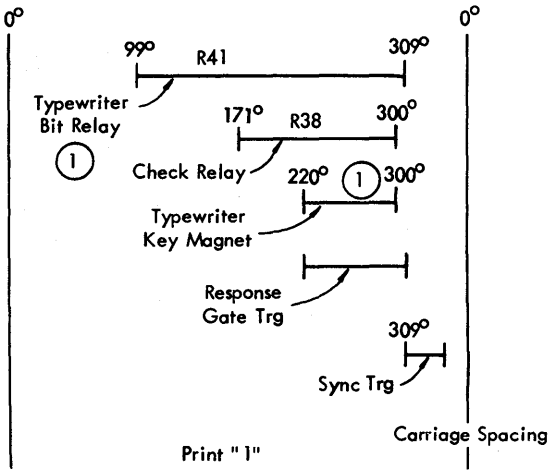




Figure 11-9. Typewriter Operation with No Parity Error

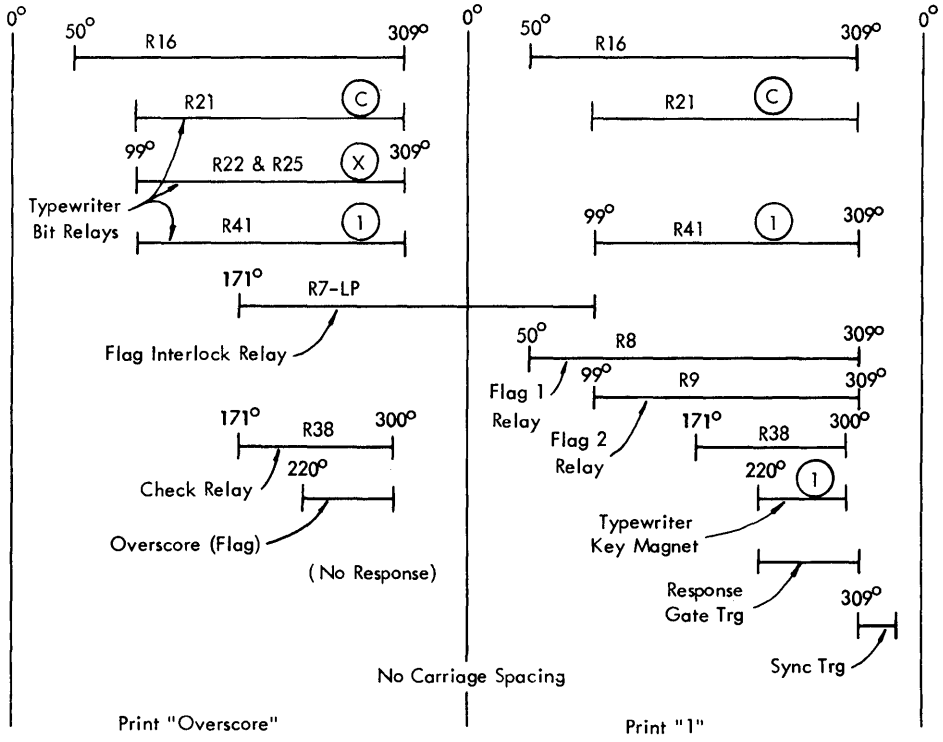



Figure 11-10. Typewriter Operation to Print Flag (Overscore) with a Numerical Character

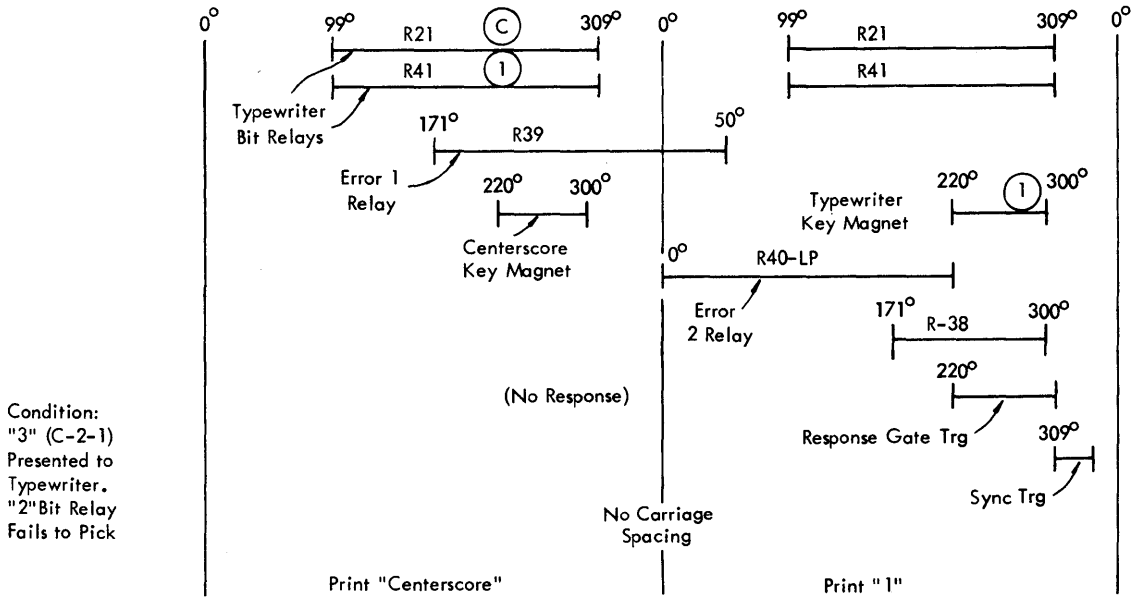



Figure 11-11. Typewriter Operation with Parity Error

next character to the typewriter. The centerscore is printed on the first cycle, the flag (overscore) on the second cycle, and a character is printed on the third cycle. The character printed depends upon which typewriter bit relays are picked. Figure 11-12 is a timing chart of this operation.

Relay 39 LP, Error-1 (01.81.55.1). This relay is latch picked at CRCB-4 time (171°) if an even number of typewriter bit relays are picked.

1. The R39-1 n/o points (01.82.72.1) provide a path for CRCB-1 (0°) to latch pick R40 (Error-2).
2. The R39-2 n/o points (01.82.75.1) provide a path for CRCB-6 (310°) to latch trip R7 (Flag Intlk).
3. The R39-3 n/c points (01.82.70.1) prevent an end-of-line carriage return from occurring by opening the pick circuit to R5 (Ctrl Carr Rtn) when an error character is at the end of a line.

The rate of printing during a write operation is such that two and possibly three typebars are in the air at a given time. Thus, when the next to last character (with the last character an error character) typebar is in the air returning from printing, Relay 39 (Error-1) is picked, the centerscore typebar is on the way to print, and the carriage is spacing into the last column contact. Relay 5 (Ctrl Carr Rtn - 01.82.70.1) cannot pick at CRCB-6 time because the R39-3 n/c points are open. If the error character has an associated flag bit (overscore) the R7-4

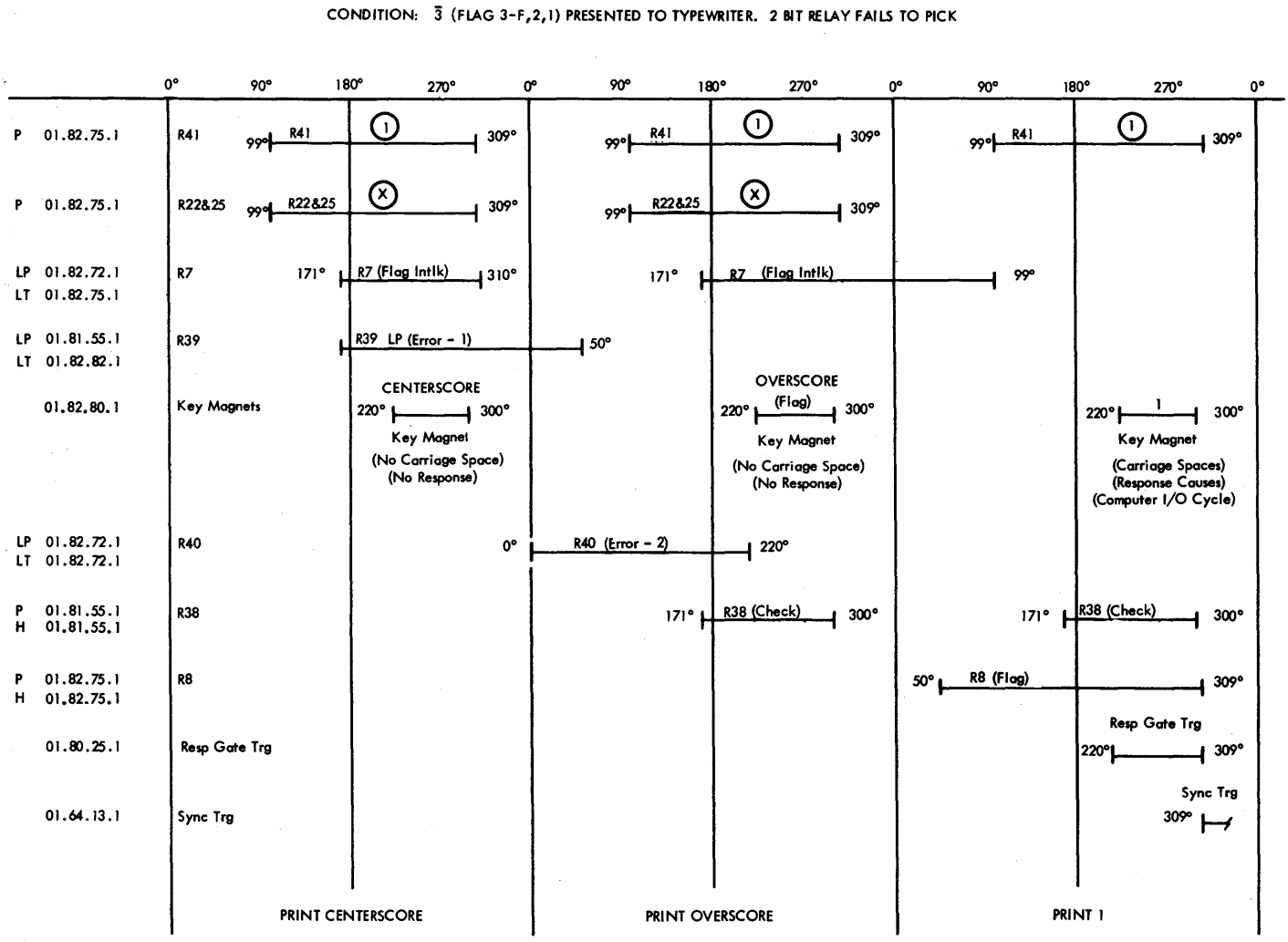



Figure 11-12. Typewriter Operation with a Parity Error and a Flag (Overscore)

n/c points prevent the carriage return operation during the cycle in which the overscore is printed. At the end of the cycle in which a character is printed, R5 can be picked at CRCB-6 time to initiate the carriage return.

Relay 40 LP, Error 2 (01.82.72.1). This relay is latch picked at CRCB-1 time via the R39-1 n/o points.

1. The R40-1 n/o points (01.82.72.1) provide a path to latch trip R39 at CRCB-2 time ($50^{o}$).
2. The R40-2 n/o points (01.81.55.1) provide a path to pick R38 at CRCB-4 time after R40 is picked. The R40-2 n/c points, when closed, provide a path to pick R39 and, when open, prevent a second pick of R39 for one error character.

Relay 40 is latch tripped when R38 is picked and CRCB-5 makes ($220^{o}$).

Relay 38, Check (01.81.55.1). This relay is picked at CRCB-4 time after R40 (Error-2) is picked.

1. The R38-1 n/o points (01.81.55.1) provide a hold for R38 during CRCB-5 time.
2. The R38-2 n/o points (01.82.72.1) provide a path to latch trip R40 at CRCB-5 time.
3. The R38-3 points are not used.
4. The R38-4 n/c points provide a path to energize the centerscore key magnet and, when ANDed with +S WRITE CALL (01.81.45.1), turns on the Write-Check trigger at CRCB-5 time.
5. The R38-4 n/o points provide a path to pick the overscore or any other key magnet depending upon which bit relays are picked.

## End-of-Line Carriage Return

When the last character (not centerscore, not overscore) at the end of a printing line is printed, the carriage is automatically returned to the left margin. During the carriage return operation the typewriter is interlocked (R11 picked) so that no characters will print while the carriage is in motion.

The rate of printing during a write operation is such that two, and possibly three typebars are in the air at a given time. Thus, when the typebar for the next to last character is in the air returning from printing, the typebar for the last character is on the way to print and the carriage is spacing into the last column position, thereby closing the last column contact. The key magnet for the last character is energized at CRCB-5 time ($220^{o}$ - $300^{o}$). The carriage spaces (after printing the previous character and before the last character prints) and closes the last column contact. At CRCB-6 time ($310^{o}$ - $360^{o}$) Relay 5 is picked. Note that the last character will print after the last column contact closes and before the carriage starts its return action.

Relay 5, Ctrl Carr Rtn (01.82.70.1). This relay is picked at CRCB-6 time after the last column contact is closed.

1. The R5-1 n/o points (01.82.70.1) provide a circuit to hold R5 via R19-1 n/c and/or the carriage return interlock contacts.
2. The R5-2 n/o points (01.82.70.1) pick the carriage return solenoid thereby initiating a carriage return operation. The carriage return interlock contacts (01.82.70.1) close and pick R19 (01.82.70.1) providing another path for holding R5. The R19-3 n/c points (01.82.70.1) drop the carriage return solenoid. Relay 19 holds through its own 19-3 n/o points and R5-2 n/o.
3. The R5-3 n/o points (01.81.50.1) have no function with this operation. The R1-4 n/o points are closed, therefore closing R5-3 n/o does not change the level on +S TPWR DISC.
4. The R5-4 n/o points (01.82.72.1) provide a path to pick R11. The R11-2 n/c points (01.82.80.1) open the circuit to: (a) all key magnets, thus preventing printing while the carriage is in motion and, (b) to +S TPWR RESP, thereby blocking the response so that a computer I/O cycle is not initiated.

When the carriage reaches the left-hand margin the carriage return interlock contacts open. Whether the carriage return interlock contacts or CRCB-3 ($99^{o}$ - $309^{o}$) drops Relay 5, depends upon when the carriage reaches the left margin. When Relay 5 drops, Relays 11 and 19 drop. When CRCB-5 makes again, the key magnet selected by the bit relays is energized and the first character of the new line is printed.

## Single-Cycle Operation

Operating the Instant Stop/SCE key with the computer in the automatic mode, stops the computer. The cycle in which the computer stops depends upon the operation being performed. The function of the Instant Stop/SCE key differs between I/O operation codes and other operation codes. Figure 6-6 (in Section 6) is a combined function chart showing the single-cycle operation.

Read Operations

Pressing the Instant Stop/SCE key during a read operation stops the computer at the end of Trigger 30 time. Successive operations of the key cause a complete character input cycle, which is completed when the end of Trigger 30 time is again reached. Note that the input character is displayed in MDR (and MBR for alpha) when the computer stops (Trigger 30 time).

Write Operations

Pressing the Instant Stop/SCE key during a write operation stops the computer with the Sync trigger ON. Each successive operation of the key causes a complete character output cycle which is completed when the Sync trigger is turned on again. Note that the output character has been printed and is displayed in MDR (and MBR for alpha) when the computer stops (Sync trigger time).

The CRCBs operate continuously when the system is being single-cycled and, if not blocked, CRCB-5 will cause repetitive printing of the character stored in the bit relays. The Write Test relay, R20, provides the points (R20-1 n/c) to prevent repetitive printing.

It should be noted that the length of the printed line differs when operating at normal system speed or at single-cycle speed. A line printed at single-cycle speed is one character shorter than a line printed at the normal speed. The single-cycle line is short because, after printing the last character, the carriage spaces and closes the last column contact. CRCB-6 makes, picking R5 which initiates a carriage return. At normal speed the typewriter prints the character mentioned with the single-cycle line and then goes through an I/O cycle starting another typebar toward the platen before CRCB-6 makes and picks R5. Thus one more character prints at normal speed than is printed during an output operation that is being single cycled.

Relay 20 LP, Write Test (01.82.72.1). Relay 20 is picked at CRCB-1 time ($0^{o}$) when TEST REL PICK is enabled. TEST REL PICK is enabled by +SEL 1 WR CALL ANDed with Not Hold trigger (+S HOLD TR inverted, on 01.64.13.1). Because, during single cycle operation, the Hold trigger is not turned on by CRCB-1 time, R20 is picked which prevents the energization of any key magnets.

1. The R20-1 n/c points (01.82.80.1) open the circuit to all key magnets and to +S TPWR RESP (01.81.50.1).
2. The R20-2 n/o points (01.82.72.1) enable +S TEST INTLK to latch trip R20 at CRCB-6 time ($310^{o}$ - $360^{o}$). Note that R20 will be latch picked at CRCB-1 time ($0^{o}$ - $51^{o}$) every CB cycle during which the Hold trigger is not ON.
3. The R20-3 n/c points (01.82.72.1) open the circuits to pick or trip R10, R11, and R7 on 01.82.72.1 and R38 (or R39) on 01.81.55.1.
4. The R20-3 n/c points (01.82.75.1) perform no function during single-cycle operations.

CONTROL ( CODE 34 - K)

The sequence block diagram for this operation is shown in Figure 11-13. The function chart for this operation is shown on page 20 in the Instructional System Diagrams. Timing charts, Figure 11-14, 11-15 and 11-16 show the operation of: space, carriage return, and tabulate.

Objective

Execute the control function designated by the $Q_{11}$ digit of the instruction on the input-output device specified by the $Q_8$ and $Q_9$ digits of the instruction.

Functions

An 01 in the $Q_8$ and $Q_9$ digits of the instruction is placed in the D/B register during the I-cycle and decoded to select the typewriter.

The $Q_{11}$ digit of the instruction is available in MDR at the end of the I-cycle for use in specifying the control function. The 1-digit codes are assigned as follows:

1 - Space
2 - Carriage return
8 - Tabulate

When the Hold trigger is turned on upon entry into E-cycle, an MDR 1, 2, or 8-bit ANDs with Select 1 (typewriter) to pick Relay 6 (Space), Relay 5 (Carriage Return), or Relay 4 (Tabulate). Each of these relays controls the performance of its particular control function.

The typewriter remains selected only until the execution of the control function is completed.

See Customer Engineering Manual of Instruction, B1 Electric Typewriter As Modified for DP Equipment, (Form 223-6653) for a description of the following typewriter components:

Space solenoid
Carriage return solenoid
Tabulate solenoid
Carriage return interlock contact
Tab interlock contact.

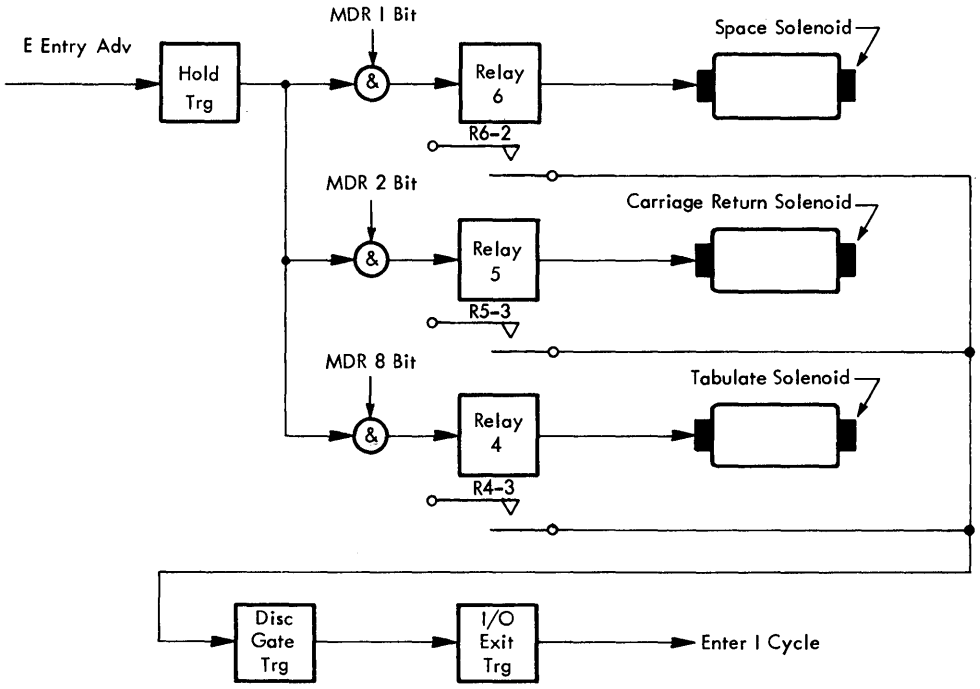



Figure 11-13. Control - Code 34

Auxiliary Trigger Status

Disconnect Gate Trigger (01.80.25.1).

1. OFF when E-cycle is entered.
2. Turned on by signal from typewriter that a control function has been initiated.
3. Turned off by I/O Exit trigger.

I/O Exit Trigger (01.64.13.1).

1. OFF when E-cycle is entered.
2. Turned on by signal from typewriter that the control function has been completed.
3. Turned off during Trigger 1 time of the I-cycle for the next instruction .

E-Timer Trigger Objectives

Hold Trigger (01.64.12.1).

1. Block MAR reset to maintain the control function code digit in MDR and to prevent VRC error.
2. Pick Relay 6, 5, or 4 for performance of control function.
3. Stop the computer clock to prevent unnecessary cycling of memory.

Relay Functions

Space

Figure 11-14 is a timing chart of this operation

Relay 6, Control Space (01.82.70.1). This relay is picked at CRCB-6 time ($310^{o}$ - $360^{o}$) when CTRL SPACE DR is enabled (01.82.60.1) by MDR 1-bit ANDed with Code 34.

1. The R6-1 n/o points (01.82.82.1) provide a circuit to energize the space magnet. The typewriter space cam operates; the space interlock contacts (No. 1 on 01.81.60.1 and No. 2 on 01.81.50.5) are closed; and the carriage spaces (Space interlock contact No. 1 performs no function during a control code space operation.) Space interlock contact No. 2 enables +S TPWR RESP via the R54-4 n/c points.
2. The R6-2 n/o points (01.81.50.1) enable +S TPWR DISC (via R19-1 n/o) which, ANDed with OP 34 K turns on the Disconnect Gate trigger. When Relay 6 is dropped and +S CRCB-4 DISCONN is enabled, the I/O Exit trigger is turned on.

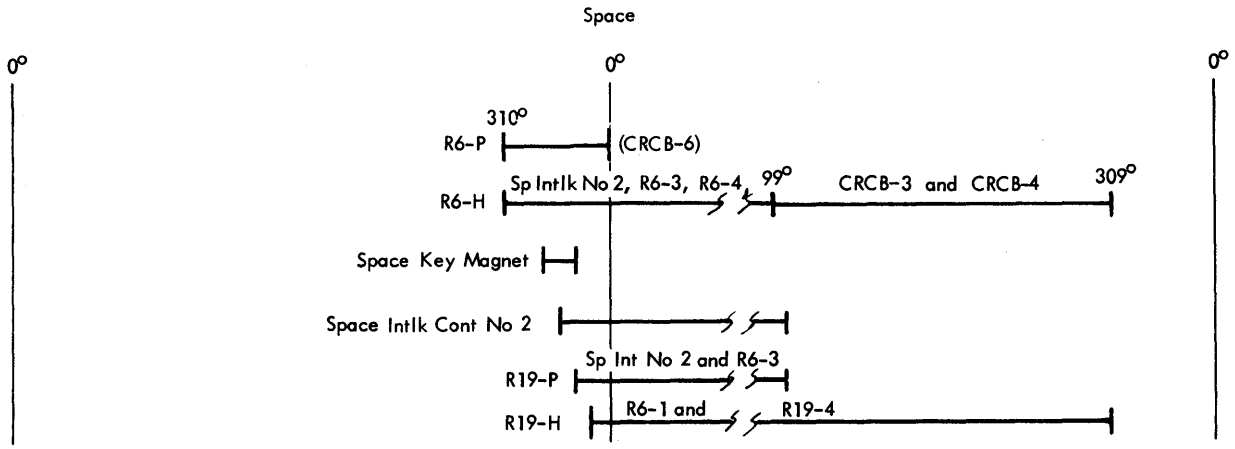



Figure 11-14. Space

3. The R6-3 n/o points (01.82.70.1) provide circuits to:
   a. Pick R19 (01.82.70.1). Starting at ground on R19P, through R19P coil, R6-3 n/o space interlock contact No. 2 (01.81.50.1) to +48v.
   b. Hold R6 via the R6-4 n/o points.
4. The R6-4 n/o points (01.80.72.1) provide a hold for R6 via CRCB-3, R19-1 n/c and also via the R6-3 n/o points as follows: from ground at R6 hold coil, through R6 H coil through R6-4 n/o to R4-1 armature as a binder, to R5-1 armature as a binder, to R19-1 n/c as a binder through the diode (TB74-7B and TB74-7A) to R19P as a binder, through R6-3 n/o through space interlock contact No. 2 n/o (01.81.50.1) to +48v.

NOTE: R6 is held momentarily (until R19 is picked) through the R19-1 n/c points and R6-4 points.

Relay 19 (01.82.70.1). Relay 19 is picked via the R6-3 n/o points when space interlock contact No. 2 n/o makes.

1. The R19-1 n/o points (01.82.70.1) provide a path via the R6-2 n/o points, to enable +S TWR DISC.
2. The R19-2 n/o points (01.82.70.1) perform no function during a control space operation.
3. The R19-3 n/o points (01.82.70.1) perform no function during a control space operation.
4. The R19-4 n/o points (01.82.82.1) provide a hold for R19H (01.82.70.1).
5. The R19-4 n/c points (01.82.82.1) open and de-energize the space magnet.

The hold on Relay 6 is dropped by the space interlock contact No. 2 going open or by CRCB-3 whichever opens last. When R6 drops, the R6-1 n/o points open the circuit to R19H and R19 drops, the R6-2 n/o points open and turn on the I/O Exit trigger at CRCB-4 time.

Carriage Return

Figure 11-15 is a timing chart for this operation.

Relay 5, Control Carriage Return 901.82.70.1). Relay 5 is picked at CRCB-6 time when CTRL CARR RTN DR is enabled by MDR 2 Bit ANDed with Code 34 (01.82.60.1).

1. The R5-1 n/o points (01.82.70.1) provide a circuit to hold R5 via R19-1 n/c and/or CRCB-3 and/or the carriage return interlock contacts.
2. The R5-2 n/o points (01.82.70.1) provide a path to energize the carriage return solenoid thereby initiating a carriage return operation. The carriage return interlock contacts (01.82.70.1) close picking R19 (01.82.70.1), and providing another path for holding R5. The R5-2 n/o points also provide a path for holding R19 via the R19-3 n/o points.
3. The R5-3 n/o points (01.81.50.1) enable +S TWR DISC (via the R19-1 n/o points) which, ANDed with OP 34 K, turns on the Disconnect Gate trigger. When R5 is dropped and +S CRCB-4 DISCONN (01.82.70.1) is enabled, the I/O Exit trigger is turned on.

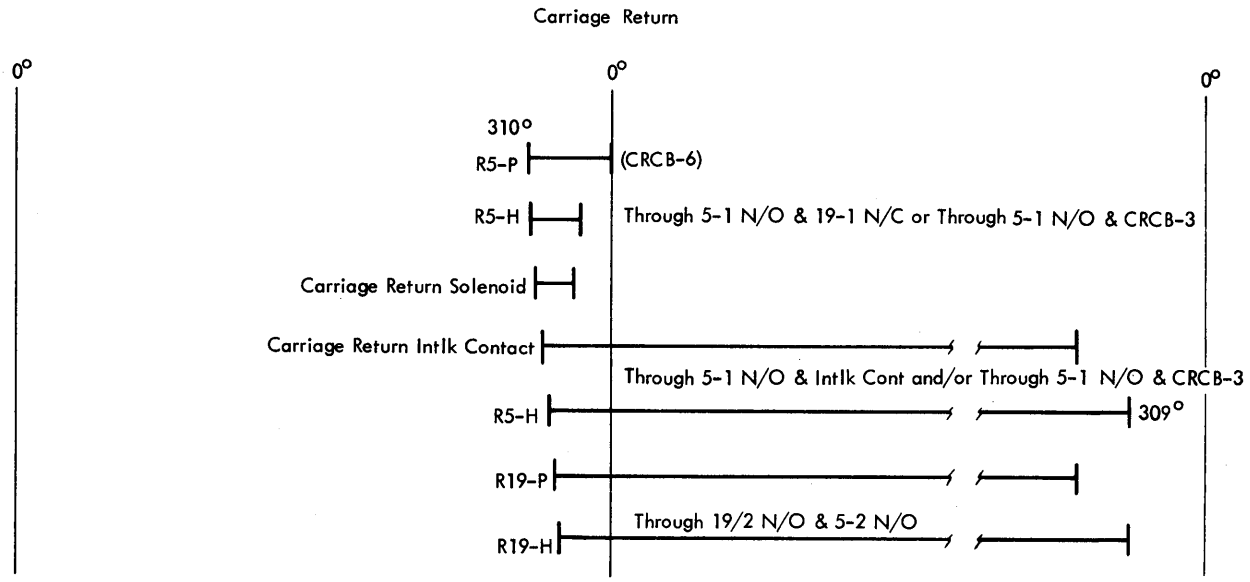



Figure 11-15. Carriage Return

4. The R5-4 n/o points (01.82.72.1) provide a path to pick R11, Shift Delay, at CRCB-4 time. Though R11 is picked and held, R11 performs no required functions for this operation.
5. The R5-4 n/c points (01.82.72.1) provide a path to enable +S CRCB-4 DISCONN when R5 is dropped at the end of the operation. +S CRCB-4 DISCONN turns on the I/O Exit trigger to terminate the operation.

Relay 19 (01.82.70.1). Relay 19 is picked when the carriage return interlock contact closes.

1. The R19-1 n/o points (01.82.70.1) provide a path (via R5-3 n/o, 01.81.50.1) to enable +S TWR DISC.
2. The R19-1 n/c points (01.82.70.1) in opening, remove one of the holds on R5.
3. The R19-2 points (01.82.70.1) perform no function during this operation.
4. The R19-3 n/o points (01.82.70.1) provide a hold for R19 (via R5-2 n/o).
5. The R19-3 n/c points (01.82.70.1) open the circuit to the carriage return solenoid.
6. The R19-4 points (01.82.82.1) perform no function during this operation.

When the carriage reaches the left margin, the carriage return interlock contacts are opened removing one of the holds on R5. When CRCB-3 breaks, the other hold on R5 is removed. Note that, whether the carriage return interlock contacts or CRCB-3 drop R5, depends upon which opens last. When R5 drops, R19 is dropped (R5-2 n/o) and R11 is dropped (R5-4 n/o). At CRCB-4 time +S CRCB-4 DISCONN (01.82.72.1) is enabled (via R5-4 n/c) and the I/O Exit trigger is turned on.

Tabulate

Figure 11-16 is a timing chart of this operation.

Relay 4, Ctrl Tab (01.82.70.1). Relay 4 is picked at CRCB-6 time when CTRL TAB DR is enabled by MDR 8 Bit ANDed with Code 34 (01.82.60.1).

1. The R4-1 n/o points (01.82.70.1) provide a circuit to hold R4 via R19-1 n/c and/or the tab interlock contacts and/or CRCB-3.
2. The R4-2 n/o points (01.82.70.1) provide a circuit to energize the tabulate solenoid thereby initiating a typewriter carriage tabulate operation. The tabulate interlock contacts (01.82.70.1) close, picking R19 and providing another path for holding R4. The R4-2 n/o points also provide a path for holding R19 via the R19-2 n/o points.
3. The R4-3 n/o points (01.81.50.1) enable +S TWR DISC (via the R19-1 n/o points) which, ANDed with OP 34 K, turns on the Disconnect Gate trigger. When R4 is dropped and +S CRCB-4 DISCONN (01.82.72.1) (01.82.72.1) is enabled, the I/O Exit trigger is turned on.

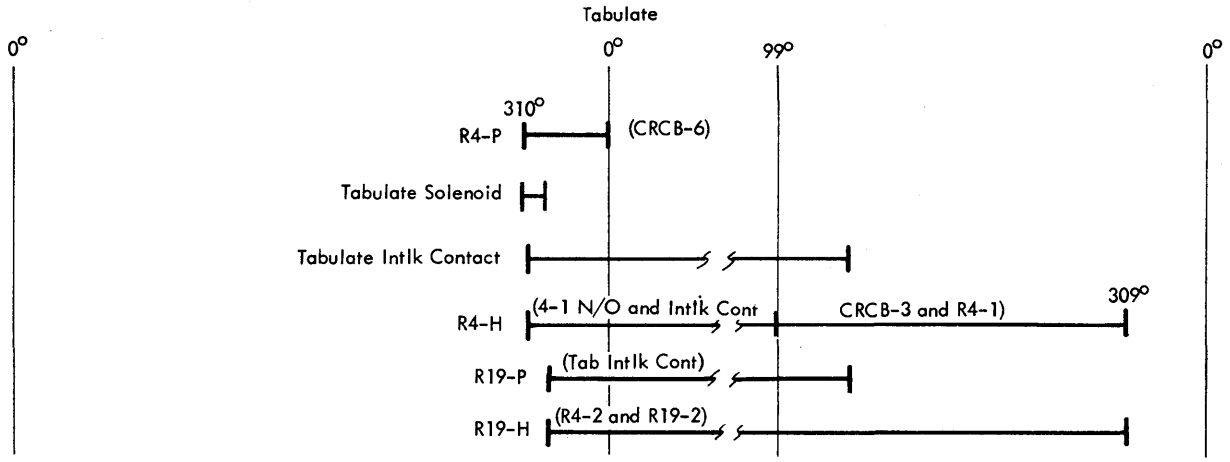



Figure 11-16. Tabulate

Relay 19 (01.82.70.1). Relay 19 is picked when the tab interlock contact closes.

1. The R19-1 n/o points (01.82.70.1) provide a path (via R4-3 n/o, 01.81.50.1) to enable +S TWR DISC.
2. The R19-1 n/c points (01.82.70.1) in opening remove one of the holds on R5.
3. The R19-2 n/o points (01.82.70.1) provide a path (via R4-2) to hold R19.
4. The R19-2 n/c points (01.82.70.1) open the circuit to the tab solenoid.
5. The R19-3 points (01.82.70.1) perform no function during this operation.
6. The R19-4 points (01.82.82.1) perform no function during this operation.

When the carriage reaches the next set tab stop, the carriage stops, the tabulate mechanism is released, and the tabulate interlock contacts are opened, removing one of the holds on R4. When CRCB-3 breaks, the other hold on R4 is removed. Note that whether the tabulate interlock contacts or CRCB-3 drop R4 depends upon which opens last. When R4 drops, R19 is dropped (R4-2 n/o). At CRCB-4 time, +S CRCB-4 DISCONN (01.82.72.1) is enabled and the I/O Exit trigger is turned on.

## SET FLAG (CODE 32 - SF)

The sequence block diagram for this operation is shown in Figure 12-1. The function chart for this operation is shown on page 21 in the Instructional System Diagrams, 1620 Model 1, Data Processing System (Form 227-5769).

### Objective

Place a flag bit in the memory location designated by the P-address (OR-2).

### Functions

Two memory cycles are required as follows:

1. The content of the location in which a flag bit is to be stored is read from memory per OR-2 and stored in MDR.
2. Reset of MDR is blocked (Read-Y). The content of the same memory location is again read out. The Read-Y condition blocks odd or even sense amplifiers per OR-2 address to prevent entry into MBR, thus clearing the memory location.

   The MDR F-bit trigger is turned on (if off). The contents of MDR are transferred to MBR as a function of Read-Y. If a C-bit is present in MDR it will be cleared by the C-bit corrector between MDR and MBR. If no C-bit is present in MDR, it will be added by the C-bit corrector between MDR and MBR. The contents of MBR are written into memory per OR-2.

   The Q-address (OR-1) is not used in this operation.

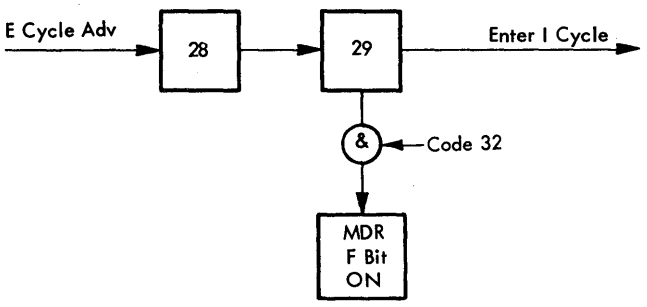



Figure 12-1. Set Flag - Code 32

### Auxiliary Triggers

None are used.

### E-Timer Trigger Objectives

Trigger 28 (01.60.58.1).

1. Read out of memory per OR-2 and store the digit in MDR.

Trigger 29 (01.60.59.1).

1. Block reset of MDR (Read-Y).
2. Read out of memory per OR-2 with either the odd or even sense amplifiers blocked (Read-Y), depending on whether the OR-2 address is odd or even, to clear the memory location.
3. Set an F-bit in MDR.
4. Transfer MDR to MBR setting or clearing a C-bit in MBR to maintain odd parity.
5. Write into memory per OR-2 from MBR.
6. End operation and enter I-cycle for the next instruction in sequence.

## CLEAR FLAG (CODE 33 - CF)

The sequence block diagram for this operation is shown in Figure 12-2. The function chart for this operation is shown in the Instructional System Diagrams on page 21.

### Objective

Remove the flag bit, if present, from the memory location designated by the P-address (OR-2).

### Functions

Two memory cycles are required as follows:

1. The content of the location from which a flag bit is to be removed is read from memory per OR-2 and stored in MDR.
2. Reset of MDR is blocked (Read-Y). The content of the same memory location is again read out. The Read-Y condition blocks the odd or even sense amplifiers

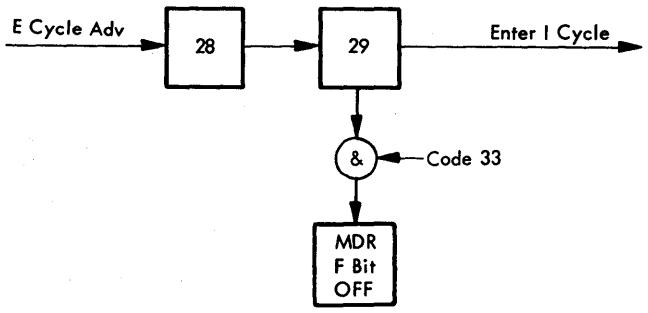



Figure 12-2. Clear Flag - Code 33

per OR-2 address to prevent entry into MBR and clear the memory location. The MDR F-bit trigger is turned off (if on). The contents of MDR are transferred to MBR as a function of Read-Y. If a C-bit is present in MDR it will be cleared by the C-bit corrector between MDR and MBR. The contents of MBR are written into memory per OR-2.

The Q-address (OR-1) is not used in this operation.

## Auxiliary Triggers

None are used.

## E-Timer Trigger Objectives

Trigger 28 (01.60.58.1).

1. Read out of memory per OR-2 and store the digit in MDR.

Trigger 29 (01.60.59.1).

1. Block reset of MDR (Read-Y).
2. Read out of memory per OR-2 with either the odd or even sense amplifiers blocked (Read-Y), depending on whether the OR-2 address is odd or even, to clear the memory location.
3. Turn off the MDR F-bit trigger.
4. Transfer MDR to MBR setting or clearing a C-bit in MBR to maintain odd parity.
5. Write into memory per OR-2 from MBR.
6. End operation and enter I-cycle for the next instruction in sequence.

# HALT (CODE 48 - H)

The sequence block diagram for this operation is shown in Figure 12-3. The function chart for this operation is shown in the Instructional System Diagrams on page 4 (Trigger 8 of the I-cycle).

## Objective

Stop the machine upon completion of the I-cycle of this instruction.

## Function

The machine stops at the end of I-cycle. The manual status light is turned on when the Run trigger is turned off. The automatic status light is turned off when the Start 1 trigger is turned off. P and Q-addresses are not used in this operation.

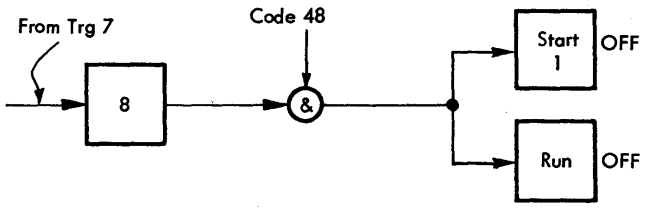



Figure 12-3. Halt - Code 48

## Auxiliary Triggers

None are used.

## E-Timer Triggers

None are used. This operation is completed by Trigger 8. Refer to I-cycle function chart shown in the Instructional System Diagrams on page 4.

Trigger 8 (01.15.18.1).

1. Turn off Start 1 trigger.
2. Turn off Run trigger.

## NO OPERATION (CODE 41 - NOP)

The sequence block diagram for this operation is shown in Figure 12-4. The function chart for this operation is shown in the Instructional System Diagrams on page 4 (Trigger 8 time of the I-cycle).

### Objective

Complete the I-cycle of this instruction and proceed to the next instruction in sequence (address in IR-1).

### Functions

See Objective. The P and Q-addresses are not used in this operation.

### Auxiliary Triggers

None are used.

### E-Timer Triggers

None are used. This operation is completed by the E-cycle Entry trigger. Refer to I-cycle function chart shown in the Instructional System Diagrams.

Trigger 8 (01.15.18.1).

1. Turn on the E-cycle Entry trigger.

E-Cycle Entry Trigger (01.15.18.1).

1. Enter I-cycle for the next instruction in sequence.

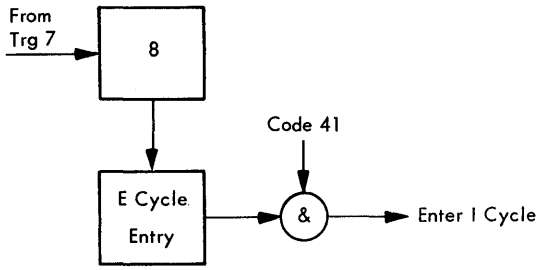



Figure 12-4. No Operation - Code 41

Arithmetic operations are accomplished by referring to tables stored in memory. The Add Table, Figure 13-1, contains all possible 2-digit sums, with a carry indicated by a flag bit with the table digit where the sum exceeds nine. The Multiply Table, Figure 13-2 contains all possible 2-digit products. Each 2-digit product read from memory consists of two adjacent digits from the multiply table area.

| High Order Positions of Address | Units Position of Address | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0030 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0031 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | $\bar{0}$ |
| 0032 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | $\bar{0}$ | $\bar{1}$ |
| 0033 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ |
| 0034 | 4 | 5 | 6 | 7 | 8 | 9 | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ |
| 0035 | 5 | 6 | 7 | 8 | 9 | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ | $\bar{4}$ |
| 0036 | 6 | 7 | 8 | 9 | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ | $\bar{4}$ | $\bar{5}$ |
| 0037 | 7 | 8 | 9 | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ | $\bar{4}$ | $\bar{5}$ | $\bar{6}$ |
| 0038 | 8 | 9 | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ | $\bar{4}$ | $\bar{5}$ | $\bar{6}$ | $\bar{7}$ |
| 0039 | 9 | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ | $\bar{4}$ | $\bar{5}$ | $\bar{6}$ | $\bar{7}$ | $\bar{8}$ |

Figure 13-1. Add Table

| High Order Positions of Address | Units Position of Address | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0010 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0011 | 0 | 0 | 1 | 0 | 2 | 0 | 3 | 0 | 4 | 0 |
| 0012 | 0 | 0 | 2 | 0 | 4 | 0 | 6 | 0 | 8 | 0 |
| 0013 | 0 | 0 | 3 | 0 | 6 | 0 | 9 | 0 | 2 | 1 |
| 0014 | 0 | 0 | 4 | 0 | 8 | 0 | 2 | 1 | 6 | 1 |
| 0015 | 0 | 0 | 5 | 0 | 0 | 1 | 5 | 1 | 0 | 2 |
| 0016 | 0 | 0 | 6 | 0 | 2 | 1 | 8 | 1 | 4 | 2 |
| 0017 | 0 | 0 | 7 | 0 | 4 | 1 | 1 | 2 | 8 | 2 |
| 0018 | 0 | 0 | 8 | 0 | 6 | 1 | 4 | 2 | 2 | 3 |
| 0019 | 0 | 0 | 9 | 0 | 8 | 1 | 7 | 2 | 6 | 3 |
| 0020 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0021 | 5 | 0 | 6 | 0 | 7 | 0 | 8 | 0 | 9 | 0 |
| 0022 | 0 | 1 | 2 | 1 | 4 | 1 | 6 | 1 | 8 | 1 |
| 0023 | 5 | 1 | 8 | 1 | 1 | 2 | 4 | 2 | 7 | 2 |
| 0024 | 0 | 2 | 4 | 2 | 8 | 2 | 2 | 3 | 6 | 3 |
| 0025 | 5 | 2 | 0 | 3 | 5 | 3 | 0 | 4 | 5 | 4 |
| 0026 | 0 | 3 | 6 | 3 | 2 | 4 | 8 | 4 | 4 | 5 |
| 0027 | 5 | 3 | 2 | 4 | 9 | 4 | 6 | 5 | 3 | 6 |
| 0028 | 0 | 4 | 8 | 4 | 6 | 5 | 4 | 6 | 2 | 7 |
| 0029 | 5 | 4 | 4 | 5 | 3 | 6 | 2 | 7 | 1 | 8 |

Figure 13-2. Multiply Table

The address for a specific table location is developed by combining in a unique manner the two factors involved in a cycle of the arithmetic operation.

Subtraction is accomplished by complement addition using the add table.

Compare operations establish the relative value of two fields, with signs taken into consideration. Compare is essentially a subtract operation, except that the difference digits are not retained.

Function charts for 1620 Operation Codes are located in the IBM Customer Engineering Instructional System Diagrams, 1620 Model 1, Data Processing System, (Form 227-5769).

## ADD (CODE 21 - A)

A sequential flow diagram for addition is shown in Figure 13-3. Sequence block diagrams for this operation are shown in Figures 13-4 and 13-5. Function charts and logic flow for this operation are shown in the Instructional System Diagrams on pages 22, 23, and 24.

## Objective

Add the field at the Q-address (OR-1) to the field at the P-address (OR-2), and store the algebraic sum at the P-address (OR-2) and successively lower memory locations.

## Functions

The location of the addend (Q-field) is specified by OR-1. The location of the augend (P-field) is specified by OR-2. The algebraic sum is stored in the P-field specified by OR-2. The Q-field remains unchanged. Minimum field lengths for either the P or Q-fields is two digits.

Four memory cycles are required for the development of each digit in the algebraic sum, as follows:

1. One digit from the Q-field is read from memory per OR-1 to the units position of the Digit/Branch (D/B) register (Trigger 11).
2. The corresponding digit of the P-field is read from memory per OR-2 to MDR. (Trigger 12).
3. The P-field digit is transferred from MDR to the tens position of MAR and the Q-field digit stored in the D/B register is transferred to the units position of MAR.

NOTE: The Q-field digit may be complemented before it is placed in MAR depending upon the signs of the P and Q-fields.

   This manufactured address with a "3" placed into the hundreds position of MAR is used to read the 1-digit sum from the add table in memory, (Figure 13-1) to MDR (Trigger 13).
4. The 1-digit sum is then written back into memory from MDR to the correct digit position (per OR-2) replacing the original P-field digit (Trigger 14).

There are two types of carries:

1. A carry resulting from the addition of two digits is noted by a flag bit with the appropriate 1-digit sum in the add table. This flag bit turns on the Carry Out trigger.
2. A carry resulting from the addition of a previous carry to a "9" output of the T/C switch is noted by turning on the Carry Out trigger.

Detection of a carry (Carry Out trigger ON) sets a logical path for the next Q-field digit so that it is increased by one before it is used to address the add table in the next add cycle.

Recomplement is required in any add operation where the sign of the P and Q-fields are initially different and the P-field is of less absolute value than the Q-field.

Addition proceeds serially, one digit at a time, building up partial sums from low-order to high-order digit of the sum field until the operation is terminated by a flag bit (Field Mark No. 2) in the high-order position of the P-field. The high-order digit of the sum is marked by storing a flag bit. The sign of the sum is marked by the presence or absence of a flag bit in the units position of the sum (a flag bit indicates a minus sign (-) and a no flag bit indicates a plus sign (+).

The number of digits in the sum is equal to the number of digits in the P-field. For a complete sum to be formed, the number of digits in the P-field must be greater than, or equal to, the number of digits in the Q-field. If this rule is violated, the overflow indicator is turned on, and the addition is performed using only as many Q-field digits as there are positions in the P-field (the extra digits in the addend are not used). The algebraic sum of the two equal length fields is then obtained. See the Add-Sequential Flow Diagram, Figure 13-3.

## Resulting Indicator Conditions

1. The High/Plus (H/P) indicator is ON if the sum is positive and is OFF if the sum is negative or zero.
2. The Equal/Zero (E/Z) indicator is ON if the sum is zero and OFF if the sum is not zero.
3. The overflow indicator is turned on if an overflow occurs; the overflow digit is lost. If the overflow indicator is ON as the result of a previous arithmetic operation, a no-overflow condition of this add instruction will not turn it off.

NOTE: Once the H/P or E/Z indicators are turned on (or off) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed (unless the Reset key on the console is pressed which turns off these indicators). Testing them with a branch indicator or branch no indicator instruction has no effect on their state. The overflow indicator will be turned off only by testing it with a branch indicator or branch no indicator instruction (or by pressing the Reset key on the console).

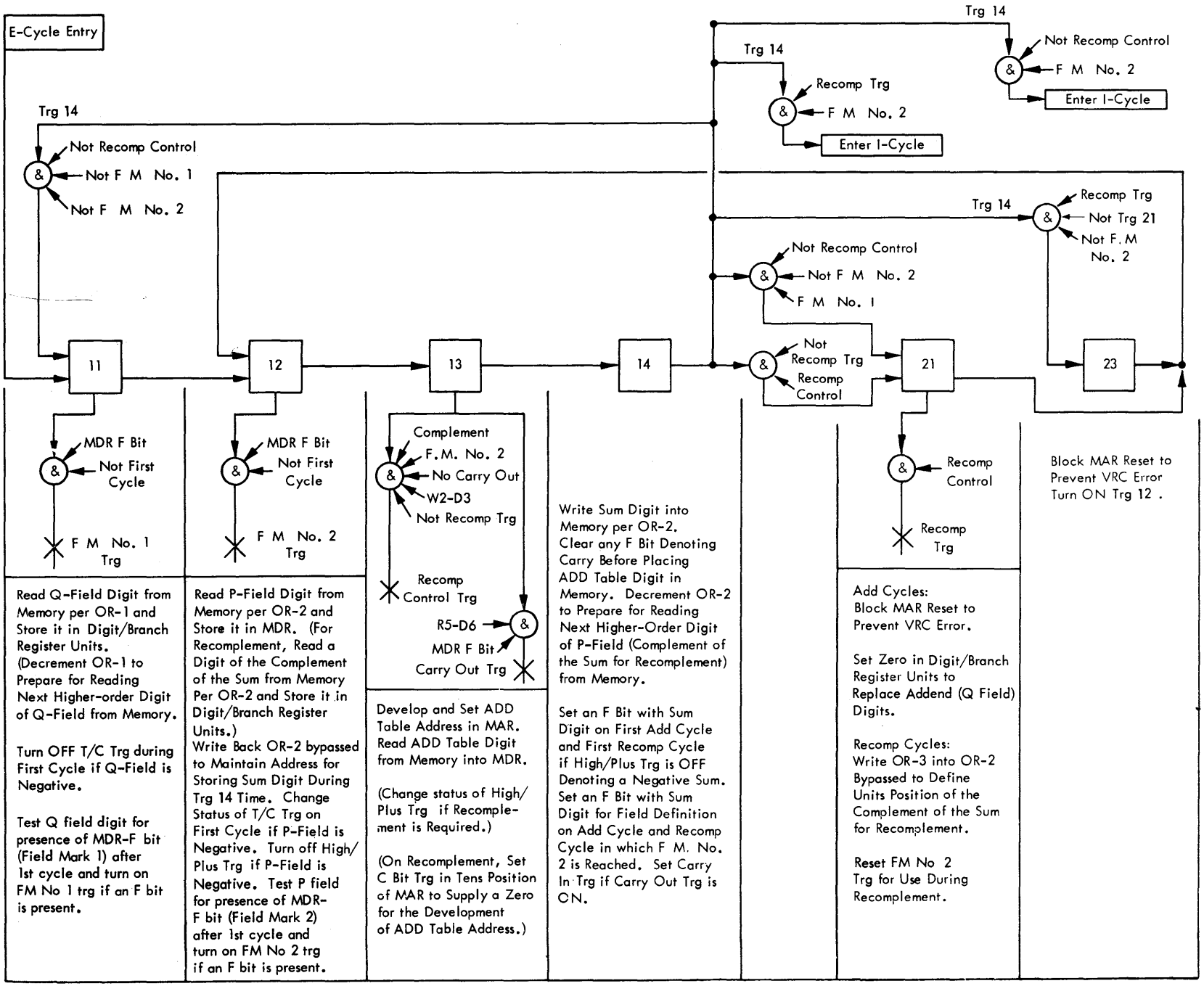



Figure 13-3. Add - Sequential Flow Diagram

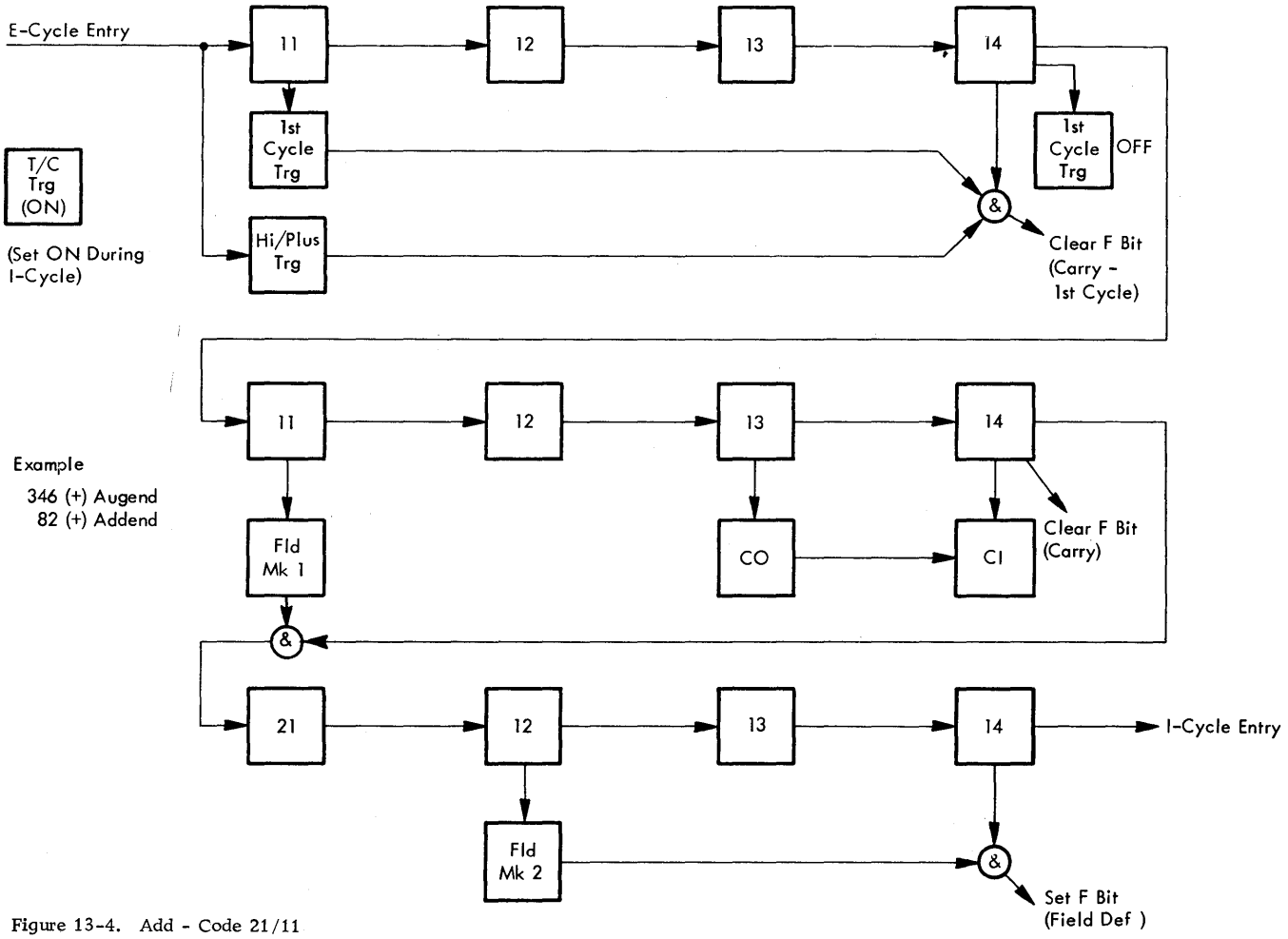



Figure 13-4. Add - Code 21/11

Auxiliary Trigger Status

True/Complement (T/C) Trigger (01.63.20.1).

1. Turned on by Trigger 1 during I-cycle and therefore will be ON when E-cycle is entered.
2. Turned off during Trigger 11 time on first add cycle if Q-field is negative.
3. Status changed during Trigger 12 time on first add cycle if P-field is negative.
4. Operation will be true if T/C trigger is ON at the end of Trigger 12 time of first add cycle and complement if T/C trigger is OFF Complement operation requires that the Q-field be complemented (10's complement in units position; 9's complement in other positions) for the development of add table addresses.

Decrement Trigger (01.60.05.1).

1. Turned on (decrement) during Trigger 8 time of the preceding I-cycle.
2. Will remain ON until the next I-cycle is entered.
3. Where it is required, during the E-cycle, that a MARS address be written back in the same storage register or transferred to another MARS storage register without being decremented, a decrement switch bypass line will be made available by an E-timer trigger.

First Cycle Trigger (01.63.10.1).

1. Turned on by Trigger 11 when E-cycle is entered.

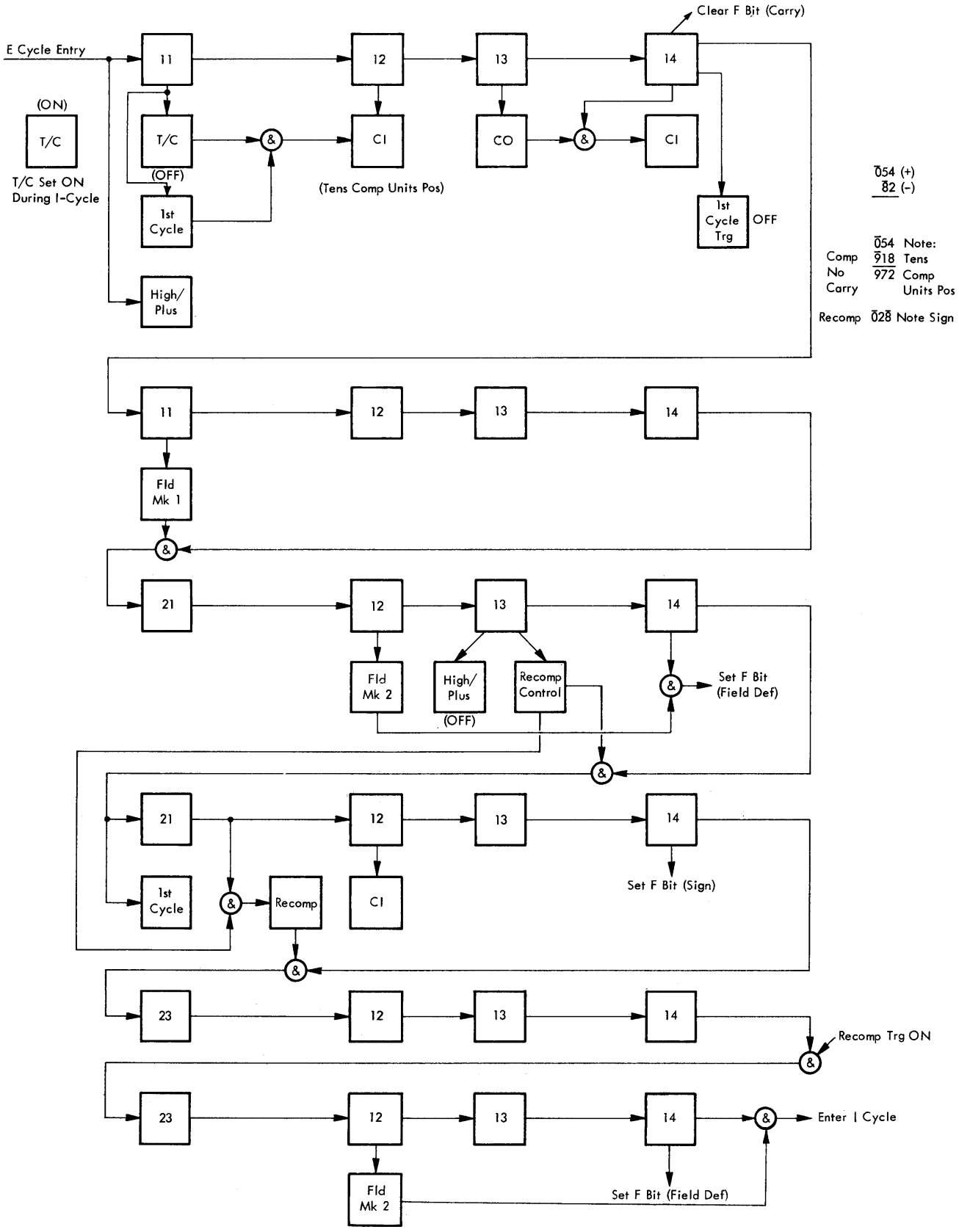



Figure 13-5. Add with Recomplement

2. Turned off at the end of Trigger 14 time on first add cycle.

If recomp is required:

3. Turned on at the beginning of recomp operation in parallel with Trigger 21.
4. Turned off by Trigger 23 at the end of first cycle recomp.

High/Plus Trigger (01.60.40.1).

1. Turned on when E-cycle is entered.
2. Turned off during Trigger 12 time on first add cycle if P-field is negative.
3. Status changed during Trigger 13 time on add cycle in which Field Mark No. 2 is reached if recomplement is required. (No carry out on a complement operation.)
4. Turned off by Trigger 14 when I-cycle is entered if the E/Z trigger is ON (zero sum or difference).

Equal/Zero (E/Z) Trigger (01.60.41.1).

1. Turned on when E-cycle is entered.
2. Turned off during Trigger 13 time if an add table digit is other than zero.

Field Mark No. 1 Trigger (01.63.30.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Cannot be turned on during first add cycle (Q-field must be a minimum of two digits).
3. Will be turned on during Trigger 11 time on add cycle in which end of Q-field is reached.

Field Mark No. 2 Trigger (01.63.30.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Cannot be turned on during first add cycle (P-field must be a minimum of two digits).
3. Will be turned on during Trigger 12 time on add cycle in which end of P-field is reached.

Carry-Out Trigger (01.63.40.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Reset OFF by Triggers 11, 21, and 23.
3. Turned on during Trigger 13 time on add and subtract cycles where the output of the T/C switch is a "9" and the Carry In trigger is ON.
4. Turned on during Trigger 13 time on add cycles where the add table digit in MDR contains an F-bit (carry).

Carry In Trigger (01.63.40.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Turned on during Trigger 12 time on first add cycle if operation is complement (to obtain 10's complement in units position).
3. Reset OFF during Trigger 13 time.
4. Turned on by Trigger 14 if the Carry Out trigger is ON.
5. Turned on during Trigger 12 time on first recomp cycle (to obtain 10's complement in units position).

Recomplement Control Trigger (01.60.24.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Will be turned on during Trigger 13 time on a complement operation if there is no carry out on add cycle in which Field Mark No. 2 is reached.

Recomplement Trigger (01.60.32.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Turned on by Trigger 21 at the beginning of a recomplement operation. (Recomplement trigger ANDed with Trigger 14 turns on Trigger 23 for the second and succeeding cycles of recomp.)

## Sign Analysis

The sign analysis chart, Figure 13-6, shows the operation of the T/C, H/P, and E/Z triggers for an add operation. The chart shows the conditions requiring a recomplement operation and the conditions causing an overflow.

## E-Timer Trigger Objectives

Trigger 11 (01.60.11.1).

1. Read out of memory per OR-1 and store the digit in D/B register units.
2. Write back OR-1 decremented.
3. Turn on Field Mark No. 1 trigger after first cycle when end of Q-field is reached.
4. Turn off T/C trigger during first cycle if Q-field is negative.

Trigger 12 (01.60.12.1).

1. Read out of memory per OR-2 and store the digit in MDR.

| | | ADD | | | |
|---|---|---|---|---|---|
| Sign of P Field (Augend) | | + | + | − | − |
| Sign of Q Field (Addend) | | + | − | + | − |
| Set High/Plus Trg (Store Sign of P Field) | | ON + | ON + | OFF − | OFF − |
| Set T/C Trigger (True or Comp Op) | | ON True | OFF Comp | OFF Comp | ON True |
| If Carry Out | | Set Overflow | No Recomp | No Recomp | Set Overflow |
| If No Carry Out | | No Recomp | Recomp | Recomp | No Recomp |
| Resulting Sign | No Recomp | + | + | − | − |
| | Recomp | | − | + | |
| NOTES: If the Equal/Zero Trigger is ON (Zero Sum) when the I-Cycle following the Add Operation is Entered, the Hi gh/Plus Trigger is turned OFF (- Sign). | | T/C Turned ON During I-Cycle High/Plus & Equal/Zero turned ON in Parallel with Trg 11 | | | |

Figure 13-6. Sign Analysis Chart for Addition

2. Write back OR-2 bypassed (to save address for writing the sum digit into memory during Trigger 14 time).
3. Change the status of the T/C trigger on first cycle if P-field is negative.
4. Turn off H/P trigger on first cycle if P-field is negative.
5. Turn on Field Mark No. 2 trigger after first cycle when end of P-field is reached.

For complement operation or recomp:

6. Turn on the Carry In trigger during first cycle to obtain 10's complement in units position.

For recomp:

7. Set D/B register units from MDR.

Trigger 13 (01.60.13.1).

1. Develop and set add table address in MAR (see Figure 13-7).
2. Read out of memory per add table address and store the sum digit in MDR.
3. Turn on the Carry Out trigger if MDR contains an F-bit (carry).
4. Turn on the Carry Out trigger if the output of the T/C switch is a "9" and the Carry In trigger is on.
5. Reset D/B register units. (See Trigger 21 Objective 2.)

For recomp:

6. Turn on Recomp Control trigger if, during a complement operation, there is no carry out on add cycle in which Field Mark No. 2 is reached.
7. Set C-bit latch in tens position of MAR to supply a zero for development of add table address.
8. Change status of H/P trigger if recomplement is required.

Miscellaneous:

9. Set Overflow trigger if:
   (a) On a true operation a carry out is detected on the add cycle in which Field Mark No. 2 is reached (sum exceeds available P-field space).
   (b) The P-field is shorter than the Q-field. (Field Mark No. 2 trigger turned on before Field Mark No. 1 trigger.)
10. Turn off E/Z trigger if add table digit is not a "zero".

Trigger 14 (01.60.14.1).

1. Block reset of MDR (Read-Y).
2. Read out of memory per OR-2 with either the odd or the even sense amplifiers blocked (Read-Y), depending on whether the OR-2 address is odd or even, to clear the memory location.

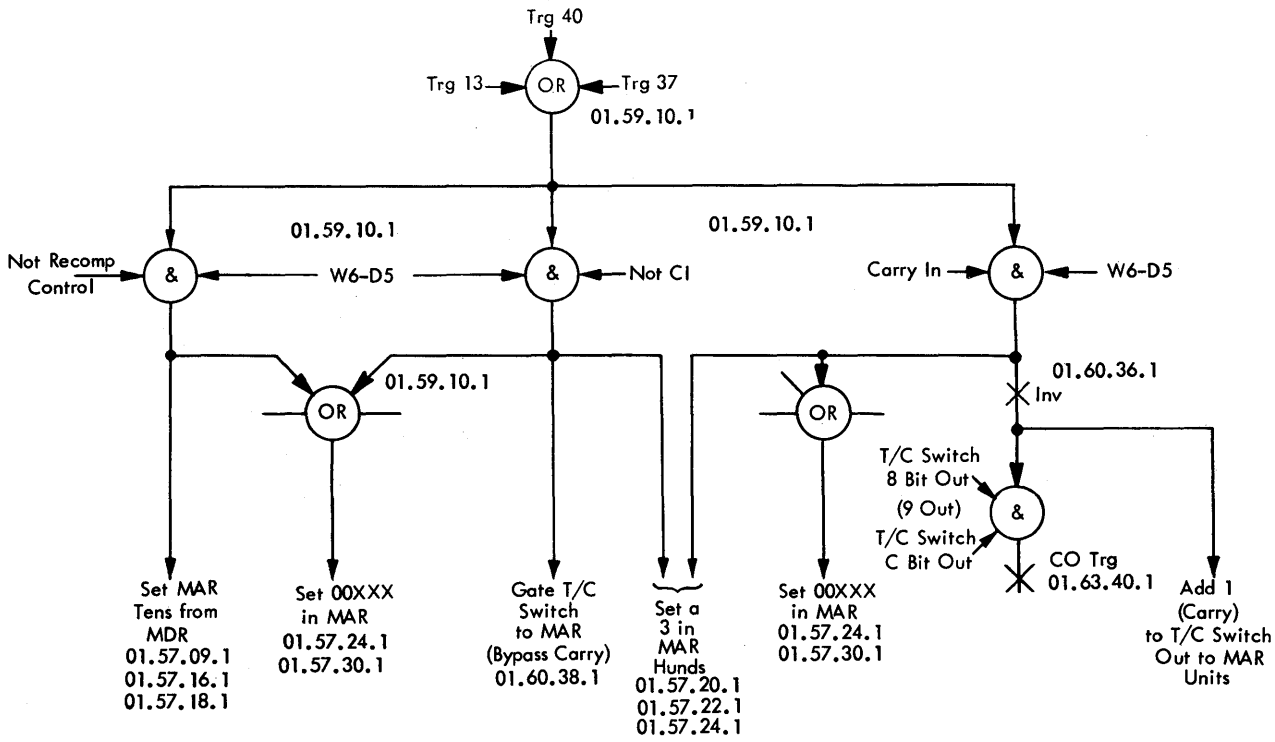



Figure 13-7. Set MAR Add Table Address

3. Write back OR-2 decremented.
4. Set an F-bit in MDR on first add cycle and first recomp cycle if H/P trigger is OFF (minus sign).
5. Clear the F-bit on first add cycle if H/P trigger is ON (plus sign) and add table digit contains a carry.
6. Set an F-bit in MDR for field definition on the add cycle and recomp cycle in which Field Mark No. 2 trigger is turned on.
7. Clear F-bit (carry) after first add cycle and before the add cycle in which Field Mark No. 2 trigger is turned on.
8. Transfer MDR to MBR.
9. Turn on Carry In trigger if Carry Out trigger is ON.
10. Turn on Trigger 11 if neither Field Mark No. 1 nor Field Mark No. 2 has been reached to repeat the four memory cycles (Triggers 11, 12, 13 and 14) for the next higher-order digits.
11. Turn on Trigger 21 if Field Mark No. 1 has been reached and Field Mark No. 2 has not.
12. Enter I-cycle for next instruction if Field Mark No. 2 has been reached and recomp is not necessary.

For recomp:

13. Turn on Trigger 21 and First Cycle trigger for the first recomp cycle.
14. Turn on Trigger 23 after the first recomp cycle if Field Mark No. 2 has not been reached.
15. Enter I-cycle for next instruction if Field Mark No. 2 has been reached.

Trigger 21 (01.60.31.1).

Not recomp: (Replaces Trigger 11 after Field Mark No. 1 has been reached.)

1. Block MAR reset to prevent VRC error.
2. Set zero in D/B register units. (This will provide zeros in place of the Q-field digits previously set in D/B register units by Trigger 11.) The D/B register units was reset during Trigger 13 time.

Recomp: (Replaces Trigger 11 on first recomp cycle.)

1. Transfer OR-3 (address of units position of P-field) into OR-2.
2. Reset OFF Field Mark No. 1 trigger.
3. Reset OFF Field Mark No. 2 trigger.
4. Turn on Recomp trigger.

Trigger 23 (01.60.32.1). This trigger is used only if a recomplement is required (replaces Trigger 11 or 21 for first memory cycle of second and succeeding recomp cycles).

1. Block MAR reset to prevent VRC error.
2. Turn on Trigger 12.

## ADD IMMEDIATE (CODE 11 - AM)

Sequence block diagrams for this operation are shown in Figures 13-3 and 13-4. Function charts for this operation are shown in the Instructional System Diagrams on pages 23 and 24.

### Objective

Add the field whose units position is the $Q_{11}$ digit of the add immediate instruction to the field at the P-address (OR-2), and store the algebraic sum at the P-address (OR-2) and successively lower memory locations.

### Functions

The Add Immediate-Code 11 operation differs from the Add-Code 21 operation only in the method of setting the Q-field address in OR-1 during the I-cycle. See Add Code 21.

### Auxiliary Triggers

See Add Code 21.

### E-Timer Trigger Objectives

See Add Code 21

## SUBTRACT (CODE 22 - S)

Sequence block diagrams for this operation are shown in Figure 13-8 and 13-9. Function charts for this operation are shown in the Instructional System Diagrams on pages 23 and 24.

### Objective

Subtract the field at the Q-address (OR-1) from the field at the P-address (OR-2), and store the algebraic difference at the P-address (OR-2) and successively lower memory locations.

### Functions

The location of the subtrahend (Q-field) is specified by OR-1. The location of the minuend (P-field) is specified by OR-2. The algebraic differences are stored in the P-field specified by OR-2. The Q-field remains unchanged. Minimum field length for either the P or Q-field is two digits.

Four memory cycles are required for the development of each digit in the algebraic difference as follows:

1. One digit of the Q-field is read from memory per OR-1 to the units position of the D/B register (Trigger 11).
2. The corresponding digit of the P-field is read from memory per OR-2 to MDR (Trigger 12).
3. The P-field digit is transferred from MDR to the tens position of MAR.

NOTE: The Q-field digit may be complemented before it is placed in MAR, depending upon the signs of the P and Q-fields.

This manufactured address with a "3" placed into the hundreds position of MAR (Figure 13-7) is used to read the 1-digit difference from the add table, in memory, Figure 13-1 to MDR (Trigger 13).

4. The 1-digit difference is then written back into memory from MDR to the correct digit position (per OR-2) replacing the P-field digit (Trigger 14).

Two types of carries can result from a subtract operation.

1. A carry resulting from the subtraction of two digits is noted by a flag bit with the appropriate 1-digit difference in the add table. This flag bit turns on the Carry-Out trigger.
2. A carry resulting from the addition of a previous carry to a "9" output to the T/C switch is noted by turning on the Carry-Out trigger.

   Detection of a carry (Carry-Out trigger ON) sets a logical path for the next Q-field digit so that it is increased by one before it is used to address the add table in the next subtract cycle.

   Recomplement is required for any subtract operation where the signs of the P and Q-fields are initially the same and the absolute value of the Q-field.

Subtraction proceeds serially, one digit at a time, building up partial differences from the low-order to the high-order digit of the difference field until the

$\overline{082}$ (+)
$\overline{54}$ (+)

082
946
C.O.←028

No Recomp on Carry Out

$\overline{082}$ (-)
$\overline{54}$ (+)

082
54
136

No Recomp on TRUE

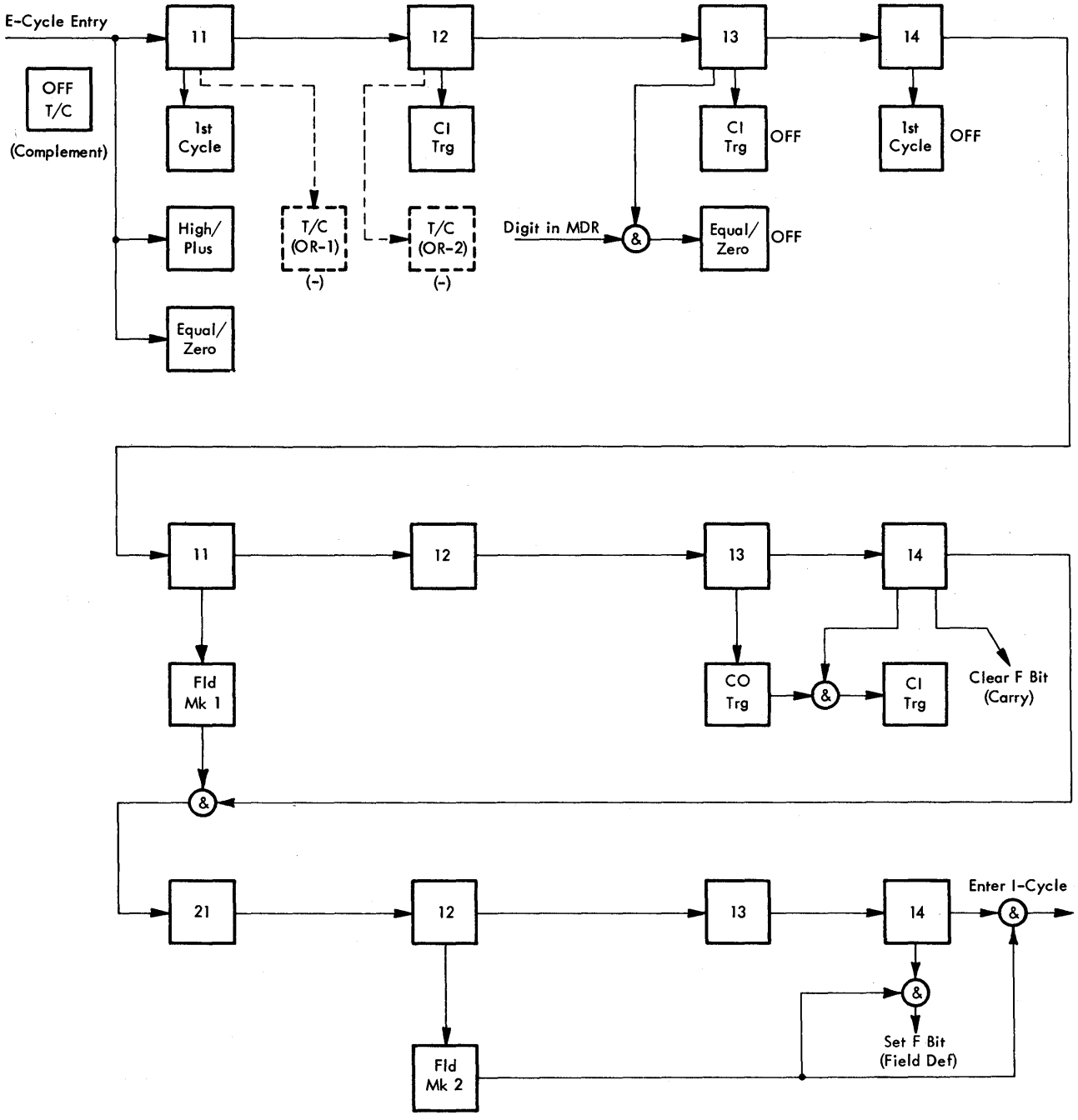



Figure 13-8. Subtract - Code 22/12

operation is terminated by a flag bit, (Field Mark No. 2), in the high-order position of the P-field. The high-order digit of the difference is marked by storing a flag bit. The sign of the difference is marked by the presence or absence of a flag bit in the units position of the difference. A flag bit indicates minus sign (-). No flag bit indicates plus sign (+).

The number of digits in the difference is equal to the number of digits in the P-field. For a complete difference to be formed, the number of digits in the P-field must be greater than or equal to the number of digits in the Q-field. If this rule is violated, the overflow indicator is turned on and the subtraction is performed using only as many Q-field digits as there are positions in the P-field. (The extra digits in the Q-field are not used.) The algebraic difference of the two equal length fields is then obtained.

Resulting Indicator Conditions

1. The H/P indicator is ON if the difference is positive and is OFF if the difference is negative or zero.
2. The E/Z indicator is ON if the difference is zero and is turned off if the difference is not zero.
3. The overflow indicator is turned on if an overflow occurs; the overflow digit is lost. If the overflow indicator is ON as a result of a previous arithmetic operation, a no overflow condition of this subtract instruction will not turn it off.

NOTE: Once the H/P or E/Z indicators are turned on or off by an arithmetic or compare operation they will retain that state until the next arithmetic or compare operation is executed (unless the Reset key on the console is pressed which turns off these indicators). Testing them with a branch indicator or branch no indicator instruction has no effect on their state. The overflow indicator will be turned off only by testing it with a branch indicator or branch no indicator instruction (or by pressing the Reset key on the console).

Auxiliary Trigger Status

True/Complement (T/C)Trigger (01.63.20.1).

1. Turned on by Trigger 1 during I-cycle.
2. Turned off by the E-cycle Entry trigger during Trigger 8 time when a subtract or subtract immediate operation code has been set in the Op register and therefore will be off when E-cycle is entered.
3. Turned on during Trigger 11 time on first add cycle if Q-field is negative.
4. Status changed during Trigger 12 time on first add cycle if P-field is negative.
5. Operation will be true if T/C trigger is ON at the end of Trigger 12 time of the first add cycle, and complement if T/C trigger is OFF. Complement operation requires that the Q-field be complemented (10's complement in units position; 9's complement in other positions) for the development of add table addresses.

Other Auxiliary Triggers. Refer to Add-Code 21 for status of other auxiliary triggers.

Sign Analysis

The sign analysis chart, Figure 13-10 shows the operation of the T/C, H/P, and E/Z triggers for a subtract operation. The chart shows the conditions requiring a recomplement operation and the conditions causing an overflow.

E-Timer Trigger Objectives

Trigger 11 (01.60.11.1).

1. Read out memory per OR-1 and store the digit in D/B register units.
2. Write back OR-1 decremented.
3. Turn on Field Mark No. 1 trigger after first cycle when end of Q-field is reached.
4. Turn on T/C trigger during first cycle if Q-field is negative.

Trigger 12 (01.60.12.1).

1. Read out of memory per OR-2 and store the digit in MDR.
2. Write back OR-2 bypassed (to save address for writing the difference digit into memory during Trigger 14 tim3).
3. Change the status of the T/C trigger on first cycle if P-field is negative.
4. Turn off H/P trigger on first cycle if P-field is negative.
5. Turn on Field Mark No. 2 trigger after first cycle when end of P-field is reached.

For complement operation or recomp:

6. Turn on the Carry In trigger during first cycle to obtain 10's complement in units position.

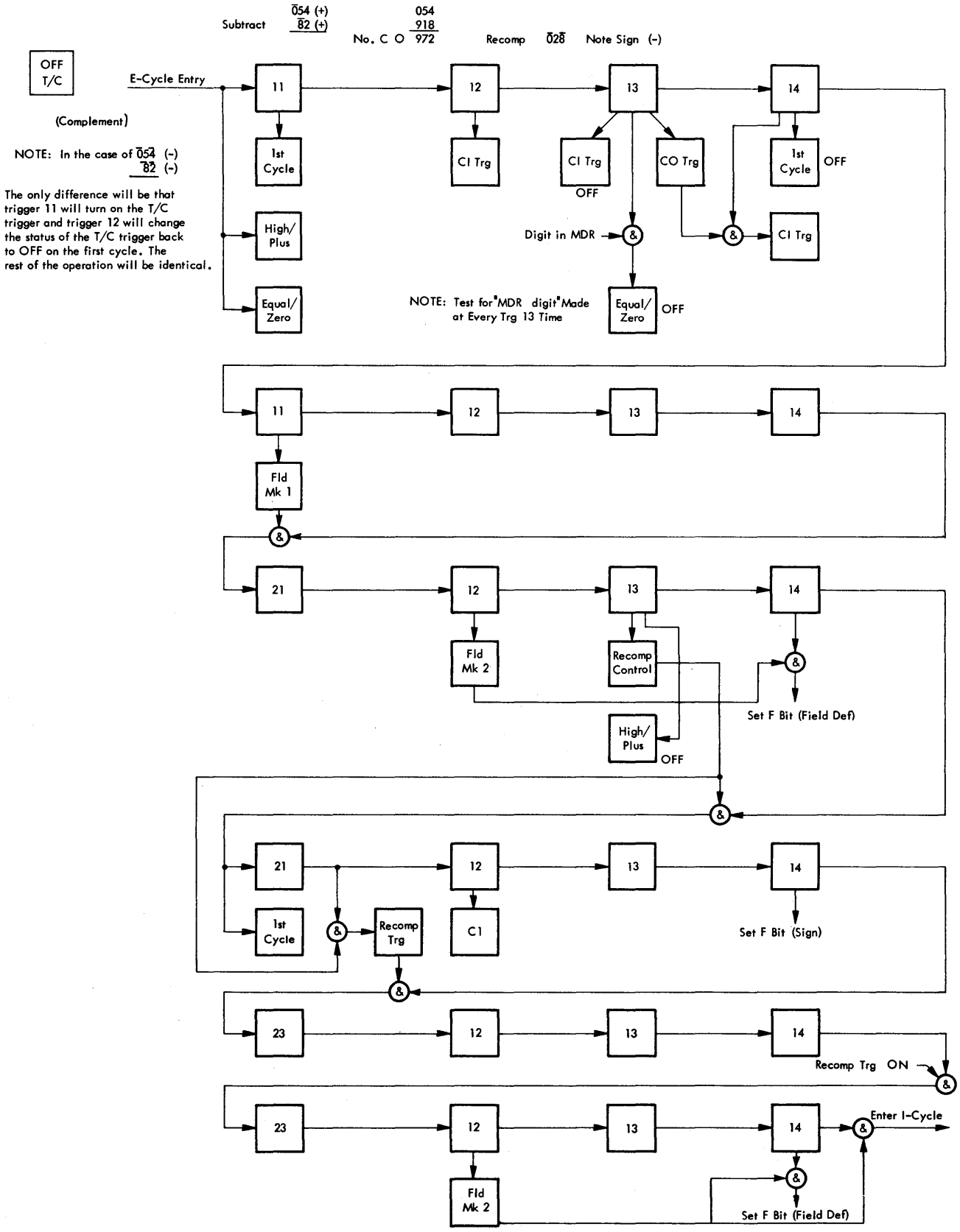



Figure 13-9. Subtract with Recomplement

| | | SUBTRACT | | | |
|---|---|---|---|---|---|
| Sign of P Field (Minuend) | | + | + | — | — |
| Sign of Q Field (Subtrahend) | | + | — | + | — |
| Set High/Plus Trg (Store Sign of P Field) | | ON<br>+ | ON<br>+ | OFF<br>— | OFF<br>— |
| Set T/C Trigger (True or Comp Op) | | OFF<br>Comp | ON<br>True | ON<br>True | OFF<br>Comp |
| If Carry Out | | NO<br>Recomp | Set<br>Overflow | Set<br>Overflow | NO<br>Recomp |
| If No Carry Out | | Recomp. | NO<br>Recomp | NO<br>Recomp | Recomp |
| Resulting Sign | No Recomp | + | + | — | — |
| | Recomp | — | | | + |
| NOTES: If the Equal/Zero Trigger is ON (Zero Difference) when the I-Cycle following the Subtract Operation is Entered, the High/Plus Trigger is turned OFF (- Sign) | | T/C turned ON and then OFF During I-Cycle<br>High/Plus and Equal/Zero turned ON in Parallel with Trg 11 at E-Cycle Entry Time | | | |

Figure 13-10. Sign Analysis Chart for Subtraction

For recomp:

7. Set D/B register units from MDR.

Other E-Timer Triggers. Refer to Add-Code 21 for objectives of other E-timer triggers. Other E-timer triggers used are: 13, 14 and 21 (also 23 if recomplement is required).

## SUBTRACT IMMEDIATE (CODE 12 - SM)

Sequence block diagrams for this operation are shown in Figures 13-8 and 13-9. Function charts for this operation are shown in the Instructional System Diagrams on pages 23 and 24.

### Objective

Subtract the field whose units position is the $Q_{11}$ digit of the subtract immediate instruction from the field at the P-address (OR-2), and store the algebraic difference at the P-address (OR-2) and successively lower memory locations.

### Functions

The Subtract Immediate-Code 12 operation differs from the Subtract-Code 22 operation only in the method of setting the subtrahend (Q-field) address in OR-1, during the I-cycle. See Subtract-Code 22.

Auxiliary Triggers

See Subtract-Code 22.

E-Timer Triggers

See Subtract-Code 22.

## COMPARE (CODE 24 - C)

Sequence block diagrams for this operation are shown in Figures 13-11, 13-12, 13-13, and 13-14. Functional charts for this operation are shown in the Instructional System Diagrams on pages 23 and 24.

### Objective

Compare the field at the Q-address (OR-1) to the field at the P-address (OR-2) to determine if the P-field is algebraically higher than, equal to, or less than, the Q-field with signs taken in consideration.

### Functions

The high, equal or low condition of the P-field specified by OR-2 relative to the Q-field specified by OR-1 is established, considering signs. Both fields remain unchanged after the comparison has been completed.

Four memory cycles are required to compare each position of the two fields as follows:

1. One digit from the Q-field is read from memory per OR-1 to the units position of the D/B register (Trigger 11).
2. The corresponding digit of the P-field is read from memory per OR-2 to MDR (Trigger 12).
3. The P-field digit is transferred from MDR to the tens position of MAR and the digit stored in the D/B register is complemented (tens complement in units position; nines complement in other positions) and placed in the units position of MAR. This manufactured address with a "3" placed into the hundreds position of MAR (Figure 13-7) is used to read the 2-digit difference from the add table in memory, Figure 13-1, to MDR (Trigger 13).
4. The difference digit in MDR is not written back into memory and therefore is lost. The fourth cycle decrements the P-address (OR-2) in preparation for the next compare cycle (trigger 14).

The comparison proceeds serially, one digit at a time, from low-order to high-order digits of the compared fields until the operation is terminated by a flag bit (Field Mark No. 2) in the high-order position of the P-field. The comparison is performed internally by subtraction of the Q-field from the P-field. However, the digits of the difference are lost.

If the signs of the two fields are initially different and one or both of the fields contains a significant digit (not zero) the compare operation is terminated after a digit in one or both fields has been interrogated. The field whose sign is positive is declared high. A comparison of zeros with unlike signs results in an equal comparison (the 1620 considers a +0 as being equal to a -0).

A comparison may be executed on two fields containing a random mixture of alphameric and special characters or on two numerical fields. A legitimate comparison may not be executed on an alphameric field and a numerical field without first expanding the numerical field to the alphameric format (or vice versa).

For a complete comparison to be performed, the number of digits in the P-field must be greater than or equal to the number of digits in the Q-field (unless their signs are not alike). If this rule is violated, the overflow indicator is turned on and the extra digits in the Q-field are not used; however, the result of the comparison is correct to the point where comparison is terminated.

Minimum length for either of the fields being compared is two digits.

### Resulting Indicator Conditions

1. The H/P indicator is ON if the P-field is higher than the Q-field and is OFF if not higher with signs taken into consideration.
2. The E/Z indicator is ON if the P-field is equal to the Q-field and is OFF if not equal.
3. The overflow indicator is turned on if an overflow occurs. If the overflow indicator is ON as the result of a previous arithmetic operation, a no overflow condition of this compare instruction will not turn it off.

NOTE: Once the H/P or E/Z indicators are turned on (or off) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed (unless the Reset key on the console is pressed which turns off these indicators). Testing them with a branch indicator or branch no indicator instruction has no effect on their state. The overflow indicator will be turned off only by testing it with a branch indicator or branch no indicator instruction (or by pressing the Reset key on the console).

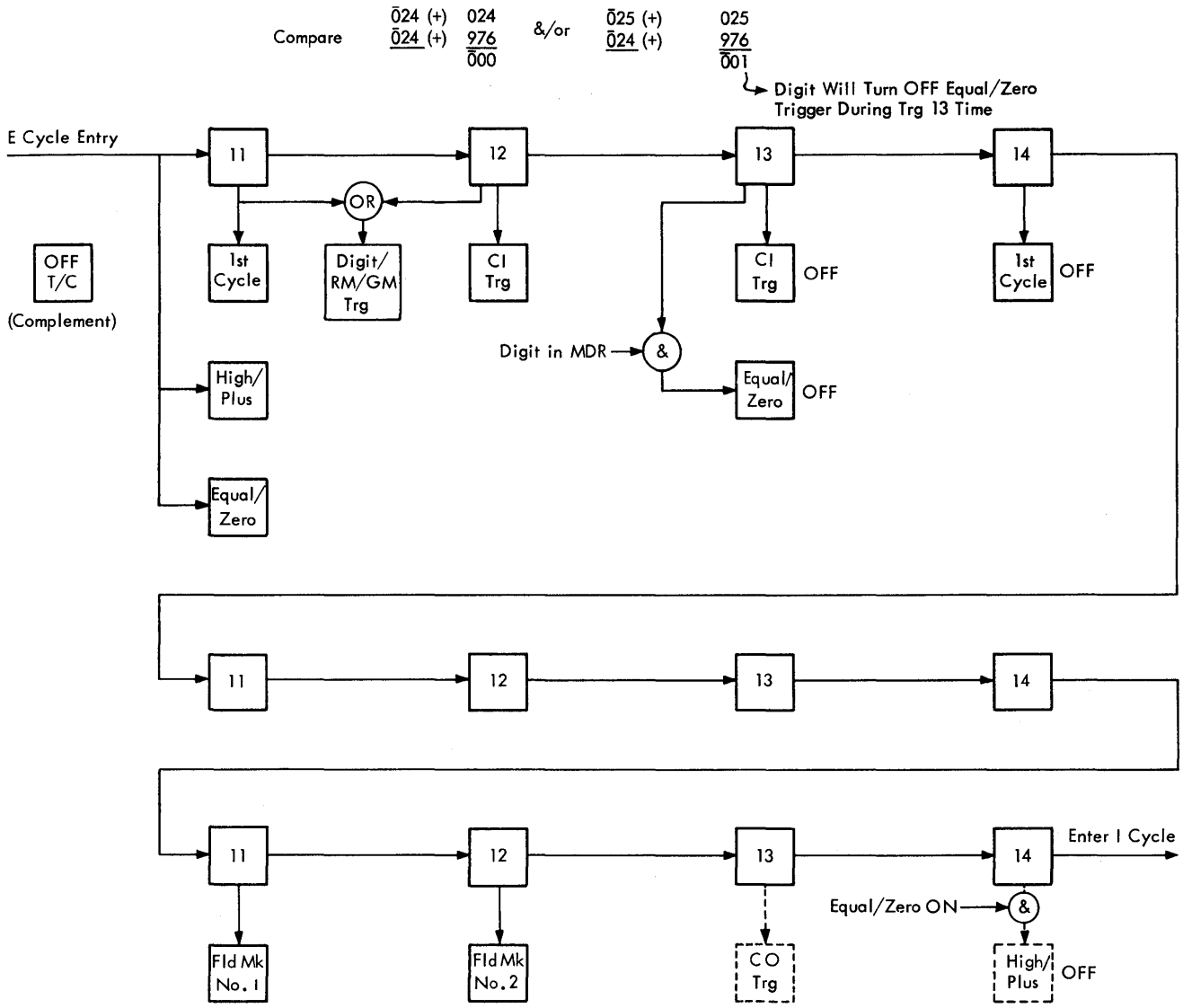



Figure 13-11. Compare - Code 24/14 (Plus Signs)

## Auxiliary Trigger Status

True/Complement Trigger (01.63.20.1).

1. Turned on by Trigger 1 during I-cycle.
2. Turned off by the E-cycle Entry trigger during Trigger 8 time when a compare or compare immediate operation code has been set in the Op register and therefore will be off when E-cycle is entered.
3. Turned on during Trigger 11 time on first compare cycle if Q-field is negative.
4. Status changed during Trigger 12 time on first compare cycle if P-field is negative.
5. The T/C trigger must be OFF (designating a complement operation) at the end of Trigger 12 time if a complete compare operation is to take place. Complement operation requires that the Q-field be complemented (tens complement in units position; nines complement in other positions) for the development of add table addresses.
6. The T/C trigger will be ON (designating a true operation) at the end of Trigger 12 time if the P and Q-fields have unlike signs.

Decrement Trigger (01.60.05.1).

1. Turned on (decrement) during Trigger 8 time of the preceding I-cycle.
2. Will remain ON until the next I-cycle is entered.

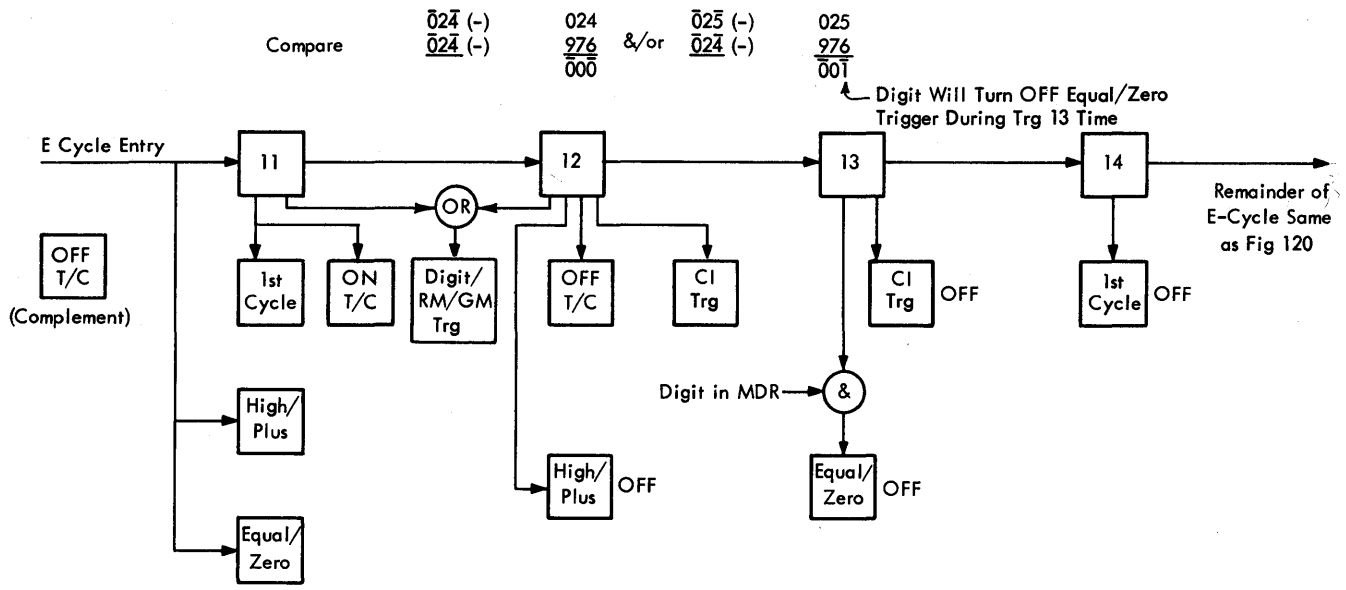



Figure 13-12. Compare - Code 24/14 (Minus Signs)

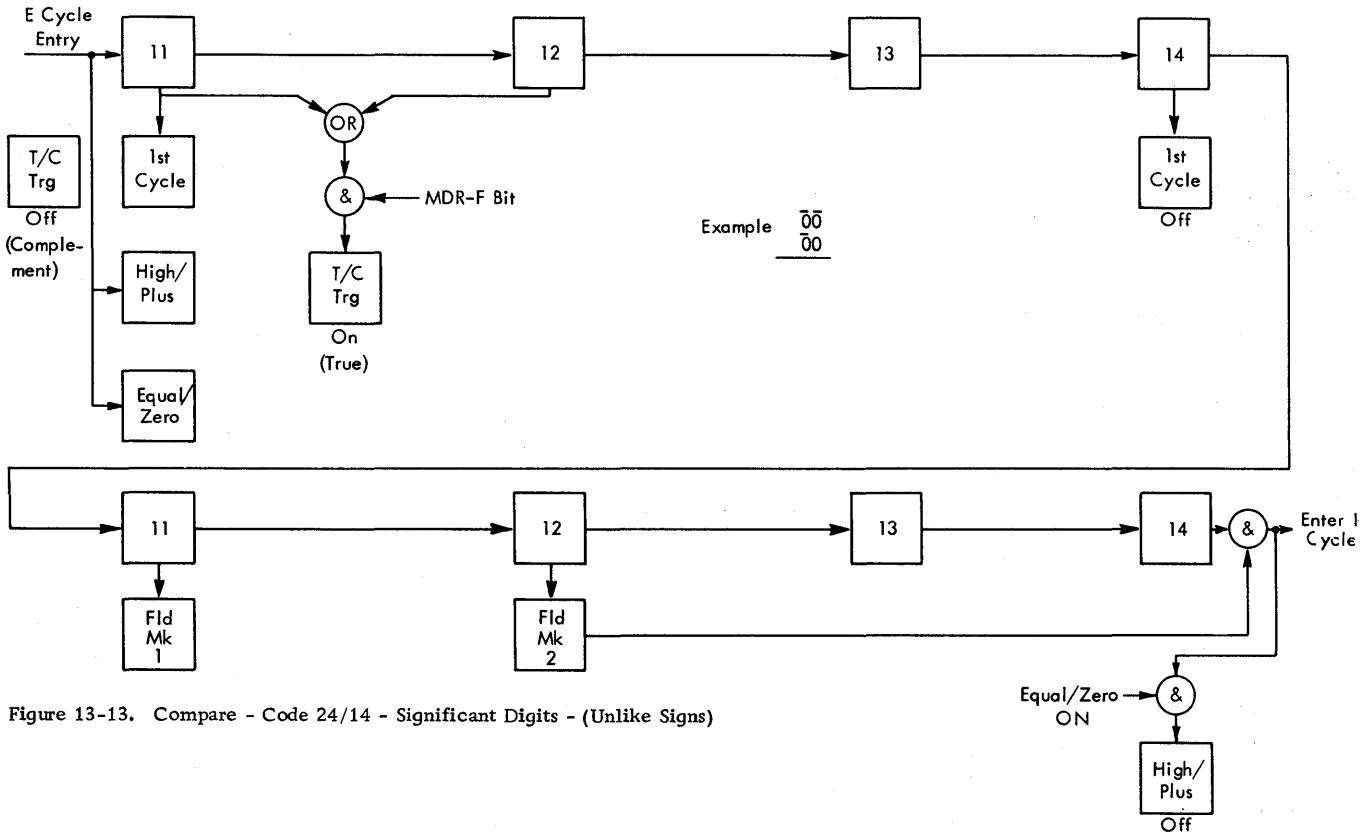



Figure 13-13. Compare - Code 24/14 - Significant Digits - (Unlike Signs)

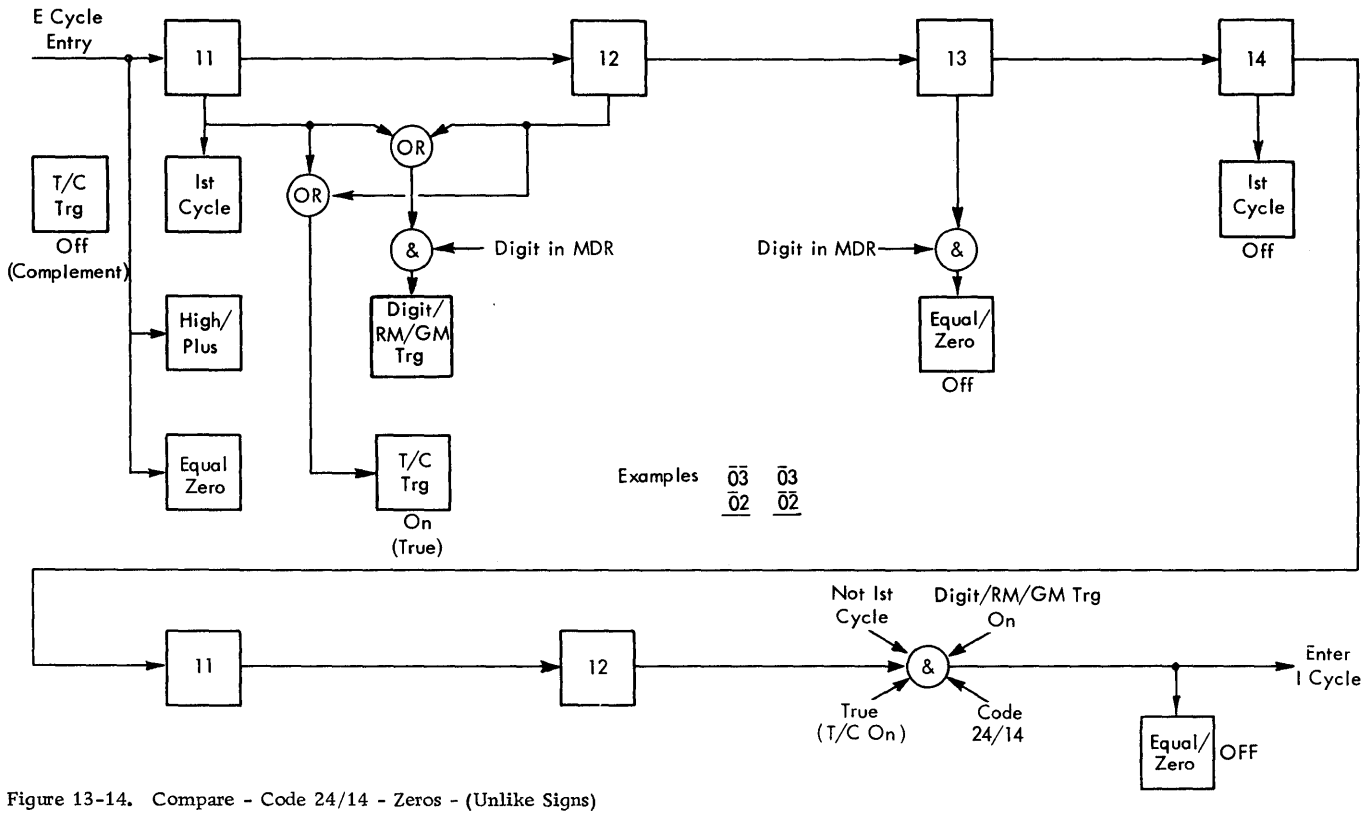



Figure 13-14. Compare - Code 24/14 - Zeros - (Unlike Signs)

First Cycle Trigger (01.63.10.1).

1. Turned on by Trigger 11 when E-cycle is entered.
2. Turned off at end of Trigger 14 time on first compare cycle.

High/Plus Trigger (01.60.40.1).

1. Turned on when E-cycle is entered.
2. Turned off during Trigger 12 time on first compare cycle if P-field is negative.
3. Status changed during Trigger 13 time of the compare cycle in which Field Mark No. 2 is reached if there is not a carry out.
4. Turned off by Trigger 14 when I-cycle is entered if the E/Z trigger is ON (comparison of zeros).

Equal/Zero Trigger (01.60.41.1).

1. Turned on when E-cycle is entered.
2. Turned off during Trigger 13 time if add table digit is other than zero.
3. Turned off during Trigger 12 time if the P and Q-fields have unlike signs, if it is not first cycle, and if a significant digit and a zero, or significant digits (not zeros) are being compared.

Field Mark No. 1 Trigger (01.63.30.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Cannot be turned on during first compare cycle (Q-field must be a minimum of two digits).
3. Will be turned on during Trigger 11 time on compare cycle in which end of Q-field is reached.

Field Mark No. 2 Trigger (01.63.30.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be OFF when E-cycle is entered.
2. Cannot be turned on during first compare cycle (P-field must be a minimum of two digits).
3. Will be turned on during Trigger 12 time on compare cycle in which end of P-field is reached.

Carry Out Trigger (01.63.40.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Reset OFF by Triggers 11, 21, and 23.
3. Turned on during Trigger 13 time on compare cycles where the add table digit in MDR contains an F-bit (carry).
4. Turned on during Trigger 13 time on compare cycles where the output of the T/C switch is a "9" and the Carry In trigger is on.

Carry In Trigger (01.63.40.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Turned on during Trigger 12 time on first compare cycle to obtain tens complement in units position.
3. Reset OFF during Trigger 13 time.
4. Turned on by Trigger 14 if the Carry Out trigger is ON.

D/RM/GM Trigger (01.63.50.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Turned on during Trigger 11 time (Q-field) if MDR contains a digit (not zero).
3. Turned on during Trigger 12 time (P-field) if MDR contains a digit (not zero).

Sign Analysis

The sign analysis chart, Figure 13-15, shows the operation of the T/C, H/P, and E/Z triggers for a compare operation

E-Timer Trigger Objectives

Trigger 11 (01.60.11.1).

1. Read out of memory per OR-1 (Q-field) and store the digit in D/B register units.
2. Write back OR-1 decremented.
3. Turn on Field Mark No. 1 trigger after first cycle when end of Q-field is reached.
4. Turn on T/C trigger during first cycle if Q-field is negative.
5. Turn on D/RM/GM trigger if MDR contains a significant digit (not zero).

Trigger 12 (01.60.12.1).

1. Read out of memory per OR-2 (P-field) and store the digit in MDR.
2. Write back OR-2 bypassed.
3. Change the status of the T/C trigger on first cycle if P-field is negative.
4. Turn off H/P trigger on first cycle if P-field is negative.
5. Turn on Field Mark No. 2 trigger on first cycle when end of P-field is reached.

| | Digits or Zeros | | Digits | | Zeros | |
|---|---|---|---|---|---|---|
| OR-2 (P-Field) | + | − | + | − | + | − |
| OR-1 (Q-Field) | + | − | − | + | − | + |
| T/C | OFF (Complement) | OFF (Complement) | ON (True) | ON (True) | ON (True) | ON (True) |
| High/Plus | ON (+) Turn OFF if "P" is Lower than "Q" | OFF (−) Turn ON if "P" is Higher than "Q" | ON (+) | OFF (−) | ON Turned OFF When I-Cycle is Entered | OFF |
| Equal/Zero | Leave ON if Diff is Zero Turn OFF if Not | Leave ON if Diff is Zero. Turn OFF if Not. | Turn OFF | Turn OFF | ON | ON |

Figure 13-15. Sign Analysis Chart for Compare

6. Turn on the Carry In trigger during first cycle to obtain tens complement in units position.
7. Turn on D/RM/GM trigger if MDR contains a significant digit (not zero).
8. Enter I-cycle for next instruction in sequence if it is not the first cycle and a significant digit (not zero) in fields with unlike signs is compared. (I-cycle entry under these conditions turns off the E/Z trigger).

Trigger 13 (01.60.13.1).

1. Develop and set add table address in MAR (Figure 13-7).
2. Read out of memory per add table address and store the digit in MDR.
3. Turn on the Carry Out trigger if MDR contains an F-bit (carry).
4. Turn on the Carry Out trigger if the output of the T/C switch is a "9" and the Carry In trigger is ON.
5. Reset D/B register units. (See Trigger 21 Objective 1.)
6. Change status of H/P trigger if there is no carry out on the cycle in which Field Mark No. 2 is reached.

Miscellaneous:

7. Turn on the Overflow trigger if the P-field is shorter than the Q-field.
8. Turn off E/Z trigger if add table digit is not a zero.

Trigger 14 (01.60.14.1).

1. Read into MAR from OR-2 (P-field) and write back OR-2 decremented.
2. Turn on Carry In trigger if Carry Out trigger is ON.
3. Turn on Trigger 11 if neither Field Mark No. 1 nor Field Mark No. 2 has been reached and repeat the four memory cycles (Triggers 11, 12, 13 and 14) for the next higher-order digits.
4. Turn on Trigger 21 if Field Mark No. 1 has been reached and Field Mark No. 2 has not.
5. Enter I-cycle for next instruction in sequence if Field Mark No. 2 has been reached.

Trigger 21 (01.60.31.1).

NOTE: Trigger 21 replaces Trigger 11 for first memory cycle after Field Mark No. 1 has been reached.

1. Set zero in D/B register units. (This will provide zeros in place of the Q-field digits previously set into D/B register units by Trigger 11.) The D/B register position is reset during Trigger 13 time.

## COMPARE IMMEDIATE (CODE 14 - CM)

Sequence block diagrams for this operation are shown in Figures 13-11, 13-12, 13-13 and 13-14. Function charts for this operation are shown in the Instructional System Diagrams on pages 23 and 24.

### Objective

Compare the field whose units position is the $Q_{11}$ digit of the compare immediate instruction to the field at the P-address (OR-2) to determine if the field at the P-address is higher than equal to or less than the field in the Q-part of the instruction, signs considered.

### Functions

The Compare Immediate-Code 14 operation differs from the Compare-Code 24 operation only in the method of setting the OR-1 address during the I-cycle. See Compare-Code 24.

### Auxiliary Triggers

See Compare - Code 24.

### E-Timer Triggers

See Compare - Code 24.

## MULTIPLY (CODE 23 - M)

A sequential flow diagram for multiplication is shown in Figure 13-16. A sequence block diagram for this operation is shown in Figure 13-17. Function charts and sequential flow diagrams for this operation are shown in the Instructional System Diagrams on pages 25 through 31.

### Objective

Multiply the field at the P-address (OR-2) by the field at the Q-address (OR-1), and store the algebraic product at location 00099 and successively lower memory locations.

### Functions

The location of the multiplier is specified by OR-1 (Q-field). The location of the multiplicand is specified

by OR-2 (P-field). Minimum field length for either the multiplier or the multiplicand is two digits. Both the multiplier and the multiplicand remain unchanged when multiplication is completed.

Multiplication proceeds serially, one digit at a time, building up partial products from the low-order to the high-order digit of the product field. The operation is terminated when the high-order digit of the multiplicand field has been multiplied by the high-order digit of the multiplier field. The high-order position of the product is marked by storing a flag bit. A negative product is marked by a flag bit in the units position; absence of a flag bit indicates a positive product.

The number of digits in the product is limited only by available memory space, and is equal to the sum of the number of digits in the multiplier and in the multiplicand. Twenty positions for the product area in memory (00080-00099) are cleared to zeros at the beginning of the multiply operation. The length of the product may exceed 20 digits if a program is written to clear to zero the required number of locations in excess of 20 before the multiply instruction is executed. If the product exceeds 100 digits, the 101st digit (high-order end of product) will be placed in location 19999 and the remaining digits in successively lower memory locations.

A minimum of eight memory cycles are required to develop and store, in the product area of memory, each digit of the product as follows:

1. One digit of the multiplier is read from memory per OR-1 to the Multiplier/Quotient(M/Q) register where it is stored for use with each digit of the multiplicand.
2. The multiplicand digit is read from memory per OR-2 to MDR.
3. The multiplicand digit is transferred from MDR to the tens position of MAR and the multiplier digit is passed through a doubler circuit to form two digits which are entered into the hundreds and units positions of MAR. (The digit entering the hundreds position is increased by one before being placed in MAR.) See Figure 13-18. This manufactured address is used to read the 2-digit product (whose digits are in reverse order) from the multiply table stored in memory in locations 00100 through 00299, (Figure 13-2). The 2-digit product is stored (with digits in the correct order) in the D/B register.
4. The appropriate digit is read from the product area in memory per PR-2 (PR-1 on the first cycle associated with each new multiplier digit) to MDR.
5. The digit in the units position of the D/B register is transferred to the units position of MAR and the product area digit in MDR is transferred to the tens position of MAR. This manufactured address with a "3" forced into the hundreds position of MAR is used to read the 1-digit sum from the add table in memory to MDR (Figure 13-1).
6. The 1-digit sum is then written back into memory from MDR to the appropriate position of the product area per PR-2. PR-2 is written back decremented.
7. The next higher-order digit is read from the product area per PR-2 to MDR.
8. The digit in the tens position of the D/B register is transferred to the units position of the digit register and from there to the units position of MAR. The product area digit in MDR is transferred to the tens position of MAR. This manufactured address with a "3" forced into the hundreds position of MAR is used to read the 1-digit sum from the add table to MDR.
9. The 1-digit sum is then written back into memory from MDR to the appropriate position of the product area per PR-2.
10. Carries, if any, are added to the partial product before the next multiplication cycle begins. See chart of Trigger Objectives and Sequence, Figure 13-16.

## Resulting Indicator Conditions

1. The H/P indicator is ON if the product is positive and OFF if the product is negative or zero.
2. The E/Z indicator is ON if the product is zero and is OFF if the product is not zero.

NOTE: Once the H/P or E/Z indicators are turned on or off by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed (unless the Reset key on the console is depressed which turns these indicators off). Testing them with a branch indicator or branch no indicator instruction has no effect on their state.

## Storage Register Functions

OR-1. At the end of the I-cycle, OR-1 contains the address of the units position of the multiplier. The units multiplier digit is read out of memory and stored in the M/Q register. OR-1 is then decremented 1 to prepare for reading out the next higher-

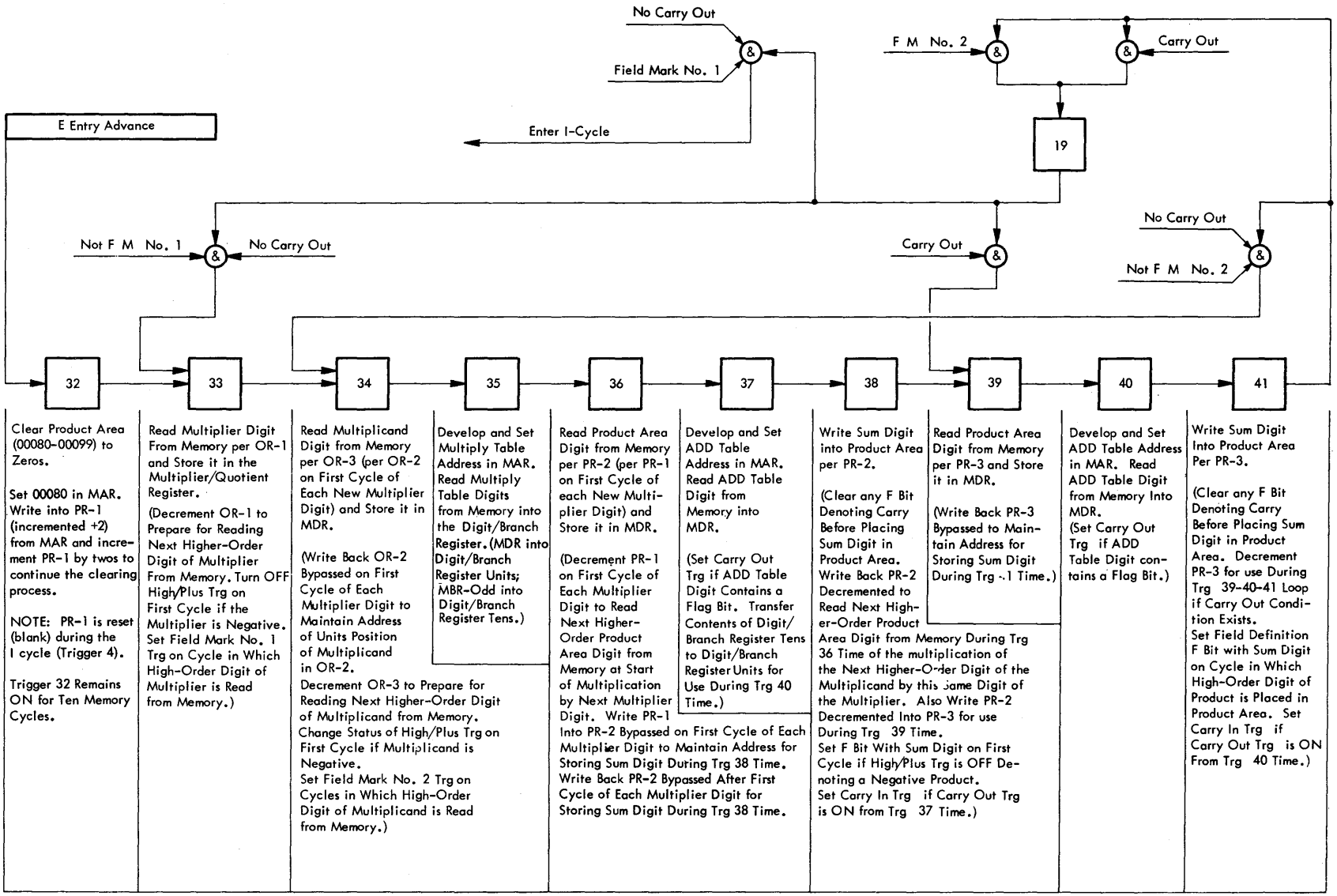



Figure 13-16. Multiply - Sequential Flow Diagram

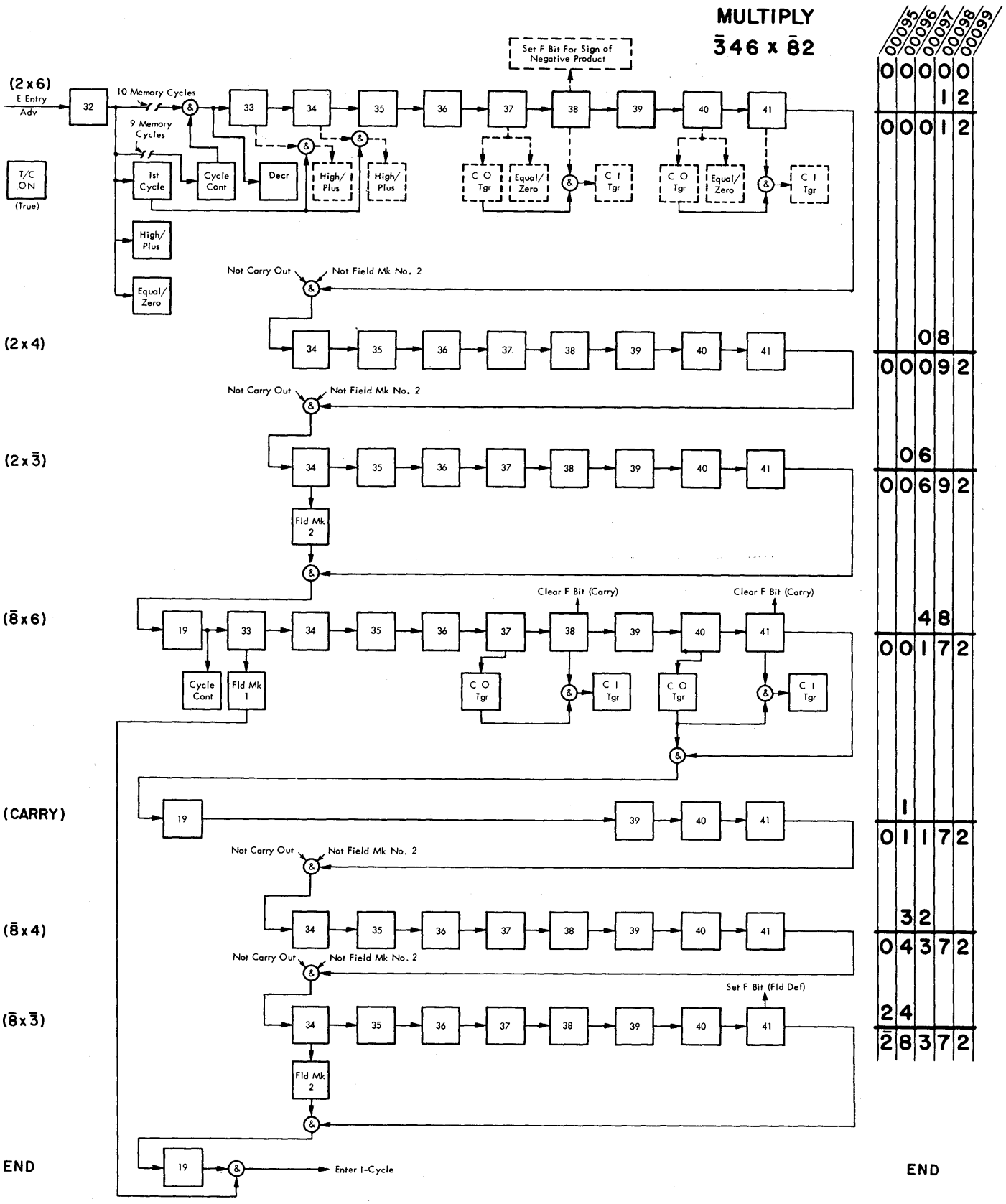



Figure 13-17. Multiply - Code 23/13

order multiplier digit. Each multiplier digit is used for all multiplicand digits before the next multiplier digit is obtained. See Trigger 33.

OR-2. At the end of the I-cycle, OR-2 contains the address of the units position of the multiplicand. OR-2 retains that address so that as each new multiplier digit is obtained, multiplication can start with the units digit of the multiplicand. See Trigger 34.

OR-3. At the end of the I-cycle OR-3 contains the address of the units position of the multiplicand. OR-2 is used to address the units position of the multiplicand and, while OR-2 is written back bypassed, OR-3 is written back decremented 1 to address the next higher-order position of the multiplicand. OR-3 is decremented 1 for each mutliplicand digit. See Trigger 34.

PR-1. This register is cleared (reset to blank) during the I-cycle, and set to 00082 on the first Trigger 32 cycle. It is then incremented 2 for the next eight Trigger 32 cycles (00098), and incremented 1 (to 00099) on the tenth Trigger cycle. PR-1 then contains the address of the units position of the product area into which the first (units) digit of the product is to be placed. PR-1 is decremented 1 for each new multiplier digit. See Triggers 32 and 36.

PR-2. This register is initially set to PR-1 (00099). PR-2 addresses the correct partial product position for the first of two add cycles that add a basic multiply-cycle result to the partial product. PR-2 is decremented 1 for each multiplicand digit. See Triggers 36 and 38.

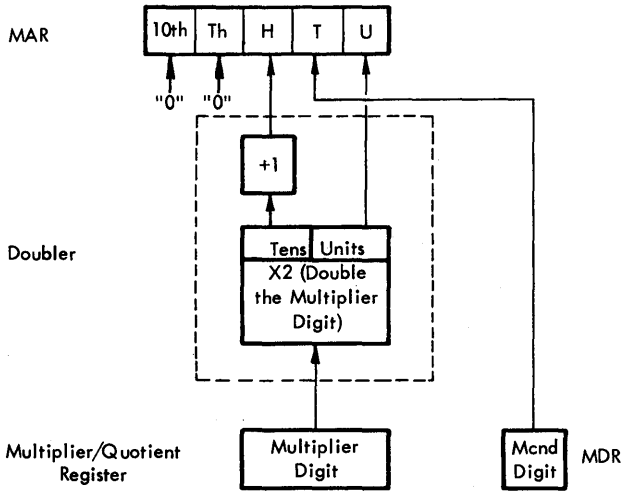



Figure 13-18. Data Flow - Multiply Table Address

PR-3. PR-3 is initially set to PR-2 (00098). PR-3 addresses the correct partial product position for the second of two add cycles that add a basic multiply-cycle result to the partial product. PR-3 is decremented 1 for each multiplicand digit and is decremented 1 to propogate (through the product area) any carries that may result from the second add cycle. See Triggers 39 and 41.

Auxiliary Trigger Status

True/Complement Trigger (01.63.20.1).

1. Turned on (true) by Trigger 1 of the I-cycle and remains ON throughout the multiply operation to provide a path for transfer of digits from the units position of the D/B register to the units position of MAR.

Decrement Trigger (01.60.05.1).

1. Turned off (increment) by Trigger 1 of the I-cycle.
2. Turned on (decrement) by Trigger 33 at end of product area clearing operation.
3. Remains ON for remainder of multiply operation.

Equal/Zero Trigger (01.60.41.1).

1. Turned on by Trigger 32.
2. Turned off during Trigger 37 or Trigger 40 time if the add table digit is other than zero.

First Cycle Trigger (01.63.10.1).

1. Turned on by Trigger 32.
2. Turned off by Trigger 39 on first multiply cycle.

High/Plus Trigger (01.60.40.1).

1. Turned on by Trigger 32.
2. Turned off during Trigger 33 time on first multiply cycle if the Q-field (OR-1) is negative.
3. Status changed during Trigger 34 time on first multiply cycle if the P-field (OR-2) is negative.
4. Status at the end of Trigger 34 time designates the sign of the product.

Cycle Control Trigger (01.62.31.1).

1. Turned on during Trigger 32 time when the address in MAR reaches 00096 to terminate the product area clearing operation.
2. Turned off by Trigger 39.
3. Turned on by Trigger 33 when the next multiplier digit is required.

Carry Out Trigger (01.63.40.1).

1. Reset OFF by Trigger 35 to ensure OFF status for entry into multiply operation.
2. Turned on during Trigger 37 or Trigger 40 time on add cycles where the add table digit in MDR contains an F-bit (carry).
3. Turned on during Trigger 40 time on add cycles where the output of the T/C switch is a "9" and a carry exists (Carry In trigger on) from the previous add cycle.
4. Reset OFF during Trigger 39 time.

Carry In Trigger (01.63.40.1).

1. Reset OFF by Trigger 1 of the I-cycle and therfore will be off when E-cycle is entered.
2. Reset OFF during Trigger 35 time.
3. Turned on by Trigger 38 or Trigger 41 if the Carry Out trigger is ON.
4. Reset OFF during Trigger 40 time.

Field Mark No. 1 Trigger (01.63.30.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Cannot be turned on during first multiply cycle (Q-field must be a minimum of two digits).
3. Turned on during Trigger 33 time on the multiply cycle in which end of Q-field (OR-1) is reached.

Field Mark No. 2 Trigger (01.63.30.1).

1. Reset OFF by Trigger 1 of the I-cycle and therefore will be off when E-cycle is entered.
2. Cannot be turned on during first multiply cycle (P-field must be a minimum of two digits).
3. Turned on during Trigger 34 time on multiply cycles in which end of P-field (OR-2) is reached.
4. Turned off by trigger 33.

E-Timer Trigger Objectives

Trigger 32 (01.62.30.1).

1. Turn on First Cycle trigger
2. Turn on H/P trigger.
3. Turn on E/Z trigger.
4. Set 00080 in MAR on first memory cycle.
5. Read out of memory per 00080, with both the even and odd sense amplifiers blocked (Block Memory SA), to clear product area memory locations 00080 and 00081.
6. Write into PR-1 the MAR address (00080) incremented +2.
7. Set C-bits into MBR-even and MBR-odd to provide zeros for the product area.
8. Write into memory per MAR address (00080) from MBR.

Trigger 32 remains on for a total of ten memory cycles during which time the 20 memory locations designated as product area (00080-00099) are set to zero. Memory locations per PR-1 are cleared two per memory cycle by incrementing +2 until 00096 and 00097 have been set to zero and 00098 written into PR-1. The Cycle Control trigger is turned on during the cycle in which 00096 is in MAR and 00098 is written back into PR-1. On the tenth memory cycle, with the Cycle Control trigger ON, 00098 is read into MAR from PR-1 and memory locations 00098 and 00099 are set to zero. The MAR address (00098) is written back into PR-1 incremented +2. PR-1 then contains 00099, which designates the location of the units position of the product area in memory.

Trigger 33 (01.62.33.1).

1. Read out of memory per OR-1 (multiplier) and store the digit in the M/Q register.
2. Write back OR-1 decremented.
3. Turn off H/P trigger during first cycle if Q-field (multiplier) is negative.
4. Set Field Mark No. 1 trigger after first cycle when end of Q-field (OR-1) is reached.
5. Turn off (reset) Field Mark No. 2 trigger.

Trigger 34 (01.62.34.1). For units position of multiplicand:

1. Read out of memory per OR-2 and store the digit in MDR.
2. Write back OR-2 bypassed.
3. Write from MAR into OR-3 decremented.

For other than units position of multiplicand:

4. Read out of memory per OR-3 and store the digit in MDR.
5. Write back OR-3 decremented.

On first multiply cycle:

6. Change status of H/P trigger if P-field (multiplicand) is negative.
7. Set Field Mark No. 2 trigger when end of multiplicand field (OR-3) is reached.

Trigger 35 (01.62.35.1).

1. Develop and set multiply table address in MAR (Figure 13-19).
2. Read out of memory per multiply table address and store, in the D/B register, the two digits that are associated with that address.
3. Turn off (reset) Carry Out and Carry In triggers.

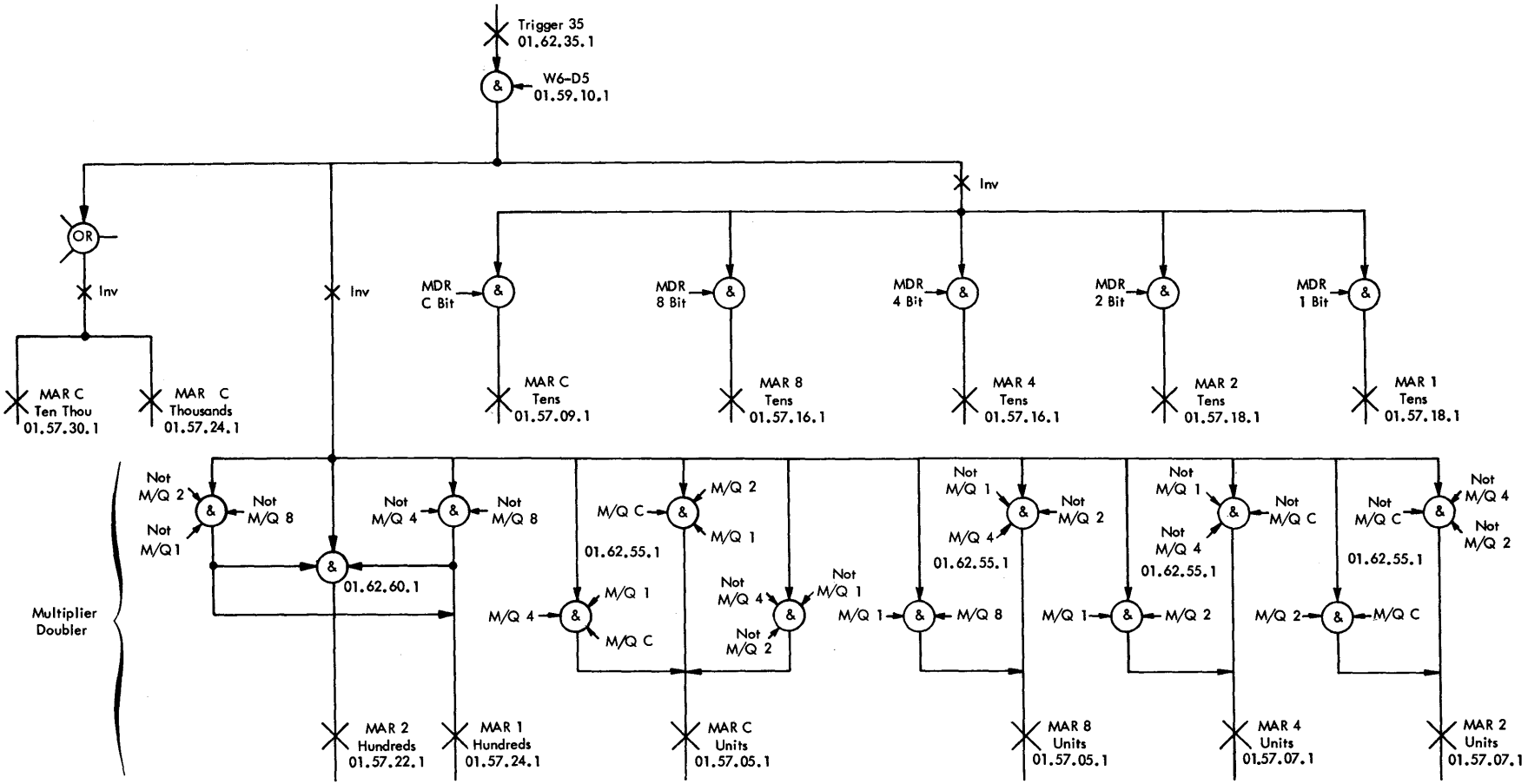



Figure 13-19. Set MAR Multiply Table Address

Trigger 36 (01.62.36.1). For units position of multiplicand:

1. Read out of memory per PR-1 (product area) and store the digit in MDR.
2. Write back PR-1 decremented and write PR-1 bypassed into PR-2.

For other than units position of multiplicand:

3. Read out of memory per PR-2 (product area) and store the digit in MDR.
4. Write back PR-2 bypassed.

Trigger 37 (01.62.37.1).

1. Develop and set add table address in MAR, transferring the digit in the units position of the D/B register into the units position of MAR and the digit in MDR into the tens position of MAR.
2. Read out of memory per add table address and store the sum digit in MDR.
3. Transfer the digit in the tens position of the D/B register into the units position of the D/B register.
4. Turn on Carry Out trigger if MDR contains an F-bit (add table carry).
5. Turn on Carry Out trigger if the output of the T/C switch is a "9" and a carry exists (Carry In trigger ON) from the previous add cycle.
6. Turn off E/Z trigger if add table digit is not a zero.

Trigger 38 (01.62.38.1).

1. Read out of memory per PR-2 with either the odd or the even-sense amplifiers blocked (Read-Y), depending on whether the PR-2 address is odd or even, to clear the memory location.
2. Write back PR-2 decremented into PR-2 and PR-3.
3. Turn on Carry In trigger if Carry Out trigger is ON.
4. Set an F-bit in MDR if the H/P trigger is OFF (minus sign) on first multiply cycle.
5. Clear the F-bit (carry) after first multiply cycle.
6. Write into memory per PR-2 from MBR.

Trigger 39 (01.62.39.1).

1. Read out of memory per PR-3 (product area) and store the digit in MDR.
2. Write back PR-3 bypassed.
3. Turn off First Cycle trigger.
4. Turn off (reset) the Carry Out trigger
5. Turn off (reset) the Cycle Control trigger.

Trigger 40 (01.62.40.1).

1. Develop and set add table address in MAR, transferring the digit in the units position of the D/B register into the units position of MAR and the digit in MDR into the tens position of MAR.
2. Read out of memory per add table address and store the sum digit in MDR.
3. Turn on Carry Out trigger if MDR contains an F-bit (carry).
4. Turn on Carry Out trigger if the output of the T/C switch is a "9" and a carry exists (Carry In trigger ON) from the previous add cycle.
5. Turn off E/Z trigger if the add table digit is not a zero.
6. Turn off (reset) the Carry In trigger.
7. Reset the D/B register units.

Trigger 41 (01.62.41.1).

1. Read out of memory per PR-3 with either the odd or the even-sense amplifiers blocked (read-Y), depending on whether the PR-3 address is odd or even, to clear the memory location.
2. Write back PR-3 decremented.
3. Turn on Carry In trigger if Carry Out trigger is ON.
4. Clear the F-bit (carry) after first multiply cycle unless an F-bit is being set for field definition.
5. Set an F-bit in MDR for field definition when Field Mark No. 1 and Field Mark No. 2 have been reached and there is no carry-out.
6. Write into memory per PR-3 from MBR.
7. Turn on Trigger 19 if there is a carry out or Field Mark No. 2 has been reached.

Trigger 19 (01.60.49.1).

1. Turn on Trigger 33 if Field Mark No. 1 has not been reached, and the Carry Out trigger is OFF.
2. Turn on Trigger 39 if the Carry Out trigger is ON.
3. Enter I-cycle for the next instruction if the Carry Out trigger if OFF and Field Mark No. 1 has been reached.

## MULTIPLY IMMEDIATE (CODE 13 - MM)

A sequential flow diagram for multiplication is shown in Figure 13-16. A sequence block diagram for this operation is shown in Figure 13-17. Function charts and sequential flow diagrams for this operation are shown in the Instructional System Diagrams on pages 25 through 31.

### Objective

Multiply the field at the P-address (OR-2) by the field whose units position is the $Q_{11}$ digit of the multiply immediate instruction, and store the algebraic product at location 00099 and successively lower memory locations.

### Functions

The Multiply Immediate-Code 13 operation differs from the Multiply-Code 23 operation only in the method of setting the mutliplier address in OR-1 during the I-cycle. See Multiply-Code 23.

### Auxiliary Triggers

See Multiply-Code 23.

### E-Timer Triggers

See Multiply-Code 23.

| | |
|---|---|
| A or B Advance | A or B Adv |
| Above 50 (greater than) | >50 |
| Binary Coded Decimal | BCD |
| Below 50 (less than) | <50 |
| Branch Indicator | BI |
| Branch No Indicator | BNI |
| Carriage Return (typewriter) | CR |
| Carry In (trigger) | CI (trg) |
| Carry Out (trigger) | CO (trg) |
| Check (bit) | C (bit) |
| Circuit Breaker | CB |
| Continuously Running Circuit Breaker | CRCB |
| Digit/Record Mark/Group Mark (trigger) | D/RM/GM (trg) |
| Decrement (trigger) | Decr (trg) |
| Digit/Branch Register | D/B Reg |
| Disconnect (gate trigger) | Disc. (gate trg) |
| Driver, Sample Pulse | DSP |
| Field Definition | Fld Def |
| Field Mark (trigger) | FM (trg) |
| Flag | F |
| *Group Mark | GM |
| Increment/Decrement (switch) | Incr/Decr (Sw) |
| Input/Output Exit (trigger) | I/O Exit (trg) |
| Instruction Cycle | I-cycle |
| Instruction Register | IR (-1, -2) |
| Integrator | Int |
| Inverter | Inv |
| Memory Address Register | MAR |
| Memory Address Register Storage | MARS |
| Memory Buffer Register | MBR |
| Memory Data Register | MDR |
| Memory Overflow (trigger) | Mem OF (trg) |
| Microampere | μa |
| Microsecond | μsec |
| Multiplicand | Mcnd |
| Multiplier/Quotient Register | M/Q Reg |
| Nanosecond | nsec |
| Negative "OR" | NOR |
| Operand Register | OR (-1, -2, -3) |
| Operation Register | Op Reg |
| Product Register | PR (-1, -2, -3) |
| Read Alphamerically | RA |
| Read Check | Rd Chk |
| Read Driver | Rd Dr |
| Read Numerically | RN |
| Read/Write (call) (trigger) (gate) | Rd/Wr (call) (trg) (gate) |
| Recomplement | Recomp |
| Record Mark | RM |
| Resistor-Capaçitor | RC |
| Response (gate) (trigger) | Resp (gate) (trg) |
| Selector Common Contacts | Sel Com Cont |
| Single Cycle Execute | SCE |
| Single Instruction Execute | SIE |
| Synchronizing (trigger) | Sync (trg) |
| Tabulate (typewriter) | Tab |
| Trigger | Trg |
| True/Complement (switch) (trigger) | T/C (sw) (trg) |
| Vertical Redundancy Check (Parity Check) | VRC |
| Write Alphamerically | WA |
| Write Check | Wr Chk |
| Write Drivers | Wr Dr |
| Write Numerically | WN |

*Used with the IBM 1311 Disk Storage Drive, a special feature.

## Appendix B Character Code Chart

| | Character | Input | | | Core Storage | | Output | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Typewriter | Tape | Card | Zone | Num | Typewriter | Tape | Card |
| ALPHAMERIC MODE | (Blank) | (Space) | C | (Blank) | C | C | (Space) | C | (Blank) |
| | . (Period) | . | X0821 | 12,3,8 | C | 3 | . | X0821 | 12,3,8 |
| | ) | ) | X0C84 | 12,4,8 | C | 4 | ) | X0C84 | 12,4,8 |
| | + | + | X0C | 12 | 1 | C | + | X0C | 12 |
| | $ | $ | XC821 | 11,3,8 | 1 | 3 | $ | XC821 | 11,3,8 |
| | * | * | X84 | 11,8,4 | 1 | 4 | * | X84 | 11,4,8 |
| | - (Hyphen) | - | X | 11 | 2 | C | - | X | 11 |
| | / | / | 0C1 | 0,1 | 2 | 1 | / | 0C1 | 0,1 |
| | , (Comma) | , | 0C821 | 0,3,8 | 2 | 3 | , | 0C821 | 0,3,8 |
| | ( | ( | 084 | 0,4,8 | 2 | 4 | ( | 084 | 0,4,8 |
| | = | = | 821 | 3,8 | 3 | 3 | = | 821 | 3,8 |
| | @ | @ | C84 | 4,8 | 3 | 4 | @ | C84 | 4,8 |
| | A-I | A-I | X0, 1-9 | 12, 1-9 | 4 | 1-9 | A-I | X0, 1-9 | 12, 1-9 |
| | 0 (—) | (None) | (None) | 11,0 | 5 | C | - (Hyphen) | X | 11,0 |
| | J-R | J-R | X, 1-9 | 11, 1-9 | 5 | 1-9 | J-R | X, 1-9 | 11, 1-9 |
| | 1-9 (—) | J-R | X, 1-9 | 11, 1-9 | 5 | 1-9 | J-R | X, 1-9 | 11, 1-9 |
| | S-Z | S-Z | 0, 2-9 | 0, 2-9 | 6 | 2-9 | S-Z | 0, 2-9 | 0, 2-9 |
| | 0 (+) | 0 | 0 | 0 or 12,0 | 7 | C | 0 | 0 | 0 |
| | 1-9 (+) | 1-9 | 1-9 | 1-9 | 7 | 1-9 | 1-9 | 1-9 | 1-9 |
| | ≠ | ≠ | 082 | 0,2,8 | C | C82 | (Stop) | EOL | 0,2,8 |
| | | | | | | | | | |
| NUMERICAL MODE | (Blank) | (Space) | C | (Blank) | | C | 0 | 0 | 0 |
| | 0 (+) | 0 | 0 | 0 | | C | 0 | 0 | 0 |
| | 0 (-) | $\bar{0}$ | X, X0C | 11,0 | | F | 0 | X | 11,0 |
| | 1-9 (+) | 1-9 | 1-9 | 1-9 | | 1-9 | 1-9 | 1-9 | 1-9 |
| | 1-9 (-) | $\bar{1}$-$\bar{9}$ | X, 1-9 | 11, 1-9 | | F, 1-9 | 1-9 | X, 1-9 | 11, 1-9 |
| | ≠ | ≠ | 082 | 0,2,8 | | C82 | ≠ (Stop, WN) (DN) | EOL(WN) 082 (DN) | 0,2,8 |
| | $\bar{\neq}$ | $\bar{\neq}$ | X82 | 11,8,2 | | F82 | $\bar{\neq}$ | X82 | 11,8,2 |
| | ≠ | ≠ | 08421 | 0,7,8 | | *C8421 | ≠ | 08421 | 0,7,8 |
| | $\bar{\neq}$ | $\bar{\neq}$ | X8421 | 12,7,8 | | F8421 | $\bar{\neq}$ | X8421 | 12,7,8 |
| | Num Blank † | @ | C84 | 4,8 | | C84 | @ | C84 | (Blank) |

† For Card Format Use Only
* Recorded as 0, 8, 4, 2, 1 in disk storage

Note: All numbered Triggers have an associated console lamp.

| Trigger Number | System Diagram Page Number |
|---|---|
| 1 | 01.15.11.1 |
| 2 | 01.15.12.1 |
| 3 | 01.15.13.1 |
| 4 | 01.15.14.1 |
| 5 | 01.15.15.1 |
| 6 | 01.15.16.1 |
| 7 | 01.15.17.1 |
| 8 | 01.15.18.1 |
| 11 | 01.60.11.1 |
| 12 | 01.60.12.1 |
| 13 | 01.60.13.1 |
| 14 | 01.60.14.1 |
| 15 | 01.60.45.1 |

| Trigger Number | System Diagram Page Number |
|---|---|
| 16 | 01.60.45.1 |
| 18 | 01.60.48.1 |
| 19 | 01.60.49.1 |
| 21 | 01.60.31.1 |
| 23 | 01.60.32.1 |
| 26 | 01.60.57.1 |
| 27 | 01.60.57.1 |
| 28 | 01.60.58.1 |
| 29 | 01.60.59.1 |
| 30 | 01.64.10.1 |
| 31 | 01.64.11.1 |
| 32 | 01.62.30.1 |
| 33 | 01.62.33.1 |

| Trigger Number | System Diagram Page Number |
|---|---|
| 34 | 01.62.34.1 |
| 35 | 01.62.35.1 |
| 36 | 01.62.36.1 |
| 37 | 01.62.37.1 |
| 38 | 01.62.38.1 |
| 39 | 01.62.39.1 |
| 40 | 01.62.40.1 |
| 41 | 01.62.41.1 |
| | |
| | |
| | |
| | |
| | |

## Appendix D Named Triggers/Latches

| Trigger Name | System Diagram Page Number | Console Lamp |
|---|---|---|
| A/B | 01.10.12.1 | * |
| A/B Auxilliary | 01.10.12.1 | No |
| Branch Test | 01.25.35.1 | * |
| Carry In | 01.63.40.1 | * |
| Carry Out | 01.63.40.1 | * |
| Clock Drive | 01.10.05.1 | No |
| Clock 1 & Clock 2 | 01.10.06.1 | No |
| Clock 3 & Clock 4 | 01.10.07.1 | No |
| Clock 5 & Clock 6 | 01.10.08.1 | No |
| Clock 7 & Clock 8 | 01.10.09.1 | No |
| Clock 9 & Clock 10 | 01.10.10.1 | No |
| Cycle Control | 01.62.31.1 | * |
| Decrement | 01.60.05.1 | * |
| Digit/Record Mark/Group Mark | 01.63.50.1 | * |
| Disconnect Gate | 01.80.25.1 | * |
| Display Address | 01.06.30.1 | * |
| E-Cycle Entry | 01.15.18.1 | No |
| Equal/Zero | 01.60.41.1 | * |
| Field Mark Number 1 | 01.63.30.1 | * |
| Field Mark Number 2 | 01.63.30.1 | * |
| First Cycle | 01.63.10.1 | * |
| Flag | 01.81.10.1 | * |
| High/Plus | 01.60.40.1 | * |
| Hold | 01.64.12.1 | * |
| I-Cycle | 01.15.10.1 | * |
| I/O Exit | 01.64.13.1 | * |

| Trigger Name | System Diagram Page Number | Console Lamp |
|---|---|---|
| Insert 1 | 01.06.20.1 | No |
| Insert 2 | 01.06.20.1 | * |
| Insert Control | 01.06.20.1 | * Note 1 |
| MAR VRC | 01.58.09.1 | * Note 2 |
| MBR - Odd Check | 01.40.10.1 | * |
| MBR - Even Check | 01.40.20.1 | * |
| Memory Overflow | 01.64.14.1 | * |
| Odd-Even | 01.43.10.1 | * Note 3 |
| Overflow | 01.60.40.1 | * Note 4 |
| Read Check | 01.81.45.1 | * |
| Read/Write Call | 01.64.14.1 | * |
| Recomplement | 01.60.32.1 | * |
| Recomplement Control | 01.60.24.1 | * |
| Response Check | 01.82.30.1 | No |
| Response Gate | 01.80.25.1 | * |
| Run | 01.06.10.1 | * Note 5 |
| Save 2 | 01.06.15.1 | No |
| Save Control | 01.06.15.1 | * |
| Sel 1 | 01.25.15.1 | No |
| Single Cycle | 01.06.10.1 | No |
| Start 1 | 01.06.05.1 | * Note 6 |
| Start Control | 01.06.05.1 | * |
| Stop 1 | 01.06.11.1 | * |
| Sync | 01.64.13.1 | * |
| True/Complement | 01.63.20.1 | * |
| Write Check | 01.81.45.1 | * |

Note 1: "Insert" light
Note 2: "MARS Check" light
Note 3: Odd=lamp on
Note 4: Arith Chk light
Note 5: On= Run lamp, Off=Manual light
Note 6: Automatic light

## Appendix E Register Triggers/Latches

Note: All register triggers have an associated console lamp.

| Register | Trigger Name | System Diagram Page Number |
|---|---|---|
| Operation | | |
| | C Bit, 8 Bit, & 4 Bit (Units) | 01.20.07.1 |
| | 2 Bit & 1 Bit (Units) | 01.20.09.1 |
| | C Bit, & 4 Bit (Tens) | 01.20.10.1 |
| | 2 Bit & 1 Bit (Tens) | 01.20.12.1 |
| | | |
| MBR - Odd | | |
| | C Bit & F Bit | 01.40.07.1 |
| | 8 Bit & 4 Bit | 01.40.08.1 |
| | 2 Bit & 1 Bit | 01.40.09.1 |
| | | |
| MBR - Even | | |
| | C Bit & F Bit | 01.40.17.1 |
| | 8 Bit & 4 Bit | 01.40.18.1 |
| | 2 Bit & 1 Bit | 01.40.19.1 |
| | | |
| MDR | | |
| | C Bit, F Bit, & 8 Bit | 01.45.05.1 |
| | 4 Bit, 2 Bit, & 1 Bit | 01.45.07.1 |
| | | |
| Digit/Branch | | |
| | C Bit, 8 Bit, & 4 Bit (Units) | 01.50.07.1 |
| | 2 Bit & 1 Bit (Units) | 01.50.09.1 |
| | C Bit, 8 Bit, & 4 Bit (Tens) | 01.50.17.1 |
| | 2 Bit & 1 Bit (Tens) | 01.50.19.1 |
| | | |
| MAR | | |
| | C Bit & 8 Bit (Units) | 01.57.05.1 |
| | 4 Bit & 2 Bit (Units) | 01.57.07.1 |
| | 1 Bit (Units) | 01.57.09.1 |
| | C Bit (Tens) | 01.57.09.1 |
| | 8 Bit & 4 Bit (Tens) | 01.57.16.1 |
| | 2 Bit & 1 Bit (Tens) | 01.57.18.1 |
| | C Bit & 8 Bit (Hundreds) | 01.57.20.1 |
| | 4 Bit & 2 Bit (Hundreds) | 01.57.22.1 |
| | 1 Bit (Hundreds) | 01.57.24.1 |
| | C Bit (Thousands) | 01.57.24.1 |
| | 8 Bit & 4 Bit (Thousands) | 01.57.26.1 |
| | 2 Bit & 1 Bit (Thousands) | 01.57.28.1 |
| | C Bit, 2 Bit, & 1 Bit (10 Thousands) | 01.57.30.1 |
| Multiplier/Quotient | | |
| | C Bit, 8 Bit, & 4 Bit | 01.62.50.1 |
| | 2 Bit & 1 Bit | 01.62.52.1 |

| | E Timer Triggers | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Operation Code | 11 | 12 | 13 | 14 | 15 | 16 | 18 | 19 | 21 | 23 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | Hold Tgr |
| 11 & 21 | Δ | Δ | Δ | Δ | | | | | Δ | Δ | | | | | | | | | | | | | | | | | |
| 12 & 22 | Δ | Δ | Δ | Δ | | | | | Δ | Δ | | | | | | | | | | | | | | | | | |
| 13 & 23 | | | | | | | | Δ | | | | | | | | | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | |
| 14 & 24 | Δ | Δ | Δ | Δ | | | | | Δ | | | | | | | | | | | | | | | | | | |
| 15 & 25 | | | | | | | | | | | Δ | Δ | | | | | | | | | | | | | | | |
| 16 & 26 | | | | | | | | | | | Δ | Δ | | | | | | | | | | | | | | | |
| 17 & 27 | | | | | Δ | Δ | | | | | Δ | Δ | | | | | | | | | | | | | | | |
| 31 | | | | | | | | | | | Δ | Δ | | | | | | | | | | | | | | | |
| 32 | | | | | | | | | | | | | Δ | Δ | | | | | | | | | | | | | |
| 33 | | | | | | | | | | | | | Δ | Δ | | | | | | | | | | | | | |
| 34 | | | | | | | | | | | | | | | | | | | | | | | | | | | Δ |
| 35 | | | | | | | | | | | | | | | Δ | * | | | | | | | | | | | Δ |
| 36 | | | | | | | | | | | | | | | Δ | * | | | | | | | | | | | Δ |
| 37 | | | | | | | | | | | | | | | Δ | Δ | | | | | | | | | | | Δ |
| 38 | | | | | | | | | | | | | | | Δ | * | | | | | | | | | | | Δ |
| 39 | | | | | | | | | | | | | | | Δ | * | | | | | | | | | | | Δ |
| 41 | (None) | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 42 | | | | | | | Δ | Δ | | | | | | | | | | | | | | | | | | | |
| 43 | | | | | | | Δ | Δ | | | | | Δ | Δ | | | | | | | | | | | | | |
| 44 | | | | | | | Δ | Δ | | | | | Δ | Δ | | | | | | | | | | | | | |
| 45 | | | | | | | Δ | Δ | | | | | Δ | Δ | | | | | | | | | | | | | |
| 46 | | | | | | | Δ | Δ | | | | | | | | | | | | | | | | | | | |
| 47 | | | | | | | Δ | Δ | | | | | | | | | | | | | | | | | | | |
| 48 | (None) | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 49 | | | | | | | Δ | Δ | | | | | | | | | | | | | | | | | | | |

Δ Actively used or can be actively used by the operation

* Turned on or off but not actively used by the operation

## Appendix G Auxiliary Trigger Chart

| Operation Code | Auxiliary Triggers | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | E-Cycle Entry | Decrement | First Cycle | Field Mk No. 1 | Field Mk No. 2 | T/C | High/Plus | Equal/Zero | Carry Out | Carry In | Recomp Ctrl | Recomp | Cycle Ctrl | Response Check | Save Ctrl. | Digit/RM/GM | Branch Test | Response Gate | Sync | Disconnect Gate | I/O Exit | Stop 1 | Rd/Wr Call | Write Chk. | Read Chk. | Mem O'Flow | Overflow | Flag |
| 11 & 21 | Δ | D | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | | | | * | | | | | | | | | | Δ | | |
| 12 & 22 | Δ | D | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | | | | * | | | | | | | | | | Δ | | |
| 13 & 23 | Δ | I&D | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | | | Δ | | | | | | | | | | | | | Δ | | |
| 14 & 24 | Δ | D | Δ | Δ | Δ | Δ | Δ | Δ | Δ | Δ | | | | | | Δ | | | | | | | | | | | | |
| 15 & 25 | Δ | D | * | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16 & 26 | Δ | D | Δ | Δ | | | | | | | | | | | | | | | | | | | | | | | | |
| 17 & 27 | Δ | D | Δ | Δ | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | Δ | I | * | | | | | | | | | | | | | Δ | | | | | | | | | | | | |
| 32 | Δ | D | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 33 | Δ | D | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 34 | Δ | D | | | | | | | | | | | | | | | | | Δ | Δ | | | | | | | | |
| 35 | Δ | I | | | | | | | | | | | Δ | | | | Δ | Δ | Δ | Δ | | Δ | Δ | | Δ | | | |
| 36 | Δ | I | | | | | | | | | | | Δ | | | | Δ | Δ | Δ | Δ | Δ | Δ | | Δ | | | | Δ |
| 37 | Δ | I | | | | | | | | | | | Δ | | | | Δ | Δ | Δ | Δ | Δ | Δ | | Δ | | | | |
| 38 | Δ | I | | | | | | | | | | | Δ | | Δ | | Δ | Δ | Δ | Δ | | Δ | Δ | | Δ | | | |
| 39 | Δ | I | | | | | | | | | | | Δ | | Δ | | Δ | Δ | Δ | Δ | | Δ | Δ | | Δ | | | |
| 41 | Δ | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 42 | Δ | D | | | | | | | | | | | | Δ | | | | | | | | | | | | | | |
| 43 | Δ | D | | | | | | | | | | | | | Δ | | | | | | | | | | | | | |
| 44 | Δ | D | | Δ | | | | | | | | | | | | | | | | | | | | | | | | |
| 45 | Δ | D | | | | | | | | | | | | | Δ | | | | | | | | | | | | | |
| 46 | Δ | D | | | | | | | | | | | | | | Δ | | | | | | | | | | | | |
| 47 | Δ | D | | | | | | | | | | | | | | Δ | | | | | | | | | | | | |
| 48 | Δ | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 49 | Δ | D | | | | | | | | | | | | | | | | | | | | | | | | | | |

Δ Actively used or can be actively used by the operation

* Turned on or off but not actively used by the operation

| Form No. | Type* | Manual Name |
|---|---|---|
| 227-5751 | CEMI | IBM 1620 Data Processing System, Model 1 |
| 227-5769 | CEISD | IBM 1620 Data Processing System, Model 1, Vol I |
| 227-5770 | CEISD | IBM 1620 Data Processing System, Model 1, Vol II |
| 227-5771 | CEISD | IBM 1620 Data Processing System, Model 1, Vol III |
| 227-5812 | CEMI | IBM 1620 Data Processing System, Model 1, Automatic Divide Feature |
| 227-5813 | CEMI | IBM 1620 Data Processing System, Model 1, Indirect Addressing Feature |
| 227-5814 | CEMI | IBM 1620 Data Processing System, Model 1, Additional Instructions Feature |
| 227-5815 | CEMI | IBM 1620 Data Processing System, Model 1, 1621 Paper Tape Unit Feature |
| 227-5816 | CEMI | IBM 1620 Data Processing System, Model 1, 1622 Card Read-Punch Feature |
| 227-5817 | CEMI | IBM 1620 Data Processing System, Model 1, 1311 Disk Storage Drive Feature |
| 227-5818 | CEMI | IBM 1620 Data Processing System, Model 1, 1443 Printer Feature |
| 227-5819 | CEMI | IBM 1620 Data Processing System, Model 1, 1626-1627 Plotter Feature |
| 227-5630 | CEMI | IBM 1620 Data Processing System, Model 1, Floating Point Feature |
| 223-6900 | CEIMM | Standard Modular System |
| 227-5715 | CEMM | IBM 1622 Card Read-Punch Unit |
| S27-5831 | CEMM | IBM 1622 Supplement to 227-5715 |

*Type
- CEMI = Customer Engineering Manual of Instruction
- CEMM = Customer Engineering Maintenance Manual
- CEIMM = Customer Engineering Instruction Maintenance Manual
- CEISD = Customer Engineering Instructional System Diagrams

| Form No. | Type* | | Manual Name |
|---|---|---|---|
| 227-5612 | CEISD | | IBM 1622 Card Read-Punch Unit |
| 227-5711 | CEMI | | IBM 1621 Paper Tape Unit |
| 227-5712 | CEMM | | IBM 1621 Paper Tape Unit |
| S27-5830 | CEMM | | IBM 1621 Supplement to 227-5712 |
| 225-3056 | CEMI | | IBM 1443 Printer |
| 225-3032 | CEMM | | IBM 1443 Printer |
| 227-5721 | CEIMM | | IBM 1626 Plotter Control Unit and IBM 1627 Plotter |
| 227-5838 | CEMI | | IBM 1710 Control System |
| 227-5839 | CEMM | | IBM 1710 Control System |
| 227-5703 | CEMI | | IBM 1311 Disk Storage Drive |
| 227-5705 | CEMI | | IBM 1311 Model 3 Controls |
| 227-5649 | CEMM | | IBM 1311 Disk Storage Drive |
| 227-5679 | CEMI | | IBM 1713 through IBM 1717 |
| 227-5680 | CEMM | | IBM 1710 Attached Units (1713 through 1717) |
| 223-6652 | CEMM | | IBM Typewriter, Model B1 |
| 223-6653 | CEMI | | IBM Typewriter, Model B1, Modified for DP Equipment |
| 229-5012 | | | IBM 1620 Service Index |
| 229-5013 | | | IBM 1620 Core Chart |
| A26-5692 | | ** | Systems Reference Library IBM 1620 Bibliography |
| A26-5695 | | | Systems Reference Library IBM 1710 Bibliography |
| 223-6725 | CEMI | | Tektronix Oscilloscopes |
| 223-6889 | CEMI | | Transistor Component Circuits |
| 223-6783 | CEMI | | Transistor Theory and Application |
| 223-6794 | CEMI | | Transistor Theory Illustrated |
| 225-6478 | CEMI | | 60 Cycle SMS Power Supply |

** Includes references to Physical Planning Information