IBM Field Engineering

Theory Of Operation

Restricted Distribution

2260 Display Station, Models 1 and 2

2848 Display Control, Models 1, 2, and 3 (Serial No. 60,000 Series)

Y27-2046-3

PREFACE

This manual presents the detailed theory of operation of the IBM 2260 Display Station Models 1 and 2, and IBM 2848 Display Control Unit, Models 1, 2, and 3. However, the description of the 2848 Display Control pertains only to those units whose serial numbers are 60,000 or above.

The following publications can be used to supplement the information provided in this manual:

- IBM 2260 Display Station, IBM 2848 Display Control Maintenance Manual (Form Y27-2047-2)
- IBM 2260 Display Station, IBM 2848 Display Control FE Diagram Manual (Form Y27-2048-2)
- 1052 Printer Keyboard and 1053 Printer Maintenance Manual (Form 225-3179-2)
- Medium Power Standard Power Supplies (Form 223-2799-0)
- IBM 1052, 1053 CEMI (Form 225-3179)
- IBM System/360 I/O Interface - Channel to Control Unit - Original Equipment Manufacturers Information (Form A22-6843-3)

This is a reprint of Y27-2046-2 incorporating changes released in the following F. E. Supplements:

Form Number	Pages Affected	Date
Y27-2165-0	4-10, 4-11 and 4-18	Sept. 11, 1967
Y27-2171-0	v through vii, 1-3 through 1-6, 1-21, 1-22, 2-97, 2-98, 2-123, 2-124, 2-125, 2-126, 6-1 through 6-4, B-1 through B-3, X-1 through X-8 add pages 2-124A and 2-124B	Dec. 1, 1967

ABBREVIATIONS LIST

The abbreviations used in this manual, together with their definitions, are as follows:

Abbreviation	Definition
ACK	Acknowledge
ASCII	American Standard Code for Information Interchange
CAN	Cancel
CRT	Cathode-Ray Tube
DAU	Data Adapter Unit
DC	Display Control
DS	Display Station
EBCDIC	Expanded Binary Coded Decimal Interchange Code
EOM	End of Message
EOT	End of Transmission
EPO	Emergency Power Off
ETX	End of Text
FC	Feature Code
LF	Line Feed
LRC	Longitudinal Redundancy Check
MI	Manual Input
NAK	Not Acknowledge
NDC	Nondestructive Cursor
NL	New Line
OLSA	Off Line Selectric Analyzer
SMS	Standard Modular System
SOH	Start of Heading
STX	Start of Text
VRC	Vertical Redundancy Check
XA	Transmit Adapter

This manual has been prepared by the IBM Systems Development Division Product Publications, Dept. 520, CPO Box 120, Kingston, N.Y., 12401. Address comments concerning the manual to this address.

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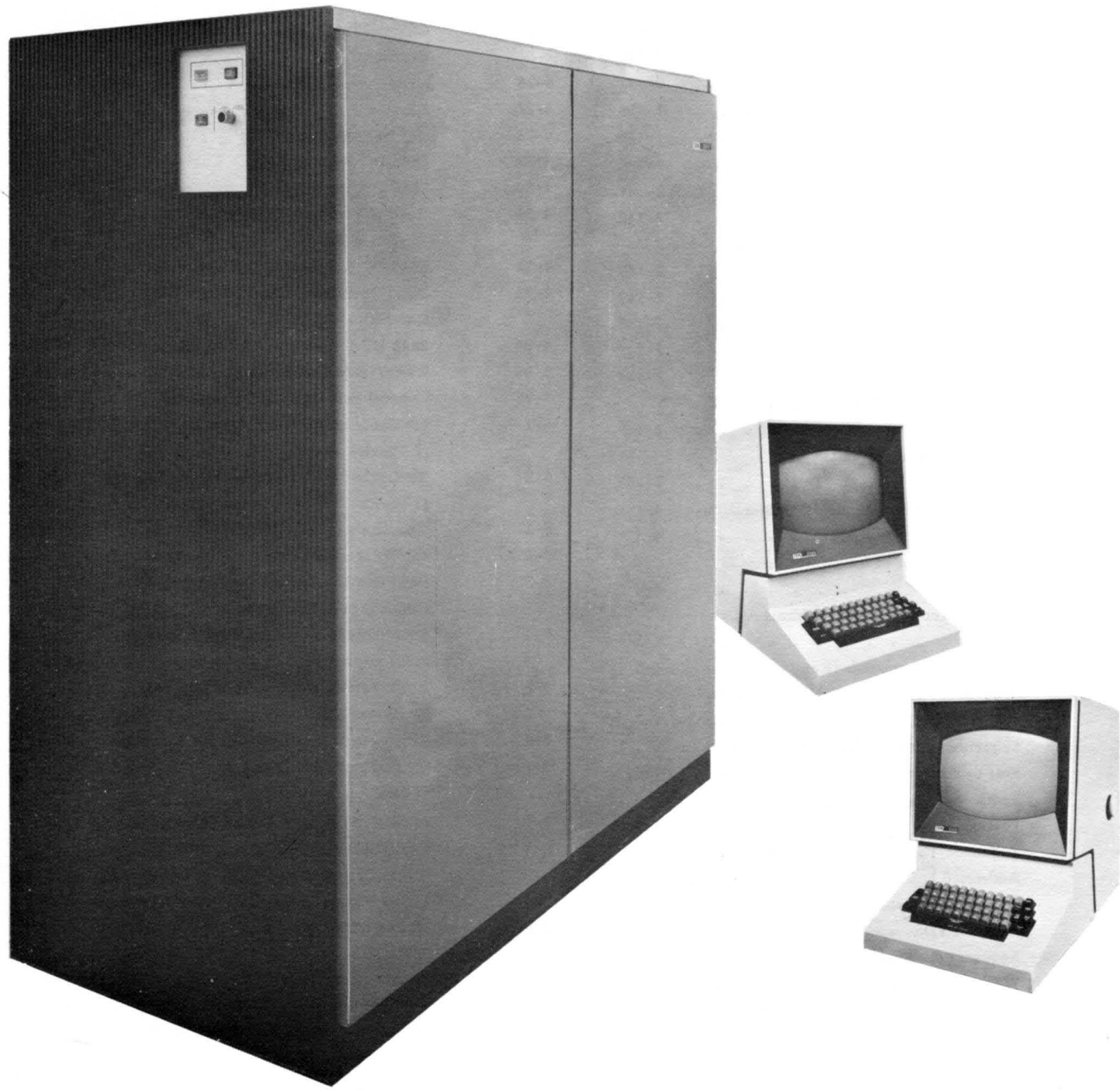
ILLUSTRATIONS



IBM 2260 Display Station • 2848 Display Control

SCOPE OF MANUAL

This manual describes the capabilities and the theory of operation of the IBM 2260 Display Station and the IBM 2848 Display Control (see Frontispiece).

The manual is divided into six chapters and three appendices:

1. Chapter 1, Introduction, provides a functional description of the equipment, including the major data flow and control signal paths. It also includes a description of the interface of the 2848 with System/360, a description of the feature structures of the 2848 and 2260, and reference data (code sets, command structure, etc.) required for an overall concept of equipment operation.
2. Chapter 2, Functional Units, gives a detailed description of the operation of the logic areas of both the 2260 and 2848, with simplified logic diagrams and timing charts.
3. Chapter 3, Principles of Operation, presents the theory of operation for the IBM 2848 Display Control through the use of a comprehensive set of flow charts.
4. Chapter 4, Features, presents the theory of operation of the remote interface adapter used in remote applications.
5. Chapter 5, Power Supplies and Control, explains the operation of the IBM 2848 Display Control power supply, control, and distribution network. (Because of its integral relation with other display station circuitry, the IBM 2260 power network is discussed in Chapter 2.)
6. Chapter 6, Console and Maintenance Features, describes the function of the controls and indicators located on the operator and CE panels of the IBM 2848 Display Control.
7. Appendix A, Machine Characteristics, summarizes equipment capabilities and characteristics.
8. Appendix B, Special Circuits, describes the special circuits found in the 2848 Display Control.
9. Appendix C, Language Features, describes the language features available with the 2260 Display Station.

There are three models of the IBM 2848 Display Control: Models 1, 2, and 3. This manual describes the operation of Model 3, which is the largest (in terms of the number of characters displayed) and the most complex. Once Model 3 operation is understood, the operation of Models 1 and 2 will be apparent. When the manual is used as reference material by those interested in Model 1 or 2 only, information unique to the Model 3 can be disregarded.

Similarly, the IBM 2260 Display Station can be used as an output-only device when it does not include either of the two input keyboards (numeric and alphanumeric) that are available as special features. Throughout this manual it is assumed that the 2260 includes an input keyboard, so that the 2260's full I/O capabilities can be described. When the manual is used as reference for output-only display stations (no keyboard), all data pertaining to keyboard input operations can be disregarded. The output capability (video display) is functionally separate from keyboard input operation.

Other features such as the printer adapter, channel adapter, and destructive and nondestructive cursor have been incorporated within the framework of the Functional Units chapter to permit a thorough analysis of the more comprehensive Model 3 tied to an IBM System/360 via the channel adapter. Although some of the features could have been placed in Chapter 4, certain advantages do accrue with the method selected. The interrelationships between the features and the adapters become more apparent when viewed and discussed on an overall systems basis rather than separated individually. As other features or optional equipment become available, they will appear in Chapter 4, Features.

IBM 2848 DISPLAY CONTROL, GENERAL DESCRIPTION

The IBM 2848 Display Control contains the storage and control logic required to interface the 2848 with either a System/360 selector or multiplexor channel or a communications data set. (The latter configuration permits remote operation of the display group.) The IBM 2848 Display Control can also control up to 24 IBM 2260 Display Stations.

The 2848 Display Control is available in three basic models; each can be supplemented by certain features to expand its basic display capabilities and to provide the display control with special functional abilities. The 2848 Display Control is described in the following paragraphs by first considering the capabilities of the three basic models and the feature combinations that can be selected to supplement each model. Then each feature is described in respect

to the display capability expansion or special function that it provides when added to the basic 2848 Display Control.

All three 2848 models offer a choice of operating voltages (primary input of 208vac or 230vac) and exterior cabinet colors (red, yellow, blue, or gray, to permit aesthetic compatibility with the host System/360). These options are not discussed in respect to each model, however.

IBM 2848 Display Control, Model 1

The basic IBM 2848 Model 1 is capable of operating two 3355 Display Adapters; each 3355 can service two IBM Model 2 2260 Display Stations. The Model 1 can generate a display that consists of six rows, each containing 40 characters (240 characters total), on the CRT of all 2260 Display Stations associated with the display control. The basic Model 1 also includes a choice of the 9011 Channel Adapter, the 9012 Data Set Adapter (1200 bps), or the 9013 Data Set Adapter (2400 bps) for interfacing with the host System/360.

Through incorporation of additional optional features, 2848 Model 1 capabilities can be extended to include the following:

1. The ability to drive six additional 3355 Display Adapters (via 3857 Expansion Panel), four additional 3355's (via 3858 Expansion Panel, or ten additional 3355's (via 3857 and 3858). A maximum of 24 IBM 2260 Display Stations (Model 2), each displaying a 240-character (maximum) message, can thus be accommodated.
2. The ability to drive the 7927 Printer Adapter, which controls an IBM 1053 Model 4 Printer, to provide a permanent record of display group data under either program or operator control.
3. A nondestructive cursor (character-entry and display-position indicator and locator) that can be moved within the display area without disturbing or destroying the data displayed on the CRT of the 2260 Display Station.
4. A line-addressing feature which enables the processor, during write operations, to select any one of the six lines within the 2260 Display Station CRT display under program control.
5. A Foreign Language feature that equips the 2848 Display Control with the character set and operator control designations in the languages of France, Germany, and United Kingdom.

IBM 2848 Display Control, Model 2

The basic IBM 2848 Model 2 can drive one 3356 Display Adapter which services two IBM Model 2 2260 Display Stations. The Model 2 can generate a display consisting of 12 rows, each containing 40 characters (480 characters total), on the CRT of all 2260 Display Stations associated with the display control.

The basic Model 2 also includes a choice of the 9011 Channel Adapter, the 9012 Data Set Adapter (1200 bps), or the 9013 Data Set Adapter (2400 bps) for interfacing with the host System/360.

Other optional features can be selected to extend the capabilities of the basic Model 2. These extended capabilities include:

1. The ability to drive three additional 3356 Display Adapters (via 3858 Expansion Panel), four additional 3356 Display Adapters (via 3857 Expansion Panel), or a maximum of seven additional 3356 Display Adapters (via 3357 and 3858 Expansion Panels). Since each additional 3356 Display Adapter enables the 2848 Display Control Model 2 to service two Model 2 2260 Display Stations, the display station complement associated with the Model 2 can vary from 1 to a maximum of 16, with each associated display station capable of displaying a 480-character message.
2. The 1053 Printer control, nondestructive cursor, line-addressing capabilities, and language features already described in conjunction with the 2848 Display Control Model 1.

IBM 2848 Display Control, Model 3

The basic IBM 2848 Model 3 can operate one 3357 Display Adapter which services two IBM Model 1 2260 Display Stations. The Model 3 can generate a display consisting of 12 rows, each containing 80 characters (960 characters total), on the CRT of all 2260 Display Stations associated with the display control.

The basic Model 3 also includes a choice of the 9011 Channel Adapter, the 9012 Data Set Adapter (1200 bps), or the 9013 Data Set Adapter (2400 bps) for interfacing with the host System/360.

Other optional features can be selected to extend the capabilities of the basic Model 3. These extended capabilities include:

1. The ability to drive up to three additional 3357 Display Adapters and, consequently, a maximum of eight Model 1 2260 Display Stations, with each display station displaying a 960-character (maximum) message.

IBM 2848 Model Summary

Figure 1-1 summarizes the three 2848 models with respect to the standard customer options, the applicable feature adapters, the models and number of 2260 Display Stations that can be serviced, and the maximum displayable message length.

Special 2848 Features

Each of the customer-selection and special features that can be chosen to complement the three basic 2848 models is described in Figure 1-2. The information provided on each feature consists of the feature code, the feature function, the 2848 models to which the feature can be attached, and any prerequisite features. Language features are described separately in Appendix C.

The Isolation Feature defined at the end of Figure 1-2 provides improved equipment performance by eliminating undesired logic signals that occur while power is removed from the unit. This feature enables the CE to perform maintenance tests on an "isolated" unit without affecting overall system operations. The feature is implemented by providing DSBL REQUEST/INTF DSBLD switch (and indicator) on the 2848 operator's panel and a special selection circuit modification (explained in Chapter 2 under "Hold Select Circuits").

Operator Controls and Indicators

The 2848 controls and indicators available to the operator are limited to the control of unit power. The controls (or indicator) and their functions are as follows:

1. Power On switch: provides ac power to dc power supplies.
2. Power Off switch: removes ac power from dc supplies.
3. Power On-Off indicator: lights when unit ac and dc power is on.
4. DSBL REQUEST/INTF DSBLD pushbutton/indicator: permits a unit equipped with the Isolation Feature to be logically disconnected from the system.
5. REMOTE-LOCAL: in LOCAL, permits operator to control unit power; in REMOTE, transfers power control to system.

CE Panel

The 2848 Display Control is provided with a CE (maintenance) panel to permit local operation of the unit during checks and/or maintenance.

IBM 2260 DISPLAY STATION, GENERAL DESCRIPTION

The basic IBM 2260 Display Station contains the CRT display used to present data transferred from the associated System/360 and processed in the 2848 Display Control. There are two models of the IBM 2260 Display Station: Model 1, which is used with the Model 3 2848 Display Control only, and

Model Number	Customer Options	Optional Feature Adapters Available	Maximum Associated 2260 Display Stations Possible	Maximum Display Length
1	9011 Channel Adapter, or 9012 Data Set Adapter (1200 bps), or 9013 Data Set Adapter (2400 bps). Exterior colors of red, yellow, blue, or gray. Operates on primary power of 208vac or 230vac. Language Features	3355 Display Adapter. 7929 Printer Adapter. 3857 Expansion Panel. 3858 Expansion Panel. 4787 Line Addressing. 5340 Nondestructive Cursor. 5341 Nondestructive Cursor Adapter.	24 (Model 2)	Six rows of 40 characters each (240 characters total).
2	Same as Model 1.	Same as for Model 1 except that 3356 Display Adapter replaces 3355 used with Model 1.	16 (Model 2)	Twelve rows of 40 characters each (480 characters total).
3	Same as Model 1.	3357 Display Adapter. 3857 Expansion Panel. 4787 Line Addressing. 5340 Nondestructive Cursor. 5341 Nondestructive Cursor Adapter. 7928 Printer Adapter.	8 (Model 1)	Twelve rows of 80 characters (960 characters total).

Figure 1-1. Summary of IBM 2848 Display Control Models

Feature Code	Feature Description	2848 Models to Which Feature Can Be Attached	Prerequisite 2848 Features
3355 Display Adapter	Contains storage and control logic to service two IBM 2260 Display Stations, Model 2.	1 only	None for up to two 3355 adapters. A 3857 for up to six additional 3355 adapters. A 3858 for up to four additional 3355 adapters. A 3857 and a 3858 for maximum of 10 additional 3355 adapters.
3356 Display Adapter	Contains storage and control logic to service two IBM 2260 Display Stations, Model 2.	2 only	None for one 3356 adapter. A 3857 for up to four additional 3356 adapters. A 3858 for up to three additional 3356 adapters. A 3857 and a 3858 for the maximum of seven additional 3356 adapters.
3357 Display Adapter	Contains storage and control logic to service two IBM 2260 Display Stations, Model 1.	3 only	None for one 3357. A 3857 for up to three additional 3357 adapters.
9011 Channel Adapter (Selective Feature)	Contains the circuitry required to interface the 2848 with a System/360 selector or multiplexor channel; operates in single-byte (8 bits) mode at a rate of up to 2560 characters per second.	1, 2, and 3	None
9012 Data Set Adapter (Selective Feature)	Interfaces the 2848 Display Control with a 1200-bps (120 characters per second) communications data set equivalent to the Western Electric 202D Data Set. The data set interface meets the requirements of the EIA 232A standard interface specification.	1, 2, and 3	Host System/360 must be equipped with an IBM 4656 Terminal Adapter, Type III (1200 bps).
9013 Data Set Adapter (Selective Feature)	Interfaces the 2848 Display Control with a 2400-bps (240 characters per second) communications data set equivalent to the Western Electric 201B Data Set. The data set interface meets the requirements of the EIA 232A standard interface specification.	1, 2, and 3	Host System/360 must be equipped with an IBM 4657 Terminal Adapter, Type III (2400 bps).
3857 Expansion Panel	Permits the attachment of other special features, as follows: For 2848 Model 1: Six 3355 adapters. For 2848 Model 2: Four 3356 adapters. For 2848 Model 3: Three 3357 adapters.	1, 2, and 3	None

Figure 1-2. IBM 2848 Display Control Features (Sheet 1 of 2)

Feature Code	Feature Description	2848 Models to Which Feature Can Be Attached	Prerequisite 2848 Features
3858 Expansion Panel	Permits the attachment of other special features, as follows: For 2848 Model 1: Four 3355 adapters, one 7927 adapter. For 2848 Model 2: Three 3356 adapters, one 7927 adapter.	1 and 2	None
4787 Line Addressing	Permits the processor of the host system to select the first displayable position of any line within the CRT display of the 2260 Display Station as the starting location for the display of output data. The number of unique starting (or line) locations is: 2848 Model 1: 6. 2848 Model 2: 12. 2848 Model 3: 12.	1, 2, and 3	None
5340 Nondestructive Cursor	Provides control logic for the nondestructive cursor feature represented by the 5341 attached to the various display adapters. Allows the operator to move the cursor vertically and horizontally within the 2260 display.	1, 2, and 3	None Note: If the 5340 Nondestructive Cursor feature is attached to a 2848 Display Control, all display adapters used with the 2848 must be provided with the 5341 Nondestructive Cursor Adapter.
5341 Nondestructive Cursor Adapter	Permits movement of the cursor within the CRT display of the 2260 without disturbing or destroying the data displayed on the CRT.	Display Adapters: 3355 (Model 1) 3356 (Model 2) 3357 (Model 3)	One 5340 per 2848.
7927 Printer Adapter	Contains a buffer storage with a capacity of 960 characters and the logic required to control an IBM 1053 Printer. Provides a means of obtaining a permanent printed record of display group data under either program or operator control.	1 and 2	3858 Expansion Panel
7928 Printer Adapter	Same as 7927.	3	None
IBM 4656 Terminal Adapter, Type III	Enables System/360 to communicate with the 2848 Display Control via a communications data set link formed by Western Electric 202D Data Sets or their equivalent. Data transfer rate is 1200 bps (120 characters per second).	Attaches to 2701 Data Adapter Units that include 2701 feature No. 3815 (one 4656 or 4657 can be attached) or 2701 feature No. 3855 (two 4656 or 4657 adapters can be attached).	2848 Display Control attached to the same transmission line require the 9012 Data Set Adapter feature.
IBM 4657 Terminal Adapter, Type III	Same as 4656 except that the data set link must be formed by Western Electric 201B Data Sets or their equivalent. Data transfer rate is 2400 bps (240 characters per second).	Same as 4656.	2848 Display Controls attached to the same transmission line require the 9013 Data Set Adapter feature.
Language Features	See Appendix C.	1, 2, and 3	
4700 Isolation Feature	Permits application and removal of power without affecting program operation.	All Models using the channel adapter feature.	None

Figure 1-2. IBM 2848 Display Control Features (Sheet 2 of 2)

Model 2, which is used with either the Model 1 or Model 2 2848. Each model contains the type of CRT and related circuitry that matches the data capacity and character regeneration rate of the associated 2848 display control. Thus, a flicker-free display is assured whether the 2848 data capacity per display station is 960 characters (as in the Model 3 2848) or 240 or 480 characters (as in Models 1 and 2, respectively).

Optional features provide for the addition of an alphanumeric or numeric-only keyboard to the basic 2260 Display Station. This extends its capabilities to include man-to-machine communication, thus providing a complete visual I/O concept.

When an optional keyboard is included in the 2260 Display Station, input messages generated at the keyboard are displayed on the CRT as they are composed. This permits the operator to verify a message before it is transferred from the display group.

A total of 64 different characters can be displayed on the 2260 Display Station CRT:

- 26 alphabetical characters
- 10 numerical characters
- 25 special symbols (includes space and new-line symbol)
- 3 control symbols (cursor, check, and start-manual-input symbols)

Special Features

Two special features, 4766 and 4767, are available to supplement the basic 2260 Display Station. Each feature provides the display station with an input keyboard as described below. The alphanumeric and numeric keyboards are also available with the key designations, special characters, and keyboard arrangements required to complement the 2848 DC Language Features. (See Appendix C for a description of the language features.)

Feature 4766 Alphanumeric Keyboard

When optional feature 4766 is selected, the basic 2260 is fitted with the alphanumeric keyboard illustrated in Figure 1-3. The keyboard contains the 26 letters of the English alphabet, Arabic numerals 0-9, special symbol keys, and the control keys required to format and enter the input message.

Feature 4767 Numeric Keyboard

Optional feature 4767 equips the 2260 Display Station with the numeric keyboard illustrated in Figure 1-4. The keyboard contains Arabic numerals 0-9 and the same set of control keys provided in the 4766 alphanumeric keyboard.

Control Key Functions

The action that occurs when the various keyboard control keys are depressed is discussed in Chapter 6 for both the standard destructive cursor and the optional nondestructive cursor.

FUNCTIONAL DESCRIPTION

This operational description of the IBM 2260 Display Station and IBM 2848 Display Control display complex is at the block diagram level; it provides only enough detail to familiarize the reader with the broad concepts of equipment operation. A detailed discussion of display complex logic operation is provided in Chapter 2.

In the paragraphs that follow, the IBM 2260-IBM 2848 display complex is first discussed at a level wherein the 2260 and 2848 are represented as blocks to show the functional make-up of the 2848 and to illustrate the relationship of the System/360 Channel, the 2848, and the 2260. Next, an expanded block diagram illustrates the major logic areas within the 2848, and the function of each logic area shown is summarized. A similar block diagram analysis is provided for the IBM 2260. Finally, the data flow for a typical operation involving a maximum of display complex logic areas is described.

IBM 2848-2260 Display Complex

A typical IBM 2848-IBM 2260 display complex is illustrated in Figure 1-5. Note that the 2848 is configured to include the channel adapter, the 1053 Printer Adapter, and two display adapters. Either the channel adapter or the data set adapter must be selected as part of the 2848. The channel adapter is shown in Figure 1-5. Similarly, at least one display adapter must be included in the 2848; two are shown in the figure to permit a more comprehensive description of complex operation. The 1053 Printer Adapter has also been included although this adapter is optional. The IBM 2260's shown all include a manual input keyboard, which is optional.

All interchange between the System/360 channel and the 2848 is accomplished through the channel adapter. The channel adapter is capable of capturing common control under direction of the channel when the channel wishes to operate with a 2260 or with the 1053 Printer. The channel adapter also initiates communications with the System/360 under direction of a 2260 Keyboard.

The common control portion of the 2848 generates basic machine timing, governs the selection and gating of inputs from the keyboards of the associated display stations, and performs the control functions required for an orderly acceptance of

Figure 1-3. Optional Alphanumeric Keyboard for 2260 DS

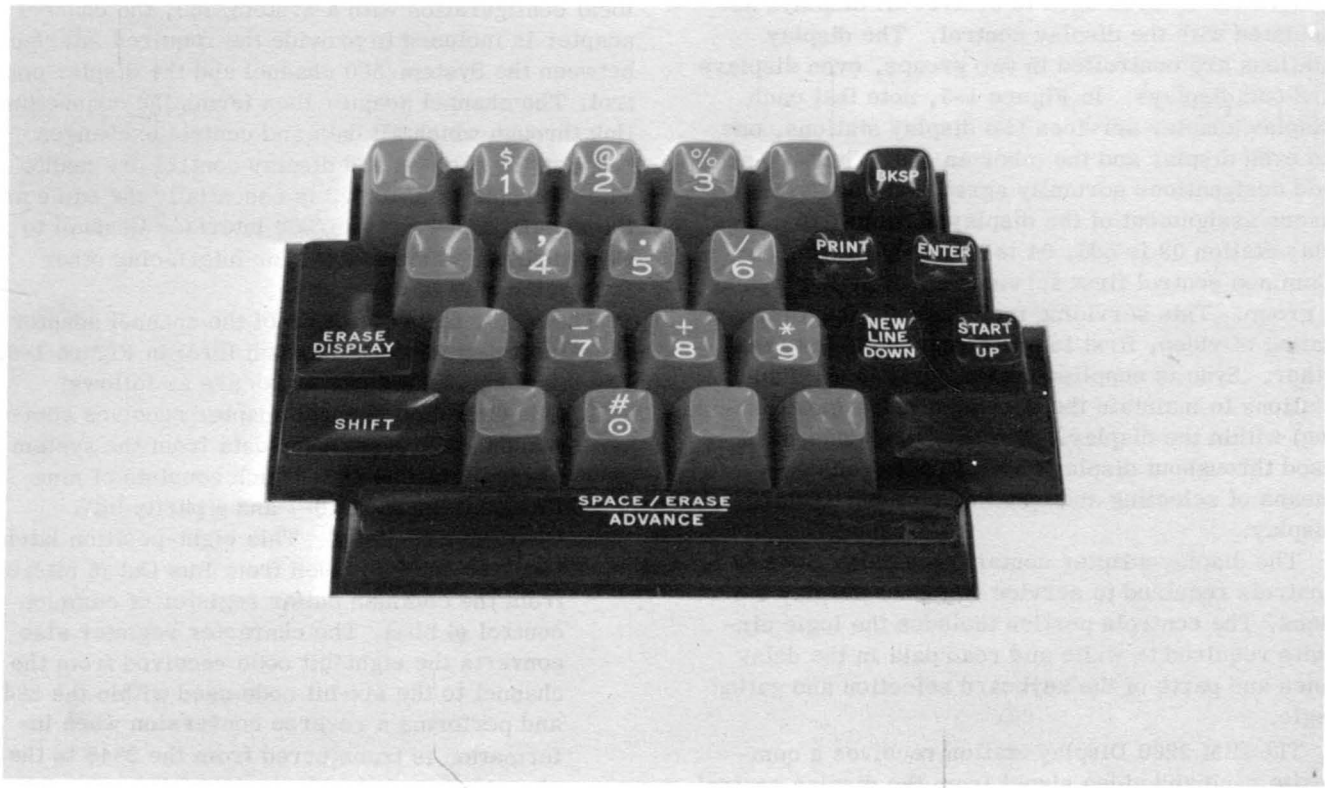


Figure 1-4. Optional Numeric Keyboard for 2260 DS

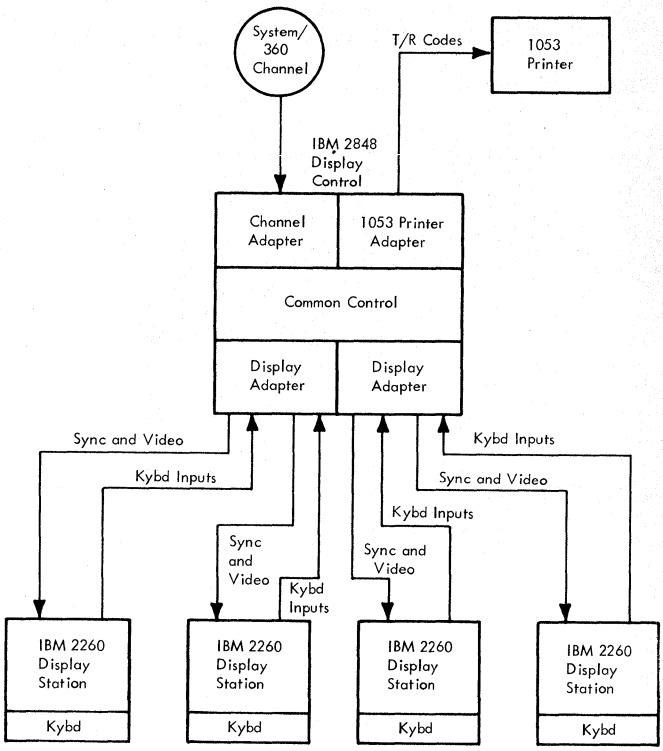


Figure 1-5. IBM 2848 - IBM 2260 Display Complex, Block Diagram

commands from the channel (via the channel adapter) and from the keyboards. Common control also generates the sync used to control all displays associated with the display control. The display stations are controlled in two groups, even displays and odd displays. In Figure 1-5, note that each display adapter services two display stations, one an even display and the other an odd. The even and odd designations normally agree with the device address assignment of the display station; i.e., Display Station 03 is odd, 04 is even, 05 is odd, etc. Common control first services all even displays as a group. This servicing includes only the alternate gating of video, first to one group and then to the other. Sync is supplied continuously to all display stations to maintain the desired sweeps (positioning) within the display. The even-odd concept is used throughout display control operations as a means of selecting and updating on a particular display.

The display adapter contains the delay lines and controls required to service two 2260 Display Stations. The controls portion includes the logic circuits required to write and read data in the delay lines and parts of the keyboard selection and gating logic.

The IBM 2260 Display Station receives a composite sync and video signal from the display control. This signal both controls the sweeps (display) on the CRT of the 2260 and transfers video that is to be displayed. Inputs to display control from the 2260 are present only when the 2260 is provided with a manual input keyboard. Then, these inputs consist of seven-bit bytes transferred as a result of a key depression at the keyboard. The seven-bit bytes contain either keyboard commands or data.

The 1053 Printer adapter contains the storage and controls required to permit control of a 1053 Printer by the channel or to print a hard copy of the contents of any display station's display.

IBM 2848 Display Control

The IBM 2848 is shown in block diagram form in Figure 1-6, with each major logical element represented as a block. The function of each block is discussed. Note that the 2848, as illustrated, includes the channel adapter, the 1053 Printer adapter, and two display adapters. The 2848 control and timing circuits are illustrated in Figure 1-7 and are discussed separately.

Channel Adapter

- Provides the required interface between System/360 channel and the IBM 2848 Display Control.
- All communication with the channel is accomplished through the channel adapter.

When the 2848 Display Control is to operate in a local configuration with a System/360, the channel adapter is included to provide the required interface between the System/360 channel and the display control. The channel adapter then forms the connecting link through which all data and control exchanges between the channel and display control are made. The interface established is essentially the same as the standard IBM System/360 Interface Channel to Control Unit, which is used for interfacing other I/O equipments to the system.

The major logic elements of the channel adapter are illustrated in block diagram form in Figure 1-6. The functions of the logic areas are as follows:

1. Bus Out: The channel adapter receives commands, addresses, and data from the system channel via Bus Out, which consists of nine lines (bit positions 0-7 and a parity bit).
2. Character Register: This eight-position latch register can be loaded from Bus Out (8 bits) or from the common buffer register of common control (6 bits). The character register also converts the eight-bit code received from the channel to the six-bit code used within the 2848 and performs a reverse conversion when information is transferred from the 2848 to the channel; i.e., six-bit to eight-bit conversion.
3. Command Decoder and Register: Decodes commands sent from channel via Bus Out and

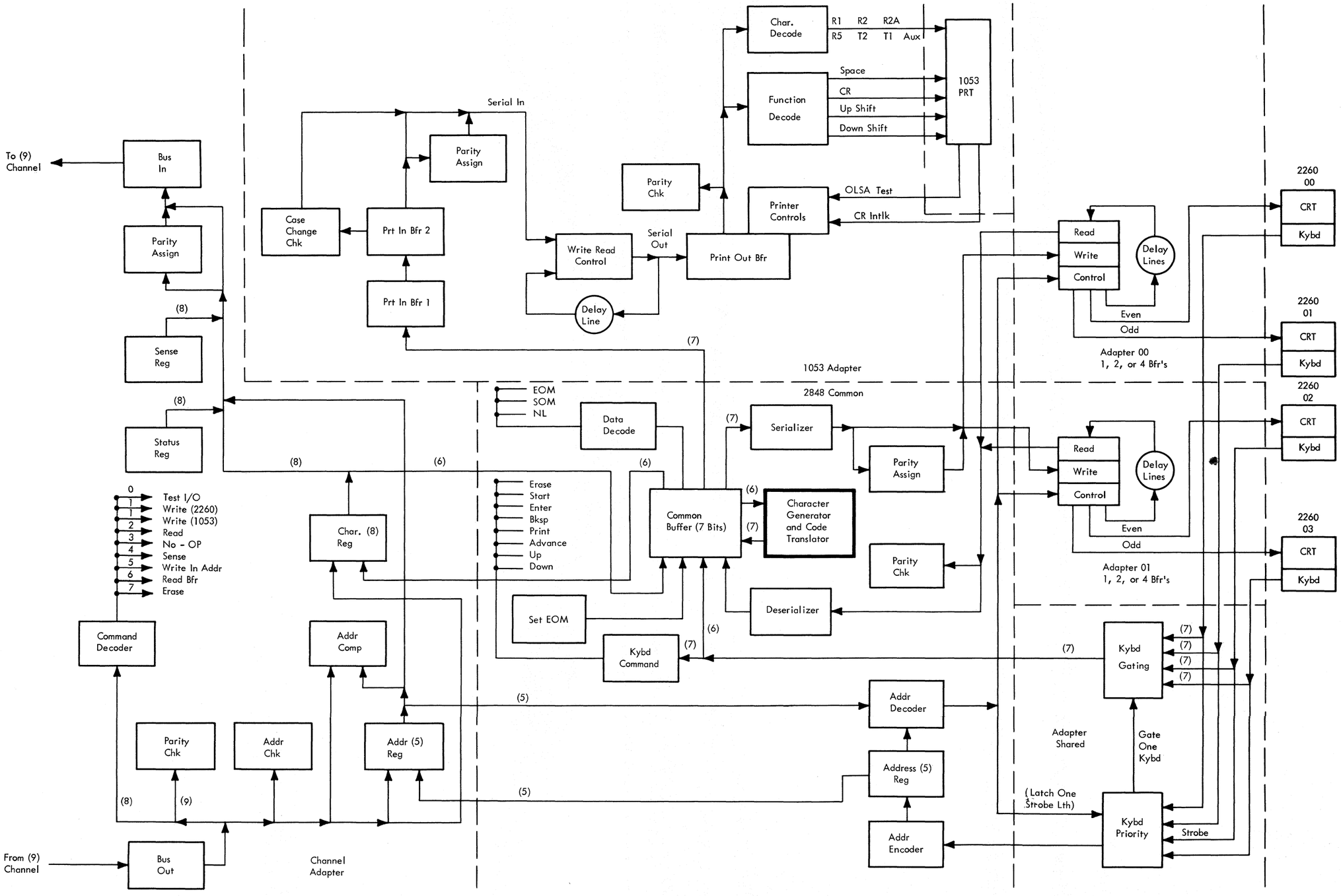


Figure 1-6. IBM 2848 - IBM 2260 Block Diagram

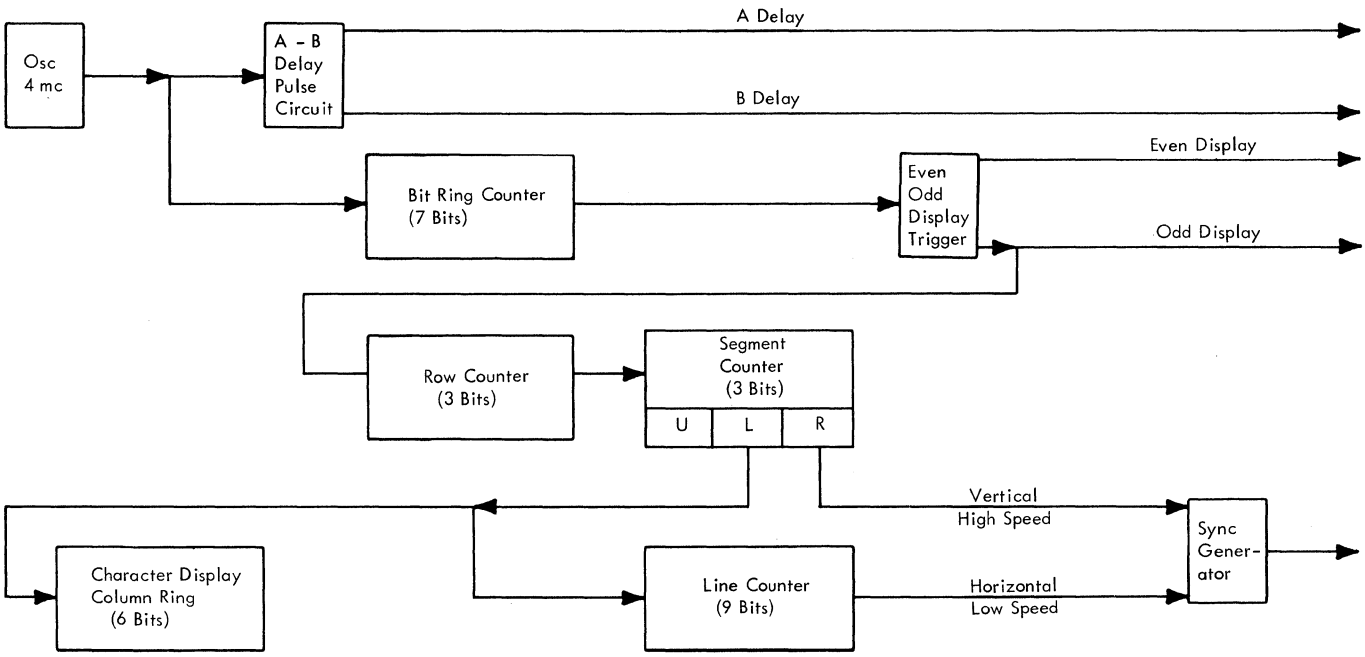


Figure 1-7. Timing and Clock Circuits, Simplified Block Diagram

sets command register latch associated with the command.

4. Bus Out Parity Check: Checks for odd parity of each byte sent to channel adapter via Bus Out.
5. Address Check: Detects unit address on Bus Out and enables address register and encoder circuits when unit address is decoded.
6. Address Register: Converts eight-bit address byte from channel into five-bit device address; sets address into address register for transfer to address decoder of 2848 common control.
7. Address Compare: Compares the address on Bus Out with contents of address register if a busy condition exists when the address is issued; if the addresses compare, a Device Busy latch is set, and a special sequence is entered. If an address compare is not made, the channel is presented with Control Unit Busy in the status byte.
8. Status Register: Records unit status for transfer to channel via Bus In.
9. Sense Register: Records information that amplifies unit status conditions indicated by the contents of the status register.
10. Parity Assign: Assigns odd parity to all eight-bit bytes transferred to the channel via Bus In.
11. Bus In: A nine-line path (bits 0-7 and a parity bit) over which all data transfers from the channel adapter to the System/360 channel are accomplished.

IBM 2848 Common

- Command and data inputs are received as six-bit bytes via the character register of the optional channel adapter.
- Address information is received as a five-bit byte from the channel adapter address register.
- Data and control information is transferred to the channel via the character register of the channel adapter.
- The address register of the channel adapter can be set with a five-bit address originating from the display control address register to identify the originating keyboard during Enter commands.
- Display common provides a seven-bit tilt-rotate code as an output to the 1053 Printer adapter.
- Accommodates up to 24 2260 Display Stations (2848 Model 1) and one 1053 Printer adapter.

The display common contains the control circuitry that is shared by the interface, printer adapter, and display stations (keyboards) to effect the various display operations. The major logical elements of display control are illustrated in block diagram form in Figure 1-6. Note that all communication with the System/360 channel is accomplished through the character register and address registers of the optional channel adapter. System/360, using the channel adapter as the connecting link, can configure

the common display control circuits to permit channel operation with any 2260 Display Station associated with the display control or with the 1053 Printer (via the optional 1053 Printer adapter).

The display common circuits can also be controlled by any associated display station provided with a keyboard. Then, display control permits data entry into, or modification of, the display data stored in the display station adapter. Display control also causes input messages to be sent to the System/360 channel via the channel adapter when this action is initiated at a display station keyboard (Enter command).

The functions of the major logic areas of display control are as follows:

1. Common Buffer: This seven-bit latch register serves as the hub for all data and control word transfers.
2. Data Decode: Senses contents of common buffer register for SOM, NL, and EOM codes except during Read Buffer commands.
3. Set EOM: Provides a means of setting the six-bit EOM code in the common buffer register when required by the operation being performed.
4. Character Generator and Code Translator: Converts the six-bit character code set in the common buffer register from either the channel (via channel adapter) or the keyboards into five 7-bit bytes, which are stored in the delay lines and used to generate video for character display; also performs code translations, e.g., six-bit character code to 1053 tilt-rotate code.
5. Serializer: Converts the contents of the common buffer register into serial data that can be written in the delay lines of the selected adapter.
6. Parity Assign: Assigns even parity to groups of data (slots) stored in the delay lines.
7. Parity Check: Checks for even parity as BCD data is read from the delay lines of the selected adapter for ultimate transfer to another location.
8. Address Encoder: Encodes a five-bit address used to select a display and to identify the active keyboard.
9. Address Register: This five-bit latch register is set from either the address encoder (keyboard operation) of the address register or the channel adapter (channel operation); also used to set address of originating keyboard in the channel adapter address register during keyboard Enter commands.
10. Address Decoder: Decodes the five-bit address to select a particular display station or the 1053 Printer.
11. Keyboard Priority: Determines which keyboard is to be serviced when more than one keyboard requests control of display control common.
12. Keyboard Gating: Accepts inputs from all associated keyboards on common bus; however, only the selected keyboard's outputs are gated through to keyboard command register.
13. Keyboard Command: Decodes keyboard command bytes and sets the command latch associated with the command.

The functions of the logic areas within the adapters illustrated in Figure 1-6 are as follows:

1. Delay Lines: Provide a storage medium for display data; provide video outputs to associated display station; provide six-bit BCD character codes during read operations.
2. Read Control: Controls the extraction of data from the delay lines.
3. Write Control: Controls the entry of data into the delay lines.

1053 Printer Adapter

- Permits the use of a 1053 Printer as a system output device under control of the channel.
- Provides hard copy of any 2260 Display Station's display upon direction either by the channel or from the display station keyboard (Print commands).

The functions of the 1053 Printer adapter logic elements, as illustrated in Figure 1-6, are as follows:

1. Print In Buffers 1 and 2: Used to buffer character inputs from display control to the printer adapter. The two buffers enable the printer adapter to accept inputs at a speed adequate for operation under control of the System/360 channel.

   When the character is in Print In Buffer 2, a check is made to determine whether a case-change (upper case to lower case, or lower case to upper case) is necessary. If a case-change must be made, a case-change character is inserted in the delay line before the character code is stored.
2. Parity Assign: Assigns odd parity to all characters written in the delay line; parity is stored with the character.
3. Delay Line: Provides a storage medium that permits proper message assembly and subsequent readout to the printout buffer.
4. Write-Read Control: Controls the storage of data in the delay lines (write) and subsequent extraction (read) of the data.
5. Printout Buffer: Provides a place for reassembling serial data (stored in the delay line) into the parallel character code required to print the character or cause the desired printer function.

6. Parity Check: Checks for odd parity in all bytes read from the delay lines to the printout buffer.
7. Character Decode: Detects the presence of nonfunction codes in the printout buffer and causes transfer of the code to the printer magnets.
8. Function Decode: Detects the presence of printer function codes in the printout buffer and causes the desired function to be performed.
9. Printer Controls: Controls the loading of print-in and printout buffers and the insertion of special characters (shift, carrier return, etc.) where required; includes a nine-bit ring counter which provides basic timing for printer adapter operations.

Control and Timing

The illustration of the common control area of the IBM 2848 in Figure 1-6 does not include the derivation of basic machine timing, which affects all areas and is significant enough to warrant separate illustration and discussion. Figure 1-7 illustrates the timing scheme. Figure 1-8 shows the odd and even displays and illustrates much of the timing discussed in the paragraphs that follow. The functions of the timing blocks in the figure are as follows:

1. Oscillator: Provides basic timing pulses at a frequency of 4.0 mc.
2. A-B Delay Circuits: Provide 2.0-mc A Delay and B Delay timing pulses 180 degrees out of phase.
3. Bit Ring Counter: This seven-bit ring counter is stepped at a rate of 4 mc; it is stepped alternately from 1 to 7 during even display readouts and from 1 to 7 during odd display readouts. The seven outputs of the bit ring counter are used throughout the machine as timing pulses and are used in bursts of 7 to write and read the delay lines of the display adapters.
4. Even-Odd Display Trigger: This trigger is complemented each time the bit ring counter reaches a count of 7. The outputs of the trigger are used to establish time intervals for operating with either the even or the odd display serviced by a display adapter.
5. Row Counter: Essentially, this counter keeps track of the horizontal rows of characters displayed on the CRT. Note that the row counter is stepped each time that the Even-Odd trigger is at Odd. This represents the indexing of (for example) row 1 on the even display, row 1 on the odd, and next (since the row counter is stepped upon odd display), row 2 of of the even display, row 2 of the odd, etc.
6. Segment Counter: The display is divided into three areas: upper, lower, and retrace. These designations represent the position of the vertical sweep: "upper" refers to the upper half of the display area, "lower" refers to the lower half of the display, and "retrace" refers to vertical retrace time during which the CRT beam must move from the bottom of the display area to the top. The segment counter is stepped each time the row counter has counted all the rows in a segment. (There are six rows in upper and six in lower, and the row counter continues to count during retrace time.)
7. Character Display Column Ring Counter: As shown in Figure 1-8, each character is composed of six lines within the display. These lines are designated as BCD, V1, V2, V3, V4, and V5. The character display column ring counter keeps track of which type of line (BCD or V1 (video 1), V2, V3, V4, or V5) is being displayed. The counter is stepped at the end of lower segment time since this represents the point at which the sweep of one particular line is ended.
8. Line Counter: This nine-bit line counter keeps track of a horizontal position within the display by counting vertical lines (or sweeps). The line counter is stepped at the end of lower segment time, which represents the end of a vertical sweep.

IBM 2260 Display Station

The IBM 2260 Display Station is illustrated in block diagram form in Figure 1-9. Note that its only interconnection with the 2848 Display Control is a composite signal which contains both video and the sync signals necessary to generate the vertical and horizontal sweeps for the CRT plus a character spacing signal. The composite signal is amplified and applied to the cathode of the CRT to effect the video presentation. Sync signals within the composite signal are extracted through the integrator and differentiator circuits shown as blocks in Figure 1-9. The horizontal and vertical deflection voltages (sweeps) are then developed and applied to the deflection coils of the CRT. The vertical sweep is very fast in relation to the horizontal sweep because, as can be seen in Figure 1-8, many vertical excursions of the beam are required for each horizontal pass across the tube.

The 12-kv high-voltage supply provides the high dc anode voltage required for CRT operation.

SYSTEM/360 - CHANNEL ADAPTER INTERFACE

- The I/O interface signal lines connect the channel adapter of the IBM 2848 Display Control to other control units and to the System/360 channel.
- The lines are functionally divided into five groups:
  1. Bus Out
  2. Bus In
  3. Tags
  4. Selection Controls
  5. Metering Controls
- All transfers of data and control information between the 2848 and the System/360 processor channel are made through these lines.

Understanding basic interface operation is essential to understanding the 2848 and, particularly, this section of the manual. This information is available in the Original Equipment Manual (OEM), IBM System/360 Channel Interface, Form A22-6843. Although an understanding of the basic interface is assumed, this information is reviewed in the following paragraph.

General

The I/O interface is a set of signal lines connecting an I/O control unit to the host System/360. The external cables physically connect all control units in a chain, with the first control unit being connected to a System/360 channel.

The signal lines of the I/O interface consist of an output and an input bus for passing information from channel to control units, tag lines for interlocking and for controlling the information on the buses, selection control lines for scanning or selecting the I/O device, and metering controls for conditioning the usage meters.

The following signal lines are used (the terms Out and In are in reference to the channel):

Line Name	Abbreviation	
Bus Out Position P	Bus Out P	Bus Out
Bus Out Position 0	Bus Out 0	
Bus Out Position 1	Bus Out 1	
Bus Out Position 2	Bus Out 2	
Bus Out Position 3	Bus Out 3	
Bus Out Position 4	Bus Out 4	
Bus Out Position 5	Bus Out 5	
Bus Out Position 6	Bus Out 6	
Bus Out Position 7	Bus Out 7	
Bus In Position P	Bus In P	Bus In
Bus In Position 0	Bus In 0	
Bus In Position 1	Bus In 1	
Bus In Position 2	Bus In 2	
Bus In Position 3	Bus In 3	
Bus In Position 4	Bus In 4	
Bus In Position 5	Bus In 5	
Bus In Position 6	Bus In 6	
Bus In Position 7	Bus In 7	
Address Out	ADR-OUT	Tags
Address In	ADR-IN	
Command Out	CMD-OUT	
Status In	STA-IN	
Service Out	SRV-OUT	
Service In	SRV-IN	
Operational Out	OPL-OUT	Selection Controls
Operational In	OPL-IN	
Hold Out	HLD-OUT	
Select Out	SEL-OUT	
Select In	SEL-IN	
Suppress Out	SUP-OUT	
Request In	REQ-IN	
Metering Out	MTR-OUT	Metering Controls
Metering In	MTR-IN	
Clock Out	CLK-OUT	

Line Description

The I/O interface signals are described in the following paragraphs and, for the sake of clarity, are defined as they appear at the input to the line terminators (LT's) of the 2848 Display Control. Regardless of their actual polarity, the lines are defined in positive terms: the "up" level represents a logical 1 or the presence of a condition; a "down" level represents a logical 0 or the absence of a condition.

Bus Out

Bus Out is a set of nine lines from the channel to all attached control units: eight information lines and one odd-parity line. This set of lines is used to transmit addresses, commands, and data to the control units.

The type of information transmitted over Bus Out is indicated by the outbound tag lines. When Address Out is up during the channel-initiated selection sequence, Bus Out specifies the address of the device for which the channel is attempting to initiate an operation. When Command Out is up during the channel-initiated selection sequence, Bus Out specifies a command. When Service Out is up in response to Service In during execution of a write or control

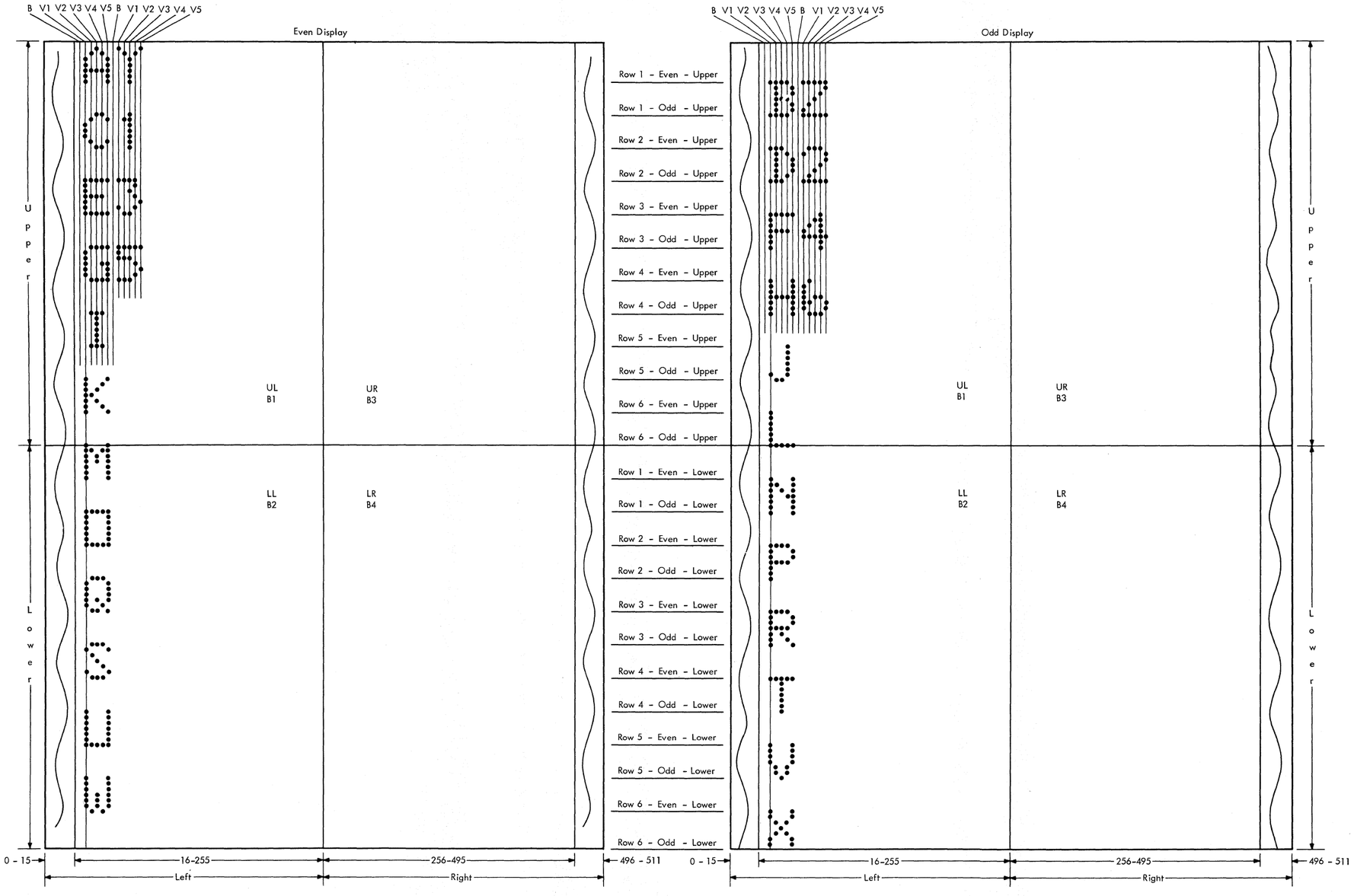


Figure 1-8. CRT Display Organization

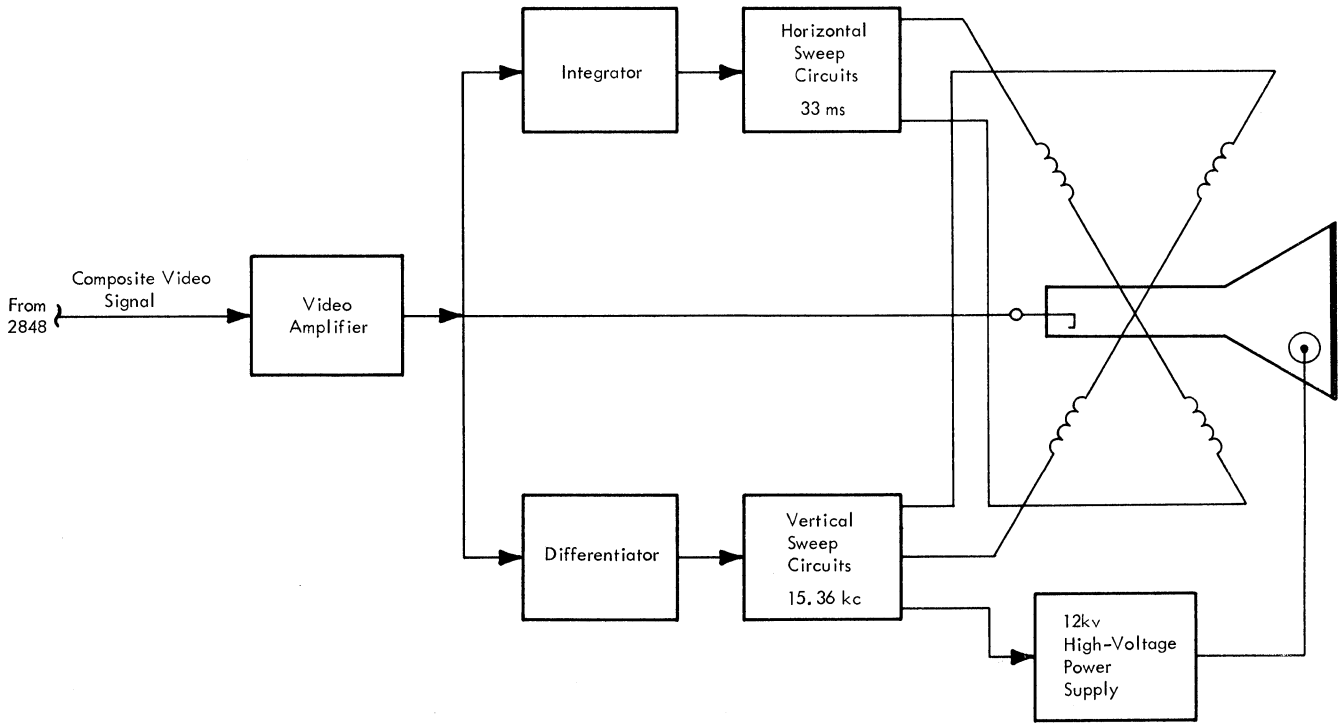


Figure 1-9. 2260 Display Station, Block Diagram

operation, the information on Bus Out depends on the type of operation. For example, during a write operation, it may contain data to be recorded by the device; during a control operation, it may specify a command code or a second-level address within the control unit or device.

The period during which information on Bus Out is valid is controlled by the tag lines. During transmission of the device address, information on the bus is valid from the rise of Address Out until the rise of Operational In or Select In or, when in a control-unit-busy selection sequence, until Status In drops. When the channel is transmitting any other type of information, the information on the bus is valid from the rise of the signal on the associated outbound tag line until the fall of the signal on the corresponding inbound tag line.

Bus In

Bus In is a set of nine lines from all attached control units to the channel: eight information lines and one odd-parity line. This set of lines is used to transmit addresses, status, and data to the channel. A control unit can place and maintain information on Bus In only when its Operational In line is up, except during the control-unit-busy selection sequence.

The type of information transmitted over Bus In is indicated by the inbound tag lines. When Address In is up, Bus In specifies the address of the currently selected device. When Status In is up, Bus In contains a byte of information describing the status of the device. When Service In is up during execution of a read or sense operation, the information on Bus In depends on the type of operation. During a read operation, it contains a byte of data from the remote device; during a sense operation, the bus contains a set of bits describing the detailed status of the device and the conditions under which the last operation was terminated.

Operational Out

Operational Out is a line from the channel to all attached control units and is used for interlocking. Except for the Suppress Out line, all lines from the channel are significant only when Operational Out is up. Whenever Operational Out is down, all In lines from the control unit must drop, and any operation currently working over the interface must be reset. Operational Out remains down until Operational In drops. The down state of both the Suppress Out and the Operational Out signals is used to reset all control units and attached devices. Unless the device is in Off Line mode, any down state of both these signals of sufficient duration to cause a response from the circuitry of the device provides the reset. To ensure a proper reset, the Operational Out and Suppress Out lines must both be down concurrently for at least 6 μs.

Request In

Request In is a line from all attached I/O control units to the channel; it is used to signal the channel when any control unit has data or status to be serviced. Request In can be signaled by more than one control unit at a time.

Request In is signaled from a control unit only if the control unit is ready to capture the interface and to present the status or data to be serviced. The Request In signal is removed by the control unit after it gains selection and has no further data or service requirements. Request In may not be up while Suppress Out is up if the request is due to an interrupt-type status. Suppress Out must degate Request In under these conditions.

Address Out

Address Out is a line from the channel to all attached control units; it serves two functions:

1. It is used to initiate selection of a device: The Address Out line signals the control unit to decode the address on Bus Out. The control unit, recognizing the address, must respond by raising its Operational In line when its incoming Select Out rises, except during Control Unit Busy. Address Out precedes the rise of Select Out by a minimum of 250 ns. Address Out can rise only when Select Out, Select In (except for item 2), and Operational In are down at the channel. Ultimate use of the address on Bus Out at the control unit is timed by the next rise of Select Out at the addressed control unit. The Address Out line must rise after the address is placed on Bus Out. Address Out must stay up until either Select In, Status In, or Operational In rises. Address Out cannot be up concurrently with any other outbound tag line.
2. It is used to disconnect operations from the interface: The Address Out line, with the down level of the Select Out or Hold Out line, signals the presently connected device to drop its Operational In line, thus disconnecting from the interface. Address Out remains up until Operational In drops. Operational In must drop within 6 μs after receiving the interface-disconnect indication. Status is generated and presented to the channel when appropriate.

If the channel is to perform Halt I/O, the channel must not execute the Interface Disconnect unless the operation is working; i.e., the Interface Disconnect must be executed only after the operation is initiated and before the end status is accepted.

A device may be so designed that it disconnects in response to the dropping of the Select Out line. In this case, the channel must execute a stop the next time an attempt is made to service the data. If Address Out is up 250 ns before Select Out drops, however, the control unit must recognize the Halt I/O.

Select Out

The control unit provides the option of connecting its selection logic in series on either the Select Out or Select In line. Descending-order priority from the channel can be established on the Select Out line, and the remaining control units can maintain an ascending-order priority from the channel on the Select In line. It is assumed that the selection logic is connected to the Select Out line. Also, Select Out is not considered active at the control unit unless Hold Out is up. If Hold Out falls while Select Out is active, Select Out will fall also.

Select Out is a line from the channel to the control unit having highest priority and from any control unit to the control unit next in priority. With the Select In line, Select Out provides a loop for scanning the attached control units. A control unit can raise its Operational In line only at the rise of its incoming Select Out signal. If a control unit does not require selection, it must immediately propagate the signal to the next control unit. Once a control unit propagates Select Out, it cannot raise its Operational In line until the next rise of the incoming Select Out line.

When an operation is being initiated by the channel, the rise of Address Out must precede the rise of Select Out by a minimum of 250 ns.

When the channel is scanning the attached control units, the Select Out line emanating from the channel is normally up. The channel must keep the Select Out line up until either Select In or any in-tag rises. When Select In rises, Select Out must drop and may not rise again until after Select In falls. When a control unit is selected, it raises its Operational In line. Select Out must drop so that Operational In may drop. After Select Out drops, however, the control unit must keep Operational In up until the current signal sequence is completed. A rise of the incoming Select Out in a control unit signals that the control unit can become selected to the channel by raising the Operational In line. If a control unit raises its Operational In line, it must suppress the propagation of Select Out to the next control unit.

Hold Out

Hold Out is a line from the channel to all attached I/O control units and is used to enable the Select

Out signal. Only when Hold Out is up can Select Out be considered active. Hold Out must gate the Select Out signal in the control units. Hold Out can be up only if Operational Out is up. Once Hold Out drops, it must not rise for at least 1.5 μs.

Select In

The control unit provides the option of connecting its selection logic in series on either the Select Out or Select In line. Ascending-order priority from the channel can be established on the Select Out line, and the remaining control units can maintain a descending-order priority from the channel on the Select In line. For clarity, it is assumed here that the selection logic is connected to the Select Out line.

Select In is a line from the lowest-priority control unit to the channel. It is the outgoing Select Out line of that control unit and provides for the Select Out signal a return path to the channel. The definition of the Select In line is the same as that of a Select Out line emanating from any control unit.

Operational In

Operational In is a line from all attached control units to the channel; it is used to signal the channel that a device has been selected. It must stay up for the duration of the selection. The selected device is identified by the address byte transmitted over Bus In.

Rise of Operational In indicates that a control unit is selected and is communicating with the channel. This communication can consist of one or a combination of three signal sequences: response to address on Bus Out, request for data on Bus Out, offer of data and/or status on Bus In.

Operational In can rise only when the incoming Select Out to the control unit is up and the outgoing Select Out is down; i.e., the control unit must raise Operational In in response to the rise of Select Out and must block Select Out from passing to the next control unit. Operational In can drop only after Select Out drops.

When Operational In is raised for a particular signal sequence, it must stay up until all required information is transmitted between the channel and the device. Operational In must drop at that time or after the rise of the outbound tag associated with the transfer of the last byte of information, if Select Out is down.

Signals on Bus In and on the inbound tag lines are significant only when Operational In is up, except during the control-unit-busy selection sequence. When Operational In is down, the channel must disregard any signals on these lines. On the other hand, each control unit must provide interlocks to ensure that it does not place any signals on Bus In and the incoming tag lines unless its Operational In line is up.

Address In

Address In is a line from all attached control units to the channel; it is used to signal the channel when the address of the currently selected device has been placed on Bus In. The channel responds to Address In by means of Command Out.

The rise of Address In indicates that the address of the currently selected device is available on Bus In. Address In must stay up until the rise of Command Out. Address In must fall in order that Command Out may fall. Address In cannot be up concurrently with any other inbound tag line.

Command Out

Command Out is a line from the channel to all attached control units; it is used to signal the selected device in response to a signal on the Address In, Status In, or Service In lines. A signal on the Command Out line indicates to the selected device that the channel has placed a command byte on Bus Out. The command byte has a fixed format.

The rise of Command Out indicates that the information on Bus In is no longer required to be valid and indicates that a command byte is available on Bus Out. Command Out must stay up until the fall of the associated Address In, Status In, or Service In signal. It cannot be up concurrently with any other outbound tag line.

When Command Out responds to Address In during a channel-initiated selection sequence, the command byte contains the operational command to be performed. At any other time, a Command Out response to Address In means "proceed". A Command Out response to Service In always means "stop". A Command Out response to Status In means "stack", indicating that the control unit is to hold its status conditions. The control unit selects the interface to present the stack status only if Suppress Out and Address Out are down when Select Out rises at the control unit.

Status In

Status In is a line from all attached control units to the channel; it is used to signal the channel when the selected device has placed status information on Bus In. The status byte has a fixed format and contains bits describing the current status at the control unit. The channel responds with either Service Out or Command Out, depending on whether it accepted the status.

The rise of Status In indicates that a byte of status information is available on Bus In. Status In cannot be up concurrently with any other inbound tag line. Status In must stay up until the rise of an out tag or, during the control-unit-busy selection sequence, until Select Out falls. It must fall in order that the responding out tag may fall. During the control-unit-busy selection sequence, status on Bus In must be valid until Select Out falls.

Service Out

Service Out is a line from the channel to all attached control units; it is used to signal the selected device in recognition of a signal on the Service In or Status In line. A signal on the Service Out line indicates to the selected device that the channel has accepted the information on Bus In or has provided on Bus Out the data requested by Service In.

When Service Out is sent in response to Service In during read or sense operations or to Status In, the Service Out signal must rise after the channel accepts the information on Bus In.

In these cases, the rise of Service Out indicates that the information is no longer required to be valid on Bus In and is not associated with any information on Bus Out. When Service Out is sent in response to Service In during a write or control operation, the rise of Service Out indicates that the channel has provided the requested information on Bus Out. In this case, the signal must rise after the information is placed on the bus. The information on Bus Out is always of the type requested by Service In and is used in the process of executing the current operation. Service Out must stay up until the fall of the associated Service In or Status In signal. Service Out cannot be up concurrently with any other out tag.

A Service Out response to Status In while Suppress Out is up indicates to the control unit that the operation is being chained. See "Suppress Out" for further details. The status is accepted by the channel.

Service In

Service In is a line from all attached control units to the channel; it is used to signal the channel when the selected device wants to transmit or receive a byte of information. The nature of the information associated with Service In depends on the operation and the device. The channel must respond to Service In by Service Out, by Command Out, or, during an interface disconnect, by Address Out.

During Read and sense operations, Service In rises when information is available on Bus In. During write and control operations, Service In rises when information is required on Bus Out. Service In cannot be up concurrently with any other inbound tag line. Service In must stay up until the rise of Service Out, Command Out, or Address Out, whichever occurs first; it can only fall after the rise of one of these signals.

As with cyclic devices, when the channel does not respond in time to the preceding Service In, an overrun condition occurs. This condition must be recognized by the (cyclic) device. In any case, Service In must not drop if an out-tag has not risen, nor may it rise if Service Out has not dropped.

Suppress Out

Suppress Out is a line from the channel to all attached control units; it is used both alone and in conjunction with the Out Tag lines to provide the following special functions:

1. Suppress Status: Interruption-type status is suppressed, and selection of the interface to present the status cannot be attempted as long as Suppress Out is up when Select Out rises at the control unit. Suppress Out must be up when Select Out rises at the control unit to ensure suppression of status. If Suppress Out rises after a status cycle is started, the Status Cycle signal sequence proceeds normally. Suppress Out also causes Request In to drop if Request In is up for interruption-status condition.
2. Chained Command Control: If Suppress Out is up when Service Out responds to Status In, a chained command is indicated. If Suppress Out is up for a Device End status, chaining is indicated only until the Suppress Out line falls or reselection is made (Operational In rises). Depending on the particular device, on the operation, and on the configuration, the chained-command indication requires certain functional control at the control-unit level. If chaining is indicated when Channel End status is presented (Device End not yet generated) from a multidevice control unit, the device presenting Channel End must be the next one to present Device End status, unless the control unit is addressed in the meantime on the same interface. If chaining is indicated on a device shared by more than one control unit or channel, the device must remain available until the chaining operation is initiated or chaining is no longer indicated.

Clock Out

Clock Out is a line from the channel to all attached control units; it is used to indicate when the CPU is not stopped and not waiting. Thus, the assignable unit may not change from the enabled state to the

disabled state, or vice versa. The Clock Out line is used only by units that have the interface isolation feature installed. Otherwise Clock Out is jumpered to the next control unit.

Metering In

Metering In is a line from all attached control units to the channel. This signal is passed through to the CPU cluster and, when present, causes the CPU cluster meter to accumulate time even though the CPU may be stopped or waiting. Metering In is used to indicate when the assignable unit is busy or an operation is in progress. An assignable unit meter's running does not necessarily activate the Metering In line, as may be the case in an off-line customer operation.

Metering Out

Metering Out is a line from the channel to all attached control units; it is used to condition all control unit and device meters to run. The signal is present whenever the CPU customer meter is running. The Metering Out line is not used by the 2848 but is jumpered out to the next control unit.

ADDRESSING

The 2848-2260 display complex in a local environment uses standard System/360 addressing and selection sequences. The 2848 Display Control and attached devices (2260 Display Stations and the optional 1053 Model 4 Printer) are addressed by eight-bit address bytes of preassigned configurations. The 2848 and each of its attached devices are adapted at time of installation to accept and respond to only an assigned address.

The 2848 is addressed by one or two (two if more than 16 devices are attached to the 2848) distinct configurations of the four high-order bits of the address byte. The attached 2260's and the 1053 Printer are assigned sequential configurations of the four low-order bits starting at 0000. If more than 16 devices, including the 1053 Printer, are attached to a 2848, a second configuration of the four high-order bits is assigned to the 2848, and the additional devices are assigned sequential configurations of the four low-order bits, again starting with 0000. Thus, a 2848 Display Control with more than 16 devices appears to the channel as two display groups. An example of address assignments for a 2848 Display Control Model 1 with the maximum number (24) of 2260 Display Stations and a 1053 Printer attached is shown in Figure 1-10.

Address Byte (EBCDIC)		Device
(High-Order) 2848 Address	(Low-Order) Device Address	2260 Display Station or 1053 Model 4 Printer*
0000	0000	1
0000	0001	2
0000	0010	3
↓	Continued Sequentially Through	↓
0000	1111	16
0010	0000	17
0010	0001	18
0010	0010	19
0010	0011	20
0010	0100	21
0010	0101	22
0010	0111	23
0010	1000	24
0010	1001	25

*The 1053 Model 4 Printer must be assigned highest-order address.

Figure 1-10. Typical Address Assignments, Model 1 2848 DC

COMMANDS AND COMMAND OPERATION

This section discusses the basic commands that can be executed by the 2848-2260 display complex. The commands and their code structure are listed in Figure 1-11.

The operation to be performed by the display complex is determined by an eight-bit command byte issued by the channel to the 2848. The low-order bits of a command byte define the basic operation. The high-order bits are used to expand (modify) an operation.

Each command received by the 2848 is tested for correct parity and command validity. The following summarizes the action taken when an invalid command or a command byte of incorrect parity is detected by the 2848:

1. Invalid Command or Command Modifier - The operation is not performed. Unit Check is set in the Status byte. Command Reject is set in the Sense byte.
2. Command Parity Error - The operation is not performed. Unit Check is set in the Status byte. Bus Out Check is set in the Sense byte.

If a command other than Test I/O is presented to the 2848 while the 2848 interface is in Busy status, the command is not accepted nor checked for validity or parity. The Busy bit and current status are presented to the channel. The Test I/O command, however, is accepted when presented to the busy device. The Test I/O command is checked for parity and validity, and it causes the 2848 Status byte to be transferred to the channel.

Command	EBCDIC Code Structure								Feature Required
Bits:	0	1	2	3	4	5	6	7	
Test I/O	0	0	0	0	0	0	0	0	
Write DS Buffer Storage	0	0	0	0	0	0	0	1	
Write 1053 Buffer Storage	0	0	0	0	0	0	0	1	Printer Feature
Sense	0	0	0	0	0	1	0	0	
Write DS Line Address	0	0	0	0	0	1	0	1	Line-Address Feature
Read DS MI	0	0	0	0	0	0	1	0	Keyboard Feature*
Short Read DS MI	0	0	0	0	1	0	1	0	Keyboard Feature*
Read Full DS Buffer	0	0	0	0	0	1	1	0	
No Op	0	0	0	0	0	0	1	1	
Erase DS Buffer Storage	0	0	0	0	0	1	1	1	

*To transfer data using the Read DS MI or Short Read DS MI command, the keyboard ENTER key of the selected 2260 DS must be depressed.

Figure 1-11. Commands and Their Code Structure

Write DS Buffer Storage Command

The Write DS Buffer Storage command is used to transfer data from the channel to the 2848-2260 display complex for presentation on the screen of the selected 2260 Display Station. This command causes the transfer of data from the channel to the 2848 Display Control under channel byte count control. Data bytes are parity-checked by the 2848 as they are received. The data bytes are converted to video data and placed in the buffer storage of the selected 2260 Display Station at the location in storage indicated by the cursor. Character data is displayed on the 2260 screen upon its entry into buffer storage.

The cursor automatically advances to the next displayable position as character data is placed in buffer storage and displayed on the 2260 screen. If a message length exceeds the displayable positions between the cursor and the last displayable position on the screen, a wraparound condition occurs. That is, the message data that exceeds the displayable positions replaced previously written data, beginning at the first displayable position.

A Write DS Buffer Storage operation is terminated by Channel Byte Count Control. The byte counter is set before execution of the Write command with a byte count (number of characters contained in the message). As data bytes are transferred from the channel to the 2848, the byte counter is decremented by 1 for each data byte transfer. When the byte counter reaches zero, Channel Byte Count Control initiates the Stop Sequence. The Stop Sequence halts transmission of data bytes and causes Channel End and Device End to be set in the 2848 Status byte for presentation to the Channel. The character data written in the 2260 buffer storage is continuously displayed and regenerated until erased or replaced by other data.

If, during a Write operation, a parity error is detected, a check symbol is displayed in place of the character in error. The operation is not terminated when a parity error is detected. However, at the conclusion of the operation, Unit Check, along with the Channel End and Device End, is set in the 2848 Status byte. Bus Out Check is set in the 2848 Sense byte. Of the 256 possible configurations of the 8-bit data byte, only those defined in Figure 1-13 should be used for transfer to the 2848-2260 Display Complex during a Write operation.

The presence of more than one EOM symbol on a 2260 screen can cause premature or incorrect termination of a Read DS MI, Short Read DS MI, or 2260-to-printer operation. Thus, the transfer of the bit configuration for the EOM symbol during a Write DS Buffer operation should be avoided.

The transfer of the bit configuration for the Start MI symbol should also be avoided if it is likely to cause more than one Start MI symbol to be displayed on a 2260 screen. The presence of more than one Start MI symbol on a 2260 screen may cause other than desired results during a Read DS MI or Short Read DS MI operation.

Write 1053 Buffer Storage Command

The Write 1053 Buffer Storage command is used to transfer data from the channel to the 1053 Printer for printing. This command causes the transfer of data from the channel to the 2848 under Channel Byte Count Control. Data bytes are parity-checked by the 2848 as they are received, converted to the Tilt and Rotate code, and placed in the 1053 buffer storage. The required shift characters are automatically inserted.

The 1053 Printer begins printing upon receipt of the first data byte in the 1053 buffer storage. The 1053 buffer storage accepts data bytes at an average rate of 360 characters per second up to its capacity of 1223 bytes (including control and shift bytes).

Upon reaching buffer capacity, data is accepted at the output print rate of the Model 4 1053 Printer (nominally 14 characters per second).

While the 1053 is printing, the Busy bit is set in the 2848 Status byte and will be presented to the channel in response to a Write 1053 Buffer Storage command.

The Write 1053 Buffer Storage operation is terminated when the byte counter (Channel Byte Count Control) is reduced to zero. When this occurs, the Stop sequence is generated by the channel. The 2848 Display Control responds to the Stop sequence by setting Channel End and Device End in the 2848 Status byte.

At the completion of the print operation, the 1053 Printer automatically advances to a new line, and the print mechanism (type head) is restored to the first print position.

If, during a Write 1053 Buffer Storage operation, a data byte of incorrect parity is detected by the 2848, the following occurs:

1. The 1053 Printer prints a quote (") symbol (last character printed) to indicate an incomplete message and discontinues printing.
2. The 1053 buffer storage is cleared.
3. Data bytes continue to be transferred from channel to 2848 until the channel byte counter decrements to zero. However, they are not printed or placed in the buffer.
4. At the end of data transfer from channel to 2848, Channel End, Device End, and Unit Check are set in the 2848 Status byte. Bus Out Check is set in the 2848 Sense byte.

If a Write 1053 Buffer Storage command is presented to the 2848 when the 1053 Printer is in a Not Ready status (out of paper, or power off), Unit Check is set in the 2848 Status byte. Intervention Required is set in the Sense byte. When the 1053 Printer is readied, Device End is set in the 2848 Status byte, indicating its Ready status.

The 2260 Display Station print requests are queued when initiated during a Write 1053 Buffer Storage operation. The print requests are accepted when Channel End and Device End are presented to the channel (at the completion of the Write 1053 Buffer Storage operation).

Write DS Line Address Command

To accept and execute the Write DS Line Address command, the 2848 Display Control must be equipped with the line-addressing feature. If the feature is not present, Command Reject is set in the Sense byte, and Unit Check is set in the Status byte.

The Write DS Line Address command combines the Write DS Buffer Storage command with 2260 line selection capabilities, thus enabling selection of a specific 2260 display line as the beginning line of a message.

The Write DS Line Address command causes the cursor to be positioned in the first displayable position of the addressed line (line address is specified by the first data byte following the Write DS Line Address command). Subsequent message data is displayed beginning at the addressed line.

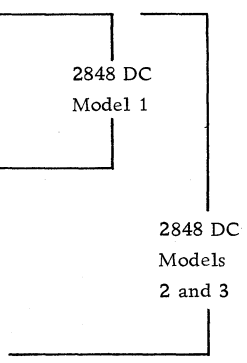
With the exception of command byte format and the positioning of the cursor (caused by the first data byte), the Write DS Line Address command is operationally the same as the Write DS Buffer Storage command.

The Write DS Line Address command provides for selection of up to 12 line addresses (the maximum number of displayable lines on 2260's attached to a Model 2 or Model 3 2848 Display Control). However, 2260's attached to a 2848 Display Control Model 1 display only six lines; therefore, the use of line addresses above six should not be used in a display complex controlled by a 2848 Display Control Model 1.

Listed below are the 12 possible line addresses and the data byte format for each:

DATA BYTE FORMAT (EBCDIC)

P	0	1	2	3	4	5	6	7	Selected Line
1	1	1	1	1	0	0	0	0	One
0	1	1	1	1	0	0	0	1	Two
0	1	1	1	1	0	0	1	0	Three
1	1	1	1	1	0	0	1	1	Four
0	1	1	1	1	0	1	0	0	Five
1	1	1	1	1	0	1	0	1	Six
1	1	1	1	1	0	1	1	0	Seven
0	1	1	1	1	0	1	1	1	Eight
0	1	1	1	1	1	0	0	0	Nine
1	1	1	1	1	1	0	0	1	Ten
1	1	1	1	1	1	0	1	0	Eleven
0	1	1	1	1	1	0	1	1	Twelve



Read DS MI (Manual Input) Command

The Read DS MI command is used to transfer manually entered messages and data from a 2260 Display Station buffer to the channel. This command is issued in response to depression of the ENTER key on a 2260 keyboard. The command causes all character data (except data on the same line as, and to the right of, a New Line Code) displayed between the start symbol and the cursor of the selected 2260 to be transferred to the channel. The Read DS MI operation is terminated when the cursor is detected by the 2848 Display Control. However, transmission of data to the channel is terminated (at the risk of an incomplete message) if the channel byte counter is set at a value that permits the byte counter to reach zero before the cursor is detected.

At the completion of the operation (cursor detected), Channel End and Device End are presented to the channel, the start symbol is deleted from the 2260 CRT, and the keyboard of the selected 2260 is restored.

If, during the operation, a 2260 buffer parity error is detected, the operation will continue. However, at the conclusion of the operation, Unit Check will be set in the 2848 Status byte along with Channel End and Device End. Equipment Check will be set in the 2848 Sense byte.

If a Read DS MI command is given and the ENTER key is not honored or not depressed, a zero-length word message is transferred to the processor. This condition also exists when an Enter is honored and a start symbol is absent on the screen of the selected 2260.

Short Read DS MI Command

The Short Read DS MI command is similar to the Read DS MI command since it is used to transfer manually entered data from a display station buffer to the channel. However, the Short Read DS MI command provides greater data input capabilities than the Read DS MI command because it requires less 2848 process time for execution.

The process time savings (33.0 to 49.7 ms per operation) is gained by omitting the Start MI symbol deletion function that is performed during a Read DS MI operation. Thus, at the conclusion of a Short Read DS MI operation, the Start MI symbol is not automatically deleted, as in a Read DS MI operation, but remains on the 2260 screen.

The Short Read DS MI command, when issued in response to Attention status (keyboard Enter key depressed), causes all data displayed between the Start MI symbol and the cursor of the selected 2260 to be transferred to the channel, except data between an NL symbol and the right end of the display line containing the symbol. The Short Read DS MI operation is terminated when the EOM symbol is detected by the 2848 Display Control.

NOTE: If the channel byte counter is set at a value that permits it to reach zero before the cursor is detected, data transfer is stopped, but the operation will continue to a normal ending; i.e., until the cursor is detected. If this occurs, an incomplete message will be transferred to the channel.

Upon completion of the Short Read DS MI operation:

1. Channel End and Device End are presented to the channel.
2. The cursor is advanced one display position, but is not visible. An EOM symbol is located in the position previously occupied by the cursor.
3. The Start MI symbol is not deleted from the 2260 screen, as in the Read DS MI operation, but remains in the display position it initially occupied.
4. The keyboard of the selected 2260 is restored (unlocked), indicating that the operation has concluded.

If a 2260 buffer parity error is detected during a Short Read DS MI operation, Unit Check will be set in the 2848 Status byte along with Channel End and Device End. Equipment Check will be set in the 2848 DC Sense byte.

Two conditions must prevail before a Short Read DS MI operation can be performed:

1. The Enter key of the selected 2260 must have been depressed.
2. A Start MI symbol must be displayed on the screen of the selected 2260.

If a Short Read DS MI command is given in the absence of one or both of these conditions, the operation is not performed. Device End and Channel End are presented to the channel.

During manual entering operations (using the Short Read DS MI command) on machines wired with the destructive cursor, an End of Message (EOM) symbol appears in the display position previously occupied by the cursor, and, at the conclusion of the operation, the cursor is placed one display position beyond the EOM symbol. (That is, a nondisplayable control bit, used within the 2848 DC to distinguish the cursor from the EOM symbol, is located one position beyond the EOM symbol.) The cursor is not visible at this time; however, if a character were entered, it would appear one position beyond the EOM symbol, and the cursor would be visibly displayed one position beyond the character.

Since the EOM symbol and the cursor look alike and are interpreted by the 2848 DC as the end of a message, the presence of both on the same screen can cause operator confusion and possibly an incorrect termination of a subsequent operation. For these reasons, the EOM symbol should be deleted from the 2260 screen, either manually or by programming, following each operation.

It is also recommended that an unsolicited Read DS MI command not be issued following a Short Read DS MI command unless the start of message (SOM) symbol is first deleted.

During manually entered operations on machines wired with the nondestructive cursor, an EOM symbol is inserted in the display position indicated by the nondestructive cursor, and, at the conclusion of the operation, the cursor is placed one

position beyond the EOM symbol. To avoid an incorrect termination of a subsequent operation, the EOM symbol should be deleted from the screen, either manually or by programming, following each operation.

It is also recommended that an unsolicited Read DS MI command not be issued following a Short Read DS MI command unless the SOM symbol is first deleted.

Read Full DS Buffer Command

The Read Full DS Buffer command causes all character data displayed on the screen of the selected 2260 Display Station to be transferred to the channel. Data transfer starts at the first displayable position (upper-left corner of the 2260 screen) and ends at the last displayable position (lower-right corner of the screen).

Included in the characters transferred are the check symbol, start symbol, and the destructive cursor (EOM symbol). The nondestructive cursor is not transferred. Spaces between characters and the blank positions between the last character displayed and the last displayable position on the screen are transferred as spaces.

The Read Full DS Buffer operation is terminated when the last position of the buffer is sensed (position 240, 480, or 960 for 2848 Models 1, 2, and 3, respectively). However, data transmission will be stopped, at the risk of transferring an incomplete message, if the byte counter (channel byte count control) is set at a value that permits it to be reduced to zero before the last buffer position is sensed.

At the conclusion of a Read Full DS Buffer operation, Channel End and Device End are presented to the channel, and the cursor is placed in the first displayable position on the 2260 screen.

If, during performance of the Read Full DS Buffer command, a buffer parity error is detected, the operation continues until the last buffer position is sensed. However, at the conclusion of the operation, Unit Check, Channel End, and Device End are placed in the 2848 Status byte. Equipment Check is placed in the 2848 Sense byte.

No Op (No Operation) Command

The presentation of the No Op command causes the 2848 Display Control to respond with the normal ending sequence (Channel End and Device End). Data is not transferred.

Erase DS Buffer Storage Command

The Erase DS Buffer Storage command causes all character data displayed on the screen of the selected 2260 Display Station to be erased and the cursor to be placed in the first displayable position. At the conclusion of the Erase DS Buffer Storage operation, the cursor appears in the first displayable position of the 2260 screen, and the remainder of the display is blank. Channel End and Device End are placed in the 2848 Status byte.

Sense Command

The Sense command causes the 2848 Display Control Sense byte to be transferred to the channel for program analysis. The Sense byte is explained under the heading, Sense and Status Bytes.

Test I/O Command

The Test I/O command causes the 2848 Display Control Status byte to be transferred to the channel. The Test I/O command also resets the Status byte. The Status byte is explained under the heading, Sense and Status Bytes.

Interleave Read

The interleave read operation (sometimes called read pause) is a built-in feature which allows keyboard servicing during execution of a Read MI or Read Buffer command. This is accomplished by interrupting the read command (Read MI or Read Buffer) at the end of each row for approximately 32ms. During this time, keyboards are serviced, thus reducing the probability of keyboard lockout. After the 32ms time period has elapsed, the read operation is continued.

The overall operation of the interleave read sequence begins when the last character of any row has been transferred from the control unit to the local interface. A line-16 search is initiated to continue either the Read MI or Read Buffer command. Because a line-16 search has been initiated coincidentally with a Read command, the Read Pause latch is set (C9.05.62.1). The output of this latch is AND'ed with the Display Compare signal to write the TIC in the first character position of the next row. This action temporarily terminates the read command and identifies the character from where the read operation will be resumed once the keyboards have been serviced.

Keyboards are serviced on the basis of priority when their associated TIC is found. While keyboards are being serviced, local interface selection is inhibited for 26ms by the output obtained from a single-shot (C9.5.36.1). When the single-shot times out, keyboard servicing is terminated. The remaining time in the frame (approximately 7.3ms) is used to prepare the control unit to resume read

operations to the local interface. The first character to be transferred to the local interface is identified by TIC.

CHANNEL-DISPLAY COMPLEX - SEQUENCES AND RESPONSES

This section discusses sequences and responses that occur between the channel and the 2848-2260 display complex and are directly related to, or influence, device operation.

Stop Sequence

The Stop sequence is initiated by channel byte count control and is used to terminate an operation involving data transfer. The Stop sequence is initiated when the byte counter is decremented to zero. (The byte counter is set with a value equal to the number of data bytes to be transferred and decremented by 1 with each transfer.)

Write commands are normally terminated by the Stop sequence; i.e., the occurrence of the Stop sequence causes the 2848 Display Control to proceed to a normal end sequence (Channel End and Device End in the 2848 Status byte).

The Stop sequence terminates the transfer of data from the 2848 to the channel. However, it does not conclude a Read operation within the 2848. Read operations are brought to a normal end sequence by detection of the cursor or by detection of the last buffer position for the Read DS MI or Short Read DS MI and the Read Full DS Buffer Storage commands, respectively. The occurrence of the Stop sequence prior to detection of the cursor or last buffer position may result in an incomplete message being sent to the channel. It is recommended, therefore, that before a Read operation, the byte counter be set at a value equal to or greater than the buffer capacity of the 2260 Display Station.

Interface Disconnect Sequence

The Halt I/O instruction causes the Interface Disconnect sequence to be generated by the channel. The Interface Disconnect sequence causes termination of all data and signals between the channel and the 2848 Display Control. If a Write operation is in progress at the occurrence of an Interface Disconnect sequence, the write operation is terminated (Channel End and Device End in the 2848 Status byte).

A Read operation in progress when the Interface Disconnect sequence is generated is not discontinued; however, data transmission from the 2848 to the channel (resulting from the Read operation) is terminated. The Read operation continues until the cursor or last buffer position is detected, depending on the type of Read command. The ending sequence and the status of the 2260 display are the same following an Interface Disconnect sequence as they would normally be had the sequence not occurred.

Selective Reset Sequence

The Selective Reset sequence terminates the operation being performed by the selected device and places the interface in a Not Selected status. Channel End and Device End are not presented to the channel following a Selective Reset sequence.

The following paragraphs describe the effect of the Selective Reset sequence on the operation of the selected 2260 Display Station when it occurs during a Read or Write operation.

Read Operation

If the selected 2260 Display Station is performing a Read operation, the Selective Reset sequence terminates the operation when the first complete data byte following the Selective Reset sequence is read from the 2260 buffer.

Write Operation

If the selected 2260 Display Station is performing a Write operation, the Selective Reset sequence terminates data transfer from the channel to the 2260. The last complete data byte received is stored in the 2260 buffer.

System Reset Sequence

The System Reset sequence occurs when the system RESET switch (System/360 CPU) is operated, when initial program loading is performed, or when the System Power On sequence is completed.

The occurrence of the System Reset sequence causes the following:

1. The 2848 interface is placed in Not Selected condition.
2. The 2848 Status and Sense bytes are reset.
3. All 2260 buffers are cleared. The cursor of each 2260 is placed in the first displayable position.
4. All 2260 keyboards are restored.
5. The 1053 Printer buffer is cleared.
6. The type head of the 1053 Printer is returned to the first print position, and the 1053 Printer is placed in the Upshift condition.

The Ready or Not Ready status of the 1053 Printer is not changed by the System Reset sequence.

Short Control Unit Busy Sequence

The Short Control Unit Busy sequence is initiated by the 2848 Display Control if the 2848 interface is busy and the channel attempts to select a device (2260 or 1053 Printer) of an address other than the address of the device creating the busy condition.

The sequence sets the Status Modifier and Busy bits in the 2848 Status byte. The Status Modifier bit indicates to the channel that selection of a device will not be honored until Control Unit End is presented in the Status byte with Attention or Ending status.

SENSE AND STATUS BYTES

Sense Byte

The 2848 Sense byte is presented to the channel in response to the Sense command. The Sense byte records and provides the channel with information regarding unusual conditions that occurred during the preceding operation. The Sense byte is reset by any command other than Test I/O, Sense, or No Op.

Four of the eight bits provides by the Sense byte are required by the 2848 to record unusual conditions occurring within the 2848-2260 display group. The bits (0 through 3) are described below:

1. Command Reject (Bit 0) - Bit 0 is set in the Sense byte if an invalid command or a command with an invalid modifier bit is presented to the 2848. This occurs during initial selection sequence.
2. Intervention Required (Bit 1) - Bit 1 is set in the Sense byte if a Write 1053 Buffer command is given when the 1053 Printer is in a Not Ready status (out of paper, or power off). Occurs during initial selection sequence.
3. Bus Out Check (Bit 2) - Bit 2 is set in the Sense byte when a parity error in a command byte or incoming data byte is detected by the 2848. The setting of bit 2 can occur during initial selection or during performance of the operation.
4. Equipment Check (Bit 3) - Bit 3 is set in the Sense byte if a buffer parity error is detected by the 2848 during a Read DS MI, Short Read DS MI, or Read Full DS Buffer Storage operation. Occurs during performance of the operation.

Status Byte

The Status byte is used to relate to the channel the current status of the 2848 Display Control and its attached devices; e.g., it may indicate that the 2848 is busy, or that the 2848 is ready to accept a command, etc. The Status byte is presented to the channel during initial and ending sequences and is reset upon channel acceptance. The eight bits of the 2848 Status byte are described below:

1. Attention (Bit 0) - The Attention bit is used to notify the channel that an ENTER key on a 2260 keyboard has been depressed. The Attention bit should be program-interpreted to mean that an MI (manual input) message is waiting to be transferred from the 2260 buffer to the channel.
   The Attention bit is set in the 2848 Status byte when the ENTER key has been depressed at a 2260 and the interface is not busy. If the interface is busy when the ENTER key is depressed, the Attention bit is set when the interface reaches a Not Busy status. The Attention bit places the interface in Busy status.
2. Status Modifier (Bit 1) - The Status Modifier bit is set during a Short Control Unit Busy sequence. The Status Modifier bit indicates to the channel that selection of a 2848 device will not be honored until Control Unit End is presented in the Status byte with Attention or Ending (Channel End and Device End) status.
3. Control Unit End (Bit 2) - Control Unit End is a delayed response to a Short Control Unit Busy sequence. It is set in the Status byte with Ending status (Channel End, Device End) or Attention, at the end of the operation in which the Short Control Unit Busy sequence occurred. It signifies that the 2848 is free to accept a new command.
4. Busy (Bit 3) - The Busy bit is set whenever the 2848 interface is in Busy status. The 2848 interface will be in a Busy state from initial selection or, if Attention is set, until Ending status or Attention status is accepted. In this state, the 2848 will respond with the Short Control Unit Busy sequence to all channel selections with the exception of a selection of the 2260 Display Station or 1053 Printer creating the Busy state. Then, only a Test I/O command to the device creating the Busy state will be honored if status is present. All other command byte configurations will receive the Busy and current status bits as a status report. Device End is not presented in response to this status report.
   When the 2848 interface is busy, keyboard entry to the selected 2260 buffer or transfer of data to the 1053 Printer buffer is not processed.
5. Channel End (Bit 4) - Channel End is set at the completion of an operation. Channel End, when presented with Device End, indicates that the 2848-2260 display complex is free to accept a new command. The presence of

Channel End without Device End indicates that the transfer of data between the channel and the 2848 has been completed and that the channel is free to service another control unit sharing the channel. Channel End without Device End can occur in a Write 1053 Buffer Storage operation.

6. Device End (Bit 5) - Device End, when presented with Channel End following a 2260 command, indicates that the 2260 has completed an operation and is free to accept a command. Device End (with Channel End) also occurs following a Write 1053 Buffer Storage command, indicating completion of data transfer from the channel to the printer buffer. However, it does not necessarily indicate that the printer has completed printing. Device End alone is used to signal the completion of printing, and will occur in response to a print command, provided a previous print command was issued while the printer was in Busy status (still printing). Device End alone is also used to signal that the printer is ready. It will occur in response to a print command issued after the printer has been readied, provided a previous print command was issued while the printer was in Intervention Required status (not ready).
7. Unit Check (Bit 6) - Unit Check should be program-interpreted as meaning that a condition exists or occurred that requires investigation. Unit Check is set upon occurrence of one or more of the following:
   a. Invalid command or command modifier.
   b. Presentation of a Write Printer command when the printer is in a Not Ready condition (out of paper, or power off).
   c. Detection of a parity error in a command byte or data byte from the channel to the 2848.
   d. Detection of a parity error in data being transferred from a 2260 buffer to the 2848 interface during a Read operation.

   The Sense command should be issued in response to a Unit Check. This command causes the 2848 Sense byte to be transferred to the channel where a bit analysis of the Sense byte can be performed and the cause of the Unit Check can be determined. The Sense byte is described under the heading, Sense and Status Bytes.

   The presence of Unit Check in the Status byte prohibits the setting of the Attention bit until the next command to the 2848 (excluding Test I/O and No Op) is completed. This prevents the Attention bit from placing the 2848 interface in Busy status (which would prevent the acceptance of the Sense command) if an ENTER key had been depressed prior to issuance of the Sense command.
8. Bit 7 - Not used.

CHARACTER CODES AND DISPLAYABLE SYMBOLS

This section contains figures that tabulate the various codes used by the 2848 Display Control and the symbols that can be displayed on the CRT of the 2260. Each code provided is discussed below.

Displayable Symbols

The symbols that can be displayed on the CRT of the 2260 are listed and illustrated in Figure 1-12. Note that asterisks appear alongside certain symbols,

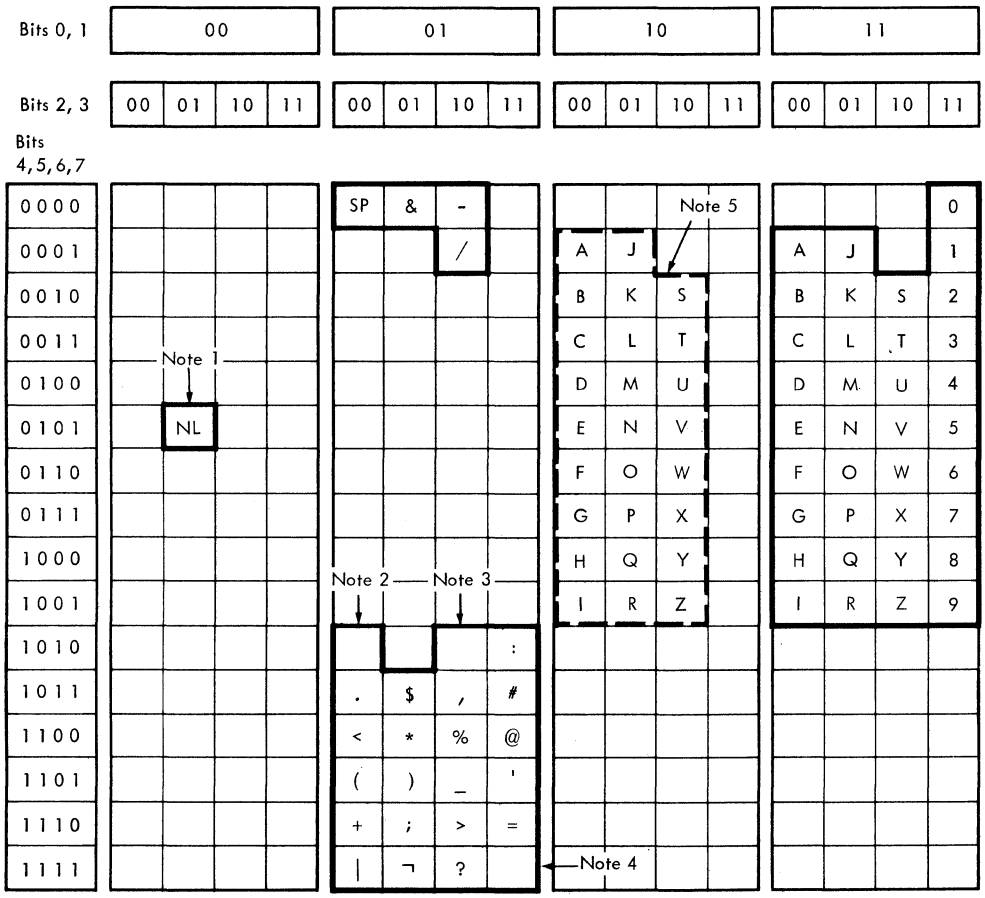
Letters and Numbers		Special Symbols		Special Symbols	
A	S	▶	Start MI*	:	Colon
B	T	.	Period	#	Number sign
C	U	<	Less than	@	At
D	V	(	Left parenthesis	'	Apostrophe
E	W	+	Plus	=	Equal
F	X	▮	Vertical bar	■	Check*
G	Y	$	Dollar	SP	Space
H	Z	*	Asterisk	◢	New line*
I	0	)	Right parenthesis	-	Hyphen
J	1	&	Ampersand	▬	Destructive cursor (EOM)*
K	2	/	Slash	▏	Nondestructive cursor
L	3	;	Semicolon		*1053 Equivalent Symbols
M	4	¬	Logical NOT	¢	Start
N	5	,	Comma	"	Check
O	6	%	Percent	None	New Line
P	7	—	Underscore	!	End of message
Q	8	>	Greater than		
R	9	?	Question mark		

Figure 1-12. Displayable Symbols

referring the reader to a 1053 Equivalent Symbols listing within the table. The printer symbols shown are those that will actually be printed in place of the asterisked symbols which will be displayed on the display station.

EBCDIC Code

The 8-bit Extended Binary-Coded Decimal Interchange Code (EBCDIC) used to transfer data between the channel and the 2848 is shown in Figure 1-13.



Note 1. Displayed on 2260's as the New Line (◢) symbol. Causes carriage return and line feed on the 1053 Model 1 Printer.

Note 2. Displayed on 2260's as the Start MI (▶) symbol. Prints on the 1053 Model 1 Printer as a cent sign (¢).

Note 3. Displayed on 2260's as the EOM (▬) symbol. Prints on the 1053 Model 1 Printer as an exclamation mark (!).

Note 4. Displayed on 2260's as the Check (▮) symbol. Prints on the 1053 Model 1 Printer as a quote (") symbol.

Note 5. The codes represented by the characters within the dotted outline are the EBCDIC codes for the lower case alphabetic characters. These codes are converted to upper case by the 2848 and displayed as upper-case characters. If retrieved by a read operation, the codes will be in the upper-case bit configuration.

Additional Notes:

A. Graphic representations are undefined for the bit patterns outside the heavily outlined portions of the chart. These bit patterns are referred to as undefined graphic bit patterns. If an undefined graphic bit pattern is sent from channel to the device, the graphic that will be displayed or printed by the device is not specified.

B. IBM reserves the right to change at any time the graphic displayed or printed by the device for an undefined graphic bit pattern sent from channel.

Figure 1-13. EBCDIC Code Used for 2848-System/360 Channel Transfers

The two low-order bits (bits 0 and 1) are stripped from the eight-bit code by the 2848 to form the internal 2848 six-bit code when data is received from the channel. Conversely, as data is transferred to the channel, the 2848 reconstructs the full eight-bit EBCDIC code from the six-bit internal code.

Keyboard Code

The seven-bit codes that result from depression of the associated keys at a 2260 Display Station are listed in Figure 1-14. Note that bit C is a 1 only when the code represents a keyboard command. Note also that the six-bit BCD codes listed in Figure 1-15 are complements of bits 2 through 7 of the keyboard codes. Remembering this relationship will help minimize references to the code tables.

Internal 2848 Six-Bit BCD Code

The internal six-bit code used within the 2848 is shown in Figure 1-15. These codes are generated as a result of the receipt of a keyboard code (Figure 1-15) or as a result of the conversion of the eight-bit EBCDIC code (Figure 1-14) received from the channel.

Code							Function/Character	Code							Function/Character
C	2	3	4	5	6	7									
1	1	0	1	0	0	0	ERASE DISPLAY	0	0	1	0	1	1	0	Z
1	0	0	0	0	1	0	SPACE/ERASE	0	0	0	1	1	1	1	⊙
1	0	1	0	0	0	0	ADVANCE	0	0	0	1	1	1	0	1
1	0	0	1	0	0	1	PRINT	0	0	0	1	1	0	1	2
0	1	0	0	1	0	1	NEW LINE	0	0	0	1	1	0	0	3
1	1	0	0	0	0	0	DOWN	0	0	0	1	0	1	1	4
1	0	1	1	0	0	0	BACKSPACE	0	0	0	1	0	1	0	5
1	0	0	1	1	0	0	ENTER	0	0	0	1	0	0	1	6
1	1	1	0	1	0	1	START	0	0	0	1	0	0	0	7
1	0	0	0	0	0	0	UP	0	0	0	0	1	1	1	8
0	1	1	1	1	1	0	A	0	0	0	0	1	1	0	9
0	1	1	1	1	0	1	B	0	1	0	0	1	0	0	$
0	1	1	1	1	0	0	C	0	0	0	0	0	1	1	@
0	1	1	1	0	1	1	D	0	1	1	0	0	1	1	<
0	1	1	1	0	1	0	E	0	0	1	0	0	0	1	>
0	1	1	1	0	0	1	F	0	0	1	0	0	1	1	%
0	1	1	1	0	0	0	G	0	1	1	0	0	0	1	+
0	1	1	0	1	1	1	H	0	0	0	0	0	0	1	=
0	1	1	0	1	1	0	I	0	0	0	0	1	0	0	#
0	1	0	1	1	1	0	J	0	1	0	0	0	1	1	*
0	1	0	1	1	0	1	K	0	1	0	0	0	0	0	¬
0	1	0	1	1	0	0	L	0	1	1	0	0	1	0	(
0	1	0	1	0	1	1	M	0	1	0	0	0	0	1	;
0	1	0	1	0	1	0	N	0	0	1	0	1	0	0	,
0	1	0	1	0	0	1	O	0	1	1	0	0	0	0	|
0	1	0	1	0	0	0	P	0	1	0	0	0	1	0	)
0	1	0	0	1	1	1	Q	0	0	0	0	1	0	1	:
0	1	0	0	1	1	0	R	0	1	1	0	1	0	0	.
0	0	1	1	1	0	1	S	0	1	0	1	1	1	1	&
0	0	1	1	1	0	0	T	0	0	0	0	0	1	0	'
0	0	1	1	0	1	1	U	0	0	1	1	1	1	1	-
0	0	1	1	0	1	0	V	0	0	1	0	0	1	0	—
0	0	1	1	0	0	1	W	0	0	1	0	0	0	0	?
0	0	1	1	0	0	0	X	0	0	1	1	1	1	0	/
0	0	1	0	1	1	1	Y	0	0	0	0	0	0	0	■ Check symbol

Note:

All keys generate an additional signal. This signal is the strobe to notify the 2848 that a keyboard operation has been initiated.

Figure 1-14. Keyboard Code

Bits:	Code 2	3	4	5	6	7	Function/ Character
	0	1	0	1	1	1	ERASE/ DISPLAY
	1	1	1	1	0	1	SPACE/ ERASE
	1	0	1	1	1	1	ADVANCE
	1	1	0	1	1	0	PRINT
	0	1	1	0	1	0	NEW LINE
	0	1	1	1	1	1	DOWN
	1	0	0	1	1	1	BACK-SPACE
	1	1	0	0	1	1	ENTER
	0	0	1	0	1	0	START
	1	1	1	1	1	1	UP
	0	0	0	0	0	1	A
	0	0	0	0	1	0	B
	0	0	0	0	1	1	C
	0	0	0	1	0	0	D
	0	0	0	1	0	1	E
	0	0	0	1	1	0	F
	0	0	0	1	1	1	G
	0	0	1	0	0	0	H
	0	0	1	0	0	1	I
	0	1	0	0	0	1	J
	0	1	0	0	1	0	K
	0	1	0	0	1	1	L
	0	1	0	1	0	0	M
	0	1	0	1	0	1	N

Bits:	Code 2	3	4	5	6	7	Function/ Character
	0	1	0	1	1	0	O
	0	1	0	1	1	1	P
	0	1	1	0	0	0	Q
	0	1	1	0	0	1	R
	1	0	0	0	1	0	S
	1	0	0	0	1	1	T
	1	0	0	1	0	0	U
	1	0	0	1	0	1	V
	1	0	0	1	1	0	W
	1	0	0	1	1	1	X
	1	0	1	0	0	0	Y
	1	0	1	0	0	1	Z
	1	1	0	0	0	0	0
	1	1	0	0	0	1	1
	1	1	0	0	1	0	2
	1	1	0	0	1	1	3
	1	1	0	1	0	0	4
	1	1	0	1	0	1	5
	1	1	0	1	1	0	6
	1	1	0	1	1	1	7
	1	1	1	0	0	0	8
	1	1	1	0	0	1	9
	0	1	1	0	1	1	$
	1	1	1	1	0	0	@
	0	0	1	1	0	0	<
	1	0	1	1	1	0	>
	1	0	1	1	0	0	%

Bits:	Code 2	3	4	5	6	7	Function/ Character
	0	0	1	1	1	0	+
	1	1	1	1	1	0	=
	1	1	1	0	1	1	#
	0	1	1	1	0	0	*
	0	1	1	1	1	1	¬
	0	0	1	1	0	1	(
	0	1	1	1	1	0	;
	1	0	1	0	1	1	,
	0	0	1	1	1	1	!
	0	1	1	1	0	1	)
	1	1	1	0	1	0	:
	0	0	1	0	1	1	.
	0	1	0	0	0	0	&
	1	1	1	1	0	1	|
	1	0	0	0	0	0	–
	1	0	1	1	0	1	—
	1	0	1	1	1	1	?
	1	0	0	0	0	1	/
	1	1	1	1	1	1	Check
	0	0	1	0	1	0	▶
	0	1	1	0	1	0	◢
	1	0	1	0	1	0	▬
	0	0	0	0	0	0	Space

Figure 1-15. Internal 2848 Six-Bit BCD Code

1053 Printer Code

The tilt-rotate codes associated with various printer characters are listed in Figure 1-16. These codes are generated as a result of a code conversion (within the character generator) from the 2848 six-bit BCD code to the tilt-rotate codes.

TERMS AND DEFINITIONS

Figure 1-17 lists (alphabetically) special terms used in this manual and their definitions. Common terms used in a special sense are also listed and defined. Figure 1-17 should be read carefully since a knowledge of these terms is a prerequisite to understanding the discussion of display complex operation.

2848 Six/Bit BCD Code Bit: 2	3	4	5	6	7	Char. or Symbol	1053 T/R Code Bit: 1	2	3	4	5	6	7	Aux
							Func: LC	T1	T2	R5	R2A	R2	R1	
0	0	0	0	0	0		0	0	0	0	0	1	0	0
0	0	0	0	0	1	A	0	0	0	1	1	1	1	1
0	0	0	0	1	0	B	0	0	0	0	1	1	0	1
0	0	0	0	1	1	C	0	0	0	1	1	1	0	0
0	0	0	1	0	0	D	0	0	0	0	1	0	1	1
0	0	0	1	0	1	E	0	0	0	1	1	0	1	0
0	0	0	1	1	0	F	0	0	0	0	1	0	0	0
0	0	0	1	1	1	G	0	0	0	1	1	0	0	1
0	0	1	0	0	0	H	0	0	0	1	0	0	1	1
0	0	1	0	0	1	I	0	0	0	0	0	0	1	0
0	0	1	0	1	0	▶	0	0	0	0	0	0	0	1
0	0	1	0	1	1	.	1	0	0	0	0	0	0	1
0	0	1	1	0	0	<	0	1	1	1	1	1	0	0
0	0	1	1	0	1	(	0	1	1	1	1	1	1	1
0	0	1	1	1	0	+	0	1	1	0	1	1	0	1
0	0	1	1	0	1	ı	0	1	1	0	1	1	1	0
0	1	0	0	0	0	&	1	1	0	0	1	1	1	1
0	1	0	0	0	1	J	0	1	0	1	1	1	1	0
0	1	0	0	1	0	K	0	1	0	0	1	1	0	0
0	1	0	0	1	1	L	0	1	0	1	1	1	0	1
0	1	0	1	0	0	M	0	1	0	0	1	0	1	0
0	1	0	1	0	1	N	0	1	0	1	1	0	1	1
0	1	0	1	1	0	O	0	1	0	0	1	0	0	1
0	1	0	1	1	1	P	0	1	0	1	1	0	0	0
0	1	1	0	0	0	Q	0	1	0	1	0	0	1	0
0	1	1	0	0	1	R	0	1	0	0	0	0	1	1
0	1	1	0	1	0	◢	0	0	1	0	0	1	0	1
0	1	1	0	1	1	$	1	1	0	0	0	0	0	0
0	1	1	1	0	0	*	0	1	1	1	1	0	0	1
0	1	1	1	0	1	)	0	1	1	1	1	0	1	0
0	1	1	1	1	0	;	0	1	1	0	1	0	0	0
0	1	1	1	1	1	¬	0	1	1	0	1	0	1	1
1	0	0	0	0	0	-	1	0	1	0	1	1	1	1
1	0	0	0	0	1	/	1	0	1	1	1	1	1	0
1	0	0	0	1	0	S	0	0	1	0	1	1	0	0
1	0	0	0	1	1	T	0	0	1	1	1	1	0	1
1	0	0	1	0	0	U	0	0	1	0	1	0	1	0
1	0	0	1	0	1	V	0	0	1	1	1	0	1	1
1	0	0	1	1	0	W	0	0	1	0	1	0	0	1
1	0	0	1	1	1	X	0	0	1	1	1	0	0	0
1	0	1	0	0	0	Y	0	0	1	1	0	0	1	0
1	0	1	0	0	1	Z	0	0	1	0	0	0	1	1
1	0	1	0	1	0	≡	0	1	0	0	0	0	0	0
1	0	1	0	1	1	,	1	0	1	0	0	0	0	0
1	0	1	1	0	0	%	0	0	0	0	1	1	1	0
1	0	1	1	0	1	—	0	0	1	1	1	1	1	0
1	0	1	1	1	0	>	0	1	0	0	1	1	1	1
1	0	1	1	1	1	?	0	0	1	0	1	1	1	1
1	1	0	0	0	0	0	1	1	1	0	1	1	1	0
1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	0	2	1	1	1	0	1	1	0	1
1	1	0	0	1	1	3	1	1	1	1	1	1	0	0
1	1	0	1	0	0	4	1	1	1	0	1	0	1	1
1	1	0	1	0	1	5	1	1	1	1	1	0	1	0
1	1	0	1	1	0	6	1	1	1	0	1	0	0	0
1	1	0	1	1	1	7	1	1	1	1	1	0	0	1
1	1	1	0	0	0	8	1	1	1	1	0	0	1	1
1	1	1	0	0	1	9	1	1	1	0	0	0	1	0
1	1	1	0	1	0	:	0	0	1	0	0	0	0	0
1	1	1	0	1	1	#	1	1	1	0	0	0	0	1
1	1	1	1	0	0	@	1	0	0	0	1	1	1	0
1	1	1	1	0	1	'	0	1	1	1	0	0	1	1
1	1	1	1	1	0	=	0	1	1	0	0	0	0	1
1	1	1	1	1	1	■	0	1	1	0	0	0	1	0
0	0	1	1	1	1	]	0	1	1	0	1	1	1	0
0	1	1	0	1	0	◢	0	0	1	0	0	1	0	1
0	1	1	1	1	1	¬	0	1	1	0	1	0	1	1
1	1	1	1	0	0	@	1	0	0	0	1	1	1	0
						UP SHIFT	0	1	0	0	0	1	0	1
						DOWN SHIFT	0	1	1	0	0	1	0	0

Notes:

1. LC - lower case. Bits with a 1 in the LC position are lower-case (no shift) characters.
2. T1, T2, R5, R2A, R2, and R1 refer to printer magnets providing increments of tilt and rotate of the type ball.
3. Aux - auxiliary bit. Used as control line to printer.

Figure 1-16. 1053 Printer Tilt-Rotate Codes and Their 2848 Six-Bit BCD Code Equivalents

Term	Definition
Active Lines	The portion of the frame actually used to display characters and the space between characters. Of the 512 lines that make up one frame, 480 lines are active.
BCD	Binary-coded data. The six-bit code used as character codes.
Buffer	A portion of a display adapter that contains two delay lines. A buffer stores the data for one quadrant of two displays. Thus, the 2848 Model 3 requires four buffers: upper-left (i.e., display), lower-left, upper-right, and lower-right. The 2848 Model 2 requires only two buffers: upper-left and lower-left. The 2848 Model 1 requires a single buffer (upper left) for its display.
Channel	A System/360 selector or multiplexor channel.
Column	A column of characters within the display. There are six types of character columns: BCD (not displayed), V1 (e.g., videl 1), V2, V3, V4, and V5.
Cursor, Destructive	A display symbol that appears as a horizontal bar on the CRT. It indicates the next character position within the CRT display. The destructive cursor actually occupies a full character position itself. Therefore, in cursor operations (such as backspace), the cursor destroys the character it replaces when it moves back one display position.
Cursor, Nondestructive	A display symbol that appears as a vertical bar on the CRT. It indicates the display position (position to right of cursor) that will be affected next. Unlike the destructive cursor, this cursor can be moved within the display without destroying or modifying other data display on the CRT. The nondestructive cursor does not occupy a character position but is essentially displayed between and below character positions.
Delay Line	Storage medium that uses the qualities of magnetostriction for dynamic data storage.
EOM	End of message. When the destructive cursor is used, the EOM is the destructive cursor since it is normally displayed on the screen. When the nondestructive cursor is incorporated, EOM is represented on the display by the destructive cursor symbol.
Even Check	The time (one bit time in duration) during which the slot parity bit for the even display is written (parity assign) or checked (parity check).
Even Display	One of the two displays that can be driven from a display adapter. The even display is normally assigned an even device number (or address). This display is serviced during even display time.
Frame	Scanning all of the CRT display area once is defined as one frame. A frame comprises 512 vertical scans.
Horizontal Sync	A signal used to synchronize the horizontal sweep circuits in the display station. The electron beam retraces from the right side to the left side of the CRT.
Line	(See row.)
Line 16	The first vertical sweep (or line) that is actually used. Line 0-15 are blanked and are not part of the display area.
Line (Scan)	A vertical sweep. Deflection of the electron beam from the top to the bottom of the screen.
Lines per Frame	(See frame)

Figure 1-17. Terms and Definitions (Sheet 1 of 2)

Term	Definition
Lower Segment	The lower half of the display in 2848 Models 2 and 3. (Model 1 does not have a lower segment.)
NL	New Line - the display symbol that results when the NL key is depressed at the keyboard. Data to the right of the NL symbol is not transferred during data transfer to the channel that results from an Enter command.
Odd Check	The time (one bit time in duration) during which the slot parity bit for the odd display is written (parity assign) or checked (parity check). Occurs at the end of the slot.
Odd Display	One of the two displays that can be driven from a display adapter. The odd display is normally assigned an odd device number (or address). This display is serviced during odd display time.
Retrace	The path of the electron beam during the return interval, usually accomplished at a high rate of speed relative to scan time.
Retrace Segment	The time period during which the segment counter is in the retrace status. Vertical retrace is accomplished during retrace segment time.
Row	A horizontal row of displayed characters. The 2848 Models 2 and 3 have 12 such rows; the Model 1 has 6. The term "line" is sometimes used to indicate a row; e.g., line change required. All such uses of the term "line" refer to a row of characters as described above.
Slot	A group of 86 bits made up as follows: 42 data bits plus a slot parity bit for the even display, and 42 data bits plus a parity bit for the odd display. All data bits of a slot are of the same type (video V1-V5 or BCD).
SOM	Start of Message - The display symbol that results when the START key is depressed at the keyboard. Determines the starting point of data transferred to the channel as a result of an Enter command.
TIC	A bit used as an index to the data stored in the delay lines of a display adapter. Each display station has a TIC; therefore, each display adapter contains two TIC's, one for the even display and one for the odd display. Once TIC is located and its position stored in the counter storage logic, operations can be performed with the adapter's delay lines, starting from the TIC location. The TIC's location within the display data is normally indicated by the position of the cursor on the CRT display. The TIC is always written as bit 1 of a character BCD byte location. With the destructive cursor, TIC is always written with the BCD code for the cursor (EOM). When the non-destructive cursor is used, TIC can be written in conjunction with the BCD code of any displayable character. The term "TIC" is not an abbreviation; its individual letters have no significance.
Slot Parity	A parity bit which is assigned to a group of 42 data bits to provide even parity. An even display parity bit is associated with the 42 even display data bits in a slot, and a parity bit is associated with the 42 data bits for the odd display.
TIC Sample Time	A TIC sample level that is generated to sample bit position 1 of each BCD character stored in the delay line to determine whether the location contains TIC.
Upper Segment	The upper half of the display in 2848 Models 2 and 3. (Model 1 has only the upper segment.)
Upper Segment Time	The period during which the segment counter is in upper status.
Vertical Sync	A signal used to synchronize the vertical sweep circuits in the display station. The electron beam retraces from the bottom to the top of the CRT.

Figure 1-17. Terms and Definitions (Sheet 2 of 2)

INTRODUCTION

This chapter describes in detail the theory of operation of each major functional area of the IBM 2848 Display Control, the IBM 2260 Display Station, and their associated supporting equipments. The areas are those illustrated in Figure 1-6 and discussed in Chapter 1. This chapter describes the following in detail:

1. IBM 2260 Display Station
2. IBM 2848 Display Control
3. Channel Adapter
4. IBM 1053 Printer adapter.

IBM 2260 DISPLAY STATION

The IBM 2260 Display Station (Figure 2-1) contains the CRT and related electronic circuits required to present information (comprising letters, numerals, and special symbols in any combination) on the viewing screen. Composition and arrangement of the display on the viewing screen, within the limits of the format area, are under control of the data processor operating program via the IBM 2848 Display Control. Additional entries, changes, and control functions can be exercised by the display station operator through use of the manual input keyboard.

The keyboard is a display station optional feature and is used to supplement the basic 2260 Display Station. A display need not be fitted with the optional feature keyboard; its incorporation into the basic unit is dependent upon the application and degree of operator intervention required. Two different types of keyboards, special features 4766 (alphanumeric) and 4767 (numeric), are available to supplement the display stations used in domestic applications. Both keyboards contain the same set of control keys. (See Figures 1-3 and 1-4.) Keyboards employed in World Trade machines are modified in relation to symbol and letter changes applicable to the country where the equipment is installed. These keyboard language changes and modifications are discussed in detail in Appendix C.

There are two models of display stations, designated Model 1 and Model 2. Model 1 display stations are wired and aligned to operate with a horizontal sync frequency of 30 cps and incorporate a CRT with a P39 phosphor. Model 2 display stations are wired and aligned to operate with a horizontal sync frequency of 60 cps and incorporate a CRT with a P4 phosphor. Model 1 display stations can be operated only with the Model 3 display control (960-character display), whereas the Model 2 display station can operate with either the Model 1 or Model 2 display control (240- and 480-character display). Note, however, that all display stations connected to a particular control unit must be operated at the same horizontal sweep frequency.

The theory of operation of the Model 1 display station is described in detail in the following paragraphs. Differences in operation between the Model 1 and Model 2 display stations are indicated when required. Model applicability, display formats, and expansion ranges are summarized as follows:

2260 Display Station	2848 Display Control	Display Format (In Inches)		Expandable Ranges (In Inches)		Total No. of Characters	CRT	
		Width	Height	Width	Height		P4	P39
Model 2	Model 1	6.5	2.25	6.0 to 8.5	1.9 to 2.4	240	60cps	
Model 2	Model 2	6.5	4.5	6.0 to 8.5	4.0 to 5.0	480	60cps	
Model 1	Model 3	9.0	3.0	7.5 to 9.5	2.8 to 5.0	960		30cps

Operation of the display station is initiated upon receipt of a composite video signal from display control. The composite video signal (Figure 2-2) contains the necessary video signals interleaved with synchronizing pulses. Video pulses control the electron beam in the CRT to form informational data by turning the beam on, and the pulses provide a time reference for the sweep oscillators. When the composite video is received by the display station, it is amplified by a video amplifier. The amplified video is fed to the cathode of the CRT, which unblanks (intensifies) the beam whenever video pulses are present. The sync signals do not intensify the electron beam because they are opposite in polarity from the video signals and therefore drive the tube deeper into cutoff. The output of the video amplifier is also fed to a sync clipper circuit where the sync is separated from the video signal. The output of the clipper is a composite high-speed sync of 15,360 cps (vertical sync) and a low-speed sync of 30 or 60 cps (horizontal sync). Both the vertical and horizontal sync signals are employed to synchronize the vertical and horizontal multivibrators, respectively. The output of the horizontal multivibrator is applied to the horizontal deflection coils via the horizontal output tube and the impedance-matching transformer. The ramp voltage generated

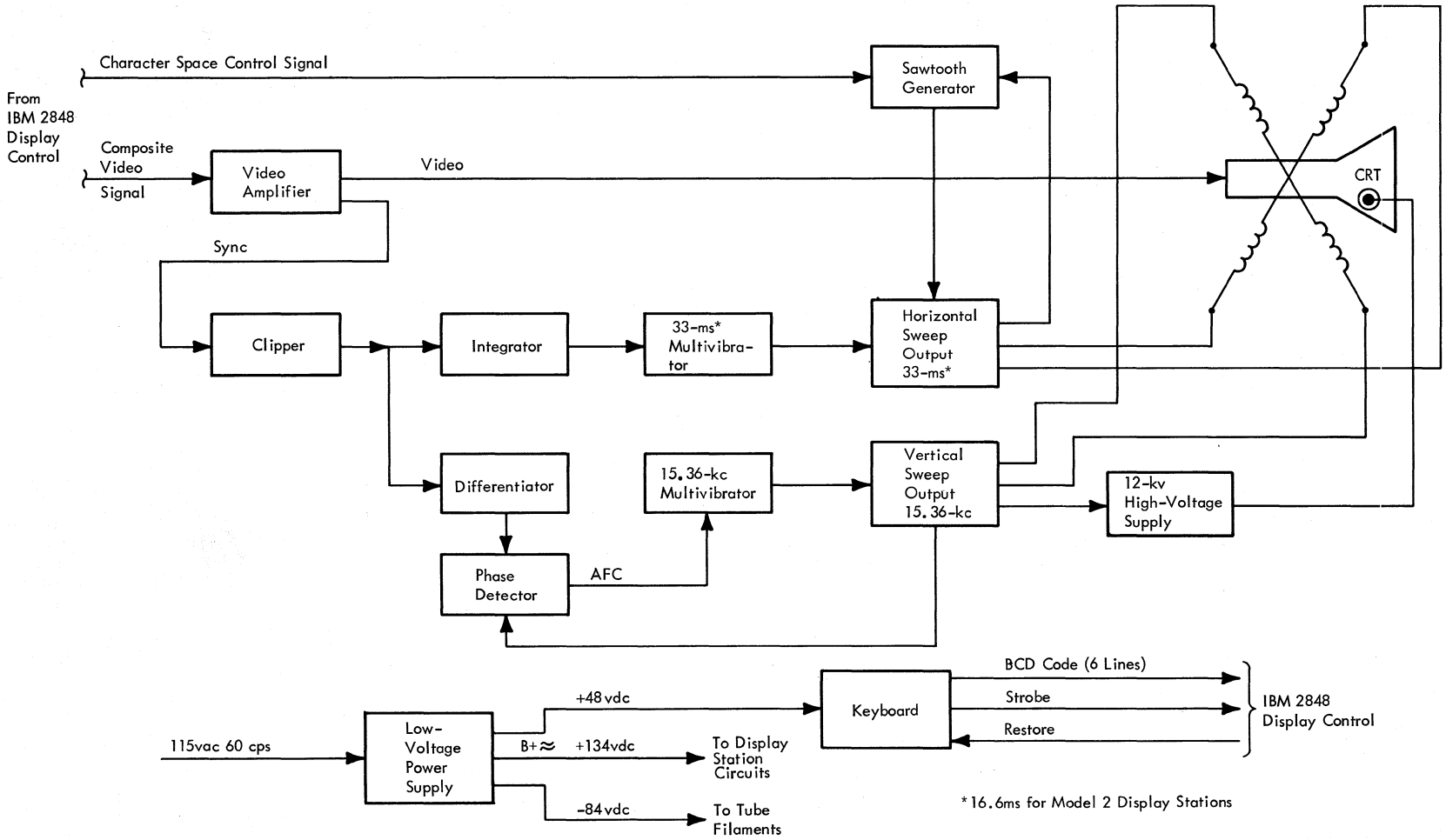
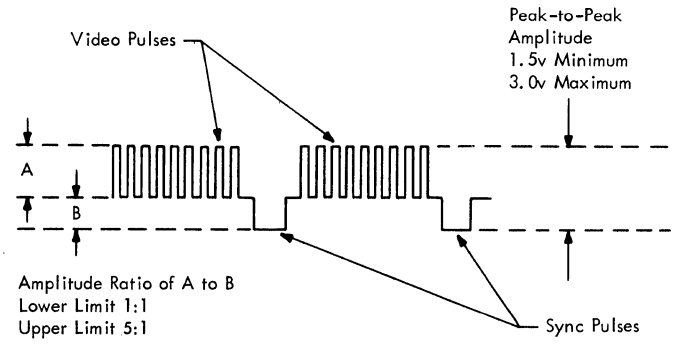


Figure 2-1. Display Station Block Diagram



•Figure 2-2. Composite Video Signal (One Vertical Scan)

by the vertical multivibrator is shaped and powered by the vertical output circuit and impedance-matched to the vertical deflection coils with a flyback transformer. Anode voltage (12 kv) for the CRT is derived from the tertiary winding on the flyback transformer when inductive energy stored in the yoke collapses during retrace time. Also included in the display station is a low-voltage power supply which makes available a B+ voltage of approximately 134vdc for the electronic circuits in the display station and +48vdc for the manual input keyboard.

Tube heaters, including the CRT, are series-connected from a -84vdc supply. The high-voltage rectifier tube filament voltage is obtained from a two-turn winding in the flyback transformer.

Cathode-Ray Tube

- The cathode-ray tube (CRT) is essentially a transducer device since it converts electrical energy to light energy.
- CRT displays alphanumeric characters and special symbols on its viewing screen; these can be interpreted and acted upon by the operator.

The cathode-ray tube (Figure 2-3) is a highly evacuated bell-shaped tube which converts electrical energy into light energy. Because it is highly evacuated, its bell-shaped glass envelope must be structurally sound to support the electrodes within the tube and to prevent breakage. To further ensure its overall strength, an epoxy-resin-filled, implosion-protection, metal-shell rim has been incorporated around the periphery of the viewing screen of the tube. The epoxy resin expands as

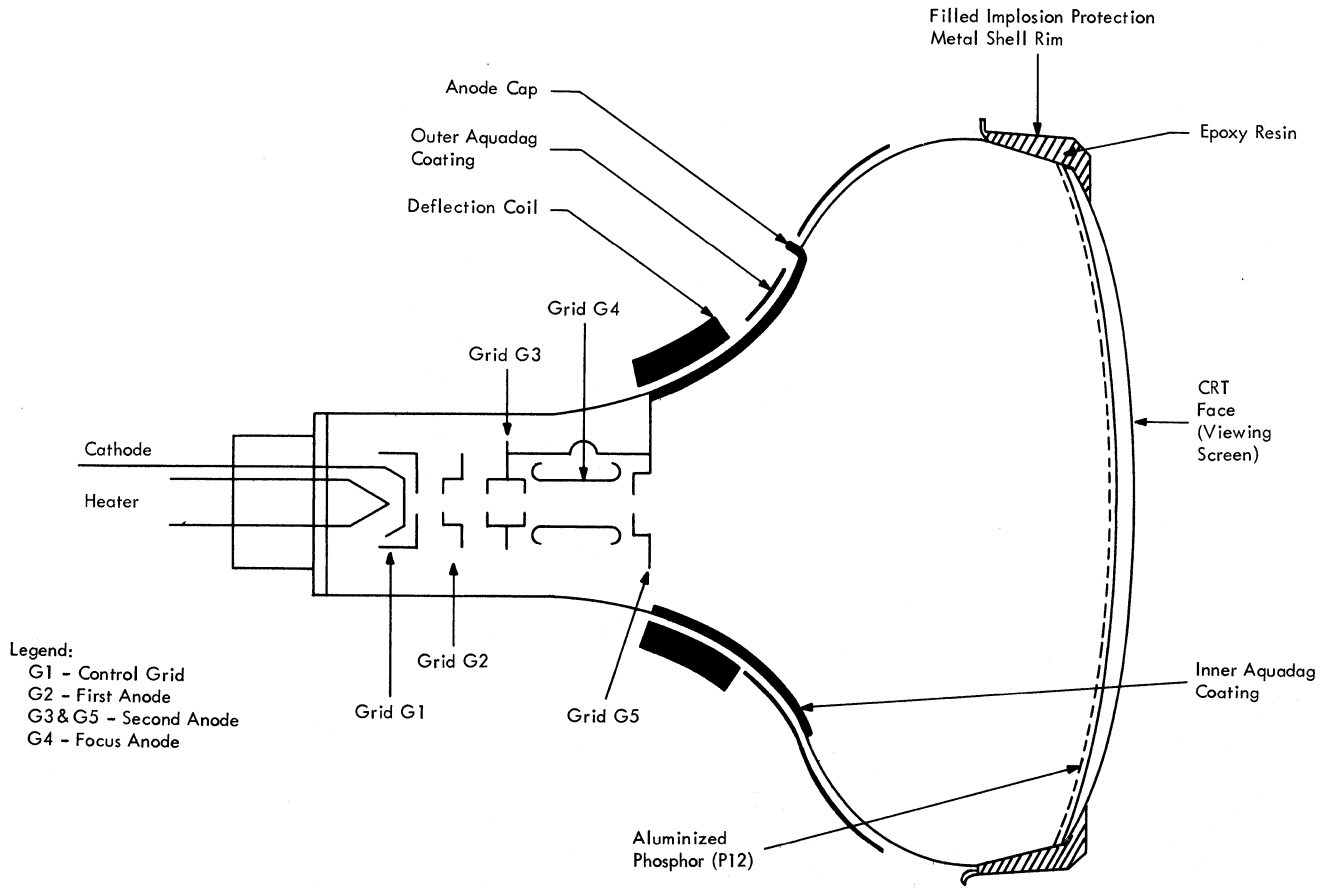


Figure 2-3. Cathode-Ray Tube

it cures, which places the tube bell and faceplate under compression and keeps the tube relatively safe from implosion.

The CRT assembly consists of an electron gun (Figure 2-4), inner and outer Aquadag* coating, a magnetic deflection yoke, and a viewing screen composed of fluorescent material with aluminum backing. The evacuated tube contains all of these elements except the magnetic deflection yoke. The CRT has an 11.625-inch usable diagonal face measurement. However, the bezel that fits around the CRT restricts the useful display area to approximately 9.5 to 5.7 inches.

In the CRT, the electron gun directs a beam of electrons toward the screen. This beam is intercepted by the various elements that control, direct, and focus it to display a spot on a specific area of the CRT face. As the beam of electrons passes through the electron gun, the electrons are accelerated so that they attain a velocity of sufficient magnitude to bombard the phosphor coat on the screen and cause it to glow. This acceleration is imparted to the electron beam by the high-voltage gradients existing along the axes of the tube as a result of the accelerating anodes. The beam, positioned by the magnetic deflection yoke, strikes the materials of the aluminized phosphor, causing the phosphor to glow and assume the shape of the electron beam. Since the beam is turned on for a relatively short time, a small spot appears on the viewing screen.

Electron Gun

The electron gun (Figure 2-4) is an electron lens structure which produces (and controls the size and energy of) the electron beam in a CRT. The electron gun consists of an indirectly heated cathode that acts as a source of electrons, a control grid (G1) that limits the number of electrons traveling toward the screen, a first and a second accelerating anode (G2 and G3), and a focus anode (G4). The cathode is coated with barium oxide, which gives up electrons freely when heated. The heater for the cathode is placed inside the cathode cylinder and is electrically insulated from the cathode. Electrons emitted by the cathode are directed through the gun by the potential gradient which exists across G2 and the cathode. The control grid (G1), normally negative with respect to the cathode, cuts off electron flow toward G2 when it is sufficiently negative, thereby deflecting the electrons back to the cathode. When G1 is made less negative with respect to the cathode, electrons are allowed to flow toward G2. The method employed in the display station impresses a negative-going video signal of 30v on the cathode of the CRT. This permits fast turn-on (and turn-off) of the electron beam because the distributed capacity between the cathode and G1 is less than that involving G1 and the other electrodes in the gun.

Once the electron beam has been turned on, the electrons emitted by the cathode pass through a small aperture in G1 and converge (cross over) toward the axis of the tube as a result of the action of the electric field between G1 and G2. Thus, beam crossover occurs just prior to entering the aperture of G2. Beam divergence (spreading out) occurs as it is accelerated by electrodes G2 and G3 and continues until it comes under the influence of the focusing anode (G4), which is the focus lens used to focus the electron beam.

Beam Focusing

Maximum divergence of the beam occurs as it passes into G4, where the beam is focused so that it again converges as it strikes the screen. Thus,

*Trademark of Acheson Colloids Co., Port Huron, Michigan

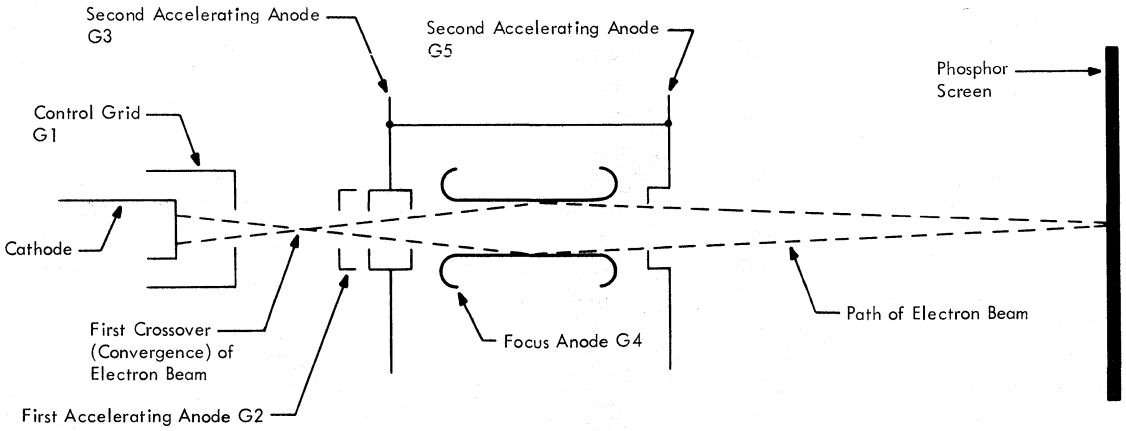


Figure 2-4. CRT Electron Gun

an image of the first crossover is projected onto the phosphor screen. The focus anode can be tied to ground, +80v, +138v, or boost. The potential required on the focus anode is a tube variable that depends upon characteristics acquired during its manufacture. Any time a CRT is changed, all four voltages must be checked; the one selected must produce a spot that is clearly defined with a minimum of blooming. In addition, the focus must be nearly the same on the edges of the display as in the center areas. The size of the spot appearing on the face of the CRT is directly related to the size of the cathode, the crossover, and the potential applied to the focusing anode, so that the beam can be re-formed in a manner similar to the action performed by an optical lens.

Deflection Yoke Assembly

The deflection yoke assembly consists primarily of two coils whose combined magnetic field positions the electron beam on the viewing screen of the CRT. One coil (horizontal) produces a magnetic field to position the beam along the horizontal axis of the screen; the other coil produces a field perpendicular to the horizontal field and positions the beam in the vertical axis. At any one time, the electron beam is under the influence of the magnetic fields produced by both the horizontal and vertical deflection coils. The resultant magnetic field produces a predetermined pattern of uniformly scanned lines called a raster. Both coils are assembled within a cylindrical plastic form with a flared front end shaped to fit the neck contour and the bell of the CRT. The coil windings are configured to generate a magnetic field that is distributed so as to produce geometrical uniformity and wide angle deflection. Other components (mounted on the yoke assembly) that contribute to deflecting the beam or adjusting the raster are the centering rings, correction magnets, ferrite core and fringe-field shields. The fringe-field shields are mounted on the inside of the flared end of the plastic form. They are used to compensate and to shield fringe-field linkages that may affect the electron beam.

Raster: The raster consists of 512 (256 lines for the Model 2 DS) parallel lines uniformly spaced. The raster is rectangular in shape, with its longer dimension extending horizontally. The lines are generated by the simultaneous application of current waveforms to the horizontal and vertical deflection coils. The instantaneous values of the current waveforms are directly proportional to the resulting magnetic field produced by the coils. The raster is visible on the viewing screen when the brightness potentiometer is adjusted to its maximum range of travel, with no video signals present. Normally, however, the CRT cannot be operated at a threshold level so that the raster is visible to the operator with the video signal present.

Figure 2-5 shows the current waveforms applied to the horizontal and vertical deflection coils to generate the raster. Recall that the magnetic field, which positions the beam, is the vector sum of the vertical and horizontal fields generated by the vertical and horizontal coil currents, respectively. The effective starting point for the electron beam is at point A. As the vertical and horizontal coil currents energize their respective coils, the electron beam traverses the path depicted in the figure from A to B in 58.1 μs. The beam then retraces to the top of the screen (point C) in 7 μs, where it is again deflected downward for the next high-speed scan. Note the progression of the high-speed scan from left to right, which is due to the fact that the electron beam is also influenced by the low-speed scan (coil current of the horizontal deflection coil). When point D is reached, the beam retraces to point A to regenerate the raster. The complete raster is generated in 33 ms. Whenever video data is impressed on the cathode of the CRT, the electron beam intensifies for the period of time the video is received. This causes a dot to appear on the screen. The alphanumeric characters are formed from a 5-by-7 dot pattern, as shown in Figure 2-5 for the letter T.

Correction Magnets: Four small permanent magnets are mounted on the deflection yoke to correct for geometric distortion of the raster (called pin-cushioning or barreling). Barreling causes the raster to expand in the center along the vertical or horizontal axes to form a barrel-like appearance; pin-cushioning defines the condition which causes the raster to flare at each end. Magnetic flux supplied by the correction magnets modifies the effects of the main field and minimizes barreling and pin-cushioning of the raster.

Centering Rings: Two centering rings, located on the rear of the yoke assembly, are used to adjust the optical axis of the beam within the viewing screen area. The adjustment is accomplished by rotating each centering ring until the raster is fully displayed on the screen in both the vertical and horizontal axes. The centering rings can be rotated individually or together until the desired results are achieved.

Tilting: If the display on the CRT is slanted or sloped in relation to the horizontal plane, the condition is called tilting. This condition results when

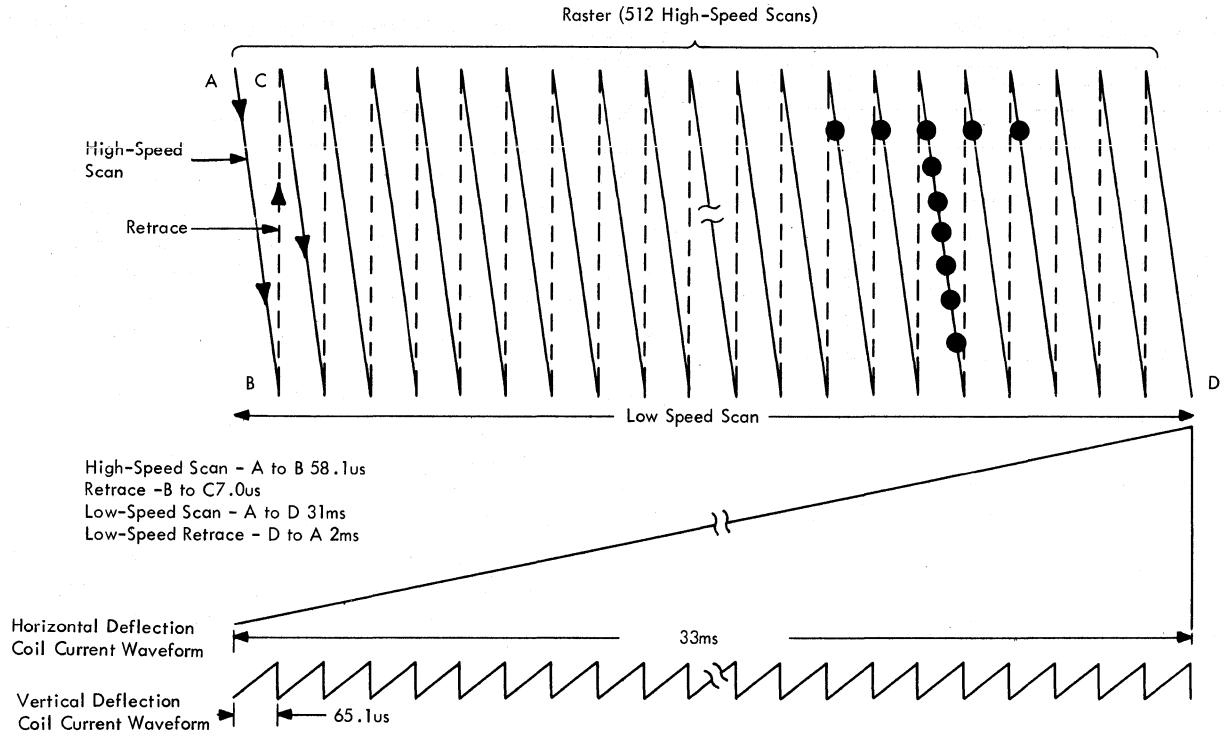


Figure 2-5. Defelection Coil Currents and Raster Relationship

the magnetic field axis does not coincide with the geometric axis of the CRT. Tilting is corrected by merely rotating the entire deflection yoke assembly until the display is aligned with the edges of the bezel. Before rotating the core, however, make certain that the clamp holding the deflection yoke assembly is loosened.

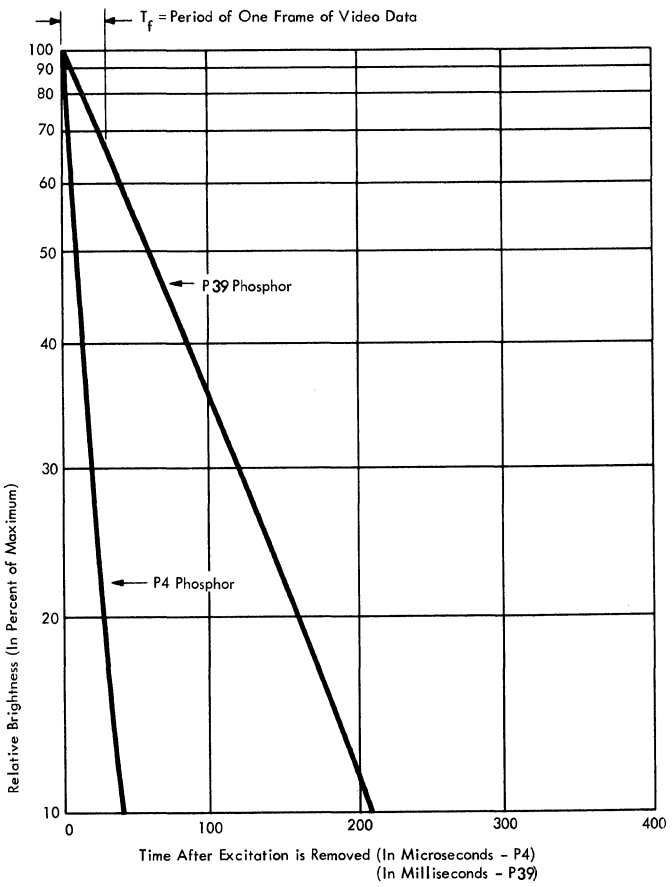
Aquadag Coating

The Aquadag coating used in the CRT is composed of fine graphite particles mixed with water; it is applied to the tube bell to form a conductive lining on its inner and outer glass structure. The inner Aquadag lining is a part of the accelerating anode and carries a potential of 12kvdc. It aids in imparting high velocity to the electron beam. Voltage entry to the Aquadag coating and accelerating anode is made possible through an anode cap located on the top of the tube bell (as viewed in the display station). No physical connection exists between the inner and outer Aquadag layers. The outer (external) layer of Aquadag coating forms a supplementary filter capacitor of 500 to 800 picofarads, which aids in filtering the high-voltage supply. The external layer is the outer plate of the capacitor and must be grounded.

Screen Phosphors

To convert the energy of the electron beam into visible light, the area where the beam strikes is coated with phosphor material which emits light when bombarded with electrons of sufficiently high velocities. This phenomenon is called fluorescence. The continuance of light output for a short time after bombardment has ceased is called phosphorescence. All fluorescent materials are associated with a characteristic relationship between the intensity of the emitted light and the colors contained in that light. Some emit a green light; others emit yellow, blue, orange, etc., depending upon the phosphor or mixture of phosphors used. All fluorescent materials have an afterglow or phosphorescence; the duration (persistence) of the afterglow varies with the material as well as with the energy (velocity and current) of the beam.

The persistence of the screen is generally designated by a "P number". Where a CRT is used for observing periodic phenomena which occur at a low repetition rate, screen material (a tube) on which the image will linger is desirable. Such a tube is described as a "long persistence" tube. Where the image changes rapidly, a "short persistence" tube is employed. The CRT used in the Model 1 display station incorporates a P39 aluminized phosphor screen; the Model 2 display stations contain CRT's with a P4 screen. The decay characteristic (persistence) of the P39 screen is shown in Figure 2-6. The figure also shows the decay characteristic of a P4 screen. Note the faster decay characteristics of the P4 curve relative to that of the P39 phosphor.



●Figure 2-6. Persistence Characteristics of P4 and P39 Phosphors

Although the P39 phosphor has inherently what is considered a medium persistence phosphor, it is necessary to periodically "repaint" the data displayed on the screen to reduce flicker. A repaint rate (frequency) of 30 frames per second is used in the Model 1 display station; a repaint rate of 60 frames per second is used in the Model 2.

CRT Electrode Potentials

Voltages applied to the various electrodes of the CRT are summarized (for reference) as follows:

Filament	6.3vdc
Cathode	+10 to +140vdc in addition to a -30v peak video signal
G1	0vdc (Ground)
G2	B+ (approx +134vdc)
G3 and G5	10.5 to 12kvdc
G4	0v (Ground), +80vdc, B+, or B boost for adapter boards -84 to +450vdc for newer level boards

Display Station Electronics for DS Using Older Level Circuit Boards

The circuit descriptions in the following paragraphs apply to older level circuit boards. Some display stations use older level circuit boards with adapters plugged into tube sockets to modify the earlier design level. The circuits affected by the adapter change are described under "Display Station Electronics for DS Using Tube Adapters". More recently manufactured display stations use a newer level circuit board (without adapters) which incorporates circuit improvements obtained by using adapters on older boards and also provides additional improvements. Circuits affected by using the newer level board are described under "Display Station Electronics for DS Using Newer Level Circuit Boards". Regardless of whether an older level board with adapters or a newer level board is used, almost all operations described for the older level boards apply to all circuit boards.

Video Amplifier

The composite video signal is transmitted from display control over a transmission line (coax) and enters the display station via jack J1 (Figure 2-7). The coax line is terminated by a 93-ohm resistor; the 93 ohms constitutes the characteristic impedance of the line and ensures maximum signal transfer to the display station. A display station can be located a maximum of 2000 feet from display control. Taps A, B, and C are provided to ensure sufficient contrast at the CRT, depending on the length of the cable servicing the display station. The selected tap should provide a peak-to-peak composite video signal of 1.5v to 3v at test point 1 (TP1).

The composite video signal is coupled through capacitor C1, developed across grid resistor R4, and applied to the grid of video amplifier V1A. Tube V1A is a wide-band video amplifier with a flat frequency response to 4.5 ms. Its upper limit of half-power frequency response is approximately 8 mc. Shunt and series peaking provided by inductors L2 and L11 aids in improving the high-frequency bandpass. Resistors R5 and R7 are plate load resistors. The amplifier is self-biased by C2 and R5 and operates essentially Class A.

The inverted amplified video of 30v peak-to-peak, appearing on the plate of V1A, is coupled through C3 to the cathode of the CRT. Video signals unblank the tube and intensify the beam during the time that each video pulse is received. Although sync signals are also impressed on the cathode of the CRT, they do not intensify the beam because they are opposite in polarity from the video signals and, hence, drive

the tube farther into cutoff. Brightness bias (threshold level) is provided by R9, R8, and potentiometer R10. Resistor R8 is a limiting resistor that prevents the console operator from adjusting the brightness to a level that will endanger the phosphor in the CRT. Normally, when video signals are impressed on the cathode and potentiometer R10 is adjusted for maximum brightness, the resistance of R8 prevents the raster from being displayed.

Sync Clipper

The sync clipper (V1B) removes the video by clipping action and passes the sync signal to the horizontal and vertical sweep circuits. Because the cathode is grounded, any negative signals (video) developed across R14 will not cause V1B to conduct, whereas the positive sync signal will permit the clipper to conduct. Negative-going sync pulses will appear on the plate of V1B each time a positive sync pulse is applied to the grid. A high-speed sync pulse appears every 65.1 μs; low-speed sync pulses recur every 33.3 ms. The composite sync (high-speed and low-speed) can be viewed at TP3.

Horizontal Multivibrator

The horizontal multivibrator generates the horizontal sweep that deflects the beam horizontally on the CRT. The multivibrator consists of V1C, V2, and associated components (Figure 2-7). As the sync pulses are passed by the clipper, they are fed to an integrating network consisting of R16, R18, and C7. The time constant of this network permits only the low-frequency serrated sync pulse to appear on the control grid of V1C. Assuming that the horizontal scan is beginning at the left edge of the raster, C11 and C16 will take on a charge through R74, R75, and R23 toward the B+ supply and boost voltage set by R23. This causes the sweep to traverse from left to right because V2 is conducting. Resistor R23 (horizontal linearity control) is tied between B+ and the boost voltage. The boost voltage will be approximately 250 to 410v. As the beam reaches the right side of the screen, the low-speed sync pulse supplied by the clipper passes into the grid of V1C and the grid of V2 through C9. As this occurs, it causes V1C to go into heavy conduction by the plate pullover action of V2. As V1C goes into conduction, capacitors C11 and C16 are rapidly discharged through the plate impedance of V1C. This discharge time is about 1 ms, and the horizontal sweep retraces from the right edge to the left edge of the screen.

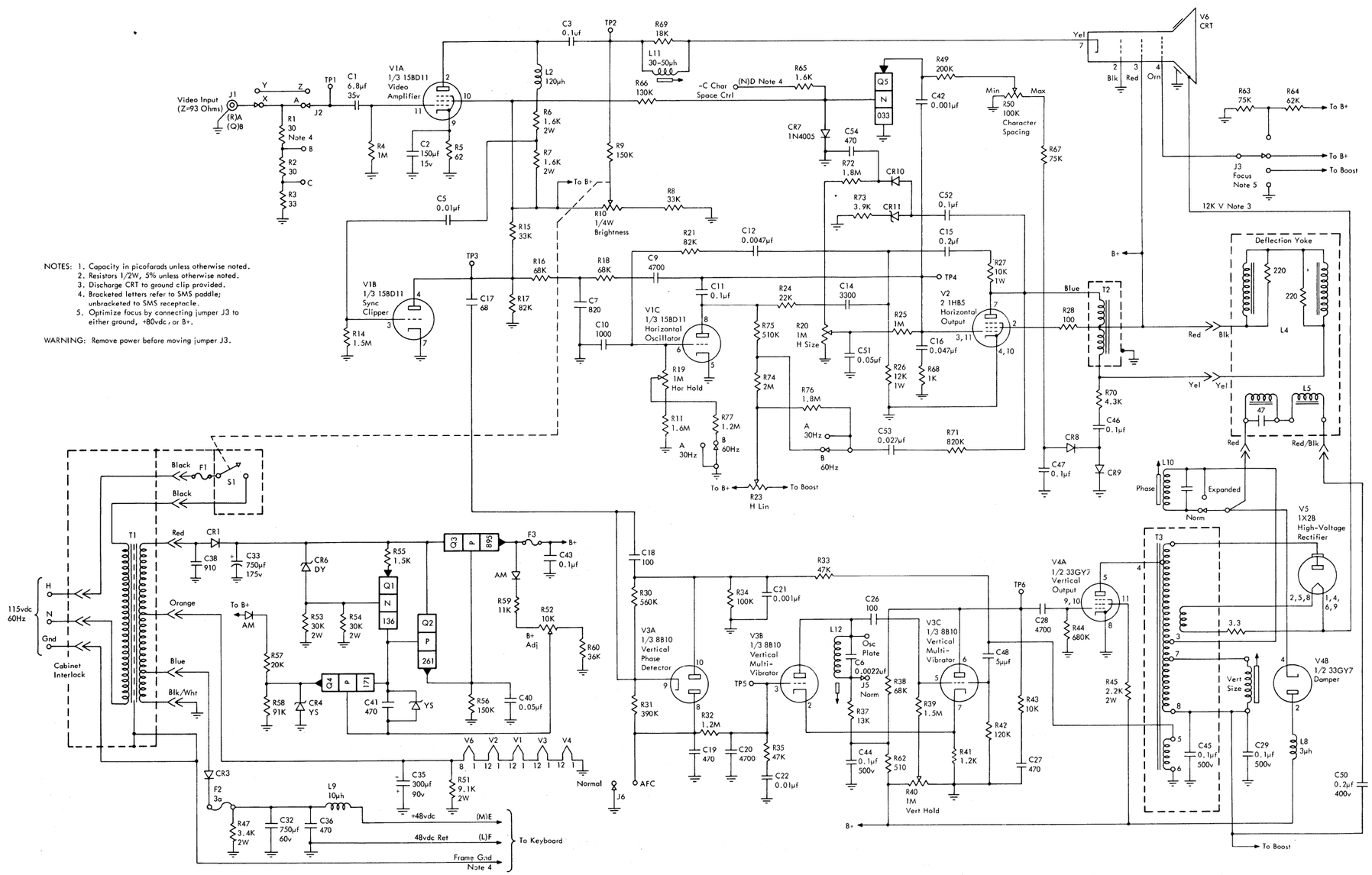
Capacitor C10, together with potentiometer R19, controls the pulse width output of the multivibrator. Potentiometer R20 adjusts the bias on the grid of V2 and, therefore, the time during which V2 is turned on. Potentiometer R20 permits adjustment of the length of the horizontal sweep. After the length of the horizontal sweep is adjusted, the network consisting of R72, R73, CR10, CR11, and C52 aids in holding the horizontal size constant. Potentiometer R23 exercises control of the charging voltage to which C11 and C16 attempt to charge. This permits control of sweep linearity of the right half of the sweep. Resistor R70 provides a faster retrace and the negative voltage required for character spacing. Transformer T2 is also used as a matching transformer to match the high plate impedance of V2 to the low resistance of the horizontal sweep coils of the deflection yoke. Capacitor C53 and resistor R71 aid in reducing the effects of S-shaping of the electron beam due to the non-flat surface of the screen. S-shaping is required more for the Model 2 display station than for the Model 1.

The pulse width output of the multivibrator is adjusted so that the duration of the ramp (scan time) is slightly longer than the time between the horizontal (low-speed) sync pulses. As a result, operation of the multivibrator is abruptly terminated when the horizontal sync pulse is received. This terminates the scan by causing V2 to turn off and V1C to conduct heavily. If the time duration of the multivibrator is less than or extremely longer than the time between sync pulses, it will be virtually impossible to synchronize the horizontal sweep. Operation of the horizontal multivibrator also varies directly with temperature.

Character width and spacing between characters are also controlled by horizontal output tube V2 in conjunction with the character spacing network. The character spacing network consists of transistor Q5 and its associated components, plus C46, C47, CR8, and CR9. During horizontal retrace time, C46 couples the high-voltage spike present on the horizontal ramp (caused by the retrace spike from the deflection yoke). Capacitor C47 is charged negatively through diode CR8. Once charged to a negative value, C47 is permitted to discharge through R67 and the CHARACTER SPACING potentiometer, R50. As C47 discharges, C42 integrates toward the voltage value across the character spacing potentiometer. The charged value appearing across C42 is impressed on the control grid of V2 and superimposed on the 33.3-ms horizontal sweep voltage. A 65-μs Character Space Control signal turns on transistor Q5 to discharge C42 during the blank scan line between characters. When a video scan line is again swept on the CRT, the Character Space Control signal is removed, Q5 turns off, and C42 is allowed to begin charging to the value across R50 as C47 continues to discharge. The maximum charging potential available to C42 is less than the previously charged

NOTES:
1. Capacity in picofarads unless otherwise noted.
2. Resistors 1/2W, 5% unless otherwise noted.
3. Discharge CRT to ground clip provided.
4. Bracketed letters refer to SMS paddle; unbracketed to SMS receptacle.
5. Optimize focus by connecting jumper J3 to either ground, +80vdc, or B+.

WARNING: Remove power before moving jumper J3.



● Figure 2-7. Display Station, Electrical Schematic Diagram for DS Using Older Level Circuit Boards

value. Hence, the positive value impressed on the control grid is diminished as the horizontal sweep progresses across the screen. This is advantageous because progressively less control need be exercised on V2 for character spacing as the horizontal sweep moves along the horizontal axis. Character width and the spacing between characters can be adjusted within the operating limits of potentiometer R50. Increasing the resistance of R50 increases the width of the characters and, simultaneously, decreases the spacing between characters; conversely, decreasing the resistance of R50 decreases character width and increases character spacing.

The horizontal multivibrator can operate at 30 cps or 60 cps, depending on how the circuit was wired at the time it was manufactured. Note the two jumpers (30- or 60-cps operation) in the horizontal multivibrator circuit. The Model 1 display station will always be wired for 30-cycle operation, whereas the Model 2 is prewired for 60 cps. A horizontal sweep frequency of 60 cps permits use of the short-persistence P4 CRT, which carries inherent characteristics of longer tube life. Model 1 display stations utilize a CRT with a P39 screen; CRT's with a P4 screen are employed in the Model 2 since they are wired to operate with a horizontal sweep frequency of 60 cps. Selection of the short- or long-persistence CRT is therefore related to the frequency of the horizontal sweep circuits.

Vertical Phase Detector

Tube V3A is a duo diode which operates as a phase comparator. The vertical phase detector provides dc error voltage to the grid of V3B whose polarity and magnitude are proportional to the difference in phase between the high-speed sync pulse and a reference pulse coupled back from the flyback transformer. If the vertical multivibrator falls out of sync or shifts in phase relative to the incoming sync pulse, the condition is detected by the phase comparator, and a correction signal is fed to the grid of V3B. This signal biases the grid of V3B and causes the multivibrator to speed up or slow down, depending on the magnitude and polarity of the correction signal. Stabilization of the multivibrator occurs when its operating frequency coincides with the repetition rate of the incoming sync pulses. The quiescent operating point for the grid of V3B (measured to ground) is approximately 0.4v. Correction voltage excursions applied to the grid of V3B can range between +0.8v and 0v. These voltage limits are related to the position of the VERT HOLD control potentiometer.

The high-speed sync signal from the clipper passes through high-pass filter capacitor C17 to supply the cathode of the vertical phase detector (Figure 2-7) with a differentiated signal. The output of the reference winding (pin 5 of transformer T3) enters the phase detector on pin 10 through a pulse-forming network consisting of R33, R34, and C21. When a difference in phase exists between the two input signals, a dc voltage is developed across R31. This voltage is fed to the grid of V3B. A filter network, consisting of R32, C19, and C20, shunts to ground any 15-kc or low-frequency components that may ride on the dc bias developed in the phase detector. The network consisting of C22 and R35 provides anti-hunt control and critically damps the AFC system. Jumper J6 is used to short the AFC voltage to ground when the vertical multivibrator is adjusted. During normal operation, the jumper is in the NORMAL position, as shown.

Vertical Multivibrator

Tubes V3B and V3C (Figure 2-7) form a voltage-controlled free-running multivibrator that utilizes cathode coupling and a common cathode resistor. The vertical multivibrator supplies the vertical output circuit with a ramp voltage to deflect the electron beam vertically on the CRT. The ramp voltage is made available at the output of the multivibrator (TP6) by permitting C26 to charge toward B+ through R38 and R45. As C26 discharges exponentially, V3B conducts linearly until the multivibrator switches. At this time V3C turns on, discharging C27 through R43, terminating the ramp waveform on C27. C26 now charges, causing the grid of V3C to become more negative and through cathode coupling turns on V3B. When V3B turns on, V3C turns off, allowing C27 to charge exponentially toward B+ through R38 and R43. This waveform is coupled through C28 to the grid of V4A. C26 then discharges and the cycle is repeated. Although the ramp, at this point, is not as linear as might be expected to produce a linear sweep, further shaping takes place in the plate circuit of the vertical output tube.

Because the vertical multivibrator operates at a much higher frequency than the horizontal multivibrator (15,360 cps vs 30 cps), self-correcting methods are employed in the vertical sweep system to maintain synchronization with the incoming vertical sync signals. The vertical multivibrator can also correct for variations in operating voltages and temperature changes within the display station. The correction is effected by a servo loop that consists of the phase detector, vertical multivibrator, and vertical output circuits. If the frequency of the vertical multivibrator drifts for any of the conditions noted, a correction voltage is generated by the phase detector to increase or decrease the frequency of the multivibrator until stabilization is

achieved. This is accomplished by inductively coupling a portion of the vertical output signal back to the phase detector. The output signal is compared with the incoming sync signal to produce a dc voltage whose magnitude and polarity are proportional to the difference in phase of the two input signals. The correction signal increases or decreases the bias of V3B, which speeds up or slows down the operation of the multivibrator. The vertical oscillator coil provides sufficient frequency control for the oscillator, thus ensuring operation within the "pull-in" limits of the phase detector during those periods when sync pulses are not supplied by the control unit or when power is initially turned on.

Jumper J5 is normally in the position shown for normal operation. When aligning the vertical multivibrator, the tank circuit comprising L12 and C6 is shorted by moving jumper J5 to the OSC PLATE jack. After the vertical hold adjustment is completed, the jumper must be returned to the NORM position.

Vertical Output Circuit

The vertical output circuit shapes and amplifies the voltage ramp supplied by the vertical multivibrator. The ramp signal is coupled through C28, developed across grid resistor R44, and applied to the control grid of V4A. Application of the ramp signal causes V4A to conduct, which produces a current ramp in the plate circuit and the primary of the flyback transformer (tap 3 to 4). As plate current flows through the primary winding, a voltage is induced in the secondary winding between taps 7 and 8. This section of the flyback transformer supplies the vertical deflection coils with the necessary current to pull the electron beam from the top to the bottom of the raster. Therefore, as plate current in V4A increases, the electron beam traverses a path from the upper to the lower limits of the screen. The time required to sweep the beam one scan is 58.1 μs. At the end of each vertical scan, the vertical output tube is turned off, the field in the vertical deflection coils collapses, and the beam retraces to the top of the screen. As the beam retraces, the inductive energy stored in the vertical deflection coils collapses, causing voltage to appear across taps 7 and 8 of the flyback transformer. This reactive energy is used to generate the high voltage required by the accelerating anode in the CRT.

The phase coil L10 and capacitor C37 limit the display along the vertical axis to 3 inches when jumpered to the NORM position. When the jumper is placed in the EXPANDED position, the display can be expanded vertically by tuning the slug in L10. Vertical expansion is only employed in the 240- and 480-character displays.

High-Voltage Rectifier

The high-voltage rectifier (V5) rectifies the high voltage developed across the flyback transformer during retrace time. Reactive energy is stored in the vertical deflection coils as the sweep is deflected vertically during scan time. When the sweep retraces, the reactive energy is reflected back into the secondary between taps 7 and 8 of the flyback transformer. This reflected energy induces a high-voltage pulse, 7 to 10 μs in duration and approximately 15 kv (peak volts), across the entire winding of the transformer. The high-voltage rectifier rectifies the high voltage obtained as a result of the field collapsing in the vertical deflection coils during retrace time and supplies approximately 12kvdc to the accelerating anode. The capacity that exists between the inner and outer layers of Aquadag coating of the CRT provides the necessary filtering for the power supply. Filament voltage for V5 is provided by a two-turn winding on the flyback transformer. A 3.3-ohm resistor, in series with the filament winding, limits the current to a safe value.

Damper Circuit

The damper circuit consists of diode V4B and inductor L8. During the scan cycle, the damper tube supplies the plate of the vertical output tube with B+ power and aids in obtaining a greater degree of vertical sweep linearity. Inductor L8 prevents the output tube from oscillating. The vertical size control, L7, in parallel with a portion of the flyback transformer, permits adjustment of the vertical height or size of the vertical sweep. Tuning the ferrite slug in the vertical size control changes the inductance of the coil, thus preventing energy generated in the flyback transformer from being fed to the deflection coils.

Capacitor C29 is employed to generate a boost voltage as the beam retraces to the top of the screen. When the field collapses in the core of the yoke, a voltage is induced in the lower winding of the flyback transformer (taps 7 and 8) as a result of current flow between L5 and tap 7. During this time, C29 charges to approximately 260vdc. This charged value is added to B+ (140vdc) to produce a total boost voltage of 400vdc. Since the charged voltage across C29 aids or is added to B+, the resulting voltage is called boost voltage. The boost voltage on old level circuit boards only is used as a focusing potential on the focusing anode, if required, as described under "Beam Focusing". The boost voltage on all circuit boards is also used in conjunction with B+ as the charging voltage for the RC sweep network employed in the horizontal multivibrator.

Display Station Electronics for DS Using Tube Adapters

Some display stations using older level circuit boards employ adapters plugged into tube sockets to provide improved circuit performance. Figure 2-7A shows the schematic diagram of a display station using tube adapters. Comparison of Figure 2-7A with Figure 2-7 shows the following circuit differences: (1) a change in the method of biasing the grid of sync clipper V1B and (2) addition of a transistor driver stage in the grid circuit of horizontal oscillator stage V1C. The remaining circuits which comprise most of the electronics are the same as shown in Figure 2-7 and described earlier for DS using older level circuit boards.

Sync clipper V1B (Figure 2-7A) removes the video and passes the sync signal to the horizontal and vertical sweep circuits. Negative signals (video) developed across R107 will not cause V1B to conduct, whereas positive sync signals will permit the clipper to conduct. CR22 and R106 form a threshold bias network preventing noise signals from passing through the clipper. DC voltage is tapped from the -84vdc filament supply to establish a bias voltage source. Negative-going sync pulses will appear on the plate of V1B each time a positive sync pulse is applied to the grid. A high-speed sync pulse (vertical sync) appears every 65.1usec; low-speed sync pulses recur every 16.6ms (horizontal sync). The composite sync (high-speed and low-speed) can be viewed at TP3.

The horizontal multivibrator generates width and spacing between characters. The multivibrator consists of V1C, V2, and associated components (Figure 2-7A). As the sync pulses are passed by the clipper, they are fed to an integrating network consisting of R100, R101, C101, and C102, causing pulse amplifier Q10 to conduct. When conducting, Q10 turns on V1C by grounding the grid. The time constant of the integrating network permits only the low-frequency serrated sync pulse to appear on the control grid of V1C. The remainder of horizontal multivibrator operation is the same as described under "Horizontal Multivibrator" for DS using older level circuit boards.

Display Station Electronics for DS Using Newer Level Circuit Boards

Recently manufactured display stations use newer level circuit boards. The electrical schematic is shown in Figure 2-7B. The new boards incorporate the circuit changes obtained by installing adapters on older level boards, as described in the preceding paragraphs. In addition, extensive changes have been made to the B+ power supply. These changes are described as part of the display station power supply under "B+ Supply for Newer Level Circuit Boards".

Display Station Power Supply

Power for the entire display station is supplied by a 115vac, 60-cycle, single-phase, self-contained power supply. The power supply makes available three dc voltages that are necessary to power the display station electronic circuits and keyboard operations. The three voltages are +48v, B+ (approximately +134v), and -84v. Only the B+ section of the supply contains a regulator. The B+ voltage services the electronic circuits of the display station. The B+ supply circuitry used on newer level circuit boards differs from that used on older level boards. The -84v is used for the tube filaments of V1, V2, V3, V4, and V6. The +48v supply services the manual input keyboard restore magnets, data contacts, and shift relay. The low-voltage power supply for display stations using older level circuit boards is illustrated in Figure 2-7. Power is applied to the primary of transformer T1 when switch S1 is closed. Switch S1 is an integral part of the brightness control and is activated by push-pull action. With the primary power applied, three voltages are made available across the four-tap secondary. The lowermost tap is grounded, and all voltages are measured in relation to ground. Transformer T1 steps up the input voltage by transformer action because of its turns ratio of 1.2 to 1. The following wire-color code defines the voltage levels of the tapped secondary:

Color Code	AC Volts (rms)
Red	136
Orange	67
Blue	42
Black/White	Ground

When the display station is powered from a 50-cycle source, a 50-cycle power transformer must be used, as shown in Figure 2-8. The primary of the transformer is also tapped to accommodate various line voltages of 112.5vac, 123.5vac, 195vac, 220vac, or 235vac. The lead on switch S1 is connected to the terminal on TB1 that corresponds to the source voltage available at the particular installation. The primary is also protected by fuse F1, rated to the proper value, dependent on whether a low- or high-voltage input is used. Frame ground originating from the power source is indicated on the transformer case with a circled ground symbol. Operation of the display station power supplies is exactly the same for both 50-cycle and 60-cycle supplies.

NOTE: The actual voltage used in a particular display station is noted on a label attached next to TB1. If the input service voltage is changed, it should be noted, and the label should be changed to reflect the actual service voltage to which the display station is connected.

B+ Supply for DS Using Older Level Circuit Boards

The B+ supply consists of a half-wave rectifier, a constant current source, and a closed loop regulator. Half-wave rectification of the stepped-up 136v appearing on the upper tap of transformer T1 is performed by silicon diode CR1 to charge C33. This produces a dc voltage at the junction of C33 and Zener diode CR6. A constant 5v is maintained across Zener diode CR6; this voltage also appears across the base emitter junction of transistor Q1 and R55. Since the voltage and resistance in the branch of Q1 remain constant, Q1 serves as a constant current source.

Resistors R53 and R54 are bias resistors for Q1. The output current of Q1 divides at the node between Q1, Q2, and Q4, depending upon the potential on the base of Q4. Note, however, that the current appearing at the node is maintained at a constant value. Transistors Q2 and Q3 are used as current amplifiers and provide a B+ voltage. The B+ voltage value (about 134vdc) is adjusted to a value relative to the ambient temperature. The B+ voltage can be adjusted by potentiometer R52, which is in series with the voltage divider network comprising R59 and R60. Approximately 100v will exist on the movable arm of potentiometer R52; this is the potential applied to the base of Q4. Resistor R58, together with Zener diode CR4, biases the emitter of Q4 to 100v. Regulation of the +134v supply is controlled by the conduction of Q4, which diverts a portion of the current at the node to ground if the output voltage increases. If the output voltage decreases, conduction of Q4 decreases, permitting more current at the node to branch to Q2. For example, assume that the B+ output increases. This causes the voltage on the arm of potentiometer R52 to increase, supplying a higher voltage to the base of Q4. This increases the conduction of Q4, which diverts more of the current at the node through Q4. Less current is branched to Q2; therefore, the output voltage decreases. Capacitors C41, C40, and R56 stabilize the regulator and prevent the circuits from oscillating. Sharp transient voltages, especially when power is initially turned on, are shunted to ground by capacitor C38.

B+ Supply for DS Using Newer Level Circuit Boards

The B+ supply consists of a half-wave rectifier and a closed loop regulator. Half-wave rectification of the stepped up 136v appearing on the upper tap of transformer T3 is performed by silicon diode CR10 to charge C43. C42 protects the supply by shunting sharp transient voltages to ground. The dc voltage is applied to the collectors of series regulators Q3 and Q4. Q3 controls conduction of Q4 and thereby the B+ supply output voltage. The current source used to supply base current to Q3 is obtained from a voltage doubler consisting of C38B, C39C, C41, CR11, CR12, R67, and R68. Base current for Q3 is obtained through series-dropping resistor R69. B+++ voltage is provided by the voltage doubler to supply G3 of the CRT. The voltage regulator operates by comparing the reduced B+ voltage at the base of Q6 and the voltage on CR14 and, as a result, varying conduction through Q6, Q3, and Q4. Emitter follower Q5 generates a reference voltage used by Q6. This voltage is developed by a 100v potential across Zener diode CR14. If the output voltage decreases, the base-to-emitter bias on Q6 becomes less positive and conduction through Q6 decreases, causing the voltage at the collector of Q6 to become more positive. The forward bias on Q3 is increased, causing Q3 and Q4 to conduct more current, thereby raising the B+ voltage. If the output voltage rises, conduction through Q6 increases, the potential at the base of Q3 drops, and conduction through Q3 and Q4 is reduced, causing the B+ voltage to drop.

-84VDC Supply

The -84vdc supply provides the voltage required to service the filaments of V1, V2, V3, V4, and V6. The filaments of these tubes are series-connected. Half-wave rectification during the negative half-portion of the input voltage is used to balance the load on T1 and prevent the core from saturating. Rectification is provided by silicon diode CR2. The dc voltage is filtered by C35, making available -84vdc with approximately a 15v peak-to-peak ripple for the filament string. Load resistor R51 discharges C35 when power is turned off in the event of a tube filament failure. The dc filament supply is employed to reduce the effects of the 60-cycle line frequency on the sweep circuits.

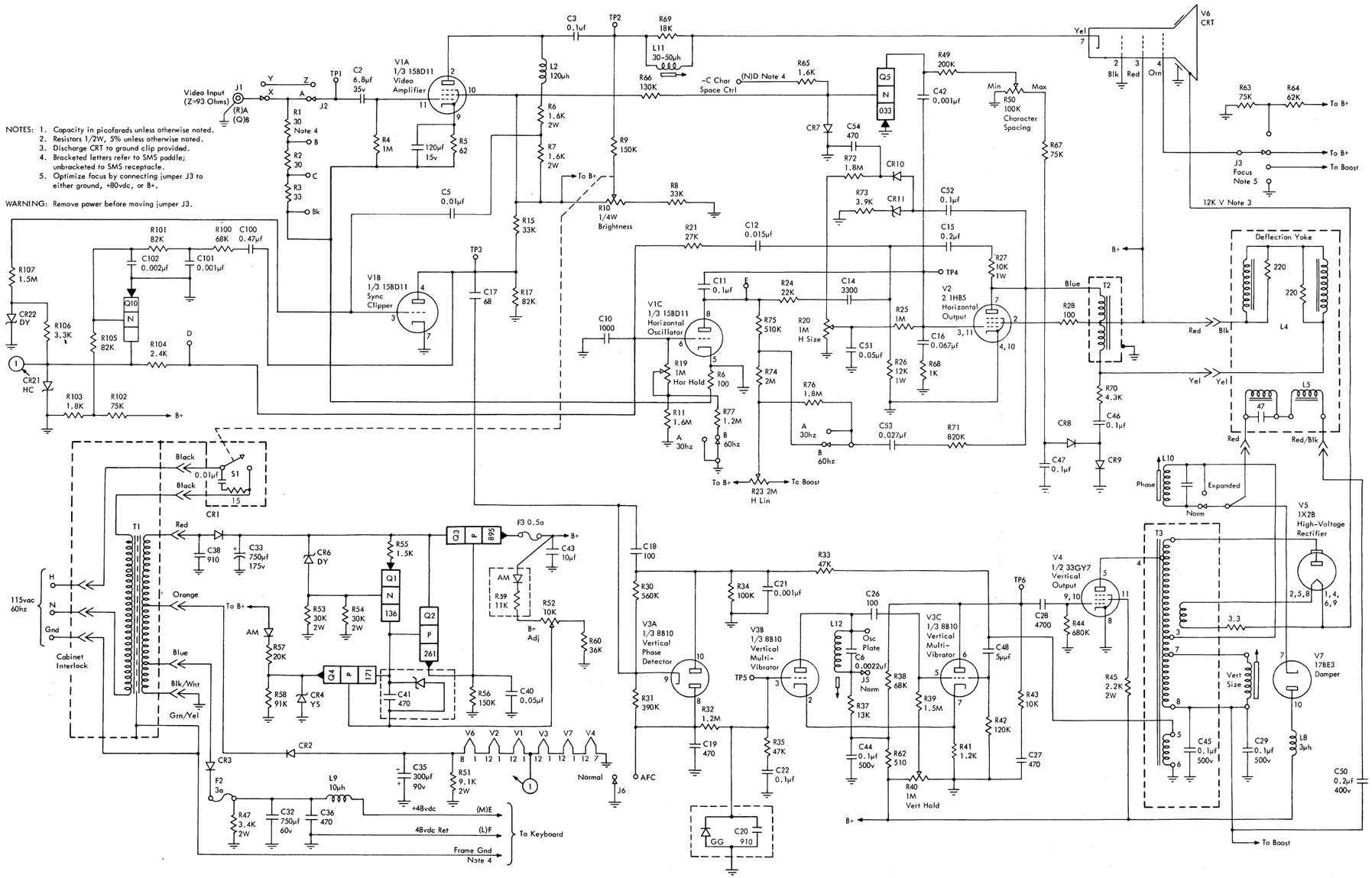
On older level circuit boards using adapters, a bias voltage for the sync clipper (V2B) designated F- is obtained by tapping a portion of the filament voltage and applying it across R76 and CR17. See Figure 2-7A. On newer level circuit boards, the bias voltage F- is also used. In addition, the full supply output, designated F- -, is applied to one side of potentiometer R14 as part of a voltage divider network for focus adjustment.

+48VDC Supply

The +48vdc supply is similar to the 84v supply. Rectification is provided by CR3, and the supply is protected by fuse F2. The dc voltage is filtered by C32.

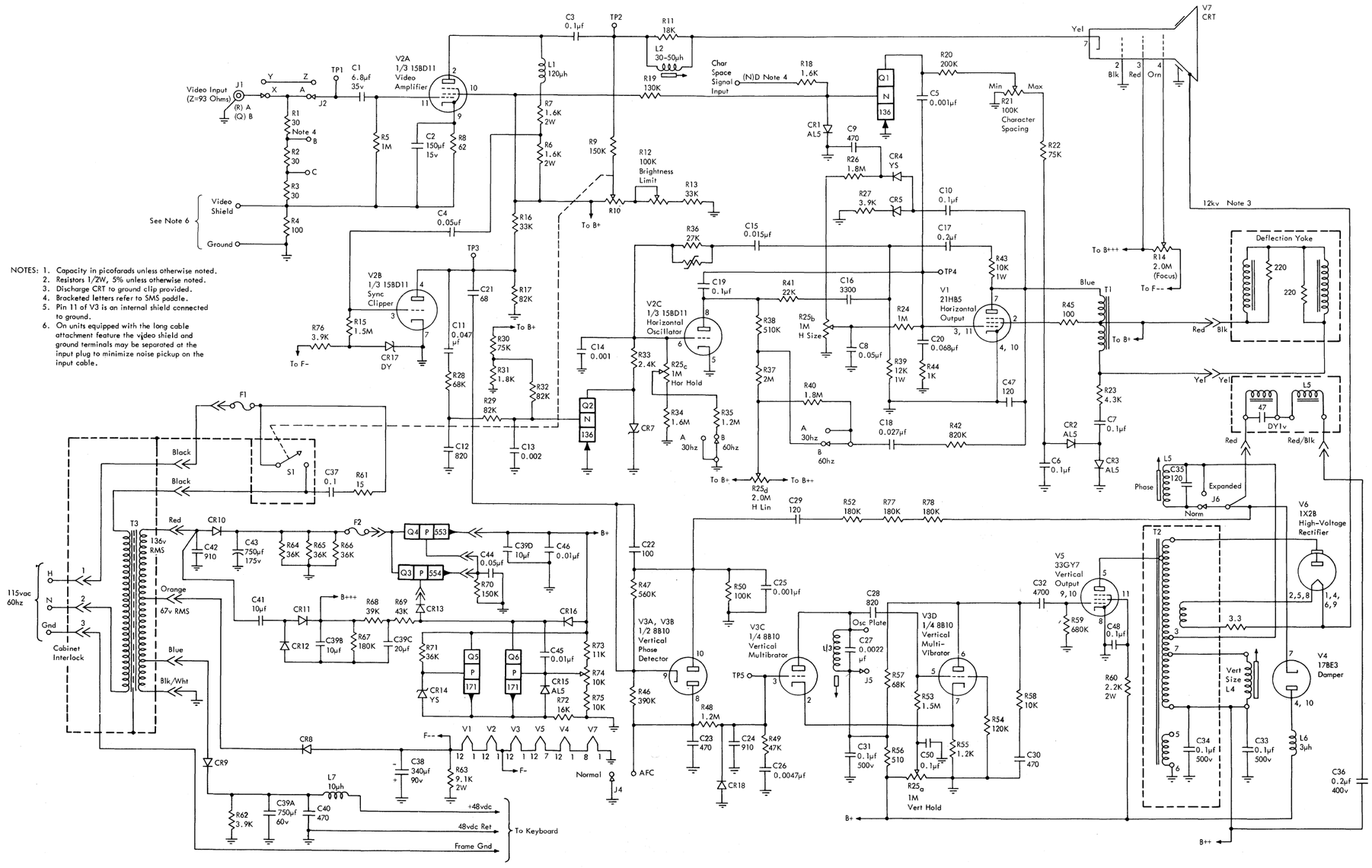
NOTES:
1. Capacity in picofarads unless otherwise noted.
2. Resistors 1/2W, 5% unless otherwise noted.
3. Discharge CRT to ground clip provided.
4. Bracketed letters refer to SMS paddle; unbracketed to SMS receptacle.
5. Optimize focus by connecting jumper J3 to either ground, +80vdc, or B+.

WARNING: Remove power before moving jumper J3.

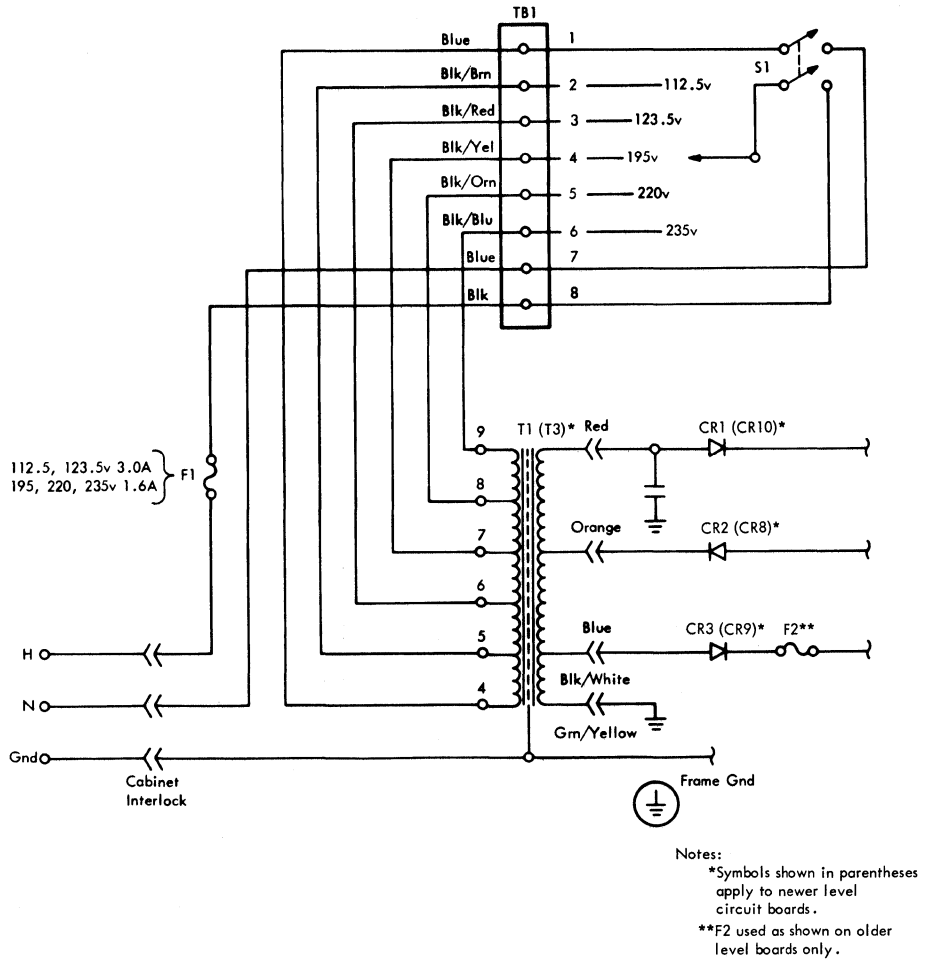


●Figure 2-7A. Display Station Electrical Schematic Diagram for DS Using Tube Adapters

NOTES:
1. Capacity in picofarads unless otherwise noted.
2. Resistors 1/2W, 5% unless otherwise noted.
3. Discharge CRT to ground clip provided.
4. Bracketed letters refer to SMS paddle.
5. Pin 11 of V3 is an internal shield connected to ground.
6. On units equipped with the long cable attachment feature the video shield and ground terminals may be separated at the input plug to minimize noise pickup on the input cable.



●Figure 2-7B. Display Station Electrical Schematic Diagram for DS Using Newer Level Circuit Boards



●Figure 2-8. Display Station Power Supply for 50-Cycle Operation

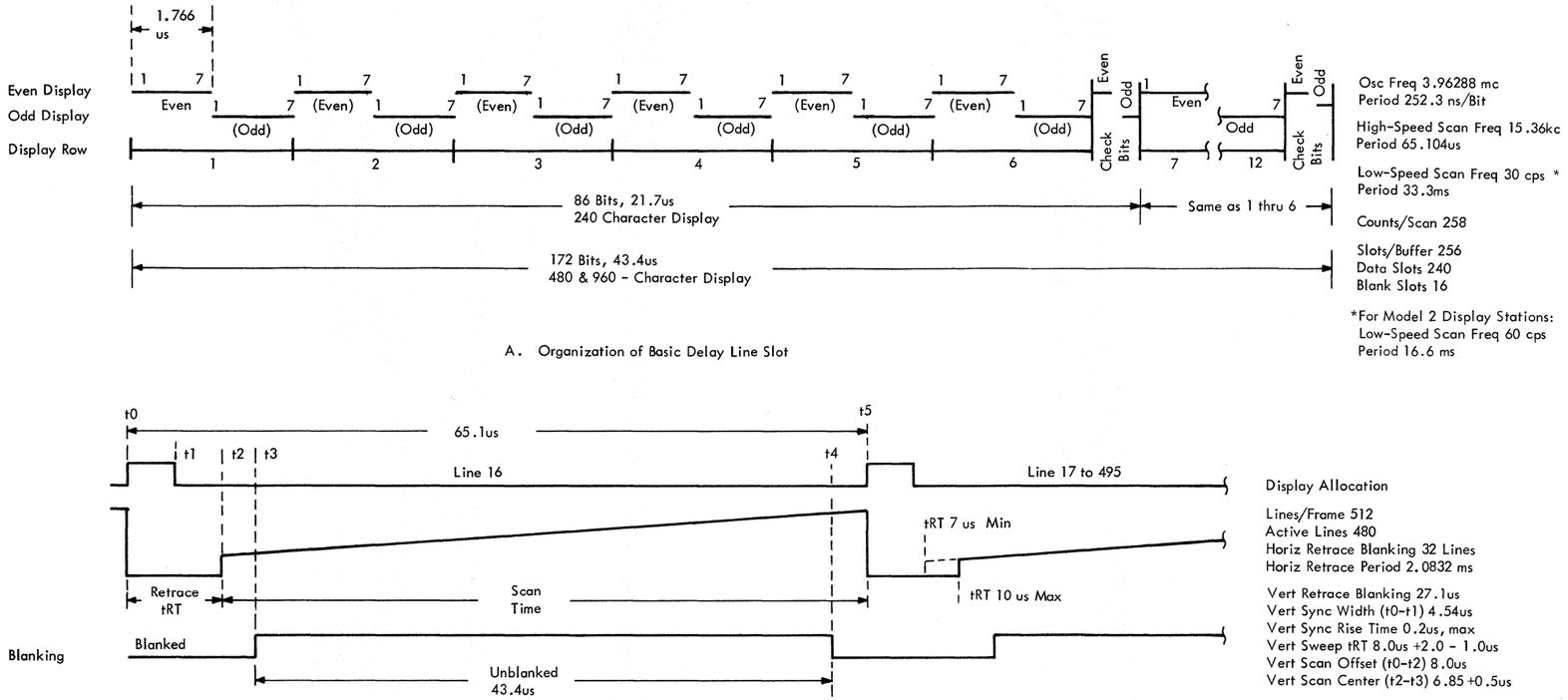
Bleeder resistor R47 discharges C32 when power is removed. This supply differs from the 84v supply in that an RF filter is used to prevent keyboard noise from interfering with the display station electronic circuits. The voltage value under no-load conditions is approximately +60vdc. The no-load value decreases to +48v as a function of the rate at which the keyboard is operated.

Display Station Timing

The overall display station timing required to display information on the viewing screen of the CRT is summarized in Figure 2-9. When composite video is received from display control, it is separated into two main elements, video and synchronizing pulses. The video signals are impressed on the cathode of the CRT to intensify the electron beam. The vertical and horizontal sweep circuits position the electron beam to form a raster on the CRT screen. Both the horizontal and vertical sweep circuits are maintained in synchronism by the sync pulses received as part of the composite video.

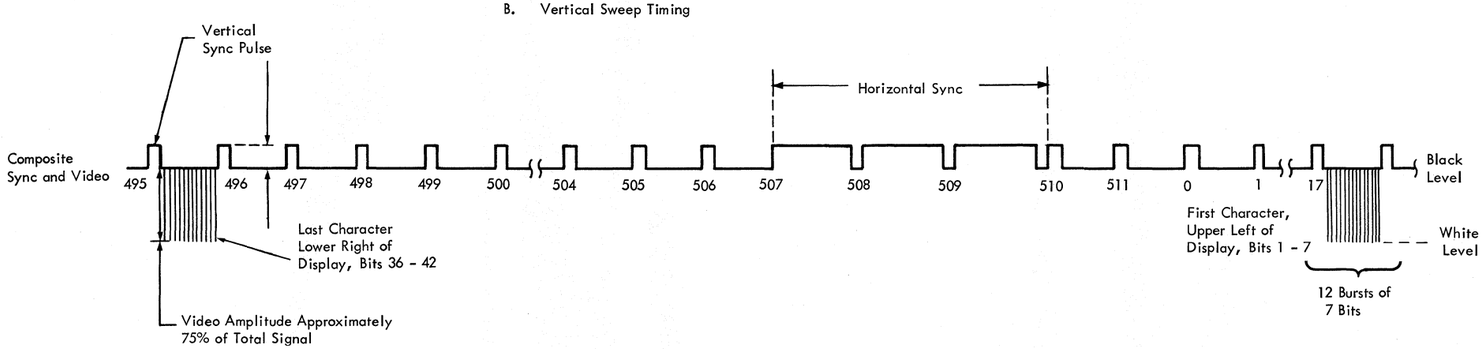
Organization of Basic Delay Line Slot

A basic delay line slot (Figure 2-9, A) consists of 7-bit readouts from a delay buffer. Each delay line buffer contains two delay lines. Data readout is accomplished by alternating bit readout from each of the two delay lines. Interleaving storage and readout of bit information in this manner increases the speed of data presentation on the CRT by a factor of 2. Each buffer has a storage capacity of 256 slots; 240 slots contain data, and 16 are blank; the blank slots allow time for horizontal retrace. Each slot consists of 86 bits, and 21.7 μs are required to present the information in one scan line on the CRT. Note, however, that each readout, consisting of seven bits, is alternately displayed on two display stations (even and odd displays). All display station models utilize a 512-line vertically oriented raster to present information on the viewing screen. As information is received, the lines that contain data are unblanked by the video pulses, thus causing the beam to intensify during the time that video data



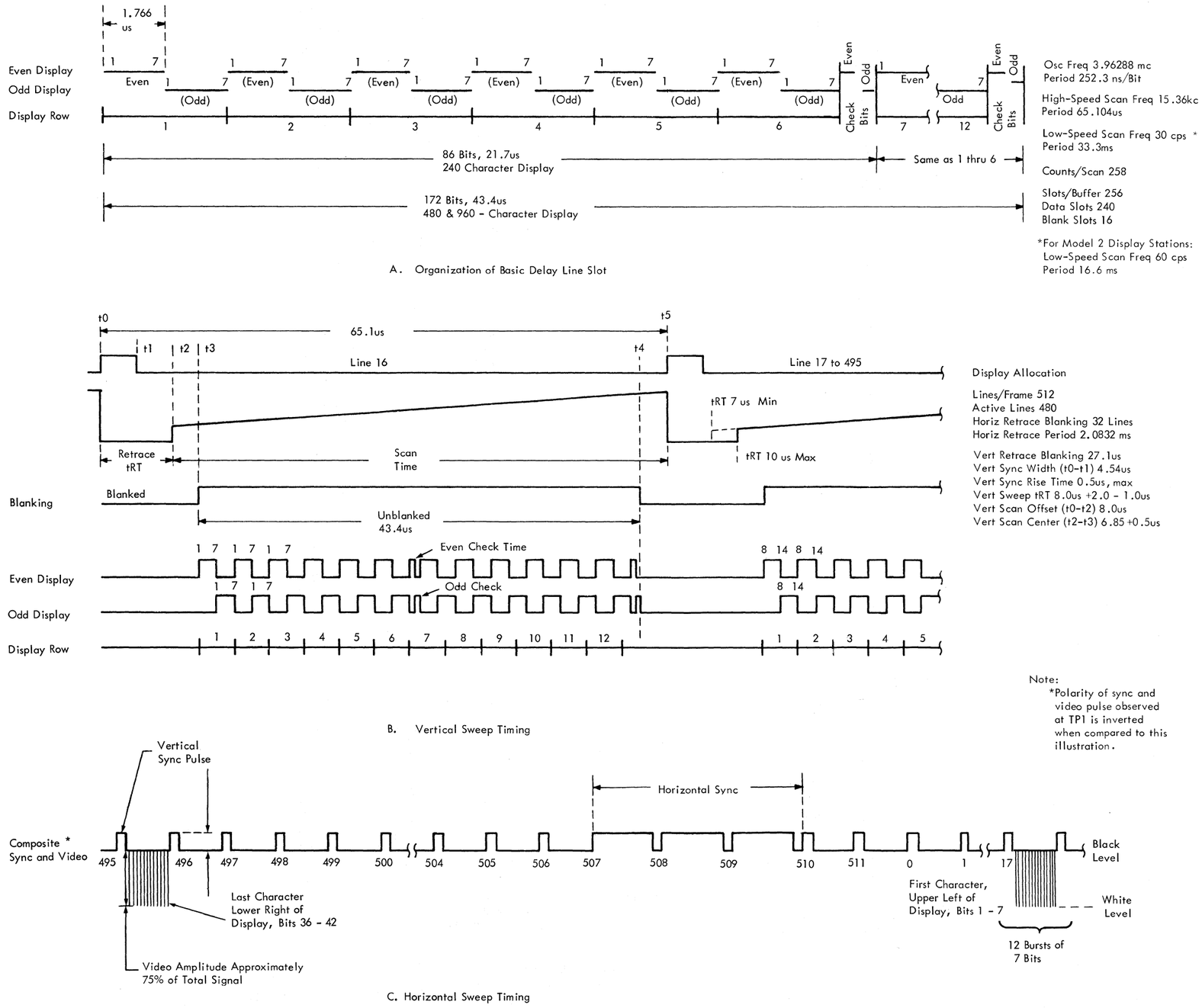
A. Organization of Basic Delay Line Slot

B. Vertical Sweep Timing



C. Horizontal Sweep Timing

Figure 2-9. Display Station Timing



A. Organization of Basic Delay Line Slot

B. Vertical Sweep Timing

C. Horizontal Sweep Timing

Note:
*Polarity of sync and video pulse observed at TP1 is inverted when compared to this illustration.

●Figure 2-9. Display Station Timing

is present. When six data rows have been displayed on both an even and an odd display station, two additional bit periods are counted to allow time to parity-check both display stations. Parity check and assignment are performed only on the BCD data slots, although the two check bit periods are also counted during video slot readouts. Binary-coded data information is never displayed.

Vertical Sweep Timing

The vertical sweep timing required to generate the 512 vertical sweep lines is shown in Figure 2-9, B. Video information and spacing between characters are read out and displayed during 480 lines, and the remaining 32 lines are used to synchronize and retrace the horizontal sweep. The 32 retrace lines are divided equally at the beginning and at the end of the frame. Information readout is initiated when line 16 is scanned and is terminated on line 496. The electron beam then retraces to the upper-left portion of the screen, and data display is reinitiated when line 16 is again scanned. Two slots are displayed within the time period (t2 to t5) of one scan. Upper and lower extremities (t2 to t3 and t4 to t5) of the scan time are not used to display data on the CRT since the vertical scan may be nonlinear in these regions due to circulating currents present in the deflection coils when the field collapses during retrace time. Vertical sync pulses recur every 65.1 μs to abruptly terminate the vertical scan and allow the beam to retrace to the top of the screen. Because the termination of scan time is controlled by the positive transition of the vertical sync pulse, the leading edge (rise time) of the transition must be as sharp as possible and should not exceed 0.2 μs.

Horizontal Sweep Timing

The horizontal sweep timing (Figure 2-9, C) controls the electron beam along the horizontal axis during the time that data is presented on the CRT and, also, during the retrace period in which the beam is returned to the left side of the screen. As the beam is deflected vertically, it is influenced by the horizontal sweep circuits to form a raster of 512 lines. The time required to generate a complete raster (frame) is 33.3 ms, which is related to the low-speed scan frequency of 30 cps. Information is displayed on the CRT during the 480 active lines of each frame. The elapsed time necessary to generate the remaining 32 lines is used to retrace the electron beam to the left side of the screen. Information cannot be displayed while the beam retraces since the CRT is blanked for this period (2.0832 ms). Because the horizontal sweep tends to be nonlinear at its extremities, the 32 retrace lines are subdivided equally at the beginning and at the end of the sweep, thus apportioning the 480 active lines into the central region of the frame where the sweep is linear. Note (in the figure) that the last active line in which data is displayed occurs when the line counter equals 495. Vertical sync pulses continually synchronize the vertical multivibrator from line 496 to 506. The horizontal sync pulses generated during line counts of 507, 508, and 509 are added to the ramp voltage generated by the horizontal multivibrator, causing it to shift conduction to discharge its associated RC time constant and, thus, retracing the electron beam to the left side of the screen. Both the vertical and horizontal multivibrators are free-running; therefore, the raster is continually generated.

Synchronization of the vertical sweep is maintained during the horizontal sync period (507-509) by the serrations in the horizontal sync pulse. The serrations recur at the same frequency as the vertical sync pulses (65.1 μs); hence, the differentiating action of C17 provides the same time reference during horizontal retrace.

Manual Input Keyboard

- Permits manual input entry to display control by operating staff.
- Converts a manual key depression into a 7-bit code.
- Keyboard interlocks so that an operator can depress only one key at a time, with the exception of the Erase Display key.
- When a key is depressed, it remains depressed until display control accepts the character.
- Two types of keyboards are available, numeric and alphanumeric.

Additional entries and changes and certain control functions (such as print, erase, etc.) can be initiated through the manual input keyboard. Two keyboards are available, numeric and alphanumeric. Operation of the numeric keyboard is exactly the same as that of the alphanumeric keyboard, both mechanically and electrically, except that its electrical output combinations are limited to numeric, special symbols, and control functions. The theory of operation of the more comprehensive alphanumeric keyboard will be treated in detail. The information provided is also applicable to the numeric keyboard.

Description

The alphanumeric keyboard resembles a regular typewriter keyboard in appearance and key layout. Operation of the mechanical portion is the same as that of the keypunch keyboard. The alphanumeric keyboard contains the 26 letters of the English alphabet, Arabic numerals 0-9, special symbol keys, and the control keys required to format and enter an input message. The numeric keyboard contains Arabic numerals 0-9, upper-case special symbols, and the same set of control keys as provided for the alphanumeric keyboard. When a key is depressed, a series of contacts are closed in a particular configuration representing the code for the depressed key. The 7-bit code for the selected character is transferred to the control unit along with a strobe signal which informs display control that data has been placed on the lines. When display control accepts the character, it acknowledges receipt of the data by responding with a Restore signal to release the selected key, thus unlocking the keyboard. Another character can now be entered simply by depressing the required key.

Keyboard Mechanics

Figure 2-10 illustrates the alphanumeric keyboard (bottom and rear views). The key components unit contains all the keys. These keys operate the seven left bail contacts when the keyboard is in upshift or the seven right bail contacts when the keyboard is in downshift. The two shift keys do not activate the bail contacts when they are depressed. Instead, they operate keystem contacts associated with each shift key and the shift relays.

Figure 2-11 is a simplified drawing showing one latch pull bar, one bellcrank, one latch, and one permutation bar. All keys except the shift keys, which are associated with keystem contacts, operate a latch pull bar through a keystem bellcrank. The key button rubber bumper, a rubber washer under the key button, is associated with the keystem. The amount of downward travel on the key when it is depressed is partly determined by the thickness of the rubber bumper. As a key is depressed, the bellcrank pivots and moves the latch pull bar toward the keystem. The hooked portion of the latch pull bar rests in a notch at the top of the latch. Each latch pull bar operates a latch. When a keystem moves downward, the latch pull bar pulls the latch off the latch bar. Near the end of the operation, the keystem is restored to its initial position by the action of the latch pull bar reed spring.

When a key is depressed, the mechanical operation is as follows (Figures 2-11, 2-12, and 2-13):

1. The keystem bellcrank moves its latch pull bar forward.
2. The latch assembly drops off the latch bar.
3. Individual keystem springs restore the keys and the pull bars to normal.
4. A separate flat spring holds each pull bar against its latch assembly and makes sure it relatches in the notch in the latch.

Note in Figure 2-13 that the latch assembly has three parts that, although attached by a rivet, are free to pivot on the rivet. Each part has its own function.

The permutation bar, contained in the permutation unit of the keyboard, supports the operating spring and pivots the contact bails to close the bail contacts. The latch pivots on the permutation bar. The latch pull bar reed spring is shown in Figure 2-13. The latch pull bar has a 90-degree hook formed at its end (Figure 2-12). The hooked end of the pull bar rests in a notch that is cut into the top of the latch (inset, Figure 2-17) and is held there by the U-shaped reed spring.

Permutation means transformation or change in groupings. In the keyboard, operation of the bail contacts is under control of the permutation bars. The latch hooks over the latch bar and holds the latch assembly and its permutation bar inoperative until a key is depressed. The key unit facilitates selection of individual characters and, after selection, operates a permutation bar. The permutation bar transfers the bail contact(s) that represents the selected key.

The permutation bar is spring-operated and held restored by the latch. The latch bar is not a moving part. When the latch is hooked onto the latch bar, the permutation bar is held restored. When the latch is pulled off the latch bar, the permutation bar is operated downward by the force of its spring. The function of the permutation bar requires it to move; the movement is guided by the upper front guide rail and the latch stop plate at the bottom.

Bail Contacts: The contact bail is pivoted by a tab attached to it and resting in a notch that is cut in the rear (as viewed in Figure 2-11) edge of a permutation bar. A permutation bar has 15 notches cut in its edge for operating any of the possible 15 contact bails. Seven contact bails are located on the left side of the keyboard; another seven are on the right side. Selected bail contacts on the left or right or on both sides can be activated by the permutation bar. Upshift contacts (left contacts) are selected for readout when the shift relays are energized. One bail contact (strobe), located with the right bail contacts, is always selected whenever a key is depressed. The strobe contacts inform display control

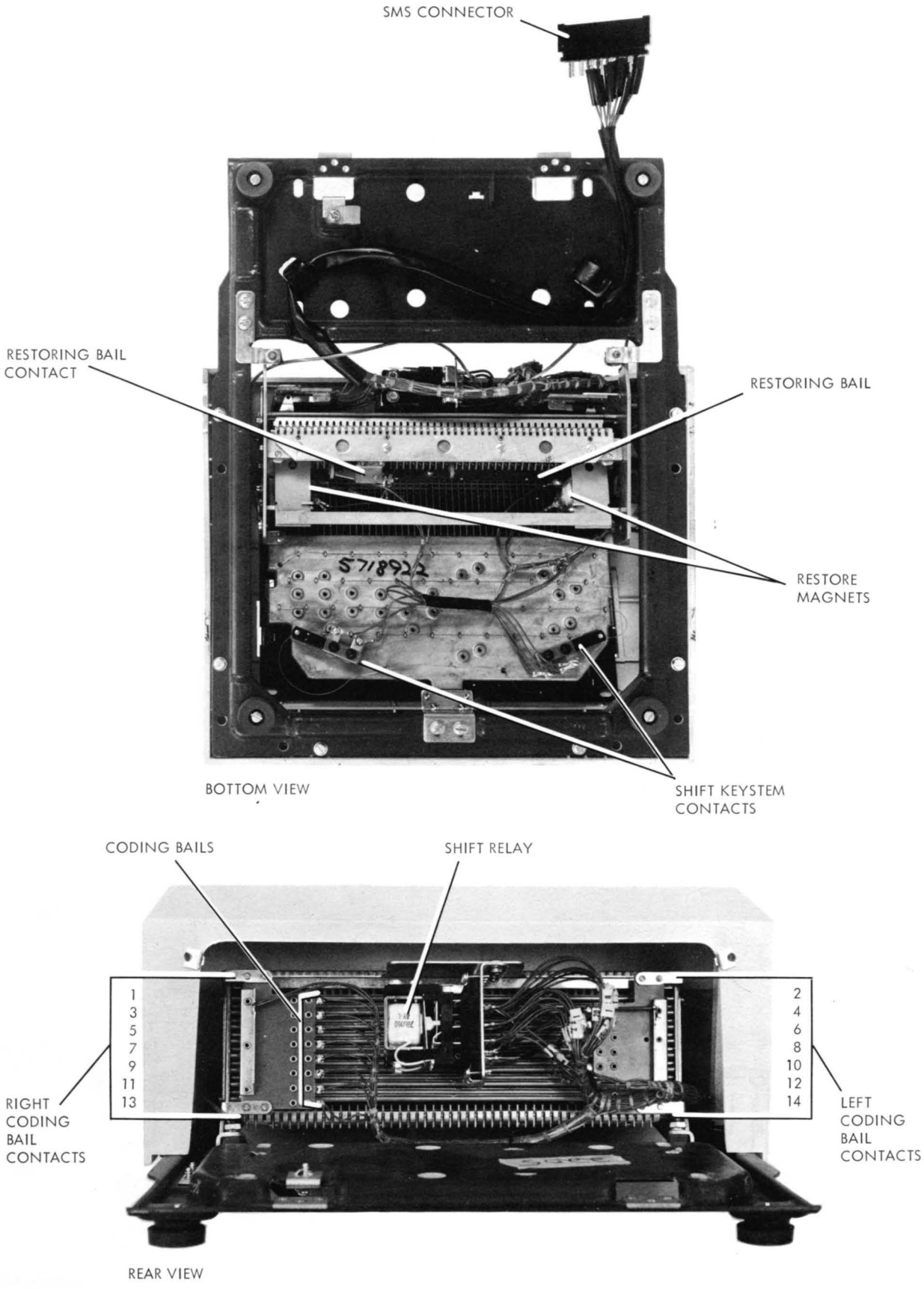


Figure 2-10. Alphanumeric Keyboard, Bottom and Rear Views

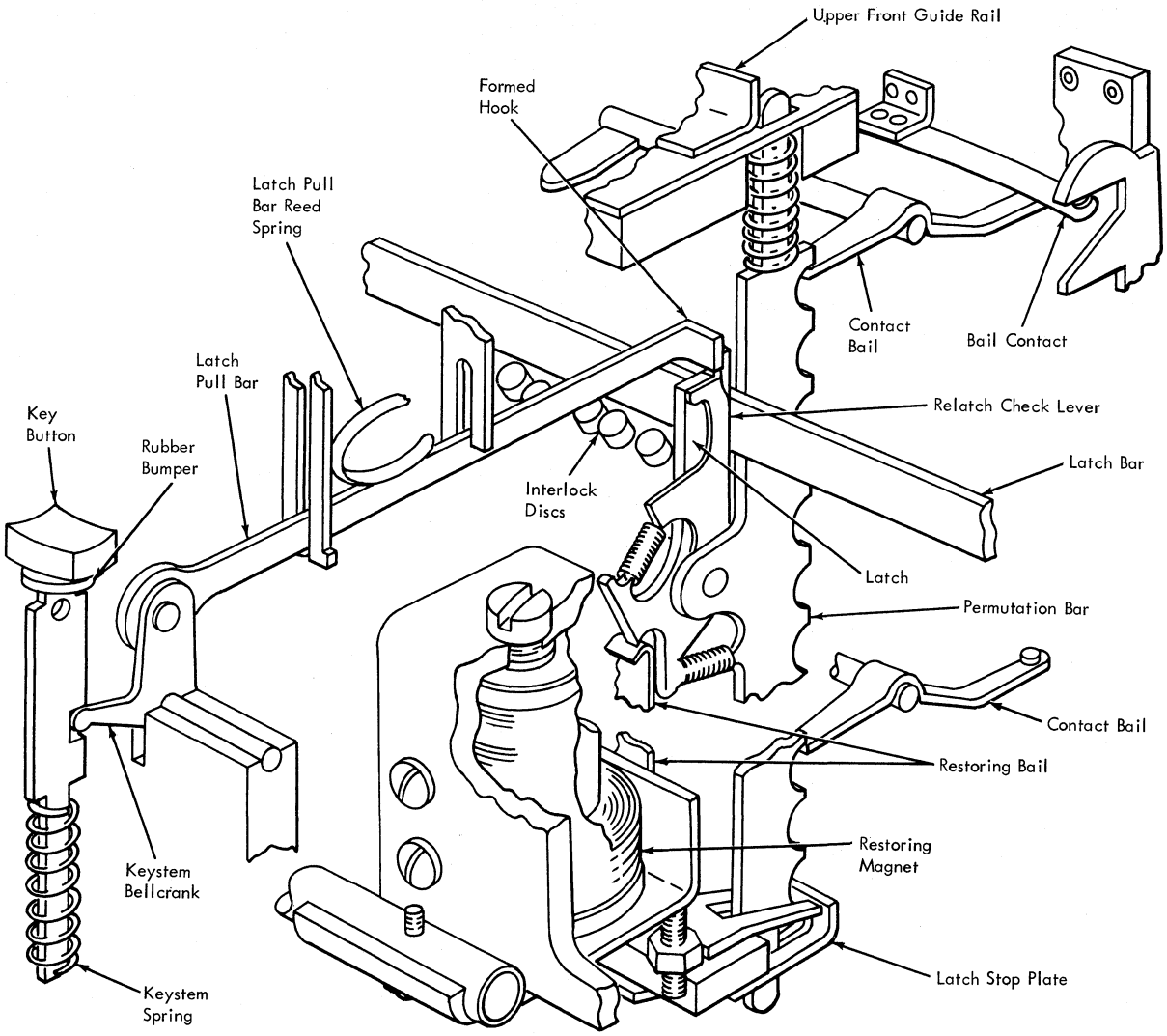


Figure 2-11. Key Position

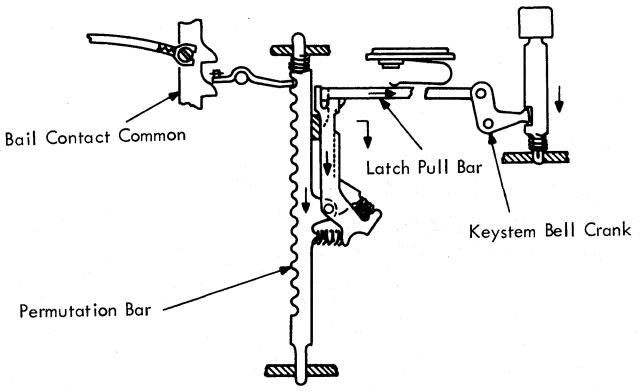


Figure 2-12. Permutation Bar and Keyboard Latch (Normal)

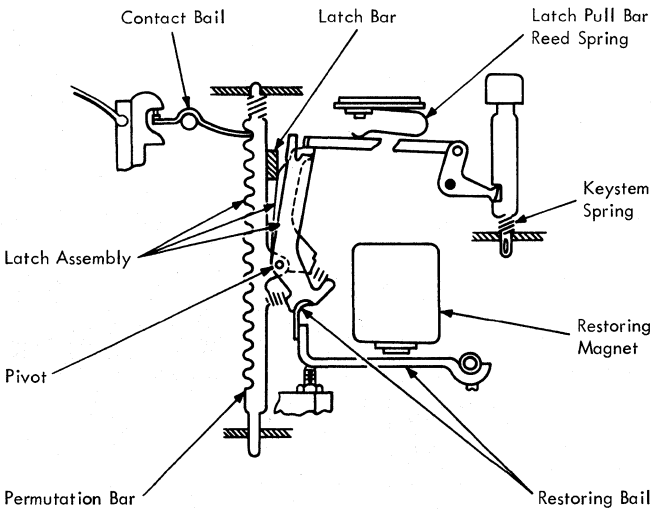


Figure 2-13. Permutation Bar and Keyboard Latch (Tripped)

that the keyboard has entered data on the lines and requests service. The chart in Figure 2-14 identifies the keystem numbering of both the numeric and alphanumeric keyboards. Depressing any key causes one or more bail contacts to transfer to display control. The bail contacts are directly related to the bit configuration for the selected character. The relationship is illustrated in Figures 2-15 and 2-16 for the alphanumeric and numeric keyboards. Each of the figures details the bail contact selections corresponding to each keystem number (key). A different configuration of bail contacts is selected (closed) for every keystem except the shift key. The strobe contact becomes active every time a key is depressed (except the shift key). Bail contacts 2 through 7 are employed to configure the 6-bit binary code for the depressed key. Contact 1 is used, in addition to contacts 2 through 7, whenever a function key is depressed. The output derived from contact 1 informs display control that a command rather than data has been issued by the keyboard.

Interpretation of the keystem and bail selection can be more readily understood by selecting a particular keystem number and itemizing the bail contacts that are selected when the keystem is depressed. Assume that the "P" key is depressed on the keyboard (Figure 2-15). The keystem number corresponding to character "P" is 40. Line 40 is traced upward, and the circled junction points are noted in the grid of Figure 2-15. Bail contacts 2 and 4 for lower case are selected because the "P" key is a lower-case character. The binary code for the "P" character is therefore 0101000. Upper-case characters activate the upper-case bail contacts. Note that the strobe contact was also activated when keystem 40 was depressed. The physical location of

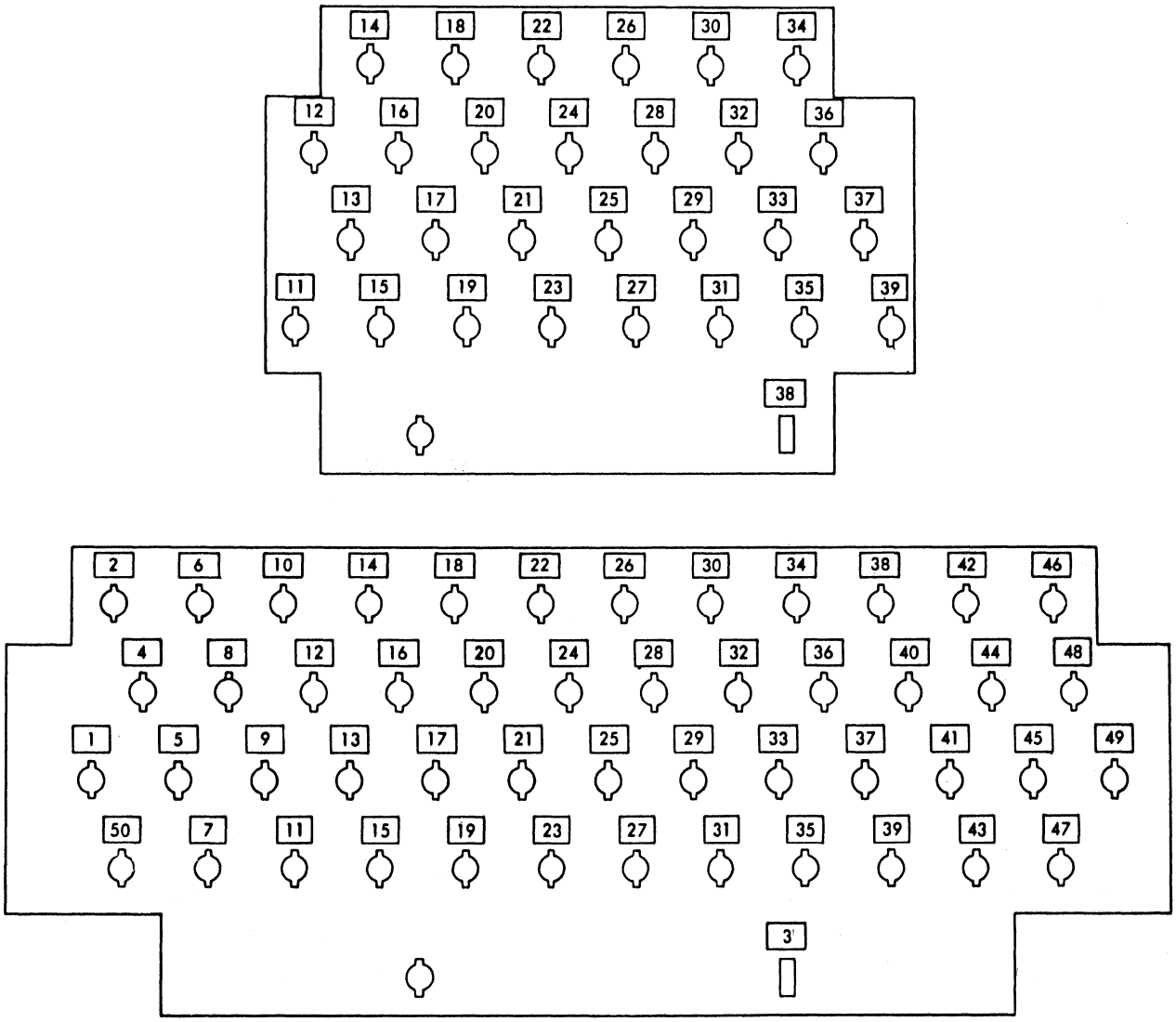


Figure 2-14. Keystem Numbering Chart

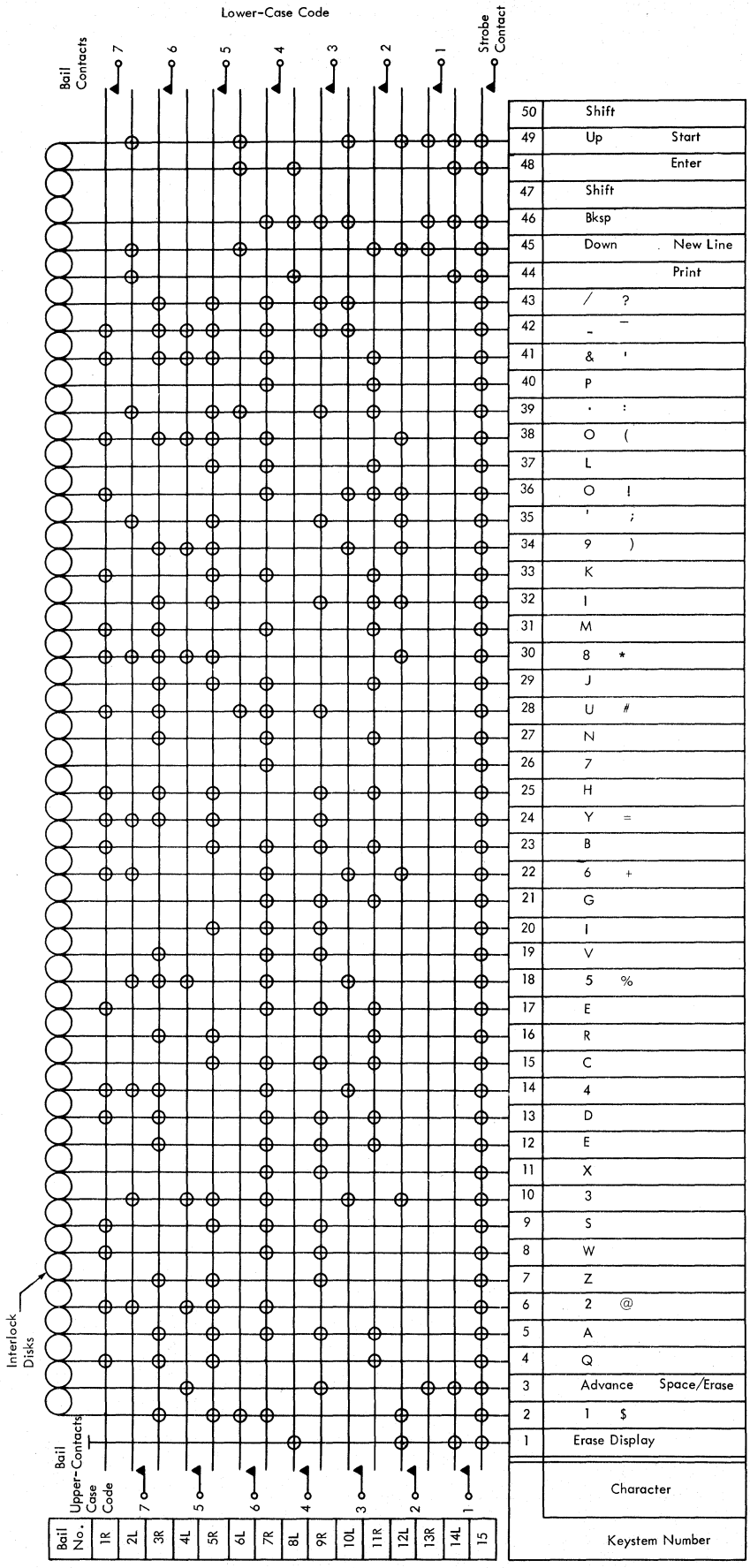


Figure 2-15. Keystem Number and Bail Selection For Alphanumeric Keyboard

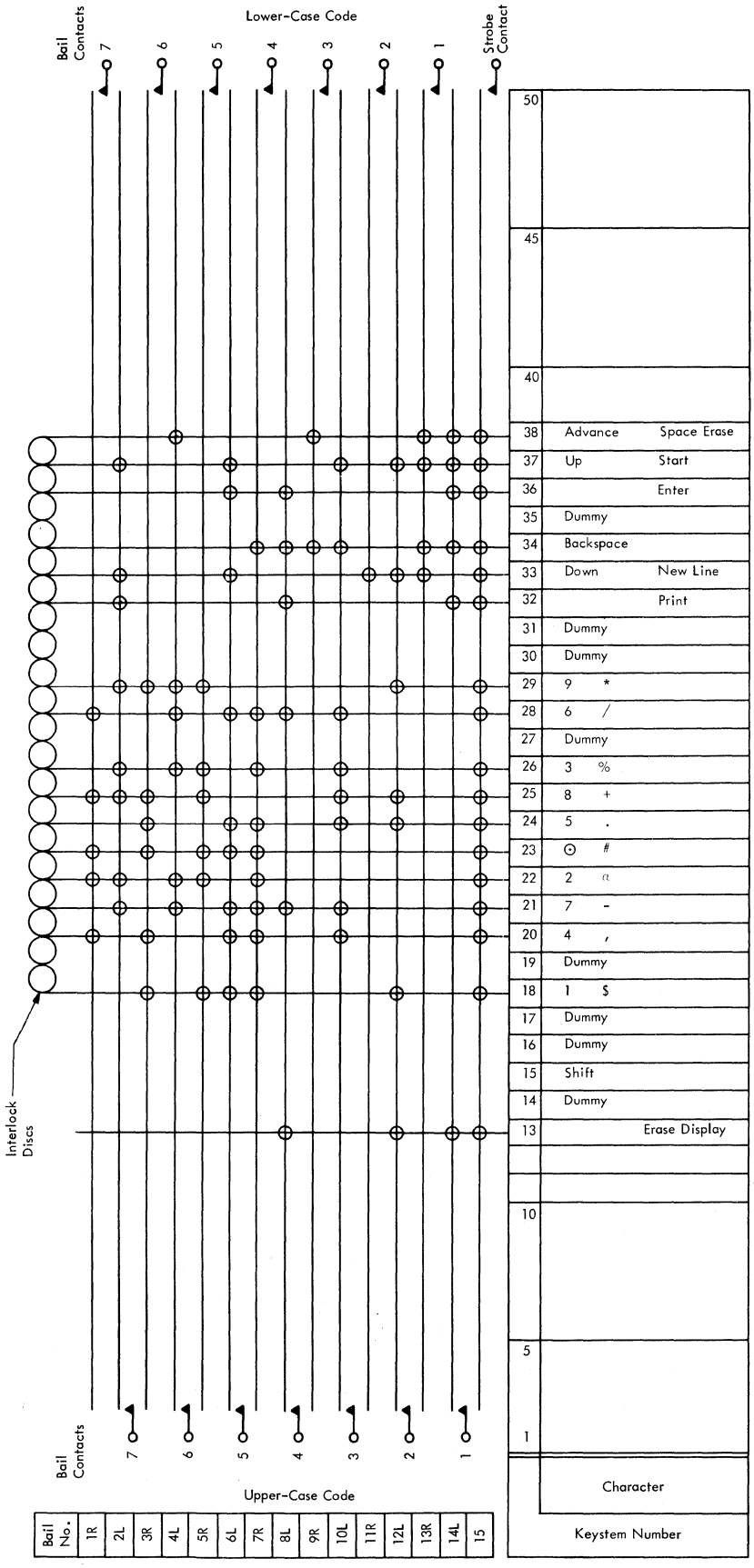


Figure 2-16. Keystem Number and Bail Selection For Numeric Keyboard

each bail in the keyboard is shown under the heading "Bail No.". The R and L designations in the listing indicate that the bail contacts, which are associated with their respective bails, are located on the right or left bail assembly (as viewed from the front of the keyboard).

The numeric keyboard operates in the same manner as the alphanumeric keyboard; however, fewer keystems are employed with the numeric keyboard. Keystems not used are either labeled "dummy" or are left blank. Bail contact selections for the numeric keyboard keys are given in Figure 2-16.

Keystem Contacts: Two keystem contact switches, located on the bottom of the key components unit, are associated with the left and right shift keys. Both switches are parallel-connected and are activated whenever one of the shift keys is depressed. Depressing either shift key permits the upshift left bail contacts to be transferred to display control. Open circuit keystem switch contacts (shift key not depressed) allow the downshift right bail contacts to transfer to display control.

Keyboard Restoring Components: When the keyboard restoring magnets are energized, the restoring bail restores the latch to the latch bar. Figure 2-17 shows the latch and relatch check levers in two different positions. The large overall drawing shows the latch on the latch bar (restored), and the inset view shows the latch off the latch bar (tripped). The latch and relatch check levers pivot on a stud on the permutation bar. The latch is held on the latch bar by the

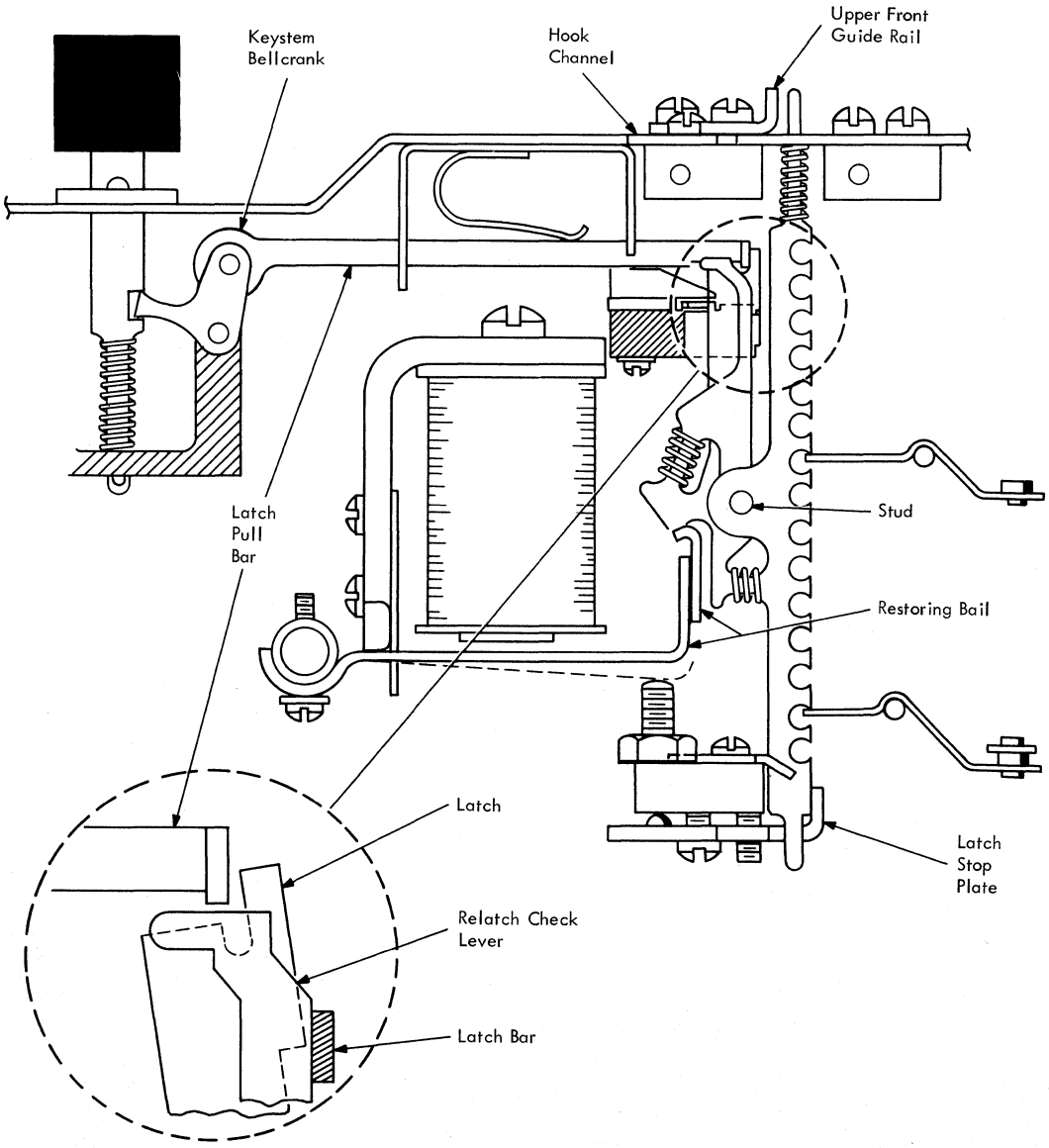


Figure 2-17. Key Position (Latched and Tripped)

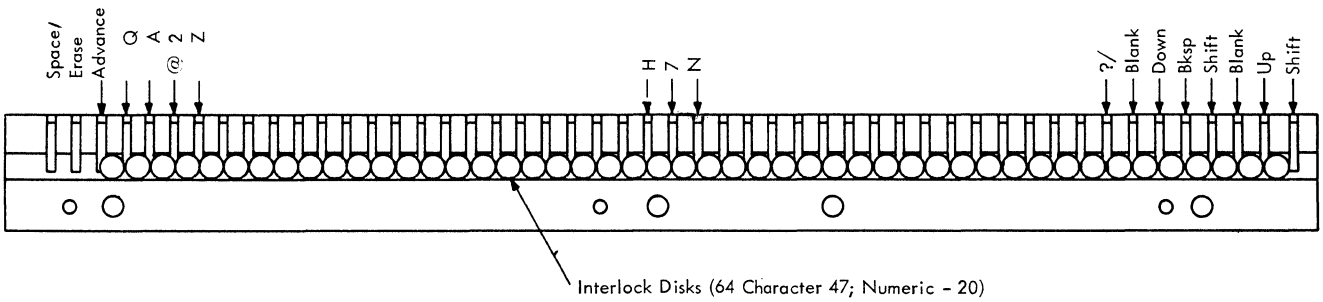


Figure 2-18. Interlock Disks

force of its spring. The relatch check lever is operated by its spring.

The machine operation is faster than the operator's finger movement on the keys. If the pull bar did not disengage from the latch as the latch was pulled off the latch bar, more than one transfer of the selected character would occur each time a key was depressed.

When the latch is pulled off the latch bar (Figure 2-17, inset), the relatch check lever pivots toward the latch bar due to the spring tension that exists between the check lever and the latch. The pull bar disengaged from the latch because it cannot follow it downward. The pull bar cannot re-engage in the slot in the latch until the latch and pull bar have been restored. A key can be depressed and held while the latch is pulled off the latch bar and restored to it. The pull bar will re-engage in the latch only if the key is restored. When a latch is pulled off the latch bar, the pull bar engaging slot is covered by the relatch check lever.

The permutation bar, along with the latch, is restored by the latch-restoring bail. Energizing the restoring magnets operates the restoring bail, which is attached to the armatures of the keyboard restoring magnets. In every keyboard, two restoring magnets restore the latch to the latch bar. For correct keyboard operation, only one latch at a time can be pulled off the latch bar (with the exception of the erase key); this prevents the operation of more than one key at a time.

Keyboard Interlocks: Figure 2-18 shows the interlock disks in the trough that contains them. The permutation bars and their latch assemblies are positioned side by side and equidistant. The interlock disks are located between each latch. The disks are placed side by side in the trough, and the line of disks spans the row of latches. Any time two disks are separated, all the disks will be moved.

Figure 2-19 shows five interlock disks with latch "B" first between two of them. When a latch is forced between two disks, the disks to the right and to the left of it will move. As shown in the figure, a key was depressed and latch "B" was pulled off the latch bar. Before latch "B" could be restored, the operator pressed the key for latch "D". Latch "D" cannot be pulled off the latch bar until latch "B" is restored.

When a latch is operated and the disks are separated, all the other latches are inoperative because the interlock disks cannot be spread apart any farther. When a key is depressed, the latch must be restored before another key can be depressed.

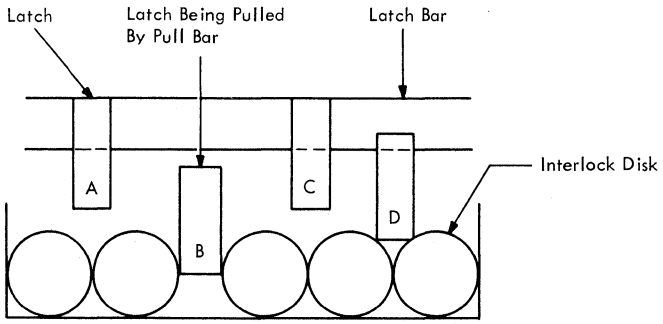
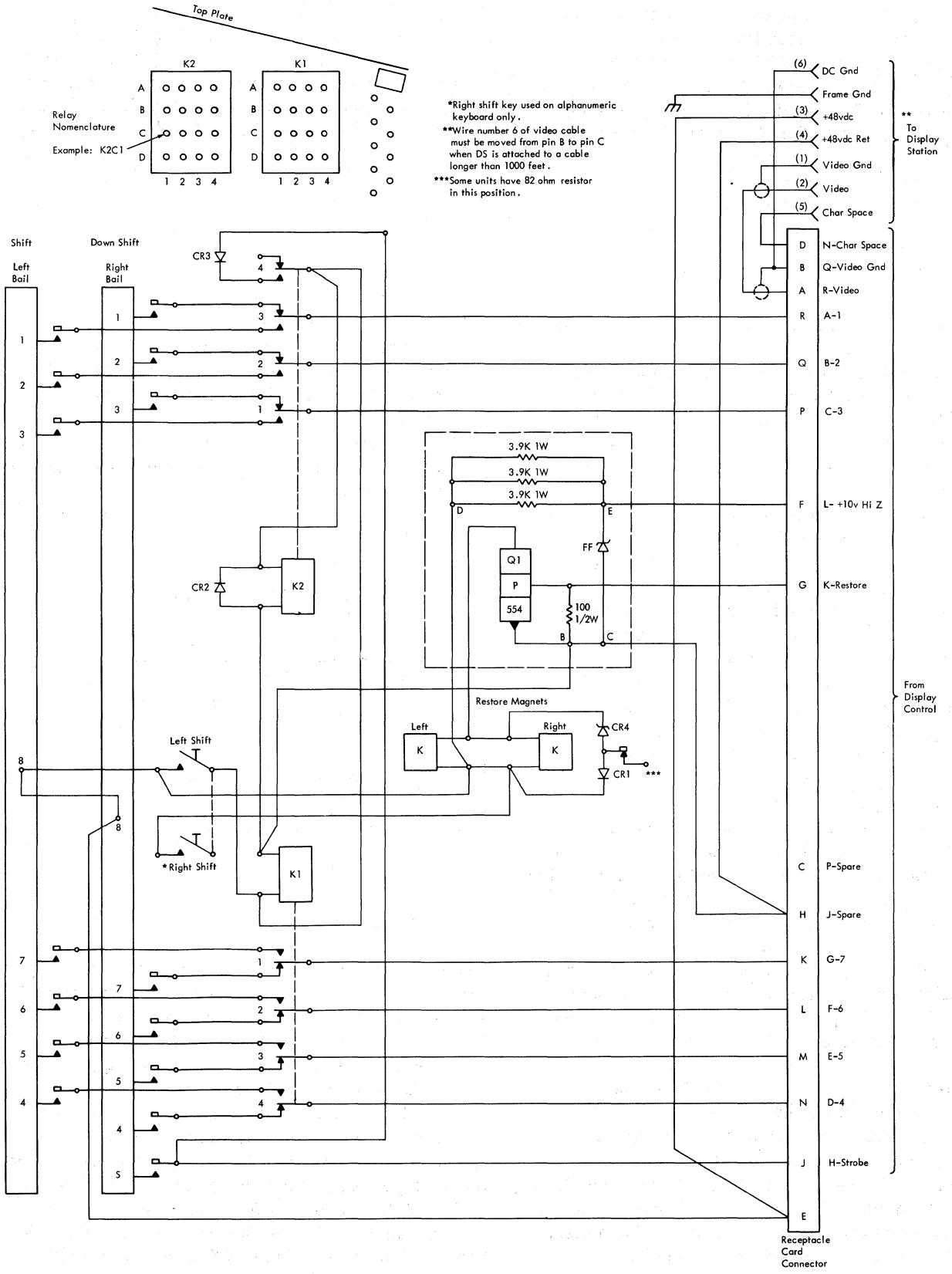


Figure 2-19. Interlock Disks (Partial)

Keyboard Electronics

The keyboard electronic circuits (Figure 2-20) generate a 7-bit code or command, depending upon the key depressed by the operator, and transfer the code to display control for service. Whenever a key is depressed, the permutation bar closes appropriate bail contacts 1 to 7 in the bit configuration representing the depressed key. Right bail contacts are active for downshift characters; left bail contacts, for upshift characters. The strobe contacts located on the right bail are special contacts that close for both upshift and downshift keys. The strobe level informs display control that data or a command has been placed on the lines and that service is requested. Bail contacts are closed when selected, transferring +48vdc to corresponding pins on the paddle card connector. Upshift bail contacts are transferred to the paddle card connector because shift relays K1 and



•Figure 2-20. Keyboard Electronics

K2 are energized when the shift key is depressed. If the shift key is depressed together with a data key, upshift relays K1 and K2 remain selected even though the shift key is released. In this case, shift relays K1 and K2 remain energized by the strobe 48v supply through the upper holding contacts of K2. The data key, however, remains locked until display control accepts the bit configuration that represents the selected character. Then, the keyboard is restored. The restore level is received by the keyboard on pin G, turns on transistor Q1, and energizes both the left and right restore magnets. The restore magnets de-energize shift relays K1 and K2 and open-circuit all bail contacts and the strobe contact (contact 8). Keyboard data transfer timing is shown in Figure 2-21. Diodes CR1-4 reduce the effects of noise and contact chatter when the keyboard restores upon termination of a data transfer.

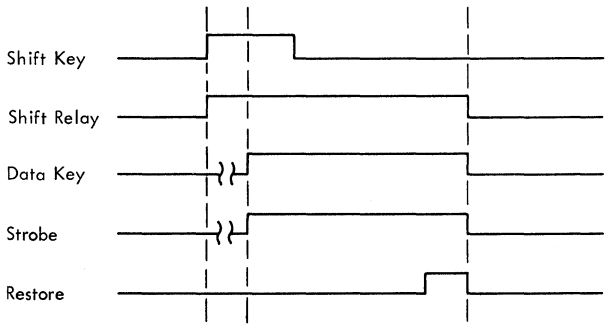


Figure 2-21. Keyboard Data Transfer Timing

IBM 2848 DISPLAY CONTROL

- Command and data inputs are received as six-bit bytes via the character register of the optional channel adapter.
- Address information is received as a five-bit byte from the channel adapter address register.
- Data and control information is transferred to the channel via the character register of the channel adapter.
- The address register of the channel adapter can be set with a five-bit address originating from the display control address register to identify the originating keyboard during Enter commands.
- Display control provides a seven-bit tilt-rotate code as an output to the 1053 Printer adapter.
- Accommodates up to 24 2260 Display Stations (2848 Model 1) and one 1053 Printer adapter.

The 2848 Display Control contains the control circuitry that is shared by the interface, printer adapter, and display stations (keyboards) to effect the various display capabilities. The major logical elements of display control are illustrated in block diagram form in Figure 2-22. Note that all communication with the System/360 channel is accomplished through the character register and address registers of the optional channel adapter. System/360 can, using the channel adapter as the connecting link, configure the common display control circuits to permit channel operation with any 2260 Display Station associated with the display control or with the 1053 Printer via the optional printer adapter.

The display control circuits can also be controlled by any associated display station provided with a keyboard. Then, display control permits data entry into, or modification of, the display data stored in the display station adapter. Display control also causes input messages to be sent to the System/360 channel via the channel adapter when this action is initiated at a display station keyboard (Enter command).

The major logical areas of display control have the following functions:

1. Common Buffer: This seven-bit latch register serves as the hub for all data and control word transfers.
2. Data Decode: Senses contents of common buffer register for SOM, NL, and EOM codes, except during Read Buffer commands.
3. Set EOM: Provides a means of setting the six-bit EOM code in the common buffer register when required by the operation being performed.
4. Character Generator and Code Translator: Converts the six-bit character code set in the common buffer register from either the channel (via channel adapter) or the keyboards into five seven-bit bytes that are stored in the delay lines and used to generate video for character display. Also performs code translations, e.g., six-bit character code to 1053 tilt-rotate code.
5. Serializer: Converts the contents of the common buffer register into serial data that can be written in the delay lines of the selected adapter.
6. Parity Assign: Assigns even parity to groups of data (slots) stored in the delay lines.
7. Parity Check: Checks for even parity as BCD data is read from the delay lines of the selected adapter for ultimate transfer to another location.
8. Address Encoder: Encodes a five-bit address used to select a display and to identify the active keyboard.

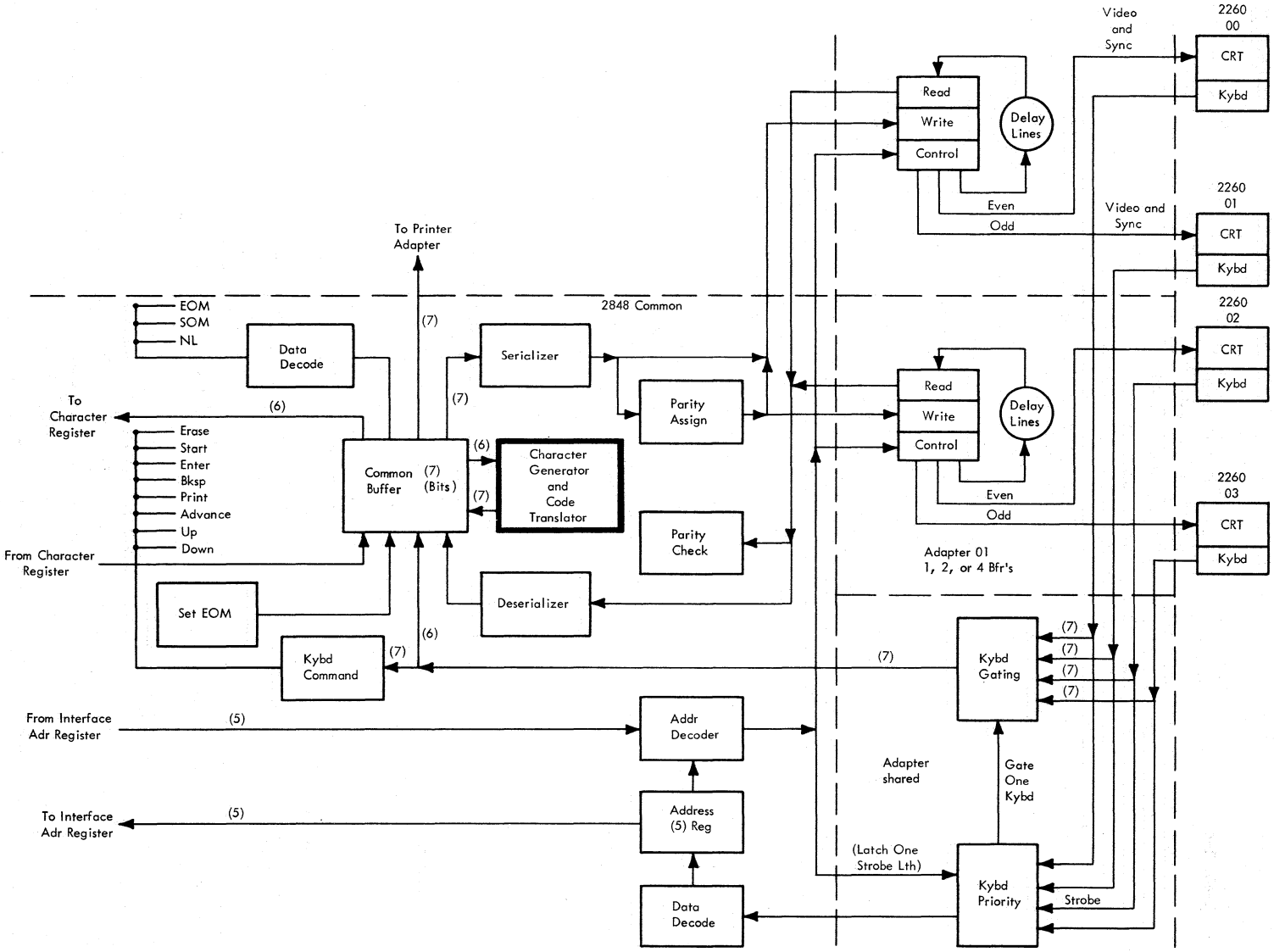


Figure 2-22. Display Control, Simplified Block Diagram

9. Address Register: This five-bit latch register is set from the address encoder (keyboard operation); also used to set address of originating keyboard in the channel adapter address register during keyboard Enter commands.
10. Address Decoder: Decodes the five-bit address to select a particular display station.
11. Keyboard Priority: Determines which keyboard is serviced when more than one keyboard requests control of display control common.
12. Keyboard Gating: Accepts inputs from all associated keyboards on common bus; however, only the outputs of the selected keyboard are gated through to keyboard command register.
13. Keyboard Command: Decodes keyboard command bytes and sets the command latch associated with the command.

The functions of the logic areas within the adapters illustrated as part of display control in Figure 2-22 are as follows:

1. Delay Lines: Provide a storage medium for display data; provide video outputs to associated display station; provide six-bit BCD character codes during read operations.
2. Read Control: Controls the extraction of data from the delay lines.
3. Write Control: Controls the entry of data into the delay lines.

In the paragraphs that follow, the operation of each area of display control is described in detail, including the operation of areas comprising the display adapters as shown in Figure 2-22.

Display Adapter

A maximum of four display adapters can be supplied with the IBM 2848 Display Control (Model 3). Each adapter contains eight delay lines plus other control circuits for the keyboards and nondestructive cursor feature. The delay lines store video information for presentation on an even and odd display station. Binary-coded data information is also stored in the delay lines; however, this data is not displayed on the CRT. The eight delay lines are paired into four groups called "buffers". Each of the four buffers stores information that will ultimately be displayed on their associated even and odd display station. Buffer 1, consisting of two delay lines, contains information that will be displayed in the upper-left quadrant for the even and odd display station. Similarly, buffers 2, 3, and 4 contain information that will be displayed in the lower-left, upper-right, and lower-right quadrants, respectively. Data entry into or exit out of the delay lines is controlled by control circuits physically located within the adapter. Other gating circuits are employed to transfer information (BCD or video) to the common buffer register (BCD only) or a display station (video only). Data readout from the delay line is destructive; therefore, when readout occurs it must be regenerated if the presentation on the CRT viewing screen is to be retained. This regeneration feature is automatic unless display control erases or changes the information before it is regenerated.

Delay Line Theory

- A delay line utilizes the qualities of magnetostriction to propagate digitized information along the line providing temporary storage.
- Storage of digitized information in a delay line is dynamic rather than static and must be regenerated when bits reach the end of the line.
- A mechanical force is applied to the delay line in such a manner as to provide torsional stress waves, creating a disturbance in the line.

Description: Magnetostrictive devices are constructed of wire or tape; however, wire is used more extensively. When a magnetic field is applied to magnetostrictive material, it either expands or contracts, producing mechanical stress waves in the delay line. Stress waves are created by a drive transducer representing digitized information in a nonreturn to zero (NRZ) mode. Storage of this type is dynamic rather than static; therefore, information must be regenerated as it emanates from the end of the line. The NRZ mode permits greater bit density in the delay line over the RZ mode. Storage capacity of a delay line is a function of the path length, wave velocity, and the pulse repetition rate. Delay line rates of several milliseconds can be packaged in a compact form by coiling the wire within the module shown in Figure 2-23.

Operation: The delay line module uses a nonreturn to zero (NRZ) mode of operation. Figure 2-24 illustrates the basic units within the delay line module. Figure 2-25 illustrates timing relationships and idealized waveforms associated with the delay line module operation in the control unit. The waveforms illustrated in Figure 2-25 are keyed to various input and output points in Figure 2-24 by letter designations A through K.

The input driver is a latching driver. A latching driver is required to ensure that only transitions from a 1 to a 0 or from a 0 to a 1 cause an acoustic wave on the magnetostrictive wire. An acoustic

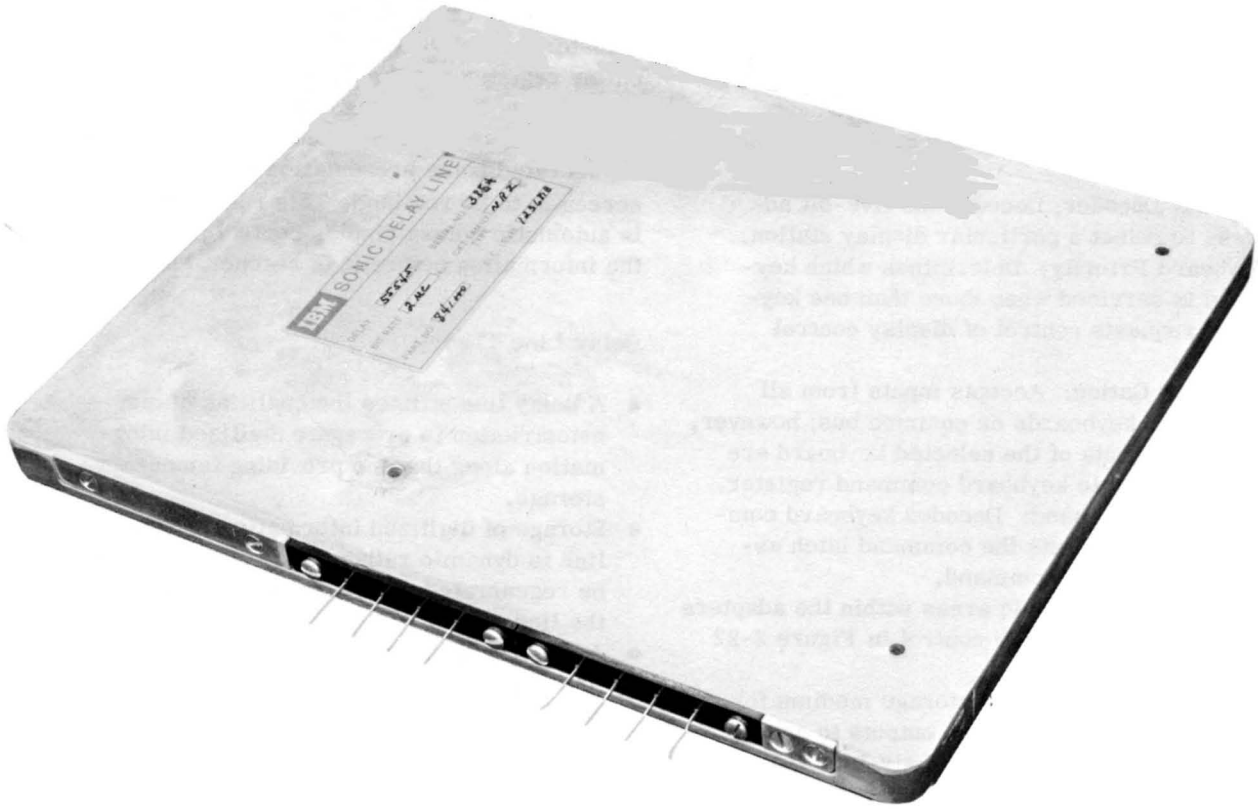


Figure 2-23. Delay Line Module

wave is caused by twisting the wire, which is accomplished by changing the current through the input transducer. The direction of the twist depends upon whether the latching driver is changed from a 0 to a 1 or from a 1 to a 0. The output transducer senses the acoustic wave on the magnetostrictive wire. The polarity of this output signal depends upon the direction of the twist introduced by the input transducer.

The sense amplifier amplifies the output from the output transducer. The amplified bipolar signal from the sense amplifier drives a transformer. This transformer generates two bipolar signals which are 180 degrees out of phase with each other. Both detectors sense a positive signal. Therefore, the out-of-phase signals ensure that only one detector generates a pulse at any one time. The output pulse from a detector causes the output trigger to assume the required state.

Delay Line Bit Organization: Two delay lines, designated A and B, are used as storage units; together they constitute a buffer. A buffer contains the information that is to be displayed in one quadrant on the CRT for two display stations. Four buffers (eight delay lines) are therefore necessary to display information on the entire screen of a 960-character display. Each delay line is 5.5545 ms in length; that is, a bit introduced by the drive transducer can be detected by the receiver located at the end of the line after an elapsed time of 5.5545 ms. Bit information can be entered serially into the delay every 500 ns (2 mc). Since the display stations require a bit every 250 ns, delay lines A and B are operated together but offset by 250 ns. By interleaving bit information into two delay lines, the resulting operating frequency is increased by a factor of 2. A buffer therefore supplies interleaved bits every 250 ns; a bit from delay A, 250 ns later a bit from delay B, a bit from delay A, etc.

When readout is initiated in buffer 1, bit information (video) is alternately read out from the A and B delay lines. The first seven bits are routed to the even display station, and the second seven bits are routed to the odd display station. Readout continues in this manner until the V1 line shown in Figure 1-8 for the L character has been gated to the odd display station. At this time, the V1 line for six characters on the even and odd display has been completed. Time for parity check or assignment, consisting of two bit periods, occurs at the end of this period. The first bit period allows time for checking or assigning parity to the even display; the second bit period does the same for the odd display. Note, however, that parity is only associated with the BCD information in the delay line although the two bit periods always occur after 12 seven-bit

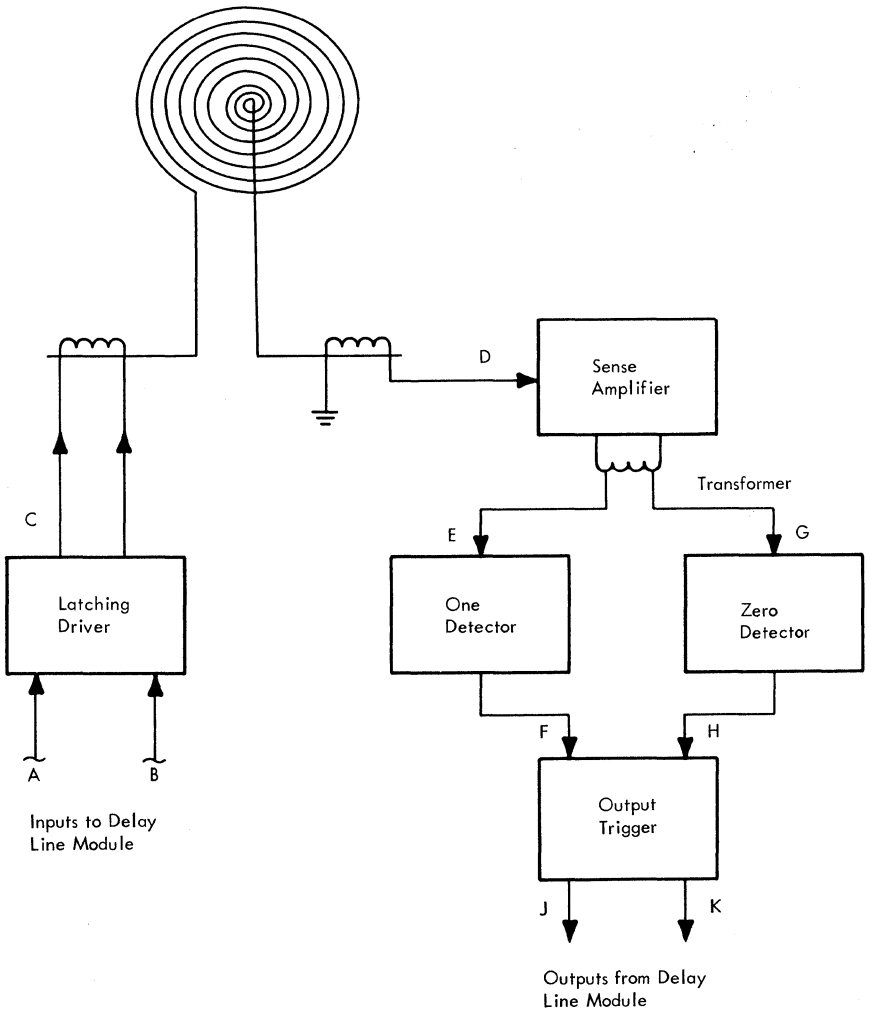


Figure 2-24. Delay Line Module, Simplified Block Diagram

readouts (including those associated with video data). The next seven-bit readout is supplied by buffer 2 (lower-left quadrant of display screen), and readout continues in the manner described for buffer 1. Beginning on line 256, alternate readouts from buffers 3 and 4 supply information for the upper- and lower-right quadrants of the viewing screen.

From the foregoing, note that 86 bits (12 seven-bit readouts plus the two parity check bits) constitute a slot. The time required to display a slot is 21.7 μs. Once the definition of a slot becomes firmly fixed in mind, it becomes apparent that the delay line buffer storage areas can be depicted and discussed on a slot basis. Buffer storage on a slot basis is treated in the following paragraph.

Buffer Slot Layout: Before considering the buffer slot layout, it is advantageous to review the presentation of information on the viewing screen so that a correlation can be made between buffer readout and the CRT display. The vertically oriented raster in the display station consists of 512 vertical sweeps. The 512 vertical sweeps are associated with a corresponding count in the line counter (0-511). Lines 0-15 and 496-511 (32 lines total) are not used since the horizontal retrace returns the electron beam to the upper-left section of the CRT during this time. The remaining 480 lines are employed to display information on the screen. Six vertical lines are required per character (BCD, V1 through V5); thus, 480 lines permit display of 80 characters along the horizontal. BCD data is positioned in the delay lines to permit spacing between characters and is never gated to the display station. Communication (such as a write operation) between the host system, 1053 Printer, and remote interface requires the use of BCD. Further code conversion may be necessary, depending upon the user. For example, the printer operates on a tilt-rotate code; therefore, the BCD

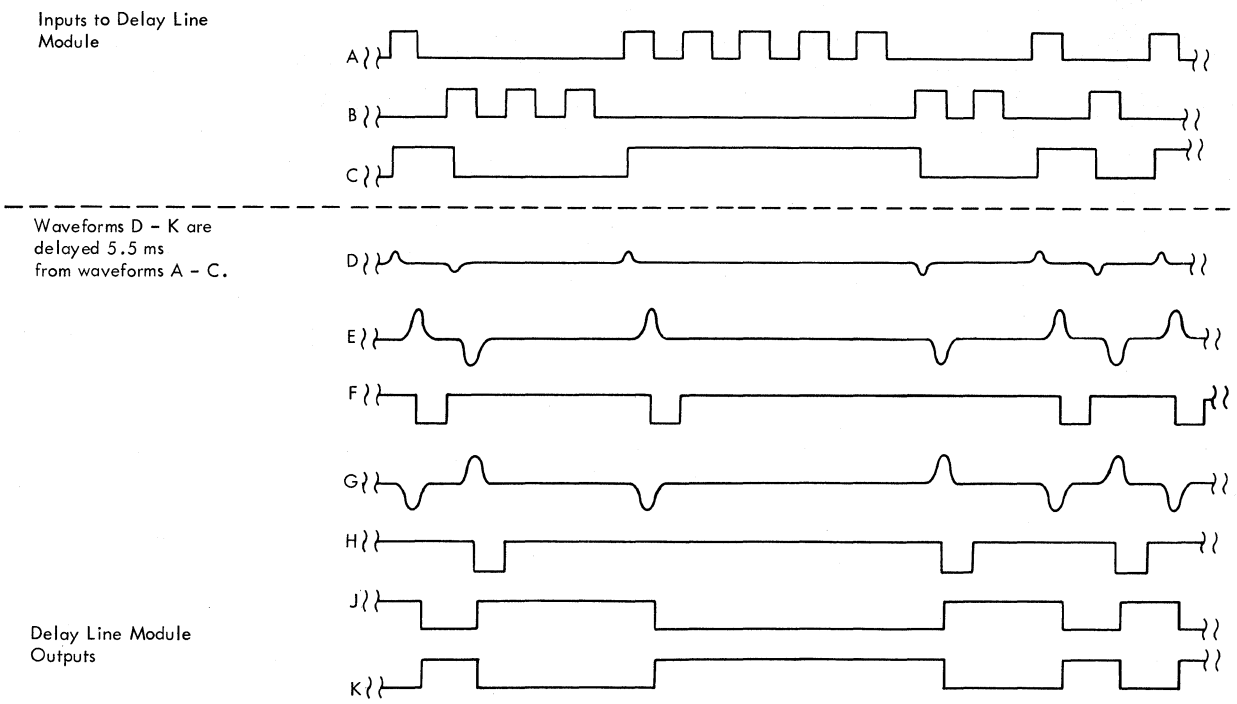


Figure 2-25. Delay Line Timing

must be converted to the tilt-rotate code when a print operation is initiated by the keyboard or the host system.

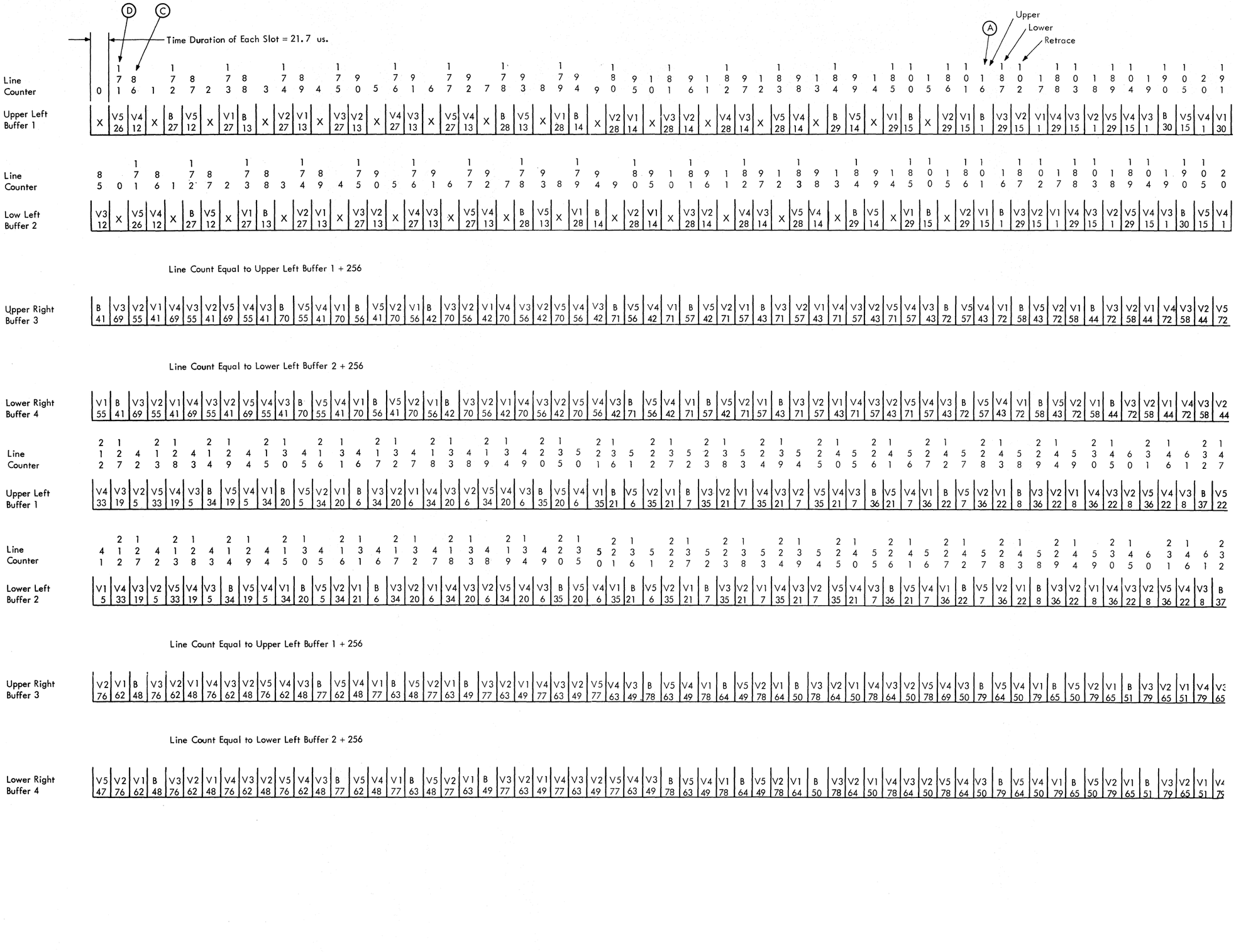
Figure 2-26 shows the slot layout of the four buffers used in a 960-character display. Line counts shown above each slot indicate when their associated slots will be read out from the buffer for display on the CRT. Slots are formatted in the buffers in an interleaved progressive pattern of three. Hence, three passes through the buffer are necessary to read a full buffer. This is because buffer 1 must be read first, followed by buffer 2; then, one slot time is required to return the electron beam to the upper portion of the CRT before buffer 1 can be selected again. Considering buffers 1 and 2, data readout for presentation on the CRT is accomplished as follows:

Buffer 1, upper left - Gate video to display station, and regenerate buffers 1, 2, 3, and 4.

Buffer 2 - lower left - Gate video to display station, and regenerate buffers 1, 2, 3, and 4.

Retrace - Regenerate buffers 1, 2, 3, and 4.

The sequence noted above is also applicable for buffers 3 and 4. Buffers 3 and 4 do not gate data to the display stations until line 255 has been displayed by buffers 1 and 2. When the line counter contains an effective count of 496, the horizontal retrace is initiated to return the electron beam to the left side of the screen. The horizontal retrace slots are identified in Figure 2-26 by the letter X. Since information in the delay lines is dynamic, information moves along the line in respect to time. As line slot 16 emanates from buffer 1 (A in Figure 2-26), slot 101 (video for character 15) is made available in buffer 2. Recall, however, that line 16 contains BCD and that slot 101 will be displayed later; therefore, both slots are regenerated and not displayed. Upon completing the BCD readout from buffer 1, buffer 2 supplies BCD for the lower-left section of line 16 (lower-left buffer 2). During this time, video 3 for character 29 is available in buffer 1. Both slots are again regenerated and not displayed. The next slot readouts from buffers 1 and 2 (102 and 187) occur during retrace and are regenerated and not displayed. Video readout for the first character begins on line 17, which is V1 for character 1. After buffer 2 supplies video for character 1, the beam retraces again during the next slot period. Line 18 is then made available by buffers 1 and 2, etc. When line 85 (B) has been displayed, readout for line 86 is supplied by precessing buffer 1 (C). That is, entry into buffer 1 occurs two slots later in time from the first cycle readout, which was initiated at a line count of 0. The third cycle readout of buffers 1 and 2 occurs at a line count of 171 (D). The third readout sequence completes readout of buffers 1 and 2. Similar controlled functions are employed to read out buffers 3 and 4. When video


D
C
A
Upper
Lower
Retrace
Time Duration of Each Slot = 21.7 us.
Line Counter
Upper Left Buffer 1
Line Counter
Low Left Buffer 2
Line Count Equal to Upper Left Buffer 1 + 256
Upper Right Buffer 3
Line Count Equal to Lower Left Buffer 2 + 256
Lower Right Buffer 4
Line Counter
Upper Left Buffer 1
Line Counter
Lower Left Buffer 2
Line Count Equal to Upper Left Buffer 1 + 256
Upper Right Buffer 3
Line Count Equal to Lower Left Buffer 2 + 256
Lower Right Buffer 4

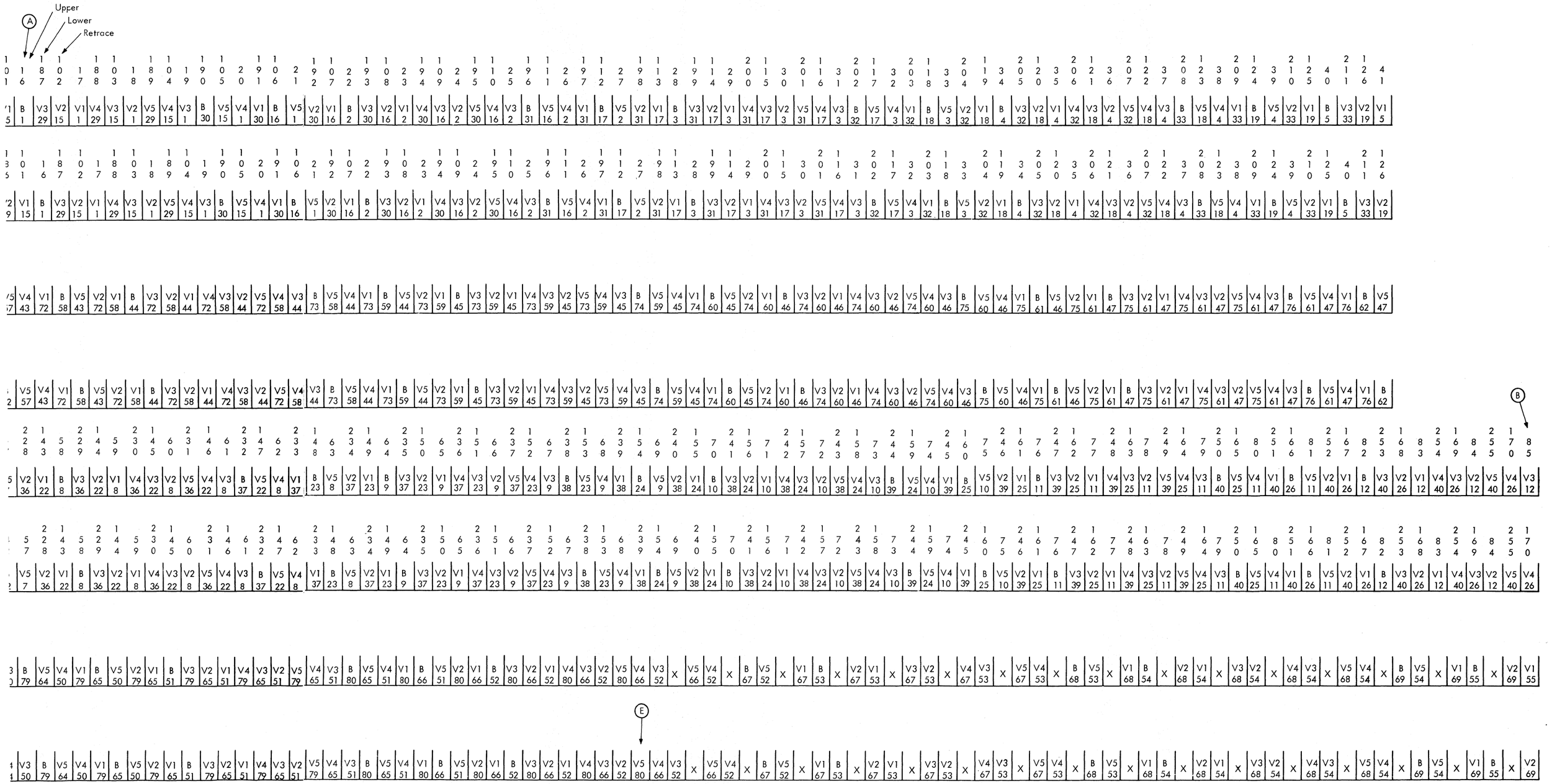


Figure 2-26. Buffer Slot Layout

for character 80 (E) has been displayed, the horizontal retrace must be initiated to return the electron beam to the upper-left section of the screen. Horizontal retrace time is denoted by slots identified by the letter X. Display of information is reinitiated when line 16 is detected. The time duration required to display the four buffers is equal to the time between horizontal retrace operations (33.3 ms).

Since the period required to display each frame is 33.3 ms, character entry or updating must be restricted to this time period unless some method can be devised to permit entry into buffer storage in addition to the actual time that data is being displayed. This time period could be reduced in many ways since the same data bit (TIC) emanates from each buffer six times during the display of one frame. Figure 2-26 shows that a slot relationship exists between buffers 1 and 2 and 3 and 4. That is, when buffers 3 and 4 are gating V4 out of their associated delay lines, BCD data is available from buffers 1 and 2. Conversely, when buffers 1 and 2 are gating V2 data, BCD is available from buffers 3 and 4. This relationship is used to obtain entry into the left or right buffers as the electron beam sweeps characters on the right or left side, respectively, on the CRT. In this manner, character readout or update can be effected into or out of any buffer every 16.6 ms.

Delay Line Controls

The delay line control circuits illustrated in Figure 2-27 control the operations in the A and B delay lines in an adapter. As data bits emanate from the delay lines, they must be regenerated and reinserted into the delay lines if the integrity of stored information is to be maintained. Since the A and B delay lines operate similarly, only the A delay line will be described in detail. The theory of operation for the A delay line will also be applicable to the B delay line. Bit readout from the A delay line loads its associated buffer trigger A (Bfr T A) to the set or clear side in direct relationship to the bit read out from the delay line. The set condition of Bfr T A requires the coincidence of a bit read out from the A delay line and the B delay pulse. A 1 or 0 bit read out from the delay line, together with the rise of the B delay pulse, sets or clears Bfr T A according to the bit read out from the delay line. The status of Bfr T A is maintained for 500 ns. At this time, the status of the Bfr T A is transferred to the Reg T A. As the register trigger is loaded, the buffer trigger reloads itself with the next bit from the delay line. The output of the register trigger conditions regenerative AND's 5 or 6, depending on its status, to regenerate the A delay upon receipt of the next A delay pulse. If a write operation has been ordered by display control, AND's 5 and 6 are inhibited by the inverted output from AND 1. In this case, new information is to be written into the delay line by the write AND circuits 7 and 8. One-bits are written in by AND 7 and 0-bits by AND 8. For overall timing of the A delay readout and regeneration, including writing of new information, refer to Figure 2-28. The timing required to read a complete slot from one buffer (A and B delays) is depicted in Figure 2-29.

The output of the buffer trigger is also used in conjunction with the Even TIC Time Bfr 1 Bfr Tgr signal to detect the TIC for the A delay in buffer 1. Early detection of the TIC is required to allow activation of the proper control circuits to execute operations within display control. Buffer TIC time sampling is discussed under the paragraph entitled TIC Sample Decoder. If an erase operation has been programmed by the keyboard (ERASE key depressed), the TIC is simulated at the input to OR 1 by the Erase Even signal. This permits the next TIC time to start an immediate erase operation without waiting for the actual TIC.

BCD Data Gating

The BCD data gating circuits separate BCD data from video data as information is read out from the delay lines. BCD information is transferred serially to the common buffer register for further processing by the user. Code translation from BCD to the code required by the user (such as printer or remote interface) is effected by the character generator. The BCD gating circuits (AND's 13-16, 21-24, 29, and 30) for adapter 00 are illustrated in Figure 2-27. Identical circuits are employed for the other three adapters. Output signals (consisting of BCD and video) supplied by register trigger A of buffer 1 are fed to buffer AND 13 associated with the A bank of AND's. Register trigger B supplies BCD and video to AND 21, which is associated with the B bank of AND's. The remaining AND's in each bank are related to the A and B register triggers for buffers 2, 3, and 4. BCD is separated from video by the BCD Bfr levels, which are active during BCD time only. Thus, video data is inhibited and cannot be gated to the common buffer register or parity check circuits. BCD data from the A and B delay lines is gated through AND's 29 and 30 and fed to the common buffer register where it is deserialized.

Video Data Gating

The remaining circuits shown in Figure 2-27 are used to gate video information read from the delay lines to the even and odd display stations associated

with the adapter. Since video information for both displays (even and odd) is stored alternately in the A and B delay lines, gating circuits must be provided to separate the bit readouts so that the information can be properly directed to the odd or even display. For this reason, two AND circuits are required to gate video from the A delay and two from the B delay. Considering the A delay only, AND 17 is used to gate video data for the even display.

AND 31 is active to gate video from the A delay for the odd display stations. The remaining AND's are used in an identical manner for gating video from their respective delay line buffers. Timing for each of the AND circuits is provided by the A or B delay TP2 pulse and by Bfr Vid Ev or Odd selection signals. The selection signals are derived from the character display column ring counter (not BCD) and from the applicable even-odd time. Horizontal and vertical synchronization pulses are mixed in the video mixers (VM 1 and 2) to form the composite video signal required by the display stations. Vertical sync signals are interleaved every 65.1 μs, the horizontal sync pulses every 33.3 ms.

Keyboard Operation

The operation of the keyboards associated with a 2848 Display Control is discussed below, first by considering the relationship between keyboards with respect to keyboard priority and, then, by discussing the control and data gating circuits of a single keyboard in detail.

Keyboard Priority: The keyboard priority scheme provides for the situation wherein one or more keyboards associated with the same control unit attempts to obtain control of the common control area. All keyboards operating with a control unit are assigned a number. For example, a maximum of eight keyboards can be attached to the 2848 Model 3; they are assigned the number 00-07. Each keyboard is further designated as either even or odd. The adapter-to-even/odd keyboard relationship is shown in Figure 2-30.

Two groups of keyboards are established: the even and the odd. A separate priority chain is established for each group. Within both the even and odd keyboard groups, the lower the keyboard number, the higher its priority. For example, in Figure 2-30, even keyboard 00 has priority over keyboards 02, 04, and 06, while keyboard 04 has priority over only keyboard 06.

This priority order is modified by using the TIC's associated with the keyboards to finally decide which keyboard is accorded service. In this manner, a higher-priority keyboard is prevented from controlling the common area during a lengthy (up to 16.5 ms) TIC search when a lower-priority keyboard has also requested service and has its TIC more immediately available. It is likely that the lower-priority keyboard operation will be completed before the higher-priority keyboard's TIC is found because of the short time required for keyboard input operation.

The priority circuits for three even-numbered keyboards are shown in the second-level diagram of Figure 2-31. Assume that the strobe inputs to A1 (KB00) and A3 (KB02) are both conditioned and that the AND's are not inhibited because common control is not busy. Then, both the KB00 and KB02 Strobe latches are set. At AND's A7 and A8, note that the TIC is required to condition the circuit completely. If the Even TIC input to A7 arrives first, A7 is conditioned and provides an output to the address encoder. The output of A7 is also inverted and used to inhibit all other "TIC AND's" in the priority circuits.

The A7 input to the address encoder eventually produces the Set KB00 Strobe latch signal which maintains the KB00 Strobe latch in the set condition. At this time, the Inhibit line deconditions all strobe AND's (A1, A3, and A5) because common control is busy (controlled by KB00). When Strobe Reset occurs, all Strobe latches except that for KB00 are reset. The Strobe input to A3 (KB02) is still present since the keyboard has not been serviced. Thus, when common is again available, the KB02 Strobe latch will be set in a second attempt to obtain service.

Now, starting again with the initial setting of the KB00 and KB02 Strobe latches, consider the sequence of events that occur when the KB02 TIC (lower-priority keyboard) is found first. AND A8 is conditioned. Its output inhibits all lower priority (TIC AND's) and causes the generation of Set KB02 Strobe latch from the address decoder. Since KB02 has control of common, the Inhibit input deconditions all "strobe AND's". The Strobe Reset occurs, and all Strobe latches (including KB00) are reset with the exception of the KB02 Strobe latch. Keyboard 00's strobe input is maintained until common control is free and the keyboard receives service.

Keyboard Controls: The keyboard control circuits for a typical keyboard are illustrated in Figure 2-32. The controls illustrated are those for Even Keyboard 00; however, the controls for all keyboards are very similar. The differences are limited to certain line names and the inhibit select inputs generated in conjunction with keyboard priority. In the latter case, note A6 in Figure 2-31. Since KB00 has the highest priority, this AND is not inhibited by the KB Sel signals from other even keyboards in the

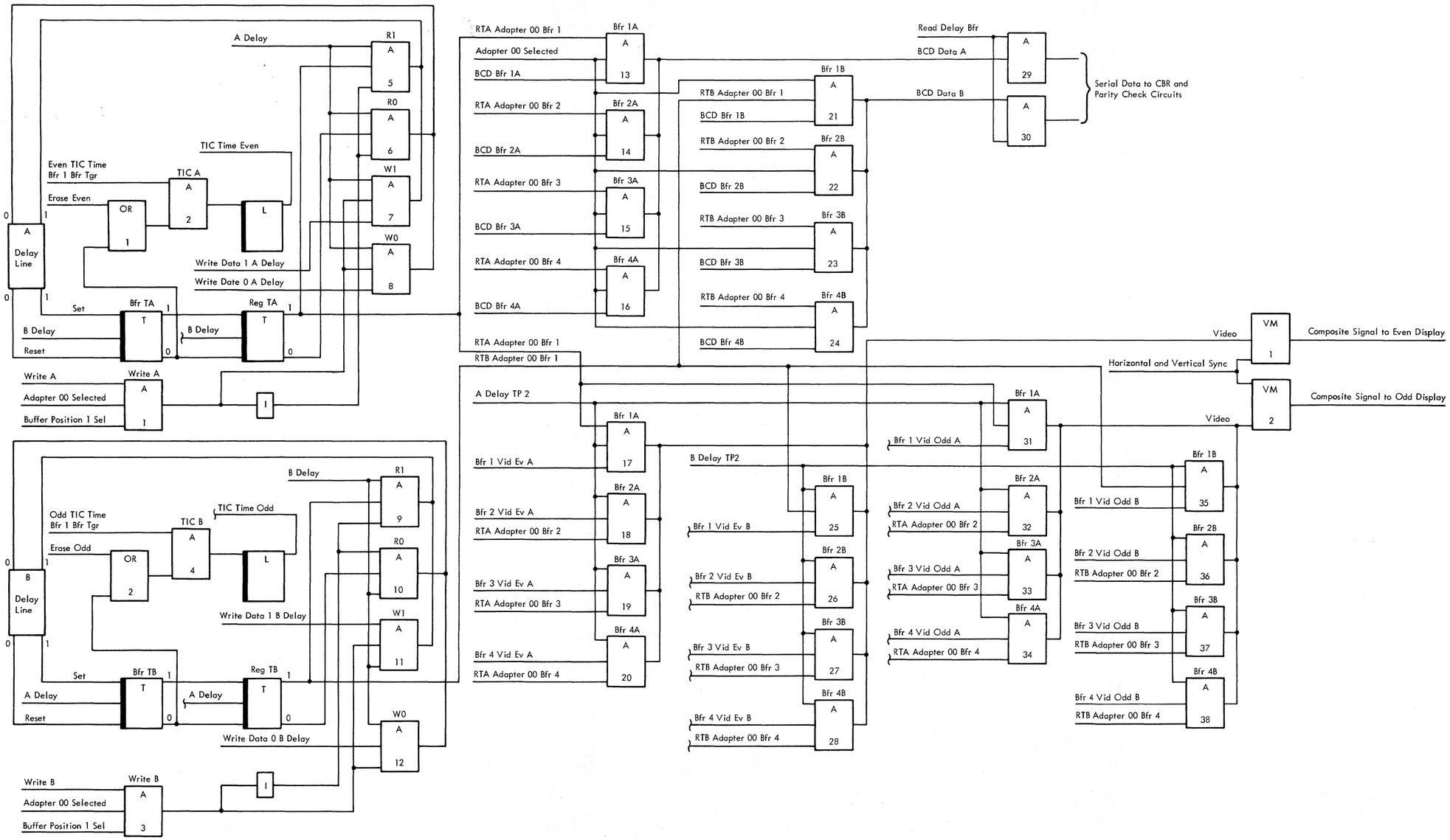


Figure 2-27. Delay Line Controls and BCD-Video Gating

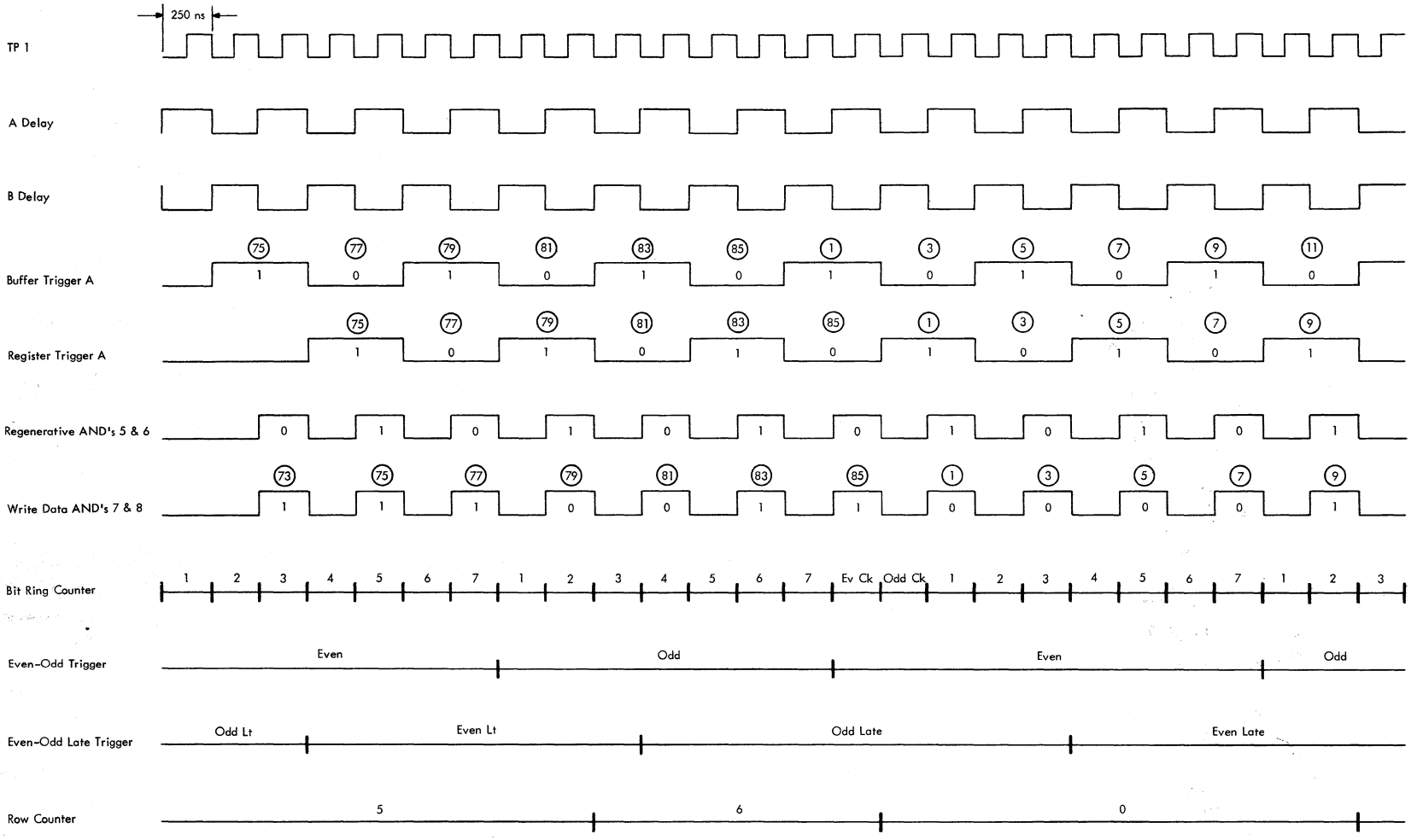


Figure 2-28. Delay Line Control Timing

priority chain. Note A10, which is included in the figure to illustrate the progressive KB Sel Inhibit. KB06 would be the lowest-priority even keyboard in a 2848 Model 3 priority chain. Therefore, its select AND is inhibited by the KB Sel signals of all other (three) even keyboards.

The keyboard control logic is initiated upon receipt of the +48v Strobe signal from the associated keyboard. The Strobe does not affect the MI Enter or KB Reset latch at this time since these latches were reset when Strobe deconditioned during a previous operation. The Strobe does condition A8, whose output conditions one input to A4. AND 1 is conditioned, and it inhibits A4 only when a Print command has been issued and the printer is busy. AND 2 represents a similar situation with respect to an Enter command and interface busy. The +Y Inhibit Keyboard Strobe is conditioned only after a keyboard is selected. Thus, A4 is conditioned and sets the KB00 Strobe latch. When the 00-even TIC is found, -Y TIC Time Even conditions A6, which produces the KB Sel signal. KB Sel is routed to the keyboard address encoder and is used to inhibit all KB Sel AND's (such as A6) in the keyboard control circuits of all lower-priority keyboards.

The addressing circuits produce the +Y Inhibit Keyboard Strobe (A4), which inhibits the set AND's for all even keyboards, and the +Y Adapter 00 Sel Even, which holds the KB00 Strobe latch set. Note that no other even keyboard Strobe latch except KB00 (which was selected) receives this set hold input from the addressing circuits. Next, the +Y Reset KY BD Strobe is applied to all even keyboard Strobe latches. All Strobe latches except the KB00 latch are reset at this time.

Near the end of the operation, the Reset KYBD input to A7 is generated. Since the KB00 Strobe latch is still set, A7 is conditioned, and the KB Reset latch is set. The +Y KYBD Reset output from the KYBD Reset latch energizes the KB Reset coil to complete the keyboard Restore line's path to the dc return. The keyboard restores, and the Strobe and data lines from the keyboard are deconditioned. The deconditioning of Strobe resets the MI Enter and KB Reset latches in preparation for the next KB00 input operation. The KYBD Reset signal is terminated when the End Op latch is set since keyboards awaiting service are permitted to set their Strobe latches at the start of End Op. If the KYBD Reset signal is not terminated by End Op, keyboards requesting service are restored before being accommodated by the control unit.

The above discussion of keyboard operation did not involve the MI Enter latch, which functions only when an Enter command is issued from the keyboard. In that case, the MI Enter latch is set to generate +Y KB 00 MI Enter, which sets the Enter latch (ALD 9.05.30.2). While the Enter command is pending, the odd keyboard (KB01) sharing the adapter with KB00 is allowed to write the delay lines. However, as soon as the Enter is honored and the read MI operation starts, no other operation is permitted. At the end of the read operation (End Op Reset), other operations are allowed. Then, the MI Sent input to A5 (Figure 2-32) falls so that the MI Enter latch is not held set. When Strobe falls, the MI Enter latch is reset.

(Although the above discussion describes the operation of a single even keyboard, the operation of the keyboard controls for the other two even keyboards and for odd keyboards is essentially the same.)

Keyboard Data Bit Conversion and Gating: A typical set of keyboard data bit conversion circuits and a portion of the data gating circuits are shown in Figure 2-32. The keyboard data converter operation can be summarized by the following two statements:

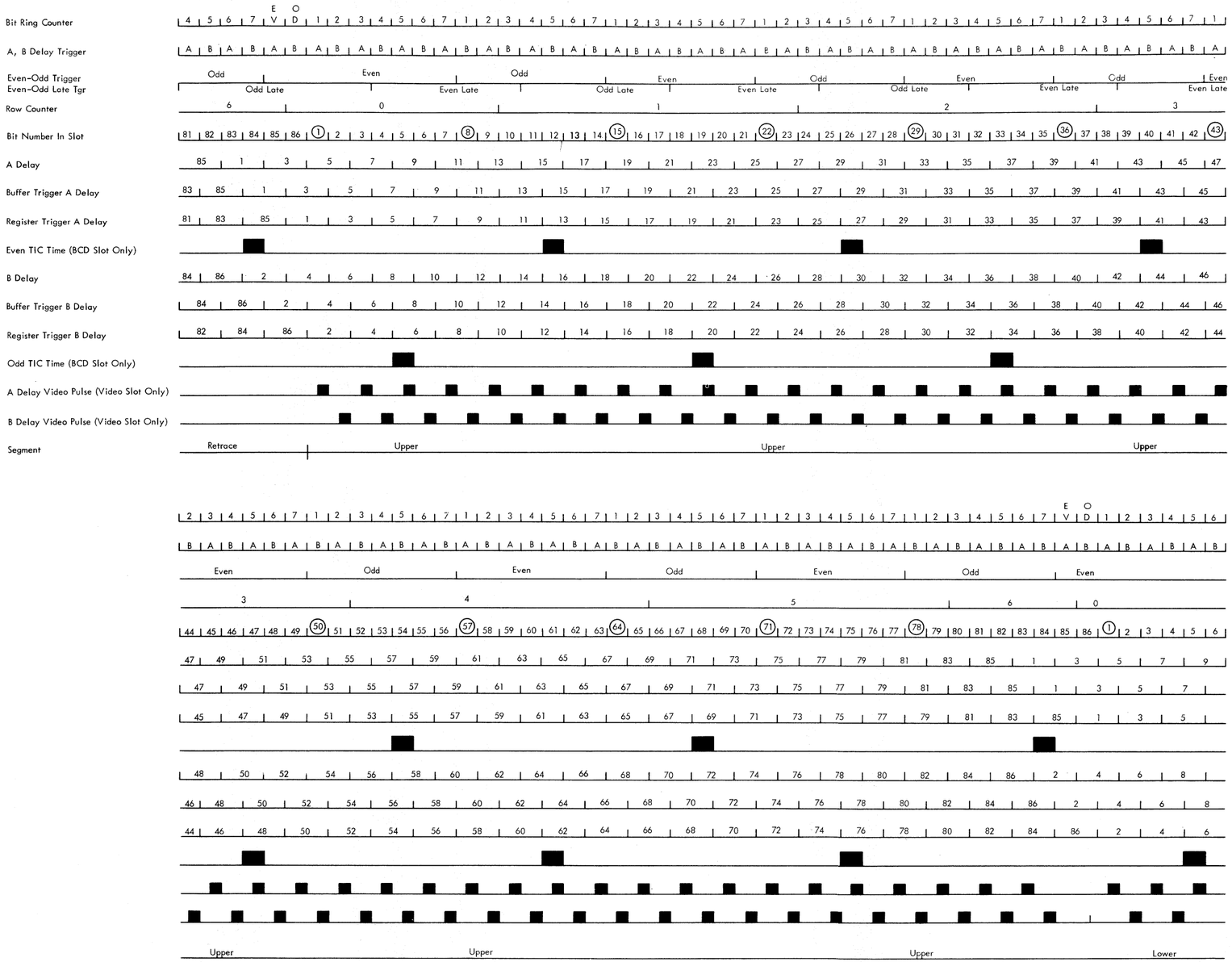
1. A +48v input from the keyboard results in a +Y output from the converter.
2. No input (open line) from the keyboard results in a -Y output from the converter.

Data gating is accomplished by OR'ing the bits from all keyboards attached to the control unit and then gating only the selected keyboard's bits through the OR to the keyboard command decoder. The OR for data bit 4 is shown in the figure. Note that OR 3 receives a bit-4 input from the maximum number of keyboards that can be associated with a 2848 Model 3. (Up to 24 keyboard-bit inputs (2848 Model 1) can be OR'ed in this fashion.) An identical OR exists for each of the other keyboard data bits.

The data gate for KB00 bit 4 only is illustrated. Remember that each data bit is routed through an AND gate of this type. Note that only the selected keyboard's data bits are gated through the OR and used as inputs to the keyboard command decoder.

Timing and Clock Circuits

The timing and clock circuits (Figure 2-33) synchronize and direct delay line storage, keyboard input operations, sequence timing, and interface operations. They also direct the displays of the associated display stations through a series of counters that effectively remember the instantaneous position of the display on the viewing screen of the CRT's. These circuits alternately service the two display stations associated with each display adapter; i.e., one display is serviced while the other is blanked (between lines). Basic timing pulses, generated by a 4-mc oscillator, are used to step the timing and clock circuits. As the counter and clock circuits are stepped, their output signals



Circled Bits Indicate Possible TIC'S.

Figure 2-29. Delay Line Timing, One Slot

Adapter	Keyboard Assignment	
	Even	Odd
00	00	01
01	02	03
02	04	05
03	06	07

Figure 2-30. Keyboard Assignments for Model 3 Machines

control the display cycle for all the display stations. The timing and clock circuits consist of the following:

1. Oscillator
2. A and B Delay pulse circuit
3. Bit ring counter
4. Even-Odd Display trigger
5. Buffer parity control circuit
6. Row counter
7. Segment counter
8. Character display column ring counter
9. Line counter
10. Sync generator
11. Reset controls

Oscillator

- Crystal-controlled square-wave oscillator.
- Provides a continuous square wave at a frequency of 3.96288 mc.
- Generates basic timing pulses called TP1 and TP2.

Basic timing pulses required by the display system are generated by a crystal-controlled square-wave oscillator (Figure 2-34). This oscillator, which provides a continuous square wave at a frequency of 3.96288 mc, is referred to as a 4-mc oscillator throughout this manual (since its operating frequency is almost 4 mc). The two basic timing pulses, TP1 and TP2, are 180 degrees out of phase in respect to each other.

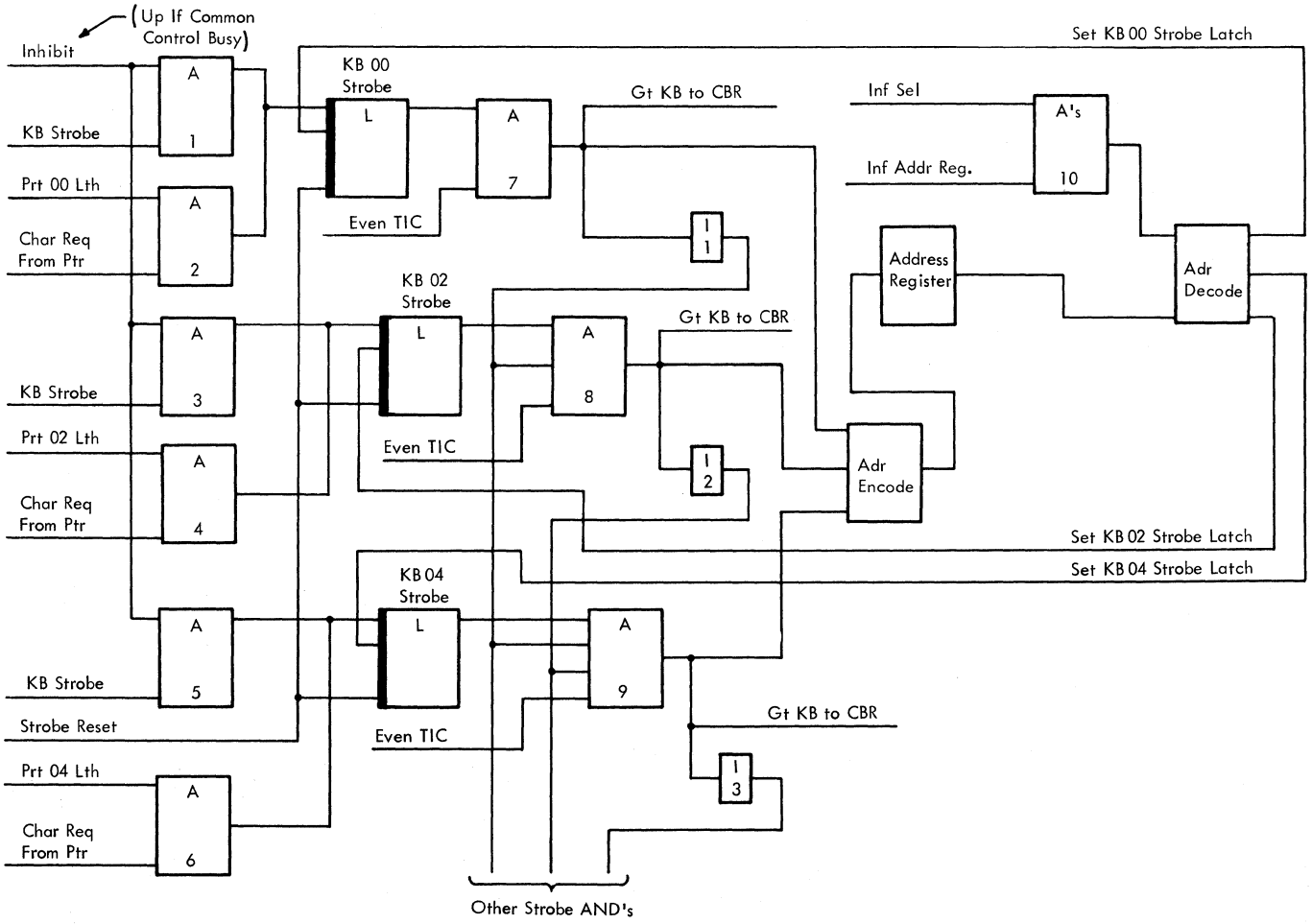


Figure 2-31. Keyboard Priority

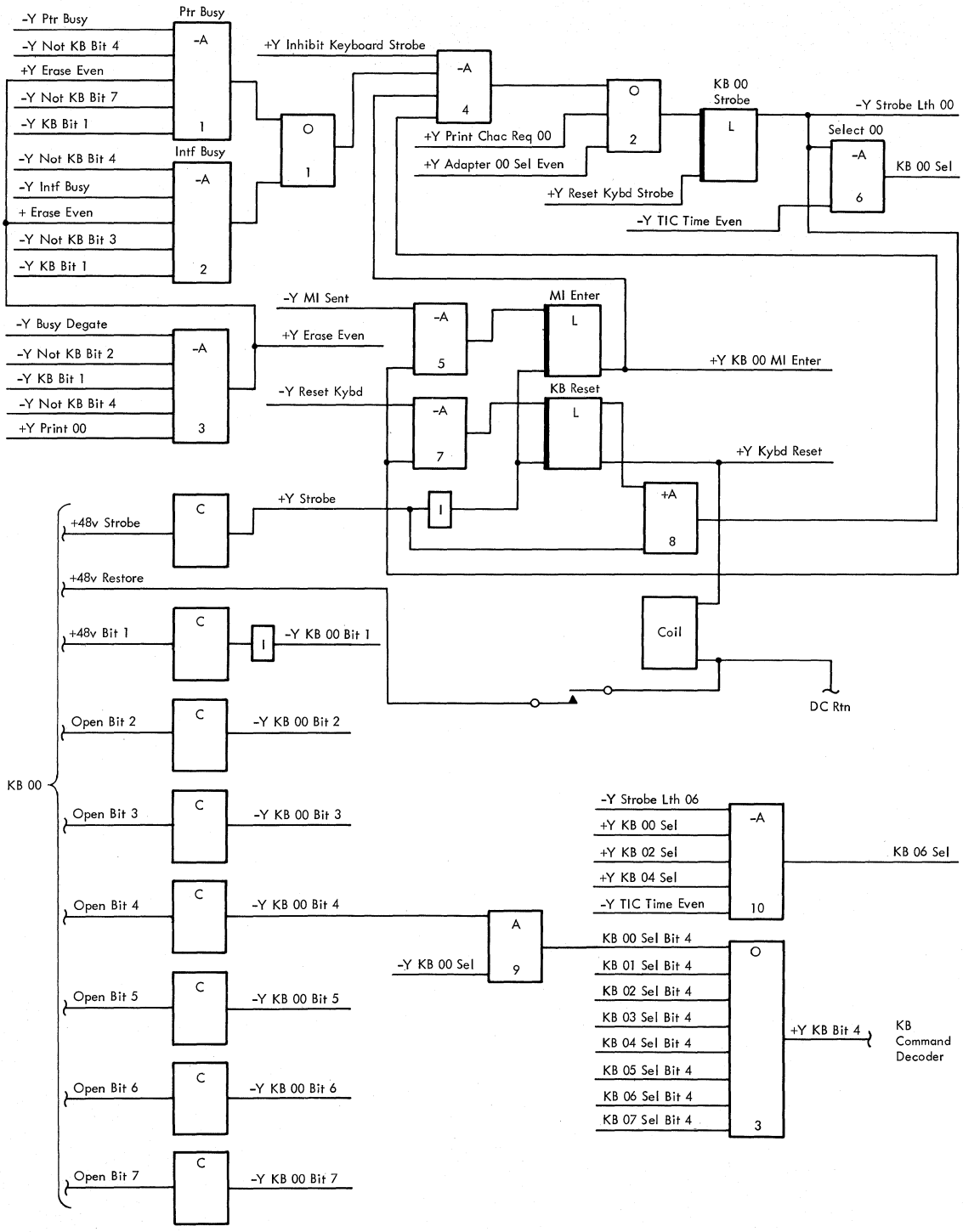


Figure 2-32. Keyboard Controls and Keyboard Data Bit Conversion and Gating

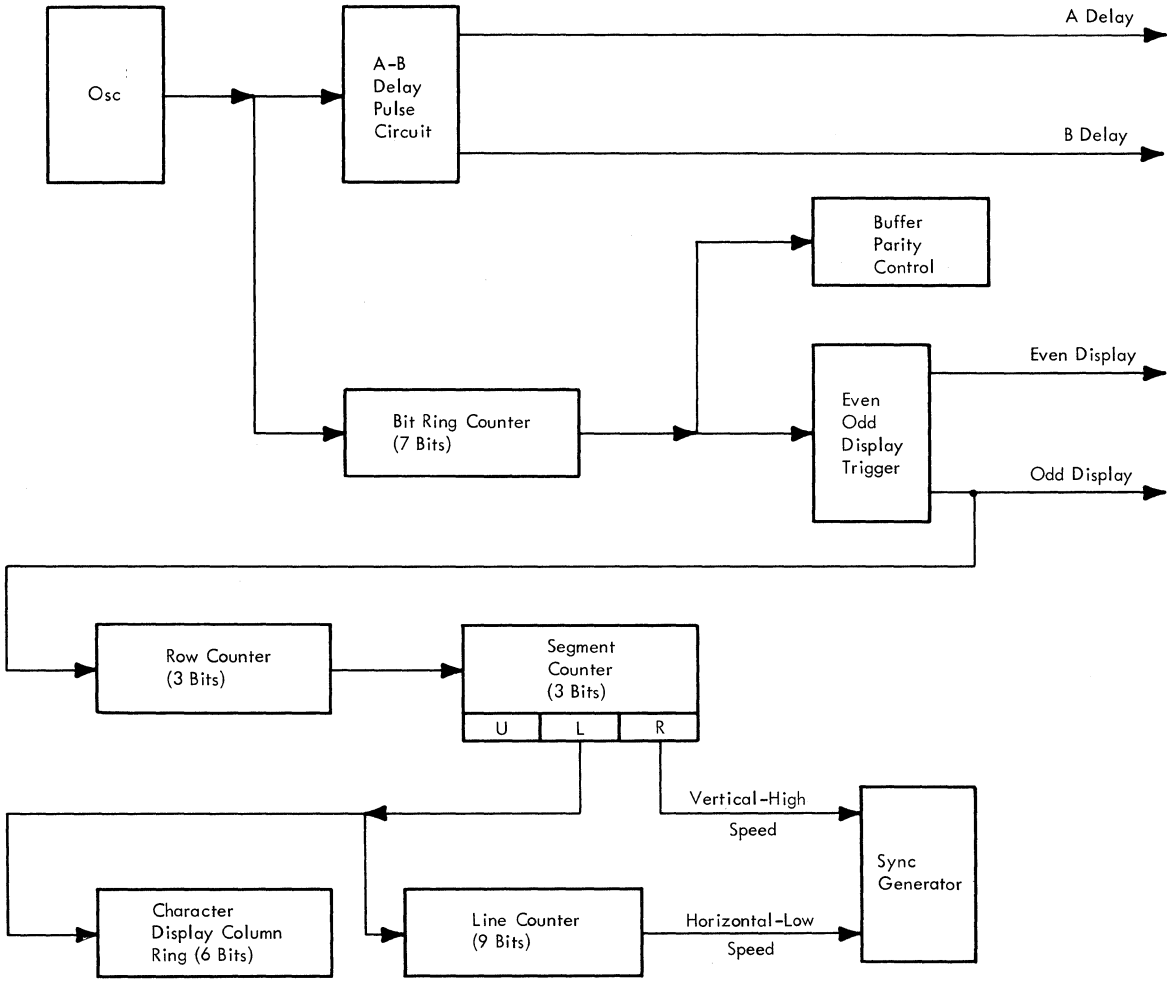


Figure 2-33. Timing and Clock Circuits, Simplified Block Diagram

A and B Delay Pulse Circuit

- Generates A and B Delay pulses recurring at a 2-mc rate.
- Supplies TP2 pulses gated by A and B Delay pulses.

The A and B Delay pulse circuit (Figure 2-34) is a high-speed frequency divider which subdivides the oscillator frequency of 4 mc into 2 mc. The A and B Delay and A and B Delay TP2 pulses are employed as read-write timing signals for entering data in or extracting data from the delay line buffers and for gating BCD and video signals within the adapter. Oscillator pulses complement the binary trigger, which produces the A, B Delay. The A, B Delay signal gates TP2 to generate the A, B Delay TP2 pulses. The Odd Check Shift level provided through I4 ensures proper synchronization of the Delay trigger (A Delay at ring 1 even). The set condition of the trigger at this time ensures generation of the A Delay pulse before the B Delay pulse when operations are initiated.

Bit Ring Counter

- Stepped at TP1 time after Bit 1 trigger is turned on by Bit 7 Shift, Odd Check Shift, or Machine Reset.
- Provides seven sequential counts to serialize or deserialize a seven-bit byte.
- Steps the row counter at a count of 3 when the Even-Odd trigger is set to odd display.
- Initiates end-of-slot parity check control when row counter contains a count of 6 (ring count equals 7) and inhibits further cycling of ring counter until Odd Check Shift level is received.
- Sets Even Check trigger when bit ring counter equals 7 and the row count is 6.

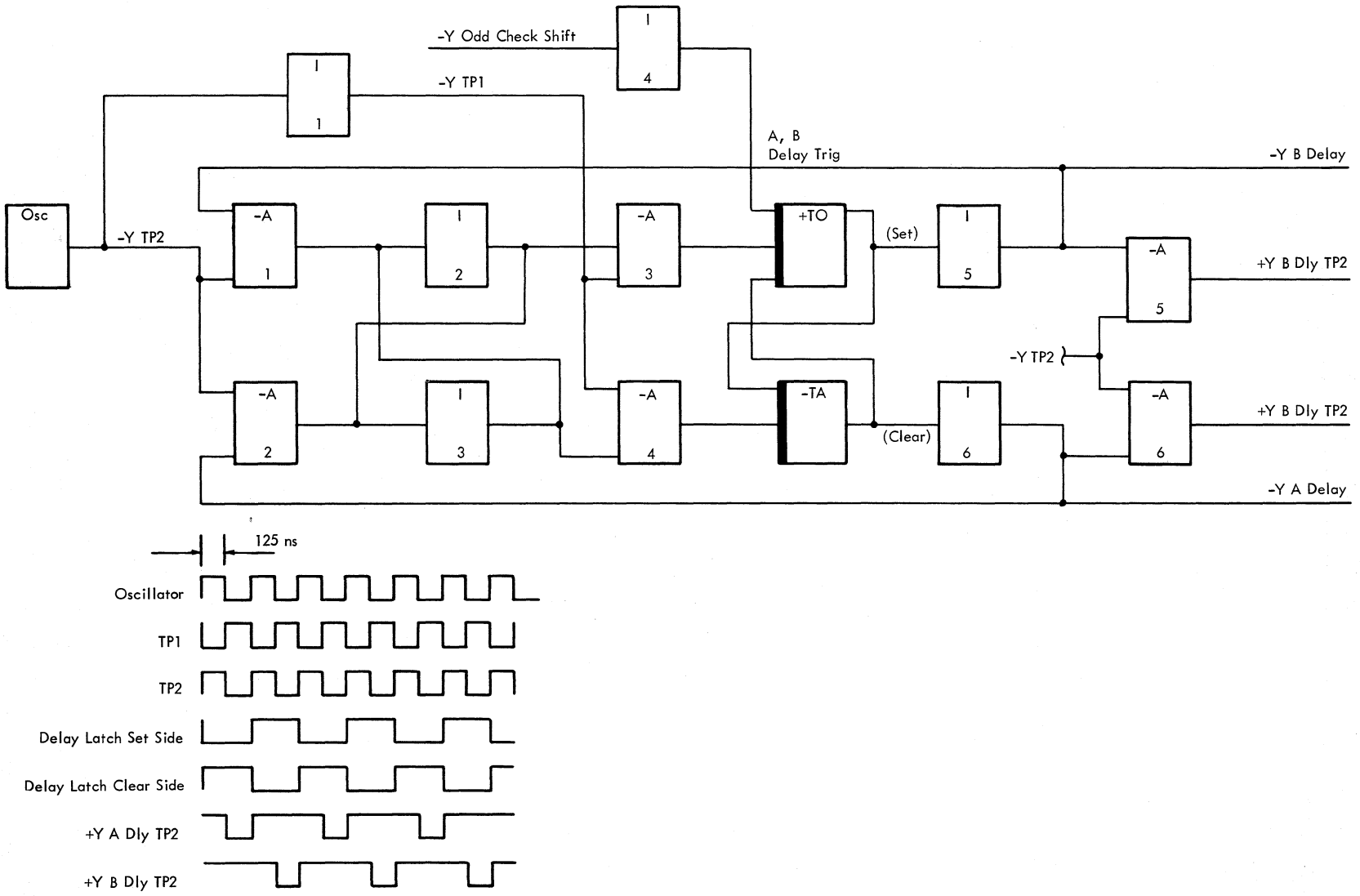


Figure 2-34. Oscillator and A-B Delay Pulse Circuit

The bit ring counter (Figure 2-35) is a seven-stage step counter which supplies seven sequential outputs. The output levels derived from the counter are used to serialize or deserialize information bytes (BCD and video) and to execute other control functions within the control unit. Operation of the bit ring counter is simply a stepping function of TP1 pulses when the first bit of the counter (L1) has been turned on. This turn-on occurs if one of the following three signals becomes active: Odd Check Shift, Bit 7 Shift, or Machine Reset. Note that the Machine Reset signal is also routed to the remaining latches in the counter (except 7), where its function is to reset them, whereas bit 1 is set. Bit 1, when set, clears the bit 7 latch. The following TP1 pulse completes the input requirements to AND 1, which clears L1 and sets L2. The next TP1 fully conditions AND 2 to clear L2 and set L3. Each successive latch is set in the same manner until L7 (bit 7) is set. Assuming that the row counter does not contain a count of 6, the output of AND 7 clears L7 and sets L1 to permit the bit ring counter to cycle continuously. The cycling process continues until the Row Ctr 6 signal becomes active to decondition AND 7, thus inhibiting the Bit 7 Shift level and recycling the counter. In this case, AND 8 is conditioned to clear L7 and makes available the End of Slot P Chk pulse. This indicates that end of slot has occurred and a pause of 500 ns (two ring counts) must elapse before the counter recycles to allow time for a BCD parity check for both even and odd displays. Upon completion of the parity check, the Odd Check Shift level is received to set L1 and permit the bit ring counter to begin stepping again.

In many instances, ring levels (and other latch circuits) are required to perform certain control functions during the latter portion of the time they are active, including transition time. Output levels during transition time cannot be used since "slivering" results and positive response of circuits cannot be predicted. To avoid the effects of slivering, overlap (OVLP) pulses are employed in those circuits where the control level normally supplied by a latch would be in its transitory state. The overlap level is derived from the same latch that provides the basic signal. If the basic signal (such as +Y Ring 7) is supplied by the cleared side of the latch, the -Y Ring 7 OVLP level is obtained from the set side. The overlap pulse becomes active slightly sooner, and the fall time of the overlap pulse occurs later in relation to the level generated by the other side of the latch. Use of the basic or overlap signal is dictated by timing considerations.

Even-Odd Display and Late Triggers

- Condition of Even-Odd Display trigger signifies that display of data is associated with even display station when reset and with odd display station when set.
- Even-Odd Display Late trigger supplies gating levels during transition time of Even-Odd Display trigger.

The Even-Odd Display trigger circuit (Figure 2-36) determines whether data is associated with an even or odd display station. The set side of the trigger signifies that operations such as readouts from the delay lines will be distributed to the odd display station, and the clear or reset side signifies that operations within display control are associated with the even display station. Since the two preceding conditions are complementary, only one of the conditions can exist at any one time. (This is readily discernible in the timing illustrated in Figure 2-36.) In the normal execution of operations within display control, it becomes necessary to maintain Even-Odd Display levels during transition time of the Even-Odd Display trigger. For this reason, the Even-Odd Late trigger has been incorporated in this circuit. In applications where the Odd-Even Display levels are required during ring counts of 6 and 7, the Late levels are used to ensure positive circuit response. The Even-Odd Display trigger is complemented at a ring count of 7, whereas the Late trigger is complemented at a ring count of 4.

Buffer Parity Control Circuit

- Controls parity check or assignment of BCD data, for both even and odd display stations, on a slot basis.
- Extends bit ring counter by two counts when end of slot has been detected.

The buffer parity control circuit (Figure 2-37) extends the ring counter by two bit periods when the end of slot (row counter equal to 6) has been detected. This time period is used to check parity of BCD data read from the delay lines or to assign parity when a slot is modified. Although the two bit periods occur at the end of each slot, parity is assigned or checked when a write or read operation has been programmed. Parity is neither checked nor assigned during regeneration of the display. Control of parity assignment or check for the even display station occurs when the Even Check

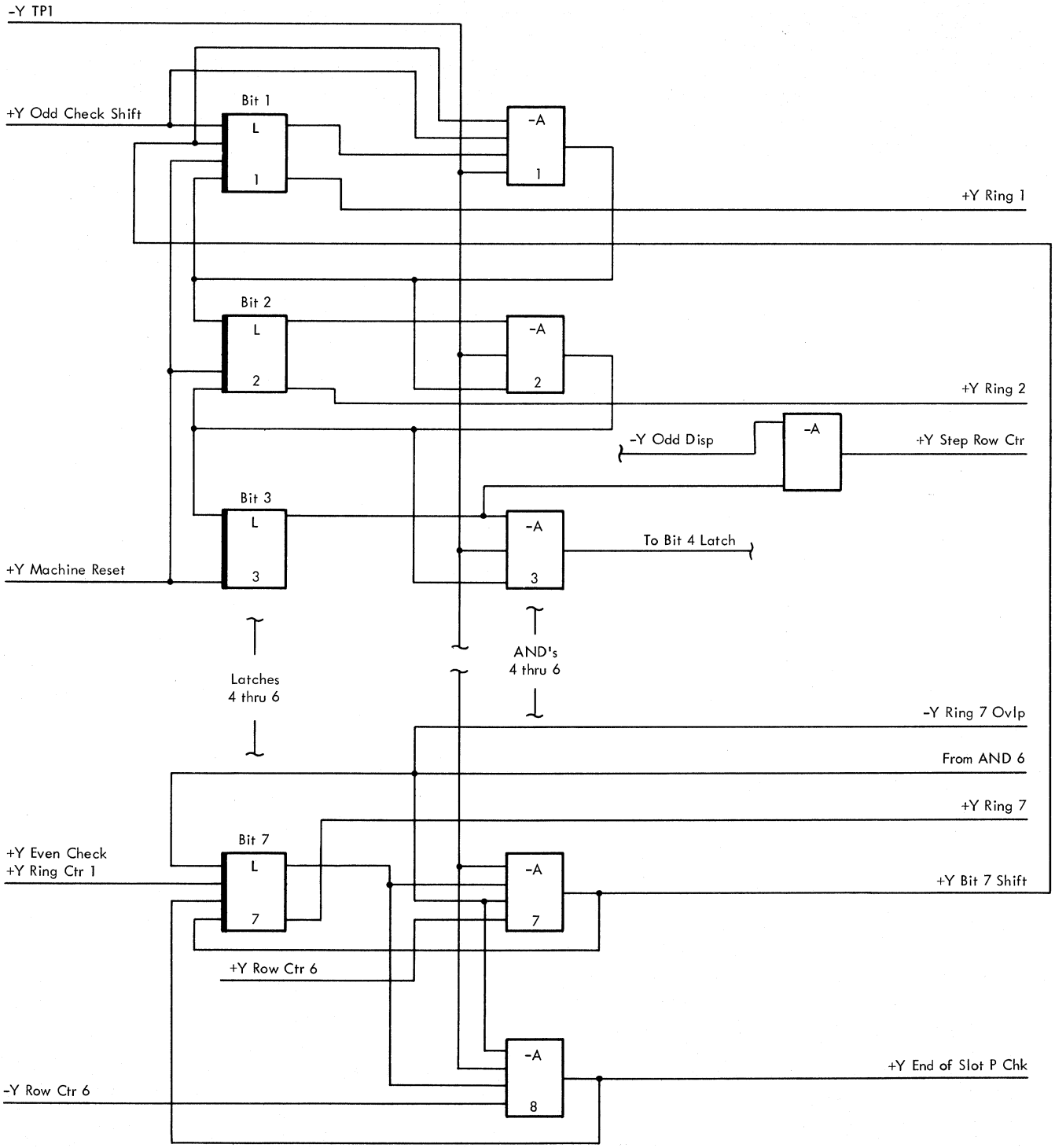


Figure 2-35. Bit Ring Counter

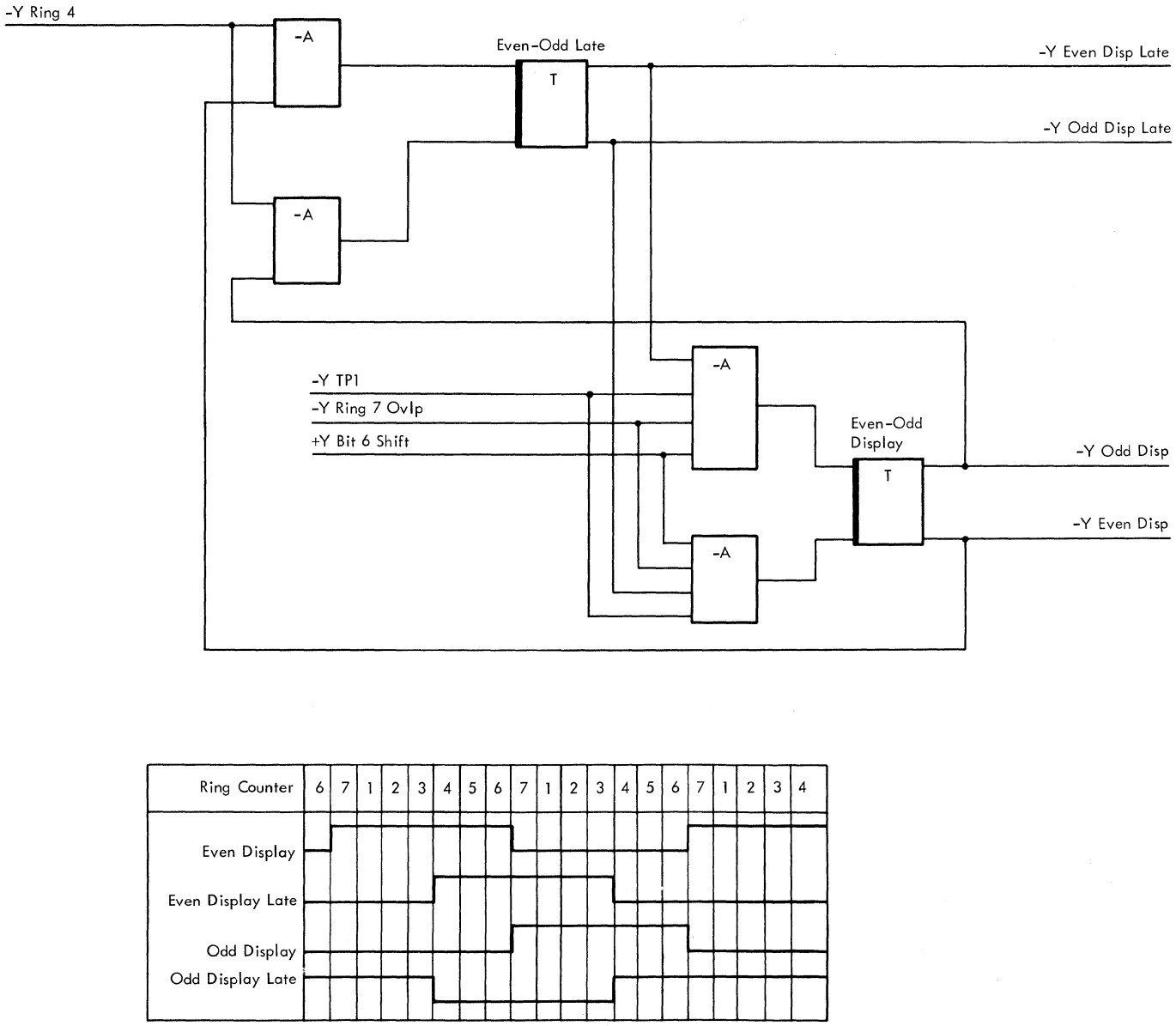


Figure 2-36. Even-Odd Display Trigger Circuit

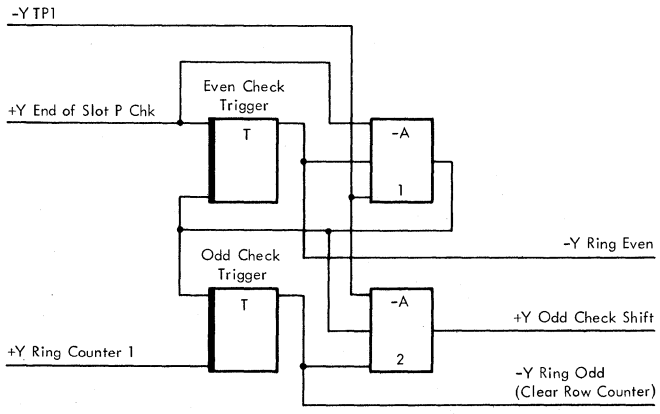


Figure 2-37. Buffer Parity Control Circuit

latch is set. The Odd Check trigger controls parity for the odd display station. Operation of the buffer parity control circuit is initiated when the bit ring counter equals 7 and the row counter equals 6, thus generating the End of Slot P Chk signal to set the Even Check trigger. The trigger output activates parity control for the even display. The next TP1 fully conditions AND 1 to clear the Even Check and set the Odd Check triggers. The Ring Odd level initiates parity control for the odd display and clears the row counter. The following TP1 completes the input requirements to AND 2, making the Odd Check Shift level available. This level reinitiates the stepping of the bit ring counter. Once bit 1 of the ring counter is set, the Odd Check trigger is

cleared. Both the Even and Odd Check triggers remain cleared until the next end of slot has been detected.

Row Counter

- Keeps track of the vertical sweep on the CRT as sweep progresses from top to bottom of viewing screen.
- Stepped when bit ring counter contains a count of 3 and Even Odd latch is set to odd.
- Inhibits bit ring counter from recycling when end of slot is detected (row count 6) until parity is either assigned or checked on BCD data.

The row counter (Figure 2-38) is a three-bit binary counter whose contents indicate the relative position of the vertical sweep on the CRT as the sweep progresses from top to bottom of the screen. The counter is advanced from 0 to 5 to indicate that the vertical sweep is passing through the row (line) count stored in the counter. Actually, the row counter is slightly ahead of the sweep position since the counter advances one count when the Ring 3 and Odd Display levels condition AND 1. When the row counter contains a count of 6, the bit ring counter is not permitted to recycle, and time must be allowed to assign or check parity. Count 6 emanates from AND 2 and extends the bit ring count utilizing the Even and Odd Check triggers. After the even check has elapsed, the Odd Check trigger signal clears the row counter so that it may be advanced as the next slot is displayed.

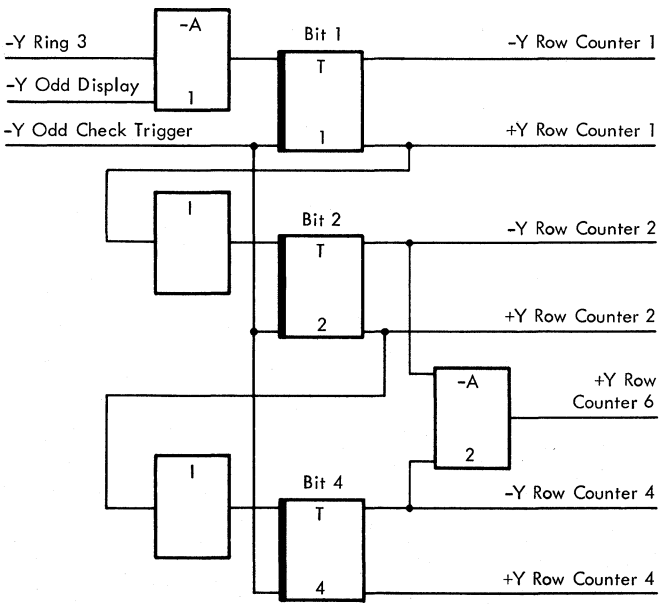


Figure 2-38. Row Counter

Segment Counter

- Selects delay line storage from where information is to be read out and displayed on the CRT.
- Upper Segment latch permits readout from buffers 1 and 3 for display in the upper six rows; Lower Segment latch permits readout from buffers 2 and 4 for display in lower six rows.
- Initiates vertical sweep retrace when Retrace Segment trigger is set.

The segment counter (Figure 2-39) selects the delay line storage from where information is to be read out for presentation on the selected display station. When the Upper Segment latch is set, character readout from buffers 1 and 3 (even and odd) will be available for display in the upper six rows of the even and odd display stations. The Lower Segment latch controls character readout from buffers 2 and 4 (odd and even) in the lower six lines of the screen. Other control functions, such as initiating the vertical retrace resetting of the parity trigger, are also performed by the segment counter.

The operation of the segment counter is merely a stepping function upon receipt of the Odd Check Shift signal at the end of each slot. Initially, the Machine Reset signal sets the Upper Segment latch and resets the Lower Segment latch. Once the Upper Segment latch is set, an output derived from its reset side is used to reset the Retrace Segment latch. This and other conditions ready the display stations to display information in the upper-left section of the screen. At end-of-slot time, the Odd Check Shift level clears the Upper Segment latch and sets the Lower Segment latch. During this period, information is displayed in the lower segment. The following Odd Check Shift level clears the Lower Segment latch and sets the Retrace Segment latch to permit the sweep to return to the upper section of the CRT. Display of information continues in the upper segment when the Upper Segment latch is set. Since the Odd Check Shift level is used to step the counter latches, the time required to sweep the beam through any of the segments (upper or lower, or retrace) is exactly the same. This is shown in the timing chart in Figure 2-39.

Upper and Retrace Segment Late signals are derived from the two additional latches shown in Figure 2-39. Late levels are used to condition various circuits throughout display control to prepare them to display the next slot. The Lower Segment latch does not require the use of a late latch because lower segment control functions can be performed during retrace time. The late levels are approximately the same width as their associated segment levels, but their turn-on and turn-off

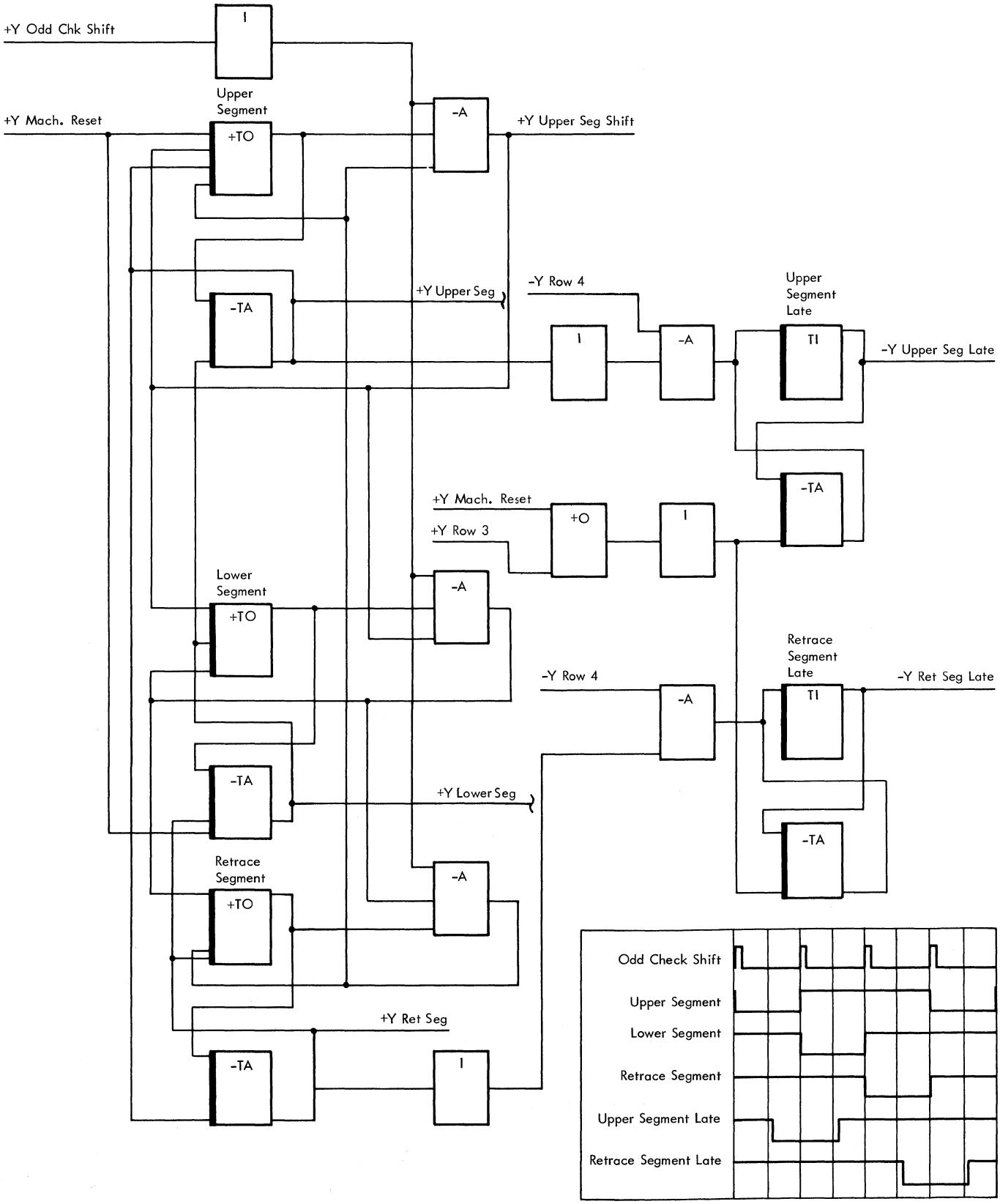


Figure 2-39. Segment Counter

times differ from the counter latches. After their associated segment latch has been turned on, each of the two late latches becomes active at a row count of 4. Both latches are reset at a row count of 3.

Character Display Column Ring Counter

- Keeps track of BCD and video readout from delay lines.
- Counter is stepped once for every high-speed sweep.
- Reset to video 2 (V2) when line counter equals zero coincident with left display.

The character display column ring counter (Figure 2-40), which consists of six triggers, keeps track of the portion of the character being swept. Recall that each character location comprises BCD and video information. When the display is sweeping the vertical space between characters, the BCD trigger is set; when video data is displayed, V1 through V5 are sequentially set, representing the video readout from the delay line. The counter is stepped during vertical sweep retrace time. Whenever the line counter contains a count of zero and video is to be displayed on the left side of the CRT, the Reset Char Col Ring signal sets the V2 trigger and clears the remaining triggers. This reset condition of the column ring counter allows the set condition of the BCD trigger to coincide with a line count of 16, at which time the BCD data for the first character is made available from delay line buffer 1. The BCD trigger remains on until all BCD data for segments 1 and 2 is read out but not displayed. During vertical retrace time, the BCD trigger is cleared and the V1 trigger is set, indicating that V1 video data will be displayed. After V1 data is displayed, the counter advances to V2, V3, V4, and V5. The character display column ring counter steps continuously until line counter equals 512. At this time, the ring counter is reset to V2 to initiate the next display cycle.

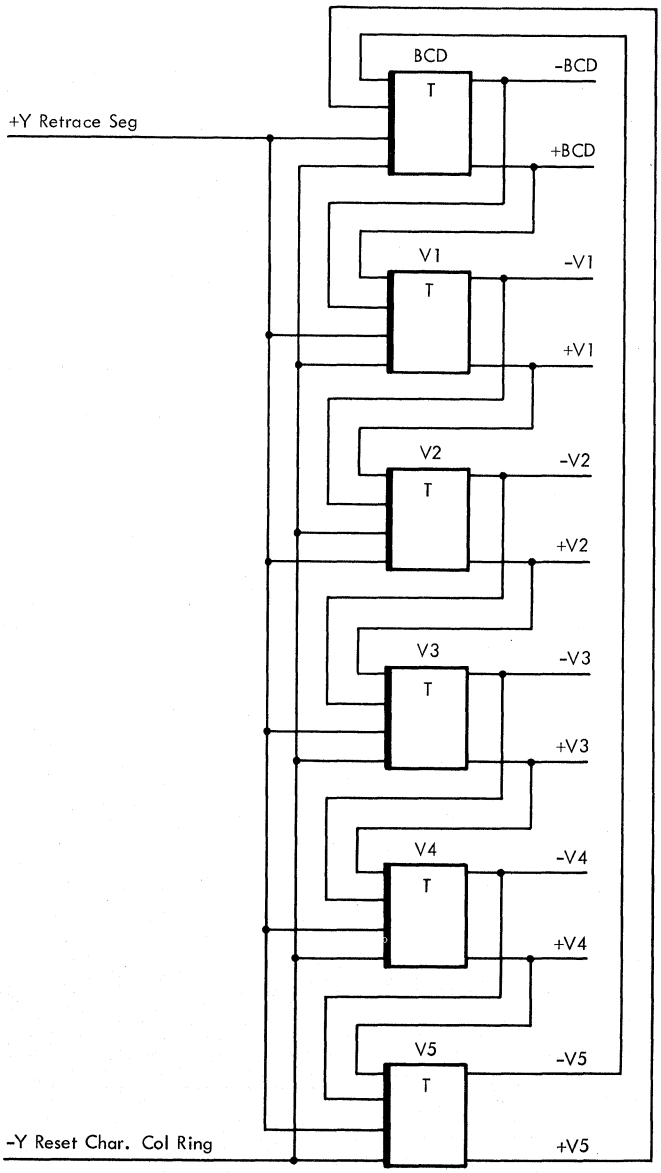


Figure 2-40. Character Display Column Ring Counter

The character display column ring counter outputs are also routed to the character generator, where BCD character representations are converted into video data representing the character.

Line Counter

- Keeps track of the 512 vertical lines that constitute one frame.
- Initiates readout from the delay lines when a line count of 16 has been detected.
- Initiates the start of horizontal retrace when a line count of 504 is decoded.
- Generates horizontal sync during line counts of 507, 508, and 509.
- Initiates horizontal blanking at a line count of 240 during right display.

The line counter (Figure 2-41), a nine-bit binary counter, monitors the vertical sweep lines on the CRT, initiates the display when a line count of 16 is detected in left display, controls the start of horizontal retrace and horizontal sync, and positions the display on the left or right side of the CRT. A nine-bit binary counter provides a maximum count of 512, which is equal to the number of vertical sweeps that make up one frame in a 960-character display. When the high-order bit trigger is cleared, the line counts are associated with the left half of the CRT (left display); line counts derived from the counter with the high-order trigger set are associated with the right half of the CRT

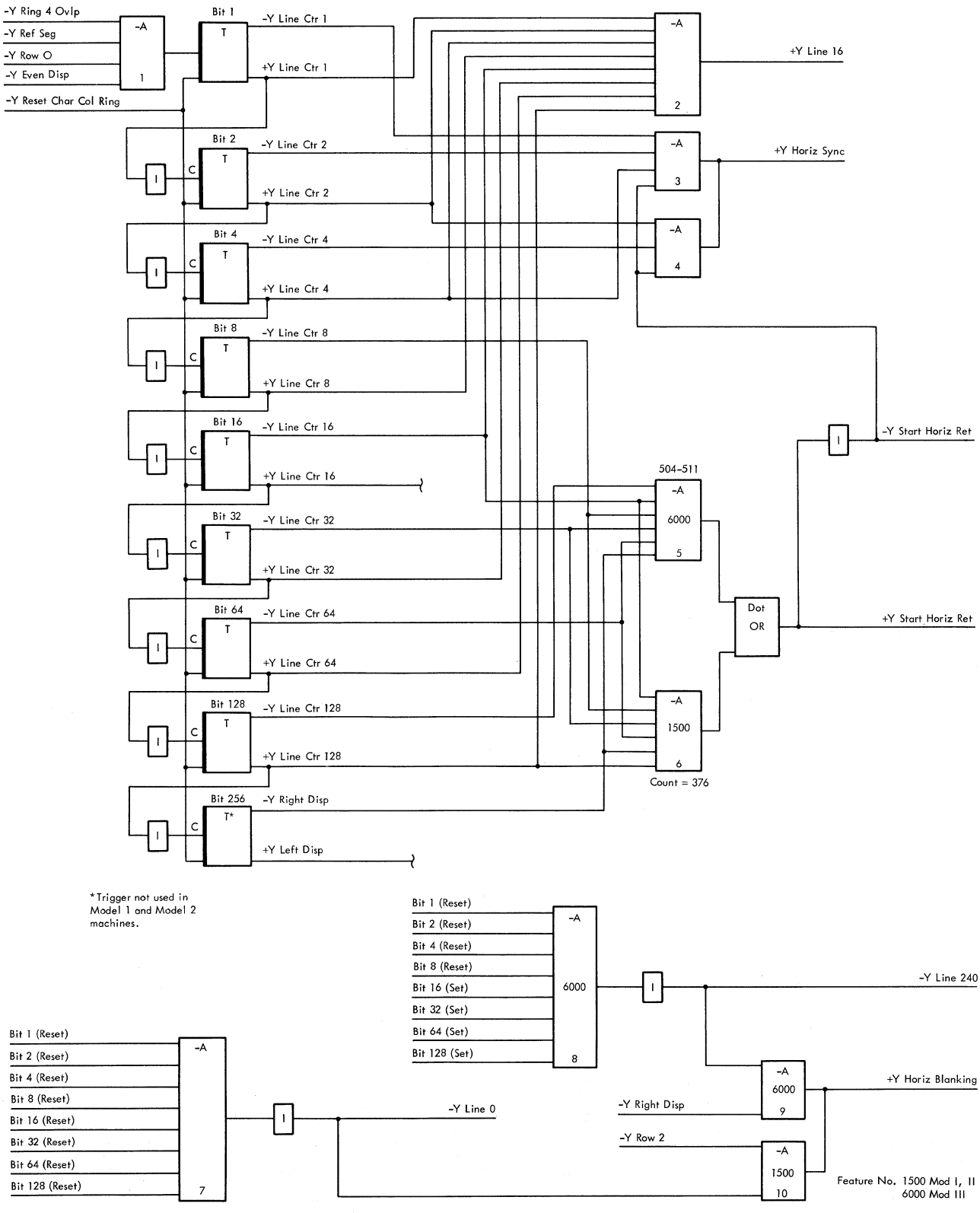


Figure 2-41. Line Counter

(right display). Information is displayed during 480 line counts, and the remaining 32 counts provide the necessary time to retrace the beam to the upper-left side of the screen. To center the display on the face of the CRT, 16 of the retrace line counts occur at the start and 16 at the right side of the viewing screen. A line count of 16 and left display (Bit 256 trigger cleared) initiates the first column readout. Since line 16 contains BCD information, it is not displayed on the CRT. Video display begins on line 17.

Figure 2-41 shows that the line counter is reset by the Reset Char. Col Ring signal. This reset signal is present whenever a Machine Reset level becomes active or during horizontal retrace time coincident with a line count of zero supplied by AND 7 and left display. The line counter is stepped when the input conditions to AND 1 are received during vertical retrace time. Each time AND 1 supplies an output, the counter advances one count. When the counter contains a count of 16 (AND 2 conditioned), buffer display is initiated for the even and odd display stations. Bit 256, when cleared, signifies that information from buffers 1 and 2 will be displayed in the upper-left or lower-left segments of the CRT; when the bit is set, information from buffers 3 and 4 will be displayed in the upper-right or lower-right segments. When AND 5 is fully conditioned at a line count of 504, the Start Horizontal Retrace signal is routed to the sync generation circuits.

NOTE: The Start Horizontal Retrace signal is generated at a line count of 504 for the 960-character display (Model 3). This signal is generated by AND 6 when line count equlas 376 for the 240- and 480-character displays (Models 1 and 2, respectively).

The output of AND 5 is also used to partially condition AND's 3 and 4, which develop the Horizontal Sync level when their additional inputs are received coincident with a line count of 504. AND 3 becomes fully conditioned at a line count of 507 to initiate the Horizontal Sync signal. Although AND 3 is deconditioned on the next successive line count, AND 4 maintains the Horizontal Sync signal for two additional line counts (line counts 508 and 507). In this manner, the Horizontal Sync signal remains on for the required three-line counts. Its use is described in greater detail in the paragraph titled "Sync Generator."

Other line counts decoded from the line counter to perform specific control functions are shown in the configuration comprising AND's 7 through 10. A line count of 240 permits the display to continue from buffer 3 for the 960-character display, thus eliminating the need for a line-16 search. A branch of the line-240 level with right display (inputs to AND 9) turns on horizontal blanking to prohibit video display during retrace time. AND 10 is used to generate the blanking for the 240- and 480-character display, which must be turned on at a line count of zero when only the Bit 1 through Bit 128 triggers are considered.

Sync Generator

- Generates composite sync signal composed of:
  1. Vertical sync
  2. Horizontal sync
- Provides horizontal blanking from the start of horizontal retrace until line 16 coincident with left display has been detected.

The sync generator circuit (Figure 2-42) generates vertical and horizontal sync pulses which are required to maintain the vertical and horizontal sweep circuits in the display stations in synchronization with video information emanating from the delay line buffers. The vertical sync pulses recur every 65.1 μs, whereas horizontal sync pulses recur every 33.3 ms. Vertical sync pulses abruptly terminate the vertical sweep multivibrator located in the display stations, thus allowing the electron beam to retrace to the top of the screen in preparation for the next scan. Horizontal sync pulses shift conduction of the horizontal multivibrator from one state to the other, thus causing the electron beam to retrace to the left side of the screen in preparation for the next frame. When horizontal retrace occurs, horizontal blanking is initiated to prohibit video information from being displayed on the CRT during retrace time. Horizontal blanking is terminated when line 16 coincident with left display has been detected. Composite sync signals derived from the Sync latch are routed to the video mixers, where they are interleaved with video data read out from the delay lines.

Vertical Sync Generation: The Vertical Sync pulse is generated by AND's 1 and 5 and the Sync latch shown in Figure 2-42. Note the feature numbers associated with each of the AND's which denote 2848 model applicability. AND's 1 and 5 are provided for display control Models 2 and 3; AND's 2 and 6 are used with the Model 1. The theory of sync pulse generation is similar regardless of the display model employed. AND 1 sets the sync latch during retrace time when the inputs to this AND are received. The Sync latch is reset by AND 5 at the

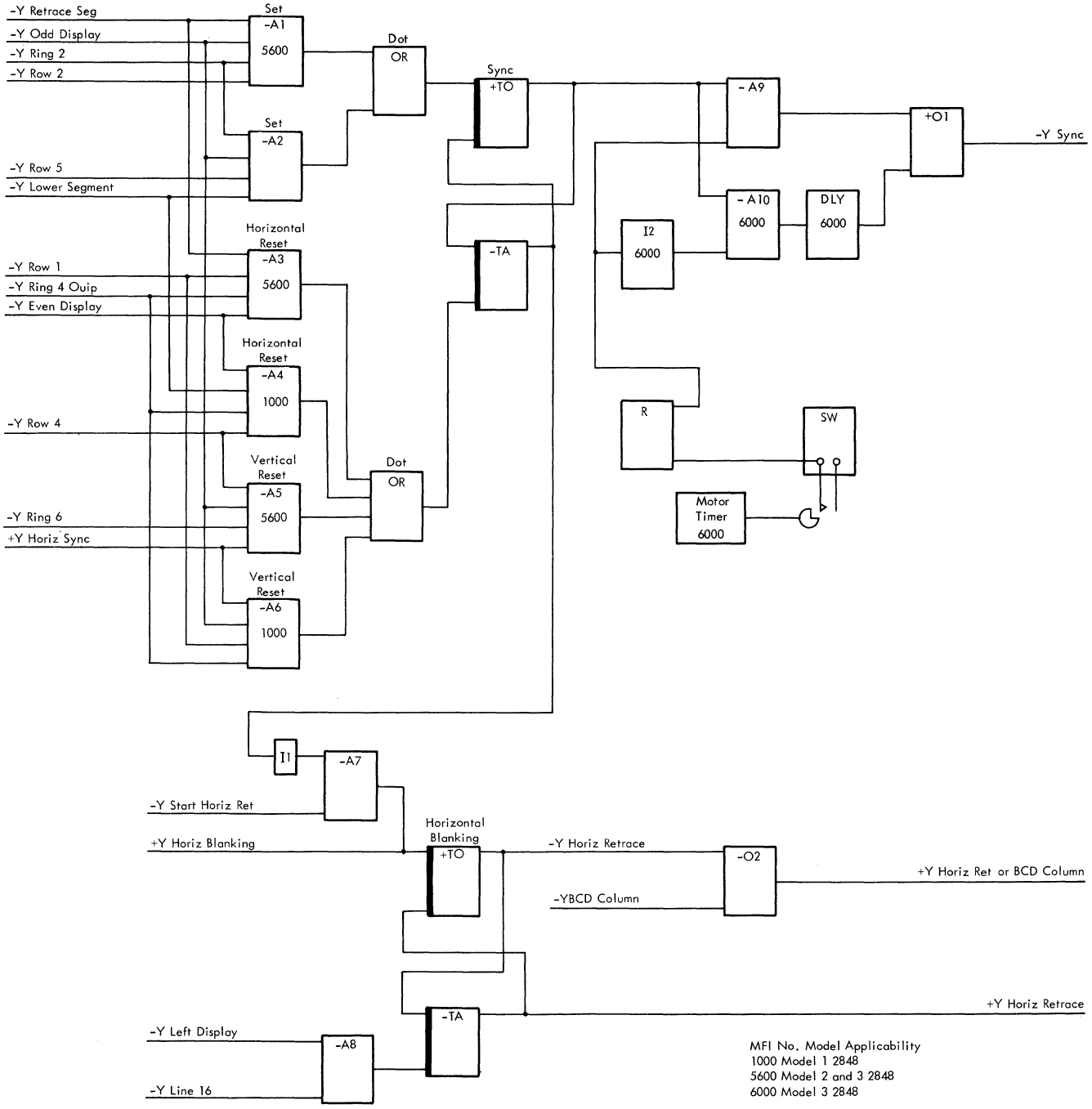


Figure 2-42. Sync Generator

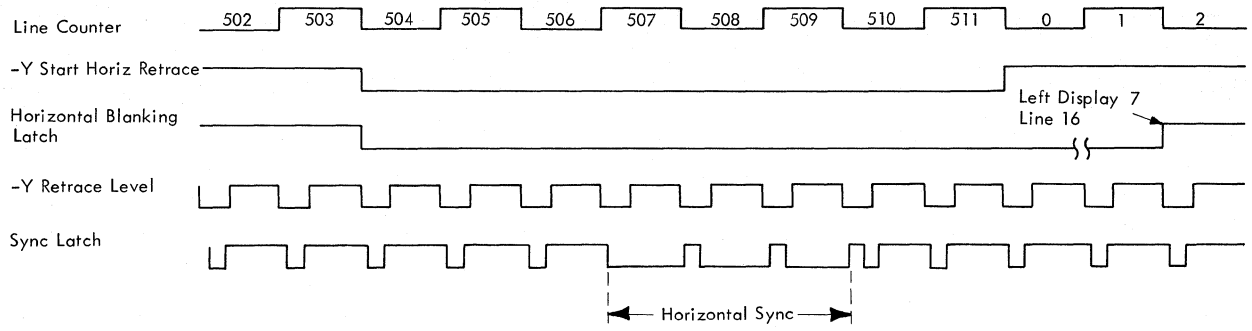


Figure 2-43. Sync Generator Timing

end of each line count (vertical sweep) except during those line counts when the horizontal sync is generated and the reset function of AND 5 is deconditioned by the +Y Horiz Sync signal. The Vertical Sync pulse that appears at the output of the Sync latch is approximately 4.54 μs wide. Vertical Sync pulses and their relationship to Horizontal Sync pulses are illustrated in Figure 2-43.

Horizontal Sync Generation: The Horizontal Sync pulse is generated by AND's 1 and 3 and the Sync latch (Figure 2-42) for Model 2 machines. Circuits applicable to display control Models 1 and 2 are also shown in the figure. AND 1 sets the Sync latch; the reset operation is performed by AND 3. The vertical reset AND (AND 5) is inhibited during generation of the Horizontal Sync by the +Y Horiz Sync level which deconditions the Vertical Reset AND's. Note that the reset conditions for horizontal sync occur later in time than those for vertical reset. This produces Horizontal Sync pulses of greater width than the Vertical Sync. The approximate pulse widths of both the Horizontal and Vertical Sync pulses are shown in Figure 2-44. Horizontal Sync pulses recur at a 30-cps rate for the 960-character display station (Model 1 Display Station) and at a 60-cps rate for the 240- and 480-character display stations (Model 2 Display Station).

Horizontal Blanking: Horizontal blanking is used to inhibit the display of video information during horizontal retrace time and during readout of BCD column information from the delay lines. The blanking level is supplied by the Horizontal Blanking latch or the -Y BCD Col signal shown in Figure 2-42 as inputs to OR 1. The output of OR 1 is routed to the video buffer selection circuits to prohibit video or BCD gating when horizontal blanking is active. Two conditions can set the Horizontal Blanking latch: when horizontal retrace is initiated and whenever the Horiz Blanking signal is received (present when the line counter contains a count of 240 coincident with right display).

NOTE: The +Y Horizontal Blanking signal becomes active at a line count of 0 for the 240- and 480-character displays (Models 1 and 2).

AND 8 terminates the horizontal blanking operation by resetting the blanking latch. This condition occurs when Line 16 and Left Display levels are supplied to AND 7.

Pulse	Pulse Width (μs)
Vertical Sync	4.54
Horizontal Sync	60.56

Figure 2-44. Sync Pulse Widths

Sync Pulse Delay Circuit

The sync pulse delay circuit (Figure 2-42), comprising the motor timer and switch, a resistor block, inverter I2, AND 10, and an adjustable delay circuit, is provided to extend the tube life of the P12 CRT. This is necessary because display stations attached to the Model 3 control unit employ CRT's with a P12 phosphor, and tube life expectancy is less than that in display stations (Model 2) which contain CRT's with a P4 screen.

The sync pulse delay circuit delays the transmission of synchronization pulses to the display stations to shift the 12 character rows displayed on the viewing screen approximately the height of a character. Thus, each character row is shifted and displayed one character position above its previous position. This technique makes use of the phosphor material between rows and increases CRT screen life by a factor of 2. The shift or sync pulse delay is effected every 8 hours of operating time.

The operation of the sync pulse delay circuit is directly related to the cam on the timing motor. As

the cam rotates, the switch associated with it is maintained closed or opened for 8 hours (operating time). Assume that the cam is in the position shown in Figure 2-42. In this position, the switch contacts remain open and the sync pulse delay circuit is inactive. As a result, the resistor block supplies a -Y level to AND 9 which gates the sync pulses (via OR 1) to the video mixers. Note that the sync pulses are not influenced by the delay circuit, and this condition is maintained for a 8 hour period. At the end of this period, the cam on the timing motor is rotated to close its associated switch contacts. The resistor block now supplies a +Y level to decondition AND 9. Note, however, that AND 10 is conditioned by the inverted level from I2. During this time period, sync pulses are delayed for a time span equal to the height of one row (character). A potentiometer is provided in the delay circuit so that the sync pulses can be delayed the amount required to shift the display upward the height of one character.

Reset Controls

- Reset levels are generated when the End Op latch is set at the end of each operation (by the host system) or when the RESET ERASE pushbutton is depressed on the CE panel.
- The system reset function originated by the computer or by the RESET ERASE pushbutton automatically erases all buffers and distributes reset signals to preset counters, registers, and latches throughout display control.

The reset controls circuit (Figure 2-45) generates and distributes reset signals, which clear or preset the various counters, registers, and latches within the control unit. This prepares the control unit to accept the next command or data transfer from the keyboard, local interface, or remote interface.

The End Op Reset signal is generated at the end of each operation, thus clearing and presetting all circuits (except counters) within display control in preparation for the next operation. If the End Op Reset signal occurs coincident with the Enter Cmd level, AND 1 provides the MI Sent pulse to indicate that the Attention bit has been set as a result of the Enter Cmd by the selected keyboard. Information stored in buffer associated with the keyboard initiating the Enter Cmd is read out by the computer at a later time. Further requests for entry by the same keyboard are inhibited until the previous Enter request has been honored.

A system reset (originated by the computer or by the RESET ERASE pushbutton) erases all buffers to all display stations by activating the 8-ms single-shot in addition to resetting all control circuits and counters. Selected display station erase functions are controlled by AND 2 and by the adapter associated with the address contained in the keyboard address register. After the 8-ms Erase single-shot times out and line 16 is found, EOM is written in the first character position on the screen for the display stations erased. When the EOM has been written on the erased display stations, the sequence is terminated with an End Op Reset.

TIC Sample Decoder

- The TIC sample is timed to detect TIC when it is in the Buffer Register trigger.
- TIC can be found within 16.5 ms.
- The TIC sample circuit complexity varies with the three 2848 models.
- The first bit position of every seven-bit byte in a BCD column must be sampled for TIC.

General

Each display adapter contains two TIC's, one for the even display and one for the odd. Each of these TIC's can be located in any one of the four buffers (B1, B2, B3, and B4) that form part of the adapter. In addition, a TIC is a single bit among the thousands of bits stored in the delay lines. TIC detection must be a precisely timed and highly selective operation. The purpose of the TIC sample decoder circuits is to generate a TIC sense level that occurs only when TIC could be in a predetermined location. The location selected was the Buffer trigger associated with each delay line. Remember that all data bits stored in a delay line are sequentially read from the delay line, shifted through the Delay Line Buffer and Register triggers, and, then, rewritten into the delay line or replaced by new data bits (write operation). The TIC passes through the Buffer trigger of the buffer in which it is located six times during each full cycle of the display (one horizontal sweep time of 33.3 ms). (See the explanation of Buffer Slot Layout for more details.) TIC remains in the Buffer trigger for 500 ns (as do all data bits) and is then shifted to the Register trigger, where it remains for an additional 500 ns. The Buffer trigger was chosen as the sample TIC location because detection of TIC when it is in the Buffer trigger provides enough time (750 ns) for a decision as to whether TIC is to be erased or rewritten.

The progression of bits through the Buffer and Register triggers is illustrated in Figure 2-28.

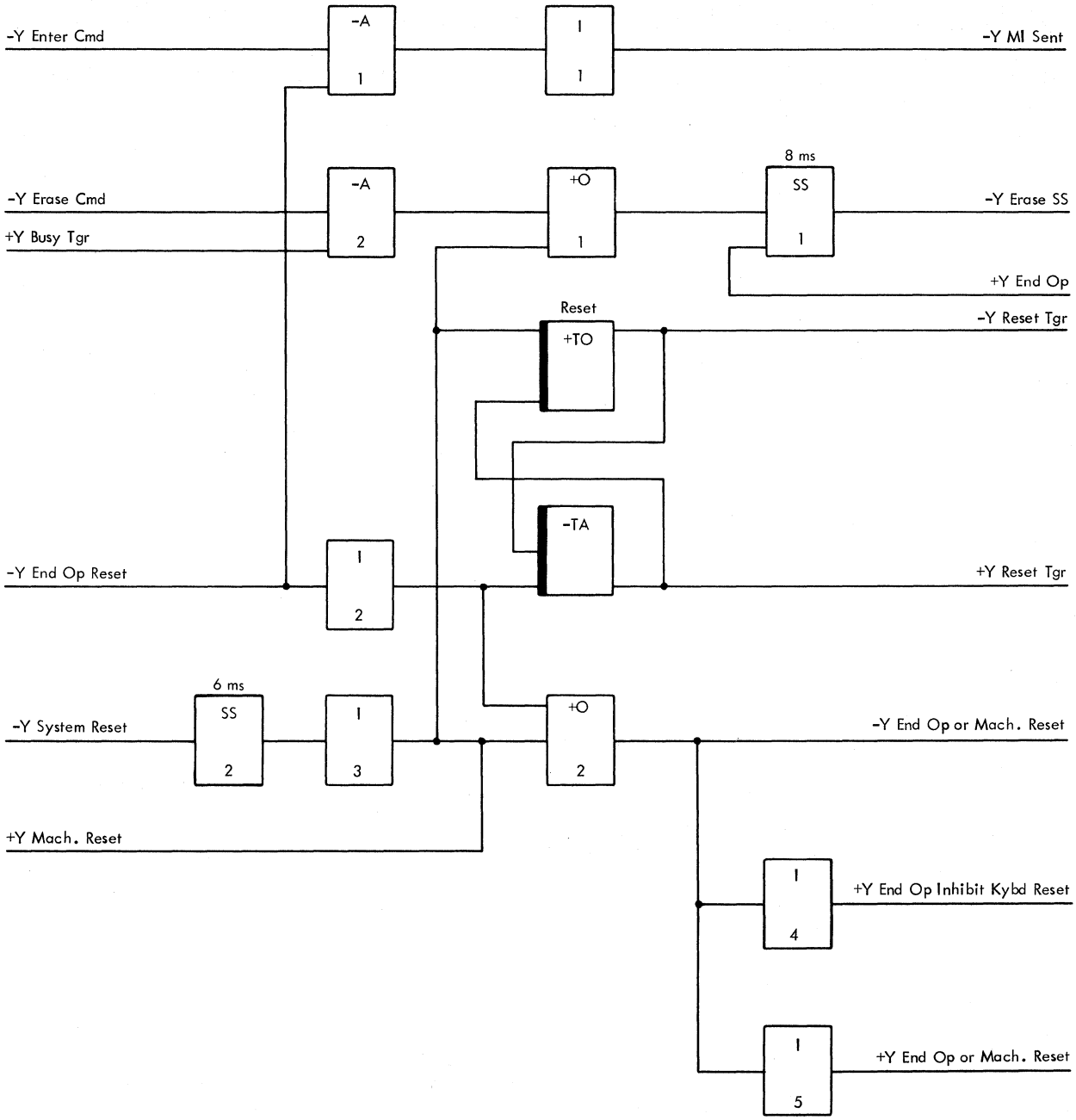
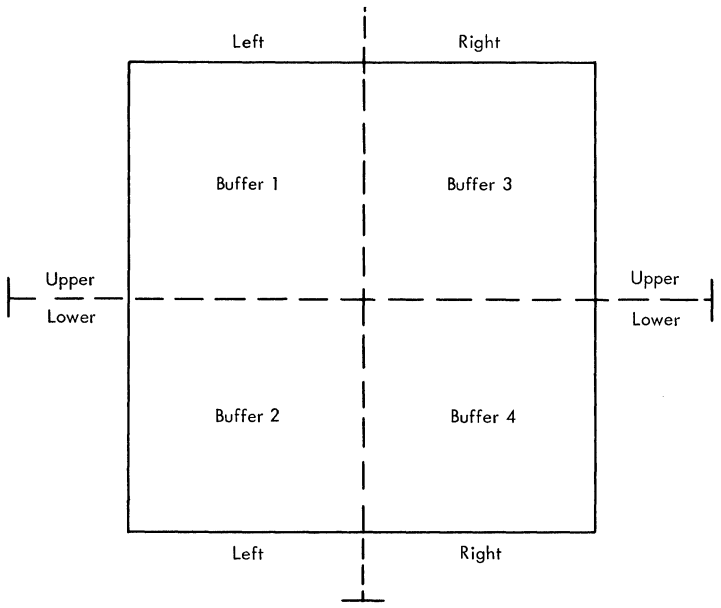


Figure 2-45. Reset Controls

As stated above, the TIC will be available in the Buffer trigger of one of the four buffers six times every 33.3 ms. Two of these times were selected as TIC sample times. Since the TIC can be located at two points within one complete display scan (or cycle) of 33.3 ms, the average TIC access time is reduced to 16.6 ms. Additional circuitry could have been included to permit the detection of TIC for any number of times that the TIC is available, up to the maximum of six. This was unnecessary because a TIC access time of 16.5 ms is adequate for all display operations and for the timely servicing of display stations associated with the control unit.

The various TIC sample times are illustrated in Figure 2-46. The TIC can be located in any one of the four buffers. Now consider the Sample-for-TIC-in-Buffer listing in the figure. Note that each buffer appears twice. The counter statuses associated with each buffer's entries describe the two specific TIC-sample times associated with each buffer.



Counter Status:	Sample For TIC in Buffer:
Left-BCD-Upper	1
Right-V4-Upper	1
Left-BCD-Lower	2
Right-V4-Lower	2
Right-BCD-Upper	3
Left-V2-Upper	3
Right-BCD-Lower	4
Left-V2-Lower	4

Figure 2-46. TIC Sample Time Decoding

A detailed analysis of the two buffer 1 sample times illustrates the derivation of the TIC sample times for all four buffers. In Figure 2-46, the first TIC sample time listed for buffer 1 is generated when the common control counters are set to left display, BCD column, and upper segment. With the counters in the status just described, the display is being serviced (supplied video) from buffer 1. The column counter indicates that BCD is being read from the delay lines. (BCD is not displayed as video.) The BCD column can contain the TIC; therefore, the bit 1 position of each seven-position BCD readout must be sampled for TIC. Note that the counter conditions necessary to sample TIC are present each time a BCD column is being read from the buffer 1 delay lines.

The second buffer 1 TIC sample time listed in Figure 2-46 reveals that the counters are set to right display, column V4, and upper segment when the TIC-sample is generated. Recall from the description of Buffer Slot Layout that there is a fixed relationship between the types of data, i.e., BCD, V1, V2, etc. being read from the various buffers. Remember also that data is being cycled through all buffers even though the output of only one buffer can be displayed at any one time. The counter status represented by right display, V4, and upper indicates that the contents of buffer 3 are displayed. Using the known fixed relationship between the data being read simultaneously from the buffers, it can be stated that when V4 data is being read from buffer 3 (right display, upper segment), BCD data is being read from buffer 1. Since buffer 1 BCD data is available in the buffer 1 Buffer trigger, buffer 1 BCD can be sampled for TIC at this time.

Thus, two times for the location of TIC in buffer 1 during the 33.3-ms duration of a complete display cycle are decoded to provide the desired 16.6-ms (maximum) TIC access time. In Figure 2-46, it can be seen that the two TIC sample times for buffers 2, 3, and 4 are derived in much the same manner as described above for buffer 1.

The complexity of the TIC-sample decoder varies with the three 2848 models. Since Model 1 has only a "buffer 1", a single sampling for TIC at BCD column time is adequate. Model 2 has buffers 1 and

2, so a search for TIC during BCD time, upper and lower segments, is all that is required. The Model 3, which has all four buffers, requires the most complex TIC-sample scheme, as has been described.

The remainder of TIC-sample decoder discussion is devoted to the detailed analysis of the decoder circuits for buffers 1 and 2. The circuits for buffers 3 and 4 are very similar; the differences are restricted to certain line names. Once buffer 1 and 2 TIC sample decoding is understood, the operation of the buffer 3 and 4 circuits should be equally clear.

Circuit Operation

The buffer 1 and 2 TIC Sample Decoder circuits are illustrated in Figures 2-47 and 2-29. The introductory information treated in the preceding paragraph should provide considerable insight into detail decoder operation. Therefore, the functions of various related logic circuits are summarized in Figure 2-48. Correlating the data in Figure 2-48 with both the information in the preceding paragraph and in Figure 2-47 will be helpful in understanding TIC sample decoder operation.

The significance of the inputs to AND's A3 and A4, which are all derived from the common control counters, has already been discussed. These AND's are conditioned each time the counters are equal to the AND's input conditions. The output of OR 2 is applied to AND's A6, A7, A9, and A12. Note that A6 is conditioned only when the segment counter is in upper segment and that A7 is conditioned during lower segment time. The inputs to A9 and A12 represent special TIC sample situations. Here, it is assumed that the vertical segment counter is in upper. Consider the inputs to AND 8, which generates the Ev TIC Time Bfr 1 Bfr Tgr level when conditioned. These inputs are as follows:

1. Output of A5: A5 is conditioned when the row counter is not at 6 and ring 5 occurs. Ring 5 was used because the TIC will be in the Buffer trigger during this timing interval. Remember that TIC was written into the delay line at ring 1 time with respect to the Buffer Register trigger. Here, since the sampling for TIC is done at the Buffer trigger, the timing reference must be moved back to compensate for the difference in the TIC location. This relation is illustrated below in conjunction with odd TIC sample time.
2. Output of A6: A6 is conditioned when the vertical segment counter is in the upper segment and BCD is being read from buffer 1 or 2 (OR 2).
3. Odd Disp Late: This signal is used to search for the even TIC with the same timing considerations as discussed in item 1. Since even-display time will not start until the TIC is in the Register trigger, the even TIC will be in the Buffer trigger during not-even time and, therefore, during part of Odd or Odd Disp Late time. The latter signal was used.

Thus, AND 8 is conditioned for a single bit time (ring 5) at precisely the time when the even-display TIC could be in the buffer 1 Buffer trigger.

AND 9 generates the Ev TIC Bfr 1 Bfr Tgr level required to detect an even TIC located in the first (or top) bit position of a BCD column. The inputs to AND 9 are as follows:

1. Output of OR 2, which indicates that BCD data is available in the buffer 1 Buffer trigger.
2. Output of AND 2, which represents the specific bit time that the first BCD bit is in the Buffer trigger. Note that ring 7 is used in place of bit 5. This change was necessitated by the presence of the even and odd check bits at the end of the slot. The end-of-slot conditions are illustrated in Figure 2-28. First consider the TIC sample at ring 5 during row counter 5 time odd. Note that ring 1 time (TIC in Register trigger) is two bit times to the right. Now, consider ring 5 during row counter 6 time. The bit in Bfr Tgr A at this time is the even check (85th) bit, which obviously cannot be TIC. The bit in Bfr Tgr A during ring 7 is bit 1, which could be an even TIC and is in fact the first bit of a column. Note also that the even and odd check times provide the normal interval (two bit times) for the shifting of TIC from the Buffer trigger to the Register trigger, where it must be at ring 1 time.
3. Ret Seg Late, which overlaps upper segment time and is used as an input in place of upper segment. At the time that the first BCD bit must be sampled for TIC, the vertical segment counter is just completing its transition from retrace segment to upper segment. Ret Seg Late was used as a gating level to avoid the effect of this transition on the TIC sample decoder circuits.

Thus, AND 9 performs the special function of searching for the one even TIC that is unique in respect to basic machine timing. In Figure 2-47, note that no such special AND circuit is required for sampling the odd TIC. Since the end-of-slot conditions (row counter at 6 and ring 7) occur only during odd-display and odd-display-late intervals, only an even TIC could be located in the first bit position of a BCD column. Remember that the TIC would have been written during even time and will be in the Buffer trigger only during an earlier (and therefore odd-display) time.

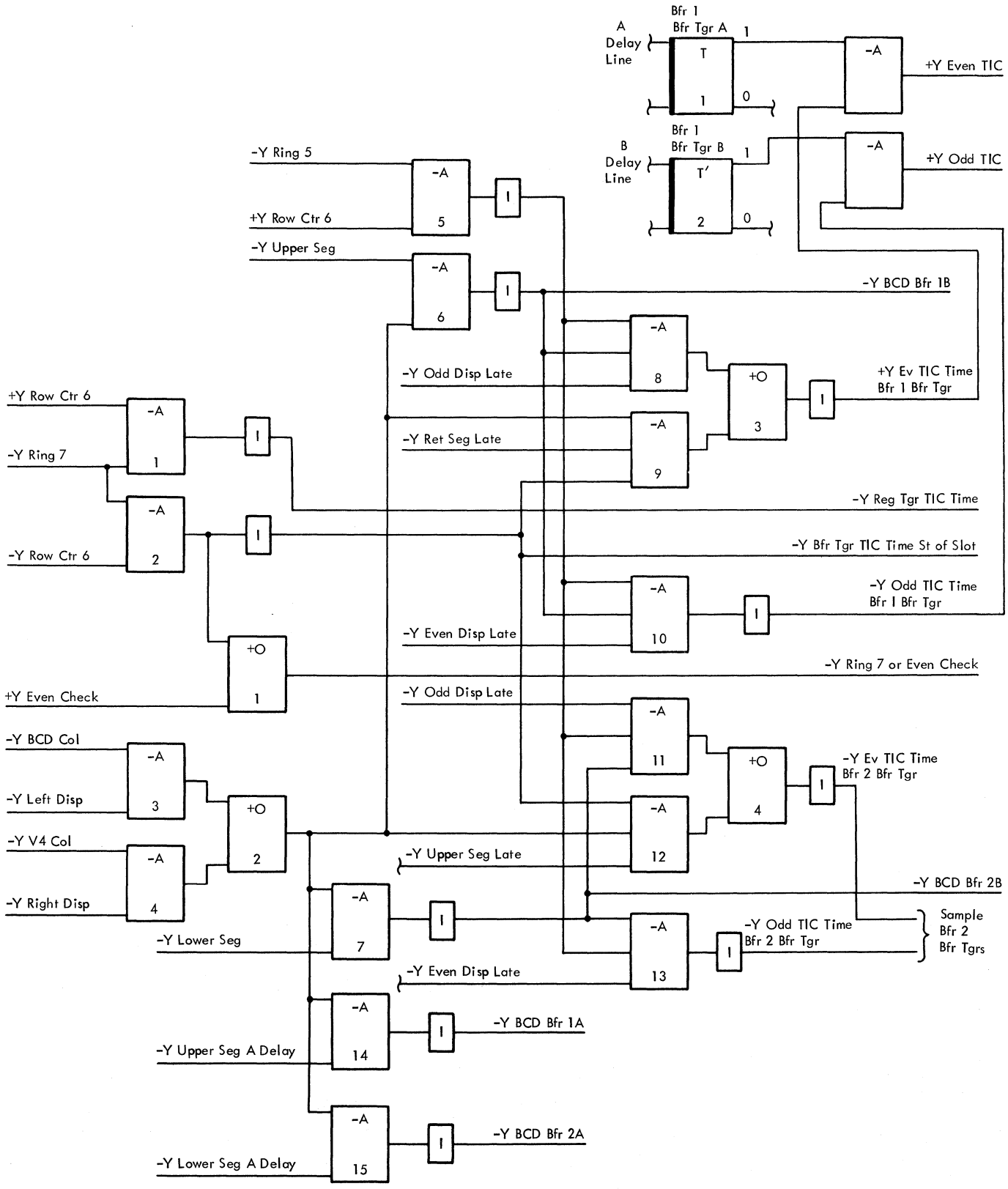


Figure 2-47. TIC Sample Decoding, Buffer 1 and 2

Circuit Group	Function When Conditioned
A3 and A4	Establishes broad TIC sample interval determined by when BCD is available in buffer 1 and 2 Buffer triggers.
A1	Indicates time that TIC is in Register trigger of buffer 1 or 2.
A2	Special time decode is used to sample for TIC in first BCD bit position after retrace or during a shift from upper to lower buffer.
A5 and A6	Decoded normal TIC sample timing. Note that ring 5 input to A5 limits the TIC sample level to one bit time.
A8	Generates buffer 1 even TIC sample for all row counts except row counter 6.
A9	Generates buffer 1 even TIC sample for special-case TIC detection during row counter 6 time.
A10	Generates odd TIC sample for all possible odd TIC locations.
A11	Same as A8, but for buffer 2.
A12	Same as A9, but for buffer 2.
A13	Same as A10, but for buffer 2.

Figure 2-48. Function of TIC Sample Decoder Circuit Groups

AND 10 generates the Odd TIC Time Bfr 1 Bfr Tgr level that is used to sample the buffer 1 Bfr Tgr B for the odd TIC. The inputs to AND 10 are identical with those already described for AND 8, except that Even Disp Late is used in place of Odd Disp Late. From the foregoing discussion it should be apparent that the odd TIC will be in Bfr Tgr B during even display time since it will be in Reg Tgr B during even-odd transition time. As described before, the search for TIC in the Buffer trigger represents a move backwards in time with respect to machine timing.

The TIC sample levels illustrated in Figure 2-47 for buffer 2 are generated as described for buffer 1. Note, in the figure, that A7 would be conditioned by Lower Seg and that AND 6 would be deconditioned during the buffer 2 TIC search. A special even TIC sample is generated for buffer 2 from AND 12 for reasons similar to those already described for the special function performed for buffer 1 by AND 9.

The TIC sample decoder circuits for buffers 3 and 4 are not illustrated, but they are very similar to those for buffers 1 and 2. The primary difference in the inputs to A3 and A4 determines BCD time. Essentially, these inputs would be as follows:

A3------BCD Col and Right Disp

A4------V2 Col and Left Disp

The use of the V2-BCD relationship for buffer 3 and 4 TIC sampling has already been discussed. TIC sample decoder operation for buffers 3 and 4 should be apparent from the associated ALD's (C9, 05.43.1 and 44.1).

BCD Gating Outputs

In Figure 2-47, note that the outputs labeled BCD Bfr 1B, BCD Bfr 2B, BCD Bfr 1A, and BCD Bfr 2A are generated during each BCD column time for their respective buffers. The levels are used within the adapters to gate BCD data from the Buffer Register triggers to the common buffer register and parity check circuits during read operations.

Character Generator Read Gate Generation

The preceding paragraphs demonstrate that TIC can be found when the character column ring counter is at other than BCD (V2 or V4). Consider the effect on the V1 through V5 read gates used to extract video data from the character generator. When TIC is found at BCD time, V1 through V5 can be read in direct relation to the V1 through V5 times of the character column ring counter; i.e., read V1 when character column ring counter equals V1 time. When TIC is found at V2 or V4 time, however, the video time essentially becomes BCD time. Then, all character column ring counter outputs must be used for other than their normal purpose, as shown in Figure 2-49.

The actual use-conversion of the character column ring counter outputs is accomplished with a set of AND gates associated with the position storage logic. The conversion gates are illustrated in Figure 2-76.

Display Addressing

General

The display addressing scheme permits the addressing and selection of any one of the 24 displays that can be associated with the 2848 control unit. The addressing logic also generates an identifying address that is transferred to the 2848 interface during an Enter command. A five-bit address is used, with the bit positions identified in the normal binary

Character Column Counter Outputs	Use as Character Generator Read Gates		
	TIC Found at BCD	TIC Found at V2	TIC Found at V4
BCD	BCD	V4	V2
V1	V1	V5	V3
V2	V2	BCD	V4
V3	V3	V1	V5
V4	V4	V2	BCD
V5	V5	V3	V1

Figure 2-49. Use of Character Column Outputs as Character Generator Read Gates

fashion of 1, 2, 4, 8, and 16. The two high-order bits (8 and 16) are used to select one of three groups of eight displays, i.e., 00-07, 08-15, or 15-23. The three low-order bits of the address are used to select one of the eight displays within the addressed group.

The addressing circuits consist of an address encoder, an address register, a display group address decoder, and a display address decoder. The address encoder is used to generate the required five-bit address from a single input which is the TIC associated with the addressed display. The display group address decoder uses the two high-order bits of the address to select one of the three groups of display addresses. Finally, the display address decoder uses the three low-order address bits to select one of the eight displays in a group. The outputs of the decoders are routed to the various display adapters and are used to select the circuits for the addressed display. The addressing circuits are illustrated in simplified form in Figure 2-50.

All display stations associated with a 2848 can be addressed from their respective keyboards (when provided) and from the channel via the 2848 interface logic. The address received from the interface consists of a complete five-bit address. Therefore, no address encoding is required, and the interface address is applied directly to the inputs of the address decoders. When a display is addressed from its keyboard, the five-bit address must be encoded from TIC, and other special provisions must be made.

Each area of the addressing circuits is discussed in the paragraphs that follow.

Address Encoder and Address Register

When a keyboard generates a request for service, the keyboard control circuits are activated and its TIC is located. This TIC signal is uniquely associated with a specific adapter and its even or odd display. Thus, the address circuits receive a "TIC" input for each keyboard associated with the 2848. In Figure 2-50, all of the 24 possible TIC inputs to the address encoder are represented. Typical of these is the Adapter 00 Even TIC. This signal indicates that the TIC found is associated with the even display serviced by adapter zero. Each TIC input to the encoder generates a unique five-bit address as shown in Figure 2-51. (The significance of the bit patterns in Figure 2-51 is discussed in conjunction with decoder operation.) When the TIC input is received by the encoder, the required latches of the address register are set (1-bits in Figure 2-51). Bit position 1 of the address is encoded in a special way. Note AND 6 in Figure 2-50. If the TIC is found during Even Disp Late time, it is known through machine timing relationships that the TIC is one for an odd display. Then, the AR1 latch is set. Even TIC's can be found only during Odd Disp Late. Thus, if an even display TIC is found, the Adr Reg 1 latch is not set. Adr Reg 1 is set for all odd displays and clear for all even displays. This is seen in Figure 2-51. Once the address has been encoded and the required latches of the address register have been set, the address register outputs are decoded.

When the ENTER key is depressed at the keyboard, the display address is encoded in the normal fashion, and the address register is set. The address register outputs are decoded to provide the usual display selection. However, since an Enter command has been issued, the contents of the address register are also transferred to the interface address register to identify the display entering the message.

Display Group Decoder

The display group decoder receives the outputs of the address register bits 8 and 16 latches as inputs. It also receives bits 8 and 16 of an interface display address as inputs. Decoder inputs from either source have an identical effect.

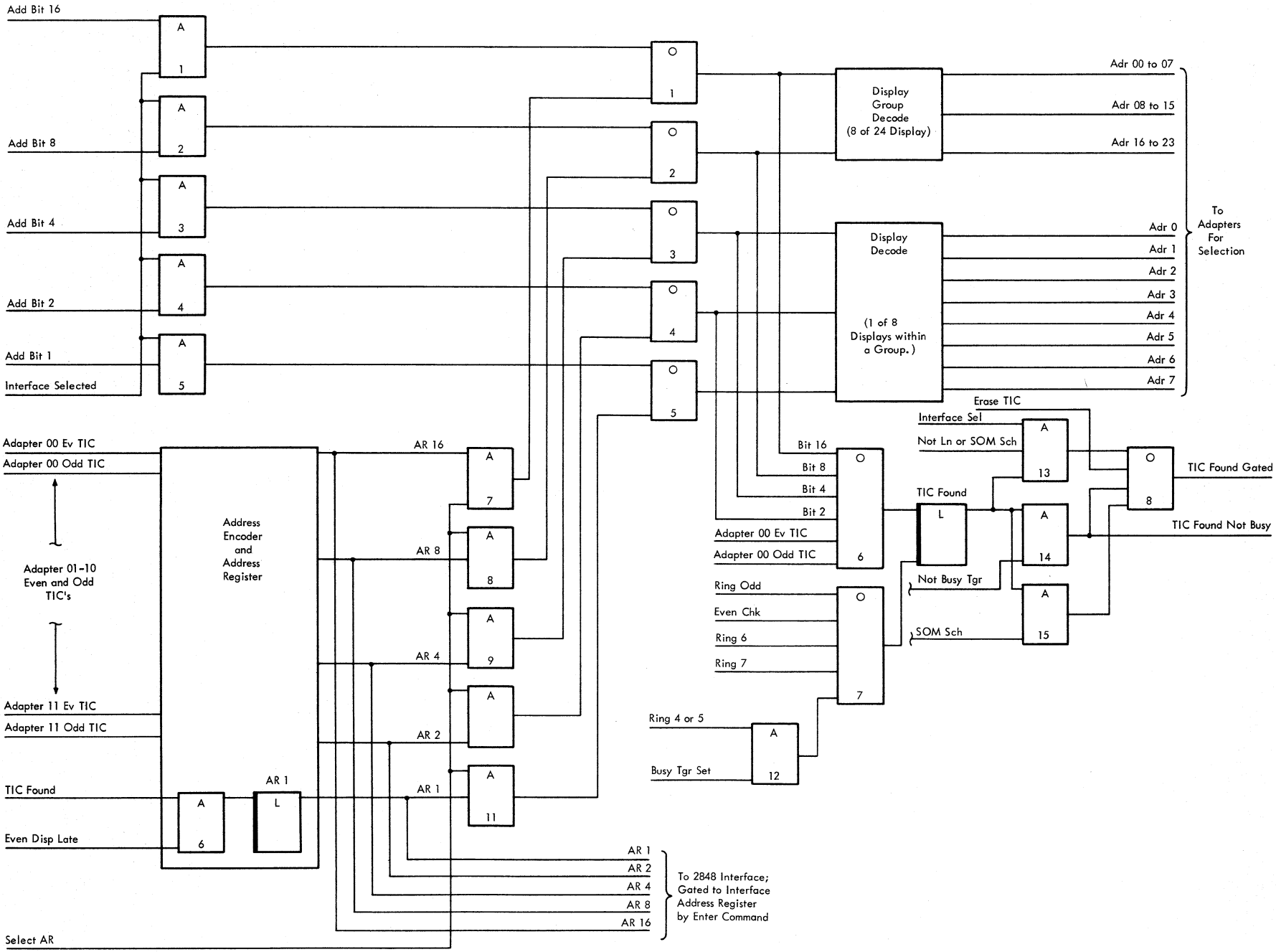


Figure 2-50. Display Addressing

Encoder Input	Address Register Output					Display Addressed
	AR1	AR2	AR4	AR8	AR16	
AD 00 EV TIC	0	0	0	0	0	00
AD 00 OD TIC	1	0	0	0	0	01
AD 01 EV TIC	0	1	0	0	0	02
AD 01 OD TIC	1	1	0	0	0	03
AD 02 EV TIC	0	0	1	0	0	04
AD 02 OD TIC	1	0	1	0	0	05
AD 03 EV TIC	0	1	1	0	0	06
AD 03 OD TIC	1	1	1	0	0	07
AD 04 EV TIC	0	0	0	1	0	08
AD 04 OD TIC	1	0	0	1	0	09
AD 05 EV TIC	0	1	0	1	0	10
AD 05 OD TIC	1	1	0	1	0	11
AD 06 EV TIC	0	0	1	1	0	12
AD 06 OD TIC	1	0	1	1	0	13
AD 07 EV TIC	0	1	1	1	0	14
AD 07 OD TIC	1	1	1	1	0	15
AD 08 EV TIC	0	0	0	0	1	16
AD 08 OD TIC	1	0	0	0	1	17
AD 09 EV TIC	0	1	0	0	1	18
AD 09 OD TIC	1	1	0	0	1	19
AD 10 EV TIC	0	0	1	0	1	20
AD 10 OD TIC	1	0	1	0	1	21
AD 11 EV TIC	0	1	1	0	1	22
AD 11 OD TIC	1	1	1	0	1	23

Figure 2-51. Address Encoder Outputs

The 8 and 16 address bits are used to select one of three groups of eight displays as follows:

Bit Status 8	Bit Status 16	Display Group Addressed
0	0	00-07
1	0	08-15
0	1	16-23

In Figure 2-51, note that 8 and 16 address bits do vary in the pattern described above.

Display Address Decoder

The display address decoder decodes the 1, 2, and 4 bits of the five-bit address either from the interface or from the keyboard (address register). Figure 2-51 illustrates how the binary bit configurations are made to represent display 0_{10} through 7_{10}; e.g., 010 equals display 2. In the figure, note that bits AR1, AR2, and AR4 assume a repetitive pattern within each of the three addressable groups of displays.

TIC Found Latch

The TIC Found Latch (Figure 2-50) is set when an address has been received from interface or when the address register is set as a result of an address encode. Note that the TIC Found latch is set whenever a 1-bit is present for address bit 2, 4, 8, or 16. All addresses except that for adapter 00 even and odd will cause at least one of these four address bits to be set (Figure 2-51). The TIC Found latch is set directly by Adapter 00 Ev TIC or Adapter 00 Odd TIC since these two addresses do not contain a 1-bit in bit positions 2, 4, 8, or 16.

The output of the TIC Found latch is gated through A13 (channel operation), A14 (keyboard operation), or A15 (Keyboard Enter command) and is used to store the TIC position in the position storage circuits. The TIC Found latch is on for a short duration and is reset as early as ring 6 time (OR 7). At A12 in Figure 2-50, note that the latch is reset at ring 4 or ring 5 if the Busy trigger indicates that common is unavailable. This reset occurs before TIC Found Gated is used to store the TIC position.

Write A and Write B Latches

- Control the gating of data to the A and B delay lines.
- The set and reset sequence of the Write latches is different for even-display and odd-display write operations.
- Write A and Write B latches are turned on 250 ns before they are actually used (to permit their output levels to stabilize).

The Write A and Write B latches are used to control the gating of data to the A and B delay lines. The A and B latches are set and reset in different sequences, depending on whether the even or odd display is being written. The Write latch sequences for the even-display and odd-display write operations are illustrated in Figure 2-52. The figure also shows the relation of A and B delay timing pulses and bit ring times with the Write latch outputs.

Figure 2-53, a simplified logic diagram of the write latches and the latch control circuits, shows that the Write A and B latches are set and reset under many conditions. This discussion of the operation of the latches applies to a seven-bit keyboard-originated write operation to either the odd of even display. Other, special operations are discussed only with respect to the set and reset of the latches.

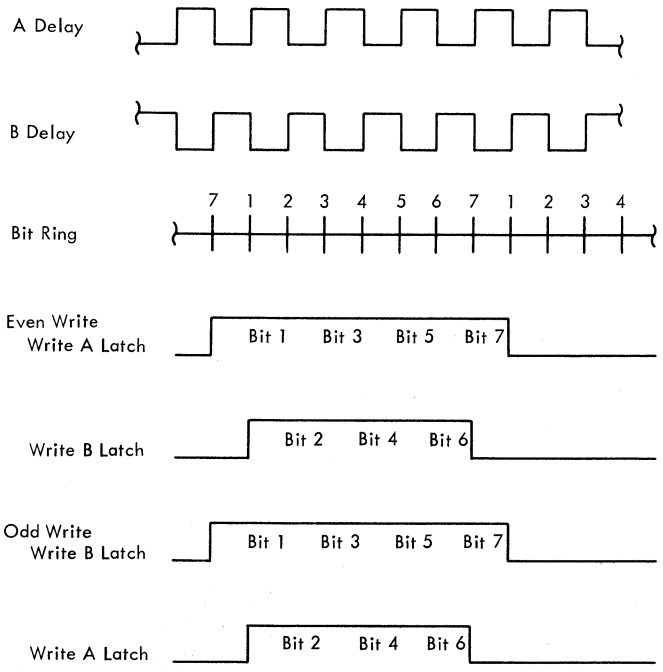


Figure 2-52. Write A and Write B Latches, Timing Chart

Keyboard Write Operation

As shown in Figure 2-53, the Set Write level (output of OR4) must be generated before the Write latches can be set initially. During a keyboard write operation, the Set Write condition is initially set upon receipt of the KYBD to CBR signal. This signal represents the transfer of the BCD character to the CBR. Its function here is to cycle the write latches so that the BCD character can be written into the delay lines of the selected buffer within the address adapter.

Once the Set Write level is present, the Write A and B latches set sequence is determined by whether the even or odd display served by the selected adapter is the object of the write operation. Assume here that the even display has been selected. The Write A latch is set first at Ring 1 Even (which starts at bit ring 7 time) through AND 19 (Figure 2-53). Then, at bit ring 1 time, the Write B latch is set (A14).

Figure 2-52 illustrates the setting of the Write A and B latches with relation to both the bit ring times and the A and B delay pulses, which gate data bits to the delay line as the BCD character is written. In the Even Write timing sketch, bit 1 is transferred in conjunction with the Write A latch and, thereafter, bits are written alternately with the B and A latches until all seven bits have been written. It is important that both Write latches are turned on well in advance (250 ns) of when they are first used to avoid problems with turn-on transients when gating data.

The Write latches are reset in the sequence shown in Figure 2-52 for an even write. The Write B latch is reset at bit ring 7 time (AND 17, Figure 2-53), and the Write A latch is reset at bit ring 1 time (+Y Ring Ctr 1 input, Figure 2-53).

At this point, only the BCD character has been written in the delay lines. The video character (V1-V5) must also be written; this requires five cycles of the Write latches. Since the Write latches are now reset, the Set Write level must be generated to recycle the Write latches. This is accomplished at AND 2. This AND is conditioned when the Write Char latch is set and a row, a display, and segment compare are made. Thus, the video is written in the delay lines, where it can be read in proper relation to the BCD character which has already been written.

The Write A and B latches are set and reset as described previously for writing the BCD. Thus, the video 1 (V1) byte is written in the delay lines. AND 2 is conditioned four more times to cycle the Write latches and cause video 2-4 to be written. Then, the Wrt Char input to AND 2 falls (Wrt Char Latch Reset) to terminate the character write operation.

Erase Operation

During an erase operation, the Set Write is generated by the conditioning of AND 1 each time that a display compare (odd or even) is made. Then, the Write A and B latches are set and reset as for a normal character write operation as shown in Figure 2-52. Since an erase is being performed, the seven bits written are all zeros. As AND 1 continues to condition on display compare and generate Set Write, the Write latches cycle so that the

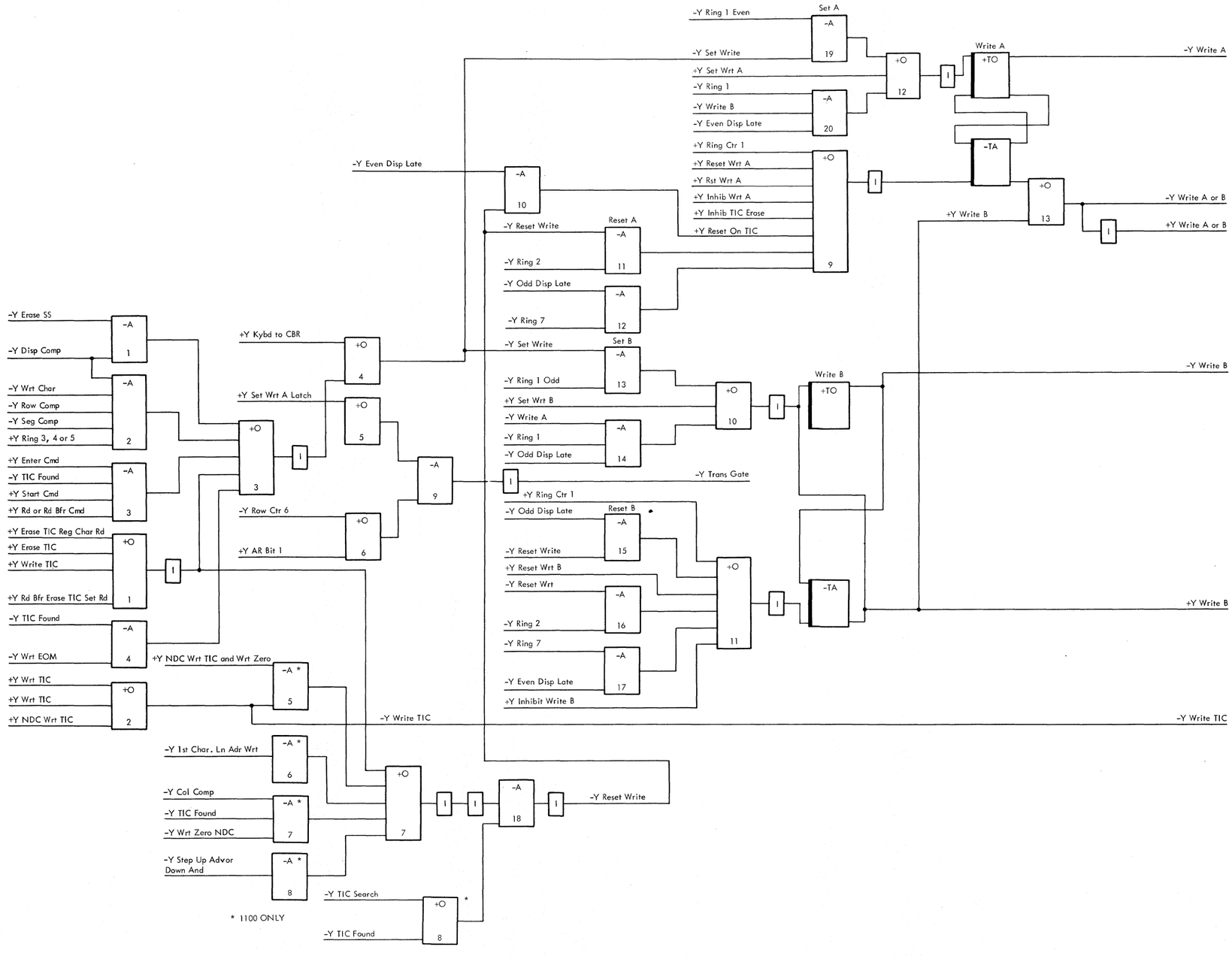


Figure 2-53. Write A and Write B Latches

selected-display buffers are erased (completely written with zeros). Write-latch activity stops when the 8.0-ms erase single-shot times out so that AND 1 is no longer conditioned.

Interface Write Operation

The operation of the Write latches during an interface write character operation is very similar to the keyboard write operations. The initial Write latch cycle is started when AND 3 is conditioned. The controlling input to AND 3 is TIC Found. When the TIC is found, AND 3 is conditioned to produce the Set Write level required to initiate Write latch operation. AND 1 also generates the Trans Gate through OR 5 to cause the input BCD character to be transferred from the character register (interface logic) to the common buffer register. Note that the AR bit 1 input to OR 6 is positive at this time to ensure that the Trans Gate is not inhibited.

As the Write latches cycle, the BCD character just loaded into the CBR is written in the selected delay lines. The Write latches set and reset as shown in Figure 2-52, the exact sequence depending on whether the odd or even display is being written.

Once the BCD character has been written, the five Write latch cycles required to write the video character are initiated through AND 2 exactly as described for the keyboard write operation. Write latch operation is also terminated in the same manner; i.e., the Wrt Char latch is reset.

TIC Write and Erase Operation

When the TIC is to be written, the Write latches must be on only long enough to permit a single bit (TIC) to be written at bit ring 1 time. When the NDC feature is present, the TIC is written as the first bit in a BCD byte that can contain the six-bit BCD code for any displayable character. This character BCD must not be affected by the Write TIC operation. Thus, the Write latches are controlled by OR 1 for the TIC operation. When OR 1 is conditioned, the Set Write condition is set through OR 3, and the Reset Write condition is set at the same time through Dot OR 7.

The Write latches respond to the Set Write level in the normal fashion for an even or odd write, as shown in Figure 2-52. As soon as bit 1 (TIC position) is written, however, AND's 11 and 16 are conditioned at bit ring 2 time, and the Write A and Write B latches are reset, thus terminating Write latch operation. This abbreviated Write latch cycle has permitted only the bit 1 position of a BCD location to be affected.

Write EOM (NDC Only)

When the NDC feature is installed, certain operations require that EOM (destructive cursor symbol) be written upon location of the TIC. In many respects, Write latch operation in this case is much like a normal keyboard character write operation.

The Set Write condition required to initiate Write latch operation is generated when AND 4 is conditioned. The conditioning of AND 4 indicates that TIC has been found, EOM is to be written, and the BCD code for the EOM character has been loaded into the CBR. The Write latches respond as shown in Figure 2-53 to permit the EOM BCD code to be written in the delay lines. As before, the Write latch sequence depends on whether an even or odd display write operation is in process. Once the BCD has been written, EOM video (V1-V5) is written by five Write latch cycles initiated by the conditioning of AND 2 (as described for keyboard character write operation). Write latch operation is terminated by the resetting of the Wrt Char latch, which prevents AND 2 from conditioning when the specified comparisons are made.

Other Write Latch Control Signals

Figure 2-53 also illustrates other, unique control signals that also affect the write latches. Discussion of these signals apart from the special functions with which they are associated would be of little value. The preceding discussion of the major Write latch operations should make the individual effects of these miscellaneous control signals on the Write latches apparent. For example, the input to AND 8 will cause Reset Write generation and, thus, Write latch reset at the next bit ring 2 time.

Serializer

The serializer accepts a seven-bit parallel input from the CBR and converts it into serial data for entry into the delay lines. The parallel data inputs from the CBR can represent character BCD or character video. The TIC can also be written through the serializer without CBR involvement.

The serializer is divided into two sections, A and B. Serializer A provides write inputs to the A delay line of the selected buffer; serializer B provides inputs to the B delay line. Data bits are written alternately to the A and B delay lines, starting with the A delay line for the even display and with the B delay line for the odd display. The division of the serializer into two sections makes it possible to start writing in the proper delay line

sooner and for a longer period. Writing the A and B delay lines alternately in a pattern ensures the proper data storage sequence.

The outputs of the serializer are gated by the Even, Odd, Even Late, and Odd Late signals in addition to ring pulses. Each signal requires some explanation before the actual operation of the serializer is discussed.

The timing relation of the Even, Odd, Even Late, and Odd Late signals with each other and with the ring pulses is shown in Figure 2-54. Each ring pulse is 250 ns wide; however, a 500-ns-wide gating pulse is required to ensure that the bit is written in the delay line. The required 500-ns pulse is provided for serializer operation by OR'ing two adjacent ring pulses. (The derivation of these double pulses will become apparent as serializer operation is discussed.) If the Even Disp and Odd Disp signals alone were used to gate data from the serializer, consider the situation at ring 7 time when the Even Disp and Odd Disp signals reverse statuses. The ring pulses OR'ed to produce the required 500-ns pulses are 7 and 1. However, since the transition of Even-Odd occurs during 7 time, the results of AND'ing ring 7 and 1 and Even Disp would not provide an uninterrupted 500-ns-wide data gate. It can be seen in Figure 2-54 that the Even Disp Late and Odd Disp Late signals reverse statuses each bit ring 4 time. Note that the Even Disp Late signal extends across the Even Disp to Odd Disp transition and that the Odd Disp Late extends across the Odd Disp to Even Disp transition. Thus, the Late signals are used as data gates to avoid the split-pulse situation that would exist if Even Disp and Odd Disp were used as data gates during bit ring 7 and ring 1 times.

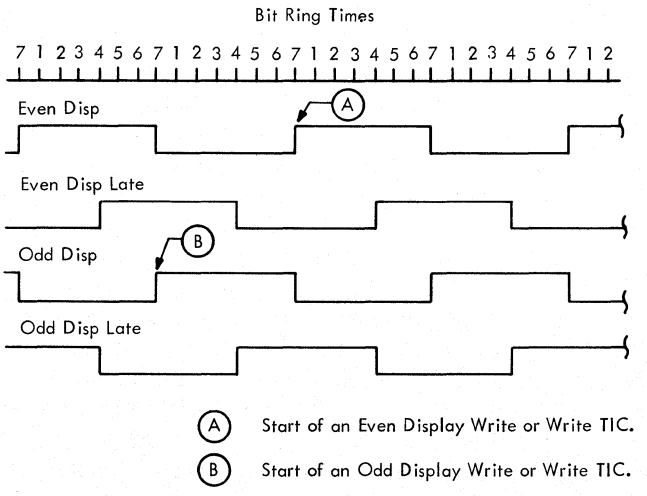


Figure 2-54. Even and Odd Display Signals, Timing Chart

Serializers A and B are illustrated in Figures 2-55 and 2-56, respectively, in simplified form. The serializers are not discussed separately since both are active in both even and odd display write operations. Instead, the overall operation of the serializers is discussed with particular attention to the interplay between them.

Write Data Operation

Whenever the CBR contains data, the CBR contents are sensed and processed by the serializer; however, unless the control logic is set to enable the write delay line operation, the serializer outputs are not used. When a write operation is being performed, the serializer outputs are gated through the control logic, and the serial data is entered in the delay lines.

In Figures 2-55 and 2-56, note that CBR bits 1 through 7 are fed to a set of AND circuits in both the A delay and B delay serializers. These inputs are directly from the CBR latches and are not conditional. Each of these AND circuits also receives a dual bit ring pulse as an input. The origin of these dual (500-ns) pulses is shown by the set of OR circuits in Figure 2-55. Note that each OR circuit is conditioned by two successive bit ring pulses. Therefore, the OR output is conditioned for two bit ring times (500 ns).

Each CBR data AND circuit also receives an output from the Even-Odd trigger (Even Disp or Odd Disp) or from the Even-Odd Late trigger (Even Disp Late or Odd Disp Late). (The relationship of the Disp and Disp Late signals has already been discussed.) Figure 2-57 is a summary of the inputs to the A delay and B delay serializer AND circuits. Now, consider how the delay lines are written. The important facts to remember are:

1. Data bits are written alternately in the A and B delay lines.
2. Delay line A receives the first bit when the even display is being written.
3. Delay line B receives the first bit when the odd display is being written.

With these facts in mind, examine the entries in Figure 2-57. When the even display is being written, the operation is initiated in part by the Ring 1 Even pulse so that the first bit written is CBR bit 1 from the serializer A delay. This bit is written in the A delay line. The second bit written is CBR bit 2 from the serializer B delay to the B delay line. The remainder of the even display bit sequence from the serializer is illustrated by the solid line connecting the serializer A and B delay sides of Figure 2-57. The bit sequence for the odd display write is shown with a dashed line.

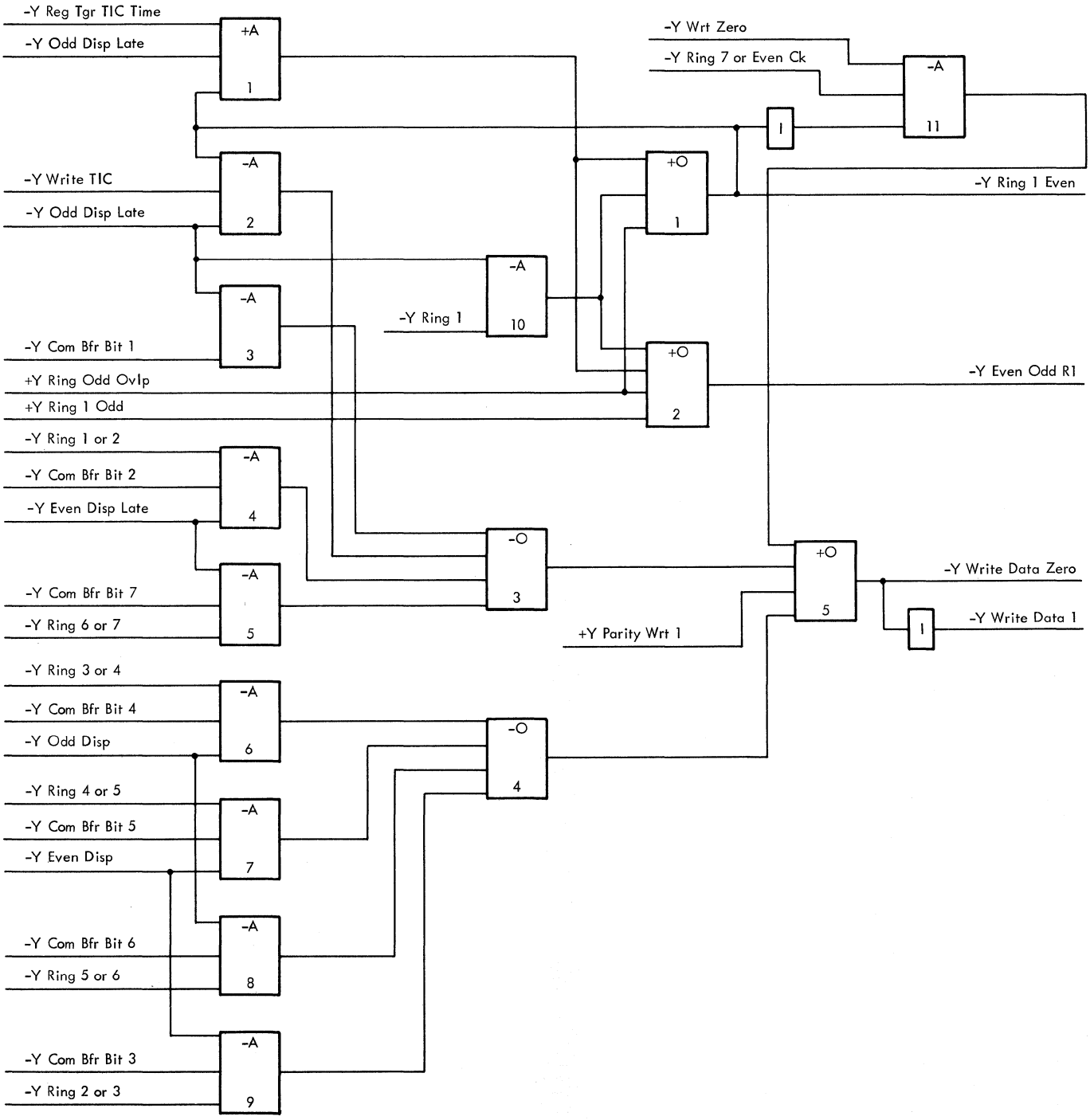


Figure 2-55. Serializer, A Delay

It can be seen that even and odd display bit sequences are similar. Therefore, the remainder of this discussion is limited to examining only the even display write in further detail.

The Disp and Bit Ring Pulse conditioning signals used to gate the even display write are as follows when extracted from Figure 2-57 (using the path of the solid flow line):

CBR Bit	Disp Signal	Bit Ring Pulse
1	Odd Late	1 Even (7 and 1) (Write TIC)
2	Odd Late	1 or 2
3	Even	2 or 3
4	Even	3 or 4
5	Even	4 or 5
6	Even	5 or 6
7	Even Late	6 or 7

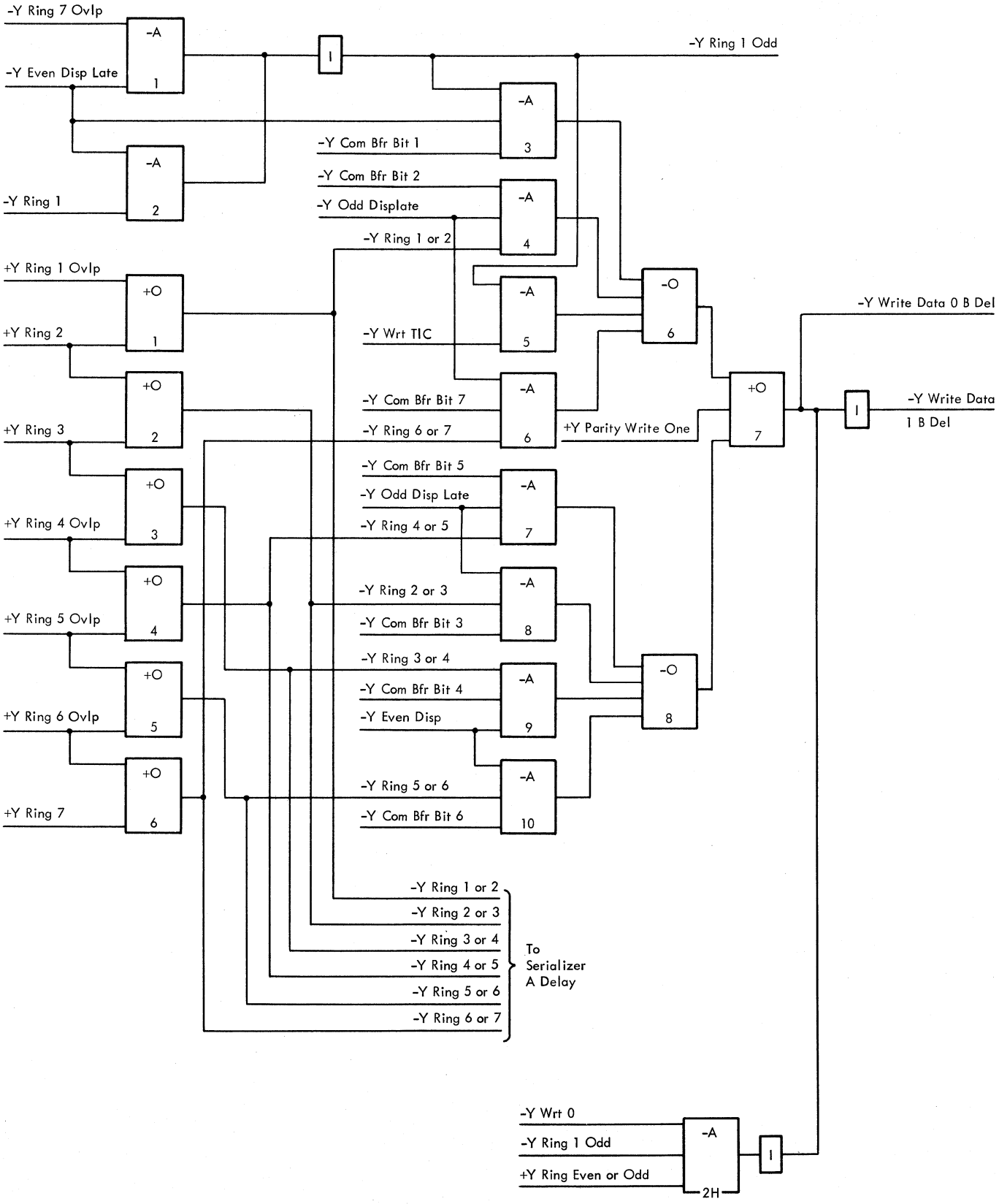


Figure 2-56. Serializer, B Delay

Serializer A Delay			Serializer B Delay		
CBR Bit	Display	Bit Ring Pulses	CBR Bit	Display	Bit Ring Pulses
1	Odd Late	1 Even (7 and 1)	1	Even Late	1 Odd (7 and 1)
2	Even Late	1 or 2	2	Odd Late	1 or 2
3	Even	2 or 3	3	Odd	2 or 3
4	Odd	3 or 4	4	Even	3 or 4
5	Even	4 or 5	5	Odd	4 or 5
6	Odd	5 or 6	6	Even	5 or 6
7	Even Late	6 or 7	7	Odd Late	6 or 7

Even Display Write Bit Sequence
Odd Display Write Bit Sequence

Figure 2-57. Serializer Data and Inputs and Even-Odd Bit Sequences

The reason for this signal selection pattern can be explained with Figure 2-54. Note that the Odd Disp Late signal is conditioned at bit ring 4 time. The first bit (CBR 1) is not gated from the serializer until ring 1 even time. Since ring 1 even is the result of OR'ing bit rings 7 and 1, it can be stated that ring 1 even starts at bit ring 7 time. Thus, in Figure 2-54, the start of the even display write operation is shown by the point labeled A. Point A reflects the conditions listed above for the gating of CBR bit 1 for an even display write (Odd Display Late and Ring 1 Even, which starts at ring 7 time).

As the remainder of the CBR bits are transferred from the serializer for an even display write, note the progression of the Disp signals listed above and the status of the signals in Figure 2-54. The use of Odd Disp Late, Even Disp, and Even Disp Late, in that order, provides a steady conditioning level. The use of Odd Disp Late for the first two bits bridges the transition from Odd to Even Disp, which occurs between bit ring 7 and ring 1 time. Similarly, the use of Even Disp Late bridges the transition from Even to Odd Disp at the following transition. Thus, each bit is gated from the serializer for a full 500 ns.

Write TIC Operation

The odd and even TIC's are also written through the serializer. In Figure 2-56, note AND 5 which has -Y Wrt TIC as an input. The other inputs to the AND show that the TIC is written upon Even Disp Late and Ring 1 Odd, representing the first bit position of a byte area within the delay line. Note that the odd TIC is always written in the B delay line. As with the data write operation, Even Disp Late is used in conjunction with Ring 1 Odd (bit ring 7 and 1) as the write TIC gate so that the full 500-ns pulse required to write the delay line is provided. With the destructive cursor, TIC is written in conjunction with write EOM.

AND 2 in Figure 2-55 illustrates a similar configuration for writing the even display TIC in the A delay line.

Other Write Operations

The +Y Parity Write One input to OR 9 in Figure 2-56 illustrates the way in which the slot parity bit is written. Note that the +Y parity signal is inverted so that a -Y Write Data 1 B Del is generated. Figure 2-55 also illustrates the path through which a parity 1-bit can be written via the serializer.

AND 11 in Figure 2-56 and AND 11 in Figure 2-55 illustrate the way in which a stream of zeros can be written in the delay line when the Write Zero latch is set (-Y Wrt Zero). Note that both AND's are held deconditioned during parity checks (+Y Ring Even or Odd at AND 11, Figure 2-28; and Not Ring 7 or Even Ck at AND 11, Figure 2-27). Note also that the Ring 1 Odd and Ring 1 Even pulses are used to synchronize the operation so that the zeros will be written starting at a "byte" location within the delay line.

Deserializer

During a read operation, serial BCD data is extracted from the A and B delay lines and transferred to the CBR. At the CBR, this serial data is reassembled (deserialized) into a six-bit byte that can be transferred to the channel as a parallel byte of read data. The actual deserialization is accomplished at the AND gates used to load the latches of the CBR. Remember that only bit positions 2-7 of the CBR are loaded with BCD data from the delay lines during read operations. CBR bit position 1 is not used since the first bit of BCD data is always a

possible TIC location and is not associated with the six-bit BCD character code.

Figure 2-58 lists the combinations of conditions that are used to load the latches of the CBR. Although bit 1 is not loaded as part of the deserialization, the appropriate ring time and even-odd signals are included in the table to provide a complete picture of the timing sequence. Recall from the discussion of the Write A and Write B latch operation that the A delay line is always written first for the even display. Conversely, the B delay line is written first for the odd display. Obviously, the delay lines must be read in the same order, i.e., A first for even, B first for odd. Now, use Figure 2-58 to visualize an even display read operation. (It is assumed here that BCD data is properly gated from the A and B delay line register triggers and that a read operation is in progress.) Once conditioned, the Even Disp level remains so for a full cycle (ring 1-7) of the bit ring counter. Note, in Figure 2-58, the order in which bits are gated into the CBR when Even Disp is conditioned:

CBR Bit	Loaded From (Delay Line)
1	Not loaded
2	B
3	A
4	B
5	A
6	B
7	A

Though associated with the even display in the role of a possible TIC location, bit 1 is not loaded in the CBR. Actually, this bit is still read from A delay first for the even display read, but it is not gated to the CBR. Thus, the bits are read from the delay lines in the desired order. After ring 7, all six bits of the BCD code have geen written in the CBR and are available for parallel transfer to the channel via the 2848 interface.

Figure 2-58 illustrates a similar situation for read operations involving the odd display. As before, bit 1 (possible odd TIC) is read from the B delay line in conjunction with ring 1 but not gated to the CBR. Thereafter, bits are read alternately from the A and B delay lines so that the odd display BCD byte is assembled correctly in the CBR.

Note, in Figure 2-58, that the Even Disp Late and Odd Disp Late are used to gate bit 7. These signals were chosen to avoid the transients resulting from the changeover from even to odd, or from odd to even, at ring 7 time. No such measures were required for bit 1 because the first bit actually used is bit 2. This situation affords a full bit time for the even-odd display signals to stabilize before they are used to gate data into the CBR.

Common Buffer Register

The common buffer register (CBR) (Figure 2-59) consists of seven latches and functions as the central point for accepting and distributing data between the interface and display control. Transfer of data into and out of the CBR is controlled by and dependent upon the operation to be performed. When the transfer has been completed, the CBR is reset to prepare it for the next transfer. Specifically, the CBR is employed for data exchanges between the following areas:

1. Interface to delay lines.
2. Delay lines to interface.
3. Keyboards to delay lines.
4. Delay lines to 1053 Printer buffer.
5. Interface to 1053 Printer buffer.

Common Buffer Register Inputs

The CBR can be loaded from five sources: sense amplifier (character generator), end of message (EOM) circuits, keyboards, interface (character register), and the delay lines. CBR bit positions

Conditions Required to Load CBR Latches			Conditions Required to Load CBR Latches			CBR
Ring	Even or Odd Disp	Delay Line Data Source	Ring	Even or Odd Disp	Delay Line Data Source	Bit Loaded
1	Even Disp	A*	1	Odd Disp	B*	*
2	Odd Disp	A	2	Even Disp	B	2
3	Even Disp	A	3	Odd Disp	B	3
4	Odd Disp	A	4	Even Disp	B	4
5	Even Disp	A	5	Odd Disp	B	5
6	Odd Disp	A	6	Even Disp	B	6
7	Even Disp Late	A	7	Odd Disp Late	B	7

*Bit 1 is not loaded from A or B delay lines. Entries shown for timing purposes only.

Figure 2-58. Deserialization of Delay Line Data at CBR Inputs

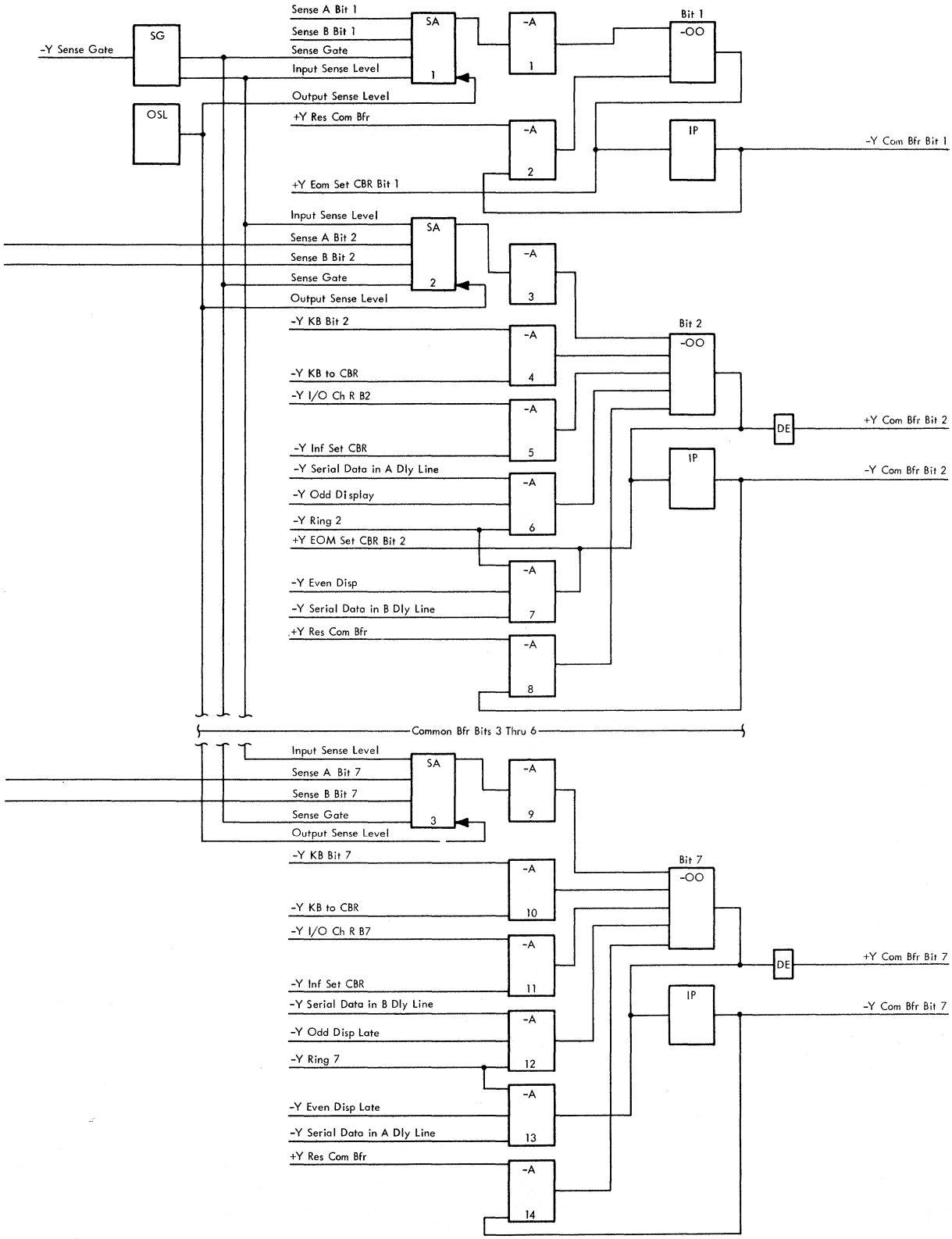


Figure 2-59. Common Buffer Register

associated with each source input are listed in Figure 2-60. Each input is described in the following paragraphs.

Source Inputs	Common Buffer Bit Positions
Sense Amplifiers	1,2,3,4,5,6, and 7
End-of-Message (EOM)	1*,2,4, and 6
Keyboards	2,3,4,5,6, and 7
Interface (Char Reg)	2,3,4,5,6, and 7
Delay Lines (A or B)	2,3,4,5,6, and 7
Reset	1,2,3,4,5,6, and 7

*Bit 1 is not used for TIC search or print command operations.

Figure 2-60. Common Buffer Register Input Signals

Sense Amplifier Inputs: The sense amplifier inputs transfer data from the selected cores in the character generator core plane to CBR bit positions 1 through 7. These inputs are provided whenever video data readout takes place or code conversion is necessary.

End of Message Inputs: The end of message (EOM) inputs condition CBR bit positions 1, 2, 4, and 6. The EOM symbol is also the destructive cursor symbol in machines that contain the destructive cursor feature.

Keyboard Inputs: Keyboard-initiated data from any of the display stations supply coded information to CBR bit positions 2 through 7. After keyboard data inputs are converted into video data and stored in the delay lines, the data is displayed on the CRT.

Interface Inputs: Interface inputs derived from the character register provide coded inputs to CBR bit positions 2 through 7. The coded inputs are translated into video signals or converted into the required code necessary to operate the addressed device.

Delay Line Inputs: Delay line inputs (A and B) provide inputs to CBR bits 2 through 7. These inputs, composed of BCD data, are used for control functions or data transfers to the interface or the printer.

Reset Inputs: The reset lines shown in Figure 2-59 clear all CBR latches to prepare them for the next load-data operation.

Common Buffer Register Outputs

The CBR outputs are routed to one of five possible destinations, depending upon the operation being performed. The possible destinations are:

1. Character generator decoders.
2. Data decode circuits (sense for SOM, EOM or new line (NL) codes).
3. Serializers.
4. Character register (interface transfer).
5. Printer buffer.

Register Control

In its role as the center of all internal data transfers, the CBR is involved in almost all control unit operations. This CBR involvement is described within the flow charts provided in the Maintenance Diagram Manual for the various machine operations. This section describes only the manner in which data entry from the keyboard and from the channel is controlled. The two control networks discussed affect only the CBR and are valid for all keyboards and channel data-entry operations.

The circuits discussed are illustrated in Figure 2-61, which also illustrates the input network of the Char Gate latch and the CBR reset network. The simplified diagram can be used to analyze and correlate events shown in the flow charts.

During a keyboard write operation, the CBR must be reset and then loaded with the BCD input generated from the keyboard. The reset applicable to the keyboard write operation is represented by A19 in Figure 2-61. The CBR is reset as soon as the TIC is found. The CBR set operation is then accomplished through OR 4, which can be conditioned by the output of A7 or by the KYBD-to-CBR signal. Note the KYBD Bit 1 input to A7. Keyboard commands are accompanied by a 1 in the bit 1 position. Thus, when a keyboard command is issued, A7 is inhibited, and the command byte is not transferred to the CBR. The KYBD-to-CBR input to OR 4 occurs as a result of a Start command from the keyboard. When a Start command is issued, an SOM search must be conducted because only one start symbol can be present on the display. After this SOM (start symbol) search has been conducted, the "write start symbol" command can be honored. Then, the +Y KYBD-to-CBR signal is generated in conjunction with write SOM. This gates the start symbol code from the keyboard logic to the CBR so that the symbol can be written.

The set CBR occurring as a result of the conditioning of A7 represents the acceptance of noncommand bytes from the keyboard. Note that the +Y Erase Cmd input inhibits the acceptance of any data from the keyboard while an erase operation is being performed.

During an interface write operation, the CBR is reset through A19 (Figure 2-61) when the TIC is found. The CBR is initially loaded through A14 to load the character BCD into the CBR. As the write

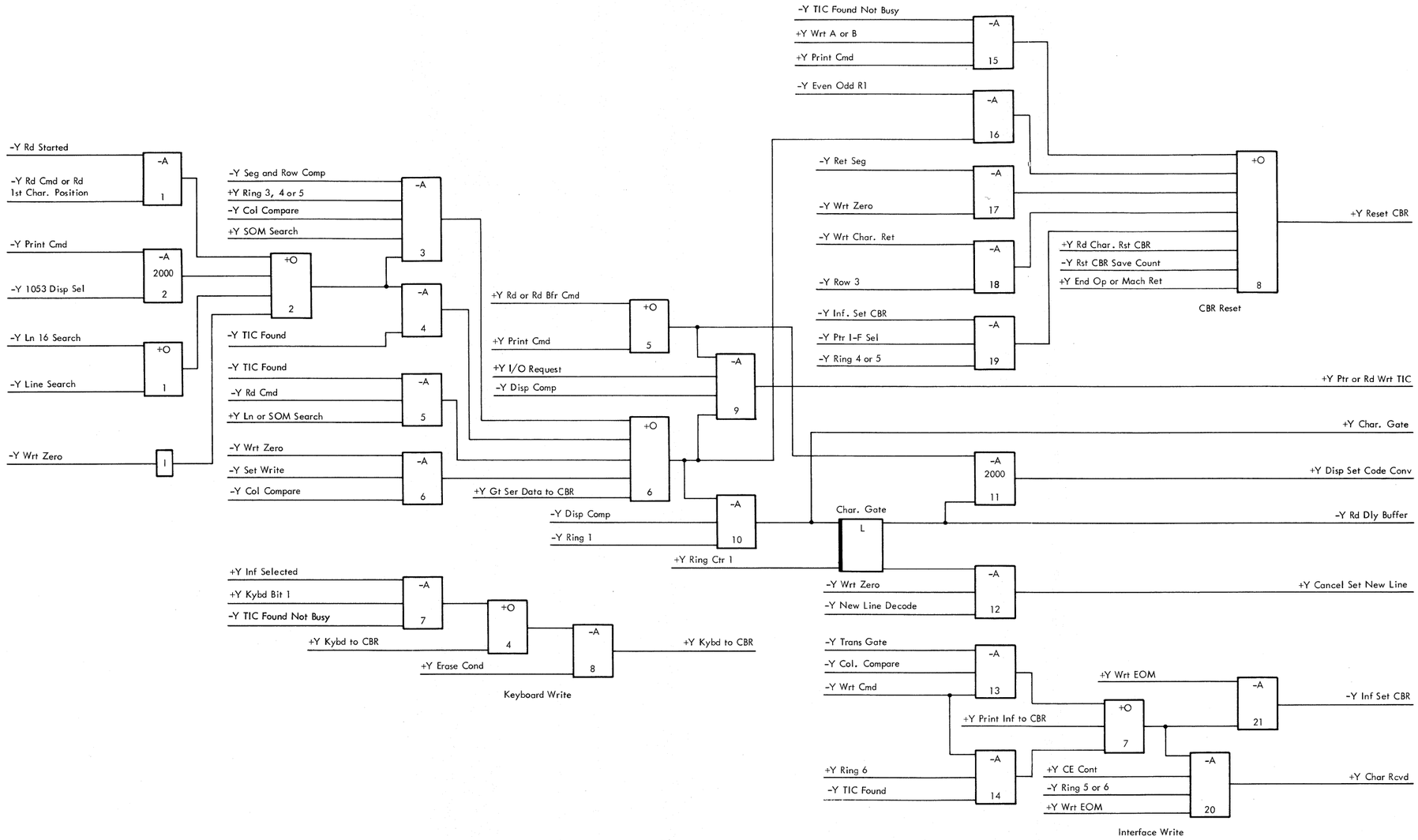


Figure 2-61. Common Buffer Register Controls

operation progresses, subsequent input characters are loaded into the CBR through the conditioning of A13. At A13 the Tran Gate input occurs when the TIC is found. The Col Compare signal indicates that the display circuitry is ready to write the next character. Note that the CBR is reset through A17 during retrace time in preparation for the loading of new data.

The +Y Wrt EOM input to A21 inhibits interface transfers during the write EOM operation.

Set EOM

The end-of-message (EOM) symbol is also the destructive cursor symbol in machines that contain the destructive cursor feature. The EOM signifies the end of a message in a manual input or print operation and is written into the delay lines under control of the Wrt EOM latch. Whenever the Wrt EOM latch is set, the EOM code (CBR bits 2, 4, and 6) is set into the CBR and written into the delay lines. The TIC is usually associated with the EOM (when used as destructive cursor), and, in these operations, bit 1 of the CBR is also set along with bit positions 2, 4, and 6. Operations involving the print command or TIC search require the EOM bits only; therefore, bit 1 of the CBR is never set during these operations.

SOM, New Line, and EOM Decode

The SOM, new line, and EOM decode circuit is illustrated in Figure 2-62. The decoder is always active except when a Rd Bfr Cmd (shown as an input to AND 1) is programmed by the local interface. During a Rd Bfr Cmd, all information contained in the selected buffer is transferred to the host system; hence, no data differentiation or decoding function is required in the CBR. For all other operations, AND's 3, 4, and 5 continually decode the CBR contents for the SOM, EOM, and new line codes. When these codes are detected, they are used to control information transfers to the local interface, remote interface, and 1053 printer. These control functions are more fully described (relative to machine operations) in flow chart form in the FE Diagram Manual.

The SOM, EOM, and new line codes are derived from CBR bits 2 through 7. Each code is listed in Figure 2-63.

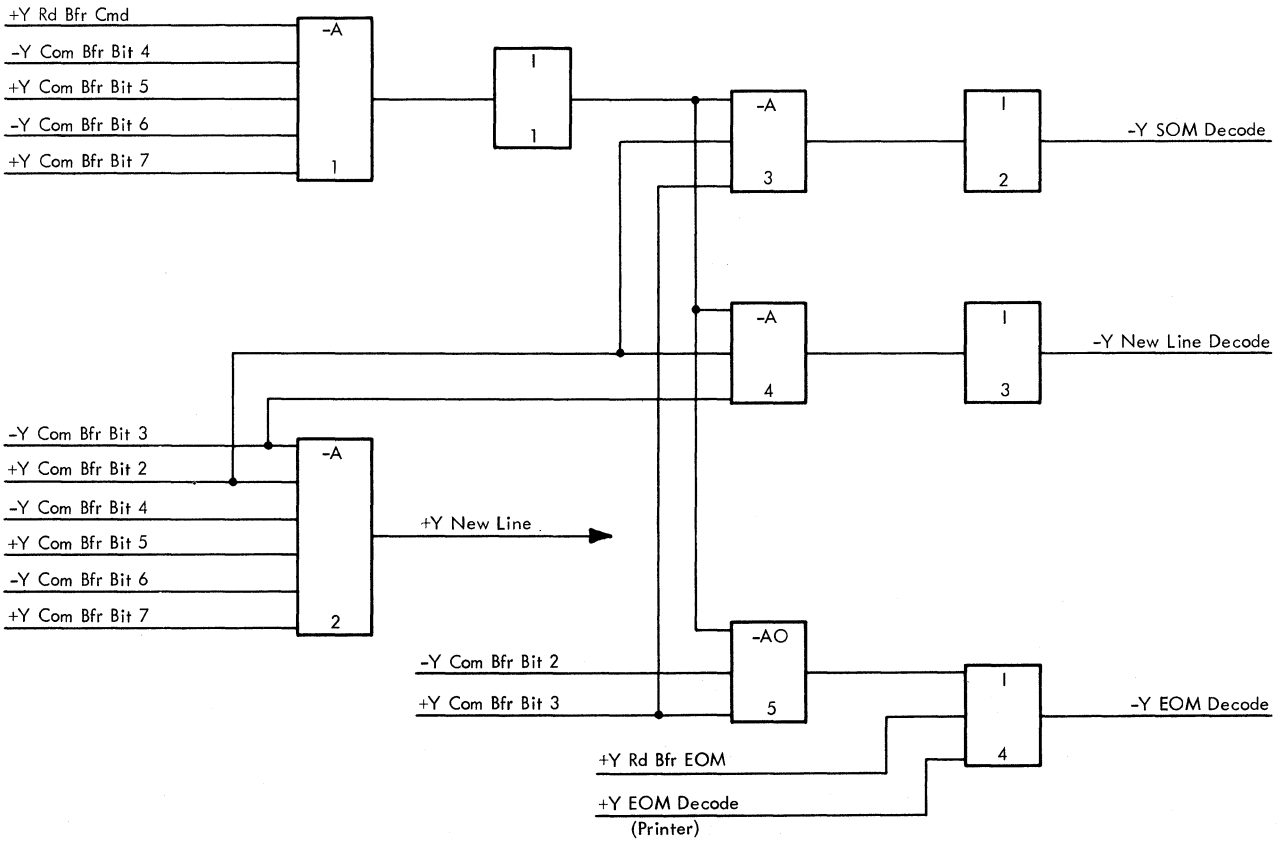


Figure 2-62. SOM, New Line, and EOM Decode Circuit

Control Function	Common Buffer Register Bits					
	2	3	4	5	6	7
SOM	0	0	1	0	1	0
EOM	1*	0	1	0	1	0
New Line	0	1	1	0	1	0

*Not used for TIC search or print command operations.

Figure 2-63. Common Buffer Register Control Codes

Character Generator

- Accepts six-bit internal code input from common buffer register.
- Generates five 7-bit bytes that represent character video for each 6-bit input that represents a displayable character.
- Character selection is accomplished by an 8 x 8 matrix used to condition cores in a single-plane memory.
- Performs the following code conversions as a result of each six-bit internal code input:
  1. Seven-bit ASCII to six-bit 2848 code
  2. Seven-bit ASCII to 1053 tilt-rotate code
  3. Six-bit 2848 to 1053 tilt-rotate code
  4. Six-bit 2848 to seven-bit ASCII.

The character generator is illustrated in block form in Figure 2-64. The figure also depicts the character generator's relation to the common buffer register.

The primary function of the character generator is to convert the incoming six-bit 2848 code from the common buffer register (CBR) into video data for storage in the buffer delay lines and for presentation on the viewing screen of the CRT. This video data output from the character generator consists of 35 bits transferred through the CBR as five 7-bit bytes. The character generator also performs a series of code conversions using portions of the fixed format core plane to effect the conversions.

When a write operation is to be performed, the six-bit 2848 code entered in the CBR either from a DS keyboard or from the associated computer via the interface logic is decoded by the character generator decoders. The three low-order CBR bits are decoded by the low-order decoders shown in Figure 2-64; the high-order decoders similarly decode the three high-order CBR bits. The decoder outputs represent the selection of one of eight possible drive lines to the core plane (lines 0-7, decoded from 000-111, respectively). The eight outputs from each decoder form an 8 x 8 selection matrix within the core plane so that 64 locations (or cells) can be selected within the plane. The actual cell selection is made in the normal manner; i.e., the selected line in each axis of the matrix half-selects many cores within the plane, and only cores at the "intersection" of two selected drive lines are fully selected.

Once CBR contents are decoded, the character generator is subjected to a write/read cycle. Figure 2-65 illustrates the timing for this write/read operation. Note that the Even-Odd latch and the row counter statuses are used to sequence the operation. This represents the use of an available and suitable timing source to operate the character generator but does not represent or indicate the

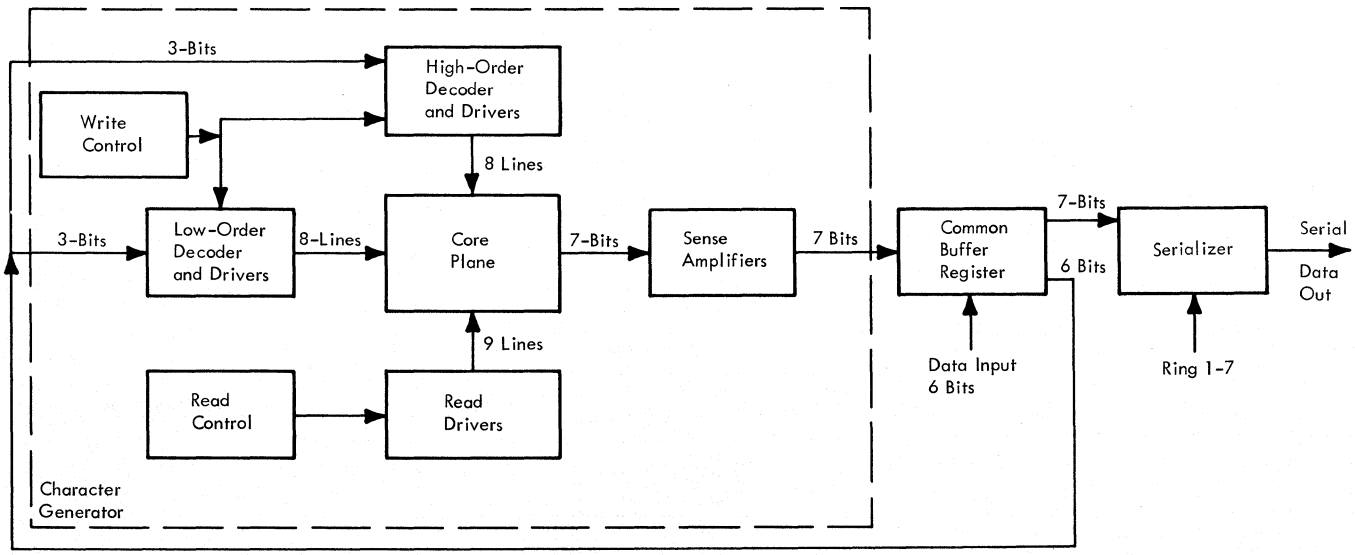


Figure 2-64. Character Generator, Block Diagram

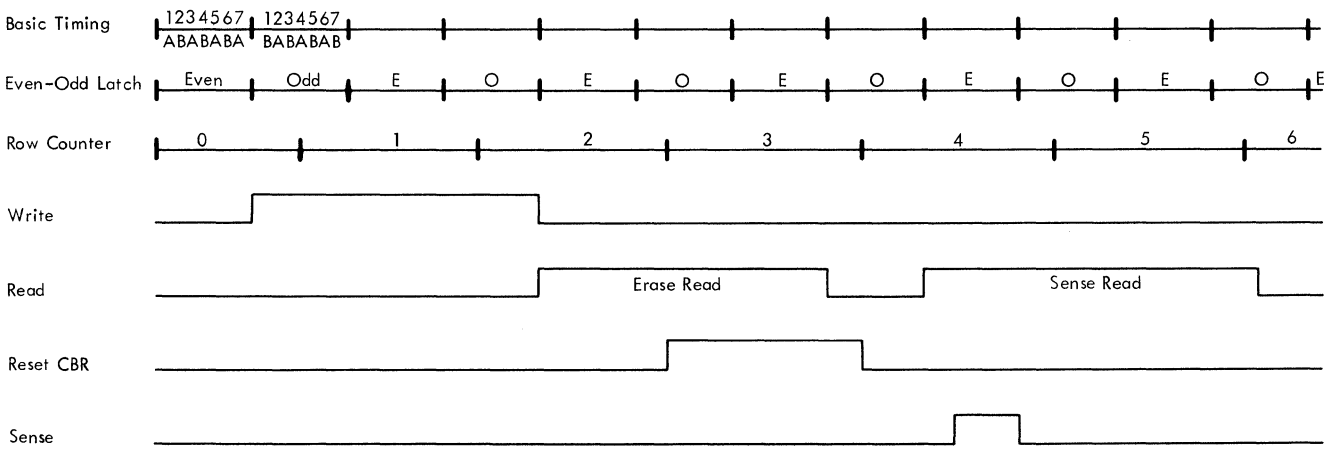


Figure 2-65. Character Generator Timing

eventual location of the character being written within the display.

The write portion of the cycle occurs first and causes all cores in the selected core plane location (cell) to be set. The group of cores (cell) set represents the video data cores and the cores for all code conversion that can be performed by the character generator. At the end of write time, the Erase Read pulse occurs. During erase read, all unwanted data is read from the selected location and destroyed; e.g., if character video is to be retained, all code conversion cores are read out and therefore reset. During the Erase Read, when undesired data within the selected memory cell is read from the cores and destroyed, the CBR is reset in anticipation of the desired core data that is read and sensed during sense read time. Next, the Sense Read occurs, and data is read from the cores to the CBR. If video data was read from the character generator (write operation), the data is sent into the CBR. It is gated at the correct time via serializer for eventual entry in the delay line. Other character generator outputs (code conversion) are routed from the CBR as required by the operation being performed.

Core Plane

The character generator core plane is a flat, single-layer storage device. Unlike less unique core arrays, the cores within the character generator core plane are located only at predetermined positions within the plane and not in an unbroken rectilinear pattern.

The core plane is divided into 64 memory cells which each contain the cores required to provide the binary video data and the code conversions for a displayable character. Each cell is individually addressable with an 8 x 8 selection matrix formed by the outputs of the high- and low-order decode circuits. Figure 2-66 illustrates the division of the core plane into memory cells and the way in which the decode circuits form the selection matrix.

Figure 2-66 also illustrates the A-character memory cell in detail. Note that the cell contains cores located only at the desired intersections of the grid formed by the seven horizontal rows (bit positions) and the nine columns (video 1-5 and code conversions). The cores in the V1-V5 columns form the data required to display the character A.

Each core has four "windings": low-order selection, high-order selection, read, and sense (Figure 2-67). The selection windings select and drive the core to the set state, the read winding drives the core to the clear state, and the sense winding detects the change in state of the core during the read operation.

The balance cores shown in Figure 2-66 at the bottom of the core plane are a design feature present for noise suppression; they do not actually contribute to character generation.

Cell Selection: The selection windings of all cores in the small cell are associated with the same high-order and low-order drive lines; e.g., all character A cell cores are driven by low-order line 001 and high-order line 000. Similarly, the cores of all eight cells driven by low-order line 001 are literally strung on and driven by the low-order 001 line. Thus, all cores in the low-order 001 column are half-selected when the 001 line is driven. (See Figure 2-67.) An identical situation exists with respect to horizontal cell rows driven by high-order decoder lines. Thus, cell selection is accomplished by simultaneously driving a low- and high-order line. Although the cores of eight cells in both the vertical and horizontal directions are half-selected, only the cores of the cell that is affected by both the low- and high-order drive lines (drive line intersection) are fully selected and set to 1.

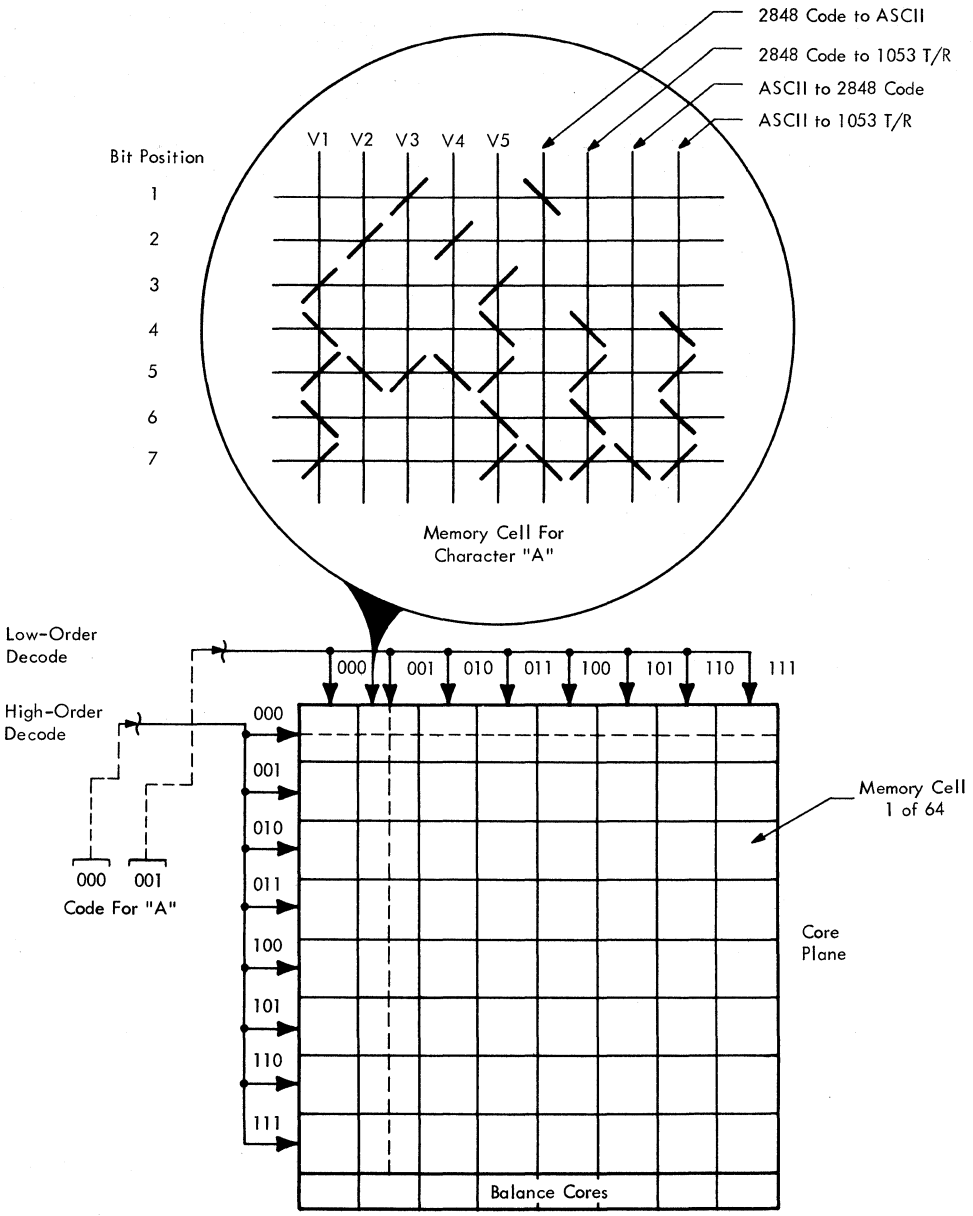


Figure 2-66. Core Plane Layout and Cell Selection

Read Winding Connection and Operation: The read windings of all cores in the plane are electrically connected with respect to the type of data in the core. The various types of data are represented in Figure 2-66 by the labels on the columns of cores in the detailed memory cell. Thus, for example, all V3 cores within the array are connected and read at the same time as all V4 cores, V5 cores, etc. (See Figure 2-67.) There are nine read loops, one for each type of data in the core plane. When current is caused to flow in the read windings, all set cores are returned to the clear state; cores that are already clear are driven further into the clear state.

Sense Winding Connection and Operation: Since data is read from the core plane in seven-bit bytes, seven sense loops service the plane. Note the memory cell grid detailed in Figure 2-68. The sense windings of the bit 1 positions of all memory cells are interconnected and provide an input to a sense amplifier circuit through which any data bit 1 is read from the plane. (See Figure 2-67.) There are six other sense loops, each corresponding to one of the other bit positions within the memory cell (Figure 2-68). Data is read from the array in parallel. Thus, all seven sense loops are activated during read time, and the bit 1-7 positions of the desired read loop are extracted from the array.

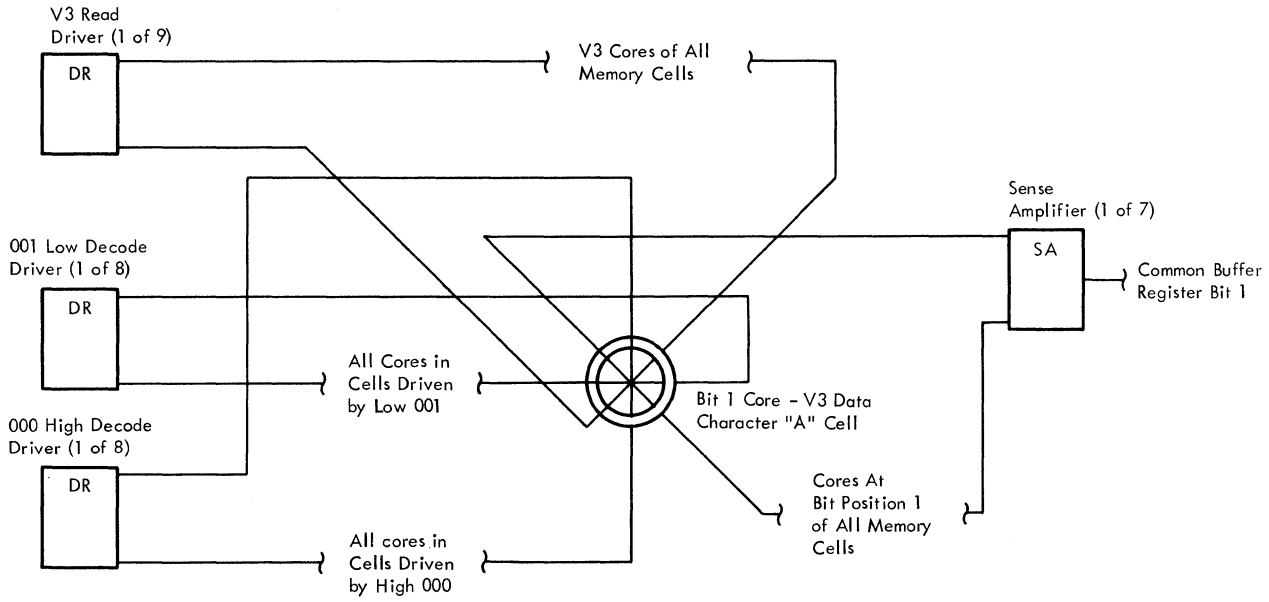
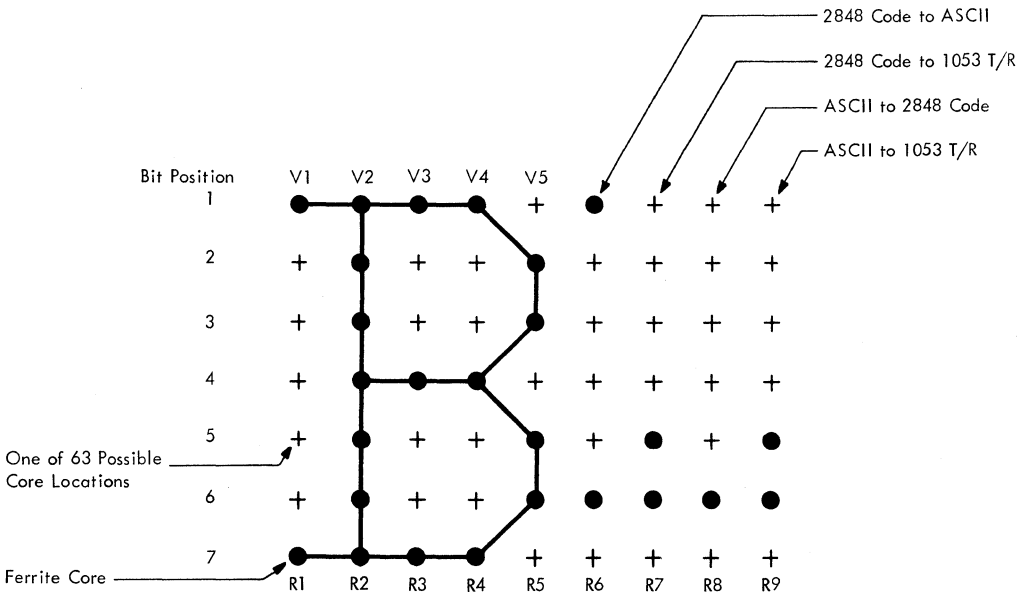


Figure 2-67. Selection, Read, and Sense Winding Connections



Video Data "B" Char.	V1	1000001	Binary Data That Can Be Read From Typical Memory Cell
	V2	1111111	
	V3	1001001	
	V4	1001001	
	V5	0110110	
Char. "B" Codes	ASCII	1000010	
	1053 T/R	0000110	
	2848 Code	0000010	
	1053 T/R	0000110	

Figure 2-68. Generation of Binary Data from Memory Cell

Binary Data Outputs: The various binary data bytes that can be read from the core array are shown in Figure 2-68, which depicts the B-character memory cell. Note the relation between the core position and the bit positions in the binay data bytes.

Decoders

The character generator decoders consist of the low-order and high-order decoders. The terms "high" and "low" refer to the CBR bit positions used as inputs to the decoders. The low-order decoder receives CBR bits 2, 3, and 4 as inputs; the high-order decoder operates with CBR bits 5, 6, and 7. Each decoder uses the three-bit input to decode for and select one of eight possible drive lines to the core array. Since the low- and high-order decoders operate essentially the same, only the operation of the low-order decoders is discussed here.

The low-order decoder circuits are illustrated in Figure 2-69. Note that there are eight decoder AND circuits labeled 000 through 111 (0-7) representing the eight drive lines that can be selected. The inputs to the AND's illustrate the various CBR bit 2, 3, and 4 combinations required to condition the AND. Assume that CBR bits 2, 3, and 4 are all 1's. Then, A8 (111) is conditioned, with the result that D8 is partially conditioned. When the write-core signal is generated by the write control circuits, D8 is fully conditioned, and all cores in cell column 8 (drive line 8) are half-selected.

The high-order decoder operates in the same manner with CBR bits 5, 6, and 7. The high-order decoder output represents the half-selection of a row of eight memory cells. The cell at the intersection of the cell column and the row driven by the decoders is fully selected.

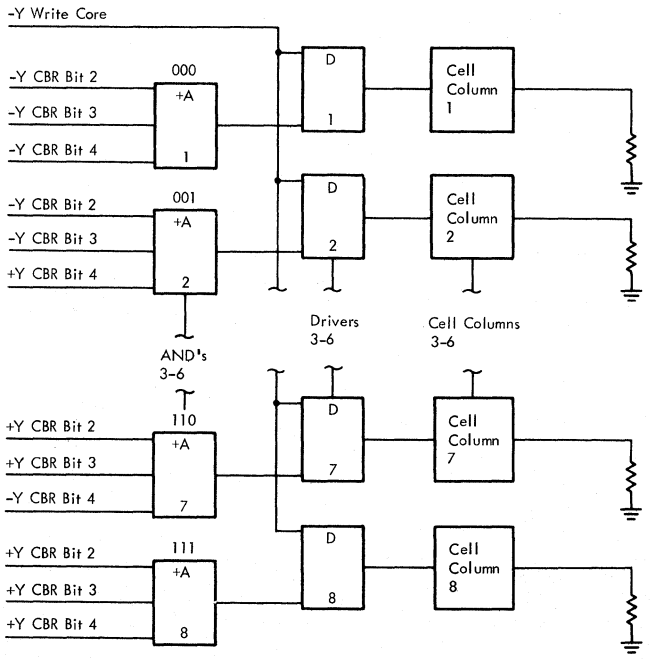


Figure 2-69. Low-Order Decoder and Driver

Write Control

The write control circuits govern the setting of the cores within the selected memory cell. The write control circuits are illustrated in simplified logic form in Figure 2-70. The write character operation is accomplished when the Write latch is set. Note, in the figure, that both A1 and A2 must be conditioned before the Write latch is set. AND 1 is conditioned when the column counter indicates that a delay line may be able to accept the BCD character in the CBR (BCD Wrt V1 Rd) and the Even/Odd trigger is in its even status. A2 is conditioned when the row counter equals zero (Row 0), the Write Character latch is set, and vertical retrace is being accomplished (Write Char Ret). When the Write latch is set, the -Y Write Core signal is generated, and the cores in the selected cell are set.

At row 2 time, A3 is conditioned and the Write latch is reset. The A3 output also generates the Set Rd Lch signal to ready the read control circuits for the character generator read operation.

At row 3 time, the CBR is reset (A5) in preparation for the transfer of data from the selected memory cell to the CBR.

Read Control

The character generator read control circuits govern the extraction of data from the selected memory cell within the core plane. The control circuits actually generate a read operation consisting of two parts: the erase read, and the sense read. During the erase read, unwanted data within the selected memory cell is read from the cores and destroyed. During the sense read, the desired data is read from the core plane, sensed, and loaded into the CBR. Thus, the read control circuits must not only cause the erase and sense reads to occur but must be capable of determining what information is to be preserved during the erase read. This latter capability is provided primarily by the Code Conversion latch. When this latch is reset, the V1 through V5 portions of the selected cell must be preserved since a character write operation is being performed. When the Code Conv latch is set, the V1 through V5 data bytes in the core plane and any unwanted code conversion bytes must be erased; only the code conversion required for the operation being performed must be preserved.

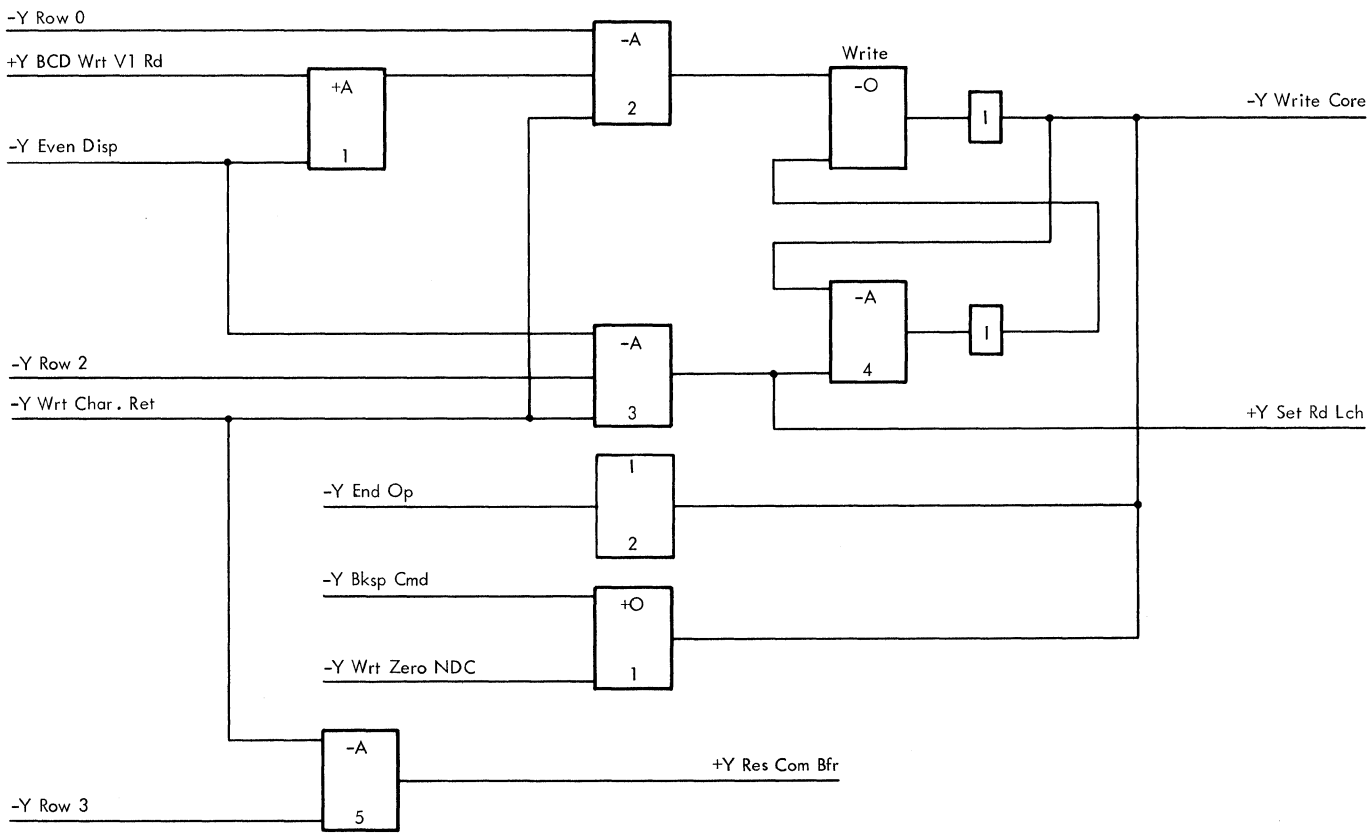


Figure 2-70. Character Generator Write Control

The read control circuits are illustrated in Figure 2-71. Read control operation is discussed first for a character-read operation (Code Conv latch reset) and then for a code-conversion operation (Code Conv latch set).

The read control circuits are first activated when the character generator Write latch (Figure 2-70) is reset during Row 2 time. When the Write latch is reset, the +Y Set Rd Lch is generated to the read control circuits. Then, the Read latch is set and the -Y Read Gate is conditioned. The Read Gate signal partially conditions drivers D1 through D9 and AND circuits A5, A6, and A8. Since the erase read occurs first, A5 and A6 are of interest now. AND 6 is conditioned when the row counter is not at 4 and the Code Conv latch is set. It is assumed here that the Code Conv latch is not set; therefore, A6 is not conditioned, its output remains negative, and the +Y Erase Read line is not conditioned. A5 is conditioned, and its positive output is inverted and applied to AND's 7, 11, 14, and 18, which are already partially conditioned because of the status of the code conversion control circuits. The resulting positive outputs of the four AND's complete the conditioning of drivers D6 through D9, with the result that all code conversion data in the selected memory cell is read and destroyed (not sensed). Note that drivers D1 through D5 are not conditioned and that the V1 through V5 data in the core plane is preserved.

During Row 3 time, A3 is conditioned and the Read latch is reset, thus ending the erase read operation. During Row 4 time, A2 is conditioned, and the Read latch is set again to initiate the sense read as indicated at A1, which produces the Sense Gate at this time. The output of the Read latch again partially conditions drivers D1 through D9. Now, since the row counter equals 4, A8 is conditioned, and its output partially conditions A20-A24. The code conversion AND's (A9, A13, A17, and A19) are also partially conditioned by the A8 output; none is completely conditioned, however, because of the status of the code conversion control circuits.

Now, V1 through V5 can be read as the required inputs to A20 through A24 are received from the character generator and gates. Remember that the character generator read operation is accomplished during retrace time and that the reading of V1 through V5 requires five vertical sweep times; i.e., read during retrace and load CBR, then store new data in selected delay lines, read during retrace, etc. Therefore, the read control circuits are actually

cycled by the row counter counts of 1 through 6, which occur during each retrace time for each data byte read from the core plane.

The read control circuits operate in a similar fashion when the Code Conv latch is set. With the latch reset, however, A6 is conditioned as part of the erase read, and V1 through V5 (character video) are read from the core plane and destroyed. Note that A5 is still conditioned during erase read to destroy unwanted code conversion data. The desired code conversion is preserved by the status of the conversion control circuits. For example, if the channel is writing to the printer buffer, A7 is deconditioned during the erase read, and the BCD-to-tilt rotate code conversion is preserved. Then, A9 is conditioned during the sense read operation so that the desired code conversion is read to the CBR.

Position Storage and Compare Logic

- Provides a static record of the status of the common control counters when TIC was found and, thus, a known reference point within the data stored in the buffers.
- Stores and compares the following common control counter information:
  1. Compares Odd or Even Display trigger status with display selected.
  2. Status of Left Display/Right Display trigger.
  3. Status of segment counter.
  4. Count in row counter.
  5. Status of character column ring counter.
  6. Count in line counter.

General

The position storage and compare logic is used to store the status of the common control counters. Remember that the control counters must operate without interruption to provide for the proper display of data at the associated display stations. When an operation is to be performed on data in the delay lines (read or write), the TIC is used as an index to provide a reference point within the buffers. Once TIC has been found, however, a record of its location must be maintained to provide a static position reference from which operations can be performed.

The way in which the reference point is defined can be illustrated by considering the data that is recorded by the position storage logic. Each area of the position storage logic is listed with its function in Figure 2-72.

The way in which the position storage circuits define a specific location within the display is illustrated in the following example:

Position Storage Circuit	Status	Indication
Display Compare latch	Odd	Odd display
Left/Right Storage trigger	Left	Buffer 1 or 2
Segment Storage	Upper	Buffer 1 or 3
Row Counter Storage	Row 0	Top row of displayed characters
Column Storage	BCD	BCD column of character
Line Counter Storage	16	Line 16 of the display

By combining the data provided by the position storage circuits, it can be seen that the position storage statuses define the BCD column of the first character in row 0, buffer 1, of the odd display. This specific location is defined each time the composite contents of position storage compare with those of the common control counters.

Note that each position storage compare value can be used individually to denote a position within the display data. For example, assume that TIC is found and that the position storage is set to the values listed in the preceding example. As soon as the character column ring counter cycles through V1-V5 and returns to BCD, a column compare is generated. This BCD-stored and next-BCD-column compare can be used as an indication that the character has been written and that the character-write operation can be terminated.

Counter Storage Control

The counter storage control circuits direct the operation of the various counter storage areas as required by the operation being performed. The storage control circuits are illustrated in Figure 2-73. Each output shown is listed in Figure 2-74, which indicates the various times and conditions in which each storage control output is generated. Only the generation of counter-storage outputs is discussed here. The significance of these outputs with respect to specific machine operations is more apparent in the flow charts provided in the FE Diagram Manual.

In Figure 2-73, note that finding TIC affects both A1 and A3. A1 is conditioned earlier to reset the address register and the command register and to gate bit 1 into the address register. A3 is conditioned after the necessary address selections have been made. A3 causes the storage logic to be set to the character position referenced by the TIC. At this time, data is gated into the command register. Thus, counter storage control feels a dual effect each time that TIC is found.

During the erase operation, counter storage is first affected by the Erase SS input to OR 8. This input resets counter storage to upper, left, and

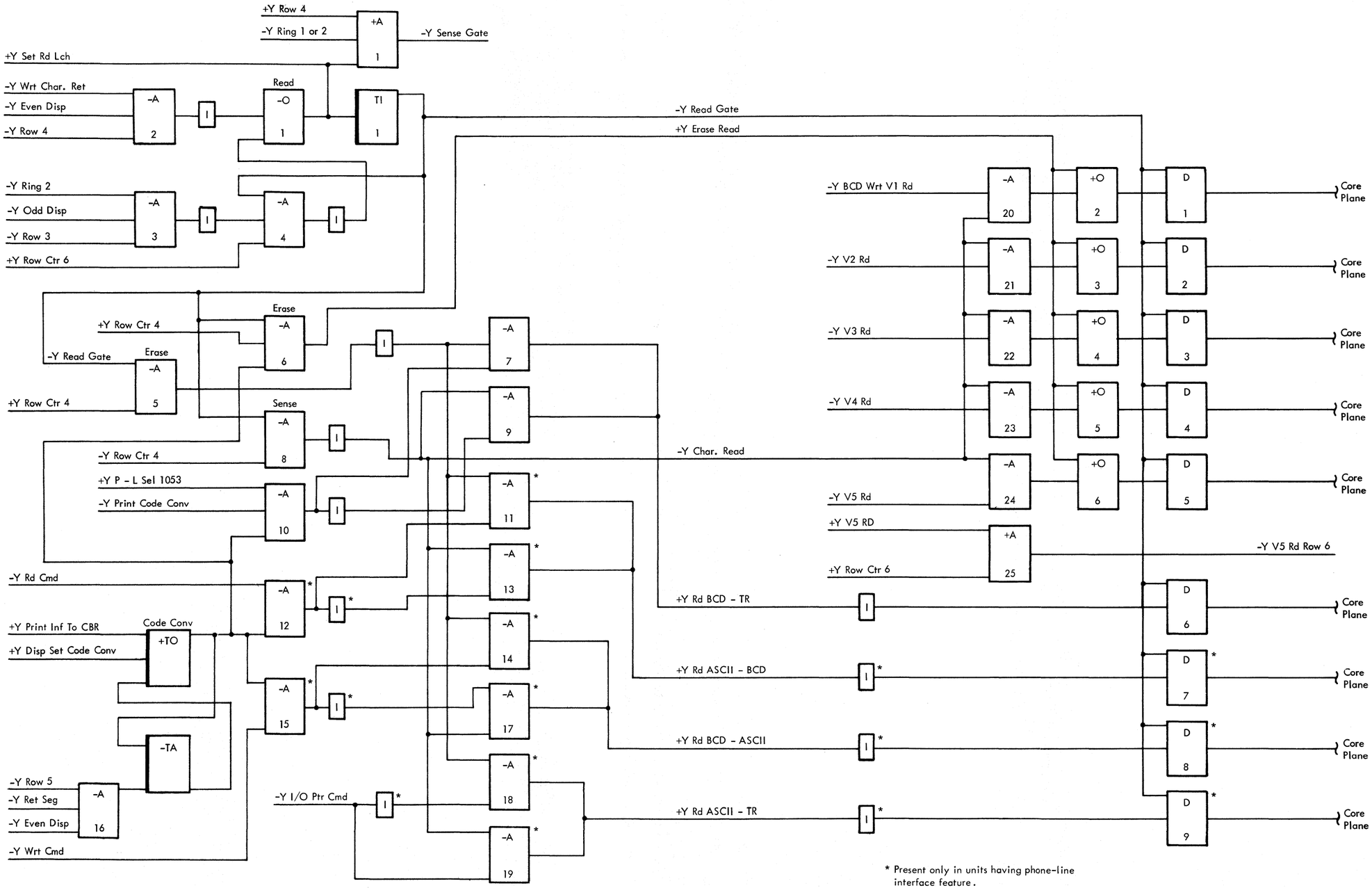


Figure 2-71. Character Generator Read Control Circuits

Position Storage Circuit	Function
Display Compare latch	Once the even or odd display has been addressed and selected, the Display Compare latch input network compares AR bit 1 with the outputs of the Even-Odd Timing trigger and the latch is set each time a compare is made; e.g., AR bit 1 equals 1 (odd display), and Even-Odd timing trigger is in odd-display time.
Left/Right Storage trigger	This trigger stores the status of bit 256 of the line counter, which indicates whether the left display (buffers 1 and 2) or right display (buffers 3 and 4) was active when the storage sequence occurred.
Segment Storage	The Upper/Lower Storage triggers within the segment storage circuits sample the status of the vertical segment counter, which can be upper or lower. When a storage sequence occurs, the Upper/Lower Storage trigger stores one of two statuses of the vertical segment counter as follows: 1. Upper -- buffer 1 or 3 displaying 2. Lower -- buffer 2 or 4 displaying (Retrace segment is not stored.) Each time thereafter, the status of the vertical segment counter is the same as the condition stored in the Upper/Lower Storage trigger; e.g., upper and upper, a segment compare signal is generated.
Row Counter Storage triggers	Row storage is loaded directly with the contents of the three-bit row counter. Then, each time the contents of the row counter are the same as the count stored in row counter storage, a Row Compare signal is generated.
Column Storage	The BCD/V2-V4 Storage trigger within the column storage logic stores the output of the character column ring counter, which can be BCD or not BCD (video V2-V4). When the storage sequence occurs, the BCD V2-V4 storage trigger stores the status of the character column ring counter. Each time thereafter, the status of the character column ring counter compares with the status stored in the BCD V2-V4 Storage trigger; e.g., BCD and BCD, a Column Compare signal is generated.
Line Counter Storage	Line counter storage is loaded directly with the contents of the line counter, except for line counter bits 1 and 256, which, for reasons explained in connection with line counter storage operation, are not required. Thereafter, a line compare is generated each time the count in the line counter equals the count stored in line counter storage.

Figure 2-72. Function of Position Storage Circuits

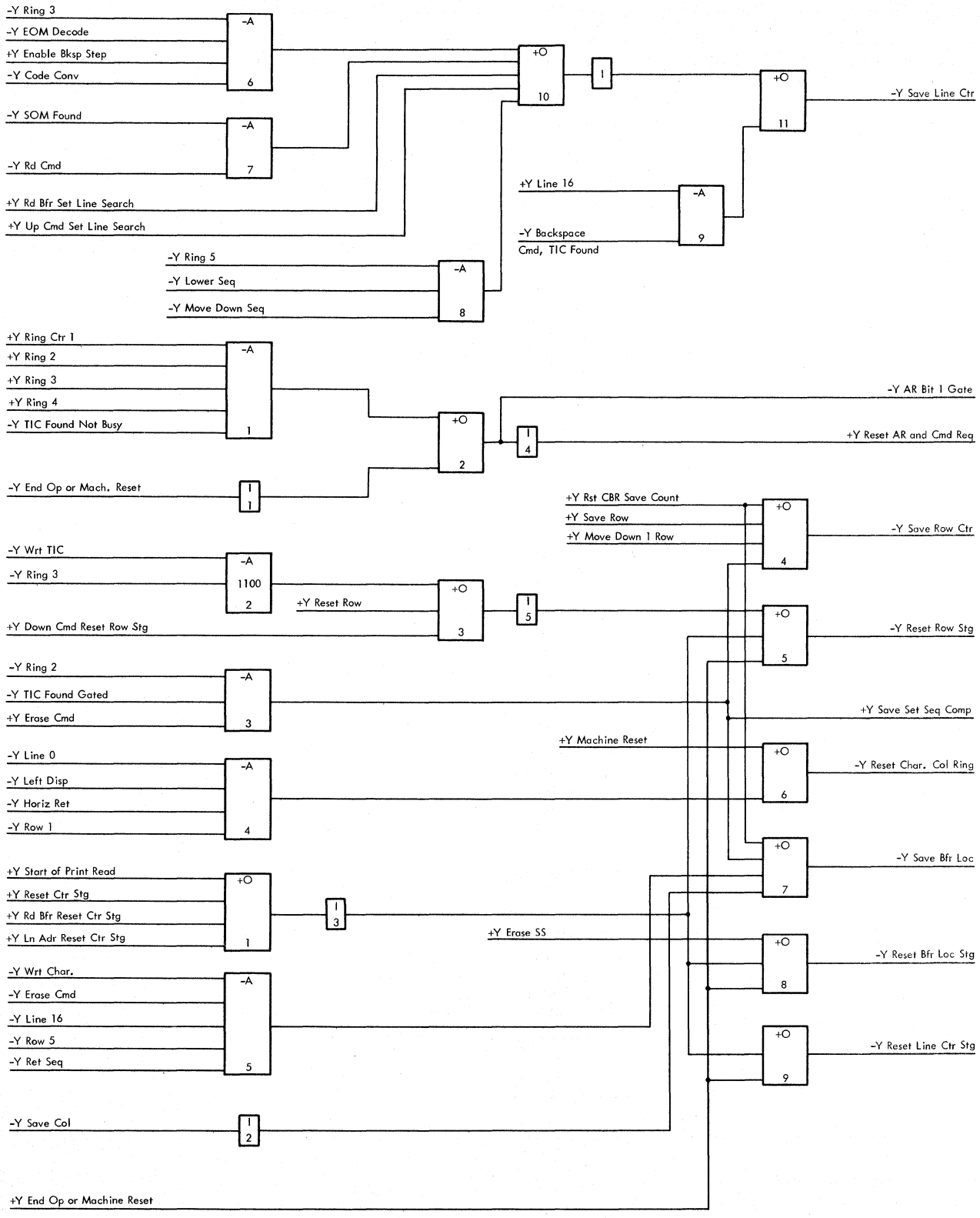


Figure 2-73. Counter Storage Control

Output and Output Function	Output Ckt	When Originated
AR Bit 1 Gate: Enables setting of AR bit 1.	OR 2	1. When TIC is found (A1). 2. At End Op or Machine Reset (I1).
Reset AR and Cmd Reg: Resets address register and keyboard command register.	OR 2	1. When TIC is found (A1). 2. At End Op or Machine Reset (I1).
Save Row Ctr: Transfers contents of row counter to row counter storage.	OR 4	1. In conjunction with an SOM search (Rst CBR Save Count, input; OR 4). 2. In conjunction with a non-backspace line change (Save Row input; OR 4). 3. In conjunction with a Down command for NDC only (Move Down 1 Row input; OR 4). 4. When TIC is found (A3).
Reset Row Storage: Resets Row Storage triggers.		1. When NDC TIC is written (A2). 2. General storage reset, as indicated by inputs to OR 1. 3. End Op or Machine Reset.
Save Set Seg Comp: Sets Segment Compare latch.	A3	When TIC is found (A3).
Reset Char Cal Ring: Resets character column ring counter; resets line counter; and resets Left/Right Display Late trigger.	OR 6	1. During horizontal retrace time (A4). 2. Machine reset.
Save Bfr Loc: Set Seg Storage trigger; sets BCD-Video (column storage) trigger and Left/Right Storage trigger.	OR 7	1. In conjunction with an SOM search (Rst CBR Save Count input; OR 4). 2. When TIC is found (A3). 3. When column is to be stored in conjunction with a line search or a set EOM operation (Save Col input; OR 7). 4. During an erase command after the storage logic has been reset to upper, left, and BCD.
Reset Bfr Loc Stg: Resets Left/Right Storage trigger; resets Upper/Lower Storage trigger; resets BCD-Video (column storage) trigger; and resets Rd Started trigger.	OR 8	1. During an erase operation (Erase SS input; OR 8). 2. General storage resets as indicated by inputs to OR 1. 3. End Op or Machine Reset (OR 8).
Reset Line Ctr Seg: resets Line Counter Storage triggers	OR 9	1. General storage resets as indicated by inputs to OR 1. 2. End Op or Machine Reset (OR 8).

Figure 2-74. Counter Storage Control Outputs

BCD. Subsequently, A5 is conditioned to store the buffer location so that TIC can be rewritten in the proper location after the erase operation is completed.

Row Counter Storage and Compare

Row counter storage consists of three triggers and a special network that is used to modify row storage during certain backspace or up command operations (Figure 2-75). The three triggers are set with the contents of three similar triggers within the row counter whenever a Save Row command is issued from counter storage control. The outputs of the Row Counter Storage triggers are exclusively OR'ed with those of the Row Counter triggers. Thus, each time that the row-storage and row-counter contents are the same, the Row Compare signal is generated. (The exclusive OR circuits forming the row compare circuits are not illustrated.)

The network formed by AND's A1, A2, and A3 in Figure 2-75 is used to modify row storage during backspace operations that require a line change. When either A1 or A2 is conditioned, the count in row storage is reduced by 1. Note that A1 is present for the NDC only. This modification of the row counter provides for backspace operations in which the cursor is moved from the first character position of a row to the last character position of the next row above.

AND 3 provides for the modification of the row counter when a backspace occurs with the cursor in row 0. Then, the cursor must be moved to row 5 of the preceding segment, i.e., lower to upper, or upper to lower. However, when a row counter storage of 0 is decremented in the normal fashion, row counter storage equals 7. Then, A3 is conditioned twice to decrement row storage from 7 to 6 to the desired count of 5.

During other operations, such as down and advance, it is necessary to increase the count in row storage by 1. This is accomplished purely through timing wherein row storage is reset, the row counter is allowed to step by 1 in the normal manner, and row counter storage is set with the new (increased by 1) row counter status. The inputs to OR4 and OR 5 in Figure 2-73 illustrate the way in which counter storage control is conditioned to provide the required reset-row and save-row sequences.

Segment Storage and Compare

The segment storage and compare logic is used to store the status of the vertical segment counter, which can be upper, lower, or retrace. Only the upper and lower segment indications are stored since there is no need to store and subsequently compare the retrace segment.

Segment storage is illustrated in Figure 2-76. It can be seen that a single trigger, the Upper/Lower Storage trigger, is the heart of segment storage. Segment counter status is stored through AND circuits A3 and A4. Each of these AND's receives an input from the segment counter (Lower Segment and Upper Segment) and an input from counter storage control (Save Bfr Loc). A third input, from the Upper/Lower Storage trigger, is sensed at A3 and A4, and the trigger is complemented only if a change in state is required to store the segment counter status correctly. For example, assume that the Upper/Lower Storage trigger is set (lower) and that the Save Bfr Loc signal is generated when the vertical segment counter is in upper. At A4, note that the set side of the Upper/Lower Storage trigger causes A4 to be fully conditioned so that the Upper/Lower Storage trigger is complemented to upper. If the trigger were already in upper under the conditions described, neither A3 nor A4 would be conditioned, and the Upper/Lower Storage trigger would not be complemented. Instead, it would be left in the upper condition (reset), thus indicating the proper stored segment.

AND circuits A1 (NDC only) and A2 (2848 Models 2 and 3 only) provide a means of complementing the Upper/Lower Storage trigger during down operations (A1) and backspace operations involving a line change between segments (A2). Here, only the fact that the Upper/Lower Storage trigger is complemented under these conditions is important. The flow diagrams for the down and backspace operations (Chapter 3) reveal the significance of this complementing action.

The segment compare is made at AND's A10 and A11. For example, if the Upper/Lower Storage trigger is set to lower, A10 will be conditioned at row ctr 6 time during Upper Seg Late time, which extends into lower segment time. Then, A10 is conditioned, and the Seg Compare latch is set. The Seg Compare latch will be reset at row 6 time of the segment that started when the compare was made; e.g., if the compare was made at row 6, upper late, Upper/Lower Storage in lower, then the Seg Compare latch is reset at the next row 6 time, which occurs at the end of the lower segment.

Column Storage and Compare

The column storage circuits are illustrated in Figure 2-76. Note the BCD/V2-V4 trigger in the figure. When a save-buffer-location order is issued from counter storage control, this trigger is conditioned to reflect the status of the character column ring counter with respect to whether the counter is at BCD or video (V2 or V4).

When a save-buffer-location order is issued from counter storage control, A5 and A6 are partially

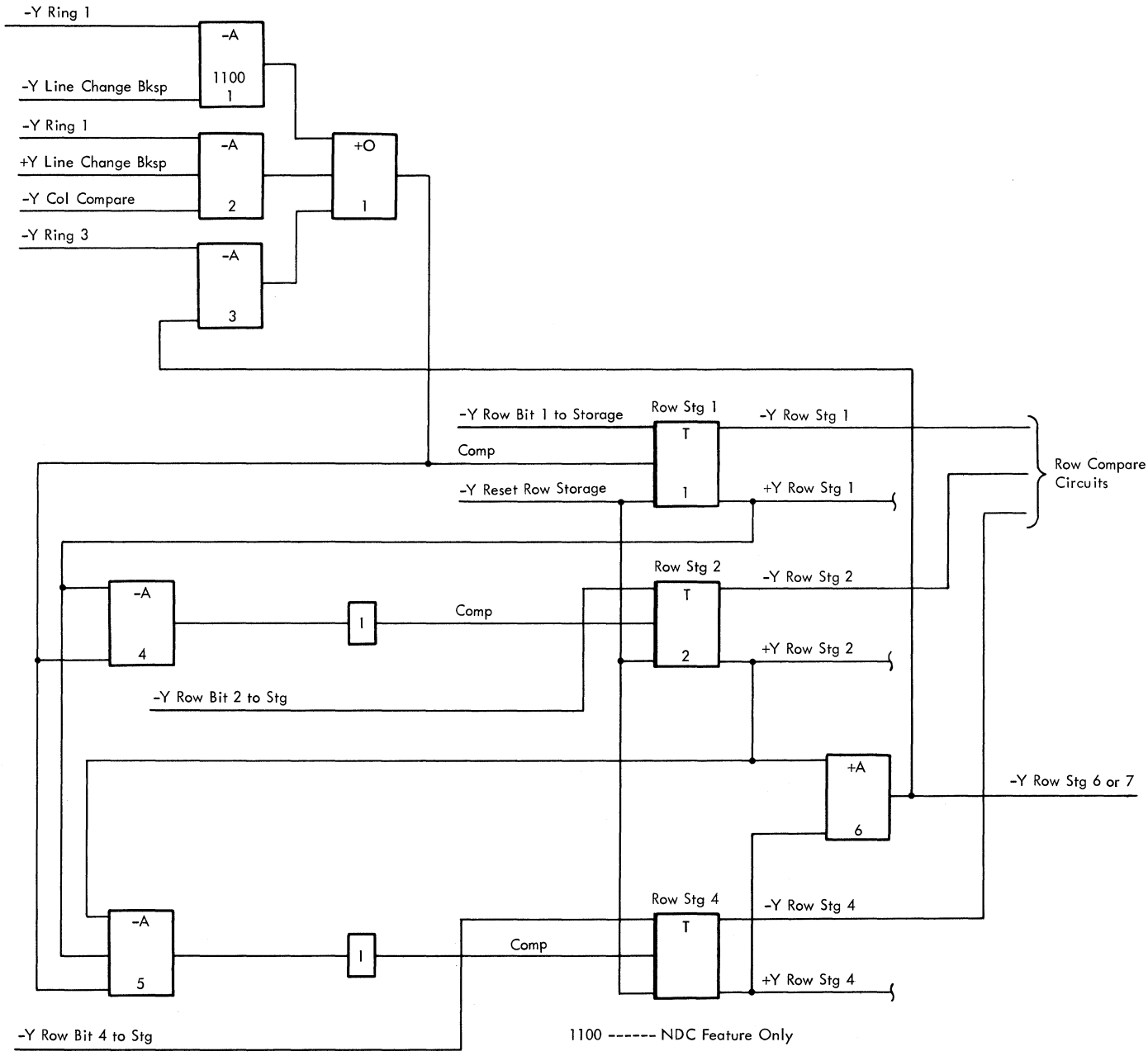


Figure 2-75. Row Counter Storage

conditioned. A5 also receives a BCD Col input, which is conditioned when the character column ring is at BCD. Similarly, A6 requires a Not BCD Col (video column) input from the column counter before it is conditioned. Both A5 and A6 sense the status of the BCD/V2-V4 to determine whether the trigger is already in the desired state (BCD or video) or whether it must be complemented. Thus, the trigger is set to represent the status of the character column counter when the save-buffer-location sequence was initiated.

The outputs of the BCD-V2-V4 latch are used to derive the column compare as follows. Assume that the BCD/V2-V4 trigger is set to BCD as a result of the save-buffer-location sequence. The BCD output from the BCD/V2-V4 trigger is negative (trigger is set) and does not affect OR 7. The video output from the BCD/V2-V4 trigger is positive, with the result that OR 8 is conditioned. At this time, either OR 9 or OR 10 is also conditioned, depending on whether the save-buffer-location operation caused left display or right display to be stored in the Left/Right Storage trigger. Assume that the Left/Right Storage trigger is set to left display. OR 9 is conditioned by +Y Not Right Stg. Thus, under the conditions established above, the save-buffer-location sequence has conditioned OR 8 (and thus input d of A16) and OR 9 (and thus input a of A16). These conditions are

static in that they do not change until the counter storage logic is reset or otherwise modified.

The remaining two inputs to A16 (b and c) can be considered dynamic in that they are alternately conditioned and deconditioned. Input b to A16 is generated during each +Y Not Right Disp Late (and thus Left Disp) time. Input c to A16 is generated from OR 7 each time the character column ring counter is at the BCD column. Since all the input conditions of A16 are satisfied, a Column Compare signal is generated. The Column Compare just described was obtained as a result of the following steps:

1. The save-buffer-location operation was initiated.
2. The BCD/V2-V4 trigger was set to BCD.
3. The Left/Right trigger was set to left.
4. As a result of 2, OR 8 was conditioned.
5. As a result of 3, OR 9 was conditioned.
6. AND 16 is conditioned each time the character column counter is at BCD.

Thus, the column storage was set when the character column counter was at BCD; a Column Compare is generated each time the counter is again at BCD.

A Column Compare can also be generated when the BDC/V2-V4 trigger is stored in the video position. Recall (TIC Sample Decoder operation) that it is possible to find TIC and initiate a save-buffer-location sequence when the character column counter is at other than BCD. In this case, the BCD/V2-V4 trigger would be stored at video (reset) state. The Column Compare under these conditions can be analyzed as follows:

1. The video status of the BCD/V2-V4 trigger conditions OR 7 and, thus, input c to A16.
2. Assuming that the Left/Right trigger was at left when the save-buffer-location operation was initiated, OR 9 (and therefore input a to A16) is conditioned by +Y Not Right Stg.
3. OR 10 (and thus input b to A16) is conditioned during each Not Right Disp Late time.
4. OR 8 (and input d to A16) is conditioned each time the character ring column is at V4 during Right Display time and each time the counter is at V2 during Left Display Late time.
5. It has already been stated that OR 10 is conditioned by +Y Not Right Display Late. Thus, A7 cannot be conditioned simultaneously with OR 10. However, A8 can be and is conditioned. Thus, each time the character column counter is at V2, a Column Compare is generated from A16.

The relation of BCD, V2, V4, left display, and right display is discussed in connection with TIC Sample Decoding (in the paragraph so entitled).

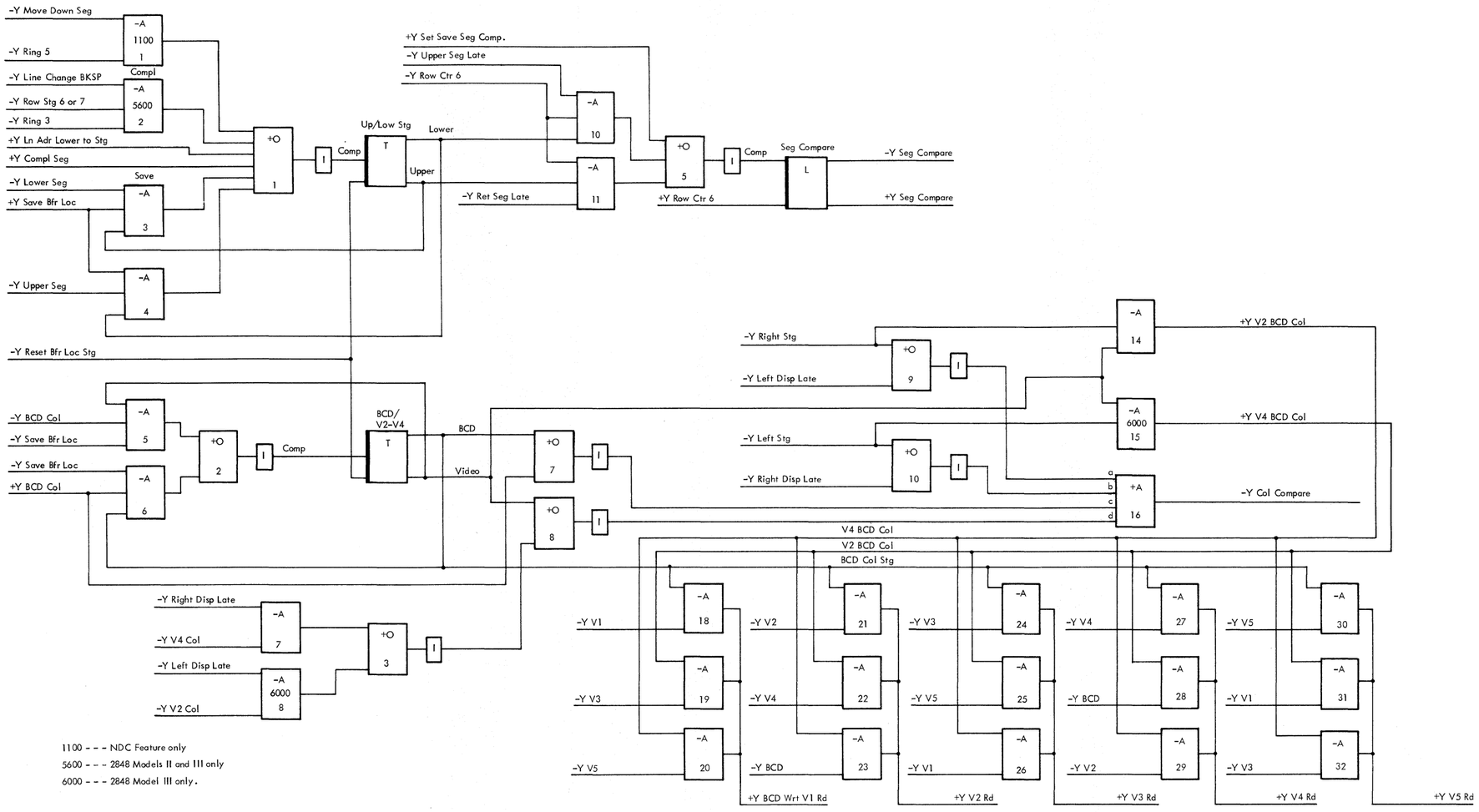
Line Counter Storage and Compare

The operation of the line counter storage and compare logic is similar to that of row counter storage. When a save-line-counter order is issued, the contents of the line counter triggers are set to line counter storage, which contains a similar trigger for each line counter bit except bits 1 and 256. Bit 1 is not required because the line counter is always stored at a BCD line, which must be an even-numbered line. Obviously, bit 1 is only required to represent odd numbers. Bit 256 of the line counter is used to indicate left and right display and is not part of the true line count. The Left/Right Storage trigger is used within the storage and buffer selection as the source of left-right display intelligence. The line counter storage is also modified during backspace operations to adjust the line count, in much the same way that the row counter storage contents are modified for certain backspace operations.

Line counter storage logic is shown on ALD C9.05.16.1. The generation of the save-line-counter order from counter storage control is illustrated in Figure 2-73. The generation and the purpose of the Save Line Counter signal are given in detail in Figure 2-77 as a supplement to the information provided in the operations flow charts in the FE Diagram Manual. Note that generation of the Save Line Counter signal always causes the exact contents of the common control line counter to be set into the line counter storage register.

In addition to the set of AND circuits used to gate the line counter contents to storage, a second set of AND gates is enabled only during backspace operations (ALD C9.05.16.1). When a backspace operation involves the simple movement of one character space to the left, the line counter storage is set in the normal fashion, the backspace AND gates are enabled, and the line count in storage is decremented by 6 during the retrace segment through AND 4A. Note that the Row Ctr 1 input to AND 4A is derived from the Bit 1 trigger of the row counter, which is conditioned three times as the row counter counts from 0-6 during retrace time. Each output from AND 4A decrements the stored line count by 2; thus, the overall reduction of the count by 6 is accomplished.

When a backspace operation involves movement of the cursor from the very start of a line to the end of the line above, the line counter storage is manipulated differently. Then, line storage is preset to a count of 240 instead of being set with the line-counter contents. A line count of 240 represents the last line on the display (line 240 and right display). After the



1100 - - - NDC Feature only
5600 - - - 2848 Models II and III only
6000 - - - 2848 Model III only.

Figure 2-76. Vertical Segment and Column Storage on Compare

Initiating Circuit or Input	Associated Operation	Purpose
Rd Bfr Set Line Search	Read Buffer	Stores line count to provide a record of where line search started.
Up and Set Line Search	Move NDC up within display (Up Cmd)	Stores line count to represent cursor's lateral position within display and so permit lateral positioning of cursor during up sequence.
A6	Read Cmd	Stores line count to represent position of EOM for a subsequent write TIC operation.
A7	Read Cmd	Stores line count to form part of record of SOM location within display.
A8	Move NDC down within display (Down Cmd)	Stores line count to represent lateral position of cursor in display.
A9	Backspace Cmd	Stores line count so that count can be reduced by 6 to provide the line count of the next character position to the left of that represented by original line count.

Figure 2-77. Generation and Purpose of Save Line Counter Signals

preset, line counter storage is decremented by 6 in the normal fashion. Thus, line counter storage is reduced to a count of 234, which represents the BCD column of the last character position of a line. The outputs of line counter storage are routed to the line counter compare circuits.

The line counter compare circuits (ALD C9.05.16.2) contain a straightforward exclusive OR'ing of the line-counter outputs and the stored line count. The Line Compare signal is generated when a successful compare is made. In the ALD, note that line counter bit 1 must be a zero before a compare can be made. Although bit 1 is not stored (for the reasons stated previously), it must be used in the compare circuits to prevent a line compare for odd-numbered line counter statuses, which are the same as line storage in all respects except for line counter bit 1.

Display Compare

The display compare logic is shown in Figure 2-78. Address register bit 1, which is set (1) for an odd display and clear (0) for an even display, is used in conjunction with the outputs of the Even/Odd trigger to detect display compare. Assume that an odd display has been addressed and that AR Bit 1 is a 1. Then, A4 will have -Y AR Bit 1 as one input. At ring 6 time of each Even Disp time, A4 is conditioned and sets the Disp Comp latch. Note that the odd display compare is made near the end of Even Disp time to permit the compare to be present during the full duration of Odd Disp time. AND 5 represents a similar compare for the even display late in Odd Disp time.

Left/Right Storage

The Left/Right Storage trigger is used to store the status of the bit 256 trigger (Left/Right trigger) of the line counter when a save-buffer-location order is issued by counter storage control. The Left/Right Storage trigger is shown as part of Figure 2-78. Note that AND circuits A1 and A3 are used to load the storage trigger in much the same way as described for both the Upper/Lower Storage and the BCD/V2-V4 Storage triggers. AND 2 functions to complement the Left/Right Storage trigger from left to right when required during a write or read operation that crosses the left-right interface of the display presentation.

The outputs of the Left/Right Storage trigger are used as inputs to the buffer selection circuits and to the column compare circuits.

Buffer Selection Circuits

The buffer selection circuits (Figure 2-78) are used to select one of the four buffers for an impending operation. The selection occurs in two phases. When the TIC Found latch is set, the buffer selection

circuits are affected immediately, and a buffer selection is made. This buffer selection must be maintained over a relatively long period. The position storage circuits are used to hold the buffer selection after the TIC Found latch is reset.

In Figure 2-78, note that buffer position 1 is selected when either A16 or A17 is conditioned. The inputs to A16 and their significance are as follows:

1. TIC Found Gated: TIC has been found, and an address selection has been made.
2. Upper buffers: A dynamic indication that the display counters were in upper (buffer 1 or 3) when TIC was found.
3. Left Disp BCD Col: A dynamic indication that TIC was found in the left display area (buffer 1 or 2).

Note that when 2 and 3 are combined, the buffer associated with TIC is narrowed down to buffer 1. Thus, the conditioning of A16 represents the initial buffer selection that occurs when TIC is found.

When TIC is found, the position storage circuits are loaded with the contents of the common control counters. In the case described above, the pertinent storage conditions are as follows:

Left/Right Storage trigger----left
Segment Storage trigger------upper

Now consider the inputs to A17 and their significance:

1. Upper Storage: Upper/Lower Storage trigger in upper.
2. Output of A9: Left/Right Storage trigger is in left, and BCD/V2-V4 Storage trigger is at BCD (A7).

   or

   The BCD V4 Col input to OR 15 is conditioned, which also indicates left display.

The input conditions to A17 narrow the buffer selected to buffer 1 (upper, left), as was true for A16. The difference is that now the buffer selection is derived from the static conditions present in the position storage circuits.

In Figure 2-78, AND circuits A10-A15 illustrate the way in which buffer positions 2, 3, and 4 are selected. Each buffer selection is derived from a pair of AND circuits that operate in a manner similar to A16 and A17 for buffer 1.

Note, in Figure 2-78, that not all buffer selections are required for all 2848 models: Model 1 has a buffer 1 only; Model 2, buffers 1 and 2; and Model 3, buffers 1, 2, 3, and 4.

Video Buffer Selection

- The video buffer selection circuits select the buffer from which video information is to be read out to the even and odd display stations.
- Separate selection circuits are employed to select the A and B delays for each buffer.

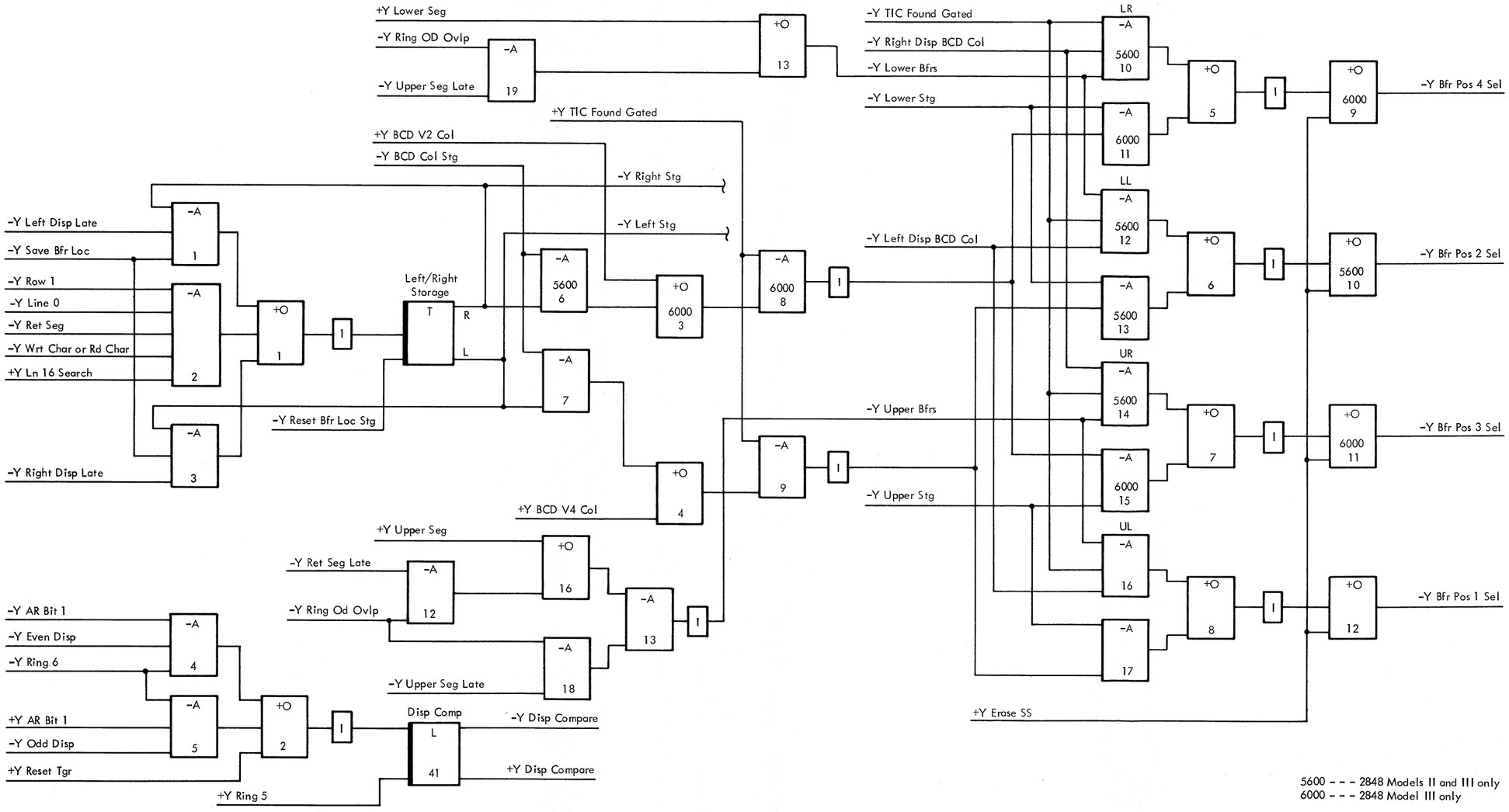
The video buffer selection circuits provide the necessary selection levels required by the display adapter to gate video information from the buffers to the display stations. Separate video buffer selection circuits are used to select the A delay lines and the B delay lines located in each of the four buffers. Since the selection circuits for the A and B delays are similar, the theory of operation for only the A delays will be discussed in detail. This information is also applicable to the B delay selection circuits.

The video buffer selection circuit for the A delays is illustrated in Figure 2-79. AND's 3 through 10, when conditioned, supply video buffer selection levels for both the even and odd A delays for the four buffers. Each AND is selected on the basis of the following input requirements:

Even or Odd Display Station
Upper or Lower Segment
Left or Right Display

The input requirements necessary to generate the video selection levels for the eight A delays used in a 960-character display are listed in Figure 2-80. The selection levels must be generated approximately 250 ns before video gating is initiated to avoid slivering or unreliable video readouts. This preselection control is accomplished by the remaining circuits shown in Figure 2-79. For example, upper segment selections (buffers 1 or 3) become active when the signal requirements to OR-AND 1 are received in conjunction with the even and odd levels supplied by OR 3 and I2, respectively. Although the Left and Right Display levels are also necessary for buffer selection, they do not determine turn-on or turn-off timing of the video selection AND's. These levels are employed to select either buffers 1 and 2 or buffers 3 and 4 for video readout.

Assuming buffer 1 is to be selected (AND 3 conditioned), it becomes advantageous to consider the status of both the even and odd display stations before the selection is made. The even display station will be readied for display as video is displayed on the odd station. After odd check time (parity check time for the odd display), the Ring Odd OVLP pulse, together with the Ret Seg Late signal, conditions AND 1, which selects the even display station for display. The final requirement to AND 3 is provided by OR-AND 1. This output becomes available when Upper Seg and the output of AND 1 are coincident. Video from buffer 1 can now be gated to the even display station from the A delay. Readouts from the B delay are effected in a similar manner. After seven video bits have been read out from the A and B delays, buffer 1 (AND 4) for the odd display station is selected to permit video data readout to the



5600 - - - 2848 Models II and III only
6000 - - - 2848 Model III only

Figure 2-78. Buffer Selection and Display Compare

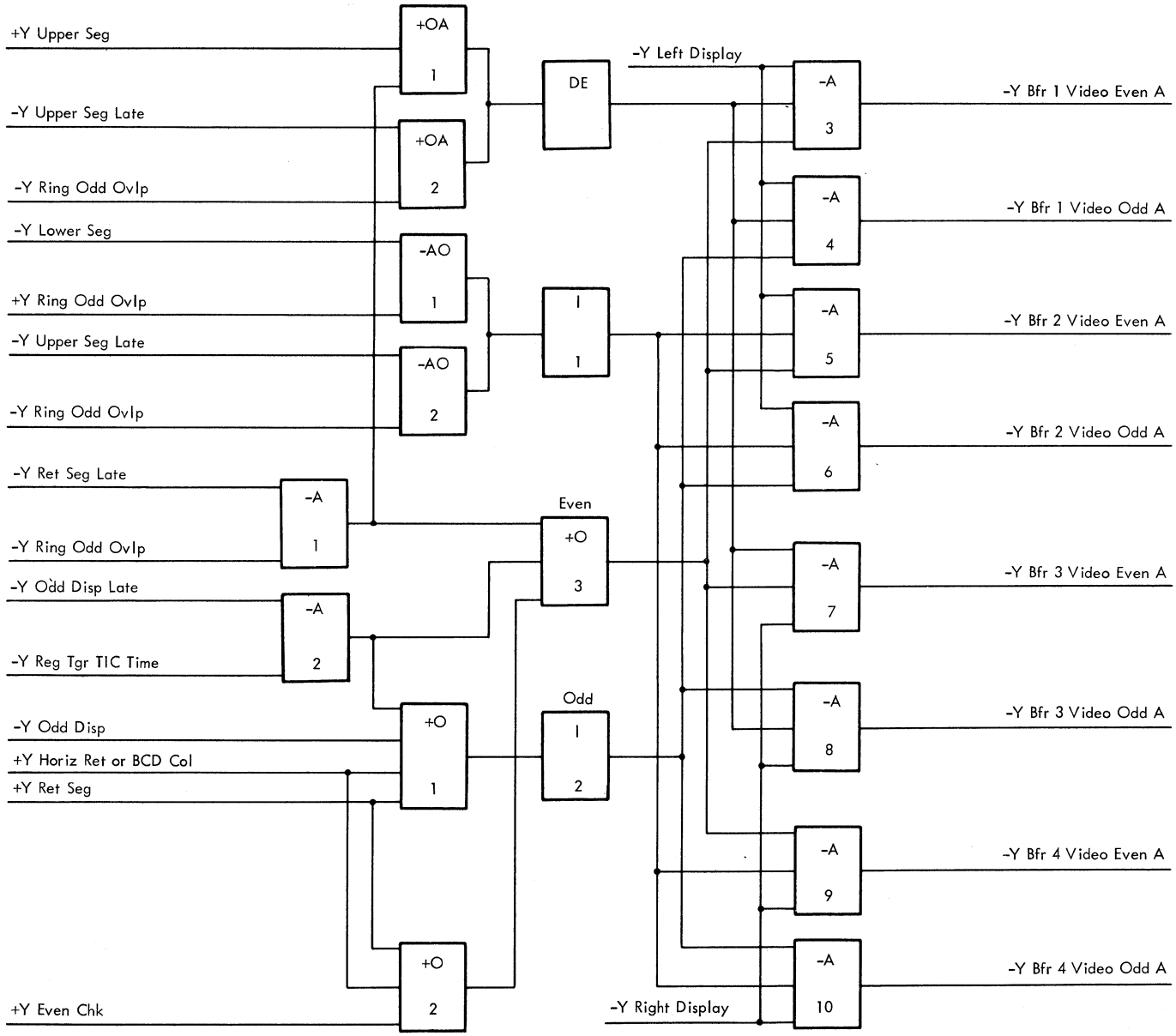


Figure 2-79. Video Buffer Selection, A Delay

odd station. AND's 3 and 4 are selected alternately in this manner until a full slot has been displayed on both stations. At this time, the Ring Odd OVLP, together with the Upper Seg Late level, fully conditions OR-AND 2, whose output deconditions buffer 1 selections (AND's 3 and 4) for both even and odd display stations. Selections for buffers 2, 3, and 4 (AND's 5 through 10) are activated in a similar manner. Buffer selection is not permitted during horizontal retrace, BCD column readouts, or vertical retrace time.

Nondestructive Cursor Generation

- The NDC is not stored in the delay lines.
- The NDC is displayed 1.75 μs after the TIC.
- An attempt is made to write NDC during each character time (ring 1-7) of all BCD columns.
- The odd display NDC is displayed during even display time.
- The even display NDC is displayed during odd display time.

The nondestructive cursor (NDC) is generated by the special logic circuits discussed below. Unlike the destructive cursor, the NDC is not stored in the delay lines but is applied as a direct input to the video mixer supplying the display. Since the cursor is not stored in the delay lines and therefore is not

Buffer	Display Station		Segment		Section	
	Even	Odd	Upper	Lower	Left	Right
1	X		X		X	
		X	X		X	
2	X			X	X	
		X		X	X	
3	X		X			X
		X	X			X
4	X			X		X
		X		X		X

Figure 2-80. Video Buffer Selections for A Delays

regenerated automatically, the cursor must be rewritten each TIC time to maintain it on the display.

The NDC generator circuits are shown in Figure 2-81, including the NDC generator circuits that are part of the display adapter. Note that the adapter circuitry shown is restricted to that for the odd display only. The even display served by the adapter has its own NDC circuits. Similarly, each adapter has NDC circuits for its odd and even displays.

In Figure 2-81, note that the Disp Cursor latch is set at each ring 1 time that occurs during BCD time and that the latch is reset at each ring 5 time. The latch outputs are gated to the even displays during odd display time (AND 2) and to the odd displays during even display time (AND 3). This action of the common NDC generator circuits represents an attempt to display the NDC in each character position of the BCD column. The success of this attempted NDC write is governed by the status of AND 6, which requires that the Odd Cursor latch be set before it will be conditioned. The Odd Cursor latch is set at odd TIC time. Therefore, the odd display NDC will be written during the first even display time following TIC. This relationship is illustrated in Figure 2-82.

In Figure 2-82, note the location of the odd TIC (T) next to the B character. When the odd TIC is found, the Odd Cursor latch is set. However, this occurs during odd display time when the common NDC generator circuits are attempting to write the even display NDC (AND 3). The Odd Cursor latch remains set when the next even display time occurs. Then, when the Disp Cursor latch sets at ring 1 time, video is gated through AND 6 for ring times 1, 2, and 3. At ring 4 overlap, the Disp Cursor latch is reset. At ring 6 time, the Odd Cursor latch is reset through AND 5. Thus, the NDC has been written on the odd display during even display time.

The even display cursor is written during odd display time as shown in Figure 2-82. Note that the character BCD associated with the TIC is not disturbed during the NDC write operation. Since the NDC is written between and below displayed characters and is not associated with the delay lines, it can be moved within the display without affecting or disturbing the display.

Write Line Address

The write line address logic permits preselection of the start of any of the 12 possible lines (rows of characters) within the display for a write operation. The Write Line Address command can be issued either by the channel or manually from the CE panel; it cannot be initiated from the manual input keyboards.

When a write line address operation is to be performed, the first byte from the channel is the command byte. The four high-order bits of the first character after the command byte is the code for the addressed line. This 4-bit code is decoded within the line address circuits and is used to preset row storage and the Upper/Lower storage trigger as required to select the addressed line.

Command Decode

The Write DS Line Address command decode circuits are illustrated in Figure 2-83. AND 1 has inputs from both Bus Out and the character register. The Bus Out inputs represent an attempt to decode a Write DS Line Address issued from the channel. The character register inputs provide a means of decoding this same command when it is entered into the character register manually during CE test operations.

When a Write DS Line Address command is decoded, the Wr Ln Adr latch is set. The latch outputs are used within the interface circuits as an indication that a valid command has been decoded and to cause the transfer of the data byte containing the line code into the character register.

Decoder Operation

The line address decoder circuits are shown in Figure 2-83. Note that the inputs to the decoder are outputs of the character register that accepts data from the channel. The decoder is enabled at ring 7 when the first character after a Write Line DS Line Address is available (A5).

Decoder operation is summarized in Figure 2-84. Note that each 4-bit code in character register bit positions 4-7 is decoded to provide a 3-bit input to row storage and 1-bit that determines the status of the Upper/Lower Storage trigger. The decoder outputs can be viewed simply as rows 0-5 in the upper segment and rows 0-5 in the lower segment as indicated by the pattern established by the row storage

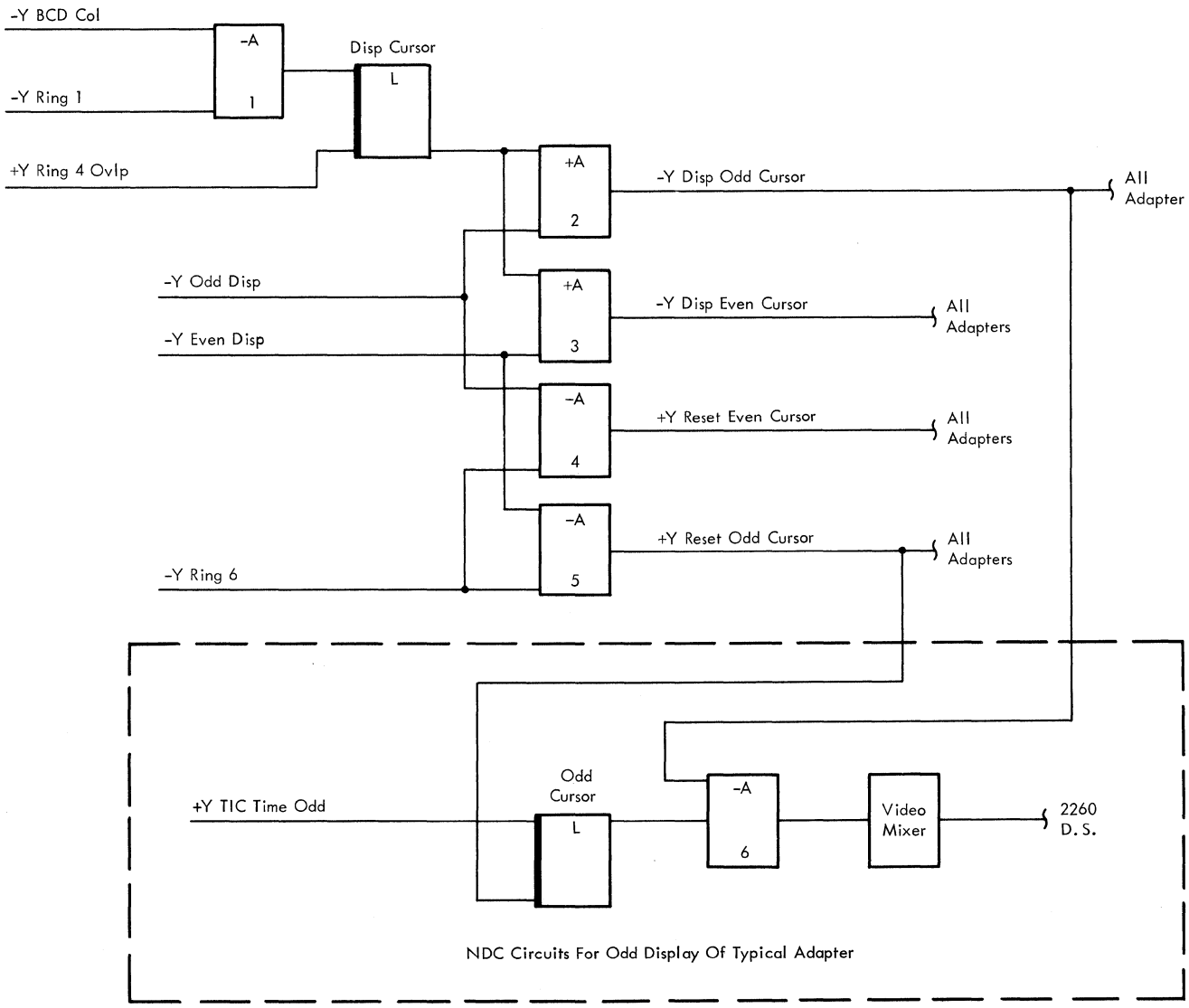


Figure 2-81. Nondestructive Cursor Generation

bits status and condition of the Upper/Lower Storage trigger in Figure 2-84.

Keyboard Command Decode

Commands are issued from the keyboard in the form of 6-bit command bits (bit positions 2 through 7). All keyboard command bytes are accompanied by a 1-bit in bit position 1 for use as a command identifier. If the command identifier bit is a 1, the 6-bit byte is decoded within the keyboard command decoder, and the associated command latch is set. When bit 1 is a 0, the keyboard input byte is treated as data and is transferred directly to the CBR. The Start command is somewhat special in that the contents of the command decoder are transferred to the CBR in addition to being decoded. This is discussed in conjunction with CBR control.

The keyboard command decode circuits are illustrated in simplified form in Figure 2-85. The command decode circuits are initially affected when the addressed display's TIC is found and common is not busy (A12). Then, the command latches are reset, and keyboard input data (bits 1-7) is gated into the input OR circuits shown as OR 2 through OR 8 in Figure 2-85. The outputs of OR 3-8 are immediately applied as inputs to the decoder AND's (A1-A9).

Now, the network formed by OR 1, OR 2, and A1 determines where the input data is to be directed. If KB bit 1 is a 1-bit, OR 2 is conditioned to produce a level that conditions one input to all command decode AND circuits (A2-A9), providing that OR 1 is not conditioned by either Inf Selected or by Busy Tgr. The gating level produced by the conditioning of OR 2 is inhibited only when the interface is selected or the Busy trigger is set. The status of the Reset AR

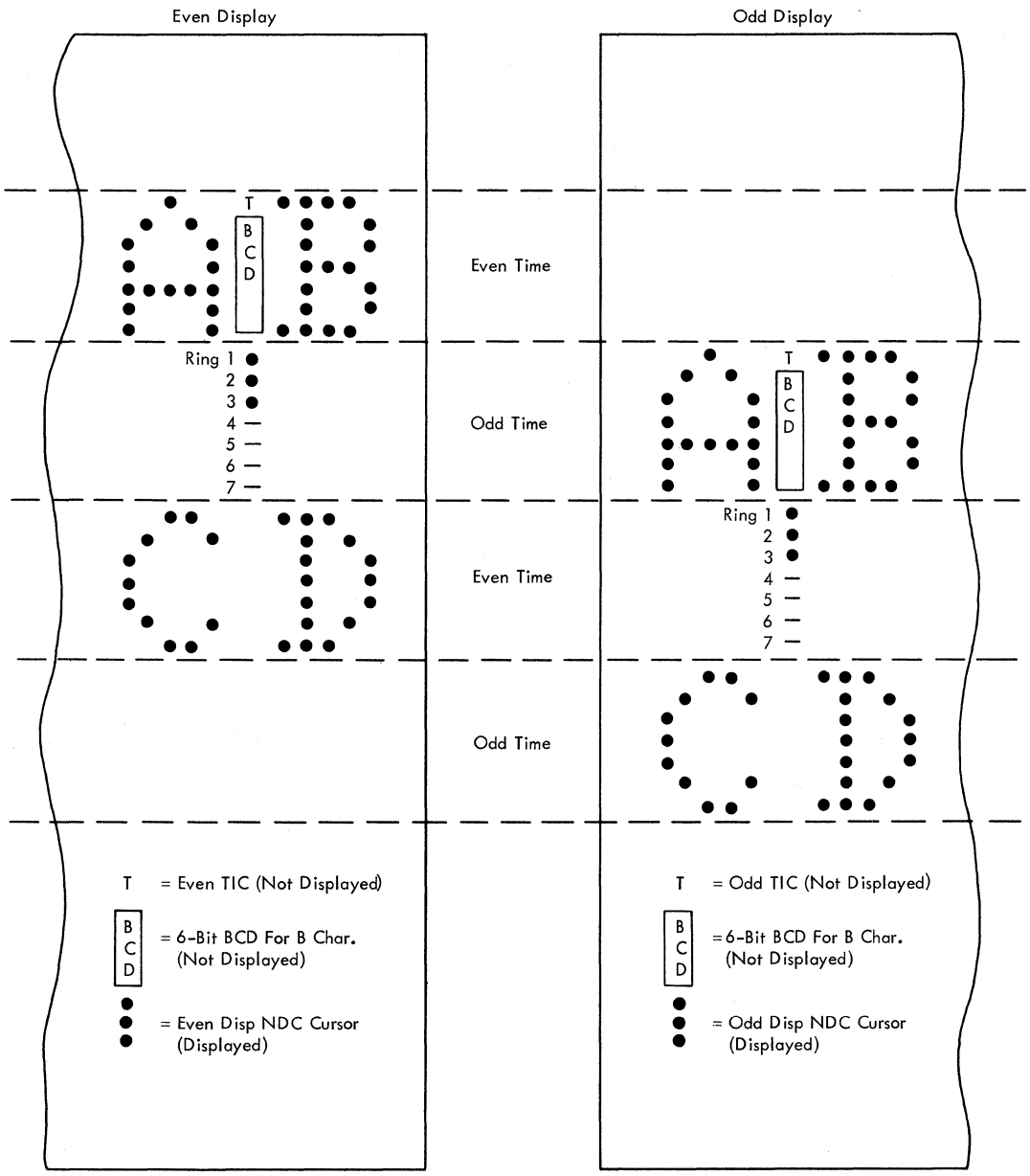


Figure 2-82. Display of NDC Cursor - Even and Odd

and Cmd Reg input to A1 at this time also fails to inhibit the gating level. Thus, one of the command latches will be completely conditioned as a result of the decode of the command byte and the generation of the decoder AND gating level produced by the 1-bit in the KB bit 1 position.

The fully conditioned AND sets its associated latch. The latch outputs are then used to effect the desired machine function.

Note that when the Erase command latch is set it inhibits the decode of the Start and Print commands. A similar relation exists between the Start latch and the Backspace and Down commands. These design measures were required to ensure proper decoder operation because the decay transients of the signal lines required for the Erase and Start commands could result in a spurious decode of the commands represented by the inhibited decoder AND circuits.

If the KB bit 1 sent with the input byte is a 0-bit, the decode AND's cannot be conditioned. Then, the outputs of OR 2-8 are transferred to the CBR as a data input. Note the +Y KB bit 1 output to the CBR

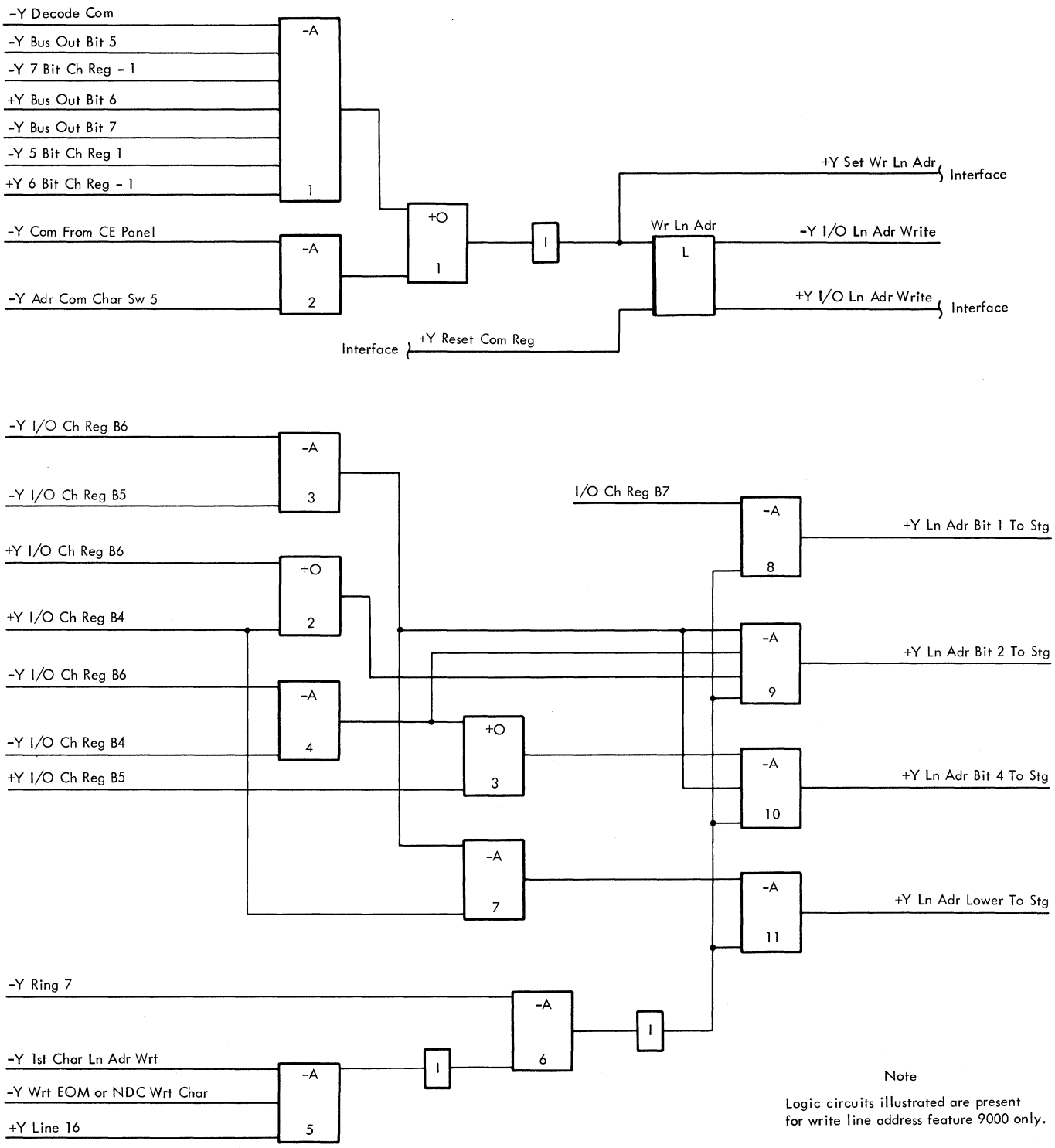


Figure 2-83. Write DS Line Address Decode and Gating

Char. Reg Bits 4-7 Line Code				Line Addressed	Row Storage Bits Set			Set Upper/Lower Storage to Lower
4	5	6	7		1	2	4	
0	0	0	0	1	0	0	0	No
0	0	0	1	2	1	0	0	No
0	0	1	0	3	0	1	0	No
0	0	1	1	4	1	1	0	No
0	1	0	0	5	0	0	1	No
0	1	0	1	6	1	0	1	No
0	1	1	0	7	0	0	0	Y
0	1	1	1	8	1	0	0	Y
1	0	0	0	9	0	1	0	Y
1	0	0	1	10	1	1	0	Y
1	0	1	0	11	0	0	1	Y
1	0	1	1	12	1	0	1	Y

Figure 2-84. Write Line Address Decoder Operation

control in Figure 2-85. The CBR control circuits use this input to permit input data to be loaded into the CBR.

The command latches are reset during the End Op operation regardless of whether data or a command was just processed through the decode circuits.

Parity Control

- Parity is assigned to each slot of even display-odd display of BCD data: one parity bit for the even display BCD data, and one parity bit for the odd.
- Even display parity bit is written in the A delay line.
- Odd display parity bit is written in the B delay line.
- Parity is updated during each write BCD operation.
- Parity is checked during execution of Read, Read Buffer commands, and the print from 2260 to 1053 adapter operation.
- TIC is not included in parity assignments or checks.

The parity control circuits are used to assign two parity bits to each slot of BCD data. (Recall that a slot consists of 84 data bits and two parity bits. Each slot contains 42 data bits plus a parity bit for the even display and an identical number of data bits plus parity for the odd display.) The parity bit assigned to each group of data bits is either a 1 or 0 as required to provide overall even parity (even number of 1-bits including the parity bit).

The overall parity scheme is most easily understood by starting with an erased even display with no data stored in the delay lines. Then, as BCD data is written to the even display, the parity circuits assign even parity at the end of the slot (even check time).

Assume now that one character of the BCD data just written is to be changed by writing a new BCD character in its place. As the write operation progresses, the parity circuits compare the old BCD bits with the new bits being entered in the delay line. In effect, this compare determines which of the four following situations exists:

1. An odd-1's BCD byte is being replaced by an odd-1's BCD byte.
2. An even-1's BCD byte is being replaced by an even-1's BCD byte.
3. An odd-1's BCD byte is being replaced by an even-1's BCD byte.
4. An even-1's BCD byte is being replaced by an odd-1's BCD byte.

It can be seen that the first two cases above will not affect the even parity previously assigned. However, the last two situations require that the parity bit be complemented to maintain overall even parity since in both cases the overall number of 1-bits has changed. Then, the parity circuits operate to modify parity.

Thus, the parity bit for each BCD column is assigned and constantly updated. When a read or print command is received and the BCD data is read from the delay lines, the read data is used as an input to the parity circuits, and, in a sense, parity is reassigned. When all 36 BCD bits (one BCD column) have been read, the odd or even count is compared with the parity that was stored with the data. If they do not compare, a parity error signal is generated.

The paragraphs that follow describe the parity assignment, parity update, and parity check operations. The parity circuits are illustrated in Figure 2-86.

Parity Assignment

Initial parity assignment is accomplished through AND circuits A11, A12, A13, and A14 in conjunction

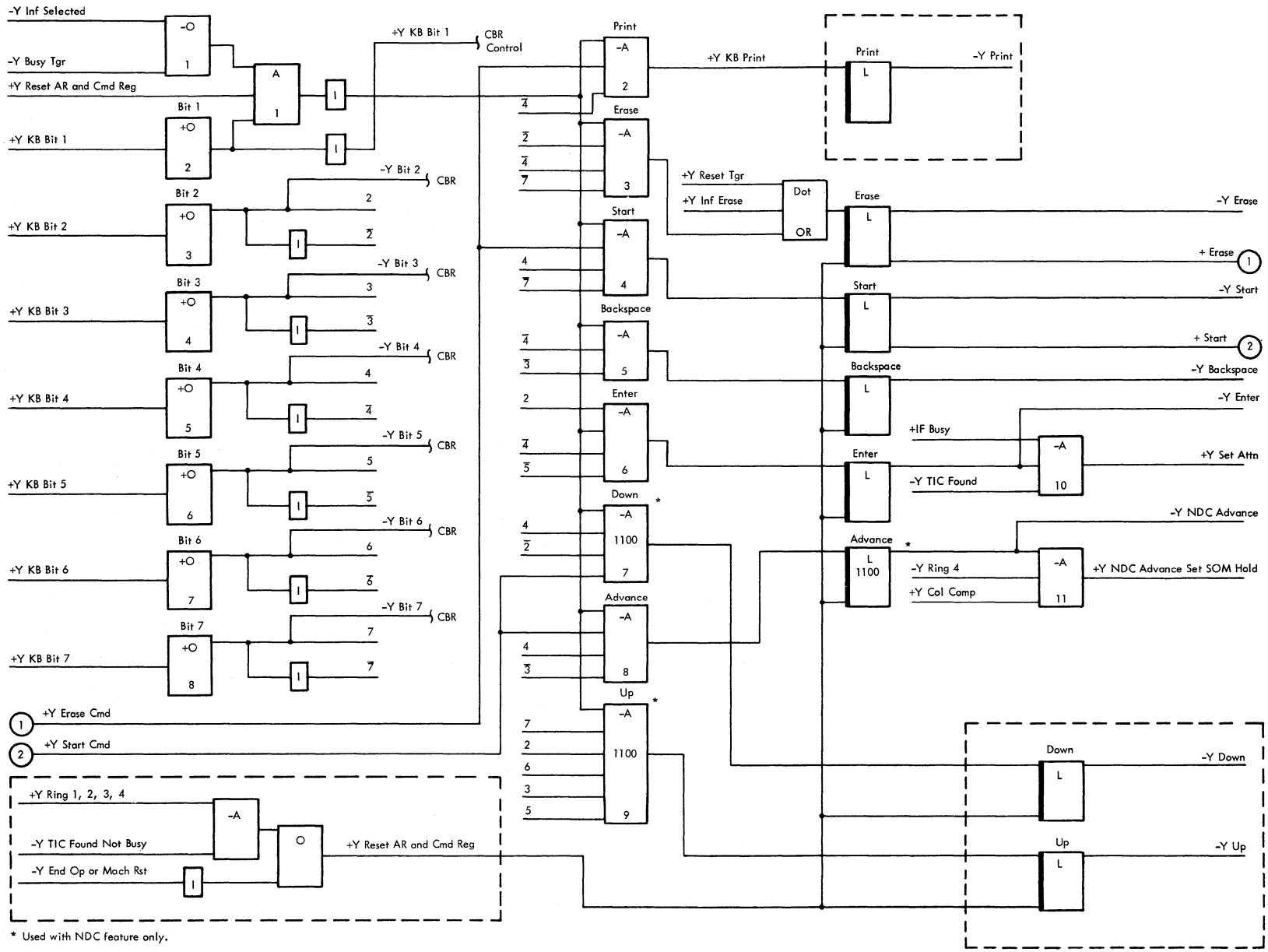


Figure 2-85. Keyboard Command Decoder and Command Latches

with the Parity trigger. Note the labeling of the four AND circuits; e.g., A11 is RD0: Wrt 1. These labels describe the conditions under which the AND circuits will be conditioned and will complement the Parity trigger. If the delay line contains no data, zeroes will be read constantly. Then, A11 will be conditioned each time a 1-bit is written to the A delay line, and A14 will be conditioned each time a 1-bit is written to the B delay line. Since the Parity trigger is reset during retrace time, the first 1-bit will complement (set) the trigger. Thereafter, each 1-bit complements the Parity trigger. At AND 21, the Parity trigger is not affected during parity check time (Ring Even or Odd) or during TIC time (Ring Ctr 1). It can be seen that any even number of 1-bits will leave the trigger reset and any odd number will leave the trigger set. At the end of the slot, the trigger's status is used to write the parity bit.

The parity bit is written through A1 or A3 for the even display and through A2 or A4 for the odd display. Note that these AND's sample the existing parity bit (A or B Dly BCD inputs) to determine whether the parity bit must be changed.

Parity Update

Once parity has been assigned to the even and odd data bits within a slot of BCD data, the parity bits must be updated to agree with the changes made to BCD characters during write operations. This update is accomplished using AND circuits A11-A14 and the parity trigger. Note the labels on the four AND circuits. Each label denotes a change in the 1's count within the BCD data. If a 1-bit is read and a 1-bit is written, no action is required since the overall 1's count remains the same. The same is true when a 0-bit is both read and written. Thus, each complement of the Parity trigger represents a change in the overall 1's count.

After the six bits of a new BCD character have been written, the status of the Parity trigger denotes whether an even or odd number of 1-bits have been added to or deleted from the overall 1's count. Then, at parity check time, the parity bit is sampled and updated as described for initial parity assignment (through AND's A1 and A3 for even displays, or A2 and A4 for odd displays). In this manner, the parity is always adjusted after each character write operation to maintain overall even parity for the BCD data.

If, for any reason, the parity bit becomes odd due to a bit dropout or pickup, a reset or erase operation must be performed to correct the condition of wrong parity.

Parity Check

The parity circuits perform a parity check on each BCD column when the BCD data for either an odd or even display is read from the delay lines.

When the read operation starts, AND circuits A15 and A16 are alternately conditioned as data is read from the delay lines. Each 1-bit read from either delay line complements the Parity trigger, which starts in the reset status. Thus, when all 42 BCD data bits for the selected display have been read, the Parity trigger will be left reset if an even number of 1's were read or set when an odd number was read. The Parity trigger's status thus directly represents what the parity bit stored with the data should be. The Parity trigger status and the parity bit are exclusively OR'ed at OR 1 and OR 2 for even displays or at OR 3 and OR 4 for odd displays. If the trigger status and stored parity are not the same, the output of the exclusive OR is gated through either AND 17 (odd display) or AND 18 (even display) as a parity error signal.

Parity Write Control

The parity check bits for the odd and even display BCD must be written at the end of each BCD slot. Only the even display or odd display parity bit can be written at any one time since either an odd or even display write (but not both) can be performed during one pass through the BCD column. The timing for the even and odd parity bit write operations is also shown in Figure 2-86.

Since the even display parity bit is always written in the A delay line, the Write A latch is used. This latch is set from AND 25 (Figure 2-86) at the start of Ring 7 or Even Chk. An attempt is made to reset the Write A latch at the start of Ring Even or Odd; however, the latch is held set at this time. The even display parity bit is written during even check time. Then, the Write A latch resets at the fall of Ring 7 or Even Check.

The odd display parity bit must be written during odd check time, using the Write B latch so that the bit is written in the B delay line. The Write B latch is set at the start of Ring Even or Odd and is held set. Then, the write B and Odd Check latches are reset at the start of Ring Ctr 1, thereby ending Ring Even or Odd time and ending the write odd display parity operation.

Note that the Write latch used in both the even and odd display write operations is turned on one bit time in advance of the actual parity write to ensure proper gating to the delay lines.

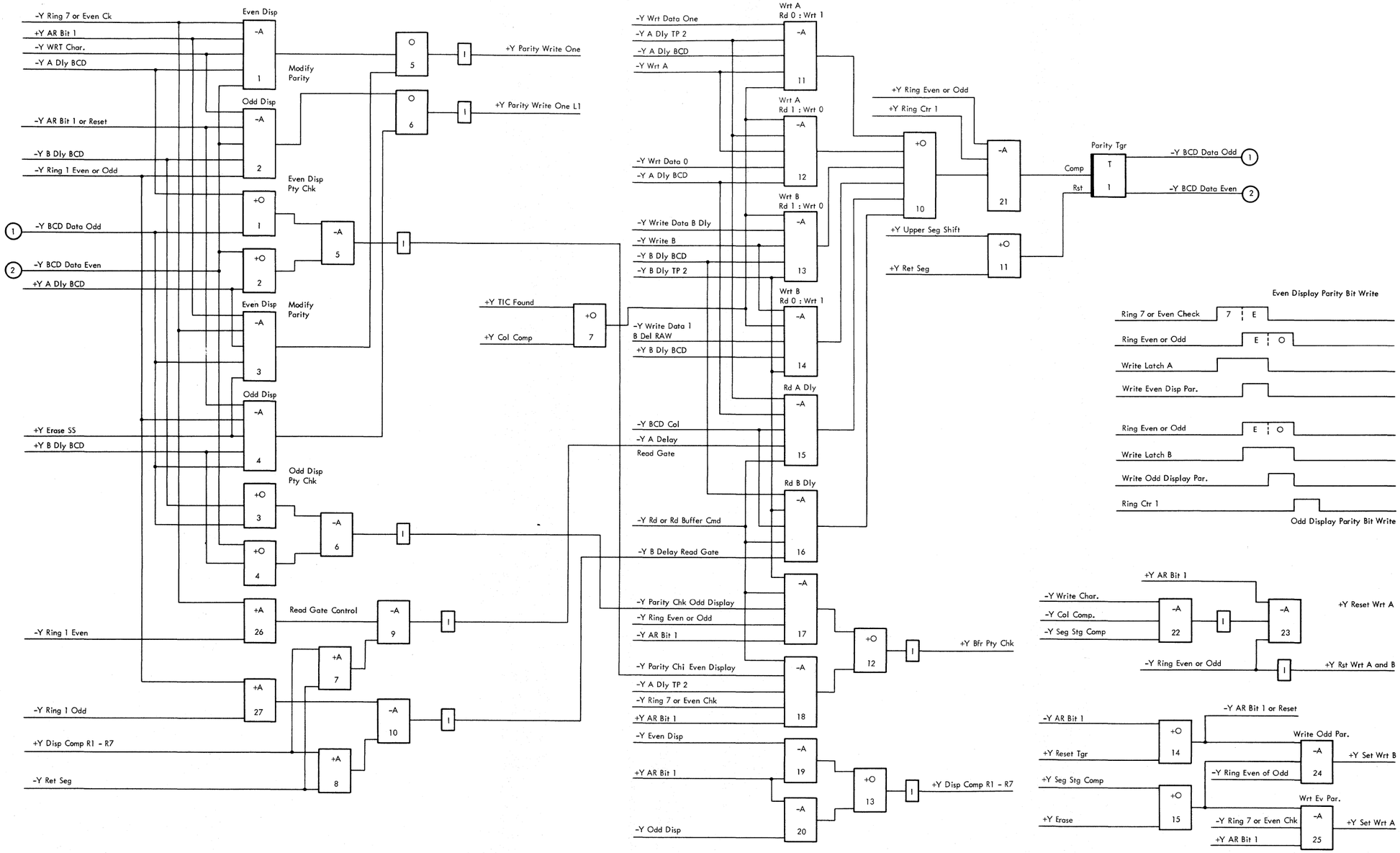


Figure 2-86. Parity Circuits

Parity Read Gate Control

The read gate control circuits ensure that the bits are read from the A and B delay lines in the proper sequence for either an even or odd display read operation. Note that the read gates are generated upon each display compare and all ring times from AND's A7 and A8 except when A9 or A10 are inhibited from A26 and A27, respectively. AND's A26 and A27 are used to inhibit reading of the parity bit during parity check time.

Printer Adapter Controls

The printer adapter control logic (Figure 2-87) within the 2848 common circuitry is activated when a Print command is decoded; it then governs the data transfer from the selected display buffer to the printer adapter. Only the printer adapter controls that are a part of the common equipment are described here. For detailed operations of the 1053 Printer, refer to the analysis provided under Printer Adapter.

The Print latch shown in the figure is set when a PRINT key is depressed at a keyboard and the ensuing Print command is decoded. The latch outputs are used to reset the write latches (A4), causing EOM to be encoded in the CBR without TIC (A6). Note that the EOM is written in the location in which TIC was found but, as stated above, that TIC is not written with the EOM code.

Now, a write cycle occurs, and EOM is written in the selected delay lines. After EOM has been written, AND 7 is conditioned, and the Start of Print Rd signal is generated. This signal sets the 1053 Disp Sel latch to indicate that the 1053 adapter is busy; resets counter storage, thus locating the first display position (upper left corner); and initiates a line search. As the line 16 search is entered, the WRT EOM latch is reset (AND 8). When line 16 is

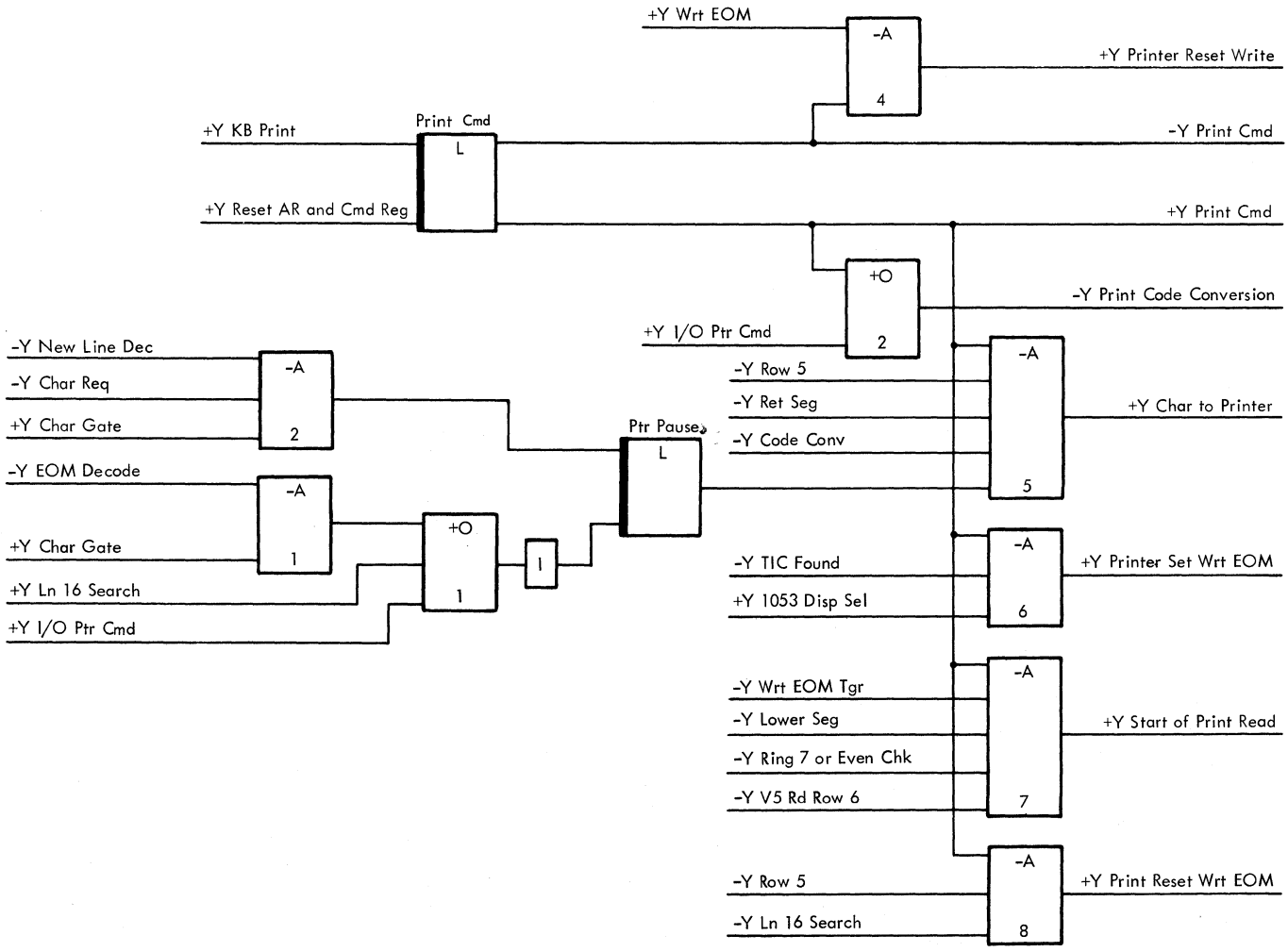


Figure 2-87. Printer Adapter Controls

found and the necessary compares are made, the first character on the display (upper-left corner) is read from the delay lines into the CBR. A character generator write/read cycle occurs, and, since the Code Conversion latch has been set, the tilt/rotate code for the first character is transferred to the 1053 Printer adapter. As long as the printer continues to request characters, the transfer continues as characters are read in succession from the selected display buffers, with each character transfer signaled to the printer adapter by the generation of Char to Printer from AND 5. If a new line code is decoded, the Ptr Pause latch is set to inhibit the Char to Printer signal until a line 16 search has been successfully completed. Then, the Ptr Pause latch is reset to gate the Char to Ptr signal to the printer adapter so that it can request the next character. If the printer does not request a character within a prescribed period, TIC is rewritten to provide a record of where the transfer is to be resumed when the printer next requests a character.

Operation of printer adapter controls, when print operation is initiated by the channel (I/O Ptr Cmd), is limited to the generation of the Print Code Conversion signal from OR 2. Other printer adapter control circuits are held deconditioned by the Not Print latch.

The overall role of the printer adapter control logic is illustrated in the flow charts in the FE Diagram Manual. The flow charts show the data and control interchange between all 2848 common control circuitry associated with printer adapter operation and the printer adapter itself.

Control Latches and Triggers

The functions of the control latches and triggers contained within display control are summarized in Figure 2-88. Also included in the figure are the logic references for the ALD pages that illustrate the latch and trigger networks. This reference can be used to locate each latch or trigger within the logic when a more detailed logic analysis is required.

The control latches and triggers, listed in Figure 2-88 in alphabetical order, are set in various combinations as part of the operational sequences depicted in the flow charts in the FE Diagram Manual. A basic knowledge of control latch and trigger functions is required to interpret these flow charts.

CHANNEL ADAPTER

When the 2848 Display Control is to operate in a local configuration with a System/360, the channel adapter is included to provide the required interface between the System/360 channel and the Display Control. The channel adapter then forms the connecting link through which all data and control exchanges between the channel and Display Control are made. The interface established, which is used to interface other I/O equipments to the system, is essentially the same as the standard IBM System/360 Interface-Channel to Control Unit.

In the paragraphs that follow, the channel adapter is described at the block diagram level to show the overall data flow within the adapter and to show its relationship to other areas of the control unit. When required, the unique logic areas of the channel adapter are discussed in detail. In addition, the interchange of control signals between the channel and the channel adapter for various operations is illustrated with timing diagrams and supporting text.

Block Diagram Analysis

The major logic elements of the channel adapter are illustrated in block diagram form in Figure 2-89. The function of each logic area is as follows:

1. Bus Out: Commands, addresses, and data are received by the channel adapter from the system channel via Bus Out; this consists of nine lines, bit positions 0-7 and a parity bit.
2. Character Register: An 8-position latch register that can be loaded from Bus Out (8 bits) or from the common buffer register of common control (6 bits). The character register converts the 8-bit code received from the channel to the 6-bit code used within the 2848 and performs a reverse conversion when information is transferred from the 2848 to the channel; i.e., 6-bit to 8-bit conversion.
3. Command Decoder and Register: Decodes commands sent from channel via Bus Out and sets Command Register latch associated with the command.
4. Bus Out Parity Check: Checks for odd parity of each byte sent to channel adapter via Bus Out.
5. Address Check: Detects unit address on Bus Out and enables address register and encoder circuits when unit address is decoded.
6. Address Encoder and Register: Converts 8-bit address byte from channel into 5-bit device address; sets address into address register for transfer to address decoder of 2848 common control.
7. Address Compare: Compares the address on Bus Out with contents of address register if a Busy condition exists when the address is issued. If the addresses compare, a Device Busy latch is set, and a special sequence is entered. If the addresses do not compare, the channel is presented with Control Unit Busy in the status byte.

Name of Latch or Trigger	ALD Page	Function
Busy trigger	C9.05.51.1	Set whenever common control unit is busy processing a display-station-keyboard, printer, or channel-adapter operation.
Cancel latch	C9.05.31.1	Set during a Start Cmd operation if an SOM character is found. This latch causes the Wrt Zero latch to be set after the EOM cursor or NDC TIC has been written in character position after SOM. Also set when existing EOM cursor is being erased. At this time, it is used to end the cancel operation.
Character Gate latch	C9.05.62.1	Turned on when a character is being assembled in the CBR for a read operation to the interface or printer, or when a particular character such as SOM, EOM, and N/L is being sought.
Code Conversion latch	C9.06.14.1	Set when the character generator is to perform a code conversion operation in lieu of character video generation.
Code Translate Read latch	C9.06.13.1	Set to initiate both the erase read and sense read portions of the character generator cycle.
Code Translate Write latch	C9.06.12.1	When set, enables the write portion of the character generator that sets all cores associated with the selected character.
End Operation latch	C9.05.36.1	Set at the end of an operation to initiate terminating sequence and to prepare common control for the next operation.
Even-Odd Display trigger	C9.05.85.1	Selects the even or odd display station for display alternately on a row basis.
Horizontal Blanking latch	C9.05.50.1	Provides a blanking level, which inhibits display of data on the CRT during retrace time and whenever BCD is read out from the delay lines.
Interface Selected trigger	C9.05.51.1	Set when the interface is actively connected to the common control unit.
Keyboard Command latches		
Erase	C9.05.61.1	Set when an Erase command is decoded; erases all data stored in the buffers associated with the display station.
Start	C9.05.61.1	Set when a Start command is decoded; after an SOM search, causes the Start symbol to be displayed. If an SOM is found during the search, the Cancel latch is set.
Backspace	C9.05.61.1	Set when a Backspace command is decoded; causes the cursor to move back one display position.
Enter	C9.05.61.1	Set when an Enter command is decoded; causes all data between start symbol and EOM to be transferred to the channel.
Advance	C9.05.61.1	Set when an Advance command is decoded; causes cursor to advance one display position.
Up	C9.05.61.2	Set when an Up command is decoded; causes the cursor to move up one line within the display with no lateral movement.

Figure 2-88. Control Latches and Trigger Functions (Sheet 1 of 3)

Name of Latch or Trigger	ALD Page	Function
Keyboard Command latches (cont)		
Down	C9.05.61.2	Set when a Down command is decoded; causes the cursor to move down one line within the display with no lateral movement.
Line Change latch	C9.05.35.1	Set when a line change is required. Will be set just before the row counter is stepped to the next-higher row count. Thus, the Row Ctr Stg Reg can be modified to the new row count.
Line Search latch	C9.05.33.1	Set when a particular character column is being sought. In a backspace operation, the line count of the character where the TIC is found is stored in the Line Ctr Stg Reg. This is then modified for the line count of the preceding character. The Line Search latch is set, and, when a line compare is obtained, the cursor can be written into the delay line. Also used during Rd MI when returning to a particular character location (such as where the SOM or EOM code is located).
Line 16 Seek latch	C9.05.35.1	Set any time the control unit is looking for the first character position of any line. This latch causes a pause in whatever operation is in progress at the time.
New Line latch	C9.05.34.1	Set when a N/L is decoded. This results in a line change to move to the first character position of the next line.
New Line Pause latch	C9.05.62.2	Set when a N/L has been read to the interface. This inhibits the transfer of all characters to the right of the N/L character (except the EOM).
Print Command latch	C9.05.61.3	Set when a keyboard Print command is decoded; configures common control to perform a print operation.
Printer Pause latch	C9.05.61.3	Set when a new line code is detected during a printer transfer; inhibits the printer character request until a line 16 search is completed.
Read Started trigger	C9.05.32.1	Used when reading to the interface. Turned on when the first character is read into CBR; then allows succeeding characters to be gated into CBR by the compare circuitry as long as the interface accepts the characters at a 390-us rate.
Reset latch	C9.05.90.1	Distributes Machine Reset and End Operation control signals, which are used to clear or preset counters, latches, and triggers throughout display control. This prepares the control unit to accept and execute ensuing commands and data transfers.
SOM Hold latch	C9.05.34.1	Set during an Enter Command operation when the SOM is located. Used to pause for one character position before writing the TIC in the character position after the SOM.
SOM Search latch	C9.05.33.1	Set when looking for an SOM code as a result of an Enter Command, Start Command, or the ending of an Rd MI operation.
Sync latch	C9.05.50.1	Generates Horizontal and vertical synchronization pulses employed by the display station sweep circuits.

Figure 2-88. Control Latches and Trigger Functions (Sheet 2 of 3)

Name of Latch or Trigger	ALD Page	Function
TIC Found latch	C9.05.47.1	Set when an address is entered in the address register to indicate that TIC was found.
TIC Search latch	C9.05.34.1	Set after TIC is written in character position after SOM on an Enter Command. At this time, the control unit is looking for the original TIC either to write an EOM code with NDC feature or just to erase the old TIC.
Write A latch	C9.05.28.1	When set, enables the writing of data in the A delay line of the selected buffer.
Write B latch	C9.05.29.1	When set, enables the writing of data in the B delay line of the selected buffer.
Wrt Char latch	C9.05.30.1	Set when a character is being written into a delay line buffer.
Wrt EOM latch	C9.05.30.1	Set whenever the binary code for the EOM symbol is to be entered into the CBR.
Wrt SOM latch	C9.05.30.1	Set when the SOM character is being written into the delay line.
Wrt TIC latch	C9.05.30.2	Used with NDC feature for writing the TIC in the delay line (similar to Wrt EOM).
Wrt Zero latch	C9.05.31.1	Causes all zeroes to be written in the delay lines of the selected adapter.

Figure 2-88. Control Latches and Trigger Functions (Sheet 3 of 3)

8. Status Register: Records unit status for transfer to channel via Bus In.
9. Sense Register: Records information that amplifies Unit Status conditions indicated by the contents of the status register.
10. Parity Assign: Assigns odd parity to all 8-bit bytes transferred to the channel via Bus In.
11. Bus In: A 9-line path (bits 0-7 and a parity bit) over which all transfers from the channel adapter to the System/360 channel are accomplished.

Out Tag Delays

- Service Out causes a Service Out Delayed signal to be generated 1.2 μs after the Service Out signal.
- Command Out causes a Command Out Delayed signal to be generated 1.2 μs after the Command Out signal and, in addition, sets the End Command Out latch.
- The End Command Out signal is not gated to 2848 circuitry until the Command Out tag is dropped.

Out tag delay circuitry is shown in Figure 2-90. Since the Command Out and Service Out tags are generated at different times, they can share the 1.2-μs delay circuit.

Command Out Delayed

The Command Out signal is generated by the channel during an initial selection to notify the 2848 that the device address returned to the channel was correct and that a command byte is being loaded on the Bus Out lines. The Command Out signal is applied to A1 (Figure 2-90), partially conditioning that circuit. In addition, Command Out is delayed 1.2 μs by the delay circuit. When the delay expires, A1 is fully conditioned and generates the Com Out Del (command out delayed) signal. The delay provides time for parity checking.

Com Out Del gates the command byte to the command decoder and, in addition, sets the End Com Ot (end command out) latch.

The EOM Com Ot signal is not gated from A2 until the Command Out tag drops. When the tag drops, the End Com Ot latch is reset after 1.2 μs due to the effect of the delay circuit. The End Com Out signal, therefore, is applied to 2848 circuitry for 1.2 μs immediately after the Command Out tag is dropped. The End Com Out signal is used by the 2848 interface controls as a flag to keep track of the operational sequence (i.e., command portion of the sequence has been completed).

During transfer sequences, the command out circuitry functions in the same manner as in initial selection, except that the Command Out tag is used only to signal the 2848 to proceed with the transfer sequence.

In a stack status sequence, the command out circuitry is used twice: the first time, for proceed (or command during initial selection); the second time, to indicate to the 2848 that the status byte was not taken. The command out response to a Status In tag is described in detail in the stack status operational sequence.

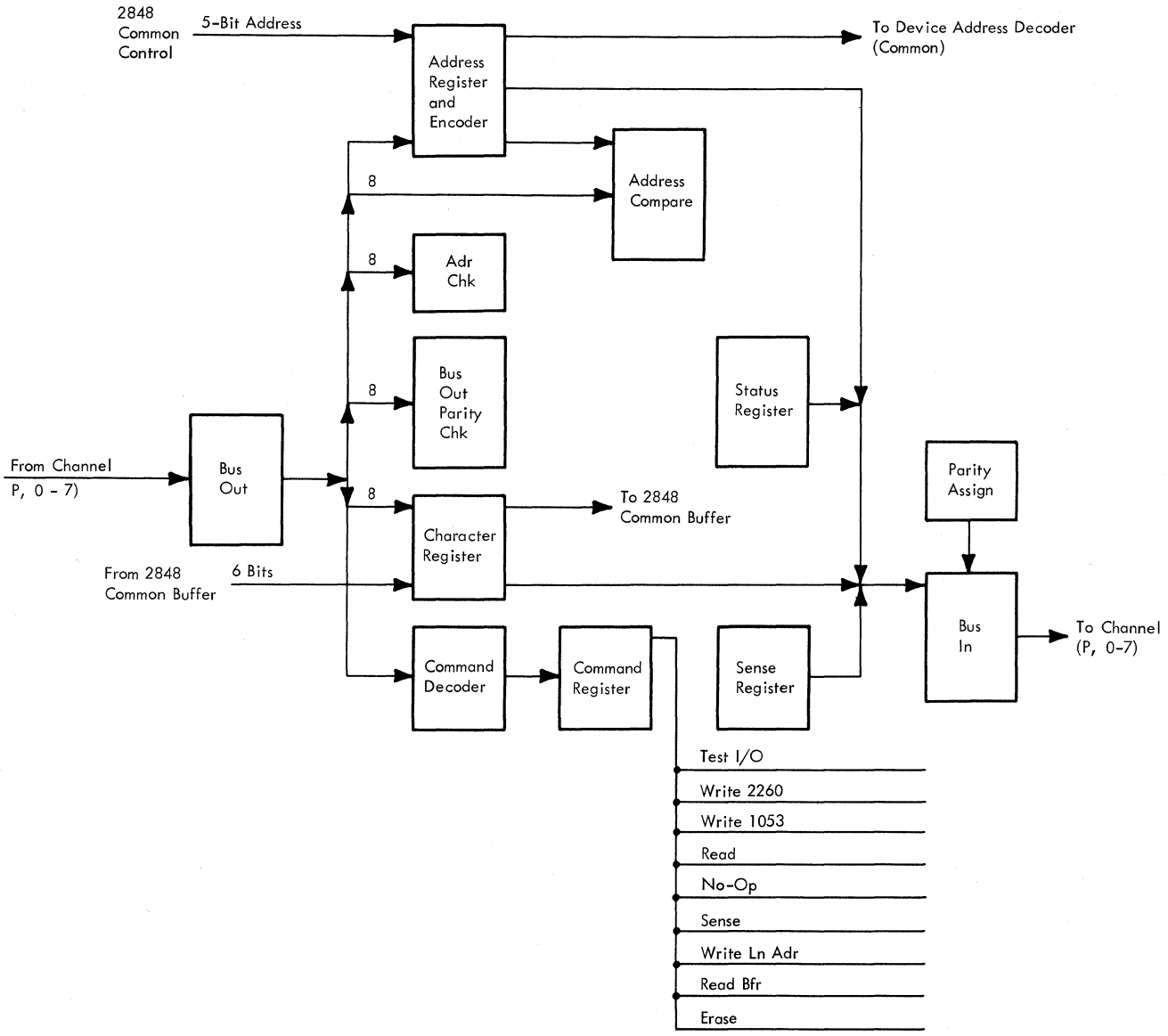


Figure 2-89. Channel Interface Controls

Service Out Delayed

The service out delay circuitry operates in the same manner as the command out delay circuitry described above. That is, Serv Out Del is developed by A3 (Figure 2-90) as a result of the Service Out signal being applied to one input and the same signal, delayed 1.2 μs, being applied to the other input.

During a write operation, the Serv Out Del signal initiates reading of the Bus Out lines. The 1.2-μs delay allows parity checking. The Service Out Delayed signal is also responsible for dropping the Service In tag.

During a read or status operation, since Service Out was generated as a result of the channel having read the Bus In lines, the Service Out Delayed signal is used mainly to continue the sequence by dropping the Service In tag. Service Out is also the normal channel response to Status In, and it causes Status In to be deconditioned.

Control Latches

In the paragraphs that follow, the latches that are used to control the operational sequences of the channel adapter are described with respect to their basic function. When required, a detailed explanation of latch operation and an accompanying illustration are provided.

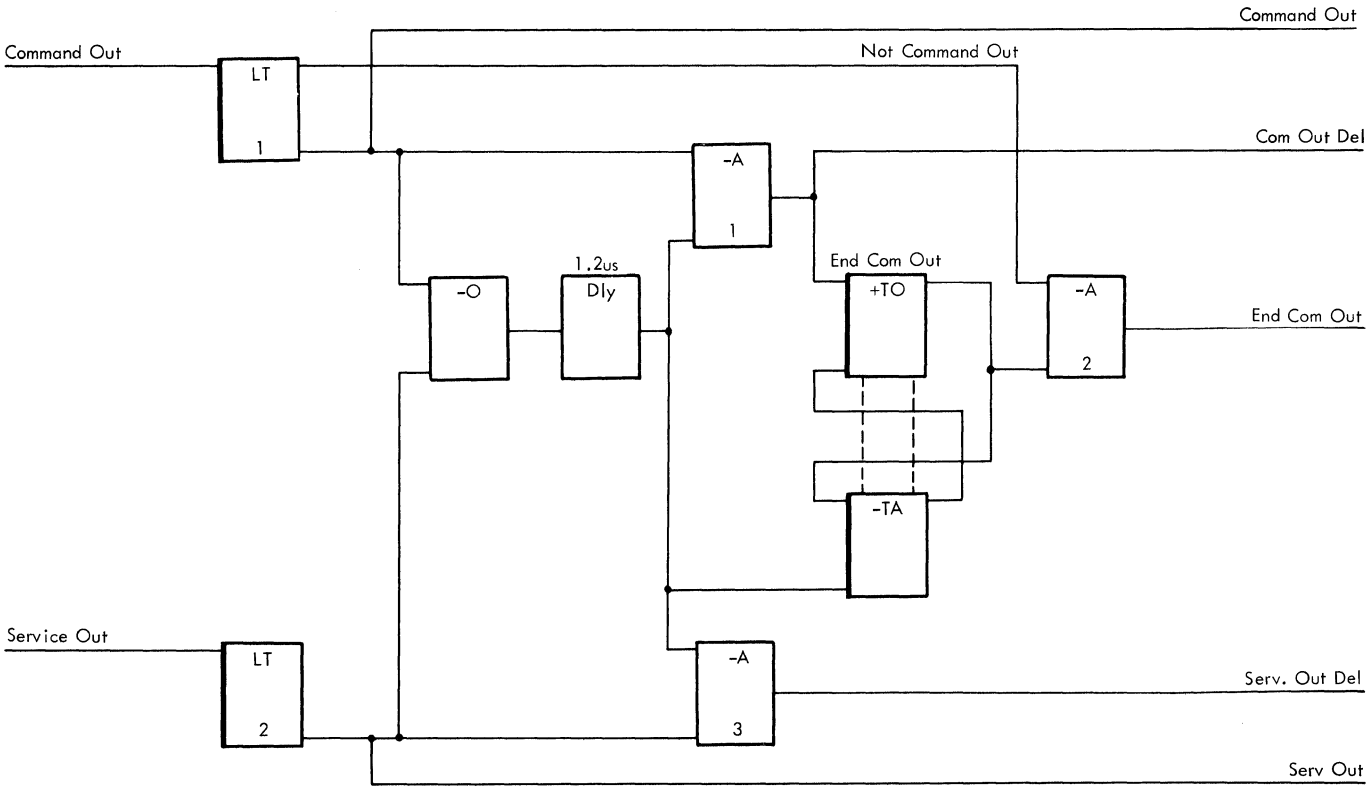


Figure 2-90. Out Tag Delays

Channel Request

The Channel Request latch is set at the beginning of all channel-initiated operational sequences when the following conditions are met:

1. Address Out (the channel has placed an address on the Bus Out lines).
2. Our address On Bus Out (a legal address is on the Bus Out lines).
3. Not Inhibit Request (select has not been propagated).
4. Not Interface Busy (control unit is not selected or does not have Status pending).

When the Channel Request latch is set, its outputs condition interface control circuitry to allow a channel-initiated selection to proceed when Select Out is raised by the channel.

The Channel Request latch is normally reset by the the Status In Delayed signal, which occurs near the end of a channel-initiated operational sequence. The latch is also reset by an I/O Reset Long signal which resets all interface control circuits.

Control Unit Request

The Control Unit Request latch generates the Request In signal, which indicates to the channel that the control unit has data or status information and is ready to begin transferring.

Status Request

The Status Request latch conditions circuitry necessary to send status information to the channel. The Status Request latch output sets the Control Unit Request latch if the Stack Status latch is not set.

Service Request

The Service Request latch is set to condition circuitry necessary for a data (sense, read, or write) transfer. Setting this latch causes the Control Unit Request latch to be set, except when the Stack Status latch is already set.

Operational In Latch

The Operational In latch is set at the beginning of all operational sequences in response to the Channel Hold Select Out signal when a device is properly selected and the operation may continue. This latch also generates the Operational In signal to the channel as an indication that the device was selected.

Busy Latches

- Interface control circuitry contains three busy latches: Interface Busy, Device Busy, and Control Unit Busy.
- The Interface Busy latch is set at the beginning of an I/O operation and remains set until completion of the operation.
- The Device Busy latch allows the channel to interrupt a busy 2848 (Interface Busy latch set) to perform a status transfer if the addressed device is the device that causes the 2848 to be busy and if status is present. The Test I/O command receives normal status. All other commands will receive the contents of the status register, with the busy bit set in the status byte.
- The Control Unit Busy latch causes control unit busy sequences to occur when the channel attempts to address a device other than the busy device. (Status modifier and busy bit are presented as an immediate status transfer.)

Interface Busy: The Interface Busy latch is set during initial selection for any operation. When the operation to be performed is initiated by the control unit, the IF Busy latch is set by the signal that sets the Control Unit Request latch. Since the only operational sequence initiated by the control unit when the Interface Busy latch is not already set is a status operation (Attention latch set or Printer End following Intervention Required or Busy), the IF Busy latch is reset at the end of the sequence.

The Interface Busy latch is reset by the Reset Status signal when the command register is reset (at the completion of the operation).

The Metering In signal is generated whenever the Interface Busy latch is set by a channel-initiated selection.

Device Busy: The Device Busy latch controls the sequence of events in a command-to-busy device sequence. The latch is set under the following conditions:

1. Interface Busy.
2. Channel Request latch not set.
3. Address Out tag up.
4. Status information available, and the address on the Bus Out compares with the address in the address register.

If the Device Busy latch is set, it will be reset by a Reset Status signal upon completion of the status transfer. If, however (before transfer of the status byte), the channel indicates that status is to be stacked (Command Out reply to Status In), the Device Busy latch is reset.

Control Unit Busy: The Control Unit Busy latch controls unit busy sequence. That operation effectively aborts any channel attempt to interrupt an operation in process. Setting the Control Unit Busy latch immediately causes a status byte to be sent to the channel, which indicates that the control unit is busy.

The Control Unit Busy latch is set under the following conditions:

1. Interface Busy.
2. Either the Bus Comp AR signal is not present, or no status information is available.
3. Address Out line is up.
4. Our address on Bus Out signal present (indicates a legal address for the 2848).
5. Channel Request latch not set.

Address In

The Address In latch is set at the beginning of all operational sequences to allow transfer of the address register to the Bus In lines. After a 1.2-μs delay (to ensure enough time for parity assignment), the Address In tag is sent to the channel, signifying that the address is on Bus In.

The Address In latch (Figure 2-91) is set in a slightly different manner for a channel-initiated selection than for other operations.

During a channel-initiated selection, the first portion of the sequence utilizes the Address Out tag, since the device address is sent to the 2848 before the Operational In signal comes up. Until the Address Out tag is dropped by the channel, A1 is deconditioned. When A1 is deconditioned, its output deconditions the upper output to A2 and simultaneously conditions the lower input to A2.

When the Address Out tag drops, the upper input to A2 becomes conditioned, and, due to the delay in A1, the lower input to A2 remains conditioned. During the time that A2 is fully conditioned, the Address In latch is set.

In operations other than channel-initiated selection, the Address Out tag is never up. As a result, as soon as the Operational In signal comes up, the A1 circuit is fully conditioned, and the Address In latch is set in the manner described for the channel.

Status In

The Status In latch (Figure 2-92) is set to initiate the status portion of an operational sequence. When any one of the AO circuits (1 through 5) is conditioned, the Status In latch is set. These circuits are conditioned under the following circumstances:

1. AO1 - During a control unit busy sequence, the Control Unit Busy latch is set. When the Hold Select Out line comes up, the Status In latch is set.

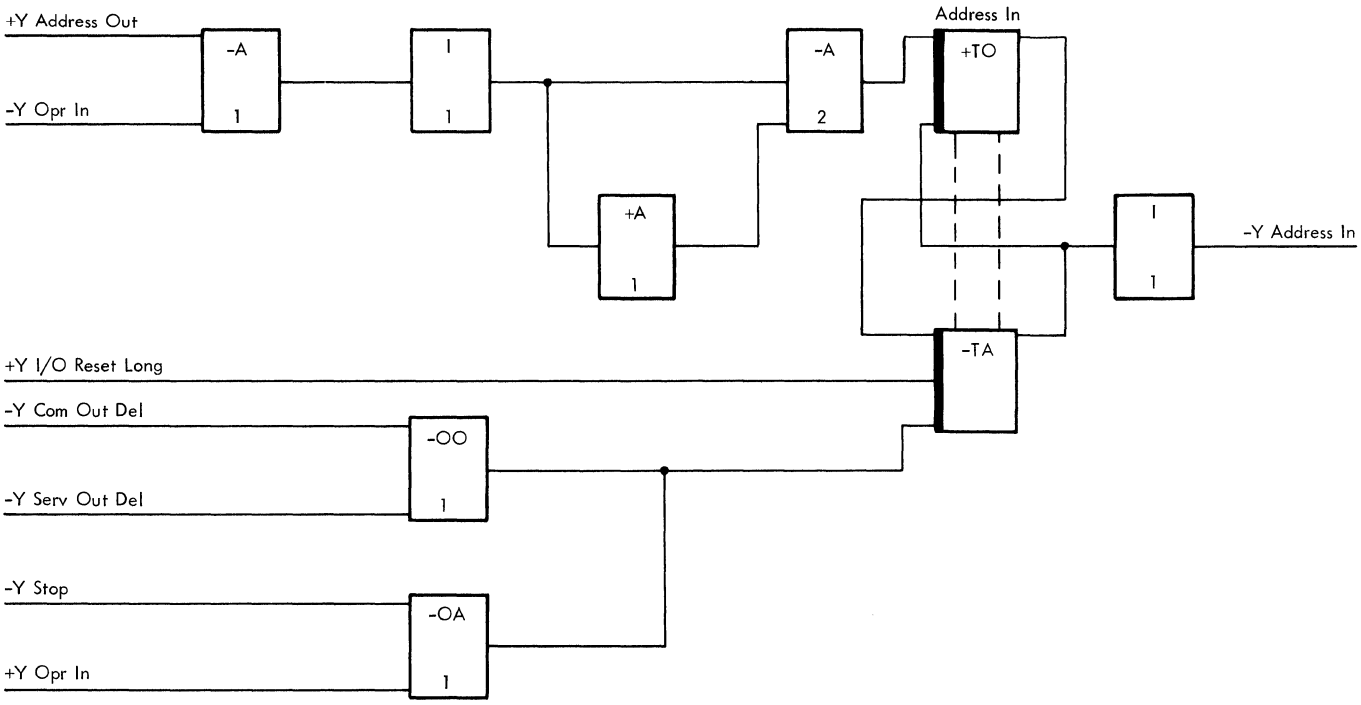


Figure 2-91. Address In Latch

2. AO2 - During the command-to-busy-device sequence, the Device Busy latch is set. When the End Command Out signal is generated, the Status In latch is set.
3. AO3 - During a channel-initiated selection sequence, the Channel Request latch is set. When the Command Out signal is generated, the Status In latch is set.
4. AO4 - During a control-unit-initiated status sequence, the Status Request and Control Unit Request latches are set. When the Operational In latch is set by the Hold Select Out signal, the Status In latch is set.
5. AO5 - When the control unit is used with a multiplexor channel in Forced Burst mode or with a selector channel, the conditions necessary to set the Status In latch can exist.

The Status In latch is reset by the same signals as the Address In latch. In addition, the Status In latch is reset at the end of a control unit busy sequence when the Hold Select Out line drops (A1, Figure 2-92).

Service In

The Service In latch is set during the data (Read) or sense sequence to control loading of data on the Bus In lines and to notify the channel that data is on Bus In. During other operations (Write), Service In is generated as a request for data from the channel.

Stack Status Latch

The Stack Status latch controls the events that occur when the channel refuses to accept status information from the 2848. This condition occurs when the 2848 raises the Status In tag to the channel (initiating the status transfer portion of an operational sequence), and the channel responds by raising the Command Out tag.

The Stack Status latch is reset by a Reset Status signal, which results from a successful status transfer, or by an I/O Reset Long signal.

Stop Latch

The Stop latch is set to terminate an I/O operation and to cause the 2848 to go to a normal ending.

The channel can set the Stop latch by responding to a Service In tag with a Command Out tag (Normal Stop). The Stop latch can also be set (Interface Disconnect) under the following conditions:

1. Address Out.
2. Not Hold Select Out - the channel is not selecting a control unit.
3. Operational In - our control unit is selected.

Remember End and Local-Remote Latches

The Remember End latch (Figure 2-93) controls the events in interface control circuitry that result from

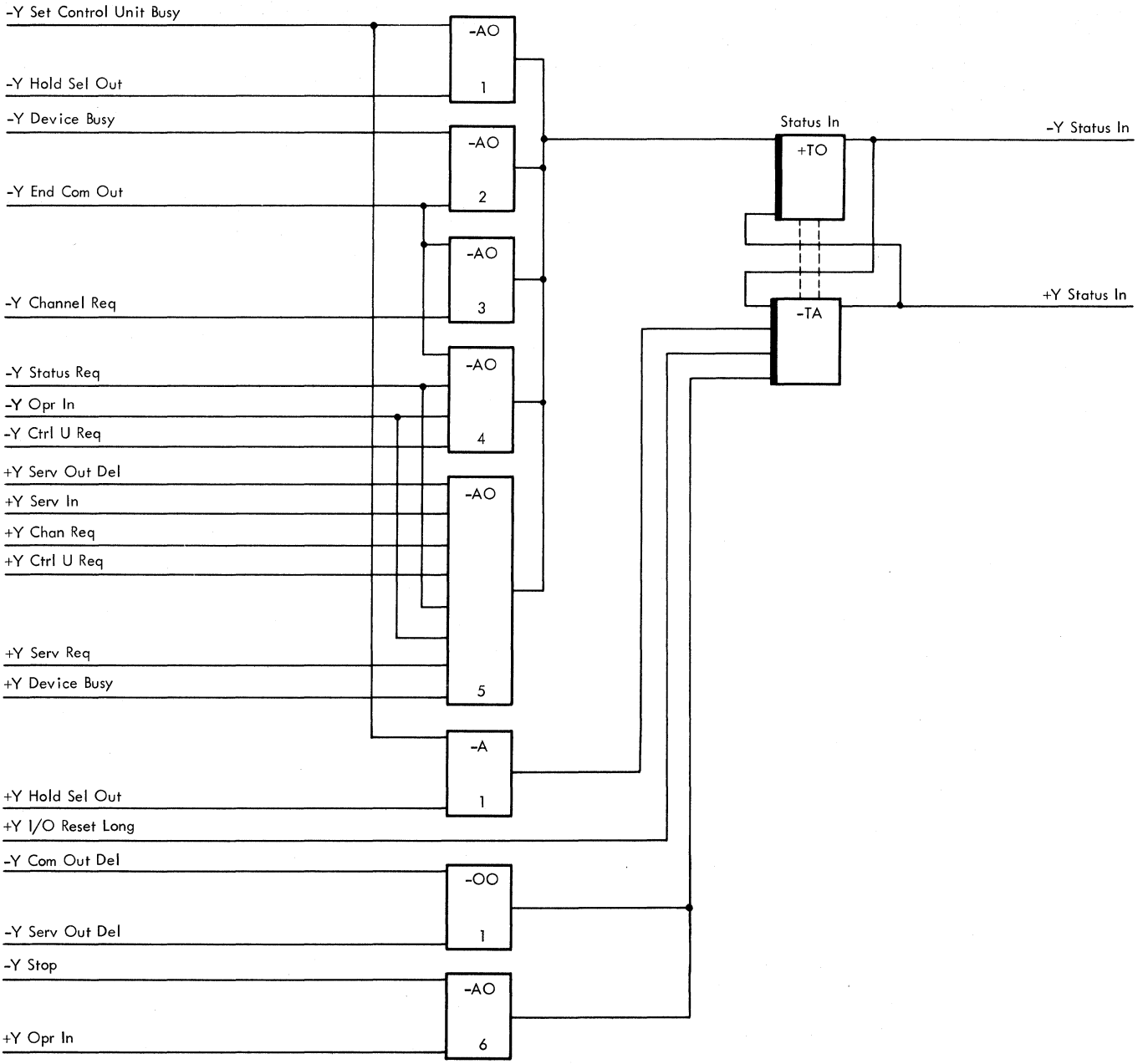


Figure 2-92. Status In Latch

the signal end operation or machine reset. When the end operation or machine reset is present, the Remember End latch develops the Condition Status Request signal. If neither AO2 nor AO3 is conditioned, the Remember End latch will remain set when the End Operation or Machine Reset signal drops.

If the Device End latch is set and the Not Interface Selected signal is present while the Remember End latch is set, the End Com Op signal is developed by AO1. This signal will set the Status Request latch and prepare control circuitry for an ending status transfer.

The Condition Status Request signal can also set the Status Request latch if the Write, Write Line Address, or Erase commands are not being performed and the Device End latch is set.

The Local-Remote latch (Figure 2-93) is set or reset as a result of the position of the LOCAL-REMOTE switch on the control panel of the 2848. When the switch is in the REMOTE position, the Remote line is up, and the CE Reset Long line is

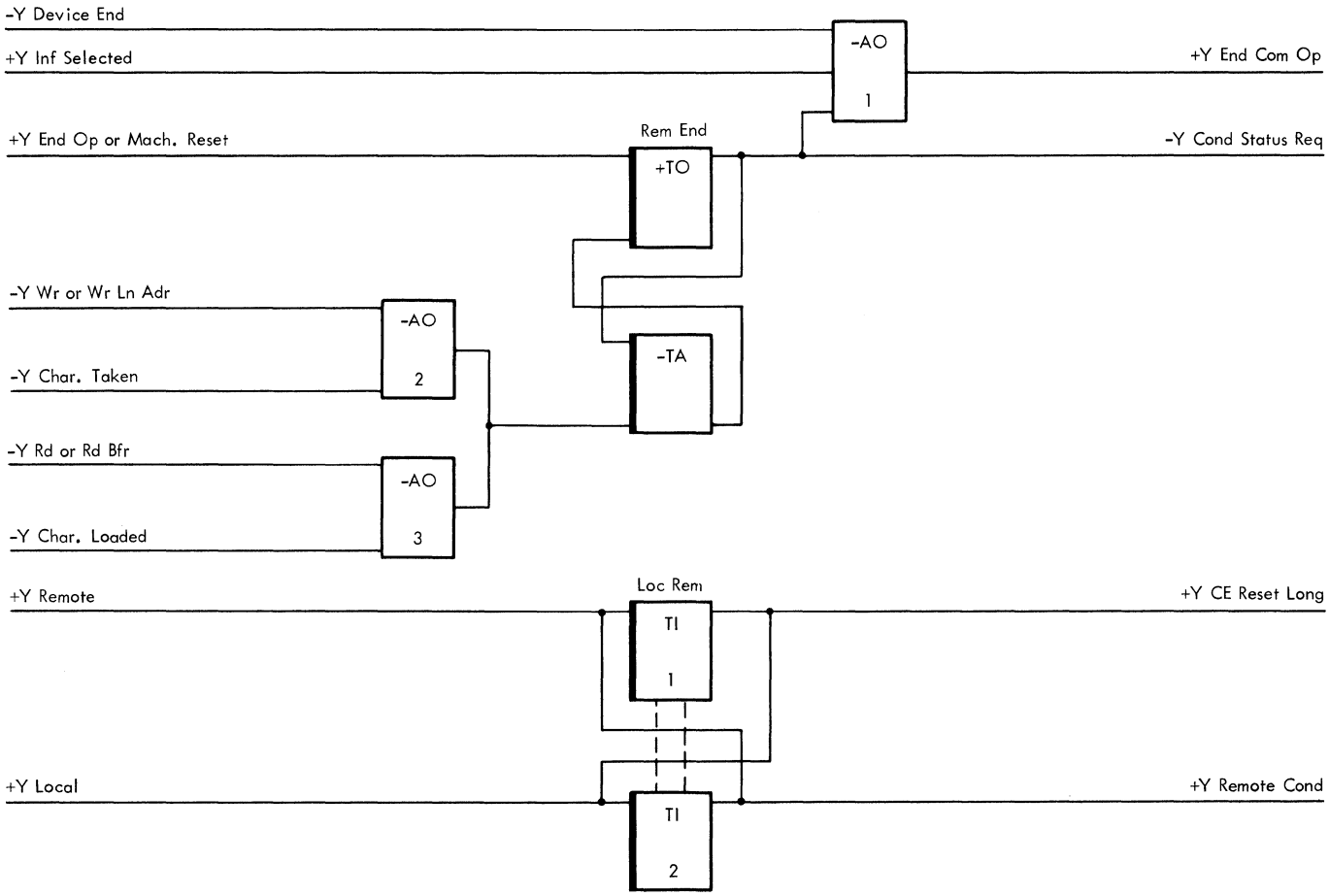


Figure 2-93. Remote End, Local-Remote

down. When the switch is in the LOCAL position, the reverse is true.

The CE Reset Long signal is used in local status to hold out circuitry which should be active only in remote operation.

The Remote Condition signal is used to deactivate System Reset in a local state.

Command Chaining and Inhibit Attention Latches

Command Chaining and Inhibit Attention latches are provided to inhibit keyboard operations after an I/O operation is completed, if the channel orders chaining or if a unit check bit was in the status byte (sense information is available).

Figure 2-94 shows the command chaining and inhibit attention circuitry. From the beginning of an I/O operation until the ending status byte is transferred, the Interface Busy latch is set, and its output is applied to OR 1. The output from OR 1 (through I1 and I2) deconditions keyboard and printer circuitry so that a status interrupt cannot occur.

Command chaining and inhibit attention circuitry is provided to maintain the Interface Busy signal to keyboard and printer circuitry even after the Interface Busy latch is reset (I/O operation ending status is transferred). The two conditions that might require this action are:

1. Command chaining requested by channel.
2. Sense information being available (if the channel chooses to initiate a sense transfer).

Command Chaining: If command chaining is requested by the channel during an ending status transfer sequence, the channel acknowledges receipt of the status byte by raising the Suppress Out signal in addition to the normal Service Out response. Since both the Service In and Device End latches are set during ending status, the Command Chaining latch is set from A1. The output of the Command Chaining latch holds up the output of OR 1, keeping the keyboards and printer locked out.

The Command Chaining latch remains set until the channel drops the Suppress Out signal, a new command is received by the interface, an I/O reset (short) is generated, or Unit Check is set as a result of a malfunction.

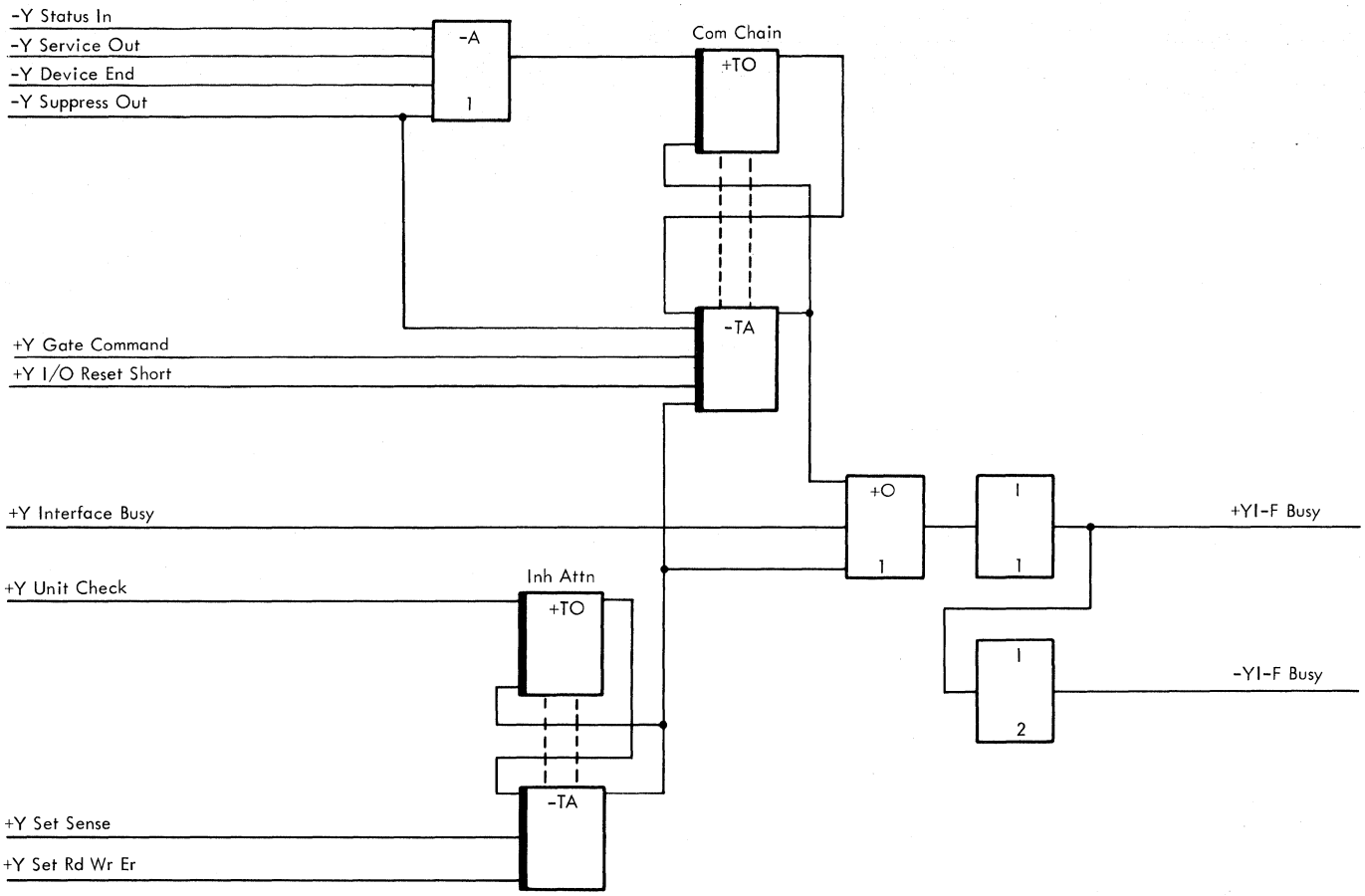


Figure 2-94. Command Chaining, Inhibit Attention

Inhibit Attention: The Inhibit Attention latch is set whenever the Unit Check latch of the status register is set. Then the Interface Busy signal is generated by OR 1 even after the Interface Busy latch is reset. This action is taken, even though ending status has been transferred to the channel, because sense information is available. The keyboards (or printer) are not allowed to interrupt the possible sense byte transfer which can now be initiated by the channel. The Inhibit Attention latch remains set until a Sense, Read, Write, or Erase operation is initiated by the channel.

Disconnect and Reset Circuits

Disconnect and reset circuitry (Figure 2-95) provides the reset signals to reset the channel adapter at the termination of an operation.

The Interface Disconnect latch provides a reset pulse when an operation is terminated by the channel (Stop latch set due to an Interface Disconnect). The Interface Disconnect latch is set from AO1 or AO2, and the output from the latch is applied to OR 1. Whenever OR 1 is conditioned, the I/O Reset signal is generated from OR 1 through I4 and through OR 2 and I5. In addition, the Reset signal resets the Interface Disconnect latch, which then terminates the signal. The result is a reset pulse. Note that the I/O Reset Long signal from I5 is conditioned only as long as the I/O Reset Short pulse is present (when caused by the I/O Reset Short). If the CE Reset Long signal is applied to OR 2 (throughout Local mode operations), the circuits to which this signal is applied are held deconditioned. Such circuits are those that are used only in Remote mode. The I/O Reset signal is also generated by A1 (Selective Reset) or A2 (System Reset) if the Operational Out signal drops.

The System Reset latch is set when a reset is generated as a result of a Reset Erase signal from the RESET ERASE pushbutton or by A2 when the Operational Out and Suppress Out lines are down.

Hold Select Circuits

The Select Out line is routed serially from the channel to the first control unit through each control unit to the last. At the last control unit, the Select Out line is jumpered to the Select In line and routed

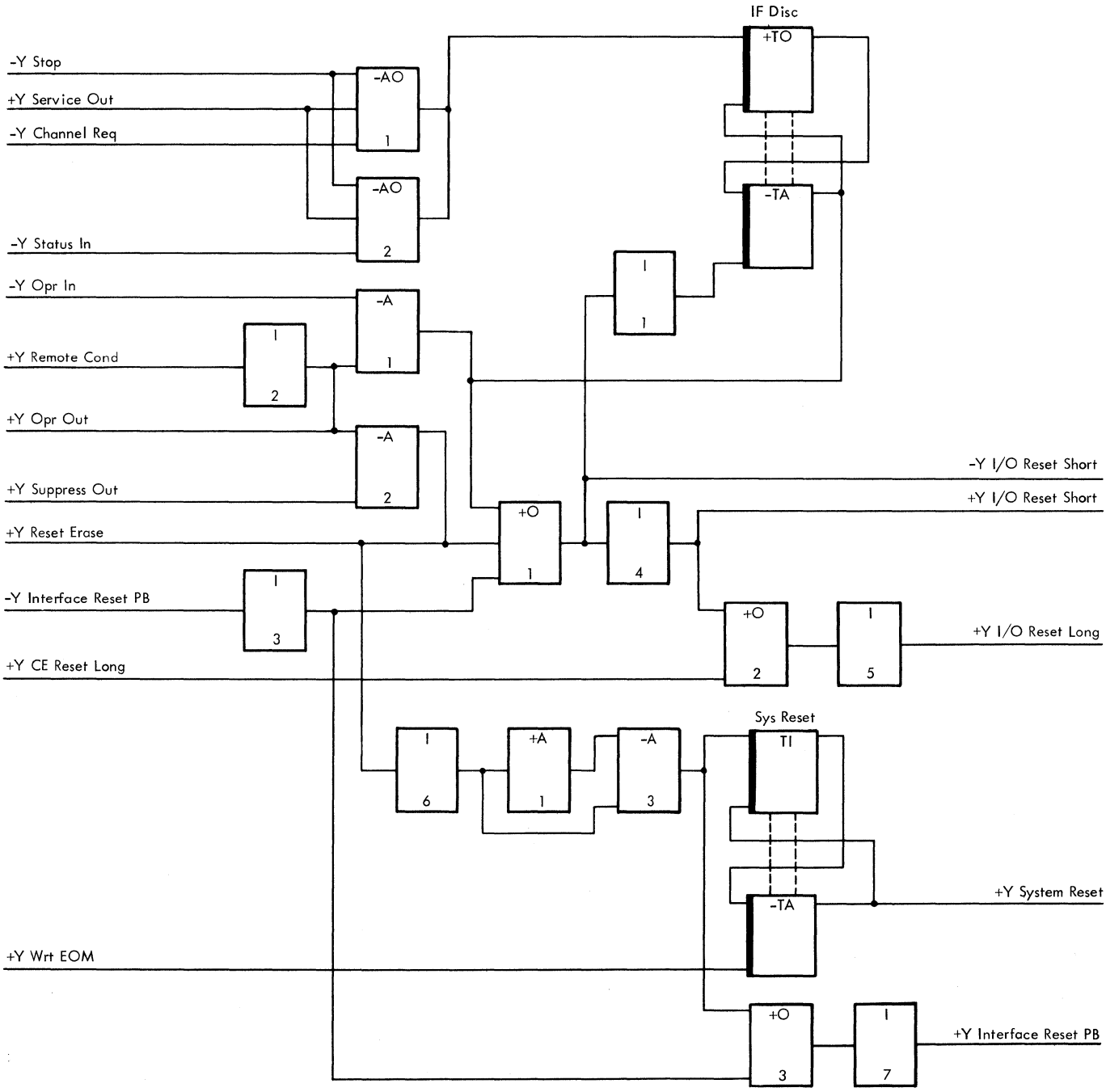


Figure 2-95. Disconnect and Reset

serially through the control units in the reverse order, as for Select Out. When the channel raises the Select Out line, the signal is applied to the first control unit. If the first control unit is not in need of capturing the channel (and is wired for high priority), the signal is propagated to the next control unit. The signal is trapped by any control unit that captures the interface. If the Select Out signal is passed by the last control unit, the signal is sent back through the control units (in reverse order) as Select In. If all control units were wired for high priority (designed to capture the channel with the Select Out line), the Select In line would ripple through them and be returned to the channel to indicate that no control units were to be serviced. However, if any control unit was wired for low priority, the unit could trap the Select In line and capture the channel if the unit was to be serviced.

The 2848 can be wired to operate on the low- or high-priority scheme and, therefore, will capture the interface by trapping either the Select Out (high-priority) or Select In (low-priority) line when service is required.

Since the Select Out and Select In lines pass through control unit interface circuitry, provision exists for passing the signals to the next control unit. Units without the Isolation Feature pass the selection signals when control unit power is off. Both select lines are routed directly through a relay to the next control unit (Figure 2-96). Unit equipped with the Isolation Feature pass the selection lines when the selector switch on the operator's panel is in LOCAL TEST. In this case one selection line is routed through a relay and one goes through a jumper wire (Figure 2-96A).

Figure 2-96 shows the select line circuitry when the Isolation Feature is not installed and power to the 2848 is on. Two relay sockets are shown, RRL1 (high priority) and RRL2 (low priority). The bypass relay can be installed in either location, depending on the priority desired.

Figure 2-96A shows the select line circuitry for a 2848 with the Isolation Feature installed when power is on and the selector switch is in REMOTE OPERATE. When the selector switch is in LOCAL TEST, the (reed) relay is dropped and the selection signals

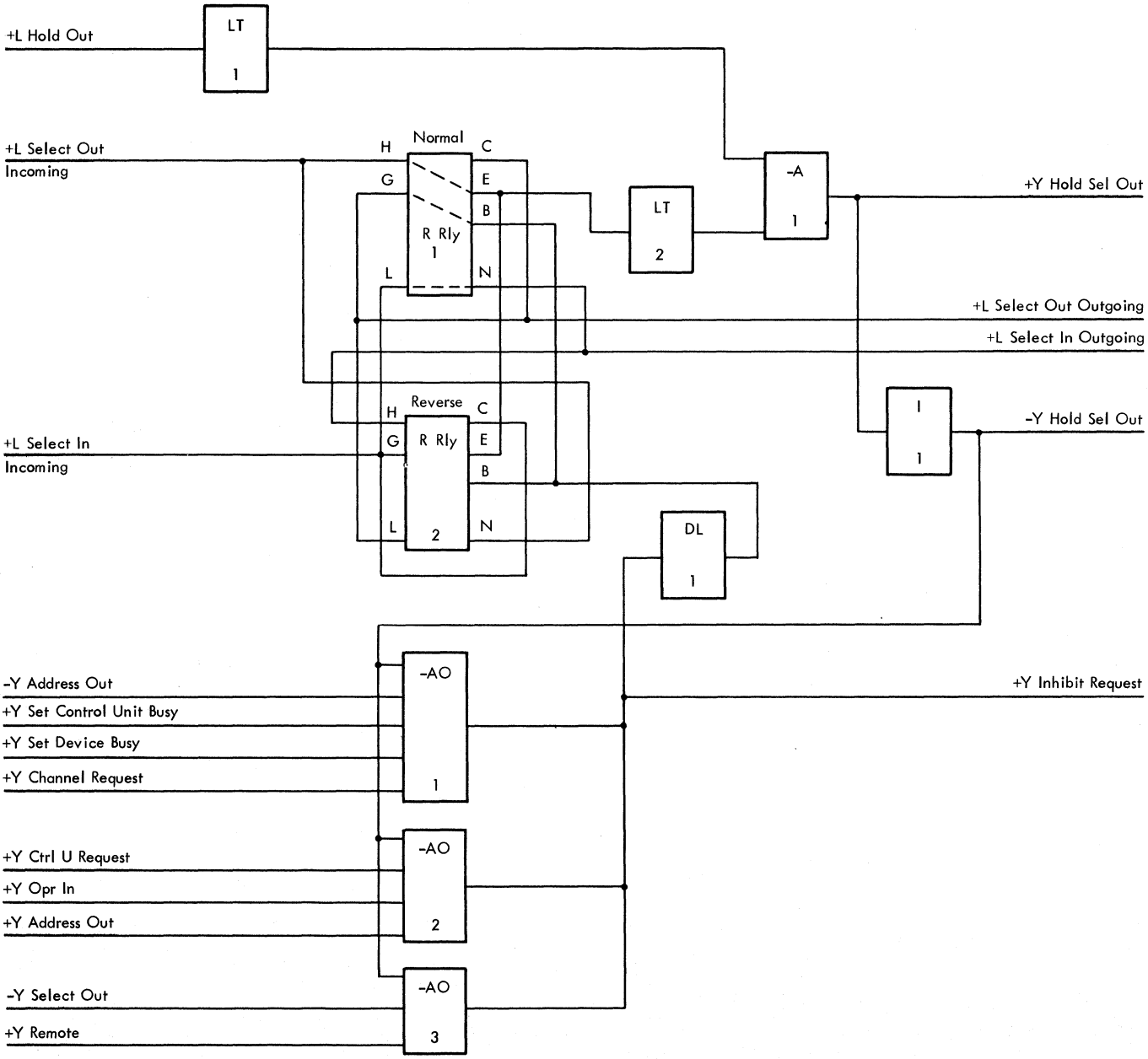


Figure 2-96. Hold-Select Circuit for Units Not Equipped with Isolation Feature

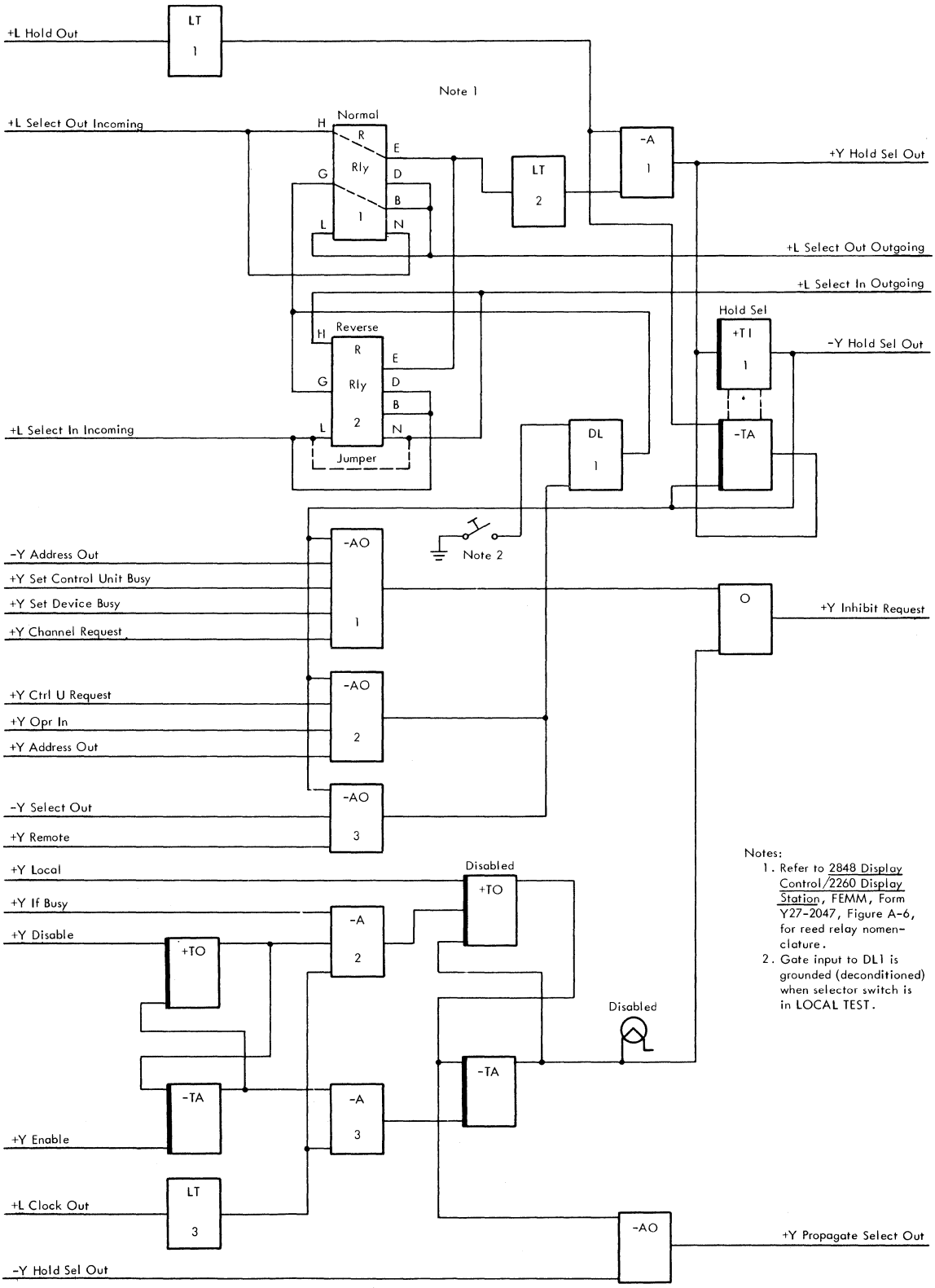


Figure 2-96A. Hold-Select Circuit for Units Equipped with Isolation Feature

are bypassed by one pair of relay contacts and a back panel jumper.

Hold Out must be active for Select Out/In to be active. Then the Hold Out signal is converted by LT1 and is applied to one input of A1. If the Select Out line reaches the control unit (not already trapped by another control unit), the Select Out signal passes through points H and E of relay RRLY1 to LT2. This occurs regardless of whether the Isolation Feature is installed as shown on Figures 2-96 and 2-96A. LT2 converts the signal and conditions the second input to A1. The Hold Select Out signal is generated by A1. In units without the Isolation Feature, the Hold Select Out signal is applied to interface control circuitry and is also inverted by I1 (Figure 2-96). In units having the Isolation Feature, the Hold Select Out signal generated by A1 sets the Hold Select latch (Figure 2-96A) and is applied to interface control circuitry. The Hold Select latch is reset by the fall of Hold Out. This latch protects against faulty operation caused by slivering of the Select line when power is applied to or removed from other units on the interface. The inverted Hold Select Out signal is applied to more control circuitry and is also applied to AO circuits 1, 2, and 3. If any of these three circuits is fully conditioned, an Inhibit Request signal is generated. This results in the propagation of the Select Out signal to the next control unit; i.e., the control unit will not capture the channel interface by trapping Select Out. These circuits will develop the Inhibit Request signal under the following conditions:

1. AO1
   a. Address out - an address is on the Bus Out lines (channel-initiated sequence).
   b. Not set control unit busy - a short control unit busy sequence is not in order.
   c. Not set device busy - command-to-busy device sequence is not in order.
   d. Not channel request - a channel-initiated sequence is not in order.
2. AO2
   a. Not control unit request - the control unit does not require service.

b. Not operational in - the control unit is not selected.
c. Not address out - no address is on the Bus Out lines and it is not a channel-initiated sequence.

3. AO3
   a. Not remote - the control unit is in local (test) status.
   b. Select Out.

In addition to the interface conditions (just described) which raise Inhibit Request, the signal is also generated in units equipped with the Isolation Feature when the CE activates the DSBL REQUEST/ INTF DSBLD switch while placing the unit in off-line status. (Refer to Chapter 4 of 2848 Display Control/ 2260 Display Station FEMM, Form Y27-2047, for procedure used to place the unit in off-line status.) As shown in Figure 2-96A, activating the DSBL REQUEST/INTF DSBLD switch sets a switch latch which partially conditions A2. Assuming that IF Busy and Clock Out are down, the Disabled latch is then set and Inhibit Request is raised. IF Busy is not active when the 2848 is not operating with the channel. Clock Out is inactive when there is no activity on the channel interface.

If the Inhibit Request signal is not generated, the Select Out line will not be developed by DL1, nor will it be sent on to the next control unit. As a result, the control unit can be selected, and the operational sequence will continue.

If the Inhibit Request signal is generated, the Select Out signal is produced by DL1. The output from DL1 passes through points B and G of RRLY1 and is sent out to the next control unit.

Note that the Select In signal (if present) passed through this control unit without possible interruption through points L and N of RRLY1. Select In is routed through RRLY2 in a manner similar to that described for Select Out and RRLY1. In units equipped with the Isolation Feature the Select In signal is passed through the control unit without interruption through points L and N by a jumper in the RRLY2 socket.

Control Unit and Device Addressing

The addressing circuits of the 2848 control unit must be capable of detecting the presence of the control unit address on Bus Out from the channel and of decoding the device address used to select one of the maximum of 25 devices (24 display stations and one printer) that can be associated with the 2848.

The addressing circuits are illustrated in Figure 2-97. The hub of the addressing scheme is the 5-bit address register. Note that this register can be loaded from any one of four sources, as follows:

1. The channel via Bus Out.
2. The address register associated with the keyboards in the 2848 common logic.
3. A prewired printer address.
4. The CE panel via the character switches.

In Figure 2-97, it can be seen that, with the exception of the channel-originated address, the address register is loaded by means of a straight 5-bit transfer. The channel-originated address is more complex because it involves the simultaneous addressing of the control unit and one of its 25 (maximum) associated devices by a single 8-bit input from the channel. In the paragraphs that follow, channel addressing is discussed in detail, and the loading of the address register from each of the other three sources is described. The discussion is limited to a description of the addressing scheme and the operation of the addressing circuits.

Channel-Originated Address

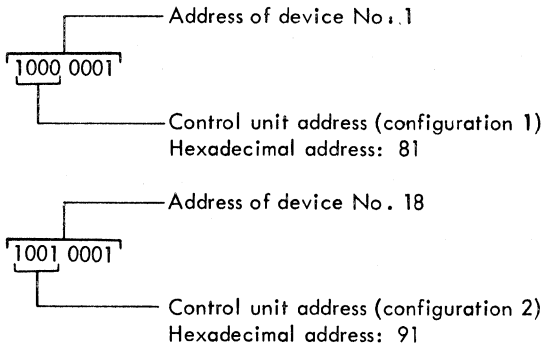
The 2848 receives an 8-bit channel output (bits 0-7) via Bus Out as the input to the addressing circuits. This address byte contains the address of both the control unit and the desired device. The control unit address is contained in Bus Out bits 0-3. The device address is represented by Bus Out bits 4-7. However, the maximum number of devices that can be addressed, using four bits, is 16, which is inadequate since a maximum of 25 is possible. Therefore, the number of device addresses was expanded by using Bus Out bits 0-3 to develop a fifth device address bit (bit 16). Bus Out bits 0-3 thus serve a dual purpose: they represent the control unit address, and they are also decoded to select one of two groups of devices, i.e., group 0-15 or group 16-24.

Under the expanded device address scheme, the control unit will recognize two configurations of Bus Out bits 0-3 as the unit address. One of these bit configurations will set Address Register bit 16 when decoded; the other will cause bit 16 to be a zero. The overall device addressing scheme is as follows:

Bus Out		Address Register					Device
Bits 0-3	Bits 4-7	16	08	04	02	01	Addressed
Configuration 1	0000	0	0	0	0	0	1
	0001	0	0	0	0	1	2
	↓	0		↓			↓
	1111	0	1	1	1	1	16
Configuration 2	0000	1	0	0	0	0	17
	0001	1	0	0	0	1	18
	↓	1		↓			↓
	1000	1	1	0	0	0	25

Assume that in the table above configuration 1 is 1000 and configuration 2 is 1001. Two typical 8-bit

channel-originated addresses can be described as follows:



The hexadecimal equivalents of the two typical addresses are given in the above examples. Note that two different unit addresses (1000 and 1001) are required because of the expanded addressing scheme; this must be considered when programming control unit addresses to multiple 2848's attached to the host system. The two addresses (configurations of bits 0-3) assigned to a 2848 need not be consecutive when more than 16 display devices are attached to a control unit. The two unit addresses (configuration of bits 0-3), required when more than 16 display devices are attached to a control unit, need not be consecutive.

In Figure 2-97, note that Bus Out bits 0-3 are sampled by the unit address decoder. If a bit configuration representing the unit address is decoded, the Our Address On Bus Out signal is generated. Then, if the Interface Busy latch is not set, the Adr From Channel signal is generated from AND 1 to set the address in the address register. Note that Bus Out bits 0-3 are also decoded to determine which group of devices is being addressed so that AR 16 can be set properly. The decoder outputs are No. 1 comp (configuration 1, device group 0-15, AR 16 equal to 0) and No. 2 Comp (configuration 2, device group 16-24, AR 16 equal to 1). Bus Out bits 4-7 are set directly to AR 08-AR 01, respectively.

If the Interface Busy latch is set when the unit address is decoded, the address on Bus Out is not gated into the address register. Instead, it is compared with the address previously set in the address register, which would be the address of the device in use and responsible for the Interface Busy condition. If the address compare, the Device Busy latch is set. This address compare enables the channel to obtain status information for a busy device. The sequence for this operation is illustrated in the interface flow charts provided in the FE Diagram Manual. If the addresses do not compare, Control Unit Busy is presented to the Channel.

The address register outputs are either transferred to the channel via Bus In or to the address decoder in 2848 common where the actual device selection is made. The destination of the register's output depends upon the operation being performed and the exact point within the operational sequence.

Control Unit-Originated Address

When an Enter command is issued from a display station keyboard, the station (device) address must be sent to the channel to identify the origin of the input data. In Figure 2-97, note that the 5-bit device address is set directly into the interface address register in conjunction with the Enter command. The address is converted into a full 8-bit address byte that can be recognized and used by the channel as it is transferred to the channel via Bus In. Thus, the channel is provided with the 2848 address (Bus In bits 0-3) and the device address so that it can re-address data to the originating source.

Printer Address

In Figure 2-97, note the Adr of Ptr AND circuits. These circuits are prewired to insert the printer device address in the interface address register in conjunction with printer device end. This identifies the printer during the ending sequence of channel-originated printer operations. The device address assigned to the printer is always the highest-order device address.

Manual Address

The interface address register can be set with a manual address originating from the character switches of the CE panel. In Figure 2-97, note the switch-to-AR bit relationship and the fact that a simple 5-bit transfer is used to load the register.

Command Decode

- Command decode circuitry establishes the time for examination of the command byte from the channel Bus Out lines.
- Command decode circuitry checks bits 0-4 for all-zeroes. If a 1-bit is present, the byte is decoded as illegal, and a Set Com Rej (set command reject) signal is developed which terminates the operation, sets the Command Reject bit in the sense byte, and sets the Unit Check bit in the status byte.
- Command decode circuitry decodes legal commands by examining all eight bits of the command byte and generating the signal which sets the correct bit in the command register.

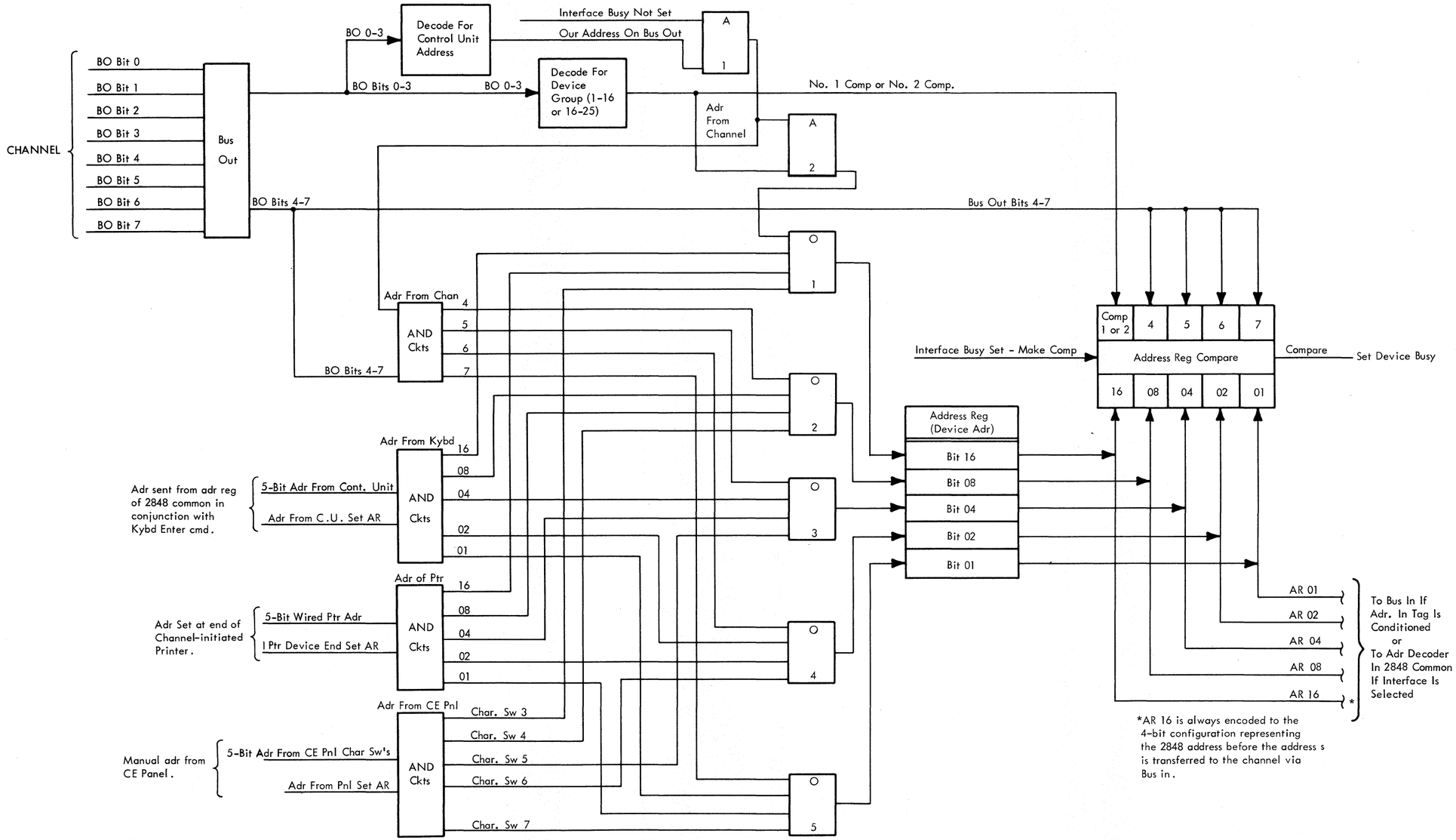


Figure 2-97. Control Unit and Device Addressing

During the command portion of a channel-initiated selection sequence, the channel sends a command byte to the control unit over the Bus Out lines. The channel signals the control unit that a command byte is on Bus Out by raising the Command Out tag. Interface circuitry delays the Command Out signals for 1.2 μs to permit parity checking before examining the command byte. The delay allows time for Bus Out and command decode circuitry to stabilize. (See Figure 2-98 for command byte formats.)

Figure 2-99 shows the command decode circuitry. Bus Out lines 0-4 are applied to OR 1. If any of these signals are present, a 1-bit is indicated, and the command is illegal. (Bits 0-4 are always zero in a legal command.)

The A2 circuit develops the Gate Command signal because the Address In, Channel Request, and Command Out Delayed signals are present. These signals indicate that a channel-initiated selection sequence has progressed to the point where a command byte on the Bus Out lines is to be read by the control unit.

The Gate Command signal is applied to A1 (through I2) to allow generation of the Set Command Reject signal if Bus Out parity is good (odd) and one or more of Bus Out lines 0-4 are up (illegal command).

Circuits A3 and IP1 generate the Decode Command signal if Bus Out parity is odd, Bus Out bits 0-4 are zeroes, and the Gate Command signal is present. The Decode Command signal is applied to decode circuits AO2, A5, A6, A7, A8, A10, and A11. These circuits are also conditioned by the appropriate (positive or negative) outputs of Bus Out lines 5, 6, and 7 to cause decoding of the command byte. Conditioning any one of these circuits results in the generation of a Set signal to the appropriate command register circuitry.

The Test I/O latch is set by decode circuits A4, I3, and AO2; it may also be set by AO1 during a test-I/O-to-busy-device sequence. During the sequence, the Device Busy latch is set. If the Bus Out lines are all zero when the Command Out Delayed signal comes up, AO1 is fully conditioned, and the Set Test I/O signal is generated.

Note that the output from A9 is applied to OR 1. If the Write Line Address command is decoded, the command will be rejected unless the Inhibit Reject Line Address signal is provided by line address control circuitry. The Reject Address signal is generated if the write line address feature is incorporated.

Sense and Status Registers

The significance and function of the bits of the sense and status registers are discussed in Chapter 1.

Write	P	0	1	2	3	4	5	6	7
Write DS Buffer Storage	0	0	0	0	0	0	0	0	1
Write 1053 Buffer Storage	0	0	0	0	0	0	0	0	1
Write DS Line Address	1	0	0	0	0	0	1	0	1
Read									
Read DS Initial Program Load	1	0	0	0	0	0	1	1	0
Read DS MI Message	0	0	0	0	0	0	0	1	0
Read Full DS Buffer	1	0	0	0	0	0	1	1	0
Control									
No Operation (No-Op)	1	0	0	0	0	0	0	1	1
Erase DS Buffer Storage	0	0	0	0	0	0	1	1	1
Sense									
Present Sense Byte	0	0	0	0	0	0	1	0	0
Test I/O									
Test I/O	1	0	0	0	0	0	0	0	0

Figure 2-98. Command Byte Format

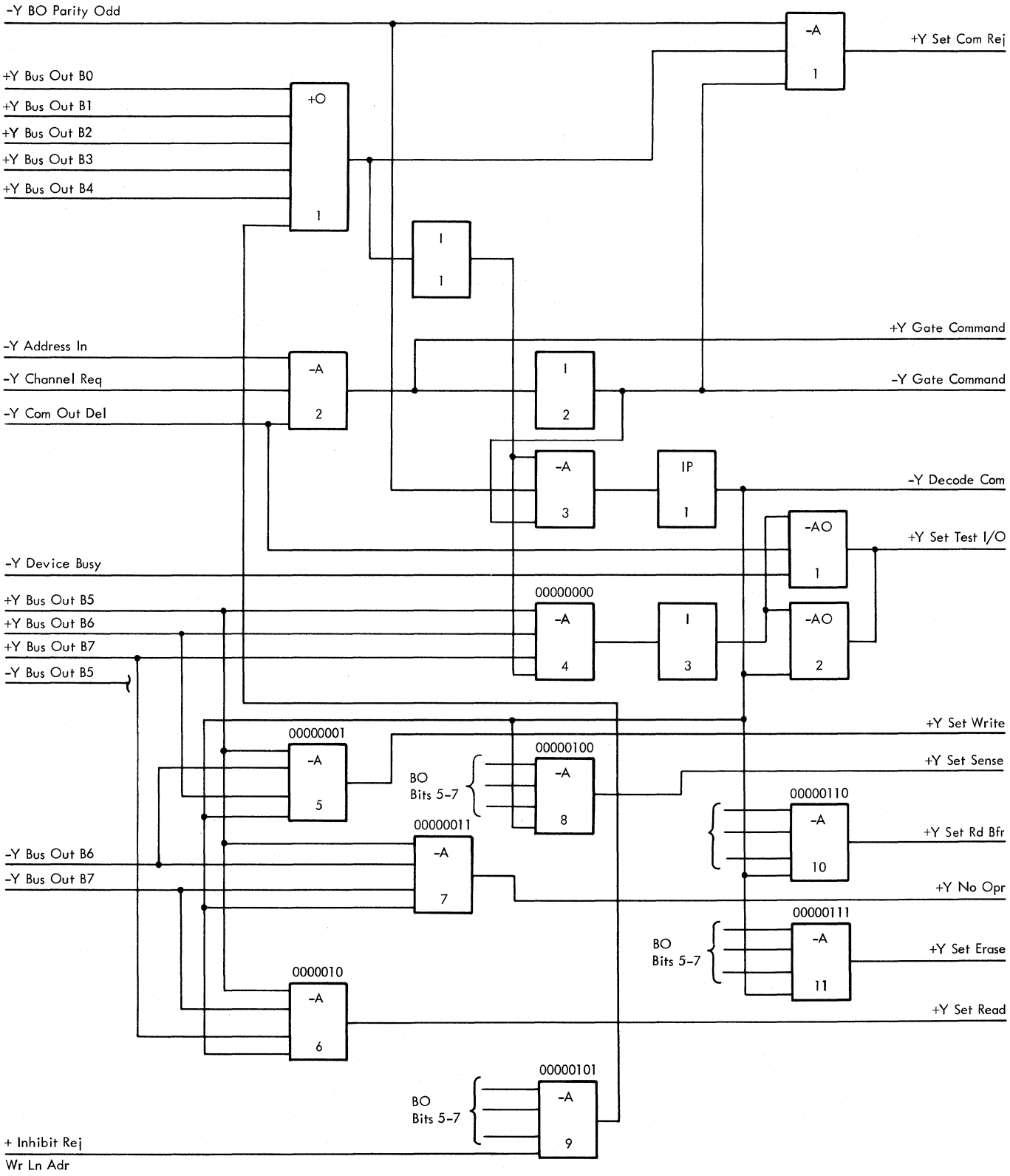


Figure 2-99. Command Decode

I/O Request and Character Register Control

I/O request and character register control circuitry controls the transfer of information between the character register and the common buffer register.

I/O Request

The I/O Request latch (Figure 2-100) output is used to notify the common equipment that the interface requires service. The AO circuits, 1, 2, and 3, can set the I/O Request latch during the Erase, Write, or Read operations, respectively.

The I/O Request latch cannot be set while the Row Compare signal is present. When in a write or write line address operation, and when a character is in the character register, the latch is set. When in a read or read buffer operation, the I/O Request latch is set if no character is in the character register and the Device End latch is not set or the Stop latch is set. When an Erase command is received, the I/O Request latch is set.

The I/O Request latch is reset by an I/O Reset, End Operation or Machine Reset, Character Sent (read), or Character Received (write).

Character Register Control

Character register control circuitry (Figure 2-101) provides the means of conditioning the read or write input circuits to the character register, forcing the new line conversion codes into the character register, and resetting the character register.

The New Line From Channel or Character From Channel signals are developed by A1, A2, I1, A3, and I2 when a data byte is received on the Bus Out lines. The New Line From Channel sets the converted code for new line into the character register. The Character From Channel signal conditions the gates that allow the character register to be loaded from the Bus Out lines.

The New Line To Channel, Character To Channel, and Set Character Register Bit 1 signals are generated by A5, A6, I4, A7, and I5.

During a read operation, if the BCD code for a new line character is detected, the New Line To Channel signal is generated. This signal sets the character register to the EBCDIC code for new line. If the BCD character read is other than new line, bit 1 of the character register is set, and the Character To Channel signal gates the BCD from the common buffer into bits 2-7 of the character register.

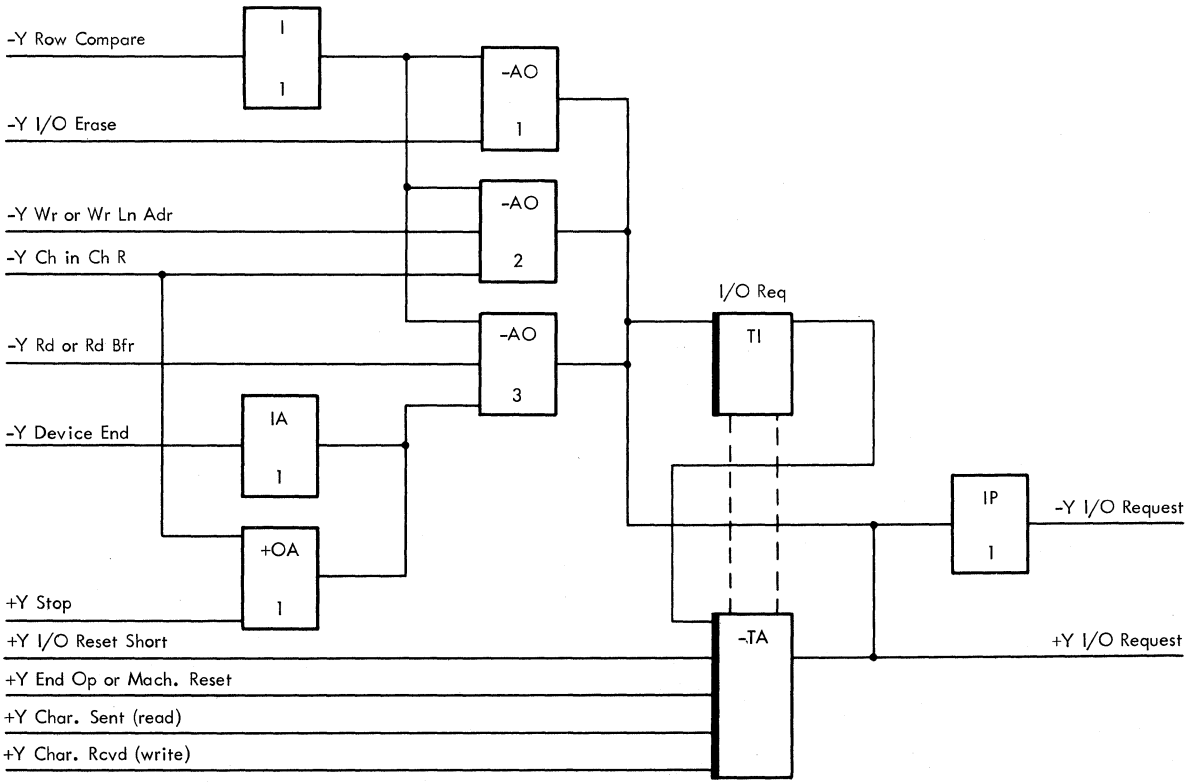


Figure 2-100. I/O Request

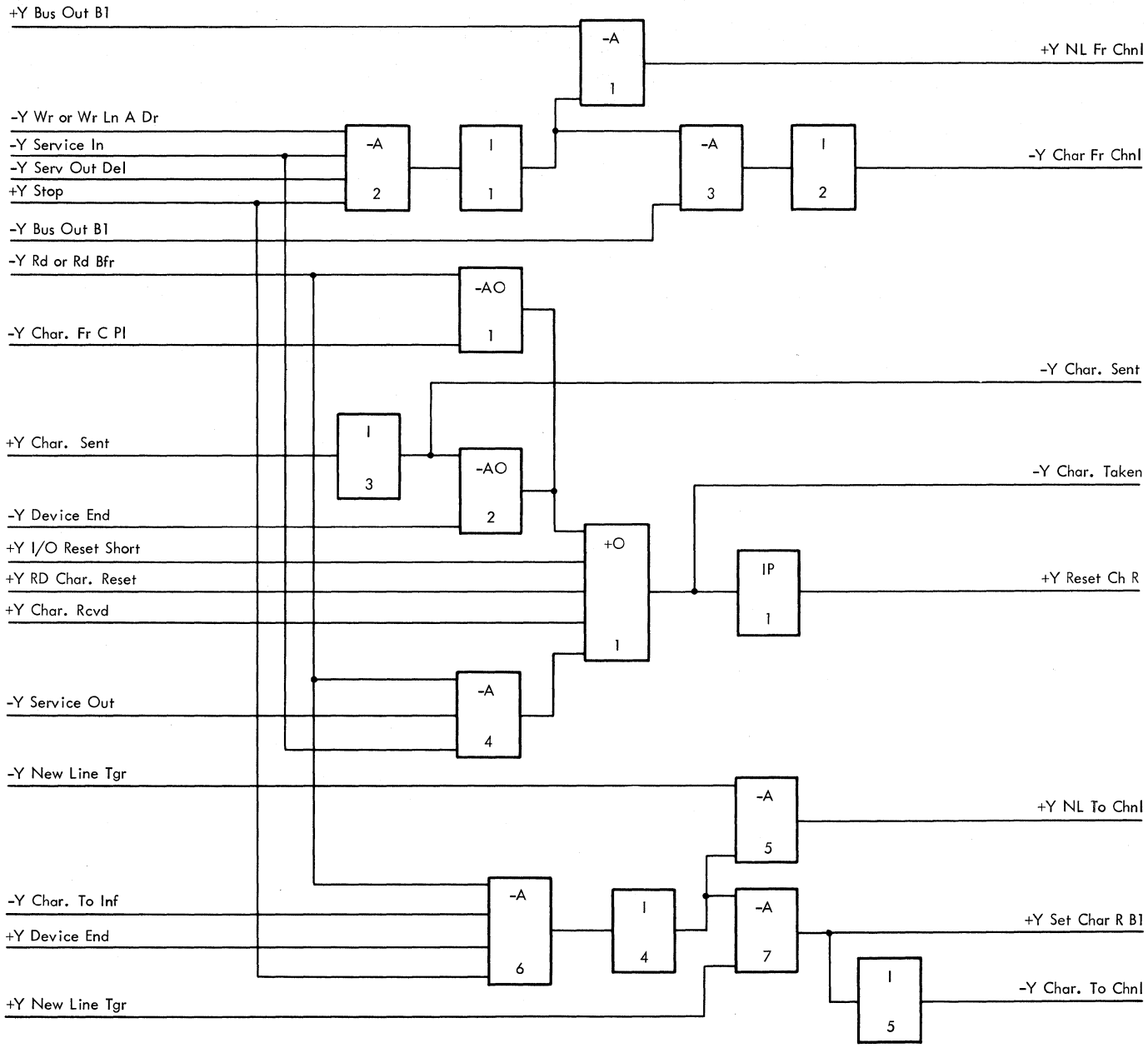


Figure 2-101. Character Register Control

The Reset Character Register signal is generated by OR 1 and IP1. This signal is generated to clear the character register so it can accept the next data byte.

Character Register and Code Converter

- Converts 8-bit data bytes (in EBCDIC code) from the channel to 6-bit BCD used by 2848 common circuitry.
- Converts 6-bit BCD data from 2848 control circuitry to 8-bit EBCDIC data used by the channel.

Character Formats

The character register and code converter is an 8-bit register between the common buffer and the Bus Out and Bus In lines. The character code used by System/360 is the 8-bit EBCDIC code, whereas the character code used by the 2848 is a 6-bit BCD code. In the case of all alphanumeric characters and most special characters, the conversion requires dropping bits 0 and 1 in a write operation and adding the appropriate configuration of the same bits in a read operation.

The exceptions to the normal code conversion are discussed below.

Start Symbol: The start symbol is displayed as a result of the receipt of the EBCDIC code for the ¢ (cent) character. No actual conversion of the bit 2-7 configuration takes place. However, as the ¢ character is processed by the character generator of the 2848, the resulting display will be the triangular Start symbol. (The start symbol can also be generated by the keyboard. However, the coded byte is fed directly to the common buffer, bypassing the character register.)

New Line Symbol: When the new line symbol is to be displayed (write operation), the EBCDIC code must be converted from the Bus Out configuration of 00010101 to the character register configuration of 01011010. This is accomplished by sensing bit 1 of Bus Out. Since the new line character of the EBCDIC code is the only character code that will not have a 1 in bit 1, the code converter recognizes the character as new line and sets the character register to 01011010. The new code results in a display of the new line character.

During a read operation, the 6-bit BCD code is transferred from the common buffer register to the code converter and character register where the appropriate EBCDIC code is generated.

Check Character: If the data byte on Bus Out is found to have even parity (bad parity) during a write operation, the character register is set to 0111111. This character code causes a solid block to be displayed. Such a display is called a check character, and it indicates that the character sent to the 2848 was in error. The check character is transmitted to the channel as a quote character (") during a read operation.

Circuit Description

Bits 0-3 and 4-7 of the character register and code converter are shown in Figures 2-102 and 2-103, respectively.

Character register bit-0 and bit-1 outputs are used only in a read operation since that is when a 6-bit BCD character is converted to the 8-bit EBCDIC code. During a write operation, bit 0 is dropped completely, and bit 1 is transferred to the character register and code converter to be used for code checking and conversion only. The output of the bit-1 latch is not applied to common circuitry.

Bit 0 is set by circuit A1 (Figure 2-102) during a read operation under the following conditions:

1. Not stop.
2. Character sent or character from control panel. (A character was sent from the common buffer, or a character is being written from the control panel.)
3. The character is alphanumeric and not a special character. (Circuits AO1, AO2, OR 2, and AO3 are used to decondition A1 if the character is a special character and not alphanumeric.)
4. Character register bit 1 must be set. (Bit 1 is set for all legal EBCDIC characters used by the 2848 except the new line character.)

Bit 1 may be set in any of the following ways:

1. Character from control panel or character from channel. (Bit 1 is always set for a legal character except the new line character.)
2. New line from channel. (The character on the Bus Out lines is a new line character. This signal sets bits 1, 3, 4, and 6 of the character register.)
3. Set character register bit 1. (The 6-bit BCD character read is not a new line character.)
4. Set BOC data. (When a parity error is detected on the Bus Out lines during a write operation, bits 1 through 7 are set in the character register.)

Note that when either bit 1 or bit 3 is set, OR 3 and I3 develop Character In Character Register signals.

Bit 2 is set by the Set BOC Data signal or by any of the circuits, A2, A3, or A4. These circuits are activated from the control panel in test operations, the Bus Out lines in write operations, and the common buffer register in read operations.

Bit 3 (Figure 2-102) and bits 4-7 (Figure 2-103) are set in the same manner as bit 2. However, remember that:

1. Set BOC Data causes bits 1-7 to be set when a parity error is detected on the Bus Out lines.
2. New line from channel presets bits 1, 3, 4, and 6.
3. New line to channel presets bits 3, 5, and 7.

The character register is reset by a Character Register Reset signal generated by character register control circuitry.

Channel Adapter Operational Sequences

The operational sequences of the channel adapter are described in three categories: channel-initiated, control-unit-initiated, and special. Refer to the channel interface flow charts provided in the FE Diagram Manual for all sequences.

Channel-Initiated Sequences

The basic operation of a channel-initiated selection is described in terms of a read or write selection.

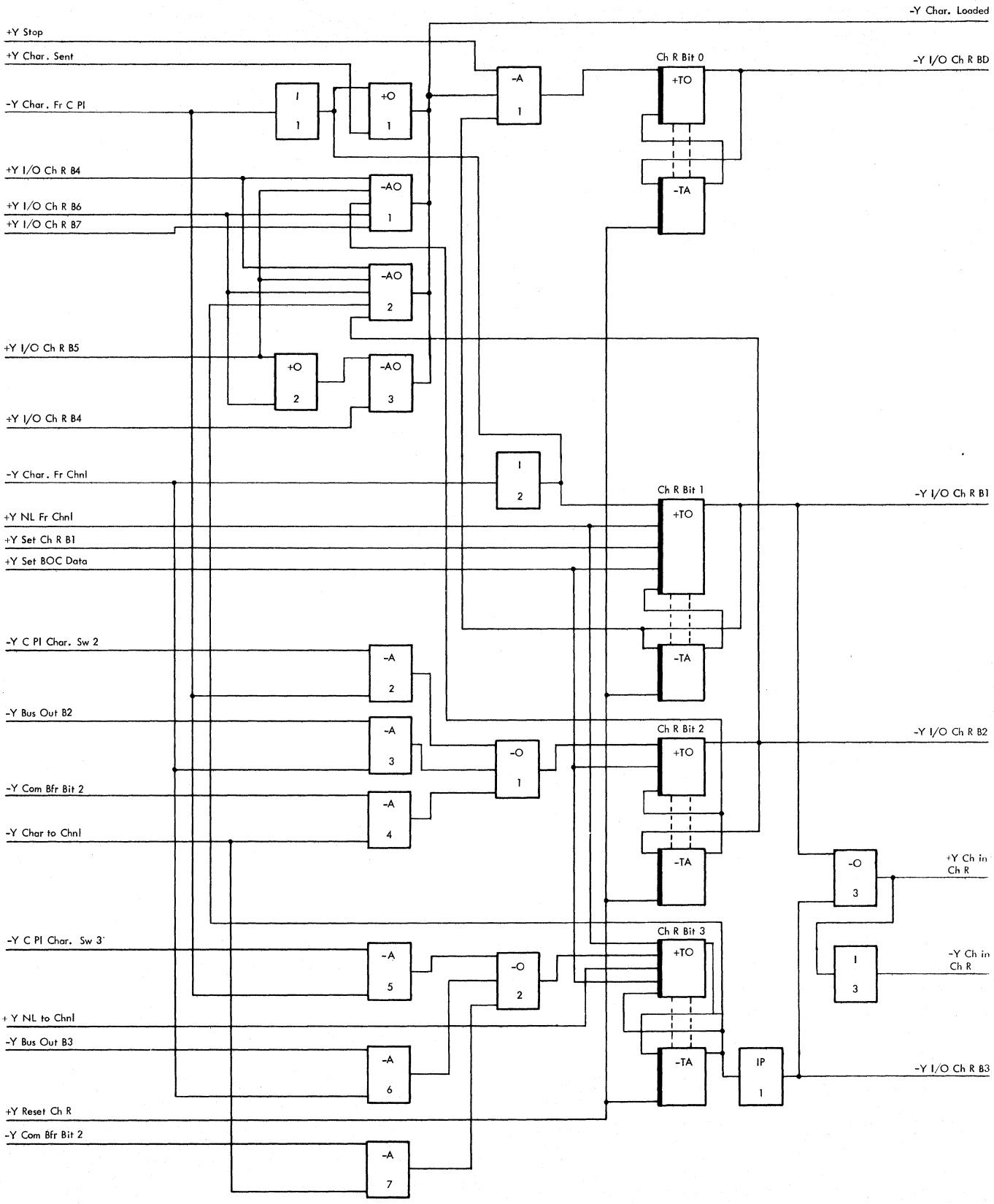


Figure 2-102. Character Register Bits 0-3

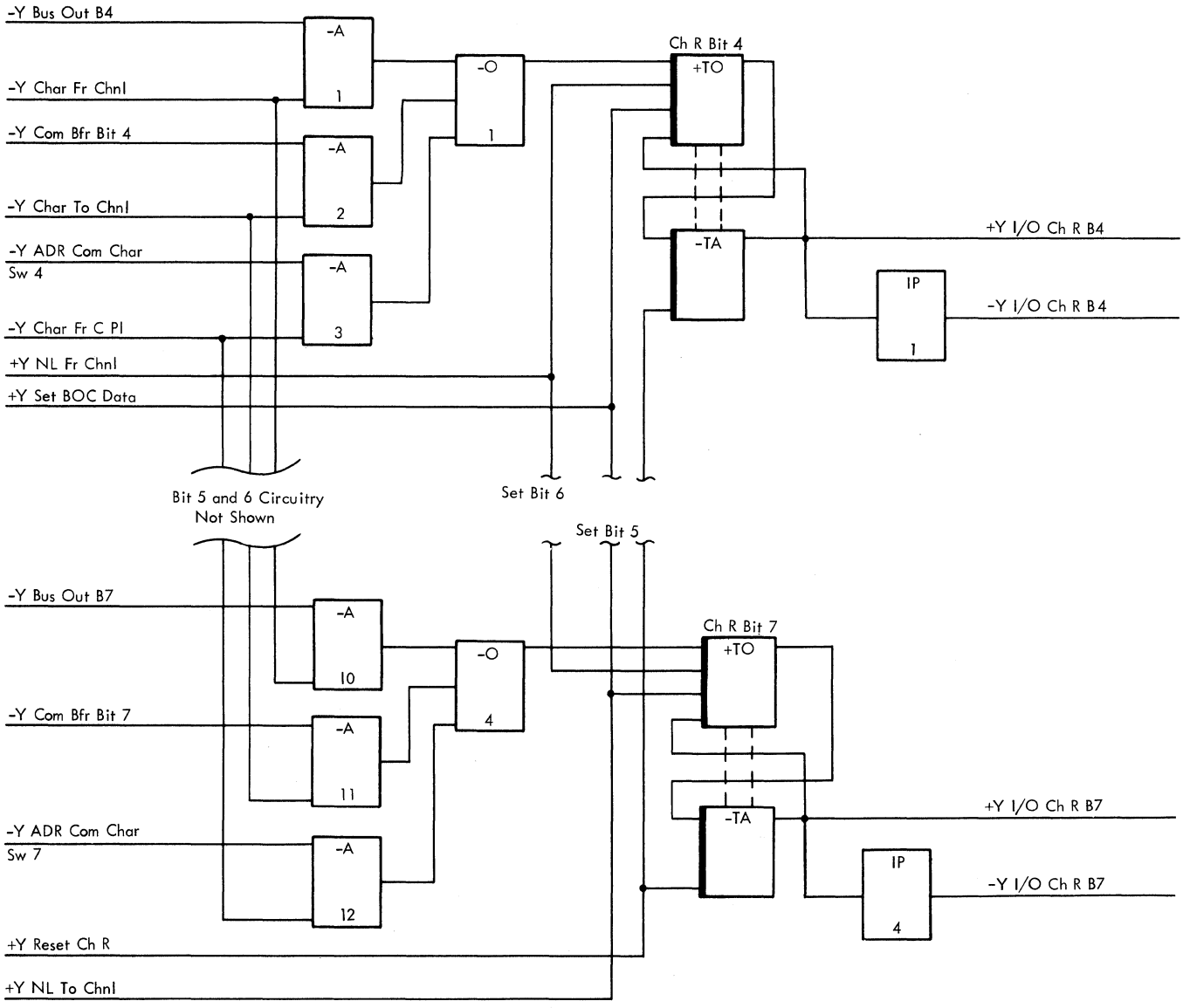


Figure 2-103. Character Register Bits 4-7

Each of the remaining channel-initiated sequences is then described in terms of the way it differs from the read or write sequence. Figure 2-104 shows the sequence of events during a channel-initiated selection for a read or write operation. The channel-initiated selection sequence is performed as follows:

1. The Operational Out line is up and remains up as long as the channel is operational.
2. Interface controls are all in a Reset state.
3. The channel addresses a device by placing the device address on the Bus Out lines and raising the Address Out tag.
4. If the address on the Bus Out lines is a legal address for our control unit and devices, the Channel Request latch is set.
5. The Interface Busy latch is set and the address byte is gated to the interface address register since the Channel Request latch is set.
6. When the Hold Select Out line is raised by the channel (since the Channel Request latch is set and the address is good), the Operational In latch is set.
7. The Operational In signal notifies the channel that the address was accepted and the interface is captured.
8. When the Address Out signal is dropped (acknowledging our operational in), the Address In latch is set.
9. The Address In signal gates the address register contents to the Bus In lines.

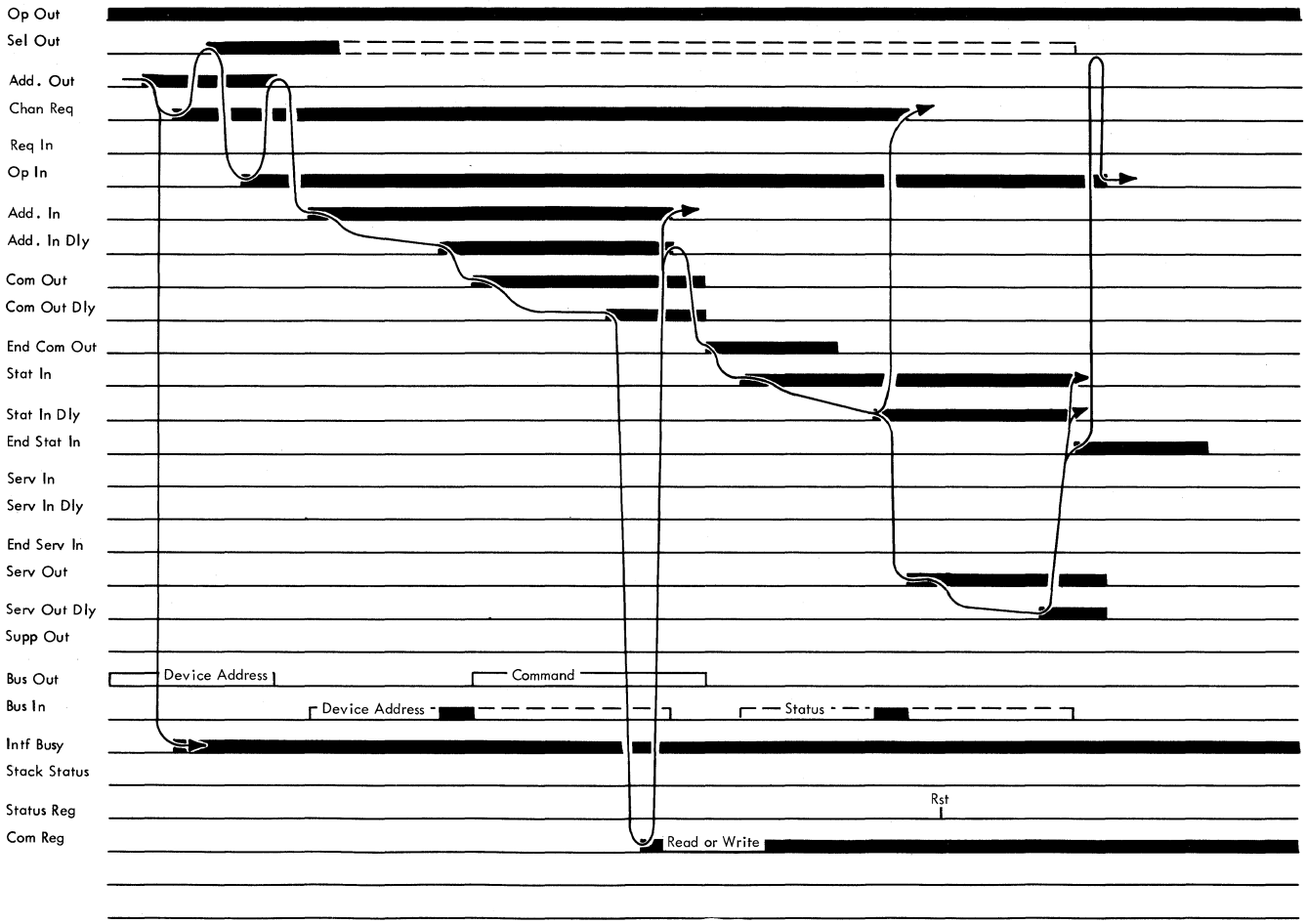


Figure 2-104. Channel-Initiated Selection (Read or Write)

10. The Address In signal is delayed 1.2 μs (to allow parity checking) and is sent to the channel as the Address In tag. This tag notifies the channel that the address is on the Bus Out lines for verification.
11. When the channel reads the address on the Bus In lines, the Command Out tag is raised by the channel to verify receipt of the address and to signal the control unit that a command byte is on the Bus Out lines.
12. After a parity-checking delay of 1.2 μs, the Command Out (delayed) signal causes the command byte to be decoded. If the resulting command is valid, the appropriate latch in the command register is set. The Command Out Delayed signal also sets the End Command Out latch and resets the Address In latch. Note, however, that the End Command Out signal is not gated out until the Command Out tag drops.
13. Dropping the Address In tag notifies the channel that the control unit has accepted the command.
14. The channel responds by dropping the Command Out tag.
15. When the Command Out tag drops, the End Command Out signal is raised. (The End Command Out latch is reset automatically after 1.2 μs.) This signal sets the Status In latch, which causes information in the status register to be placed on the Bus In lines.
16. After a 1.2-μs delay (for parity checking), the Status In Delayed signal is sent to the channel as a Status In tag. This tag notifies the channel that a status byte is on the Bus In lines. The Status In Delayed signal also resets the Channel Request latch and sets the End Status In latch. (The End Status In signal is not gated out until later, however.)
17. When the channel has accepted the status byte, the Service Out tag is raised.
18. The Service Out tag is delayed 1.2 μs; it resets the Status In latch, which results in gating out the End Status In signal.
19. Since the channel will have dropped the Select line earlier, the End Service Out and Not Select Out signals cause the Operational In latch to be reset. This notifies the channel that the sequence is completed.

20. The channel responds to the dropping of the Operational In line by dropping the Service Out line.
21. The End Status In latch is reset automatically 1.2 μs after the Status In latch was reset.

The channel-initiated selection (read or write) is now complete. The channel and control unit are disconnected from each other (temporarily), and the control unit is left in the following condition:

1. The Interface Busy latch is set.
2. The address register contains the address of the device selected for a read or write operation.
3. The command register is set to the command specified by the channel (Read, Read Buffer, Write, or Write Line Address).

When the 2848 common circuitry is ready to perform a data transfer, the interface circuitry will be advised, and the control-unit-initiated data transfer sequence will begin.

Sense: The channel-initiated selection for a sense command is used to transfer the contents of the sense register to the channel. Figure 2-105 shows the sequence of events.

The channel-initiated selection for a sense command is identical with the selection for a read-write command until the Operational In latch is reset at the end of the basic sequence. When the Sense Command latch is set in the command register, the operation continues as follows:

1. Because the Sense latch in the command register is set, when the Operational In signal drops, the Service Request latch is set.
2. The Service Request latch sets the Control Unit Request latch, which causes generation of the Request In signal to the channel.

At this point, the channel-initiated selection sequence is completed, and the control-unit-initiated sense transfer can be performed. The channel-initiated sense selection leaves the control unit in the following state:

1. The Interface Busy latch is set.
2. The address register contains the address of the device selected for a sense byte transfer.

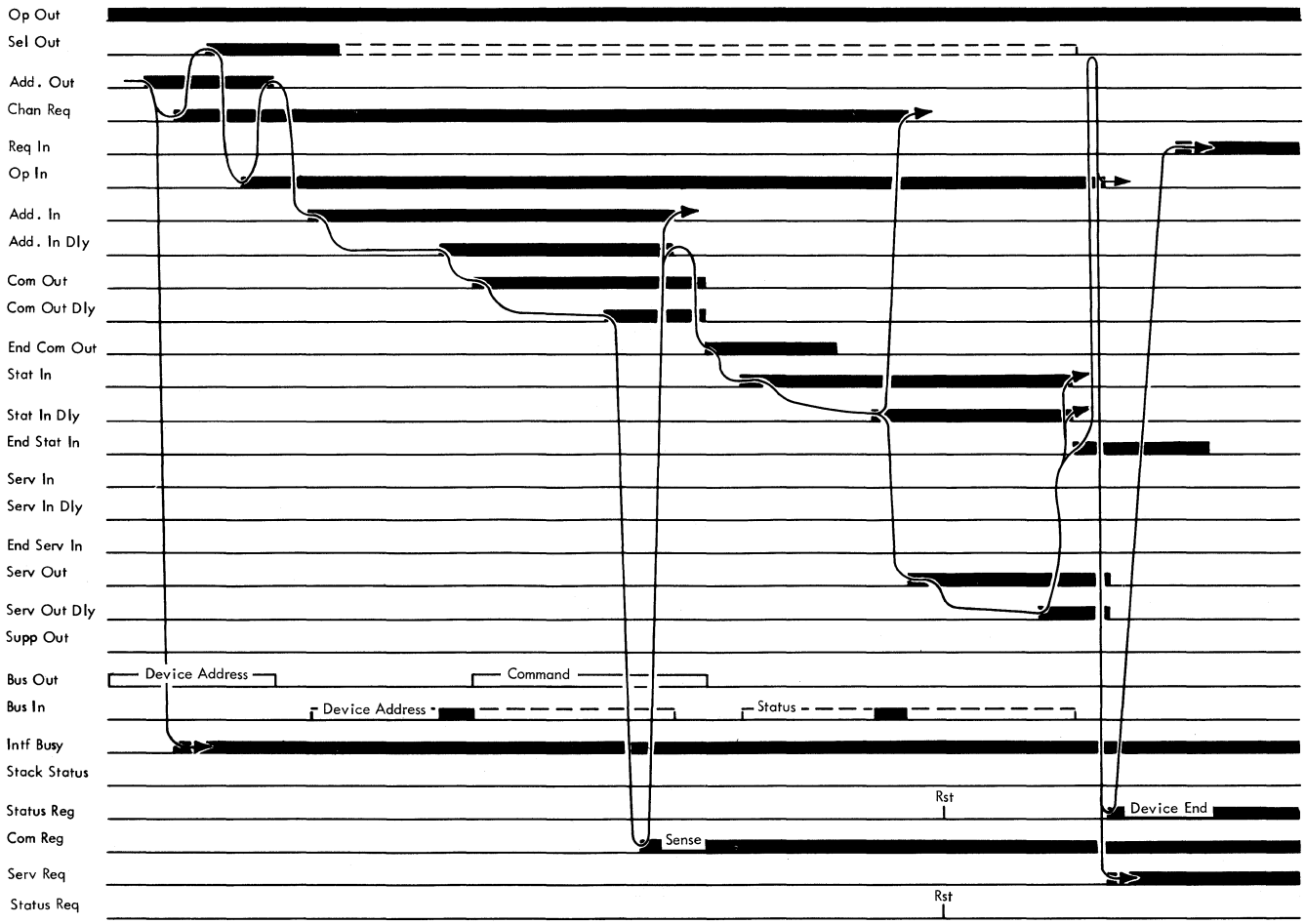


Figure 2-105. Sense Operation

3. The Sense latch is set in the command register.
4. The Device End latch is set in the status register.
5. The Service Request latch is set.
6. The Channel Request latch is set, and its output generates the Request In signal to the channel.

The above conditions are necessary to cause the control-unit-initiated sense transfer sequence described later in this section.

Erase: The channel-initiated erase sequence is used to allow the channel to select a device and erase the buffer storage for that device. The sequence of events for the selection (Figure 2-106) is identical with the channel-initiated selection for a read or write operation. At the completion of this selection, the only way in which it differs from the read or write selection is that the Erase latch is set in the command register.

When this selection is made, the channel is disconnected from the control unit, but the control unit is left in a Busy state for the erase operation to be performed. At the completion of the erase operation, the control unit notifies the channel by initiating a status sequence.

No Operation: The channel-initiated NO OP sequence (Figure 2-107) functions in a manner similar to the basic channel-initiated selection sequence. The major difference is that, as a result of the command byte being decoded, no command is set in the command register, and the Device End latch is set in the status register. As a result, the status byte transfer indicates ending status. The Interface Busy latch is reset by Service Out, and, when the Operational In latch is reset at the end of the sequence, the control unit is completely disconnected from the channel. All controls are reset in the control unit.

Test I/O: The test I/O channel-initiated sequence is used by the channel to obtain the status of any device (Figure 2-108). The sequence of events for a Test I/O command is identical with the channel-initiated selection up to the end of the status byte transfer

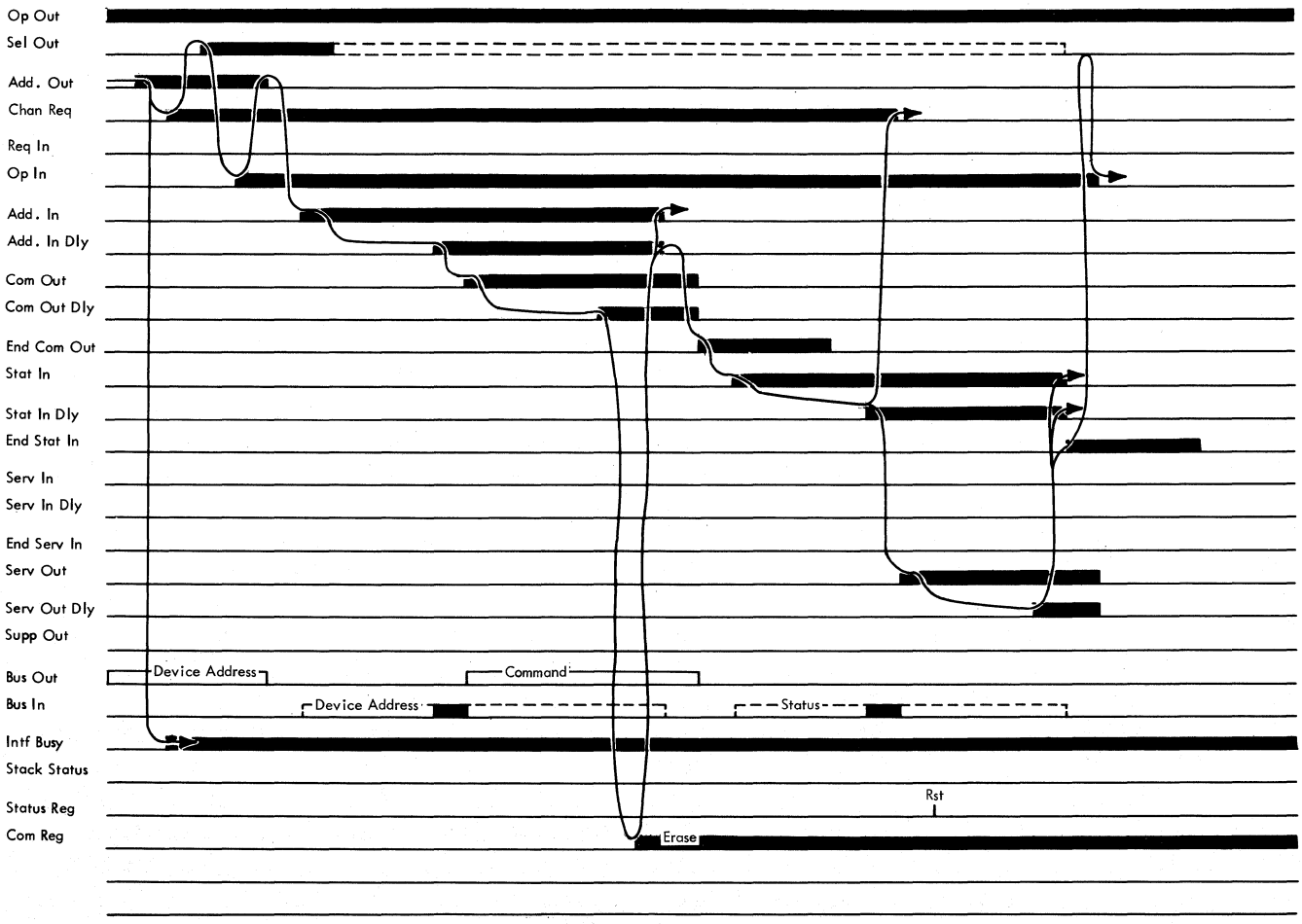


Figure 2-106. Erase Operation

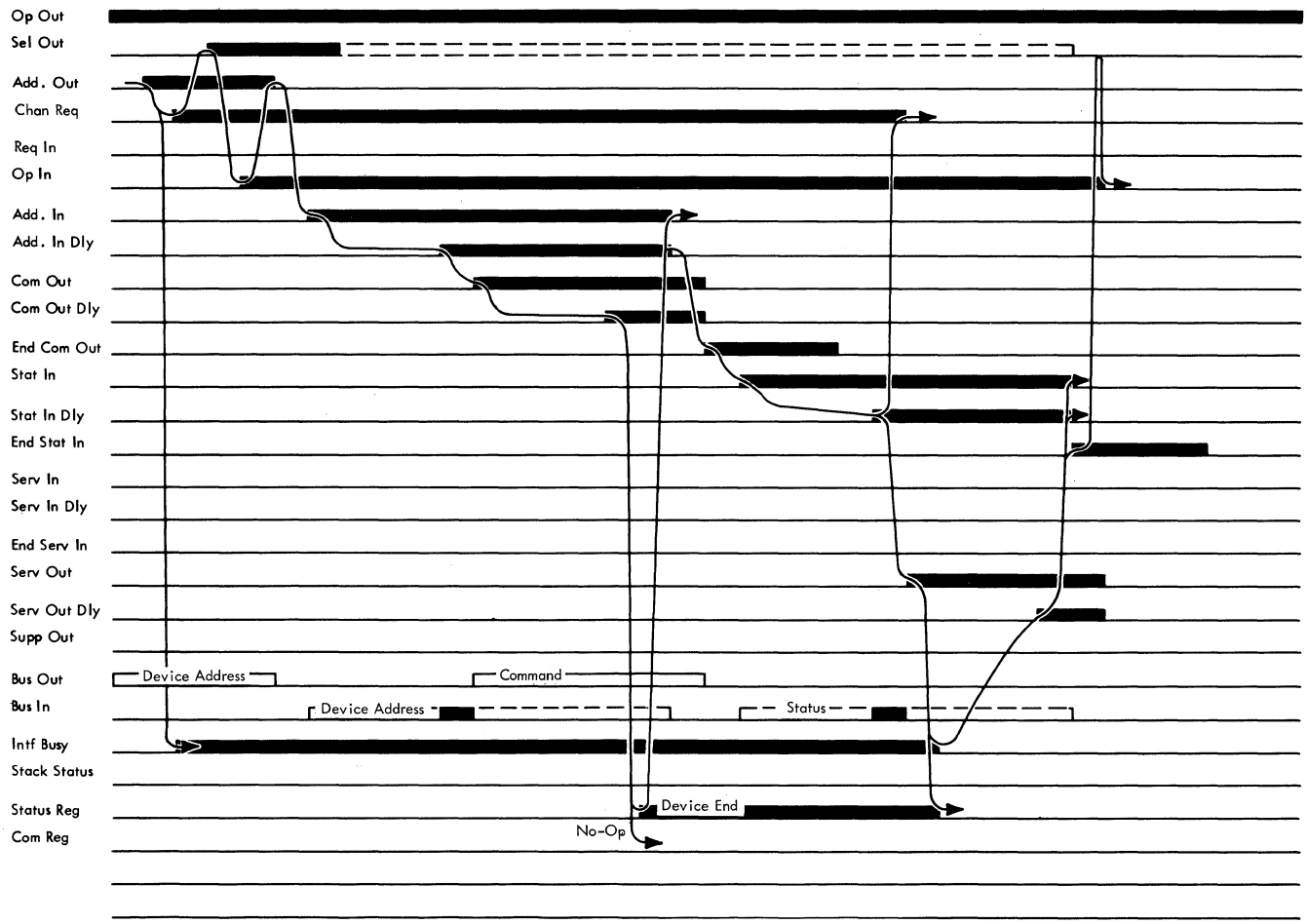


Figure 2-107. No Op Operation

(Service Out). As a result of the Test I/O command being specified by the command register, when the status byte is read by the channel, the Interface Busy latch is reset. At the end of the sequence, the command register is reset by the End Status In signal. Thus, when the test I/O sequence is completed, the channel and control unit are disconnected, and the control unit is left in a Reset state.

Command-To-Busy Device: The command-to-busy device sequence is the means whereby the channel obtains the status of a device even though that device is being used in another operation. This sequence functions in the manner described below only if status information is available and only if the addressed device is the same as the device selected. If these conditions are satisfied, a status byte is transferred to the channel. However, the status information depends upon the command specified. If the command is Test I/O, normal status (contents of the status register) is transferred. Any other command will cause busy status (busy bit and status modifier only) to be transferred.

The command-to-busy device sequence (Figure 2-109) is performed as follows:

1. The Interface Busy latch is already set from an operation in process.
2. The address of the selected device is contained in the address register.
3. A command is contained in the command register.
4. The status register contains attention or ending status.
5. The channel initiates this sequence by placing the address of the busy device on the Bus Out lines and raising the Address Out tag.
6. Because the Interface Busy latch is set, status is available, and the address on the Bus Out lines is the same as the address in the address register, the Device Busy latch is set. (If status were not present or if the address were illegal, the operation would be abandoned. If there were status but the addresses did not compare, the Device Busy latch would not be set.)
7. Since the Device Busy latch is set, when the

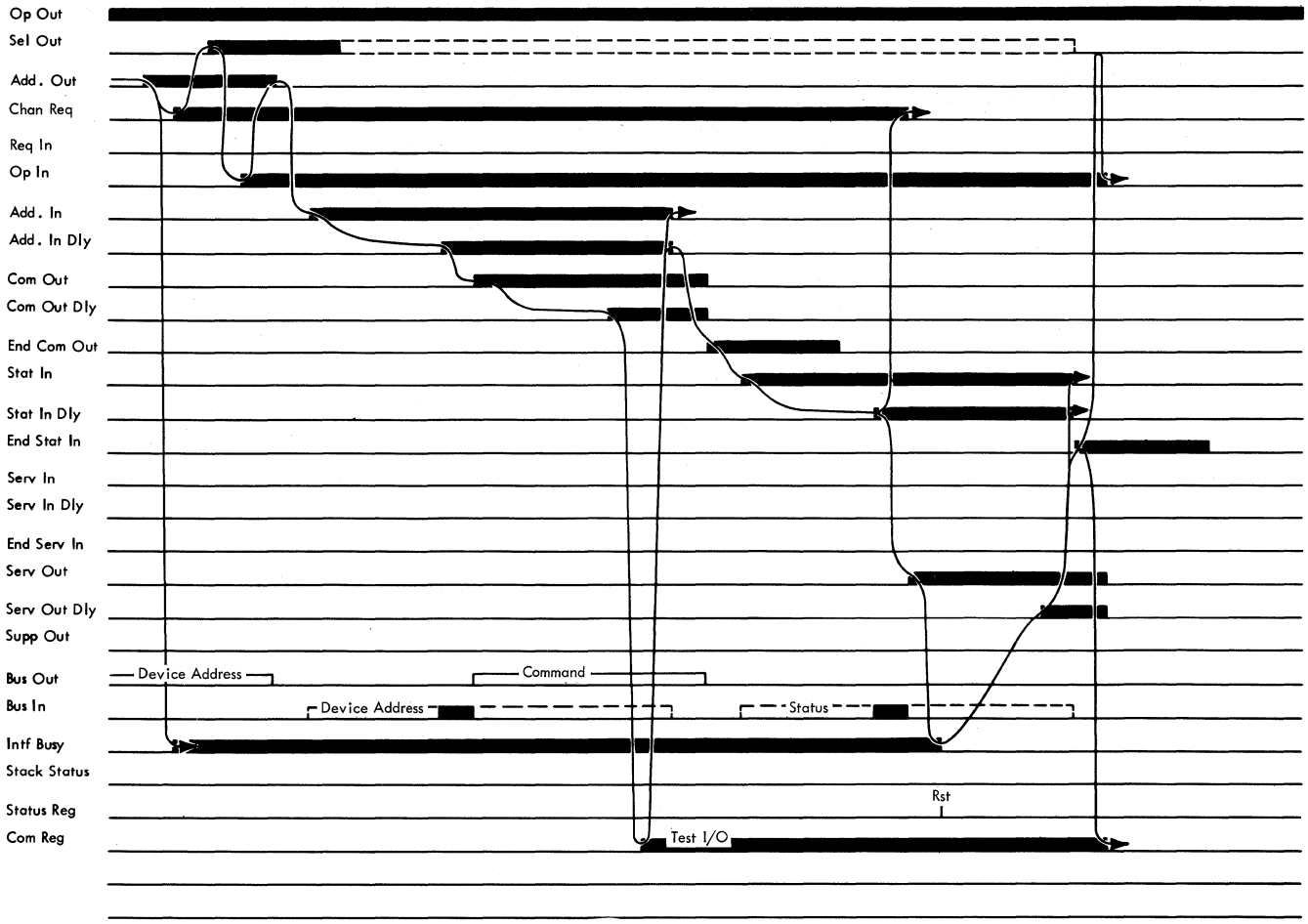


Figure 2-108. Test I/O Operation

Select Out line comes up from the channel, the Operational In latch is set to indicate to the channel that this operation is to continue.

8. The channel drops the Address Out line, and the control unit sets the Address In latch and places the contents of the address register on the Bus In lines.
9. The Address In tag is sent to the channel 1.2 μs after the Address In latch is set, notifying the channel to read Bus In.
10. The channel acknowledges the address by raising the Command Out tag.
11. The control unit decodes the command 1.2 μs later and responds to channel by dropping the Address In tag.
12. After the Command Out tag drops, the Status In latch is set, and the status byte is assembled on the Bus In lines. (If the command received was Test I/O, the contents of the status register are placed on the Bus In lines. Any other command results in a status byte that contains only the busy bit and the status modifier.)
13. Status In Delayed is sent to the channel as a Status In tag. The channel then reads Bus In.
14. When the channel responds with the Service Out tag, the Interface Busy and Device Busy latches and the status register are reset.
15. Service Out Delayed resets the Status In latch.
16. The End Status In signal resets the remaining controls (Operational In and the command register).

At the completion of the command-to-busy device sequence, the control unit is left in a Reset state.

Control Unit Busy: The control unit busy sequence is the response of a busy control unit to a channel-initiated selection of a device other than that which has caused the control unit to be busy. The control unit sends a status byte containing the busy bit and status modifier to the channel without going through the usual address verification (Address In) or command functions.

Figure 2-110 shows the sequence of events in the control unit busy operations. Before this sequence begins, the Interface Busy latch is set, the address

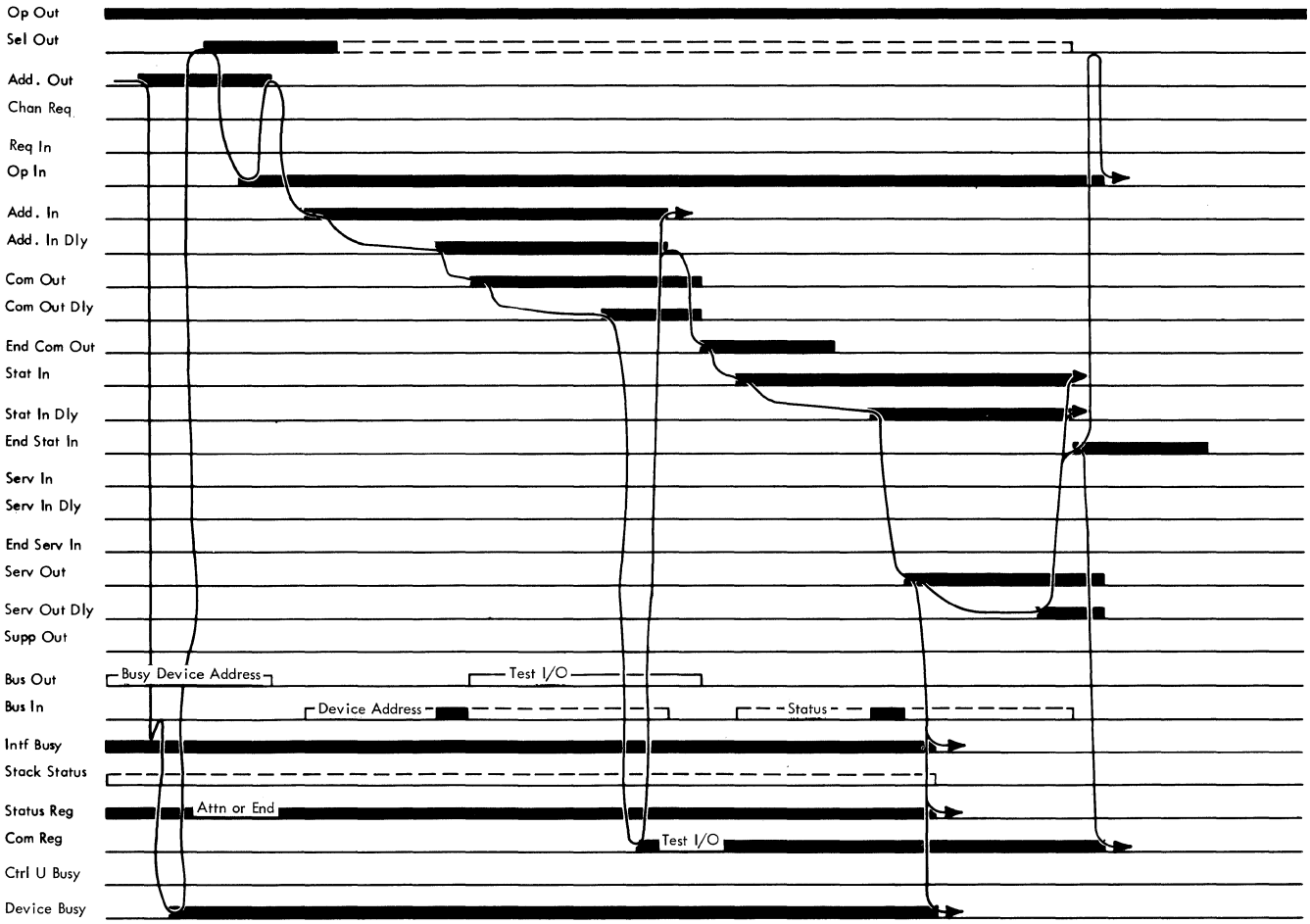


Figure 2-109. Test I/O To Busy Device

of a selected device is in the address register, and a command is set in the command register. The sequence proceeds as follows:

1. The channel places a device address on the Bus Out lines and raises the Address Out line.
2. The address is decoded and compared with the address register. (Although this is a legal address for our control unit, it is not the same as the selected device.)
3. Because the addresses do not compare, the Control Unit Busy latch is set.
4. When the Select Out line is raised by the channel, the Status In latch is set. (This is a result of the Control Unit Busy latch being set.)
5. A busy status byte is assembled on the Bus In lines, and the Status In Delayed signal is sent to the channel as a Status In tag.
6. The channel acknowledges receipt of the status byte by dropping the Select Out line.
7. Select Out drops and resets the Status In latch.
8. The Status In line drops, causing the channel to drop the Address Out tag.

At the completion of the control unit busy sequence, the control unit is left in the same state as it was before the sequence.

Control-Unit-Initiated Sequences

There are three control-unit-initiated sequences: data transfer, sense transfer, and status. The data and sense transfer sequences are control unit responses to channel-initiated selection sequences. The status sequence can be initiated as the ending to a channel-initiated selection or as a result of a device ENTER key being depressed. In the latter case, the channel is expected to respond with a channel-initiated read sequence.

Data Transfer: A data transfer sequence is performed for the transfer of each data byte during a read or write operation (Figure 2-111). The control unit is in the following condition at the beginning of each data transfer:

1. The Interface Busy latch is set.
2. The selected device address is in the address register.

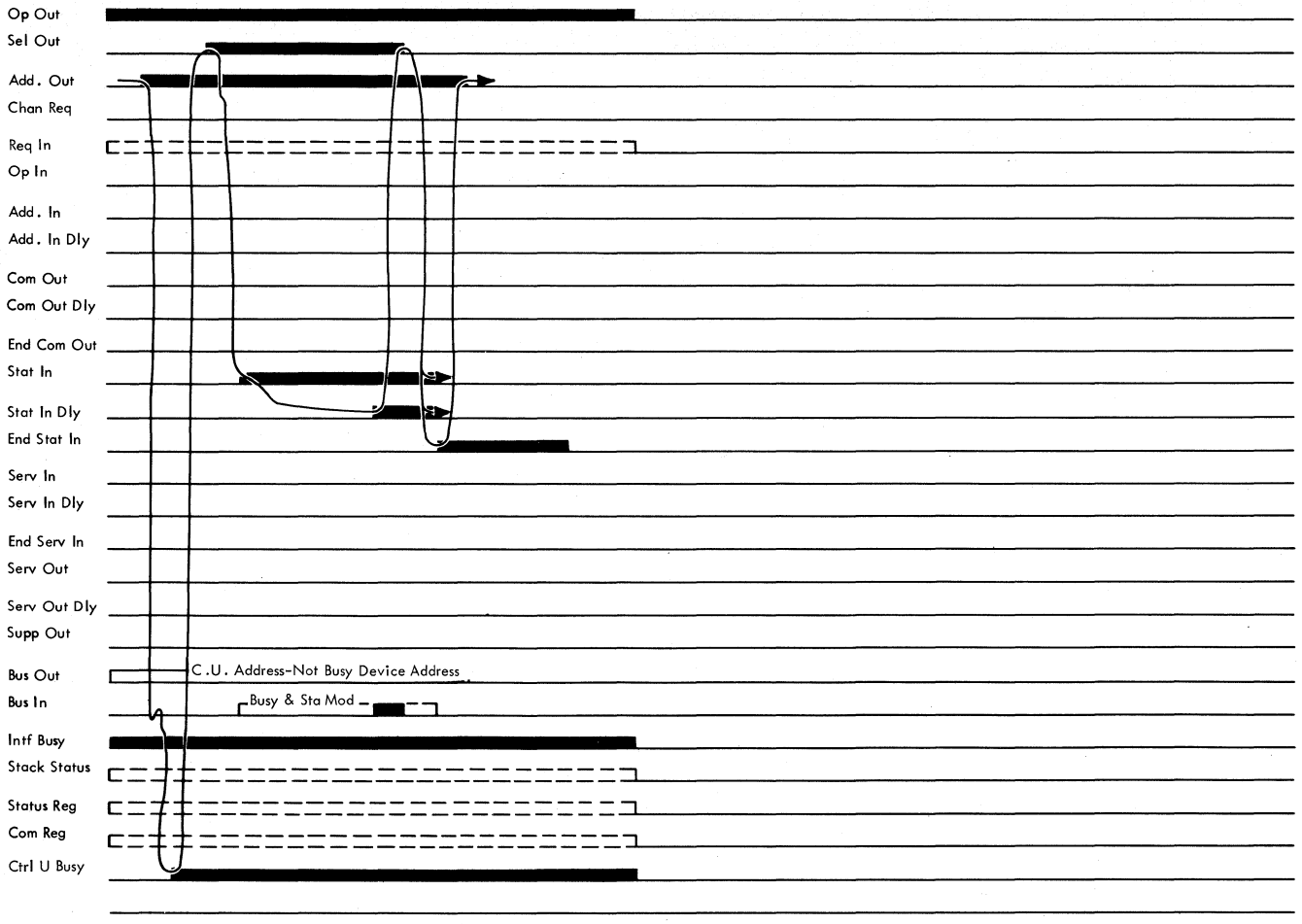


Figure 2-110. Control Unit Busy Sequence

3. A Read, Read Buffer, Write, or Write Line Address command is in the command register.

The data transfer is initiated by the control unit as follows:

1. When the control unit is ready to receive service (send or receive a data byte), the Control Unit Request latch is set, which causes the Request In signal to be sent to the channel. (This occurs in a write operation when the character register is reset and capable of receiving a new data byte. During a read operation, the control unit is ready when a data byte has been read and is loaded into the character register.)
2. The channel responds to the Request In signal by raising the Select line.
3. The Operational In latch is set as a result of the Select and Request In lines being up.
4. The Operational In signal sets the Address In latch, which causes the address register contents to be assembled on the Bus In lines.
5. The Address In tag (1.2 μs later) notifies the channel that an address is on the Bus In.
6. The channel acknowledges receipt of the address by raising the Command Out tag. (Unlike the channel-initiated sequences, the Command Out tag simply signals "proceed." No command is placed on the Bus Out lines as before.)
7. The Command Out Delayed signal resets the Address In latch, which drops the Address In tag.
8. The channel responds by dropping the Command Out tag.
9. The End Command signal sets the Service In latch.
10. If a Read command is specified, the Service In signal gates the data byte to the Bus In lines. Service In Delayed becomes the Service In tag, which notifies the channel that a byte is to be read (if the command specified is Read). Service In Delayed also resets the Control

Figure 2-111. Control Unit Initiated Data Transfer (Read or Write)

Unit Request latch, dropping the Request In line.

11. If a Write command is specified, the channel responds to the Service In tag by placing a data byte on the Bus Out lines and raising the Service Out tag.
12. In a read operation, the Service Out tag acknowledges receipt of the data byte. In a write operation, the Service Out tag causes a data byte to be loaded on the Bus Out lines.
13. Service Out Delayed resets the Service In latch, dropping the Service In tag. (In a write operation, the data byte is loaded into the character register from the Bus Out lines by Service Out Delayed.)
14. End Service In resets the Operational In latch, dropping the Operational In signal to the channel.
15. The channel responds by dropping the Service Out line.

Thus, the data transfer sequence for one byte is completed, and the control unit is left in the same status it was in before the sequence began.

One variation of this sequence should be described: the burst mode operation. If the channel has prescribed this mode of operation, it is possible to transfer one byte after another without going through the address and command (proceed) portions of the sequence. This is accomplished by having the channel hold up the Select line. Then, after the data byte is transferred, the End Service In signal will not drop the Operational In signal. The control unit sets the Service In latch as soon as the next byte can be transferred, and the Service In/Service Out portion of the sequence is repeated. This can continue until all bytes of the message are transferred without disconnecting from the channel.

Sense Transfer: The control-unit-initiated sense transfer is a result of the channel-initiated sense selection. This sequence transfers the contents of the sense register to the channel via the Bus In lines

and sets up the control unit to perform a status transfer following the sense transfer (Figure 2-112).

The control unit is left in the following status after a channel-initiated sense selection:

1. The Interface Busy latch is set.
2. The address register contains the address of the selected device.
3. The Sense latch is set in the command register.
4. The Channel Request latch is set, causing the Request In line to the channel to be up.

The sense transfer sequence (Figure 2-112) proceeds in a manner similar to the data transfer sequence, as follows:

1. The channel responds to the Request In signal by raising the Select Out line.
2. Operational In is raised by the control unit.
3. The Address In latch is set, and the address register contents are assembled on the Bus In lines.
4. The Address In tag (Address In Delayed) is generated.
5. The channel reads the address and responds with Command Out.
6. Command Out Delayed drops Address In.
7. End Command Out sets the Service In latch.
8. The Service In signal gates the sense register contents to Bus In and, in addition, sets the Status Request latch.
9. Service In Delayed resets the Service Request and Channel Request latches, dropping the Request In line. Service In Delayed is also sent to the channel as the Service In tag (data on Bus Out).
10. The channel acknowledges receipt of the sense byte by raising Service Out.
11. Service Out Delayed resets the Service In latch, dropping the Service In tag.
12. The End Service In signal resets the Operational In latch and the command register. In addition, since the Status Request latch is set, the Control Unit Request latch is reset, which results in raising the Request In signal to the channel.

Figure 2-112. Sense Transfer

At the completion of the sense transfer, the sense byte has been sent to the channel, and the control unit is left in the following condition to perform a status transfer:

1. The Interface Busy latch is set.
2. The address register contains the address of a selected device.
3. The Device End latch is set in the status register.
4. The Status Request latch is set.
5. The Control Unit Request latch is set, causing the Request In signal to be sent to the channel.

In this state, the control unit is conditioned to perform a control-unit-initiated status transfer sequence, which is described below.

Status Transfer: The control-unit-initiated status transfer is used by the control unit to cause an attention or ending status byte to be transferred to the channel. This sequence (Figure 2-113) may be initiated by the keyboard on an otherwise not-busy control unit, or the sequence may be the ending status byte transfer to a previous operation. If the keyboard initiates the operation, the control unit is in a reset state until the Attention bit is set. At that time, the Interface Busy latch, the Control Unit Busy latch, and the Control Unit Request latch are set. The latter raises the Request In line to the channel. The address of the device setting Attention is in the address register also.

If the status transfer is a result of a device end, the control unit is left in the following condition by the previous sequence:

1. The Interface Busy latch is set.
2. Ending status is in the status register.
3. The Status Request latch is set.
4. The Control Unit Request latch is set, and the Request In signal is sent to the channel.
5. The address of the selected device is in the address register.

Figure 2-113. Status Transfer

No matter which way the Control Unit Request latch was set, the sequence begins when the Request In line is raised to the channel and proceeds as follows:

1. The channel responds to the Request In by raising the Select Out line.
2. Operational In is raised by the control unit.
3. The Address In latch is set, and the contents of the address register are assembled on the Bus In lines.
4. The Address In tag (Address In Delayed) is generated to the channel.
5. The channel reads the address and responds with Command Out.
6. Command Out Delayed drops Address In.
7. End Command Out sets the Status In latch.
8. The Status In signal gates the contents of the status register to the Bus In lines.
9. Status In Delayed becomes the Status In tag, which notifies the channel that a status byte is on the Bus In.
10. Status In Delayed also resets the Control Unit Request latch, which drops the Request In line.
11. The channel acknowledges receipt of the status byte by raising the Service Out tag.
12. The Service Out tag resets the Interface Busy latch and the status register.
13. The Service Out Delayed signal resets the Status In latch.
14. The End Status In signal resets the Operational In latch, causing a disconnect from the channel.

At the completion of a control-unit-initiated status sequence, the control unit is left in the Reset state.

Special Sequences

Two special sequences are described in the following paragraphs: the stack status sequence, and the stop sequence.

Stack Status: The stack status sequence is the means whereby the channel refuses to accept a status transfer from the control unit. The channel may stack (refuse) any status byte transfer. The control unit completes the sequence without resetting the status register.

Figure 2-114 shows the stack status sequence as it would occur during a control-unit-initiated status sequence. Stack status can also be specified by the channel during the status byte transfer of a channel-initiated selection sequence. Since the difference in operation occurs during the status-in portion of any sequence, the description begins at the point where the Status In latch is set (Figure 2-114). The stack status sequence proceeds as follows:

1. Status information may or may not be available, depending upon whether this is a control-unit or a channel-initiated sequence.
2. Setting the Status In latch causes the contents of the status register to be assembled on the Bus In lines.
3. Status In Delayed becomes the Status In tag to the channel. The Status In Delayed signal also resets the Request latch (channel or control unit).
4. Since the channel will not accept this status byte, the channel responds to the Status In tag with a Command Out tag. (In the normal status transfer, the channel would respond with a Service Out tag.)
5. The Command Out response to a Status In results in setting the Stack Status latch.
6. The End Command Out Delayed signal resets the Status In latch and drops the Status In tag.
7. The channel responds by dropping Command Out.
8. When the Status In latch is reset, the End Status In signal resets the Operational In latch.

At the completion of the stack status sequence, the control unit is left in the following condition:

1. The Interface Busy latch is set.
2. Status information is available in the status register.
3. The Stack Status latch is set.
4. A device address is contained in the address register.
5. If the stack status occurred during a channel-initiated selection, there may be a command in the command register.

Since the Interface Busy latch is now set, the control unit will be in a busy state until the channel accepts the status by performing a Test I/O command operation using the command-to-busy device sequence.

Stop: The stop sequence is the means whereby the channel can terminate a read or write operation during a data transfer. Since the first portion of this sequence is the same as the normal control-unit-initiated data transfer, the discussion begins when the Service In latch is set (Figure 2-115).

1. If a read operation is in process, the Service In signal assembles the data byte on the Bus In lines.
2. The Service In Delayed signal resets the Control Unit Request latch, dropping the Request In line. The Service In Delayed signal is also sent to the channel as the Service In tag.
3. Since the channel is to terminate this operation, the response to Service In is the Command Out tag. (The usual channel response to Service In is Service Out.)

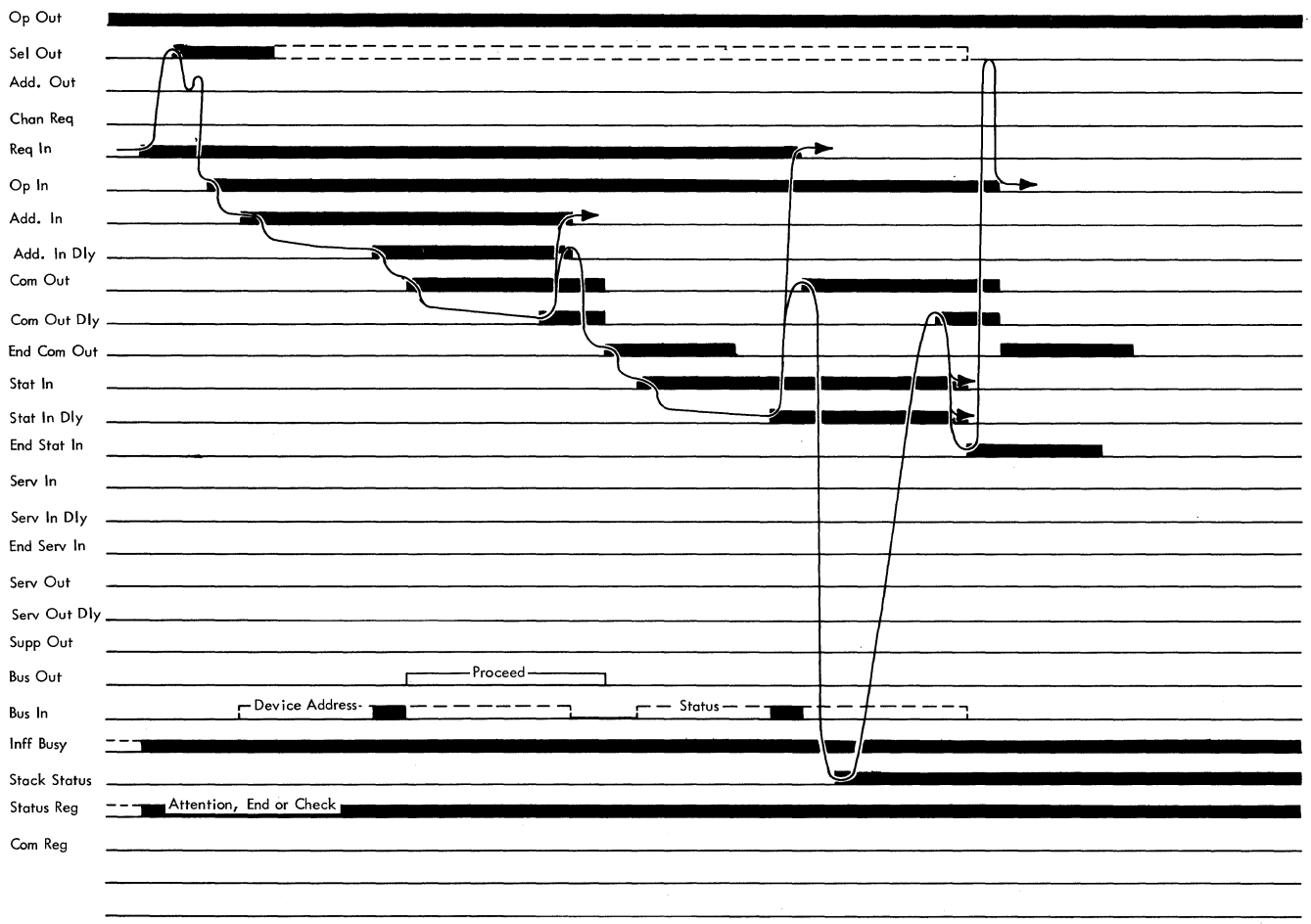


Figure 2-114. Stack Status Sequence

4. As a result of the Command Out response, the Operational In latch and the Service In latch are reset, and the Stop latch is set.
5. When the Service In latch is reset, the End Service In signal (under these circumstances) sets the Device End latch in the status register. The command register is reset.
6. As a result of the Device End and Stop latches being set, the Status Request latch is set, and the Stop latch is reset.
7. The Status latch sets the Control Unit Request latch, which generates the Request In line to the channel.

At the completion of a stop sequence, the channel is left in a state which will result in a control-unit-initiated status transfer of an ending status byte.

PRINTER ADAPTER

The printer adapter, shown in simplified form in Figure 2-116, contains the circuits necessary to operate an IBM 1053 Printer. The printer produces typed copy of selected displays presented on individual display stations. The typed copy is a permanent record that can be used by operating personnel for review and analysis. Data inputs to the printer adapter can also be supplied by the computer or remote interface. Operations from any of these sources are accomplished asynchronously on a data-demand and response basis.

A 7-bit tilt-rotate code, representing a character, is entered in Print In Buffer 1 (PIB1). The contents of PIB1 are then transferred to PIB2. Use of two input buffer registers allows the adapter to operate at a rate suitable to remote interface operations. Once the contents of buffer 1 are transferred to buffer 2, the next 7-bit tilt-rotate code representing the next character can be entered in buffer 1. A case-change check is then performed on the first character by decoding the case bit in buffer 2. Upper-case characters are coded with a 0 in the case bit. Lower-case characters are coded with a 1 in the case bit. The character presently in PIB2 is retained in the buffer until the case bit is decoded

Figure 2-115. Stop Sequence

and entered in the delay line. The tilt-rotate code in PIB2 is then written into the delay line. Odd parity is also assigned for each character input to the delay line.

Succeeding characters are loaded into the delay line in an identical manner. All characters stored in the delay line are automatically regenerated in the manner described for the delay lines in the paragraph entitled Display Adapter. When the Print Cycle latch is set by the printer control circuits, readout of the delay line contents is initiated by loading the printout buffer (POB) bit-by-bit. Parity is checked as data is read out of the delay line serially. A decode operation is performed to determine whether the POB contains a character code or a function code, and the proper lines to the printer are activated in accordance with the decoded output. The Off Line Selectric Analyzer (OLSA) Test line informs the printer control circuits that the operation has been completed and the next character or function code can be gated out of the delay line buffer and placed in the POB. Transfer of data to the printer adapter continues until an EOM occurs.

Printer Adapter Circuit Description

The following paragraphs describe the major logic areas that make up the printer adapter. Each circuit description is discussed in relation to overall printer operations, as shown in Figure 2-116.

Ring Counter

- Stepped by B Delay pulses supplied by display control every 500 ns.
- Provides nine sequential counts used for gating and timing operations within the printer adapter.

The bit ring counter contained in the printer adapter consists of nine triggers. It provides nine separate outputs in sequential order. The counter

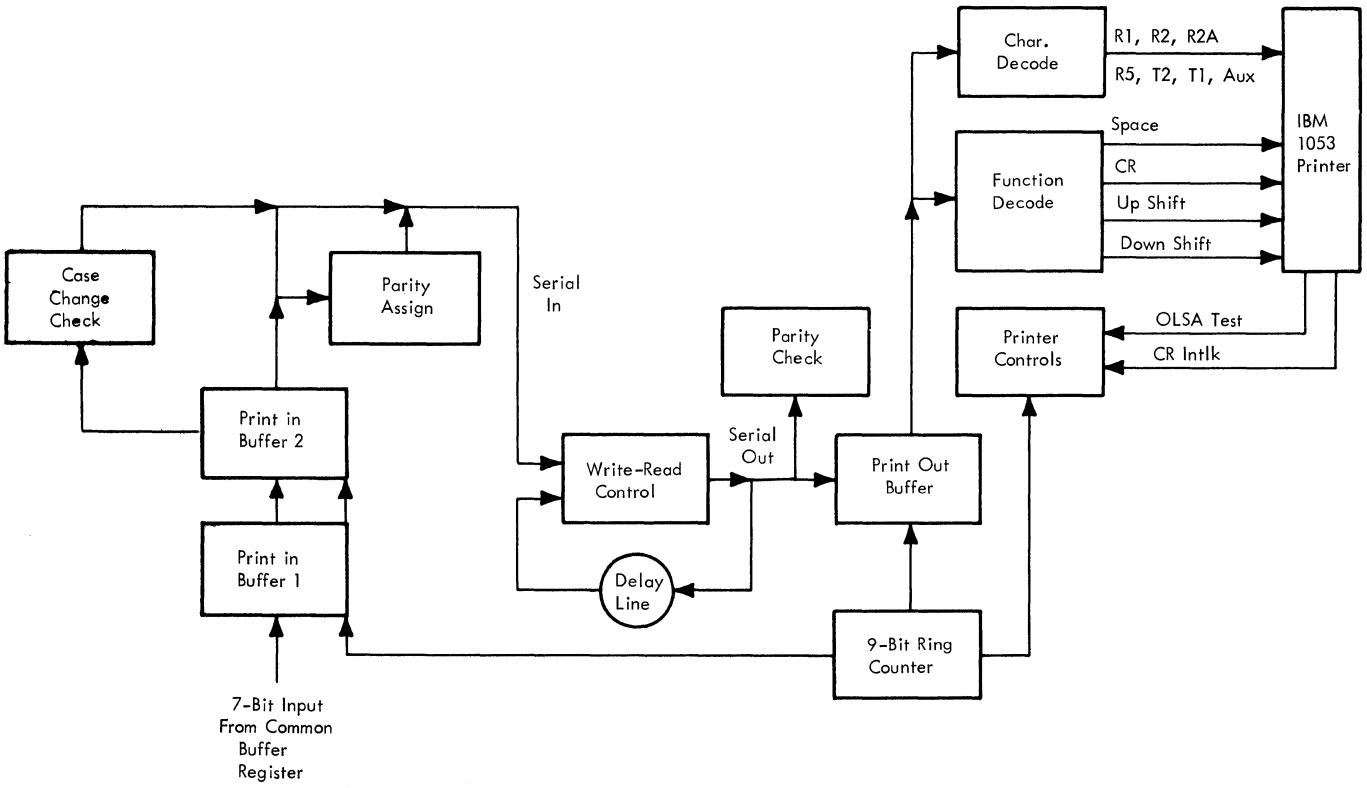


Figure 2-116. Printer Adapter, Simplified Block Diagram

is stepped by B Delay pulses supplied by display control. Operation of the bit ring counter is simply a stepping function of B Delay pulses. Outputs derived from the ring counter are designated -Y Ring Ctr 1 through -Y Ring Ctr 9. The outputs are used to gate data from register to register, to serialize information into and out of the delay line, and for a variety of other control functions throughout the printer adapter.

Print In Buffers

- Buffer character inputs to the printer adapter.
- Two buffer registers are used to speed up input operations.
- Each buffer consists of seven latch character inputs to the printer adapter.
- Upshift or downshift bit decode is performed when the character is stored in PIB2.

Two print-in buffers are used to buffer character inputs from display control to the printer adapter. The sources that provide character inputs to PIB1 can originate from the display station or from the local or remote interface. Tilt-rotate character codes, consisting of seven bits, are transferred from the common buffer register into PIB1. When PIB1 is loaded, the contents transfer to PIB2. The first buffer can now be cleared and reloaded with the next character.

Print In Buffer 1: Print In Buffer 1 consists of seven latches; it receives its inputs from the common buffer register. Bit information received from the common buffer register is made up of a tilt-rotate code which represents the character that is to be printed. Tilt-rotate codes are also used to perform special functions such as space, carrier return, upshift, downshift, or new line. Common buffer register bits transferred to the PIB1 latches are as follows:

CBR Bits	1	2	3	4	5	6	7
PIB1 Latches	Upper or Lower Case	T1	T2	R5	R2A	R2	R1

Print In Buffer 2: Print In Buffer 2 consists of seven latches. When PIB1 is loaded and proper synchronization has been established, the contents of PIB1 are transferred to PIB2. Here the character is checked to determine whether a shift character should be inserted in the delay line before the tilt-rotate code representing the character is written in it. Once PIB2 is loaded, PIB1 is cleared to prepare

it for the next character load. Serial readout of the PIB2 bits is gated by the following ring counts:

Ring Count	3	4	5	6	7	8
PIB2 Bits	R1	R2	R2A	R5	T2	T1

Case-Change Check

- Lower Case latch of PIB2 register stipulates whether the incoming tilt-rotate code is an upshift or downshift character.
- A 1 bit in the Lower Case latch denotes a downshift; a 0 bit signifies an upshift.

The case-change check logic decodes the Lower Case bit latch when the character is in the PIB2 register. If the Lower Case latch contains a 1, the downshift code is entered serially in the delay line. A 0 bit in the Lower Case latch programs an upshift code in the delay line. After the upshift or downshift code has been entered, the character stored in PIB2 is written serially into the delay line.

Parity Assignment

- Parity is assigned to each character entered in the delay, including upshift and downshift codes.
- Odd parity is used.

Each character entered in the delay line has a parity bit associated with it. Odd parity is employed. That is, if the total number of 1-bits that make up a character is even, the parity bit (1) is assigned; if the total number is odd, the parity bit (0) is assigned. Parity bit is written when the ring counter equals nine, following the last character bit which was written at eight time.

Delay Line

- Provides buffer storage for characters and function codes to operate the printer.
- Storage capacity is approximately 1220 9-bit characters.
- Information is written into the delay line in the character position that contains the write marker.
- Information is read out of the character position that contains the read marker.

The delay line used in the printer adapter is similar to the delay lines used in the display adapter. The length of the line is 5.5545 ms; the line has a capacity of approximately 11,000 bits. Each character stored in the delay line requires nine bits; hence, 1220 characters can be stored in the delay line. Bit entry into or out of the delay line is controlled by the 9-bit ring counter at a rate of 500 ns per bit. The format of a delay line character is as follows:

Character Bit Position	1	2	3	4	5	6	7	8	9
	Read Marker	Write Marker	R1	R2	R2A	R5	T2	T1	AUX*

*Check (Parity) bit

Information in the delay line is continually regenerated until the printer reads out and prints the character information. New information can be written into the delay line whenever it is supplied by PIB2 and a 1 is detected in the Write Marker bit. This bit informs PIB2 where the character can be loaded in the delay line. When the character is loaded, the Write Marker bit is advanced to the next character position.

Only one of 1220 character locations will contain a 1-bit in the read marker position. The read marker identifies the character that the printout buffer (POB) will read out during a print operation. When the character has been placed in the POB, the read marker is advanced to the next character. Both the read and write markers can occupy their respective bit locations (bits 1 and 2) in the same character position on two occasions; i.e., when the delay line is empty and when it is full. If the read marker is inserted in the character position containing the write marker, the buffer is empty. If the write marker is inserted in the character position containing the read marker, the buffer is full.

Parity Check Circuit

- Parity associated with each character is checked each time a character is read out of the delay line.
- If a parity error is detected, printing of the character is inhibited and the space function is performed. Quotation marks also appear after the EOM symbol (!").

Parity is checked when each character is read out of the delay line. A parity Check Out trigger is employed for this purpose. The Check Out trigger is initially set at Ring Counter 2 time; thereafter, the trigger is complemented each time a 1-bit is present for the character being read out. If the number of 1-bits associated with the character read out (including parity) is odd, the Check Out trigger is reset. Its condition is checked at Ring Counter 1 time. Detection of a parity error (set condition of Check Out trigger) at Ring Counter 1 time activates the Check Character latch, thus causing the printer to insert a space in place of the character and quotation marks (") after the end-of-message character (!).

Print Out Buffer

- Stores character information read out of the delay line.
- POB is a 7-bit latch register (with the AUX latch not used).
- Transfers tilt-rotate character codes to 1053 Printer and printer function codes to the function decoder.

The printout buffer (POB) is a 7-bit latch register that stores the tilt-rotate code read out of the delay line. Bit entry to the POB is controlled by the Print Cycle latch and the ring counter. Each POB latch input is controlled by the following ring counts:

Ring Count	3	4	5	5	7	8	9
POB Latch	R1	R2	R2A	R5	T2	T1	AUX

If the POB contains a character, its contents are gated to the 1053 Printer by the Enable Print latch level. Printer functions contained in the POB, such as space, upshift, downshift, and carrier return, are decoded in the function decoder circuit and are then routed to the printer.

Function Decoder

- The function decoder directs printer operation when a function code is present in the POB.
- The printer is inhibited from printing a character when a function code is in the POB.
- Function codes direct the printer to return carrier and line feed, space, upshift, and downshift.

The function decoder directs the operation of the printer when the POB contains a function code. The code is detected in the POB when the R2 latch is selected and the R1, R2A, and R5 latches are not selected. Under these conditions, transfer of the POB to the printer is inhibited, and the contents of the T1 and T2 latches are routed to the function decoder circuits. The T1, T2 and $\overline{T1}$, $\overline{T2}$ levels are decoded and routed to the printer to direct the following functions:

Status	Printer Function
$\overline{T1}$, $\overline{T2}$	Space
$\overline{T1}$, T2	Carrier return and line feed
T1, T2	Downshift
T1, $\overline{T2}$	Upshift

Keyboard Print Operation

- Only one display station can perform a Print command at one time.
- Messages from many display stations can be entered and buffered in the printer adapter delay line. As soon as an EOM is received from a display station, the printer adapter will honor another display station print request. The next message will be inserted following the last message in the delay line.
- A carrier return is performed at the start of each message.
- After the EOM symbol is printed, a carrier return is performed.
- A carrier return is performed when an NL is decoded or when the end of a line is reached on the display station.
- If a parity error is detected by display control, the questionable characters will be printed. The printed message will insert a quote symbol before the EOM character ("!). The quote symbol indicates that a character(s) in the printer message may be printed in error.
- Each tilt-rotate character stored in the printer buffer has a parity bit associated with it. If the printer adapter detects a parity error during readout operations, the character read out will be destroyed, and a blank space will be shown on the printed copy. A quote symbol will be printed after the EOM character (!").

Printer Adapter Input Operation

A print operation is initiated from the keyboard when the PRINT key is depressed. An EOM symbol is written on the CRT of the display station from which the print request was made, and the TIC is moved to the first character position on the screen. The Start of Print Read signal sets the 1053 Disp Sel latch, which places the printer adapter in a busy status. The first character is read from the display station buffer into the common buffer register so that the tilt-rotate code for the character can be extracted from the character generator. The tilt-rotate coded character is then transferred to the PIB1 register located in the printer adapter. Once the PIB1 register is loaded, the CBR to PIB1 signal is returned to display control. (See Figure 2-117, sheet 1.) Common then waits for a segment, row, column, and display compare. A compare of the preceding conditions indicates that the next character readout should be executed. (This occurs 390

μs after the first character was read.) If the printer adapter is not ready to accept another character (not Printer Char. Req), common will insert TIC in the character position and initiate an End Op. The TIC marks the character for the next readout operation from the display station buffer when common is again captured by the printer adapter. If the printer adapter were ready to accept another character, the next tilt-rotate code would be transferred to it.

Printer Operation, Case Change Not Required

As the first character enters the common buffer register and if the Print Cmd is active, AND 4 sets the Carrier Return latch (Figure 2-117, sheet 1). This generates a carrier return at the start of the print operation. The Char. to Prt signal transfers the contents of the common buffer to PIB1 and sets the PIB1 Ld trigger. At Ring Ctr 8 time, the PIB1 Sync trigger is set to synchronize operations between the two input buffer registers. AND 10 is held deconditioned by the set state of the Carrier Return latch until the carrier return code is placed in PIB2. This operation is executed under control of the Insert latch, at a ring count of 9 and during the reset status of the PIB2 Ld trigger, to condition AND 7, thus inserting the carrier return code in PIB2. Note that the PIB2 Ld trigger is complemented, indicating that buffer 2 is loaded. Assuming that the Case Hold latch is reset, no case change will be required.

Although at this time the reset condition of the Carrier Return latch would normally permit AND 10 to transfer PIB1 to PIB2, AND 10 is now deconditioned by the condition of the PIB2 Ld trigger. When the write marker is found and the delay line is not full (indicated by cleared condition of Read Marker latch), the Wrt Cycle latch turns on (Figure 2-117, sheet 2) to condition AND 17. The contents of PIB2 (carrier return code) are written into the delay line during ring counts 3 through 8. Odd parity for the carrier return code is inserted at a ring count of 9. As parity is inserted in the delay line, A11 resets PIB2 and complements the PIB2 Ld trigger to the reset side (Figure 2-117, sheet 1). Transfer of the contents of PIB1 to PIB2 occurs at a ring count of 1 (AND 10), and their associated load latches are complemented. AND 25 (Figure 2-117, sheet 2) cannot reset the Wrt Cycle latch (unless the carrier return character filled the delay line, thereby setting the Hold latch), and a write cycle will occur for the character in PIB2. At the completion of this cycle, the write marker will be written (AND 14) in the next character location at ring 2 time.

Printer Operation, Case Change Required

The following operations are executed if a character is loaded into PIB2 and a case change is required. The case-change operations are described from the point when PIB2 is loaded by AND 10 (Figure 2-117, sheet 1). If the case accompanying the character loaded in buffer 2 is the opposite of the case indicated by the Case Hold latch, the Set Shift signal prevents gating of the character presently in PIB2 and forces the proper shift code, utilizing AND's 7, 8, and 9. (See Figure 2-117, sheets 1 and 2.) Following this operation, the Case Hold latch is complemented to the proper state by AND 16 or 17. The Case Hold latch keeps track of the last case change inserted in the delay line. It does not indicate the shift status of the 1053 Printer. Two write cycles are executed: the first stores the shift change in the delay line, and the second stores the character in buffer 2. If the first write cycle fills the delay line, the Hold latch inhibits the second cycle until the delay line can accept the character. The Hold latch performs this operation by resetting the Wrt Cycle latch (AND 25) and inserting the wire marker (AND 15, Figure 2-117, sheet 2).

EOM and Display Adapter Parity Check

When EOM is decoded in the common buffer register, AND 23 sets the EOM latch shown in Figure 2-117, sheet 2, to signify that the end of message has occurred for the message entered in the printer adapter. The tilt-rotate code for the EOM character is transferred to PIB1. However, the input buffer cannot be transferred to PIB2 until the EOM latch is reset by an End Op originated by display control. Display control decodes the EOM character and checks parity for the message transferred to the printer adapter. After the parity check operation, display control activates End Op to reset the Kybd Sel latch, which clears the EOM latch. If a parity error has been detected by display control, the Check latch is set (Figure 2-117, sheet 1), and the EOM tilt-rotate code is retained in PIB1 because AND 10 is deconditioned. The set status of the Check latch permits the insert check (AND 6) operation to occur, which inserts a quote symbol (") in the delay line before the EOM symbol. The quote symbol (") is always inserted before the EOM character if a 2260 buffer parity check is detected in a keyboard print operation.

When EOM character is transferred to PIB2, the printer adapter can be selected by another display station. The not-busy status of the printer adapter is supplied to common by OR 26 (Figure 2-117, sheet 2).

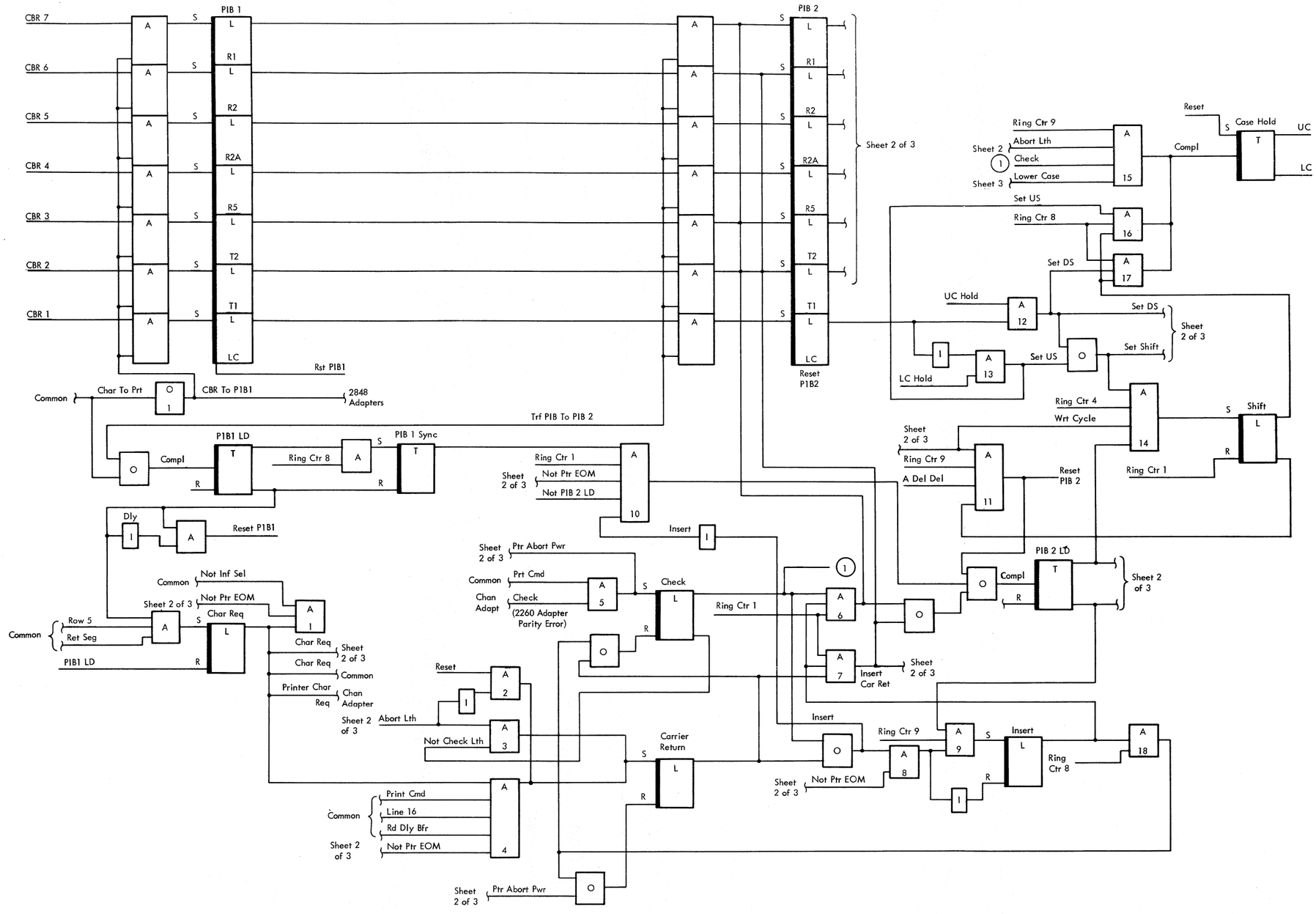


Figure 2-117. Printer Adapter, Logic Diagram (Sheet 1 of 3)

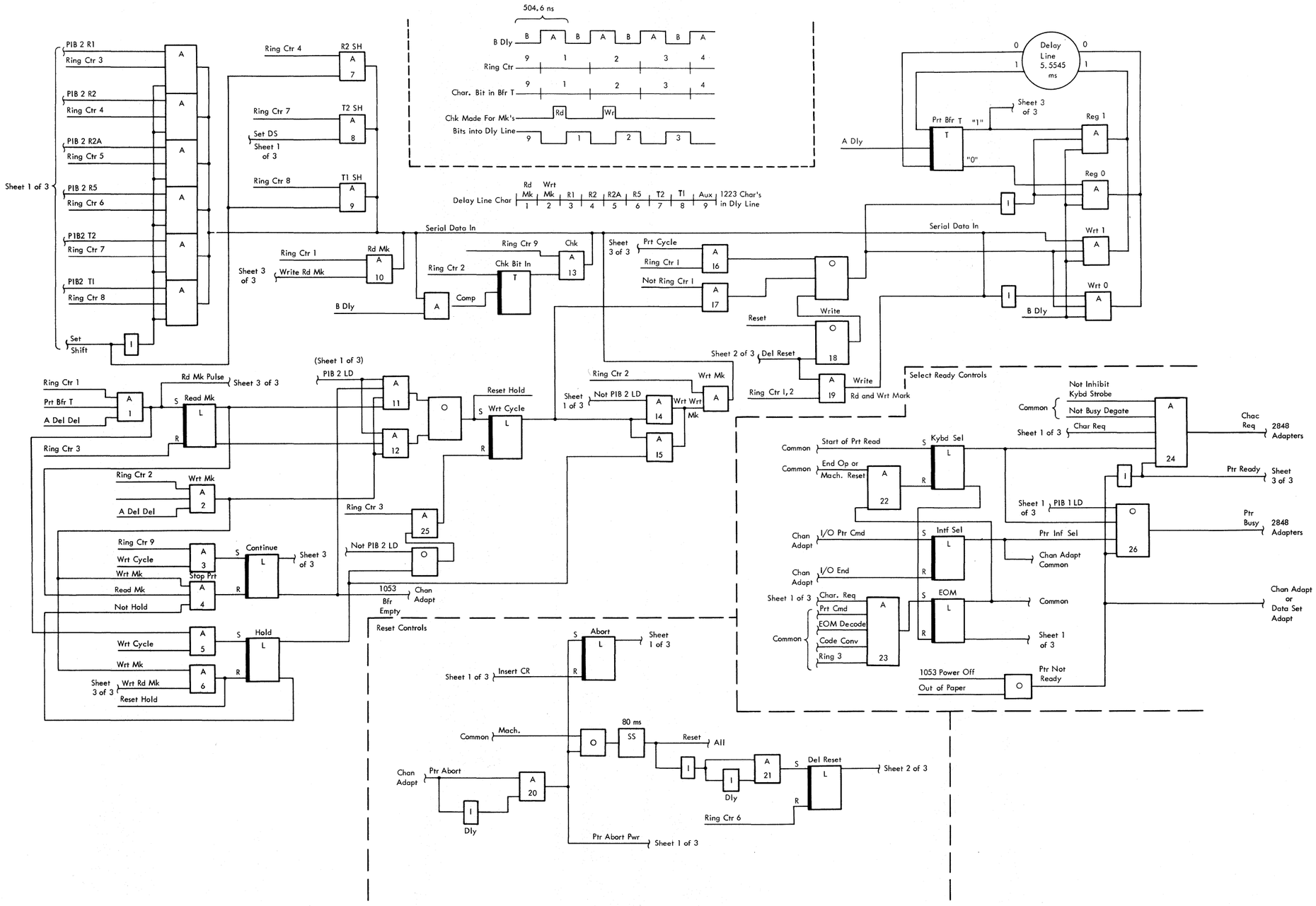


Figure 2-117. Printer Adapter, Logic Diagram (Sheet 2 of 3)

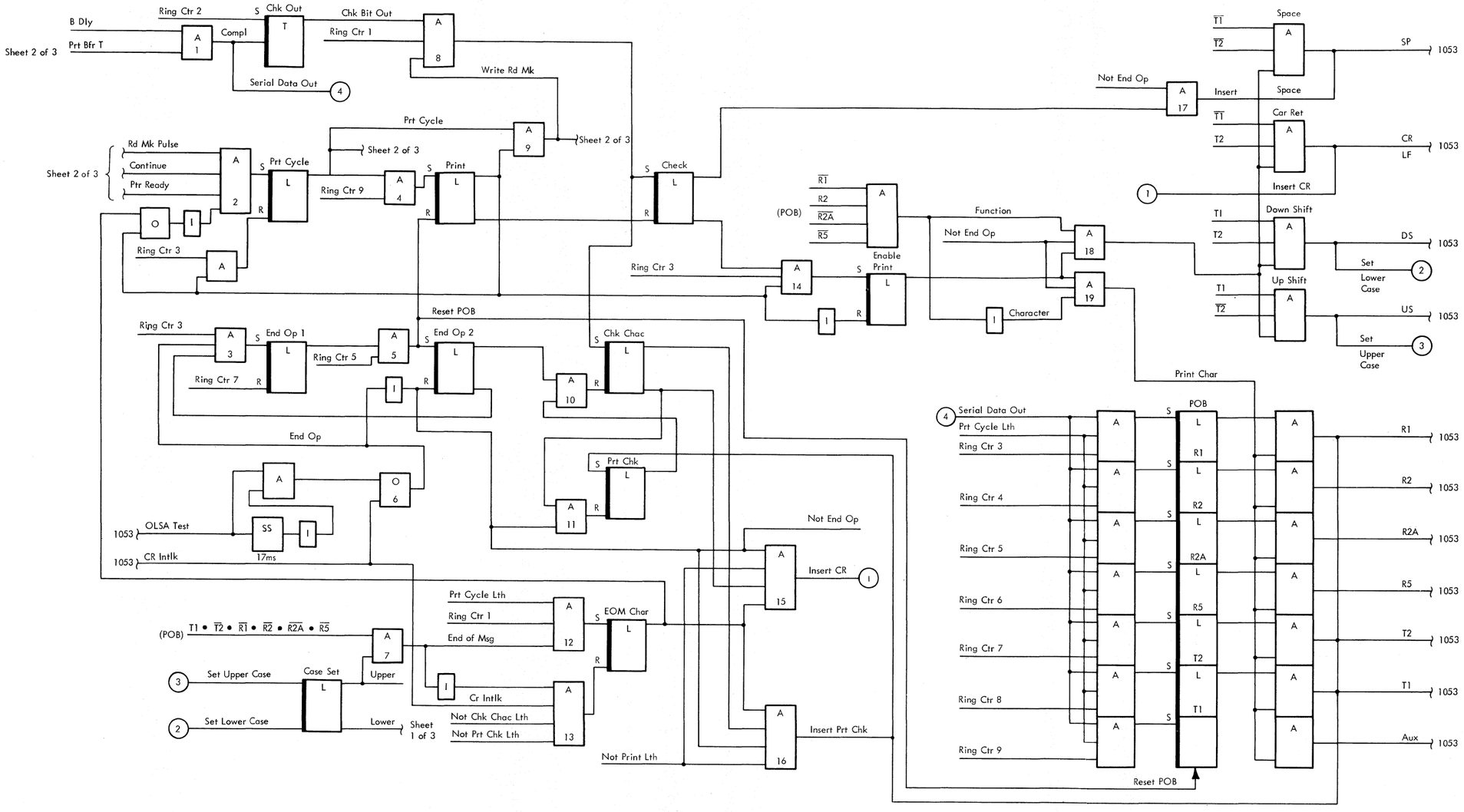


Figure 2-117. Printer Adapter, Logic Diagram (Sheet 3 of 3)

If operations cannot be maintained by the printer, such as when the delay line is full, PIB1 is full, etc., AND 24 is used to reinitiate character requests when the printer is ready. The Chac Req signal function is depicted in the display control flow chart contained in the Maintenance Diagram Manual.

Print Cycle Operations

Print Cycle and No Parity Check

The print cycle operation includes those operations necessary to read a character out of the delay line until the character is printed. The print cycle is initiated when AND 2 sets the Prt Cycle latch, which gates the character containing the read marker from the delay line to the POB. (See Figure 2-117, sheet 3.) Next in sequence, the Print latch is set at Ring Counter 9 time. This conditions AND 9, whose output initiates a parity check and inserts the read marker (AND 10, Figure 2-117, sheet 2) in the next character position. AND 16 becomes active twice while the Prt Cycle latch is on, once when the read marker is erased, and again when the read marker is inserted in the following character position. At Ring Counter 3, the Prt Cycle latch is cleared and the Enable Print latch is set in preparation to transfer the contents of the POB to the printer. The transfer is made by AND 18 if the POB content is a print function or by AND 19 if the content is a character function. A shift function also necessitates sending a Set or Clear signal to the Case Set latch, depending on whether an upshift or downshift was decoded.

Execution of the function or printing of the character by the printer is accomplished asynchronously, and, when it is completed, the printer responds with an OLSA Test or CR Intlk signal to set the End Op 1 latch via AND 3. The End Op 1 latch output conditions AND 5 at a ring count of 5 to reset the Print latch and POB and to set the End Op 2 latch. The preceding operations are repeated when the read marker is detected identifying the next character that should be read from the delay line.

Print Cycle with Parity Check

If a parity check occurs during a readout operation, the Chk Out trigger will be set at Ring 2 time to set the Chk Chac and Check latches at the next Ring 1 time. (See Figure 2-117, sheet 3.) The Check latch prevents printing of the character (AND 14) and forces the printer to space one character position (AND 17). After the printer spaces, the Check latch is reset, and the Chk Chac latch remains set. The next print cycle operates normally, as described under Print Cycle and No Parity Check, if a parity check does not recur.

Print Cycle with EOM and Chk Chac Latch On

The following operations occur if the Chk Chac latch is set and the EOM character is in the POB. Operations are described from the point when the Print latch is set by AND 4. The EOM code from the POB is used to set the EOM Char latch via AND's 7 and 12. Time is permitted to print the EOM character (!), and then the quote symbol (") code is forced into the printer through AND 16. After the quote symbol is printed, the printer adapter terminates the operation by setting the End Op 1 and End Op 2 latches. As a result of the End Op, AND's 10 and 11 reset the Chk Chac and Prt Chk latches. AND 15 forces a a carrier return operation to return the carrier in the printer, thus preparing it for the next operation. Once the carrier is returned, the EOM Char latch is cleared (AND 13, Figure 2-117, sheet 3). AND 2 then checks for more characters to be printed, which permits operations to continue.

Print Cycle with EOM Set and Chk Chac Latch Off

The following operations are executed if the EOM character is in the POB and the Chk Chac latch is reset. This signifies that an EOM has been detected and a parity check did not occur during readout of the preceding message. Operation of the printer adapter is described from the point at which the Print latch is set by AND 4. The EOM code in the POB is used to set the EOM Char latch via AND's 7 and 12. (See Figure 2-117, sheet 3.) Time is permitted to print the EOM character (!). After the EOM character is printed, the output of AND 15 forces the printer to execute a carrier return. AND 13 then resets the EOM Char latch to terminate the operation.

Write 1053 Buffer Storage

- A carrier return is not executed by the printer at the start of a print operation unless the first character is an NL code.
- If the processor transmits a message with more characters on a line than the printer line capacity, multiple characters will overprint in the last character position of the line until an NL character is received.
- A Bus Out Check on data transfer from the channel adapter causes the print operation to abort immediately. All characters in the printer buffer (delay line), PIB1, PIB2, and

POB are destroyed. A quote symbol is printed, followed by a carrier return.

- If the printer adapter detects a parity error during a character readout from its buffer, a space for the character in error is forced, and a quote symbol (") is inserted after the EOM (!) character.
- An EOM character must be the last data byte from the processor to cause an EOM symbol (!) to be printed as the last character of a message. A carrier return is performed following the EOM. A carrier return operation is performed only if preceded by an EOM at the completion of the message.

A Write 1053 Buffer Storage command, programmed by the processor via the channel adapter, is similar to the keyboard Print command. The following discussion concerns a Write 1053 Buffer Storage operation with an abort function. An abort function results when a Bus Out Check occurs, signifying that the operation must be immediately terminated due to a parity check. When the abort function occurs, the Ptr Abort signal from the channel adapter sets the Abort latch (Figure 2-117, sheet 2) and Check latch (Figure 2-117, sheet 1), resets the Carrier Return latch, and fires an 80-ms single-shot. The single derived from the 80-ms single-shot is used to reset all the latches and circuits in the printer adapter except the following:

Check Latch	Figure 2-117, sheet 1
Case Hold	Figure 2-117, sheet 1 (set)
Inf Sel	Figure 2-117, sheet 2
Abort	Figure 2-117, sheet 2
Case Set	Figure 2-117, sheet 3 (remember case of 1053)
Ring Counter	Set to a count of seven
Delay Line	Completely erased

After the 80-ms single-shot times out, the Del Reset latch is set (Figure 2-117, sheet 2), and the Case Hold latch (Figure 2-117, sheet 1) is complemented to lower case (AND 15) if the Case Set latch is in lower case. AND 9 sets the Insert latch, which permits AND 6 to insert the check character in PIB2. The load condition of PIB2 is indicated by the set condition of the PIB2 Ld latch. Both the read and write markers are written into the delay line at ring counts 1 and 2, respectively. At Ring 6, the Del Reset latch is cleared (Figure 2-117, sheet 2), and the Check latch is cleared at Ring 8 time (Figure 117, sheet 1). Once the Check latch clears, AND 3 sets the Carrier Return latch. Approximately 5.5 ms later, the write marker is read out of the delay line, and the check character in PIB2 is written into the buffer. If the Case Hold latch were reset (noted above), an upshift code would be inserted before the check character.

After the check character has been written into the delay line (Ring 9 time), AND 11 complements PIB2 Ld to the clear side, AND 9 sets the Insert latch, and AND 7 is fully conditioned at Ring 1 time to load the carrier return code in PIB2. Simultaneously, the Insert Car Ret signal is used to reset the Abort latch. The result of the abort operation is the check symbol (") and a carrier return. Since the abort operation is initiated immediately when a parity check is detected in the channel interface, the last character printed on the 1053, in most instances, will not be the last character transferred to the printer adapter. Recall that receipt of the Ptr Abort signal also erases the contents of the delay buffer.

GENERAL

This chapter describes machine operations that can be executed by the IBM 2848 Display Control and IBM 2260 Display Station. The operations reflect the more comprehensive control unit (Model 3) and display station with an alphanumeric keyboard attached to a channel adapter interface. This machine configuration is the largest (in terms of the number of characters displayed) and the most complex. Once Model 3 operation is understood, the operation of Models 1 and 2 will be apparent. All features that can be installed in the Model 3 are assumed to be a part of the machine configuration. When optional features can be attached, each feature is described in detail in the operation or sequence where the optional feature affects machine operation.

Channel-initiated commands and keyboard operations described in this chapter are illustrated in various types of diagrams (i.e., flow charts and IOP diagrams) provided in the FE Diagram Manual, IBM 2260 Display Station and IBM 2848 Display Control, Form Y27-2048.

CHANNEL ADAPTER OPERATIONAL SEQUENCES

The channel adapter feature interfaces the IBM 2848 Display Control Unit with a System/360 selector or multiplexor channel. Interfacing of these units through the channel (local) adapter can be accomplished in one of three ways: channel-initiated sequences, control-unit-initiated sequences, or by two other operations termed special sequences. All of the sequence types are discussed in the following paragraphs.

Channel-Initiated Sequences

The basic operation of a channel-initiated selection is described in terms of a read or write selection. Other sequences are then described in terms of the way they differ from the basic read-write selection.

Read or Write Selection

- Establishes channel-to-unit communications.
- Addresses a device (2260 Display Station or 1053 Printer).
- Transfers the command that dictates the operation to be executed.
- Applicable figures: FC-1 and IOP-10.

The channel initiates a read or write sequence by sending a device address on the Bus Out lines, together with Select Out and Hold Out. If the address transmitted to the local interface is a legal address (pertains to a device attached to the control unit), the Control Unit Request latch is set. The Interface Busy latch is turned on to indicate that the local interface is in use; hence, any future requests for service are inhibited. At the same time, the channel adapter address register is loaded and Operation In is sent to the channel, which indicates that the control unit is ready. When Address Out drops, the device address is transmitted to the channel so that the command can be received. Thus, the command register can be loaded (assuming the command is legal and of the correct parity) when the Command Out tag becomes active. The command is analyzed, and if it is not a Test I/O, Print, or No Operation command, the Address In tag is dropped, signifying that the control unit has accepted the command. When Command Out drops, the status of the 2848 channel adapter is examined. If a read, write, or erase command had been received, the sense register and Channel Request latch are reset and the Status In latch is set. When channel responds with Service Out (indicating status was accepted), both the status register and Status In tag are reset. Since the channel will have dropped the Select line earlier, the End Service Out and Not Select Out signals cause the Operational In latch to be reset. This notifies the channel that the sequence is completed, and the channel responds by dropping the Service Out line. The channel-initiated selection (read or write) is now complete. The channel and control unit are disconnected from each other (temporarily), and when the 2848 is ready to perform a data transfer, the control-unit-initiated data transfer sequence will begin. This sequence is discussed in the paragraph titled "Control-Unit-Initiated Sequence".

Sense

- Channel requests the contents of the sense register, followed by a status transfer.
- Operation ends with Device End set in the Status byte and with Status Request, Interface Busy, and Operational In latches turned on.
- Applicable figures: FC-1 and IOP-14.

The channel-initiated selection for a sense command is programmed whenever the contents of the

sense register are to be transferred to the channel. Sense operations are identical with a channel-initiated read (write) selection up to the point where the Operational In latch is reset. Because the Sense latch in the command register is set, when the Operational In signal drops, the Service Request latch is set. The output of the Service Request latch sets the Control Unit Request latch, which causes generation of the Request In signal to the channel. At this point, the channel-initiated sense sequence is completed, and further action on the sense transfer is under control of the display common equipment described under "Control-Unit-Initiated Sequences."

The channel-initiated sense selection leaves the control unit in the following state:

1. Interface Busy latch is set.
2. Address register contains the address of the device selected for a Sense byte transfer.
3. The Sense latch is set in the command register.
4. The Device End latch is set in the status register.
5. The Service Request latch is set.
6. The Channel Request latch is set, and its output generates the Request In signal to the channel.

Erase

- Allows channel to select a device and erase the buffer storage for that device.
- Sequence of events for selection is identical with channel-initiated selection for read or write except that Erase latch is set.
- Applicable figures: FC-1 and IOP-19.

The sequence of events for a channel-initiated erase sequence is identical with a channel-initiated read or write sequence. However, because the erase command has been programmed, the Erase latch is set in the command register. Once this is accomplished, the channel is disconnected from the control unit. The control unit is maintained in a Busy state to allow the erase operation to be performed. Upon completion of this operation (8 ms to 24.5 ms), the control unit notifies the channel by initiating a status sequence.

No Operation

- No-operation sequence is similar to the basic read-write selection sequence.
- No command (No Op) is set in the command register; hence, the Device End latch is set in the status register.
- All controls are reset in the control unit.
- Applicable figures: FC-1 and IOP-12.

The no-op sequence is similar to the basic channel-initiated selection sequence. The major difference is that, as a result of the No-Op command being decoded, no command is set in the command register, and the Device End latch is set in the status register. Hence, the Status byte indicates ending status. The Interface Busy latch is reset by Service Out, and, when the Operational In latch is reset at the end of the sequence, the control unit control circuits are reset and the unit is disconnected from the channel.

Test I/O

- Test I/O command is used by the channel to obtain status of a device.
- When status is transferred to channel, the Interface Busy latch is reset.
- Applicable figures: FC-1 and IOP-11.

The test I/O channel-initiated sequence is used by the channel to obtain the status of any device. This sequence is identical with the channel-initiated selection up to the end of the Status byte transfer (Service Out). As a result of the Test I/O command specified by the command register, the Status byte is transferred to the channel and the Interface Busy latch is reset. At the end of the sequence, the command register is reset by the End Status In signal. The channel and control unit are disconnected and the control unit is left in the reset state.

Command to Busy Device

- This sequence permits channel to obtain status of a device that is busy.
- Addressed device must be the device which is busy.
- Status byte is transferred to channel.
- Applicable figures: FC-1 and IOP-16.

The command-to-busy-device sequence permits the channel to obtain the status of a device even when the device is performing another operation. This sequence functions as described only if status information is available and the addressed device is the same as the device selected. If these conditions are satisfied, a Status byte is transferred to the channel. The content of the Status byte is dependent upon the command specified. A Test I/O command dictates that normal status is transferred. Any other command will cause only the Busy bit and status modifier to be transferred.

Initially, the Interface Busy latch is set from a previous operation and the address of the selected

device is contained in the address register. A command is in the command register, and the status register contains Attention or Ending status.

Channel initiates the command-to-busy-device sequence by placing the address of the busy device on Bus Out and raising the Address Out tag. Since the Interface Busy latch is set, status is available, and the address on Bus Out corresponds to the address in the address register, the Device Busy latch is set. If the address were illegal or status were not present, the operation would be aborted. (If a status byte were available but the addresses did not compare, the Device Busy latch would be set.) Because the Device Busy latch is set, the Operational In latch is set (when Select Out line becomes active), informing the channel that the operation is to continue. Channel then drops the Address Out line, and the control unit sets the Address In latch and routes the contents of the address register on the Bus In lines. When the address has been received, channel responds with Command Out. The control unit decodes the command, and, after the Command Out tag drops, the Status In latch is set and the Status byte is assembled on Bus In. (If the command received was a Test I/O, the content of the status register is placed on Bus In. Any other command results in a Status byte which contains the Busy bit and status modifier.) When channel receives the device status, it responds with Service Out, which resets the Interface Busy and Device Busy latches and the status register. Remaining controls are reset by the End Status In signal.

Control Unit Busy

- This sequence permits channel to obtain status of a device when another device is tied to the display control unit.
- A Status byte containing the Busy bit and status modifier is sent to channel.
- Applicable figures: FC-1 and IOP-16.

This sequence is similar to the command-to-busy Device sequence. Because the address (legal address) placed on the Bus Out lines do not compare with the device presently tied to the control unit, the Control Unit Busy latch is set. Consequently, a busy Status byte (Busy bit and status modifier) is assembled on the Bus In lines for transfer to channel. At the completion of the control-unit-busy sequence, the control unit is left in the same state as it was before the sequence.

Control-Unit-Initiated Sequences

There are three control-unit-initiated sequences: data transfer, sense transfer, and status. The data and sense transfer sequences are responses provided by the control unit to channel-initiated selection sequences. The status sequence is a response supplied by the control unit to terminate a channel-iniaited selection or as a result of a keyboard Enter key being depressed. If an Enter key initiates the status sequence, the channel is expected to respond with a Read operation to service the display station.

Data Transfer

- The data transfer sequence is performed to transfer a Data byte during a Read or Write operation.
- Applicable figures: FC-1, IOP-20, and IOP-28.

When the control unit is ready to receive service (send or receive a Data byte), the Control Unit Request latch is set, which causes the Request In signal to be sent to channel. This occurs in a Write operation when the character register is reset and capable of receiving a new Data byte. During a Read operation, the control unit is ready when a Data byte has been loaded into the character register from the CBR. Channel responds to the Request In signal by raising the Select line to set the Operational In latch. Next in sequence, the Address In latch becomes active, which permits the address register contents to be assembled on the Bus In lines. The Address In tag notifies the channel that an address is on the Bus In. Receipt of the address on Bus In is acknowledged by channel by making Command Out active. In this case, the Command Out tag signifies "proceed," but no command is placed on the Bus Out lines, though it would be in the case of a channel-initiated sequence. Command Out (delayed) resets the Address In latch. Channel responds by dropping the Command Out tag to set Service In.

If a Read command is specified, the Service In signal gates the Data byte to the Bus In lines. Service In (delayed) becomes the Service In tag, which notifies the channel that a byte is to be read. Service In Delayed also resets the Control Unit Request and Service Request latches. The Service Out tag signifies that the channel has received the Data byte.

If a Write command is specified, the channel responds to the Service In tag by placing a Data byte on the Bus Out lines and raising the Service Out tag. Service Out Delayed resets the Service In latch and loads the character register with the Data byte from the Bus Out lines.

End Service In resets the Operational In latch, dropping the Operational In signal to the channel.

The channel responds by dropping the Service Out line. Thus, the data transfer for one byte (read or write) is completed. If the channel had prescribed the burst mode of operation, it would have been possible to transfer one byte after another without readdressing and reissuing the command portion of the sequence. This is accomplished by keeping the Select line active after the Data byte has been transferred, and the Service In/Service Out portion of the sequence is repeated. In this manner, Data bytes can be continually transmitted until all bytes of the message are transferred without disconnecting from the channel.

Sense Transfer

- Transfers the contents of the sense register to the channel via the Bus In lines followed by a status transfer.
- Applicable figures: FC-1 and IOP-14.

This sequence transfers the contents of the sense register to the channel and sets up the control unit to perform a status transfer following the sense transfer. Note, however, that a sense operation is always preceded by a channel-initiated sense selection. Its purpose is to inform the channel of the condition of a particular device. A response from the control unit is mandatory to complete the interrogation. Assuming that the channel-initiated sense selection has been executed, the following conditions exist in the control unit:

1. Interface Busy latch is set.
2. Address register contains address of selected device.
3. Sense latch is set in the command register.
4. Channel Request latch is set, thus making available the Request In line to the channel.

The sense transfer continues when channel responds to the Request In signal by raising the Select Out line. Operational In is raised by the control unit. When the Address In latch is set, the address register contents are assembled on the Bus In lines for transfer to channel. Upon receipt of the address, channel responds with Command Out to drop Address In. The Service In latch becomes active (by output of End Command Out latch); its output gates the sense register contents to Bus In and, in addition, sets the Status Request latch. Service In Delayed resets the Service Request and Channel Request latches, dropping the Request In line. Service In Delayed is also routed to the channel as the Service In tag, signifying that data is available on Bus Out. Channel then acknowledges receipt of the Sense byte by raising Service Out which, in turn, resets the Service In latch. To conclude the sense operation, the End Service In signal resets the Operational In latch and the command register. Since the Status Request latch remained on, the Control Unit Request latch is reset, which results in raising the Request In signal to the channel. At this time, the Sense byte has been transferred to the channel and the control unit is left in the following condition to perform a status transfer:

1. Interface Busy latch is on.
2. Address register contains address of selected device.
3. Device End latch in status register is set.
4. Status Request latch is set.
5. Control Unit Request latch is set, generating the Request In signal to be sent to the channel.

The control unit is now ready to perform a control-unit-initiated status transfer sequence, which is described below.

Status Transfer

- Permits control unit to transfer Attention or Ending status to the channel.
- Operational sequence can be initiated by control unit or keyboard.
- Applicable figures: FC-1 and IOP-18.

A control-unit-initiated status sequence is issued by the control unit to transfer Attention or a Status byte to the channel. This sequence can be initiated by a keyboard or can be associated with an Ending Status byte transfer to a previous operation. If a keyboard initiates the operation, the control unit is in a Reset state until the Attention bit is set. At this time, the Interface Busy, Control Unit Busy, and Control Unit Request latches are set. The latter raises the Request In line to the channel. At the same time, the address of the device setting Attention is in the address register.

If the status transfer is a result of a Device End, the control unit circuits are conditioned as listed under Sense Transfer. Regardless of the conditions under which the Control Unit Request latch was set, the sequence begins when the Request In line is raised to the channel and proceeds as described below.

Channel responds to Request In by raising the Select Out line. Operational In is raised by the control unit. The Address In latch is set, which assembles the contents of the address register on the Bus In lines. At the same time, the Address In tag is generated to inform the channel that the device address is on Bus In. The channel reads the address and acknowledges its acceptance with Command Out. Command Out (delayed) drops Address In and sets the End Command Out latch

which, in turn, sets the Status In latch. Once the Status In latch has been set, a signal derived from its output (Status In) gates the contents of the status register to the Bus In lines. The Status In signal (delayed) is used to inform the channel that a Status byte is on the lines and to reset the Control Unit Request latch. This last action drops the Request In line. Receipt of the Status byte is acknowledged by channel by means of the Service Out tag which resets the Interface Busy and Status In latches and the status register. The End Status In signal clears the Operational In latch, causing a disconnect from the channel. At the completion of a control-unit-initiated status sequence, the control unit is left in the Reset state.

Special Sequences

Two special sequences are described in the following paragraphs: the stack status sequence and the stop sequence.

Stack Status

- Permits channel to reject (stack) a Status byte transfer.
- Control unit completes sequence without resetting the status register.
- Applicable figures: FC-1 and IOP-15.

The stack status sequence allows the channel to stack (reject) a status transfer from the control unit. Rejection of a Status byte by the channel can occur during any Status byte transfer, and when a stack status sequence is employed, the control unit completes it without resetting the status register. The stack status sequence operates as it would during a control-unit-initiated status sequence. Stack status can also be specified by the channel during the Status byte transfer of a channel-initiated sequence. Since the difference in operation occurs during the status-in portion of any sequence, the description begins at the point where the Status In latch is set. The operational sequence is as follows.

Status information may or may not be available, depending upon whether this is a control-unit or channel-initiated sequence. Setting the Status In latch causes the contents of the status register to be assembled on the Bus In lines. The Status In (delayed) line becomes the Status In tag to channel and is also used to reset the Request latch in the channel or control unit, depending upon which unit originated the status sequence.

Since the channel is to reject this Status byte (stack status sequence), the channel responds to the Status In tag with Command Out. In a normal status transfer, the channel would respond with a Service Out tag. The Command Out response to a Status In causes the Stack Status latch to be set, and the End Command Out (delayed) signal resets the Status In latch to drop the Status In tag. Channel responds by dropping Command Out. When the Status In latch was reset, the End Status In signal cleared the Operational In latch.

At the completion of the stack status sequence, the control unit is left in the following condition:

1. Interface Busy latch set.
2. Status information is maintained in status register.
3. Stack Status latch set.
4. A device address is stored in address register.
5. If a stack status occurred during a channel-initiated selection, a command byte may be stored in the command register.

Because the Interface Busy latch is now set, the control unit will be maintained in the Busy state until the channel accepts the Status byte by executing a Test I/O command operation, making use of the command-to-busy device sequence.

Stop

- Sequence used by channel to terminate a Read or Write operation during a data transfer.
- Applicable figures: FC-1 and IOP-17.

The stop sequence is used by the channel whenever the need arises to terminate a Read or Write operation during a data transfer. Since the first portion of this sequence is identical with a normal control-unit-initiated data transfer, the description of the operation is given from the point when the Service In latch is set.

If a Read operation is in process, the Service In signal assembles the data byte on the Bus In lines. The Service In (delayed) signal is fed to the channel as the Service In tag and also resets the Control Unit Request latch, deactivating the Request In line. Because the channel must terminate this operation, the response to Service In is the Command Out tag. (The usual response to Service In is Service Out.) As a result of the Command Out response, the Operational In and Service In latches are reset, and the Stop latch is set. When the Service In latch is reset, the End Service In signal sets the Device End latch in the status register, and the command register is cleared. With the Device End and Stop latches set, the Status Request latch becomes active; this, in turn, resets the Stop latch. The Status latch sets the Control Unit Request latch which generates the Request In

line to the channel. At the completion of a stop sequence, the channel is left in a state which will result in a control-unit-initiated status transfer of an Ending Status byte.

KEYBOARD OPERATIONS

Keyboard data and function key operations are described using flow charts and IOP diagrams provided in the FE Diagram Manual, IBM 2260 Display Station and IBM 2848 Display Control, Form Y27-2048. The operations are described on an overall basis and are provided as an aid in using the flow charts and IOP diagrams where more detail and operational timing are given.

Alphanumeric Key

- Establishes keyboard priority on the basis of address and TIC found.
- Determines whether key depressed is a data key, keyboard command, or new line.
- Selects proper buffer associated with the selected display station.
- Stores BCD information for selected character.
- Remembers character location where TIC was found.
- Stores video for selected character in the proper buffer.
- After BCD and video have been stored in delay lines, writes a new TIC in the next displayable character position and, if required, writes a destructive cursor symbol (EOM).
- Restores keyboard and reset display control, thus permitting display control to service another keyboard, printer, or the channel adapter.
- Applicable figures: FC-2 (sheets 1, 2, 3, 4) and IOP-1.

When a keyboard data key is depressed, its associated Strobe signal is routed to display control, which signifies that a display station is requesting service. If the key depressed is not the Enter or Print key, the Strobe latch for that keyboard will be set. The keyboard data is also checked to determine whether the Erase key is selected. Assuming that the Erase key is not active, a priority check is made to determine keyboard priority if two or more TIC's were detected at the same time. When priority has been established, the selected display station transfers its address to display control and all other display stations are locked out when their Strobe latches are reset. The display station address is decoded to select the proper adapter and its associated buffer. After TIC is found, its location is stored in the clock storage logic (Store row, segment, side, and column where TIC was found). Keyboard data (selected key) is then gated to the display control. If the selected key is not a command (i.e., keyboard data bit 1 set to 0), the keyboard code for the alphanumeric character is transferred to the CBR. At this point, the BCD (complemented keyboard data) for the selected character is stored in the CBR and the display adapter and buffer have been selected. The TIC Found latch is reset since counter storage contains the TIC location, and the control unit Busy latch is set, indicating that the control unit is busy.

The Set Write level is activated to prepare the 2848 to write the BCD, presently in the CBR, into the selected delay line. Write operations are initiated by writing the first BCD bit into the A delay if an even display station originated the data transfer. (Recall that odd displays write the first BCD bit into the B delay line and even displays write the first BCD bit into the A delay line.) Assume that an even display requested service (address register bit 1 equals 0); hence, the Write A latch would be set. The set condition of the Write A latch inhibits regeneration of TIC. This occurs at a ring count of 7 if the row count does not equal 6 or during odd check time if the row count equals 6. Next in sequence, the Write B latch is set and data (BCD) contained in the CBR (representing the character selected at the keyboard) is inserted alternately in the B and A delay lines. The BCD data is also retained in the CBR. During retrace time the BCD in the CBR is employed to prime the character generator to translate the BCD into video data for the selected character. Video data (V1 through V5) is read out of the character generator through the execution of five read cycles which occur during five successive retrace times. The video is stored in the delay lines and displayed on the CRT. Completion of the code translation for the selected keyboard character is indicated when the contents of the line and line storage counters are equal.

When a column compare is detected, an analysis of the command register is effected to determine whether the operation was originated by the channel (Write Command and I/O Request on) or by a keyboard. A channel-originated operation would require that the next character (if available) be transferred from the character register to the CBR. Since this analysis assumed a keyboard-originated write operation, an EOM symbol must be written into the next character position. Coincidence of Retrace Segment, Column Compare, Row 6, and Not Line 16 Search signals allows the Wrt EOM latch to be set at Ring 4 while the Wrt Char

latch is reset. On standard machines, the code for EOM and a 1 in bit position 1 (TIC) are encoded into the CBR.

Machines that contain the NDC feature require that a TIC be written in the next character position. This is accomplished by setting the Wrt TIC latch, resetting the Wrt EOM latch, and activating the Write A or B latch when the Row, Segment, Display Compare, and Not Line 16 Search signals are detected. After the TIC has been written, the end operation sequence is performed to restore the keyboard and display control in preparation for the next operation.

Machines which incorporate the destructive cursor feature require that an EOM symbol, in addition to TIC, be written into the delay lines. This is accomplished by encoding EOM and TIC into the CBR and writing the contents of the CBR into the delay lines. The BCD bits that represent the destructive cursor in the CBR are also employed to create the video (V1 - V5) bits for the EOM symbol from the character generator. When EOM has been inserted in the delay lines, an end operation sequence is performed to restore the keyboard and prepare the display control for the next operation.

New Line Key

- Establishes keyboard priority on the basis of address and TIC found.
- Writes a New Line symbol into the selected buffer.
- Writes TIC in the first character position one line down.
- Applicable figures: FC-2 (Sheets 1, 3, 5) and IOP-7.

Keyboard priority for this operation is exactly the same as previously described for an alphanumeric key. If the new line code is detected in the CBR, the New Line latch is set and the New Line symbol is written in the character position where TIC was found. During Odd Display and ring 2 time, the Line Change latch is set to permit a line change. This is accomplished by resetting row storage (ring 3 time) and permitting it to advance one count. If the row counter is stepped to a count of 6, a buffer change is required. For Model 2 and 3 machines this is accomplished by complementing the Upper/Lower Storage trigger. Because a line change is required, it is also necessary to set the Line 16 Seek latch. At this time, if the row counter does not equal 6, row storage will be set to the next row count. Once the Line 16 Seek latch is set, the New Line and Line Change latches are reset and the Wrt EOM is made active. The column and left/right Storage Counter triggers are updated to reflect the first character position on the next line. When Line 16 Search ends (line 16 detected), the EOM symbol and TIC are encoded in the CBR. When the row, segment and display compare condition is detected, TIC and EOM are written into the buffer selected by the updated contents of counter storage. The foregoing operation applies to machines which contain the destructive cursor. Machines wired with the nondestructive cursor function from the point when the Line 16 Search latch is reset, as follows.

The Write TIC latch is set and the Write EOM latch is reset. When the Line 16 latch is cleared and the row, segment, and display compare conditions are coincident, only TIC is entered into the selected buffer stipulated by the updated counter storage. After the TIC or the EOM has been written into the delay lines, and if the Cancel or Write Zero latches (NDC) are not set, the end op sequence (FC-2, Sheet 4) concludes the operation.

Up and Down Keys

- Up and down keys are active on only those machines equipped with the NDC feature.
- Move NDC up or down one row at a time.
- Operation involves finding, erasing, and storing location of TIC.
- Adjust row storage (and upper/lower storage on Model 2 or 3 machine) in accordance with up or down Command key.
- Write a new TIC using updated storage counter location.
- Applicable figures: FC-2 (Sheets 1, 6, 8, and 4), IOP-2 (Up key), and IOP-3 (Down key).

Keyboard entry into the common equipment is accomplished in the same manner as described for the alphanumeric key. When keyboard data is decoded as a command (up or down command), the respective latch for that command is set. The Wrt A or B latch is set but immediately reset one bit time later. This action causes the TIC to be erased from its original location. At this point, the up and down commands are acted upon differently, and each will be considered separately.

If a down key command were entered, row storage would be reset at odd display ring 3 time. Normally, row storage is stepped at ring 3 odd time. After row storage is reset, it is allowed to reflect the content of the row counter. If the row counter does not step to 6, the new row count is locked into row storage and the Wrt TIC latch is set. The TIC is written into

the character position one row down, and the operation is concluded by execution of an end op sequence. If the cursor is in the bottom line (lower segment and row counter equal to 6), it moves to the top line. The lateral position of the cursor remains constant. A row count of 6 also stipulates that upper/lower segment storage must be complemented (in addition to resetting the row counter) to permit TIC to be written in the first row of the opposite segment. If TIC were found in the lower segment, the line count would be preserved in storage and the Line Search latch would be set. After cycling through the retrace segment and after a line compare is detected in the upper segment, TIC is written in the first row of the upper segment. Since the line count has not changed, the lateral position of TIC has remained constant.

TIC manipulation for an up key command is basically the same as the down key command except that TIC is moved up instead of down. If the TIC position (cursor) is already in the top line when the up key is activated, it is moved to the last line. Because TIC moves up one row, it becomes necessary to subtract 1 from the row counter, but the content of the line counter is maintained in storage. The Line Search latch is set, and, when line compare is detected, the TIC is written up one row from its previous position. An end op sequence completes the operation.

When a count of 1 is subtracted from row counter storage and the result produces a count of 6 or 7, it becomes nessary to complement the upper/lower storage counter in Model 2 and 3 machines. (Model 1 machines reset row counter storage and wait for line compare.) Then row counter storage is again decremented one count at a time until row storage equals 5. When a line compare is detected during retrace segment time and row 5, the Write TIC latch is set and TIC is moved up one row. The operation is concluded by execution of an end op sequence.

Advance Key (NDC Feature)

- Advances cursor one display position with no other modification of display (NDC only).
- Finds and erases TIC and stores its location.
- Writes a new TIC one character position to the right.
- Applicable figures: FC-2 (Sheets 1, 6, 8, 3, and 4) and IOP-4.

Keyboard entry into the common equipment is accomplished in the same manner as described for the alphanumeric key. When keyboard data is decoded as a command (Advance command), the Advance latch is set. TIC is found and erased by inhibiting its regeneration. The Advance command sets the SOM Hold latch to inhibit writing into the delay lines. When the segment, row, display, and column counters compare, the Wrt TIC latch is set to force a 1 into the serializer. This writes TIC into the next displayable character position. The NDC is written automatically in the BCD character position identified by TIC. The operation is completed by execution of an end op sequence.

Advance Key (Destructive Cursor Feature)

- Causes storage of a blank in cursor position and advances cursor to next displayable position.
- Same function is performed if up or down key is depressed on machines wired with destructive cursor feature.
- Applicable figures: FC-2 (Sheets 1, 6) and IOP-4.

Start Key

- Used to display the start of message (SOM) symbol which flags the start of a message.
- Only one SOM should be displayed on the screen at any one time. A second selection of the Start key initiates a Cancel operation.
- Operation begins with determination of keyboard priority and when Start key is decoded as a command.
- Initiates SOM search to determine whether this is first or second selection of the Start key.
- If no SOM is found, writes the Start symbol in the position the cursor was in when Enter key was depressed. Advances cursor one display position.
- If a SOM is found (before TIC is detected a second time), executes a Cancel operation to erase all data between the Start symbol and position of original TIC. Erases one more character on machines wired with destructive cursor to remove cursor. Places cursor immediately to the right of SOM. If a New Line symbol is detected, erases it, performs a line change, and does not erase character(s) to the right of the New Line symbol.
- Normal operation of the cancel function requires that the cursor not be positioned to the right of a New Line symbol in the same row. If cursor is located to the right of this symbol, the following will occur:
  1. The characters to the left of a New Line symbol and the first New Line symbol are erased (cancelled); if no New Line

symbol is present, all characters in the line are erased.
2. The Start symbol is erased.
3. Erasing (cancelling) continues until the cursor is found. The cursor is kept in its original location.

- A New Line symbol immediately following the Start symbol will not be the last character on the line to be erased. It will not be recognized and therefore treated as any other character (destructive cursor only).
- If the NDC is in the same location as the Start symbol, depression of the Start key will cause the cursor to be moved to character position after the Start symbol.
- Applicable figures: FC-2 (Sheets 1, 6, 9, 2, 3, 10, and 5) and IOP-6.

The Start key is used together with the Enter key to transfer a message from the keyboard to the computer for further processing. To format the message, the operator depresses the Start key which displays the Start symbol on the CRT. The message is then typed on the keyboard and appears on the CRT following the Start symbol. The message can be formatted as required, using the New Line symbol. When the message is completed, the operator depresses the Enter key. This action locks the keyboard and Attention is set in the status register to inform the channel that a device is requesting service. In addition, as a result of the Enter key being depressed, the EOM symbol is written and the cursor is moved to the right of the Start symbol (NDC machines).

Only the TIC is moved to the character position immediately to the right of the Start symbol in the machines that employ the destructive cursor. When the channel responds with a Read command, data between the cursor and the EOM symbol is transferred to the computer (except characters in the line to the right of a New Line symbol), the Start symbol is erased, and the cursor is moved to its original location (character position occupied by the EOM symbol). If the computer programmed a Short Read MI command, the start symbol is not erased and the cursor is positioned in the character position immediately to the right of the EOM symbol. In machines where the destructive cursor is employed, the cursor is not visible until a character is typed on the keyboard. When the typed character is displayed (as a result of a Data key being depressed), the cursor appears in the next character position.

If a typing error occurred, the operator can cancel the typed message which appears on the viewing screen merely by depressing the Start key a second time before activating the Enter key. This results in a Cancel operation which erases all characters between the Start symbol and the cursor except those on the line to the right of a New Line symbol. Note, however, that the New Line symbol is erased. The overall operation of the Start key is described below, using the flow charts in the diagrams manual.

Keyboard selection is accomplished on the basis of priority, keyboard address, and TIC Found, as described for the alphanumeric key. When keyboard data is decoded as a command (Start command), its associated Command latch is set. The Wrt A or B latches are maintained in the reset state, and the SOM Search latch is set. At this time, four operations are performed simultaneously:

1. The TIC Search latch is reset.
2. A SOM search is executed. During BCD time, every character of the selected display is read out to the CBR to determine whether a Start symbol was previously written on the CRT.
3. Check for SOM decode or TIC. If a SOM is found, initiate a Cancel operation; if a TIC is found before a SOM is detected, write a Start symbol in the cursor position.
4. Counter storage is continually updated to enable recording the position of the SOM if it exists on the screen. As each character position is checked and no SOM is found, counter storage is reset and the next character position is checked.

Assume that no SOM is detected but a TIC is found. Under these conditions, the Wrt SOM latch is set, keyboard data (BCD for Start symbol) is transferred into the CBR, and the SOM Search latch is reset. Counter storage reflects the character position where TIC was found and the position where the SOM will be written. Writing of the SOM was required because the TIC was found before a SOM was detected, indicating that no SOM existed on the screen. A SOM must therefore be written into storage and displayed on the screen.

Now assume that SOM was decoded as noted in step 3 above and that the Start key was depressed. Under these conditions, the Cancel latch will be set. The next ring 1 time, together with Not Display Compare, allows the SOM Search latch to be cleared. Counter storage is now set to the character position for the Start symbol. An EOM symbol, together with TIC, is written in the next character position next to SOM on machines wired with the destructive cursor feature.

NOTE: Only TIC will be written in the character position immediately to the right of SOM in those machines wired with the nondestructive cursor feature.

On standard machines (destructive cursor), the EOM with TIC is now next to SOM and a Write Zeros is initiated to destroy the old TIC. As a result, all

characters between SOM and TIC are also erased. The Character Gate latch is turned on to allow BCD to transfer into the CBR to check for new line codes. Note, however, that if a new line code had been located immediately to the right of the SOM it would not be recognized since the EOM symbol would have replaced it.

Machines that incorporate the NDC feature make the character gate active and read the BCD to the right of SOM into the CBR where it is checked for a new line code. At the next ring 1 time, the Char Gate is reset. When a new line code is decoded, it is erased and a row change sequence is performed by making the Line Change latch active. When the Line 16 Seek latch is set, the Wrt Zero latch will not function; hence, the data to the right of where the New Line symbol appeared will not be erased. Upon completion of the row change sequence (back to line 16), the Wrt Zero latch will become active again. When the old TIC is found, an end op sequence is initiated in NDC machines. At ring 2 time, Write A or B is reset to prevent erasing valid characters. On standard machines (destructive cursor) the Cancel latch is set for the second time. This permits zeros to be written for one more character, thus destroying (erasing) the old EOM and the old TIC. When the next column compare occurs, the Cancel and Write Zero latches are reset; the end op sequence is executed to complete the operation.

Enter Key

- Establishes keyboard priority and decodes Enter key command.
- Finds SOM and writes TIC in character position immediately to the right of SOM.
- For NDC machines, writes EOM where TIC was originally found and erases TIC. Machines employing the destructive cursor find and erase the old TIC.
- Does not restore keyboard.
- Applicable figures: FC-2 (Sheets 1, 6, 9, 11, 3, and 4) and IOP-5.

Keyboard selection is accomplished on the basis of priority, keyboard address, and TIC Found, as described for the alphanumeric key. If the interface is busy, the Enter will not be honored. The interface must be in a not busy state to permit the Enter operation to continue. The Enter command is decoded and its associated latch is set. A SOM search is initiated to locate the start of message. The interface is notified that a display station is requesting service by setting Attention and transferring the display station address to the interface address register. Assume that SOM has been decoded. As a result, the SOM Hold latch is set, SOM Search is cleared, and counter storage contains the location of the SOM. A check for TIC is made when a row, segment, display, and column compare occur. If TIC were detected, it would indicate that it was positioned immediately to the right of SOM. This condition would be interpreted as a zero length message. Machines with the NDC feature would immediately insert an EOM symbol, whereas standard machines (with destructive cursor) would execute an end op sequence.

Assume that TIC was not found. In this case, the TIC Search and Write TIC latches would be set. A TIC is written to the right of SOM by activation of the Write A or B latch for one bit time. Placing TIC in the character location following SOM identifies it as the first character position which will be transferred to the local interface. It now becomes necessary to locate the old TIC and destroy it since two TIC's are presently in the delay lines. After TIC is erased, an end op sequence completes the operation.

Machines that employ the NDC feature require that Wrt A or B latches be maintained in the active state. The Wrt EOM latch is also turned on. Remember that the TIC Search latch is still set. The EOM symbol is encoded into the CBR without TIC because the TIC Search latch is on. EOM is written into the delay lines, and an end op sequence concludes the operation to reset the 2848. Because an Enter command has been processed, the Restore Keyboard operation is bypassed and the Enter key remains locked until channel responds with a Read operation to read out the displayed message.

Backspace Key

- Establishes keyboard priority on the basis of address and TIC Found.
- Decodes command and sets associated Command latch.
- Finds and erases TIC and EOM symbol.
- Writes a new TIC and EOM symbol one character to the left of where TIC was found.
- If TIC is found in line 16 (left display), it becomes necessary to change rows and write the EOM with TIC in the last character position one row above where it was found.
- If TIC is in first display position, it will be moved to the last displayable position.
- Applicable figures: FC-2 (Sheets 1, 6, 7, 3) and IOP-8.

The backspace command is initiated when the Backspace key is selected on one of the keyboards. When keyboard priority has been established, keyboard

data is decoded as a command and its associated latch is set. As a result, the Wrt A or B latch becomes active, depending on whether an odd or even display initiated the backspace operation. The Wrt Zero latch erases TIC and the BCD (destructive cursor) for the character associated with TIC. When the TIC is detected, the content of the line counter is checked. A count of 16 (left display) indicates that a row change is required; however, assume that the line count does not equal 16. The line count is then transferred to counter storage where the count is decremented by six during retrace time to reflect the display position to the left of where TIC was found. A line search is initiated to locate the character position contained in the storage counters. When a line compare occurs, an EOM, together with TIC, is encoded into the CBR and written into the delay lines. The operation is completed by execution of an end op sequence to restore the keyboard.

If the line counter contains a count of 16, both the line and row storage counters must be manipulated to reflect the last character position in the preceding row. For Model 3 machines, line counter storage is first set to 240 and then decremented by six, producing a final count of 234. This is the line count for the BCD of the last character (80th character) position in a row. For Model 1 and 2 machines, line counter storage is not preset (equals 0) but is decremented by six, resulting in a count of 250. Line 250 reflects the BCD sweep for character position 40. Similar manipulations of the row counter are required to backspace properly when the TIC is located in line 16. If row counter storage were set to zero and then decremented a count of one, its resultant would be seven. This would indicate a segment change in Model 2 and 3 machines, and upper/lower storage must be complement. Recall that TIC can only be written into the delay lines when the row counter storage equals five or less. Therefore, row counter storage must be continually decremented one count at a time until row storage equals five or less.

The backspace operation is modified in those machines which incorporate the nondestructive cursor feature, to prevent destroying the character in the position identified by TIC. This is accomplished by holding the character generator Write latch off. During retrace time, the Line Search latch is set and the Wrt Zero latch is reset. The reset condition of the Wrt Zero latch prevents activation of the Wrt A or B latch during V1 through V5 time. Therefore, the character (if present) in the cursor position will not be destroyed.

Erase Key

- Establishes keyboard priority.
- Decodes Erase command.
- Writes zeros in each buffer position for selected display, which erases the display.
- Writes a TIC and cursor symbol in the first character position of the display.
- Applicable figures: FC-2 (Sheets 1, 6, 3) and IOP-19.

The Erase operation, as its name implies, performs an erase function to delete all characters and symbols stored in the delay line buffers associated with the keyboard originating the request. After the display has been erased, the cursor is written into the first character position. When the Erase key is made active, the TIC latch is set and the Erase key simulates the TIC. It is not necessary to wait for the actual TIC since an Erase operation does not require circuit timing related to TIC. The address of the selected display is placed in the address register and the Erase latch is set.

The output of the Erase latch fires an 8-ms single-shot while counter storage is cleared (left display and upper segment selected). All buffer positions are selected, and, when display compare occurs, the Write level is made active to write zeros continually into the selected buffers until 8 ms have elapsed. Timeout of the single-shot signifies that buffers associated with the selected display have been erased. A search is then made to locate line 16. When the line is found, row storage is locked to a count of 0. Counter storage now reflects the first character position where the EOM is to be written. The TIC and EOM Write sequence is performed, followed by an end op for those machines which incorporate the destructive cursor. Machines wired with the nondestructive cursor feature force a TIC into the serializer, display the NDC, and conclude the operation with an end op sequence.

Print Key

- Establishes keyboard priority on the basis of address and TIC Found.
- Decodes Print command and sets associated latch.
- Inserts EOM in character position identified by TIC and writes TIC in upper left character position of display.
- Writes BCD into CBR for character identified by TIC.
- Converts BCD for character in CBR into tilt/rotate code for printer and transfers to PIB1.
- Character or shift code is inserted in 1053 delay line buffer.
- Tilt/rotate character codes are read from 1053 buffer to printout buffer to activate printer.

- Continues to print characters until EOM symbol is detected and printed.
- If a parity error is detected by display control, the questionable character(s) is printed and a quote symbol is inserted immediately before the EOM character (" !).
- If printer adapter detects a parity error during Readout operations, the character with bad parity is destroyed and a blank space is shown on the printed copy. A quote symbol is printed after the EOM character (! ").
- Applicable figures: FC-2 (Sheets 1, 6, 17, 4) and IOP-9.

A Print operation is initiated from the keyboard when the Print key is depressed. Keyboard priority is established on the basis of TIC Found and keyboard address, when the printer is not busy. The Print command sets its associated Command latch. An EOM symbol is written on the CRT of the display station from which the print request was made, and TIC is moved to the first character position on the screen. The first character is read from the display station buffer into the CBR so that the tilt/rotate code for the character can be extracted from the character generator. The tilt/rotate code for the character is then transferred to the PIB1 register located in the printer adapter. The printer adapter processes the character asynchronously to produce typed copy of the display. Succeeding characters are loaded on a demand basis. If the printer adapter is not ready to receive the next character (Not Printer Character Request), TIC is inserted and the end op sequence terminates the operation. The TIC is employed to identify the next character transfer when operations are resumed.

At the start of a Print command, a carrier return is performed to ensure that the carrier begins typing at the left-hand margin. Carrier returns are also performed after the EOM symbol is typed, a new line is decoded, or when the end of line on the display is detected. The resultant message typed by the printer is formatted as displayed on the CRT (except control characters).

If a parity error is detected during readout of the DS buffer, the questionable character is printed. This condition will be apparent to the operator because a quote symbol will be printed immediately before the EOM character (" !). If the 1053 adapter detects a parity error in the printout buffer, indicating that the parity error occurred in the adapter, a space is programmed for the character in error and a quote symbol is printed immediately after the EOM symbol (! "). Under this condition, the carrier return function will be performed after the quote character is printed.

INTRODUCTION

The features available for the IBM 2848 Display Control and the IBM 2260 Display Station are described in Chapter 1. The operation of these features is interwoven with the discussion of the basic (nonfeature) machine circuits. This approach was taken because the feature structure is unusually complex and because the operation of the features, with few exceptions, is so intricately related with nonfeature circuits that discussing the features as functional entities is neither practical nor desirable.

As stated in Chapter 1, this manual describes the operation of a 2848 Model 3 equipped with all available features. Since there are two distinct interface adapter feature types, a choice had to be made in respect to the interface adapter attached to the hypothetical 2848 Model 3 described. The 9011 Channel Adapter (local interface) was selected.

The operation of the remote interface adapters (9012 and 9013 Data Set Adapters) is discussed herein. Essentially, these adapters are functional entities and have a minimal effect on the circuitry of the basic 2848 (when attached to the unit in lieu of the 9011 Channel Adapter).

The operation of the data set adapter features is described by providing information under three major headings, as follows:

1. Introduction
2. Functional Units
3. Theory of Operation

REMOTE INTERFACE ADAPTER

The remote interface adapter enables the 2848 Display Control and its associated 2260 Display Stations to operate with a System/360 that is remotely located with respect to the 2848. Thus, the physical proximity of the 2848 and the host System/360 imposed by the local interface adapter is not necessary.

When the 2848 is fitted with the remote interface adapter, the 2260 - 2848 display complex communicates with the IBM System/360, in a half-duplex mode, through an IBM 2701 Data Adapter Unit and appropriate data sets. A typical remote installation is illustrated in Figure 4-1. The computer terminal of the configuration illustrated consists of IBM System/360 which includes the 2701 Data Adapter Unit (2701 DAU) and a data set. The 2701 DAU performs the functions of communicating with System/360 in the 8-bit ASCII code. The 2701 converts the ASCII-8 data to ASCII (seven bits) for subsequent transmission by the data set over the communications lines; this is the code accepted by the remote interface adapter of the 2848. The data set converts the output of the 2701 DAU into a data train that can be transmitted successfully over the communications line forming the link between System/360 and the 2260 - 2848 display complex.

At the display terminal of the configuration, a second data set reconverts the communication line signals into serial data that can be accepted and recognized by the remote interface adapter of the 2848. Note that both data sets can perform the function of either converting communications line data to serial data or converting serial data to communications line data, depending upon whether data is being written to or read from the display complex.

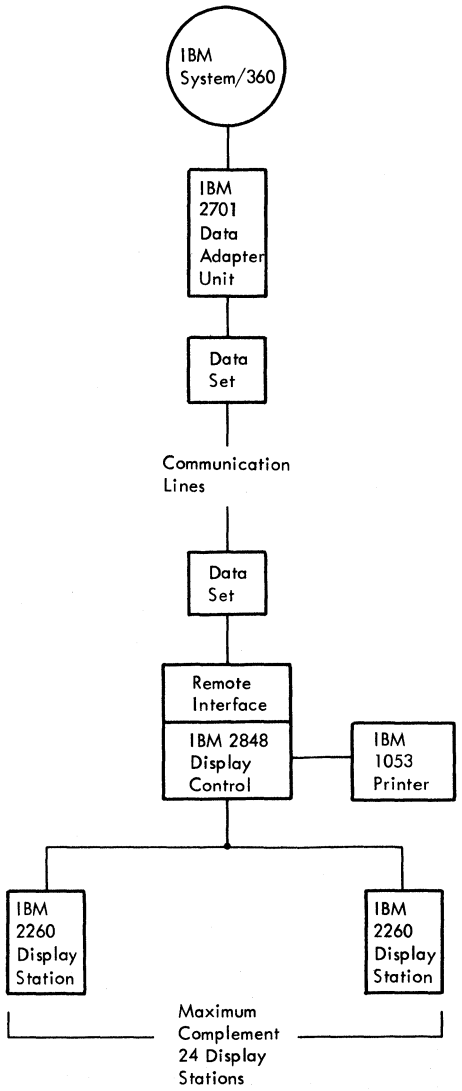


Figure 4-1. Remote Display Complex Configuration

A choice of two remote interface adapters permits data transmission at the rate of either 1200 or 2400 baud (bits per second). The two adapters, identified by their feature codes, are as follows:

1. Data Set Adapter - 9012: permits operation at 1200 baud over Common Carrier Schedule 4, type 4A, four-wire, leased private-line telephone service. Western Electric Data Set 202D (or equivalent) is used to attach a 2848 Display Control fitted with Data Set Adapter 9012 to the communication lines. Clocking is provided by the 2848.
2. Data Set Adapter - 9013: permits operation at 2400 baud over Common Carrier Schedule 4, type 4B, four-wire, leased private-line telephone service. Western Electric Data Set 201B (or equivalent) is used to attach a 2848 Display Control fitted with Data Set Adapter 9013 to the communication lines. Clocking is provided by the data set.

The operation of the remote interface adapter is discussed by first presenting all required general information concerning the adapter. Then, the operation of each logical area of the adapter is treated, with the discussion keyed to a functional block diagram of the adapter. Finally, the adapter theory of operation, which describes the relation of the adapter's functional units during read and write operations, is presented. Simplified diagrams of the read and write control logic are provided to support the theory discussion.

General

In the paragraphs that follow, the operation of the 2848 (provided with the remote interface adapter) is described with respect to the codes used, 2848 modes of operation, addressing, and commands and command operation. A description of the response sequence applicable to each valid command that can be issued is also presented. This general information provides the basic data required to read and understand paragraphs titled "Functional Units" and "Theory of Operation."

ASCII Code Set

The American Standard Code for Information Interchange (ASCII) is the basic code set used for all communication exchanges between the System/360 channel and the remote display complex (via the IBM 2701 DAU and the data set link). This code, approved by the American Standards Association (ASA), is a seven-bit code that provides 128 possible characters, of which 71 are used in data exchanges between the System/360 channel and 2848 Display Control. Since ASCII is a seven-bit code, and since all data transmitted or received over the System/360 channel must be of eight-bit structure, it is necessary to modify the ASCII code to an eight-bit structure. This modified version is called ASCII-8. Modification is accomplished by adding an x-bit between bits 5 and 6 of the ASCII code; e.g., 76x54321. The x-bit is always the same as bit 7. For example, the ASCII code for the letter A is 1000001.

ASCII-8 is used only within the channel and for data transmission between the channel and the 2701. Data transmission between the 2701 and 2848 is in ASCII. The 2701 converts ASCII-8 to ASCII for transmission to the 2848. Conversely, the 2701 converts ASCII to ASCII-8 for transmission to the channel.

The 71 ASCII characters used in data exchanges betwen the channel and the 2848 are shown in Figure 4-2. The characters are shown in ASCII-8 structure.

IBM 2701 Data Adapter Unit

The IBM 2701 Data Adapter Unit (DAU) serves as a data buffer, data converter, and synchronizer. The 2701 also provides the channel with 2848 Display Control status and sense information through the 2701 status and sense registers.

Data transferred from the channel and intended for the 2848 Display Control is received by the 2701 DAU in data bytes of ASCII-8 code structure. The 2701 converts the ASCII-8 data bytes to ASCII (seven bits) and places it in a transmit adapter (XA) register for transfer to the 2848. The 2701 transfers the seven bits of the ASCII character serially (one bit at a time) to the 2848. The seven bits are preceded by a Start bit and followed by a Vertical Redundancy Check (VRC) bit and a Stop bit. The Start, VRC, and Stop bits are developed by the 2701 and accompany the seven bits of every ASCII character transmitted to the 2848 in the order shown in Figure 4-3. The data received from the 2848 is also the same ten-bit format. All ten bits are of the same signal length and are transmitted at the speed (1200 or 2400 baud) specified by the data set adapter and data sets used. The ten-bit format which every character transmitted between the 2701 DAU and 2848 assumes is illustrated in Figure 4-3.

Data Sets

Data sets, also known as subsets or modems (a contraction of modulator), are used at each termination of the communication lines; they provide the necessary compatibility between the 2701 Data Adapter Unit, 2848 Display Control, and the communication facilities. The basic function of the data

Bits	B_7	B_6	B_X	B_5		0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1
	B_4	B_3	B_2	B_1	Col ► Row ▼	0	1	2	3	4	5	6	7
	0	0	0	0	0	Note 1 Note 2		SP	0		P	@	P
	0	0	0	1	1	SOH			1	A	Q	A	Q
	0	0	1	0	2	STX			2	B	R	B	R
	0	0	1	1	3	ETX		#	3	C	S	C	S
	0	1	0	0	4	EOT		$	4	D	T	D	T
	0	1	0	1	5		NAK	%	5	E	U	E	U
	0	1	1	0	6	ACK		&	6	F	V	F	V
	0	1	1	1	7			'	7	G	W	G	W
	1	0	0	0	8		CAN	(	8	H	X	H	X
	1	0	0	1	9			)	9	I	Y	I	Y
	1	0	1	0	10	LF		*	:	J	Z	J	Z
	1	0	1	1	11			+	;	K	Note 4	K	Note 5
	1	1	0	0	12	Note 3		,	<	L		L	¬
	1	1	0	1	13			-	=	M		M	
	1	1	1	0	14			.	>	N		N	|
	1	1	1	1	15			/	?	O	_	O	

ASCII-8 is converted to ASCII by deleting bit X.

Note 1. Displayed on 2260's as the EOM (▬) symbol. Prints on the 1053 Model 1 Printer as the exclamation mark (!).

Note 2. Displayed on 2260's as the Check (▮) symbol. Prints on the 1053 Model 4 Printer as the quote symbol (").

Note 3. Displayed on 2260's as the New Line (◢) symbol. Causes a carriage return and line feed on the 1053 Model 4 Printer.

Note 4. Displayed on 2260's as the Start MI (▶) symbol. Prints on the 1053 Model 4 Printer as a cent sign (¢).

Note 5. The codes represented by the characters within the dotted outline are the ASCII-8 codes for the lower-case alphabetic characters. These codes are converted to upper case by the 2848 and displayed as upper-case characters. If retrieved by a read operation, the codes will be in the upper-case bit configuration.

Additional Notes:

A. Graphic representations are undefined for the bit patterns outside the heavily outlined portions of the chart. These bit patterns are referred to as undefined graphic bit patterns. If an undefined graphic bit pattern is sent from channel to the device, the graphic that will be displayed or printed by the device is not specified.

B. IBM reserves the right to change at any time the graphic displayed or printed by this device for an undefined graphic bit pattern sent from channel.

Figure 4-2. ASCII-8 Code Set

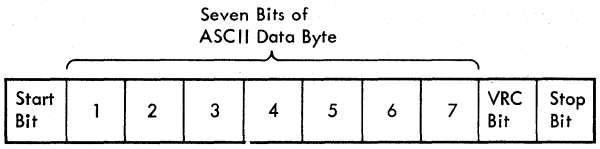


Figure 4-3. Ten-Bit Format of Transmitted ASCII Characters

sets is modulation and demodulation of 2701 and 2848 signals for data transmission.

ASCII Communication Control Characters

In multidrop applications (where more than one device is attached directly to the lines), a method of control is necessary. Line traffic between System/360 channel and the remote display system is controlled by the use of six of the ASCII communication control characters. These six codes, used singly or in sequences, perform all the control functions necessary to establish and maintain an orderly flow of traffic between the channel and 2848's attached to the communication lines.

In addition to the six ASCII communication control characters, an ASCII format effector (LF) and an ASCII control character (CAN) are used in data transmission between a remote display complex and the channel. The definition of each of these eight ASCII characters is given below. The code structure for each is given in Figure 4-2. For a detailed description of each (when it is used, its significance, and its interpretation), see Summary of Sequences and Responses.

1. STX (Start of Text) - A communication control character which precedes a sequence of characters that is to be treated as an entity. This entity is usually terminated by ETX.
2. ETX (End of Text) - A communication control character used to terminate a sequence of characters started with STX and transmitted as an entity.
3. CAN (Cancel) - A control character used to indicate that the data with which it is sent is in error. The CAN control character is transmitted, following text and before ETX, if a buffer parity error is detected by the 2848 Display Control during transmission. CAN is transmitted only by the 2848.
4. ACK (Acknowledge) - A communication control character transmitted by a receiver as an affirmative response to a sender.
5. NAK (Negative Acknowledge) - A communication control character transmitted by a receiver as a negative response to the sender.
6. SOH (Start of Heading) - A communication control character used at the beginning of a sequence of characters which constitute a machine-sensible address.
7. EOT (End of Transmission) - A communication control character used to indicate the conclusion of a transmission which may have contained one or more texts and any associated heading (addresses). EOT is also used, instead of SOH, as the first byte of the addressing sequences in the specific poll, general poll, and read operations.
8. LF (Line Feed) - The LF is a format effector and should be included only as part of text (message). The LF character causes the New Line symbol to be displayed and the cursor of the selected 2260 Display Station to move to the first display position in the next display line. If the cursor is in the bottom line, it will be caused to move to the first display position of the top line. If more than six consecutive LF's are sent to a selected 2260, loss of data may result. The LF character received by the channel from the 2848 Display Control indicates that the following data byte is the first character of the next 2260 display line.

2848 Display Control Modes of Operation

A remote 2848 Display Control operates in two modes. These modes, Control and Text, are described below.

Control Mode

Control mode is the mode in which the 2848 Display Control is placed preparatory to receiving an addressing sequence or control data. The 2848 enters Control mode, while in selected or nonselected status, upon receipt of transmission of an SOH, EOT, or ETX control character. Receipt of an STX control character by a 2848 in selected status switches that 2848 from Control mode to Text mode.

Text Mode

Text mode is the mode in which a 2848 Display Control is placed while it is receiving or transmitting text data. The 2848 enters Text mode, while in selected status only, upon receipt of transmission of an STX control character. Receipt of an ETX, EOT, or SOH control character switches the 2848 from Text mode to Control mode.

In a multi-drop application only one 2848 can be in Text mode at a given time.

2848 Display Control Status

At a given time, a 2848 may be in Transmit status, Selected status, Nonselected status, Receive status, or certain combinations of these.

Transmit Status

A 2848 Display Control directed by a 2701 to transmit other than ACK, NAK, or EOT is considered to be in Transmit status. To attain Transmit status, the 2848 must also be in Selected status.

Selected Status

A 2848 Display Control directed by a 2701 to receive or transmit data other than an addressing sequence or control data is in Selected status. In a multidrop application only one 2848 can be in Selected status at a given time. A 2848 in Selected status can also be in receive or transmit status.

Nonselected Status

A 2848 Display Control not indicated by an addressing sequence is in Nonselected status. A 2848 Display Control in Nonselected status can also be in Receive status.

Receive Status

A 2848 Display Control that is not in Transmit status is in Receive status. A 2848 in Receive status may also be in Nonselected or Selected status.

Addressing Sequence

Each command issued by the channel to the remote display complex is transmitted to the 2848 Display Control in four sequential bytes of a definite format called an addressing sequence. The addressing sequence prepares the 2848 and the 2260 or the 1053 Printer and specifies the operation to be performed.

The addressing sequences for each command are described under Summary of Sequences and Responses.

The following describes the specific function of each of the four bytes of the addressing sequences:

1. First Byte - The first byte of an addressing sequence must be either an SOH or an EOT communication control character. The SOH or EOT communication control character places the 2848 Display Control in Control mode, Nonselected status.
2. Second Byte - The second byte in the addressing sequence contains the address of the 2848. Any configurations of the ASCII-8 code, except configurations in which bit positions 6 and 7 are zero, may be assigned the 2848. This structure provides 96 possible addresses, any one of which may be assigned as the address of a 2848.
3. Third Byte - The third byte contains the address of the device (2260 Display Station or 1053 Printer) to be selected. Device addresses are assigned in consecutive order, starting at 10100000 or 01000000, with the 1053 Printer occupying the highest order position. Figure 4-4 illustrates address assignments for 24 2260 Display Stations and a 1053 Printer (the maximum number of devices that can be attached to a 2848 Display Control Model 1). Note that bit position 6 or 7 is a 1 bit. This is necessary to prevent a 2260 or 1053 Printer address from being interpreted as an ASCII communication control character.
4. Fourth Byte - The fourth byte of an addressing sequence specifies the command to be executed by the selected 2848 Display Control and 2260 Display Station or 1053 Printer.

Each of the four bytes of every addressing sequence is parity-checked by the 2848 as it is received. The address bytes are also checked for address validity, and the command byte is checked for command validity.

To maintain operational continuity, the 2848 must respond to an addressing sequence within 2 seconds after the addressing sequence is transmitted to the 2848. Failure to respond (no response) results in a

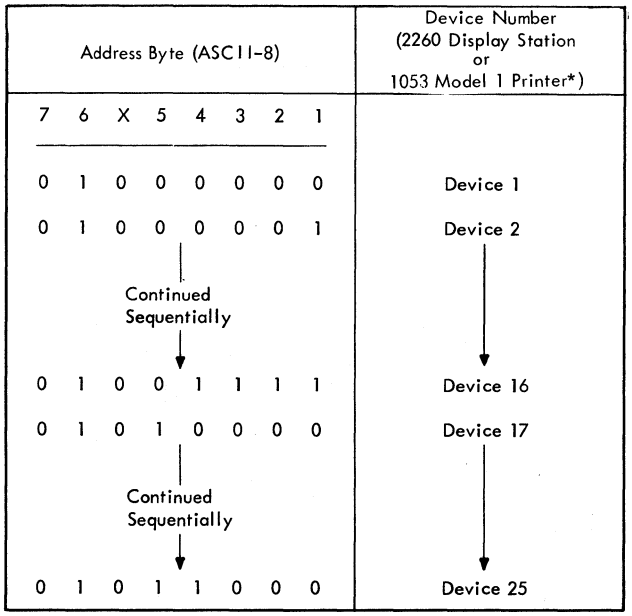


Figure 4-4. Typical Remote Device Address Assignments

2701 line timeout condition. (See 2701 Line Time Out. Also see description of No Response under Summary of Sequences and Responses.)

The 2848 response to an addressing sequence depends on the nature of the command and on conditions at the 2848 and selected device. The various 2848 responses to an addressing sequence are described in Summary of Sequences and Responses.

Commands and Command Operation

The remote display system equipped with keyboards, line-addressing, and printer features can execute eight commands. These commands, their ASCII-8 bit structure, and the feature required (if any) to enable command execution are given in Figure 4-5.

The operation of each command is controlled and monitored by exchanges, between the channel and the 2848 Display Control, of a single ASCII communication control character or a sequence of characters of which one (or more) is an ASCII communication control character. These exchanges are called sequences and responses.

The sequences and responses that occur during an operation depend upon the command, upon conditions at the display complex, and upon the program. The sequence/response diagrams (Figures 4-6 through 4-13) illustrate the possible sequences and responses that may occur during each operation. Each figure is divided vertically by a broken line. The sequence and responses to the left of the line represent those that may be transmitted by the channel to the 2848. The sequence and responses to the right of the line represent those that may be transmitted by the 2848. The heavy lines depict the sequences and responses that normally occur during each operation; the lighter line indicates other possible responses and sequences. For example, in the Specific Poll operation (Figure 4-6), the addressing sequence is initiated, and the 2848 responds with a transmission sequence (STX, device address, text, ETX, and LRC). Upon receipt of the transmission sequence, the channel responds with ACK, indicating correct receipt of the transmission sequence. The 2848 responds to ACK with EOT, and the operation is concluded. As determined by the program, the channel, instead of responding to the transmission sequence with ACK, could respond with one of the following:

NAK
SOH
EOT
STX, EOT
STX, Text, ETX, LRC

The function and operation of each command is described in the following paragraphs. Included are descriptions of sequences and responses that normally occur (as shown in Figures 4-6 through 4-13) and descriptions that are necessary to explain each operation. All sequences and responses are described under Summary of Sequences and Responses.

Specific Poll to a 2260 Display Station

The Specific Poll, when directed to the 2260 Display Station (Figure 4-6), tests for the presence of a

Command	ASCII-8 Code Structure	Feature Required
	7 6 X 5 4 3 2 1	
Specific Poll - 2260	0 1 0 0 0 0 0 0	Keyboard Feature
Specific Poll - Printer	0 1 0 0 0 0 0 0	Printer Feature
General Poll*	0 1 0 0 0 0 0 0	Keyboard Feature or Printer Feature
Read Addressed Full DS Buffer	0 1 0 1 0 0 0 0	
Write 2260	1 0 1 0 0 0 0 0	
Write Printer	1 0 1 0 0 0 0 0	Printer Feature
Line Address Write	1 0 1 1 0 0 0 0	Line Addressing Feature
Erase/Write	1 1 1 0 0 0 0 0	

* The General Poll is identified by the third character of the addressing sequence (Device Address). An all ones code for this character and the indicated Command Code signifies the General Poll.

Figure 4-5. 2848-2260 Commands (Remote)

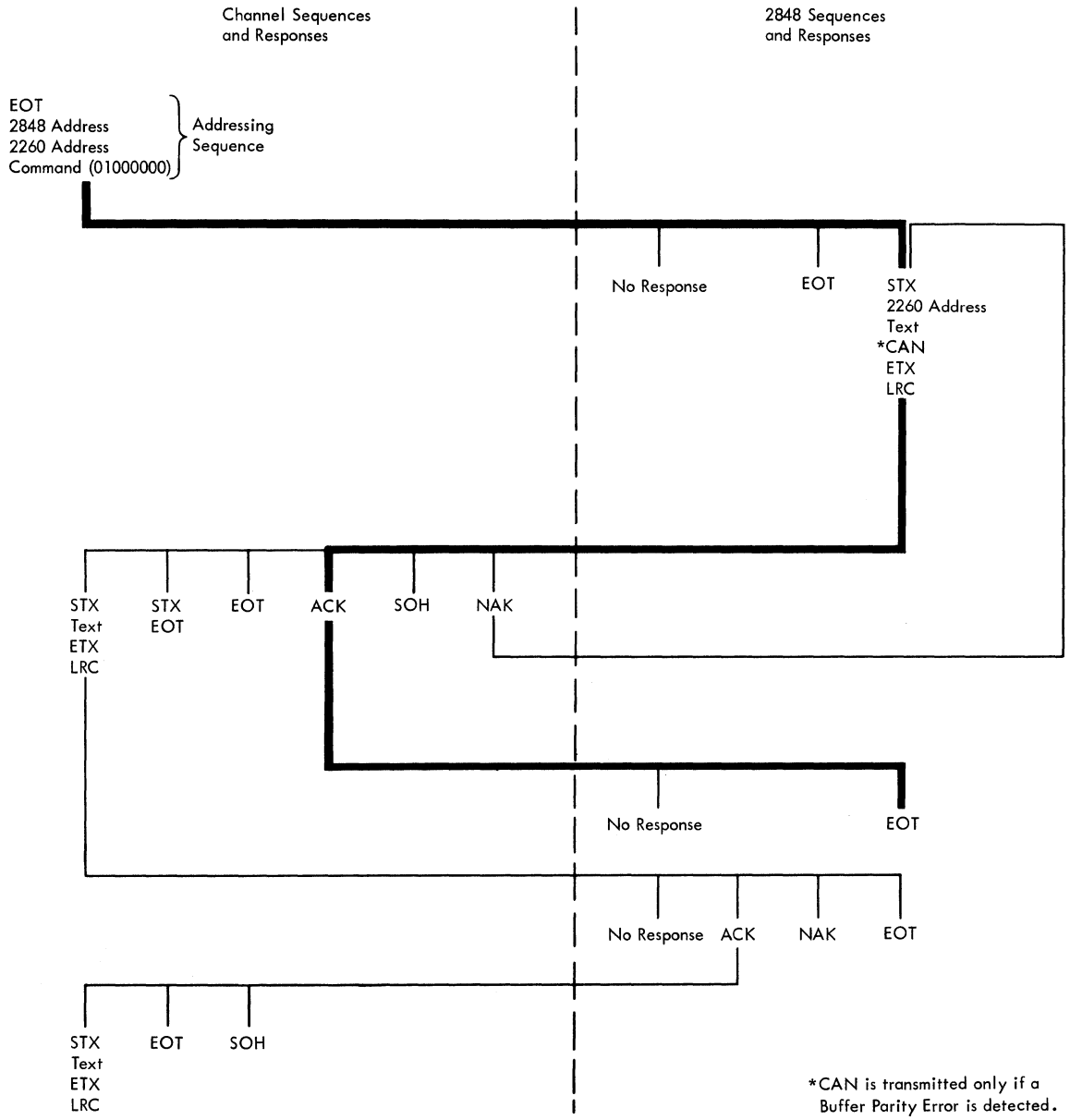


Figure 4-6. Sequence/Response Diagram - Specific Poll to 2260 DS

manually entered message awaiting transfer to the channel. If a message is pending, the Specific Poll command causes the message to be transferred to the channel.

The Specific Poll command to a 2260 causes the 2848 to test for the following conditions at the selected 2260:

1. Enter key depressed.
2. Start symbol displayed.

If both conditions are present, the 2848 transmits the STX line control character, the address of the selected 2260, and all the character data displayed between the start symbol and the cursor; however, it does not transmit data between an NL symbol and the end of the display line containing the symbol. The message data is followed by the ETX line control character and an LRC byte. The CAN character is transmitted following the text and prior to ETX only if a buffer parity error is detected during the transmission. If a start symbol is not present on the display, the STX is followed by device address, 0-length message, ETX, and LRC.

Upon receipt of the transmission sequence, the channel responds with ACK, indicating to the 2848 that the message was received correctly. The ACK response causes the start symbol to be erased from

the screen of the selected 2260 and the keyboard to be restored. The 2848 responds to ACK with EOT, and the operation is concluded. The channel may also respond with STX-Text, restoring the keyboard and placing the remote interface in a Write mode.

The 2848 will respond to the Specific Poll addressing sequence with EOT if the Enter key of the selected 2260 has not been depressed.

All responses that can occur during a Specific Poll to a 2260 operation are shown in Figure 4-6. Each is explained under Summary of Sequences and Responses.

Specific Poll to the 1053 Printer

The Specific Poll sequence (Figure 4-7), when directed to a 1053 Printer, causes the 2848 Display Control to test the Readiness and Busy status of the printer and to respond accordingly.

Three 2848 responses to the Specific Poll sequence provide the channel with the Busy and Ready status of the printer:

1. NAK - The NAK response from the 2848 indicates that the printer is not ready. The 2848, upon responding with NAK, also sets

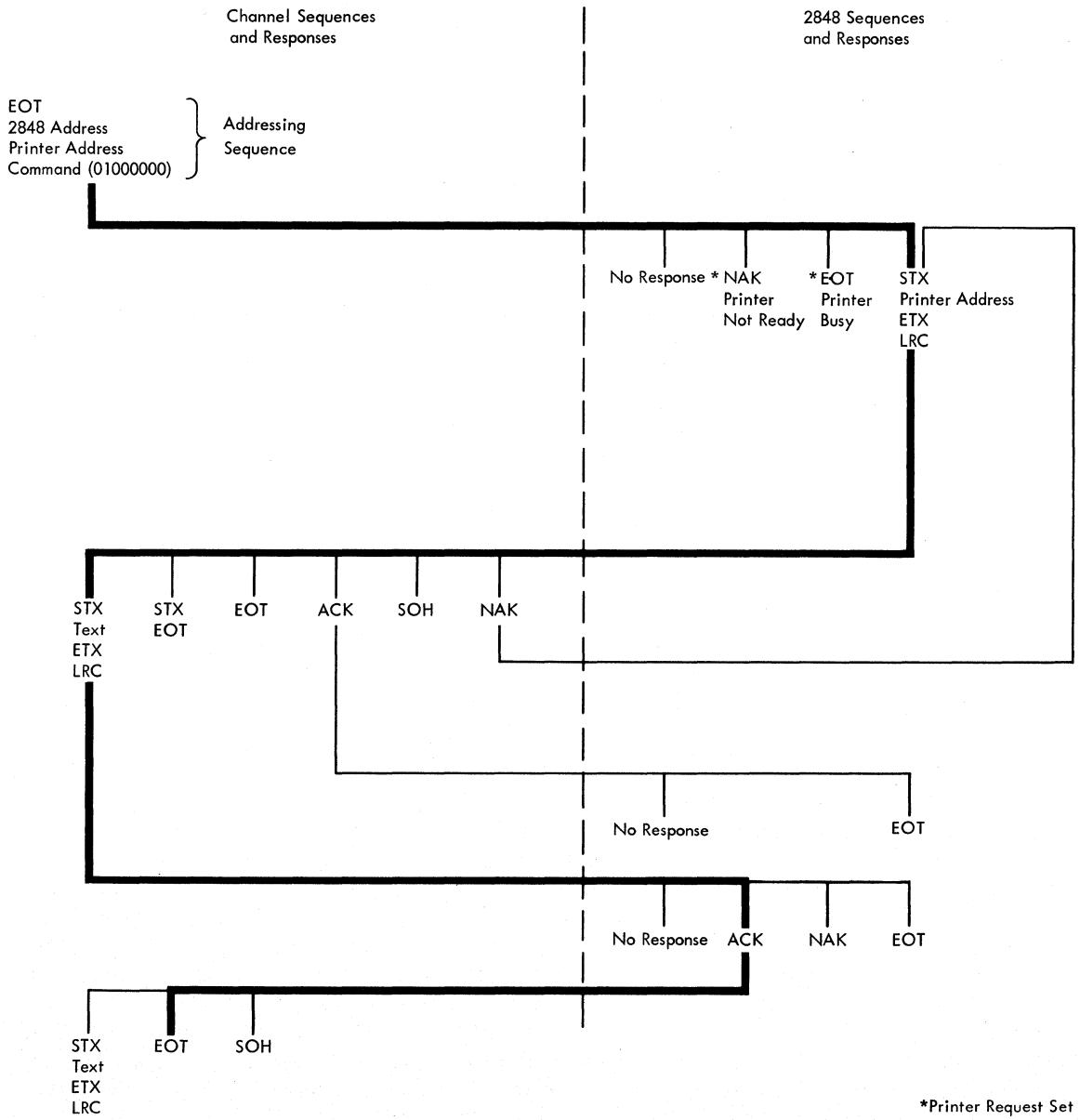


Figure 4-7. Sequence/Response Diagram - Specific Poll to Printer

Printer Request (described under Printer Request Condition).

2. EOT - The EOT response from the 2848 indicates that the printer is busy. The 2848, upon responding with EOT, also sets Printer Request (described under Printer Request Condition).

3. STX Printer Address, ETX, LRC Byte - This sequence response from the 2848 indicates to the channel that the printer is ready and free to accept a message. Subsequent action is determined by the program. Normal channel response will be an STX communication control character, the message (text) to be printed, an ETX communication control character, and the LRC byte. This response (and all other possible responses) is shown in Figure 4-8 and explained under Summary of Sequences and Responses.

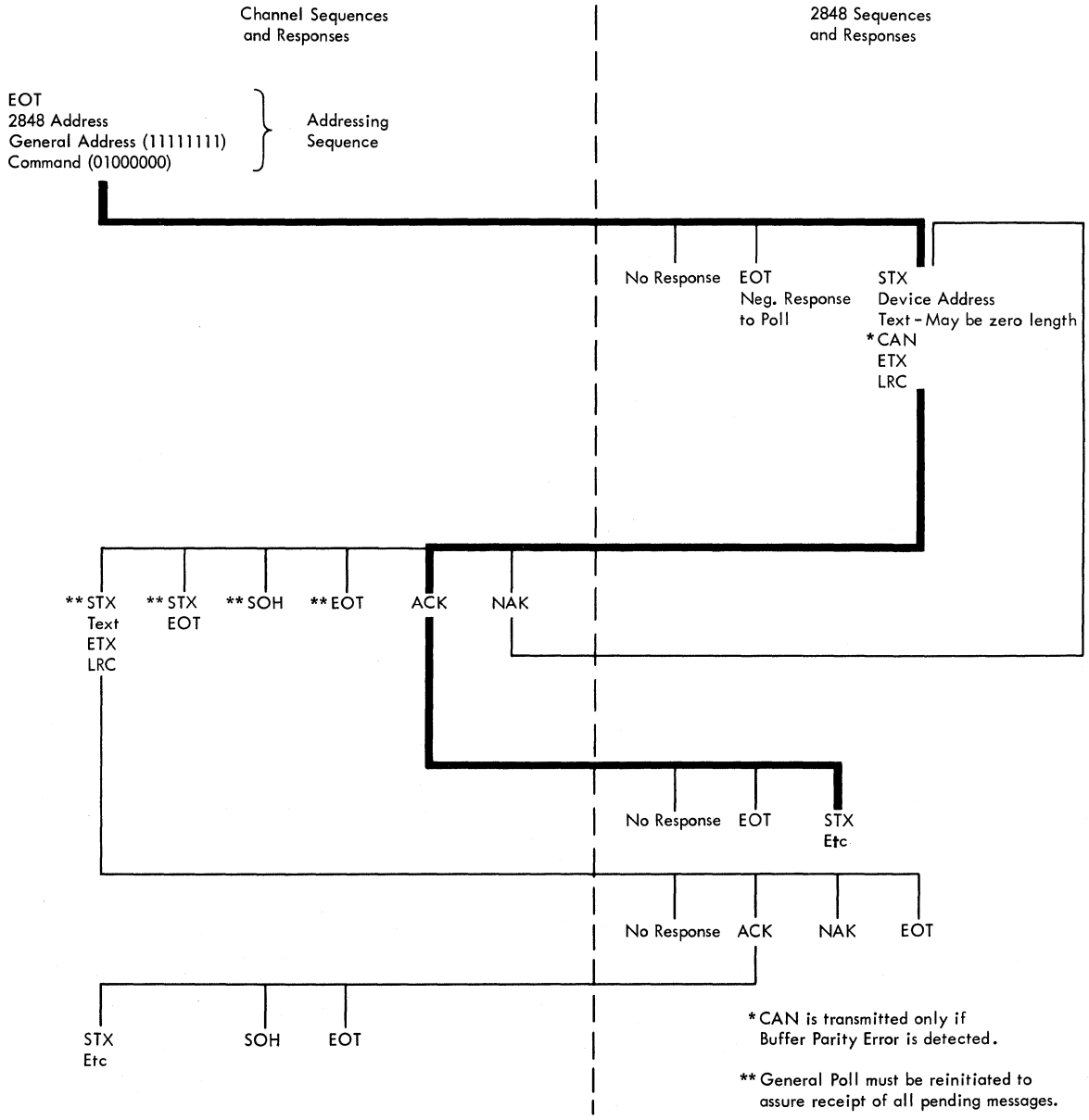


Figure 4-8. Sequence/Response Diagram - General Poll

General Poll

The General Poll command (Figure 4-8) causes the 2848 to test each 2260 Display Station for the presence of a manually entered message pending transfer to the channel. If one or more messages are present and all requirements are met (start symbol displayed and Enter key depressed), the message or messages are transferred to the channel. Each message is accompanied by the address of the 2260 from which it originated.

If the printer feature is installed, the General Poll also determines Printer Request status. Printer Request is set as a result of a previous attempt to select the printer while it was busy or not ready (see Printer Request Condition).

Upon receipt of the General Poll sequence, the 2848 first tests the Printer Request condition. If Printer Request is not set, polling of the 2260's is performed.

The 2848 tests the Enter key circuit of each attached 2260. Upon detection of a depressed Enter key and of the presence of a start symbol on the screen of the 2260, the 2848 responds with the following transmission sequence:

STX
2260 DS Address
Text (message between start symbol and EOM symbol)
ETX
LRC byte

The text will contain all the character data (except data on the same line as, and to the right of, a New Line code) displayed between the start symbol and the EOM. The CAN character is transmitted following the text and prior to ETX if a buffer parity error is detected by the 2848 during the transmission.

Upon completion of the message transfer, the channel responds with ACK, and the General Poll continues until all 2260's have been polled and pending messages have been transferred . When this occurs, the 2848 responds with EOT, indicating that no further messages are awaiting transfer, and the operation is concluded.

The following describes the General Poll operation as it occurs when the Printer Request condition is set: The 2848, upon receipt of the General Poll, first tests the Printer Request condition. If Printer Request is busy or not ready, the 2848 continues the General Poll as described in the preceding paragraphs. If the printer is ready and not busy, the 2848 responds with the following sequence:

STX
Printer Address
ETX
LRC byte

Receipt of this sequence indicates to the channel that the printer is ready and free to receive a message. Normal channel response to this sequence will be the following transmission sequence to the 2848 containing the message to be printed:

STX
Text (message to be printed)
ETX
LRC byte

Upon completion of the Printer operation, the 2848 responds with ACK. At this time, the channel may transmit another message to the printer, or it may terminate the operation. In any case, the General Poll is terminated by the STX line control character that precedes the message to be printed. To poll the 2260's, the General Poll must be reinitiated.

NOTE: If the channel responds with STX, EOT, or SOH at any time during the General Poll operation, the General Poll is terminated; however, generation of an SOH or EOT alone does not free the keyboard. To do so, these responses must be followed by an ACK or STX.

Read Addressed Full DS Buffer

The Read Addressed Full DS Buffer command (Figure 4-9) causes all character data stored in the buffer of the selected 2260 Display Station to be transferred to the channel in the following sequences:

STX
Address of the selected 2260 DS
Text (all character data displayed except nondestructive cursor)
ETX
LRC byte

Data is transferred starting at the upper-left corner of the screen and ending at the lower-right corner.

Included among the characters transferred, if they are displayed, are the check symbol, the start symbol, and the destructive cursor (EOM symbol). The nondestructive cursor is not transferred.

The normal channel response to receipt of the transmission sequence will be STX/EOT, indicating to the 2848 that the message sequence was received correctly. The STX/EOT response received by the 2848 causes the cursor to be placed in the first displayable position (upper-left corner) of the screen and the operation is terminated.

If an error is detected by the 2848 during transmission of the message from the selected 2260 to the channel, the 2848 transmits the CAN control character following the text. The sequence is as follows:

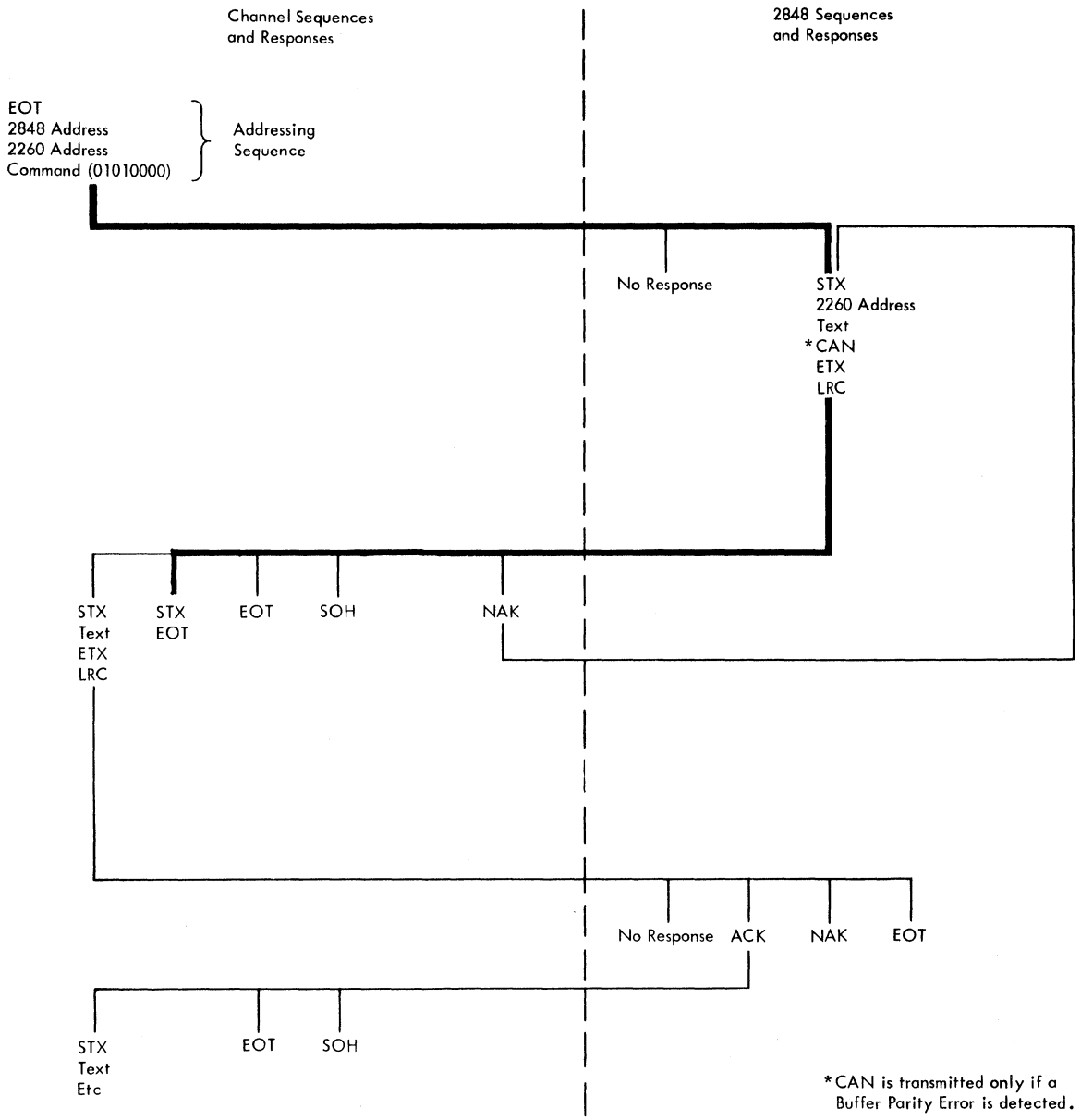


Figure 4-9. Sequence/Response Diagram - Read Addressed Full DS Buffer

STX
2260 DS address
Text (message)
CAN - indicates detection of an error by the 2848.
ETX
LRC byte

The CAN control character indicates to the channel that a buffer parity error has been detected by the 2848 in the preceding message. (Note that the character in error is assigned correct parity by the 2848 before it is transmitted to the channel.) Subsequent channel response to the CAN control character is determined by the program.

If an error is detected (by the channel) in the message as it is being received, a NAK response from the channel causes the 2848 to retransmit the message.

NOTE: Following a Read Addressed Full DS Buffer operation, the next character entered in the buffer of the selected 2260 causes a second cursor (EOM) symbol to appear on the 2260 screen. (This does not occur if the 2848 is equipped with the nondestructive cursor feature.)

Write Addressed DS

The Write Addressed DS command is used to transfer data from the channel for presentation on the screen of the selected 2260 Display Station.

Upon receipt of the Write Addressed DS addressing sequence, the 2848 Display Control responds with ACK (Figure 4-10). The ACK response indicates that the 2848 and addressed 2260 are selected and ready to receive the message. Upon receiving the ACK response, the normal channel response is the following transmission sequence containing the message to be written on the screen of the selected 2260:

STX
Text (message to be written)
ETX
LRC byte

The 2848 receives the character data contained in the message in bit-serial form (ten bits for every character). (See Figure 4-3.) The 2848 assembles the seven ASCII bits that form a character. The Start and Stop bits perform control functions; the VRC bits are used for error checking only. These bits are not assembled as part of the ASCII character.

The assembled ASCII characters are parity-checked, converted to video data, and placed in the buffer of the selected 2260 at the location indicated by the cursor. Upon entering buffer storage, the character is displayed on the screen of the selected 2260. The cursor advances to the next displayable

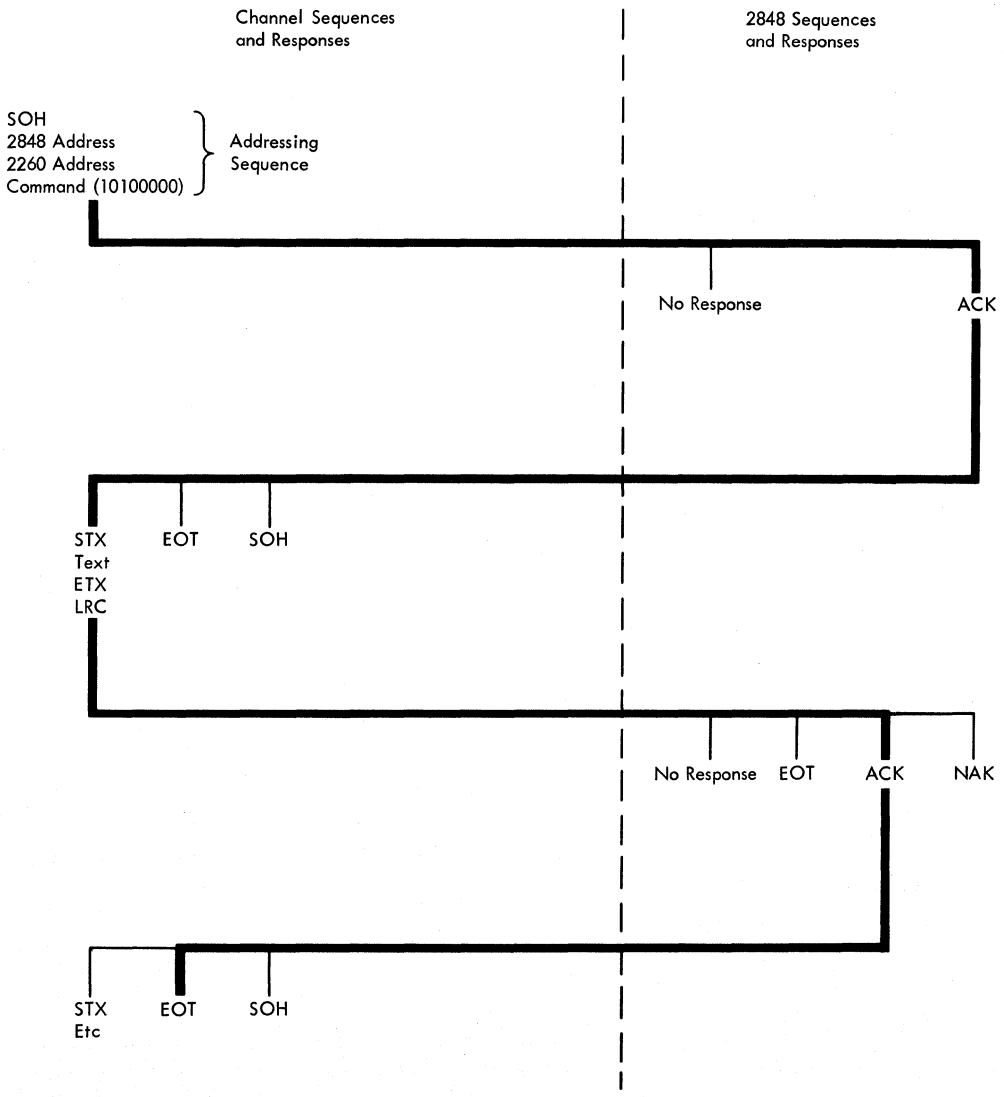


Figure 4-10. Sequence/Response Diagram - Write Addressed DS

position as character data is placed in buffer storage and displayed on the screen.

If a parity error is detected by the 2848 during the transmission sequence, a check symbol is displayed in place of the character in error.

Upon receipt of the ETX line control character, indicating the end of text, and upon receipt of the LRC byte, the 2848 performs an LRC accumulation check by comparing the LRC byte with the accumulated LRC. If the LRC byte agrees with the accumulated LRC, and if no parity errors were detected during the operation, the 2848 responds with ACK. The ACK response indicates to the channel that the message was received correctly. Subsequent channel response is determined by the program (Figure 4-19).

The NAK line control character is transmitted by the 2848, in response to the transmission sequence, if one or both of the following conditions occur during the Write operation:

1. A parity error is detected by the 2848 during receipt of the message (also indicated at the 2260 by a check symbol being displayed in place of the character in error).
2. A disparity exists between the LRC byte and the accumulated LRC.

The NAK response indicates to the channel that an error was detected during the operation. Subsequent action is determined by the program.

Erase/Write Addressed DS

The Erase/Write command sequence is essentially an Erase command combined with a Write sequence.

The Erase/Write command causes the 2848 Display Control to erase the message displayed on the screen of the selected 2260 Display Station and causes the cursor to be positioned in the first displayable position (upper-left corner of the screen). Thus, it is ensured that the message following the addressing sequence will be written on the screen of the selected 2260, beginning at the first displayable position.

Normal 2848 response to the Erase/Write addressing sequence is ACK. The ACK line control character indicates to the channel that the screen of the selected 2260 is erased and that the cursor is in the first displayable position. Channel response to ACK may be an EOT or an SOH (either terminates the operation), or it may be the transmission of a message beginning with STX (Figure 4-11). The sequences and responses that occur during the Write portion of the operation are the same as those described in the Write Addressed DS Buffer Storage operation.

The erase function is only performed following the addressing sequence containing the Erase/Write command (SOH, 2848 Display Control address, etc.). Subsequent erasures require reinitiating the addressing sequence.

Write Printer

The Write Printer command is used to transfer data from the channel to the 1053 Printer buffer.

The Write Printer addressing sequence (Figure 4-12) causes the 2848 Display Control to test the Ready and Busy status of the 1053 Printer. If the printer is operational and not being used, the 2848 responds with ACK. In response to ACK, the following transmission sequence containing the message to be printed is transmitted by the channel:

STX
Text (message to be printed)
ETX
LRC byte

The 2848 receives the character data of the message in bit-serial form (ten bits for every character; Figure 4-3) and assembles the seven ASCII bits that form a character. The Start and Stop bits perform control functions and are not part of the character.

The assembled ASCII characters are parity-checked, converted to the tilt-and-rotate code used by the 1053 Printer, and placed in the printer buffer along with the required shift characters. The printer begins printing upon receipt of the first character in the 1053 Printer buffer storage.

Upon receipt of the ETX line control character (indicating the end of text) and the LRC byte, the 2848 performs the LRC accumulation check by comparing the LRC byte with the accumulated LRC. If the LRC byte agrees with the accumulated LRC, the 2848 responds with ACK. The ACK response from the 2848 indicates to the channel that the message was received correctly.

An EOM code should be transmitted as the last character of each complete message to ensure separation of messages. The EOM code causes an exclamation mark to be printed and causes the print mechanism to be advanced to the first print position of the next line. A New Line (NL) code should be used as the first character of a message when additional separation between messages is desired. The NL code also causes the print mechanism to be advanced to the first print position of the next line. However, unlike the EOM code, the NL code does not cause a character to be printed.

During transmission of the message, if the 2848 detects a parity error or if the printer storage capacity is exceeded, the following occurs:

1. The 2848 causes the printer to print a quote (") symbol. The quote symbol is the last character printed and indicates an incomplete message.

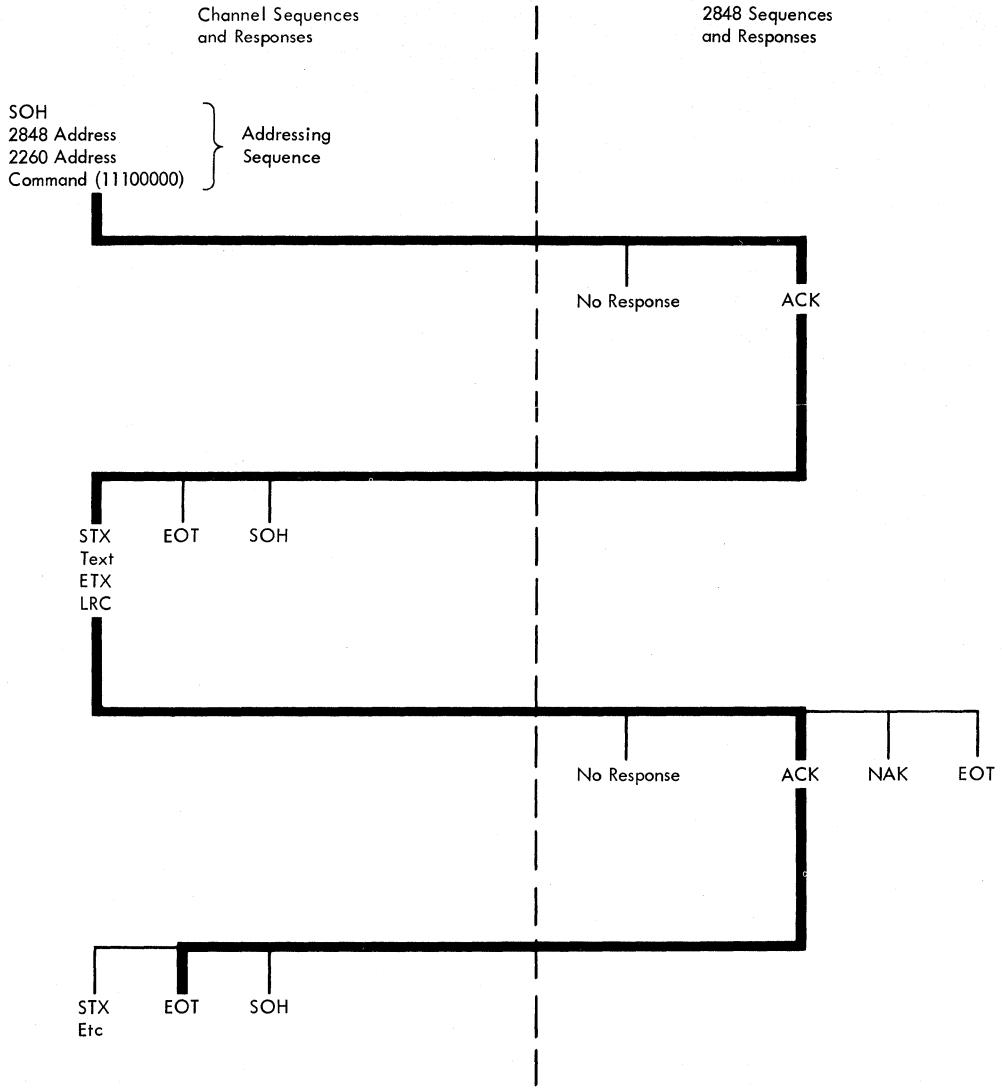


Figure 4-11. Sequence/Response Diagram - Erase/Write

2. Printing is discontinued, the type head is restored to the first print position, and the printer spaces to a new line.
3. The 1053 Printer buffer is cleared.
4. Data continues to be transferred until the end of the message (ETX); however, the data is not placed in the 1053 Printer buffer.
5. Upon receipt of the ETX and the LRC byte, the 2848 responds with the EOT line control character, indicating to the channel that a parity error has been detected in the message or that a buffer overrun condition has occurred. Channel response to the EOT line control character is determined by the program error routine.

NOTE: The 1053 Printer buffer storage accepts characters up to its capacity of 1223, including control and shift characters. When printer buffer storage capacity is exceeded (buffer overrun), the print operation is terminated immediately.

Printer Request Condition

The Printer Request condition is a means of indicating to the 2848 Display Control that the channel has a message for transmission to the 1053 Printer. Printer Request is set as a result of an attempt (by channel) to use the printer while it is busy or not ready (out of paper or power off).

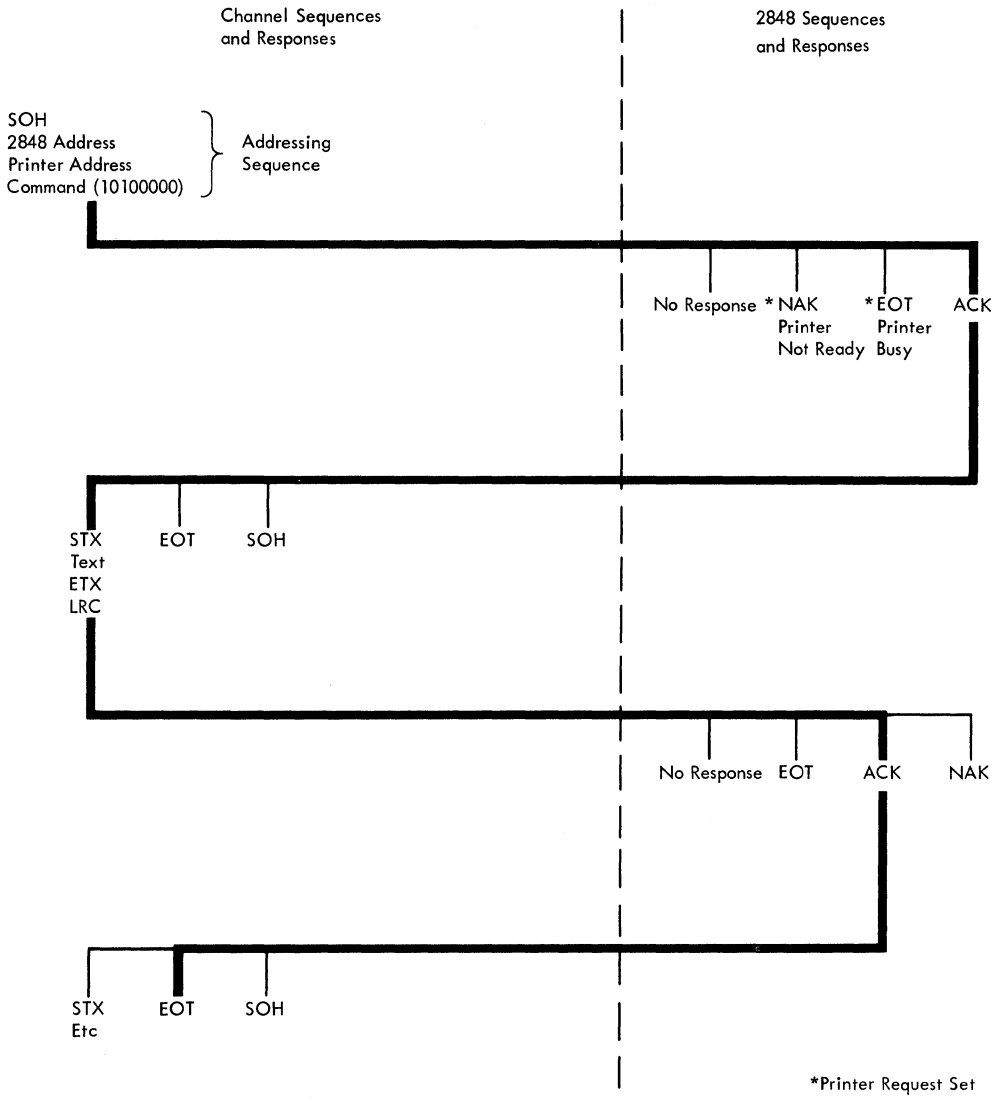


Figure 4-12. Sequence/Response Diagram - Write Printer

The Printer Request condition is set by an NAK or EOT response from the 2848 to a Specific Poll or Write Printer sequence.

The Printer Request condition causes the 2848, upon receipt of a General Poll sequence, to test the printer Ready and Busy status. If the printer is ready and not busy, the first transmission sequence to the channel in response to the General Poll is the following:

STX
Printer address
ETX
LRC byte

This sequence indicates to the channel that the printer is ready and free to receive a message.

The 2848, upon transmitting this sequence, prevents the transfer of messages from the 2260 Display Station to the printer until the channel replies to the Printer Available sequence. The next successfully completed addressing sequence to the 2848 following the Printer Available sequence cancels Printer Request.

If the printer is still not ready or is still busy when the General Poll sequence causes the 2848 to test the printer status, the Printer Request condition is unchanged.

Write DS Line Address

To accept and execute the Write DS Line Address command, the 2848 Display Control must be equipped with the line addressing feature.

The Write DS Line Address command combines the Write Buffer Storage command with line selection capabilities, thus enabling the selection of a particular line on the display as the beginning line of a message.

The Write DS Line Address command causes the cursor of the selected 2260 Display Station to be positioned in the first displayable position of the specified line. The line address is specified by the first character following the STX line control character (Figure 4-13). Subsequent message data (text) is displayed beginning at the line indicated by the cursor.

The Write DS Line Address command provides for the selection of up to 12 line addresses (the maximum number of display lines on 2260's attached to a 2848 Display Control Model 2 or Model 3). Note that 2260's attached to a Model 1 2848 display only six lines. Therefore, line addresses numbering more than six should not be used in a display complex controller by a 2848 Display Control Model 1.

Except for the command sequence and the positioning of the cursor, the Write DS Line Address command operates the same as the Write DS Buffer Storage command. All sequences and responses, other than those specified above, apply to the Write DS Line Address operation.

Figure 4-14 lists the 12 possible line addresses and the ASCII-8 bit format for each.

Summary of Sequence and Responses

The sequences and responses that occur between the channel and the 2848 Display Control comprise seven of the eight ASCII control characters. These characters, used singly or in sequences, facilitate or are directly responsible for the following:

1. Perform line control functions.
2. Maintain operational continuity.
3. Provide the channel with the current status of an operation or a specific device.

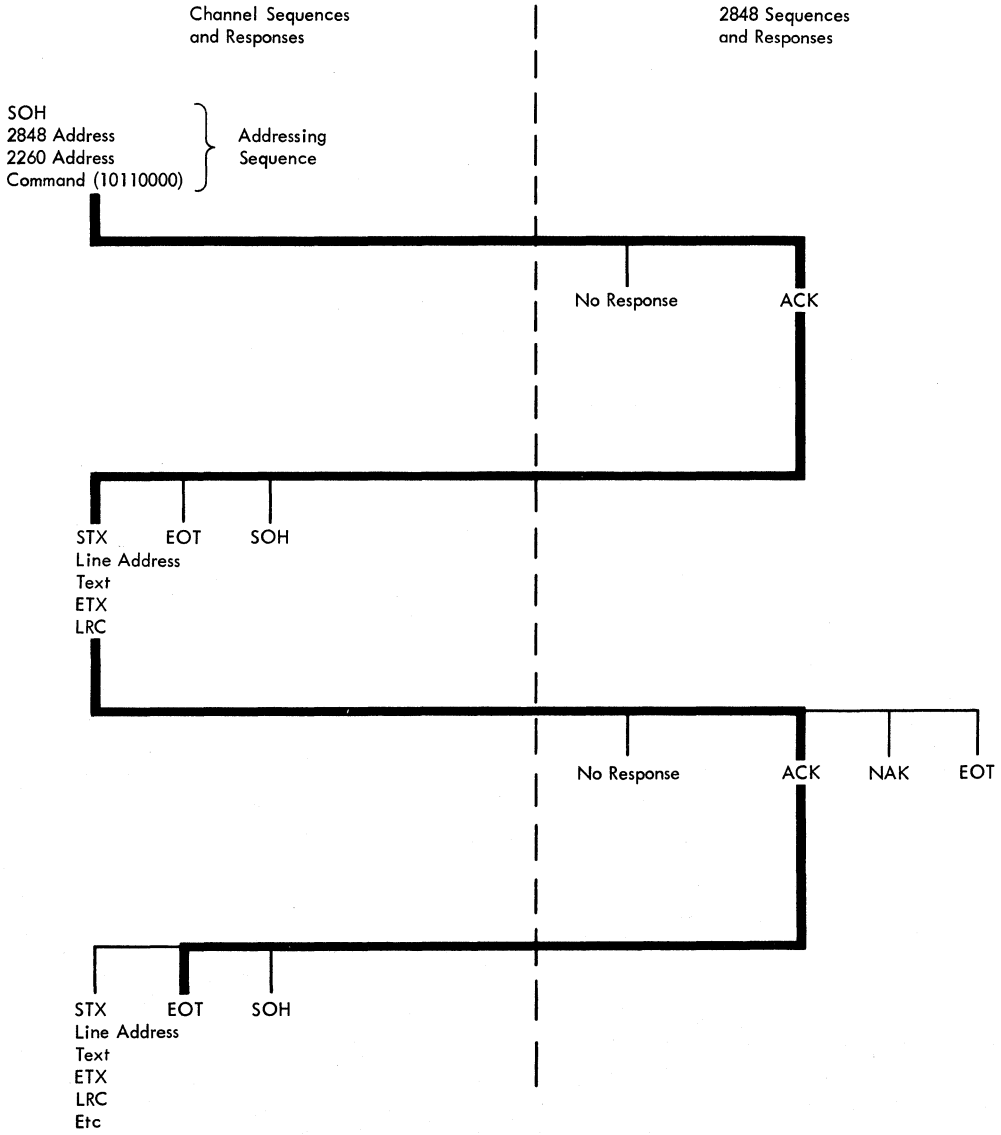


Figure 4-13. Sequence/Response Diagram - Line Address Write

ASCII-8 Data Byte Format								Selected Line
Bits								
7	6	X	5	4	3	2	1	
0	1	0	1	0	0	0	0	One
0	1	0	1	0	0	0	1	Two
0	1	0	1	0	0	1	0	Three
0	1	0	1	0	0	1	1	Four
0	1	0	1	0	1	0	0	Five
0	1	0	1	0	1	0	1	Six
0	1	0	1	0	1	1	0	Seven
0	1	0	1	0	1	1	1	Eight
0	1	0	1	1	0	0	0	Nine
0	1	0	1	1	0	0	1	Ten
0	1	0	1	1	0	1	0	Eleven
0	1	0	1	1	0	1	1	Twelve

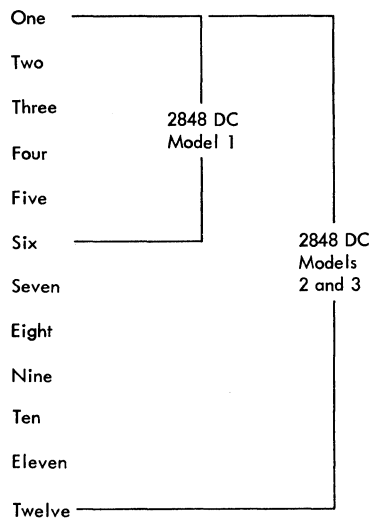


Figure 4-14. Display Line Addresses (Remote)

4. Signal detection of an error or unusual condition to the channel or to the 2848.
5. Provide the channel with specific information regarding an error or unusual condition.

The significance of a given sequence or response may differ, depending on the operation and the receiver; i.e., a specific response received at the 2848 may be interpreted differently from the same response directed to the channel. Thus, the sequences and responses are described for their significance both to the channel and to the 2848 Display Control.

2848 Display Control Sequences and Responses

STX: The STX communication control character precedes all transmission sequences transmitted by the 2848 Display Control. The receipt of STX at the 2701 signals the beginning of a message and causes the 2701 to begin the LRC accumulation. However, the STX character is not included in the LRC check.

ETX: The ETX communication control character, as part of a 2848 Display Control transmission sequence response, indicates the end of a message. Upon receipt of the ETX and the LRC byte following the ETX character, the 2701 performs an LRC accumulation check. At the conclusion of the LRC check, Channel End and Device End are set in the 2701 status register, and the Status byte is presented to the channel. Unit Check is also set in the 2701 Status byte and presented to the channel along with Channel End and Device End if a VRC or LRC error is detected by the 2701.

CAN: The CAN control character is transmitted by the 2848 Display Control only if a buffer parity error is detected by the 2848 during a Read operation (Read Full DS Buffer Storage or Read MI). The 2848 inserts the CAN character between the Text and the ETX communication control character as follows:

STX
2260 address
Text (message)
CAN (Indicates detection of buffer parity error).
ETX
LRC byte

The receipt of the CAN character at the 2701 Data Adapter Unit causes Unit Check to be set in the 2701 status register and Equipment Check to be set in the 2701 sense register.

ACK: An ACK response from the 2848 Display Control to an addressing sequence beginning with SOH indicates that the address has been accepted and that the device is ready to receive the message. An ACK response from the 2848 to a message sequence beginning with STX is an affirmative response, indicating that the message has been received correctly. The ACK response in this case sets Channel End and Device End in the status register of the 2701.

NAK: The 2848 responds with NAK upon completion of a Write operation if, during the operation, the 2848 detects a VRC or LRC error. Channel End, Device End, and Unit Check are set in the status register of the 2701. Data Check is set in the sense register. The 2848 responds with NAK if an addressing sequence is directed to the 1053 Printer while the printer is in a Not Ready condition. Channel End, Device End, and Unit Exception are set in the status register of the 2701.

EOT: The EOT, as a 2848 Display Control response, has more than one interpretation. The following describes the situations under which the 2848 responds with EOT and its significance under each:

1. EOT as a negative response from the 2848 to a Specific or General Poll, indicating the absence of a message pending transfer to the channel. Channel End, Device End, and Unit Exception are set in the status register of the 2701.
2. EOT as a 2848 response to ACK, following a Read operation, indicates the end of transmission (no further messages). Channel End, Device End, and Unit Exception are set in the 2701 status register.
3. EOT as a 2848 response to the transmission of a message during a Write operation indicates loss of data. Channel End, Device End, and Unit Exception are set in the 2701 status register.
4. EOT as a 2848 response to the transmission of a message to the printer indicates a printer buffer overrun condition. That is, the message exceeded printer buffer capacity. Channel End, Device End, and Unit Exception are set in the 2701 status register.
5. The 2848 responds with EOT if an addressing sequence is directed to the 1053 Printer while the printer is busy. Channel End, Device End, and Unit Exception are set in the 2701 status register.

No Response: If a response from the 2848 is operationally anticipated but is not forthcoming within the time allotted (2 seconds), the 2701 Data Adapter Unit times out (see 2701 Line Time Out). When this occurs, Channel End, Device End, and Unit Check are set in the 2701 status register. Time Out is set in the 2701 sense register.

The causes of a No Response condition are:

1. An illegal command (fourth byte of an addressing sequence).
2. An illegal 2848 address (second byte of an addressing sequence).
3. An illegal 2260 or printer address (third byte of an addressing sequence).
4. Detection of a parity error in the addressing sequence.
5. Detection of a parity error in a line control character, or an improperly transmitted line control character.
6. Defective communication facility.

Channel Sequences and Responses

STX: STX is transmitted by the channel as the first character of a transmission sequence. The receipt of STX by the 2848 causes the 2848 to initiate the LRC accumulation. STX may also be used as a positive response from the channel, in substitution for ACK, following a Read MI operation. In this case, it causes the keyboard of the selected 2260 Display Station to be restored, causes the start symbol to be erased, and places the 2848 in the WRITE mode.

ETX: ETX as a channel response to the 2848 indicates the end of a message. Upon receipt of ETX and the LRC byte following the ETX character, the 2848 performs an LRC accumulation check. Channel End and Device End are set in the status register of the 2701 upon transmission of ETX and the LRC byte from the channel.

ACK: An ACK response from the channel to a message received from the 2848 as a result of a Specific or General Poll is an affirmative response indicating that the message was received correctly. Upon receipt of the ACK response at the 2848, the keyboard of the selected 2260 Display Station is restored, and the start symbol is deleted.

NAK: A NAK response from the channel indicates that an error was detected in a message sequence transmitted by the 2848 Display Control. The NAK response from the channel causes the 2848 to retransmit the message.

SOH: The SOH communication control character is transmitted by the channel only, and it is used as the first character of all addressing sequences containing a Write command. This control character may also be used as a negative response to a message sequence from the 2848. In this case, it terminates the operation.

EOT: The EOT is used as the first character of the Specific Poll, General Poll, and Read Addressed Full DS Buffer addressing sequences. EOT concludes an operation. An EOT response from the channel to a transmission sequence from the 2848 ending in ETX and LRC indicates a negative response to the transmission sequence and terminates the operation.

2701 Line Time Out: 2701 Line Time Out can be defined as the lapse of a specific time period (2 seconds) allotted for the receipt of a line signal, during which time a line signal does not occur. The term "line signal" refers either to the Start bit of a data character or the Start bit of a response. Line Time Out causes Channel End, Device End, and Unit Check to be set in the 2701 status register. Time Out is set in the 2701 sense register.

FUNCTIONAL UNITS

This paragraph describes the operation of each major logical area of the remote interface adapter in terms of its contribution to overall adapter operation. References to the pertinent ALD logic pages are provided to support the text presentation for areas where the ALD can be interpreted without simplification. Simplified diagrams are provided for areas whose ALD page(s) are not easily understood without some simplification. The control areas (write control, read control, delay line control, etc.) are not explained with simplified diagrams, nor is reference made to the ALD pages for these areas. The control area logic has been simplified in a series of diagrams provided as Figures 4-15 through 4-33, which are used to support the theory of operation discussion for the write and read operations.

The remote interface adapter is shown in block diagram form in Figure 4-15. Each major logic area is shown as a block; the blocks are interconnected to illustrate the major data and control exchanges between logic areas. Overall data flow for both the read and the write operations is also shown in the figure. The write operation data path is indicated by the heavy, solid line connecting the blocks. Read operation data flow and operations unique to the read operation are indicated by a heavy, dashed line.

Adapter Data Flow

All command operations of the remote interface result in the adapter performing one of two basic operations: read or write, with only minor variations for specific commands. In the paragraphs that follow, the data flow for both the write and the read operations is discussed in conjunction with the block diagram provided as Figure 4-15.

Write Operation

During normal operation, data is constantly received by the adapter from the data set. This serial input data is accepted and shifted into the Serdes register at a rate of 1.2 kc or 2.4 kc, depending upon the data set associated with the display control. When a complete character (9 bits) has been shifted into Serdes, the seven data bits and the check bit are transferred to the character register. The outputs of the character register are sampled at the ASCII command decoder to determine whether an SOH or an EOT control character is in the character register. If a control character is not detected, the data in the character register is disregarded, and new data is accepted from Serdes.

If an SOH or EOT is detected, the next two bytes containing the 2848 address and the 2260 address are decoded to determine which 2848 is being addressed and, if so, which display station is involved in the impending operation. The fourth byte is routed to the command decoder to determine what operation is to be performed. Thereafter, an ACK response is generated to the channel. Here, assume that a Write command has been decoded.

As the write operation progresses, data is accepted from the data set, assembled in Serdes, and transferred to the character register. When the start-of-text character (STX) is decoded, only the text bytes are used to update the LRC register (accumulate LRC). In the block diagram, note that the parity of each character is checked as soon as it is loaded into the character register. The outputs of the character register that are text bytes are transferred to the serializer through the code converter, which reduces the seven-bit ASCII code to a six-bit code that is used by the 2848 control circuits. The serializer enters the parallel outputs of the character register in the delay line as a string of serial data bits. The delay line acts as a character buffer and can store up to 35 characters during the write operation; normally, however, only five or six characters will be present in the delay line. (This is because of new line codes, which can take 16.5 ms/character to process.)

As the write operation progresses, data is extracted from the delay line, deserialized, and

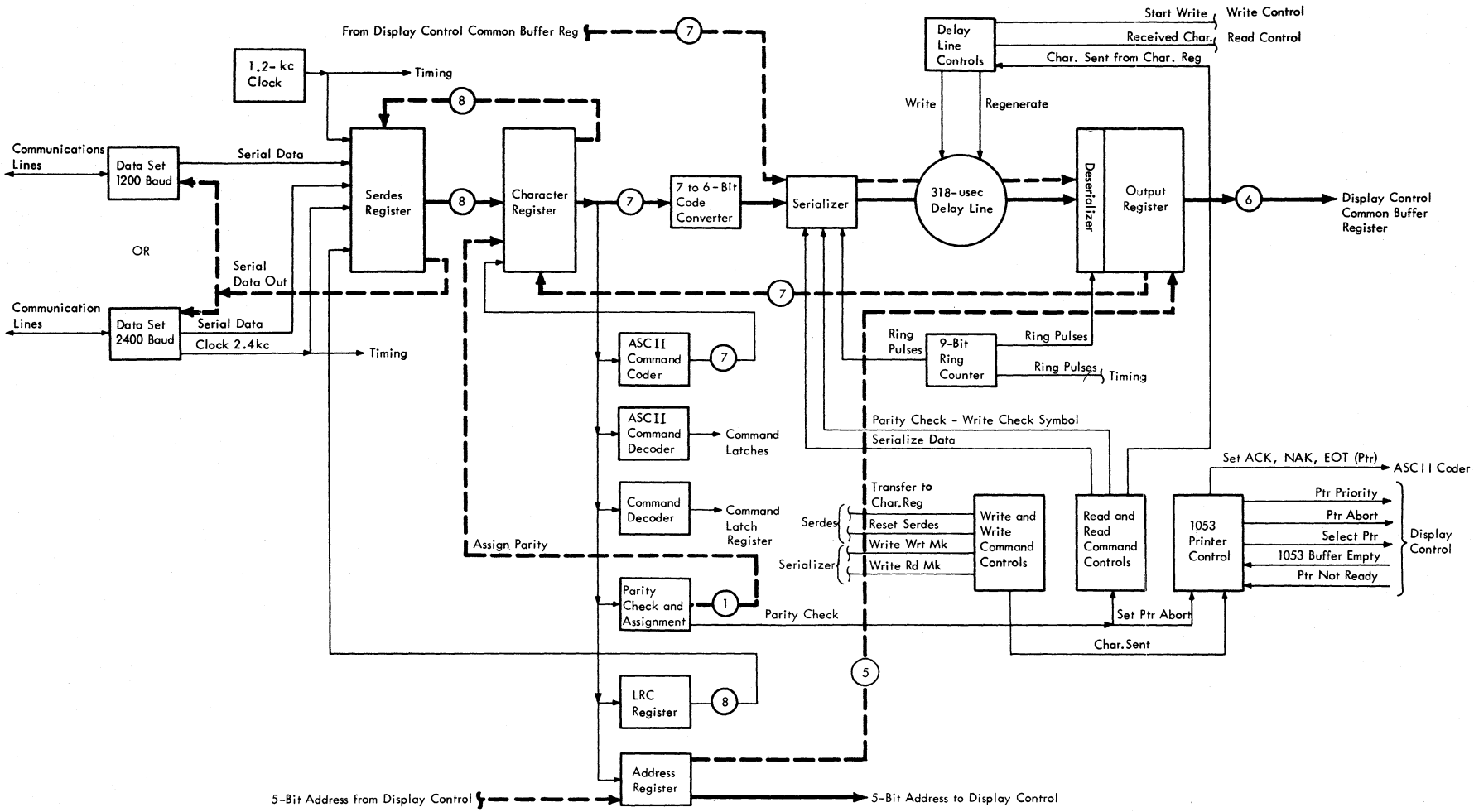


Figure 4-15. Remote Interface Adapter, Data Flow Diagram

transferred to display control through the output register as six-bit bytes of parallel data. Thus, data has been received from the data set, processed within the adapter, and transferred to the display control, where it is entered in the storage of the addressed 2260 Display Station and displayed on its CRT.

Read Operation

During a read operation initiated by the host system, initial selection of the adapter (first four bytes) is much the same as that described for a write operation. Then, as shown in the block diagram, data is transferred from the common buffer register of display control to the serializer in the form of seven-bit parallel bytes. This data is serialized and written in the delay line. Almost immediately, the data is extracted from the delay line, deserialized, and loaded into the output register. The seven-bit output of the output register is transferred to the character register. Here, parity is assigned, and the LRC register is updated. The character register contents are transferred to Serdes. In Serdes, the complete output character is assembled so that a complete 10-bit ASCII character is in Serdes (seven data bits, a check bit, and the Start and Stop bits). This character is then shifted from Serdes as serial output data. Near the end of the read operation (after all text characters have been transferred and an ETX character response has been generated), the contents of the LRC register are transferred directly to Serdes as the LRC character.

Ring Counter

The nine-bit ring counter (ALD C9.20.08.1) is a step counter which supplies a set of nine 1.0-μs timing pulses (ring times) that are used to serialize and deserialize data. These pulses are also used for more general timing purposes within the adapter.

The stepping signal for the ring counter is developed at trigger 5B (ALD C9.20.08.1). The inputs to the trigger are A Delay pulses from display control. The A Delay pulses occur every 500 ns; however, the counter is stepped every 1.0 μs by alternate A Delay pulses because of the frequency divider action of trigger 5B. As the counter is stepped, the counter's triggers are set in succession to generate the string of nine 1.0-μs pulses required as the ring counter outputs.

On ALD C9.20.08.1, note that the Reset signal, which occurs in conjunction with an SOH, ETX, or Printer Reset and whenever the Interface Reset pushbutton on the CE panel is depressed, clears ring counter triggers 1 through 8 and sets ring counter trigger 9. This action sets the counter triggers to the statuses that will cause the counter to generate ring bit 1 when it is next stepped. Once started, the ring counter cycles continuously, producing successive sets of nine timing pulses until ring counter operation is interrupted by the reset condition described above.

1.2-kc Clock and Serdes Control

The oscillator and Serdes control logic (C9.20.16.1) is provided to control data input into the Serdes register when the Type 202D Data Set is used to transmit data at a rate of 1200 baud. The 1200-baud 202D Data Set does not contain a clock; therefore, clocking must be provided by the remote interface adapter. External clocking is not required for the 2400-baud data set because timing pulses are derived from a data set clock. A 76.8-kc oscillator is frequency-divided by a series of triggers until a square wave is derived from trigger 1G (logic page C9.20.16.1). The output of trigger 1G is the midpoint of the first Start bit supplied over the phone lines by the data set. Each 833-μs output of the 1.2-kc trigger is used to gate a data bit into Serdes. The first Start bit received on the Receive Data line sets the Char Start trigger and initiates the Find Bit Center AND located at 3F. If a false start had been detected, signifying that a noise spike had set the Char Start trigger, AND 4G becomes conditioned to reset Serdes and the frequency divider trigger network on logic C9.20.16.1. For transmit operations, the Char Start trigger is turned on by the Send Data line to initiate essentially the same operation as detailed for Receive Data.

Serializer-Deserializer Register

All data, address, and control byte exchanges between the data set and the remote interface adapter are made through the serializer-deserializer register (Serdes). Thus, the Serdes is involved in all remote-interface adapter operations (read and write).

The Serdes is illustrated on ALD logic pages C9.20.00.1 and C9.20.01.1. The Serdes is a 10-bit character used for data and control transfers. On the ALD pages, note that the bit positions are Stop bit, Ser C (check) bit, data bits 7-1, and a Ser Start bit. (The significance of these bits is described in conjunction with the Character Structure and Interface Code discussion.)

During a write operation, Serdes accepts serial data at a rate of either 1.2 kc or 2.4 kc, depending upon the data set associated with the display group. The register assembles the serial input data into the full 10-bit character code to permit the detection of command or control characters (by making input data available in the form of parallel data).

During read operations, the primary function of the Serdes is to convert parallel data received from the character register into serial data which can be transmitted to the data set. The Serdes also accepts the parallel transfer of the LRC character near the end of a read operation and transmits the bits of the LRC character as serial data.

Serdes Data Inputs

The Receive Data input to the Stop trigger of Serdes (C9.20.00.1) is the serial data input to the register. This input represents data sent from the data set. Note that although the data is entered through the Stop trigger, the bits of the input character are arranged so that, when the entire character has been received, the Start bit is received first and is shifted from the Stop trigger through the other triggers of Serdes. When the entire character has been received, the Start bit will have been shifted to the 1-bit position, which is its proper position when receiving a character from the data set.

Parallel data inputs are entered in data bit positions 1 through 7 of Serdes. These inputs originate from either the character regiter (read data) or from the LRC register (LRC character).

The Ser C bit (check bit or VRC bit) is loaded from the parity assignment circuits to provide the proper parity for characters being sent from the adapter to the data set. The Ser C bit trigger is also set from the LRC register. In this case, however, the Ser C bit trigger is merely serving as a repository for one bit of the LRC character and has no significance with respect to LRC byte parity.

The Stop bit and Ser Start bit triggers can be set by the Set Tag input (ALD C9.20.00.1 and 01.1). This input provides for setting the Start and Stop bits of characters being sent to the data set from the Serdes.

Serdes Data Outputs

Once a complete character has been received from the data set and assembled in Serdes, the seven data bits of the character (Serdes bits 1-7) and the check bit are transferred in parallel to the character register. Thus, Serdes provides input data to the character register.

During a read operation, Serdes provides the serial data output to the data set from the Ser Start trigger. The serial output from the Ser Start trigger occurs as a result of loading a character in Serdes and of shifting the register at the required frequency (1.2 kc or 2.4 kc).

Special Serdes Outputs

Two special-purpose (nondata) outputs are derived from Serdes. On ALD C9.20.01.1, note the 1 Bit Ser output from the Ser 1 bit trigger. This output represents the detection of the Start bit in the Ser 1 bit position of the register. It is used to indicate that a complete character is in Serdes. The 1 Bit Ser signal is used to set the Character Sent latch, which causes the transfer of the input character data bits to the character register. Note that the detection of the Start bit while it is in the Ser 1 bit trigger provides a lookahead concept with respect to the presence of a complete character in Serdes.

A second special-purpose output of Serdes is shown as the output of the Ser Empty latch (ALD C9.20.01.1). AND circuits 2D and 2H are used to detect the condition of Serdes being empty (all triggers reset). This condition is significant during read operations since it indicates that a complete character has been sent to the data set and that Serdes is available to accept the next output character.

Register Operation

During a write operation, Serdes accepts serial data input from the data set. The input bits are shifted through Serdes at either 1.2 kc or 2.4 kc. When the Start bit is detected in the Ser 1 bit trigger, the seven data bits of the character and the check bit are transferred to the character register. Serdes is then reset and is ready to accept new serial data.

During a read operation, the output character is assembled in Serdes. This includes the seven data bits, the check bit, and the two tag bits (Start and Stop). The register is then shifted at either 1.2 kc or 2.4 kc to provide serial data outputs to the data set at the proper rate.

Character Register

The character register is an eight-bit latch register (seven data bits plus a check bit) that accepts parallel data inputs from the Serdes register (Control mode and write operation), the output register (read operation), the ASCII command codes (control character exchange), and from the data switches of the CE panel (manual data entry). The register is illustrated on ALD logic pages C9.20.02.1 and C9.20.03.1.

The outputs of the character register are fed to the LRC register, the address register, the ASCII command decoder, the parity circuits, Serdes, the command decoder, or the serializer, depending upon the operation being performed. The latches of

the character register also drive indicators located on the 2848 CE panel.

Control Mode Operation

When the 2848 is in the Control mode, serial data from the data set is continually received through Serdes. When a full character is detected in Serdes, the seven data bits and the check bit of the character are transferred to the character register. Once the data is loaded into the character register, the register's outputs are sampled by the ASCII command decoder to determine whether an SOH or EOT control character has been sent. Character parity (VRC) is also checked at this time. If an SOH or EOT is detected, the 2848 is placed in the control-mode-not-selected. Then, the next two characters loaded into the character register from Serdes are parity-checked and routed to the address register, where a comparison is made to determine whether the address is that of the 2848 Display Control.

If the 2848 was addressed, the fourth character transferred to the character register from Serdes is routed to the command decoder to determine what operation is to be performed. Once the command is decoded, the operation of the character register is determined by the type of operation (read or write) associated with the command. Character register operation for both read and write operations is discussed below.

Write Operation

Once the write operation has started, data bytes are transferred from the Serdes to the character register, where a parity check is immediately performed. Since a write operation is in progress, the character register outputs are gated to the 7-to-6-bit converter where they are converted to the six-bit internal 2848 code and written in the delay line. Succeeding data bytes are treated in the same manner. Note that as each byte is loaded in the character register, the register's contents are sampled for ASCII control characters at the ASCII command decoder. This permits the detection of control characters such as STX, EOT, etc., which can modify or terminate the write operation.

As the write operation takes place, the character register's outputs are also used to update the LRC register so that LRC is accumulated.

Read Operation

During a read operation, the character register is loaded with seven-bit parallel data bytes from the output register. As in the write operation, the character register outputs are used to modify the contents of the LRC register. The contents of the character register are gated to the Serdes, where the complete output character is assembled (data from character register, check bit, and tag bits). Successive read data bytes are transferred from the output register through the character register to Serdes. Near the end of the read operation, the contents of the LRC register (accumulated LRC character) are loaded into the character register and are gated to Serdes for transmission as the LRC character associated with the data characters transmitted as part of the read operation.

Address Register

The address register (logic C9.20.40.1) consists of five bit latches (bits 01, 02, 04, 08, and 16) that are used to store the address of the selected 2260 Display Station during a read or a write operation (or the printer address during execution of a printed command).

The following describes the operation of the address register during a write or channel-initiated read operation and a read manual input operation.

The significance of the address bits and the overall display control and display station addressing scheme is described in Chapter 2 under "Display Addressing."

Write/Channel Initiated Read Operation

During a write or channel-initiated read operation, the contents of the character register are transferred to the address register as follows:

The third byte of the address sequence (device address) causes +Y XFER CR-ADR line to become positive. This signal is inverted to condition one leg of the negative-AND blocks that provide the inputs to the address register bit latches. The remaining leg of the negative-AND blocks is conditioned by the respective outputs of the character register. Thus as the +Y XFER CR-ADR line becomes positive, the contents of the character register are transferred to the address register, and the respective bit latches are set.

The output of the address register is routed to the display control address register, decoded, and used to select a display station.

Read Manual Input Operation

During a read manual input operation, the adapter address register is loaded with the five-bit address originating from the display control when the Attention latch is set as a result of depressing a display station Enter key. The output of the address register is routed to the output register and then

transferred to the data set through the normal character register - Serdes read data transfer path.

Command Decoder

The command decoder (C9.20.11.1) consists of a five-AND-level decoder; it decodes the fourth non-ASCII control character after an SOH or EOT, which defines the command that the selected 2848 will perform. Only one AND is conditioned to issue its associated command, as defined in Figure 4-17. Six different commands (Figure 4-16) are employed in the addressing sequence, although only five AND's make up the command decoder. This appears to be a discrepancy; however, the remaining command (Write DS Line Address) is not decoded by the command decoder (20.11.1) but, rather, by the 2848 Display Control. The 2848 Display Control must contain the line addressing feature (feature code 4787) before the Write DS Line Address command can be accepted. The Write DS Line Address command causes the cursor of the selected 2260 to be positioned in the first displayable position of the specified line. The line address is specified by the first character following the STX line control character. If a write address line feature is not incorporated, and if a 2848 were selected to perform that command, the remote interface would time out, and an SOH or EOT would have to be generated in order to recover.

The command decoder becomes active whenever the Decoder Command level is up. This level is supplied by the Device Address trigger, which signifies that the contents of the character register represent a command and, therefore, must be decoded by the command decoder.

ASCII Command Decoder

The ASCII command decoder (C9.20.10.1) is used to decode seven of the eight ASCII communication control characters, which can be programmed singly or in sequence format to perform all the control functions necessary to establish and maintain an orderly flow of traffic between the remote interface and the data set. The eight control characters are as follows:

Start of Text	(STX)
End of Text	(ETX)
Start of Heading	(SOH)
Acknowledge	(ACK)
Negative Acknowledge	(NAK)
End of Transmission	(EOT)
Line Feed	(LF)
Cancel	(CAN)

NOTE: Cancel is only transmitted by 2848 Display Control if a buffer parity error is detected during transmission of a message.

The ASCII command decoder receives its level inputs from the character register and decodes them in accordance with the sequences and command operations treated elsewhere in this manual. Also shown in logic C9.20.10.1 is the decoder AND (3H) used to select the 2848 Display Control. Input signals to AND 3H must be wired to the proper character register latches associated with its assigned address.

Command Name	Decoder AND	Function Code Bits 7	6	5	4	3	2	1
Specific Poll	2A	0	1	0	0	0	0	0
General Poll*	2D	1	1	1	1	1	1	1
Read Buffer	2C	0	1	1	0	0	0	0
Write DS or Printer	4A	1	0	0	0	0	0	0
Erase	4C	1	1	0	0	0	0	0
Write by Line Address**	--	1	0	1	0	0	0	0

*The general poll is identified by an all-1's condition in the third character of the addressing sequence. An all-1's code for this character and the indicated function code signifies the general poll.
**Decoded by 2848 Display Control.

Figure 4-16. Command Decoder Function Codes

ASCII Command Coder

The ASCII command coder (ALD C9.20.12.1) provides a means for the remote interface adapter to generate the ASCII control characters required for adapter responses to the data set during the various adapter operations. The codes for ASCII control characters ACK, NAK, EOT, and STX Trans can be generated from the coder. Other characters such as ETX and CAN are generated by other control circuitry in the remote interface.

When the adapter control logic determines that a response in the form of an ASCII control character is required, a latch within the ASCII coder is set (for example, the ACK latch). The ACK latch outputs are used to set the bit positions of the character register that are required to load the ACK character code into the character register. The ACK latch's output is also used to indicate to the adapter control latch that an ACK response is being sent to the data set.

The other ASCII control characters (NAK, EOT, and STX Trans) are generated in much the same way by the ASCII coder. In each case, the character register bit positions that must be set (so that the register contains the desired character code) are set through use of the coder latch's outputs.

As with the ACK latch, the outputs of all coder latches are used to indicate to the adapter control logic that a particular response is being generated.

LRC Register

The LRC (longitudinal redundancy check) register provides a means of determining whether a message has been received correctly during write operations. During read operations, the LRC register is used to accumulate LRC data so that an eight-bit LRC character (contents of LRC register) is available for transfer to the IBM 2701 via the data set link. The IBM 2701 uses the adapter-originated LRC character to determine whether the read data was received without error.

The overall concept of LRC error checking can be illustrated by considering LRC operation during a write operation. Initially, the LRC register is cleared. Then, as the first data byte is transferred through the character register, the outputs of the character register latches (including the parity bit latch) are used to load the triggers of the LRC register. Thereafter, as successive data bytes are transferred through the character register, the LRC register contents are modified as follows:

Character Register Contents	Old LRC Register Contents	New LRC Register Contents
1 (check bit)	1	0
1	0	1
1	1	0
0	0	0
1	1	0
0	1	1
1	0	1
1	1	0

Note that each 1-bit in the character register complements the associated LRC register trigger. This updating of the LRC register continues until all data bytes of the input (write) message have been transferred through the character register. Then, the LRC character transferred to the adapter as part of the input message is loaded into the character register. If the message was received without error, this LRC character should match the end contents of the LRC register. Thus, when the LRC character is used to update the LRC register, the LRC register should be reduced to zero, as follows:
(Remember that each 1-bit in the character register complements the associated LRC register trigger.)

Contents of LRC Register (LRC Character)	End-Contents LRC Register	New Contents of LRC Register
1	1	0
0	0	0
0	0	0
1	1	0
0	0	0
1	1	0
1	1	0
1	1	0

If any 1-bits remain in the LRC register after it is updated with the LRC character, an error condition is indicated.

LRC Operation During Write

When the data set is performing a write operation and the Start of Text command is decoded, the LRC register is cleared. This prepares it to accept text character inputs. The bits making up the text character are tied directly to the LRC register, where they complement their associated bit position if the input bit is a 1. Updating of the LRC register continues as long as text character bytes are received. The set condition of the EOT latch signifies that all text bytes have been transferred and that the next character received will be the LRC character. The LRC character should match the contents of the LRC register, thus reducing its contents to zero. The cleared state of the LRC register is a positive indication that transmission of the preceding message was executed correctly. This condition is checked by AND 2E (logic C9.20.20.1). If the content of the LRC register does not equal zero after receipt of the LRC character, the remote interface responds with a NAK, which causes the data set to retransmit the message.

LRC Operation During Read

The operation of the LRC register during a read operation begins when the STX-Transmit latch is set, which clears the LRC register. As data bytes are entered into the character register, the LRC register content is accumulated in the same manner as during the write operation. Note, however, that since parity must be assigned to each byte, the input to the LRC check bit position is provided by the Assign Parity input to OR 5A instead of by the character register bit-1 position. When the last text character (immediately following ETX) is transmitted to the data set, the content of the LRC register must be the next character transmitted to the data set. The

2701 checks the LRC character in the same manner as the remote adapter performs its check during write operations. The TSM LRC character signal is used to transmit the content of the LRC register by shifting its contents into the Serdes register.

Parity Check and Assignment

The parity check and assignment circuit (ALD C9.20.30.1) is used to assign (read operation) or check (write operation) parity on a data byte basis. This parity checking scheme is also called the vertical redundancy check. Parity is checked during a write operation and assigned during a read operation. Even parity is used; that is, if the total number of 1-bits in the character byte equals an odd number, the parity bit is assigned (1). If the total number of 1-bits in the character equals an even number, the parity bit is not assigned (0).

Parity Assignment

During read operations, parity is assigned to each text character whenever the character is placed in the character register. Coincident with the parity assignment operation in the character register, the Check bit in the LRC register is also updated to reflect the content status of the character register. The Check bit in the LRC register is accumulated in the same manner as the data bits each time parity is assigned.

Parity Check

During write operations, each incoming character is checked in relation to the parity bit (Check bit) associated with the character. As stated above, if the Check bit is found to be even, no parity error exists, and the incoming character is accepted. If odd parity is detected, the Parity Check latch is set at Character Sent R4 time (C9.20.13.1). The output of the Parity Check latch and the Text Mode level are AND'ed to reject the incoming character, substituting the Check symbol in its place as the data is written in the delay line. Therefore, a check symbol is displayed on the CRT of the selected display station, and the message is continued. If a parity check is detected during a message transfer to the printer, a quote symbol (") is the last character printed. This alerts the operator to the fact that a parity check occurred and than an incomplete message has been printed. Data entry in the remote interface continues until ETX occurs; however, the data is not channeled to the 1053 buffer. Further operations during this message sequence are aborted.

Serializer and 7-to-6 Bit Code Converter

The serializer provides a means of converting parallel data into the serial data form that is required to enter data in the adapter delay line. The data that can be written through the serializer is listed below:

1. Output of character register (seven bits)
2. Output of common buffer register in display control (seven bits)
3. Code for Line Feed character to printer (two bits: bits 3 and 7)
4. Code for Check symbol (two bits: bits 2 and 6)
5. Write mark (one bit)
6. Read mark (one bit)

The serializer logic also includes provisions for converting the seven-bit ASCII code from the character register into the six-bit code required by display control as the data is written from the serializer. The serializer logic is shown on ALD pages C9.20.04.1 and 05.1.

All of the multiple-bit inputs listed above are serialized in an identical manner. Therefore, the serialization of parallel data as discussed here is applicable to all data inputs. In paragraphs that follow, the unique gating and ring-bit time-to-bit position relationships for each data input are discussed. The operation of the 7-to-6 bit converter is discussed in conjunction with the character register input to the serializer.

The outputs of the ring bit counter are used to serialize data for entry into the delay line. For example, note AND circuits 4E, 4D, 4B, and 4A (ALD C9.20.05.1) and AND circuits 4C, 4B and 4A (ALD C9.20.04.1) to which the common buffer register outputs are applied as inputs. These AND circuits also have ring bits 3 to 9 as inputs. If the data outputs of CBR are present at the AND circuits, the AND's will be successively conditioned as the ring bit cycles. It is seen that the CBR data bits are reflected in the status of the -Y Serial to DL (delay line) output from ALD C9.20.05.1. Each time the -Y Serial to DL line is conditioned, a 1-bit is written in the delay line. At the completion of the ring bit cycle (ring 9 time), the parallel data byte from the CBR will have been written in the delay line as a string of serial data bits. The serialization of other inputs to the serilizer is accomplished in the same manner, using ring bit pulses.

Character Register Inputs

The serializer accepts a seven-bit input from the character register; however, this seven-bit input is converted to an intermediate six-bit code as the data is serialized and written in the delay line.

On ALD C9.20.05.1, note OR circuit 5F and AND circuits 4F and 5G. These circuits combine to provide the required code conversion. The actual conversion consists of detecting the status of bits 6 and 7 of the character register and using the results to determine the status of bit position 2 of the byte written in the delay line. The decoding of bits 6 and 7 and the actions resulting are shown below:

Character Reg Bit Status		Circuits Conditioned	Circuits Deconditioned	Serializer Bit 2 Status
Bit 7	Bit 6			
1	1	AND 5G OR 5F	AND 4F	0
1	0		OR 5F AND 5G AND 4F	0
0	1	OR 4F AND 4F	AND 5G	1

It is seen that serializer bit 2 is a 1 only when bit 6 is a 1 (negative output from a conditioned OR 4F) and bit 7 is a 0 (negative output from a deconditioned AND 5G). Then, since both inputs B and C to AND 4F are negative, AND 4F is conditioned upon Serialize Write Data and Ring Bit 4, and a 1 bit is written in bit position 2 of the serializer.

The following relationships exist among the character register bits, the serializer bits, and the ring bit pulses used to write into the delay line.

Character Register Bit	Serializer Bit Position	Ring Bit Time
-	1 (not used)	
6 and 7 (high-order bit)	2 (high-order)	4
5	3	5
4	4	6
3	5	7
2	6	8
1 (low-order bit)	7 (low-order)	9

The outputs of the character register are written in the delay line when the Serialize Write Data signal is issued from the write control logic during a write operation.

Common Buffer Register Inputs

During a read operation, the serializer accepts a seven-bit input from the common buffer register of display control. This input represents the seven data bits of the ASCII character that is to be sent to the data set.

Since the serialization is accomplished in the standard fashion, only the data-bit and ring-bit relationships are discussed here.

It can be seen on the ALD logic that a Char Avail level is required before CBR data is serialized and written in the delay line. This level is issued from the read control logic when a character is available in the CBR.

The bit and ring bit time relationships are as follows:

CBR Bit	Serializer Bit Position	Ring Bit Time
1	1	3
2	2	4
3	3	5
4	4	6
5	5	7
6	6	8
7	7	9

Special Character Inputs

The serializer also receives parallel inputs that permit wiring the codes for a line feed (printer) or a check symbol in the delay line.

The Line Feed character is written when the +Y Line Feed level is issued from the control logic (see ALD's). The bit position of the serializer and the ring bits used to write the line feed character are as follows:

Serializer Bit Position	Line Feed Input	Ring Bit Time	Data Bit Written
1	-	3	0
2	-	4	0
3	x	5	1
4	-	6	0
5	-	7	0
6	-	8	0
7	x	9	1

Note that the above inputs to the serializer result in the required line feed code of 1000100 (bits 7 to 1 respectively).

The code for the check symbol is written in much the same way. The bit positions, data parity check inputs, and ring bit times associated with writing the check code are as follows:

Serializer Bit Position	Data Pty Chk Input	Ring Bit Time	Data Bit Written
1	None	3	0
2	AND 5G and OR 4F; ALD 05.1	4	1
3	AND 4C; ALD 05.1	5	0
4	AND 4H; ALD 04.1	6	0
5	AND 4G; ALD 04.1	7	0
6	OR 5D; ALD 04.1	8	1
7	AND 4F; ALD 04.1	9	0

As shown above, the six-bit check symbol code is written in the delay line as a result of a data parity error condition. Note that the check code is written through the same serializer AND's that service the character register and that the -Y Serialize Write Data level is required to write the check code.

Read and Write Mark Inputs

The read and write marks are written in the delay line through the serializer. On ALD C9.20.05.1, note that the read mark is always written in conjunction with ring bit 1 and that the write mark is written with ring bit 2. Ring bit 1 and 2 times are reserved for these purposes and are not used to write any other data in the delay line. Thus, the write and/or read mark can be written in the "unoccupied" bit positions of any character written in the delay line.

Delay Line

The delay line used in the remote interface adapter is similar to the delay lines used in the display adapter. Delay lines in the display adapter utilize a non-return-to-zero (NRZI) mode of operation, whereas the remote delay line operates in the return-to-zero (RZI) mode. The length of the line is 317.6 μs; the line has a capacity of 315 bits. Each character stored in the delay line requires nine bits; hence, 35 characters can be stored in the delay line. Bit entry into or exit from the delay line is controlled by the nine-bit ring counter at a rate of 1 μs per bit. The format of a delay line character is as follows:

Character Bit Position	1	2	3	4	5	6	7	8	9
	Read Marker	Write Marker	B1	B2	B3	B4	B5	B6	B7

Information in the delay line is continually regenerated until the information is read out from the delay line and routed to its destination. New information can be written into the delay line whenever it is supplied by the character register and a 1 is detected in the Write Marker bit. This bit indicates where the character can be loaded in the delay line. When the character is loaded in the delay line, the Write Marker bit is advanced to the next character position in the delay line.

Only one of the 35 character locations will contain a 1 bit in the read marker position. The read marker identifies the character that the output buffer register will accept during a readout operation. When the character has been placed in the output buffer register, the read marker is advanced to the next character. Both the read and write markers can occupy their respective bit locations (bits 1 and 2) in the same character position under two conditions, i.e., when the delay line is empty and when it is full. If the read marker is inserted in a character position that contains a write marker, and if the Continuous latch is not set, the delay line is empty. Conversely, if the write marker is inserted in a character position that contains a read marker, and if the Continuous latch is set, the delay line is full. If the delay line becomes full, additional store or write operations are inhibited until one of the character positions has been emptied (read out), thus permitting the next word to enter the delay line.

Deserializer and Output Register

The deserializer and output register accepts serial data outputs from the adapter delay line and, using the outputs of the ring counter as timing pulses, reassembles (deserializes) the serial bits into a parallel byte during both write and read operations. After the serial bits are assembled, the contents of the output register are transferred to either the common buffer register of the 2848 Display Control (write operation) or to the character register of the adapter (read operation). The Output register also accepts a 5-bit parallel input from the Address register when the display address must be transferred to Display Control during a Write operation.

The output register and deserializer circuits are shown in ALD logic pages C9.20.06.1 and C9.20.07.1. In the paragraphs that follow, the operation of the deserializer as it loads the latches of the output register and the entry of the address in the output register are discussed. The operation of the Output Reg Empty latch is also discussed.

Deserializer

The deserializer consists of a set of seven AND circuits that gate serial data outputs from the delay line into the latches of the output register. AND circuit 4A (ALD C9.20.06.1), which is associated with the

Bit 7 latch of the output register, is representative of the deserializer AND circuits. Note that AND 4A has a Serial Data Out input which is also routed to the deserializer AND circuits for the other six bit positions of the register. This input is the serial data output of the delay line. AND 4A also has Ring Bit 8 as an input. When data is to be read from the delay line and assembled in the output register, the delay line output is gated to all deserializer AND circuits. However, since all deserializer AND's are conditioned by a different ring bit time, only one AND at a time is conditioned. For example, AND 4A is conditioned at ring bit 9 time if data is gated to the AND and the data bit is a binary 1. The data bits were written into the delay line in conjunction with these same ring times so that both the data bit and the proper bit ring pulse will occur at the same time. Now, on ALD's C9.20.06.1 or 07.1, note the relation between the bit positions of the output register and the ring bit times used to condition the deserializer AND's and, therefore, load the register's latches. This relationship is as follows:

Output Register Bit Position	Ring Bit Time
1	3
2	4
3	5
4	6
5	7
6	8
7	9

If the serial delay line data is available at the deserializer AND circuits, the seven output register latches will be loaded in succession as the ring bit cycles. At ring bit 9 time, a complete byte (seven bits) will have been loaded in the output register. Thus, the serial delay line data is available in the output register in the form of a parallel data byte.

As stated previously, the deserializer AND's are used to load the output register with delay line data during both read and write operations.

Address Transfers to Output Register

When the display address is to be transferred to display control, the address is loaded directly into the output register from the adapter's address register. On ALD C9.20.06.1, note that address bit 01 is associated with output register bit 7 (AND 4B). When the Load Add Reg input to AND 4B occurs, the 01 bit of the address is loaded into the Bit 7 latch. Other bits of the five-bit address are associated with bit positions 3-6 of the output register. Once the address has been loaded in the output register, it is transferred to display control.

Output Register Empty Latch

The Output Register Empty latch (ALD C9.20.06.1) is set at ring bit 9 time whenever all latches of the output register are in the reset state (AND 2D). The latch's output indicates that the output register is available to accept new data and indicates that data in the register has been transferred.

Write and Write Command Controls

The write and write command control logic governs the write sequence by directing the transfer of input data through the adapter and by initiating the required exchange of ASCII control characters with the data set. The write controls also direct the entry of all data into the adapter delay line. The operation of the write and write command logic is described in detail in conjunction with the adapter theory of operation.

Read and Read Command Controls

Data is read from the 2848 Display Control, through the adapter to the data set, under direction of the read and read command control logic. During the read operation, the read control logic causes the adapter to request and process data from the 2848. Read control establishes the sequence wherein the data is assigned parity and tag bits (Start and Stop) and is transferred from the adapter as serial data.

The read and read command control logic is illustrated in simplified form and discussed in detail in conjunction with the adapter theory of operation description.

1053 Printer Controls

When a write operation that involves the 1053 Printer Model 1 is being performed, the printer control logic provides the required interface between the printer logic within the 2848 Display Control and the remote adapter. In Figure 4-15, note that the printer control logic accepts printer-status signals from the 2848 and both select and direct printer operation. The printer control logic also determines when printer-oriented ASCII control characters should be issued to the channel by providing the required input to the ASCII coder.

THEORY OF OPERATION

General

The information presented here relates to the theory of operation of the remote interface adapter, an

optional feature, when it is used in conjunction with a 2848 Display Control and associated 2260 Display Station(s) or 1053 Printer(s). The remote interface is capable of responding to eight common operations; however, for brevity, only three of the command operations are described here since they are the basis from which the other operations are derived. A detailed description and supporting simplified diagrams are provided in the following paragraphs for each of the three command operations: Write Addressed DS, Write Printer, and Specific Poll to 2260 DS.

Addressing Sequence - Write Operation

Channel Response - SOH, EOT Character

Data transmission from a data set to the remote interface begins with the transmission of an EIA (Electronic Industries Association) Receive Data signal to all remote interfaces, in preparation for generation of the addressing sequence that is to follow. The data set proceeds to transmit an SOH (Start of Heading), which is a communication control character that precedes the issuance of a display control address, device address, and command function.

Once the SOH character is entered into the Serdes register (Figure 4-17 and FC-101(3)) of the remote interface (refer to Write Operation paragraph), its Start bit causes the Character Sent latch to be set at ring 1 time of the ring counter. At ring 2 time, the Parity Check latch is reset. At ring 3 time, the data entered in Serdes is transferred in parallel to the character register. At ring 4 time, the Serdes register is reset, and a Char Sent 4 signal (Char Sent latch set and Ring Bit 4 Time signal) is AND'ed at A3 with the SOH or EOT signal to produce a DC Sel Rst signal and set the SOH-EOT Detect latch (Figure 4-18). In addition, this signal is also routed to reset the SOH-EOT trigger, the DC Select trigger, and the Device Adddress triggers contained in each of the remote interfaces before generation of the display control selection and display station address characters of the addressing sequence.

At ring bit 5 time, a Char Sent R5 signal is AND'ed at A4 with the SOH-EOT Decode signal to set the SOH-EOT trigger. This trigger provides the gating level to A5, which allows the DC Selected trigger to be set in the event of a legal display control address (second character of the addressing sequence) by the data set. At ring 8 time, with the Character Sent latch set, the character register is reset in anticipation of the next character (DC Address). At ring 8 time, with the SOH-EOT Detect latch set, A8 is conditioned to generate a general reset signal. Subsequent setting of this latch, as a result of another SOH-EOT signal being detected during the operation in progress, causes a general reset operation to occur, aborting the operation.

At ring bit 9 time, the Character Sent latch is reset, thus terminating the processing of the first character in the addressing sequence by the remote interface.

Channel Response - DC Address

The second 10-bit character generated by the data set contains the address of a specific control unit and is entered serially into the Serdes registers of the various remote interfaces. With the receipt of the Start bit (tag) (Figure 4-17 and FC-101(2)) of the second character, the character is processed in the manner described for the first character up to the point at which it is entered into the character register at ring bit 3 time.

With the entry of the display control address character in the character register, the display control address is decoded by the address decoder, and the remote interface involved proceeds to process the byte in the following manner. Upon the receipt of the display control address byte, a DC Select signal from A1 is AND'ed with the output of the SOH-EOT trigger (gating level), previously set by receipt of the first character entered in the character register, and with a Char Sent R5 signal (ring bit 5 time) at A9 to set the DC trigger. This trigger, when set, generates a signal (DC Selected) which is routed to reset the address register (Figure 4-19) and to set the Request to Send trigger. The output of this trigger is an EIA Request to Send signal which is routed to the transmitting data set as an indication that a 2848 has been selected and is awaiting receipt of a particular display address associated with the selected 2848. In turn, the data set transmits a Clear to Send signal to the remote interface, which subsequently allows the interface to transmit to the data set. At ring bit 8 time, the character register is reset. At ring bit 9 time, the Character Sent latch (Figure 4-17) is reset, thus terminating the processing of the second character by the remote interface.

Channel Response - 2260 DS Address

The third character in the addressing sequence generated by the data set contains the address of the device (2260 Display Station or 1053 Printer Model 1) to be selected. This particular character contains a 1-bit either in position 6 or in position 7 to distinguish it from that of a communication control character.

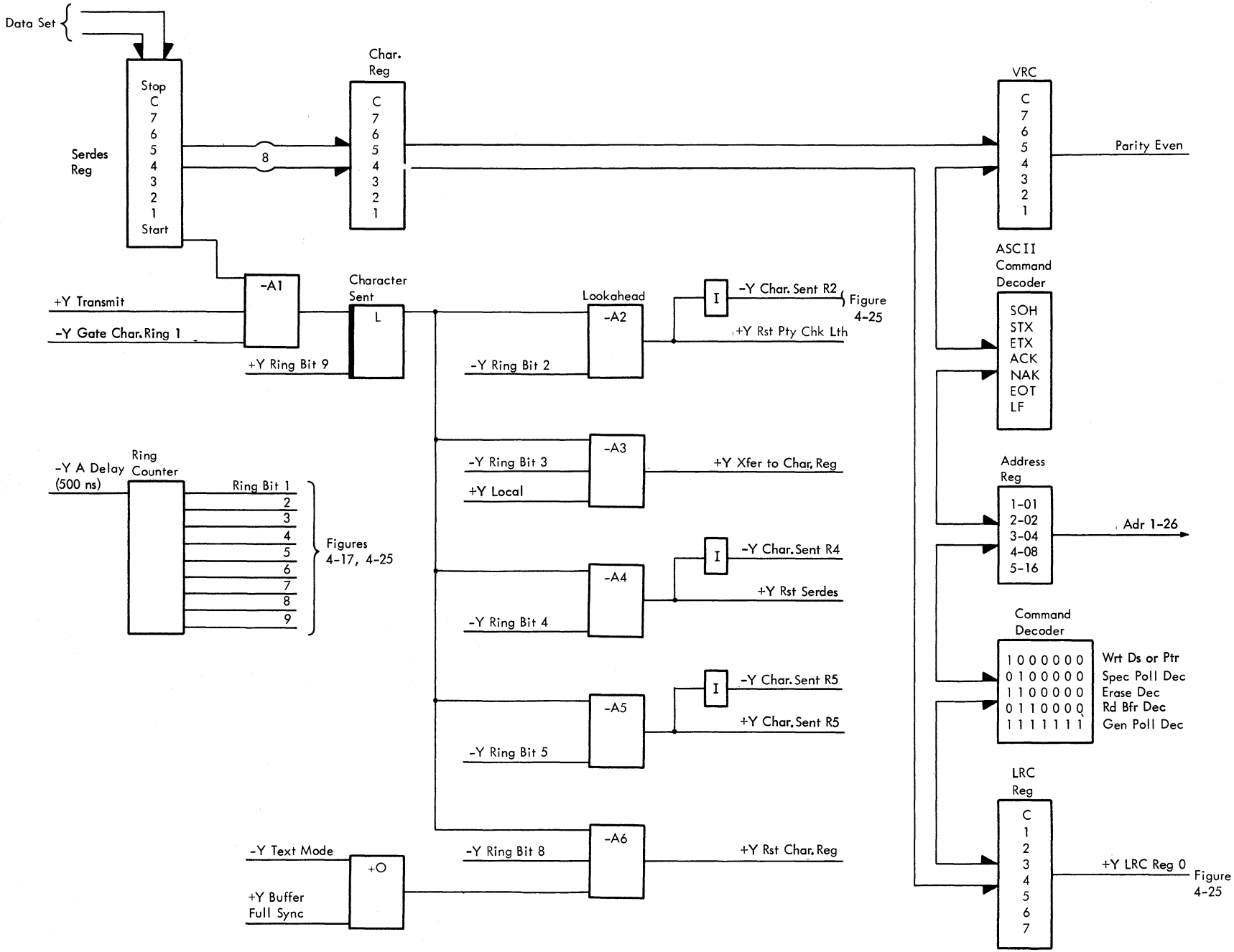


Figure 4-17. Character Register Control

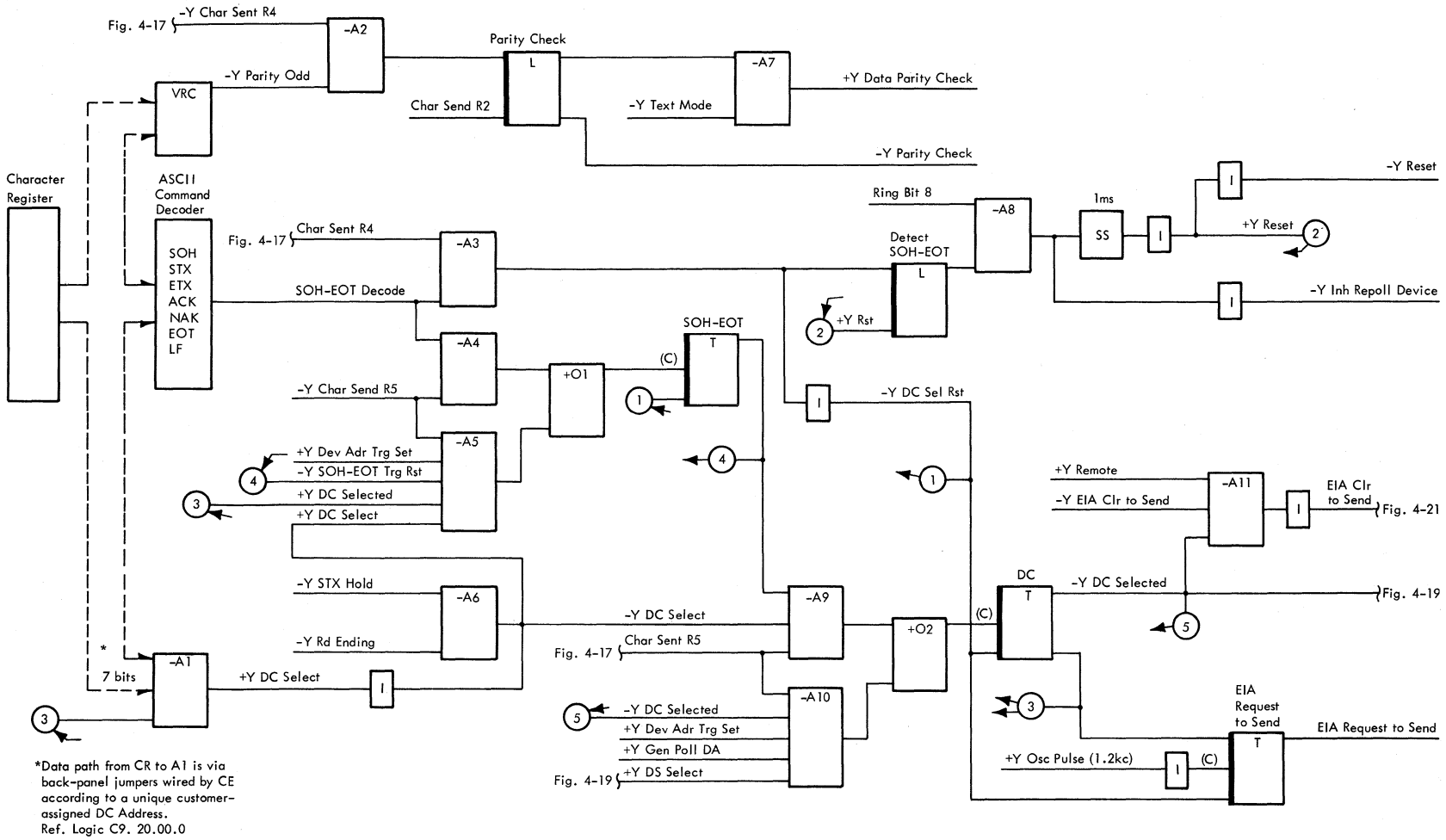
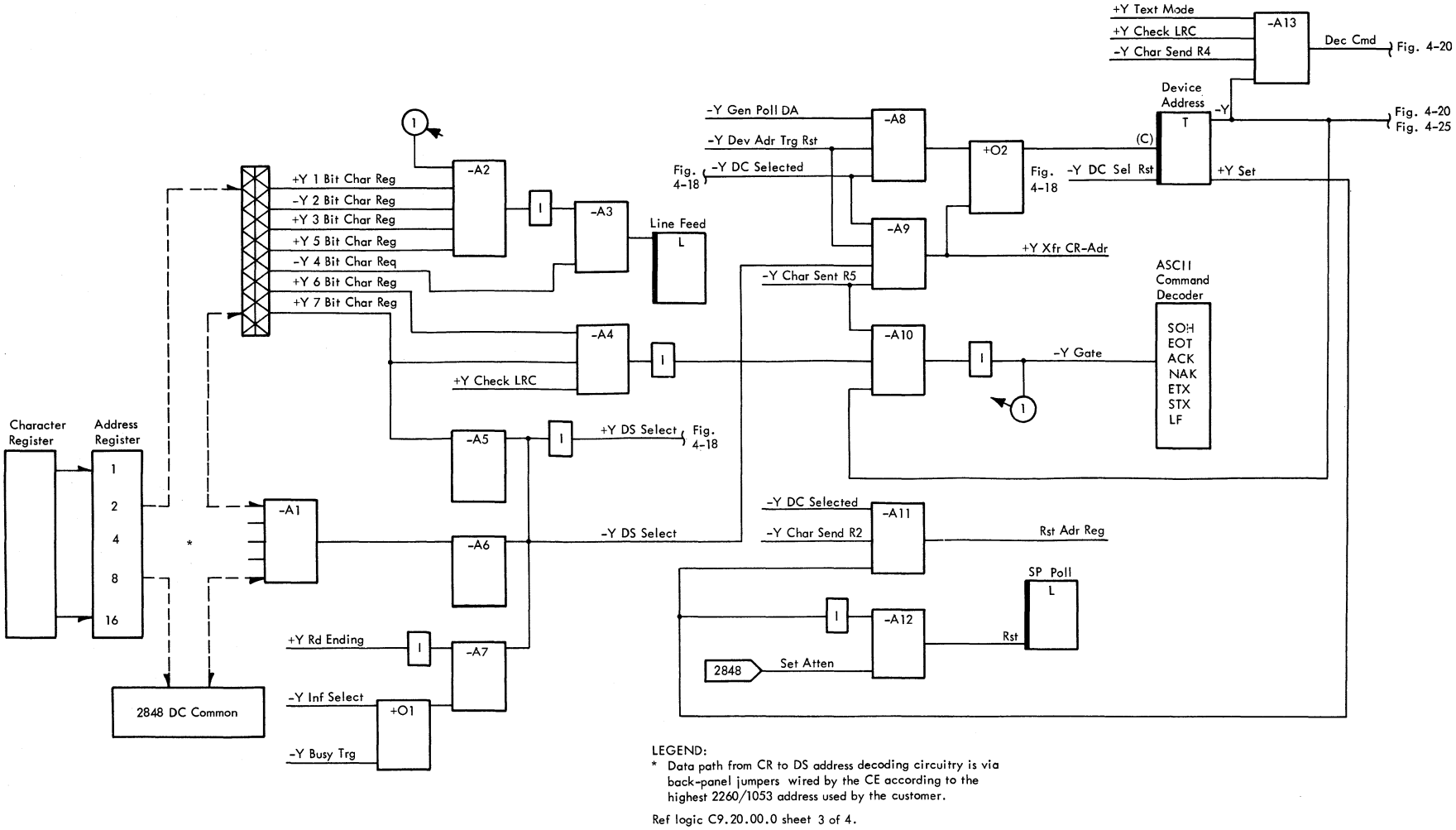


Figure 4-18. Channel Response, SOH-EOT and DC Address Characters



LEGEND:
* Data path from CR to DS address decoding circuitry is via back-panel jumpers wired by the CE according to the highest 2260/1053 address used by the customer.

Ref logic C9.20.00.0 sheet 3 of 4.

Figure 4-19. Channel Response, Device Address Character

Again, the character transferred from the data set is processed the same as the two characters previously received (to the point at which it is to be entered into the character register). The Character Sent latch having been set, a Char Sent R2 signal is generated. This signal is AND'ed with the output signal generated by the DC Select trigger (DC Selected) and with the reset output signal from the Device Address trigger; this conditions A11 (Figure 4-19) and produces a signal that will reset the address register.

At ring bit 3 time, the device address character is transferred from Serdes to the character register. At ring bit 4 time, the Serdes register is reset.

When the device address entered in the character register is decoded, a signal (DS Select) is generated (Figure 4-19 and FC-101(3)) which is AND'ed with a Char Sent R5 signal (ring bit 5 time), with the set output (DC Selected) signal from the DC Selected trigger, and with the reset output signal from the Device Address trigger to Condition A9 and turn on the Device Address trigger. In addition, a signal (+Y DS Select) is also routed to prevent the DC Select trigger from being reset. Conditioned AND 9 also generates an XFR CR-ADR signal to enable the device address contained in the character register to be transferred to the address register and then to the five-bit address register in the 2848.

If bits 6 and 7 are 1-bits (indicating selection of a display station) coincident with the Device Address trigger being set and with a Char Sent R5 signal, A10 is conditioned to produce a signal which is routed to gate the response AND gates (STX, ETX, ACK, NAK) in the ASCII command decoder preparatory to the receipt of the fourth character (command character). At ring bit 8 time, the character register is again reset, followed by reset of the Character Sent latch at ring bit 9 time. This completes the processing operation of the Device Address character in the remote interface.

Command - Write Addressed DS

The fourth character in the addressing sequence from the data set specifies the command to be executed by the 2848 and the 2260 or 1053. The character transfer operation from the data set to Serdes and, thence, to the character register is effected in the same manner as for the other characters in the addressing sequence. Once entered in the character register (ring 3 time), the command is decoded by the command decoder shown in Figure 4-20. Assuming that the decoded command is a Write DS or PTR command (FC-101(3)), the command signal is gated out of the command decoder via A3 and A2 by a Char Sent R4 (ring bit 4 time) signal to set the Write latch and the ACK (Acknowledge) response latch via A1 and A4 if no printer is being addressed. This occurs as a result of the Device Address trigger being set, and Test Mode or Check LRC operations are not being performed. The Serdes register is also reset at this time.

With the setting of the Write latch, the I/O Write signal is generated via A6 to the selected 2848 as an indication of the operation that is to be performed by the data set. In addition, a Wr or Wr Line Adr signal is also generated via O2 and routed as a gating signal to those circuits required for processing the data intended to be written on the 2260 Display Station.

At ring bit 8 time, the character register is reset and the output signal from the ACK response latch (Answer ACK) is routed via A2 (Figure 4-21 and FC-102) to set bits 2 and 3 (ACK code) in the character register. The response latch output is also routed as a Reply ACK, NAK, EOT signal to set the Reply (ACK, NAK, EOT) latch. At ring bit 9 time, the Character Sent latch is reset. Since no data has been entered into the delay register up to this time, the output signal from the Write Reply latch, in coincidence with a Delay Register Clear signal, conditions A6 to set the Transmit latch and reset the LRC latch. Setting of the Transmit latch permits the remote interface to transmit the ACK response to the data set as an acknowledgment that the 2848 and 2260 are ready to accept the data to be written.

Remote Interface Response - ACK Character

The ACK response operation (FC-102) occurs in the following manner. The Transmit latch output signal (Transmit) is AND'ed at A3 with a Clear to Send signal (previously generated by the data set when the 2848 was selected) to fire a 17-ms single-shot. Firing of the single-shot provides time for the 2701 to check its Receive line. The Transmit signal is further routed to reset the Text Mode latch and to serve as a blocking signal to inhibit the setting of the Character Sent latch.

The time interval provided by the 17-ms single-shot allows a Transmit Ready signal of 17 ms to be generated via the output of A3, A4, and the single-shot. This signal is AND'ed with signals indicating that the Serdes register is empty and that the character register (CR1) is loaded (bits 2 and 3) to condition A8 and, thus, turn on the Send Data trigger. This trigger is complemented by 78.6-kc pulses from the oscillator; consequently, its output serves as a gating level (approximately 13 μs) to allow the response character to be transmitted to the data set. In addition, the Send Data trigger output signal (Send Data) is routed to set the CR1-Serdes latch at

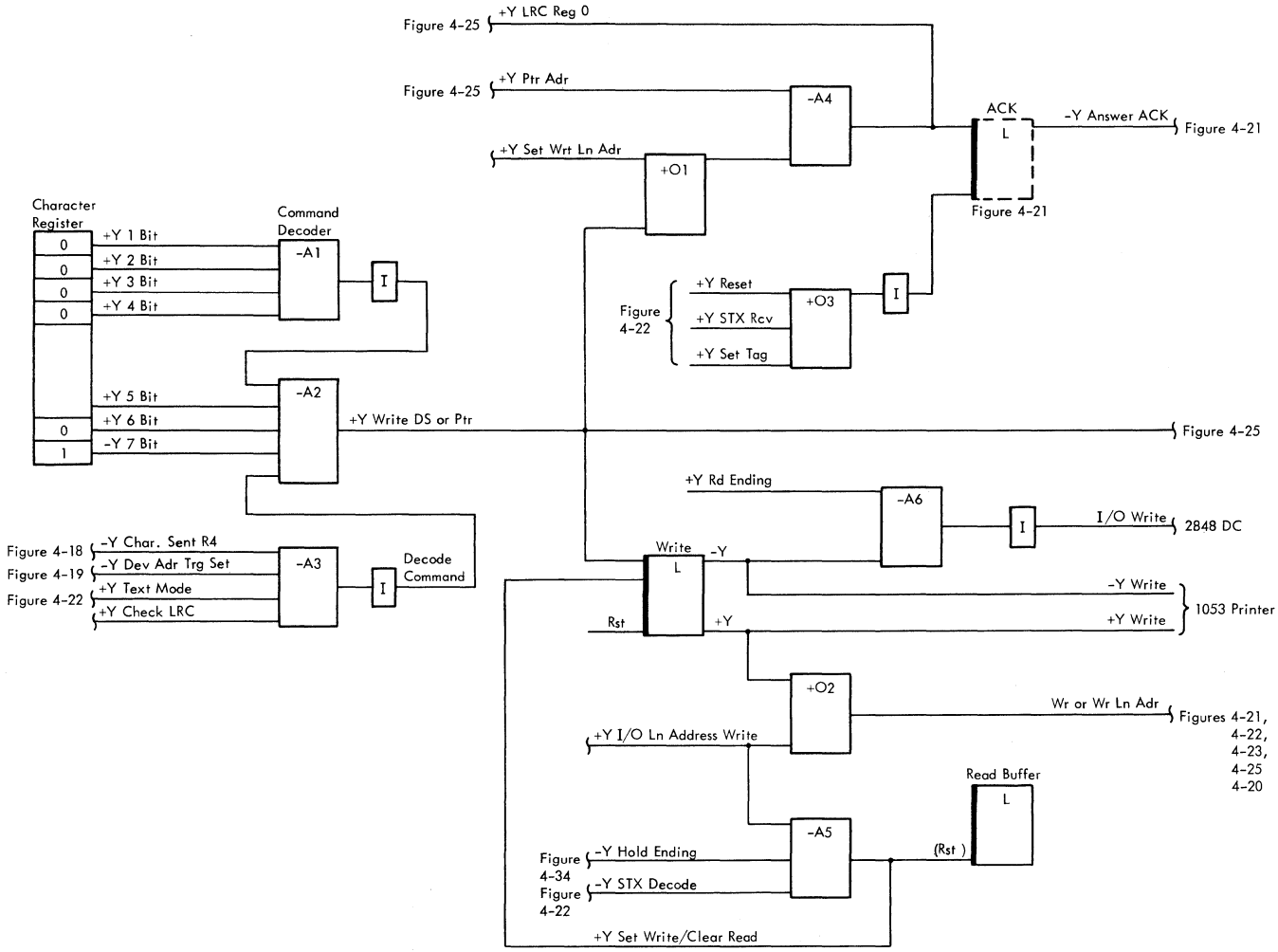


Figure 4-20. Channel Response - Command Character Decode

ring 3 time via conditioned A11 if the Serdes register is empty and the character register is loaded with the ACK character (FC-103). At ring bit 4 time, with the CR1 Serdes latch set, A13 is conditioned and an IO Bfr to Shift Reg signal is generated to shift the ACK response (bits 2 and 3) from the character register to the Serdes register. At ring bit 5 time, A15 is conditioned, and a Set Tag signal is generated to set the Stop bit trigger in the Serdes register and to clear the character register. At ring bit 6 time, A14 is conditioned, and another Set Tag signal is generated to set the Start Bit trigger in the Serdes register. The latter Tag signal is also routed to reset the ACK Response latch at this time. (See Figures 4-20 and 4-22.) At ring bit 8 time, the Serdes Empty latch is reset. At ring bit 9 time, the CR1 Serdes latch is also reset. The ACK response character and its associated tag bits are subsequently shifted out of the Serdes register at a 1.2-kc rate (8.3 ms per character) under control of the Serdes oscillator. The data bits are gated by the Send Data trigger output level at A12 and routed to the data set as EIA Send Data pulses. Thus, the ACK response generated indicates that the 2848 and the addressed 2260 are selected and ready to receive a message from the data set.

At ring bit 2 time following the transfer of characters from the Serdes register, the Send Data trigger is reset via conditioned A9, indicating no further transfer of data to the data set; the Serdes register is also reset before receiving new data from the 2701.

Channel Response - STX Character

Upon receipt of the ACK response, the normal channel response is the following transmission sequence (containing the message to be written on the screen of the selected 2260): STX, text (message to be written), ETX, and the LRC byte.

Upon receipt of the Start bit of the STX character transmitted from the data set, the Character

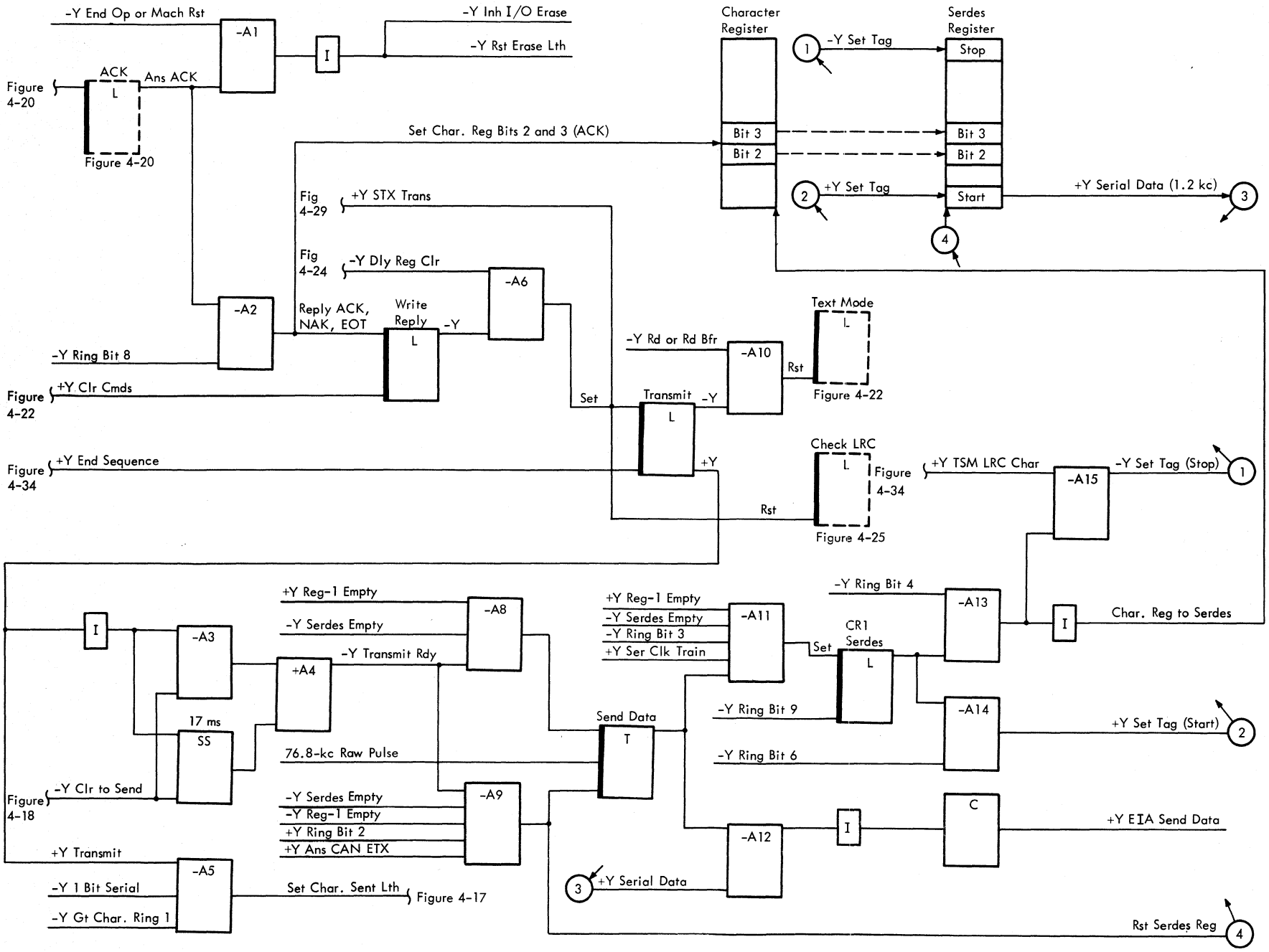


Figure 4-21. Remote Interface Response - ACK Character

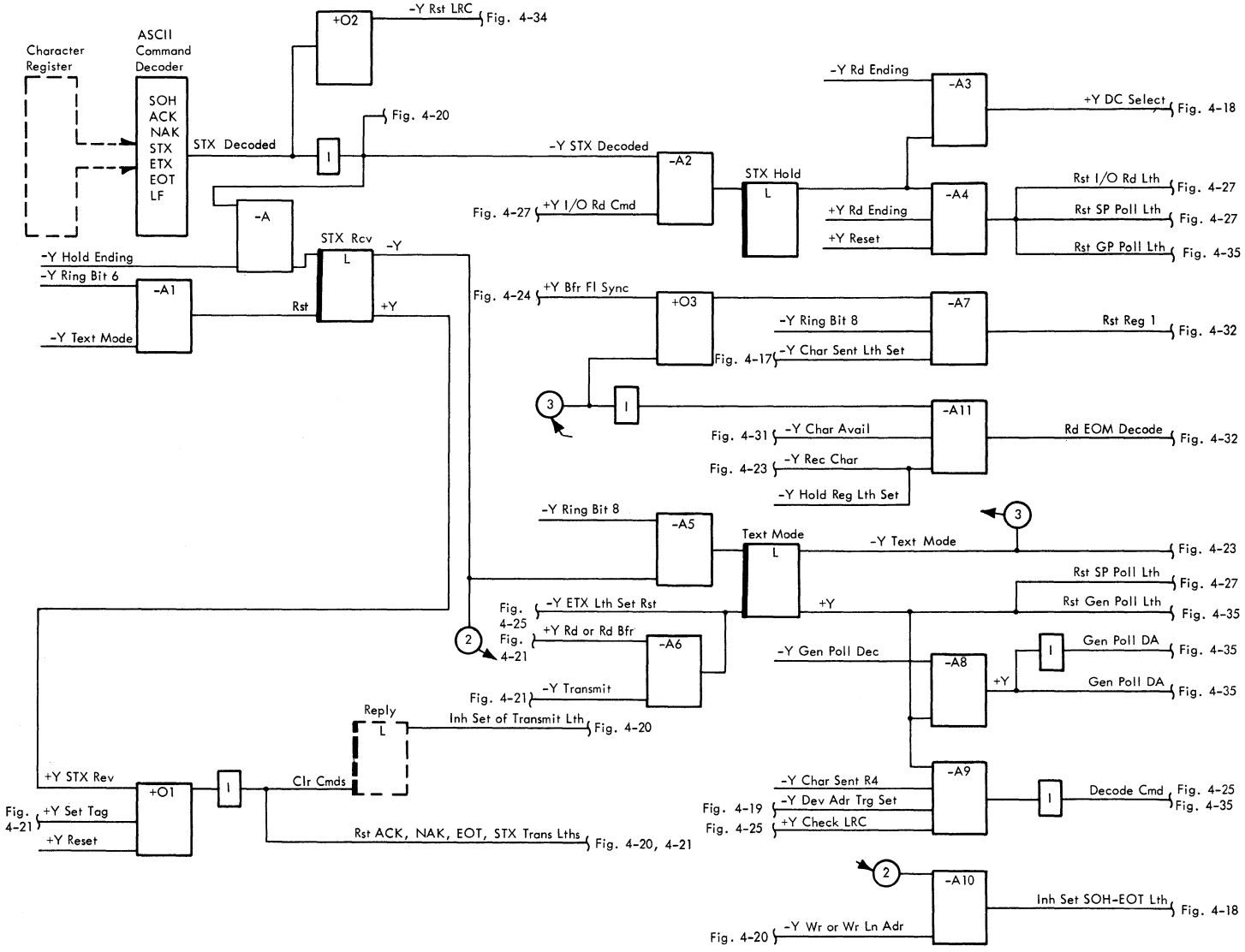


Figure 4-22. Channel Response, STX Character

Sent latch (Figure 4-17) is set. At ring bit 2 time, and with the latch set, the Parity Check latch is reset so that a parity check of the incoming data can be performed. At ring bit 3 time, the STX character is transferred in parallel to the character register to be decoded by the ASCII command decoder.

The STX control character having been decoded (Figure 4-22), an STX Decoded signal is generated to set the STX Rcv latch (FC-105). Since the Write latch (Figure 4-20) was set by the receipt of the command character, its output level (Wr, or Wr Ln Adr Ln) is AND'ed at A10 with the STX Rcv latch output signal (STX Rcv) to inhibit setting of the SOH-EOT trigger. The STX Rcv signal is also routed to reset the ACK, EOT, NAK, STX Transmit, and Reply latches. The latter latch, when reset, ensures that the Transmit latch is not set during the forthcoming operation. (Refer to Figure 4-22.) At ring bit 8 time, the character register is reset (via A7) since the STX is not written on the 2260 display. Also at ring bit 8 time, the STX Rcv signal is gated via A5 to set the Text Mode latch, thus removing the 2848 from Control mode operation and placing it in the Text mode in preparation for receipt of the text data that is to be written on the 2260 display. At ring bit 9 time, the Character Sent latch is again reset, completing the STX character processing operation.

Channel Response - Text Character

The next character to be processed represents the first byte of text data. With the receipt of its Start bit, the Character Sent latch is again set at ring bit 1 time. At ring bit 3 time, the text byte is transferred in parallel into the character register. At ring bit 4 time, the Serdes register is reset. In addition, a Char Sent R4 is AND'ed with the output signal from the Text mode latch and the Write latch (Wr or Wr Ln Adr) to condition the Gate to Delay Line AND 1 gate (Figure 4-23 and FC-106). A Char Sent from Reg 1 signal is derived, which is routed via O1 and A7 to set the Receive Character trigger. With the first character of text contained in the character register, no further operation upon the data is performed for the remainder of the bit ring cycle until the Char Sent latch is reset at ring bit 9 time.

Since the text character is to be routed and entered into the delay line, a search operation of the write marker in the delay line ensues. (See FC-106.) When the write marker is detected at ring bit 2 time of the following ring bit cycle and when the Receive Character trigger is set, A4 is conditioned to set the Start Write latch. The output signal of this latch is AND'ed with the Receive Character and Wr or Wr Ln Adr signals to condition A11 and produce the Serialize Write Data signal. This signal causes the character register data (bits 1 through 7) to be entered into the delay line, under control of the ring bit counter, beginning at ring bit 3 time. At the completion of the data entry operation into the delay line, at ring bit 9 time, and with both the Start Write latch and Receive Character trigger in a set state, a signal is gated by conditioned A12 to set the Continue latch. This latch remains set until both the read and write markers are detected in their respective character positions; at this time, the latch is reset, indicating that the delay line is empty.

The output signal from the Start Write latch is gated at A6 by the presence of the A2 and B Delay signals (500 ns) to complement the Receive Character trigger to its reset state. When this occurs, the reset output signal of the trigger is AND'ed at A10 with the output signal of the Start Write latch (set side) to produce a Write Wrt Marker signal. This signal, in conjunction with the Wr or Wr Ln Adr signal at A14, resets the character register and the Character Available latch.

At ring bit 1 time of the ring bit cycle, with the Start Write latch set, a Write Delay Line signal is generated from conditioned O2 and A9 and routed as a gating level to the Write-1 AND gate (Figure 4-24) in the delay line control circuit. This gate, when conditioned, allows a Write Marker bit to be written in the delay line. At ring bit 2 time, the Write Marker bit signal is gated by conditioned A13 and AND'ed with the Write Delay Line and A2 pulses (500 ns) to insert the Write Marker bit signal 1.5 μs after entry of the text character into the 318-μs delay line.

The delay line entry operation (Write Command) continues until the delay line becomes full. This condition is manifested when the write marker is inserted in a character position that contains a read marker while the Continuous latch (Figure 4-24) is in a set state. As shown in the figure, when the Read Mark latch is set and a Write Wrt Mark signal is generated, A15 is conditioned to set the Buffer Full Sync latch.

As a result, a signal is generated to reset the I/O Request latch and to inhibit the setting of the Start Write latch. This prevents gating of further data into the delay line via the serializer. The output from the Buffer Sync latch is also routed to set the Buffer Full latch. Since a Write command is in progress and the latch is in a set state, A17 is conditioned and a signal is generated to reset the LRC register. Further, the latch output signal is routed to degate A11 and A12, thereby preventing the ACK and NAK response latches from being set, until such time as an LRC check is performed following data entry.

At ring bit 3 time, with the Receive Character trigger in a reset state, A5 is conditioned to reset

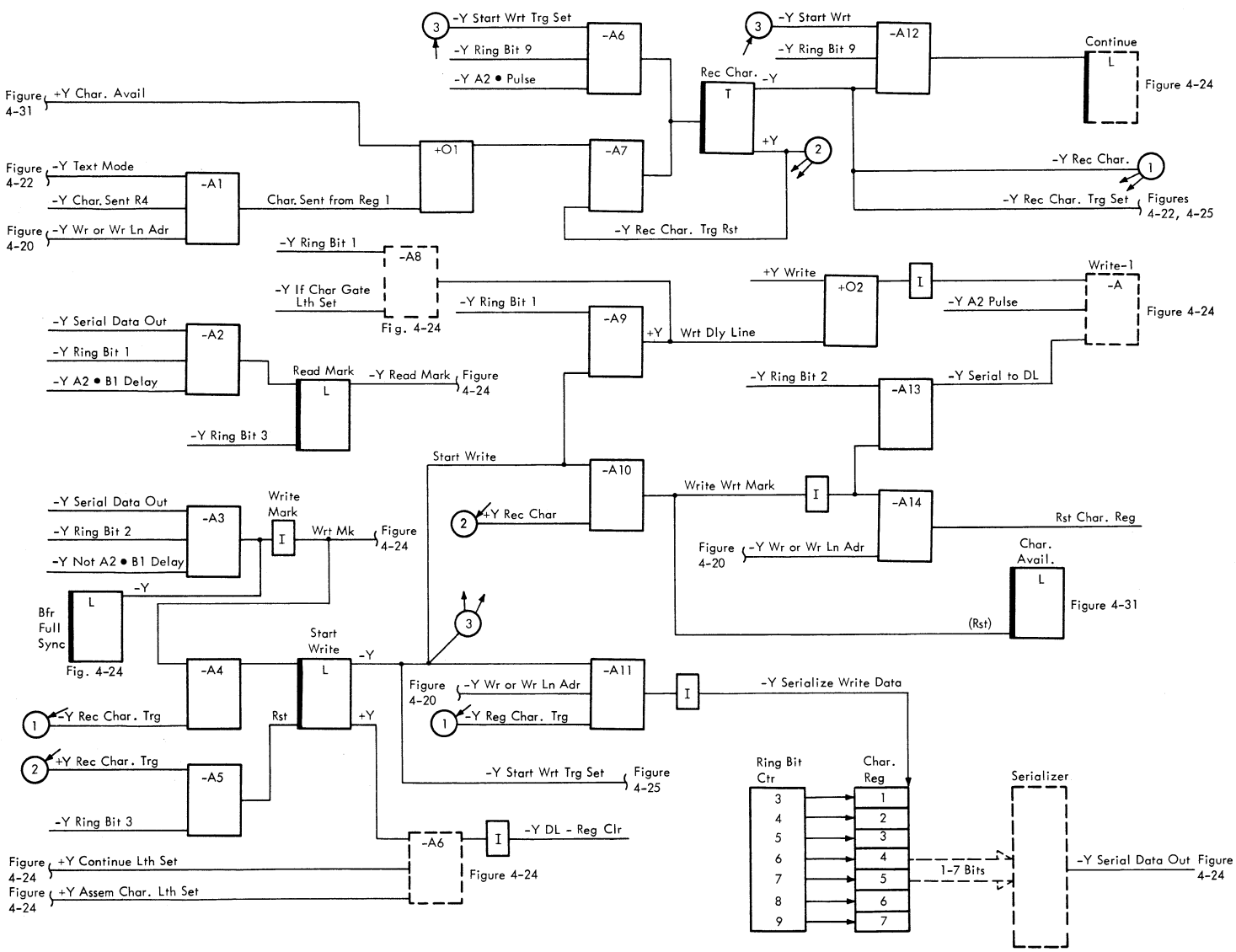


Figure 4-23. Channel Response, Text Character

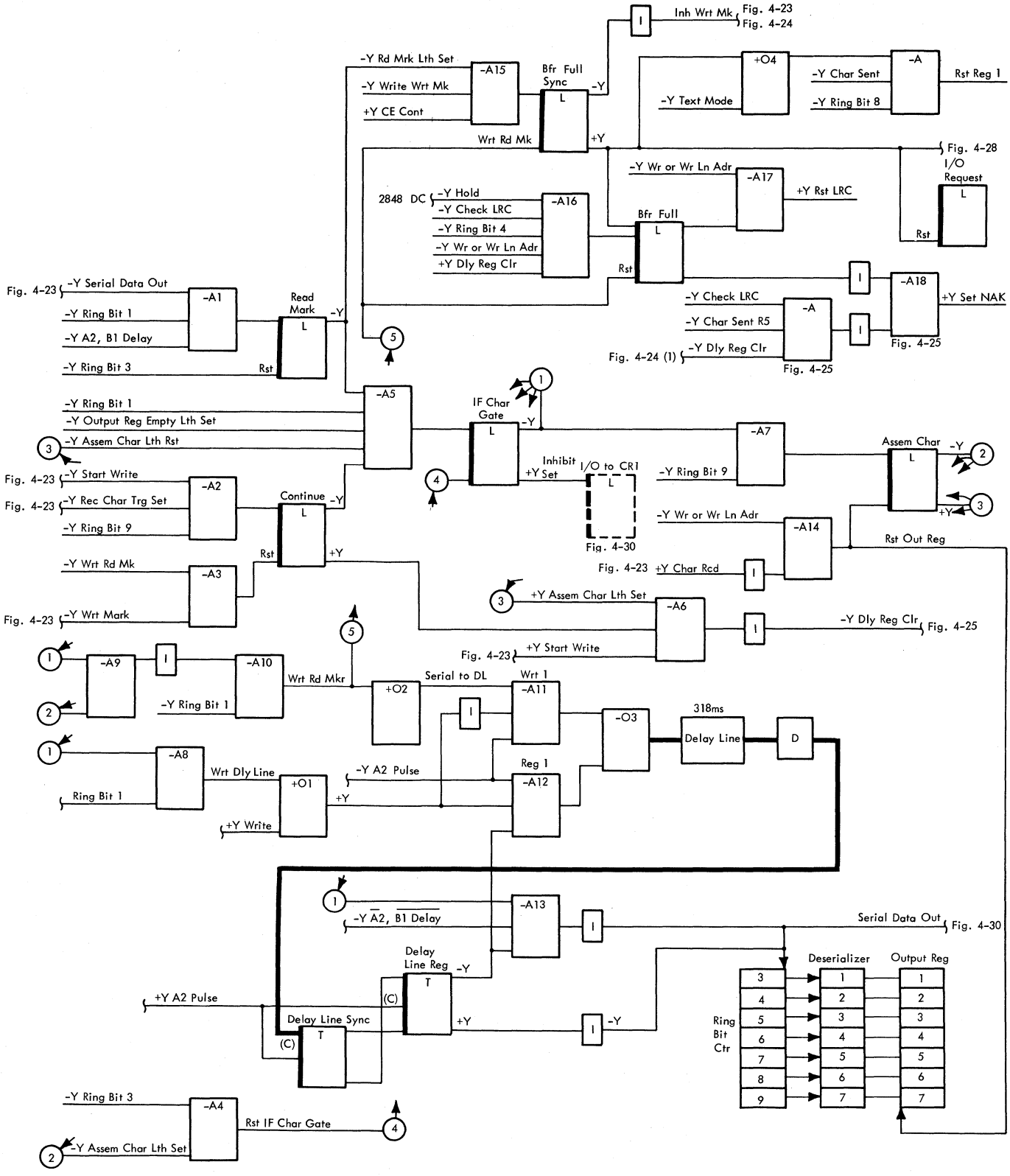


Figure 4-24. Delay Line Readout Control

the Start Write latch, in anticipation of the receipt of the next character of text to be processed.

Delay Line Readout - Write Operation

The delay line used in the remote interface is a Return-to-Zero (RZI) type as opposed to the Non-Return-to-Zero (NRZI) type delay lines used in the display adapter. The length of the line is 317.6 μs; the line has a capacity of approximately 315 bits. Each character stored in the delay line requires nine bits, hence, 35 characters can be stored in the delay line. Bit entry into or exit out of the delay line is controlled by the nine-bit ring counter at a rate of 1.0 μs/per bit. The format of the delay line character is as follows:

Character Bit Position	1	2	3	4	5	6	7	8	9
	Read Marker	Write Marker	B1	B2	B3	B4	B5	B6	B7

For brevity, the following discussion relates to the processing of one character of text from the delay line to the output register (see Figure 4-24 and FC-107). Once entered into the delay line, the character is regenerated within the delay line until its associated Read Marker bit is detected. When this occurs, at ring bit 1 time, the Read Mark latch is set via conditioned A1. The Read Marker signal is AND'ed at A5 with the following set of signals: Continue Latch Set, Output Reg Empty, Assemble Character Latch reset, and Ring Bit 1 to set the IF Character Gate latch. The output signal from this latch is routed to A13 as a gating level to allow the character bits from the Delay Line Register trigger to be gated out by NOT A2 and B1 Delay Line pulses as serial data to the deserializer and output register. At ring bit 1 time and with the IF Character Gate latch set, A8 is conditioned to produce a Write Delay Line signal which is routed to inhibit regeneration of the Read Marker by deconditioning A12. At ring bit 3 time, the Read Mark latch is reset, and the first character bit is read out to the deserializer and output register. At the completion of the character readout operation, at ring bit 9 time, the Assemble Character latch is set via A7. The output of this latch, in conjunction with the output of the IF Char Gate latch at A9, produces the Read Mark signal. At ring 1 time, the Read Mark signal is gated by A10 (to reset the Buffer Sync and Bfr Full latches) and is routed via O2 to the Wrt-1 AND gate. Since the IF Char Gate latch is set during this ring bit time, A8 is conditioned, and its output level is routed (via OR 1) to the Wrt-1 AND gate. With the presence of two conditioning levels, the Read Marker bit is inserted into the delay line upon receipt of the A2 pulse (500 ns). Thus, the character having been read out of the delay line, the Read Marker bit is inserted in its respective ring bit 1 time position 500 ns after the last bit of the character was read out. At ring bit 3 time, with the Char Assemble latch set, A4 is conditioned, and a signal is generated to reset the IF Character Gate latch. When this occurs, the Wrt-1 AND gate is deconditioned and a conditioning level from A8 is routed to the Reg-1 AND gate. Since only one character was entered into and read out of the delay line, only the Read and Write Marker bits are present in the delay line at this time; these are regenerated until new data is introduced into the delay line.

Deserializer and Output Register Transfer - Write Operation

The data bits emanating from the delay line as Serial Data Out signals are entered (in serial fashion) into the deserializer. (See Figure 4-24.) The latter comprises seven AND gates, which are conditioned by the Serial Data Out signals in coincidence with the various Ring Bit Time signals. Following the generation of an I/O Request, the data entered into the deserializer is transferred in parallel to the output register. The parallel data transfer from the deserializer is effected, at a 1-μs rate, under control of the ring bit counter; the first bit of the character is entered at ring bit 3 time, and the seventh bit is entered at ring bit 9 time, completing the transfer operation. The data entered into the output register is supplied directly to the common buffer register of the 2848. Once the common buffer acknowledges receipt of the character, a Character Received signal is transmitted to the remote interface; this resets the I/O Request latch (FC-107). Since the Write latch is still set at this time, its respective output signal is AND'ed with the Character Received signal at A14 to reset the output register. An I/O Request signal is sent to the 2848 every time a character is presented to the CBR from the output register. When the 2848 gates the character into the CBR, it then responds with a Character Received signal.

Channel Response - ETX Character

At the conclusion of the text transmission operation to the remote interface, the data set transmits an ETX control character as an indication (FC-101(1)). Upon receipt of the Start bit of the ETX character in the Serdes register, the Character Sent latch is set (see Figure 4-17). At ring bit 2 time, with the latch set, the Parity Check latch is reset so that a parity check of the character can be performed. At ring bit 3 time, the ETX character is transferred

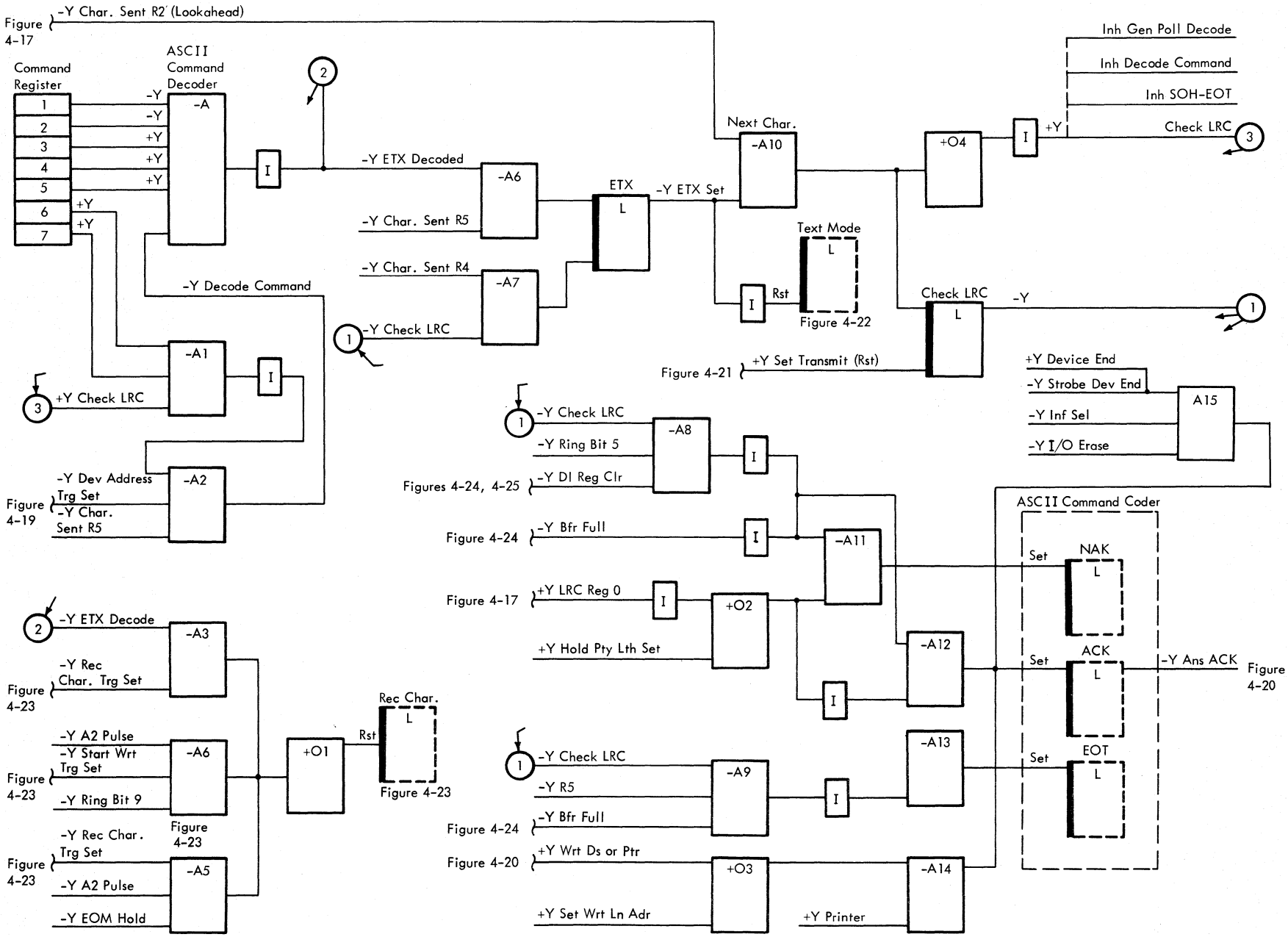


Figure 4-25. Channel Response - ETX and LRC Character

(in parallel) to the character register for subsequent decoding by the ASCII command decoder (Figure 4-25). At ring bit 4 time (Figure 4-23), a Char Sent R4 signal is generated to reset the Serdes register; since the remote interface is in Text mode, and since the Write latch is set, the signal is AND'ed with the signals of the respective latches to condition the Gate to DL gate (Figure 4-23). The output signal from this gate (Char Sent from Reg 1) is routed and AND'ed with the reset output signal from the Receive Character trigger at A7 to set the trigger (FC-106(1)). At ring bit 5 time (see Figure 4-25), the ETX character is decoded by the ASCII command decoder, and an ETX Decoded signal is generated via A6 to set the ETX latch. In addition, the signal is AND'ed at A3 with the set output signal of the Receive Character trigger to reset the trigger. The set output signal (EXT Set) from the ETX latch is sent to reset the Text Mode latch and is sent to the Next Character gate (A10) as a gating level. Since the remote interface is no longer in Text mode, and since the Character Sent latch is set, at ring bit 8 time, the Character register is reset preparatory to receiving the LRC character from the 2701 via the data set. At ring bit 9 time, the Character Sent latch is again reset, completing the ETX control character processing operation.

Channel Response - LRC Character

Following transmittal of the ETX character, the 2701, via the data set, transmits its LRC character for comparison with the LRC byte accumulated in the LRC register of the remote interface. The operation commences with the entry of the LRC byte into the Serdes register (Figure 4-15). When this occurs, the Start bit of the character causes the Character Sent latch to be set at ring bit 1 time. At ring bit 2 time, a Character Sent R2 signal is generated and routed as a Lookahead signal (Figure 4-25) to sense the Next Character AND A10 gate. Since a gating level from the ETX latch is present at the gate at this time, the Next Character gate is conditioned; as a result, a signal is generated to set the Check LRC latch (FC-108). Thus, the Lookahead signal establishes that the character currently being entered in the Serdes register is the LRC accumulation check byte. The conditioned gate also routes a signal (Check LRC) via O4 to inhibit the conditioning of the SOH-EOT, Gen Poll Decode Command AND gates. At ring bit 3 time, the LRC byte is transferred from Serdes to the character register for the LRC accumulation check. Once entered in the character register, the LRC byte from the 2701 is compared with the LRC byte contained in the LRC register of the remote interface. At ring bit 4 time, the Serdes register is reset. Also, a Character Sent R4 signal, in coincidence with the set output signal from the Check LRC latch, conditions gate A7 to reset the ETX latch. Since no data has been entered in the delay line up to this time, a Delay Reg Clear signal is AND'ed at A8 with the set output signal from the Check LRC latch and with Ring Bit 5 to sample the results of the LRC compare operation (FC-108). If a successful compare of the LRC register contents is obtained, an LRC Reg 0 signal is generated via O2 and A12 to set the Acknowledge latch. If the compare operation is unsuccessful, a Not LRC Reg 0 signal is AND'ed at A11 with the sample signal to set the Negative Acknowledge latch.

At ring bit 8 time, the character register is reset, and the output signal from the ACK response latch (Answer ACK) is routed to set bits 2 and 3 (ACK Code) in the character register for eventual transmission to the data set as an indication that the text message was received correctly. (See Figure 4-20 and 4-21.) The ACK response operation that ensues is similar to that described in the paragraph entitled "Command-Write Address DS."

Channel Response - EOT Character

The channel responds to the ACK response generated from the remote interface with an EOT communication control character (to terminate the Write operation). Upon receipt of the Start bit of the EOT character in the Serdes register (Figure 4-17), the Character Sent latch is set. At ring bit 2 time, the Parity Check latch is reset. At ring bit 3 time, the character is transferred to the character register. Now refer to Figure 4-18 and FC-101. At ring bit 4 time, a Character Sent R4 signal is AND'ed at A3 with the SOH-EOT Decode signal to set the SOH-EOT Detect latch. Also, this signal (DC Sel Rst) is routed to reset the EIA Request to Send, SOH-EOT, DC Select and Device Address triggers, thereby releasing the selected 2848 and the associated 2260. At ring bit 5 time, a Character Sent R5 signal is AND'ed at A4 with the decoded (SOH-EOT) signal to set the SOH-EOT trigger again. At ring bit 7 time, the character register is reset, causing A4 to be deconditioned and the SOH-EOT trigger to be reset. At ring bit 8 time, the output signal from the SOH-EOT Detect latch is gated at A6 to fire a 1-ms single-shot, the output of which is used as a general reset signal that is routed to the control circuits of the remote interface. At ring bit 9 time, the Character Sent latch is reset, thereby terminating the operation of the remote interface.

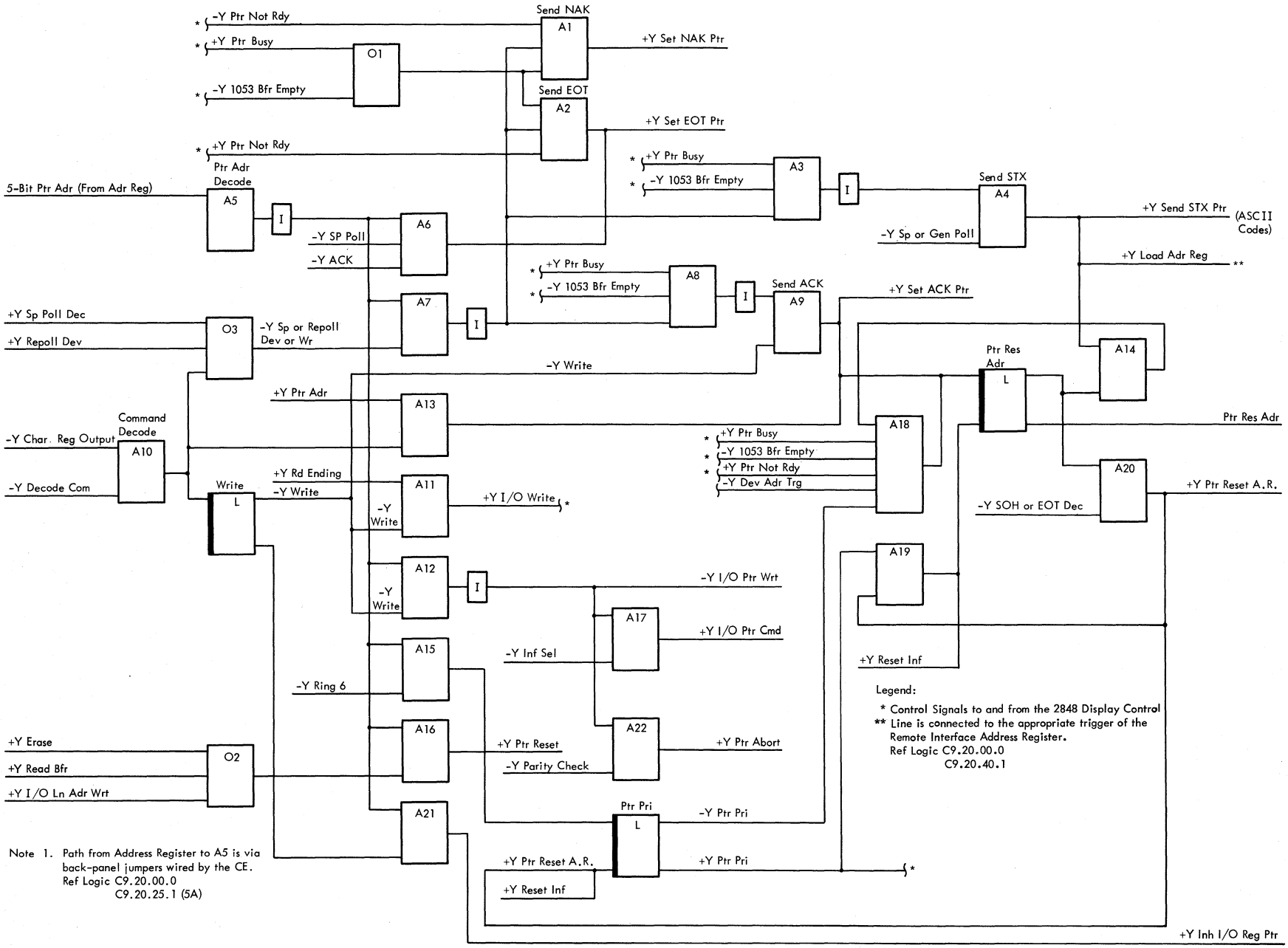


Figure 4-26. Write Printer Control

Command - Write Printer

The channel issues the Write Printer command as the fourth byte of the normal address sequence when it has data to be written in the 1053 Printer buffer. The operation of the remote interface adapter during execution of the Write Printer command is similar to the adapter's response to the Write Addressed DS command. This similarity is illustrated in the sequence/response diagrams for the Write Addressed DS command (Figure 4-10) and for the Write Printer command (Figure 4-12). In these two figures, note that the only difference is in the 2848's initial response to the two commands. For the Write Printer command, this initial response includes provisions for indicating printer status to the channel. Thereafter, both commands result in an identical transfer of the input message. The required responses between the 2848 and the channel remote interface adapter are the same as for a Write Addressed DS command, which has already been discussed in detail. Therefore, the discussion of the Write Printer command is limited here to a description of the unique portions (initial selection) of the operation. Adapter operation from the receipt of SOH to the end of the write printer sequence (Figure 4-12) can be reviewed by rereading that portion of the "Write Addressed DS" description.

The adapter printer operation control logic is illustrated in Figure 4-26. Note that many of the control inputs to the adapter logic originate in the common control area of the 2848; these signals are identified by asterisks.

Address Sequence

The address sequence for the Write Printer command consists of four bytes, as follows:

1. SOH
2. 2848 address
3. Printer address
4. Write printer command

The effect of the SOH and 2848 address bytes of the addressing sequence is the same as that already described in conjunction with the Write Addressed DS command. The printer address and printer command bytes are decoded and used to activate the adapter printer control logic, as described in the following paragraph and illustrated in FC-109.

Initial Adapter Response

Printer Ready and Not Busy

In Figure 4-26, note that the printer address is decoded at A5 and that the path from the address register to A5 is via back-panel jumpers wired by the CE. Also note that the printer command is decoded at A10. Once the printer address is decoded, the inverted output of A5 partially conditions AND circuits A6, A7, A12, A15, A16, and A21.

At ring 6 time, A15 is fully conditioned, and its output sets the Ptr Pri latch. (The significance of the Ptr Pri latch is discussed later.) Note that the reset status of the Write latch at this time conditions A21 and ensures that the I/O request is not made to the 2848 common area until the Write latch is set to indicate that an I/O operation is to be performed.

Next, the command byte of the address sequence is decoded. If a Write Printer command is present, A10 is conditioned. Its output conditions OR3 and sets the Write latch. With OR3 conditioned, all required inputs to A7 are present. Thus, A7 produces an output which is inverted to partially condition A1 and A2. AND circuits A1 and A2 also receive inputs which indicate the status of the printer from the printer logic of 2848 common control.

If the printer is not ready (nonoperational), A1 is conditioned, and a NAK response is issued to the channel. (See FC-109.) If the printer is busy, A2 is conditioned, and an EOT response is issued to the channel.

If the printer is ready (operational) but is busy (OR1), A2 is conditioned, and an EOT response is sent to the channel. Thus, A1 and A2 are the source of the printer status-oriented response shown in the Write Printer Sequence response diagram provided as Figure 4-12.

If the printer is ready and not busy, an ACK response to the channel must be initiated. This is accomplished at A9. Since the Write latch was set when the Write Printer command was decoded, A9 is partially conditioned. In Figure 4-26, it is seen that A8 is also conditioned. Thus, the ACK latch of the ASCII coder is set (A9), and the Ptr Hold latch is set.

The output of the Write latch also completes the conditioning of A11 and A12. The I/O Write signal from A11 is routed to 2848 common to identify the impending operation.

The output of A12 causes A17 to be conditioned, thus providing the I/O Ptr Cmd signal to 2848 common, enabling it to configure the common area for a printer operation. The output of A12 is also used to generate the I/O Ptr Wrt signal, which sets the I/O Request latch (see "Write Addressed DS" discussion). AND circuit A22 is also held partially conditioned and remains in this status throughout the write printer operation unless a parity check occurs. If a parity check does occur, A22 is fully conditioned, and the print operation is aborted; i.e., the input data is accepted but is not written in the 1053 Printer buffer.

Printer Busy

If the printer is busy when it is addressed by the channel, the initial response of the 2848 is limited to the generation of EOT from AND circuit A2, as described earlier. However, remember that the Ptr Pri (printer priority) latch was set (A15) as soon as the printer address was decoded. In Figure 4-26, note that A18 will be fully conditioned as soon as the printer is ready and not busy. Then, the Ptr Res Adr latch is set by the output of A18. Once set, the Ptr Res Adr latch prevents all keyboards of the 2260's associated with the 2848 from issuing a print command and causing the printer to be busy. In effect, the printer is reserved for the channel. The next command issued by the channel must be for the use of the printer, or the Printer Reset Address latch is reset (+Y Reset Inf), and the 2260 keyboards are permitted to use the printer.

If the channel uses its printer reservation, the Write Printer command is executed in the normal fashion. Then, at the end of the operation, the Ptr Pri latch is reset (+Y Ptr Reset A. R. input to latch from A20).

Data Transfer

Once the 2848 has made an initial response and this response has indicated that the printer is available (ACK response), the channel responds with STX, the message text, EXT, and LRC. (See Figure 4-12 and FC-109.) This data is accepted as described for the identical channel response that forms part of the Write Addressed DS operation (Figure 4-10).

The printer logic is activated upon receipt of an SOH or EOT at the end of the write printer operation. In Figure 4-26, note A20. When SOH or EOT is decoded, A20 is conditioned, and the address register is reset. Once the printer address is no longer in the address register, A5 is deconditioned, and the adapter printer logic is deactivated.

Address Sequence - Read Operation

The addressing sequence required to perform a read operation is identical with that described for a write operation. Refer to the paragraph entitled "Address Sequence - Write Operation."

Command - Specific Poll to 2260 DS

The Specific Poll is directed to a particular 2260 Display Station; it tests for the presence of a manually entered message awaiting transfer to the channel. If a message is present on the queried 2260 Display Station, the command effects the transfer of the message to the initiating channel.

The Specific Poll command to a selected 2260 causes the associated 2848 to test for the following conditions:

1. Enter key is depressed.
2. Start symbol is displayed.

If both conditions are present, the 2848 transmits the STX line control character, the address of the selected 2260, and all character data displayed between the start symbol and the EOM. A detailed description of the aforementioned sequence of events is presented in the following paragraphs.

2848 DC Response - STX Character

The sequence/response diagram for a Specific Poll to 2260 DS command is shown in Figure 4-6. As illustrated, the addressing sequence that occurs for this command is similar to that described for a write operation. Thus, further discussion of the addressing sequence is unnecessary.

Upon receipt of the Specific Poll command by the remote interface, the command character is routed, via the Serdes and character registers, to the command decoder (refer to Figure 4-27 and FC-101(3)). Once the character is decoded, an SP Decode signal is generated by the decoder and sent to set the Specific Poll latch. The latch output signal (SP or Gen Poll) is routed as a gating level to condition Poll gate A6, the output of which sets the I/O Request latch (Figure 4-28 and FC-110). Setting the latch causes an I/O Request signal to be generated and sent via OR1 to determine whether the Enter key of the polled 2260 is depressed.

Assuming the Enter key of the polled device is depressed, the 2848 immediately proceeds to generate an STX character and transfer the address of the polled device to the remote interface. This operation is initiated when, as a result of the Enter key being depressed, a Set Attention signal (FC-110(2)) is sent to the remote interface to condition A2, the output of which is used to set the I/O Read latch. With the latch in a set state, A4 is deconditioned, and an I/O Read signal is generated. This signal, which deconditions A5 and Poll gate A6, is routed to the 2848 as notification that a Read operation is to occur.

The Set Attention signal is also sent as a gating level (Load Address Reg) to enable the address of the polled device entered in the address register (Figure 4-30) to be transferred from the register into the output register. In addition, the Set Attention signal is AND'ed at A1 (Figure 4-29) with the reset signal of the Start Read latch, conditioning A1. The output signal from AND A1 sets the Start Read trigger; this signal is also routed as an STX

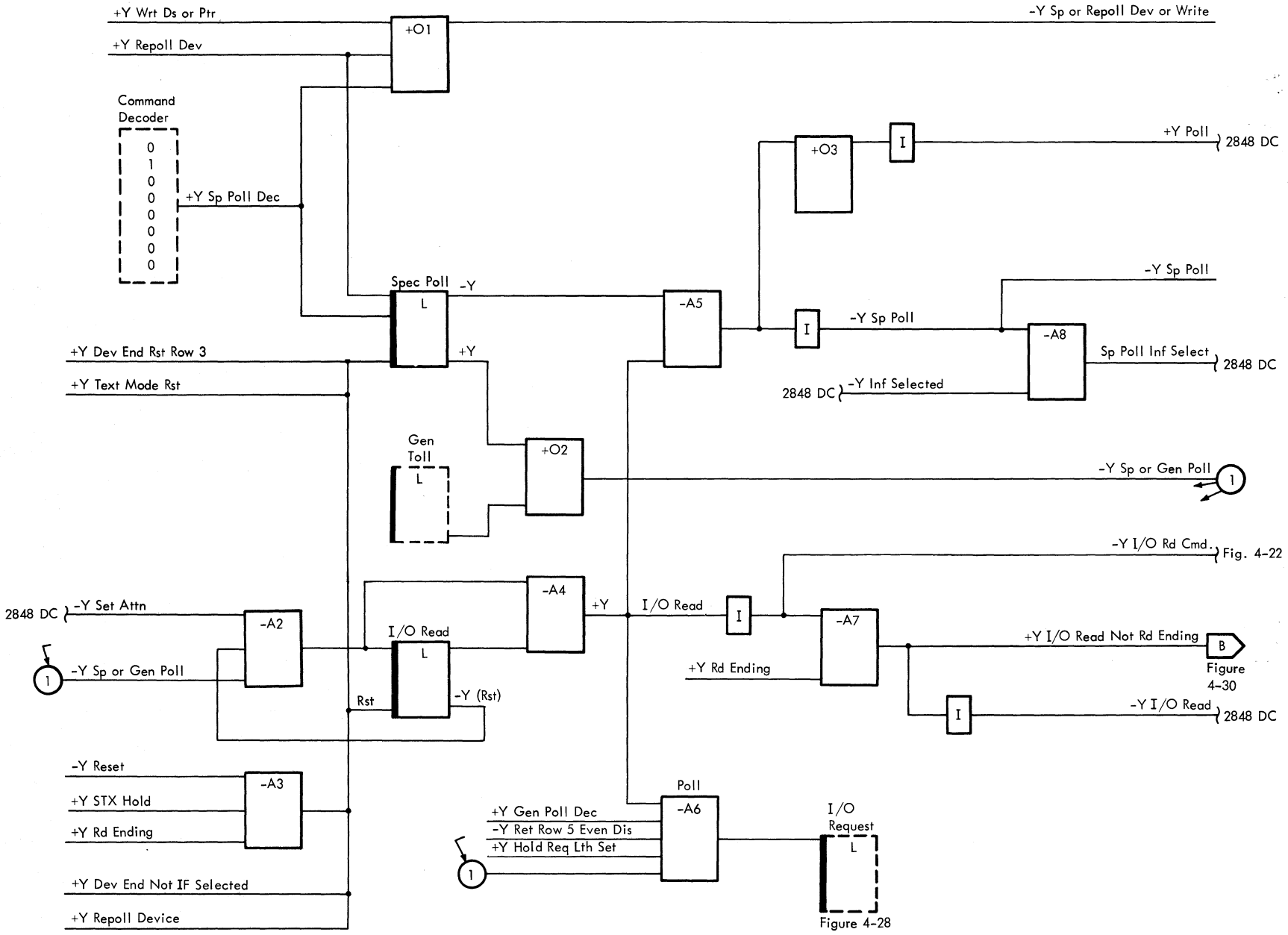


Figure 4-27. Specific Poll Command Decode

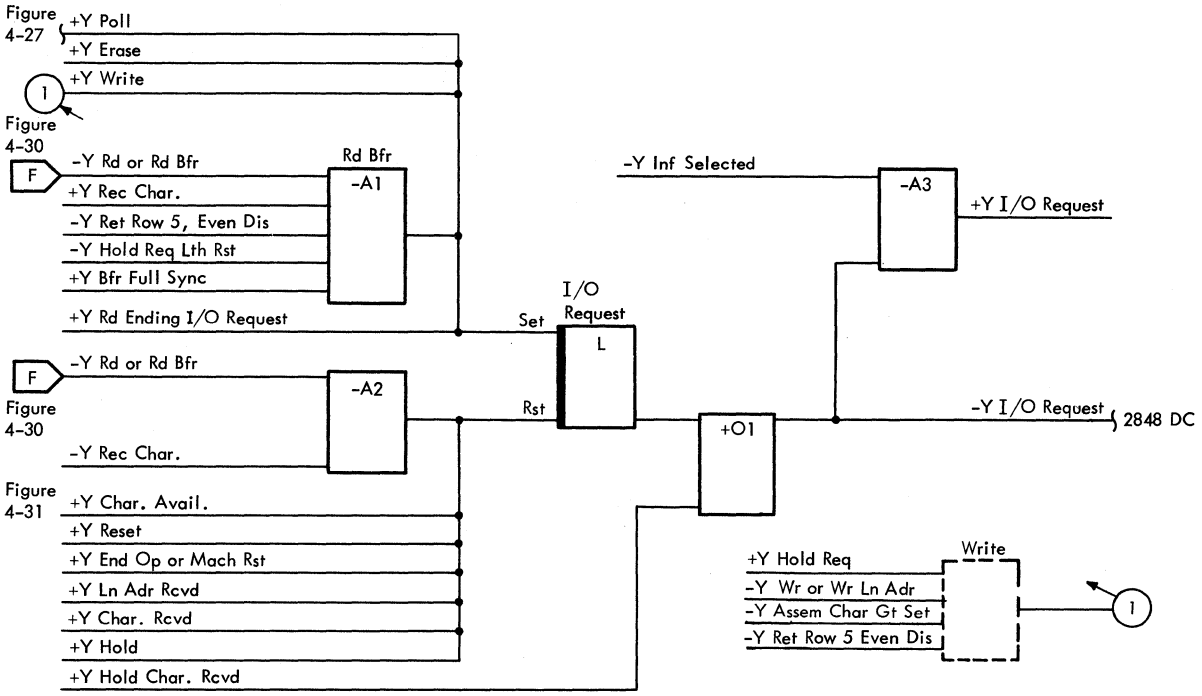


Figure 4-28. I/O Request Control

Trans signal to set both the STX Transmit latch (Figure 4-29) and the Transmit latch (Figures 4-21 and 4-29). In addition, the signal is sent to set the Bit 2 latch in the character register, in effect placing the STX character (0100000) transmitted from the 2848 into the character register (FC-111). The STX transfer operation occurs in the following manner.

Refer to Figure 4-21 and FC-102. Once the Transmit latch is set, its output signal is AND'ed at A3 with a Clear to Send signal (previously generated by the data set when the 2848 was selected) to fire a 17-ms single-shot. Firing the single-shot provides time for the 2701 to check its Receive line. The Transmit signal is also routed to reset the Text Mode latch and to serve as a blocking signal to inhibit setting of the Character Sent latch.

The time interval provided by the 17-ms single-shot allows a Transmit Ready signal of 17-ms duration to be generated (via the outputs of A3, A4, and the single-shot). This signal is then AND'ed at A8 with signals that indicate that the Serdes register is empty and that the character register is loaded with the STX character (bit 2) to turn on the Send Data trigger. This trigger is complemented by 78.6-kc pulses from the oscillator. Consequently, its output signals serve as gating levels (13 μs duration) to allow the STX character to be transmitted to the data set. The Send Data trigger output signal (Send Data) is routed to set the CR1-Serdes latch at ring bit 3 time, via conditioned A11, if the Serdes register is empty, and the Character register is loaded with the STX character (FC-103). At ring bit 4 time, with the CR1-Serdes latch set, A13 is conditioned, and an I/O Bfr to Shift Reg signal is generated to shift the STX character (bit 2) from the character register to the Serdes register, A15 is conditioned, and a Set Tag signal is generated to set the Stop bit trigger to the Serdes register and to clear the character register. Also, the Set Tag signal is AND'ed with the output of the STX Trans latch at A5 (Figure 4-29) to reset the LRC register. At ring bit 6 time, A14 (Figure 4-21) is conditioned, and another Set Tag signal is generated to set the Start bit trigger in the Serdes register and to reset the character register. The latter tag signal is also routed to reset the STX Transmit latch (Figure 4-29). At ring bit 8 time, the Serdes Empty latch is reset. At ring bit 9 time, the CR1-Serdes latch is also reset. The STX character and its associated tag bits are subsequently shifted out of the Serdes register at a 1.2-kc rate (8.3 ms per character) under control of the Serdes oscillator. The STX data bits are gated by the Send Data trigger at A12 (Figure 4-21) and routed to data set as EIA Send Data pulses. This terminates the STX character transmission by the 2848 in response to a Specific Poll command.

2848 DC Response - 2260 DS Address

The second character of the 2848 response to the Specific Poll command represents the address of

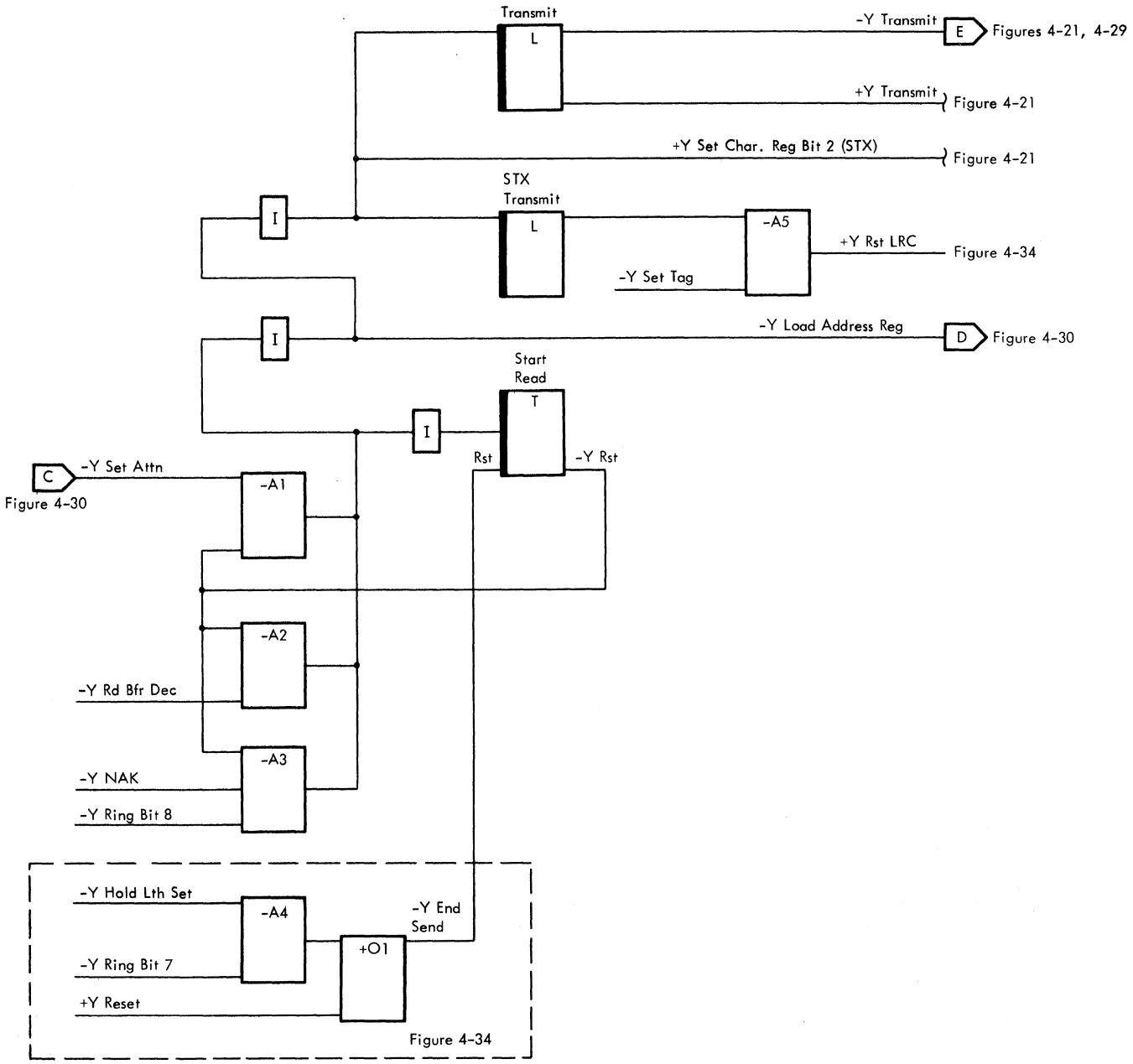


Figure 4-29. 2848 DC Response - STX Character

the 2260 display that was specifically polled. Upon the receipt of the Set Attention signal by the remote interface, the address of the device that is polled is gated into the address register (Figure 4-30 and FC-110, -111) of the remote interface.

The content of the address register is gated into the output register by the Load Address Reg signal, which was generated upon receipt of the Set Attention signal.

Since the I/O Read latch is set at this time, an I/O Rd, Not Rd Ending signal is AND'ed at A2 (Figure 4-30) with a signal indicating that Reg-1 is empty, the IF Char Gate latch is reset, and the Output Reg is not empty. At ring bit 3 time, A2 is conditioned to set the I/O to CR1 latch (FC-104), and Bit 1 in the output register remains reset. At ring bit 4 time, bit 2 in the output register remains reset. At ring bit 5 time, with the I/O to CR1 latch set, A4 is conditioned and a Gate I/O to CR1 signal is generated to gate the device address stored in the output register to the character register. Note that the output register bit 1 is transferred to the bit-7 position in the character register. This is because the 2848 common control uses the EBCDIC code (six bits, 2 through 7), with bit 2 the high-order bit. ASCII uses a seven-bit code (1 through 7), with bit

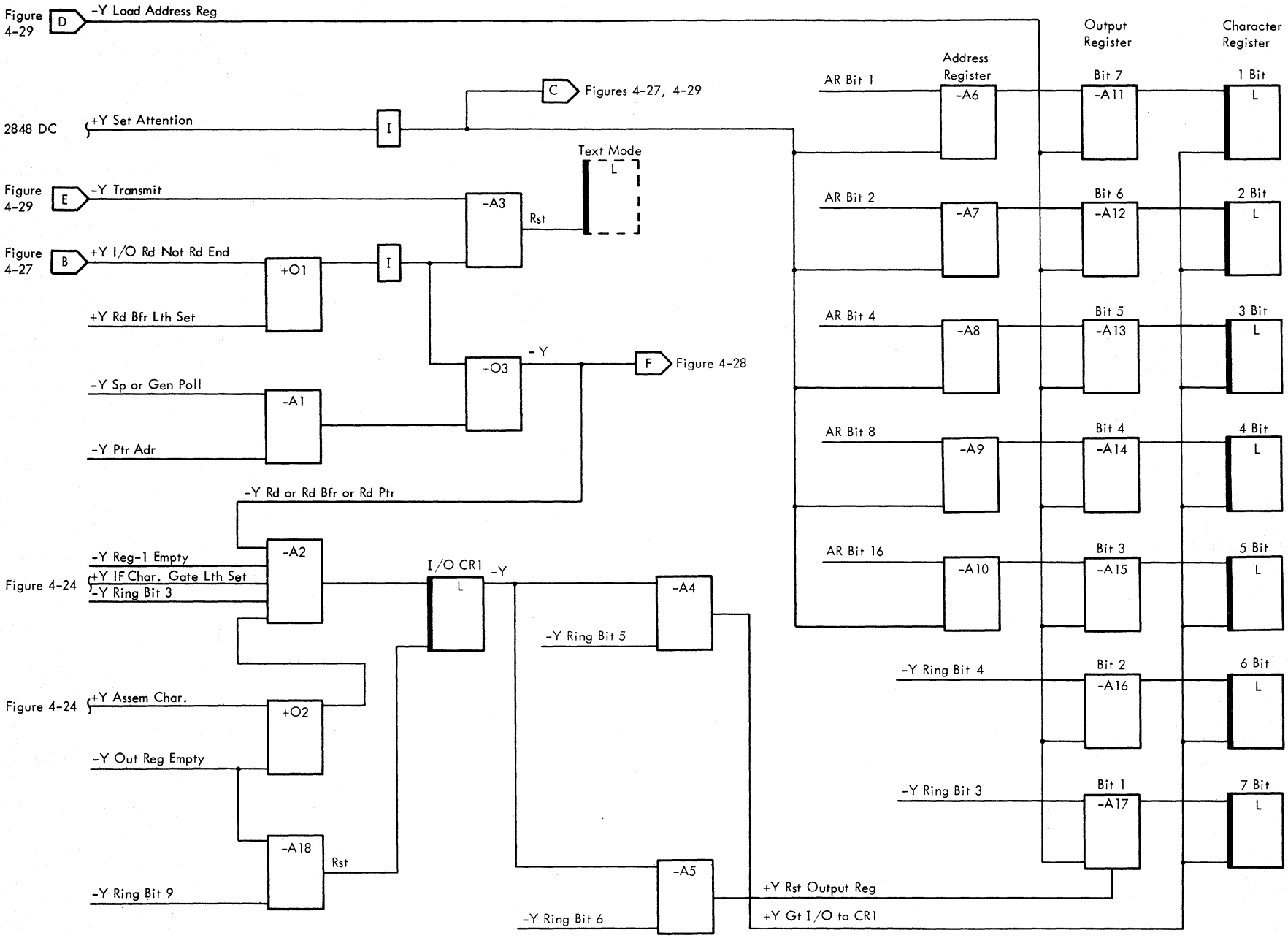


Figure 4-30. 2848 DS Response - Device Address

7 the high-order bit. At ring bit 6 time, with the I/O to CR1 latch set, A5 is conditioned, and its output resets the output register. Once entered in the character register, the address is shifted into the Serdes register in the manner described for the STX character.

2848 DC Response - Text Character

Following transmittal of the STX character and device address of the specifically polled device, the remote interface generates an I/O Request to the 2848. When the 2848 has presented the first character of text to the input of the serializer, the 2848 sends a Character Sent signal to the remote interface (FC-112). The signal sets the Character Available latch (Figure 4-31) as notification that a character of data has been transmitted to the remote interface. The output signal from the conditioned latch (Char Avail) is routed to reset the I/O Request latch (Figure 4-28) and to set the Receive Character trigger via A7 (Figure 4-23). In addition, the Char Avail signal provides the gating level required to transfer the text character data stored in the serializer of the remote interface into the delay line. This terminates the first request for a data character by the remote interface. The I/O Request latch is set for each character of text that is requested from the 2848.

When the I/O Request operation is complete, and the first text character is entered into the delay line, the remote interface conducts a search operation for the Write Marker bit in the delay line (FC-106). The operation is as follows:

When the Write Marker bit is detected at ring bit 2 time (refer to Figure 4-23), and with the Receive Character trigger is in the set state, A4 is conditioned to set the Start Write latch. At ring bit 3 time, the first bit of the text character (Figure 4-31) data is gated out of the serializer into the delay line. The remaining data bits are gated out with each subsequent count of the ring bit counter. At the completion of the data entry operation into the delay line, at ring bit 9 time, and with both the Start Write latch and Receive Character trigger in a set state, A12 becomes conditioned to set the Continue latch. This latch remains set until both the Read and Write markers are detected in their respective character positions. When this occurs, the latch will be reset, indicating that the delay line is full; no further data can be entered.

In addition, the output signal from the Start Write latch is AND'ed at A6 with a Ring Bit 9 signal and with A2 B Delay signals (500 ns) to complement the Receive Character trigger to its reset state. When this occurs, the reset output signal of the trigger is AND'ed at A10 with the output signal of the Start Write latch (set side) to provide a signal that resets the Character Available latch, inhibiting any further data bit transfer from the serializer.

The following discussion relates to the processing of only one data character into the delay line. Since one character has been entered into the delay line during one ring bit cycle, provision must be made at this time to reinsert the Write Marker bit into the delay line (FC-106). This operation commences at ring bit 1 time of the following ring bit cycle, with the Start Write latch set, at which time a Write Delay Line signal is generated from conditioned A9 and routed as a gating level, via OR2, to the Write-1 AND gate (see Figure 4-24) in the delay line control circuit. This gate, when conditioned, allows a Write Marker bit to be written in the delay line. Since the Start Write latch is still set at this time, and since the Receive Character trigger is now in a reset state, A10 becomes conditioned to generate a Write Wrt Mk signal which is routed to half-conditioned A13. At ring bit 2 time, the Write Marker Bit signal is gated by conditioned A13 and AND'ed with the Write Delay Line and A2 pulses (500 ns) to insert the Write Marker bit 1.5 μs after the entry of the text character into the 317.6-μs delay line.

At ring bit 3 time, with the Receive Character trigger is a reset state, A5 is conditioned to reset the Start Write latch preparatory to receiving the next character for processing.

Delay Line Readout - Read Operation

The delay line readout operation for a Read command is identical with that described for a Write command. Refer to the paragraph entitled "Delay Line Readout - Write Operation."

Deserializer and Output Register Transfer - Read Operation

The data bits emanating from the delay line (Figure 4-24) as Serial Data Out signals are entered in serial fashion into the deserializer. The latter comprises seven AND gates which are conditioned by the Serial Data Out signals in coincidence with the various Ring bit time signals. Subsequently, the data entered in the deserializer is transferred in parallel to the output register. The parallel data transfer is effected at a 1.0-μs rate under control of the ring bit counter; the first bit of the character is entered at ring bit 3 time, and the seventh bit is entered at ring bit 9 time, completing the transfer operation.

Output Register to Character Register Transfer

The text character entered into the output register is transferred to the character register in the following manner. (Refer to Figure 4-30 and FC-104.) Note that OR2 is conditioned by the Not Output Reg

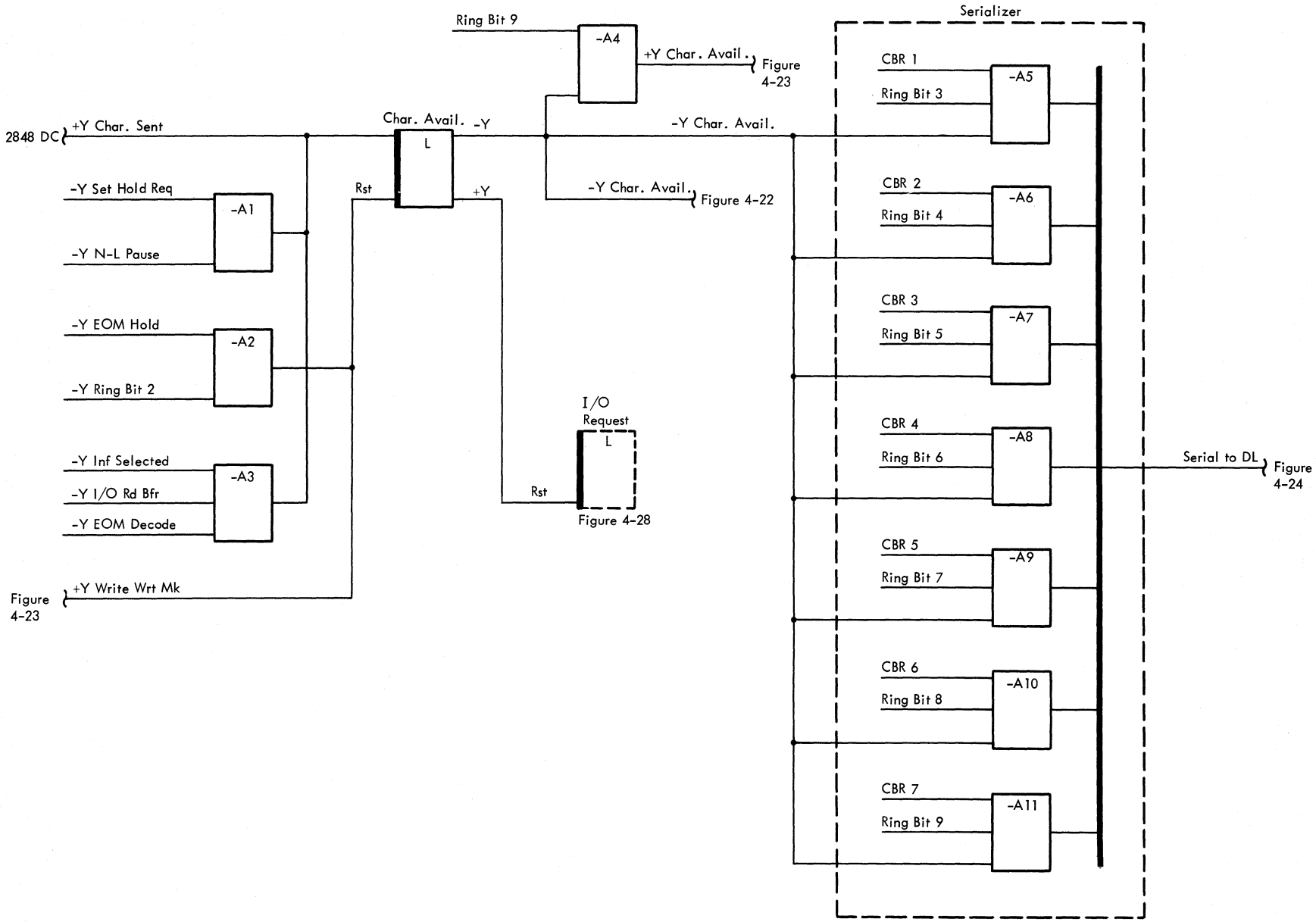


Figure 4-31. Read Operation - Common Buffer to Serializer Transfer

Empty signal derived as a result of the status of the output register at this time. The output signal of the conditioned OR is AND'ed with a Rd or Rd Bfr, Rd Ptr signal, Reg-1 Empty, IF Char Gate Lth Reset, and a Ring Bit 3 time signal to condition A2, whose output sets the I/O to CR1 latch. At ring bit 5 time, with the I/O to CR1 latch set, A4 is conditioned to gate the contents of the output register to the character register. At ring bit 6 time, with the I/O to CR1 latch set, A5 is conditioned to reset the output register. At ring bit 9 time, an output Reg Empty signal is generated and AND'ed at A18 with the Ring Bit signal to reset the I/O to CR1 latch, thereby terminating the transfer operation. Once entered in the character register, the text character is subsequently shifted into the Serdes register in the manner described in the paragraph entitled "2848 DC Response (STX)."

2848 DC Response - ETX Character

At the completion of the data transfer operation sequence, an ETX is developed in the remote interface as a result of the 2848 common decoding an EOM character. The character is transmitted following the Character Sent signal that precedes every character transfer and is received by the remote interface as an EOM Decoded signal. This signal is AND'ed with a Rd or Rd Bfr and Ring 2 signal to partially condition A2 (Figure 4-32). Since no Enter Cmd or Remote IF Rd Set End OP signals are evident at this time, OR1 and A3 are conditioned, and their respective signals are routed as gating levels to condition A2. Once conditioned, the output signal from A2 sets the Hold Request latch (FC-112(1)). When set, the Hold Request latch generates a signal to de-gate the Read Bfr, Write gates (Figure 4-28) and the Poll gate (Figure 4-27), thereby inhibiting the setting of the I/O Request latch (Figure 4-28). In addition, the output of the Hold Request latch is AND'ed with the set output of both the Receive Character and Character Available triggers (the latter turned on with the receipt of the Character Sent signal, the former by the setting of the Character Available trigger) and with the reset output of the Text Mode latch to condition A7 (Figure 4-22). Conditioned A7 emits a Rd EOM Decode signal to set the EOM Hold latch (FC-112(2)). The output signal generated from the latch is AND'ed with the set output of the Receive Character trigger and A2 Pulses (500 ns) to condition A5 (Figure 4-25). Conditioned A5 generates a signal to complement the Receive Character trigger to its reset state once again. At ring bit 2 time, with the EOM Hold latch set, A2 (Figure 4-32) is conditioned to reset the Character Available latch, thus inhibiting further data entry into the serializer. As shown in Figure 4-33, the EOM Hold signal, in conjunction with a Not Inf Selected signal, conditions A1. The output A1, together with the Rd or Rd Bfr, Rd Ptr, Delay Reg Clear, Reg-1 Empty, and Ring Bit 7 signals,causes A3 to be conditioned and, in turn, sets the Cancel ETX latch. The set side of the latch is connected to I1 and I2, whose relatively slow inversion time is sufficient to allow A4 to be conditioned. In addition, the latch output is routed to degate A6, thus inhibiting the reset of the Serdes register. The output derived from the conditioned AND is an Answer ETX signal which is routed to set bits 6 and 7 (ETX) latches in the output register. Thus, the ETX ot EOM signal generated from the 2848 is entered directly into the output register; in the next ring bit cycle, it is transferred to the character register in the manner described in the paragraph entitled "Output Register to Character Register Transfer."

Buffer Parity Check - Read Operation

Of significant note is the fact that had a Buffer Parity Check condition occurred during the 2848 response sequence, the sending unit would have generated a Bfr Parity Check signal (Figure 4-33 and FC-112) which, in turn, would have turned on the Set Cancel latch in the remote interface. This latch remains set until the ETX or EOM control character is transmitted. When this occurs, the output of the latch is AND'ed at A5 with the Cancel ETX latch output to produce the Answer Cancel signal. This signal is then routed to set bit 4 and 5 latches (Cancel code) in the character register. Thus, a Buffer Parity Check condition causes the cancel control character to be entered in the character register while the ETX control character is entered in the output register. Thereafter, each character is transferred from its respective register in the manner described in other paragraphs of this chapter.

2848 DC Response - LRC Character

Following the transmittal of the ETX or EOM character, the 2848 transmits the LRC character accumulator in the LRC register to the data set via the Serdes register (FC-112(3)). The operation begins at the completion of the ETX character readout operation from the Serdes register. When this occurs, a Serdes Empty signal is generated, and, since no data is present in the output register and character register, and since the Cancel ETX latch is still set, the resultant status signals are AND'ed with the Serdes Empty signal to condition A1 (Figure 4-34) at ring bit 4 time. The signal output derived from the conditioned AND is a Transmit LRC Character signal which is routed to gate the contents of the LRC register into the Serdes register. Also, the signal

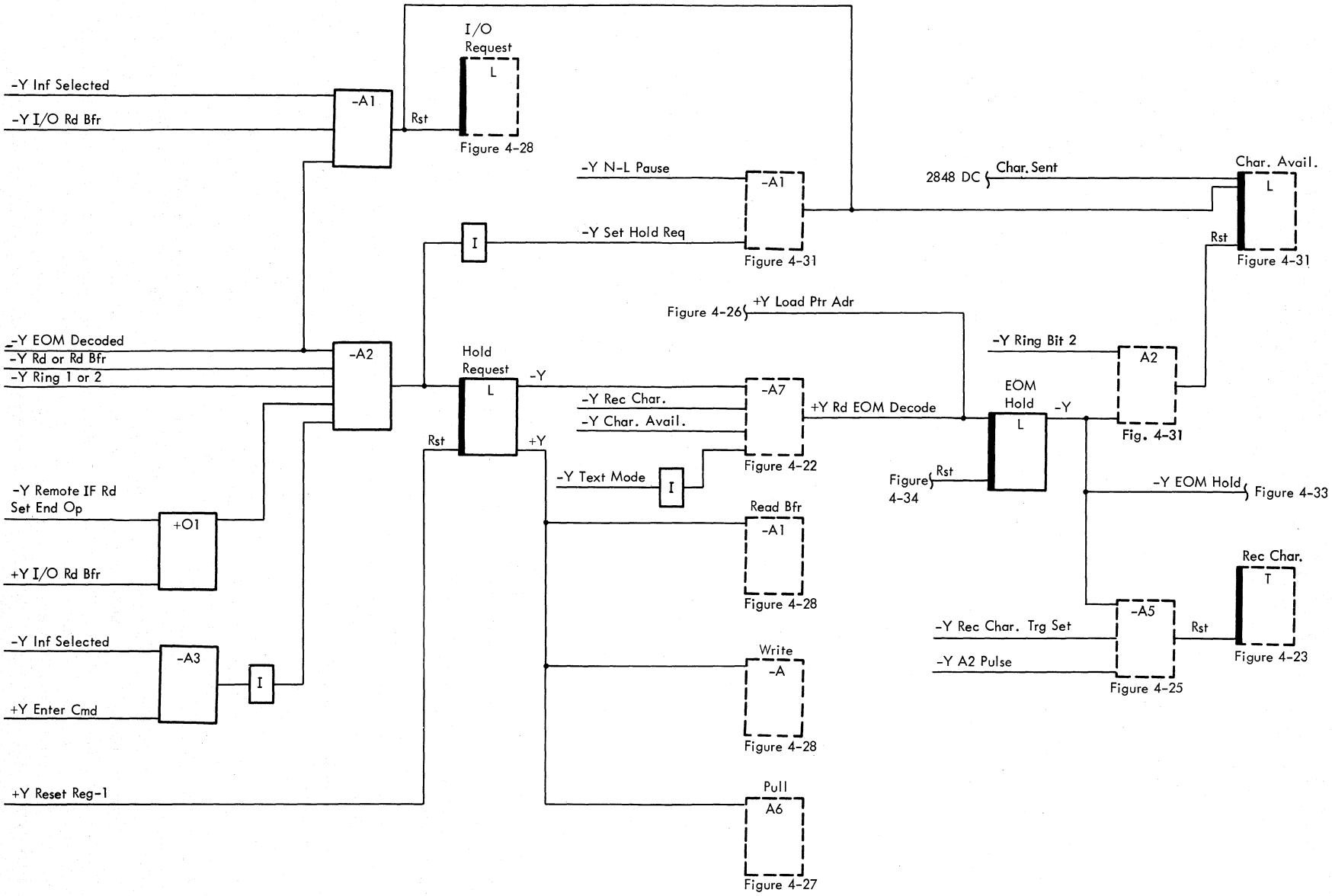


Figure 4-32. 2848 DC Response - ETX Character

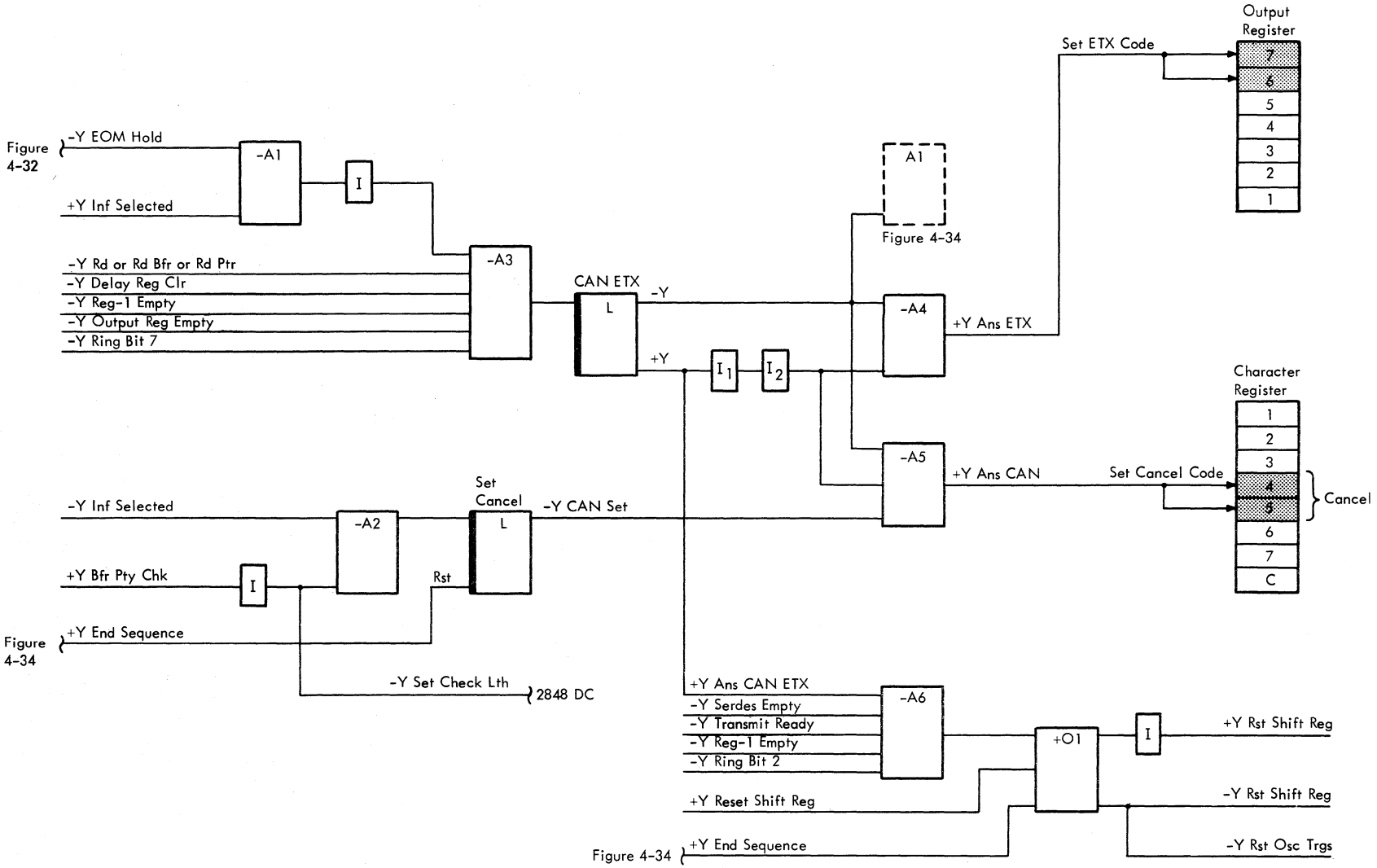


Figure 4-33. Read Operation - Buffer Parity Check Control

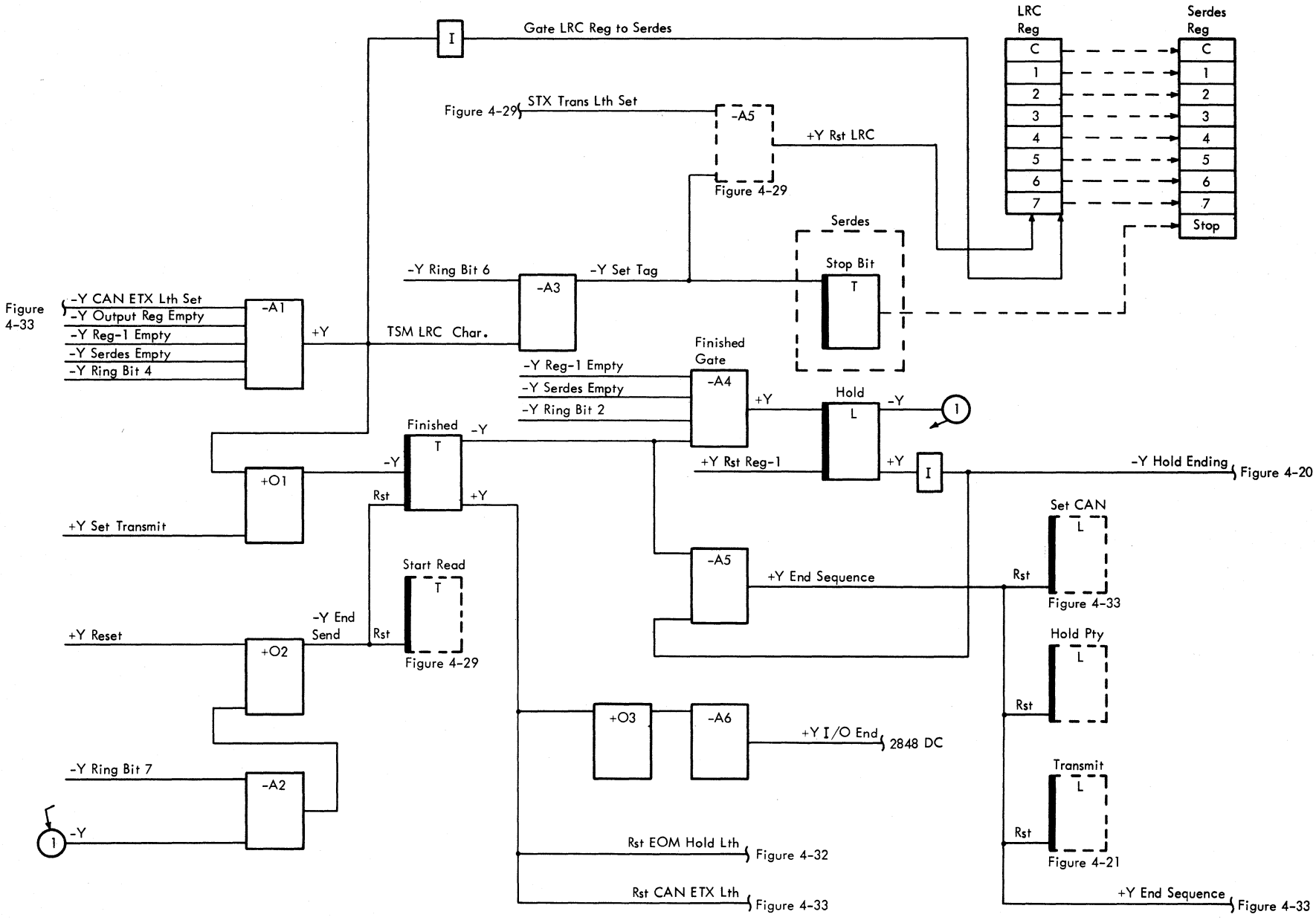


Figure 4-34. 2848 DC Response - LRC Character

is sent via OR1 to set the Finished trigger. The set output signal of the Finished trigger is sent to reset the EOM Hold (Figure 4-32) and the Cancel ETX (Figure 4-33) latches. The signal is also sent to the 2848, via O3 and A6, as an IO End signal.

The Cancel ETX latch having been reset causes A1 to be deconditioned and enables A3 to be conditioned at ring bit 6 time. The conditioned AND generates a Set Tag signal, which is AND'ed with an STX Trans signal at A5 (Figure 4-29) to produce a signal (Rst LRC) that resets the LRC register. The Set Tag signal is also sent to set the Stop bit trigger in the Serdes register. Once the LRC character and its associated Stop bit have been shifted out of the Serdes register to the data set, the resultant Serdes Empty signal is AND'ed with a Reg-1 Empty and the set output signal of the Finished trigger to condition the Finished Gate at ring bit 2 time. Conditioned A4 generates a signal to set the Hold latch. The set side of this latch, in turn, is AND'ed at A5 with the set output signal of the Finished trigger to produce the End Sequence signal. This signal is sent to reset the Set Cancel, Hold Parity, and Transmit latches and the Serdes register following the transmittal of the LRC byte to the data set. At ring bit 7 time, the reset output signal from the Hold latch is sent to condition A2, the output of which is routed, via OR2, as an End Send signal to reset the Finished trigger and to reset the Start Read trigger (Figure 4-29), thus terminating the Specific Poll Read Operation.

Channel Response - STX to Read End Sequence

The reset output of the Hold latch is sent as a Hold Ending signal, which serves as a provisionary signal to condition A5 (Figure 4-20). Since, in effect, the Read operation is terminated, should the channel desire to transmit a message to the 2260 device just polled, it need only generate a Start of Text (STX) signal to the remote interface to again establish communication with the device. This obviates the need for the channel to undergo an addressing sequence operation (SOH, DC address, Device Address, Command) in order to reselect the device. Upon receipt of an STX signal from the channel, it is AND'ed with the Hold Ending signal and a Not I/O Adr Write signal to condition A5 (Figure 4-20 and FC-105). Conditioned A5 generates a Set Write/Clear Read signal, which, as the name implies, will reset the Read Buffer latch and set the Write latch, thus enabling the channel to transmit its message to the 2260 device.

Write DS Line Address

The Write DS Line Address command combines the Write Addressed DS command with line selection capabilities, thus enabling the selection of a 2260 display line as the beginning line of a message. The command causes the cursor to be positioned in the first displayable position of the addressed line (line address is specified by the first data byte following the STX line control character; see Figure 4-13). With the exception of the command byte format and the positioning of the cursor, the Write DS Line Address command is the same as the Write Addressed DS command previously described.

The basic difference between the Write Addressed DS and Write DS Line Address command operations is that when the latter command is entered into the character register, at the conclusion of the addressing sequence, the command is routed directly to the 2848 DC where it is decoded. The 2848 DC subsequently decodes the command (FC-113) and, in turn, responds by generating a Set Write Ln Adr signal and an I/O Ln Adr signal to the remote interface (Figure 4-20). The Set Write Ln Adr signal is routed through OR 1 to condition AND 4 and thereby set the ACK response latch. The I/O Ln Adr signal circumvents the need to set the Write latch, which is necessary for a Write Address DS command, by being applied to OR 2 in order to produce the Wr or Wr Ln Adr signal to effect a Write operation. Thereafter, the operation is identical with that described for the Write Addressed DS command. The line address contained in the first data byte after transmittal of the STX control character is processed by the remote interface as a regular data byte. Subsequent message data (text) is then displayed, beginning at the line indicated by the cursor.

Write/Erase Command

The Write/Erase command is essentially an Erase command with a Write sequence. The command erases a message displayed on the screen of a selected 2260 Display Station and causes the cursor to be displayed in the first displayable position (upper left-hand corner) on the screen. This ensures that the succeeding message, intended for display on the display station, will be written beginning at the first displayable position following the normal addressing sequence operation. A description of the Write/Erase command operation is presented in the following paragraphs and is illustrated in FC-114.

The Write/Erase command is issued following the performance of the addressing sequence operation (SOH-EOT, DC Address, Device Address) described in previous paragraphs of this chapter. Once the command has been entered into the Character register (ring 3 time), it is decoded by the command decoder shown in Figure 4-35. As shown

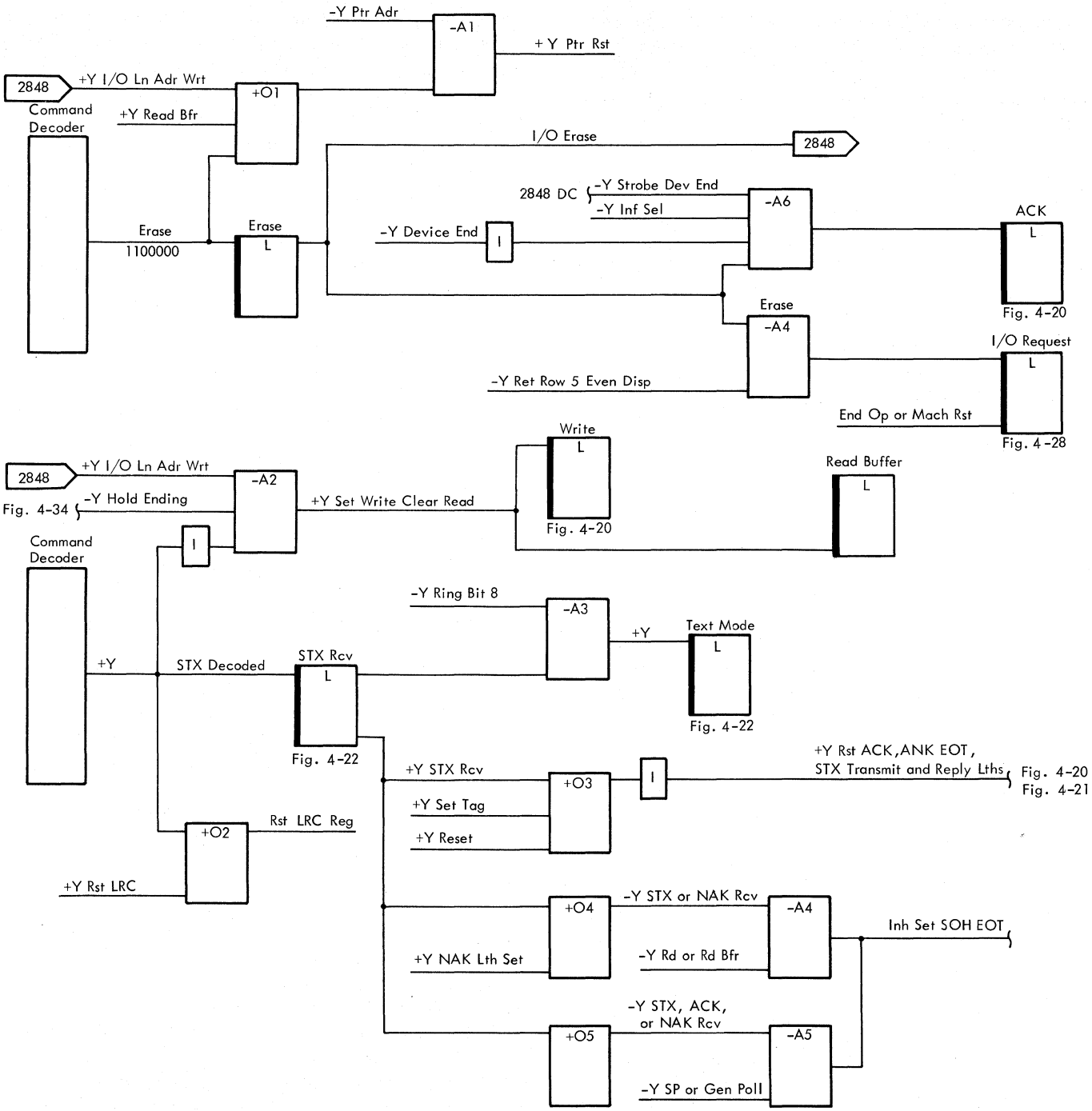


Figure 4-35. Write/Erase Command

in the figure, decoding of the Erase command (1100000) produces an Erase signal which is routed to set the Erase latch. The output signal (I/O Erase) derived from this latch is routed to partially condition AND's A4 and A6, and is routed to the 2848 DC.

AND 4 is conditioned when the remote interface receives a Retrace Row 5 Even Display signal from the 2848 DC. When this occurs, the I/O Request latch is set and an I/O Request signal is generated to the 2848 DC. When the 2848 DC acknowledges the remote interface, it responds with the Interface Selected signal, which is routed to AND 6. This signal, in conjunction with the I/O Erase command signal generated by the remote interface, causes erasure of the data displayed on the 2260 DS. At the conclusion of the Erase operation, the 2848 DC transmits a Strobe Device End signal, which is

routed to AND 6, as an indication to the remote interface that the Erase operation was performed. Conditioned AND 6, in turn, generates a signal (Set ACK) to set the Acknowledge latch (FC-102). The latch having been set, the remote interface sends the ACK response back to the data set in the same manner as that described in the paragraph titled "Remote Interface Response - ACK Character." Transmission of the ACK character indicates to the channel that the screen of the 2260 DS has been erased and that the cursor is in the first displayable position. At this time, channel response to ACK may be an EOT or SOH (either terminates the operation), or it may be the transmission of a new message beginning with an STX character as described in the following paragraph.

Write Erase Command - Channel Response (STX)

Once the STX character has been decoded by the ASCII command decoder (Figure 4-35), an STX Decoded signal is produced and routed to set the STX RCV latch, reset the LRC register via OR 4A, and condition AND 2. The conditioned AND generates a Set Write Clear Read which, as the name implies, sets the Write latch and resets the Read Buffer latch. (See FC-101, sheet 3 of 3, and FC-105.) The output signal from the STX RCV latch is sent, via OR 3, to reset the ACK, NAK, EOT, STX Transmit, and Reply latches, and is sent, via OR 4, OR 5, AND 4 and AND 5, to inhibit setting of the SOH, EOT latch. At ring bit 8 time, the STX RCV signal is gated via A3 to set the Text Mode latch, thereby removing the 2848 DC from Control Mode operation and placing it in Text Mode in preparation for receipt of the message intended for display on the 2260 DS.

The operation that follows is essentially the same as that described for the Write DS command.

General Poll

The General Poll command (Figure 4-36) causes the 2848 DC to sense each 2260 DS for the presence of a manually entered message, pending transfer to the channel. If one or more messages are present and all requirements are met (Start symbol displayed and Enter key depressed), the message(s) is transferred to the channel. Each message is accompanied with the address of the 2260 DS being queried.

If the Printer feature is incorporated in the system configuration, the General Poll command must first interrogate the printer for its status before an attempt can be made to interrogate the 2260 DS's in the system configuration. That is to say, if a previous attempt was made by the channel to select the printer (Write Printer command) while it was communicating with another device in the system configuration (Busy or Not Ready status), a Printer Priority condition is initiated, which gives the channel priority over other devices desiring access to the Printer.

Once the Printer Priority condition is established and a General Poll command is issued by the channel, the 2848 DC is caused to sense the status of the 1053 Printer (FC-109) before an attempt is made to sense the associated 2260 DS's in the configuration. Should the printer again be in a Busy or Not Ready status when the General Poll command is issued, the 2848 DC will poll the associated 2260's in the configuration. If, during this sequence, communication is established with a particular 2260 DS while the printer is in a Busy or Not Ready status, the 2848 DC, at the completion of its communication with the polled 2260 DS, will repeat its interrogation of the printer. This procedure is repeated until communication is established with the printer. The General Poll command operation is described in the following paragraphs and is shown in Figure 4-36.

The General Poll command operation commences with the receipt by the remote interface of the third byte (1111111) in the addressing sequence, which signifies that a general poll operation is to occur (FC-101, sheet 3 of 3). As shown in Figure 4-36, the address byte is decoded by A1 in the command decoder of the remote interface. As a result, a General Poll DA signal is generated to set the GP Decode latch and to inhibit A6 from being conditioned. The latter function prevents the DC Select trigger from being reset (it was set with the receipt of the second byte of the addressing sequence), since a particular 2848 DC has been selected at this time. The DC Select trigger being set, its output signal (-Y DC Selected) is AND'ed with the -Y Gen Poll DA signal and the reset output signal from the Device Address trigger to set this trigger via A7. In this case, no specific device is addressed (as with other command addressing sequences), but rather a general address to all devices is implied.

The GP Decode latch having been set, A5 is deconditioned and A4 is partially conditioned until the fourth byte (Poll) of the addressing sequence is decoded by the command decoder at ring bit 4 time. When this occurs, the Gen Poll latch is set (FC-115) and Poll gate A8 is inhibited from being conditioned to set the I/O Request latch. The Gen Poll latch also generates a signal (-Y Gen Poll) which is AND'ed with signals that indicate that both the SP Poll and I/O Read latches are in a reset status, to condition A9. The output signal from A9, in turn, is sent via OR 4 to the 2848 DC as notification that a Poll operation is being performed. The signal is also routed

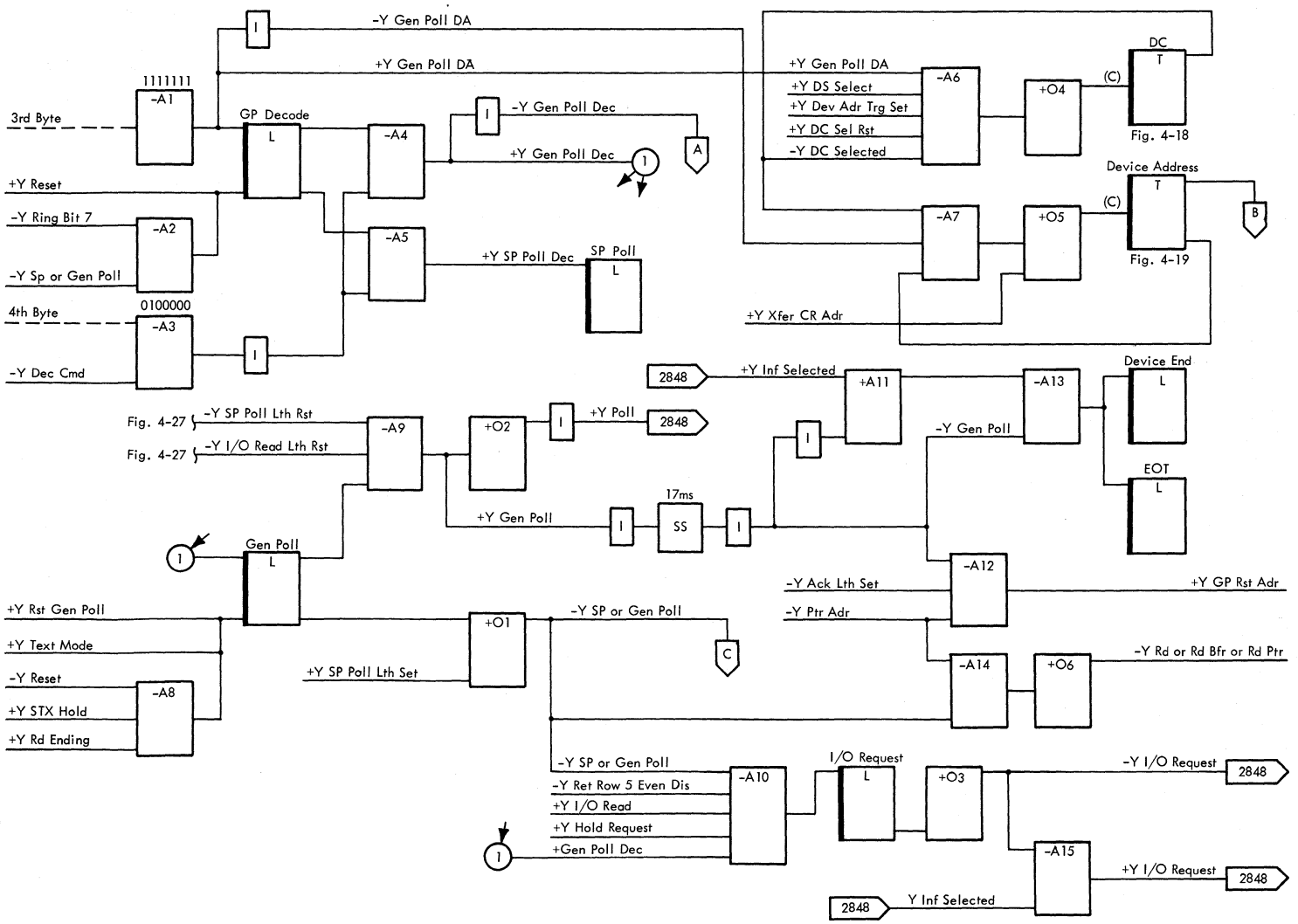


Figure 4-36. General Poll Operation (Sheet 1 of 2)

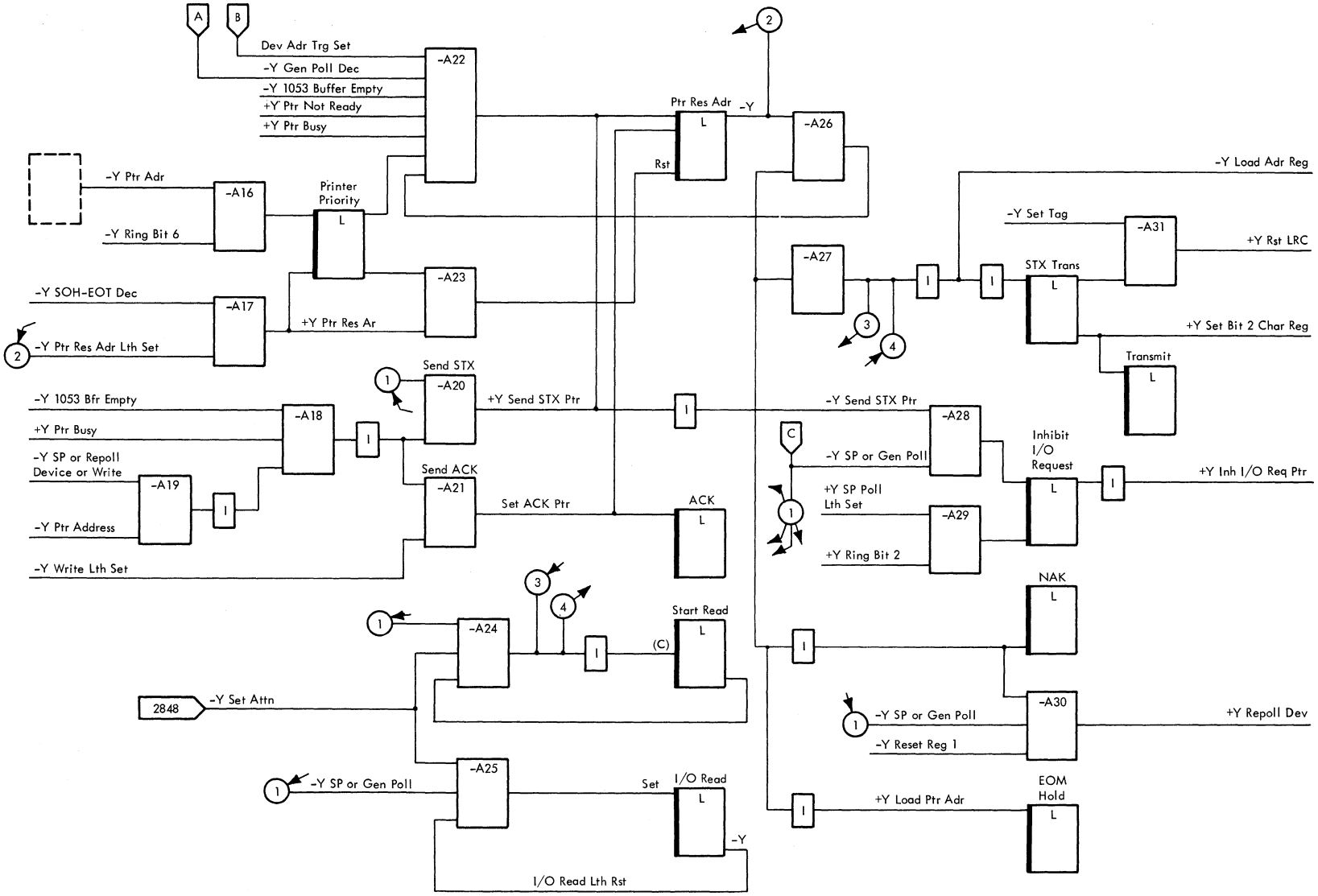


Figure 4-36. General Poll Operation (Sheet 2 of 2)

to fire a 17-ms single-shot, whose output is used to partially condition A11 and A13. This is an anticipatory function; if an Interface Selected signal is not received from the 2848 DC within the allotted 17 ms, A11 and A13 will be conditioned and a Set EOT signal will be generated to set both the EOT and Device End latches (FC-110), thereby terminating the General Poll operation.

The General Poll Decode latch also generates another signal (-Y Gen Poll Decode) which is routed to sample A22 (Figure 4-36, sheet 2 of 2, and FC-109) and thus determine the status of the 1053 Printer. As shown in the figure, if the Printer Priority latch is set, as a result of a previous request to interrogate the printer (Write Printer or Specific Poll to Printer command), a signal is generated by the latch to condition A21 and reflect this condition. The Printer Priority latch is set by the output of A15 which is conditioned as a result of a Printer Address having been decoded at ring bit 6 time due to a previously issued Write Printer or Specific Poll to Printer command. Therefore, if the Printer Priority latch was set at this time and the Printer status was Not Busy, Ready, 1053 Buffer Empty, Device Address trigger set, and Ptr Res Adr (Printer Reset Address) latch reset, the presence of the Gen Poll Decode signal, in conjunction with the status signals, would condition Printer Status gate A22. The conditioned gate, in turn, generates a signal that sets the Printer Reset Address (Ptr Res Adr) latch. This causes the address register to be reset and, at the same time, prevents any 2260 keyboard associated with the 2848 DC from issuing a Print command since, in effect, the printer is reserved for the channel.

The Printer Priority and Ptr Res Adr latches remain in a set state until an SOH-EOT control character is received from the channel. The conditioned output signal is also routed as a Send STX Ptr signal to initiate the following:

1. The signal is AND'ed with the set output signal from the Ptr Res Adr latch to condition A26, whose output signal is used to degate A22.
2. The signal is AND'ed with a -Y SP or Gen Poll signal to condition A28, whose output signal is sent to set the Inhibit I/O Request latch. The latch generates a signal that resets the I/O Request latch. This latch remains in the reset state until the following ring bit 2 time.
3. The signal is routed to reset the NAK latch.
4. The signal is inverted and sent as a Load Ptr Adr signal to set the EOM Hold latch.
5. The Send STX Ptr signal is sent to condition A27, whose output signal (Load Address Reg) is sent as a gating level to enable the address of the printer previously entered in the address register to be transferred to the output register.
6. The signal is also routed to complement the Start Read trigger to its set state, and to set the STX Trans latch (FC-111).

The STX Trans latch having been set, a signal is sent to set the Bit 2 latch in the character register, thereby placing the STX (0100000) transmitted from the 2848 DC in the character register. The output signal from the latch is also routed to set the Transmit latch.

Thereafter, the STX, Printer Address, ETX, and LRC character transfer operations to the channel are similar to those discussed under "Command - Specific Poll to 2260 DS."

Upon completion of the printer interrogation operation, the channel responds with ACK (FC-101, sheet 3 of 3) or NAK (FC-117). Receipt of the ACK control character causes the ACK latch to be set (FC-116). When this occurs, a -Y ACK signal is generated to A12, and, since the printer address is still contained in the address register and the Gen Poll latch is still set, these signals are AND'ed to condition A12. The output of this conditioned AND is routed to reset the address register. Since no address is contained in the address register and no Write operation is in progress, A32 is deconditioned, thereby removing the Inhibit I/O Request Ptr signal which prevented the I/O Request latch from being set.

The last function allows the I/O Request latch to again be set by Poll gate A10 which is conditioned as a result of the following: SP or Gen Poll, Ret Row 5 Even Display, No I/O Read operation in progress, the Hold Request latch reset, and No Gen Poll Decode signal present (FC-115). The I/O Request latch being in a set state, an I/O Request signal is generated to the 2848 DC to sample for the presence of a depressed Enter key associated with a 2260 DS.

If an Enter key of a 2260 DS is found to be depressed, a Set Attention signal is sent to the remote interface (FC-110), and, since a Gen Poll is still in progress and the I/O Read and Start Read latches are in a reset state, A24 and A25 are conditioned to set their respective latches. With the I/O Read latch in a set state, an I/O Read signal is generated to decondition Poll gate A10 and is routed to the 2848 DC as notification that a Read operation of the polled 2260 DS is to occur.

Subsequently, the 2848 DC response operations (STX, Device Address, Text, CAN, ETX, LRC) are processed in a manner identical with that described under the paragraph titled "Command - Specific Poll to 2260 DS."

INTRODUCTION

This chapter describes the power distribution and control system for the IBM 2848 Display Control by explaining the operation of the circuits during such power sequences as power on, power off, and emergency power off. The IBM 2848 Display Control can be powered from either a 50- or 60-cycle service voltage. The frequency employed depends upon the particular installation. Both the 50- and 60-cycle power systems are described in this chapter. (The reader should bear in mind that only one description will be applicable to a particular installation. The other power description can be ignored.) Since the power system of the IBM 2260 Display Station is functionally allied with other 2260 circuits, it is discussed in Chapter 2 under Display Station Power Supply.

For the operation of the standard medium power standard (MPS) power supplies, the reader is referred to IBM Form 223-2799-0, which describes all standard SMS power supplies.

60-CYCLE POWER SYSTEM

Initial Power Distribution

The 60-cycle power circuits of the 2848 Display Control are illustrated in Figure 5-1 (sheets 1 and 2). Assume that CB1, CB2, and the CB's of the dc power supplies are closed and that a 208v 60-cps input voltage is available at transformer T1 and at terminals T1 and T2 (Figure 5-1, sheet 1).

Terminals 1 and 2 (EPO) of the remote power interface are closed (no emergency-power-off condition exists). Thus, relay K1 is energized, closing the K1-1 contacts and thereby energizing relay K4. The contacts of K4 cause voltage to be applied to the convenience outlet transformer and to the fan and heater circuits (through CB2). When the logic and power gate overtemperature contacts are closed (normal condition), 24vac is supplied to the thermal reset circuit from the full-wave bridge rectifier. Relay K7, the thermal reset relay, is energized until capacitor C1 is charged. While K7 is energized, contacts K7-1 and K7-2 are closed. Thus, since the logic, power gate, and delay-line overtemperature switches are closed (normal conditions), the thermal relay (K2) and delay line circuit relays (K6 and K6A) are energized. Relay K7 remains energized for from 4 to 5 seconds and is then de-energized. Relays K6 and K6A are held energized through K6A-1. Relay K3 is held energized through K2-2, its holding contacts. Since the K6-1 and K6-2 contacts are closed, 208vac is applied to the delay-line heaters. Contacts K6A-2 open the delay-line circuit to the overtemperature indicator. Contacts K2-1 open the logic and power gate circuits to the overtemperature indicator. Contacts K6A-3 close, energizing relay K5.

No further sequencing of the power circuits occurs until a power-on or power-off sequence is initiated.

Power Control Sequences

Power On - Remote

Assume that the LOCAL-REMOTE switch (S1) is in the REMOTE position and that the initial power distribution sequence is complete.

A Power On signal is received from the system through contact A7 of the LOCAL-REMOTE switch. This signal energizes relays K3 and K3A. A power-hold voltage is received through pin 5 of the remote power interface. Since relay K5 was energized during the initial power distribution sequence, a path is provided through S1 to K3 and K3A, which are then held energized through the K3A-1 contacts.

Energizing K3 provides power to the dc supplies, the power gate fan, and the logic blowers. Relay contacts K3A-2 close and indicate to the system that a power-complete condition exists by shorting pins 3 and 4 of the remote power interface connector.

Power On - Local

Assume that the LOCAL-REMOTE switch is in LOCAL and that the initial power distribution sequence is complete.

When the PWR ON pushbutton (S2B) is depressed, relays K3 and K3A are energized, and the unit is energized as described for remote power on.

The power hold required is provided through the normally closed PWR OFF pushbutton (S3), the LOCAL-REMOTE switch, and holding contacts K3A-1.

Power Off - Remote

A remote power-off sequence is initiated when the power hold through pin 5 of the remote power interface connector is opened by the system. Relays K5, K3, and K3A are de-energized, thus removing power from the dc supplies, the power gate fan, and the logic blowers. The POWER ON indicator is turned off, and contacts K3A-2 open to indicate an incomplete power-on condition to the controlling system.

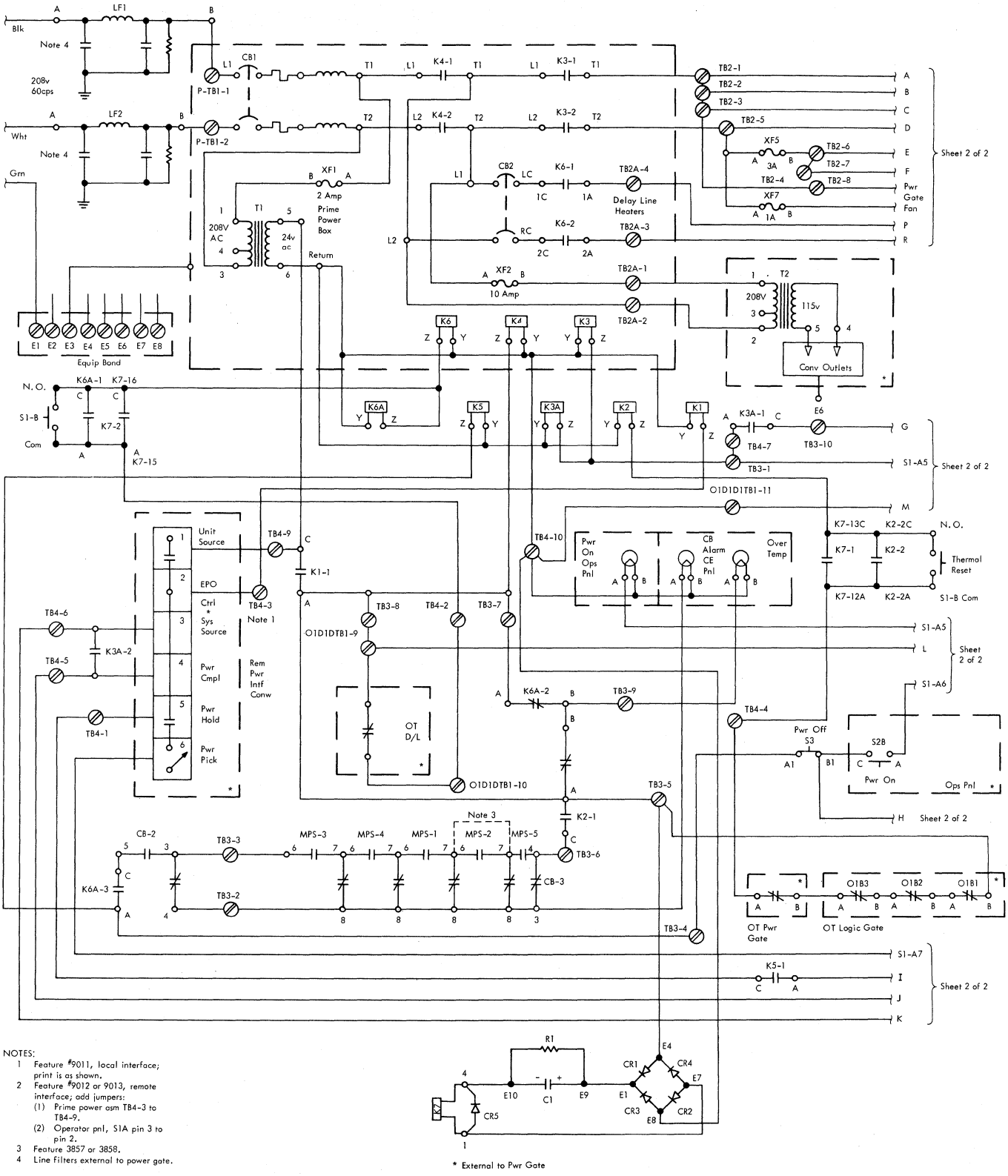
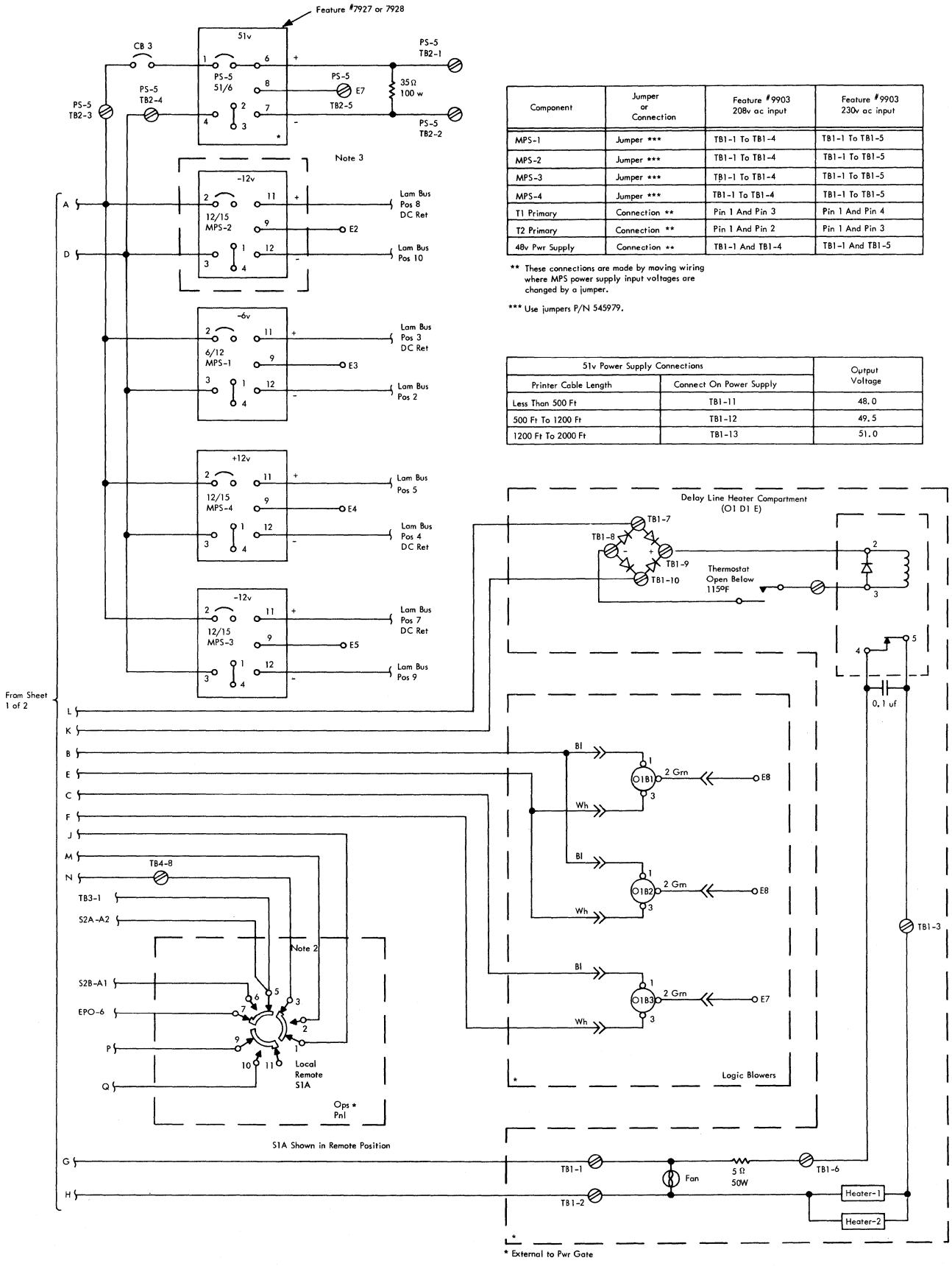


Figure 5-1. 60-Cycle Power Distribution and Control (Sheet 1 of 2)



Component	Jumper or Connection	Feature #9903 208v ac input	Feature #9903 230v ac input
MPS-1	Jumper ***	TB1-1 To TB1-4	TB1-1 To TB1-5
MPS-2	Jumper ***	TB1-1 To TB1-4	TB1-1 To TB1-5
MPS-3	Jumper ***	TB1-1 To TB1-4	TB1-1 To TB1-5
MPS-4	Jumper ***	TB1-1 To TB1-4	TB1-1 To TB1-5
T1 Primary	Connection **	Pin 1 And Pin 3	Pin 1 And Pin 4
T2 Primary	Connection **	Pin 1 And Pin 2	Pin 1 And Pin 3
48v Pwr Supply	Connection **	TB1-1 And TB1-4	TB1-1 And TB1-5

** These connections are made by moving wiring where MPS power supply input voltages are changed by a jumper.

*** Use jumpers P/N 545979.

51v Power Supply Connections		Output Voltage
Printer Cable Length	Connect On Power Supply	
Less Than 500 Ft	TB1-11	48.0
500 Ft To 1200 Ft	TB1-12	49.5
1200 Ft To 2000 Ft	TB1-13	51.0

Figure 5-1. 60-Cycle Power Distribution and Control (Sheet 2 of 2)

Power Off - Local

In local operation, power is turned off when the POWER OFF pushbutton is depressed. This de-energizes relays K3 and K3A, removing power from the power gate fan, the dc supplies, and the logic gate blowers.

Emergency Power Off

Terminals 1 and 2 of the remote power interface are routed through the remote EPO switch. When an EPO condition exists, terminals 1 and 2 are opened. This action de-energizes K1, which, in turn, de-energizes K4 (EPO contactor). Contacts K1-1 open, causing a power-off sequence.

Fault Condition Operation

Circuit Breaker Open During Local Operation: If CB2 opens, the CB alarm indicator lights. The power-hold voltage circuit to K3 and K3A is opened. Power is removed from the dc supplies, the power gate fan, and the logic blowers.

If CB1 opens, a unit power-off sequence occurs without a CB alarm indication.

Circuit Breaker Open During Remote Operation: If a CB opens while the unit is operating in remote, relay K5 is de-energized. Contacts K5-1 open and break the power-hold circuit. The unit power-off sequence occurs, and power is removed from the dc supplies, the power gate fan, and the logic blowers.

Overtemperature Conditions: If an overtemperature condition is sensed in the power or logic areas (remote or local operation), relay K2 is energized, and contacts K2-1 transfer and de-energize relay K5. Contacts K5-1 open, and unit power is turned off.

If a delay line overtemperature is sensed during remote operation, relays K6 and K6A are de-energized, removing power from the delay-line heaters. Contacts K6A-3 open and de-energize relay K5. Contacts K5-1 open and de-energize relays K3 and K3A, turning unit power off. In local operation, a delay-line overtemperature condition de-energizes K6 and K6A as above; contacts K6A-3, however, de-energize K3 and K3A directly.

DC Power Supplies

Up to five dc power supplies are used to provide the dc voltages required to operate the 2848. The supplies are MPS assemblies.

Three basic supplies provide the four different voltages required:

Part No.	No. Used	Output Voltage (vdc)
5261050	1	-6.0
5261130	3	±12.0
196418*	1	+51.0

*Required for 1053 Printer Adapter feature only.

For detailed information on the operation and maintenance of these standard power supplies, see IBM Form 223-2799-0.

50-CYCLE POWER SYSTEM

Initial Power Distribution

The 50-cycle power circuits of the 2848 Display Control are illustrated in Figure 5-2 (sheets 1, 2, and 3). Before power is turned on, contactor PK1 should be reset to ensure that overload contacts PK1-6 and PK1-7 are closed. Assume that circuit breakers PCB1, PCB2, PCB3, and the CB's of the dc power supplies are closed and that the input 50-cycle service voltage is available at transformers PT1 (Figure 5-2, sheet 1).

With the system EPO contacts closed (no emergency-power-off condition exists), 24v is applied to relay K6 through terminals 1 and 2 of the power control interface connector. Contacts K6-1 close, supplying voltage to the delay-line heater control circuit, the 2-second time delay relay (TD1) of the thermal reset circuit, and contactor PK3. When contactor PK3 closes, line voltage is supplied to autotransformer T1 via contacts PK3-1, PK3-2, and PK3-3. Relay K1 is energized through the normally closed overload contacts PK1-6 and PK1-7. Thermal relay K2 is energized by the closed contacts of TD1-1 and the overtemperature thermal switches located at the power gate, autotransformer, and logic gates. Relay K2 is held energized by contacts K2-2. Delay line thermal relay K4 and delay line heater circuit relay PK2 are picked through the normally closed contacts TD1-2 and the delay line overtemperature thermal switch. Relays PK2 and K4 are held energized by contacts K4-1. Line voltage is supplied to the delay line heaters by the closed contacts of PK2-1 and PK2-2. With relays K4 and K2 energized, contacts K4-2 open (sheet 2) and contacts K2-1 transfer to open the overtemperature indicator light circuit. As a result of energizing relay K1, the contacts of K1-1 transfer, opening the CB/OC alarm indicator light circuit and completing the circuit to relay K5 through contacts K2-1, K4-3, and the circuit breaker auxiliary switches.

No further sequencing of the power circuits occurs until a power-on or power-off sequence is initiated.

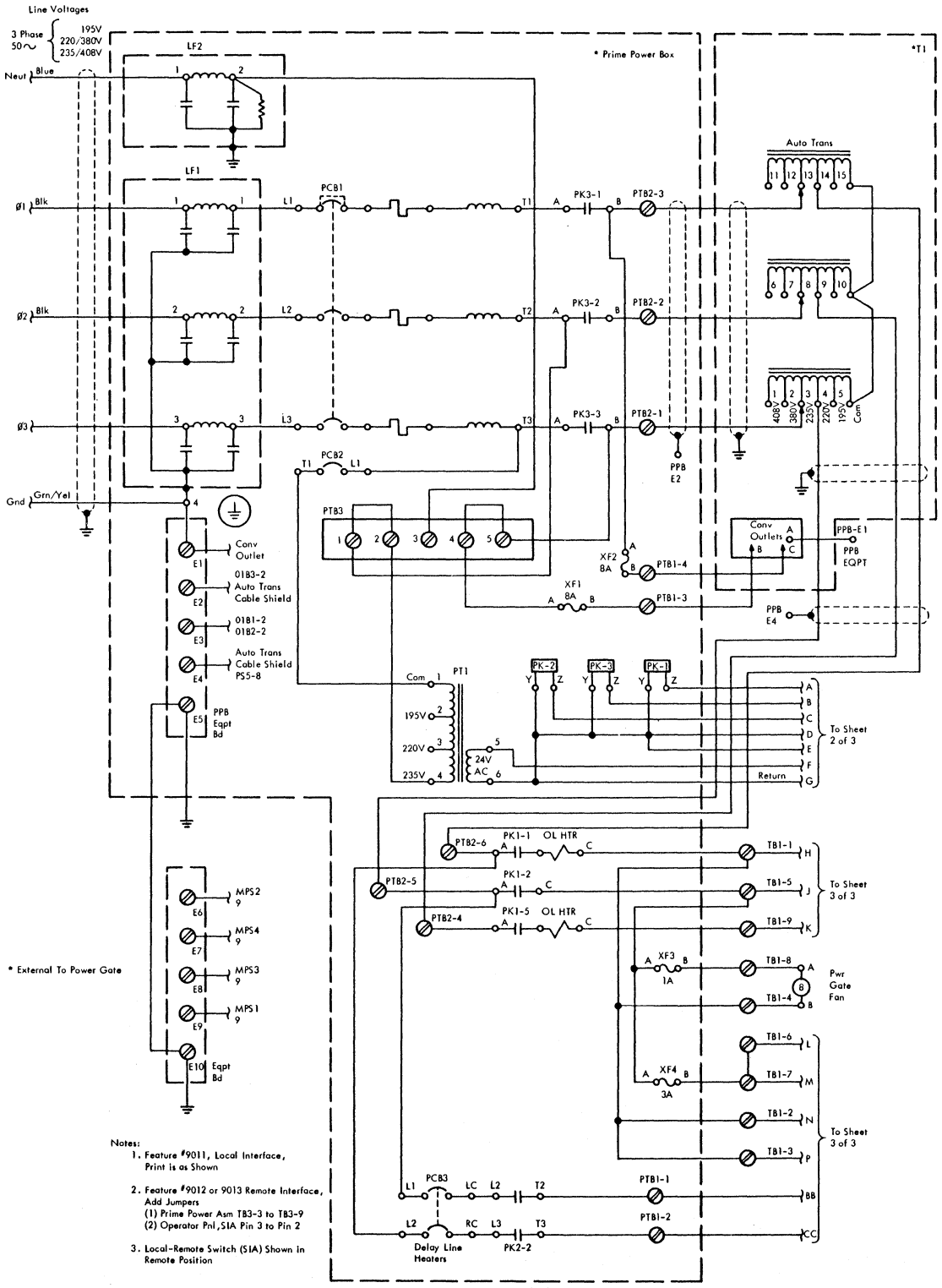


Figure 5-2. 50-Cycle Power Distribution and Control (Sheet 1 of 3)

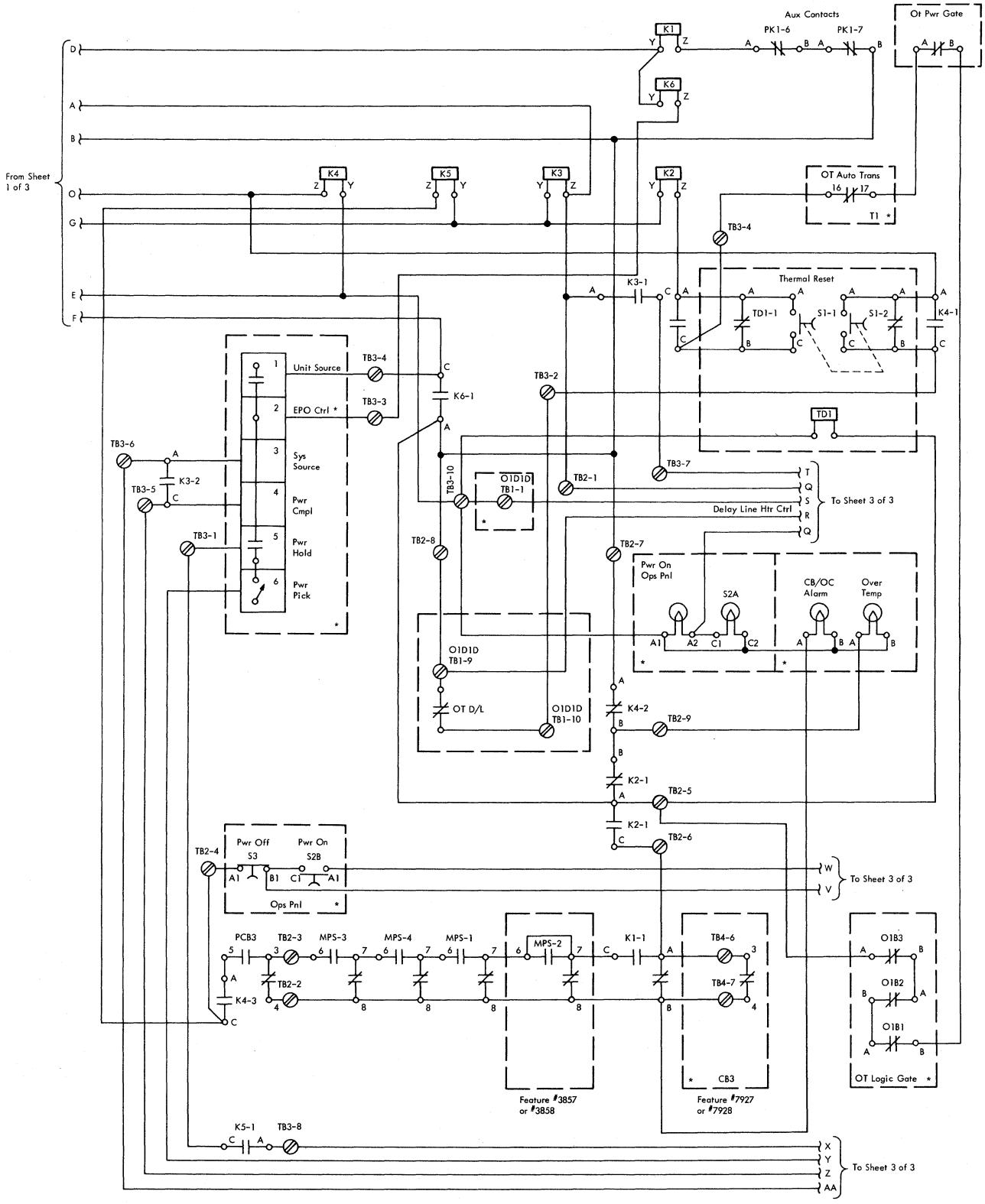


Figure 5-2. 50-Cycle Power Distribution and Control (Sheet 2 of 3)

Component	Jumper or Connection	Feature # 2817 195 Vac Input	Feature # 2815 220 Vac Input	Feature # 2818 235 Vac Input	Feature # 2816 380 Vac Input	Feature # 2819 408 Vac Input
Auto (T1) Tfmr	CONNECTION**	TERM 5	TERM 4	TERM 3	TERM 2	TERM 1
Auto (T1) Tfmr	CONNECTION**	TERM 10	TERM 9	TERM 8	TERM 7	TERM 6
Auto (T1) Tfmr	CONNECTION**	TERM 15	TERM 14	TERM 13	TERM 12	TERM 11
PT1-Primary	CONNECTION**	TERM 2	TERM 3	TERM 4	TERM 3	
PTB3	JUMPER	PTB3-1 TO PTB3-2	PTB3-1 TO PTB3-2	PTB3-1 TO PTB3-2	PTB3-2 TO PTB3-3	PTB3-2 TO PTB3-3
		PTB3-4 TO PTB3-5	PTB3-4 TO PTB3-5	PTB3-4 TO PTB3-5	PTB3-3 TO PTB3-4	PTB3-3 TO PTB3-4

** These connections are made by moving the wiring to the required transformer taps which is determined by the service voltage at the installation.

48/51v Power Supply Connections		Output Voltage
Printer Cable Length	Connect on Power Supply	
Less Than 500 FT	TB1-11	48.0
500 FT TO 1200 FT	TB1-12	49.5
1200 FT TO 2000 FT	TB1-13	51.0

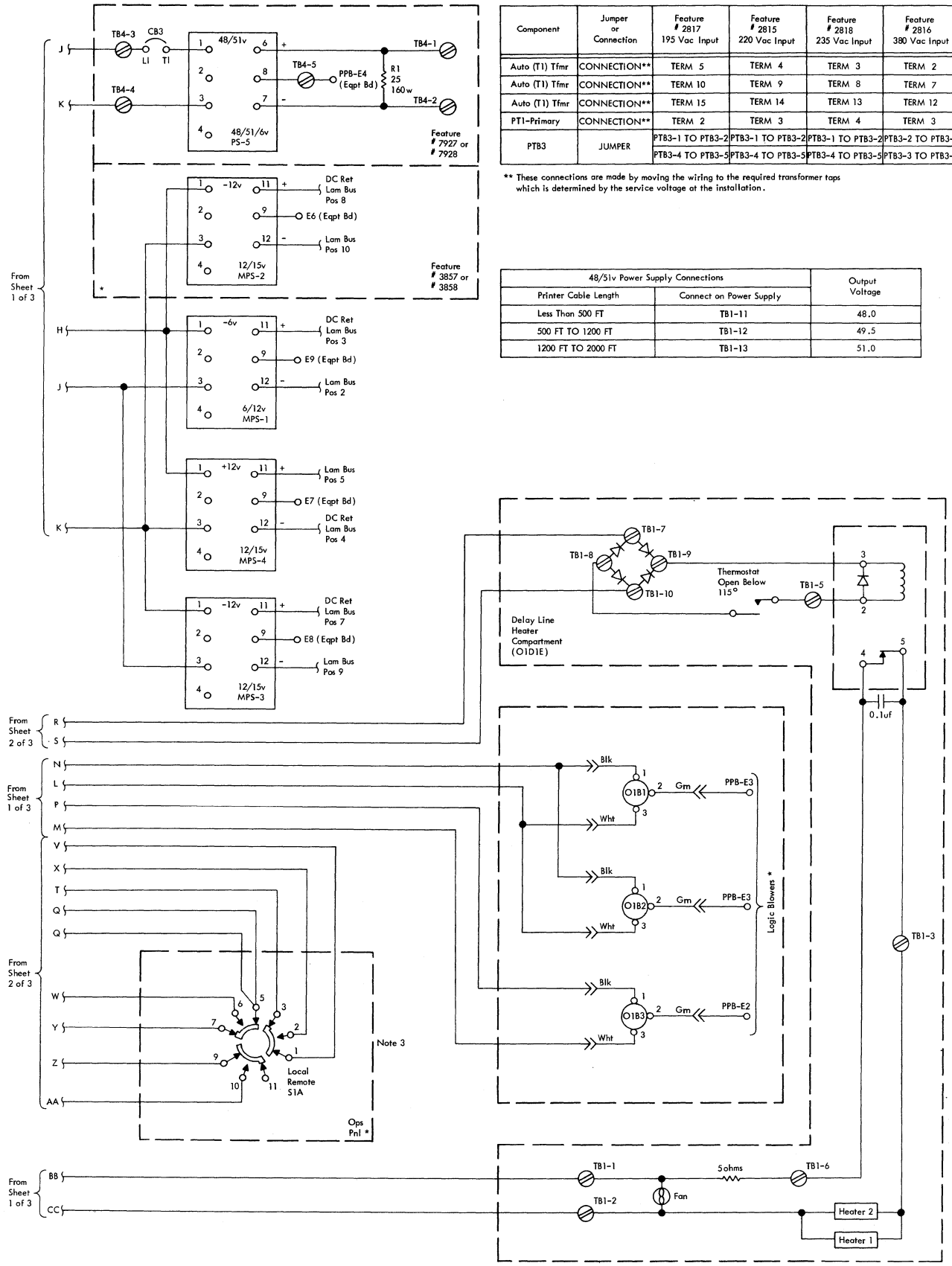


Figure 5-2. 50-Cycle Power Distribution and Control (Sheet 3 of 3)

Power Control Sequences

Power On - Remote

Assume that the LOCAL-REMOTE switch is in the REMOTE position and that the initial power distribution sequence is complete.

A power pick voltage is obtained from the system through terminal 6 of the remote power interface connector (Figure 5-2, sheet 2). The power pick voltage is applied to the power-on indicator light, contactor PK1, and relay K3 through the LOCAL-REMOTE switch S1A. Contacts K3-1 provide a hold voltage path from terminal 5 of the remote power interface connection through K5-1 contacts, switch S1A to contactor PK1, relay K3, and the power indicator light. Line voltage is made available through contacts PK1-1, PK1-2, PK1-5, and the overload heaters to the power supplies, power gate fan, and the logic blowers. (See Figure 5-2, sheets 1 and 3.) Contacts K3-2 close to signify a power complete condition by shorting pins 3 and 4 of the remote interface connector.

Power On - Local

Assume that the LOCAL-REMOTE switch is in LOCAL and that the initial power distribution sequence is complete.

When the PWR ON pushbutton (S2B) is depressed, contactor PK1 and relay K3 are picked via the LOCAL-REMOTE switch S1A. The power hold required is derived by the closed contacts of K3-1, switch S1A, and the power-off momentary switch S3.

Power Off - Remote

A remote power off sequence is initiated when the power hold voltage at terminal 5 (Figure 5-2, sheet 2) of the remote power interface connector is opened by the system. As a result, contactor PK1 and relay K3 are de-energized, thus removing power from the dc supplies, power gate fan and logic blowers. The POWER ON indicator is turned off, and contacts K3-2 open to indicate an incomplete power-on condition to the controlling system.

Power Off - Local

In local operation, power is turned off when the PWR OFF pushbutton S3 (Figure 5-2, sheet 2) is depressed. This de-energizes relay K3 and contactor PK1, removing power from the dc supplies, power gate fan, and the logic blowers. The POWER ON indicator is also turned off.

Emergency Power Off

Terminals 1 and 2 of the remote power interface are routed through the remote EPO switch. When an EPO condition exists, terminals 1 and 2 are open-circuited. This action de-energizes K6, which, in turn, drops out contactor PK3 (the EPO contactor) and all other relays.

Fault Condition Operation

Circuit Breaker Open During Local Operation: If an MPS power supply CB is tripped, the CB auxiliary switch transfers to turn on the CB/OC ALARM lamp I2 (Figure 5-2, sheet 2) and opens the hold voltage circuit to contactor PK1 and relay K3. Power is removed from the dc supplies, the power gate fan, and logic blowers. The same sequence also occurs if the delay line heater and circuit breaker PCB3 (sheet 1) is tripped. If the 48-51v power supply PS-5 (sheet 3) circuit breaker CB3 is opened, power to PS-5 drops and the CB/OC indicator lamp turns on. Since the CB3 auxiliary switch is not a part of the hold circuit, PK1 and K3 remain energized. The MPS power supplies, power gate fan, and the logic blowers remain on. When PCB-2 is tripped, the machine sequences down without a CB/OC alarm indication, and power is still present at contacts PK3-1, PK3-2, and PK3-3. If circuit breaker PCB1 is opened, the machine sequences down without a CB/OC alarm indication, and no power is available at contacts PK3-1, PK3-2, and PK3-3.

Circuit Breaker Open During Remote Operation: All circuit breakers and associated circuits operate in the same manner as detailed for fault conditions in local operation except for the following. With switch S1A in the remote position, control of the hold voltage circuit is transferred to contacts K5-1. If PCB2 or any of the MPS power supply CB's are tripped, relay K5 is de-energized, opening contacts K5-1. This action breaks the hold voltage circuit to PK1 and K3 (to sequence machine power down) and opens contacts K3-2 (to indicate an incomplete power condition to the system).

Contactor PK1 Overload Contacts Open in Local: If an overcurrent condition occurs, the overload heaters connected in series with contacts PK1-1 and PK1-5 (Figure 5-2, sheet 1) will cause overload contacts PK1-6 and PK1-7 (sheet 2) to open, thus dropping relay K1. De-energizing relay K1 causes its associated contacts K1-1 to transfer, to turn on the CB/OC indicator lamp, and break the hold voltage circuit to contactor PK1 and relay K3. This removes power from the power supplies, power gate fan, and logic blowers.

Contactor PK1 Overload Contacts Open in Remote: The operation of the overload heaters, PK1-6 and PK1-7 contacts, and associated circuits is the same as detailed in local operation, except for the following. When relay K1 is de-energized, K1-1 contacts transfer, which de-energizes relay K5 to open its associated contacts (K5-1) and break the hold voltage circuit to PK1 and K3, sequencing the power down. Relay contacts K3-2 are also opened to indicate an incomplete power condition to the system.

Reset of PK1 Overload Contacts: After an overcurrent condition has occurred and been corrected, the PK1 reset pushbutton must be depressed to close overload contacts PK1-6 and PK1-7 and permit relay K1 to pick. If the unit is in local, the PWR ON pushbutton (S2B) is depressed, causing contactor PK1 and relay K3 to pick, sequencing power on. If the unit is in remote operation, the LOCAL-REMOTE switch should be placed in the LOCAL position and the PK1 reset pushbutton should be reset; then, the power can be turned on by depressing the PWR ON pushbutton.

After machine power has been turned on, the LOCAL-REMOTE switch (S1A) can be returned to the REMOTE position.

Overtemperature Conditions: If an overtemperature condition is sensed in the power or logic areas, power is sequenced down in the following manner. When the unit is operating in remote, relay K2 drops, causing K2-1 contacts to transfer and open the circuit to relay K5. With relay K5 de-energized, contacts K5-1 open and PK1 and relay K3 drop, causing machine power to sequence down. Contacts K3-2 open to indicate an incomplete power condition to the system. When the machine is in local operation, relay K2 de-energizes, opening its associated contacts K2-1. This, in turn, opens the hold circuit to PK1 and K3, causing machine power to cycle down.

If a delay-line overtemperature is sensed during remote operation, relays PK2 and K4 drop, PK2-1, and PK2-2 contacts open to turn off the delay line heaters, and K4-3 contacts open, de-energizing relay K5. Contacts K5-1 open to break the hold voltage circuit to PK1 and K3. Relay contacts K3-2 are also opened to indicate an incomplete power condition to the system as the unit power sequences down. In local operation, relays PK2 and K5 drop, and PK2-1 and PK2-2 contacts open to turn off the delay-line heaters. Relay contacts K4-3 open to break the hold voltage circuit to PK1 and K3, thus sequencing unit power down.

Thermal Circuit Reset: After the overtemperature switch has reset (normally closed condition), the thermal reset pushbutton (S1) should be depressed to energize relays K2, K4, and PK2. Machine power can be sequenced on (PK1 and relay K3 energized) by depressing the power on switch (S2B) if the unit is in local operation. During remote operation, place the LOCAL-REMOTE switch (S1A) to LOCAL, and depress the thermal reset and PWR ON pushbuttons. After power has sequenced on, return switch S1A to REMOTE position.

DC Power Supplies

The dc power supplies used to provide the dc voltages required to operate the 2848 serviced by a 50-cycle source are the same as those required for 60-cycle operation. These basic supplies are listed, by voltage rating and part number, under DC Power Supplies for the 60-cycle power system.

INTRODUCTION

This chapter describes the functions of the controls and indicators located on the operator and CE panels of the IBM 2848 Display Control. The panels are illustrated in Figures 6-1 and 6-2.

Also described are the control keys of the 2260 Display Station. The function of each key (for both nondestructive and destructive cursor operation) is provided. The alphanumeric and numeric keyboards available as features for the 2260 are also described and illustrated (Figures 6-5 and 6-6).

CONTROLS AND INDICATOR FUNCTIONS

2848 Display Control, Operator's Panel

The controls and indicators mounted on the operator's panel of the 2848 Display Control are shown in Figure 6-1. Their function is described in Figure 6-3.

2848 Display Control, CE Panel

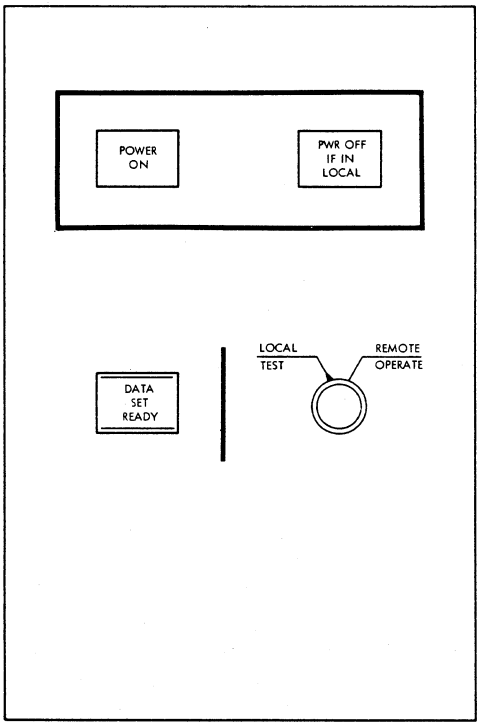
The controls and indicators mounted on the CE panel of the 2848 Display Control are shown in Figure 6-2. Their function is described in Figure 6-4.

2260 Display Station

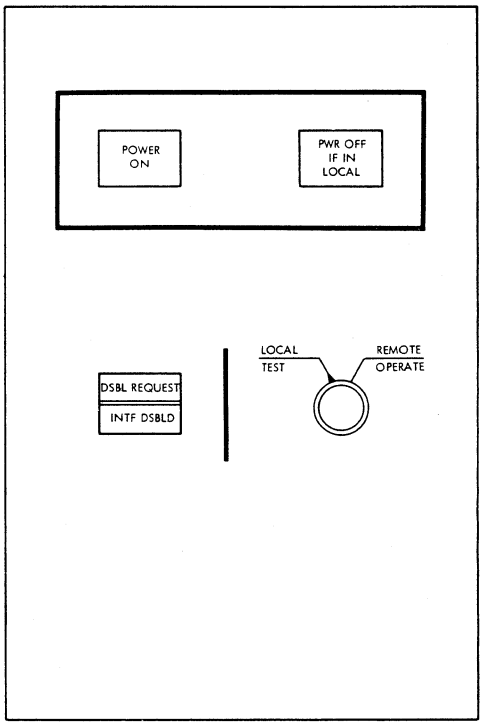
Operating Control

One combination function control is provided for operator use on all models.

1. Power on/off. Used to control primary power. Activated by push/pull motion of switch.
2. Character Brightness. Used to adjust intensity of the symbols displayed in the CRT. Activated by rotary motion of the switch.



Notes:
1. This panel is used on units equipped with data set adapter of System/360 channel interface without the Isolation Feature.
2. PWR OFF IF IN LOCAL appears on units using System/360 channel interface. Units equipped with data set adapter are labeled PWR OFF.



Notes:
1. This panel is used on units using System/360 channel interface with the Isolation Feature.

Figure 6-1. Operator's Panel - IBM 2848

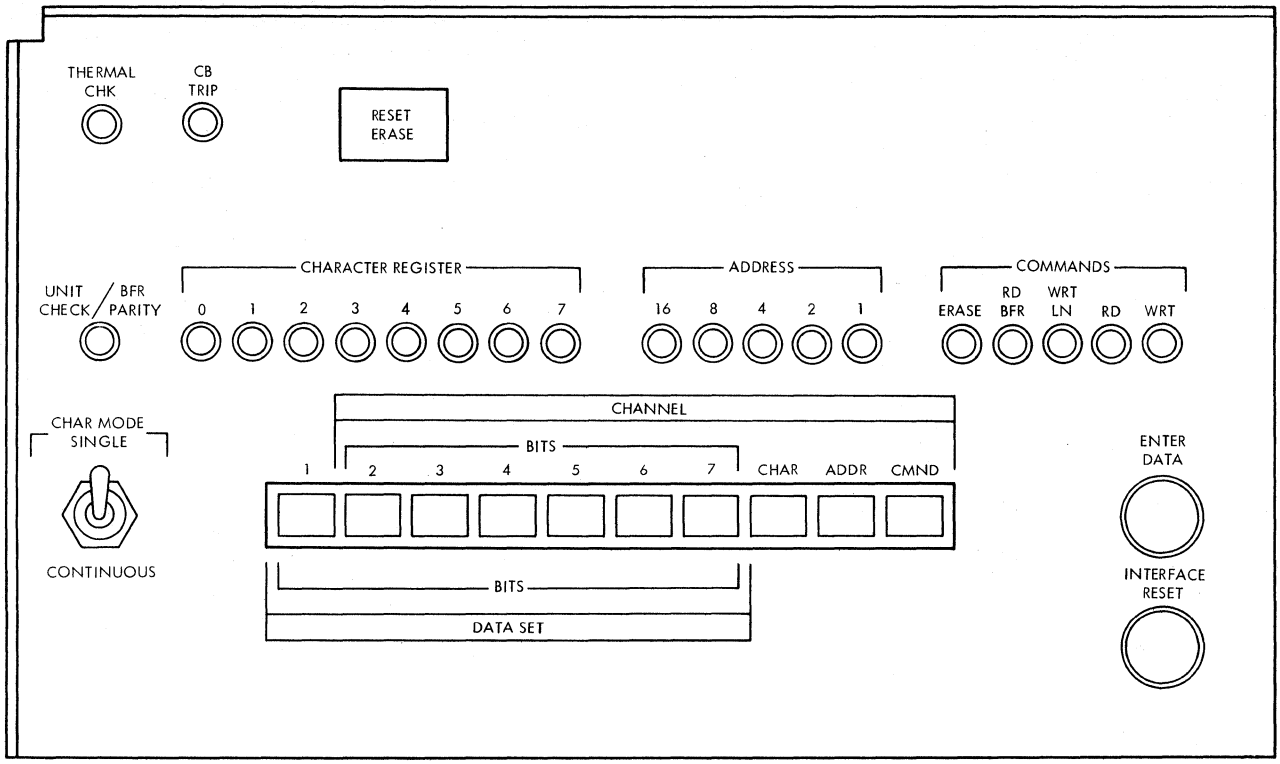


Figure 6-2. CE Panel - IBM 2848

Alphanumeric Keyboard

The alphanumeric keyboard (optional feature), fitted to the basic 2260 Display Station, is illustrated in Figure 6-5. The keyboard contains the 26 letters of the English alphabet, Arabic numerals 0-9, special symbol keys, and the control keys required to format and enter the input message.

Numeric Keyboard

The numeric keyboard (optional feature), fitted to the basic 2260 Display Station, is illustrated in Figure 6-6. The keyboard contains Arabic numerals 0-9 and a set of control keys similar to those provided in the alphanumeric keyboard.

Control Key Functions

The action that occurs when the various keyboard control keys are depressed is discussed in the following paragraphs. The description presented is applicable to both the standard destructive cursor and the optional nondestructive cursor.

The display symbols associated with control key functions, where applicable, are as follows:

1. Start MI symbol ▶
2. New Line symbol ◢
3. Destructive Cursor ABC ▬
   The small horizontal bar is the cursor symbol; it denotes the next available display position. Thus, if the D character key were depressed, the display above would be extended to ABCD▬.
4. Nondestructive Cursor ABC▮
   The vertical line is the cursor symbol. The next available display position is above and to the right of the vertical line (cursor). Thus, if the D character key is depressed, the new display appears as ABCD▮.

The control keys described in Figure 6-7 appear on all 2260 Display Station keyboards, even when the feature associated with a particular key has not been attached to the 2848 Display Control. For example, the PRINT key is present when the 1053 Printer adapter has not been selected for attachment to the 2848. The data provided for each control key includes a description of the effect of depressing the key when the associated feature is not present.

Control	Panel Designation	Type	Function
POWER ON	S2	Pushbutton/Indicator	Depressing this switch will energize the main power contactor and fans and cause a master reset of the DC. When power is on, the indicator is lit. NOTE: On a DC with a System/360 channel interface, the POWER ON switch is operative with LOCAL TEST/ REMOTE OPERATE switch in LOCAL TEST position only. On a DC with a data set interface, POWER ON switch operates independently of LOCAL TEST/REMOTE OPERATE switch.
PWR OFF IF IN LOCAL*	S3	Pushbutton	Depressing this switch will de-energize power supply fans and most control relays. Convenience outlets, control preparatory circuits, and delay line heaters remain energized. NOTE: This switch is interlocked with LOCAL TEST/REMOTE OPERATE switch in same manner as POWER ON. See Note above.
LOCAL TEST/REMOTE OPERATE	S1	2-position rotary	The LOCAL TEST/REMOTE OPERATE switch is used to select remote or local power on/off control. When in LOCAL TEST, power switches are operative. When this switch is REMOTE OPERATE and display control unit is used with System/360 channel interface, power switches are inoperative.
DATA SET READY	I1	Indicator	Indicates status of associated data set. Operative only on units with data set interface.
DSBL REQUEST/ INTF DSBLD	S4	Pushbutton/Indicator	Is used on channel interface unit equipped with the Isolation Feature. Depressing this switch prepares the unit for a logical disconnect from the system. The DSBL REQUEST (upper) indicator lights when the operator initiates a disable request by depressing the DSBL REQUEST/INTF DSBLD pushbutton. The INTF DSBLD (lower) indicator lights after the DSBL REQUEST lights and the Clock Out signal has dropped (manual or programmed stop). NOTE: After INTF DSBLD lights, the PWR OFF IF IN LOCAL and LOCAL TEST/REMOTE OPERATE switches may be operated.

*This control is labeled PWR OFF IF IN LOCAL on units equipped with System/360 channel interface and PWR OFF on units using the data set adapter.

Figure 6-3. 2848 Display Control Operator's Panel Controls and Indicators

Control	Panel Designation	Type	Function
THERMAL CHK	11	Indicator	When lit, indicates that a thermal sensor has detected a thermal overload condition within its region and dc power has dropped.
CB TRIP	12	Indicator	When lit, indicates that a CB has tripped and dc power has dropped.
UNIT CHECK/ BFR PARITY	13	Indicator	This indicator is lit in Test mode by a buffer parity error during transfer to the interface from the 2848 unit or when the printer is not ready. The indicator is lit in Operate mode when the Unit Check bit is set in the System/360 interface status byte.
CHARACTER REGISTER	14 through 111	Indicators (8)	Indicates eight data register bits corresponding to bits 0 through 7 of the right-bit EBCDIC code or bits 1 through 7 of the 7-bit ASCII code stored in the interface character register.
ADDRESS	112 through 116	Indicators (5)	Indicates the 5-bit address configuration of the 2260 Display Station using the interface.
COMMANDS ERASE READ BFR WRITE LINE READ WRITE	117 through 121	Indicators (5)	On 2848 Display Control units with a System/360 channel interface, these indicators light when Write, Read MI, Write Line Address, Read Full Buffer, or Erase commands have been entered into the interface command register through the interface or through the CE panel. On 2848 units with a data set interface, they indicate when the Specific Poll, General Poll, Read MI, Write Line Address, Write, or Erase/Write commands have been entered through the interface or CE panel.
RESET ERASE	S1	Pushbutton switch	When depressed, resets the interface and 2848 and erases all information stored in the 2848 buffers and the 1053 (if present).
CHAR MODE SINGLE/ CONTINUOUS	S2	Toggle Switch	Selects single-character mode or continuous run.
BITS	S3 through S9	Pushbutton switch	Data switches used in conjunction with CHAR, ADDR, or CMND switches to enter data into the appropriate registers of the interface.*
INTERFACE RESET	S14	Pushbutton switch	Resets all registers in the interface, and restores the control latches to nonselected condition.

*BIT (data) switch settings are as follows:

1	2	3	4	5	6	7	
0	0	0	0	0	0	1	Write command
0	0	0	0	0	1	0	Read command
0	0	0	0	1	0	0	Write Line Address command
0	0	0	1	0	0	0	Read Full Buffer command
0	0	1	0	1	1	1	Erase command

Figure 6-4. 2848 Display Control CE Panel Controls and Indicators

Figure 6-5. 2260 Display Station Alphanumeric Keyboard

Figure 6-6. 2260 Display Station Numeric Keyboard

Key	Standard Destructive Cursor		Optional Nondestructive Cursor	
	No Shift	Shift	No Shift	Shift
SHIFT	Provides Shift column function for control keys or enables selection of special characters on upper half of keys.		Same	
SPACE/ERASE ADVANCE	Causes storage of a blank in the cursor position. Advances cursor to next display position.	Same	Advances cursor one display position with no other modification of display	Erases display position to the right of the cursor and advances cursor one display position.
BACKSPACE	Backs cursor by one position, erasing character (if any) previously displayed in new cursor position. If cursor is in first display position, it will move to last display position.	Same	Backs cursor by one position with no erasures. If cursor is in first display position, it will move to last display position.	Same
ERASE DISPLAY (can be operated any time	Puts check symbol in cursor position. Cursor moves to next display position	Erases entire display and locates cursor in upper left corner of display (first displayable position).	Puts check symbol in cursor position. Cursor moves to next display position.	Erases entire display and locates cursor in upper left corner of display area (first cursor position).
START UP	Causes a blank to be written and moves cursor one display position.	If no Start MI symbol is displayed, the Start MI symbol is placed in the position the cursor was in when key was depressed. The cursor is advanced one display position. If a Start MI symbol is displayed when key is depressed, all display data between the Start MI symbol and the cursor, except data to the right of a new line character, is erased. Cursor moves to first display position following Start MI symbol. (See Notes 1 and 2.)	Cursor moves up one line on the display. If cursor is already in top line, it will go to the last line. The lateral position of the cursor within the display remains constant.	If no Start MI symbol is displayed, the Start MI symbol is placed in the position the cursor was in when key was depressed. The cursor is advanced one display position. If a Start MI symbol is displayed when the key is depressed, all display data between the Start MI symbol and the cursor, except data to the right of a new line character, is erased. The cursor moves to first display position following the Start MI symbol. (See Notes 1 and 3.)
ENTER	Puts check symbol in cursor position. Cursor moves one display position.	Upon receipt of the Read or Short Read DS MI command, all data between the Start MI symbol and the cursor is transferred to the computer, except data between an NL symbol and the end of the display line containing the symbol. After a successful message transfer, the cursor remains in its previous position and the Start MI symbol is deleted for a Read MI.	Puts check symbol in cursor position. Cursor moves one display position.	Places the End of Message symbol (▬) in the cursor position. Upon receipt of the Read or Short Read DS MI command, all data between the Start MI symbol and the End of Message symbol is transferred to the computer via the 2848. If this data contains an NL symbol, the data between the NL symbol and the end of the line containing it is not transferred.

Figure 6-7. Function of 2260 DS Control Keys (Sheet 1 of 2)

Key	Standard Destructive Cursor		Optional Nondestructive Cursor	
	No Shift	Shift	No Shift	Shift
ENTER (continued)		For a Short Read MI, the cursor is located one position beyond the previous cursor position and the Start MI symbol remains displayed.		After a successful message transfer (Read MI), the cursor remains in its previous position and the Start MI symbol is deleted. After a Short Read MI transfer, the cursor is located one position beyond the EOM symbol and the Start MI symbol displayed.
PRINT	Causes a check symbol to be put in the cursor position. Cursor moves to next position.	Causes all data between first display position in first line and the cursor symbol, except data to the right of an NL symbol in any line, to be printed by the 1053 Model 4 Printer. If no print feature is attached to the 2848, a space is written in the cursor position and the cursor moves to the next position.	Causes a check symbol to be put in the cursor position. Cursor moves to next position.	Places the EOM in the cursor position. Causes all data between first display position in first line and the EOM symbol, except data to the right of an NL symbol in any line, to be printed by the 1053 Model 4 Printer. If no print feature is attached to the 2848, a space is written in the cursor position, and cursor position, and cursor moves to next position.
NEW LINE DOWN	A blank is written. Cursor moves to next position.	Places the NL symbol in the cursor position. The cursor moves to the first display position of the next lower display line. If it is already in the bottom line, it moves to the first display position of the top line. Data between the NL symbol and the end of line is left undisturbed.	Cursor moves down one line. If it is already in the bottom line, it moves to top line. The lateral position within display remains constant.	Places the NL symbol in the cursor position. The cursor moves to first display position of next-lower display line. If it is already in the bottom line, it moves to first display position of the top line. Data between the NL symbol and the end of the line is left undisturbed.
Single-Character Keys	Cause symbol to be displayed.	Put check symbol in cursor position. Cursor moves to the next display position.	Cause symbol to be displayed.	Put check symbol in cursor position. Cursor moves to next display position.
Double-Character Keys	Cause function on lower half of key to be performed.	Cause function on upper half of key to be performed.	Cause function on lower half of key to be performed.	Cause function on upper half of key to be performed.

Notes:

1. Correct operation of the start (cancel) function requires that the cursor not be located to the right of an NL symbol. If the cursor is located to the right of a NL symbol, the following will happen:
   a. The characters to the left of an NL symbol and the first NL symbol will be erased (cancelled) as normally occurs; or, if no NL symbol is present, all characters in the line will be erased.
   b. The start symbol will be erased.
   c. The 2848 control will keep erasing (cancelling) until the cursor is found. The operation will end when the cursor is found, leaving the cursor at its starting location.
2. An NL symbol immediately following the Start MI symbol will not be the last character on the line to be erased. It will be treated like the other characters.
3. If the NDC cursor is in the same location as the Start symbol ($BA_{I}\blacktriangleright$), depression of the START key will cause the cursor to be moved to just after the Start symbol ($BA\blacktriangleright_{I}$). No other change will be observed on the display.

Figure 6-7. Function of 2260 DS Control Keys (Sheet 2 of 2)

Physical Description:

	Model	Width (in.)	Height (in.)	Depth (in.)	Weight (lbs)
IBM 2848 (with covers)	1	62-3/4	70-3/4	32-1/4	1000 (max)
	2	62-3/4	70-3/4	32-1/4	1000 (max)
	3	62-3/4	70-3/4	32-1/4	1000 (max)
IBM 2260		14	17-1/2	13	30
IBM 2260 (with keyboard attached)		14	17-1/2	19-1/2 (17 at base)	43

Interunit Cabling

Two cables (or a single combination cable) are required to connect the IBM 2848 and each associated IBM 2260 Display Station. When two cables are used, the conductor requirements for each cable are:

1. A single-conductor coaxial cable to transfer composite video.
2. A multiconductor cable to transfer keyboard data and control signals.

The single combination cable must contain the conductors listed in both 1 and 2.

The cables between the IBM 2848 and each IBM 2260 and between the 2848 and the IBM 1053 may be up to 2000 feet in length.

Power Requirements:

IBM 2848 Display Control Unit: 208vac/230vac, ±10%, single-phase, 3-wire

IBM 2260 Display Station: 115vac ± 10%, 60 ± 1/2 cps

Environmental Conditions:

IBM 2848 Display Control: 60° F to 90° F, 8%-80% Relative Humidity

IBM 2260 Display Station: 50° F to 110° F, 8%-80% Relative Humidity

Character Positions for One CRT Display

Model	No. of Rows	No. of Characters per Row	Total Characters
1	6	40	240
2	12	40	480
3	12	80	960

CRT Display:

Raster Orientation: High Speed - Vertical; Low Speed - Horizontal

Character Brightness: Light Ambients up to 50 foot-candles.

Keyboard Key Execute Times:

Alphabetic key	0.8 ms
Numeric key	0.8 ms
Space	0.8 ms
Backspace	16.7 ms
Start MI	16.7 ms to 400 ms*
Erase	8 ms to 24.5 ms
New Line	1.8 ms to 16.7 ms
Up	16.7 ms
Down	21.7 μs or 16.7 ms (if on bottom line).

CHARACTERISTIC	DESCRIPTION
Keyboard Key Execute Times (cont):	
Enter**	16.7 ms + 0-16.7 ms (maximum) + I/O + ending time***.
Print	2.2 ms to 17.5 ms for first two characters. Additional characters require 1.2 ms. When the printer buffer is full, additional characters require 0.8 ms per character every 67.5 ms.

*It requires 400 ms to cancel 959 characters. If the cursor is improperly to the right of an NL line code, it can exceed 400 ms.

**The I/O time is approximately 0.4 ms/character. All lines except the starting and ending lines take a multiple of 16.7 ms regardless of the number of characters on the line. A 33.4-ms pause occurs after each line is transferred. The ending time for a Read MI command is 33.4-50.1 ms. The ending time for a Short Read DS MI command is 0.4 ms. The ending time for a Read Full DS Buffer command is 16.7 ms.

***Including read time.

INTRODUCTION

This appendix describes the theory of operation of SMS circuits designed specifically for IBM 2848 Display Control applications. The theory of operation of each circuit is limited to the circuit block configuration as it appears in the ALD, theoretical timings when required, and a general description of circuit input and output signals. Special circuits employed in the control unit described in this appendix consist of:

1. Integrator Card A, Type FYM
2. Integrator Card B, Type FYN
3. Four Diode Coupled, 3-Way AND Circuit, Type FZK
4. Video Mixer, Type EFY
5. Output Sense Level and Sense Gate, Type FYZ
6. Reed Relay Card, Type FYF
7. Reed Relay Card, Type YPM

INTEGRATOR CARD A, TYPE FYM

- Converts +48vdc voltage level supplied by keyboard contacts to standard Y level.
- When input voltage drops (+48vdc to 0v), the circuit supplies a negative pulse of -12vdc.

The integrator card A, Type FYM, contains four voltage converter networks which translate a +48vdc level supplied by the keyboard to a -12vdc (-Y level) required by the display control circuits. Each network shown in block form in Figure B-1 is associated with a corresponding bit that makes up a coded character from the keyboard. The input

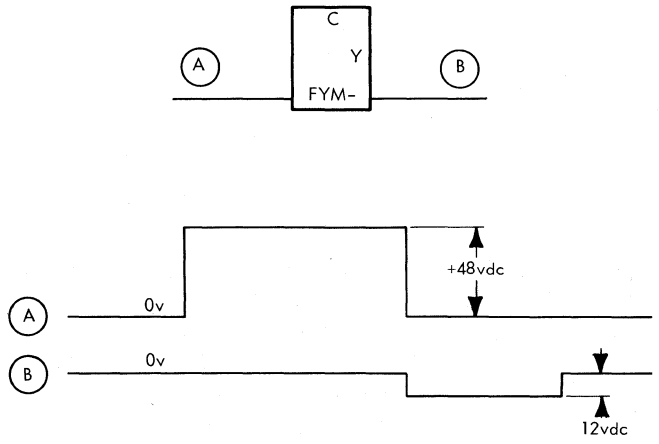


Figure B-1. Integrator Card A, Type FYM

is either +48vdc or is open-circuited. During these voltage conditions, the output supplied by the converter is 0v. However, during the time when the input falls from +48vdc to 0v, the fall transition is integrated by an RC network and the output rises to approximately -12vdc. This output is used to decode keyboard data associated with each key.

INTEGRATOR CARD B, TYPE FYN

Integrator Card B, Type FYN, is similar to Card A, Type FYM, described above. It also contains four voltage converter networks that translate a +48vdc input level to -12vdc (-Y level) required by the display control circuits. The networks associated with keyboard data inputs are identical with those used in Card A. The network associated with keyboard strobe, however, is modified to provide additional driving capability necessitated by its characteristic load. Additional drive is derived by modifying the strobe RC network (by increasing the value of its RC time constant) to provide the additional output.

FOUR DIODE COUPLED 3-WAY AND CIRCUIT, TYPE FZK

- Provides negative AND function, followed by negative OR function.
- Output signals are used as inputs to the video mixer.

The four diode coupled 3-way AND circuit, Type FZK (Figure B-2), performs a negative AND function by employing the In Phase signal in the first bank of AND circuits. Note that Y levels are used as inputs and outputs to the logic blocks. The configuration shown is designed specifically to supply Video Voltage levels to the video mixer. Video signals read out of the display adapter storage buffers are gated by the AND's and supplied as inputs to the OR whenever each AND is conditioned. The output (video) of the OR is fed to the video mixer where the display station composite signal of video and sync is generated.

VIDEO MIXER, TYPE EFY

- Provides composite signal comprising video and synchronization pulses required by the display station.

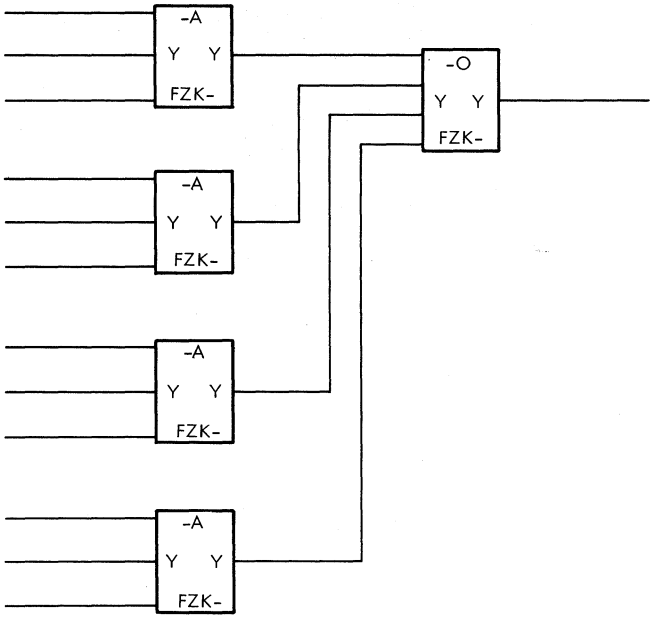


Figure B-2. Four Diode Coupled 3-Way AND Circuit, Type FZK

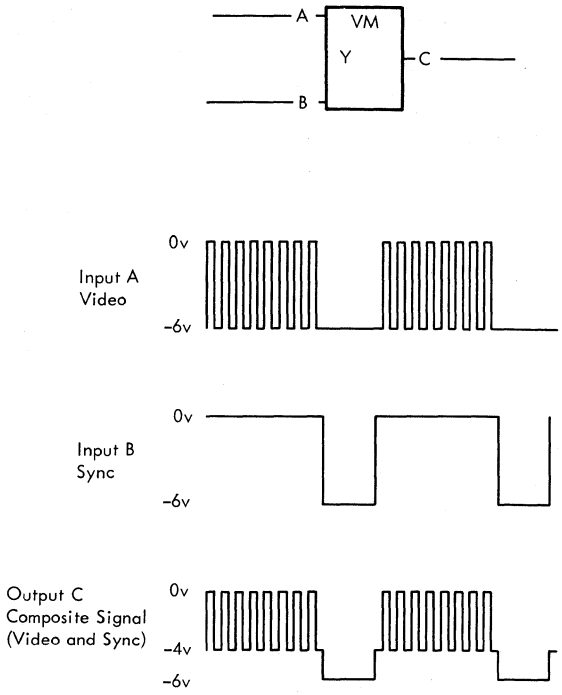


Figure B-3. Video Mixer, Type EFY

- Circuit is capable of providing signals of sufficient drive to operate a remote display station up to a distance of 2000 feet.

The video mixer (Figure B-3) combines video signals received from the display buffers with synchronization pulses supplied by the sync generator into one composite signal. This signal is fed over a 93-ohm transmission line to a display station that can be located up to a maximum of 2000 feet from the control unit. Video signals are applied to Input A shown in Figure B-3, and the sync signals are applied to Input B. Note that both signal inputs are standard +Y levels. The video mixer output is a nonstandard composite signal of video and synchronization pulses.

SENSE GATE AND OUTPUT SENSE LEVEL, TYPE FYZ

- The sense gate (SG) and output sense level (OSL) circuits are packaged on the same SMS card.
- Sense gate circuit supplies two signals: a Sense Gate level which enables the sense amplifier to respond to memory core readouts and a Threshold level which specifies the operating point of the sense amplifier.
- The OSL circuit operates as a voltage regulator to compensate for variations in the ±12vdc supplies.

The output sense level (OSL) and sense gate (SG) circuits supply the threshold, gating, and compensation voltages required by the sense amplifier during video and code translation readouts from the character generator. One bit position involving these circuits is illustrated in Figure B-4. The OSL circuit compensates for voltage variations in the ±12vdc power supplies. If either dc supply varies because of line voltage variations, a compensating voltage approximately equal in value but opposite in polarity is fed to the SA. Thus, proper operation of the SA is ensured by maintaining its B+ supply constant. The compensating voltage supplied by the OSL when both of the 12vdc supplies are operating within prescribed limits is approximately 0v (ground level).

To better understand the operation of the SG circuit, it is necessary to consider the input signals required by the SA. Note from Figure B-4 that Input B to the SA is provided by a memory core while data is read out of the array. Output B corresponds to a 1 read out of the core. A 0-bit read out of the core results in the absence of the voltage shown. The core output must be accompanied by a gated level (waveform A), which is supplied by the SG, or the SA will not respond to the core input. Coincidence of core input B and gate pulse A results in the standard level shown as Output C. Also provided by the SG (Output D) is a variable dc voltage

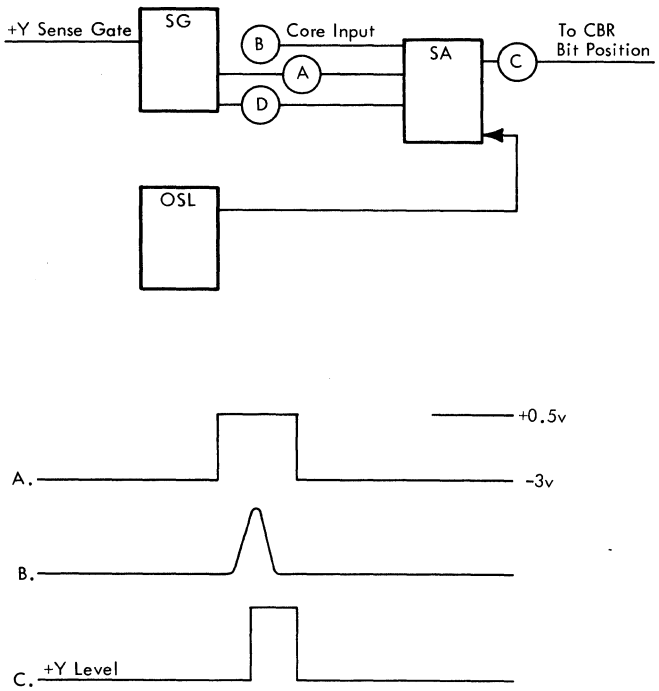


Figure B-4. Output Sense Level, and Sense Gate, Type FYZ

which is employed as a threshold voltage by the SA. This voltage aids in rejecting noise that may accompany the Core Input signal. The threshold voltage is adjusted to a value of -4vdc ±0.2v.

The timing relationship of the Core and Gate signals is extremely important because memory cores provide signals of low amplitude. The Gate pulse must also completely envelop the core output to ensure proper readout and bit detection. Therefore, it would be advantageous to control the turn-on of the SG within adjustable limits. This is accomplished by an adjustable delay circuit to time the Sense Gate level input to the SG. Sense gate delay and threshold voltage adjustment procedures are given in detail in the FE Maintenance Manual, Form Y27-2047.

REED RELAY, TYPE FYF

- The reed relay is a dc relay with one set of contacts.
- Contacts are normally open when relay is de-energized; contacts are closed when relay is energized.
- Four relay coils are packaged on one SMS card. Contacts associated with each relay coil are packaged on an extender card.
- An RCL spark suppressor network protects the relay contacts during break time.
- Reed relay logic block, as it appears in the ALD, is illustrated in Figure B-5.

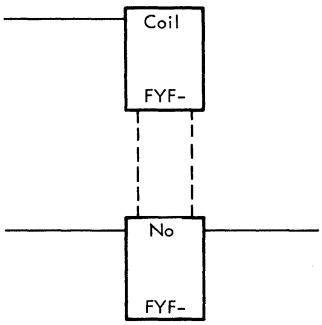
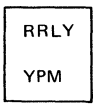


Figure B-5. Reed Relay, Type FYF

REED RELAY, TYPE YPM

- The reed relay is a dc relay with two sets of contacts.
- One set consists of two-pole double-throw contacts.
- The other set consists of a pair of NC contacts when the relay is not energized.
- Two relay coils are packaged on one SMS card.
- Reed relay logic block, as it appears on ALD, is shown in Figure B-6.



•Figure B-6. Reed Relay, Type YPM

FEATURE DESCRIPTION

This appendix discusses the language features which modify the display station keyboards, display control unit, and the 1053 printer. Modification of the domestic components is necessitated by language requirements in the country where the equipment is to be installed. These features encompass language variations for France, Germany, and the United Kingdom. System operation, as described for domestic machines, is affected only to the extent that certain unique characters have been substituted for those used in domestic machines. In addition, identification and instruction labels for use by operating personnel have been relabeled in the language of the country where the units are installed. The following paragraphs contain comparative descriptions of the areas affected when each of the language features is installed.

IDENTIFICATION AND INSTRUCTION LABEL CHANGES

Figure C-1 lists the control designations, identifications, and instruction labels as they appear on the French, German, or United Kingdom language features. Entries listed under the United Kingdom heading are the same as those employed on domestic machines. The function of the switches and indicators is given (by standard nomenclature) in Chapter 6, Console and Maintenance Features.

CHARACTER CODES

Figure C-2 contains the EBCDIC, ASCII, and keyboard codes for the language feature characters used by the 2848 Display Control. Code changes are required for the Ä, Ö, and Ü characters required for the German keyboard and the monetary unit symbols for the French and United Kingdom keyboards. The basic (domestic) characters replaced by the language feature characters are also listed in the figure.

CHARACTER GENERATOR MODIFICATION

The character generator is modified so that the monetary unit symbols (£ and f) and German characters (Ä, Ö, and Ü) can be displayed on the viewing screen of the CRT. Memory cells which make up the new characters are reconfigured to provide binary video data and the code conversions for the new symbols and characters that can be displayed. The new characters occupy the memory cell location for the corresponding characters listed in Figure C-2 for domestic machines.

1053 PRINTER PRINT ELEMENT

The standard 1053 printer print element is modified to provide the special symbols and characters applicable to the three language keyboards. (See Figure C-3.) All other characters on the print element are identical with those provided on the standard (domestic) print element. The language characters and symbols are made available merely by installing the applicable sphere-shaped typehead in its transport mechanism.

KEYBOARD CHANGES

Standard domestic key characters are changed in accordance with French, German, or United Kingdom language requirements. Each language feature-associated keyboard features the keyboard arrangement familiar in the country for which the feature is selected and the key designations in the language of that country. Function key notations are also altered as necessary. These key changes are summarized in Figure C-4 and described in the following paragraphs for each of the three language features.

French Keyboard

Figures C-5 and C-6 illustrate the French alphanumeric and numeric keyboards. Note that the function keys have been labeled in French. The standard domestic graphic character, $, is replaced with the French monetary franc symbol, f. Alphabet keys A, Z, and M are also interchanged with Q, W, and &, respectively, to agree with the standard typewriter keyboard used in France. Figure C-7 shows the keystem number and bail selection for each key of the alphanumeric keyboard. Keystem and bail selection for the French numeric keyboard is the same as that for the domestic keyboard except for the franc symbol noted above.

German Keyboard

Figures C-8 and C-9 illustrate the German alphanumeric and numeric keyboards. Function keys are labeled in German. The standard domestic graphic characters, #, @, and $, are replaced with

the German characters, Ä, Ö, and Ü. Note also that the standard alphabet keys, Z and Y, are interchanged. Keystem numbering and bail selection for the German alphanumeric keyboard is depicted in Figure C-10.

United Kingdom Keyboard

Figures C-11 and C-12 illustrate the United Kingdom alphanumeric and numeric keyboards. The United Kingdom keyboards are the same as domestic keyboards except for the monetary unit graphic character. The graphic character, $, is replaced with the English monetary unit pound symbol, £. For keystem numbering and bail selections applicable to the United Kingdom alphanumeric and numeric keyboards, refer to the applicable domestic keyboard (Figures 2-15 and 2-16).

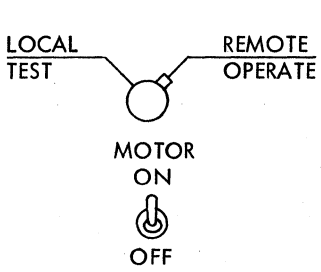
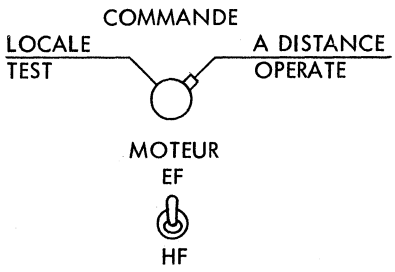
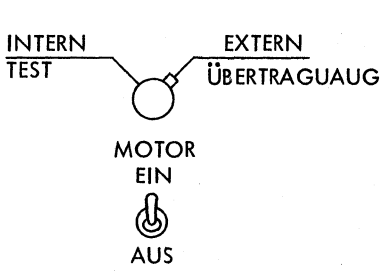
United Kingdom	French	German
DISPLAY CONTROL	UNITE DE CONTROLE D'AFFICHAGE	STEUEREINHEIT
MODEL	MODELE	MODELL
DISPLAY STATION	UNITE TERMINALE D'AFFICHAGE	OPTISCHE ANZEIGE
POWER ON	SOUS TENSION	NETZ EIN
POWER OFF	HORS TENSION	NET AUS
POWER OFF IF IN LOCAL	HORS TENS SI EN CDE LOC	NETZ AUS BEI STELLUNG INTERN
DATA SET READY	MODEM PRET	SIGNAL- UNSETZER IN BETRIEB
		
TO UNLATCH COVER: INSERT SCREWDRIVER IN SLOT AND PRY TAB IN DIRECTION OF ARROWS.	POUR DELOQUETER LE COUVERCLE: INTRODUIRE UN TOURNEVIS DANS L'ENCOCHE ET SOULEVER DANS LE SENS DE LA FLECHE.	VERKLEIDUNG MIT SCHRAUBENZIEHER IN PFEILRICHTUNG ÖFFNEN.

Figure C-1. Identification and Instruction Label Summary

Language Feature Character				EBCDIC Code								ASCII Code								Keyboard Code							
Basic Character	FC 2928 French	FC 2929 German	FC 2927 United Kingdom	0	1	2	3	4	5	6	7	7	6	X	5	4	3	2	1	C	2	3	4	5	6	7
#	#	Ä	#	0	1	1	1	1	0	1	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0
$	f	Ü	£	0	1	0	1	1	0	1	1	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0
@	@	Ö	@	0	1	1	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1

Figure C-2. Language Feature Character Codes

Typehead Print Element			
Domestic	French (FC 2998)	German (FC 2999)	United Kingdom (FC 2997)
#	#	Ä	#
@	@	Ö	@
$	f	Ü	£
"	■ (check)	■	■
!	■ (EOM)	■	■
¢	▶ (start)	▶	▶

Figure C-3. 1053 Printer Typehead, Language Symbol and Character Variations

Keyboard			
Domestic	French	German	United Kingdom
ERASE DISPLAY	EFF ECRAN	ANZEIGE LÖSCHEN	
SHIFT	⇧	UMSCH	
BKSP	⇦	⇦	
PRINT	IMP	DRUCH	
ENTER	TM	EIN-GABE	
NEW LINE	NL	NEVE ZEILE	
DOWN	↓	↓	
START UP	DM ↑	START ↑	
SPACE/ERASE ADVANCE	ESPACE/EFFACE	⇨/LÖSCHEN	
A	Q		
M	' &		
Q	A		
W	Z		
Y		Z	
Z	W	Y	
& ´	M		
$	f	Ü	£
#		Ä	
@		Ö	

Figure C-4. Graphic Character and Function Key Change Summary

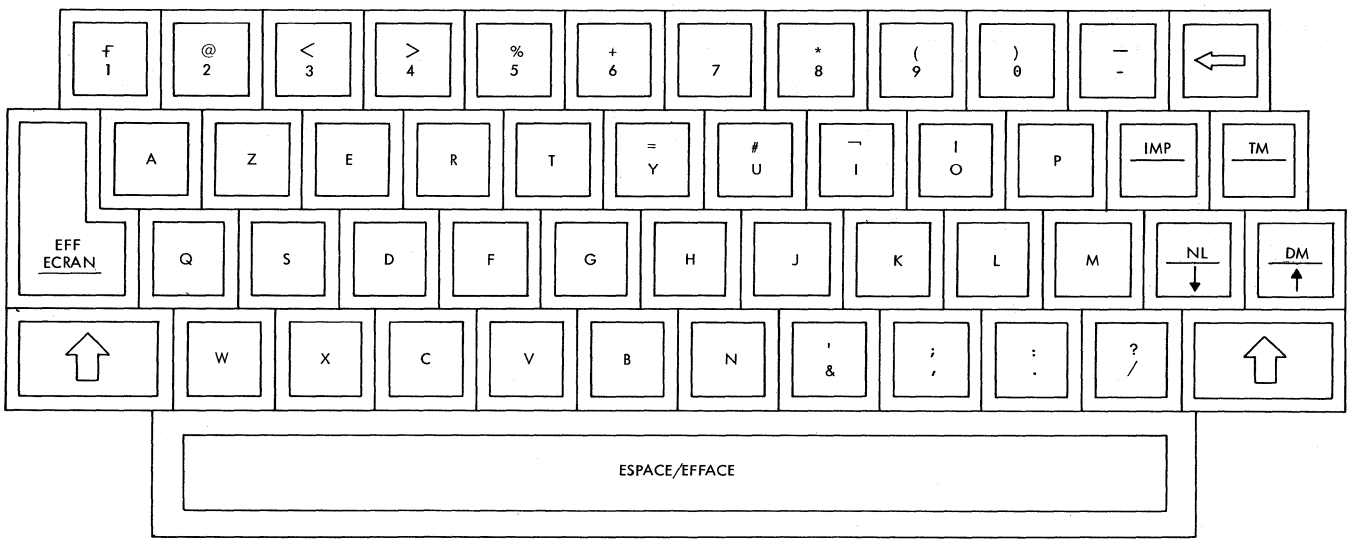


Figure C-5. French Alphanumeric Keyboard

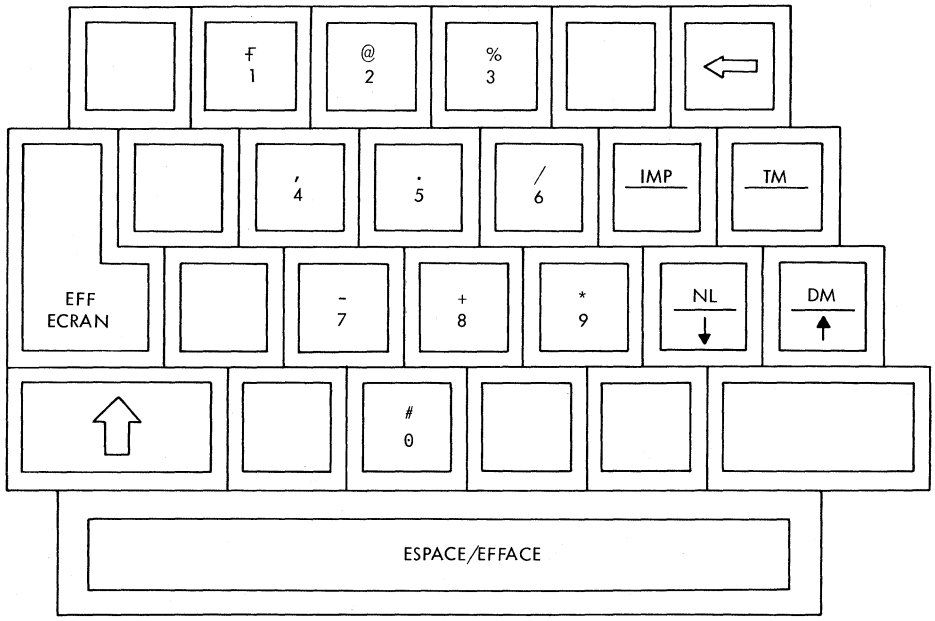


Figure C-6. French Numeric Keyboard

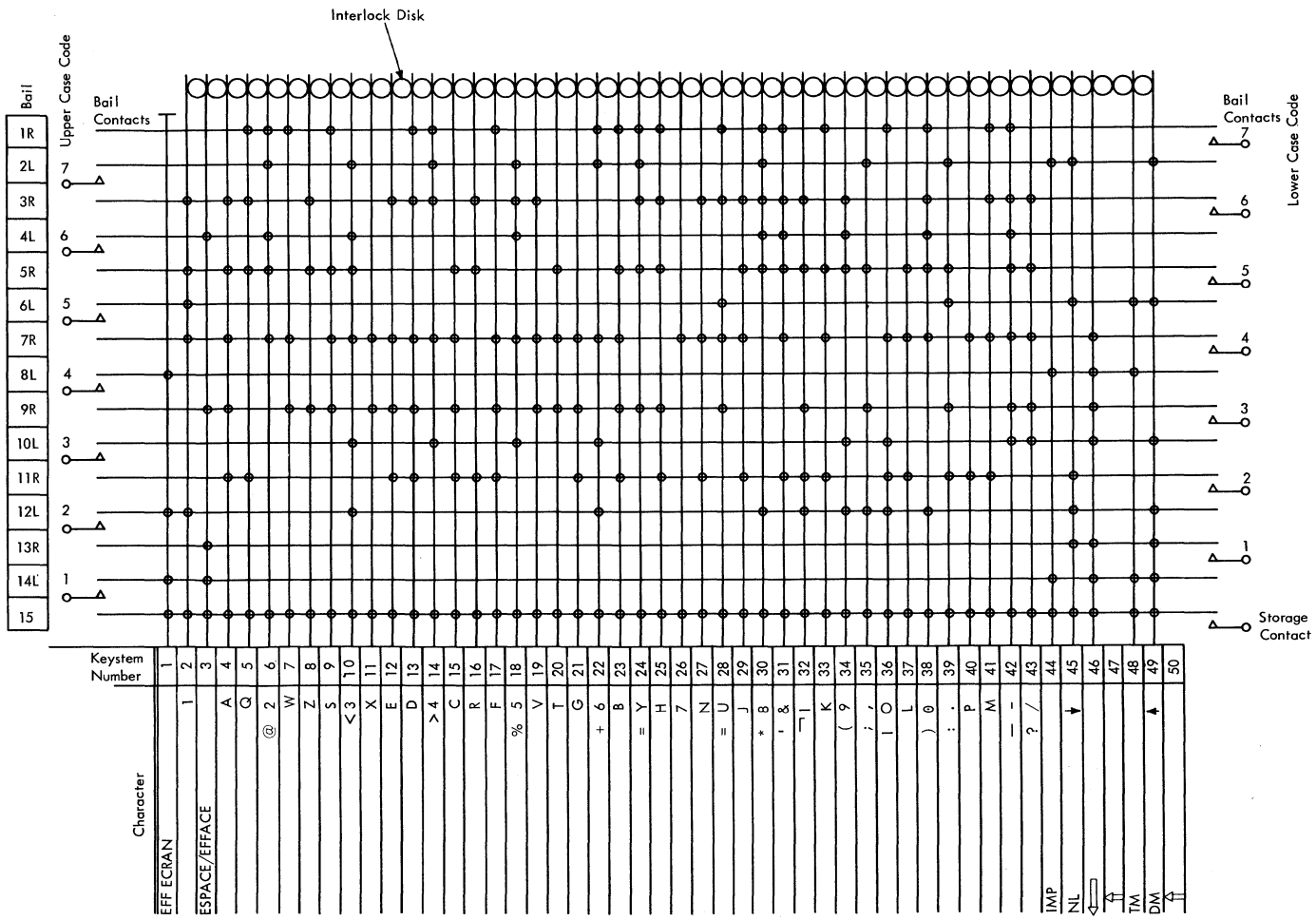


Figure C-7. Keystem Number and Bail Selection, French Alphanumeric Keyboard

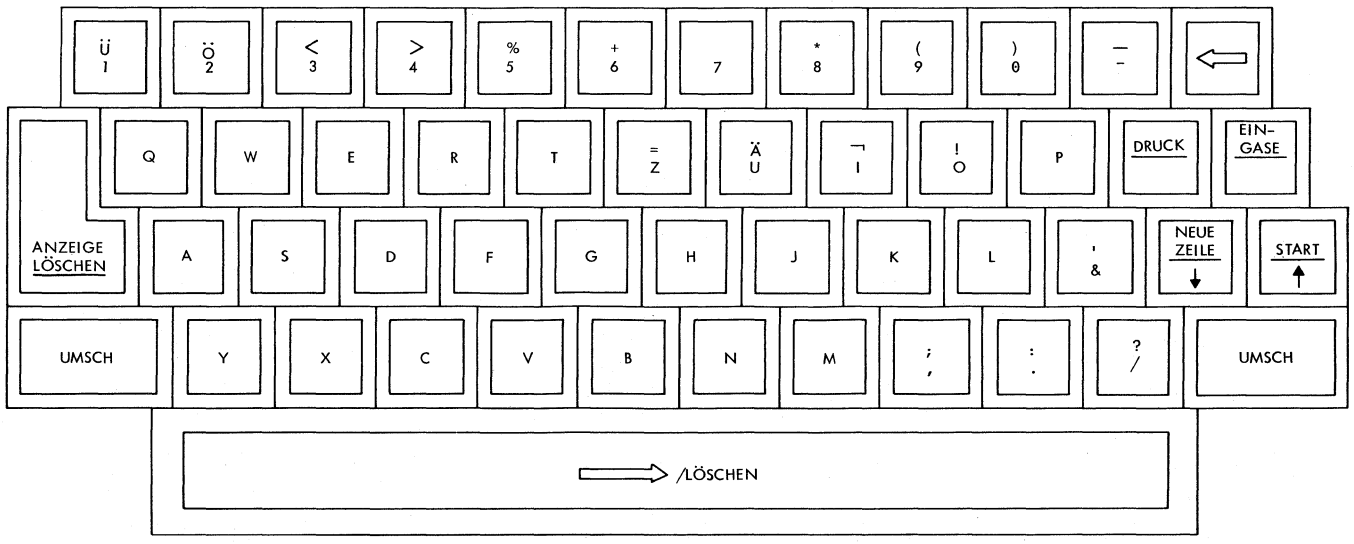


Figure C-8. German Alphanumeric Keyboard

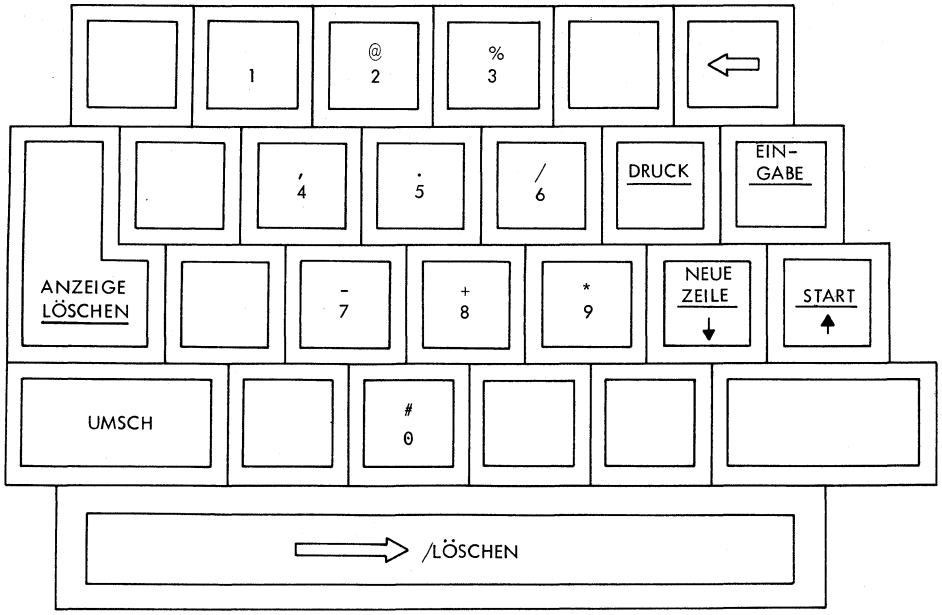


Figure C-9. German Numeric Keyboard

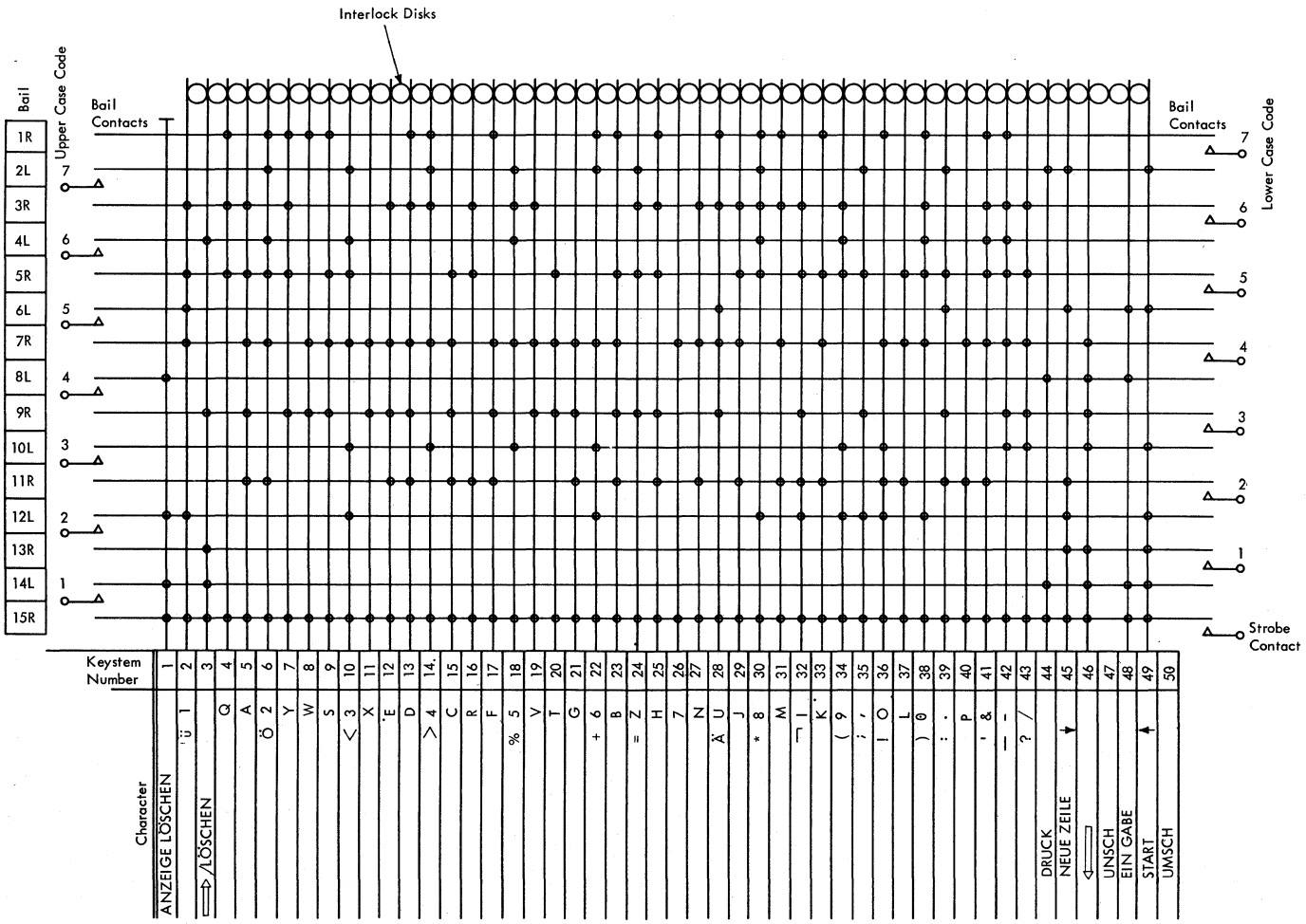


Figure C-10. Keystem Number and Bail Selection, German Alphanumeric Keyboard

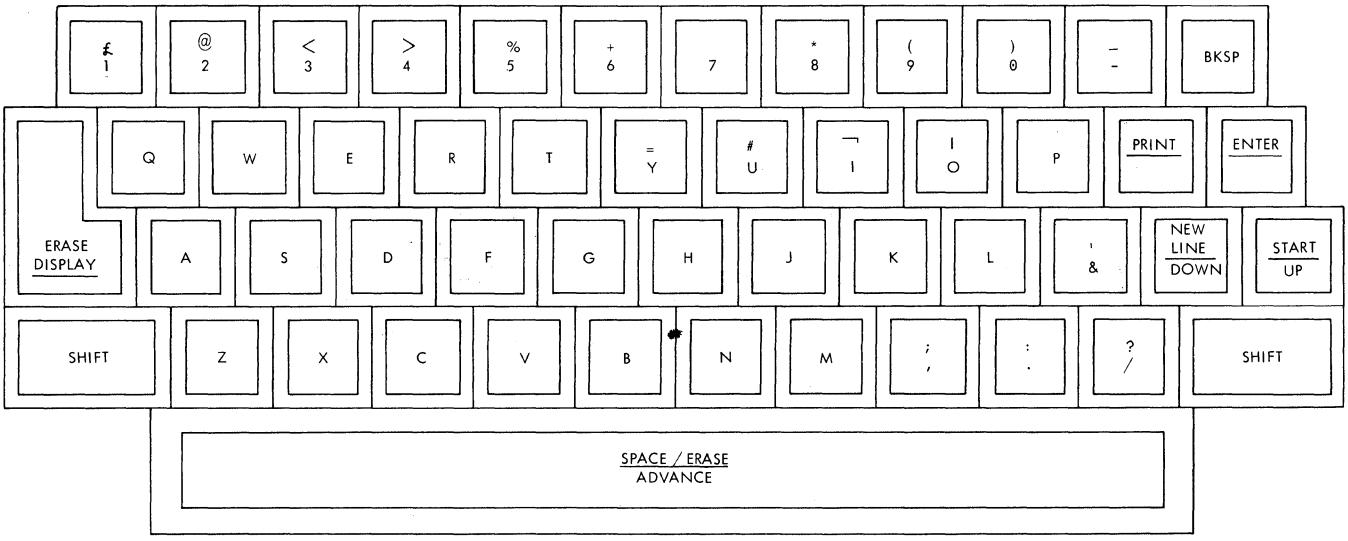


Figure C-11. United Kingdom Alphanumeric Keyboard

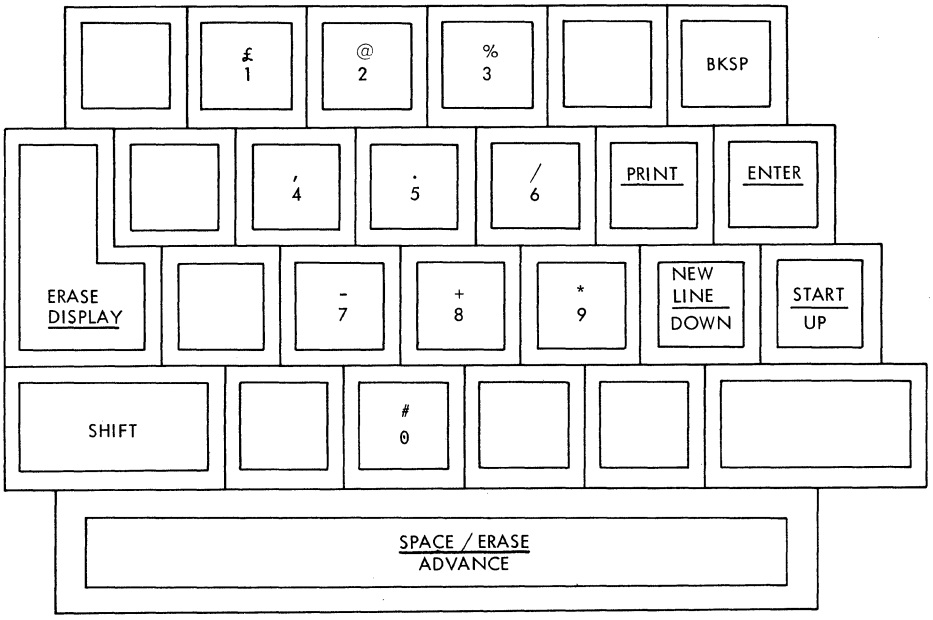


Figure C-12. United Kingdon Numeric Keyboard

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Y27-2046-3

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IBM **FE Supplement**

System/Unit	2260 Display Station 2848 Display Control
Re: Form No.	Y27-2046-2, -3
This Supplement No.	Y27-2190
Date	March 8, 1968
Previous Supplement Nos.	Y27-2165-0 Y27-2171

This supplement to the 2260 Display Station 2848 Display Control FETOM (Form Nos. Y27-2046-2 and -3) affects the 2260 section of Chapter 2 as follows:

1. Adds a description of a more recently manufactured circuit board.
2. Adds a description of older level circuit boards fitted with tube adapters.
3. Revises the keyboard electronics diagram.

This supplement affects two editions of the 2260 Display Station 2848 Display Control FETOM: Form Y27-2046-2, the basic manual which has been updated by two supplements; and Form Y27-2046-3, a reprint of the basic manual and which incorporates the two supplements made to the basic manual. To incorporate the revised pages, follow the page replacement procedure listed below regardless of whether a -2 or -3 manual is being updated:

1. Replace pages i through vi with new pages supplied.
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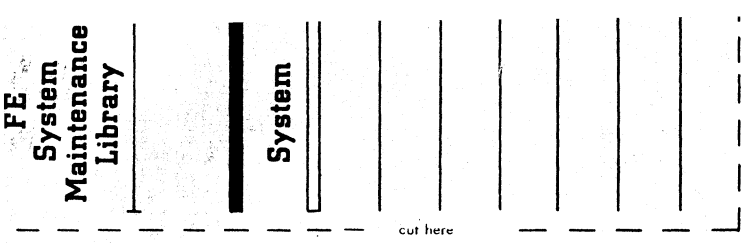

Y27-2046-3

IBM 2260/2848 - 60,000 Series Printed in U.S.A. Y27-2046-3

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