IBM

Field Engineering

Manual of Instruction

2075 Processing Unit — Volume 4

Special Features

Power Supply and Control

Appendix

PREFACE

This is one of six Field Engineering manuals for the 2075 Processing Unit. These six manuals contain the 2075 theory of operation, figures for reference when troubleshooting, and maintenance procedures.

The theory of operation is contained in four volumes (manuals of instruction). A prerequisite for studying these manuals is a basic knowledge of the IBM System/360 as contained in the IBM System/360 Principles of Operation, Form A22-6821. Volume 1 is a prerequisite for the detailed theory of operation contained in volumes 2, 3, and 4. Volume 1 contains the introduction to the system and the processing unit and a description of the functional units (registers, adders, and decoders) of the processing unit. Volumes 1-4 reference figures (four-digit references) contained in the diagrams manual.

The complete titles and form numbers of the six 2075 Field Engineering Manuals are:

2075 Processing Unit--Volume 1, Comprehensive Introduction, Functional Units, Field Engineering Manual of Instruction, Form 223-2872

2075 Processing Unit--Volume 2, Theory of Operation: Storage Bus Control; Instruction Preparation; FLT, Logout, MCW; Interrupts, Field Engineering Manual of Instruction, Form 223-2873

2075 Processing Unit--Volume 3, Theory of Operation: Fixed Point, I Execute, Branch, Floating Point, Variable Field Length, Field Engineering Manual of Instruction, Form 223-2874

2075 Processing Unit--Volume 4, Special Features, Power Supply and Control, Appendix, Field Engineering Manual of Instruction, Form 223-2875

2075 Processing Unit, Field Engineering Diagrams Manual, Form 223-2876

2075 Processing Unit, Field Engineering Maintenance Manual, Form 223-2880

ILLUSTRATIONS

LCS ATTACHMENT FEATURE

- A Model 75 system can have one to four 2365 storages plus one to four 2361 storages. The 2361 storages are referred to in this manual as large capacity storage (LCS).

- LCS storages come in two models:
    Model 1 - 128K double words
    Model 2 - 256K double words

- LCS cycle is 8 microseconds with a 3-microsecond access time.

- Two systems can share one or more 2361 units.

As a special feature, a Model 75 system can have one to four 2361 Core Storage units in addition to one to four 2365 Processor Storage units. The LCS units are available in two models:
    Model 1 - 1,048,576 bytes, or 131,072 (128K) 72-bit words.
    Model 2 - 2,097,152 bytes, or 262,144 (256K) 72-bit words.
The four possible LCS units can be in any combination of models. LCS storage units have an 8-microsecond cycle with a 3-microsecond access time.

The LCS attachment feature also allows a second system (Model 50, 65, or another 75) to share one or more of the LCS units.

The 2361 attachment feature is presently described in a separate FE Manual of Instruction, 2075 Processing Unit, LCS Attachment Feature, Form Z22-2913. The LCS attachment publication, presently IBM Confidential, will be added to this manual (Volume 4) in the future. Text pages 5-12 and three figure numbers have been reserved in this manual for the addition of the LCS attachment information: presently, the first text page in this manual is 13 and the first figure is Figure 4.

This section describes power control and distribution for all system components, including CPF, MCF, storages, and I/O devices. The various power-on conditions are shown by distribution diagram; the sequencing of power-on and power-off is shown by sequence charts. A theory of operation portion explains the reasons for certain sequencing routines, stepping switch operation, marginal checking of regulators, emergency power off (EPO) conditions, and thermal trip conditions.

Initial AC Power Distribution

Figures 9550 and 9551 show the distribution of all AC power in the system. Main 208 volts, 3-phase, 60-cycle power is available at the customer service outlet. When the service outlet circuit breaker is turned on, 3-phase, grounded, 4-wire power is applied to a feed-through capacitor box (YA631), where the ground wire is separated and attached to the frame ground bus. Lines 1, 2, and 3 are applied through overload circuit breaker CB11 (YA631) to EPO contactor K6. Lines 1 and 2 are applied through fuses F1 and F2 to the +24 volts DC power supply (YA631).

Initial 28-Volt AC and +24-Volt DC Distribution

Figure 9552 shows the conditions required to place 28-volts AC and +24-volts DC on their respective distribution buses. When all EPO switches are closed, +24-volts DC from the prime power supply is applied to EPO control relay K3 (YA631). When K3 picks, contacts of K3 apply the 28-volts AC and +24-volts DC outputs of the prime power supply onto the distribution buses. Any EPO switch opening removes the prime power supply outputs from distribution.

EPO relay K6 picks from the +24-volts DC at K3-19. Figure 9550 shows the subsequent AC distribution resulting from the closure of K6 contacts.

Fig. re 9553 shows the +24-volts DC distribution under power status 1, or standby, and without an EPO condition. The main power lamp is lit. All logic lamps may be tested by pressing the console lamp test key (YA661). Provided all interlocks are closed and all thermal sense contacts are normal, K10 and K12 pick (YA651). MCF thermal trip lamp DS1 (YA661) and the console MCF power check lamp (YA671) are off. Relays K11 and K26 (YA651) pick through contacts of K10, K12, and thermal reset switch Z3 (YA651), and are self-holding through contacts of K11.

If K12 drops due to a thermal condition, it can be reset only by pressing the console thermal reset key, thereby holding the thermal trip indication.

A valid CPF interlock and circuit breaker string allows K13 (YA661) to pick. Time delay relay K14 (YA651) picks five seconds after the +24-volts DC bus is energized.

Figure 9555 shows the power status 1 distribution sequence in flow diagram form. The rectangles contain the events, the ALD page in question is denoted to the left, and the circuits which implement the step are listed to the right. Power status 1 is necessary to place the system in readiness for the power up procedure.

Power Up Procedure

Figure 9554 shows the distribution of +24-volts DC to the various portions of the system once power status 1 has been achieved and the system power on switch is pressed. Figure 9555 denotes the sequence of events, along with the ALD page numbers and the listing of the circuits required to implement the sequence step.

Operation is initiated by pressing the console power on key, which picks K19 and K20. Contacts of K19 bypass the power on key and hold the relays on. Contacts of K19 pick K21 and K22. Note that should K19 drop, contacts 9 and 10 of K14 (which is dropped by K19-8, 9) hold the system power on for the five seconds required to again pick K14. The net effect is that storage power is allowed to drop five seconds prior to system shutdown, thus preventing a change of stored information because of inadequate logic circuit power.

Relay K27 prevents reactivation of the system power on switch until five seconds after power shutdown. This allows full capacitor discharge in the regulators.

Power Down Procedure

Figures 9554 and 9556 illustrate the power down sequence of events that are the same as described previously for the power down procedure.

Emergency Power Off (EPO) Conditions

System EPO Conditions

Figure 9552 shows the effect of a system EPO event. EPO control relay K3 drops, removing the +24-volt DC and 28-volt AC outputs of the prime power

supply from bus distribution. EPO contactor K6 is dropped; Figure 9550 illustrates the resultant effect upon main AC distribution. All bulk supplies are de-energized, along with the gate blowers, customer use meter, and convenience outlets.

All externally connected units lose power-hold capability when system relays K17 and K18 drop. Thus, a system EPO condition causes loss of not only system power, but a power down condition in all connected units as well. The +24-volt DC and 28-volt AC main power supply remains on, unless it caused the EPO event. All units in power status 1, Figure 9550, are dropped due to interruption of the +24-volt DC bus.

The system EPO switch is a mechanical latch-type switch that must be manually reset.

Unit EPO Conditions

When externally connected units, except the main storages, enter an EPO condition, the system power status remains unaffected. The unit power on lamp goes off, the unit power check lamp turns on, and the lamp behind the console power on key changes from white to red. The CE is cognizant that a unit power check has occurred, and a glance at the frame power indicators shows which frame caused the power check.

Thermal Conditions

Figure 9553 shows the effect of a thermal trip condition. If any normally-closed thermal sense switch opens in the regulators, gate A, or gate B, K12 drops. The MCF thermal trip lamp (DS1) and the console MCF power check lamp (S6) turn on. Thermal reset control relays K11 and K26 remain energized through the console thermal reset switch (Z3) and K11-6,7.

When the thermal reset key is pressed, K11 drops, and the energizing path for K12 is enabled

through the thermal sense switches, CR, and K11-5, 6 to +24-volt DC. If the thermal condition is over, K12 picks. If it is not over, pressing the thermal reset key has no effect.

When K12 drops it also drops relays K19 and K20 (Figure 9554), and the entire system, including all frames, shuts down. When thermal reset is accomplished, the system must be powered up by pressing the console power on key (W90).

The thermal reset key (Z3) may also be used to remotely actuate a unit thermal reset circuit.

THEORY OF OPERATION

With exception of the CE and customer use meter circuits and the voltage sense circuits, all units of the power distribution system are described in Field Engineering Manual of Instruction, Power Supplies, Form 223-2799. All metering circuits are described in Customer Engineering Manual of Instruction, Metering, Form 223-2728.

Voltage Sense Unit

The voltage sense unit, wiring diagram 5270760, shown on ALD page YA692, is schematically illustrated in Figure 4. The circuit uses three transistors and one relay to sense that all DC regulator outputs in the system are operating within tolerance.

The loss of any positive input causes relay driver Q3 to cut off, and the relay in the overvoltage assembly drops. The loss of any negative input causes cutoff of Q1, saturation of Q2, and again the cutoff of relay driver Q3. Thus, in either case the relay drops, giving an indication of power failure.

Regulator Sense Points

The points at which regulator output voltages may be measured are listed by frames in Figure 5.
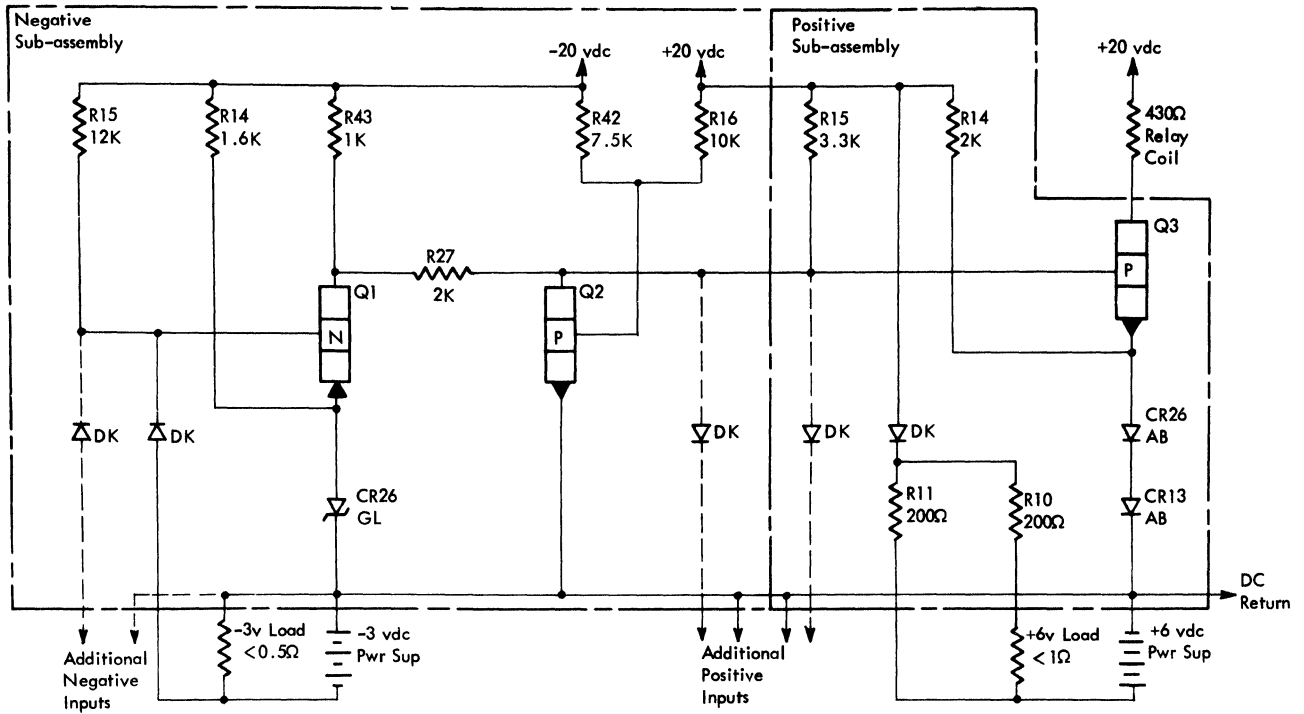
FIGURE 4. VOLTAGE SENSE CIRCUIT, SCHEMATIC

	Regulator	Voltage	Sense Point	
CPF	1	∕3	KU3BD-12 (11)	
	2	∕3	KU3BD-6 (5)	
	3	∕3	JU3BD-12 (11)	
	4	∕3	HU3BD-12 (11)	
	5	∕6M	JU3BD-12 (11)	
	6	∕3	GU3BD-12 (11)	
	7	∕3	KL3BD-5 (4)	
	8	∕6M	JU3BD-4 (3)	
	9	∕3	JL3BD-6 (5)	
	10	∕3	HL3BD-6 (5)	
	11	∕3	GL3BD-6 (5)	See ALD page YA561
	12	-3	GL3BD-10 (9)	for layout of sense points
	13	-3	KL3BD-10 (9)	
	14	∕3	KL3BD-8 (7)	
	15	∕3	JL3BD-8 (7)	
	16	∕6M	HL3BD-12 (11)	
	17	-3	HL3BD-10 (9)	
	18	∕6M	GU3BD-8 (7)	
	19	∕6M	KU3BD-8 (7)	
	20	∕6M	KL3BD-12 (11)	
	21	∕6M	JL3BD-12 (11)	The console voltmeter
	22	∕3	HL3BD-8 (7)	monitors regulator 18
	23	∕6M	GL3BD-12 (11)	
	24	∕3	GL3BD-8 (7)	
MCF	1	-3	ATB2-10 (9)	
	2	∕3	AU3BD-12 (11)	
	3	∕6M	AL3BD-12 (11)	See ALD page YA761
	4	∕3	AL3BD-8 (7)	for layout of sense points
	5	∕5.1	Regulator Output Terminals	
CPW	1	∕6M	LU1BD-8 (7)	
	2	∕3	LU1BD-12 (11)	See ALD page YD711
	3	-3	LU1BD-10 (9)	for layout of sense points
	4	∕3	LL1BD-8 (7)	

Note: The numbers in parentheses are power supply return points.

FIGURE 5. REGULATOR SENSE POINTS

CHARACTERISTICS
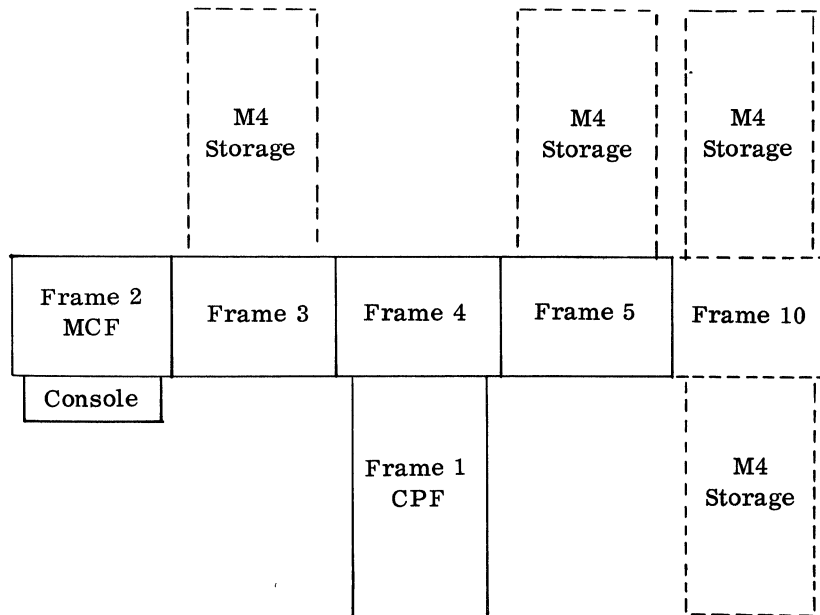
```
  ┌─────┐           ┌─────┐ ┌─────┐
  │  M4 │           │  M4 │ │  M4 │
  │Storage│         │Storage│ │Storage│
  │     │           │     │ │     │
  └─────┘           └─────┘ └─────┘
┌───────┬───────┬───────┬───────┬─────────┐
│Frame 2│       │       │       │         │
│ MCF   │Frame 3│Frame 4│Frame 5│Frame 10 │
└───┬───┴───────┴───────┴───────┴─────────┘
    │Console│       │           ┌─────┐
    └───────┘   ┌───────┐       │  M4 │
                │Frame 1│       │Storage│
                │ CPF   │       │     │
                │       │       └─────┘
                └───────┘
```

Weight	Frame 1	1,700 pounds
	Frame 2	2,200 pounds
	Frame 3	125 pounds
	Frame 4	550 pounds
	Frame 5	550 pounds
	Frame 10	200 pounds
	M-4 Storage (each)	2,560 pounds
Power Requirement	Main Frame	12.6 KVA
	M-4 Storage (each)	12.5 KVA
Input Line	Main Frame and each M-4 Storage	3 phase, 4 wire Connector: Russell and Stoll SC7328
Cooling	Main Frame	Forced room air, 3,350 cu.ft./min.
	M-4 Storage (each)	Forced room air, 2,150 cu.ft./min.
Heat Dissipation	Main Frame	43,000 BTUs/hr.
	M-4 Storage (each)	33,000 BTUs/hr.
Mounting	Leveling Feet	

This section contains a description of the lights, pushbuttons, and switches on the system control panel (Figure 6) with the exception of those concerned with Fault Location Test FLT; FLT indicators, pushbuttons, and switches are described in the FLT section of Volume II.

SWITCHES AND PUSHBUTTONS

Toggle switches are used for the data keys, the address keys, and the control switches.

Generally, a two-position switch (one that either activates a function or does not) transfers all of its sets of contacts when the switch is in the active position (on).

A three-position switch has one set of transfer points associated with the normal (middle) position. Two other sets of transfer points are associated with the up or down positions. Throwing the switch transfers the set associated with the middle position and also transfers one of the other sets associated with the position the switch is thrown to.

The pushbuttons, when pressed, emit a 370-ns pulse that initiates the manual operation associated with that pushbutton. One pulse-forming network, consisting of a latch and a singleshot, supplies the 370-ns pulse for all of the pushbuttons. Integrator circuits soften the sharp change in voltage level on the pushbutton lines when the pushbutton contacts make and break, thereby reducing noise pickup by adjacent cable wires.

The switches and pushbuttons on the panel are divided into four sections: operator control, operator intervention, customer engineer intervention, and power control. In the following paragraphs, the switches and pushbuttons of each section are described either individually or as they contribute to a manual operation.

Operator Control Section (V-Z, 89-101)

● Pushbuttons turn power on and off.

● Interrupt PB causes external interrupt.

● IPL procedure: Set up input unit; set rotaries; press LOAD.

The operator control section contains the necessary controls for the operator to turn the machine on and off, to initially load programs and data into the machine, and to manually interrupt the CPU.

Power On, Power Off

The power-on pushbutton initiates the system power-on sequence. When the sequence is completed, a system reset is activated. The pushbutton is back-lighted with a white light to indicate power-on. Any abnormal power condition causes the light to go from white to red.

The power-off pushbutton initiates the system power-off sequence.

Manual Interrupt

The operator can request an interrupt of the CPU by pressing the interrupt pushbutton. If the CPU is running or waiting, the console interrupt request is sent to the interrupt controls and there vies with other possible requests for priority. When priority is obtained, an external interrupt is taken, causing an exchange of external PSW's. The CPU continues processing under control of the new PSW.

If the CPU is stopped when the interrupt pushbutton is pressed (the stopped status being indicated by the manual light on), the interrupt is not taken but remains pending until the CPU is started; the interrupt is then taken when console interrupt priority is obtained.

Initial Program Load

Initial program load is the manual operation for initially loading programs and data into storage. The procedure is as follows:

1. Initialize the input unit (load the tape, etc.).

2. Set the left of the three rotary switches to the channel that is to be used. Set the other two rotary switches to the address of the input unit.

3. Press the load pushbutton.

The first machine action is a system reset. Next, the input unit starts to read, placing the first three double words into storage locations 0, 1, and 2. The channel then obtains the first CCW from storage location 1 and uses it to continue reading from the input unit, placing the words in storage.

When the read operation is completed, an IPL Load PSW interrupt sequence occurs which loads the PSW register with the double word at storage location 0. The IPL Load PSW is not a true interrupt because there are no request or priority considerations; the interrupt sequencers, however, are forced into action by a channel signal that occurs at the end of the read operation. The interrupt

sequencers load the PSW register in much the same way that they load a new PSW on any interrupt, but since an IPL control trigger is on, the double word that is loaded comes from storage location 0.

Next, an IC recovery takes place, which always happens following the load of a PSW (provided the PSW does not specify the wait state). The recovery fetches instructions into the instruction buffers. The I unit starts processing the first instruction.

CPU action on initial program load is covered in detail in Volume II, "Interrupts".

Operator Intervention Section (W-Z, 53-86 Plus the Data Keys at Row V)

- Manual controls active only when manual light is on.

- CPU can be started and stopped only by push-buttons.

- Resets: entire system or CPU only, or check conditions only.

- Store: data keys to storage, GR or FPR.

- Display: Storage to J reg; GR and FPR to RBL.

- Set PSW: data keys to PSW reg; IC recovery.

- Set IC; data keys 40-63 to IC; IC recovery.

- PSW restart: system reset, storage location 0 to PSW reg, IC recovery, automatic start.

- Address compare stop: CPU stops when address keys equal address sent to BCU.

This section of the panel contains switches and push-buttons to stop, start, or reset the machine; to manually store instructions or data into any storage location or into any of the addressable registers; to set up an entire new PSW in the PSW register, or to set only the IC portion of the PSW register; to start processing over again from the very beginning by reloading the PSW from storage location 0; to display the contents of any storage location or of any addressable register; and to manually step through a program, either one instruction at a time or one machine cycle at a time.

Stopping and Starting the CPU

The CPU is stopped automatically on an address compare stop operation (explained later) and following the execution of each instruction on instruction-step or multiple-step operations. The CPU is stopped manually by pressing the stop pushbutton or the CPU or system reset pushbuttons.

The stop pushbutton turns on the halt trigger, blocking further I-unit processing of instructions. Any instruction being executed at the time, however, is completed, and any outstanding interrupts are taken before the CPU stops. The stopped status is indicated by the manual light on.

The CPU starts automatically following an IPL operation or a PSW restart. Otherwise the CPU must be started by pressing the start pushbutton. CPU functions depend on the setting of the rate rotary switch when the start pushbutton is pressed.

Process: If the rate switch is in the process position the start pushbutton turns off the halt trigger, allowing the I unit to continue processing instructions; the E unit always executes whatever the I unit transfers to it. With the rate switch in process, stopping and starting the CPU by the stop and start pushbuttons is a matter of blocking and unblocking the I unit with the halt trigger. During the stop the controlled clock and the running clock keep operating.

Instruction - Step: If the rate switch is in the instruction-step position, each depression of the start pushbutton results in the execution of one instruction plus any pending interrupts that are not masked off. Pressing the start pushbutton turns off the halt trigger the same as before, allowing the I unit to start processing the next instruction. Because the rate switch is in the instruction-step position, however, the halt trigger immediately turns on, blocking the I unit from starting up again. Only one instruction, therefore, is executed.

Multiple-Step: If the rate switch is in multiple-step position, holding down the start pushbutton causes the instruction-step operation to repeat approximately four times per second. Before multiple-step or instruction-step can be used, the CPU must first be in the stopped status (the manual light must be on).

In instruction-step or multiple-step, the timer is not updated.

Single-Cycle: If the rate switch is in the single-cycle position, each depression of the start pushbutton causes one machine cycle. In single-cycle mode the halt trigger is not turned off and on as it is in instruction-step and multiple-step. The halt trigger is left off so that the I and E units may operate whenever they receive pulses from the controlled clock.

When the rate switch is thrown to single-cycle, the controlled clock is turned off. Each depression of the start pushbutton then turns the controlled clock on and back off right away, allowing only one
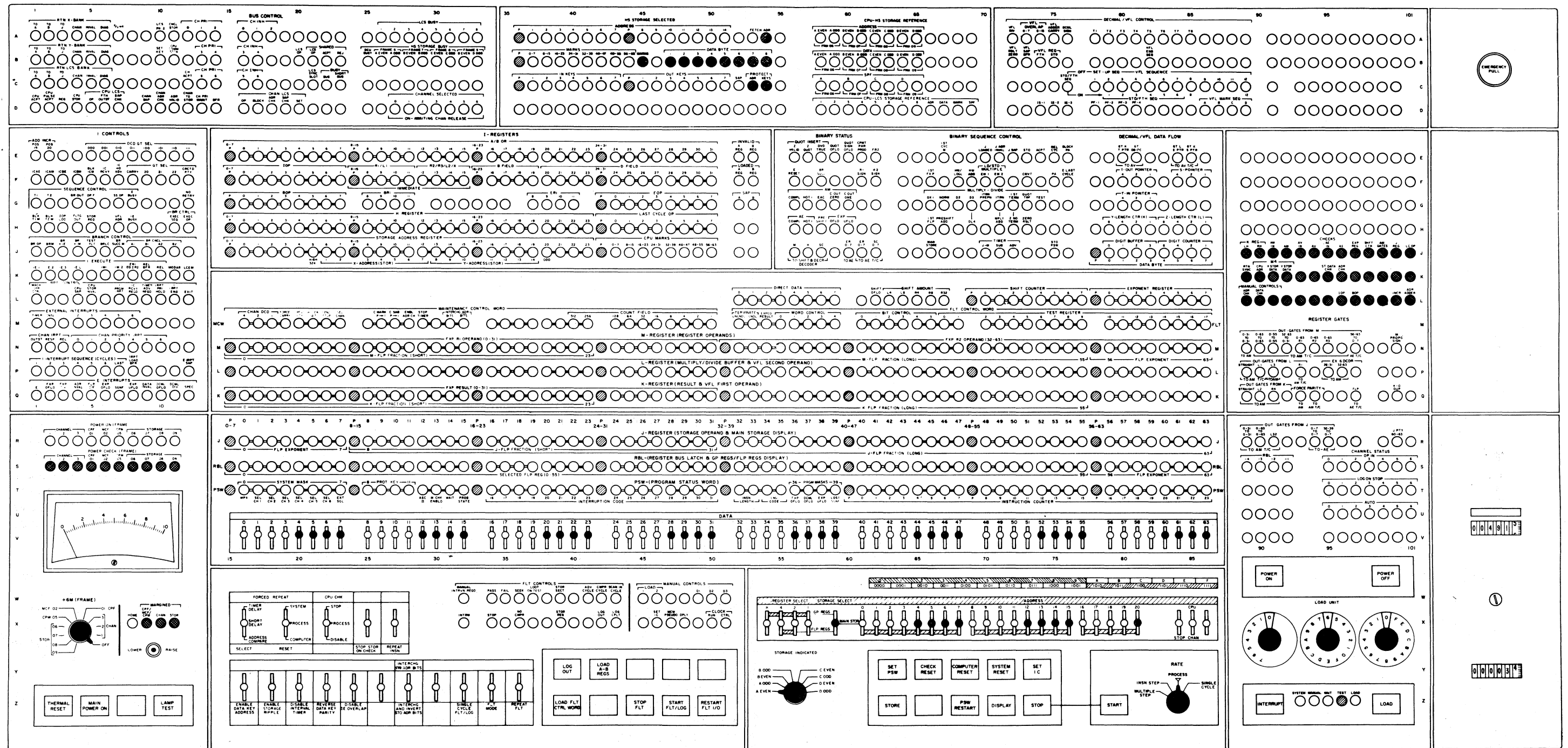
FIGURE 6. SYSTEM CONTROL PANEL

controlled pulse to be emitted. The one controlled pulse generates all of the timed control pulses that occur in one machine cycle.

Resets

Three kinds of resets can be made from the system control panel: system reset, computer reset, and check reset.

System Reset: This pushbutton resets the maintenance control word and all control and check triggers in CPU, channels, and storage with the exception of the addressable registers and the program status word. Instruction execution is blocked after completion of the reset, and the CPU is left in the stopped status with the manual light on.

System reset can also be generated by any of the following conditions:

1. Power up sequence is successfully completed.

2. The load pushbutton is pressed (no instruction block in this case).

3. On a forced repeat operation with the forced repeat reset switch set to system.

Computer Reset: This pushbutton causes action similar to the system reset pushbutton except that the channel triggers, the maintenance control word and the BCU are not affected. Channel operations, therefore, may continue uninterrupted.

CPU reset can also be generated by any of the following conditions:

1. All cases of system reset.

2. Logout-over condition following a machine check.

3. Certain fault locating test (FLT) conditions.

4. On a forced repeat operation with the forced repeat reset switch set to computer.

Check Reset: This pushbutton resets only the check triggers in the CPU and storage. Check reset is forced by CPU reset or system reset.

Store

The store pushbutton may be used to store data into any storage location or into any of the addressable registers. The pushbutton is active only when the manual light is on.

To manually store into a storage location, the storage select switch is set to the middle (main storage) position, the storage address is set into the address keys, the data to be stored is set into the 64 data keys, and the store pushbutton is pressed. The contents of the data keys are then stored into the selected location (Figure 7).

To manually store into a general register, the storage select switch is set to the up (general register) position. The register is selected by setting the four register select keys, the data to be stored is set into positions 0-31 of the data keys, and the store pushbutton is pressed. The 32 bits from the data keys are then stored into the selected general register (Figure 8).

To manually store into a floating point register, the storage select switch is set to the down (floating point) position. The floating point register is selected by the middle two register select keys, the data to be stored is set into the 64 data keys, and the store pushbutton is pressed. Contents of the data keys are then stored into the selected floating point register (Figure 8).

Display

The display pushbutton may be used to display any storage location or any general or floating point register. The pushbutton is active only when the manual light is on.

To display a storage location the storage select switch is set to the main storage position, the storage location to be displayed is set into the address keys, and the display pushbutton is pressed. The selected storage location is displayed in the J register (Figure 7).

To display a general register, the storage select switch is set to the general register position, the general register to be displayed is selected by the four register select switches, and the display pushbutton is pressed. The selected general register is displayed in the left half of the RBL latch indicators (Figure 9). Other general registers can now be displayed merely by changing the register select switches.

To display a floating point register, the storage select switch is set to the floating point register position, the floating point register to be displayed is selected by the middle two register select switches, and the display pushbutton is pressed. The selected floating point register is displayed in the 64 RBL latch indicators (Figure 9).

Set PSW

The set PSW pushbutton is active only when the manual light is on. Pressing the pushbutton causes the contents of the 64 data keys to be set into the PSW register (Figure 10). Provided the new PSW does not specify the wait state, the CPU does an IC recovery fetching the instructions located by the IC of the new PSW to the instruction buffers, registers A and B. Processing starts with these instructions whenever
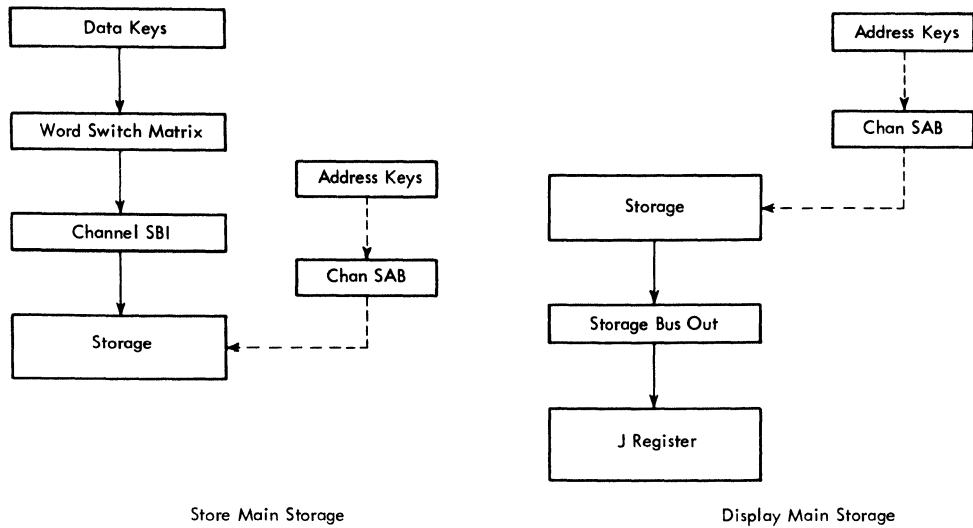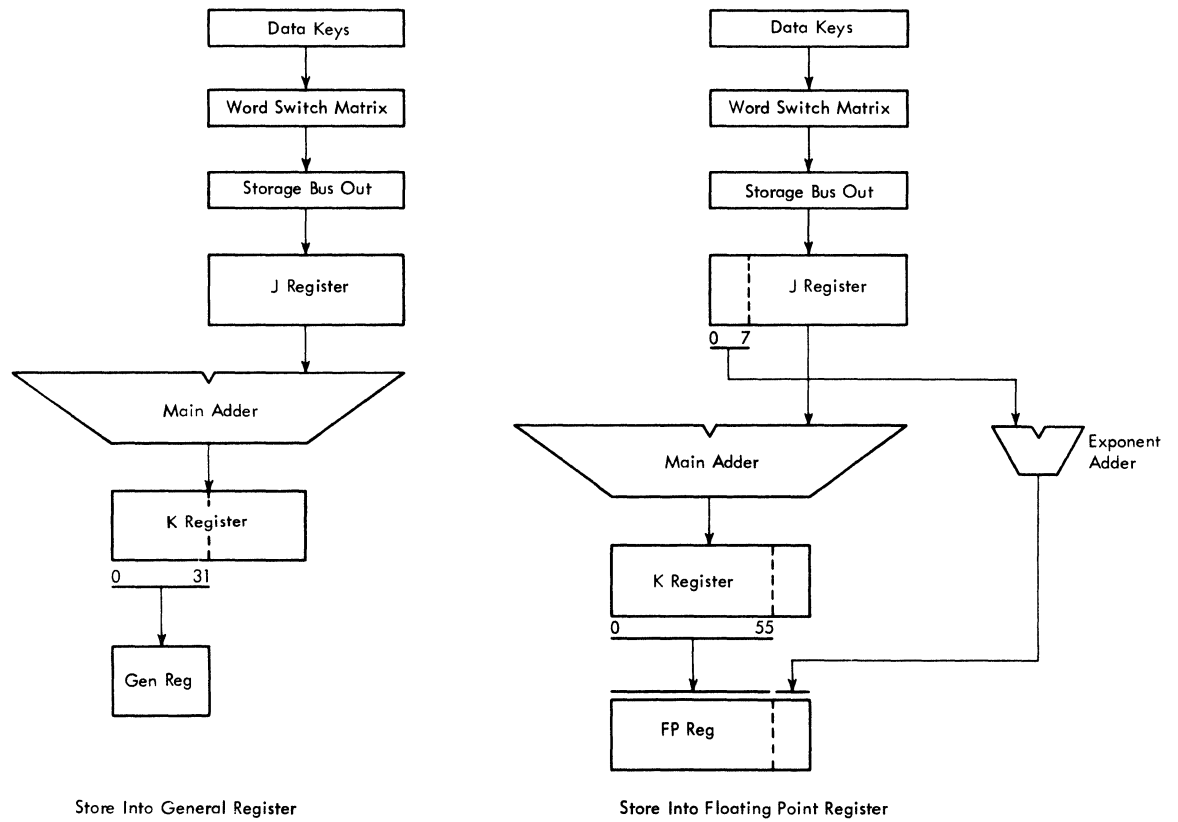
Store Main Storage

Display Main Storage

FIGURE 7. DATA FLOW STORE AND DISPLAY MAIN STORAGE

Store Into General Register

Store Into Floating Point Register

FIGURE 8. DATA FLOW, STORE INTO GENERAL OR FLOATING POINT REGISTER

```
┌──────────────────────┐
│  General Register    │
└──────────────────────┘
           │
           ▼
┌──────────────────────┐                    ┌────────────────────────────────┐
│  General Bus Left    │                    │     Floating Point Register    │
└──────────────────────┘                    └────────────────────────────────┘
           │                                              │
0          ▼         31                                   ▼
┌──────────────────────┐                    ┌────────────────────────────────┐
│  Register Bus Latches│                    │      Register Bus Latches      │
└──────────────────────┘                    └────────────────────────────────┘

    Display General Register            Display Floating Point Register
```
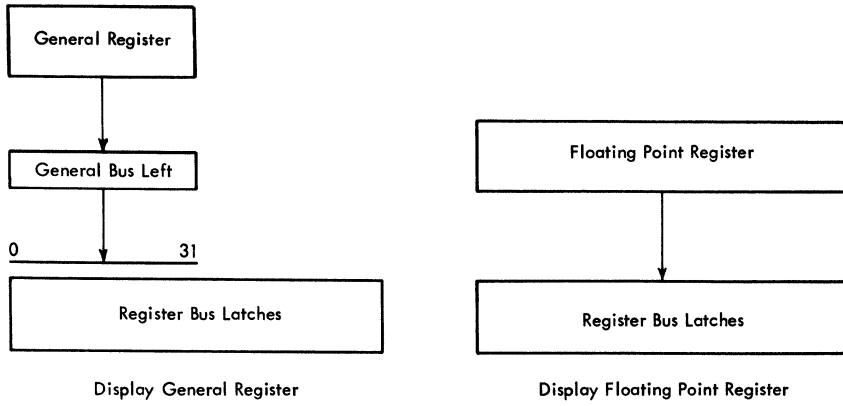
FIGURE 9. DATA FLOW, DISPLAY GENERAL OR FLOATING POINT REGISTER

```
┌──────────────────┐       ┌──────────────────┐       ┌──────────────────┐
│    Data Keys     │       │    Data Keys     │       │    Data Keys     │
└──────────────────┘       └──────────────────┘       └──────────────────┘
         │                          │                          │
         ▼                          ▼                          ▼
┌──────────────────┐       ┌──────────────────┐       ┌──────────────────┐
│ Word Switch Matrix│      │ Word Switch Matrix│      │ Word Switch Matrix│
└──────────────────┘       └──────────────────┘       └──────────────────┘
         │                          │                          │
         ▼                          ▼                          ▼
┌──────────────────┐       ┌──────────────────┐       ┌──────────────────┐
│ Storage Bus Out  │       │ Storage Bus Out  │       │ Storage Bus Out  │
└──────────────────┘       └──────────────────┘       └──────────────────┘
         │                          │                    ┌─────┴─────┐
         ▼                          ▼                    ▼           ▼
┌──────────────────┐       ┌──────────────────┐   ┌──────────┐ ┌──────────┐
│   J Register     │       │   J Register     │   │A Register│ │B Register│
└──────────────────┘       └──────────────────┘   └──────────┘ └──────────┘
        40    63                    │
         │                          ▼
         ▼                 ┌──────────────────┐
┌──────────────────┐       │   PSW Register   │
│ PSW Register│ IC  │       └──────────────────┘
└──────────────────┘

      Set IC                    Set PSW                    Load A-B
```
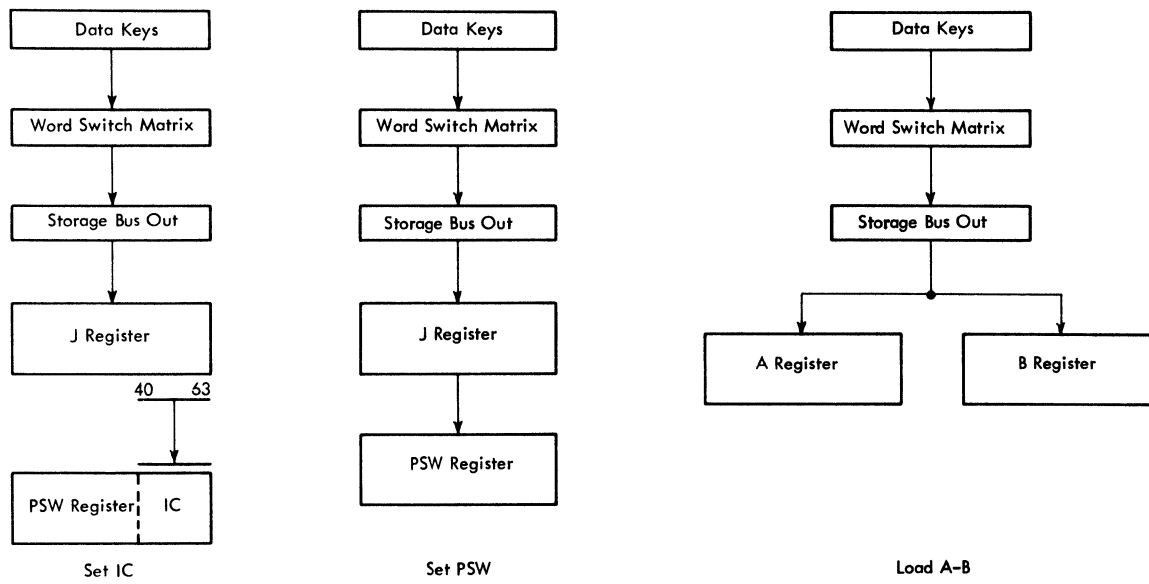
FIGURE 10. DATA FLOW, SET IC, SET PSW, LOAD A-B

the start pushbutton is pressed.

If the new PSW specifies wait, IC recovery is suppressed and the wait trigger is turned on. The wait trigger on causes the CPU to enter the wait state; no instructions are processed.

Set IC

The set IC pushbutton is active only when the manual light is on.

Pressing the pushbutton causes the contents of data keys 40-63 to be set into the IC portion of the PSW register (Figure 7). Provided the PSW does not specify wait, CPU does an IC recovery fetching the instructions located by the new IC of the PSW to the instruction buffers, registers A and B. Processing starts with these instructions whenever the start pushbutton is pressed.

If the PSW specifies the wait state, the IC recovery portion of the operation is suppressed and the wait trigger is turned on. Pressing the start pushbutton causes the halt trigger to be turned off, but the wait trigger on causes the CPU to enter the wait state; no instructions are processed.

PSW Restart

The PSW restart pushbutton is active only when the manual light is on. Pressing the pushbutton causes first a system reset and then a load of the PSW register from storage location 0, which is the location of the initial PSW. Next, an IC recovery takes place, fetching the instructions located by the PSW just loaded. The CPU is automatically started.

If the PSW loaded from location 0 specifies the wait state, the IC recovery portion of the operation is suppressed and the wait trigger is turned on. The halt trigger then turns off and the CPU enters the wait state.

Address Compare

The address compare feature utilizes two switches: a 3-position switch labeled address compare CPU-Chan, and a 2-position switch labeled address compare stop. While the machine is running, and with the CPU-Chan switch in the middle position, any address sent to the BCU (whether from the CPU or the channels) is compared with the address in the address keys. If the comparison is equal, a sync pulse is generated which goes to all the gates; this pulse can be used for scoping. If the CPU-Chan switch is in the CPU position, only addresses from CPU are compared with the address keys; if the switch is in the Chan position, only addresses sent from the channels are compared with the address

keys. The foregoing is true regardless of the setting of the address compare stop switch.

If the address compare stop switch is in the stop position, the sync pulse generated because of the equal comparison also turns on the halt trigger. The halt trigger on stops the machine after the current instruction is completed and all outstanding interrupts are taken.

Customer Engineer Intervention Section (W-Z, 15-52)

● Logout pushbutton: 19 double words of trigger-status stored.

● Load A-B reg pushbutton: Data keys to both A reg and B reg.

● Interchange storage adr bits switch: Allows sequential instructions to be located solely in odd or even storage.

● Disable overlap switch: Causes I and E units to operate serially, without overlap.

● Reverse data key parity switch: Inverts the parities generated by the data keys. Forces errors.

● Disable interval timer switch: Blocks updating of interval timer word.

● Enable storage ripple switch: Allows the multiple store and multiple load instructions to act as a storage test.

● Enable data key address switch: Allows data keys to be used as an operand.

● Repeat instruction switch: Instruction in left end of A reg executed repetitively.

● Stop storage on check switch: Storage check inhibits further selection of that storage.

● CPU check switch: Machine check stops machine, causes logout, or is ignored.

● Forced repeat switches: Portion of program is repeated every 100 microseconds, every 16.6 milliseconds, or on address compare.

Logout

Pressing the logout pushbutton causes a CPU logout operation to take place. During a logout, the status of 1216 CPU triggers (both register positions and

control triggers) is stored away into storage as the bits of nineteen 64-bit words. The 19 double words are stored into storage locations 16 through 34 (double-word locations).

The logout pushbutton is active only when the manual light is on. The CPU remains in manual status during and after logout.

Load A-B Registers

Load A-B registers pushbutton is active only when the manual light is on. Pressing the pushbutton places the contents of the 64 data keys into both the A and the B registers (Figure 7). This operation is useful as a prior step to the repeat instruction operation.

Interchange Storage Address Bits

For the Model 75H, the normal addressing scheme of the storages (with the interchange-storage switch in the middle position) is such that sequentially located instructions are in two separate storage units, odd and even. Under some circumstances it may be desirable to have a program contained in only one of the units, for example, when the other unit (odd or even) is to be tested; the reverse storage address switch would permit this. In the up position, this switch causes what normally is address bit 20 to become address bit 6, and bit 6 to become bit 20. Instructions with addresses up to 16K can be sequentially located solely in the even unit, leaving the odd unit free to be tested. Similarly, instructions with addresses from 16K to 32K can be located solely in the odd unit, leaving the even unit free to be tested.

The down position of the switch causes what is normally address bit 20 to become address bit 6, and what is normally the inverse of bit 6 to become bit 20. The down position also permits sequentially located instructions to be contained solely within the odd unit or the even unit, but the contents of the two 16K areas in the unit in question are reversed from what they would be were the switch in the up position.

For Models 75 I and J, the interchange storage address switch interchanges address bits 19 and 5 (switch up), or 19 and not 5 (switch down). The result is that sequential instructions are 2-way interleaved instead of the usual 4-way, which means that 2 of the M4's can be filled leaving the other 2 M4's empty for testing. Address switching is covered in more detail in Volume II, BCU.

Disable Overlap

This switch prevents the overlap of the I and E units. Normally, the I unit processes an instruction while the E unit executes the previous instruction. The disable overlap switch blocks the I unit from starting until the E unit has finished its execution; therefore, the two units operate in a serial fashion and not in the normal overlapped fashion.

Reverse Data Key Parity

This switch inverts the eight parity bits generated on the data keys. These forced parity errors facilitate checking of the error detection circuits.

Disable Interval Timer

This switch blocks the output of the interval timer singleshot, thus preventing the updating of the timer word.

Enable Storage Ripple

This switch modifies the store multiple and load multiple instructions to provide a storage test, that is, a method of filling all of storage with the same data or fetching data from all storage locations. The instructions are modified to operate as follows: On store multiple, the contents of the beginning general register specified in the instruction are stored into successive storage locations, starting at the effective address and wrapping around throughout all of storage.

On load multiple, the contents of all successive storage locations are fetched and loaded into the general register that is specified in the load multiple instruction as the beginning register. Storage starts fetching from the effective address and continues fetching from each successive location, with wrap-around occurring the same as in store.

On both storing and loading, the instruction counter advances up through the invalid range. The BCU handles the invalid addresses in the same manner as it normally does, except that no invalid address signal is returned to CPU; CPU, therefore, does not stop on the invalid addresses.

Once started, the storage ripple keeps running, and can be stopped only by computer or system reset.

Enable Data Key Address

A bit in position 0 of an address normally causes the storage request to be cancelled and the data keys to be fetched to the receiving register instead of the storage word. A bit in position 0 of the address can also result in a BCU invalid address check. If the enable data key address switch is in the down position, the bit-0 address causes a storage cancel and a fetch of the data keys, with the BCU invalid address check inhibited. Use of this switch, therefore, permits the

data keys to be fetched in lieu of a storage operand without a BCU invalid address check.

Repeat Instruction

When the repeat instruction switch is in the down position the instruction located in the left end of the A register is executed repetitively. All instructions may be processed in repeat instruction mode except branches, load PSW, and execute.

To repeat an instruction: Set up the A register with the instruction to be repeated (this can be done by using the load AB registers pushbutton). Turn on the repeat instruction switch. Press start.

Stop Storage on Check

If a check condition is detected in a storage unit while the stop storage on check switch is on, the switch prevents further selection of that storage unit. The storage check condition may be cleared by the check reset pushbutton, but the BCU will usually require a system reset before processing can continue.

CPU Check

If the CPU check switch is in the middle (process) position, a CPU error causes the following: the CPU stops, a logout operation takes place, the CPU is reset, and a machine check interrupt occurs.

If the switch is in the up (stop) position, a CPU error stops the machine. No logout takes place. Both the machine and the program will require initialization to resume processing. If the switch is in the down (disable) position, a CPU error goes undetected. The CPU continues without interruption.

Forced Repeat

Forced repeat switches permit repetitive runs of a particular section of a program. The starting point is determined by a PSW automatically loaded from the data keys. Instructions are processed in accordance with this PSW until a particular time has elapsed, or until a particular address has been reached. At this point, a reset is made. The PSW is again loaded from the data keys and the process is repeated. The kind of reset that occurs at the beginning of each loop is determined by the setting of the reset switch; the reset can be either computer or system. The period of time that instructions are executed before the repeat occurs is determined by the setting of the select switch. The time period can be a "short delay" (100 microseconds) or it can be a "timer delay" (16.6 milliseconds). If desired, the repeat point of the instruction loop can be when

an address referencing storage compares with an address in the address keys. A forced repeat operation might be as follows:

Assume that the forced repeat select switch is on short delay and that the forced repeat reset switch is thrown to computer. Moving the reset switch to the computer position fires a series of two singleshots that time out in 100 microseconds. The time-out of the singleshots initiates a computer reset and causes another firing of the singleshots. As soon as the reset is over, a load PSW operation occurs; the contents of the 64 data keys are placed into the PSW register. An IC recovery then occurs, which loads the instruction buffers from the storage location specified by the IC of the PSW just loaded. The machine starts executing instructions. The two single-shots are still timing out.

Instructions are executed under control of the PSW until the two singleshots time out. The time-out of the singleshots again resets the CPU and causes another firing of the singleshots. The reset over causes another load PSW from the data keys, followed by an IC recovery. The same instructions are executed again. This sequence keeps repeating every 100 microseconds.

With the select switch on timer delay, the action would be the same except that other singleshots would cause the sequence to be repeated every 16.6 milliseconds.

If the select switch is on address compare, the forced repeat operation must be started with the manual computer or system reset key; that is, the select switch is set to address compare, the repeat switch is set to computer reset or system reset, and the manual computer or system reset key is pressed. (The reset key that is pressed should correspond to the forced repeat reset switch setting.) The reset over loads the PSW register from the data keys, and an IC recovery takes place. Instructions are executed under control of the PSW until an address sent to the BCU compares favorably with the address contained in the address keys. An address compare signal then fires the same two singleshots used on short delay. After the 100-microsecond time-out, the CPU (or system) is reset, the PSW is reloaded, and the sequence is repeated.

Power Control Section (R-Z, 1-12)

- +6M voltage of storage frames, channel frames, central processing frames, or maintenance console frame can be varied for test.

- Abnormal power condition indicated by frame.

- All indicators can be turned on for test.

This section describes all controls concerned with system power including marginal check controls, thermal controls, and emergency controls.

Thermal Reset

This pushbutton resets the thermal interlock circuitry after a thermal fault in the system. The reset must take place before power is restored to the system.

Lamp Test

This pushbutton lights all indicators on the panel except those associated with power controls.

Emergency Off

This switch, in the upper right corner of the panel, shuts off power beyond the entry terminal on every unit of the system. The out position latches the switch and makes inactive the power-on pushbutton. Restoration to the in position is done from the back side of the panel.

Raise-Lower Switch

This three-position (spring loaded to off) switch controls variations in the +6V marginal power supply to the frame selected by the +6M rotary switch. The +6V is varied by holding the switch toward the raise or lower position and watching the monitor voltmeter that is mounted on the panel. Releasing the switch locks the voltage in the selected frame at the value created by the hold-down. The raise-lower switch is interlocked by the customer engineer key switch mounted on the metering panel (far right side of console).

+6M Switch

This rotary switch selects the frame to be marginally checked. Frames that can be selected are:

    Central Processing Frame (CPF)
    Maintenance Console Frame (MCF)
    Central Processing Wall (CPW)
    Channel Frames 1, 2, or 3
    Storage Frames 6, 7, 8, or 9

Voltmeter

This meter continuously monitors the +6M regulator of the frame selected by the +6M switch and shows the margined voltage as set by the raise-lower switch.

In the CPF, only one +6M regulator (number 18) is monitored. Monitoring for other regulators, if necessary, is via external voltmeters.

Metering Section (lower right corner)

The CPU metering logic and metering lines between the CPU and channels are shown in Figure 5764.

INDICATORS

This section describes all indicators on the system control panel except those concerned with Fault Location Testing (FLT). FLT indicators are described in Volume 2.

The following descriptions are grouped according to the layout of the panel. A particular indicator may be located in this section by noting the indicator's group on the panel and then finding the starting page for that group in the "Contents."

Group Name	Grid Boundaries
Bus Control	A-D, 1-33
Storage	A-D, 36-39
Decimal/VFL Control	A-D, 72-89
I Controls	E-K, 1-12
Interrupts	L-Q, 1-12
I Registers	E-J, 15-53
Binary Status	E-J, 56-62
Binary Sequence Control	E-J, 64-76
Decimal/VFL Data Flow	E-J, 78-86
Common Registers	L-T, 15-86 (RBL to 92)
Checks	J-L, 89-101
Register Gates	N-R, 89-101
Channel Status	S-U, 95-101
Manual Controls	W-X, 45-51
Power and Marginal Checking	R-S, 2-11; X8-11
Status Lights	Z93-97

Some CPU triggers are always off when viewed between single-cycles. This is because the triggers either turn off in the same cycle that they turn on, or they turn off by a storage pulse which occurs independently of the CPU clock. These triggers are:

    CPU Pulse Accept (D2)
    Request (D3)
    ICAM (F2)
    ICBM (F4)
    BrM (J2)
    Br + 1E (J3)
    Br Cancel (J8-11)

Bus Control

Return X Bank, Return Y Bank (A-B, 1-6) MB605, 611: Address registers used alternately on 2365 storage selections to route data and error indications to the proper destination.

The BCU sets one or more positions in one of these registers (X or Y) during the storage selection cycle; the set positions subsequently route the storage

advance pulse to the proper destination:

    A: Set on even-word instruction buffer fetches; returns double word to A register.

    B: Set on odd-word instruction buffer fetches; returns double word to B register.

    J: Set on operand fetches; returns double word to J register.

    Channel: Set on channel fetches and stores; returns storage advance signal to channel.

    Invalid: Set when BCU receives invalid address (one outside available storage) on CPU fetches or on channel fetches or stores. Result: storage is cancelled and storage advance is routed to set A Invalid, B Invalid, J Invalid, or to send invalid address signal to channel.

    Diagnose: Set on diagnose instruction to gate fetched word into MCW register.

Return LCS Bank (C1-6) MB612: For LCS selections. Returns data and error indications to the proper destination. Individual positions function the same as those of the X and Y banks for high-speed storages.

CPU Accept (D1) MB521: Turned on by a CPU-initiated storage select pulse, and turned off by early B (controlled) of the following machine cycle. Indicates to CPU that the storage request is being honored.

CPU Pulse Accept (D2) MB521: Generated in parallel with CPU accept. The difference is that CPU pulse accept is turned off by a running clock pulse rather than a controlled clock pulse.

Request (D3) MB511: Indicates that a CPU request is present in BCU. Turned on by store or fetch request from the I or E unit; turned off when no request is present or when storage is selected for CPU.

CPU Store (D4) MB507: Indicates that a store request from CPU is present in the BCU. Turned on by CPU store request; remains on until the next release of SAR.

CPU LCS Operation (D5) MB508: Indicator for the processor LCS operation (PLOP) trigger. Blocks selection of high-speed storages and substitutes an LCS storage. Turned on by CPU LCS flag (when BCU decodes an LCS address); turned off at B time of the storage selection cycle.

CPU LCS Fetch Outstanding (D6) MB602: Blocks CPU requests until data is returned by the LCS. This action prevents a subsequent request to a high-speed storage (which might return its data before the LCS does), thereby ensuring returned data to be in the proper sequence. Turned on when select is sent to LCS for a CPU fetch; turned off by LCS advance.

CPU LCS SAP Check (D7) MB634: Indicates an address protection violation on a CPU store or fetch using LCS. The trigger turns on at LCS advance time and remains on until interrupt is taken.

Channel SAP (D9) MB631: Indicates an address protection violation on a channel fetch or store using a high-speed storage. The trigger turns on during the machine cycle following the storage selection cycle and remains on until the next channel storage selection.

Channel Address Check (D10) MB625: Indicates a parity error on a channel-to-high-speed-storage operation at one of the following places:

    1. BCU addressing OR

    2. Storage MAR

    3. Mark Register (store only)

    4. SPF SPAR

    5. In key register or out key OR (when used).

Turns on during the machine cycle following the storage selection cycle; remains on until the next channel storage selection.

Address Valid (D11) MB727: Indicates to BCU that the address from the channel is valid at the BCU addressing OR. Signal causes BCU to give priority to channel (instead of CPU). Turns on at coincidence of B time, address valid signal from channel, and delay of approximately 600 nanoseconds following BCU response. Turns off by reset channel bus priority (when storage selection is made for the channel).

Channel to Storage (D12) MB175: When on, indicates that ChSAB is being gated through BCU addressing OR; when off, indicates the SAR is being gated through BCU addressing OR. Turns on at the B time prior to the channel storage selection cycle; turns off in the cycle following the storage selection cycle.

Channel Priority 0, 1, 2 (A12-14); 3, 4 (B13-14); 5, 6 (C13-14); Maint Chan (D13) MB703-711: These 7 lights cover the priority AND circuits. Only one of the lights should be on at a given time. A light on indicates that BCU has granted priority to that channel to use the channel buses (signaled to channel by BCU response).

Buffer (D14) MB701: Trigger controls when BCU examines channel requests. Turns on when channel priority is granted by BCU, and while on, prevents further change of channel request latches. Turns off, allowing a new priority selection, when channel storage selection is made.

LCS Panel Key 2 (A10) MB516: On a cancelled LCS operation, the BCU generates a dummy LCS advance pulse. The LCS Panel Key 2 trigger gates this dummy advance pulse so that it will be compatible

with M-4 advance timing. The LCS Panel Key 2 trigger turns on at B time of the post-selection cycle and turns off at the B time following the fall of the dummy advance.

X/Y to X (A7) MB625: When on, indicates that X-Y binary trigger is in X position, thereby gating return address register inputs (return to J, return to A-B, and so on) into the return X bank register. When off, indicates X-Y binary trigger is in Y position, thereby gating inputs into the return Y bank register. The trigger changes state (binary) every post select cycle of a high-speed storage reference.

Cancel Storage (A11) MB525: Indicator is off the panel key fetch trigger and indicates that a storage reference is being cancelled. Turns on at B time of the storage select cycle; turns off at B time of the following cycle.

Storage is cancelled upon (1) bad parity at addressing OR, (2) an invalid address, or (3) a panel key fetch operation.

Set Key (B10) MB535: The set key trigger is used on the set key instruction in those instances where two SPF's must be set with the same key because of storage interleaving. The set key trigger is on for the first of the two set key storage references. When on, it reverses address bit 19 (for high-speed storages) or address bit 20 (for LCS), at the same time blocking the accept pulse to CPU. By blocking accept, the input conditions to BCU, such as address, request, and so on, remain active so that the second of the two storage references can be made.

CPU Communicate Storage (B11) MB525: This trigger controls the setting of the high-speed and LCS storage address and storage data error triggers (baby-sitter latches) so that these triggers will turn on only if the error is on a CPU-initiated storage operation. The CPU communicate storage trigger is turned on by pulse accept or PLOP and is turned off by the following B clock.

Channel Accept (C12) MB733: Indicates to a requesting channel that storage has been started. Channel accept trigger turns on at B time of the storage select cycle and turns off at B time of the following cycle.

Channel Inhibit 0, 1, 2 (A12-14); 3, 4 (B13-14); 5, 6 (C13-14) MB702-706: Used only on LCS operations. Blocks a channel out of the request priority scheme to allow the BCU to examine other channel requests. Turns on when BCU signals a channel (LCS set signal) that the channel's request is for an LCS. Turns off when the channel responds with an LCS priority signal.

LCS Operation (B20) MB563: This trigger is the BCU control trigger for LCS operations. For non-shared operations, the LCS Op trigger (LOP) is on during the selection cycle of an LCS. For shared operations, it is turned on by the accept signal from the selected LCS.

Shared LCS Operation (B21) MB563: Used only for shared operations. Indicates that BCU is waiting for an accept or reject signal from an LCS unit in reply to a select. On shared operations, the shared LCS Op trigger (shared LOP) is set instead of the LOP trigger, and stays on until an accept or reject signal is received from LCS unit in question.

Shared Accept (B22) MB593: Indicates that BCU has received an accept from the selected shared LCS. Shared accept turns off the shared LOP trigger and turns on the LOP trigger.

Shared Reject (B23) MB593: A signal from a shared LCS to BCU indicating that select signal has been rejected. Shared reject turns off the shared LOP trigger but does not turn on the LOP trigger (as does shared accept).

LCS Sync Slot (C21) MB571: Set by a pre-advance signal from a selected LCS and reset by the advance signal. While on, it blocks high-speed storage selections to prevent data that might be returned from a high-speed storage from interfering with data returned from LCS.

Bus Busy (C22) MB571: Turns on when LCS is selected, and is turned off by the selected LCS advance signal. While on, blocks all other LCS selects.

Short Bus Busy (C23) MB573: Turns on when an LCS is selected; turns off by pre-advance from the selected LCS. Trigger is used by channel priority circuits to block out any channel's request for an LCS. Short bus busy goes off before bus busy to allow channels to access LCS units at maximum rate.

Channel LCS Operation (D16) MB731: Indicates that BCU has honored a channel's request for an LCS. Turns on by the LCS set signal (BCU signal to channel) if the bus busy trigger is off. Chan LCS Op trigger is on for one cycle and results in turning on the LOP trigger.

Channel LCS Block (D17) MB702: Turns on when BCU recognizes that a channel is making an LCS request (LCS set signal to channel). Stays on as long as any channel is either using or waiting for an LCS. While on, blocks CPU and maintenance channel requests for LCS (inhibits the turn-on of PLOP).

Channel LCS Address Check (D18) MB626: This trigger turns on for the same reasons as the channel address check trigger (D10) but for LCS operations only. See description of the channel address check indicator.

Channel LCS SAP Check (D19) MB634: Indicates an address protection violation on a channel fetch or store using an LCS. The trigger turns on at LCS advance time and remains on until the next LCS selection.

Channel LCS Set (D20) MB723: A signal from BCU to a channel indicating to the channel that the address received by the BCU is in an LCS. Signal causes requesting channel to bring up an LCS priority line to BCU. Channel LCS set signal is up for one machine cycle, starting with the late BR clock that follows address valid.

LCS Busy 1-8 (A26-33) MB573-581: One light for each LCS unit. LCS busy trigger turns on by the AR clock following the rise of the busy line from the LCS, and turns off by the early BR clock following the fall of the busy line. Busy line from LCS rises with select and falls at the completion of the LCS cycle. While on, the LCS busy trigger prevents the BCU from selecting that LCS.

High-Speed Storage Busy, BCU Busy (B25) MB517: Sets the maximum BCU selection rate at 1 selection every 2 machine cycles. BCU busy turns on when BCU makes any storage selection; turns off at B time of the following cycle. While on, it blocks all selects.

High-Speed Storage Busy, Odd-Even, A-D (B26-33) MB523: These triggers prevent BCU from selecting a busy high-speed storage. Triggers are turned on when their corresponding storage is selected and turned off just prior to the storage going not busy.

Channel Selected 0-6 (D27-33) KD601-611: Lights indicate channel selected. Channel selection originates either at the H register (on channel instructions), or at the console rotary switch (for IPL). A channel selected light remains on until CPU receives release signal from the channel.

Storage

HS Storage Selected

Rotary switch at bottom of panel selects high-speed storage. This group of lights (A-C, 36-55) pertains to the high-speed storage that is selected. Lights turn on and off at storage select time. Lights apply to both CPU and channel operations.

Address (A36-51) MT292, 295: These 14 lights are directly off the address register (MAR), indicating the address at the M4.

Fetch (A53) MT281, 283: Light turns on during any storage operation that is not a store. Light comes from the off side of the store latch. Store latch is set on or off at storage select time.

Address (A54) MT291: Red light indicates parity error at the storage unit MAR. Light turns on shortly after storage select and remains on until next storage select for that storage.

Marks (B36-44) MT263, 264: Lights indicate contents of mark register in storage unit. BCU sends mark bits to the storage unit; mark register is set at storage select time. Each bit in mark register allows its corresponding byte on the SBI to be gated into the MDR. Each mark register position that does not have a bit causes its corresponding byte to be regenerated into storage.

Marks (B45) MT254, 255: Red light indicating bad parity at the mark register on a store, or on the test and set instruction. This condition causes storage address check signal to be sent to BCU. If a channel selected the storage, BCU sends an address check signal to that channel. If CPU selected the storage, CPU Adr light (K90) turns on and a machine check results.

Data Byte (B47-54) MT266, 267: Red data byte lights indicate bad data at the MDR. If a channel selected storage, the BCU sends a channel data check signal to that channel. If CPU selected storage for a store operation, BCU turns on X Store Data, or Y Store Data (K91, 92) and signals a machine check.

In Keys, Out Keys (C36-51) SP571: Lights indicate contents of the in key and out key registers in the storage protect unit. In key register is set with a protection key obtained from the PSW on CPU operations, from the channel on channel operations, or from a general register on the set key instruction. Out key register is set with a storage key from the SPF storage; storage key identifies a certain block of 2048 main storage byte locations. The 4-bit keys in the in key and out key registers must agree on a store, and must agree on a fetch if the out key register contains a read protect bit (position 5); otherwise, a SAP check is generated.

SAP (C52) SP571: Light turns on when there is a no-compare between in key and out key registers on a store, or read-protected fetch. SAP condition causes SAP interrupt request; interrupt taken is a program interrupt.

Protect, Address (C53) SP571: Red light turns on when bad parity is detected at storage protect unit's address register (SPAR) on a CPU or channel store or fetch, or on the instructions set key, insert key, or test and set. If storage operation is CPU initiated, a machine check also results.

Protect, Keys (C54) SP571: Red light is turned on by bad parity at the in key register, or bad parity at the out key OR.

During a store, if the in key is all zeros with good parity, the out key is not checked because in this case the out key is not to be used. (An all-zeros in key makes any store address legal.) However, if the in key parity is bad, zeros or not, the out key is checked for parity. Either key, if bad, turns on the key check light. If CPU initiated the store, a machine check also results

CPU-HS Storage Reference

The lights in this group indicate CPU-initiated high-speed storage errors. Once on, they remain on until turned off by check reset.

Address (A58-65) MT282, 284: Lights indicate an addressing error in one of the eight high-speed storage units. Lights are turned on by (1) bad parity detected at the storage address register (MAR) on a fetch request or store request, (2) bad parity detected at the mark register on a store request. Either condition sends a storage address check signal to BCU, turning on the CPU address check trigger (K90) and causing a machine check.

Data (B58-65) MT282, 284: Lights indicate bad data on a CPU-initiated store or fetch and are turned on by bad parity detected at data register (MDR). Storage in question sends storage data check signal to BCU, and if the operation is a store, the signal there turns on either the X Store Data or Y store Data trigger (K91, 92) and causes a machine check.

An MDR parity error on a fetch turns on a data light, but a machine check does not result unless the fetched data are used by the instruction. A later machine check condition might stop the machine, and the data light, turned on earlier, would still be on. The light, therefore, indicates a possible storage trouble, but the trouble is not necessarily associated with the instruction that caused the stop.

SPF (C58-65) SP571: Each of these four lights indicates an address parity error or a key parity error in its corresponding storage protect unit. See descriptions of Protect, Address (C53) and Protect, Keys (C54).

CPU-LCS Storage Reference

Lights in this group indicate CPU-initiated LCS storage errors. Once on, they remain on until turned off by check reset.

1-8 (D58-65) LCS MK351: Each of these lights identifies the LCS with which the four error lights in the same row on the panel are associated; any error condition that turns on one of the four lights also turns on one of these eight identification lights.

Address (D66) LCS MK351: Light indicates a parity error at the LCS storage address register (SAR), or an incorrect transfer of address bits from SAR to the address register of the SPF.

Data (D67) LCS MK351: Light indicates a key parity error or a storage data register (SDR) parity error.

Mark (D68) LCS MK351: Light indicates a parity error at the mark register on a store, or on the test and set instruction.

SPF (D69) LCS MK351: Light indicates an in key or out key parity error. Either of these conditions also turns on the data light (D67).

Decimal/VFL Control

VFL Divide (A72) AV971: Light indicates status of the non-restore trigger. Non-restore trigger turns on and off during the divide process, depending on the value of the dividend digits. When on, trigger causes non-restore division to be performed; when off, trigger causes restore division to be performed.

VFL Overlap 0-7, 8-15 (A73, 74) KV125: During a VFL setup sequence, the starting addresses of the operands are compared. If starting addresses are from 0 to 7 bytes apart, the 0-7 overlap trigger is turned on; if starting addresses are 8 to 15 bytes apart, the 8-15 overlap trigger is turned on. These triggers control byte gating, such as from K and L to the decimal adder, to the AOE, and so on.

VFL Adder Carry (A75) AV611: On decimal arithmetic operations, this trigger turns on when there is a carry out of the high-order position of the decimal adder. Trigger provides the carry-in to the low-order position of the adder during the next add cycle.

Decimal Sign (A76) KV041: Light indicates status of minus sign trigger used to remember the sign of a decimal operand. Minus sign trigger is set at various times, such as during setup time, at the beginning of the iteration sequence, or during iterations, depending on the VFL operation. Uses of the

sign trigger include establishing the sign of the result on arithmetic operations and setting the condition code.

T1-T8 (A78-85) KV035-055: These triggers perform various functions on VFL operations, the function of each trigger depending on the instruction and the operation within the instruction. Description and use of triggers is given in Volume III, section VFL.

VFL Result Zero (B72) AV621: Light indicates that the result of a VFL operation is not zero. Light is reset off at the beginning of an operation and turns on when any result bytes placed into the K register are anything but zero. At the end of the operation, light on indicates that at least one of the bytes of the result is not zero.

VFL SAP Buffer (B73) KV135: For all SS instructions except MP, DP, TR, and TRT, trigger turns on at PF 4 of a prefetch sequence if BCU has received a storage address protect violation from storage on this fetch. At next prefetch sequence, SAP buffer trigger causes E interrupt trigger to turn on. The delay in turning on E interrupt trigger assures that the VFL operation is actually going to use the word that has the SAP check.

The first store-fetch sequence following the turn-on of the E interrupt trigger forces an E last cycle and terminates the operation. During E last cycle, the interrupt condition is detected by the interrupt controls and results in a program interrupt.

VFL Fetch Request (B74) KX351: Trigger turns on (1) during setup sequences to fetch the initial words of each operand, (2) during setup sequences or prefetch sequences to prefetch words of operand 2, and (3) during store-fetch sequences to fetch subsequent words of operand 1.

Fetch request trigger makes a fetch request of BCU, holding the request until BCU accept is returned. BCU accept turns the fetch request trigger off.

VFL Store Request (B75) KX351: Trigger turns on during a store-fetch sequence whenever a result word is to be stored; trigger makes a store request of BCU, holding request until BCU accept is returned. BCU accept turns the store request trigger off.

VFL End Sequence (B82) KV055: Trigger turns on during final store-fetch sequence of an operation to start the termination procedure. For decimal operations, final store-fetch sequence is determined by all bytes having been processed (Y and Z counters have stepped to 15). For logical operations, final store-fetch sequence is determined by Y and Z

coupled being equal to the IOP L field. The end sequence trigger is on for 1 cycle, its main purpose being to turn on E last cycle trigger.

Store-Fetch Sequence (C76) KV031: Trigger controls the use of the 12 VFL sequence triggers. Store-fetch trigger is reset off during the cycle following E last cycle to ensure that each VFL operation starts with trigger off. While off, the store-fetch trigger causes the 12 VFL sequence triggers to become setup sequencers. During cycle following the last setup cycle, store-fetch trigger turns on; while on, the trigger causes VFL sequence triggers 2-6 to become store-fetch sequencers.

On decimal multiply and divide, specification tests are made during setup cycle 2. If a violation is found, the store-fetch trigger is turned on immediately to force a store-fetch sequence and terminate the operation.

VFL Sequence 1-12 (C78-89) KV001-025: These lights show the status of the 12 VFL sequence triggers. Sequence triggers are used for both setup and store-fetch operations, depending on the status of the store-fetch trigger. See description of store-fetch indicator.

Iteration Sequence 1, 2, 3 (D74-76) KV131, 135: These lights show the status of iteration sequence (IS) triggers. Iteration sequencing varies with instructions. In general, however, iteration sequencers (in conjunction with instruction decoding) determine what operations are to be performed on each cycle that bytes are processed.

Prefetch Sequence 1-4 (D78-81) KV111, 115: These lights show the status of the prefetch sequence (PF) triggers. These four triggers establish the sequence for prefetching words of operand 2 such that an operand 2 word will always be available for processing before the prior word of operand 2 is exhausted.

Generally, the durations of prefetch 1 and 2 are one cycle each; the duration of prefetch 3 is a variable number of cycles, depending on storage priority; the duration of prefetch 4 depends on the type of storage (approximately 3 cycles for an M-4).

VFL Mark Sequencers A-D (D86-89) KV101, 105: On the translate and test, and the edit and mark instructions, mark sequencing triggers turn on in order, each staying on for one cycle. The four triggers gate the functions necessary to accomplish the mark portion of these instructions.

On decimal multiply, the four mark sequencing triggers provide the correct multiplier and multiplicand alignment during the multiply process; on decimal divide, the triggers provide dividend and divisor alignment during the divide process.

I Controls

Add Incrementer 19, 20 (E1, 2) AC341: The add incrementer 19 light indicates that a 1 is being added into position 19 of the incrementer; the 20 light indicates that a 1 is being added into position 20. The combination of these lights on, therefore, indicates whether the value 1, 2, or 3 is being added to the word address in the incrementer. These lights are not off of triggers, but rather are off of the logic that determines the amount to be added.

Decoded Gate Select (E5-12) RA243: These lights are off the gate select register decoder and indicate which group of 32 bits is gated out of the A-B registers. The gate select register (and the decoder outputs) normally changes at TON T2.

Instruction Counter A Execute (F1) KB041: Trigger (ICAE) turns on when an IC fetch to the A register is required due to the A register empty, or about to go empty, and no IC fetch blocking conditions present. Conditions that turn on ICAE trigger also make the fetch request, provided there are no inhibiting interrupt conditions. The ICAE trigger generates the return to AB line to BCU and steers the accept, if received, to turn on ICAM. The ICAE trigger turns off on any cycle during which the turn-on conditions are not present.

Instruction Counter A Memorize (F2) KB051: Trigger (ICAM) indicates that a fetch request to A has been made and accept has been received, but the data has not yet returned. The trigger prevents another fetch request (A loaded is still off). The ICAM trigger turns on by ICAE on and accept; it turns off by the coincidence of A advance, branch cancel A1 trigger off, and no turn-on conditions.

ICAM trigger may also turn on by a branch + 1 fetch to A. Turn-off is the same as described before.

Instruction Counter B Execute (F3) KB061: Trigger (ICBE) has the same function as ICAE except that it is for the B register. See description for ICAE.

Instruction Counter B Memorize (F4) KB071: Trigger (ICBM) has the same function as ICAM except that it is for the B register. See description for ICAM.

Block Instruction Counter Memorize (F5) KA141: Trigger (Block IC-M) blocks the generation of IC fetch addresses and blocks IC fetch requests. Trigger turns on by interrupt reset (a pulse that occurs when an interrupt sequence is started), or by TON T2 ANDed with I decode block IC. This later turn-on condition arises when an IC fetch must be blocked

in favor of an operand fetch, or when the incrementer must be used for some purpose other than IC address generation. The block IC-M trigger turns off by a signal generated by the unit that required the block (when the blocking requirement no longer exists).

IC Recovery (F6) KB081: Trigger indicates that the A-B registers do not contain the proper instructions and that a new IC fetch must be made. The trigger turns on by (1) a program store compare condition (a store has been made to an address that may have been prefetched to the A-B registers), or (2) the execution of an execute instruction whose object instruction does not branch, or (3) the IC being set with a new value, such as occurs on the load PSW instruction, on any interrupt, or on any of several manual operations. IC recovery trigger turns off by accept ANDed with the ICAE or ICBE trigger on.

IC High-Order Advance (F7) KB091: Trigger turns on by a gate select carry and I to E transfer and no interrupts; trigger turns off automatically after 1 cycle. The IC high-order advance trigger gates the ICR to the incrementer, at the same time gating a 1 into position 19 of the incrementer. Net result is to update the ICR to the correct value.

Gate Select Register (F8-12) KB331, 341, 371: The gate select register has 5 positions: carry, 20, 21, 22, and corrected parity. The gate select register is normally set from the gate select adder at TON T2; the gate select adder adds the instruction length code to the ICR value. Positions 20-22 of the gate select register determine which 32 bits are gated from the A-B registers to the IOP register.

A carry out of position 20 of the gate select adder turns on carry trigger (F8), which subsequently initiates a high-order advance.

Each update of the ICR may or may not change the parity of ICR byte 16-23. As the gate select register is set, the corrected parity trigger (F12) is set to indicate what the new parity of ICR 16-23 should be after the ICR updating.

T1, T2, (G1, 2) DA031: The T1 trigger is the first of the 2 preparation sequencers. Main function of T1 cycles is to generate the storage operand address (effective address).

The T2 trigger is the second preparation sequencer. Main function of T2 cycles is to deliver operands from general or floating point registers to executing units.

T1 turns on at the start of every instruction preparation and may stay on for any number of cycles. T2 turns on when T1 turns off; T2 may stay on for any number of cycles, turning off when the preparation is complete. If the preparation of the next instruction is to start immediately, T1 immediately follows T2.

General Register Out (G4) DA021: Trigger (GROUT) gates general registers to the RBL during instruction execution. For any instruction requiring this gating, GROUT is turned on at I to E transfer by BOP decoding. Gating continues through E cycles as long as GROUT is on; GROUT is turned off by the executing unit when this gating is no longer required.

Operand Fetch (G5) KB171: At TON T2, IOP decoding determines whether a fetch is required. If a fetch is required, IOP decoding makes the fetch request and turns on the operand fetch trigger, which maintains the request until accept is received. Accept turns off the operand fetch trigger.

Storage to Storage Operation (G7) KB101: IOP decoding turns on the storage to storage operation (SS Op) trigger to gate the D field of IOP and the general register designated by the B field of IOP to the addressing adder during E cycles. VFL controls send a signal (VFL thru) to the I unit to turn off SS Op when storage addressing is no longer required.

SS Op trigger also locks the original ICR value in the gate select pre-latch so that when the ICR is changed at the I to E transfer, the original ICR value is still available for VFL use.

E Busy (G8) KB121: Trigger turns on at I to E transfer indicating that E unit has been started. E busy turns off at E last cycle. E busy trigger, in conjunction with the IE busy trigger and the last cycle sequencers, determines when the next execution can be started (I to E transfer).

No Retry (G12) KC071: Indicator turns on when any of 4 conditions arises:
  1. BCU check (storage data, CPU addresses, sync check)
  2. Incrementer check
  3. SAP check
  4. Modar trigger on

The no retry indicator is not off of a trigger, but rather off of an OR of the above 4 lines. The purpose of the indicator is to logout the fact that, upon the occurrence of a machine check, the instruction in process at the time cannot be retried.

Block T1 Memorized (H1) KA031: At I to E transfer, an execution unit starts and, normally, the I unit starts preparing the next instruction. If, however, the execution of the instruction requires the use of a machine area that would also be used by T1, T1 is prevented from turning on at I to E transfer. The block T1 memorized trigger turns on at this time (I to E transfer) to retain the blocking condition for T1 until the execution unit is through with the machine

area in question. Block T1 memorized trigger is turned off by the executing unit whenever the blocking of T1 is no longer required.

Block T2 Memorized (H2) KA041: Trigger serves the same function for T2 cycles as the block T1 memorized trigger does for T1 cycles. In addition, block T2 memorized turns on for branch instructions to hold off the actions of T2 until it is decided whether the branch is successful.

Block T2 memorized is turned on by BOP decoding at I to E transfer time; it is turned off by the executing unit when the blocking of T2 is no longer required.

IOP Loaded (H3) KB151: The IOP loaded trigger indicates that the next instruction to be prepared has returned from storage and is in the A-B registers. IOP loaded on during T1 indicates that the instruction to be prepared has been set into IOP.

IOP loaded is one of the conditions for the turn-on of T2. Turn-on of IOP loaded considers the gate select register, bits 0 and 1 of IOP, and the A and B loaded triggers. Turn-on pulse is a B clock.

IOP loaded turns off at any B time that the turn-on conditions are not present.

Floating Point Registers Out (H4) KB141: On floating point operations, trigger (FLOUT) gates floating point registers, instead of general registers, to the RBL during T2 cycles and E cycles. FLOUT turns on by I decode floating point operation and TON T2. E unit turns off FLOUT whenever the floating point register gating is no longer required.

Store Request (H5) KB201: Store request can be initiated by BOP decode store request and I to E transfer, or by E store request, or by IE store request. The condition that makes the store request also turns on the store request trigger, which (1) maintains the store request until accept is received for I unit stores, and (2) initiates a program store compare for all stores. Store request trigger is turned off by the accept.

VFL Address (H7) KB111: Trigger is turned on by the SS Op trigger on and I to E transfer. VFL address trigger conditions the gate select adder circuits so that the proper address field of the instruction in the A-B registers will be gated into IOP. VFL address trigger turns off when the SS Op trigger is off and the final store request has been accepted.

IE Busy (H8) KB131: Trigger turns on at I to E transfer whenever the IE unit or the branch unit is to be used in the execution of the instruction. (An exception is the execute instruction, which does not set

a busy trigger.) IE busy turns off at IE last cycle or branch last cycle. IE busy trigger, along with the E busy trigger and the last cycle sequencers, determines when the next I to E transfer may be made.

Branch Operation (J1) KB521: This trigger is the first of three branch unit sequencers (the other two are test complete and branch last cycle). The branch operation trigger turns on at TON T2 and I decode branch op. When on, it defines the operation as a branch, generates the return to A-B for the branch fetch, and initiates the branch + 1 fetch.

The branch op trigger turns off for unsuccessful branches by test complete and branch unsuccessful; it turns off for successful branches when the branch fetch has been returned and the branch + 1 fetch has been accepted.

Branch Memorized (J2) KB581: Trigger remembers that the branch fetch has been accepted by BCU but has not yet been returned. Branch memorized turns on by the accept pulse and branch op and op fetch latches on. Branch memorized turns off by the advance for the branch fetch or by the setting of a cancel trigger for the branch fetch.

Branch + 1 Execute (J3) KB611: The branch + 1 request is made and the branch + 1 execute trigger (Br + 1 E) is turned on at I to E transfer for all branch instructions except branch on condition and branch on index. The Br + 1 E trigger maintains the branch + 1 fetch request until the fetch is accepted, or until the branch is determined unsuccessful. The Br + 1 E trigger turns off by the accept pulse or by test complete and branch unsuccessful.

For branch on condition instructions, the Br + 1 E trigger is turned on, and the branch + 1 fetch is made only if the branch is successful. In this case, the turn-on of the Br + 1 E trigger and the fetch request occur at I to E transfer (not E set CR), or one cycle later. For BXH or BXLE, Br + 1 E is turned on at I to E transfer, but the fetch is not made until one cycle later.

Branch + 1 Memorize (J4) KB571: Trigger indicates that the branch + 1 fetch has been accepted. The branch + 1 memorize (Br + 1 M) trigger turns on by pulse accept and the Br + 1 E trigger on. The Br +1 M trigger turns off by branch last cycle. At branch last cycle, if the branch + 1 fetch is still outstanding, this fact is remembered by a branch cancel trigger if the branch was unsuccessful, or by the ICAM or ICBM trigger if the branch was successful.

Test Complete (J5) KB501: This trigger is the second of three sequencers used on branch operations. Test complete is turned on at I to E transfer for

unconditional branches (BALR, BAL, EX) or for branch on condition instructions (BCR, BC). For the remaining branch instructions, a line from the E unit (E TON Tsts Cmplt) turns on the test complete trigger at the beginning of the second E cycle (for BCTR, BCT), or at the beginning of the third E cycle (for BXH, BXLE).

The test complete trigger controls the disposition of the fetches according to the successfulness of the branch.

For successful branches, test complete trigger turns off when the branch fetch has returned and the branch + 1 fetch has been accepted; for unsuccessful branches, it turns off by test complete on and branch unsuccessful.

Branch Last Cycle (J6) KB531: This trigger is the third of three sequencers for branch operations. Branch last cycle turns on when the test complete trigger turns off (see description of the test complete indicator). Branch last cycle terminates the branch operation; for successful branches, it sets the ICR with the branch address.

The branch last cycle trigger turns off automatically after one cycle.

For the execute instruction, branch last cycle is not used; instead, the execute sequence trigger (XEC SEQ) terminates the operation.

Branch Successful Memorized (J7) KB591: Trigger remembers that conditions for branching have been met. Trigger turns on the cycle following the turn-on of the test complete trigger and turns off the cycle following branch last cycle.

Branch Cancel A1, B1, A2, B2 (J8-11) KB691, 711: Branch cancel triggers are turned on to remember that outstanding branch fetches are to be discarded. Turn-on occurs during test complete if the branch fetch is outstanding and the branch is unsuccessful. The four cancel triggers allow two successive unsuccessful branches to be executed without waiting for outstanding branch fetches to return.

Each cancel trigger turns off by its corresponding advance pulse.

Execute Sequence (H11) KB541: For execute instructions, the execute sequence trigger turns on in place of the branch last cycle trigger. Like branch last cycle, the execute sequence trigger terminates the branch instruction (in this case, execute), but in addition, accomplishes the necessary ORing of general register contents into IOP along with the object instruction. Execute sequence trigger turns off by IOP loaded.

Execute Operation (H12) KB511: Trigger turns on along with the execute sequence trigger and remains on throughout the execution of the object instruction.

Execute operation trigger controls those functions peculiar to the object instruction's execution, such as the blocking of normal IC fetches and the starting of an IC recovery.

IE 1, 2, 3, Last (K1-4) KD061, 081, 131: These four triggers are the sequencers for the I-execute unit. The instructions performed entirely by the I-execution unit are: load PSW, diagnose, set program mask, branch no-op, set key, start I/O, test I/O, halt I/O, and test channel. The instructions performed by the IE unit and the E unit combined are: set system mask, insert key, load multiple, and store multiple. The I-execution unit also performs a portion of IPL.

Two or more of the IE sequencers are used in each of the above instructions. The order of their turn-on and their specific use vary with the instruction being executed. All four sequencing triggers are turned on and off with A clocks; their outputs are latched under control of the L clock.

IM1, IM2 (K6, 7) KD101: Sequencing triggers, used only on the load multiple and store multiple instructions. IM1 and 2 turn on and off alternately, working in conjunction with the IE sequencers, as half-words are fetched from or stored into storage; IM1 controls storage left-half words, and IM2 controls storage right-half words.

ER1 Equals IR2 (K8) KX171: This latch indicates that all but the last of the half-words of a load multiple or store multiple instruction have been processed. The latch on causes the last half-word to be processed, and leads to an E last cycle, which terminates the E unit's part on these instructions.

Release Buffer (K9) KD141: Trigger is used only on channel instructions and IPL. Purpose is to synchronize the release signal from the channel to CPU timing. Once on, the release buffer turns on the release trigger the following CPU cycle.

Release (K10) KD141: Trigger is used only on channel instructions and IPL. The release trigger is turned on by the release signal from the channel (via the release buffer trigger). On channel instructions, the release trigger turns off IE1, turns on IE3, and generates the lines to set the condition code in the PSW and reset the channel priority circuits.

On IPL, the release trigger turns off IE1 and IE3 and initiates the interrupt sequence that will load the PSW register.

Modified Addressable Register (K11) KC081: Trigger (MODAR) turns on in the course of an instruction whenever a general register, a floating point register, the PSW, or a storage location has been changed. Besides being indicated on the console (and logged

out), the Modar trigger is ANDed with certain machine check conditions to bring up no-retry, meaning that the instruction that caused the machine check might have its own operand, therefore being non-retryable.

MODAR trigger turns off (1) during a control last cycle or during an interrupt last cycle, provided no interrupts are outstanding, and (2) at the start of an IC recovery.

The CPU reset that occurs during an IPL or following a machine check-caused logout turns MODAR trigger on because the IPL or the machine check interrupt would have changed the PSW. Any other CPU reset turns MODAR trigger off.

Last Cycle E Memorized (K12) KC081: Trigger (LCEM) turns on when MODAR turns off. LCEM turns itself off after one cycle. The LCEM trigger is effectively a one-cycle extension of MODAR. Purpose of LCEM is to bring up no-retry in the case where a machine error occurs in the E unit during E last cycle and an addressable register has been changed during the execution of the instruction.

Interrupts

Machine Check Control (L1) KF571: Trigger starts the machine check interrupt sequence that follows a machine check-caused logout. Trigger turns on with CPU reset and starts the interrupt sequence after CPU reset is completed. Trigger turns off at the end of the interrupt sequence.

CPU SAP (L4) MB631: This trigger, located in the BCU, is turned on by a storage address protection violation (on a store) and retains the SAP condition until the interrupt (program) is taken. Trigger turns off by interrupt end reset, which occurs at interrupt cycle 5.

CPU Store Invalid (L5) MB603: This trigger, located in the BCU, is turned on when the BCU detects an invalid address (one outside available storage) at the addressing OR on a CPU store operation. The CPU store invalid trigger retains the invalid address condition until the interrupt (program) is taken. Trigger turns off by interrupt end reset, which occurs at interrupt cycle 5.

I Program Interrupt (L7) KF141: Trigger turns on whenever any of the I program group of interrupt conditions occurs, or when the supervisor call instruction is decoded. At I to E transfer time, provided there are no E interrupt conditions, the I program interrupt trigger turns on the I interrupt end trigger, which is the entrance trigger for the "I from I" class interrupt sequence. I program interrupt trigger turns off by interrupt end reset, which occurs at interrupt cycle 5.

IC Recovery Required (L8) KF621: Trigger turns on when a program store compare condition occurs (an instruction stores into the location of a possible next instruction to be executed), or when an execute instruction is executed and its object instruction does not branch. Either of these conditions requires that an IC recovery operation take place. At E last cycle, the EXIT trigger turns on, and if the condition necessitating the IC recovery has priority over other outstanding interrupt conditions, the IC recovery trigger in the I unit turns on and causes an IC fetch to the A-B registers. The EXIT trigger turning on turns off IC recovery required.

Timer Advance Required (L9) KF641: A timer advance signal (60-cycle) from the power supply fires a 500 nanosecond single-shot, which is subsequently synchronized with CPU cycles by a timer advance sync polarity hold circuit. The next AR clock turns on the timer advance request trigger; the timer advance required indicator is off this trigger. Timer advance request stays on until a timer advance interrupt is taken, and turns off at the end of interrupt cycle 2.

Interrupt Priority Hold (L10) KF621: This trigger turns on along with EXIT or I interrupt end and stays on throughout most of the interrupt sequence, turning off at the end of interrupt cycle 5 (for timer advance request sequence, at the end of interrupt cycle 2). Purpose is to prevent EXIT trigger from turning on again once an interrupt sequence is under way.

I Interrupt End (L11) KF131: This is the entrance trigger to the interrupt sequence for those interrupt conditions detected in the I unit during T1 or T2. Trigger is turned on at I to E transfer time and remains on for 1 cycle. Purposes of the I interrupt end trigger are to block the I unit from further processing and to turn on interrupt cycle 1.

EXIT (L12) KF131: This is the entrance trigger to the interrupt sequence for those interrupt conditions detected during the control last cycle of an instruction execution, or during wait, or during the last cycle of another interrupt sequence. Trigger is turned on immediately following the control last cycle, or immediately following the interrupt last cycle, or anytime during wait that the interrupt request is recognized. Once on, EXIT remains on for 1 cycle. Purposes are to block further I unit processing and to turn on interrupt cycle 1.

External Interrupts, Timer (M1) KS091: The timer trigger indicates that the timer word overflowed (went from a positive to a negative value) during a timer update. Timer trigger turns on during the timer update interrupt sequence by the timer subtract latch on and an overflow condition in the main

adder. The timer trigger sends a timer interrupt request to the interrupt controls. Since the only interrupt conditions that can be detected at the end of an interrupt sequence (the timer update in this case) are external and I/O interrupts, and external has priority over I/O, the external interrupt (timer overflow) is always taken immediately following the timer update sequence that caused it. (All external interrupts must be enabled by PSW bit 7.)

The timer trigger turns off at cycle 4 of the external interrupt sequence.

External Interrupts, Console (M2) KF641: The light is off the console interrupt trigger. Trigger turns on when the interrupt button on the console is pressed. The console interrupt trigger sends an interrupt request (external) to the interrupt controls, holding up the request until an external interrupt is taken. (External interrupt requests must be enabled by PSW bit 7.) The console interrupt trigger turns off at cycle 4 of the external interrupt sequence.

External Interrupts 1-6 (M3-8) KF681-701: These lights are off the 6 external signal interrupt triggers, and indicate external interrupt signals from another computer. External signal interrupt trigger outputs are OR'ed to send an interrupt request to the interrupt detection logic. (External interrupt requests must be enabled by PSW bit 7.) External signal interrupt triggers remain on until the external interrupt is taken, turning off at cycle 4 of the external interrupt sequence.

Channel Interrupt Outstanding (M1) KD651: This light is off the channel interrupt trigger, and indicates that an interrupt request has been received from one of the channels. The channel interrupt trigger sends the request on to the interrupt detection logic. At control last cycle, interrupt last cycle, or during wait, the interrupt request turns on the EXIT trigger, which starts an interrupt sequence. If I/O interrupts have priority, the sequence becomes an I/O interrupt. The channel interrupt trigger (and consequently the I/O interrupt request) turns off: (1) at cycle 5 of any interrupt sequence, (2) on any operation that might change the system mask bits in the PSW, such as the load PSW instruction, the set system mask instruction, or a manual set IC or PSW; and (3) on a channel instruction.

The same reset that turns off the channel interrupt trigger also turns off the channel priority triggers, and a new channel priority is immediately set up if any channel request is still up from the channels. In this case, the channel interrupt trigger turns on again, making an interrupt request for the newly established channel priority.

Channel Interrupt Response (N2) KF611: When EXIT trigger turns on and I/O interrupt has priority, channel interrupt response trigger turns on to send a channel response signal to the channel that was granted interrupt priority. Channel interrupt response trigger stays on until CPU receives a release signal from the channel.

Channel Interrupt Release (N3) KF611: Channel interrupt release trigger turns on when release signal is received from the channel. The channel interrupt sequence started when the EXIT trigger turned on, but stopped after cycle 1 to wait for release signal from the channel. Channel interrupt release trigger sets the unit address into the PSW that will be stored and turns on interrupt cycle 2 to continue the interrupt sequence. Channel interrupt release trigger turns off automatically after one cycle.

Channel Priority Interrupt 0-6 (N4-10) KD631, 641: These lights are off the priority A triggers and indicate which channels have made I/O interrupt requests. The 7 triggers feed a priority circuit in which one of the requests is selected for an interrupt. Triggers are turned off by the same conditions that turn off the channel interrupt trigger. See description of channel interrupt outstanding indicator for the turn-off.

Interrupt Sequence Cycles 1-6, Last (P1-7) KF581-601, 631: These lights indicate status of interrupt sequencing triggers. Most interrupts use all 7 sequencers. The following three interrupts, however, use only the sequencers listed:
    Timer advance request: 1, 2, last.
    Initial Program Load: 1, 2, 5, 6, last.
    Recovery only: none.

Interrupt Load Buffer (P8) KF651: This light is off the IPL buffer trigger. On an IPL load PSW interrupt, a fetch of the new PSW is made, but no store. Consequently, interrupt cycles 3 and 4 are not needed. The IPL buffer trigger fills the gap between the time interrupt cycle 2 trigger turns off, and interrupt cycle 5 trigger turns on. IPL buffer trigger turns on by BCU accept (when cycle 2 goes off) and turns off when interrupt cycle 5 turns on, which is at the A clock following J loaded.

E Interrupt (Q1) KX071: Trigger turns on when any of a number of interrupt conditions occurs during instruction execution. Trigger retains the fact that an E program interrupt condition occurred, and at E last cycle vies with any other interrupt conditions to obtain interrupt priority. The particular E unit interrupt condition that occurred is indicated by one of the lights Q2 through Q12, or P12.

If E program obtains priority, a program interrupt is taken; the current PSW (before it is stored) is set with an interrupt code corresponding to the condition causing the interrupt.

E interrupt trigger turns off at interrupt end reset (cycle 5 of an interrupt sequence).

Fixed-Point Overflow (Q2) KX915: This condition occurs whenever significant bits are lost due to a high-order carry on fixed-point addition or subtraction or significant bits are lost due to a shift on a shift-left operation. The condition turns on the E interrupt and fixed-point overflow triggers provided fixed-point overflow is enabled by a bit in PSW 36. E interrupt trigger requests an interrupt, and, if E interrupt is taken, the fixed-point overflow trigger sets interrupt code 1000 into the PSW.

Fixed-point overflow trigger turns off along with the E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Fixed-Point Divide (Q3) KX921: This trigger and the E interrupt trigger turn on whenever the quotient of a fixed-point division (or the result of a convert to binary operation) exceeds the size of its receiving register. If E program interrupt is taken, the fixed-point divide trigger sets interrupt code 1001 into the PSW.

Fixed-point divide trigger turns off along with the E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Address Invalid (Q4) KX911: This trigger and the E interrupt trigger turn on during instruction execution whenever a fetch is tried from an invalid storage address and the storage data is to be used in the operation. If E interrupt is taken, the address invalid trigger sets interrupt code 101 into the PSW.

Address invalid trigger turns off along with the E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Floating-Point Divide (Q5) KX935: This trigger and the E interrupt trigger turn on during a floating point divide operation if an attempt is made to divide by zero. If the E program interrupt is taken, floating point divide trigger sets interrupt code 1111 into the PSW.

Floating-point divide trigger turns off along with the E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Exponent Overflow (Q6) KX925: This trigger and the E interrupt trigger turn on during a floating point arithmetic operation if the result characteristic exceeds 127. If E program interrupt is taken, the exponent overflow trigger sets interrupt code 1100 into the PSW.

Exponent overflow trigger turns off along with the E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Significance (Q7) KX931: This trigger (also called lost significance) and the E interrupt trigger turn on if the result of a floating point addition or subtraction has an all-zero fraction and there is an enabling bit in PSW 39. If E program interrupt is taken, the significance trigger sets interrupt code 1110 into the PSW.

Significance trigger turns off along with E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Exponent Underflow (Q8) KX931: This trigger and the E interrupt trigger turn on during a floating point arithmetic operation if the result characteristic goes less than zero and there is an enabling bit in PSW 38. If E program interrupt is taken, the exponent underflow trigger sets interrupt code 1101 into the PSW.

Exponent underflow trigger turns off along with E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Data Invalid (Q9) KX915: This trigger and the E interrupt trigger turn on during a VFL operation if the sign or digit codes of operands are not correct, if the fields overlap incorrectly, or if a multiplicand has too many high-order significant digits. If E program interrupt is taken, data invalid trigger sets interrupt code 111 into the PSW.

Data invalid trigger turns off along with E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Decimal Overflow (Q10) KX921: This trigger and the E interrupt trigger turn on during a decimal operation if the destination field is too small to contain the result and if there is an enabling bit in PSW 37. If E program interrupt is taken, the decimal overflow trigger sets interrupt code 1010 into the PSW.

Decimal overflow trigger turns off along with E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Decimal Divide (Q11) KX925: This trigger and the E interrupt trigger turn on during a decimal divide operation if the quotient exceeds the specified data field size. If E program interrupt is taken, the decimal divide trigger sets interrupt code 1011 into the PSW.

Decimal divide trigger turns off along with E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

Specification (Q12) KX911: This trigger and the E interrupt trigger turn on during decimal multiply if the multiplier exceeds 15 digits and sign, or if the multiplier is not shorter than the multiplicand; the triggers turn on during decimal divide if the divisor exceeds 15 digits and sign or if the divisor is not shorter than the dividend. If E program interrupt is taken, the specification trigger sets interrupt code 110 into the PSW.

Specification trigger turns off along with E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

E Interrupt SAP (P12) KX935: This trigger and the E interrupt trigger turn on if a SAP violation occurs on (1) a fetch to J (the J SAP trigger turns on); or (2) a prefetch to J on VFL (the VFL SAP buffer trigger turns on). If E program interrupt is taken, the E interrupt SAP trigger sets interrupt code 100 into the PSW.

E interrupt SAP trigger turns off along with E interrupt trigger at interrupt end reset (cycle 5 of an interrupt sequence).

I Registers

A-B OR (E15-50) RA201-231: Indicators show the bits from the A register or the B register that are being gated into IOP. Gate select register determines which group of 32 bits is gated from A or B.

Instruction Operation Register (F15-50) RA251-281: Indicators show status of individual IOP positions. IOP sets by an A clock of T1 cycles.

Buffer Operation Register (G15-28) RB511, 011: Register (BOP) is set by an A clock of a T2 cycle provided the IE unit is not busy. If the IE unit is busy, BOP sets by an A clock of IE last cycle.

R1 portion of BOP can also be set independently from the BR1 incrementer by IE increment BR1.

Execution Operation Register (G37-50) RB011, RN011: Positions 0-7 of this register (EOP) are set from IOP 0-7 at least 1 cycle before I to E transfer. Positions 8-11 (ER1) are set from BOP 8-11 at every I to E transfer, or from the ER1 incrementer by increment ER1.

H Register (H15-41) RH111: Register sets from the addressing adder at TON T2, or for multiple load/store and VFL operations, from the incrementer.

Last Cycle Operation Register (H42-50) RN061-075: Register (LCOP) sets from EOP 0-7 not later than A time of the first E cycle of an execution. LCOP register provides operation decoding for the last cycle of an execution so that EOP can be freed to receive the next operation code.

Storage Address Register (J15-41) MB111-131:
Storage address register (SAR) is set in parallel
with the H register from either the addressing adder
or the incrementer (see description of H register in-
dicators).

The only output of SAR is to the addressing OR,
which gates either the address in SAR or the address
on the channel address bus to main storage.

CPU Marks (J42-50) MB303-323: Mark register
holds the eight mark bits used for CPU store oper-
ations. For instructions that store half words or
multiples of half words, mark register positions are
set in pairs from BOP decoding and the decoding of
the 3 low-order positions of the H register. Set oc-
curs at I to E transfer.

For instructions that store single or variable
numbers of bytes, the mark register is set from the
T pointer, a single mark register position being set
as each result byte is processed.

Mark register is reset by CPU accept on stores
and test and set. As the mark register is reset, the
mark parity bit is set on so that it will indicate odd
parity for an empty register. As pairs of mark reg-
ister positions are set (half word or multiple half
word instructions), the parity position is left undis-
turbed, always indicating odd parity. As individual
mark register positions are set (VFL), parity posi-
tion is complemented, keeping the total bit count odd.

Invalid A Register, B Register (E52, 53) RA185: In-
valid A Reg is set by A advance, and invalid B Reg is
set by B advance if their corresponding register, A
or B, is being set and if the BCU has raised the in-
valid A-B line (the BCU detected an invalid address
at the addressing OR). Invalid A Reg and invalid B
Reg turn off by the next A advance or B advance,
respectively, that is not accompanied by the invalid
A-B condition from BCU.

If the gate select register gates any portion of A
or B to IOP, and the gated register is flagged invalid
by its invalid trigger, an invalid address signal is
sent to the interrupt controls, causing a program in-
terrupt.

**A Register Loaded, B Register Loaded (F52, 53)
KB651, 661:** A register loaded trigger turns on when
data is loaded into the A register; similarly, the B
register loaded trigger turns on when data is loaded
into the B register. Triggers turn on at storage ad-
vance time; they turn off at TON T2 when the present
instruction being prepared is the last one in their
corresponding register (A or B). Either trigger off
is a main condition for an IC fetch.

Storage Address Protect A, B (G52, 53) RA191: SAP
A trigger is set by A advance, and SAP B trigger is
set by B advance if their corresponding registers, A
or B, are being set and if the BCU has raised the
SAP A-B line (the BCU received an address protec-
tion violation condition from storage on a fetch).
SAP A and SAP B turn off by the next A advance or
B advance, respectively, that it not accompanied by
the SAP A-B condition from BCU.

If the gate select register gates any portion of A
or B to IOP, and the gated register is flagged invalid
by its SAP trigger, A SAP signal is sent to the inter-
rupt controls, causing a program interrupt.

Binary Status

Quotient Insert, Z Valid (E56) RJ951: Trigger indi-
cates that the Z quotient trigger contains a 3rd quo-
tient bit, derived from an iteration that used the 3/4
multiple. The Z valid trigger causes this quotient
bit to be inserted in place of the first quotient bit
generated by the following iteration.

Z valid trigger turns on in the cycle following the
3/4-multiple iteration and turns off 1 cycle later.

Quotient Insert, Z Quotient (E57) RJ951: Trigger
stores the 3rd quotient bit (on if a 1; off if a 0) gen-
erated on a 3/4-multiple iteration. This quotient bit
is inserted into the J register in place of the first
quotient bit generated on the next iteration.

Quotient Insert, Dividend True (E58) RJ951: Dividend
true trigger is set after each iteration according to
whether the partial dividend is true (on) or comple-
ment (off). Status of trigger helps select the proper
quotient bits and helps select the divisor multiple to
be used in the next iteration.

Quotient Overflow (E59) RJ991: Trigger turns on at
the end of the first iteration if the first quotient bit
generated is a 1 (the first quotient bit should be a
zero). In fixed divide this condition constitutes a
divide check and results in an E program interrupt.

Quotient Sign Overflow (E60) RJ991: Trigger turns
on at the end of the first iteration if the second quo-
tient bit is a 1. This condition constitutes a divide
check (in fixed divide) unless the developed quotient
is a maximum negative number (100---00) that will
be complemented due to the original operand signs
being unlike.

Complement Partial Product (E61) RJ951: Trigger
is used only on floating point multiply. When a par-
tial product in the K register is gated R4 to the adder,
and the partial product is in complement form, the
complement partial product trigger forces 1-bits in-
to adder positions AM 0, 1, 2, and 3.

Complement partial product trigger is on for the
cycle in which R4 K-to-adder transfer occurs.

Floating Register 2 (E62) RP074: Trigger turns on for all RR instructions but has significance only on floating point RR instructions. Trigger turns on at T2 time to gate the FP register specified by the R2 field to the J register; trigger turns off at I to E transfer time to gate FP register specified by the R1 field to the M register. Floating register out trigger (FLOUT) must be on to complete gating of the FP registers to the RBL.

E Reset (F56) KX605: Trigger turns on with computer reset or system reset and turns off with the first A clock following the reset; trigger provides a reset for the K register, the exponent register, and the shift counter.

Branch Successful (F58) KS001: This E unit trigger is used on the branch-on-count and the branch-on-index instructions to indicate that the condition for branching has been met. Branch successful trigger (which is on for one cycle) turns on the branch successful latch in the branch unit. The branch successful latch indicates that branch fetches will be used.

R1 Sign (F61) KS121: Trigger indicates the sign of operand 1 (on for minus; off for plus). Trigger turns on when contents of a general or floating point register are gated to the RBL (during T2) if the register contains a 1 in position 0. R1 sign trigger turns off at the beginning of the next execution.

R2 Sign (F62) KS121: Trigger indicates the sign of operand 2 (on for minus; off for plus). Operand 2 can come from a general register, floating point register, or from storage. R2 sign trigger sets in the same manner as R1 sign trigger if operand 2 comes from a general or floating point register. If operand 2 comes from storage, the R2 sign trigger sets from a 1-bit in J0 or J32 each cycle that the first fixed point sequencer is on. R2 sign trigger turns off at the beginning of the next execution.

For half-word expansions, the R2 sign trigger is set from position 8 of the main adder.

AM, Complement (G56) KS042: Depending on the operation code and the operand signs, this trigger turns on at A time to complement the operand gated into the T/C side of the main adder. Complement trigger turns off at the next A clock.

AM, Hot 1 (G57) KS042: Trigger turns on at A time to effect a 2's complement addition in the main adder. Trigger turns off at the next A clock.

AM, End Around Carry (G58) KS042: Trigger turns on at A time to gate a carry out of the high-order position of the main adder back into the low-order position. Trigger turns off at the next A clock.

AM, Carry Out Zero (G59) KS025: Trigger turns on the cycle following the adder cycle if there was a carry out of position 0 of the main adder. Trigger turns off if there are no turn-on conditions at A time.

AM, Carry Out One (G60) KS025: Unless inhibited, this trigger turns on the cycle following the adder cycle if there was a carry out of position 1 of the main adder.

AE, Complement (H56) KS063: Trigger has the same function for the exponent adder as the AM complement trigger has for the main adder. See description of AM complement indicator.

AE, Hot 1 (H57) KS521: Trigger has the same function for the exponent adder as AM hot 1 trigger has for the main adder. See description of AM hot 1 indicator.

Pre-Shift (H58) KS072: On floating-point add, subtract, and compare, this sequencing trigger controls pre-shifting necessary to align the exponents. Trigger turns on following the 1st FLP cycle and turns off when pre-shifting is completed.

Exponent Overflow (H59) KS301: Trigger indicates that during a floating point operation, the result characteristics exceeded 127. This condition results in an E program interrupt.

Exponent Underflow (H60) KS311: Trigger indicates that during a floating point operation, the result characteristic went less than zero. This condition, if enabled by a bit in PSW 38, results in an E program interrupt.

M Register to Shift-Decrement Decoder (J56) KS082: Trigger turns on whenever shift-decrement decoder is to decode data contained in the M register. Decoding occurs on floating point arithmetic operations and on fixed point divide. Trigger turns on at the beginning of the cycle in which decoding is required and turns off at the beginning of the next cycle.

H Register to Shift-Decrement Decoder (J57) KS501: This trigger, used on shift instructions, allows shift-decrement decoder to decode data contained in the H register. Trigger turns on at the beginning of the cycle in which decoding is required and turns off at the beginning of the next cycle.

Shift Counter to Shift-Decrement Decoder (J58) KS501: This trigger, used on floating point arithmetic, fixed point divide, and shift instructions, allows shift-decrement decoder to decode the contents of the shift counter. Trigger turns on at the beginning of the cycle in which decoding is to occur and turns off at the beginning of the next cycle.

ER 0-7 to AE (J60) KS511: This trigger, used on floating point instructions, turns on to gate the exponent register to the AE side of the exponent adder. Trigger turns on at the beginning of the cycle in which the transfer is to occur and turns off at the beginning of the next cycle.

ER 0-7 to AE T/C (J61) KS511: This trigger, used on floating point instructions, turns on to gate the exponent register to the TC side of the exponent adder. Trigger turns on at the beginning of the cycle in which the transfer is to occur and turns off at the beginning of the next cycle.

SC 0-7 to AE T/C (J62) KS521: This trigger, used on floating point instructions, turns on to gate the shift counter to the TC side of the exponent adder. Trigger turns on at the beginning of the cycle in which the transfer is to occur and turns off at the beginning of the next cycle.

Binary Sequence Control

1st Cycle Memorized (E67) KT055: Trigger turns on immediately following first valid execution cycle of fixed point, floating point, or VFL operations, and stays on until the end of E last cycle. Trigger indicates that the first valid cycle of an execution has occurred.

J Loaded (E70) KT045: Trigger turns on by the same pulse that sets the J register and indicates that J register now contains new data. J loaded trigger turns off, generally, when J register data are used (gated out to some destination).

J Address Invalid (E71) KT047: If fetch request is made of an invalid storage address (one outside available storage), storage is cancelled; if J was specified as the return register, J advance sets the panel key contents into the J register and turns on the J address invalid trigger. When the instruction tries to use the contents of J, an E program interrupt occurs, placing the invalid address code (101) into the interrupt code field of the old PSW. J address invalid trigger turns off when the J register is next loaded with valid data.

J SAP (E72) KT049: If a fetch is attempted from a read-protected storage location, with J specified as the return register, the J advance pulse sets all zeros with good parity into the J register and turns on the J SAP trigger. When the instruction tries to use the contents of the J register, an E program interrupt occurs, placing the SAP code (100) into the interrupt code field of the old PSW. The J SAP trigger turns off when the J register is next loaded with valid data.

Store (E73) KX081: Trigger turns on during any of the store-type instructions to indicate that the storage reference is to be a store. Trigger turns off whenever there are no conditions for turn-on.

Accept (E74) KT051: Trigger turns on when accept is received from the BCU and turns off after 1 cycle; trigger determines when the store multiple operation may proceed, and when the load multiple operation may proceed when on single-cycle.

Release Cycle (E75) KX015: Trigger times the release of general and floating point registers. Trigger turns on at late B of the cycle preceding the cycle in which the register is set, and turns off at late B of the next cycle. For double put-aways, release cycle is on for two consecutive cycles.

Block Put-Away (E76) KX075: This trigger and its turn-on conditions prevent turn-on of the release cycle trigger, thereby blocking release of general or floating point registers. Put-away is automatic in E last cycle unless blocked; put-away is blocked on those instructions that do not require a put-away, such as compare, and, in certain instances of program errors, such as invalid address.

1st Fixed-Point (F66) KT055: Trigger is primarily used as the first sequencing trigger in fixed point instructions, fixed sequence VFL instructions, and those branch instructions using the E unit.

Half-Word or Logical (F68) KT025: Trigger is the second sequencer on certain fixed-point half-word instructions, used to complete the second half of half-word expansions. Trigger is the second sequencer on certain VFL fixed-sequence instructions (its use depending on the instruction) and also on the insert key instruction.

Half-Word Add (F69) KT025: A sequencing trigger for the half-word instructions load, add, subtract, and compare. Trigger turns on following the half-word/logical sequencer and remains on for 1 cycle.

EM1, EM2 (F70, 71) KT065: These triggers are sequencers for the load multiple and store multiple instructions. EM1 is associated with the transfer of the left half of the double words from the J register to the general register (load multiple), or from the general register to the K register (store multiple). EM2 alternates with EM1 to control data flow of the right half of the double words. Both sequencers increment ER1.

Convert (F73) KT071: Trigger is used on the convert to binary and the convert to decimal instructions. Convert trigger is on for each cycle that a digit is converted, staying on until shift counter goes to zero.

Put-Away (F75) KX075: This trigger is primarily a sequencing trigger, used on instructions requiring a double put-away. Put-away trigger turns on the cycle preceding E last cycle to do the first of the two put-aways; E last cycle does the second of the two put-aways. The put-away trigger is also used on the branch and index instructions to cause an early put-away (before E last cycle).

E Last Cycle (F76) KS551: Trigger (ELC) is the last cycle sequencer for the E unit. Functions of this trigger include turn off E busy, turn off MODAR. Trigger also allows for the testing of interrupt conditions. ELC trigger is on for 1 cycle.

DX1 (G66) KT001: On RX divide, this trigger turns on for one cycle following the first fixed point sequencer and complements the divisor if the divisor is negative.

Normalize (G67) KT035: Trigger is used during housekeeping portion of various instruction executions to normalize certain operands (reduce the number of leading zeros). For example, on convert to decimal the binary number is normalized before the conversion; on fixed or floating divide the divisor is normalized; on floating multiply the multiplicand is normalized.

D2 (G68) KT001: Sequencer used in the fixed and floating divide instructions to generate the 3/2 multiple and to set the first eight bits of the divisor into the DB-DC register. Trigger follows the normalizing cycles and is on for one cycle.

D3 (G69) KT015: On fixed and floating divide, this trigger turns on for a number of cycles following the D2 cycle to normalize the dividend. On floating divide, if the dividend is all zeros, D3 cycle is skipped.

DL4 (H69) KT015: On floating divide, this trigger follows D3 (or D2 if D3 is skipped) if the dividend is equal to or greater than the divisor. Trigger shifts the dividend right one digit to make the dividend smaller than the divisor.

Iteration Preparation (G70) KT035: Trigger is a sequencer in fixed or floating multiply and fixed or floating divide. Trigger use varies according to the instruction; one primary use is to decode the next multiple to be used in the operation.

Iteration (G71) KT021: Sequencer used in fixed or floating multiply and fixed or floating divide to identify iteration cycles. On divide, iteration cycles develop the quotient by reducing the dividend with divisor multiples. On multiply, iteration cycles develop the product by adding multiplicand multiples.

Multiply Add (H71) KT021: On fixed or floating multiply, this trigger adds the X8 multiple during the 2nd cycle of a 2-cycle iteration sequence.

1st Termination (G72) KT005: On fixed and floating divide, this trigger generates the cycle in which the last quotient bit is developed.

2nd Termination (H72) KT005: On fixed divide, this cycle follows the 1st termination cycle to place the remainder into K and L, and, if necessary, to adjust the remainder (add the X1 divisor to it).

Quotient Transfer (G73) KT031: One-cycle sequencer used on fixed and floating divide to transfer the quotient from the J register to the K register. Cycle follows 1st termination on floating divide, 2nd termination on fixed divide.

Test (G74) KT051: Trigger turns on in fixed or floating multiply or divide to indicate abnormal condition, such as an exponent underflow, a divisor all zeros, or a multiplier or multiplicand all zeros. Main function of the test cycle is to set K register (the result of the operation) to all zeros.

1st Floating Point (H66) KT071: This trigger is the first E unit sequencer for floating point instructions. Trigger turns on at I to E transfer and turns off one cycle later.

Preshift Add (H67) KT011: This floating point sequencer turns on following the 1st FLP cycle or following the preshift cycles to control adding of the fractions. On FP add, subtract, or compare, trigger turns off after one cycle; on FP multiply, trigger turns off when multiplication is complete.

Zero Result (H73) KT031: On fixed and floating divide, this sequencing trigger turns on after the D2 cycle if the J register (dividend) is all zeros. Condition results in setting K register and exponent register to all zeros.

Manual Store (J66) KT047: This light is off the manual J loaded trigger. On a manual store operation, manual J loaded trigger ensures that J register is loaded (from the data keys) before the general or floating point registers are released to receive the data.

Timer J to M (J70) KT075: Trigger turns on during the timer advance interrupt sequence to gate J 0-31 (the timer word) to M 0-31. M 0-31 subsequently has a value of 5 subtracted from it (60-cycle machines) to complete the timer updating. Timer J to M trigger turns on following interrupt cycle 2 and turns off the cycle after J is loaded.

Timer Subtract (J71) KT075: During a timer advance interrupt sequence, the timer subtract trigger turns on following the turn-off of timer J to M trigger to gate both halves of the M register (the timer word and its decrement) through the main adder into the K register. Timer subtract trigger turns itself off after 1 cycle.

Timer Advance (J72) KT081: Timer advance trigger turns on by the timer J to M trigger and J advance. Purpose of timer advance trigger is to turn on interrupt last cycle and IC recovery when BCU accept is received for the store of the updated timer word. BCU accept turns off the timer advance trigger.

Store PSW (J75) KT081: Trigger is used on interrupt sequences to help store the current PSW. Interrupt cycle 3 transfers the right-half of the current PSW to the left-half of K. Store PSW trigger turns on coincident with interrupt cycle 4 to shift the left-half of K into the right-half of K while interrupt cycle 4 transfers the left-half of the PSW into the left-half of K. The PSW is subsequently stored from K via the SBI. Store PSW trigger turns itself off after 1 cycle.

Decimal/VFL Data Flow

Gate K with the T Pointer (E80) KV141: Trigger causes the K register byte selected by the T pointer to be gated through the left byte gate (LBG). Trigger turns on at various times and is on for various durations, depending on the VFL operation.

Gate Digit Buffer-Digit Counter (E81) KV141: Trigger causes digit buffer and digit counter to be gated through the LBG. Turn-on time and duration of this trigger depend on the VFL operation being performed.

Gate L with the S Pointer (E84) KV121: Trigger causes the L register byte selected by the S pointer to be gated through the right byte gate (RBG). Turn-on time and duration are variable, depending on the VFL operation being performed.

Gate K with the S Pointer (E85) KV121: Trigger causes the K register byte selected by the S pointer to be gated through the RBG. Gate K with S pointer trigger is mutually exclusive with the gate L with S pointer trigger. Gate K with S pointer trigger turn-on and duration depend on the VFL operation being performed.

T Out Pointer 4, 2, 1 (F80-82) CV031-051: These lights are off the T register triggers; the count indicates which byte from the K register is to be gated through the LBG.

T In Pointer 4, 2, 1 (G80-82) CV031-051: These lights are off the T register latches; the count indicates the byte position of the K register into which a result byte is to be placed.

S Pointer 4, 2, 1 (F84-86) CV061-081: These lights are off the S register triggers; the count indicates which byte of the L register is to be gated through the RBG.

Y-Length Counter 8, 4, 2, 1 (H79-82) CV151, 161: Y-length counter is set from IOP during E last cycle and indicates the length, in bytes, of operand 1. The Y-length counter value is used (1) in the calculation of operand 1 fetch addresses; and (2) to determine when all bytes of operand 1 have been processed. The Y-length counter steps as each byte is processed, stepping up on some instructions and down on others.

Z-Length Counter 8, 4, 2, 1 (H83-86) CV121, 131: Z-length counter is set from IOP during E last cycle and indicates the length, in bytes, of operand 2. The Z-length counter value is used (1) in the calculation of operand 2 fetch addresses; and (2) to determine when all bytes of operand 2 have been processed. The Z-length counter steps as each byte is processed, stepping up on some instructions and down on others.

Digit Buffer-Digit Counter (J79-86) CV261, 271; CV221, 231: The digit buffer is a 4-position register, used to retain zone bits of the fill-character on edit instructions, and used as temporary storage for the high-order digit of a quotient byte on decimal divide instructions.

The digit counter is used as a 4-position register on edit, edit and mark, pack, unpack, and move with offset instructions, and is used as a counter on decimal multiply and divide.

At times, the digit buffer and the digit counter are combined and used to contain one data byte. When so used, the parity position (J78) indicates odd parity for the entire byte.

Turn-ons and durations of the digit buffer and the digit counter vary according to the VFL operation being performed.

Common Registers

Indicators bounded by the area L to T and 15 to 86 are mostly the common working registers of the CPU.

Only those registers having a unique purpose or whose individual positions have particular significance are described here. All other registers in this area are listed merely for ALD page reference.

Direct Data 0-7 (L52-59) RZ101-121: These lights indicate contents of the direct data register. Register is set during the execution of the write direct instruction and retains the setting until the next write direct instruction is executed. The 8 outputs of the direct data register feed the direct control bus out.

Shift Overflow (L62) KS141: The shift overflow trigger indicates that a significant bit has been lost off the left end of the shifter. This condition can occur on a left-shift instruction, on a divide instruction (dividend normalized too far), and on the convert to binary instruction (decimal number converted to more that 31 binary bits).

When shift overflow trigger turns on, it remains on until the end of E last cycle. If trigger turns on by a shift instruction, the E program interrupt taken is a fixed-point overflow; if trigger turns on by divide or convert to binary, the E program interrupt taken is a fixed-point divide.

Shift Amount (L63-67) AQ091: Each light, L4, L8, R4, R8, or R32 indicates amount of shift applied to data passing through the shifter portion of the main adder. When a light indicates a shift amount, the shifter outputs (instead of the adder sum outputs) are gated to the AM output latches. Each shift amount light is off of a line that is the OR of all the sources of that shift requirement.

Shift Counter (L70-77) RS041-061: These 8 lights, plus parity, indicate contents of the shift counter register. Shift counter register holds binary counts; use includes shift amounts for shift instructions, iteration counts for certain arithmetic instructions, and exponent-equalizing counts for floating point instructions.

Maintenance Control Word (M16-50) PW001: The maintenance control word (MCW) register is set by the diagnose instruction and retains its setting until set again by another diagnose instruction or until reset to all zeros by system reset. When turned on, the individual positions control certain CPU and channel operations; most of the positions force abnormal operations so that the various checking stations can be tested. A feature of MCW control is an automatic logout of CPU indicators a predetermined number of cycles after the diagnose instruction is executed.

The significance of each MCW position is described in Volume II, section "FLT and MCW."

FLT Control Word (M52-86, M40-44, X37-39): ALD locations of parts of the FLT control word are:

Termination bits	PR201
Expected result	PN181
Word control counter	PQ001
Bit control register	PN001, 011
Test register	PN201-241
Advance counter	PW051
Clock pulse select	PR061

An FLT control word is the 17th (last) double word of a Fault Locating Test. The FLT control word register is set from the storage FLT buffer area immediately following the scan-in of a test, and thereafter determines (1) how many cycles the CPU shall run before a comparison is made, (2) the CPU trigger to be compared to the expected result, and (3) the selection of the next test to be run or the termination of the testing.

The FLT control word register may also be set manually from the data keys by pressing the load FLT control word pushbutton; the CPU must be in FLT mode.

Description of the make-up and use of the FLT control word is given in Volume II, section "FLT and MCW."

Program Status Word (T15-86) RE111-841: These lights indicate the various positions of the program status word (PSW). The entire PSW register is set during initial program load, during many of the interrupt sequences, during a forced repeat operation, and by the set PSW and PSW restart pushbuttons. Bits 0-7 can be set independently of the rest of the PSW by the set system mask instruction; bits 36-39 can be set independently by the set program mask instruction. Bits 40-63 can be set manually by the set IC pushbutton.

Portions of the PSW, such as instruction length code, condition code, and instruction counter register, are changed during the course of instruction execution.

The PSW register is not reset by CPU or system reset.

Exponent Register (L78-86) RS011

M Register (N15-86) RM011

L Register (P15-86) RL011

K Register (Q15-86) RL011

J Register (R15-86) RJ011

Register Bus Latch (S15-86) RR011

RBL -4, -3, -2, -1 (S89-92) RR001: These latches are a left extension of the RBL. The four positions

are used on fixed-point and decimal multiply instructions to effect a shift of right 4 of the contents of the J register. J register is gated left 4 to the RBL; then RBL is gated right 8 back to the J register.

Checks

Red lights in this group represent machine errors which (except for manual address check and manual data check) result in a logout and a machine check interrupt. Lights are turned on by the error described; lights are turned off by the check reset pushbutton.

K Reg LH and RH (J89,90) KR051, 061: Lights indicate that a parity error exists in the left or right half of the K register.

AM In (J91) KR031: Light indicates a half-sum parity mismatch in the main adder. Half-sum parity checking of the inputs to the adder shows, when the AM In light is on, that a byte of input data to the adder had bad parity.

AM (J92) KR041: Light indicates that adding circuits themselves made an error, either in the bit function circuits or in the carry lookahead circuits. These checks are more fully explained in the description of the main adder, Volume I, Functional Units.

AV In (J93) AV601: Light indicates half-sum parity error in the decimal adder. Half-sum parity checking effectively checks the correctness of the input data.

AV (J94) AV601: Light indicates that a carry error has occurred in the decimal adder.

AE In (J95) KR301: Light indicates a half-sum parity error in the exponent adder. Half-sum checking effectively checks the parity of the input data.

AE (J96) KR301: Light indicates an error in either the bit function circuits or the carry lookahead circuits of the exponent adder.

Exp Reg (J97) KR311: Light indicates bad parity at the exponent register.

SC (J98) KR311: Light indicates bad parity at the shift counter.

AM Gates (J99) KR431: Light indicates that one or both of the inputs to the main adder failed to be gated in.

J Reg (J100) KT445: J register is checked for parity only on a multiply instruction. Multiplier can be in either the left or the right half of the J register, and as the multiplier is shifted right during the multiply

process, each byte is checked for correct parity. Any byte in the multiplier with bad parity turns on the J Reg light.

LCOP (J101) RN081: Light indicates bad parity in the last cycle operation register.

Rtn Sync (K89) MB617: Light indicates that the two return address banks are not operating in correct synchronism; specifically, WZ trigger is not in step with XY trigger. Under this condition, the validity of subsequent and/or possibly previous storage communication cannot be guaranteed; this applies to both channel and CPU communication with storage.

M-4 CPU Adr (K90) MB625: Light indicates one of the following:
    1. Bad parity at the BCU addressing OR or the storage unit MAR on a CPU store or fetch using an M-4 storage.
    2. Bad parity at the storage unit mark register on a CPU store.
    3. Bad parity at the storage protect unit SPAR on a CPU store or on the instructions set key, insert key, or test and set.
    4. Bad parity at the storage protect unit in key register on a store or fetch or on the set key instruction.
    5. Bad parity at the storage protect unit out key register on any storage operation except the set key instruction.

M-4 X Store Data, Y Store Data (K91, 92) MB623: Lights indicate that CPU data to be stored had incorrect parity detected at an M-4 storage unit MDR. Either light indicates bad store data; the distinction between the X and Y is irrelevant.

CPU-LCS (K95, 96) MB626: These lights, Store Data Chk and Adr Chk, have the same function for a large capacity storage as the previously described CPU Adr and X, Y Store Data lights have for an M-4 storage.

Manual Control Adr Check (L89) PY031: Light turns on if, during a manual operation, an address with bad parity is detected at either the BCU addressing OR or at the storage unit MAR.

Manual Control Data Check (L90) PY031: Light indicates a data parity error, detected at the storage unit MDR, on a display or store main storage operation.

IOP (L96) DA101: Light indicates bad parity on byte 8-15 (R1 and R2) of the I Operation register.

BOP (L97) RB581: Light indicates bad parity on byte 0-7 (operation code of the instruction) of the B Operation register.

Incr (L100) AC541: Light indicates bad parity anywhere in the incrementer, including incrementer extender.

Adr Adder (L101) AA393: Light indicates an addressing adder half-sum parity error or carry lookahead error. The half-sum check is effectively a check on the correctness of inputs to the adder; the carry lookahead checks the internal adding circuits.

Register Gates

Out Gates from M (N89-97) RM831-901: These triggers gate the M register, or various portions of it, to the main adder and to the exponent adder. Each trigger turns on at A time for the cycle in which the gating is necessary and turns itself off the following A time.

M Propagate Sign (N100) RM001: When a complement value is transferred right 1, 2, or 3 from the M register to the main adder, the M propagate sign trigger turns on to insert ones into the high-order adder positions that did not receive inputs from the M register. This insertion maintains the complement 1's in the high-order positions of the number.

Out Gates from L (P89-93) RL801-831: Triggers gate the L register to the main adder. Each trigger turns on at A time for the cycle in which the gating is necessary and turns itself off the following A time.

Excess 6 Decoder (P95, 96) RL851, 861: On the convert to decimal instruction, these triggers gate the specified portion of the L register to the main adder for decimal correction. Each trigger turns on at A time for the cycle in which the correction is required and turns itself off the following A time.

Out Gates from K (Q89-91) RK809-831: Triggers gate the K register to the main adder. Each trigger turns on at A time for the cycle in which the gating is necessary and turns itself off the following A time.

Force Parity (Q93, 94) KS531, RJ843: Triggers cause parity bits to be forced into either side of the main adder whenever the opposite side of the adder has the only data input. Each trigger turns on at early B time for the cycle in question and turns itself off at the next early B time.

Floating-Point to AE T/C (Q97) KX081: For RR floating point add, subtract, and compare instructions, trigger turns on with the first floating point

sequencer to gate the exponent of R1 into the exponent adder; this transfer is a part of the comparison process to determine if the characteristics require equalization. The floating point to AE T/C trigger turns off after 1 cycle.

K0 Duplicate (Q100) RK001: When a complement value is transferred right 4 from the K register to the main adder, the K0 duplicate trigger turns on to insert ones into adder positions 0-3. This insertion maintains the complement 1's in the high-order positions of the number.

Out Gates from J (R89-95) RJ821-842: Triggers gate the J register, or portions of it, to the main adder or the exponent adder. Each trigger turns on at A time for the cycle in which the gating is necessary and turns itself off the following A time.

J Parity 60-63 (R100) KT445: Trigger remembers the odd-even count (odd, on; even, off) of the low-order half of a multiplier byte from the J register. The count is subsequently considered along with the odd-even count of the high-order half of the multiplier byte to determine total bit count for a parity check on the whole byte.

Channel Status

Operational In (S95-101) ZR010: Each light indicates that the corresponding channel is currently at work with one of its I/O devices. An operational in light indicates that the channel corresponding to the light has its operational in line up from one of its attached I/O units.

Log on Stop (T95-101) ZR010: Each light indicates that the corresponding channel's log-on-machine-check switch is down (the normal position) and the channel's auto-test switch is in the auto position.

If the channel's log-on-machine-check switch is down, a channel machine check or data check causes a channel logout; if the switch is up, checks cause the channel to stop without a logout.

Automatic (U95-101) ZR010: Each light indicates that the corresponding channel is in automatic mode (not test mode): the auto-test switch on the channel's CE panel is in the auto position and the channel enable-meter switch is on.

Manual Controls

Load 1, 2 (W45, 46) PY071: Load 1 light indicates that an IPL is being initiated from operator's console. Load 2 light indicates that an IPL is being initiated from system control panel. Lights turn on when their corresponding load pushbuttons are

pressed; lights remain on until the release buffer trigger turns on (the read-in portion of the IPL is completed).

D1, D2, D3 (W49-51) PW161-181: These triggers are used on MCW and FLT operations. On an MCW operation, the three triggers monitor the outputs of the MCW counter (M40-50) to stop the clock and cause a logout whenever the count reaches zero. Trigger D1 monitors for an initial count of zero, trigger D2 monitors for an initial count of 1, trigger D3 monitors for a count of 1, reduced from some higher count. Purpose of all three triggers on MCW control is to turn on the MCW pseudo check trigger at the proper time, thereby causing a simulated machine check which stops the control clock and initiates the logout.

On FLT, the three triggers monitor the outputs of the advance counter field (M40-44), which was set as part of the FLT control word. Purpose of the triggers on FLT is to turn on the MCW pseudo check trigger whenever the advance portion of an FLT is completed, thereby stopping the control clock and starting the compare portion of the test.

Set IC (X46) PY051: Trigger turns on when the set IC pushbutton is pressed; trigger controls the various actions that set contents of the data keys into the IC portion of the PSW. These actions include sending several signals to the BCU to cause a panel key fetch to the J register, gating J 40-63 to the IC as soon as J is loaded, and initiating an IC recovery. Set IC trigger turns off by J loaded and a C clock.

MCW Pseudo (X47) PW191: This light is off the MCW pseudo check trigger. Trigger is used to simulate a machine check on MCW and FLT operations so that the control clock will be stopped and a logout taken at the end of an MCW advance, or so that the control clock will be stopped and the compare cycle entered at the end of an FLT advance. See description of D1, D2, and D3 indicators for turn-on of the pseudo check trigger. Trigger turns off by the compare cycle trigger on FLT or by the diagnose select signal on an MCW operation.

Display (X48) PY041: Trigger turns on when the display pushbutton is pressed. For display storage, trigger AND's with BCU response to send a return-address-to-J signal to the BCU and to gate the address keys to the ChSAB. For display general or floating point registers, the display trigger gates the register select keys to select the specified register and gates that register to the RBL.

Display trigger turns off (1) by J loaded and a C clock on display storage; or (2) as the halt trigger turns off on display registers.

Clock, Running and Controlled (X50, 51) KC061: These lights are off the running and controlled clock triggers, respectively, and indicate that their corresponding clock pulses are being emitted to the CPU circuits.

Power and Marginal Checking

Main Power On: Indicator is on when primary power from customer's wall receptacle is available to the CPU, and the 24-volt DC control voltage supplied by the CPU is operative.

Unit Power On Lights: These ten lights are on whenever DC voltage is up in their corresponding frames.

Power Check Lights: These ten lights turn on whenever a power failure such as overcurrent, overvoltage, tripped CB, or thermal failure occurs in their corresponding frames.

Margined Lights: Each of the three lights immediately above the raise-lower switch indicates that the +6M voltage at the designated frame (CPW/CPF/MCF, channel, storage) is margined from normal level.

Home Light: Light turns on when the frame selected by the +6M rotary switch has its +6M voltage at the normal setting.

Status Lights

System: Light is on if CPU is running (not waiting) or if any I/O unit is operating.

Manual: Light turns on when CPU goes into stopped status (the halt trigger on). In stopped status, no instructions are processed nor are any interrupts taken. Instead, the manual circuits, such as store or display, are readied for use; hence the term manual for this light.

The stopped status can be entered by: (1) pressing the stop pushbutton or the CPU or system reset pushbuttons, (2) an address compare stop condition, or (3) after each instruction is processed on an instruction-step or a multiple-step operation. There is no provision for programming the machine to stop.

Wait: Light turns on when CPU goes into the wait status, which is whenever PSW position 14 contains a one. No instructions are processed in the wait status; however, external and channel interrupts are taken and the timer is updated.

Test: Light turns on if:
1. The maintenance control word has a bit in any

of the positions 3-15.

2. Any switch on the system control panel or on any separate maintenance panel for CPU, storage, or channels is set to a position that affects the operation of the customer program.

3. A circuit breaker trips or a thermal condition occurs.

Load: Light turns on when the load pushbutton is pressed and remains on during the IPL operation. Light turns off when the new PSW is loaded. If the IPL operation is not completed, light stays on and CPU hangs up.

CIRCUITS

Common Circuits

Pushbutton

Each pushbutton, when pressed, emits a 370-ns pulse that initiates the manual operation associated with that pushbutton. One pulse-forming network, consisting of a latch and a singleshot, supplies the 370-ns pulse for all of the pushbuttons (Figure 5750).

Pressing a pushbutton opens its normally-closed contact; this action conditions the AND circuit that gates the singleshot pulse to the proper circuits for that pushbutton, and, at the same time, conditions the latch for turn-on. As the pushbutton is pressed down, the normally-open contact closes, causing the latch to turn on. The singleshot fires when the latch turns on, sending out the 370-ns pulse.

Once the latch turns on, it holds itself on until the pushbutton restores and closes its normally-closed contact; the singleshot, therefore, fires only once for a given pushbutton depression, and the button must be released before another pushbutton can activate the singleshot.

Integrator circuits are used off the pushbutton contacts to soften the sharp change in voltage level on the pushbutton lines when the pushbutton contacts make and break, thereby reducing noise pickup by adjacent cable wires.

Indicator Logic

The console indicators are incandescent lamps lit by current supplied by indicator drivers (Figure 5751). Indicator drivers are located throughout the system and usually operate off the trigger to be indicated. As shown in Figure 5751, the driver current, through the lamp, returns to +5.1 volts to turn on the lamp. When the driver is not active, the lamp draws a lesser amount of current through the 1.2K resistor, not enough to turn on the lamp but enough to keep the filament warm. This preheating prolongs the filament life.

The indicator drivers also are the source for logout data. The driver outputs (1216 of them) feed the word switch matrix; the matrix selects 19 groups of 64 driver outputs, each group to be stored away during the logout.

Pressing the lamp test pushbutton on the system control panel energizes the lamp test relay. Points on the relay cause 3 volts to be applied across each lamp, turning all lamps on for a visual check.

Manual Circuits

Manual Interrupt

Figure 5752 shows that when the interrupt pushbutton is pressed, the console interrupt trigger turns on. Latched output of the trigger goes to the interrupt controls resulting in an external interrupt. (The sequence for external interrupts is covered in detail in Volume II, Interrupts.)

Note: Once the console interrupt trigger turns on, it can turn off only by CPU reset or an external interrupt; therefore, once the pushbutton is pressed, the console interrupt request stays pending (even though the CPU is stopped) and will be taken eventually.

Initial Program Load

CPU circuits for the IPL operation are given in detail in Volume II, Interrupts.

Start, Stop, and Clock Controls

Figures 5753 and 5754 show the generation of clock pulses including the controls involved on single-cycle, instruction-step, and multiple-step.

The timed pulses that are distributed throughout the CPU originate at a 10-megacycle oscillator. The oscillator output is halved by a frequency divider, creating 50-nanosecond pulses that occur every 200 nanoseconds; these pulses are the basic machine pulses.

The basic machine pulses are then gated by the two clock triggers, running and control. Running pulses are stopped only by a system reset; controlled pulses are stopped by either CPU or system reset, by a machine check, or when the CPU is put in the single-cycle mode. The basic running and controlled pulses both generate their own A, B, early B, late B, L, and C pulses.

Manual stopping and starting of the CPU does not involve the clocks. Pressing the stop pushbutton merely turns on the halt trigger, blocking T1; the I unit cannot process instructions further with T1 blocked. The start pushbutton turns off the halt trigger via singleshots 6 and 7, releasing the I unit to continue processing instructions.

If the rate rotary switch is turned to single-cycle, SS 4 stops the control clock. Thereafter, each depression of the start pushbutton turns on the start clock sync trigger via singleshots 6 and 8 and, subsequently, the control clock trigger. The same oscillator pulse that turns on the control clock trigger is allowed to pass through the gating AND circuit.

Meanwhile, the start clock sync trigger has turned on the stop control clock sync trigger; the next oscillator pulse coming along turns off the control clock trigger, blocking this and further oscillator pulses from getting through the gating AND. Only one machine cycle, therefore, is allowed to occur by the depression of the start pushbutton.

With the rate rotary switch on instruction-step, pressing the start pushbutton turns off the halt trigger via singleshots 6 and 7. The clocks keep running. The halt trigger off releases T1, allowing the I unit to start processing the next instruction, but the very fact that T1 came on turns the halt trigger back on, blocking T1 from coming on again. One instruction, therefore, is processed by a depression of the start pushbutton. The block of T1 is the controlling factor on instruction-step; the E unit is not controlled. The E unit merely executes whatever is transferred to it at I to E transfer time.

With the rate rotary switch on multiple-step, pressing the start pushbutton causes one instruction to be processed, just as in instruction-step. The multiple-step position of the rate rotary, however, conditions SS 5 to fire whenever SS 6 times out, and if the start pushbutton is held down, SS 6 fires whenever SS 5 times out. Singleshots 5 and 6, therefore, fire each other in tandem with SS 6 firing every 230 milliseconds. Because SS 6, through SS 7, turns off the halt trigger, T1 is released to process a single instruction every 230 milliseconds.

A machine check stops controlled pulse distribution to the CPU by turning off the control clock trigger. The various parity-checking stations throughout the CPU are tested at different pulse times; that is, some are tested at A time, some at L, some at B, and so on. Regardless when in the machine cycle the parity check occurs, the control trigger cannot go off until the next oscillator time, which is too late to block the previous oscillator pulse from getting through the control clock gating AND. All of this means that on a machine check, one more set of pulses operates on the CPU before the control clock actually stops.

Set IC

On regular instruction processing that calls for a storage fetch, a bit on the BCU addressing OR position 0 is detected as an invalid address by the BCU, resulting in a panel key fetch operation instead of the normal storage fetch. The panel key fetch operation sends the contents of the data keys to the normal destination.

The set IC procedure simulates an invalid address condition to the BCU, causing a panel key fetch, and then provides for gating positions 40-63 of J into the PSW register.

Figure 5755 shows the logic and the data flow of the set IC operation. The CPU must be in stopped status (the halt trigger on) before the set IC pushbutton is effective.

Pressing the pushbutton turns on the storage request trigger and the set IC trigger. The storage request trigger makes a storage request of the BCU, and when storage is obtained (signalled by BCU response), the set IC trigger on causes a bit to be forced onto position 0 of the ChSAB. The channel address 0 line to the BCU causes the storage cycle just requested to be cancelled - storage times out but no actual fetch is made - and causes instead the panel key fetch line to become active. The panel key fetch line gates the contents of the data keys, which are at the output of the word switch matrix, into the SBO latches.

When BCU response sends the channel address 0 to the BCU, it also raises the line "return to J maintenance channel." This line causes the BCU, at advance time of the storage cycle, to generate the J advance signal, which gates the output of the SBO latches into the J register.

When J is loaded, the J loaded trigger turns on. The triggers set IC and J loaded set positions 40-63 of the J register into the corresponding positions of the PSW register. Set IC and J loaded also unblock the I unit and start an IC recovery.

The simulated invalid address to the BCU helps the set IC operation to come about, but the BCU must not actually detect it as an invalid address condition. To accomplish this, a line "enable PK address" is made active by the set IC trigger; this line blocks the BCU invalid address detection circuits.

Set PSW

The set PSW operation is similar to the set IC operation. Pressing the set PSW pushbutton turns on the storage request trigger, the set IC trigger, and the set PSW trigger (Figure 5756). The data key contents are placed into the J register by a panel key fetch, and J 40-63 is set into PSW 40-63, the same as in set IC. In addition, the set PSW trigger on gates J 0-39 into PSW 0-39. The end result is that the 64 data keys are set into the entire PSW register. As in the set IC operation, J loaded unblocks the I unit and starts an IC recovery.

Load A and B Registers

Figure 5757 shows the logic and data flow for the load A-B operation. The CPU must be in the stopped status before the load A-B pushbutton is effective. Pressing the pushbutton turns on the storage request and load A-B triggers. The storage request trigger makes a request of BCU, and the load A-B trigger forces a bit onto ChSAB position 0 when BCU response is returned.

As with set IC and set PSW, the forced channel address 0 causes a panel key fetch operation in which the data keys, instead of the usual storage data, are fetched to the normal destination, in this case the A and B registers.

The enable PK address line sent to the BCU blocks the BCU's invalid address detection circuits.

Display Storage

Figure 5758 shows the logic and the data flow for display storage. The CPU must be in the stopped status (halt trigger on).

The storage select switch is set to the middle position (main storage) and the address keys are set to the storage location to be displayed. Pressing the display pushbutton turns on the storage request trigger and the display trigger. The storage request trigger makes a request of BCU, and the display trigger (when BCU response is received) instructs the BCU to return the storage data to the J register. BCU response and the display trigger also gate the address keys to the ChSAB.

Storage runs through its cycle; at advance time, the BCU generates J advance to gate the SBO into the J register.

Display General Register

Figure 5759 shows the logic and data flow for displaying a general register. The CPU must be in the stopped status (halt trigger on). The storage select switch is set to the up position (general registers) and the four register select keys are set to a binary count corresponding to the number of the general register to be displayed.

Pressing the display pushbutton turns on the display trigger, which does all the gating necessary to display the register in the left half of the RBL. The binary count of the four register select keys is decoded into one of 16 select lines. The one active select line gates the register in question to the GBL, which in turn is gated on to the RBL.

Once a general register is displayed, any other general register may be displayed merely by changing the set-up of the register select keys. The display pushbutton need not be pressed again.

Display Floating Point Register

Figure 5760 shows the logic and data flow for displaying a floating point register. CPU must be in stopped status. The storage select switch is set to the down position (floating-point registers), and the two middle register select keys are set to a binary count corresponding to the number of the register to be displayed (0, 2, 4, or 6); these counts correspond to register numbers 0, 1, 2, and 3.

Pressing the display pushbutton turns on the display trigger, which does all the gating necessary to display the floating point register in the full RBL. The two inputs into the BOP decoder are decoded into one of four select lines, the active select line gating the proper register.

As with general registers, once a floating point register is displayed, the others may be displayed merely by changing the set-up of the register select keys.

Store Into Main Storage

Figure 5761 shows the logic and data flow for storing into main storage. The store pushbutton is active only when the CPU is in stopped status (halt trigger on). The storage select switch is set to the middle position (main storage), the location to be stored into is set into the address keys, and the data to be stored is set into the data keys.

Pressing the store pushbutton turns on the storage request trigger and the store trigger. The storage request trigger makes a request of BCU. When BCU response is received, the store trigger gates the address keys to the ChSAB and brings up the store line to the BCU. The store line causes the storage cycle just started to become a store operation instead of a fetch. Shortly after BCU response occurs, the BCU generates data request, which gates the output of the word switch matrix (the data key contents) to the Channel SBI. The storage cycle times out, storing what is on the SBI.

Store Into General Register

Figure 5762 shows the logic and data flow for storing into a general register. The store pushbutton is effective only if the CPU is stopped (halt trigger on). The storage select switch is set to the up position (general registers), the four register select keys are set to a binary count that corresponds to the number of the general register to be stored into, and the data to be stored is set into position 0-31 of the data keys.

Pressing the store pushbutton turns on the storage request trigger and the store trigger. The storage request trigger makes a request of the BCU.

When BCU response is received, the store trigger forces a bit onto the 0 position of the ChSAB and instructs the BCU to return the data to the J register. Because of the ChSAB 0-bit, however, the storage is cancelled (storage still times out) and a panel key fetch operation takes place. The PK fetch sends the contents of the data keys to the normal destination, which in this case is the J register. The J loaded trigger turns on (not shown in the figure).

The store trigger gates J to the main adder; the adder here is used only as a flush path. The store trigger and J loaded trigger gate the adder output to the K register. The four register select key lines are decoded into 1 of 16 general register select lines; the active register select line gates 0-31 of K into the proper general register.

The enable PK address line to the BCU prevents the BCU from detecting the 0-bit on ChSAB as an invalid address.

Store Into Floating Point Register

Figure 5763 shows the logic and data flow for storing into a floating point register. The storage select switch is set to the down position (floating-point registers), the two middle register select keys are set to a binary count corresponding to the number of the floating point register to be stored into (counts 0, 2, 4, 6 correspond to registers 0, 1, 2, 3), and the data to be stored is set into the 64 data keys.

Pressing the store pushbutton causes the same sequence of events to occur as in store to general register, down to the point of setting the J register. As the J register contents go to the main adder, J 0-7 contents go to the exponent adder. The main adder shifts J 8-63 left 8 and sets it into K 0-55. The two register select key lines are decoded into 1 of 4 select floating point register lines; the active line gates K 0-55 (the floating-point fraction) into 0-55 of the proper floating point register and at the same time gates the exponent from the exponent adder into 56-63 of the floating-point register.

As in all manual operations that use a forced 0-bit on the ChSAB, the BCU does not recognize the 0-bit address as invalid because of the enable PK address line sent to the BCU.

Error Circuits

Machine errors are hardware malfunctions, and, under normal processing, result in a logout of CPU followed by a machine check interrupt.

This section describes the error-detection circuits that monitor the various data and addressing paths in the CPU; the final outputs from all of these checking circuits are OR'ed to turn on a check latch, which in turn stops the control clock and initiates the logout operation.

BCU Stop Clock

Figure 3500 shows conditions causing the BCU to generate a machine-check signal. For the signal to be generated, CPU (not channel) must be communicating with storage. The BCU generates the check signal for three error conditions:
  1. Address parity check detected at the BCU addressing OR, at storage, or at an SPF.
  2. Data parity check detected by storage on a store operation.
  3. The X/Y and W/Z triggers out of synchronization.
During a CPU-storage operation, an address parity check turns on the CPU address check trigger, which turns on the stop clock trigger. During a channel-storage operation, an address parity check sends an address-check signal to the channel; the channel in turn requests an I/O interrupt.

Storage tests the MDR for proper parity on both stores and fetches and sends a data-check signal to the BCU if an error occurs. The BCU ignores a storage data check on CPU fetch operations, but sets either the data check X CPU trigger or the data check Y CPU trigger if the error occurs on a CPU store. The line "not X (or Y) return to A, B, J, or diagnose" indicates that the operation is a store. Which trigger turns on, whether X store data or Y store data, is not pertinent; either trigger does no more than indicate that the MDR was bad on a store from CPU. Either trigger turns on the stop clock trigger.

The XY trigger and the WZ trigger are compared for the proper relationship to one another whenever both the odd and even storages are not busy. If the two triggers are not in synchronism, the XY-WZ check trigger turns on, which in turn sets the stop clock trigger.

K Register Check

K register is checked for parity at every B clock, except during those cycles that the K register normally may be invalid as far as parity is concerned (Figure 3501). The left half and the right half are checked separately, each half setting its own trigger and indicator.

Main Adder

Figure 3502 shows the circuits involved in checking for main adder errors. The AM In light indicates bad input to the adder; the AM light indicates an internal error either in the generation of the bit functions or in the generation of carry lookahead.

These checks are illustrated in detail in Volume I, Functional Units.

The enabling of the half-sum checks (Am In) is such that the half-sum parities are checked only after the adder starts operating on valid data. For example, at the beginning of an instruction execution, several machine cycles may occur before the data is returned from storage and set into the J register, ready for the adder. During these cycles, the adder half-sum checking is disabled.

On certain operations, such as multiply or divide, the adder input is shifted off byte boundaries. The input parities on individual bytes in this instance may be incorrect (normal), but the number of bytes with incorrect parity should be even. On these operations, the straight half-sum checking is blocked and the checking circuit looks for an odd number of byte errors.

Decimal Adder

Figure 3503 shows the two decimal adder checks, AV In and AV. Decimal adder checking is very similar to main adder checking; see description of the main adder, Volume I, Functional Units, for a detailed description of adder checking. The AV In light indicates bad input to the adder, and the AV light indicates an internal adder error. Either error constitutes a machine check.

Decimal adder checking is enabled by the VFL circuits such that the adder is checked only when it is operating on valid data.

Exponent Adder, Exponent Register, Shift Counter

Figure 3504 shows the circuits involved in the checking of these three components. Exponent adder is checked similarly to the main adder (see main adder description, Volume I, Functional Units, for details of adder checking). The exponent register and the shift counter both are reset to zeros with correct parity on a CPU reset. Thereafter, these two registers are checked for correct parity on every B clock.

Gating Trigger Check

On no machine cycle should data be gated into only one side of the main adder. Figure 3505 shows the circuit that tests to make sure that both sides of the adder have a gating trigger set whenever the adder output is to be used. One side gated without the other or both sides not gated results in an AM gate check (machine check).

J Register, LCOP Register

The J register is checked for proper parity only on multiply instructions (Figure 3506). On multiply,

the J register contains the multiplier. Each byte of the multiplier is checked for correct parity, the checking of each byte being done in two stages: First, the low-order half of a multiplier byte plus the byte parity bit are tested for a total odd-even count, and the J parity trigger is set if the count is odd. Second, the high-order half of the byte plus the J parity trigger setting are tested for a total odd-even count, and the J parity error trigger is set if this count is even.

The shift counter odd or even determines which half of the byte is tested. Because the shift counter is even initially, and the low-order halves of the bytes are tested on SC odd, the SC odd gate is forced at the very beginning of the checking. Thereafter, the actual odd-even contents of the shift counter gate the proper half of the byte for checking at the proper time.

The LCOP register is checked for correct parity every cycle that the LCOP register contains valid data. The first cycle memorize trigger prevents the checking until the LCOP data is valid.

IOP Check

Figure 3507 shows the checking of the IOP register. Note that only byte 8-15 is checked; this field is R1-R2, R1-X2, R1-R3, or L1-L2, depending on the instruction format. The register is tested at the turn-on of T2 except when T2 is for the object instruction of an execute. At this particular time, bits 8-15 of the IOP register are gated into from two sources simultaneously and the parity of the field will not be correct.

BOP Check

Byte 0-7 of the BOP register is tested for proper parity at I to E transfer time (Figure 3508). Byte 0-7 is the operation code of the instruction.

Incrementer

Figure 3509 shows the logic for checking the parity of the incrementer. Positions 0-23 are tested whenever the incrementer is gated to H, K, SAR, or the ICR. The entire incrementer plus the extender is tested two times on the load PSW instruction to test the correctness of the whole PSW register after the load; the incrementer plus extender is tested on interrupt cycles 5 and 6 to check the entire PSW register after setting in the new PSW on an interrupt.

Addressing Adder

Figure 3510 shows the checking circuit for the addressing adder. The adder is checked for half-sum

parity errors and carry errors, much the same as the main adder. Detection of an error is allowed whenever the adder output is being used, such as when the adder is gated out to the H register or SAR.

Checking OR to Machine Check

Figure 3511 shows how all of the errors described in this section are OR'ed to turn on the check latch. The check latch turns off the control clock and generates the log-on-check signal. This signal starts the logout procedure, which stores the status of the CPU triggers into storage. The completion of the logout resets the CPU and starts a machine check interrupt.

Machine errors are prevented from causing a machine check by:
1. All manual operations.
2. The CPU in FLT mode.
3. The CPU check switch set to disable.
4. No bit in PSW position 13.

OPERATING INSTRUCTIONS

Initially Load Storage from I/O

1. Set up the input unit (load the tape, etc.).
2. Set the rotary switches to the channel and unit addresses.
3. Press the load pushbutton.
Note: Input unit reads into storage. PSW register is loaded from storage location 0. CPU does an IC recovery. Processing starts automatically.

Stop the CPU

Press the stop pushbutton. (CPU stops after the instruction in process at the time is executed and after outstanding interrupts are taken.)

Start the CPU

Press the start pushbutton. (CPU continues from where it left off.)

Load a Storage Location

1. Set storage select switch to "main storage."
2. Set storage address into address keys.
3. Set data to be loaded into data keys 0-63.
4. Press the store pushbutton.

Load a General Register

1. Set storage select switch to "GP regs."
2. Set register address into register select switches (binary count 0-15).

3. Set data to be loaded into data keys 0-31.
4. Press the store pushbutton.

Load a Floating Point Register

1. Set storage select switch to "FLP regs."
2. Set register address into two middle register select switches (binary count 0, 2, 4, 6).
3. Set data to be loaded into data keys 0-63.
4. Press the store pushbutton.

Display a Storage Location

1. Set storage select switch to "main storage."
2. Set address keys with storage address to be displayed.
3. Press the display pushbutton.
4. Observe J register indicators.

Display a General Register

1. Set storage select switch to "GP regs."
2. Set register select switches to register to be displayed (binary count 0-15).
3. Press the display pushbutton.
4. Observe RBL 0-31 indicators.

Display a Floating Point Register

1. Set storage select switch to "FLP regs."
2. Set the two middle register select switches to register to be displayed (binary count 0, 2, 4, 6).
3. Press the display pushbutton.
4. Observe RBL 0-63 indicators.

Load the A-B Registers

1. Set data to be loaded into data keys 0-63.
2. Press the load A-B regs pushbutton.
Note: The same data sets into both A and B.

Load the PSW Register

1. Set data to be loaded into data keys 0-63.
2. Press the set PSW pushbutton.
Note: CPU does an IC recovery, which fetches the instructions located by the new IC to the instruction buffers A and B. Processing starts with these instructions when the start pushbutton is pressed.

Load the Instruction Counter Register

1. Set address to be loaded into data keys 40-63.
2. Press the set IC pushbutton.
Note: CPU does an IC recovery, which fetches the instructions located by the new IC to the instruction buffers A and B. Processing starts with these instructions when the start pushbutton is pressed.

Restart from Initial PSW

1. Press the PSW restart pushbutton.

Note: The PSW register is loaded from storage location 0. CPU does an IC recovery. Processing starts automatically.

Step Through a Program One CPU Cycle at a Time

1. Set the rate switch to single-cycle.
2. Press the start pushbutton for each cycle.

Step Through a Program One Instruction at a Time

1. Set the rate switch to "instruction-step" or "multiple-step."
2. Press and release the start pushbutton to execute a single instruction. Hold down the start pushbutton to step through instructions (approximately 4 per second).

Repetitively Execute the Same Instruction

1. Load the instruction into the A-B registers.
2. Turn on the repeat instruction switch (down).
3. Press the start pushbutton.

Repetitively Execute a Group of Instructions

1. Set data keys with a controlling PSW (starting instruction address and any other desired controls).
2. Set address keys with address of instruction that is at, or near, the end of the group. (The repeat will occur 100 microseconds after this instruction is reached.)
3. Set the forced repeat select switch to "address compare."
4. Set the forced repeat reset switch to computer.
5. Press the computer reset key.

Stop at a Predetermined Address

1. Set the stop address into the address keys.
2. Turn on the address compare stop switch (X84).

Note: The CPU stops when an address sent to BCU equals the address in the keys.

Clear Memory

1. Load GR 0 with zeros.
2. Set the data keys with a multiple-store instruction (Op code 90, R2 other than 0, all other positions zero).
3. Press the load A-B regs pushbutton.
4. Turn on the enable storage ripple switch.

5. Press start.

Note: Successive storage locations are stored with zeros. Storage wraps around and keeps running until computer or system reset is pressed. The storage ripple switch blocks invalid address detection.

CHECK HANDLING DURING MANUAL OPERATIONS

● Address or data check only turns on indicator (L-89, 90)

● Machine-check condition not detected until processing starts

During manual operations, certain checks can occur; Figure 11 shows which checks on the various operations can occur.

Address check may come from a parity check at the BCU addressing OR, or from a parity check of the address in the storage unit. On all operations (except display general or floating point registers) storage is selected and a parity check of the BCU addressing OR is made, even though on load A-B, set IC or PSW, and store general or floating point registers no address is sent to the BCU from the address switches. On these operations the storage cycle is subsequently cancelled, but because it was selected, the BCU makes the address parity check. On store or display main storage, the address is checked in the storage unit as well as in the BCU.

If bad parity is found, BCU sends an address check signal to the manual controls which results only in turning on the address check indicator on the system control panel (L89).

A data check can occur only on store or display main storage because these two operations are the only ones using storage. The data check is a parity check of the memory data register (MDR) in the storage unit. The MDR is checked on both stores and fetches and if bad parity is found, a data check signal is sent to the BCU which forwards it on to the manual controls. There it results only in turning on the data check indicator on the system control panel (L90).

A machine check can occur only on the operations specified in Figure 11. Load A-B operation might load the A or B register with a bad byte (bad parity), but if this happened, it would not be known until the CPU was started again and the I unit tried to use the bad byte. Then a machine check would occur, resulting in a logout and a machine check interrupt.

If on the set IC or set PSW operation the IC is loaded with data having bad parity, the bad parity is detected at the incrementer during the IC recovery that automatically follows the loading of the IC. This detection turns on the incrementer check (L100) but

does not immediately cause a machine check. Machine check is not immediate because on set IC and set PSW, a special trigger called manual operation disable check is turned on, and held on, throughout the manual operation, including the IC recovery. This disabling-check trigger prevents a machine check from occurring even though a condition for machine check is detected. The check condition is held, however, and will cause a machine check once the CPU is started again.

A machine check condition can also occur on store to general or floating point registers. If the store data from the data keys picks up bad parity, the bad parity is detected at some register in the data path, for example, in the main adder as bad main adder input. (The adder is in the data path for storing to registers.) The machine check condition is indicated on the system control panel (AM In, J91), but the actual machine check does not occur until the CPU is started again. The reason is the same as for set IC or set PSW: the manual operation disable check

trigger inhibits the machine check during the manual operation but does not inhibit the setting of the particular check trigger, in this case, AM In.

On store to main storage, an invalid address (one that is outside available storage) might be sent to the BCU from the address switches. This causes storage to be cancelled (with no actual storing), but no indication of such a condition is given.

An invalid address might also be sent to the BCU on display main storage. This also results in a cancellation of storage, but since the storage request is for a fetch, the data keys are set into the J register (panel key fetch of invalid address and the J invalid indicator turns on (return to J, A3 or B3; invalid, A5 or B5).

Note: If a manual store is made followed by a display of the same location, and the location is an invalid one, the J register will appear as though the store and the display were all right. In reality, neither the store nor the display takes place; the J register merely gets what was set up in the data keys.

MANUAL OPERATIONS	ADDRESS CHECK	DATA CHECK	MACHINE CHECK	INVALID ADDRESS
LOAD A and B	Turns on Address Check trigger in manual controls. Lights Address Chk indicator (L89)	Not Applicable	Detected when data is used. Normal machine check sequence.	Not Applicable
Set IC or PSW	"	"	Incrementer Check set during IC recovery. Mach Chk interrupt occurs when start is pressed.	"
Store into Main Storage	"	Turns on Data Chk trigger in manual controls. Lights Data Chk indicator (L90)	Not Applicable	Store cancelled. No indication given.
Display Main Storage	"	"	"	Sets J Reg from Data Keys. Turns on J Invalid. J Inv reset next time · J is loaded. No interrupt.
Store Gen or FP Registers	"	Not Applicable	Check trigger for register in data path is set. Mach Chk interrupt occurs when start is pressed.	Not Applicable
Display Gen or FP Regs	Not Applicable	Not Applicable	Not Applicable	Not Applicable

FIGURE 11. CHECKS DURING MANUAL OPERATIONS

COMMENT SHEET

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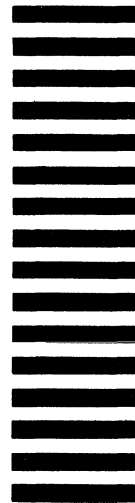FOLD ON TWO LINES (LOCATED ON REVERSE SIDE), STAPLE AND MAIL

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