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ADDED STANDARD INSTRUCTIONS FOR MODEL 44

Replace pages 9 through 12 in IBM System/360 Model 44 Functional Characteristics, Form A22-6875-3 with the corresponding pages attached to this Newsletter. Pages 9 and 11 are unchanged.

Text changes are indicated by a vertical line to the left of the text affected; figure changes are indicated by a bullet (•) to the left of the figure title.

File this sheet at the back of the publication. It provides a reference to changes, a method of determining that all changes have been received, and a check that the publication contains the proper pages.

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that suppression is impossible, the operation is terminated when the protection exception is recognized. When a fetch violation is caused by an instruction in the CPU program, the operation is likewise terminated.

When a protection mismatch is detected during an I/O operation, the operation is terminated: a protection check causes an I/O interruption, data transmission stops, and the mismatch is indicated in the CSW which is stored as a result of the channel operation.

In any case, the protected location remains unchanged.

Programming Notes

Store protection is always active, and when the fetch protection bit is a one, fetch protection is always active. Protection is independent of the problem, supervisor, or masked state of the CPU and of the type of instruction or I/O command being executed. All main-storage locations specified in the program are protected. Data stored in a protected location cannot be moved into an addressable register or to another storage location unless the proper key is supplied.

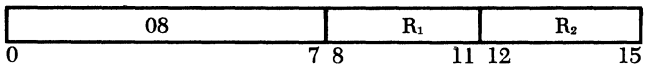
When the protection feature is not installed, the protection key in the PSW and the protection key of the channels must be zero; otherwise, a program interruption or program-check I/O termination results.

Instructions Added for Protection Feature

The key in storage can be changed by the SET STORAGE KEY instruction and inspected by the INSERT STORAGE KEY instruction; these two instructions are added to the Model 44 instruction set only when the protection feature is installed. The instruction timings are included in Figure 4.

Set Storage Key

SSK ***R_1, R_2*** ***(RR)***



The key of the storage block addressed by the register designated by R_2 is set according to the key in the register designated by R_1.

The storage block of 2,048 bytes, located on a multiple of the block length, is addressed by bits 8-20 of the register designated by the R_2 field. Bits 0-7 and 21-27 of this register are ignored. Bits 28-31 of the register must be zero; otherwise, a specification exception causes a program interruption.

The five-bit key is obtained from bits 24-28 of the register designated by the R_1 field. Bits 0-23 and 29-31 of this register are ignored.

Condition Code: The code remains unchanged.

Program Interruptions

Operation (if the protection feature is not installed)

Privileged operation

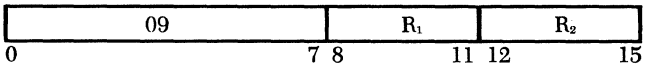
Addressing

Protection

Specification

Insert Storage Key

ISK ***R_1, R_2*** ***(RR)***



The key of the storage block addressed by the register designated by R_2 is inserted in the register designated by R_1.

The storage block of 2,048 bytes, located on a multiple of the block length, is addressed by bits 8-20 of the register designated by the R_2 field. Bits 0-7 and 21-27 of this register are ignored. Bits 28-31 of the register must be zero; otherwise, a specification exception causes a program interruption.

The five-bit key is inserted (for inspection) in bits 24-28 of the register specified by the R_1 field. Bits 0-23 of this register remain unchanged, and bits 29-31 are set to zero.

Bit 28 of the register designated by R_1 is the fetch protection bit and is set to one for both store and fetch protection or to zero for store protection only.

Condition Code: The code remains unchanged.

Program Interruptions

Operation (if the protection feature is not installed)

Privileged operation

Addressing

Protection

Specification

Console Printer-Keyboard

The console printer-keyboard (Figure 1) provides for communication between the operator and the system. Facilities are provided for interrupting the processing unit and for signalling the end of a data transmission.

The printer-keyboard has a stationary carriage and a replaceable, interchangeable printing sphere. Its typewriter-style keyboard and the printing function can be used independently: the keyboard for system input and the printer for computer output. The font of each printing sphere is specified by the customer.

The functions and operations of the console printer-keyboard are the same as those described for the IBM 1052 Printer-Keyboard Model 7 in *IBM System/360 System Summary*, Form A22-6810.

The console printer-keyboard is attached to one of the system channels via an adapter which is physically located within the CPU as a standard feature. The installation of the console printer-keyboard is standard and takes up one control-unit position and one subchannel of either a multiplexor channel or high-speed multiplexor channel.

Single-Disk Storage Drive

The single-disk storage drive provides direct access auxiliary storage for a minimum of 1,171,200 bytes on a single disk permanently enclosed in an IBM 2315 Disk Cartridge and housed within the CPU, with side access for replacement of cartridges. It is a standard feature.

The data rate of the disk storage is 90,000 bytes per second, necessitating operation in burst mode. Average access time is 70 milliseconds.

Information is written on or read from the disk by a pair of magnetic read/write heads, one head for each surface. The disk is organized in 200 cylinders and three spare cylinders; a cylinder consists of a pair of tracks, one track per disk surface. Each cylinder contains 16 sectors (eight per track and surface). Each sector has a fixed length of 366 bytes. The three spare cylinders ensure that the stated capacities are maintained for the life of the cartridge. The read/write heads move, under a single seek command, directly to the track addressed. Error detection is accomplished on reading data from the disk.

No programming compatibility exists between the single-disk storage drive and disk storage drives controlled through the IBM 2841 Storage Control.

The drive is attached to one of the system channels only via an adapter, which is also installed in the CPU as a standard feature. A second drive may be installed in the CPU, as a special feature, to double the storage capacity. The two drives use the same shared-path adapter and operate on one shared subchannel, requiring one control-unit position on either a multiplexor or a high-speed multiplexor channel. Seek overlap is permissible when both drives are installed.

Commands

Control Seek – 00001011: One byte is transferred to the adapter. The byte contains the required cylinder address (0 through 202). The channel is free after the transfer of this byte, and the drive is free at the end of the seek.

Read Data – HSSS1010: Reading begins with the head for track H, sector SSS, and continues to the end of the track. If SSS=0, the entire track of 2,928 bytes is read. If the CCW count goes to zero at the end of sector 7 (end of track) or before the end of any other sector, the drive is free at the end of the sector being read. If the CCW count goes to zero at the last byte of a sector 0-6, however, the device end is delayed until the end of the following sector.

Write Data – HSSS1001: Writing begins at track H, sector SSS, and continues to the end of the track. If the CCW count goes to zero before the end of the track, the remainder of the sector being written is filled with zeros by the adapter and the drive is then free.

Other Commands: The adapter also recognizes read IPL (00000010), control no-op (00000011), and sense commands (00000100).

Programming Notes

The formal record length of the single-disk storage drive is 2,928 bytes (one full track); therefore, "incorrect length" is a normal indication. The CCW for a read or write command must contain the SLI flag (suppress-length-indication, bit 34) unless the operation is to end with the 366th byte of the eighth sector.

Command chaining to the next sector may take place at a sector boundary without rotational delay unless a read operation ends with the 366th byte of sectors 0-6.

Keys and Lights

All keys and lights for the proper operation of each drive are located above each disk cartridge slot.

Start Key starts the drive motor.

Stop Key turns off the drive motor.

Ready Light lights when power is on, the disk is at full rotational speed, and the arm is ready to receive a seek command.

Cartridge Unlocked Light indicates that the disk cartridge is unlocked from the drive and may be removed by the operator.

Instructions

The Model 44 executes the following instructions:

	MNEMONICS			
	RR	RX	RS	SI
INSTRUCTION	FORMAT	FORMAT	FORMAT	FORMAT
Add	AR	A	---	---
Add Halfword	---	AH	---	---
Add Logical	ALR	AL	---	---
AND	NR	N	---	NI
Branch and Link	BALR	BAL	---	---
Branch on Condition	BCR	BC	---	---
Branch on Count	BCTR	BCT	---	---
Compare	CR	C	---	---
Compare Halfword	---	CH	---	---
Compare Logical	CLR	CL	---	CLI
Divide	DR	D	---	---
Exclusive OR	XR	X	---	XI
Halt I/O	---	---	---	HIO
Insert Character	---	IC	---	---
Load	LR	L	---	---
Load Address	---	LA	---	---
Load and Test	LTR	---	---	---
Load Complement	LCR	---	---	---
Load Halfword	---	LH	---	---
Load Negative	LNR	---	---	---
Load Positive	LPR	---	---	---
Load PSW	---	---	---	LPSW
Move	---	---	---	MVI
Multiply	MR	M	---	---
Multiply Halfword	---	MH	---	---
OR	OR	O	---	OI
Set Program Mask	SPM	---	---	---
Set System Mask	---	---	---	SSM

INSTRUCTION	MNEMONICS RR FORMAT	RX FORMAT	RS FORMAT	SI FORMAT
Shift Left Double	——	——	SLDA	——
Shift Left Double Logical	——	——	SLDL	——
Shift Left Single	——	——	SLA	——
Shift Left Single Logical	——	——	SLL	——
Shift Right Double	——	——	SRDA	——
Shift Right Double Logical	——	——	SRDL	——
Shift Right Single	——	——	SRA	——
Shift Right Single Logical	——	——	SRL	——
Start I/O	——	——	——	SIO
Store	——	ST	——	——
Store Character	——	STC	——	——
Store Halfword	——	STH	——	——
Subtract	SR	S	——	——
Subtract Halfword	——	SH	——	——
Subtract Logical	SLR	SL	——	——
Supervisor Call	SVC	——	——	——
Test and Set	——	——	——	TS
Test Channel	——	——	——	TCH
Test I/O	——	——	——	TIO
Test Under Mask	——	——	——	TM

An optional feature provides the full complement of floating-point instructions for both long and short operands and the RR and RX formats:

INSTRUCTION	MNEMONICS RR FORMAT LONG	RR FORMAT SHORT	RX FORMAT LONG	RX FORMAT SHORT
Add Normalized	ADR	AER	AD	AE
Add Unnormalized	AWR	AUR	AW	AU
Compare	CDR	CER	CD	CE
Divide	DDR	DER	DD	DE
Halve	HDR	HER	——	——
Load	LDR	LER	LD	LE
Load and Test	LTDR	LTER	——	——
Load Complement	LCDR	LCER	——	——
Load Negative	LNDR	LNER	——	——
Load Positive	LPDR	LPER	——	——
Multiply	MDR	MER	MD	ME
Store	——	——	STD	STE
Subtract Normalized	SDR	SER	SD	SE
Subtract Unnormalized	SWR	SUR	SW	SU

As already described under "Protection Feature," two more instructions are added when that special feature is installed:

INSTRUCTION	FORMAT	MNEMONICS
Set Storage Key	RR	SSK
Insert Storage Key	RR	ISK

Full description of each instruction will be found in *IBM System/360 Principles of Operation,* Form A22-6821.

Variable Long-Precision Floating-Point

Some floating-point problems need more than short precision but do not require the maximum 56 bits of long precision. With the variable long-precision floating-point feature, the user can adjust long-precision instructions for execution with 32, 40, 48, or the full 56 bits of precision. The adjustment for variable long-precision floating-point is made at program execution time by setting a rotary switch on the system control panel to one of four positions (Figure 3). Each successive, lower setting truncates eight bits from the fraction length. Figure 5 shows the effect on execution time.

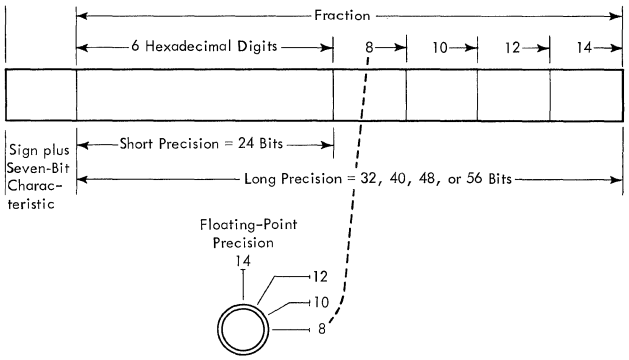


Figure 3. Variation of Fraction Length in Long Precision

SWITCH SETTING (NO. OF HEXADECIMAL DIGITS IN FRACTION)	LONG PRECISION (FRACTION LENGTH IN BITS)
14	56
12	48
10	40
8	32

For maximum speed, the switch is set to 8; for maximum precision, it is set to 14. Setting the switch to 14 maintains complete compatibility with other System/360 models using long-precision floating-point. At settings 8, 10, or 12, all floating-point operations fetch the operands (from storage or floating-point registers) truncated to the selected fraction length; low-order zeros are assumed to exist to the right of the truncation point. Model 44 always performs long-precision arithmetic with 56 bits. Therefore, when the truncated fraction is right-shifted for alignment during the performance of addition, subtraction, and comparison instructions, two, four, or six guard digits (depending on the selected precision) participate in the computation. With unnormalized addition and subtraction, the fraction in the result is tested for lost significance up to the selected fraction length.

Indexing Time

All Model 44 instruction timings (Figures 4 and 5) include the 1-microsecond I time and, for instructions that reference storage, the time to perform single indexing by one general register as referenced in the instruction (i.e., $B \neq 0$).

For instructions in which double indexing is possible (i.e., all RX format instructions) the time required for the second indexing is 1 microsecond on the basic Model 44, or 0.75 microsecond when the high-speed general register feature is installed. The times shown for the eight shift instructions assume no indexing (i.e., $B = 0$). For special timing calculations, the following adjustments may be made:

Microseconds**

Instruction	Format	Mnemonic	Basic Model 44		Model 44 with High-Speed General Register Feature	
Add	RR	AR	3.75		1.75	
Add	RX	A	4.75		2.25	
Add Halfword	RX	AH	4.75		2.25	
Add Logical	RR	ALR	3.75		1.75	
Add Logical	RX	AL	4.75		2.25	
AND	RR	NR	3.75		1.75	
AND	RX	N	4.75		2.25	
AND	SI	NI	3.75		3.00	
Branch and Link	RR	BALR	3.25		2.25	
Branch and Link	RX	BAL	3.25		2.50	
Branch on Condition	RR	BCR	BR 2.50 No BR 1.00		1.75 1.00	
Branch on Condition	RX	BC	BR 2.75 No BR 2.00		2.00 1.25	
Branch on Count	RR	BCTR	3.75		2.50	
Branch on Count	RX	BCT	3.75		2.75	
Compare	RR	CR	3.00		1.75	
Compare	RX	C	4.00		2.25	
Compare Halfword	RX	CH	4.00		2.25	
Compare Logical	RR	CLR	3.00		1.75	
Compare Logical	RX	CL	4.00		2.25	
Compare Logical	SI	CLI	3.25		2.50	
Divide	RR	DR	31.75		28.50	
Divide	RX	D	32.75		29.00	
Exclusive OR	RR	XR	3.75		1.75	
Exclusive OR	RX	X	4.75		2.25	
Exclusive OR	SI	XI	3.75		3.00	
Halt I/O	SI	HIO	10-40		10-40	
Insert Character	RX	IC	4.00		2.50 EA,2.25 OA	
*Insert Storage Key	RR	ISK	3.00			
Load	RR	LR	3.00		1.00	
Load	RX	L	4.00		2.25	
Load Address	RX	LA	3.00		1.25	
Load and Test	RR	LTR	3.00		1.00	
Load Complement	RR	LCR	3.00		1.75	
Load Halfword	RX	LH	4.00		2.25	
Load Negative	RR	LNR	3.00		1.75	
Load Positive	RR	LPR	3.00		1.75	
Load PSW	SI	LPSW	4.50		3.75	
Move	SI	MVI	3.75		3.00	
Multiply	RR	MR	13.00 - 21.00		11.25 - 19.25	
Multiply	RX	M	14.00 - 22.00		11.75 - 19.75	
Multiply Halfword	RX	MH	10.00 - 14.00		8.25 - 12.25	
OR	RR	OR	3.75		1.75	
OR	RX	O	4.75		2.25	
OR	SI	OI	3.75		3.00	
Set Program Mask	RR	SPM	2.00		1.50	
*Set Storage Key	RR	SSK	3.00			
Set System Mask	SI	SSM	3.50 EA,4.00 OA		2.75 EA,3.00 OA	
			S ≤ 3	S > 3	S ≤ 1	S > 1
Shift Left Double	RS	SLDA	5.50	5.50 + 0.25 (S-3)	3.25	3.25 + 0.25 (S-1)
Shift Left Double Logical	RS	SLDL	5.50	5.50 + 0.25 (S-3)	3.25	3.25 + 0.25 (S-1)
Shift Left Single	RS	SLA	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Left Single Logical	RS	SLL	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Right Double	RS	SRDA	5.50	5.50 + 0.25 (S-3)	3.25	3.25 + 0.25 (S-1)
Shift Right Double Logical	RS	SRDL	5.50	5.50 + 0.25 (S-3)	3.25	3.25 + 0.25 (S-1)
Shift Right Single	RS	SRA	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Right Single Logical	RS	SRL	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
			For single indexing of shift instructions, Add 1.00		For single indexing of shift instructions, Add 0.25	
Start I/O	SI	SIO	10-43		10-43	
Store	RX	ST	4.25		2.50	
Store Character	RX	STC	4.75 EA,4.25 OA		3.00 EA,2.50 OA	
Store Halfword	RX	STH	4.25		2.50	
Subtract	RR	SR	3.75		1.75	
Subtract	RX	S	4.75		2.25	
Subtract Halfword	RX	SH	4.75		2.25	
Subtract Logical	RR	SLR	3.75		1.75	
Subtract Logical	RX	SL	4.75		2.25	
Supervisor Call	RR	SVC	1.00		1.00	
Test and Set	SI	TS	3.50		2.75	
Test Channel	SI	TCH	4.00		3.25	
Test I/O	SI	TIO	10-40		10-40	
Test Under Mask	SI	TM	3.00 EA,3.25 OA		2.25 EA,2.50 OA	
			For double indexing of RX format instructions, add	1.00		0.75

NOTES: EA = Even Address
OA = Odd Address
S = Number of bits shifted
*Instruction added with protection feature
**All times except those for the eight shift instructions include single indexing; see "Indexing Time."

● Figure 4. Execution Time for Standard Instructions and Protection-Feature Instructions of Model 44