IBM Maintenance Library

3705 Communications Controller
Theory—Maintenance
Volume II

SY27-0107-6

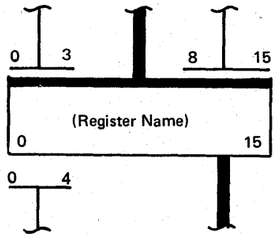
ABBREVIATIONS

A	And circuit or ampere
AA	automatic answering
ABAR	attachment buffer address register
ABO	adapter bus out (register)
ac	alternating current
ACO	automatic call originate
ACF/NCP/VS	Advanced Communications Function for Network Control Program/Virtual Storage
ACR	abandom call and retry
ACU	automatic calling unit
adr	address
AEQ	automatic equalizer
AHR	add halfword register (instruction)
ALD	automated logic diagram
ALU	arithmetic logic unit
AMP	amplifier
APAR	authorized program analysis report
AR	add register (instruction)
ARI	add register immediate (instruction)
B	branch (instruction)
BAL	branch and link (instruction)
BALR	branch and link register (instruction)
BAR	buffer address register
BB	branch on bit (instruction)
BC	bit clock
BCB	bit control block
BCC	bit clock control
BCL	branch on C latch (instruction)
BCT	branch on count (instruction)
BO	bus out
BP	break point
bps	bit per second
BSC	binary synchronous communication
BSM	bridge storage module
BZL	branch on Z latch (instruction)
CA	channel adapter
CACHKR	channel adapter check register
CACR	channel adapter control register
CADB	channel adapter data buffer
CAMR	channel adapter mode register
CASNSR	channel adapter sense register
CASTR	channel adapter status register
CB	circuit breaker
CBAR	CSB buffer address register
CCB	character control block
CCR	compare character register (instruction)
CCT	coupler cut through (modem)
CCU	central control unit
CD	carrier detect
CDS	configuration data set
CE	Channel End (status)
chan	channel
char	character
CHR	compare halfword register (instruction)
ck	check
clk	clock
cm	centimeter
CMDR	channel adapter command register
CMND	command
com	common
COS	Call Originate Status
CP	circuit protector
CPU	central processing unit
CR	compare register (instruction)
CRC	cyclic redundancy check
CRI	compare register immediate (instruction)
CRQ	Call Request
CS	cycle steal
CSAR	cycle steal address register
CSB	communication scanner
CSCD	clear to send, carrier detect
CSMC	cycle steal message counter
ctrl	control
CTS	Clear To Send
CUCR	Cycle Utilization Counter Register
CUE	Control Unit End (status)
CW	control word
CWAR	control word address register
CWCNTR	control word byte count register
DAA	data access arrangement
DA	data modem ready
dB	decibel
DBAR	diagnostic buffer address register
dc	direct current
DCE	data circuit-terminating equipment
DCM	diagnostic control module
DCR	data channel ready
DE	Device End (status)
DET	detector
diag	diagnostic
dist	distance
DLO	data line occupied
DOS	Disk Operating System
DPR	digit present
DR	display register or data ring (modem)
DCS	distant station connect (ACO only)
DSR	data set ready
DT	data tip (modem)
DTE	data terminal equipment
DTR	data terminal ready
EC	edge connector
EB	extended buffer
ECP	emulation control program
EIA	Electronic Industries Association
enbl	enable
EON	end of number (ACO only)
EPO	emergency power off
ESC	emulation subchannel
EXT	external
FCS	final control sequence
FET	field effect transistor modem card
FETOM	Field Engineering Theory of Operation Manual
FF	flip flop
FL	flip latch
FRU	field replaceable unit
GB	ground bus
gnd	ground
hex	hexadecimal
Hlfwd	halfword
horz	horizontal
HS	heat sink
Hz	Hertz
I	instruction (cycle)
IAR	instruction address register
IC	insert character (instruction)
ICS	initial control sequence
ICT	insert character and count (instruction)
ICW	interface control word
IFT	internal functional test
IN	input (instruction)
INCWAR	inbound control word address register
Init	initial
int	internal
intf	interface
I/O	input/output
IPL	initial program load
IR	interrupt remember
ISACR	initial selection address and command register
L	load (instruction)
LA	load address (instruction)
LAR	lagging address register
LCD	line code definer
LCOR	load character with offset register (instruction)
LCR	load character register (instruction)
LED	light emitting diode
LGF	leading graphics flag
LH	load halfword (instruction)
LHOR	load halfword with offset register (instruction)
LHR	load halfword register (instruction)
LIB	line interface base
lim	limiter
LOR	load with offset register (instruction)
LOSC	last oscillator sample condition
LR	load register (instruction)
LRI	load register immediate (instruction)
LS or ls	local store
lt	latch
L1	level 1
L2	level 2
L3	level 3
L4	level 4
L5	level 5
mA	milliampere
Mem TB	memory terminal board
modem	modulator/demodulator
ms/divn	milliseconds per division
MST	monolithic system technology
mV	millivolt
NB	Digit Signal
N/C	normally closed
NCP	network control program
NCR	and character register (instruction)
NHR	and halfword register (instruction)
N/O	normally open
NR	and register (instruction)
NRI	and register immediate (instruction)
NRZI	non-return-to-zero inverted
ns	nanoseconds
NSC	native subchannel
OBR	outboard recorder
O/C	overcurrent
OCR	or character register (instruction)
OE	exclusive or
OH	off hook (modem)
OHR	or halfword register (instruction)
OLT	on line test
OLTEP	on line test executive program
OLTLIB	on line test library
OLTSEP	on line test standalone executive program
op	operation
op reg	operation register
OR	or register (instruction)
ORI	or register immediate (instruction)
OS	Operating System
OSC	oscillator
OUT	output (instruction)
OUTCWAR	outbound control word address register
OVRN	overrun
O/V	overvoltage
P	parity
PC	parity check
PCF	primary control field
PCI	program controlled interrupt
PDF	parallel data field
PEP	partitioned emulation programming
PG	parity generation
pgm	program
PH	polarity hold
PND	Present Next Digit
P/N	part number
POR	power on reset
pos	position

POSC	present oscillator sample condition
pot	potentiometer
P-P	post processor modem card
PPB	prime power box
PUT	programmable unijunction transistor
PWI	power indicator
R	resistance or resistor
rcv	receive
rd	read
rdy	ready
RE	register and external register (instructions)
ref	reference
reg	register
regen	regenerative
req	request
RI	register immediate (instruction) or ring indicator (modem)
RLSD	receive line signal detector
RMS	root mean square
ROS	read-only storage
RPL	remote program loader
RR	register to register (instructions)
RS	register to storage (instructions)
RSA	register and storage with addition (instructions)
RT	register branch or register and branch (instructions)
RTS	Request To Send
rly	relay
SAR	storage address register
SCF	secondary control field
SCR	silicon controlled rectifier or subtract character register (instruction)
SCRID	silicon controlled rectifier indicator driver
SDF	serial data field
SDLC	synchronous data link control
SDR	storage data register
sec	second
sel	selection
SEP	separator (ACO only)
seq	sequence
SG	signal ground
SH	switch hook (modem)
SHR	subtract halfword register (instruction)
SIG	signal
SIO	start I/O
SMS	standard modular system
SR	subtract register (instruction)
SRI	subtract register immediate (instruction)
SRL	Systems Reference Library
S/S	start/stop
ST	store (instruction)
STC	store character (instruction)
STCT	store character and count (instruction)
STH	store halfword (instruction)
stk	stacked
svc	service
sw	switch
SYN	synchronous idle
sync	synchronization or synchronous
TAR	temporary address register
TB	terminal board
TIC	Transfer In Channel
tr	trigger
TRM	test register under mask (instruction)
TSL	Technical Service Letter
T2	test 2
T3	test 3
T4	test 4
UC	Unit Check (status)
UE	Unit Exception (status)
V	volts
V/divn	volts per division
wd	word
wr	write
XCR	exclusive-or character register (instruction)
xfer	transfer
xfmr	transformer
XHR	exclusive-or halfword register (instruction)
xmt	transmit
XR	exclusive-or register (instruction)
XRI	exclusive-or register immediate (instruction)
2W	two-wire line connection (implies half-duplex)
4W	four-wire line connection (implies duplex, but actual duplex depends on the line set type and telephone company equipment.

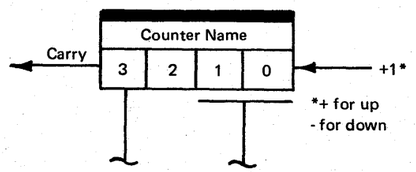
LEGEND

1. Logic Diagrams

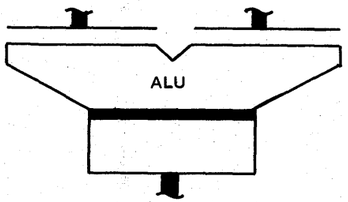


Register

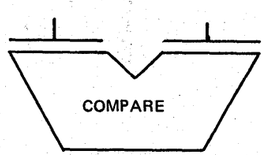
The input side is denoted by a thick line. A partial transfer of contents is shown by numbered input and/or output lines.



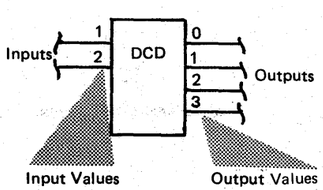
Counter



ALU

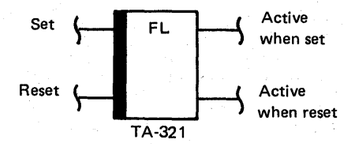


Compare



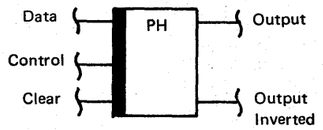
Decode

The active output is the output whose output value equals the sum of the active input values.



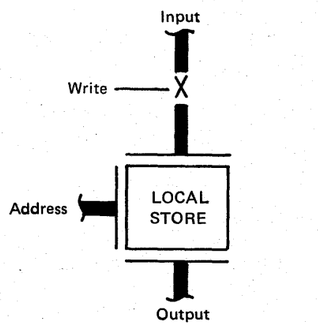
Flip Latch

Input side is denoted by a thick line. ALD reference page may be shown beneath.



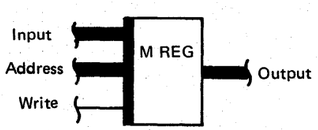
Polarity Hold

The 'output' of the polarity hold block is at the indicated polarity when both the 'data' and the 'control' lines go to their indicated polarity. When the 'control' line goes to the polarity opposite to that indicated, the 'output' line holds at the polarity it is at. When the 'clear' line goes to its indicated polarity, the 'output' line goes to the polarity opposite to that indicated.



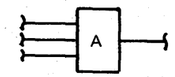
Local Store

Read---Output from the local store addressed. Contents of local store is not destroyed.
Write---Input contents stored in the local store addressed when 'write' is active.

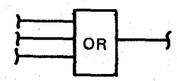


M REG

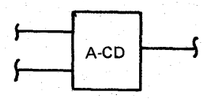
See Local Store



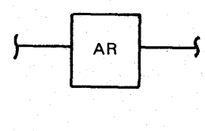
AND



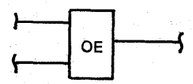
OR



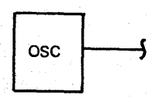
AND Current Driver



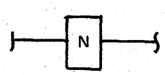
Amplifier



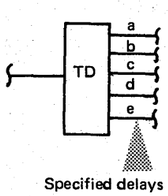
Exclusive OR



Oscillator



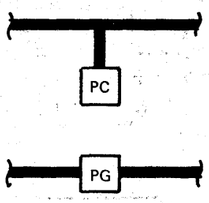
Negator (Inverter)



Time Delay

An input pulse starts the time delay. Each output pulse has the same duration as the input pulse but is delayed by the specified amount.

LEGEND (PART 2)

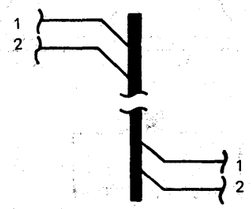


Parity Check

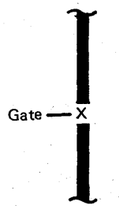
Parity check on the data bus

Parity Generate

Parity generated on the data bus



Multiple Line Transfer

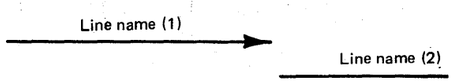


Gated Bus

Gate must be active for data to flow on bus.

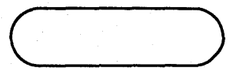
Test Point

Signal that may be scoped.



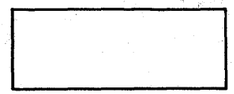
Above symbol indicates change in line name.

2. Flowcharts



Terminal

Indicates the beginning or end of the event.

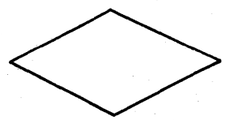


Process

Indicates a major function or event.

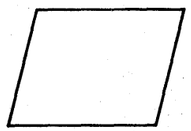
Annotation

Gives descriptive comment or explanatory note.



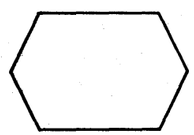
Decision

Indicates a point in a flowchart where a branch to an alternate path is possible.



Input-Output

CCU executes the control program input/output instructions.

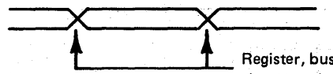


Hardware Process

Type 2 scanner hardware action resulting from input/output instructions or signals from the line/autocall interface.

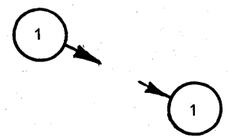
3. Timing Charts

Numerals at the beginning and end of the bar identify the signal(s) (also on the same chart) that activate and deactivate this line. '(Not)' with the number indicates that lack of the signal conditions the line.



Register, bus, or local store content changes value at these points.

4. General



On-page Connector

Indicates a connection between two parts of the same page. The arrow leaving the symbol points (line-of-sight) to a correspondingly-numbered symbol.

Off-page Connector

Indicates a connection between diagrams located on separate pages. The location of the correspondingly-lettered symbol is shown adjacent the symbol.

CONTENTS VOLUME 2

CONTENTS-VOLUME 2

TYPE 2 CHANNEL ADAPTER

INTRODUCTION

The 3705 type 2 channel adapter (type 2 CA) is a high performance adapter capable of instantaneous channel data transfer rates of up to 276 kilobytes per second, and is limited to 277, 166, 92, or 49 kilobytes per second with jumpers on the card in location Z4F2, (logic page QN003).

A maximum of two type 2 channel adapters can be installed in the 3705 system—one in the basic 3705 frame and one in the first 3705 expansion frame. The type 2 CA can be attached to a multiplexer channel, selector channel, or block multiplexer channel available on the System/370. The adapter operates in byte, burst, or block mode, and disconnects from the channel at the appropriate time. No hardware modification is necessary for the different modes of operation. Both of the CAs can be attached to the same channel or to separate channels, and both can operate simultaneously.

The type 2 CA is minimally dependent upon the 3705 control program. Channel operation is initialized by the control program in much the same way as an I/O operation is initiated in a System/370. Data transfer and cycle-steal control word chaining are handled without control program intervention. As in the System/370, the type 2 CA notifies the control program, when a data transfer is complete, with an interrupt (type 2 CA level 3 interrupt). If an error occurs during the data transfer operation, the adapter requests a level 1 interrupt.

The control program uses input and output instructions to:

- Initialize the type 2 channel adapter to accept channel I/O Read or Write type commands.
- Determine what ending status should be presented (normal or unusual) to the host processor when the data transfer is complete.

The type 2 channel adapter responds to the following seven valid channel commands:

- Sense X'04'
- Write IPL X'05'
- Write X'01'
- Read X'02'
- Test I/O X'00'
- No/Op X'03'
- Write Break X'09'

All other commands are control commands. The 3705 control program has the option of (1) having the CA hardware command reject the control commands during initial selection or (2) having the CA hardware accept the control commands by presenting an initial channel end status and then requesting a level three interrupt (see Page 9-311). The Network Control Program uses the following control commands:

- Write Start Zero X'31'
- Write Start One X'51'
- Read Start Zero X'32'
- Read Start One X'52'
- Restart Reset X'93'

ADDRESS SELECTION

The 3705 must be assigned a channel address. The address can be any channel address from 0 and 255. If no address is selected, the type 2 CA responds to address 255 on the channel bus out.

Refer to the type 2 CA reference Page, QA071, for address selection Jumper information.

If the channel adapter is enabled (control panel enabled light on) and the CCU 'hard stop' latch is set, the CA does not recognize its address and trap 'select out'. However, the enabled light remains on.

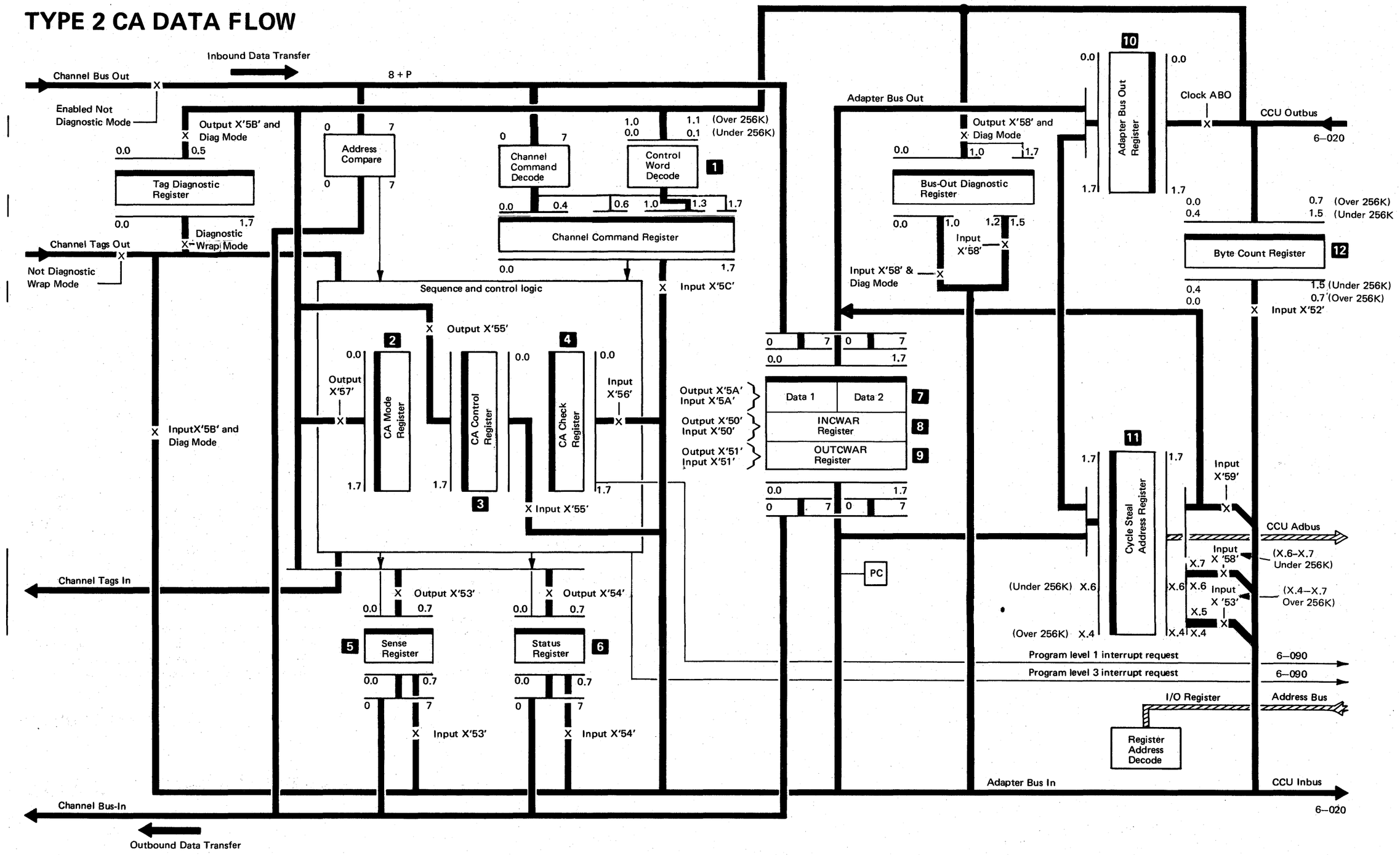
CYCLE STEAL RATE SELECTION

Cycle-steal rate selection is a plug variable delay in the generation of 'Allow CS Req'.

The delay is selected by plugging jumpers on the MST card at Z4F2. If no rate is selected, 'Allow CS Req' does not turn on.

Refer to the type 2 CA reference page, QA071 for cycle steal data rate jumper information.

TYPE 2 CA DATA FLOW



TYPE 2 CA DATA FLOW (PART 2)

1
COMMAND REGISTER

The channel adapter command register (CMDR) indicates the last channel command in process and the last cycle-steal control word executed.

2
CHANNEL ADAPTER MODE REGISTER

The channel adapter mode register (CAMR) is used to initiate and halt channel adapter operation.

3
CHANNEL ADAPTER CONTROL REGISTER

The 3705 control program controls initiation and termination of channel adapter operations with the channel adapter control register (CACR).

4
CHANNEL ADAPTER CHECK REGISTER

Latches are set in the channel adapter check register (CACHKR) to request level 1 interrupts. When the 3705 control program services the interrupt request, the contents of this register can be transferred to a CCU general register so that the control program can determine the exact cause of the interrupt.

All latches except Bus Out check are reset when an Output to the channel adapter mode register (CAMR) to reset the L1 interrupt request is executed. Bus Out check is reset when the sense register is reset. The sense register is reset when a command other than Sense, Test I/O, or No-Op is accepted by the CA.

5
CHANNEL ADAPTER SENSE REGISTER

The channel adapter sense register (CASNSR) provides the sense byte to be gated onto the channel Bus-In in response to a channel Sense command.

The sense byte is standard for the System/360 except for bits 6 and 7, which are unique to the 3705. See 9-150 for the definitions of sense register bits.

6
CHANNEL ADAPTER STATUS REGISTER

The channel adapter status register (CASTR) contains the standard IBM System/360 status byte to be gated to the channel Bus-In for status presentations. The status register bits are defined on 9-160.

7
CHANNEL ADAPTER DATA BUFFER

The channel adapter data buffer register (CADB) forms the CA buffer for all channel data transferred through the CA.

The contents of this register are unpredictable when power is turned on in the 3705. As a result, the control program should first load the register before attempting to transfer the contents into a CCU general register. If an Input X'5A' instruction is executed before an Output X'5A', a CWAR/Data buffer parity check may occur.

8
IN-BOUND CONTROL WORD ADDRESS REGISTER

The in-bound control word address register (INCWAR) contains the low order 16 bits of the storage address of the cycle-steal control word to be fetched when a channel Write type command is decoded. The contents of INCWAR are incremented by 4 (bytes) for each CW fetch operation.

When power is turned on in the 3705, the contents of this register are unpredictable. Therefore, the control program should first load this register with predictable contents before attempting to transfer the contents of the register to the CCU. If an Input X'50' is executed before an Output X'50' instruction, a CWAR/Data buffer parity check may occur.

9
OUT-BOUND CONTROL WORD ADDRESS REGISTER

The out-bound control word low order 16 bits of the storage address register (OUTCWAR) contains the address of a control word to be fetched for a channel Read command. The contents of this register are incremented by 4 (bytes) for each CW fetch operation.

When power is turned on in the 3705, the contents of this register are unpredictable. Therefore, the 3705 control program should load the register with predictable contents before attempting to transfer the contents of the register to a CCU general register. If an Input X'51' instruction is executed before an Output X'51' instruction, a CWAR/Data buffer parity check may occur.

10
CHANNEL ADAPTER BUS OUT REGISTER

The adapter bus out register (ABO) provides buffering between the CCU Outbus and the channel adapter.

11
CYCLE STEAL ADDRESS REGISTER

The cycle-steal address register (CSAR) contains the current data address while data transfer is in progress. This register is loaded with the CW address at the beginning of a CW fetch cycle-steal operation, and is loaded with the starting address of the data at the end of the CW fetch cycle steal. CSAR is incremented by 2 for each halfword (two bytes) of data stored or fetched on data-handling cycle-steal operations.

12
CONTROL WORD BYTE COUNT REGISTER

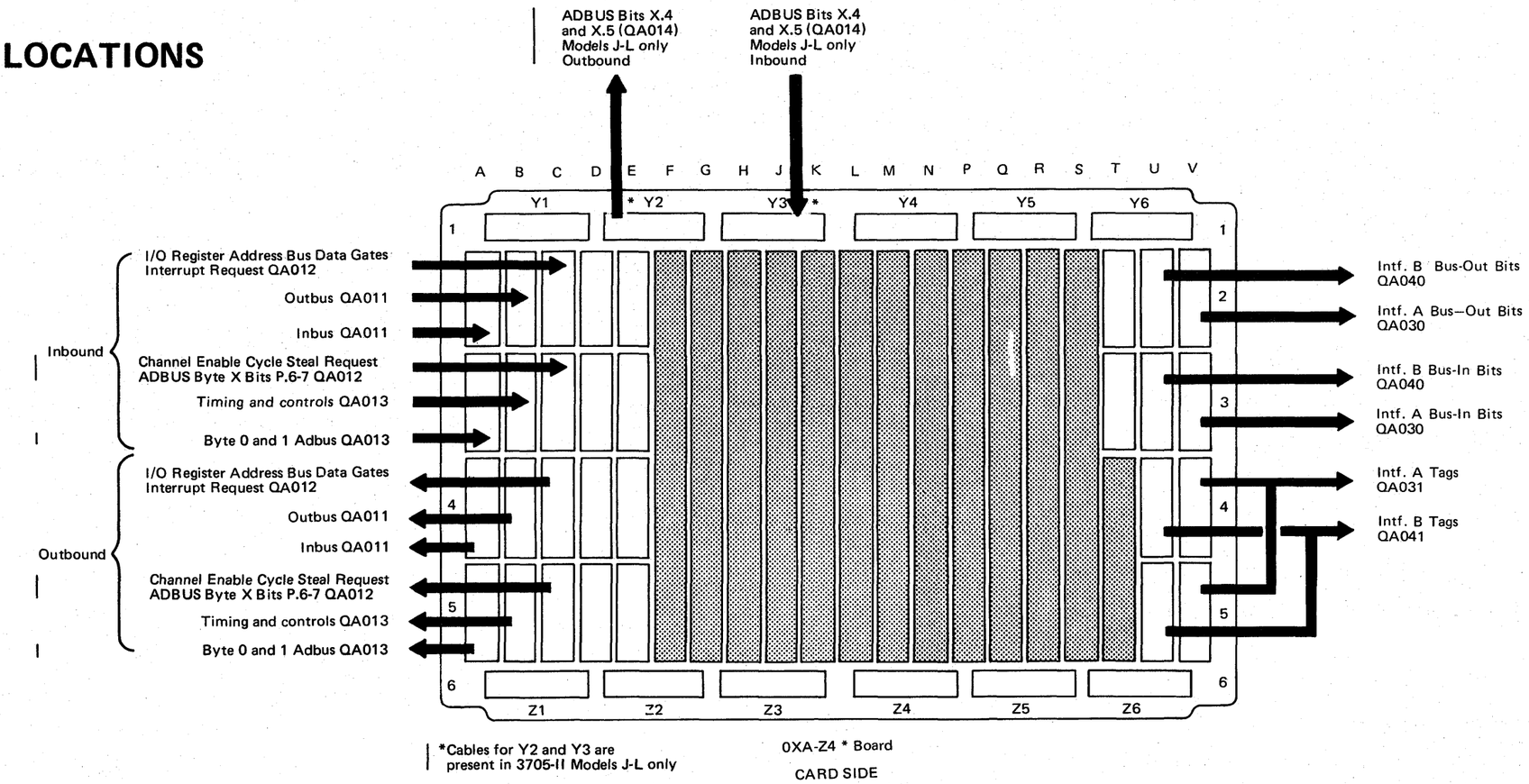
The control word byte count register contains the 10-bit byte count. In non-IPL mode, 3705-II Models J-L use only eight of the ten bits in the byte count.

In IPL mode, however, a 10-bit byte count is forced by turning on the two high-order bits. The first half of the control word fetched (9-260) loads the byte count into CWCNTR. As each byte is transferred across the channel interface, the byte count is decremented by 1.

CARD FUNCTIONS AND LOCATIONS

Card Loc.	First ALD Page	Function
Z4T2	QR001	Cycle Steal Address Register Byte X
Z4Q2	QB001	Interface A Drivers
Z4P2	QC001	Interface A Receivers Diagnostic Registers
Z4S2	QD001	Intf. B Drivers
Z4R2	QE001	Intf. B Receivers
Z4N2	QF001	Channel Tag Clock Tag Control Tag Control Powering
Z4M2	QG001	Cycle Steal Control Channel Buffer Control Data Transfer Control Control Command Enabled
Z4L2	QH001	Input/Output Decode Adapter Select Jumpering CW Count Register CWAR valid latches CW Command Decode Diagnostic Wrap Mode Latch
Z4K2	QJ001	Interrupt Requests Channel Command Decode Reset and Diagnostic Clock
Z4J2	QK001	Sense and Status Latches and Gates
Z4H2	QL001	Byte 0 of CWAR Data Buffer CSAR CCU Outbus Buffer
Z4G2	QM001	Byte 1 of CWAR Data Buffer CSAR CCU Outbus Buffer
Z4F2	QN001	CA Check Register Cycle Steal Rate Jumpering Active latch End Busy latch CE Remb latch Increment CSAR Burst Mode latch Error Latches

Note:
Z4Q2 and S2 can be swapped
Z4P2 and R2 can be swapped
Z4H2 and G2 can be swapped



*Cables for Y2 and Y3 are present in 3705-II Models J-L only

0XA-Z4 * Board

CARD SIDE

See G-030 for the card functions and locations for the type 3 CA.

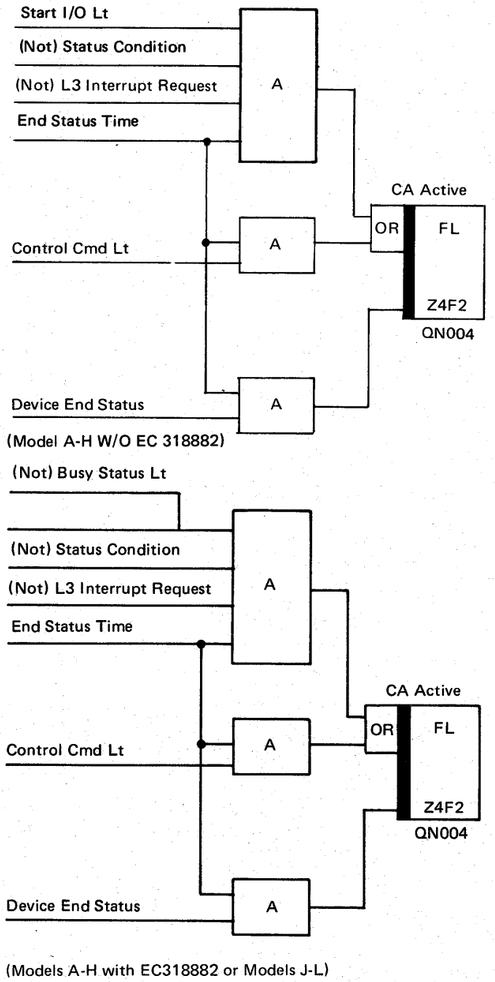
*Z4 is the pseudo board location for the type 2 channel adapter. The actual board location is 0XA-A4.

CHANNEL ADAPTER STATES

The problems associated with handling two asynchronous interfaces require that the type 2 channel adapter be in a certain state with respect to one interface before permitting access to the adapter by the other interface.

ACTIVE STATE

This state is defined as the period from the acceptance of a channel I/O command by the adapter until the acceptance of Device End (DE) status by the channel for that command.



(Models A-H with EC318882 or Models J-L)

LEVEL 3 INTERRUPT STATE

This state may be initated either by the control program or by completion of the current cycle-steal control word. The CA may be either active or inactive when this state is initiated. If the CA is active, the control program has access to all CA registers. If the CA is not active, the control program has access to all registers except the channel sense and status registers.

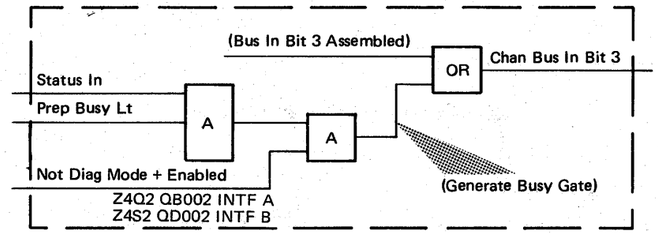
LEVEL 1 INTERRUPT STATE

This state is initiated only when the CA detects an error during the execution of an input or output instruction to the channel adapter, during a cycle steal operation, or during a data transfer across the channel interface.

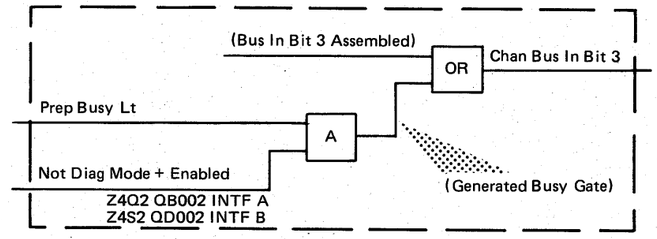
If a channel command is being executed when the error is detected, the command is ended with a hardware generated Channel End (CE), Device End (DE), and Unit Check (UC) status when the level 1 interrupt is requested.

BUSY STATE

This state refers to Busy status generation for the channel, independent of the status register. The channel is notified that the 3705 is busy without disturbing the contents of the channel adapter status register. This state exists when the channel attempts an initial selection sequence when the CA is both active and engaged in either a level 1 or a level 3 interrupt.



Generating Busy status without disturbing the status register contents.
(Models A-H W/O EC 318882.)



Generating Busy status without disturbing the status register contents.
(Models A-H with EC 318882 or Models J-L.)

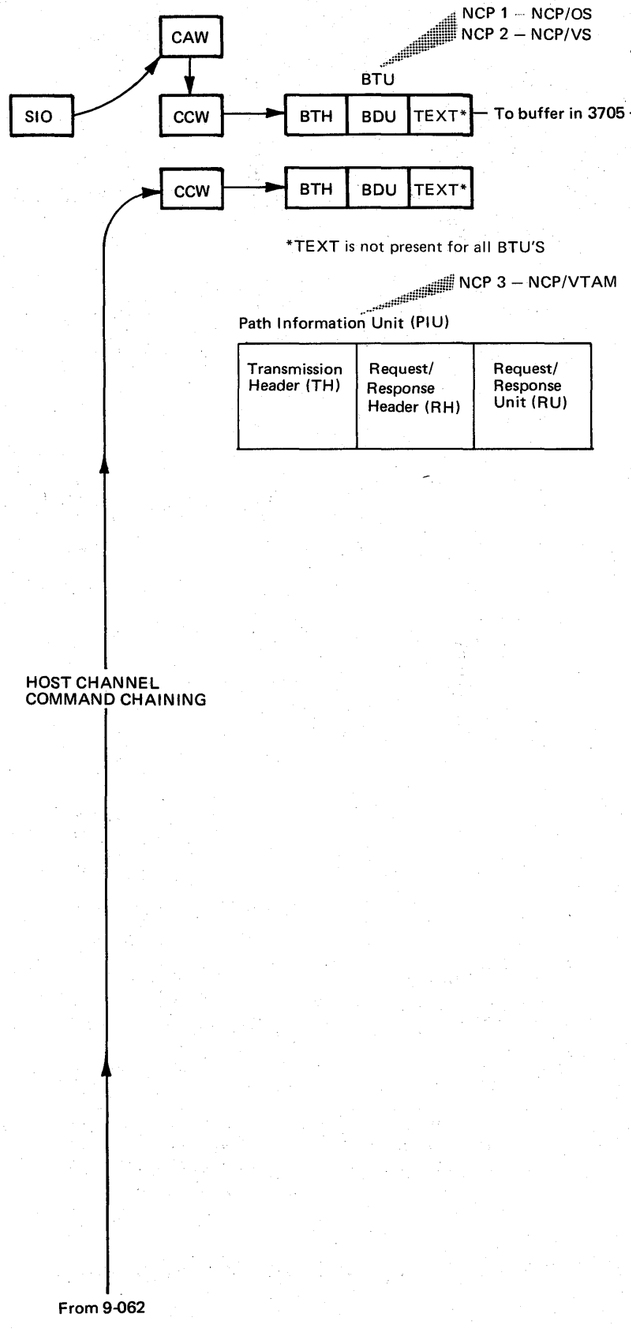
DIAGNOSTIC WRAP STATE

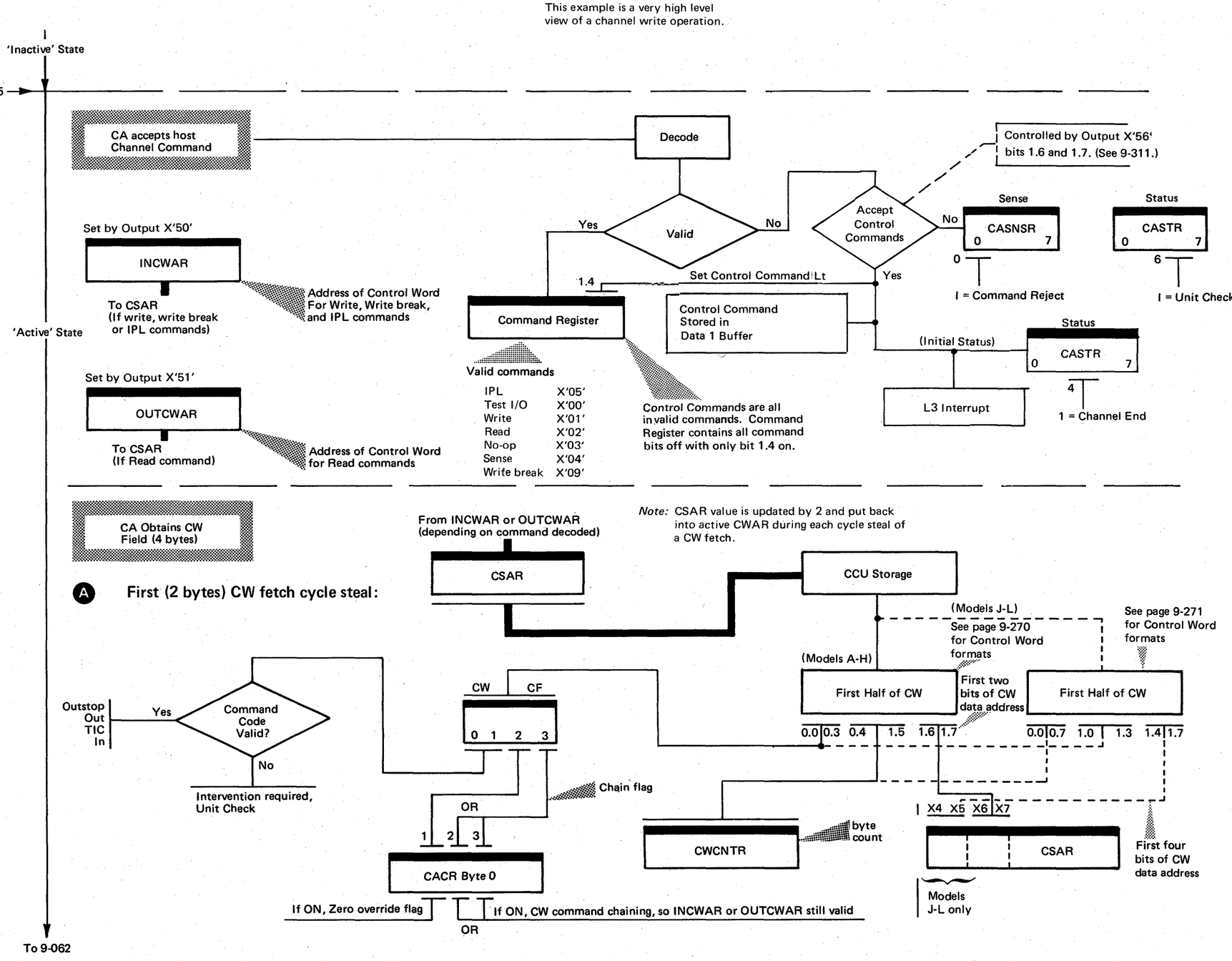
Execution of an Output X'57' with bit 1.7 on forces the type 2 CA to go offline when the required CPU transition parameter occur, ('clock out' down, etc.). Even though the control panel ENABLE DISABLE switch is in the enable position, the enable light is turned off.

All CA registers are available to the control program in this state, including the IPL portion of the channel adapter mode register. The diagnostic registers can be loaded with Output instructions X'58' and X'5B' to simulate the channel interface in this state.

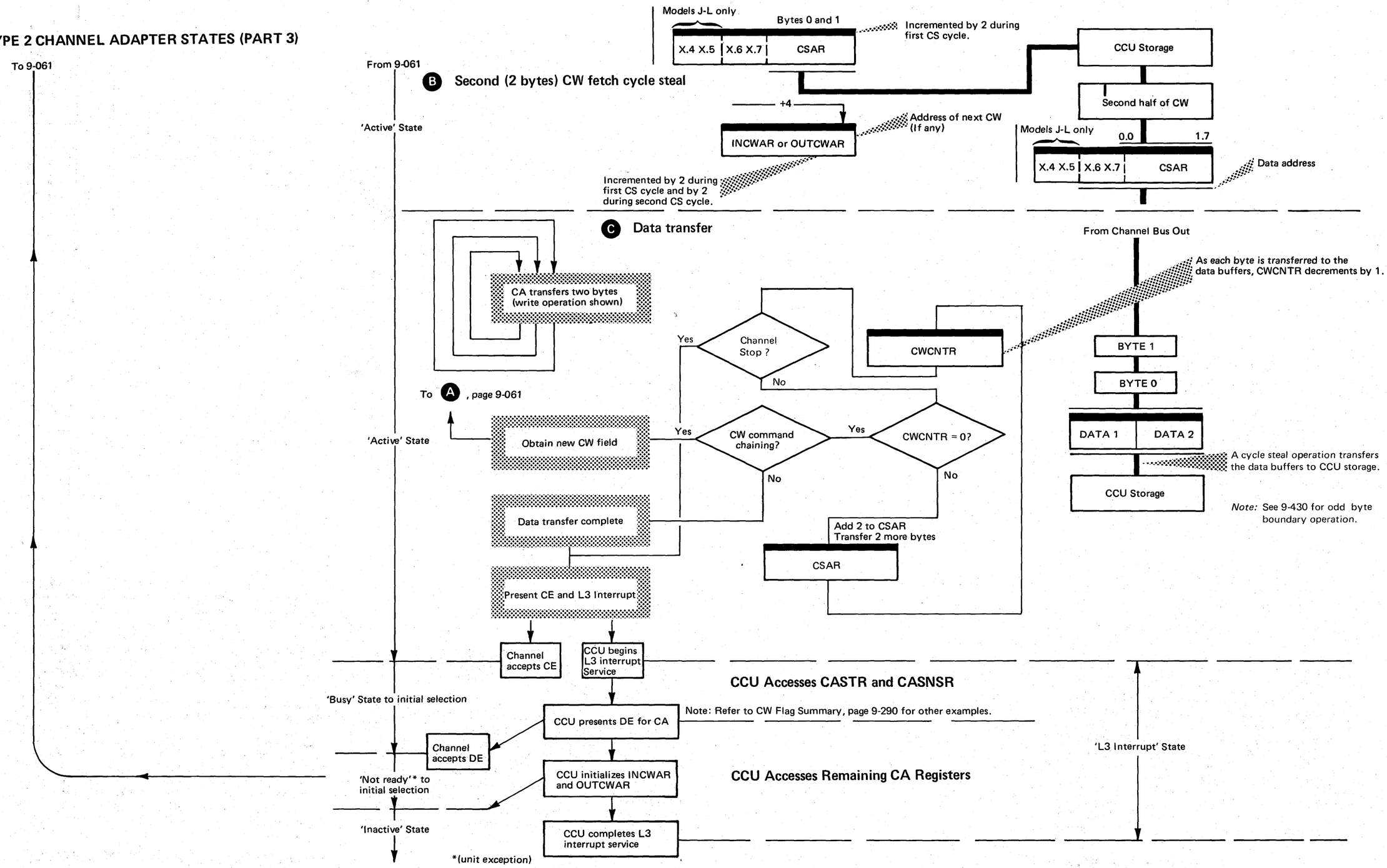
TYPE 2 CHANNEL ADAPTER STATES (PART 2)

This example is a very high level view of a channel write operation.





TYPE 2 CHANNEL ADAPTER STATES (PART 3)



CHANNEL ADAPTER INITIALIZATION

Before the 3705 control program can access the CA's external registers, it must select the CA. Only one CA can be selected at a time. The 3705 control program has access to the channel adapter mode register (CAMR) at all times, so that it can select a CA with an Output X'57'. If bit 1.4 is on in the general register specified in the instruction, CA number one is selected; if bit 1.4 is off in the general register, CA number 2 is selected.

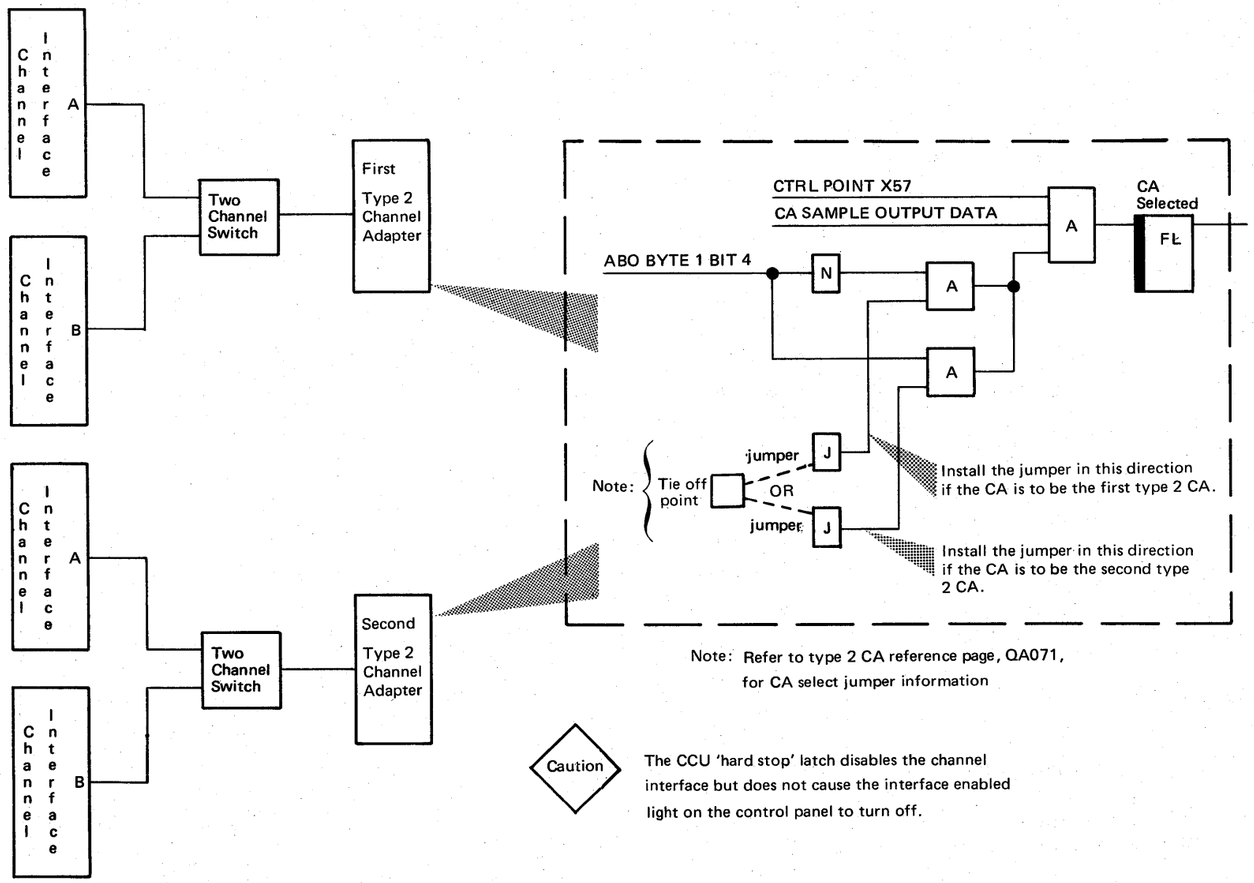
An Input X'55' transfers bit 1.6 to a CCU general register if CA number 2 is selected, and bit 1.7 if CA number 1 is selected.

Although only one CA can be selected at a time, both can transfer data across the channel simultaneously. Assuming two CAs are installed, the 3705 control program can select one of the CAs, initialize it and deselect it. Then the channel can transfer data with that CA while the 3705 control program is selecting and initializing the other CA. When both CAs are initialized, both can transfer data across their channel interfaces simultaneously.

Both interfaces can be attached to the same channel, or to different channels. The channels can be attached to the same CPU or to different CPUs. However, the CA can be enabled to only one of the interfaces at a time. See 1-050 for the interface enable procedure.

Whenever the CA is enabled to an interface and not initialized is signaled from the CCU, any channel command decode other than Write IPL causes UC status to be set in the CA status register, and not initialized sense to be set in the sense register.

The type 2 CA selection circuit is installed in each CA on the card at Z4L2 (QH001). Whether the CA is the first or second is determined by the position of the card jumper.



Note: Refer to type 2 CA reference page, QA071, for CA select jumper information

Caution

The CCU 'hard stop' latch disables the channel interface but does not cause the interface enabled light on the control panel to turn off.

CCU Not-Initialized State

The 3705 is in its Not-Initialized state until the end of IPL phase three. The Not-Initialized state remains set until 3705 control is passed from the ROS program code to the program module loaded into the 3705 with a Write IPL command. The 3705 CA must request channel service to signal the CPU that the 3705 needs a Write IPL command to become initialized.

With Device End and Unit Check status set by ROS in the CASTR, (result of entering the Not-Initialized state), the CA initiates a selection sequence to the channel. The channel should respond to the CA initiated sequence with a channel Sense command to determine why the CA needs service.

If the CA receives a Write, Write Break, or Read command while the 3705 is in the not-initialized state, bit 0.7 (Unit Exception) and bit 0.6 (Unit Check) are set on in the CASTR and returned to the channel as initial status to the command. Not-initialized (CASNSR bit 0.6) is returned in the sense byte to the channel.

When the CA decodes a Write IPL command from the channel, the CA requests a level 3 interrupt. The 3705 control program (ROS program code) loads INCWAR with the address of the control word to be used with this command. When the level 3 interrupt is ended, the CA requests two cycle-steal operations to fetch the control word, and the CA external registers are intialized to handle the command. The data transfer for the Write IPL command is completed. When final status is presented to the channel for the Write IPL command, the CA requests a level 3 interrupt to signal the CCU that the command is ended. Program control of the 3705 is passed from the ROS program to the program just loaded into the 3705. With the transfer of control, the 3705 becomes initialized, and the IPL phase 3 ends.

Before the CA can handle any other channel commands, the CA external registers must be initialized to handle them. INCWAR and OUTCWAR must be loaded with valid addresses of control words, and INCWAR Valid, and OUTCWAR Valid must be set in the CACR.

INPUT/OUTPUT INSTRUCTIONS

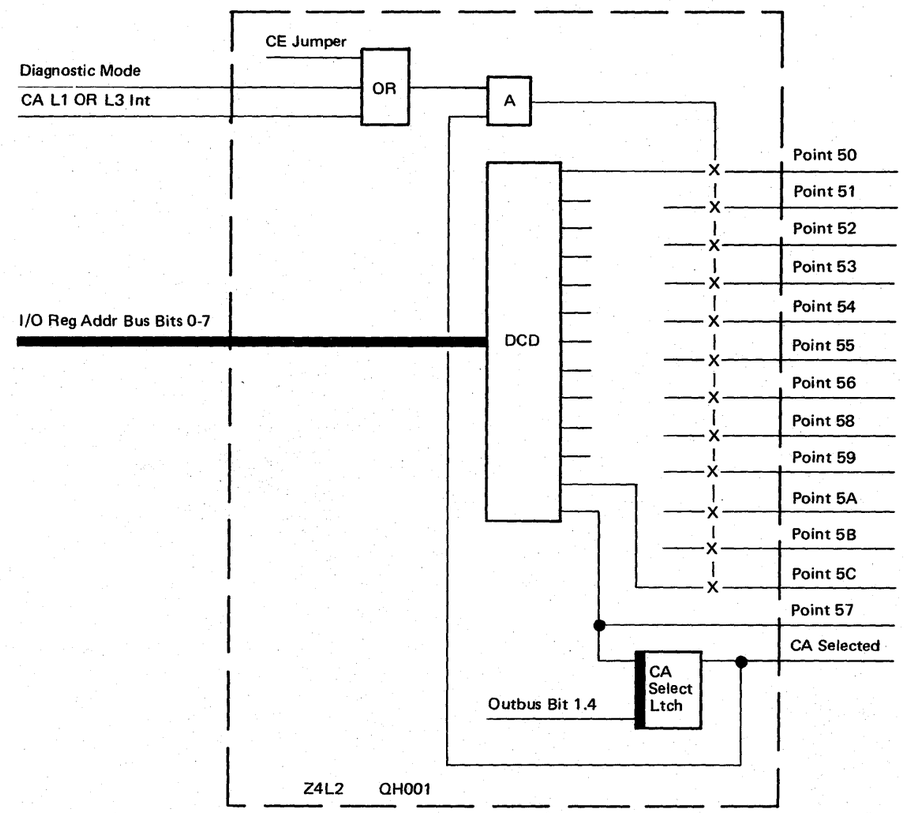
External registers X'50' through X'5F' are used to control the type 2 channel adapter. These external registers may be accessed by the control program only when the type 2 CA has been selected and one of the following conditions exists:

- The type 2 CA level 1 or level 3 'interrupt request' latch is on.
- The type 2 CA is in diagnostic wrap mode.
- A special CE aid jumper is installed from L2G12 to ground (logic page QH001).

When these conditions are satisfied, an output to registers X'52', X'59', X'5C', X'5D', X'5E', and X'5F' is ignored, and an input from registers X'57', X'5D', X'5E', and X'5F' transfers zeros to the CCU general register designated in the input instruction. When the adapter is selected and none of the other conditions necessary to access the external registers are satisfied, outputs to these registers, except X'57', are ignored. Under this condition, inputs from these external registers result in an in/out check level 1 interrupt request because of incorrect parity on the CCU Inbus.

If the adapter is not selected or not installed, an input or output to one of these registers results in an in/out check level 1 interrupt request because the adapter does not decode the register addresses.

Input instruction X'53' and X'54' are ignored if the CA is not active (not executing a channel command or control command), except for Register X'53' bits 1.4-1.7. With 3702-II Models J-L, Byte X of the CSAR (Reg X'53', bits 1.4-1.7) can be accessed.



Note: Outbus bit 1.4 must be on to select Type 2 CA number 1 and off to select type 2 CA number 2.

CONTROL PANEL ACCESS TO CA REGISTERS

Access to external registers X'50' thru X'5F' should be attempted from the 3705 console as follows:

1. Output to register X'57' to select either type 2 CA number 1 in the first frame (byte 1 bit 4 on) or type 2 number 2 CA in an expansion frame (byte 1 bit 4 off).
2. One of the following conditions must also be present:
   (a) The Type 2 CA Level 1 or Level 3 interrupt request has been set. This may be accomplished by an output to register X'57' with byte 1 bit 0 on.
   (b) The Type 2 CA's Diagnostic Mode state has been set by an output to register X'57' with byte 1 bit 7 on.
   (c) The CE aid jumper has been installed from 01A-Z4L2G12 to ground.

CAUTION

When the CE aid jumper is installed, the hardware interlocks are overriden and 3705 control panel Input/Output operations addressed to the type 2 CA may interfere with the attached CPU.

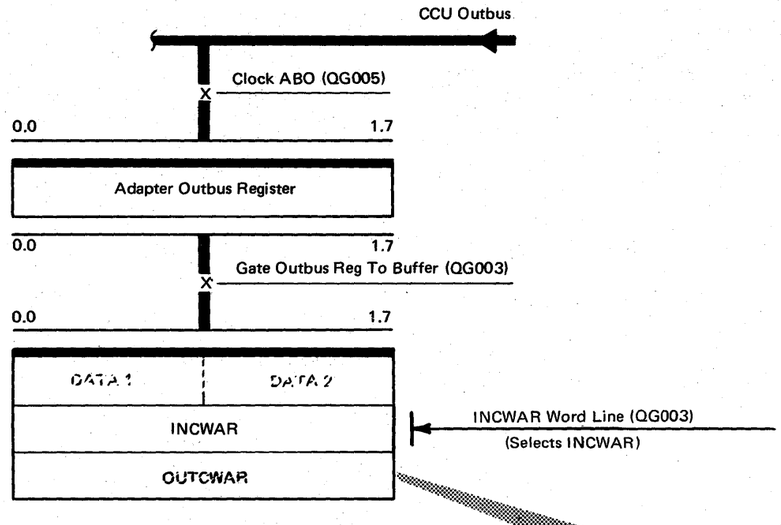
3. If one of the above listed pairs of conditions is not met, an Input from X'50' thru X'5F' displays 0000 in display B, and except for output X'57', and output to X'50' thru X'5F' is ignored. No check condition should occur.
4. If the type 2 CA is not in diagnostic mode, the CE aid jumper is not installed, the adapter is selected and has its level 1 or level 3 interrupt request pending, all type 2 CA registers except sense and status, registers X'53' and X'54', may be accessed. In this situation the adapter must also be in the active state, (executing a channel command or control command). Otherwise, an Output X'53' or X'55' is ignored and an Input X'53' or X'54' causes 0000 to be displayed in display B. No check condition should occur.

Note: With 3702-II Models J-L, an Input X'53' operation gates the CSAR Byte X bits (1.4-1.7) into display B.

OUTPUT X'50' INSTRUCTION

This instruction is used by the control program to load INCWAR (register X'50') with a valid address of an In control word. This address is used when the CA is executing a Channel Write, Write Break, or Write IPL command.

LOGIC REFERENCE: QL001 & QM001.



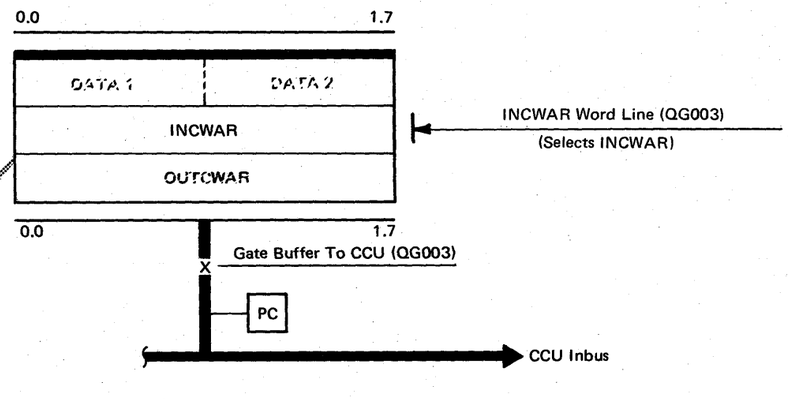
The data buffer, INCWAR, and OUTCWAR are located in the local store array on cards Z4H2 (byte 0) and Z4G2 (byte 1).

INPUT X'50' INSTRUCTION

The control program uses this instruction to transfer the contents of INCWAR into a CCU general register specified in the instruction.

If this instruction is executed before the register is loaded with an Output X'50' instruction after 3705 power is turned on, a CWAR/Data buffer parity check may occur.

LOGIC REFERENCE: QL001 & QM001.

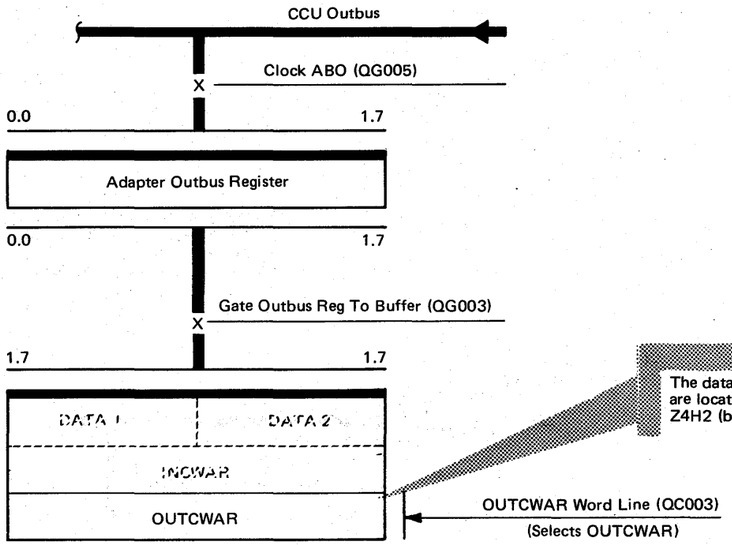


OUTPUT X'51' INSTRUCTION

The 3705 control program uses this instruction to load a valid Out CW address into OUTCWAR. This address is used when the CA is executing a channel Read command.

Because the contents of this register are unpredictable when the 3705 power is turned on, the 3705 control program should load OUTCWAR with an Output X'51' before executong an Input X'51' to prevent a possible CWAR/Data buffer parity check.

LOGIC REFERENCE QL001 & QM001.

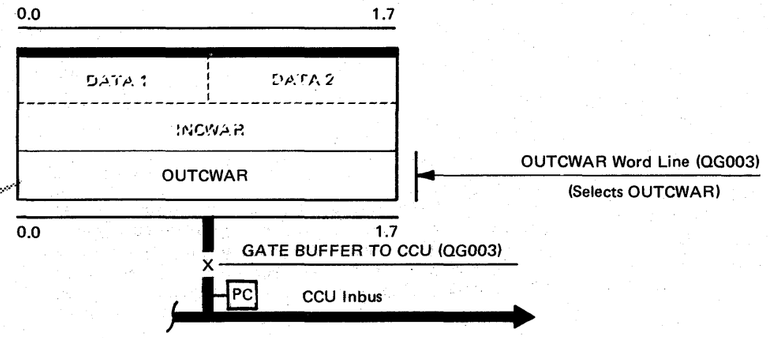


INPUT X'51' INSTRUCTION

The 3705 control program uses this instruction to transfer the contents of OUTCWAR into a CCU general register.

If this instruction is executed before the register is loaded with an Output X'51' instruction after 3705 power is turned on, a CWAR/Data buffer parity check may occur.

LOGIC REFERENCE QL001 & QM001.

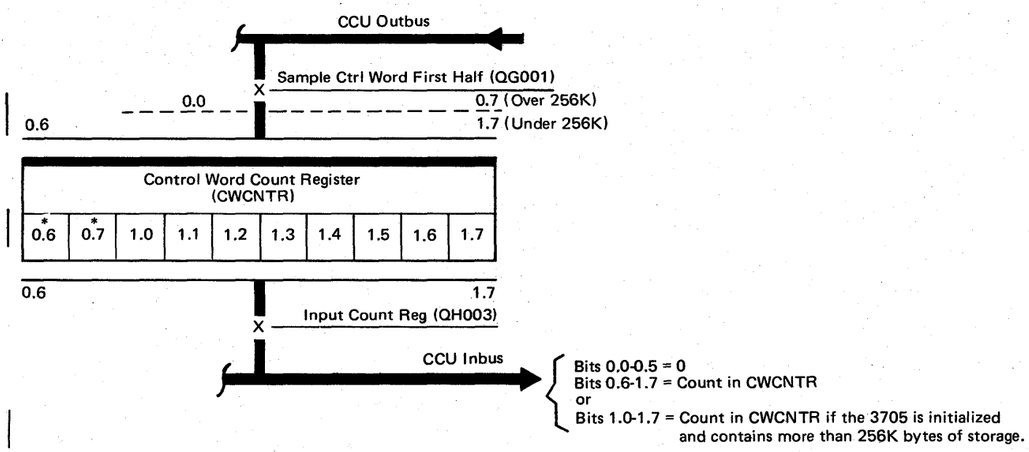


INPUT X'52' INSTRUCTION

This instruction transfers the contents of the control word byte count register (CWCNTR) into a CCU general register.

If this instruction is issued while the CA is operating in diagnostic wrap mode and the simulated channel data transfer has not ceased, a CCU Inbus parity check may occur.

LOGIC REFERENCE QH002, QH003

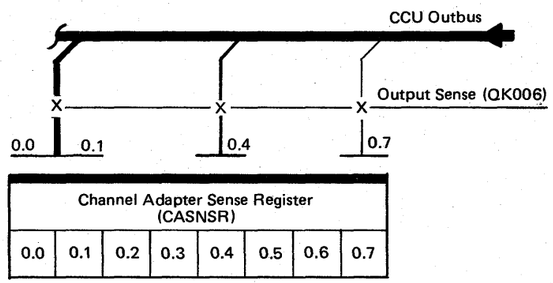


*For 3705s containing more than 256K bytes of storage, the two high-order bits are always 1 during the not initialized state. Otherwise, the bits are 0 because 3705s with more than 256K bytes of storage use an 8-bit count instead of 10.

OUTPUT X'53' INSTRUCTION

The control program can use this instruction to set bits 0.0 (Command Reject), 0.1 (Intervention Required), 0.4 (Data Check), and 0.7 (Abort) in the channel adapter sense register (CASNSR) when 'CA active' is on or if the CA is in diagnostic mode.

LOGIC REFERENCE QK003–QK008



NOTE

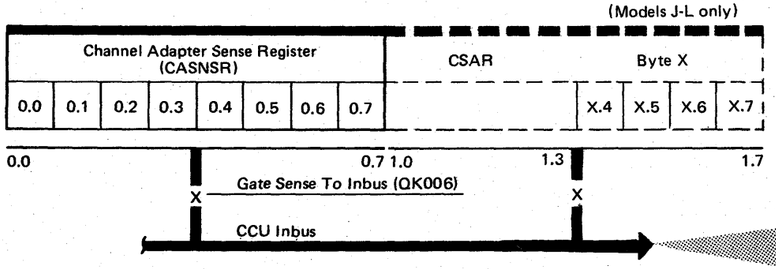
Whenever any bit is set in the channel adapter sense register, Unit Check (bit 0.6) is set in the channel adapter status register. Any data transfer that was in progress is halted.

Except for bit 0.6, the channel adapter sense register is reset during the initial selection sequence whenever the CA accepts a channel command other than Sense, Test I/O, or No-Op.

INPUT X'53' INSTRUCTION

The 3705 control program uses this instruction to transfer the contents of the channel adapter sense register (CASNSR) and Cycle Steal Address Register byte X (Models J-L only) into a CCU general register. If the instruction is executed while none of the conditions listed in *INPUT/OUTPUT INSTRUCTIONS, 9-090,* are satisfied, a CCU Inbus Parity check is caused. If the CA is not active but the CA level 1 or level 3 'interrupt request' latch is set when this instruction is executed, all zeros are transferred into the CCU general register. With 3705 Models J-L, CSAR Byte X is gated to the general register (the CA does not have to be active).

LOGIC REFERENCE QK003, QK008, QR001



NOTE

Whenever any bit is set in the channel adapter sense register, Unit Check (bit 0.6) is set in the channel adapter status register. Any data transfer that was in progress is halted.

Except for bit 0.6 and bits 1.4-1.7, the channel adapter sense register is reset during the initial selection sequence whenever the CA accepts a channel command other than Sense, Test I/O, or No-Op.

Bit 0.0—Command Reject.
Command reject is set whenever an invalid command with proper parity is decoded by the CA during initial selection and the CA is not in the active state.

The 3705 control program can set this bit during a level 3 interrupt by executing Output X'53' with bit 0.0 set to a 1.

Bit 0.1—Intervention Required.
This bit indicates programming errors were detected by either the CCU, the CA hardware, or the control program. The bit is set under hardware control when any of the following occur:

- The CCU hardstop latch is set when the CA is transferring data either across the channel interface or on the CCU Inbus or Outbus.
- An address used by the CA for a cycle-steal operation caused a CCU address exception or protection check. This also sets bit 0.2 in the channel adapter control register.
- A TIC or chain to a CW address above 64K was detected during a CW fetch cycle-steal operation. This also sets bit 0.0 in the CA control register.
- During a CW fetch cycle-steal operation, (1) an Out or Out Stop CW was decoded when executing a channel Write, Write Break, or Write IPL command, (2) an In CW is decoded for a channel Read command or (3) an In, Out, or Out Stop CW is decoded with a count of zero. This also causes bit 0.1 to be set in the CA control register.

  Additional indications may be conveyed to the host CPU program if this bit is set by the 3705 control program issuing an Output instruction X'54' with bit 0.1 on.

Bit 0.2—Bus-Out Check.
This bit indicates a parity check was detected on the I/O channel Bus-Out during the initial selection command byte transfer or during a host processor to 3705 data transfer. The 3705 control program cannot set this bit.

Bit 0.3—Equipment Check.
This bit is set any time the type 2 channel adapter detects an internal hardware check or a parity check is detected by:

- The type 2 channel adapter on Outbus for an output instruction or data/CW fetch cycle-steal operation.
- CCU on Inbus for a data store cycle-steal operation.
- CCU on Adbus during a cycle-steal operation.
- The type 2 channel adapter during an Input X'50', X'51', or X'5A' instruction when data containing bad parity is read from the CWAR/Data Buffer.
- The type 2 channel adapter during a channel data transfer when data, address, sense, or status containing bad parity is sent to the channel Bus-In.
- The type 2 channel adapter whenever the Bus-Out check sense bit is on.

Bit 0.4—Data Check.
The 3705 control program can set this bit during a level three interrupt with 'CA active' on (or if the CA is in diagnostic mode) by executing Output X'53' with bit 0.4 set to a 1.

Bit 0.5—Not used by the 3705 type 2 channel adapter.

Bit 0.6—Not Initialized.
The ROS program sets this bit by executing an Output X'57' (with bit 0.7 set to a 1) when the 3705 is not initialized or when in diagnostic mode. CA hardware sets this bit whenever a Read, Write, or Write Break channel command is decoded and the 3705 is not initialized. The ROS program resets this bit by executing an Output X'77' with bit 0.0 set to a 1.

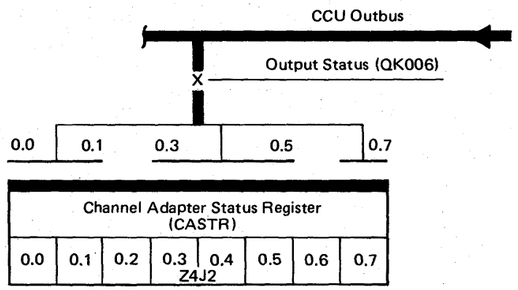
Bit 0.7—Abort.
Abort indicates to the host processor that the 3705 control program has halted its channel operation abnormally.

Bit 1.0-1.3 = zero				
Bit 1.4	CSAR	Byte X,	Bit 4	Models J-L only
Bit 1.5	CSAR	Byte X,	Bit 5	
Bit 1.6	CSAR	Byte X,	Bit 6	
Bit 1.7	CSAR	Byte X,	Bit 7	

OUTPUT X'54' INSTRUCTION

The 3705 control program uses this instruction to load the channel adapter status register (CASTR) with the correct ending status for a channel command. If the CA is not in the active state, and the CA level 1 or level 3 'interrupt request' latch is set, this instruction is ignored.

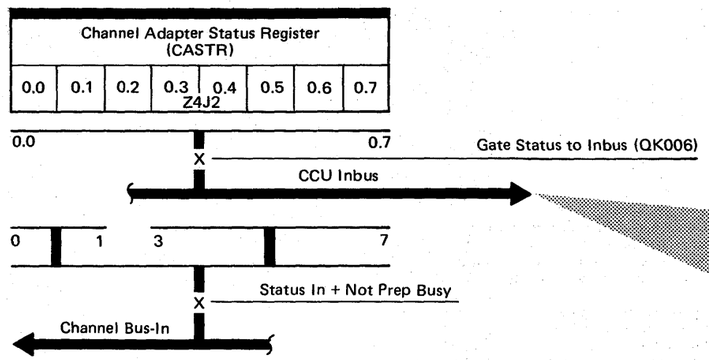
LOGIC REFERENCE QK001, QK002



INPUT X'54' INSTRUCTION

The 3705 control program uses this instruction to transfer the contents of the channel adapter status register (CASTR) into a CCU general register. If the instruction is executed while none of the conditions listed in *INPUT/OUTPUT INSTRUCTIONS, 9-090,* are satisfied, a CCU Inbus parity check is caused. If the CA is not active but the CA level 1 or level 3 'interrupt request' latch is set when this instruction is executed, all zeros are transferred into the CCU general register.

LOGIC REFERENCE QK001, QK002



DEFINITION OF STATUS REGISTER BITS TRANSFERRED TO CCU

Bit 0.0—Attention.
This bit indicates that the 3705 requires service from the channel. The 3705 control program can set this bit directly with an Output X'54' instruction and indirectly with an Output X'55' to set bit 0.6 in CACR. The Output X'55' should be executed after an Output X'57' has requested a CA level 3 interrupt.

Bit 0.1—Status Modifier.
Status modifier is presented only with ending status and should convey to the host processor a unique indication for the particular command being executed.

Bit 0.2—Not used by the type 2 channel adapter.

Bit 0.3—Busy.
This bit is presented as initial status to all host processor channel commands except Test I/O if the adapter has its level 1 or level 3 interrupt request set, or if initial selection is attempted before Device End status is presented to the host for the channel command currently being executed, then busy status is presented to all host processor channel commands except Test I/O.

Bit 0.4—Channel End.
Channel End (CE) indicates that the 3705 has completed the data transfer portion of the channel command in progress. Channel End may be set by Output instruction X'54' when the adapter interrupt and active states exist and CE has not already been presented to the channel for the command being executed. CA hardware can set this bit for each channel I/O command.

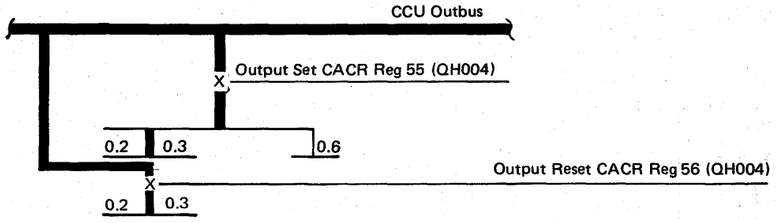
Bit 0.5—Device End.
Device End (DE) indicates that the 3705 is finished with the current host processor channel command and is ready to accept another command from the channel. Channel End and Device End are not always presented together. When CE and DE are presented separately, the CA requests a level 3 interrupt after CE is accepted by the channel. DE is presented to the channel, if set with an Output X'54' instruction, along with any other status set by the 3705 control program whenever the level 3 request is reset.

Bit 0.6—Unit Check.
Unit Check (UC) indicates that an abnormal condition exists, and more information on the condition is contained in the sense byte. Type 2 CA hardware sets UC when any of the sense register bits are set. When the CCU is in the not initialized state, UC is returned as initial status to Write, Read, and Write Break channel commands.

Bit 0.7—Unit Exception.
Unit Exception (UE) indicates in the initial status to the channel that the 3705 control program has not set up a control word to handle the particular command. UE can be presented to the channel with DE. Whenever UE is presented with DE, the intent is to break host processor channel command chaining, when the 3705 no longer needs service, without going through another selection sequence.

OUTPUT X'55' AND OUTPUT X'56' INSTRUCTIONS

The Output X'55' instruction allows the 3705 control program to set bits 0.2, 0.3, and 0.6 in the channel adapter control register (CACR). Output X'56' permits the 3705 control program to reset bits 0.2 and 0.3 in the CACR. The 3705 control program must use the Output X'56' instruction with bit 1.7 on to activate the CA to accept control commands (invalid commands). It must use Output X'56' with bit 1.6 on to reject control commands. (See 9-311)



Channel Adapter Control Register (CACR)															
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

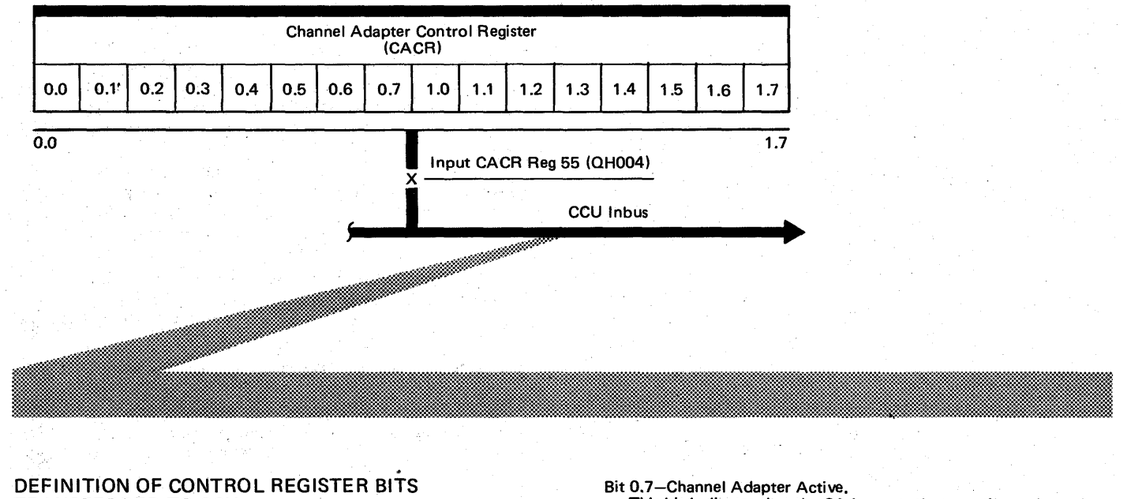
LOGIC REFERENCE

CACR is not located on one MST card. The bits are located on the cards indicated in the chart and can be found on the referenced logic page.

Bit	Card loc.	Logic Page
0.0	Z4L2	QH006
0.1	Z4L2	QH005
0.2	Z4L2	QH005
0.3	Z4L2	QH005
0.4	Z4K2	QJ002
0.5	Z4K2	QJ002
0.6	Z4J2	QH005
0.7	Z4F2	QN004
1.0	Z4N2	QF004
1.1	Z4K2	QJ002
1.2	Z4N2	QF004
1.3	Z4N2	QF005
1.4	------	----------
1.5	Z4K2	QJ002
1.6	Z4L2	QH006
1.7	Z4L2	QH006

INPUT X'55' INSTRUCTION

The 3705 control program uses this instruction to transfer the contents of the CACR into a CCU general register.



DEFINITION OF CONTROL REGISTER BITS TRANSFERRED TO CCU

Bit 0.0—Diagnostic Wrap Mode.
This bit indicates that an Output X'57' instruction has been executed and has set bit 1.7 on in the channel adapter mode register. The channel adapter has gone offline to the attached channel interface.

Bit 0.1—Zero Count Override.
This bit indicates the condition of the zero count override flag in the control word just executed.

Bit 0.2—INCWAR Valid.
This bit indicates that the CWAR for inbound data transfer contains a valid address. The address must be smaller than 64K.

Bit 0.3—OUTCWAR Valid.
This bit indicates that the CWAR for outbound data transfers contains a valid address. The address must be smaller than 64K.

Bit 0.4—Program Requested Level 3 Interrupt.
This bit indicates that the control program has initiated an adapter level 3 interrupt with Output instruction X'57' setting bit 1.0 on in the channel adapter mode register.

Bit 0.5—Program Requested Abort/Level 3 Interrupt.
This bit indicates that the CA level 3 interrupt was requested by the control program while the CA was transferring data across the channel interface.

Bit 0.6—Program Requested Attention.
This bit is set by Output instruction X'55' (indirectly) and causes Attention status to be presented to the channel.

Bit 0.7—Channel Adapter Active.
This bit indicates that the CA is currently executing a channel command for which DE status has not been presented to the channel.

Bit 1.0—I/O Command Chaining.
This bit indicates that Suppress-Out was up when the channel accepted the ending status from the adapter.

Bit 1.1—I/O Write Break Command Remember.
This bit indicates that a channel Write Break command (X'09') was decoded by the CA and that the channel has not accepted ending status for the Write Break Point command.

Bit 1.2—Channel Stop/Interface Disconnect.
This bit indicates that a channel stop or interface disconnect sequence is detected on the channel interface.

Bit 1.3—Selective/System Reset.
This bit indicates that a system or selective reset indication was received on the channel interface.

Bit 1.4—Not used by the channel adapter.

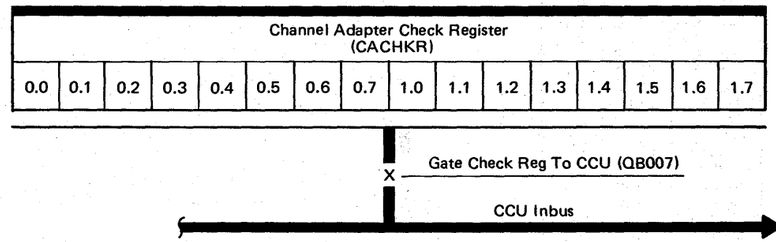
Bit 1.5—Channel Read Command Remembrance.
This bit indicates that a channel Read command was decoded by the CA, and that the channel has not accepted ending status for the Read command.

Bit 1.6—Type 2 Channel Adapter 2 Selected.
This bit indicates that the second type 2 channel adapter located in the first 3705 expansion frame has been selected.

Bit 1.7—Type 2 Channel Adapter 1 Selected.
This bit indicates that the first type 2 channel adapter located in the basic 3705 frame was selected.

INPUT X'56' INSTRUCTION

Input X'56' transfers the contents of the channel adapter check register (CACHKR) into a CCU general register. The 3705 control program uses this instruction to determine the cause of a type 2 channel adapter error interrupt (9-500).



LOGIC REFERENCE

CACHKR is not located on one MST card. The bits are located on the cards referred to in the chart.

Bit	Card Loc.	Logic Page
0.0	Z4F2	QN002
0.1	Z4F2	QN002
0.2	Z4F2	QN002
0.3	Z4F2	QN001
0.4	Z4F2	QN001
0.5	Z4F2	QN001
0.6	Z4J2	QK004
1.4	Z4Q2	QB007
1.5	Z4S2	QD007

CHANNEL ADAPTER CHECK REGISTER BITS TRANSFERRED TO THE CCU

Bit 0.0—Invalid CWAR Address.
This bit indicates that the address contained in the CWAR for the current channel command is greater than 64K.

Bit 0.1—Invalid Control Word Format.
This bit indicates that:

- An Out or Out-Stop Control Word was fetched for a channel Write, Write Break, or Write IPL command.
- An In Control Word was fetched for a channel Read command.
- An In, Out, or Out Stop control word was fetched that contained a byte count of zero.

Bit 0.2—Cycle Steal Address Check.
This bit indicates that the cycle-steal address is beyond the capacity of storage available or that the address is out of parity. It also indicates the address is in a protected area of storage.

Bit 0.3—CWAR/Data Buffer Check.
This bit indicates that either the INCWAR, OUTCWAR, Data 0, or Data 1 register contained incorrect parity when its contents were transferred to the CCU. This also indicates that the data transferred to the channel during a channel Read command was out of parity.

Bit 0.4—CCU Outbus Check.
This bit indicates that the halfword on the CCU Outbus was out of parity.

Bit 0.5—CCU Inbus Check.
This bit indicates that the halfword on the CCU Inbus was out of parity.

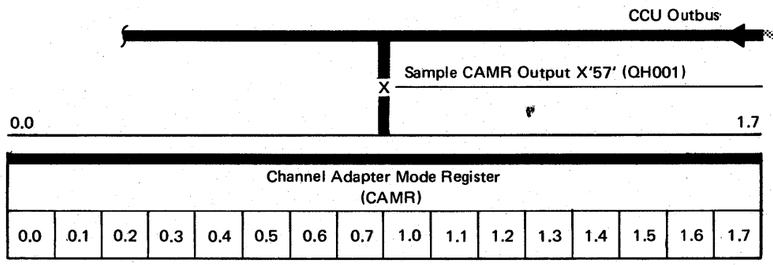
Bit 0.6—Channel Bus-Out Check.
This bit indicates that the address, command, or data byte transferred from the channel to the CA was out of parity.

Bit 1.4—Channel Bus-In Check Interface A.
This bit indicates that the address, status, sense, or data byte presented to channel interface A was out of parity. The most probable cause of this error is a failing channel driver card located in socket Q2.

Bit 1.5—Channel Bus-In Check Interface B.
This bit indicates that the address, status, sense, or data byte presented to channel interface B was out of parity. The most probable cause of this error is a failing channel driver card located in socket S2.

OUTPUT X'57' INSTRUCTION

This instruction permits the 3705 control program to load the channel adapter mode register (CAMR).



LOGIC REFERENCE

CAMR is not located on one MST card. The bits are located on the cards indicated in the chart and can be found on the referenced logic page.

Bit	Card Loc.	Logic Page
0.0	Z4J2	QK008
0.1	Z4J2	QK008
0.2	-------	----------
0.3	Z4J2	QK008
0.4	Z4J2	QK008
0.5	-------	----------
0.6	-------	----------
0.7	Z4J2	QK008
1.0	Z4K2	QJ002
1.1	Z4K2	QJ002
1.2	Z4K2	QJ001
1.3	Z4K2	QJ001
1.4	Z4L2	QH001
1.5	Z4N2	QF006
1.6	Z4N2	QF006
1.7	Z4L2	QH006

DEFINITIONS OF BITS TRANSFERRED TO THE CA MODE REGISTER

Bit 0.0—Set IPL Prep Attention (Models A-H without E.C. 318882). This bit causes the channel adapter 'Attention status' latch to set when the adapter hardware determines that the channel is not examining the status register. (See Note.)

Bit 0.0—Set Sense Unit Exception Latch (Models A-H with E.C. 318882 or Models J-L). With Bit 0.0 set to 1, a Sense Command ends with CE, DE, and UE final status (*after* the sense byte transfer). The Sense Unit Exception Latch cannot be set unless the 3705 is in the initialized state (IPL Phase 3 reset). The latch resets automatically if the 3705 enters the not initialized state. The IPL Unit Exception Latch, if set by Output X'57', bit 0.6, overrides the Sense Unit Exception Latch.

Bit 0.1—Set IPL Prep Channel End. (See Note.)
This bit causes the channel adapter 'Channel End status' latch to set when the adapter hardware determines that the channel is not examining the status register and the 'CE remembrance' latch is not on.

Bit 0.3—Set Device End.
This bit causes the channel adapter 'Device End status' latch to set when the adapter hardware determines that the channel is not examining the status register.

Bit 0.4—Set IPL Prep Unit Check. (See Note.)
This bit causes the channel adapter 'Unit Check status' latch to set when the adapter hardware determines that the channel is not examining the status register.

Bit 0.5—Reset Sense Unit Exception Latch. In diagnostic mode only, setting this bit to "1" resets the Sense Unit Exception Latch.

Bit 0.6=1—Set Unit Exception initial status to Sense command. This bit causes Unit Exception initial status to be returned to the CPU when the channel attempts to execute a Sense command. Its intended function is to signal that an IPL is currently in progress on the other 3705 channel adapter. (See Note.)

0.6=0—Reset IPL Unit Exception Latch. (Note for Bit 0.6=1 is not applicable when Bit 0.6=0.)

Bit 0.7—Set IPL Prep Not Initialized. (See Note.)
This bit causes the channel adapter Not Initialized sense bit to set when the channel is not executing a channel Sense command.

Bit 1.0—Set Program Requested Level 3 Interrupt.
This bit causes the channel adapter to request a level 3 interrupt when:

- The adapter is in the inactive state, with no outstanding status and no channel chaining indicated.
- The adapter is active, and the CCU is not in the initialized state.

Note: This bit is ignored unless the channel adapter is in diagnostic mode, or the 3705 is in IPL Phase 3 (not initialized).

Bit 1.1—Set Program Abort.
This bit causes the channel adapter to give a level 3 interrupt whether a channel operation is in progress or not:

- If a channel operation is in progress with a Write, Write Break, Write IPL, or Read command, the command is terminated with the CE, DE, UC, and Abort sense. Once the status is accepted, a level 3 interrupt is requested.
- If some other channel operation is in progress, the level 3 interrupt is requested after the operation has completed.
- If no channel operation is in progress, the level 3 interrupt is requested immediately.

Program Abort is reset when the level 3 interrupt request is reset.

Bit 1.2—Reset type 2 channel adapter level 1 interrupt Request.
This bit resets the channel adapter level 1 'interrupt request' latch.

Bit 1.3—Reset type 2 channel adapter level 3 interrupt Request.
This bit resets the channel adapter level 3 'interrupt request' latch.

Bit 1.4—Select type 2 channel adapter 1 or 2.
If this bit is set to "1", CA 1 is selected, and if set to "0", CA 2 is selected. The control program must ensure that this bit is correct before any output X'57' instruction is issued, or the intended adapter may be deselected.

Bit 1.5—Reset Selective System Reset.
This bit resets the selective/system reset condition received by the channel interface. This bit must be reset in order to reset the level 3 interrupt requested by the selective/system reset.

Bit 1.6—Reset Channel Stop/Interface Disconnect.
This bit resets the channel stop/interface disconnect received from the channel interface. This bit must be set in order to reset the level 3 interrupt requested by the channel stop/interface disconnect.

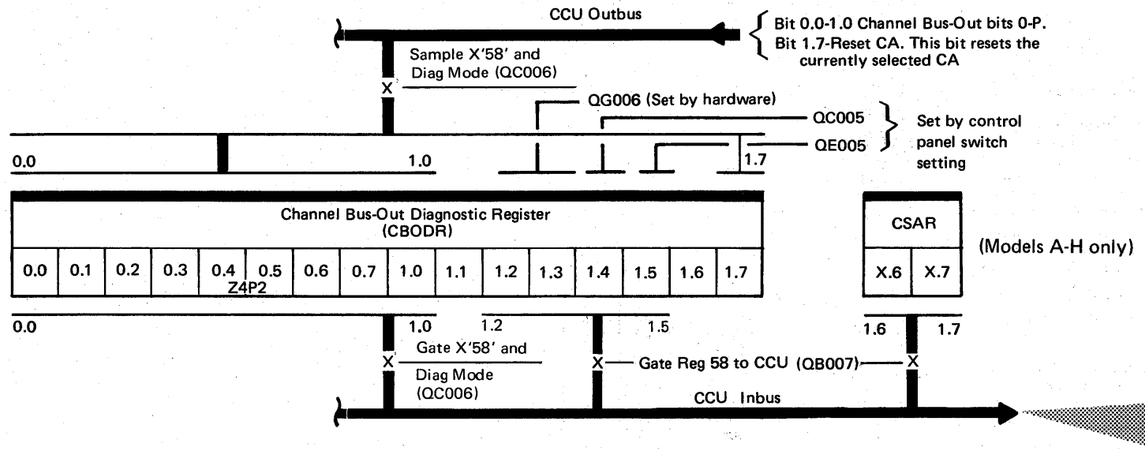
Bit 1.7—Set/Reset Diagnostic Wrap Mode.
If this bit is set on, the CA is forced offline to its attached channel interface. Setting this bit to the off condition allows the CA to go back online.

CA2

OUTPUT X'58' INSTRUCTION

This instruction permits the 3705 control program to load the channel bus out diagnostic register (CBODR) when in diagnostic mode. With this instruction and the Input X'58' instruction, the control program can simulate channel bus operations.

LOGIC REFERENCE QC001, 002, 003, 004



INPUT X'58' INSTRUCTION

This instruction permits the 3705 control program to transfer the contents of the CBODR and CSAR bits X.6 and X.7 to a CCU general register when in diagnostic wrap mode. If the 3705 control program issues this instruction when the CA is not in diagnostic wrap mode, only bits 1.2 – 1.7 are transferred to the CCU. With 3705-II Models J-L, bits 1.6 and 1.7 are always zero.

CBODR BIT DEFINITIONS TRANSFERRED TO CCU

Bits 0.0-0.7 Channel Bus Out bits 0–7.

Bit 1.0—Channel Bus Out Parity.
This bit is used to check the parity error detection circuitry.

Bit 1.2—Transfer byte 1.
This bit cannot be set by output instructions. It indicates to the input instruction that the CA is transferring an odd byte across the channel.

Bit 1.3—Transfer byte 2.
This bit cannot be set by output instructions. It indicates to the input instruction that the CA is transferring an even byte across the channel.

Bit 1.4- Type 2 Channel Adapter Interface A Enabled and not Diag mode. This bit indicates that the channel adapter is currently enabled on interface A and not in diagnostic mode.

Bit 1.5- Type 2 Channel Adapter Interface B Enabled and not Diag mode. This bit indicates that the channel adapter is currently enabled on interface B and not in diagnostic mode.

| Bit 1.6—CSAR bit X.6. (Note)

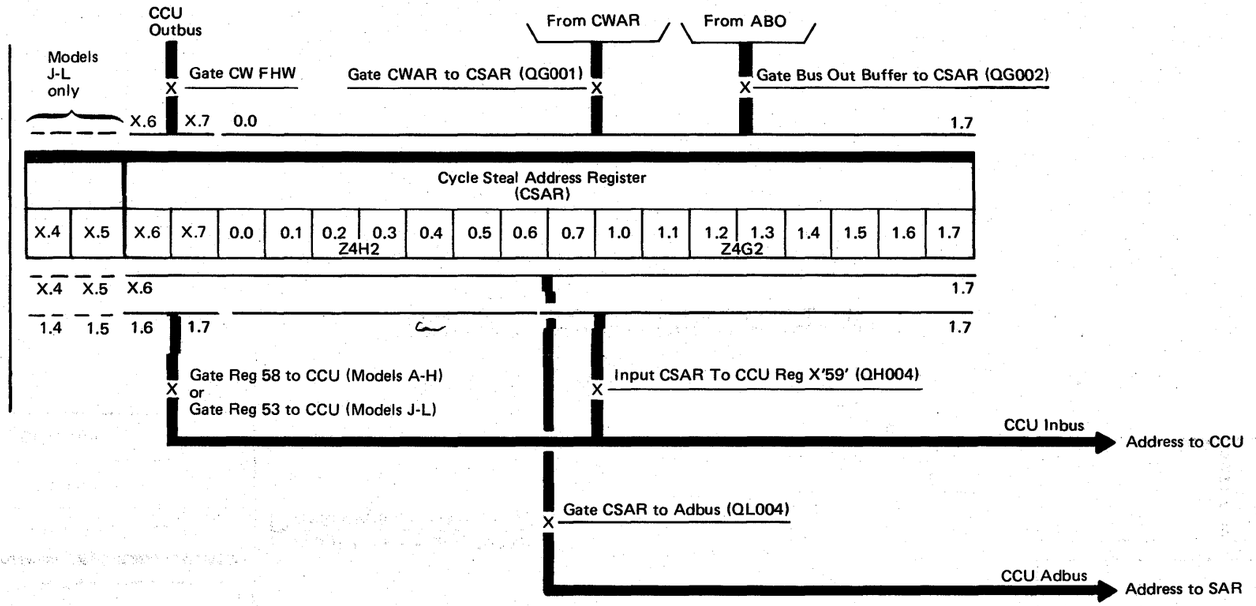
Bit 1.7—CSAR bit X.7 during input. During Output X'58' this bit resets the selected CA. (Note)

| Note: Bits are zero for Models J-L only.

INPUT X'59' INSTRUCTION

The instruction transfers the contents of the cycle-steal address register (CSAR), bytes 0 and 1, into a CCU general register. This instruction is used mainly for diagnostic purposes.

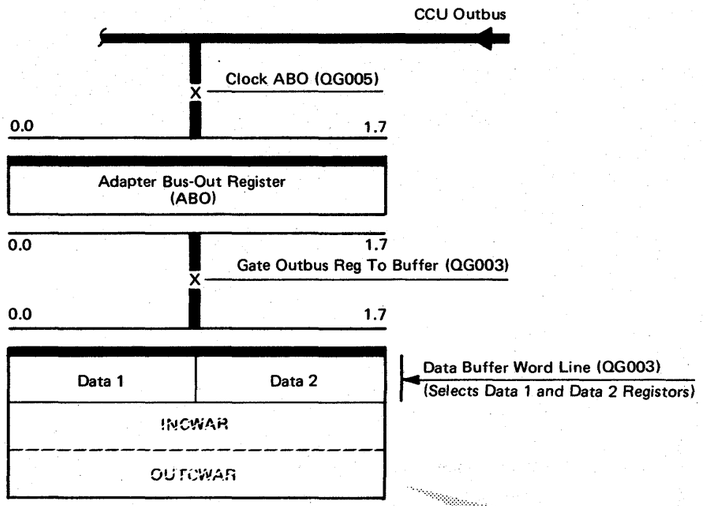
LOGIC REFERENCE QL004, 005, QM004, 005



OUTPUT X'5A' INSTRUCTION

The 3705 control program uses this instruction to load the data 1 and data 2 buffer. This instruction is used mainly for diagnostic purposes.

LOGIC REFERENCE: QL001 & QM001.



The data buffer, INCWAR, and OUTCWAR are located in the local store array on cards Z4H2 (byte 0) and Z4G2 (byte 1).

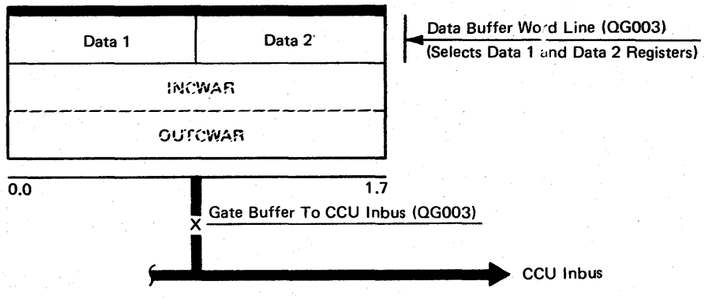
INPUT X'5A' INSTRUCTION

The control program uses this instruction to transfer the contents of data 1 and data 2 into a CCU general register.

During initial selection when the CA accepts a channel command (invalid command), the CA loads the control command byte into data 1 buffer. The 3705 control program uses Input X'5A' to transfer this control command byte to a CCU general register for control program use.

This instruction is also used for diagnostic purposes.

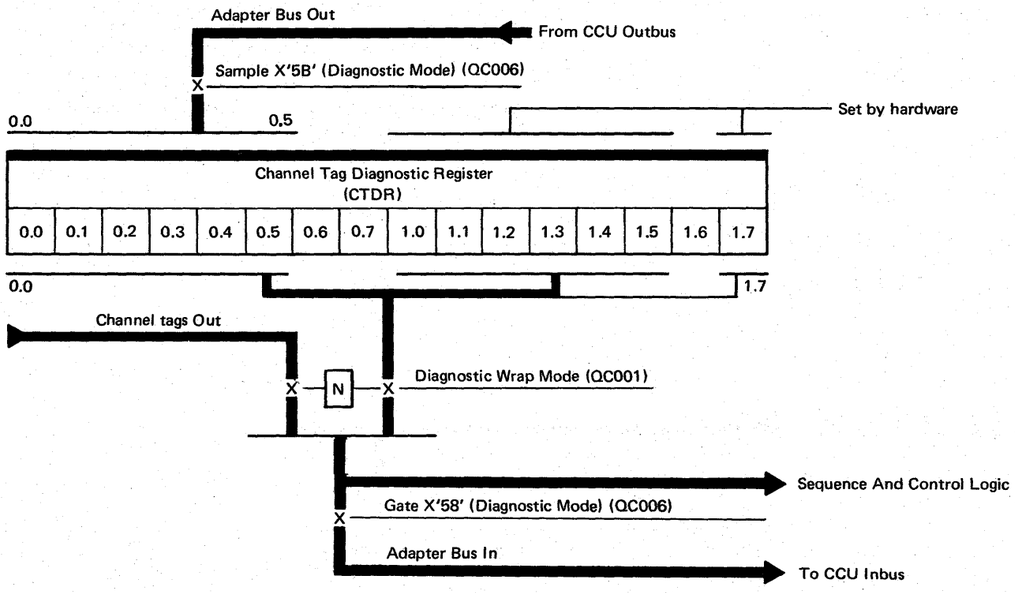
LOGIC REFERENCE: QL001 & QM001.



OUTPUT X'5B' INSTRUCTION

The Output X'5B' instruction, when in diagnostic mode, loads byte 0 of the channel tag diagnostic register (CTDR), and is used for diagnostic purposes to simulate channel tag out conditions. When the CA is in diagnostic wrap mode, the various channel tag out lines can be simulated for the channel adapter. Using the Input and Output X'58' and X'5B' instructions, the diagnostic program can simulate any channel sequence.

LOGIC REFERENCE QC003, 004



INPUT X'5B' INSTRUCTION

The Input X'5B' instruction transfers to a CCU general register the contents of the channel tag diagnostic register if the CA is in diagnostic mode.

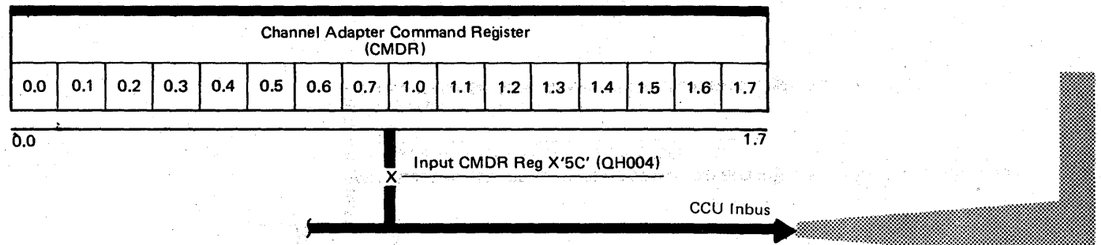
This instruction is used for diagnostic purposes.

The bits transferred by the Input and Output X'5B' are defined below. Output X'5B' only transfers byte 0.

Byte 0	Bit 0	Select-Out/Hold-Out (inbound)
	Bit 1	Address-Out
	Bit 2	Command-Out
	Bit 3	Service-Out
	Bit 4	Operational-Out
	Bit 5	Suppress-Out
	Bit 6	0
	Bit 7	0
Byte 1	Bit 0	Select-Out (outbound)
	Bit 1	Request-In
	Bit 2	Operational-In
	Bit 3	Address-In
	Bit 4	Status-In
	Bit 5	Service-In
	Bit 6	0
	Bit 7	Generate Busy

INPUT X'5C' INSTRUCTION

The 3705 control program uses this instruction to transfer the contents of the channel adapter command register into a CCU general register.



LOGIC REFERENCE

Bit	Card	Logic page	Line name
0.0	Z4K2	QJ003	Channel Test I/O
0.1		QJ003	Channel Write command
0.2		QJ003	Channel Read command
0.3		QJ003	Channel No-Op command
0.4		QJ003	Channel Sense command
0.5	--------		--------
0.6	Z4K2	QJ003	Channel Write command
0.7	--------		--------
1.0	Z4L2	QH005	Out Ctrl Wd.
1.1		QH005	Out Stop Ctrl Wd.
1.2		QH005	In Ctrl Wd.
1.3		QH005	TIC CW
1.4	Z4K2	QJ006	Channel Control Command
1.5	--------		
1.6	--------		
1.7	Z4K2	QJ003	Channel Write IPL command

Notes:

- The Test I/O command is set into the command register (CMDR) without resetting the previous command.
- The 3705 control program determines that a control command (invalid command) was issued by the channel by the fact that bit 1.4 is on when none of the command bits are on in Register X'5C'. (See 9-311 for the control command operation.)

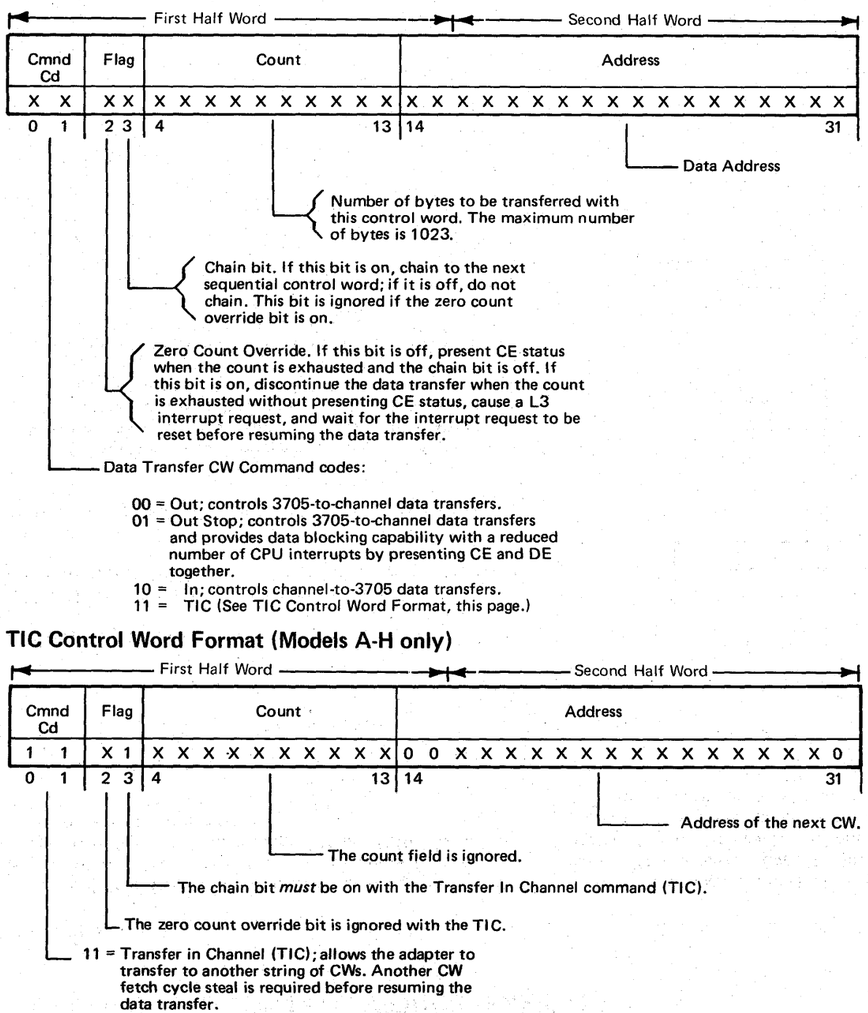
CYCLE STEAL CONTROL WORDS

A four-byte control word (CW) controls cycle-steal operations during Write, Write Break, Write IPL, and Read channel I/O commands. The control program builds the control words according to the operation to be performed. The control words reside in storage until changed or overlaid by the control program or a cycle steal operation.

The address of the CW is loaded into either INCWAR or OUTCWAR depending upon the channel command being executed. If the address is greater than 64K, or the CW at the address is incorrect for the command, a CA level 1 interrupt is requested so that the control program can correct the situation.

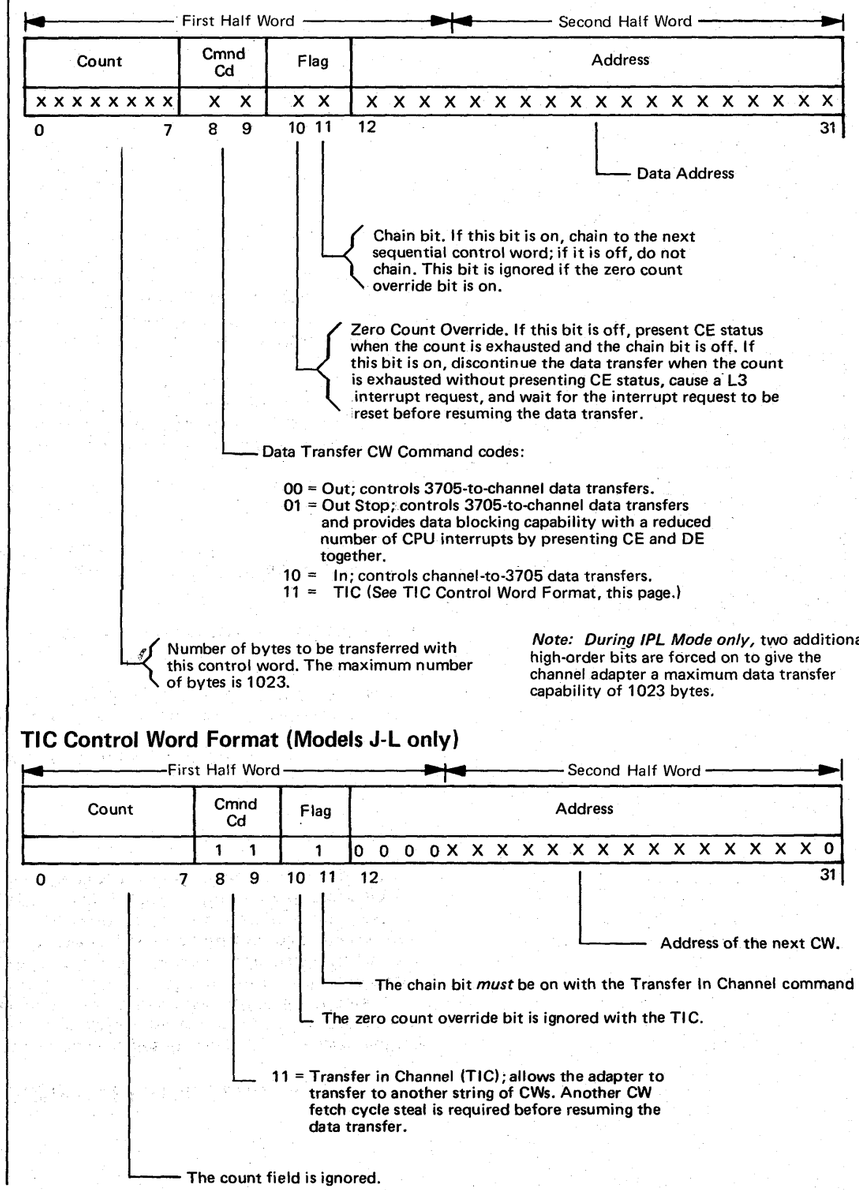
CW FORMATS (Models A-H only)

In, Out, and Out Stop



TIC Control Word Format (Models A-H only)

CW FORMATS (Models J-L only)



Note: ***During IPL Mode only,*** two additional high-order bits are forced on to give the channel adapter a maximum data transfer capability of 1023 bytes.

TIC Control Word Format (Models J-L only)

CYCLE STEAL CONTROL WORDS (PART 2)

CHAIN FLAG

The CW chain flag causes immediate chaining to the next sequential CW when the byte count decrements to zero and the CA is executing a channel Read, Write, Write IPL, or Write Break command.

When the count decrements to zero, the chain flag causes the appropriate CWAR valid latch to remain set during the CW fetch cycle-steal operation. No status is presented to the channel until the chain is broken, or a channel stop sequence is detected by the CA hardware.

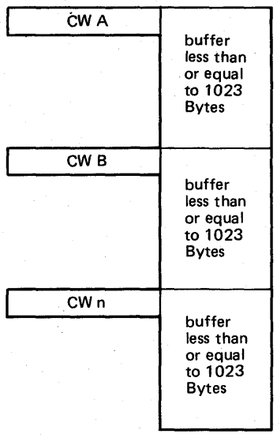
Chain Operation:

The 3705 control program loads the CW address into the appropriate CWAR with an Output X'50' or X'51' instruction.

The CA decodes the channel command and fetches control word A.

The CA transfers data between the channel and the 3705. When the byte count decrements to zero, the CA fetches the control word B without presenting status or requesting a level 3 interrupt.

Chaining ends when the chain is broken by a CW without the chain flag or a channel stop sequence.



ZERO COUNT OVERRIDE FLAG

Zero count override enables the adapter to transfer multiple buffers under a single host processor channel command with a minimum number of buffers assigned to the adapter.

When this flag is on, the CA requests a level 3 interrupt when the CW byte count reaches 0. If the chain flag is off and zero count override is on the adapter disconnects from the byte multiplexer or remains connected to the burst channels without giving Channel End and resumes data transfer when the proper CWAR Valid latch comes on.

Zero Count Override Operation:

The 3705 control program loads the CW address into the appropriate CWAR with an Output X'50' or X'51' instruction.

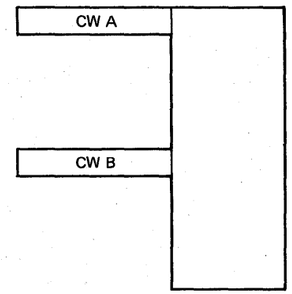
The CA decodes the channel command and fetches control word A.

The CA transfers data between the 3705 and the channel according to the channel command.

When the byte count decrements to zero, the CA requests a level 3 interrupt without presenting channel status.

The 3705 control program loads the address of control word B into the appropriate CWAR, and sets the appropriate 'CWAR Valid' latch. When the level 3 interrupt is reset, the CA fetches the control word B.

The transfer normally ends with a channel stop sequence.



CYCLE STEAL CONTROL WORDS (PART 3)

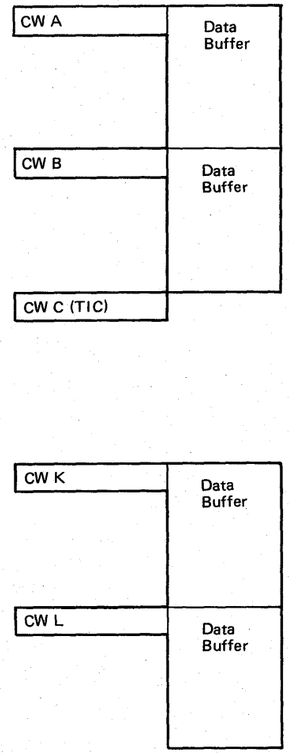
CA TRANSFER IN CHANNEL CONTROL WORD

The CA transfer in channel (TIC) control word causes the cycle steal mechanism to load the address field of the TIC control word with the address of a new string of control words. The adapter can transfer from one sequential string of control words to a new sequential string without control program intervention.

TIC Operation

The CA transfers data using a sequential string of control words. When the byte count for CW B decrements to 0, the cycle steal mechanism fetches CW C.

Channel adapter hardware decodes the TIC control word and requests another CW fetch cycle steal operation to fetch CW K. The address in CW C is the address of CW K. When the CW fetch is complete, the CA resumes the data transfer.



CW FLAG SUMMARY

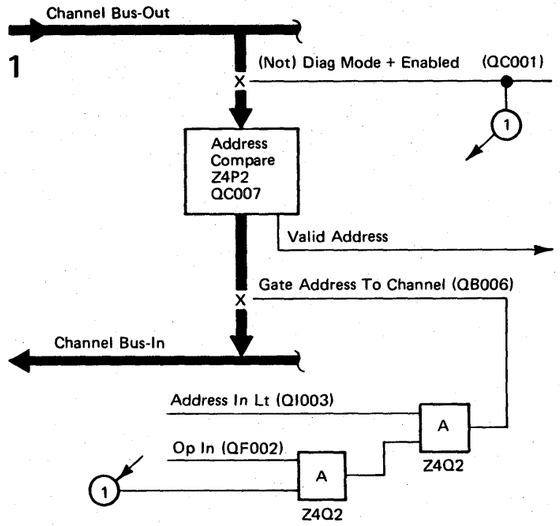
Control Word	Chan Stop	Byte Count	Zero Cnt Override Flag	CW Chain Flag	Level 3 Interrupt Request	Status Presented to Channel	Comments
Out	no	0	0	1	no	none	Chain immediately to next sequential CW.
Out	no	0	0	0	yes	CE	The 3705 control program must set additional status (DE plus other) to be presented. See PLM.
Out	no	0	1	0	yes	none	Wait for the level 3 interrupt request to be reset before resuming the data transfer.
Out	no	0	1	1	yes	none	Chain when level 3 interrupt request is reset.*
Out	yes	X	X	X	yes	CE	Proceed to normal ending for the command. The 3705 control program may set DE plus other. See PLM.
Out Stop	no	0	0	1	no	CE, DE	Channel Command ended.
Out Stop	no	0	0	0	yes	CE	The 3705 control program must set additional status to be presented.
Out Stop	no	0	1	0	yes	none	Wait for the level 3 interrupt request to be reset before resuming the data transfer.
Out Stop	no	0	1	1	yes	none	Chain after level 3 interrupt request is reset.*
Out Stop	yes	X	X	X	yes	CE	Proceed to normal ending for the channel command. The 3705 control program may set DE plus other. See PLM.
In	no	0	0	1	no	none	Chain immediately to next sequential CW.
In	no	0	0	0	yes	CE	3705 control program must set additional status to be presented.
In	no	0	1	0	yes	none	3705 control program must set additional status to be presented.
In	no	0	1	1	yes	none	Chain to the next sequential CW after level 3 interrupt.
In	yes	X	X	X	yes	CE	Proceed to normal ending for the channel command. The 3705 control program may set DE plus other. See PLM.

X = don't care

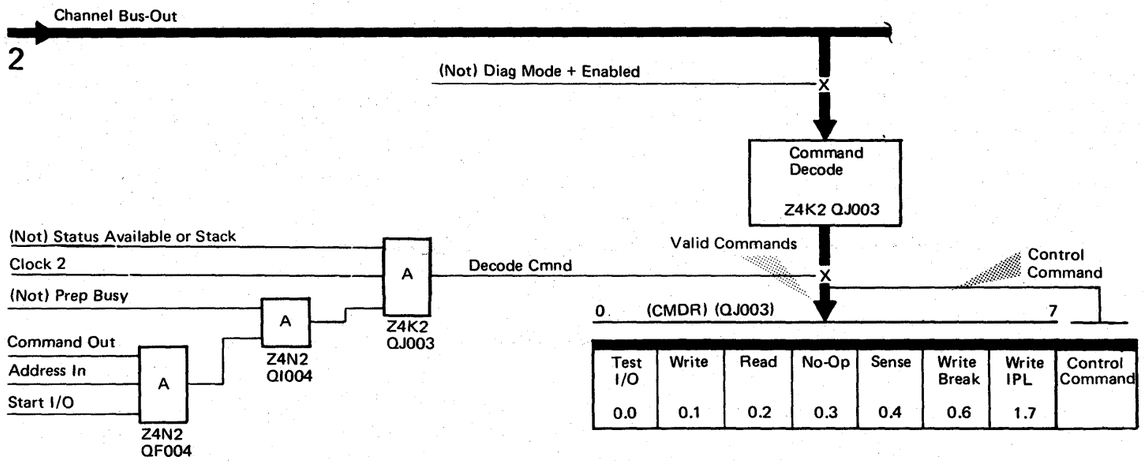
*The 3705 program decides if and when it will continue.

INITIAL SELECTION

Initial selection consists of addressing the CA and sending the CA a channel I/O command. The initial selection tag line sequences are not the same for all types of channels the CA can be attached to. Refer to *IBM System/360 and System/370 Interface Channel to Control Unit, Original Equipment Manufacturers' Information*, GA22-6974, for the sequencing differences of byte, block, and burst channels.



Note: Unit Exception — valid status for a Sense command only if an IPL is in progress over another channel adapter.



3 Initial status is CA hardware generated and presented to the channel without control program intervention.

0	0	0	0	0	0	0	0	Channel I/O Command accepted.
0	0	0	0	0	0	1	0	Unit Check—one of the following conditions exists: ● The command is a control command and the CA has been programmed to reject control commands. ● 3705 is not initialized, and a command other than TIO, NOP, Sense, or IPL was issued. ● The command byte has bad parity.
0	0	0	0	0	0	0	1	Unit Exception-valid status only for channel Sense (see note), Read, Write, or Write Break commands. The command cannot be executed because the associated CWAR valid latch has not been set.
0	0	0	0	1	1	0	0	Channel End and Device End—always presented for a channel No-Op command.
0	0	0	1	0	0	0	0	Busy—the 3705 is already executing a channel I/O command. If the ending status for the command in progress has been generated, it is presented with this status unless the channel command initiating the selection is a channel Test I/O command.
0	0	0	0	1	0	0	0	Channel End—always presented for a control command when the CA has been programmed to accept control commands. A L3 interrupt follows.

CHANNEL CONTROL COMMANDS

All commands are control commands except the valid commands listed below.

Test I/O	X'00'
Write	X'01'
Read	X'02'
No-Op	X'03'
Sense	X'04'
Write IPL	X'05'
Write Break	X'09'

The 3705 control program has the option of having the CA hardware command reject the control commands during initial selection, or having the CA hardware accept the control commands by presenting an initial channel end status and then requesting a level three interrupt.

To activate the CA hardware to accept the control commands, the control program must execute an Output X'56' with bit 1.7 on. 1 This turns the 'control command enabled' latch on.

To deactivate the CA hardware to reject the control commands, the control program must execute an Output X'56' with bit 1.6 on. 2 This turns the 'control command enabled' latch off. The following actions also turn the 'control command enabled' latch off.

- Power on reset
- Reset button pressed
- Load button pressed
- Diagnostic reset (Output X'58' with bit 1.7 on)
- Write IPL command issued

'Control Command Enabled' Latch Off

A valid command is accepted at initial selection as shown on 9-310.

A control command is rejected at initial selection by presenting unit check status and turning on the command reject sense latch. 3

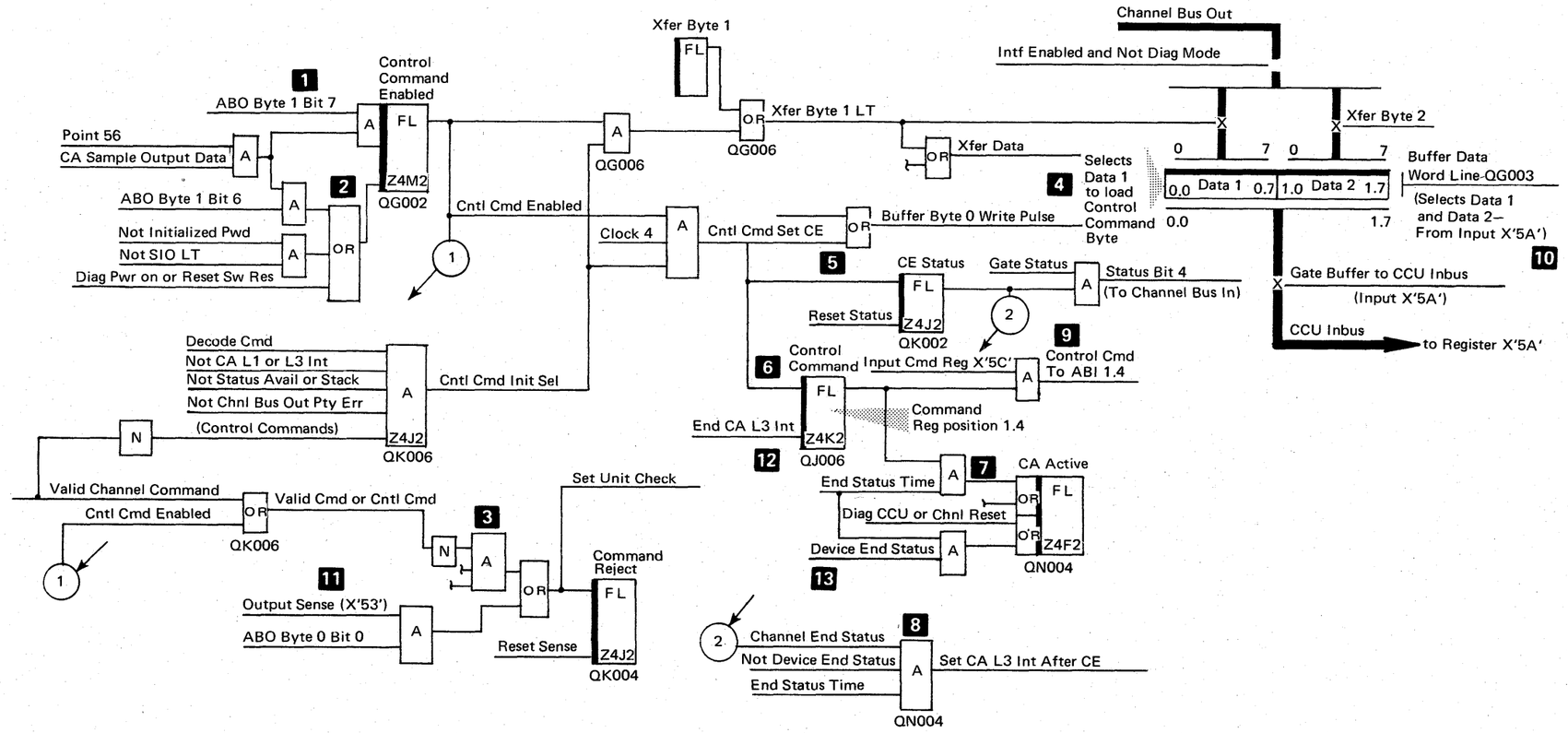
'Control Command Enabled' Latch On

A valid command is accepted at initial selection as shown on 9-310.

A control command generates the following action:

1. The CA forces lines 'xfer data', 'buffer byte 0 write pulse', and 'xfer byte 1 Lt' on to load the control command byte from the 'channel bus out' into the Data 1 data buffer. 4
2. The CA sets the 'channel end' latch in the status register then CE is presented to the channel as initial status. 5
3. The CA sets the 'control command' latch in the command register position 1.4. 6 No other command bits are set in the command register because the control command did not decode as a valid command.
4. At 'end status time' of the initial selection status, the CA sets the 'CA active' latch. 7
5. At the same time, the CA sets the level 3 interrupt latch. 8
6. During the level 3 interrupt, the control program can execute Input X'5C' to examine the command register. 9 If none of the command bits in register X'5C' are on and bit 1.4 is on, the channel has issued a control command.
7. During the level 3 interrupt, the control program can determine the bit configuration of the control command byte by executing Input X'5A'. This transfers the contents of Data 1 and Data 2 to register X'5A'. 10 The control command byte is in byte 0 of the register in channel format.
8. During the level 3 interrupt, the control program can set Command Reject in the sense register, if desired, by executing Output X'53' with bit 0.0 on. 11 This also sets Unit Check in the status register.
9. During the level 3 interrupt, the control program must always set Device End in the status register by executing Output X'54' with bit 0.5 on.
10. When the control program executes Output X'57' with bit 1.3 on, the CA resets the 'level 3 interrupt request' latch. This resets the control command latch. 12 The CA presents the ending status of Device End (plus Unit Check if Command Reject was set) to the channel and resets the 'CA active' latch ending the command. 13

Note: No data transfer can take place during the execution of a control command.



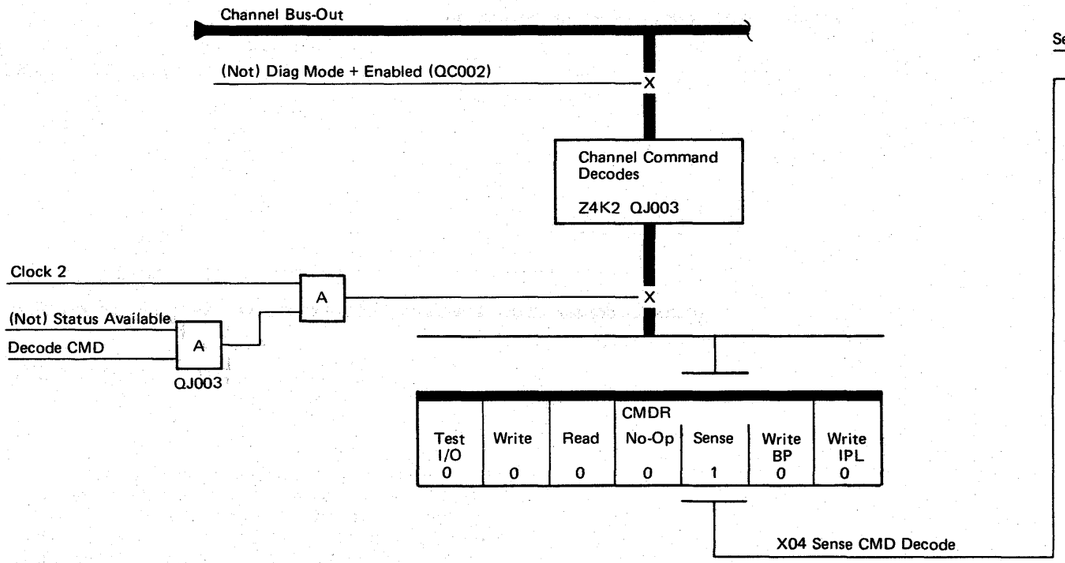
CA2

CHANNEL SENSE COMMAND

The channel Sense command causes the CA to gate the byte contained in the CASNSR on to the channel bus-in. No cycle-steal operations are required nor is any 3705 control program intervention required.

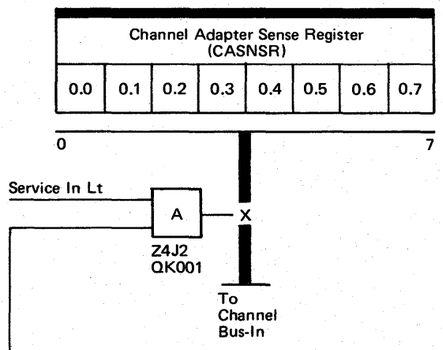
CA DECODES A SENSE COMMAND

During the initial selection sequence, the channel presents a Sense command to the CA. If the command byte is valid, the CA responds with an appropriate initial status; see *INITIAL SELECTION, 9-310.*



CA GATES THE SENSE BYTE TO BUS-IN

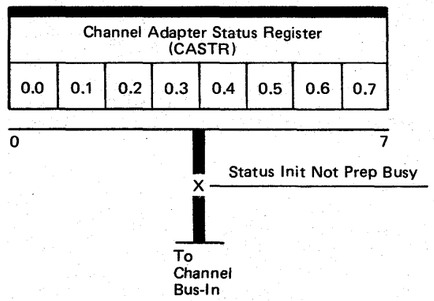
The CA gates the contents of CASNSR onto the channel Bus-In.



Note: See page 9-150 for sense register bit definitions.

CA GATES FINAL STATUS TO BUS-IN

The command is ended when the channel accepts the status from the CA.



0 0 0 0 1 1 0 0 Channel End and Device End status returned to channel.

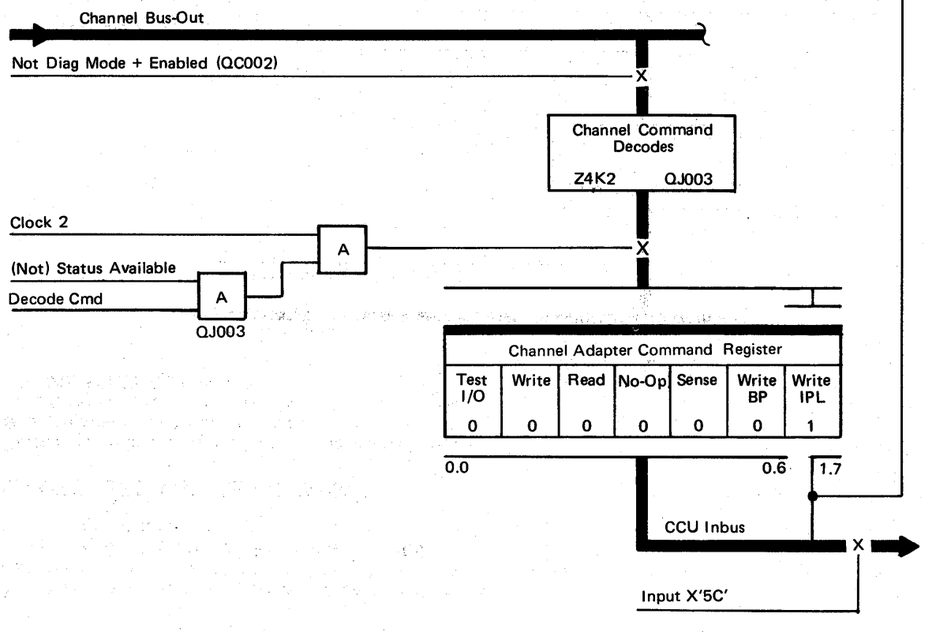
Channel End, Device End, Unit Exception final status is returned if 3705 is in the initialized state and the Sense Unit Exception Latch is set.

CHANNEL WRITE IPL COMMAND

- The channel Write IPL command transfers the program load module from the CPU to 3705 storage.
- The CA requests a level 3 interrupt when the channel accepts initial status so that the control program can initialize the CA registers.

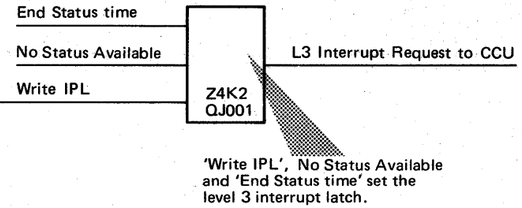
During the initial selection sequence in which the channel issues a Write IPL command to the CA, the CA command decode circuits decode the Write IPL and set the 'WRITE IPL' latch in the command register. Because the CA external registers may not be initialized at this time, the CA requests a level 3 interrupt to signal the 3705 control program that the Write IPL command has been received. Whenever the control program initializes the CA external registers and resets the level 3 request, the CA requests cycle-steal operations to fetch the control word to be used in executing the channel Write IPL command.

CA DECODES A WRITE IPL CMD



CA REQUESTS A LEVEL 3 INTERRUPT

When the CA decodes the Write IPL command, initial status is presented to the channel; see INITIAL SELECTION, 9-300. When the channel accepts the all zero initial status with the 'Write IPL' latch on in CMDR, a 'level 3' interrupt is requested.



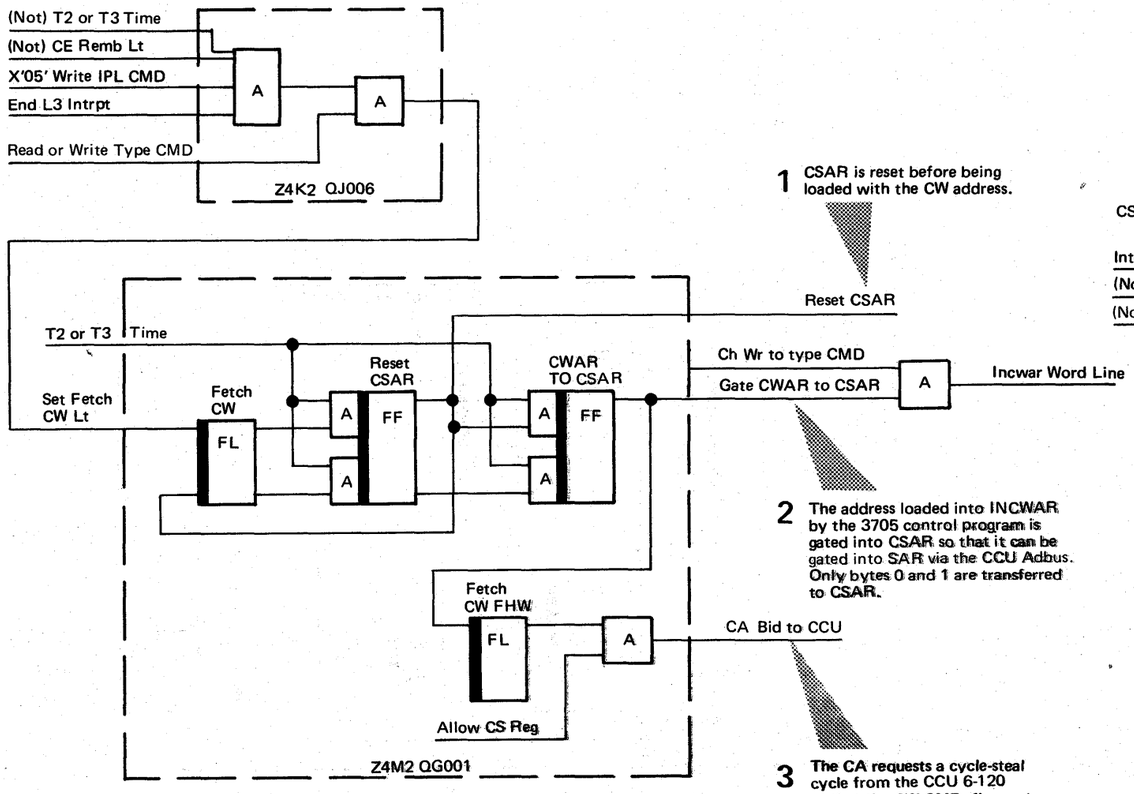
3705 CONTROL PROGRAM RESPONDS TO THE INTERRUPT

By executing an Input X'77' instruction, the 3705 control program (ROS program) determines that the type 2 CA requested the level 3 interrupt. With an Input X'5C' (9-250) the control program determines which channel command was decoded when the interrupt request occurred. When the program determines the command was a channel Write IPL command (bit 1.7 on in register X'5C'), the 3705 control program must initialize the CA external registers to handle this command. Because the command is a Write type command (uses INCWAR), the control program must load INCWAR with the address of the control word to be used in executing this command. The 3705 control program must also set INCWAR valid latch with an Output X'55' instruction, 9-170

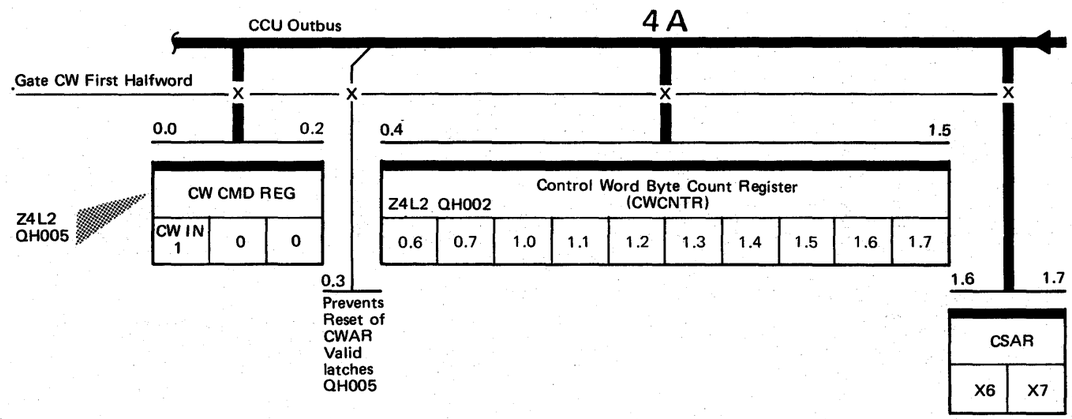
CHANNEL WRITE IPL COMMAND (PART 2)

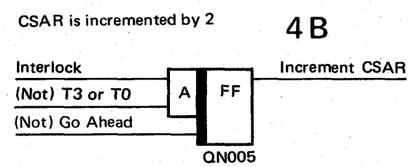
CA REQUESTS CW FETCH CYCLE STEAL OPERATION

The 3705 control program services the level 3 interrupt and resets the 'level 3 request' latch by executing an output X'57' instruction, setting bit 1.3 in the CAMR. When the level 3 request latch is reset, the CA executes a CW fetch cycle-steal operation to transfer the byte count, CW command, flag and data address to the correct CA registers.

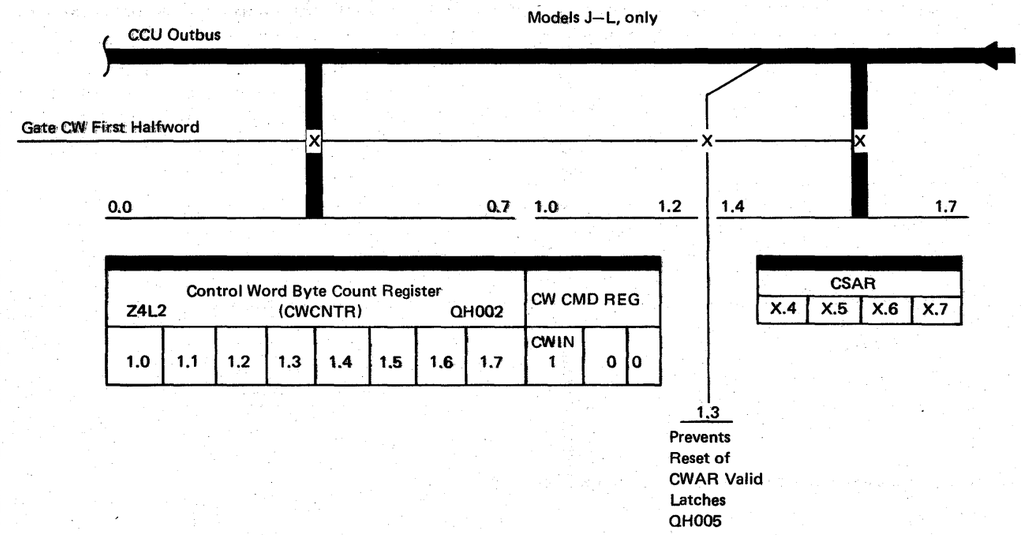


Models A—H, only



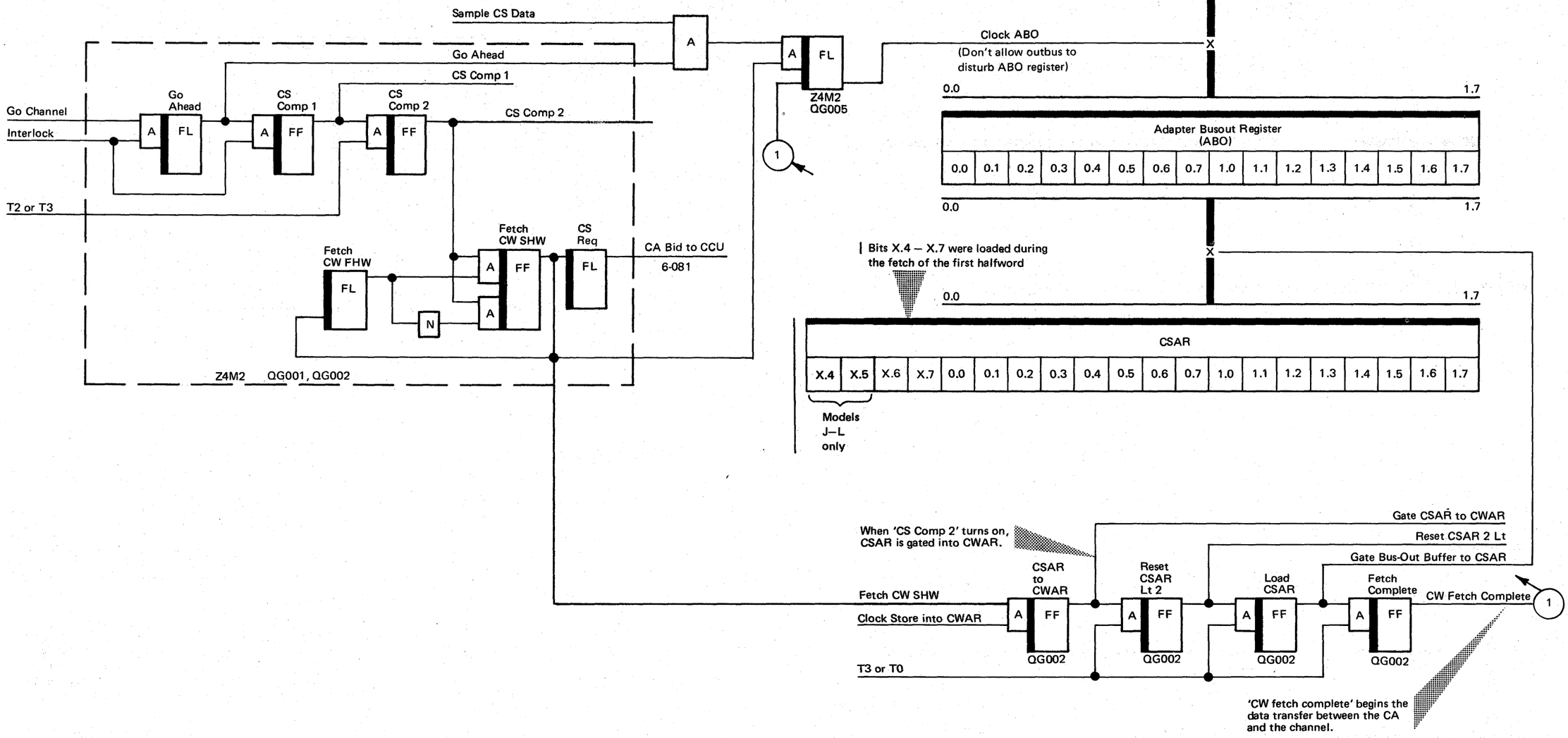


Models J—L, only



CHANNEL WRITE IPL COMMAND (PART 3)

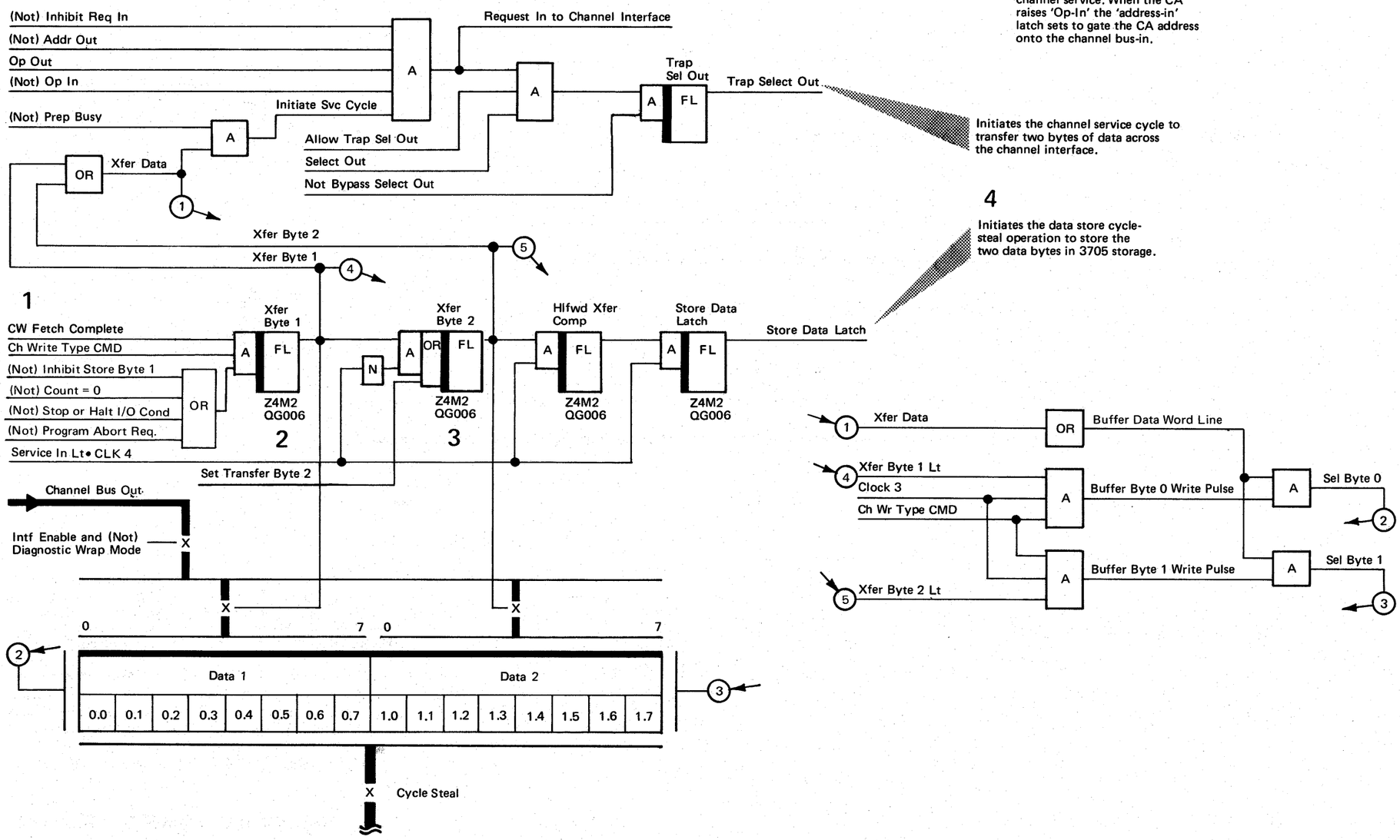
The CA requests a second CW fetch cycle-steal cycle. During this cycle, the second halfword of the CW (storage address) at which the data is to be stored is transferred into CSAR. However, before CSAR is loaded with the new address, CSAR is incremented by 2 and gated into INCWAR. INCWAR is now plus 4 from its original contents and contains the address of the next sequential CW.



WRITE IPL COMMAND (PART 4)

CA AND CHANNEL TRANSFER DATA

For a multiplex channel when 'CW fetch complete' turns on, the CA initiates a channel service cycle by raising 'request in tag' and trapping select out if the adapter is attached to the byte multiplex channel. The CA remains attached to the channel until two bytes of data are transferred from the channel to the data buffer register.



Note: On the multiplexer channel, each time the CA initiates a channel service cycle, the CA address is gated onto the channel Bus-In to identify the device requesting channel service. When the CA raises 'Op-In' the 'address-in' latch sets to gate the CA address onto the channel bus-in.

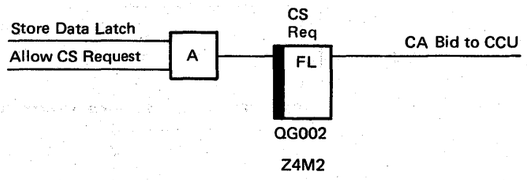
WRITE IPL COMMAND (PART 5)

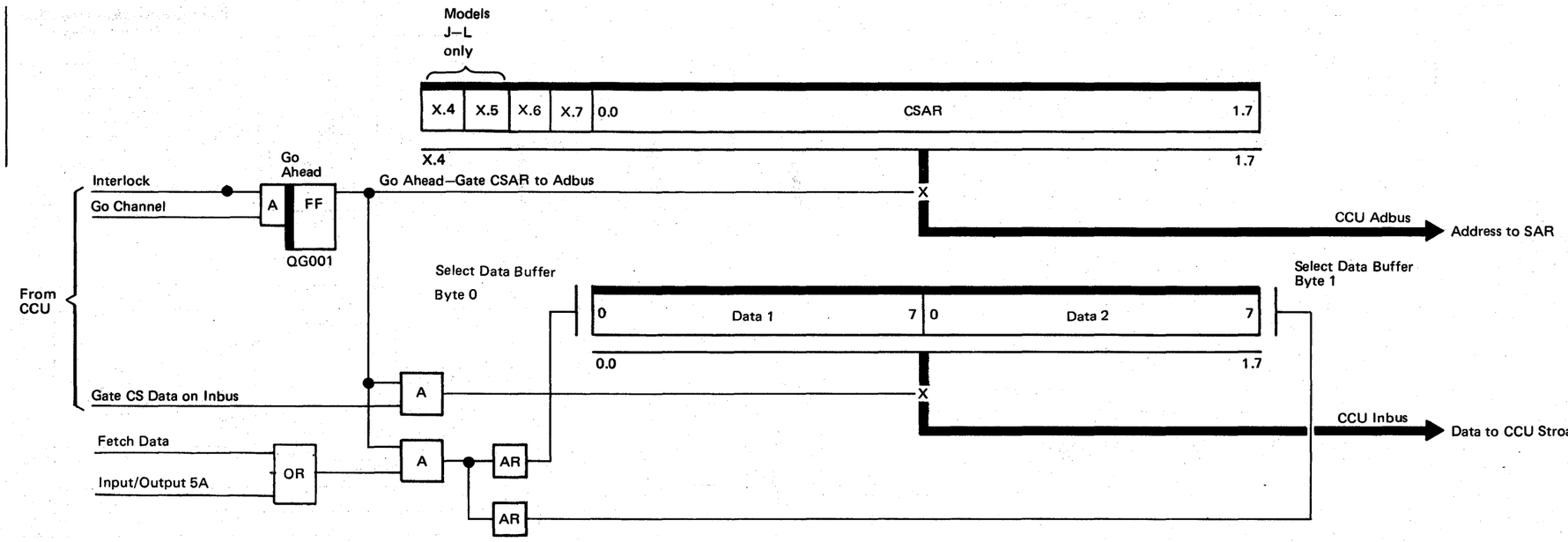
CA REQUESTS A CYCLE STEAL OPERATION

When the 'store data' latch turns on, the CA bids for a cycle-steal operation to store the halfword in the data buffer. When attached to the byte multiplexer channel, the CA disconnects from the channel while the CA cycle steals.

During the cycle-steal cycle, CSAR is gated into SAR via the CCU adbus and addresses 3705 storage where the data is to be stored. The data buffer is gated onto the CCU Inbus and hence to 3705 storage through the CCU's ALU.

Each cycle steal operation increments CSAR plus 2.

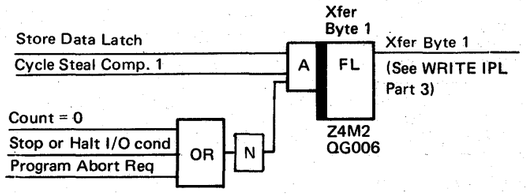




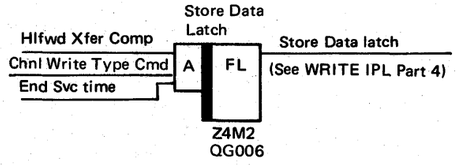
WRITE IPL COMMAND (PART 6)

CA ALTERNATES CHANNEL SERVICE & CYCLE STEALS

The CA and channel continue alternate data transfer and data-store cycle-steal operations until the byte count decrements to zero, a channel stop or Halt I/O (Interface disconnect) is signalled from the channel, or the control program sets 'program abort' with Output X'57' (byte 1.1 = 1).



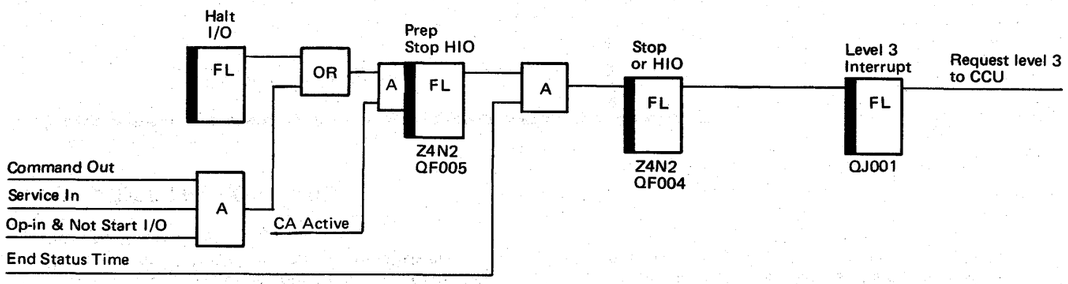
Begins channel data transfer



Begins Cycle Steal operation.

WRITE IPL ENDING

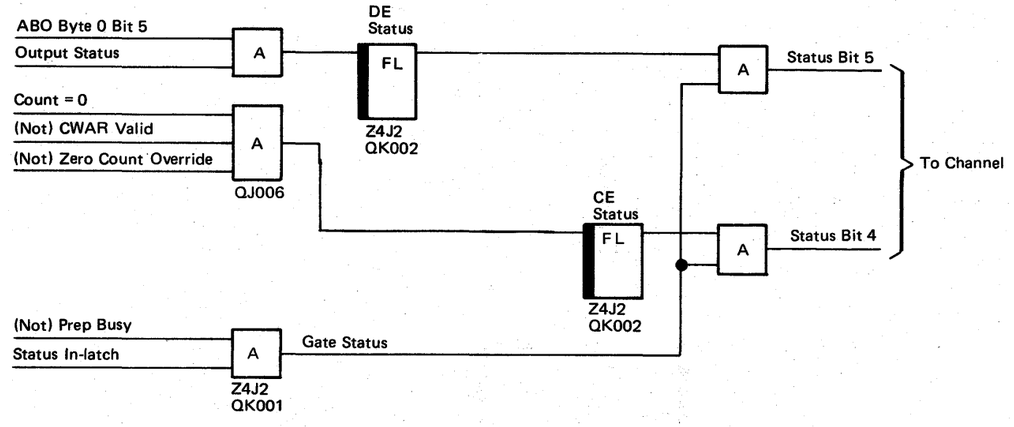
The normal ending for the channel Write IPL command is a channel-initiated stop sequence. The channel initiates a stop sequence by raising 'command-out' in response to 'service-in' from the CA. A 'not-stop' or 'halt I/O condition', a 'not count equal zero' or 'not program abort req' is required to request a channel data transfer. When a stop condition exists, Channel End (CE) is generated automatically by CA hardware. The CA requests a level 3 interrupt to signal the 3705 control program (ROS program) that the stop sequence has been detected. The stop sequence causes bit 1.2 to be set in the CACR so that the control program can determine the exact cause of the interrupt by issuing an Input X'55' instruction.



CA PRESENTS ENDING STATUS

The CA hardware generates Channel End (CE) status to present to the channel. Device End (DE) is loaded into the CASTR by the level 3 interrupt program that was just loaded into the 3705 by the Write IPL command.

If a Halt I/O is issued by the channel to the CA during a Write IPL command, the channel must reissue the Write IPL command.

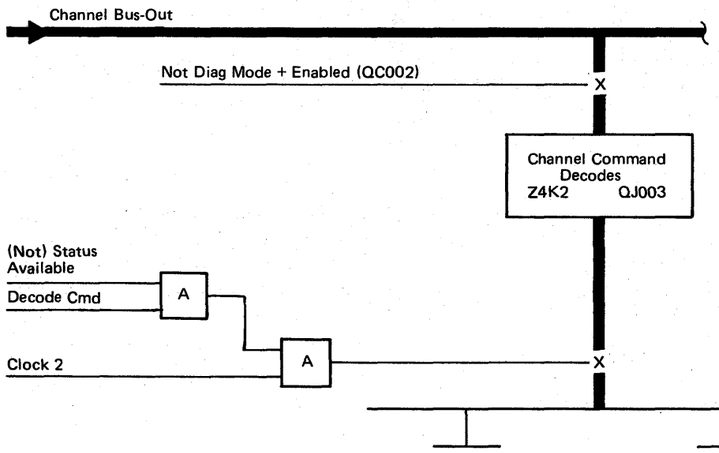


CHANNEL WRITE AND WRITE BREAK CMD'S

- Channel Write Break commands differ from channel Write commands only in that they set bit 1.1 (I/O Write Break Command Remember) in the CACR.
- Channel Write and Write Break commands transfer data from the host CPU to the 3705.
- If INCWAR Valid is not set when the CA decodes one of these commands, Unit Exception initial status is returned to the CPU.
- Decoding a Write or Write Break command does not cause a level 3 interrupt to be requested. The 3705 control program must have previously initialized the CA external registers to handle these commands.

  When the CA decodes either of these commands, a control word fetch cycle-steal operation is requested so that the control word to be used can be loaded into the appropriate registers.

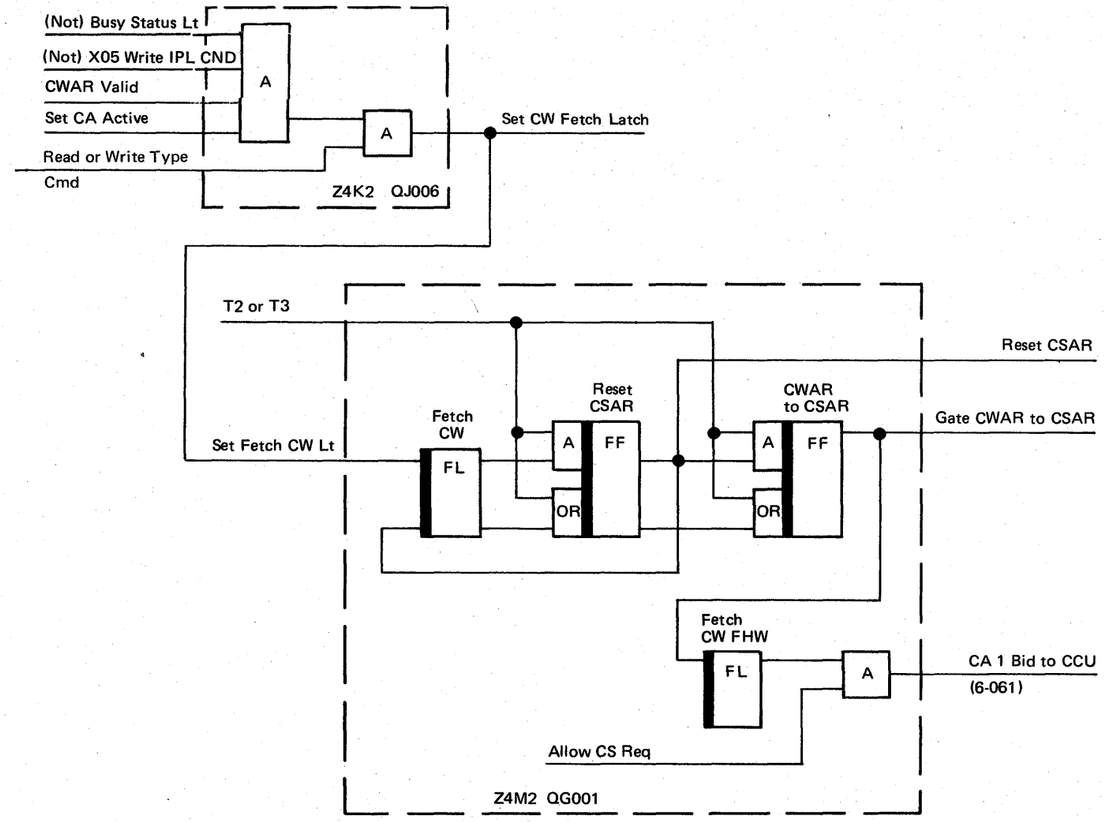
CA DECODES THE COMMAND



Channel Adapter Command Register CMDR						QJ003
Test I/O	Write	Read	No-Op	Sense	Write BP	Write IPL
0	X	0	0	0	X	0

Note: The CMDR Write BP latch is gated to the CCU Inbus during an Input X'55' instruction to signal the status of the Write Break Remember Condition.

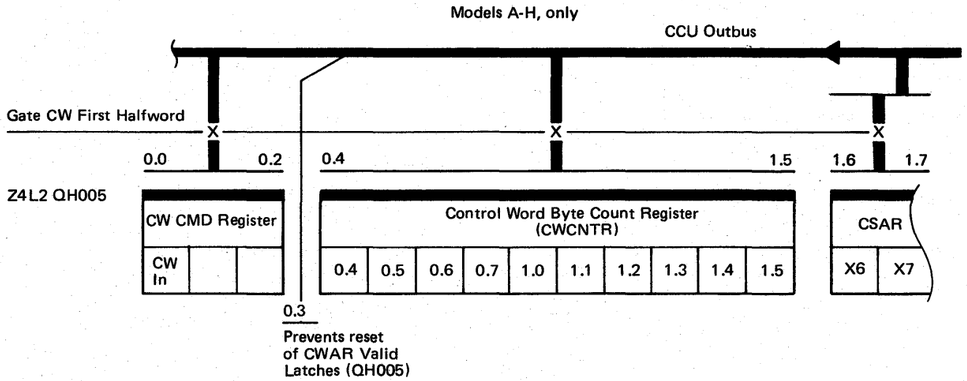
CA REQUESTS A CW FETCH CYCLE-STEAL OPERATION

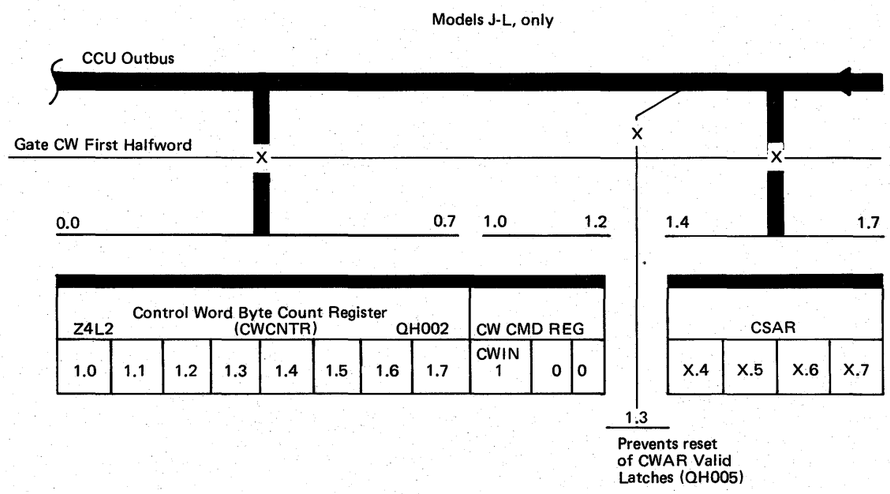


CHANNEL WRITE AND WRITE BREAK COMMAND (PART 2)

CW FETCH CYCLE STEAL

A CW fetch cycle-steal operation is two cycles long. The first cycle fetches the CW command, the flag, the byte count, and bits X.6 and X.7 in CSAR. The second cycle fetches the bytes 0 and 1 of the beginning address to be used for data storage. When the cycle-steal operation ends, transfer data begins.





CHANNEL TRANSFERS DATA TO CA

The CA request for channel service for Write and Write Break commands is exactly the same as for a Write IPL command.

See 9-330 for the description of the CA request for service and subsequent cycle steal operation request.

Alternate channel data transfers and data store cycle-steal cycles continue the same as they did for the channel Write IPL command.

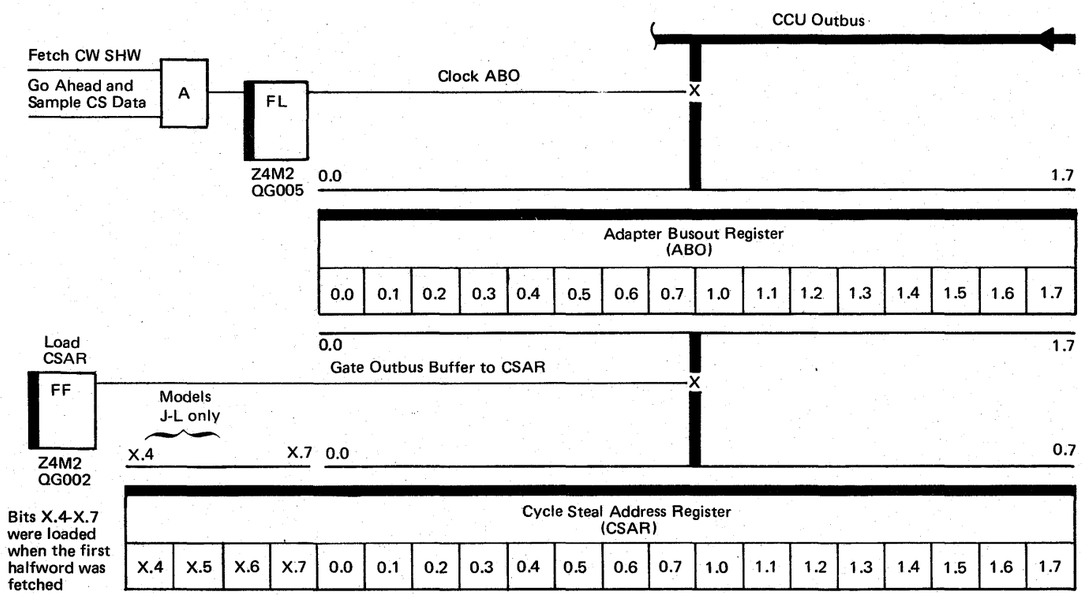
CA REQUESTS DATA STORE CYCLE STEAL

The CA cycle-steal requests for Write and Write Break commands occur exactly the same as for the Write IPL command.

See 9-360 for a description of the CA cycle-steal request.

The CA and channel alternate cycle-steal cycles and channel transfers until the command is ended.

See 9-430 for a description of single byte data transfers.



CA2

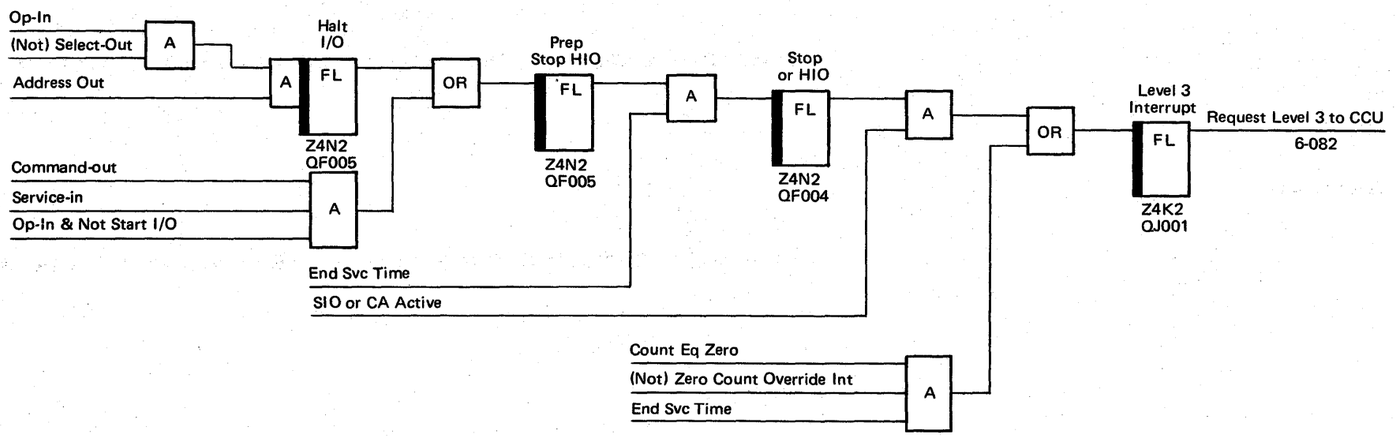
CHANNEL WRITE AND WRITE BREAK COMMAND (PART 3)

WRITE COMMAND ENDING

Write and Write Break commands can end by:

- A channel Stop sequence or a channel Halt I/O.
- CW byte count decremented to zero and CW chaining not indicated.

When either of the conditions to end a Write or Write Break command occur, Channel End status is generated by CA hardware and a level 3 interrupt is requested, so that the 3705 control program can take whatever action may be appropriate for the channel command. The 3705 control program must also set Device End (DE) status to be presented to the channel.

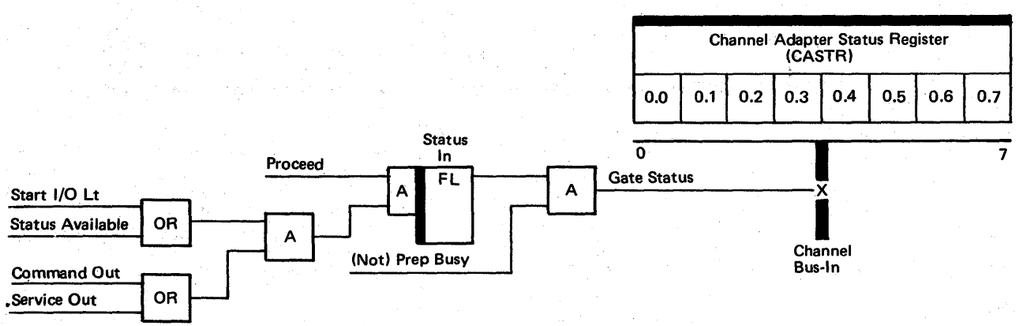


CA PRESENTS ENDING STATUS TO CHANNEL

Channel End (CE) is generated by the CA hardware while the 3705 control program determines whether or not to present DE.

See INPUT X'54' INSTRUCTION, 9-170 for the definitions of status bits that can be transferred to the channel.

Status presentation is subject to stacking by the channel. Stacked status is retained in CASTR until accepted by the channel. The CA attempts to present status whenever the channel drops 'suppress out'.



CHANNEL WRITE OPERATION WITH ODD BYTE BOUNDARY

ODD BOUNDARY STARTING DATA ADDRESS

The CSAR (Cycle Steal Address Register) is initially loaded with the CW (Control Word) address at the beginning of a CW fetch operation and then is loaded with the starting data address when the CW fetch is complete.

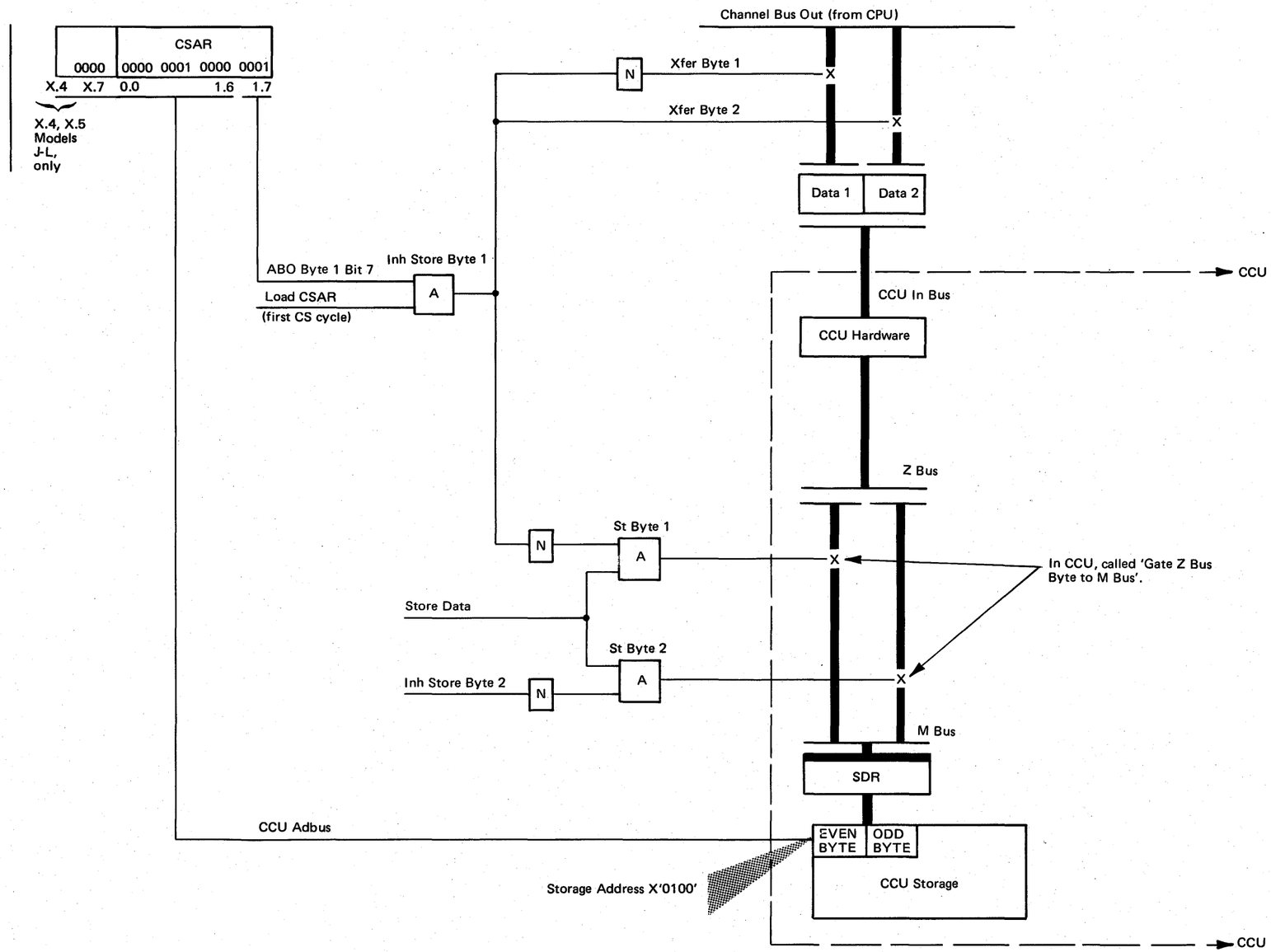
During the first data transfer to storage in a write operation, if the storage address specified by the Write Command starts on an odd boundary, CSAR bit 1.7 will be on. This turns on the line 'inh store byte 1' which (1) prevents gating the data from the 'channel bus out' to data buffer 1, and (2), forces 'xfer byte 2' to gate the data into data buffer 2. After the data buffers are transferred to the CCU In Bus by cycle steals, 'store byte 2' gates the odd byte onto the M bus. CCU hardware gates the byte into SDR and then into storage. This concept is shown in the diagram.

Subsequent cycle steal operations write data into CCU storage on even boundaries two bytes at a time, because 'load CSAR' is only active during the first data transfer.

LAST DATA BYTE LOCATED AT EVEN BYTE BOUNDARY

If the byte count reaches zero or a channel stop occurs at a byte boundary, 'inh store byte 2' comes on, and the odd byte is not gated to the M bus. A storage write operation stores the new even byte data as the odd byte from storage is rewritten.

Note: This concept illustrates an odd byte being transferred during the first data transfer cycle only.



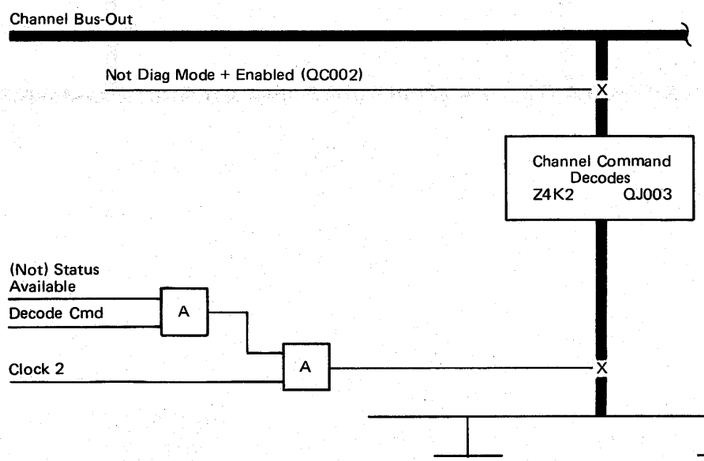
CHANNEL READ COMMAND

- A channel Read command transfers data from 3705 storage to the CPU.
- The 3705 control program must initialize the CA registers so that it can execute the channel command.

When the CA decodes a channel Read command, it does not request a level 3 interrupt to initialize the control register and OUTCWAR. If OUTCWAR Valid (CACR bit 0.3) is not set when the Read command is decoded, Unit Exception initial status is returned to the channel.

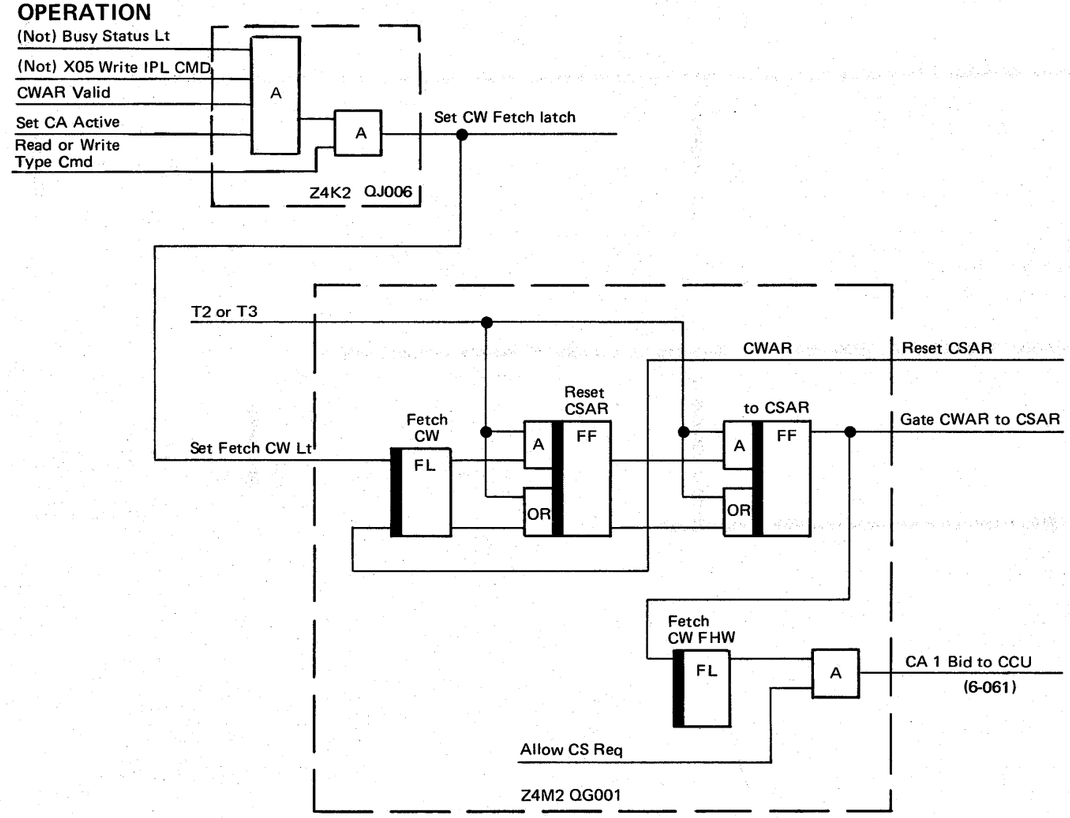
Out and Out-Stop control words are used with this channel command to control cycle-steal operations. See CYCLE STEAL CONTROL WORDS, 9-170, for an explanation of the formats for these control words.

CA DECODES A READ COMMAND



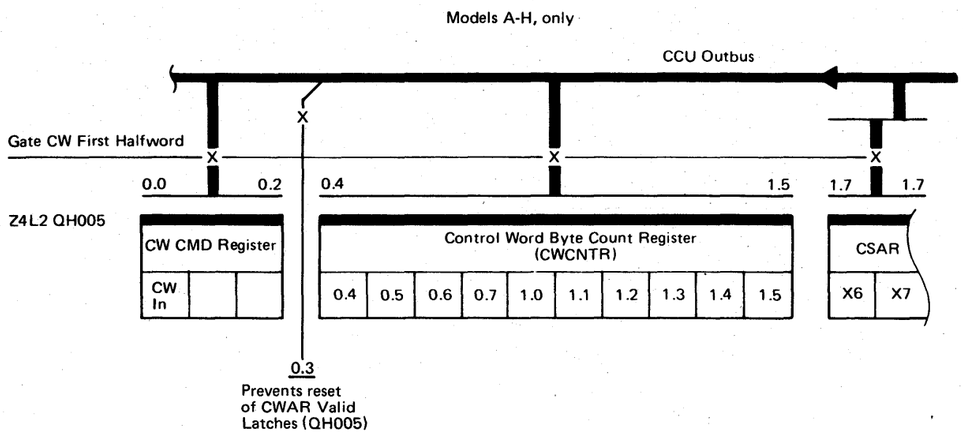
Channel Adapter Command Register CMDR						
0.0 Test I/O	0.1 Write	0.2 Read	0.3 No-Op	0.4 Sense	0.6 Write BP	1.7 Write IPL
0	0	1	0	0	0	0

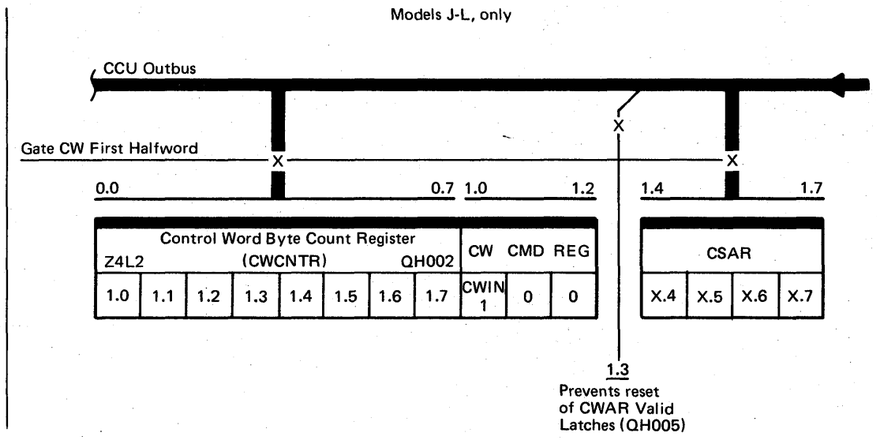
CA REQUESTS A CW FETCH CYCLE STEAL OPERATION



CW FETCH CYCLE STEAL OPERATION

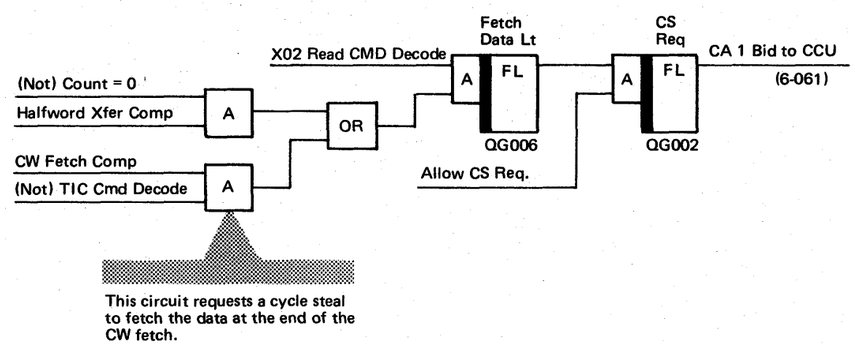
A CWfetch cycle-steal operation is two cycles long. The first cycle fetches the CW command, flag and byte count. The second cycle fetches the beginning address of the data storage. When the cycle-steal operation ends, both the CA and the channel transfer data.

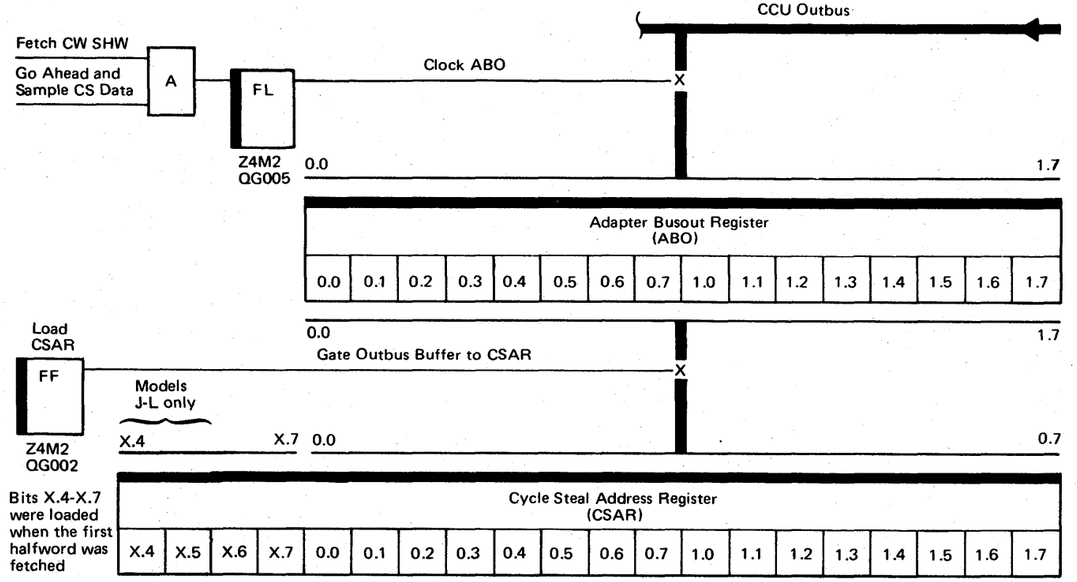




CA REQUESTS A DATA FETCH CYCLE STEAL OPERATION

The CA must have two bytes of data loaded into the data buffer (data 0 and data 1) to transfer to the channel during the channel service operation. These two bytes are fetched from storage by a data fetch cycle-steal operation.

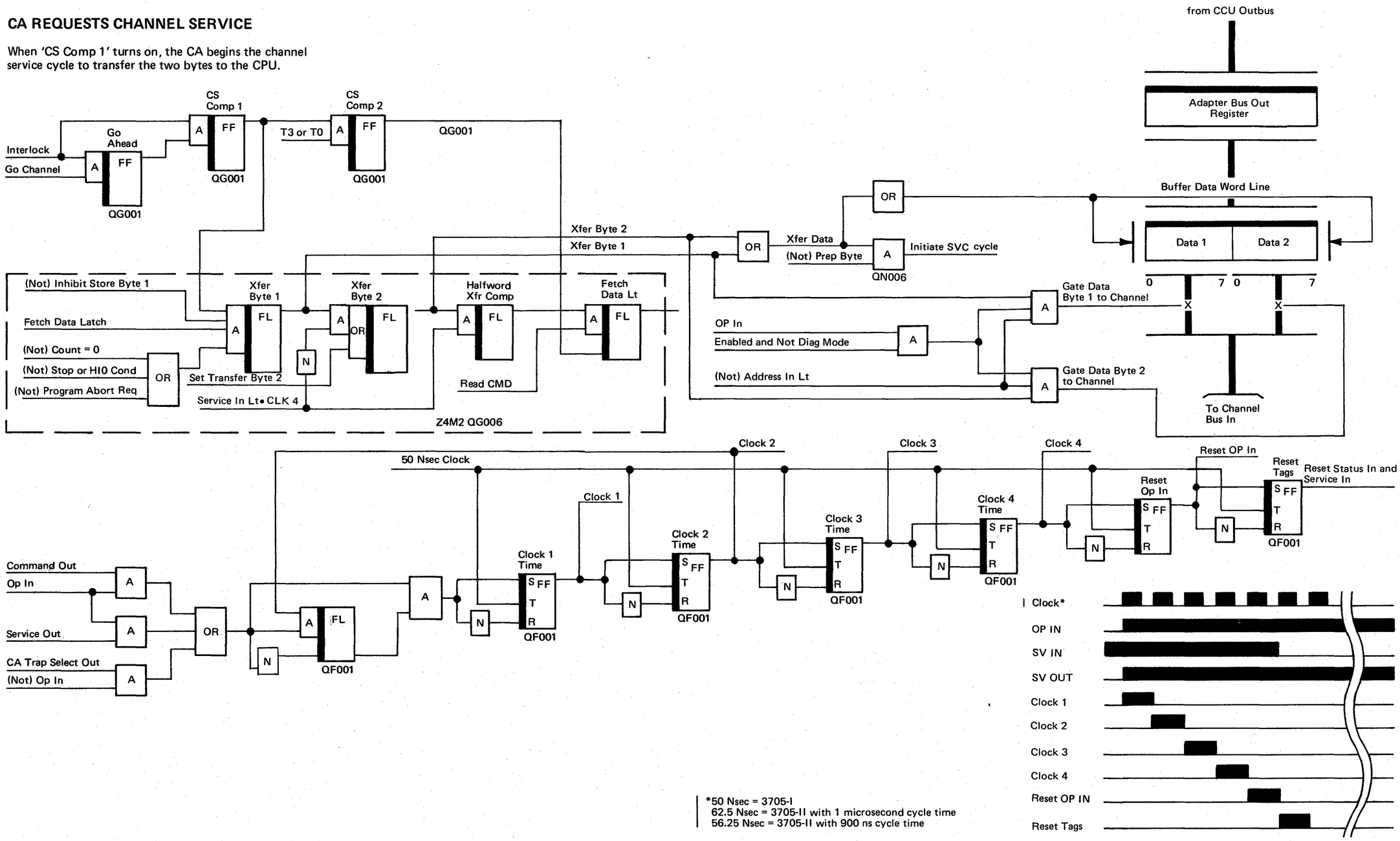




CHANNEL READ COMMAND (PART 3)

CA REQUESTS CHANNEL SERVICE

When 'CS Comp 1' turns on, the CA begins the channel service cycle to transfer the two bytes to the CPU.



*50 Nsec = 3705-I
62.5 Nsec = 3705-II with 1 microsecond cycle time
56.25 Nsec = 3705-II with 900 ns cycle time

CHANNEL READ OPERATION WITH ODD BYTE BOUNDARY

ODD BOUNDARY STARTING DATA ADDRESS

The CSAR (Cycle Steal Address Register) is initially loaded with the CW (Control Word) address at the beginning of a CW fetch operation and then is loaded with the starting data address when the CW fetch is complete.

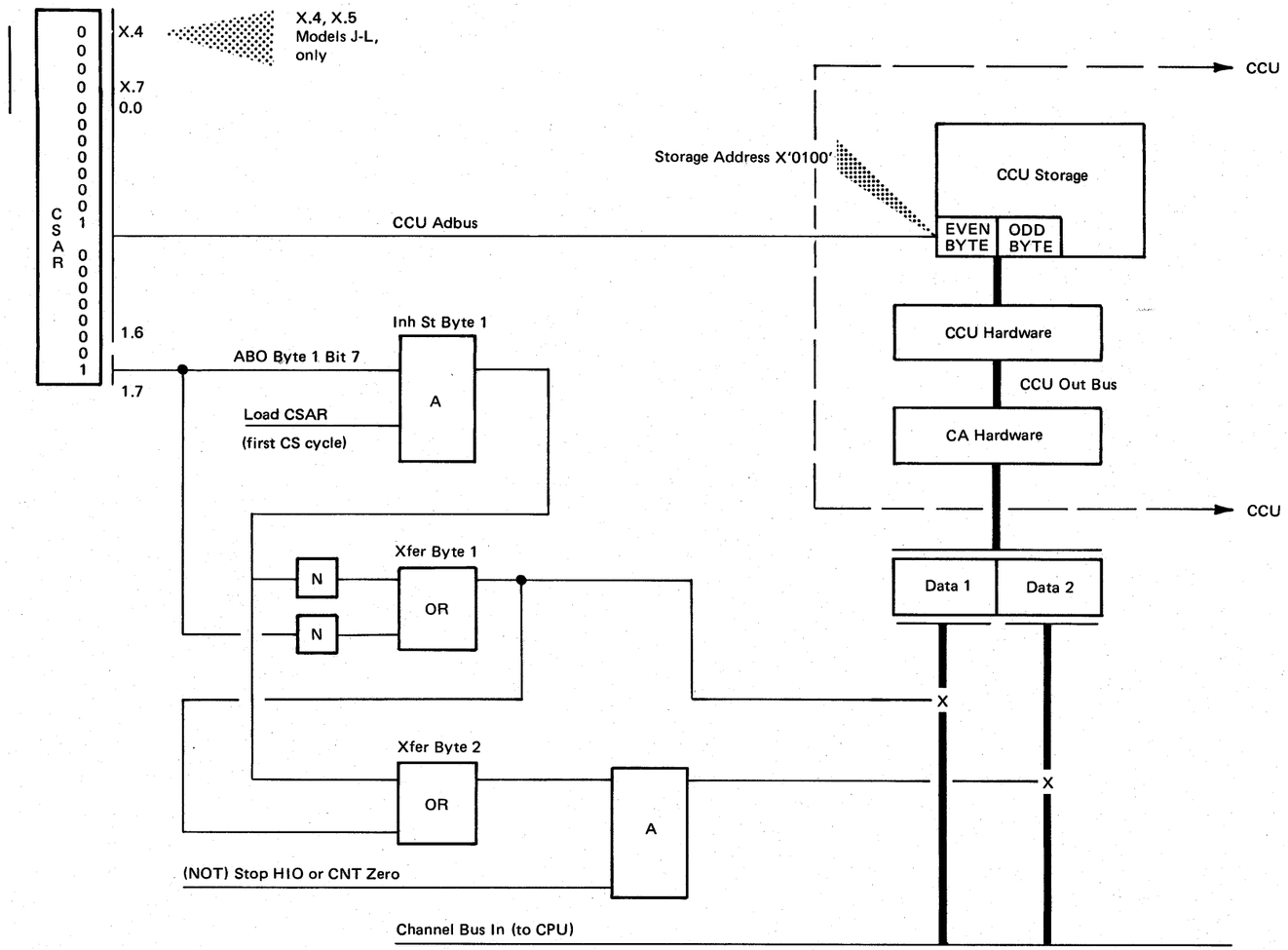
If the data address in the CSAR specifies an odd boundary in CCU storage, the CCU will access the half-word (SAR bit 1.7 is not used for addressing storage), but the CA prevents the even byte from being gated to the CPU channel.

The bit that specified the odd byte in storage is used only to activate the line 'inh store byte 1'. When the data is in the CA data buffers, the line 'inh store byte 1', (1) prevents the data in data 1 buffer from being gated onto the 'channel bus in' and (2) causes the line 'set xfer byte 2' to gate the odd byte in data buffer 2 onto the 'channel bus in' to the CPU. This concept is shown in the diagram.

The data address in the CSAR is increased by 2 on subsequent data transfer cycles. The CA continues to gate both data buffers to the 'channel bus in' because 'inh store byte 1' can only come up on the first data transfer cycle.

LAST DATA BYTE LOCATED AT EVEN BYTE BOUNDARY

If the byte count field in the CA byte count register reaches zero or a channel stop occurs at an even byte, the odd byte in the data 2 buffer will not be gated to the 'channel bus in' and the data transfer operation ends.



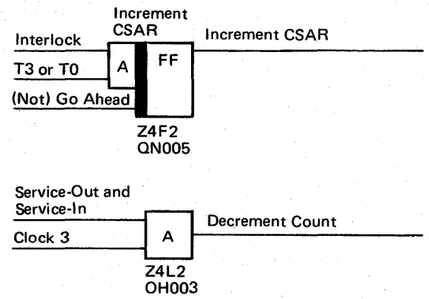
CHANNEL READ COMMAND (PART 4)

ALTERNATE FETCH AND TRANSFER

Data fetch cycle-steal operations and channel data transfers alternate until the channel command is ended either by the control word byte count decrementing to zero with no control word chaining indicated, a channel stop, or Halt I/O sequence.

Each halfword fetched from 3705 storage causes the data address in CSAR to be incremented by two.

Each byte transferred across the channel interface decrements the byte count by one.



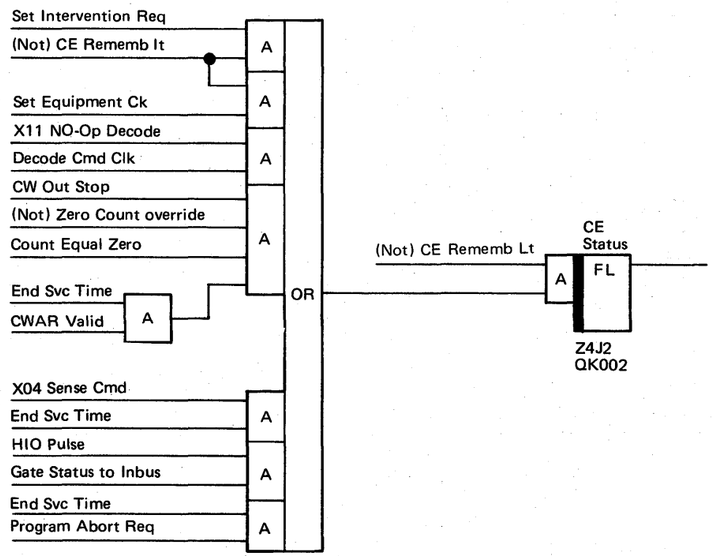
READ CMND ENDING

The channel Read command can be ended by either the control word byte count decrementing to zero with no control word chaining indicated, a Channel stop, or Halt I/O sequence. Ending status is presented to the channel in two parts. Channel End is generated by CA hardware. Device End plus any other unusual ending conditions (Status Modifier, Unit Exception) is generated by the 3705 control program during the L3 interrupt caused by the CA hardware having generated Channel End.

If chaining is indicated and the byte decrements to zero, the CA fetches the next sequential CW.

If control word chaining is not indicated, the CA hardware generates CE status and requests a level 3 interrupt so that the 3705 control program can indicate any other status that should be presented to the channel along with Device End.

If a channel stop sequence ends the command, the CA hardware generates CE status and requests a level 3 interrupt so that the 3705 control program can indicate what other status to present with Device End.



TEST I/O COMMAND

The channel adapter presents the following initial status indications to the channel for this command:

- All zeros indicates that the CA is command free and contains no pending or stacked status.
- Busy status is presented if the CA has accepted a previous channel command and has not yet presented DE, or the CA has its L1 or L3 interrupt request latch set.
- CE, DE (together or separately) status is presented without Busy if the status is pending or stacked for a previous channel command.
- Device End (DE) and Unit Check (UC) are presented if the 3705 enters the not initialized state while waiting for a channel Write IPL command.
- When the channel accepts the initial status from the CA, the command is ended, and no further action is taken by the CA.

Note: The Test I/O command is set into the command register (CMDR) without resetting the previous command.

NO/OP

The channel adapter presents CE, DE as initial status for this command and takes no further action. No control program intervention is necessary.

CA ERROR INTERRUPTS

Whenever the channel adapter detects a hardware error or a program check, an appropriate bit is turned on in the channel adapter check register (CACHKR), and a level 1 interrupt is requested. The control program may examine the error causing the interrupt by executing an Input X'56' instruction.

The address in CWAR associated with the current channel command is greater than 64K.

The control word fetched is not correct for the current channel command. An Out or Out Stop control word was fetched for a Write, Write IPL, or Write Break command, or an In control word was fetched for a Read command. If either control word is fetched with a byte count of zero, this bit is turned on.

The CCU signals an address or SAR parity error to the channel adapter during cycle-steal operations to turn this bit on. One of the following is indicated:

- Cycle-steal address is beyond storage capacity.
- The address is out of parity.
- The address is in a protected area of storage.

Either the INCWAR, OUTCWAR, data 1, or data 2 local store register contains incorrect parity during a transfer to the CCU or to the channel.

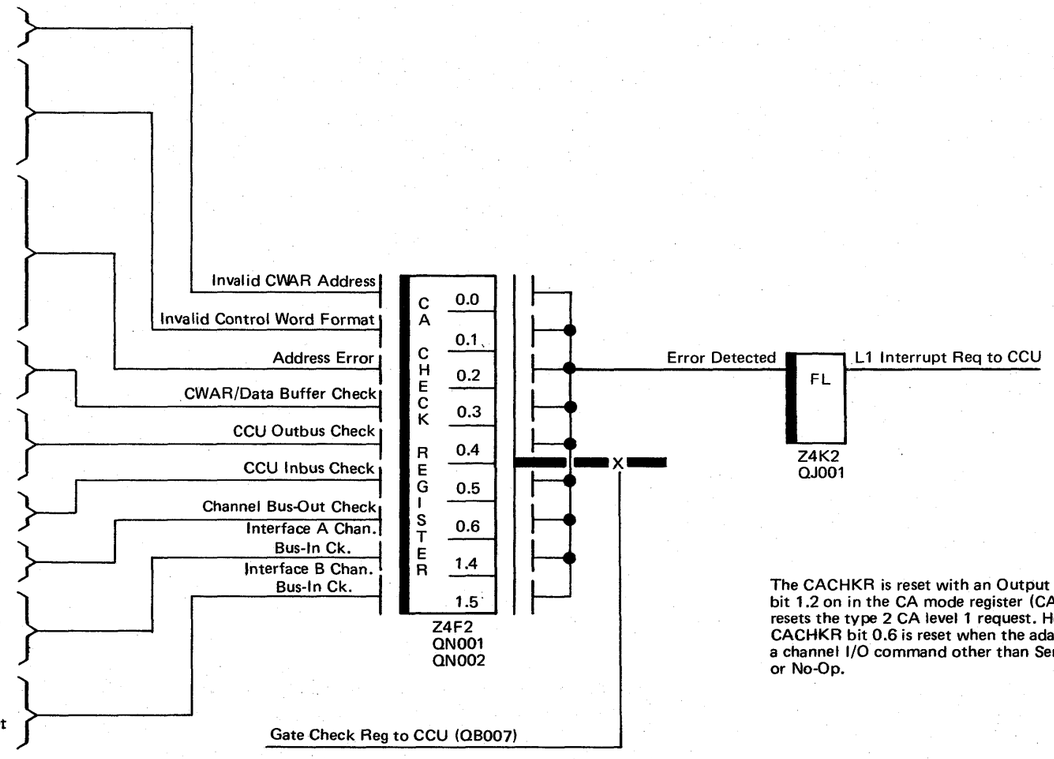
Incorrect parity in the data on the CCU Outbus during either an Output instruction to the CA or a cycle-steal operation fetching data or control words causes this bit to turn on.

Incorrect parity on the CCU Inbus during a data store cycle-steal operation causes this bit to turn on.

This bit is set when incorrect parity is detected on the channel Bus-Out.

This bit is set when incorrect parity is detected in the byte presented to the channel Bus-In. The most probable cause of this failure is a failing channel driver card in socket Q2.

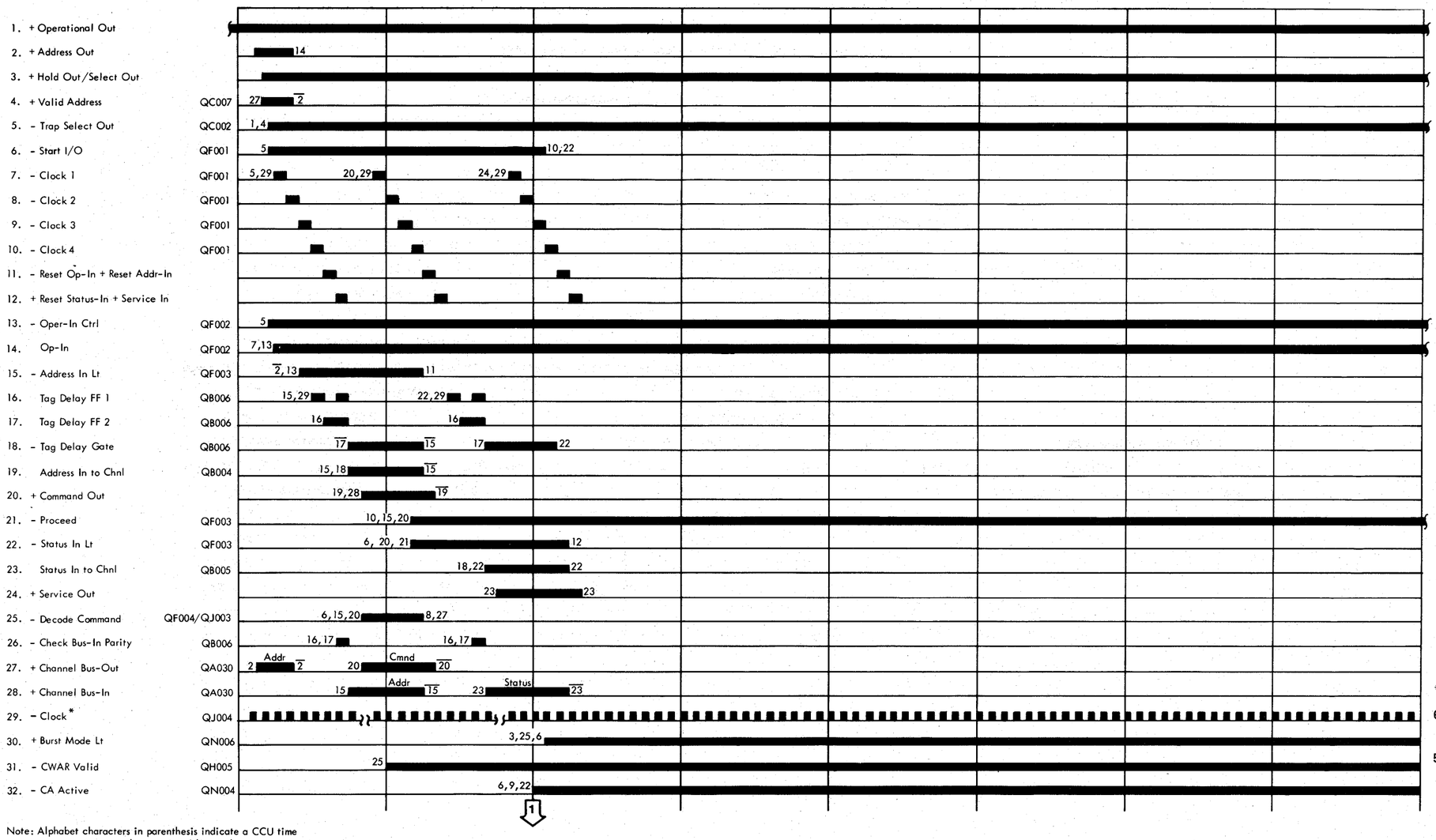
This bit is set when incorrect parity is detected in the byte presented to the channel bus-in. The most probable cause of this error is a failing channel driver card in socket S2.



The CACHKR is reset with an Output X'57', setting bit 1.2 on in the CA mode register (CAMR). Bit 1.2 resets the type 2 CA level 1 request. However, CACHKR bit 0.6 is reset when the adapter accepts a channel I/O command other than Sense, Test I/O, or No-Op.

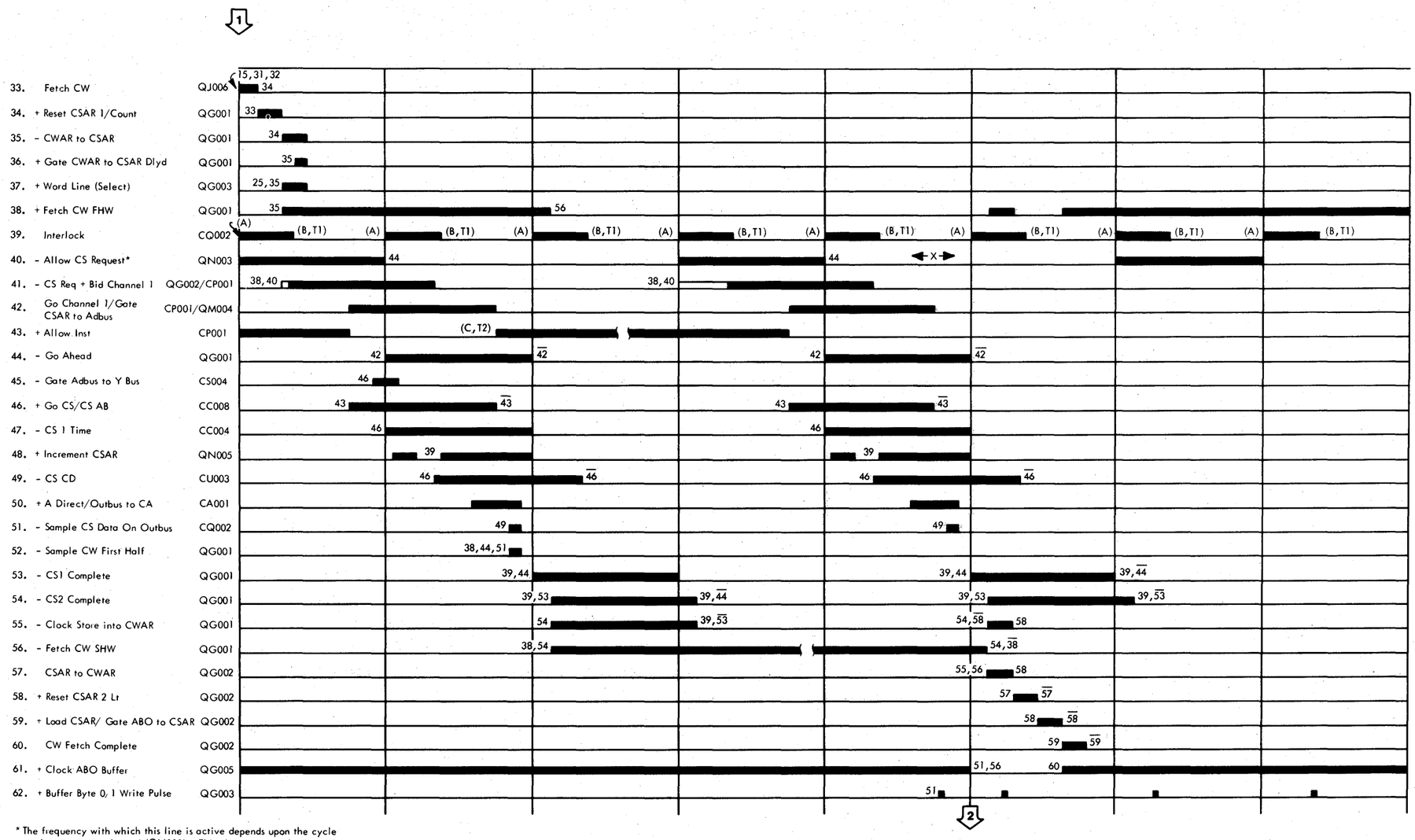
TYPE 2 CA TIMING

INITIAL SELECTION



Note: Alphabet characters in parenthesis indicate a CCU time necessary to cause the associated line to become active

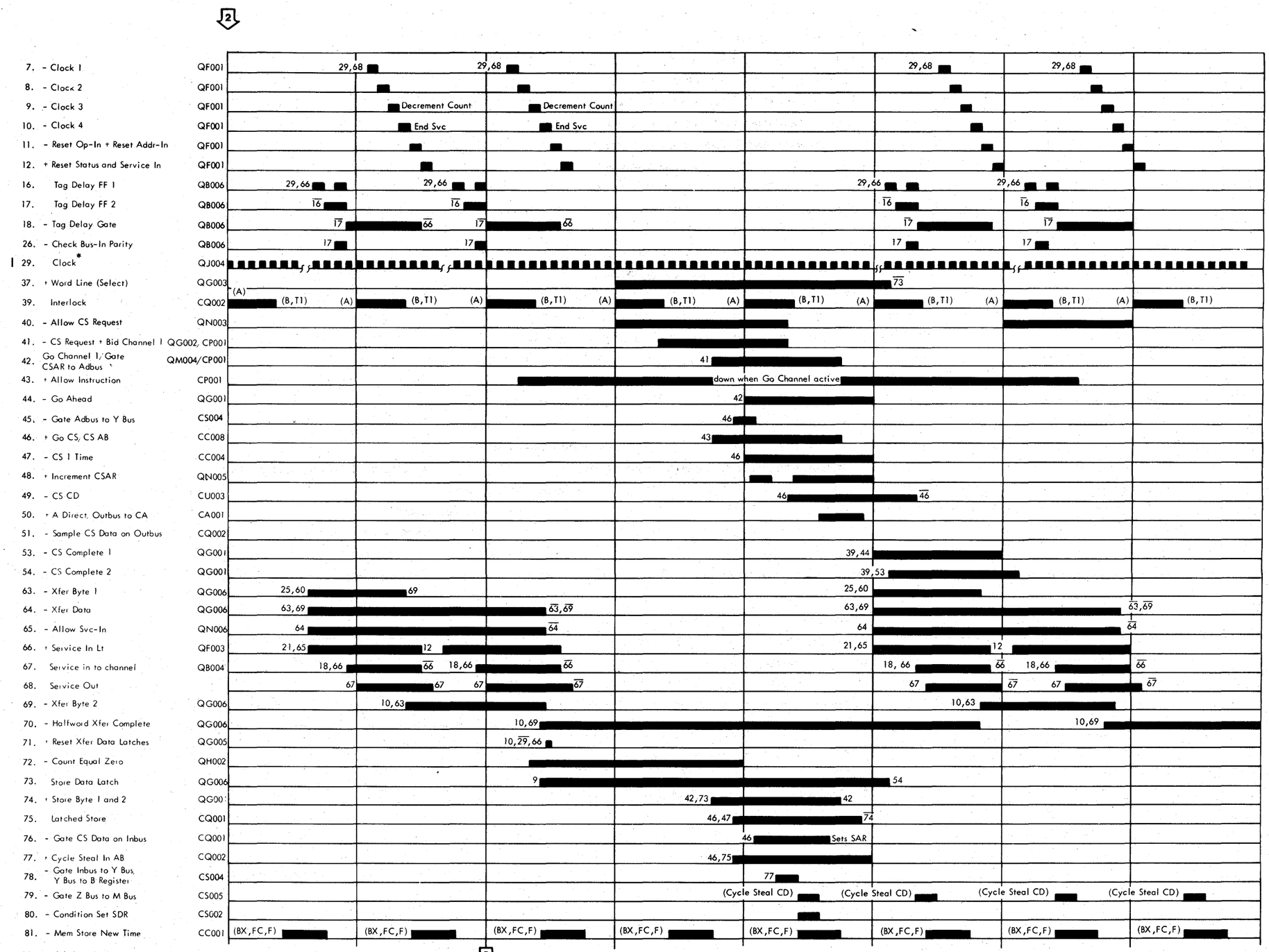
CONTROL WORD FETCH



* The frequency with which this line is active depends upon the cycle steal request rate plugged (QN003). This chart assumes the fastest possible rate 376 kilobytes.

Note: Alphabet characters in parenthesis indicate a CCU time necessary to cause the associated line to become active

WRITE COMMAND DATA TRANSFER



*50 Nsec = 3705-I

62.25 Nsec = 3705-II with 1 micro-second cycle time

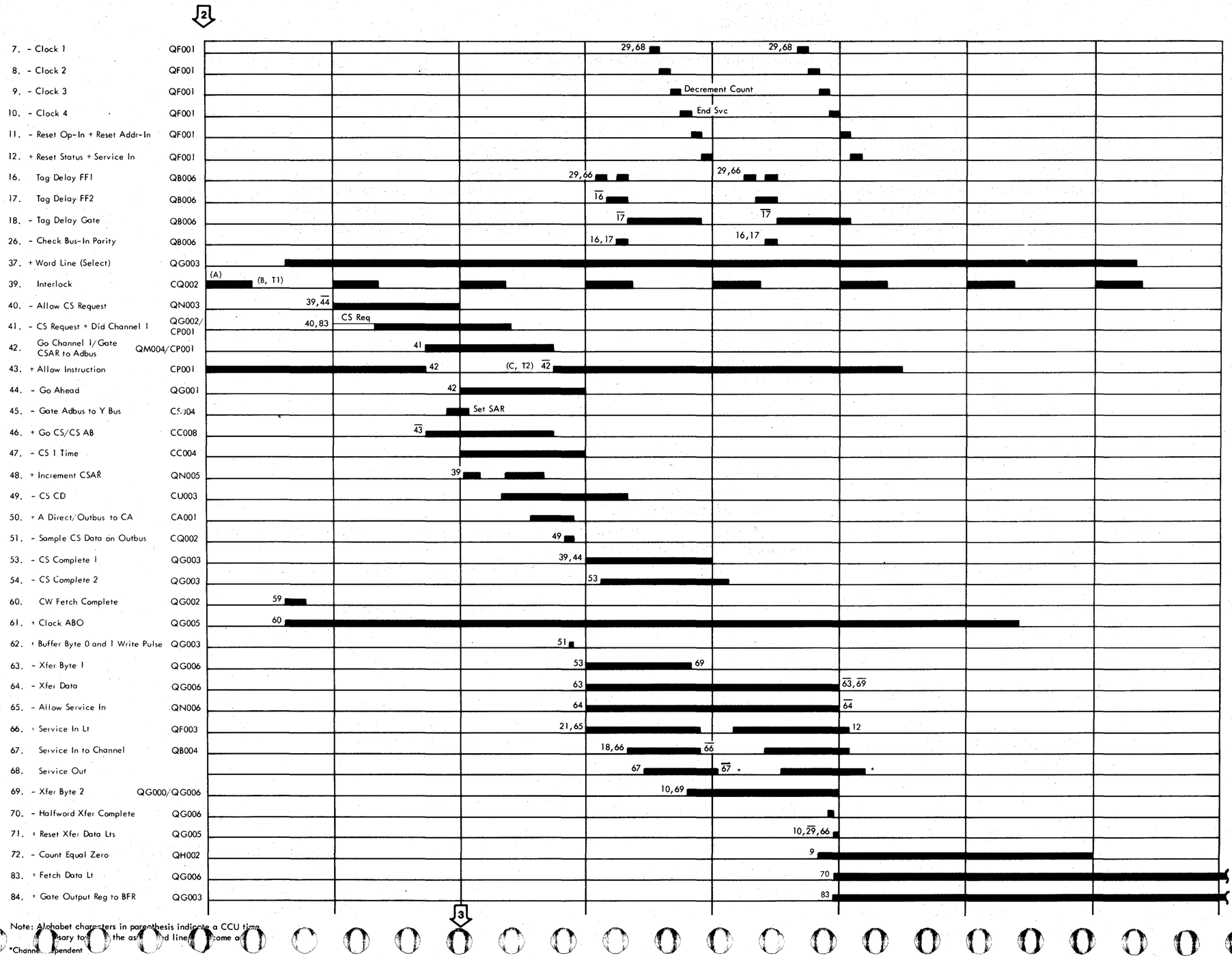
56.25 Nsec = 3705-II with 900 ns cycle time

Note: Alphabet characters in parenthesis indicate a CCU time necessary to cause the associated line to become active

3

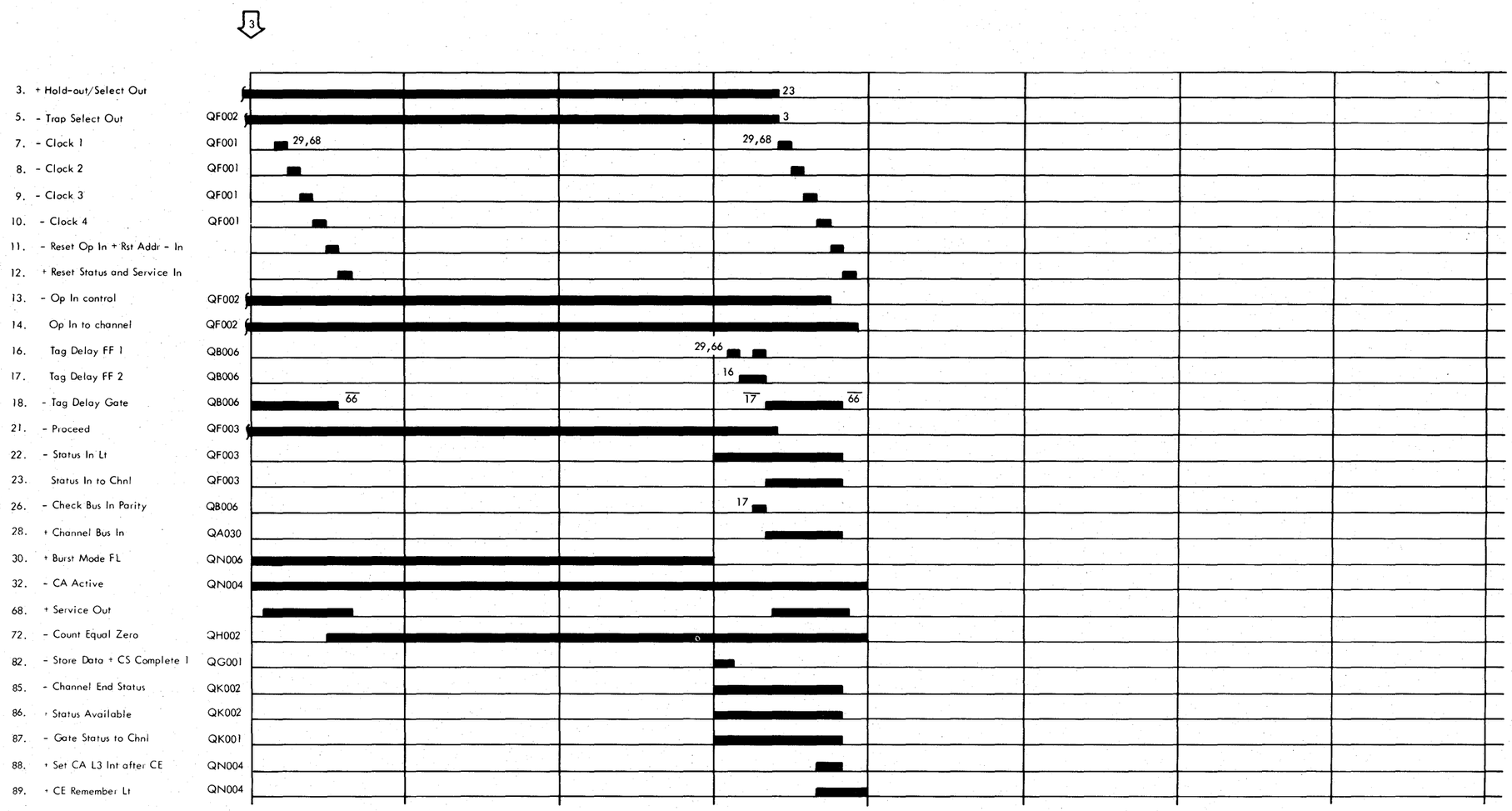
CA2

READ COMMAND DATA TRANSFER



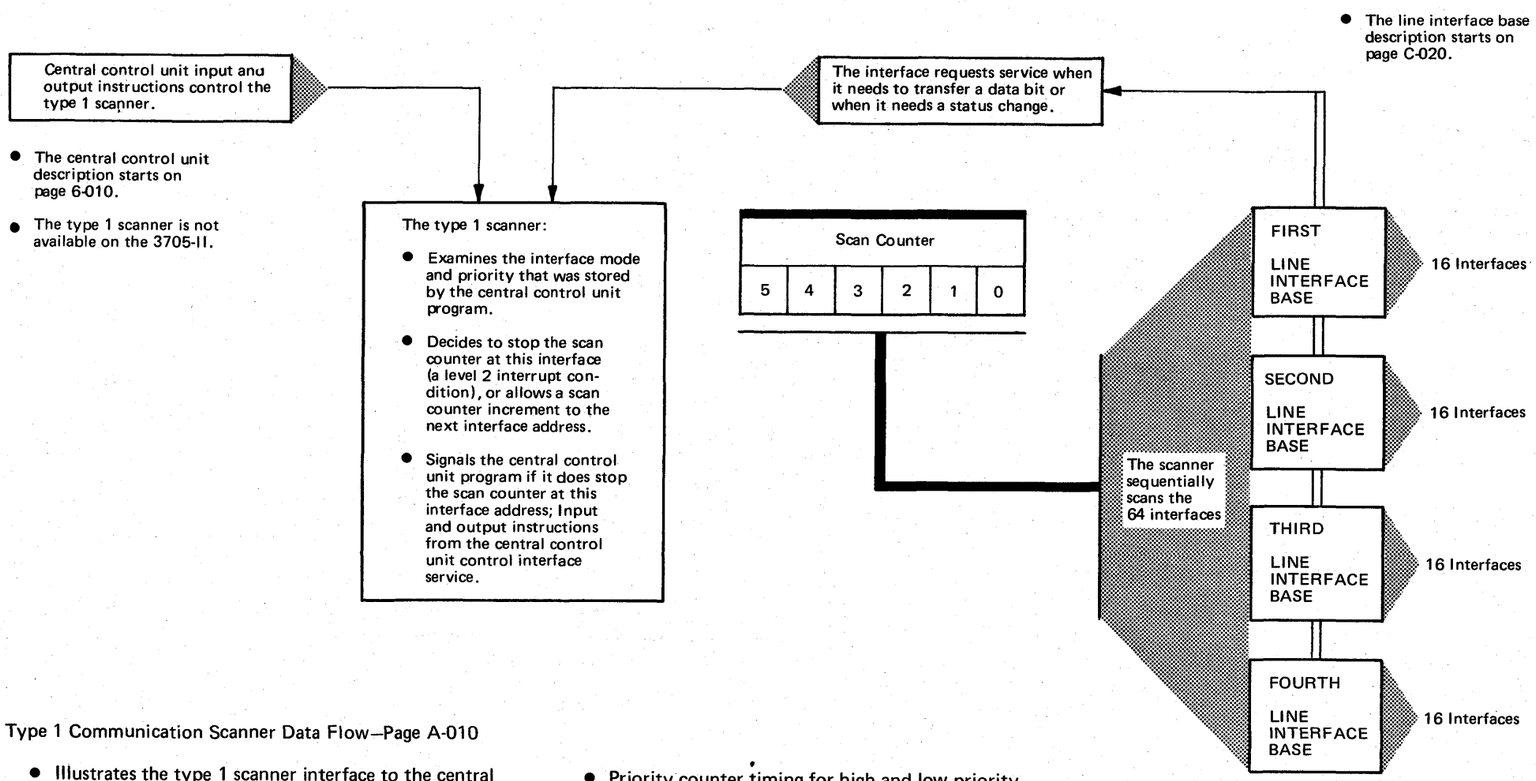
Note: Alphabet characters in parenthesis indicate a CCU time
sary to the asserted line come a
*Channel dependent

ENDING SEQUENCE



Note: Alphabet characters in parenthesis indicate a CCU time necessary to cause the associated line to become active

INTRODUCTION: TYPE 1 COMMUNICATION SCANNER



Type 1 Communication Scanner Data Flow—Page A-010

- Illustrates the type 1 scanner interface to the central control unit and the line interface base.
- A data flow drawing of the type 1 scanner.

Card Functions And Locations—Page A-020

- Illustrates the location of the type 1 scanner cards.
- Lists card functions by location, and provides reference to ALD pages.

Basic Timing: Type 1 Communication Scanner—Page A-030

Describes type 1 scanner timing for:

- Incrementing the scanner to the next interface address.
- Sampling bit service request from an interface.
- Sampling receive data from an interface.
- Setting the bit service L2 latch to stop the scan counter at an interface address and initiate a level 2 central control unit program interrupt.
- Priority counter timing for high and low priority interfaces.
- Character service governor timing to initiate a level 2 character service interrupt to the central control unit program.

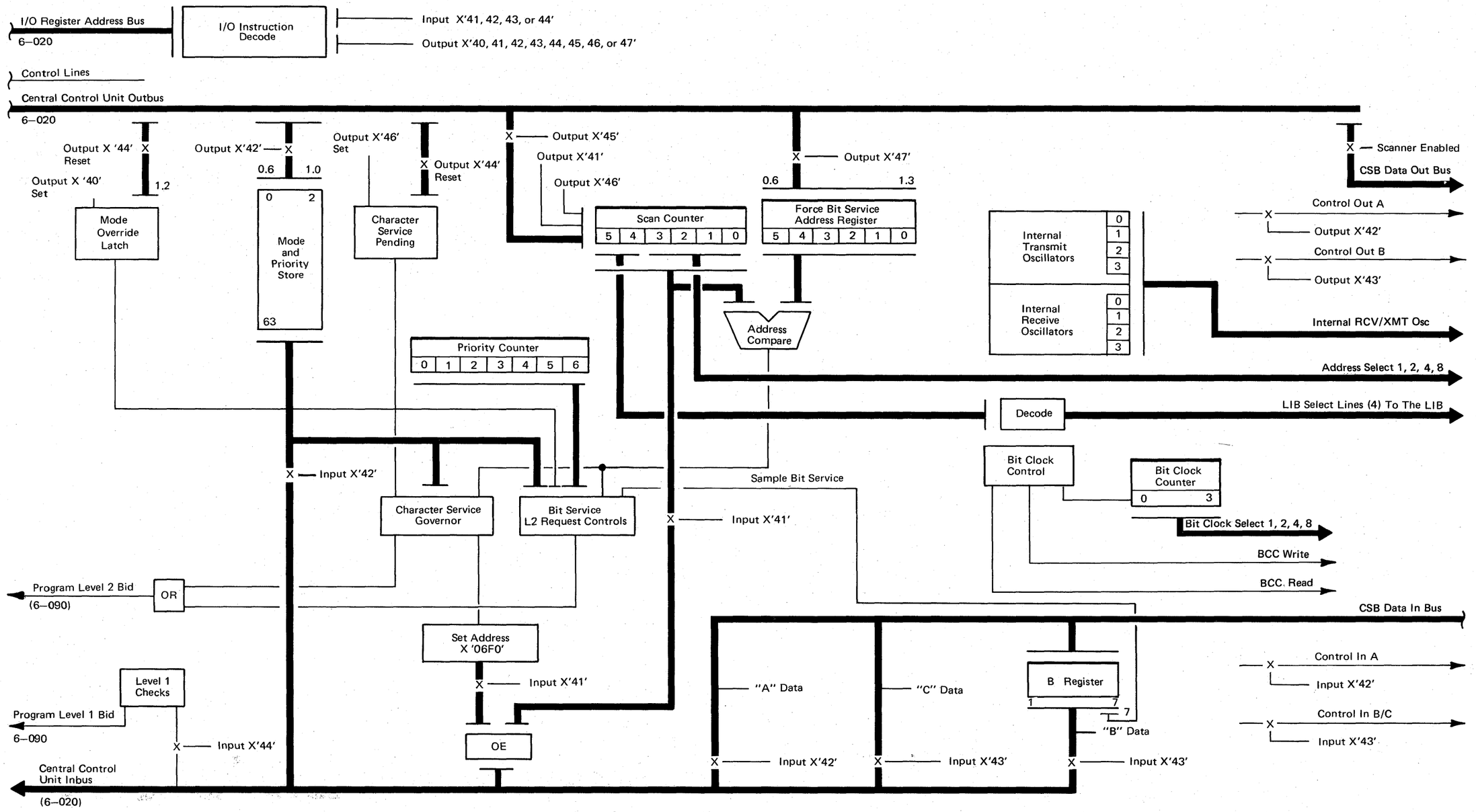
Type 1 Communication Scanner Input/Output Instructions—Page A-070

- Lists a sequence of input and output instructions to illustrate the interaction of the type a communication scanner hardware and the central control unit program.
- Provides a description of each of the type 1 scanner input and output instructions.

Diagnostic Wrap Mode—Page A-340

- Describes how the program uses the type 1 scanner 'test data' latch to transmit from one of the interface set to diagnostic wrap mode to one or more of the interfaces set to diagnostic wrap mode.

TYPE 1 COMMUNICATIONS SCANNER DATA FLOW

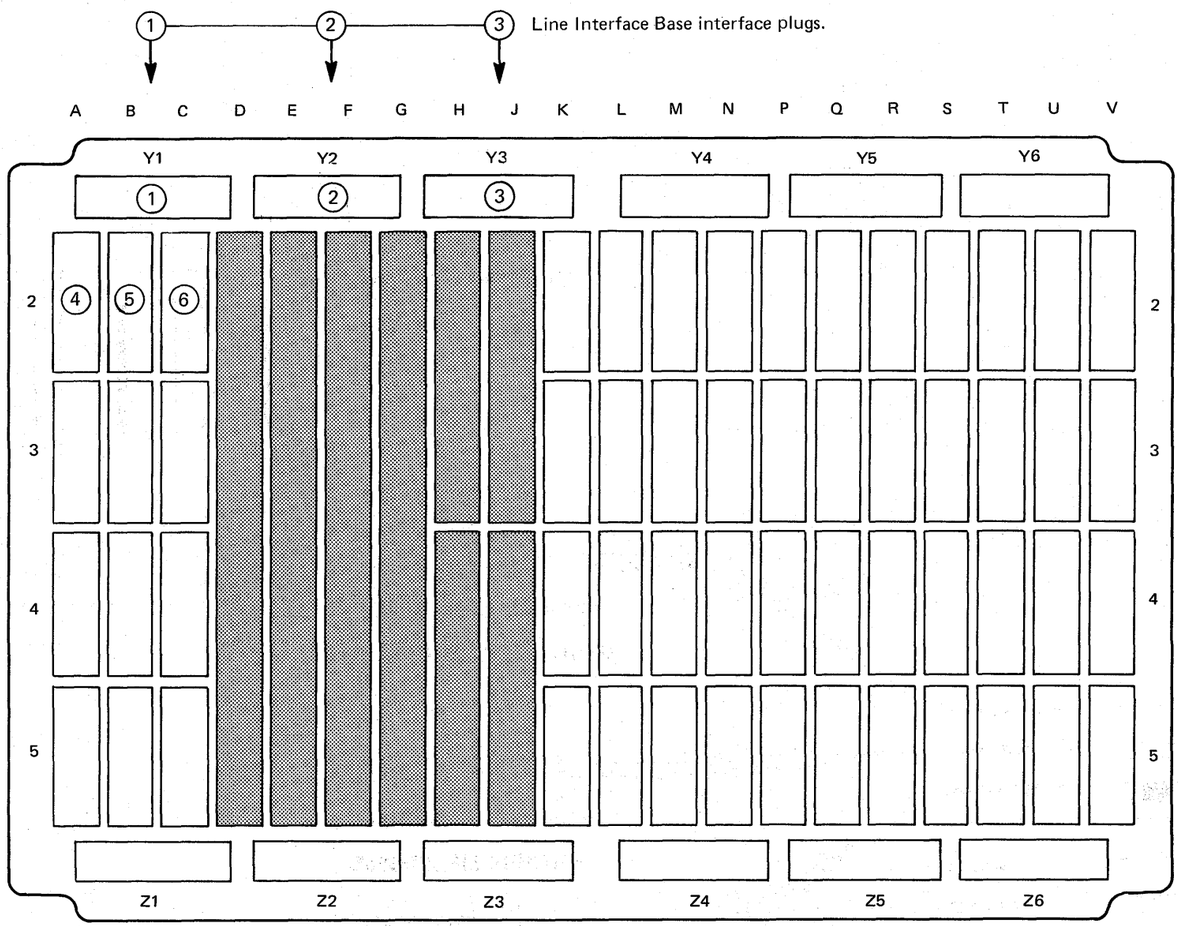


CARD FUNCTIONS AND LOCATIONS

Card Loc.	ALD Page	Function
Y4D2	RA101	• I/O Decodes (Type 1 Communication Scanner and Type 1 Channel Adapter).
	RA103	• Basic Clocking: 50 Nanosecond clock, and T0 through T3 time.
	RA104	• Central Control Unit Inbus Doting.
	RA106	• Central Control Unit Inbus Gating.
Y4E2	RS101	• Central Control Unit Outbus Termination.
	RS103	• Input/Output Instruction Gate, Sample, and Decode.
	RS104	• Output Instruction X'41', X'43', and X'46' Delay Control. • Mode Bit Override and Override Remember latches.
	RS105	• Latches: Character Service Pending, Diagnostic Bit Service, Scanner Enabled, and Test Data.
	RS106	• CSB Data Out Bus (to the Line Interface Base).
	RS107	• Data Controls to the Line Interface Base: 'control in A, B, and C', 'control out A and B'. • Mode and Priority Store Control (Stack Bits).
Y4F2	RS201	• Output 47 latch, and Force Bit Service Address Register.
	RS202	• Character Service Level 2 latch. • Feedback Check latch. • Bid Level 2 Interrupt signal (to the Central Control Unit).
	RS203	• "S-Ring": Basic timing for the Type 1 Communication Scanner.
	RS204	• Bit Clock Control Ring, and Bit Clock signals to the Line Interface Base.
	RS205	• Bit Clock Select Ring, and Bit Clock Select signals to the Line Interface Base.
	RS206	• Bit Clock Error Register, and Bit Clock Error signals from the Line Interface Base. • Disable LIB (Line Interface Base) Controls. • Address Error latch, and LIB address error signal from the Line Interface Base.
Y4G2	RS301	• Scan Counter (positions 1, 2, and 3). • Scan Counter (positions 4 and 5). • LIB (Line Interface Base) select lines (4) to the LIB.
	RS303	• Input Instruction X'41': gate scan counter to the Central Control Unit Inbus.
	RS304	• Mode and Priority Store (Interface Control Stack).
	RS305	• Low Priority Scan Counter. • Bit Service Level 2 Latch.
	RS306	• Input 'A' Data (from the Line Interface Base).
	RS307	• Input 'B' Data (from the Line Interface Base). • 'B' Data Sampling, and 'B Register'.
	RS308	• Input 'C' Data (from the Line Interface Base). • Reset Bit Service signal to the Line Interface Base.
Y4H2	RS401	• Internal Transmit and Receive Oscillator '0'. • Oscillator '0' signals to the Line Interface Base.
Y4H4	RS402*	• Internal Transmit and Receive Oscillator '1'. • Oscillator '1' signals to the Line Interface Base.
Y4J2	RS403*	• Internal Transmit and Receive Oscillator '2'. • Oscillator '2' signals to the Line Interface Base.
Y4J4	RS404*	• Internal Transmit and Receive Oscillator '3'. • Oscillator '3' signals to the Line Interface Base.

*Contains card P/N by bit rate

This board also houses the Type 1 Channel Adapter or the Remote Program Loader feature



01A-Y4*BOARD
CARD SIDE

* Y4 is the pseudo board location for the Type 1 Communication Scanner. The actual board location is 01A-A4.

BASIC TIMING: TYPE 1 COMMUNICATION SCANNER

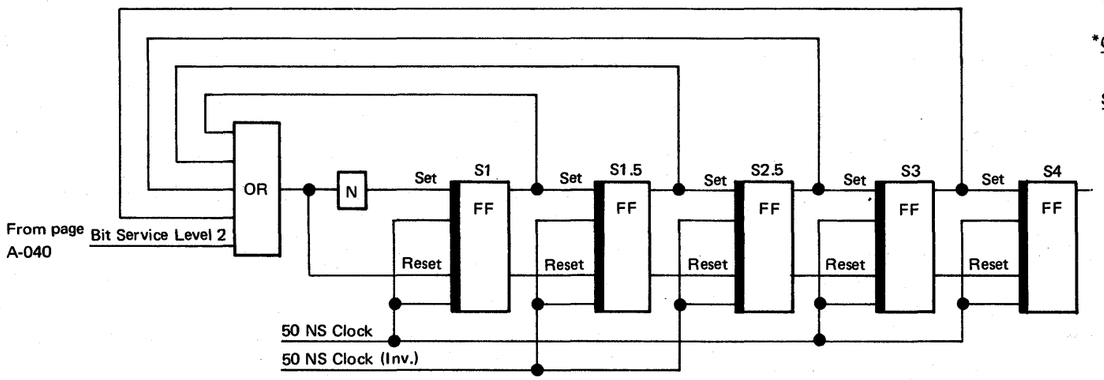
"S-RING" TIMING

- The "S-Ring" provides timing signals for:

  1. Incrementing the scanner to the next interface address.
  2. Sampling bit service requests from the interface the scanner is addressing.
  3. Sampling receive data from the interface the scanner is addressing.
  4. Setting the 'bit service level 2' latch.

The "S-Ring" does not advance to the next "S1" time when the 'bit service level 2' signal is on.

LOGIC REFERENCE: RS203



INCREMENT SCANNER

LOGIC REFERENCE: RS302

S1 Time
Not S1.5 Time
A
Increment Scanner

SAMPLE BIT SERVICE

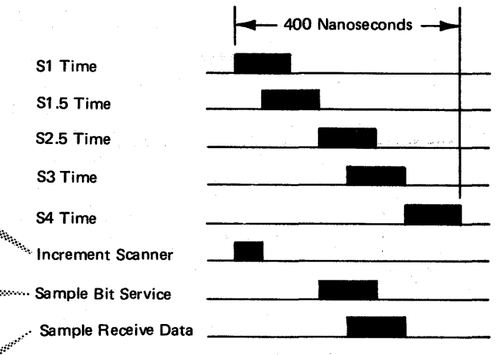
LOGIC REFERENCE: RS307

*CSB Data In 7
S2.5 Time
PH
Sampled Bit Service

SAMPLE RECEIVE DATA

LOGIC REFERENCE: RS307

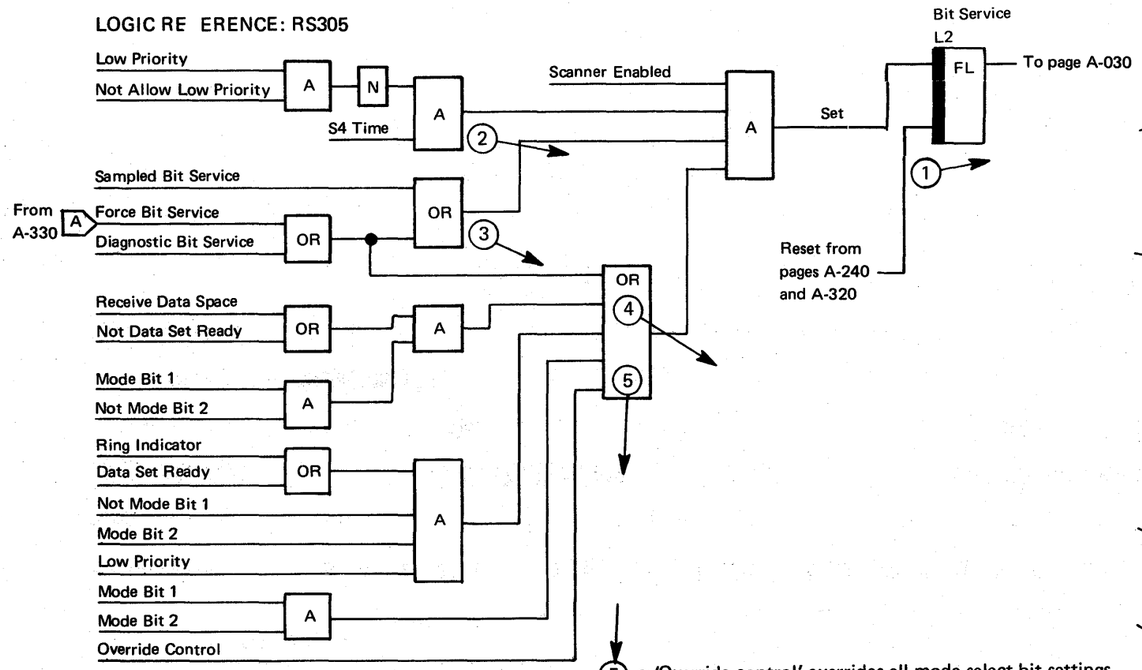
*CSB Data In 5
S3 Time
PH
Receive Data Space



*Communication Scanner Base

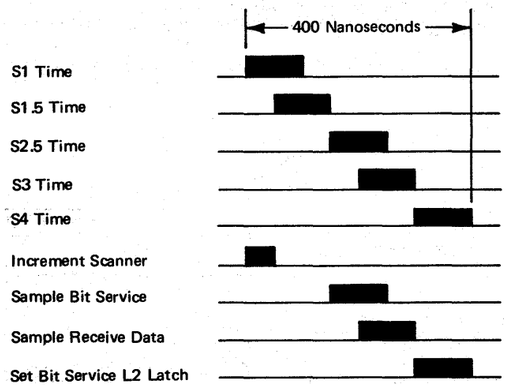
SET BIT SERVICE L2 LATCH

LOGIC RE ERENCE: RS305



5 • 'Override control' overrides all mode select bit settings except for a high priority interface in mode "01". 'Override control' is described on page A-230.

SET BIT SERVICE L2 LATCH TIMING



1 • The scanner "S-Ring" does not advance to the next "S1" time when the 'bit service level 2' latch is ON.

• 'Bit service level 2' latch on, stops the 'S ring' causing the scanner to stop on the interface it is addressing.

2 • The interface priority is set by Output Instruction X'42' to either high or low priority. A priority counter determines when a low priority line is serviced during a specific interface scan. The priority counter is described in more detail in the following page of this manual, "Priority Counter".

• The line 'not allow low priority' is from the priority counter. When 'not allow low priority' is on, the scanner services interrupts from high priority interfaces only. When 'not allow low priority' is off, the scanner services interrupts from high or low priority interfaces.

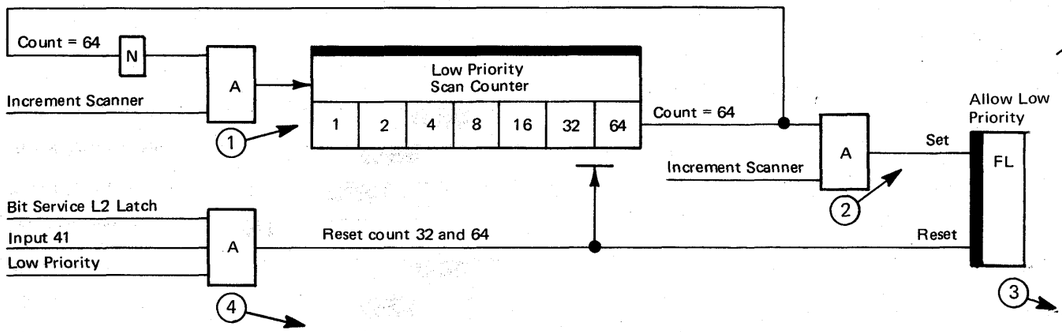
3 • Each time the scanner address the interface, 'bit service request' is sampled. Either 'force bit service' or 'diagnostic bit service' overrides the sampled bit service from the interface.

4 • Mode bit 1 and mode bit 2 (mode select bits) are set by Output Instruction X'42'. The program sets these mode select bits to select the conditions that set the 'bit service level 2' latch and stop the scanner when a bit service request is received from an interface. Either 'force bit service' or 'diagnostic bit service' overrides the mode select conditions for setting the 'bit service level 2' latch.

Mode Select Bits 1 2	Conditions Requiring Interface Service
0 0	• Diagnostic Bit Service Request • Force Bit Service Request
0 1	• Ring Indicator or Data Set Ready Active • Diagnostic Bit Service Request • Force Bit Service Request
1 0	• Space Received • Data Set Ready Inactive (off) • Diagnostic Bit Service Request • Force Bit Service Request
1 1	• Normal Bit Service Request (interrupt every bit time) • Diagnostic Bit Service Request • Force Bit Service Request

PRIORITY COUNTER

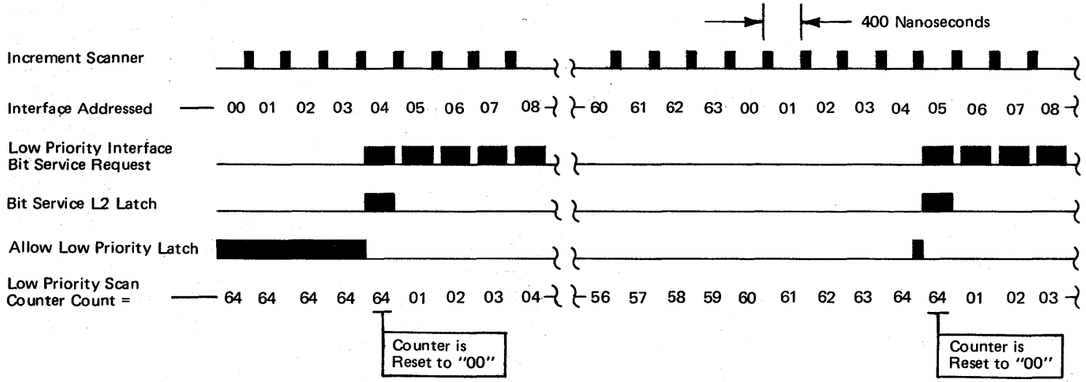
LOGIC REFERENCE: RS305



- (1) The low priority scan counter advances one count each time the scanner is incremented to a new interface address; the low priority scan counter does not advance after a count of 64 is reached.
- (2) The 'allow low priority' latch is set on the 'increment scanner' signal following a low priority scan counter count of 64.
- Starting at the last low priority interface serviced, 65 interfaces are addressed before the 'allow low priority' latch is set.
- (3) The 'bit service level 2' latch is not set when the scanner is addressing a low priority line and the 'allow low priority' latch is off. This logic is illustrated in note "(2)" on page A-040.
- The Bit Service Level 2 latch is set when the scanner is addressing a low priority line, and the 'allow low priority' latch is on.
- (4) The 'allow low priority' latch is reset, and the low priority scan counter is reset to a "0" count when the program issues an Input X'41' instruction for a low priority line that has stopped the scanner ('bit service level 2' is on).

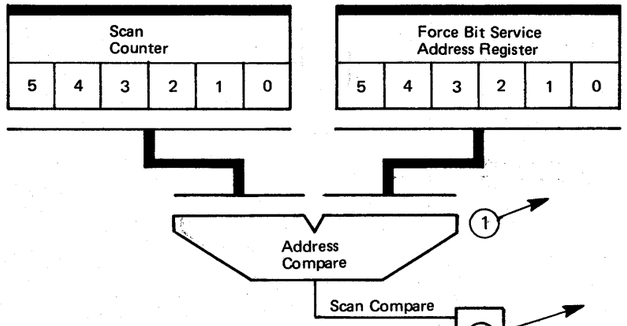
LOW PRIORITY INTERFACE SCAN EXAMPLE

Assume that:
1. Low priority interfaces "04", "05", "06", "07", and "08" are requesting bit service.
2. The mode select set by Output instruction X'42' for each of these low priority interfaces is "11" (allow a level 2 interrupt every bit time).

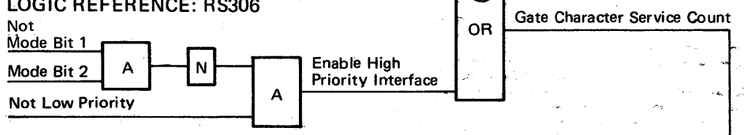


CHARACTER SERVICE GOVERNOR

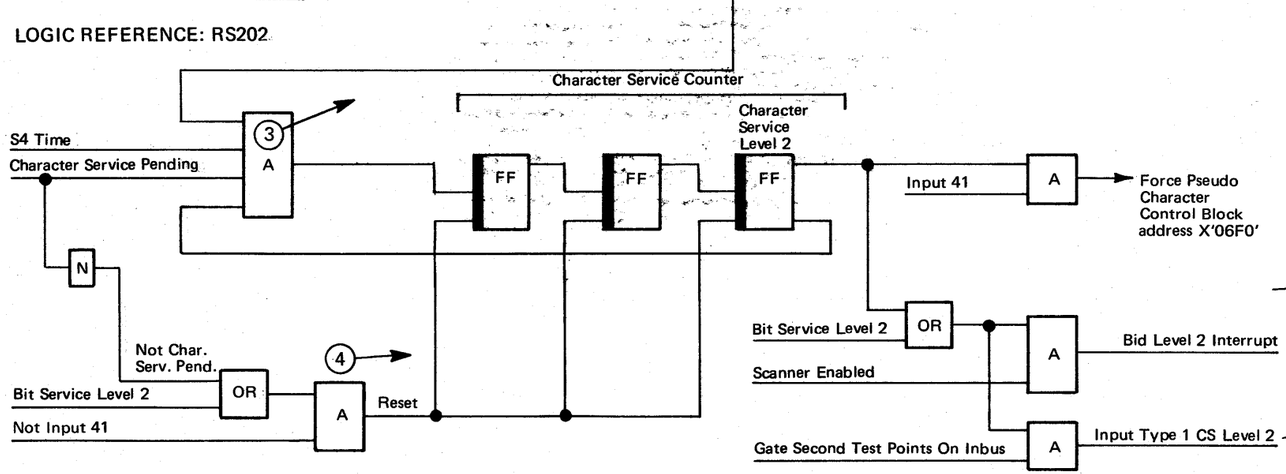
LOGIC REFERENCE: RS201



LOGIC REFERENCE: RS306



LOGIC REFERENCE: RS202



1 • A 'scan compare' occurs each time the interface address in the scan counter is equal to the interface address stored in the force bit service address register by the last output instruction X'47'.

• A 'scan compare' occurs once for each scan of the 64 interfaces.

2 • The 'gate character service count' signal occurs once for each scan of the 64 interfaces, and each time the scanner addresses a high priority interface that is not in mode select "01".

3 • Character service level 2 sets on the fourth 'gate character service count' after the character service pending latch sets.

• A character service level 2 interrupt occurs after the program sets the character service pending Latch, and any one of these three conditions occur without an intervening bit service interrupt:

1. All 64 interfaces are scanned four times.
2. Four high priority interfaces, not in mode select "01", are scanned.
3. Any combination of four occurrences of:
   (a) All 64 interfaces are scanned once.
   (b) A high priority interface, that is not in mode select "01", is scanned.

For example, all 64 interfaces scanned three times, and a high priority interface (not in mode select "01") addressed once is a combination of four occurrences.

4 • The character service count and character service level 2 reset when the program resets the character service pending latch via an output instruction X'44'.

The central control unit uses these signals to determine that the bit or character service level 2 interrupt is from the type 1 communication scanner. Level 2 interrupt is described on page 6-090.

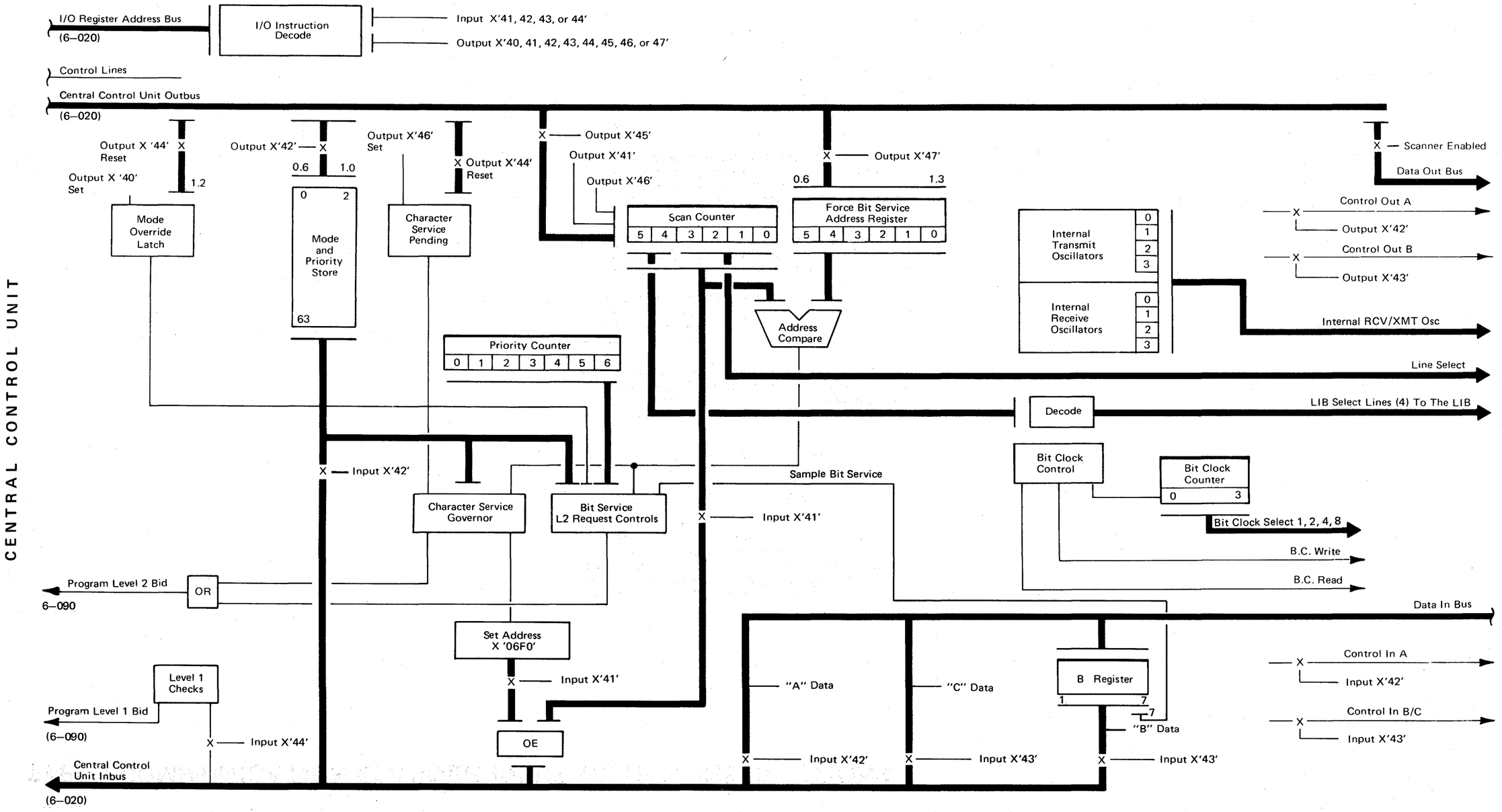
TYPE 1 COMMUNICATION SCANNER INPUT/OUTPUT INSTRUCTIONS

The type 1 communication scanner and the line interface bases it supports are controlled by input/output instructions from the central control unit. Each input or output instruction transfers to the scanner on the "I/O register address" bus. Page A-130 describes the input and output instruction decode.

An example of a series of input/output instructions follows; this example is not an actual program, it is a sequence of input/output instructions that illustrates the interaction of the type 1 communication scanner hardware and the program.

- "Initial Service Of The Interface"—stops the scanner at an interface address, sets the mode and service priority of the interface, sets the state of the data set or auto call unit interface leads, and restarts the scanner.
- "Bit Service: Transmit or Receive"—identifies the interface that stopped the scanner and requested service, transfers a data bit to or from the interface, checks for error conditions, and restarts the scanner.
- "Character Service: Transmit or Receive"—identifies the interface that stopped the scanner and requested service, initiates character service, checks for error conditions, and restarts the scanner.
- "Auto Call Unit Interface"—identifies the interface that stopped the scanner and requested service, transfers control signals to or from the auto call unit interface, checks for error conditions, and restarts the scanner.

TYPE 1 COMMUNICATIONS SCANNER DATA FLOW



INPUT/OUTPUT SEQUENCE EXAMPLE

Turn to the page listed with each input or output instruction for a more detailed description of the instruction.

INITIAL SERVICE OF THE INTERFACE

A Output Instruction X'47'
Force Bit Service Request—
Page A-330

The program:
- Transfers the interface address set in the "R" field general register to the scanner on the central control unit outbus.

The scanner:
- Stores the interface address in the Force Bit Service Address register.
- Stops and initiates a level 2 interrupt when the Scan Counter and Force Bit Service Address register interface addresses are equal.

LEVEL 2 INTERRUPT

B Input Instruction X'77'
Adapter Interrupt Group
2—Page 6-820

The program:
- Determines that this interrupt is from the type 1 scanner.

C Input Instruction X'44'
Status—Page A-210

The scanner:
- Transfers the status of character service pending, scanner enabled, and error conditions for this interface to the "R" field general register.

The program:
- Checks the status of the interface.

D Input Instruction X'41'
Interface Address—Page A-140

The scanner:
- Transfers the scan counter interface address to the "R" field general register.
  This register now contains the Hex address of the bit control block for the interface the scanner is addressing; the scanner is stopped at this address.

E Output Instruction X'42'
Control A—Page A-250

The program:
- Sets bits in the "R" field general register to select the interface mode and priority, selects normal or diagnostic mode, and selects the state of interface leads to the data set.

The scanner:
- Stores the interface mode and priority.
  The mode/priority storage provides 3 bit storage (2 mode bits and 1 priority bit) for each of the 64 interfaces.
- Transfers the "R" field general register diagnostic mode bit and the data set interface state bits to the CSB data out bus (the data bus to the line interface base).
- Transfers the 'control out A' signal to the line interface base; 'control out A' defines the data on the CSB data out bus.

F Input Instruction X'42'
Control A—Page A-150

The scanner:
- Transfers the 'control in A' signal to the line interface base. The line interface base transfers the status of the interface to the scanner when 'control in A' is received, This status transfers to the CSB data in bus.
- Transfers the following information to the "R" field general register:
  (1) The interface status received on the CSB data in bus.
  (2) Mode bits 1 and 2, and the priority bit read from mode/priority storage.

The program:
- Checks the status of the interface mode and data set interface leads.

G Output Instruction X'43'
Control B—Page A-280

The program:
- Sets bits in the "R" field general register to select one of the following:
  (1) Data Set Interface: transmit or receive mode, data set 'request to send' lead ON or OFF, data set 'new sync' lead ON or OFF, and the send data bit MARK or SPACE.
  (2) Auto Call Unit (ACU)
  Interface: ACU 'digit present' lead ON or OFF, ACU 'call request' lead ON or OFF, and the next dial digit.

The scanner:
- Transfers the "R" field general register bits to the CSB Data Out Bus (the data bus to the Line Interface Base).
- Transfers the 'control out B' signal to the line interface base; 'control out B' defines the data on the CSB data out bus.

H Input Instruction X'43'
Control B/C—Page A-180

The scanner:
- Transfers the 'control in B' signal to the Line Interface Base (LIB). The LIB transfers the 'B' data part of the data set or auto call unit interface status to the scanner B register; This status is transferred on the CSB data in bus.
- Transfers the 'control in C' signal to the LIB. The LIB transfers the the 'C' data part of the data set or auto call unit interface status to the scanner; This status is also transferred on the CSB data in bus.
- Transfers 'B' data from the scanner B Register, and 'C' data from CSB data in bus to the "R" field general register. This data is transferred on the central control unit in bus.

The program:
- Check the status of the data set or auto call unit interface leads.

J Output Instruction X'41'
Start Scanner and Reset
Bit Service Level 2—Page A-240

The scanner:
- Transfers the 'reset bit service' signal to the LIB.
- Performs a feedback check to determine that the 'bit service' signal from the LIB is OFF.
- Resets the bit service level 2 latch. The scan counter increments to the next interface address.

The program:
- Waits for the next level 2 interrupt from the interface.
- Has selected the interface mode and priority.
- Has set the interface to transmit or receive mode.

The next level 2 interrupt from this interface will be for bit service.

INPUT/OUTPUT SEQUENCE EXAMPLE (CONTINUED)

BIT SERVICE: TRANSMIT OR RECEIVE

Turn to the page listed with each input or output instruction for a more detailed description of the instruction.

- Assume that the program completed the "Initial Service Of The Interface" procedure on page A-090. The state of data set interface leads are selected; And the interface was placed in transmit or receive mode. This level 2 interrupt from the interface is for bit service.

LEVEL 2 INTERRUPT

(A) Input Instruction X'77'
Adapter Interrupt Group 2—Page 6-820

The program:
- Determines that this interrupt is from the type 1 scanner.

(B) Input Instruction X'44'
Status—Page A-210

The scanner:
- Transfers the status of character service pending, scanner enabled, and error conditions for this interface to the "R" field general register.

The program:
- Checks the status of the interface.

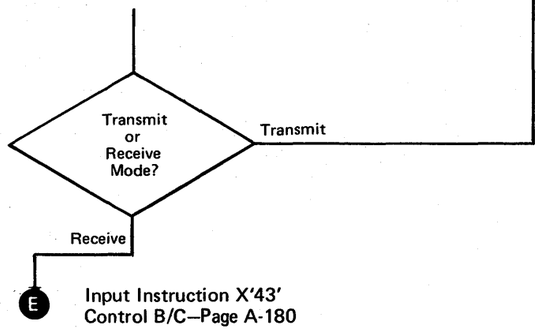
(C) Input Instruction X'41'
Interface Address—Page A-140

The scanner:
- Transfers the scan counter interface address to the "R" field general register.
  The input instruction X'41' "R" field general register now contains the Hex address of the bit control block for the interface the scanner is addressing; the scanner is stopped at this address.

(D) Input Instruction X'42'
Control A—Page A-150

The scanner:
- Transfers the 'control in A' signal to the line interface base. The line interface base transfers the status of the interface to the scanner when 'control in A' is received; This status transfers on the CSB data in bus.
- Transfers the following information to the "R" field general register:
  (1) The interface status received on the CSB data in bus.
  (2) Mode bits 1 and 2, and the priority bit read from mode/priority storage.

The program:
- Checks the status of the interface mode and data set interface leads.



(E) Input Instruction X'43'
Control B/C—Page A-180

The scanner:
- Transfers the 'control in B' signal to the line interface base (LIB). The LIB transfers the 'B' data part of the data set interface or auto call unit interface status to the scanner B Register; This status transfers on the CSB data in bus.
- Transfers the 'control in C' signal to the LIB. The LIB transfers the the 'C' data part of the data set interface status to the scanner; This status also transfers on the CSB data in bus.
- Transfers 'B' data from the scanner B Register, and 'C' data from the CSB data in bus to the "R" field general register. This data is transferred on the Central Control Unit Inbus.

The program:
- Checks the status of the data set interface leads.
- Transfers the receive data bit (MARK or SPACE) to the bit control block.

Continue this sequence at step "8".

(F) Output Instruction X'43'
Control B—Page A-280

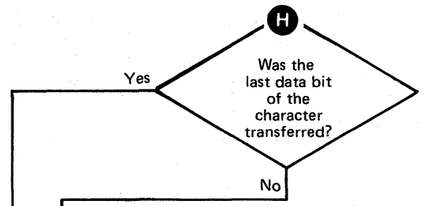
The program:
- Sets bits in the "R" field general register to select: transmit mode, data set 'request to send' lead ON, data set 'new sync.' lead ON or OFF, and the send data bit MARK or SPACE.

The scanner:
- Transfers the "R" field general register bits to the CSB data out bus (the data bus to the line interface base).
- Transfers the 'control out B' signal to the line interface base; 'control out B' defines the data on the CSB data out bus.

(G) Input Instruction X'43'
Control B/C—Page A-180

The scanner:
- Transfers the 'control in B' signal to the line interface base (LIB). The LIB transfers the 'B' data part of the data set interface status to the scanner B Register; This status transfers on the CSB data in bus.
- Transfers the 'control in C' signal to the LIB. The LIB transfers the 'C' data part of the data set interface or auto call unit interface status to the scanner; This status also transfers on the CSB data in bus.
- Transfers 'B' data from the scanner B register, and 'C' data from the CSB data in bus to the "R" field general register. This data transfers on the central control unit inbus.

The program:
- Checks the status of the data set interface leads.



(J) Output Instruction X'41'
Start Scanner and Reset Bit Service Level 2—Page A-240

The scanner:
- Transfers the 'reset bit service' signal to the LIB.
- Performs a feedback check to determine that the 'bit service' signal from the LIB is OFF.
- Resets the 'bit service level 2' latch. The scan counter increments to the next interface address.

The program:
- Waits for the next level 2 interrupt from the interface. The interface mode and priority are selected. The state of data set interface leads are selected, the interface was placed in transmit or receive mode, and a data bit was transferred to or from the interface. The next level 2 interrupt from the interface will be for bit service.

(A) Output Instruction X'46'
Set Character Service Pending—Page A-320

The scanner:
- Sets the 'character service pending' latch.
- Transfers the 'reset bit service' signal to the LIB.
- Performs a feedback check to determine that the 'bit service' signal from the LIB is OFF.
- Resets the 'bit service level 2' latch. The scan counter increments to the next interface address.

The program:
- Posts the interface address in a character service waiting list, and continues processing until the character service L2 interrupt occurs.

INPUT/OUTPUT SEQUENCE EXAMPLE (CONTINUED)

CHARACTER SERVICE: TRANSMIT OR RECEIVE OPERATION

Turn to the page listed with each input or output instruction for a more detailed description of the instruction.

Assume that:
- The program completed the "Initial Service Of The Interface" sequence on page A-090.
- The 'character service pending' latch was set when performing the "Bit Service: Transmit or Receive" sequence on page A-100.
- The Character Service Governor (described on page A-060) set 'character service level 2' to the ON condition; this level 2 interrupt is for character service.

LEVEL 2 INTERRUPT

(A) Input Instruction X'77'
Adapter Interrupt Group 2—Page 6-820

The program:
- Determines that this interrupt is from the type 1 scanner.

(B) Input Instruction X'44'
Status—Page A-210

The scanner:
- Transfers the status of character service pending, scanner enabled, and error conditions for the interface the scanner is addressing to the "R" field general register. The scanner does not stop when requesting a character service level 2 interrupt.

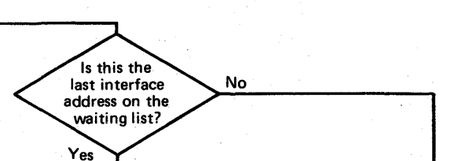
The program:
- Checks the status of the interface.

(C) Input Instruction X'41'
Interface Address—Page A-140

The scanner:
- Transfers address X'06F0' (the address of the 'pseudo character control block') to the "R" field general register.

The program:
- Gets an interface address from a character service waiting list.

(D)



(E) Output Instruction X'44'
General Control—Page A-300

The scanner:
- Resets the 'character service pending' latch.
- Resets the 'character service pending' latch, and character service governor; this reset is described on page a A-060.

The program:
- Uses the interface address from the character service waiting list to transfer a character to-or-from the interface bit control block.
- Has serviced all character service requests on the character service waiting list. The next level 2 interrupt from the scanner will be for bit service.

(F)

The program:
- Uses the interface address from the character service waiting list to transfer a character to-or-from the interface bit control block.
- Waits for the next level 2 interrupt from the scanner, which will be for bit service.

INPUT/OUTPUT SEQUENCE EXAMPLE (CONTINUED)

AUTO CALL UNIT INTERFACE

Turn to the page listed with each input or output instruction for a more detailed description of the instruction.

Assume that:
- The program completed the "Initial Service Of The Interface" sequence on page A-090; the state of the auto call unit interface leads was set to transfer digits of the telephone number to the interface.
- This level 2 interrupt is for bit service; A digit of the telephone number transfers to the auto call unit interface.

LEVEL 2 INTERRUPT

A Input Instruction X'77'
Adapter Interrupt Group 2—Page 6-820

The program:
- Determines that this interrupt is from the type 1 scanner.

B Input Instruction X'44'
Status—Page A-210

The scanner:
- Transfers the status of character service pending, scanner enabled, and error conditions for this interface to the "R" field general register.

The program:
- Checks the status of the interface.

C Input Instruction X'41'
Interface Address—Page A-140

The scanner:
- Transfers the scan counter interface address to the "R" field general register.
  The input instruction X'41' "R" field general register now contains the Hex address of the bit control block for the interface the scanner is addressing; the scanner is stopped at this address.

D Input Instruction X'42'
Control A—Page A-150

The scanner:
- Transfers the 'control in A' signal to the line interface base. The line interface base transfers the status of the interface to the scanner when 'control in A' is received; this status transfers on the CSB data in bus.
- Transfers the following information to the "R" field general register.
  (1) The interface status received on the CSB data in bus.
  (2) Mode bits 1 and 2, and the priority bit read from mode/priority storage.

The program:
- Checks the status of the interface mode and data set interface leads.

E Input Instruction X'43'
Control B/C—Page A-180

The scanner:
- Transfers the 'control in B' signal to the line interface base (LIB). The LIB transfers the the 'B' data part of the auto call unit interface status to the scanner B register; This status transfers on the CSB data in bus.
- Transfers the 'control in C' signal to the LIB. The LIB transfers the the 'C' data part of the auto call unit interface status to the scanner; this status also transfers on the CSB data in bus.
- Transfers 'B' data from the scanner B register, and 'C' data from CSB data in bus to the "R" field general register. This data is transferred on the Central Control Unit Inbus.

The program:
- Checks the status of the auto call unit interface leads.

F Output Instruction X'43'
Control B—Page A-280

The program:
- Sets bits in the "R" field general register to select: The dial digit, the 'digit present' lead to ON, and the 'call request' lead to ON.

The scanner:
- Transfers the "R" field general register bits to the CSB data out bus (the data bus to the line interface base).
- Transfers the 'control out B' signal to the line interface base; 'control out B' defines the data on the CSB data out bus.

G Input Instruction X'43'
Control B/C—Page A-190

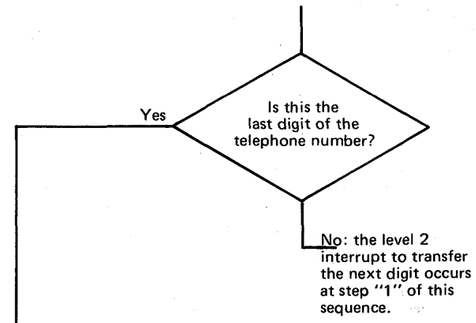
The scanner:
- Transfers the 'control in B' signal to the line interface base (LIB). The LIB transfers the the 'B' data part of the auto call unit interface status to the scanner B register; this status transfers on the CSB data in bus.
- Transfers the 'control in C' signal to the LIB. The LIB transfers the the 'C' data part of the auto call unit interface status to the scanner; this status also transfers on the CSB data in bus.
- Transfers 'B' data from the scanner B register, and 'C' data from CSB data in bus to the "R" field general register. This data transfers on the central control unit inbus.

The program:
- Checks the status of the auto call unit interface leads.

H Output Instruction X'41'
Start Scanner and Reset Bit
Service Level 2—Page A-240

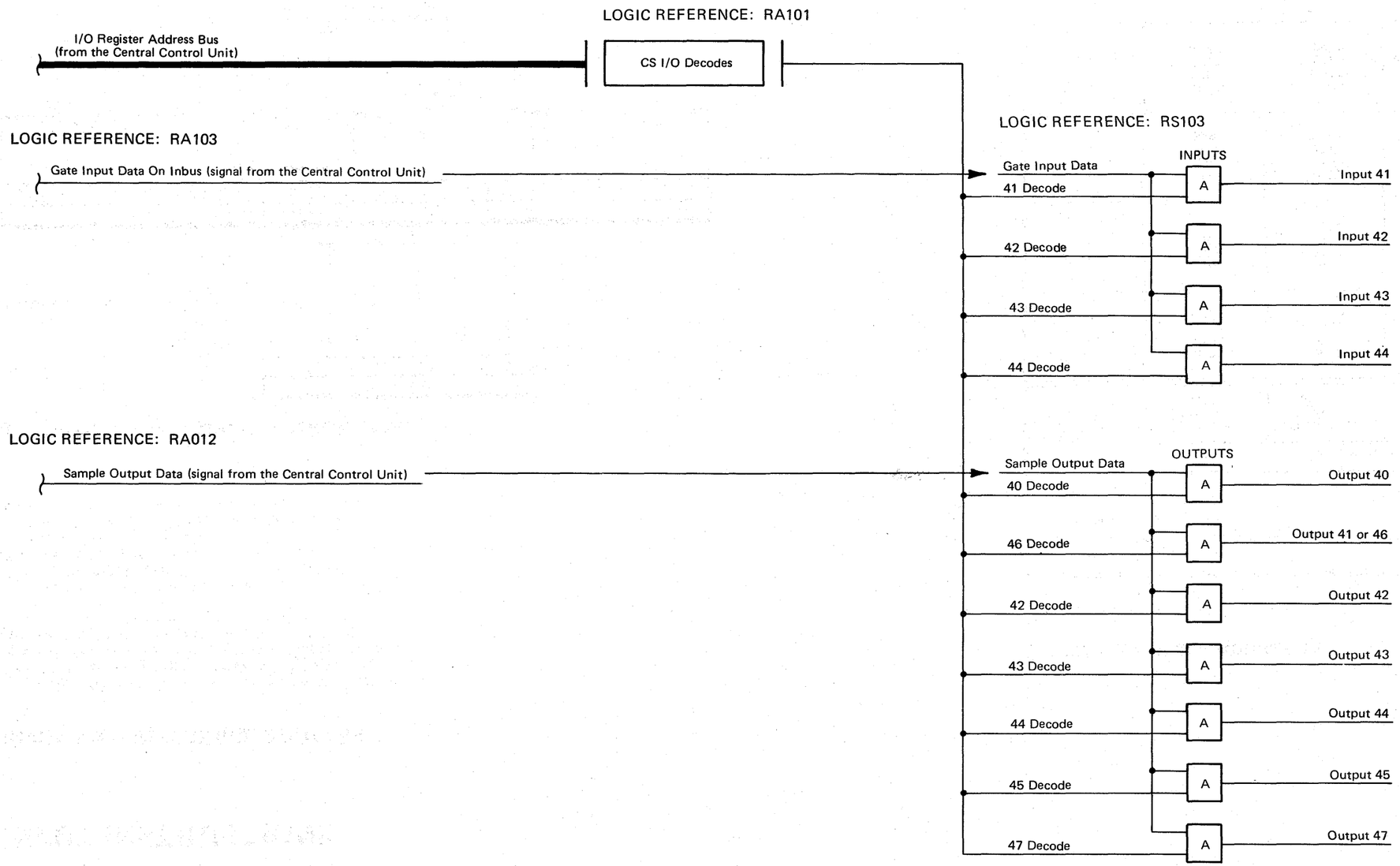
The scanner:
- Transfers the 'reset bit service' signal to the LIB.
- Performs a feedback check test to determine that the 'bit service' signal from the LIB is OFF.
- Resets the 'bit service level 2' latch. The scan counter increments to the next interface address.

The program:
- Has transferred a digit of the telephone number to the auto call unit interface.
- Waits for the next level 2 interrupt from the interface.



- The auto call unit automatically connects the communications line to the data set when the telephone call is completed.
- The program performs the "Initial Service Of The Interface" procedure on page A-090 when the data set that is attached to the auto call unit is in a ready condition; the data set is ready when the 'data set ready' signal is ON. The program checks the status of 'data set ready' during the initial service of the interface procedure.

INPUT/OUTPUT INSTRUCTION DECODE



INPUT INSTRUCTIONS

INPUT X'41' INTERFACE ADDRESS

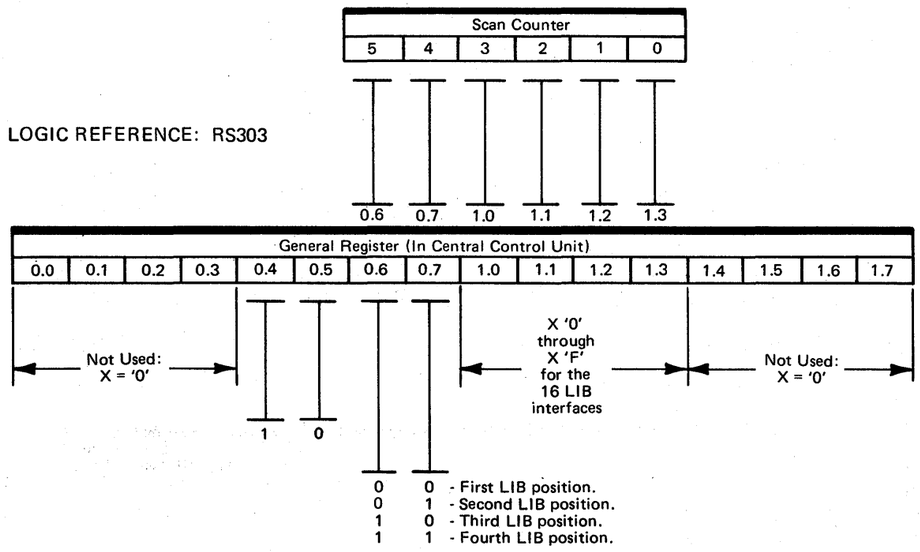
The Input X'41' instruction loads a general register with the Hex address of the Bit Control Block (BCB) that is used with the interface the scanner is addressing. Each time the scanner stops because of a bit-service request, this input may be issued to determine which interface caused the request.

If the level 2 interrupt is the result of a character-service request, the address loaded into the register is X'06F0'. This is the address of the pseudo character control block used for character service handling.

Note: The Input X'41' instruction should be executed only when a level 2 interrupt has occurred.

BIT CONTROL BLOCK ADDRESS GENERATION:

LOGIC REFERENCE: RS303



Example: Bit Control Block address X'0A10' is generated for the third LIB position, line interface 1.

BIT CONTROL BLOCK ADDRESSES

- Use the bit control block Hex address when addressing an interface from the control panel.
- Program interface addressing uses the bit control block Hex address.
- Logic references to an interface use LIB position and interface assignment.

Line Interface Assignment	Bit Control Block Address			
	First LIB Position "00"*	Second LIB Position "01"*	Third LIB Position "02"*	Fourth LIB Position "03"*
0	0800	0900	0A00	0B00
1	0810	0910	0A10	0B10
2	0820	0920	0A20	0B20
3	0830	0930	0A30	0B30
4	0840	0940	0A40	0B40
5	0850	0950	0A50	0B50
6	0860	0960	0A60	0B60
7	0870	0970	0A70	0B70
8	0880	0980	0A80	0B80
9	0890	0990	0A90	0B90
A	08A0	09A0	0AA0	0BA0
B	08B0	09B0	0AB0	0BB0
C	08C0	09C0	0AC0	0BC0
D	08D0	09D0	0AD0	0BD0
E	08E0	09E0	0AE0	0BE0
F	08F0	09F0	0AF0	0BF0

*"00", "01", "02", and "03" denote the tailgate plug locations of the LIB. These plug locations are illustrated in "I/O Gate Interface Connector Positions" in the *Line Interface Base* section of this manual.

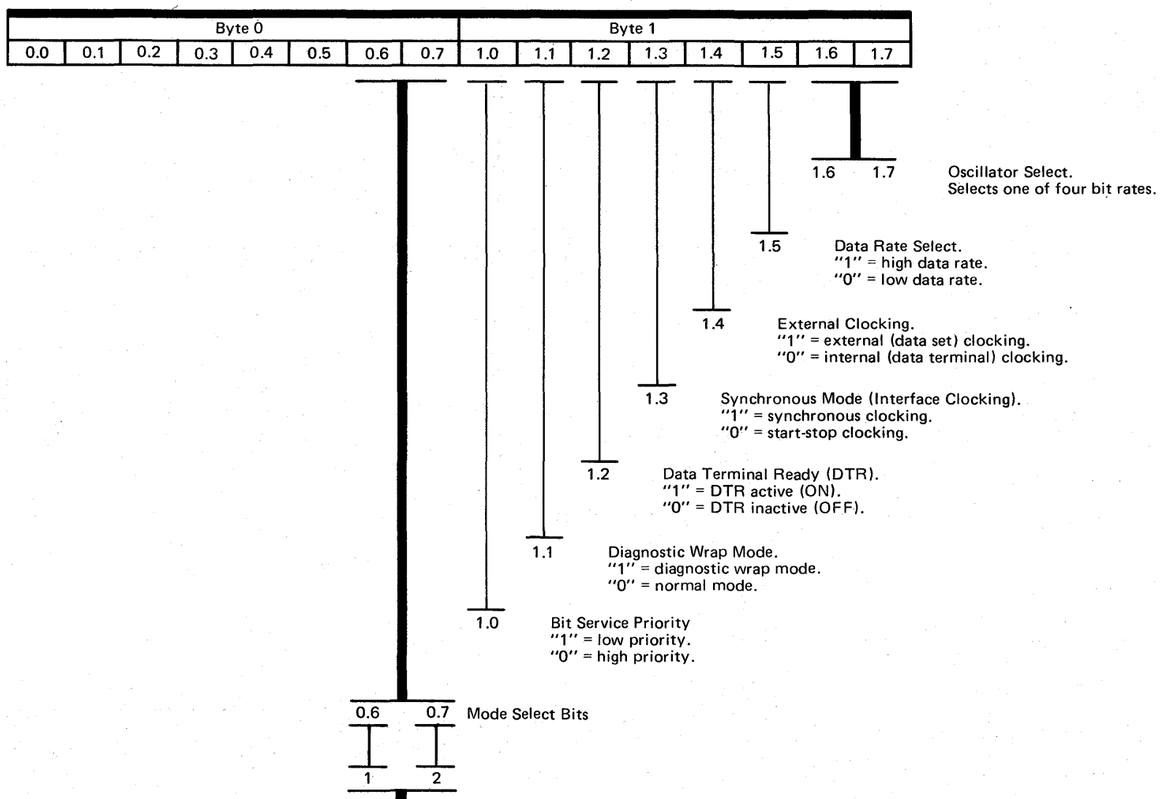
INPUT X'42' CONTROL A

The Input X'42' instruction loads a general register with the 'control A' information. An Input X'42' instruction is a direct bit for bit reflection of the last Output X'42' instruction.

Note: The Input X'42' instruction should be executed only when the scanner is stopped.

COMMUNICATIONS LINE INTERFACE

Input X'42' General Register Bits:

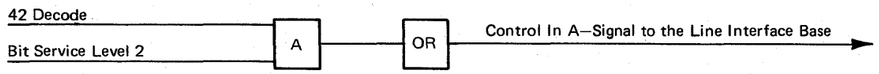


Mode Select Bits 1 2	Conditions Requiring Interface Service
0 0	• Diagnostic Bit Service Request • Force Bit Service Request
0 1	• Ring Indicator or Data Set Ready Active • Diagnostic Bit Service Request • Force Bit Service Request
1 0	• Space Received • Data Set Ready Inactive (OFF) • Diagnostic Bit Service Request • Force Bit Service Request
1 1	• Normal Bit Service Request (interrupt every bit time) • Diagnostic Bit Service Request • Force Bit Service Request

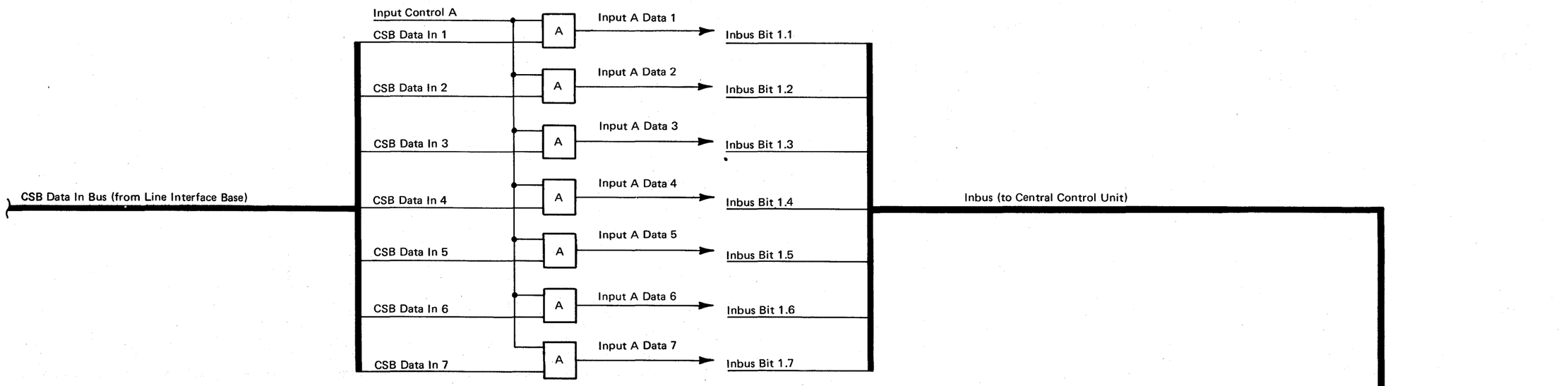
INPUT X'42' CONTROL A (PART 2)

INPUT X'42' DATA FLOW FROM LINE INTERFACE BASE

LOGIC REFERENCE: RS107



LOGIC REFERENCE: RS306



General Register (in Central Control Unit)														
0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

INPUT X'42' CONTROL A (PART 3)

AUTO CALL UNIT INTERFACE

Input X'42' General Register Bits:

Byte 0								Byte 1							
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

1.0 Bit Service Priority
A "1" = Low priority
A "0" = High priority

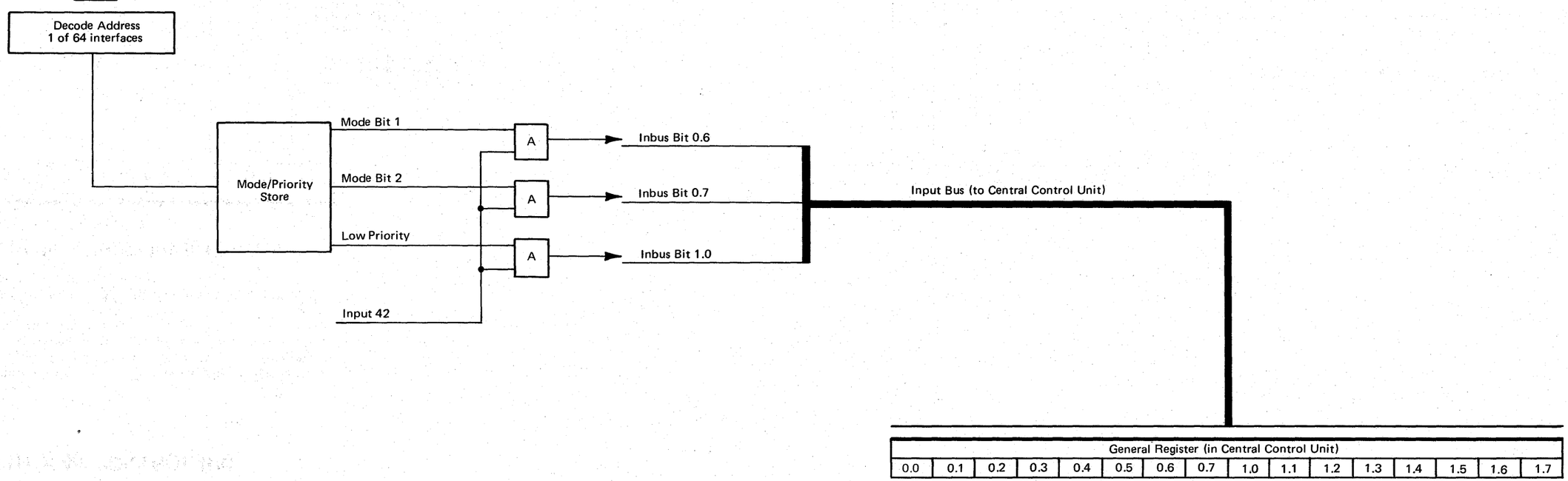
0.6 0.7 Mode Select Bits

1 2

Mode Select Bits 1 2	Conditions Requiring Interface Service
0 0	• Diagnostic Bit Service Request • Force Bit Service Request
1 1	• Normal Bit Service Request (interrupt every bit time) • Diagnostic Bit Service Request • Force Bit Service Request
0 1 1 0	• These modes are not used with the auto call unit interface.

INPUT X'42' MODE AND LINE PRIORITY STORE DATA FLOW

LOGIC REFERENCE: RS304



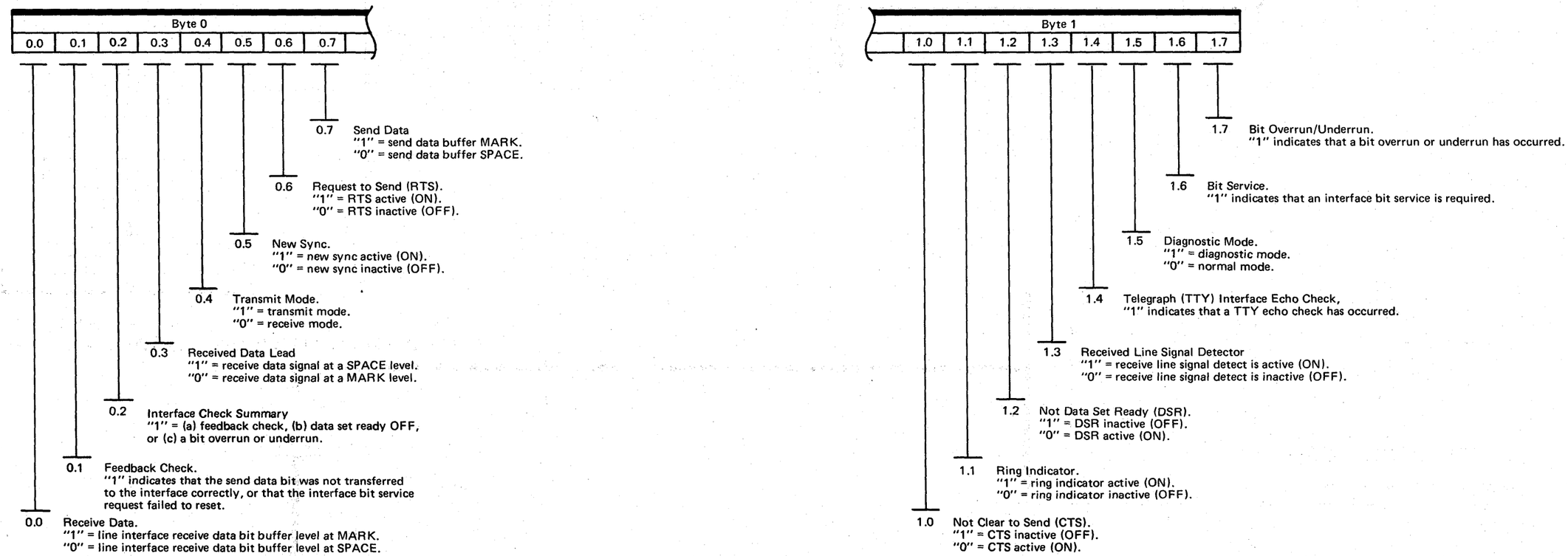
INPUT X'43' CONTROL B/C

The Input X'43' instruction loads a general register with 'control B/C' information. 'Control B/C' information contains data received from the interface, error information, and interface status.

Note: The Input X'43' instruction should be executed only when the scanner is stopped.

COMMUNICATIONS LINE INTERFACE

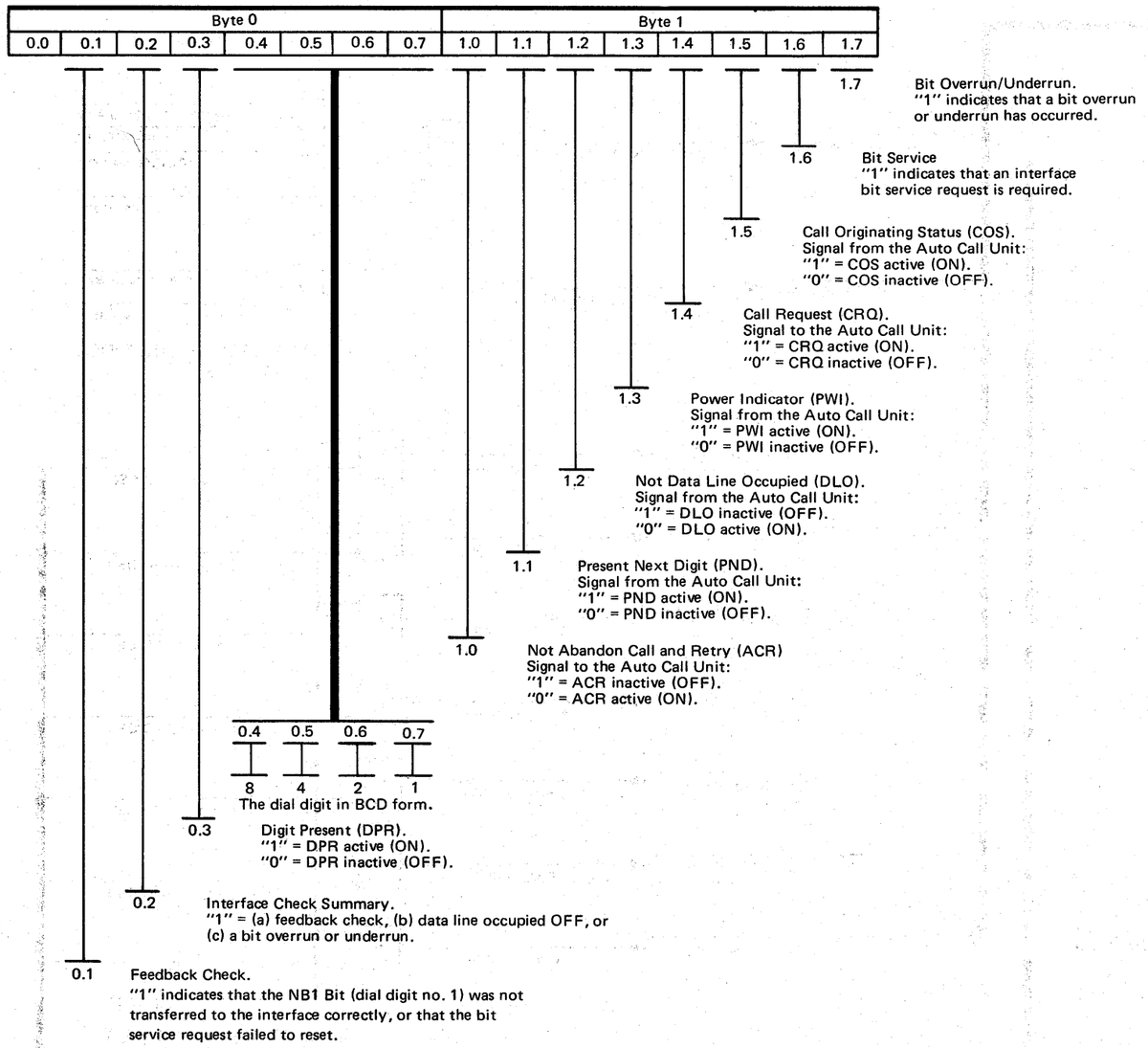
Input X'43' General Register Bits:



INPUT X'43' CONTROL B/C (PART 2)

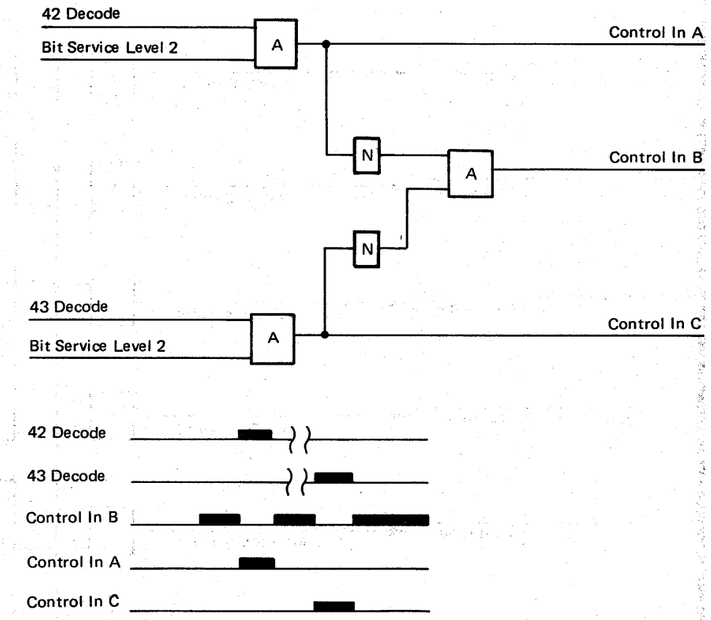
AUTO CALL UNIT INTERFACE

Input X'43' General Register Bits:



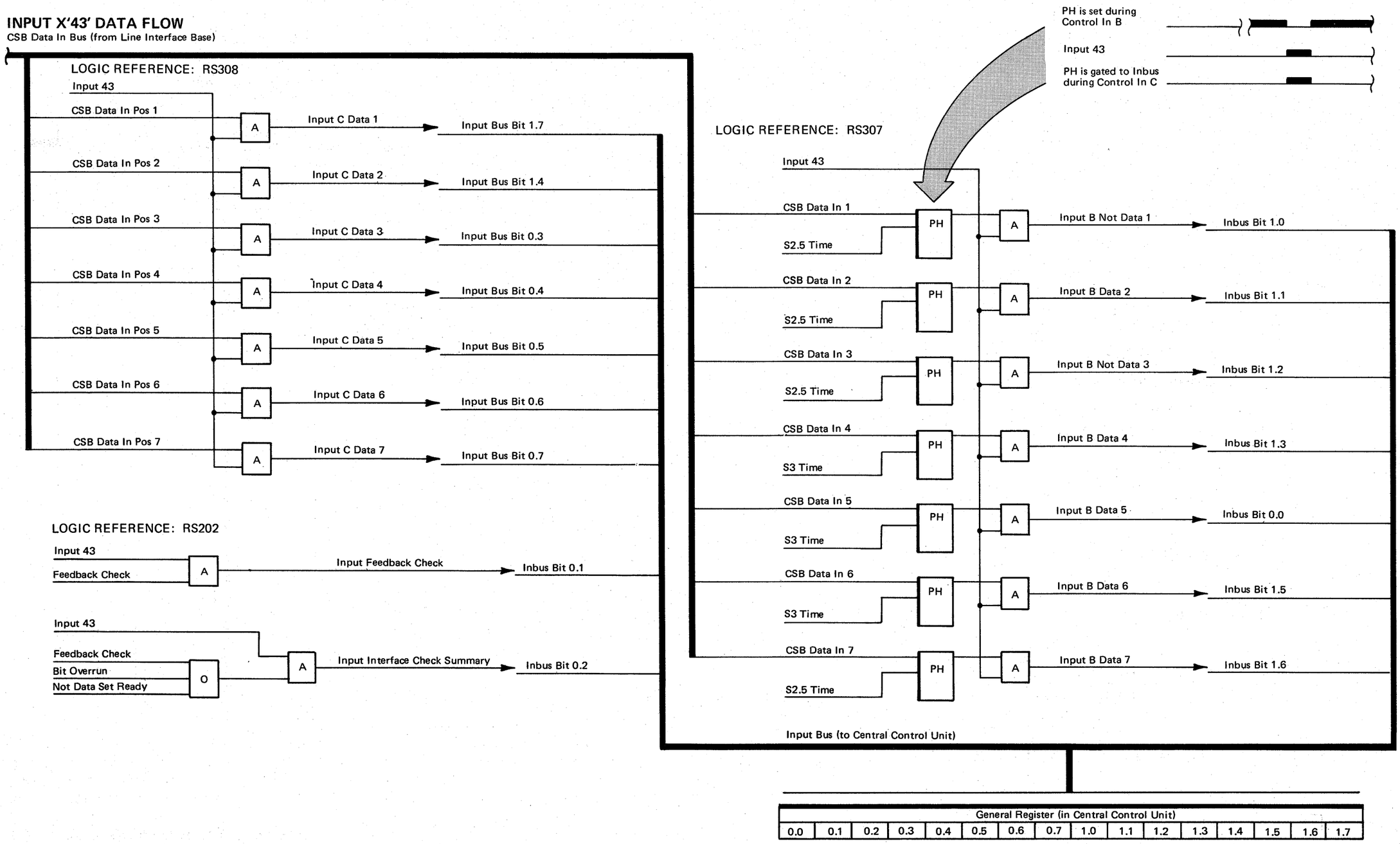
CONTROL IN SIGNALS TO THE LINE INTERFACE BASE

LOGIC REFERENCE: RS107



INPUT X'43' CONTROL B/C (PART 3)

INPUT X'43' DATA FLOW

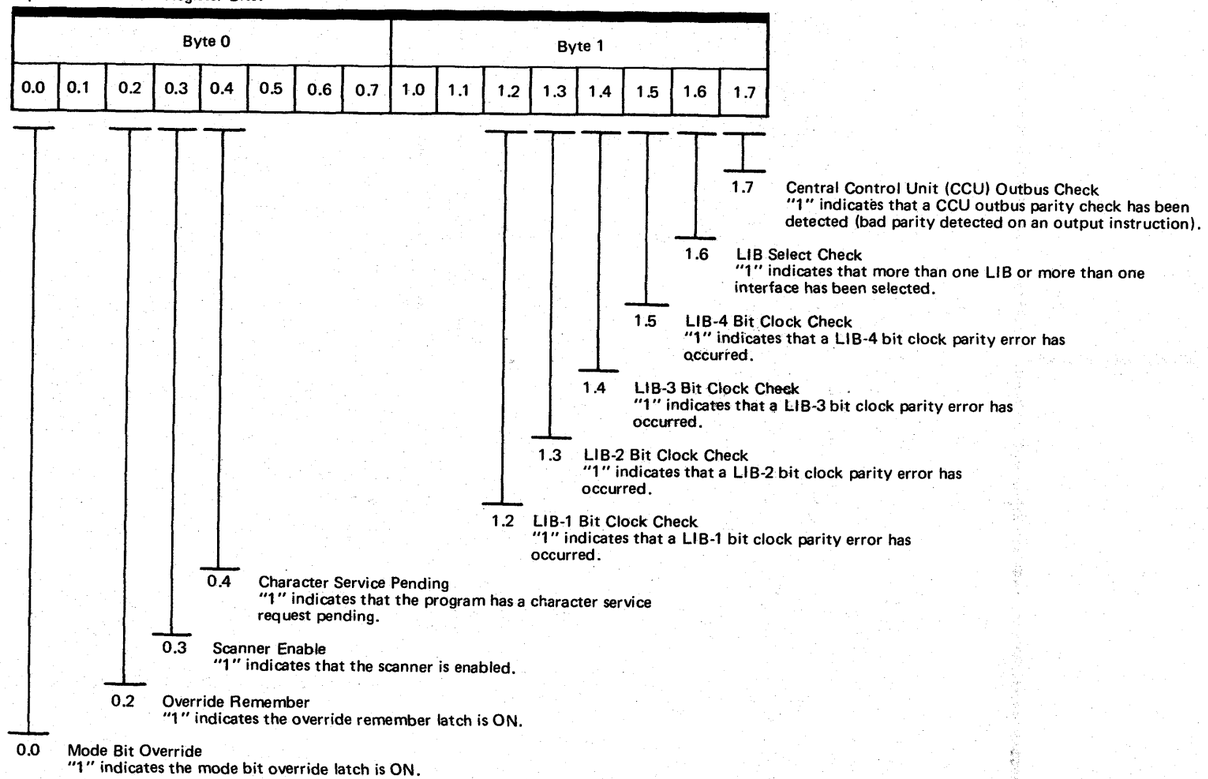


INPUT X'44' STATUS

The Input X'44' instruction loads a general register with the contents of the Type 1 Scanner status register. This register contains (1) indications of level 1 check interrupt requests from the scanner, (2) the scanner enable/disable condition, and (3) character service request information.

COMMUNICATIONS LINE AND AUTO CALL UNIT INTERFACE

Input X'44' General Register Bits:



INPUT X'44' STATUS (CONTINUED)

INPUT X'44' DATA FLOW

LOGIC REFERENCE: RS102

Input 44
Outbus Parity Check
A
Input Outbus Parity Check
CCU
Inbus bit 1.7

LOGIC REFERENCE: RS105

Input 44
Scanner Enabled
A
Input Scanner Enabled
Inbus Bit 0.3

Input 44
Char. Serv. Pend.
A
Input Character Service Pending
Inbus Bit 0.4

LOGIC REFERENCE: RS206

Input 44
BC Error 1
A
Input Bit Clock Error LIB 1
Inbus Bit 1.2

BC Error 2
A
Input Bit Clock Error LIB 2
Inbus Bit 1.3

BC Error 3
A
Input Bit Clock Error LIB 3
Inbus Bit 1.4

BC Error 4
A
Input Bit Clock Error LIB 4
Inbus Bit 1.5

Address Error
A
Input Address Error (LIB Select Check)
Inbus Bit 1.6
CCU

Inbus (to Central Control Unit)

General Register (in Central Control Unit)															
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

OUTPUT INSTRUCTIONS

OUTPUT X'40' MODE BIT OVERRIDE

(1) • The output X'40' instruction sets two scanner latches, the 'mode override' latch and the 'override remember' latch.

• The scanner ignores the output instruction X'40' "R" field general register bit settings.

(2) • The program issues an output instruction X'44' to reset the 'mode override' latch.

• Output instruction X'44' "R" field general register bit 1.2 is set to a "1" to reset the latch.

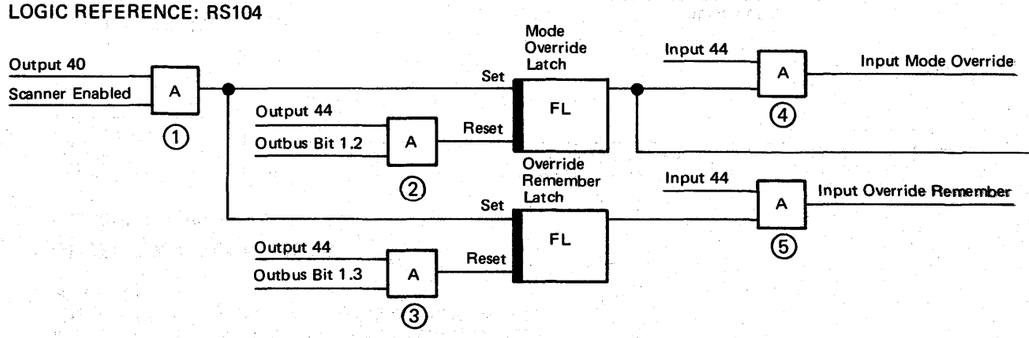
(3) • The program issues an output instruction X'44' to reset the 'override remember' latch.

• Output instruction X'44' "R" field general register bit 1.3 is set to a "1" to reset the latch.

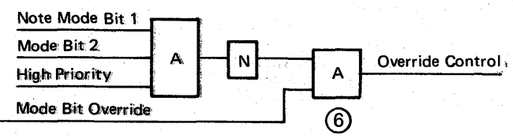
(4) • The program issues an input instruction X'44' to check the status of the 'mode override' latch.

(5) • The program issues an input instruction X'44' to check the status of the 'override remember' latch.

LOGIC REFERENCE: RS104



LOGIC REFERENCE: RS304



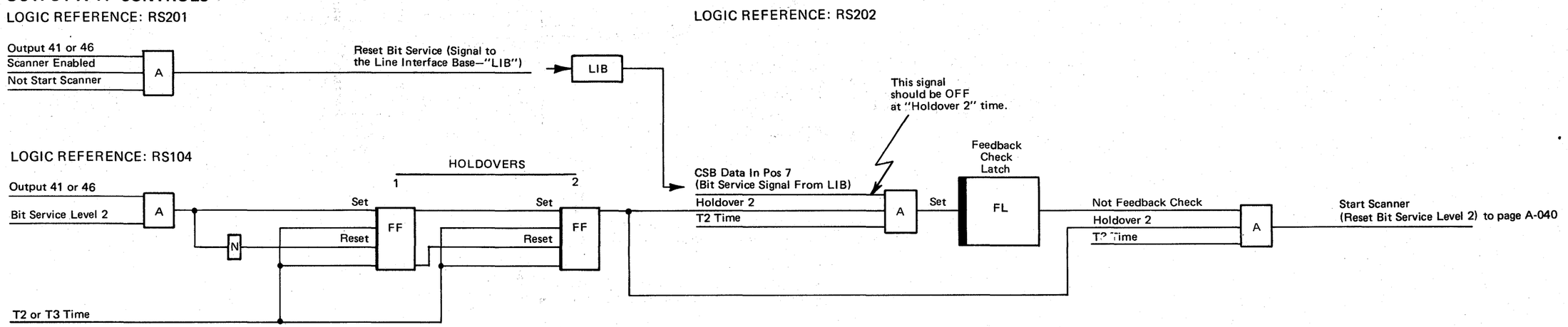
(6) • The 'override control' signal overrides all interface mode select bit settings for conditions requiring interface service with one exception; 'Mode bit override' will not cause a level 2 interrupt for a high priority interface with a mode select bit setting of "01".

• The 'override control' signal allows a bit service L2 interrupt every bit time for all scanner interfaces, except those interfaces with a mode select bit setting of "01"; This logic is illustrated on page A-040, "Set Bit Service L2 Latch".

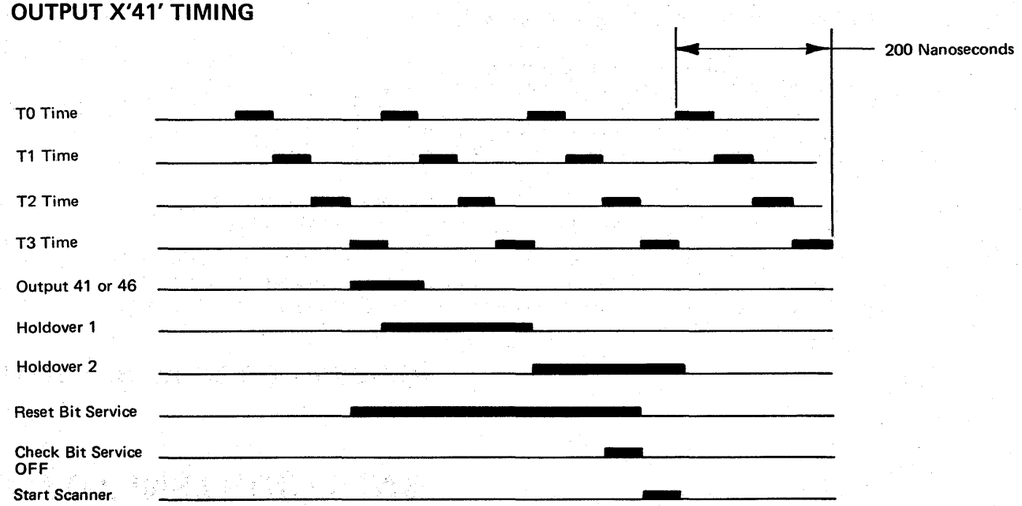
OUTPUT X'41' START SCANNER AND RESET BIT SERVICE L2 REQUEST

The Output X'41' instruction starts the scanner at the completion of the line interface servicing and resets the bit service request of the interface the scanner is addressing. It also resets the program level 2 bit service interrupt request. The bit settings of the register specified by the R operand are ignored.

OUTPUT X'41' CONTROLS



OUTPUT X'41' TIMING



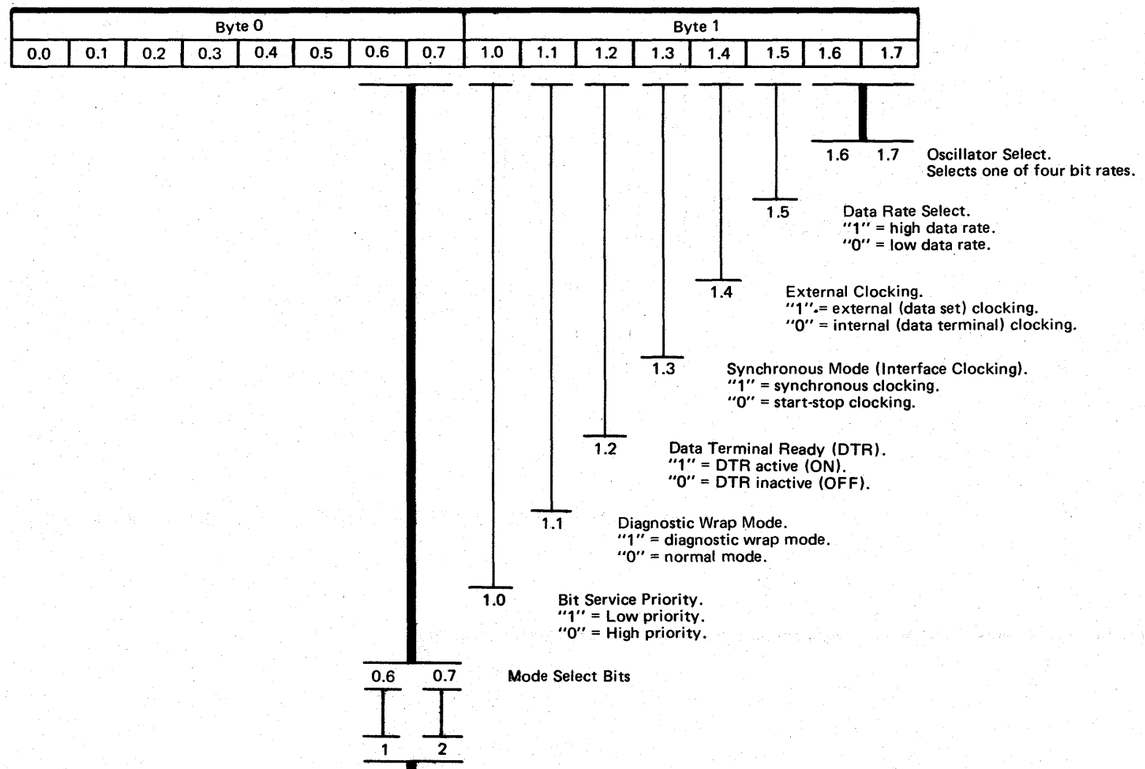
OUTPUT X'42' CONTROL A

The Output X'42' instruction sets the mode of an interface according to the bit setting of the specified general register. This instruction also sets, line priority, clocking, data rate, oscillator selection, and diagnostic mode for the interface.

The Output X'42' instruction should be executed only when the scanner is stopped.

COMMUNICATIONS LINE INTERFACE

Output X'42' General Register Bits:

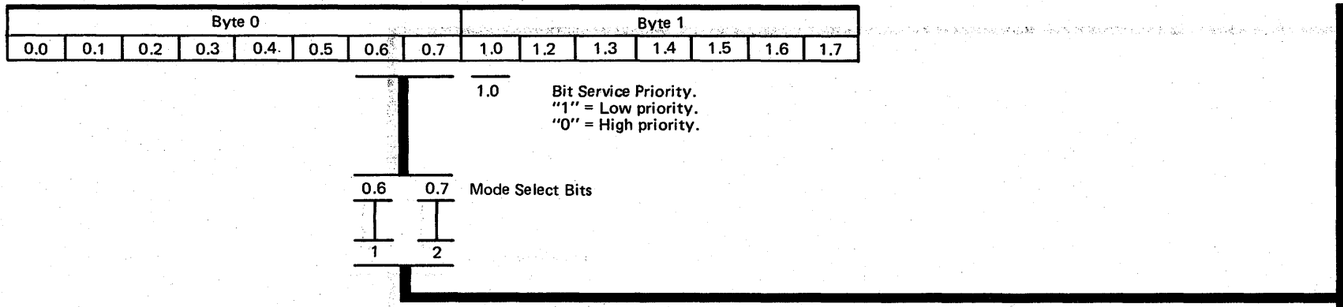


Mode Select Bits 1 2	Conditions Requiring Interface Service
0 0	• Diagnostic Bit Service Request • Force Bit Service Request
0 1	• Ring Indicator or Data Set Ready Active • Diagnostic Bit Service Request • Force Bit Service Request
1 0	• Space Received • Data Set Ready Inactive (OFF) • Diagnostic Bit Service Request • Force Bit Service Request
1 1	• Normal Bit Service Request (interrupt every bit time) • Diagnostic Bit Service Request • Force Bit Service Request

OUTPUT X'42' CONTROL A (PART 2)

AUTO CALL UNIT INTERFACE

Output X'42' General Register Bits:

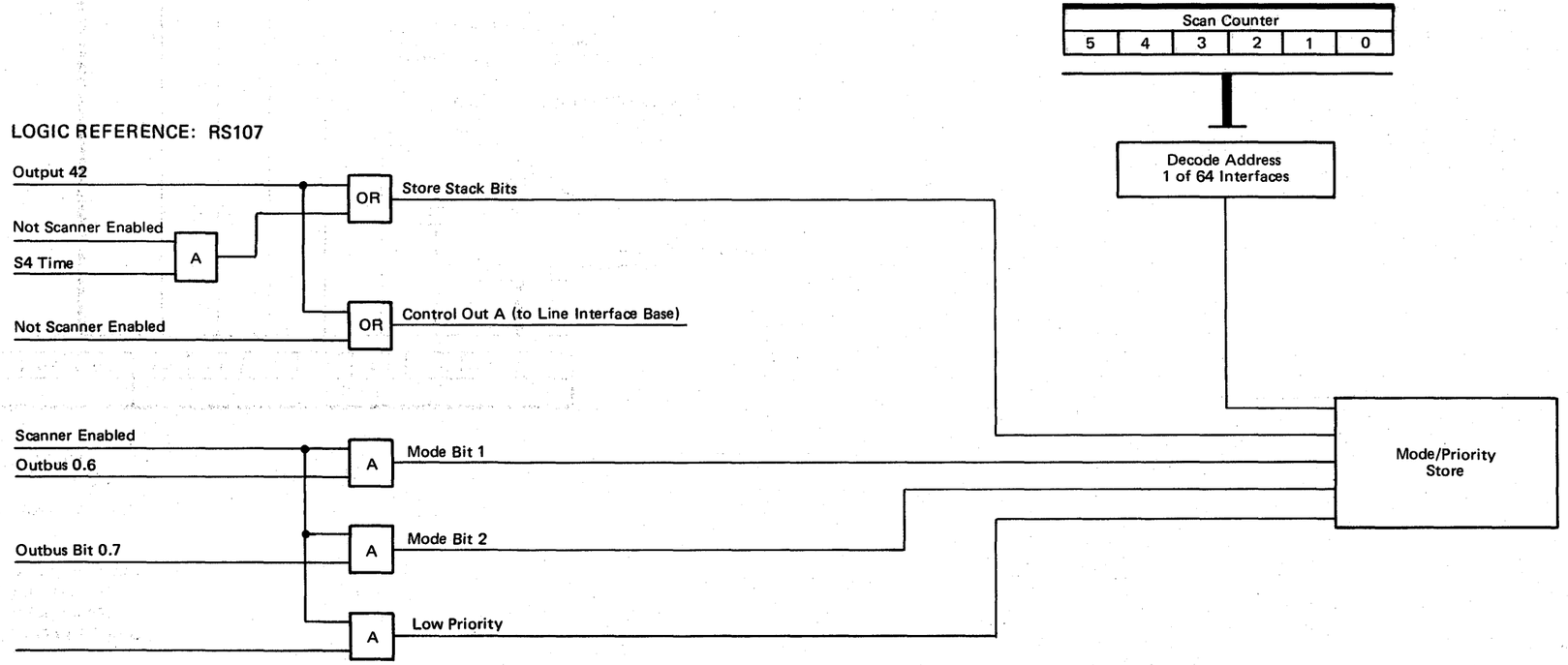


Mode Select Bits 1	2	Conditions Requiring Interface Service
0	0	• Diagnostic Bit Service Request • Force Bit Service Request
1	1	• Normal Bit Service Request (interrupt every bit time) • Diagnostic Bit Service Request • Force Bit Service Request
0 1	1 0	• These modes are not used with the auto call unit interface.

OUTPUT X'42' MODE AND LINE PRIORITY STORE DATA FLOW

LOGIC REFERENCE: RS304

LOGIC REFERENCE: RS107

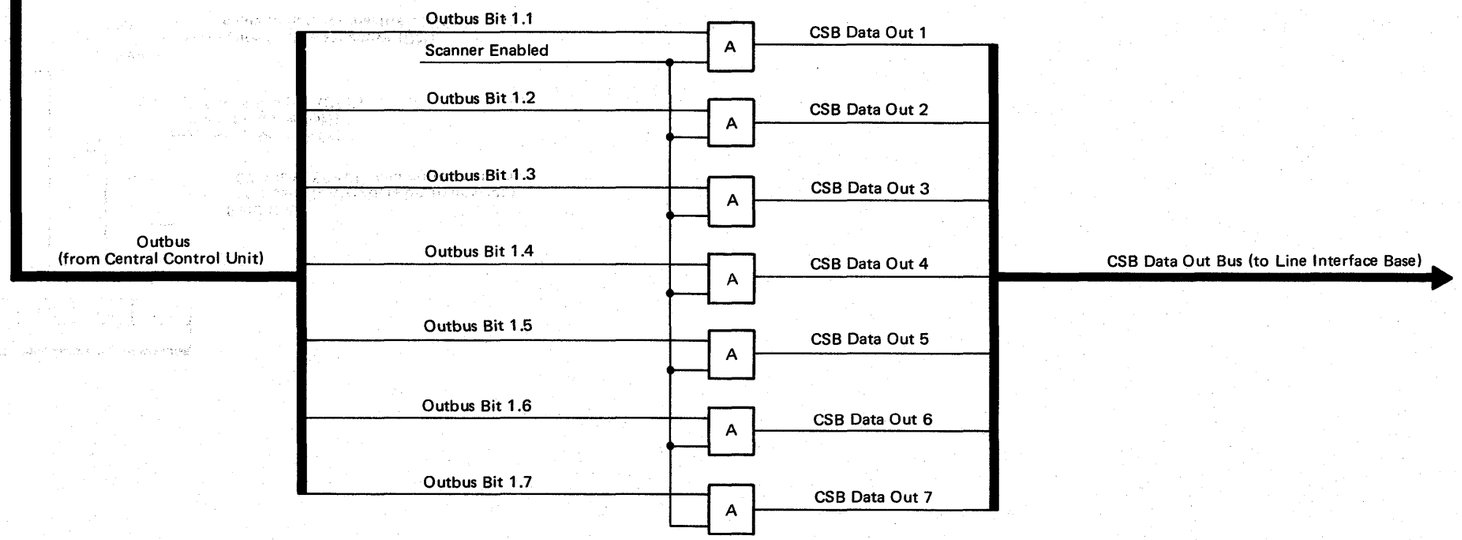


OUTPUT X'42' CONTROL A (PART 3)

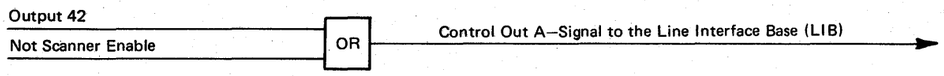
AUTO CALL UNIT INTERFACE

General Register (in Central Control Unit)															
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

LOGIC REFERENCE: RS106



LOGIC REFERENCE: RS107



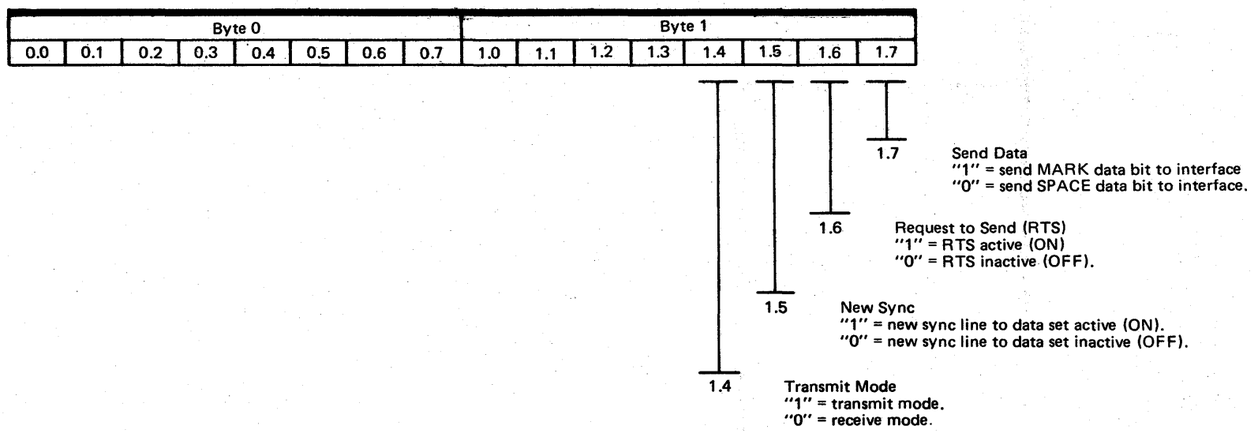
OUTPUT X'43' CONTROL B

The Output X'43' instruction sets the interface into a transmit or receive mode and, in the case of transmitting, sets the 'request-to-send' signal. Byte 1, bit 7 of the general register must be loaded with the mark or space that is to be sent to the interface.

Note: The Output X'43' instruction should be executed only when the scanner is stopped.

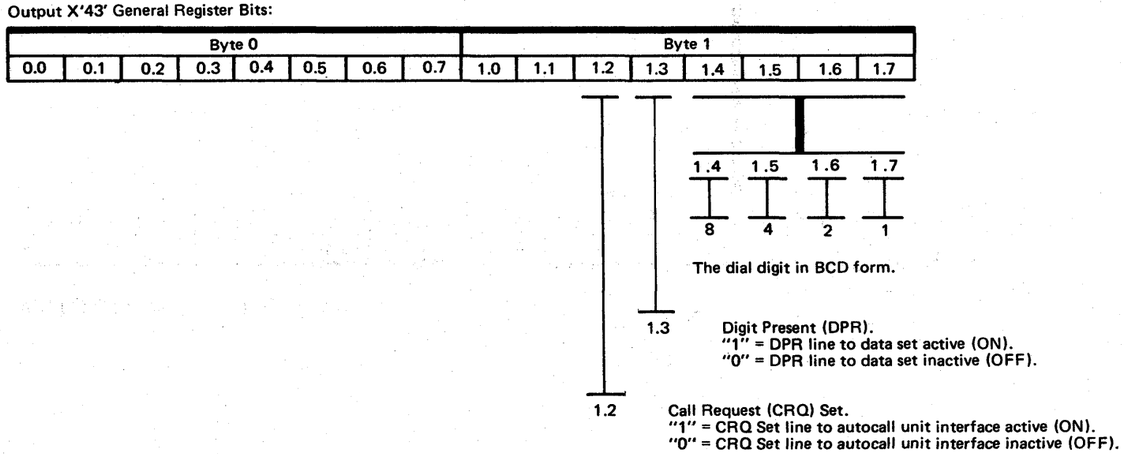
COMMUNICATIONS LINE INTERFACE

Output X'43' General Register Bits:



AUTO CALL UNIT INTERFACE

Output X'43' General Register Bits:

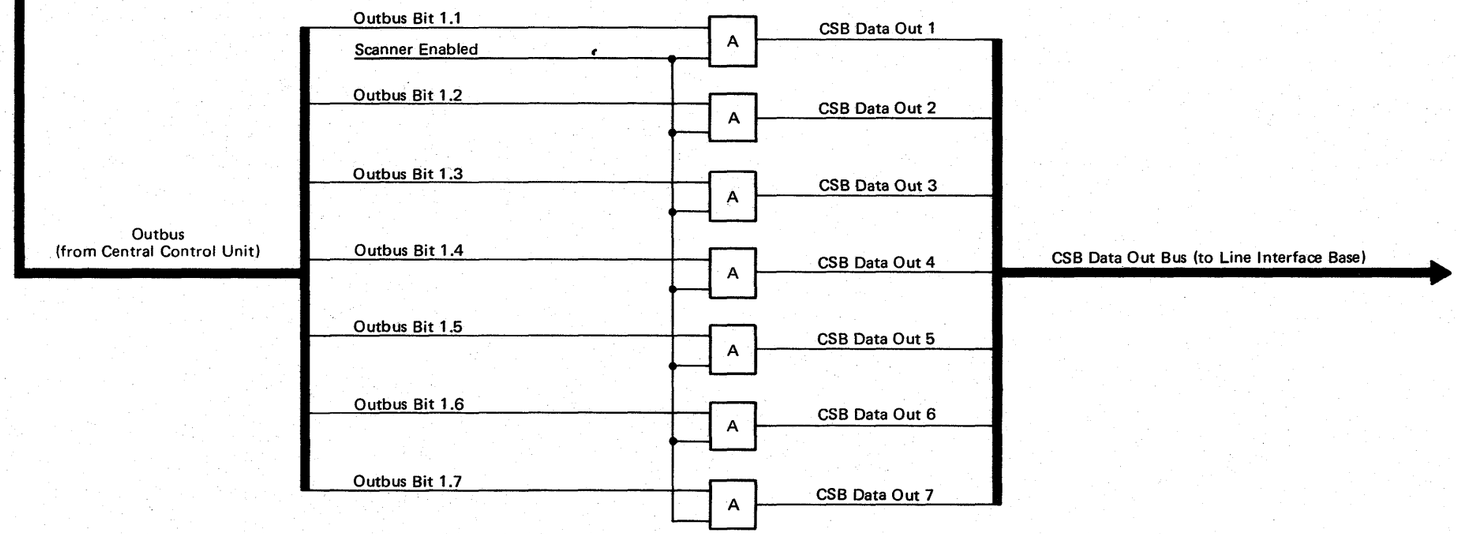


OUTPUT X'43' CONTROL B (PART 2)

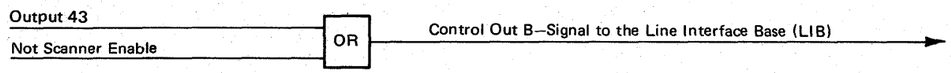
OUTPUT X'43' DATA TRANSFER TO THE LINE INTERFACE BASE

General Register (in Central Control Unit)															
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

LOGIC REFERENCE: RS106



LOGIC REFERENCE: RS107

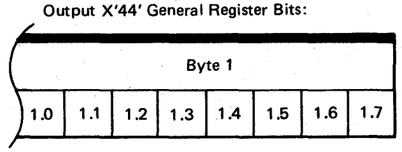


OUTPUT X'44' GENERAL CONTROL

The Output X'44' instruction sets or resets the diagnostic bit service request latch, resets the mode override and override remember latches, and resets outstanding error indications.

COMMUNICATIONS LINE AND AUTO CALL UNIT INTERFACE

Output X'44' General Register Bits:



1.7 Reset Bit Overrun/Underrun
"1" resets the bit overrun/underrun latch for the interface the scanner is addressing.

1.6 Reset Feedback Check
"1" resets the feedback check latch for the interface the scanner is addressing. It is not possible to start the scanner or reset the bit service interrupt until output instruction X'44' is executed with this bit set to "1".

1.5 Reset Level 1 Checks
"1" resets all level 1 checks.

1.4 Reset Character Service Pending
"1" resets the character service pending latch.

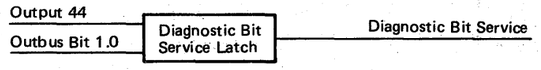
1.3 Reset Override Remember
"1" resets the override remember latch (see page A-230 for a description of 'mode override').

1.2 Reset Mode Override
"1" resets the mode override latch (see page A-230 for a description of 'mode override').

1.0 Diagnostic Bit Service
"1" sets a latch that causes continuous bit service requests for all 64 interfaces (used and unused).
"0" resets the latch.

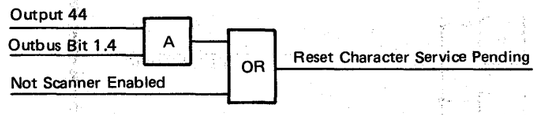
Diagnostic Bit Service

LOGIC REFERENCE: RS105



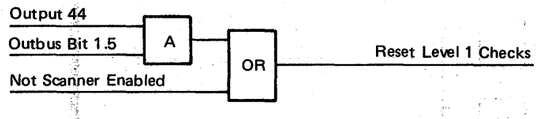
Reset Character Service Pending

LOGIC REFERENCE: RS105



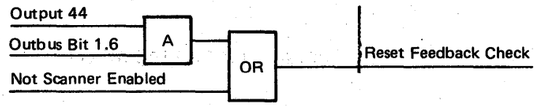
Reset Level 1 Checks

LOGIC REFERENCE: RS105



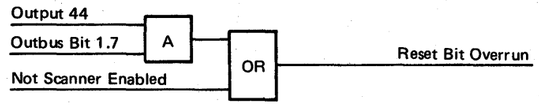
Reset Feedback Check

LOGIC REFERENCE: RS105



Reset Bit Overrun/Underrun

LOGIC REFERENCE: RS105



OUTPUT X'45' SCANNER CONTROL

The Output X'45' instruction causes the scanner and/or the line interface bases to be enabled or disabled. Normally, this instruction is used only during initialization or when an error has occurred that requires a LIB to be disabled.

Programming Note
Output X'45' disables interrupts from any LIB attached to the Type 1 Scanner. This can be particularly useful when a bit-clock error occurs in a LIB causing a level 1 interrupt. Interrupts from the failing LIB can be disabled, which allows the remaining LIBs to continue operation. 'Diagnostic Bit Service' and 'Force Bit Service' override the LIB and scanner disables.

COMMUNICATIONS LINE AND AUTO CALL UNIT INTERFACE

Output X'45' General Register Bits:

Byte 0								Byte 1							
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

0.7 Disable LIB 4
"0" disables LIB 4 and any L1, L2, or bit service interrupts from LIB 4.
"1" resets the disable condition.

0.6 Disable LIB 3
"1" disables LIB 3 and any L1, L2 or bit service interrupts from LIB 3.
"0" resets the disable condition.

0.5 Disable LIB 2
"1" disables LIB 2 and any L1, L2 or bit service interrupts from LIB 2.
"0" resets the disable condition.

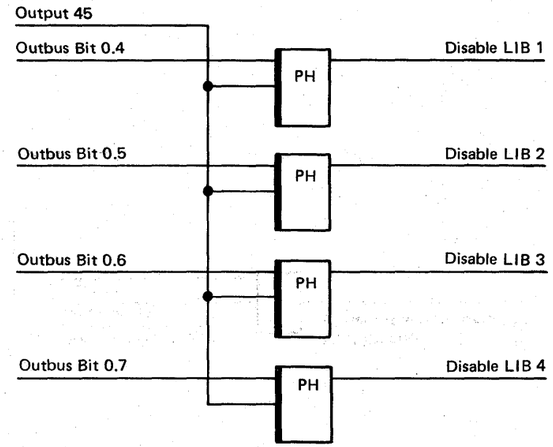
0.4 Disable LIB 1.
"1" disables LIB 1 and any L1, L2 or bit service interrupts from LIB 1.
"0" resets the disable condition.

0.2 Reset Scanner Enable
"1" resets the scanner enable latch, prevents further interrupts, forces all interfaces to be reset, and allows no bit services.

0.1 Set Scanner Enable
"1" sets the scanner enable latch, allowing normal operation of the scanner.

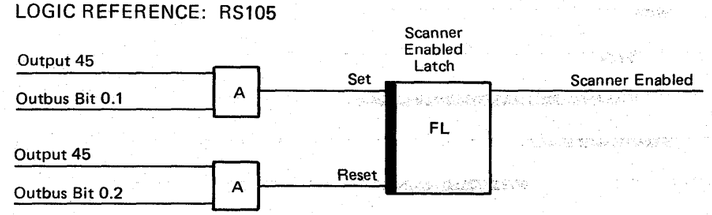
Disable LIB

LOGIC REFERENCE: RS206



Set or Reset Scanner Enable

LOGIC REFERENCE: RS105

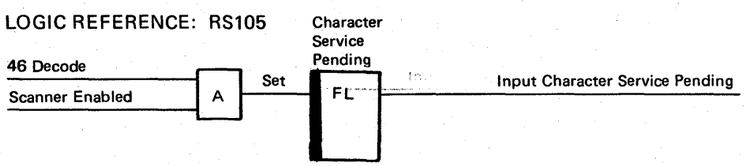


OUTPUT X'46' SET CHARACTER SERVICE PENDING

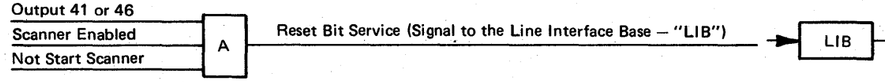
The Output X'46' instruction is normally used at the end of a bit-service request when a character is ready for processing. It sets the 'character-service pending' latch to signal the control program that a character-service interrupt is required. The instruction then resets the level 2 bit-service request and starts the scanner. Since this instruction performs a function instead of an operation, the bit settings of the register are ignored.

OUTPUT X'46' CONTROLS

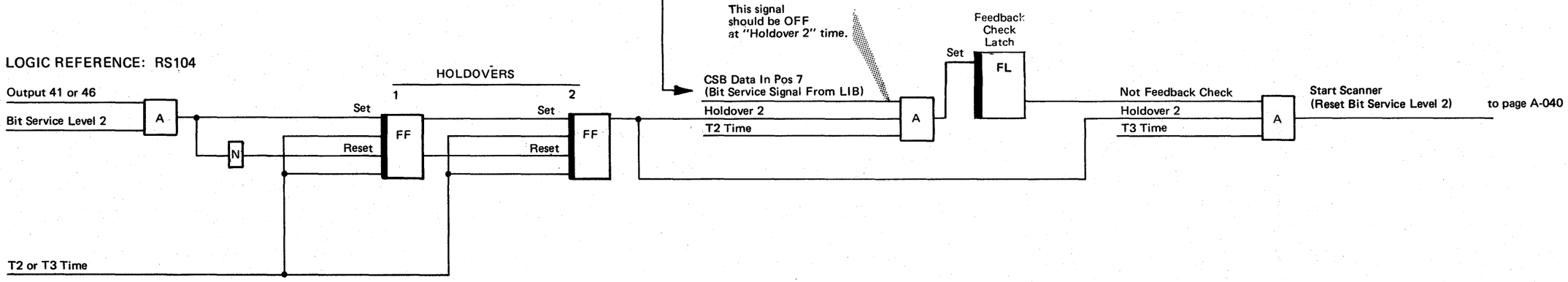
LOGIC REFERENCE: RS105



LOGIC REFERENCE: RS201

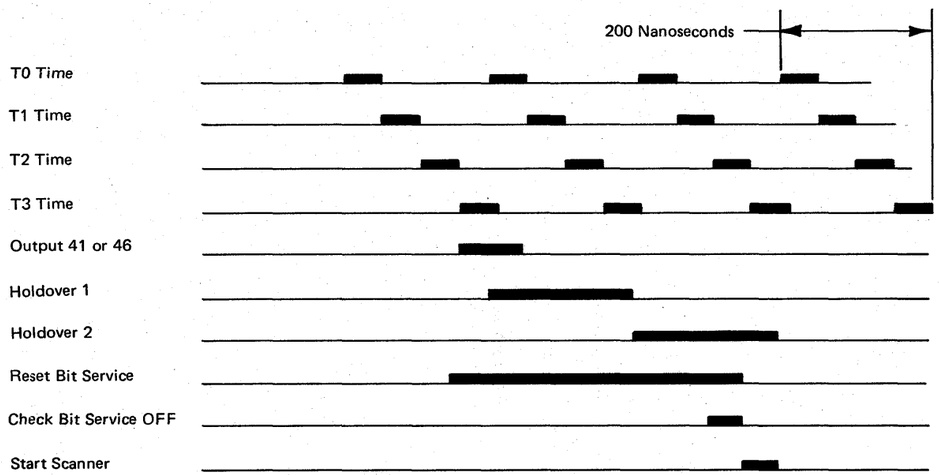


LOGIC REFERENCE: RS104



OUTPUT X'46' TIMING

LOGIC REFERENCE: RS202



OUTPUT X'47' FORCE BIT-SERVICE REQUEST

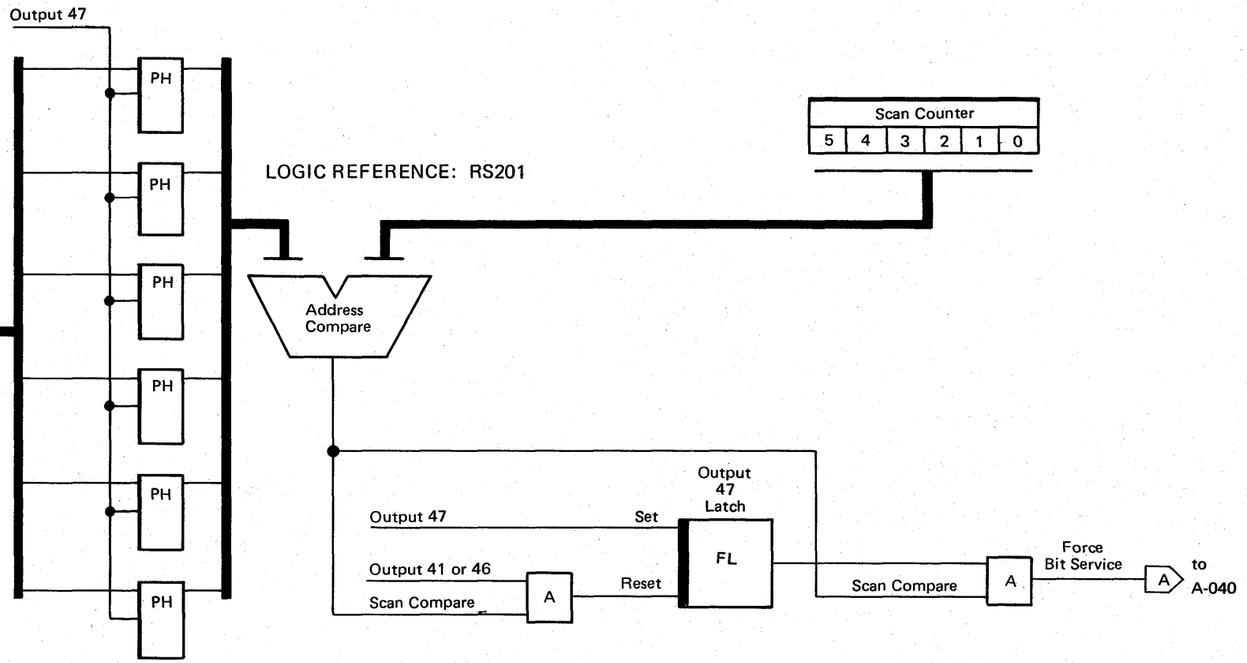
The Output X'47' instruction forces a bit-service interrupt request for the interface address specified in the general register. This instruction is normally used to stop the scanner on a disabled interface so that the program may enable it.

COMMUNICATIONS LINE AND AUTO CALL UNIT INTERFACE

Output X'47' General Register Bits:

Byte 0								Byte 1							
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

0.6 — 1.3



GENERAL REGISTER BIT DEFINITIONS

Output X'47' General Register Bits:

Byte 0								Byte 1							
0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

X '0' through X 'F' for the 16 LIB interfaces

0	0 - First LIB Position
0	1 - Second LIB Position
1	0 - Third LIB Position
1	1 - Fourth LIB Position

SCAN COUNTER BIT DEFINITIONS

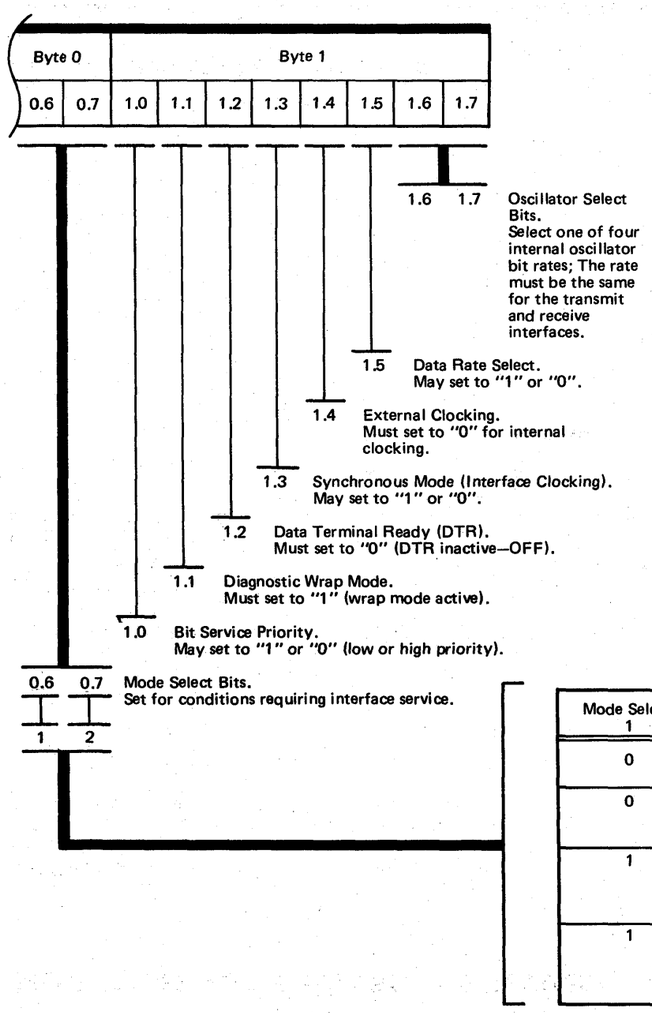
Scan Counter					
5	4	3	2	1	0

X '0' through X 'F' for the 16 LIB interfaces

0	0 - First LIB Position
0	1 - Second LIB Position
1	0 - Third LIB Position
1	1 - Fourth LIB Position

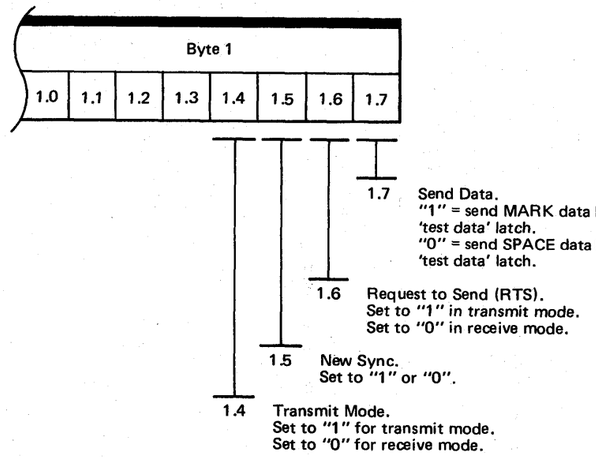
DIAGNOSTIC WRAP MODE

- Provides ability to wrap transmit data from an interface set to 'diagnostic' and 'transmit' mode to one or more interfaces set to 'diagnostic' and 'receive' mode.
- The program issues an output instruction X'42' to set an interface to 'diagnostic' wrap mode.
- The program sets these bits in the output instruction X'42' "R" field general register:



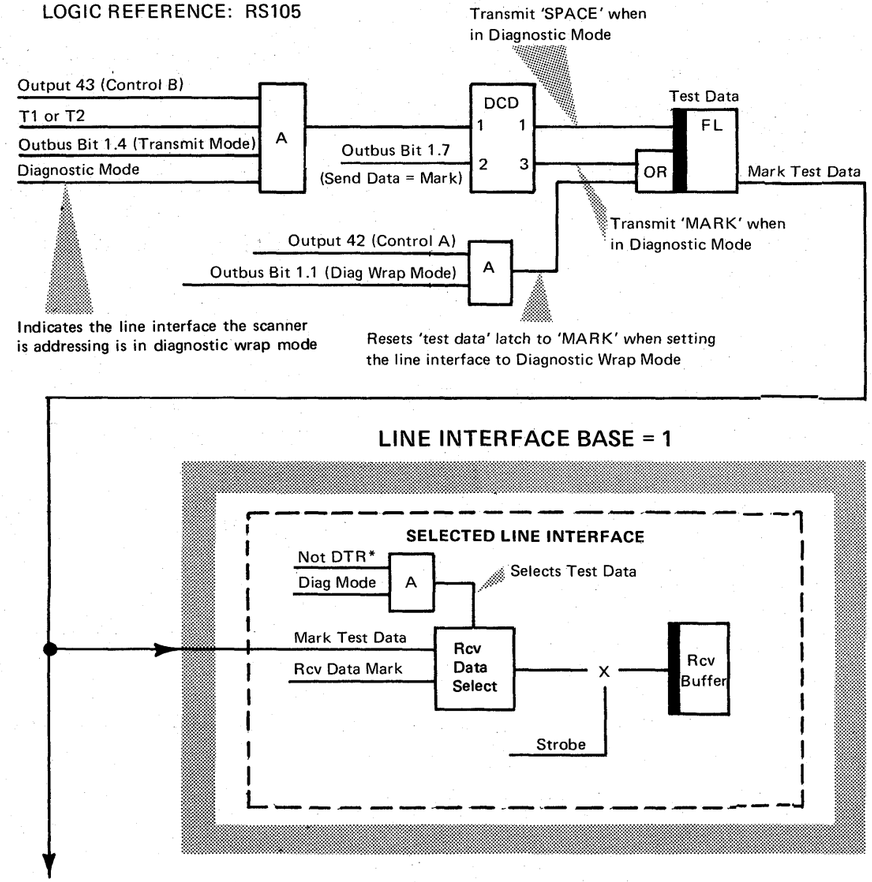
Mode Select Bits 1 2	Conditions Requiring Interface Service
0 0	• Diagnostic Bit Service Request • Force Bit Service Request
0 1	• Ring Indicator or Data Set Ready Active • Diagnostic Bit Service Request • Force Bit Service Request
1 0	• Space Received • Data Set Ready Inactive (OFF) • Diagnostic Bit Service Request • Force Bit Service Request
1 1	• Normal Bit Service Request (interrupt every bit time) • Diagnostic Bit Service Request • Force Bit Service Request

- The program issues an output instruction X'43' to set an interface to transmit or receive mode; One interface is set to transmit mode, the other interfaces in 'diagnostic wrap' mode are set to receive.
- The program sets these bits in the output instruction X'43' "R" field general register:



TEST DATA LATCH

LOGIC REFERENCE: RS105



*This line not present on all line sets.
See the specific line set data flow page.

TYPE 2 COMMUNICATION SCANNER

INTRODUCTION

The type 2 communication scanner provides the interface between the line attachment hardware (line or autocall interfaces) and the CCU. The primary function of the scanner is to monitor the communication lines for service requests. Four scanners may be installed in the 3705, as indicated in the type 2 scanner configuration diagram. Each scanner supports both synchronous and asynchronous half-duplex *lines* operating at various line speeds. For each line interface, the control program initializes the line type (BSC, start-stop, autocall), character length, type of bit clocking (business machine or modem), bit clocking speed for business machine clocking, and interrupt priority.

Functions of the Type 2 Scanner

The type 2 scanner:

- Scans the line/autocall interface addresses in the LIB positions it supports.
- Performs character assembly/disassembly
- Provides character buffering
- Signals program level 2 interrupts to the attachment base when program service is required—such as character service
- Provides bit clock addresses for the LIB positions it supports so the LIB can generate the strobe pulse for receive operations.
- Provides up to four oscillators that generate business machine transmit and receive pulses for use by the line/autocall interfaces.
- Signals program level 1 interrupts for failures in the scanner, LIB, and line/autocall interface. The cause of the level 1 interrupt is buffered in the check register.
- Monitors the state of certain carrier equipment and autocall unit lines for interfaces that are selected by the control program and buffers the state in the display register where the program may display it on the control panel.

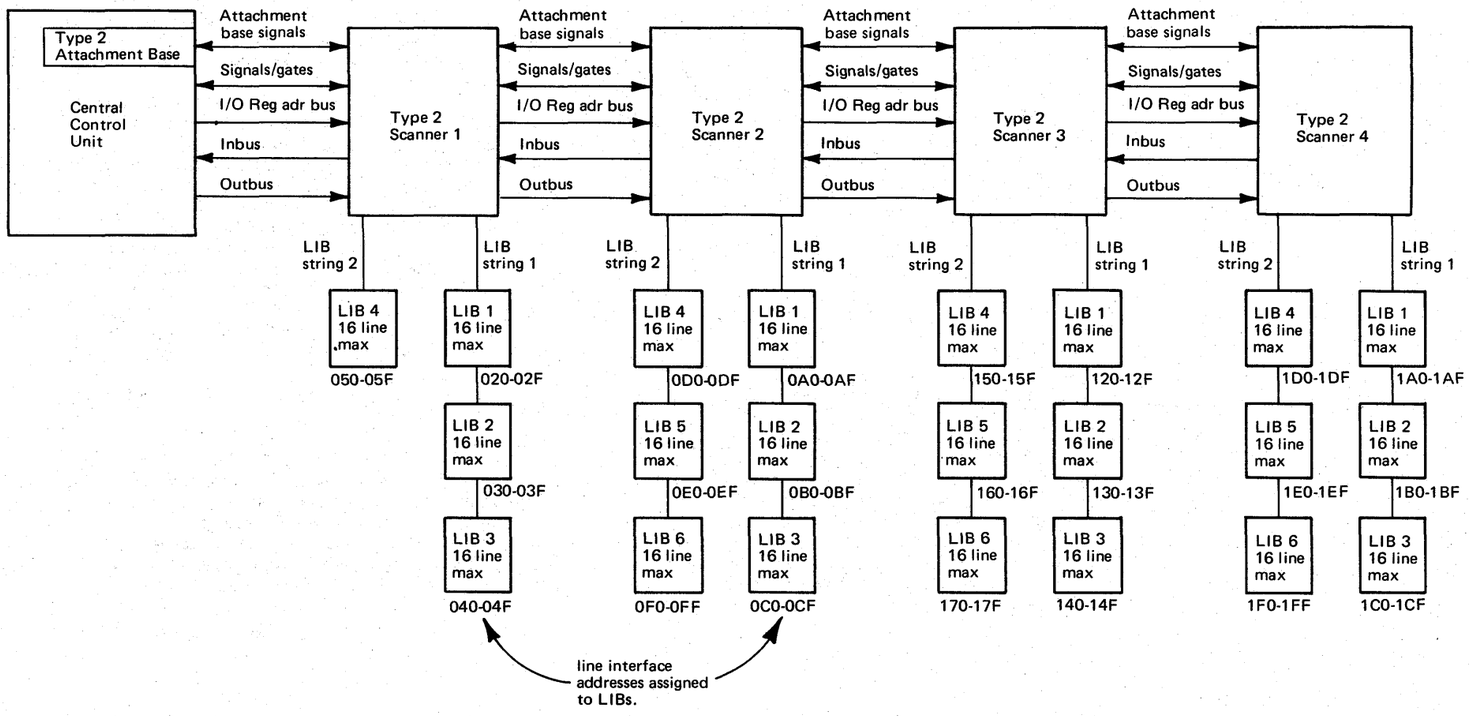
Type 2 Attachment Base

The type 2 attachment base provides common interface controls to the central control unit and line addressing controls for the type 2 scanner and is contained on two cards located at A-B3D2 and A-B3E2 (see B-030).

The attachment base:

- Generates line interface addresses for all type 2 scanners for scan addressing
- Performs address substitution under program control
- Provides a buffer for the interface address for program addressing
- Provides the mechanism for buffering program level 2 interrupts by priority.

TYPE 2 SCANNER CONFIGURATION



Scanner Initialization

The scanner and its associated LIBs are placed in a disabled state (1) during a power-on sequence, (2) during an IPL, (3) by a control panel reset, or (4) during the execution of an Output X'43' when the general register specified by the R field contains appropriate bits. The control program must *enable* each scanner by executing Output X'43' with bits 0.1 = 1 and 1.6 = 1 before the control program can initialize each ICW (interface control word) and the associated line or autocall interface. This initialization must occur before the line interface can be placed in operation.

Interface Control Word

The ICW provides the normal communications link between the control program and the scanner, and between the control program and the interface hardware. The scanner contains 96 ICWs, one for each of the line/autocall interfaces that may be attached. Certain fields within the ICW are used to buffer information about the interface between successive scans.

The ICW:

- Buffers and serializes the character to be transmitted
- Deserializes and buffers the received character
- Buffers the autocall digit
- Buffers the status of autocall lines
- Buffers the mode of operation
- Buffers the status of the operation
- Is used to initialize the line interface hardware and the scanner operation for that interface.

TYPE 2 COMMUNICATION SCANNER INTRODUCTION, PART 2

PROGRAM ADDRESSING

The control program accesses the ICW or scanner during that part of the scanner cycle called CCU time. During CCU time, the scanner implements the input and output instructions (see Input/Output section) that apply to that scanner.. During this time, the interface address in ABAR (attachment buffer address register) accesses the associated ICW and selects the scanner. The control program executes input instructions to obtain the status of this ICW, or executes output instructions to change the contents of this ICW.

The control program also executes input instructions to obtain (1) the interface address in ABAR, (2) the status of the check register, and (3) the status of the display register.

The control program also executes output instructions to (1) set the interface address in ABAR, (2) set the state of the substitution control register, (3) set the state of the upper scan limit latches in the selected scanner, (4) enable or disable a LIB or scanner, or (5) set or reset the scanner control functions.

SCAN ADDRESSING

Each scanner services the line/autocall interface during that part of the scanner cycle called CSB time. During CSB time, the scan counter in the attachment base provides an interface address to all scanners in parallel to be used by each scanner for scan addressing. Each scanner uses this interface address to access the corresponding line/autocall interface and the associated ICW. The scanner receives the status of the line/autocall interface and determines if a bit service request is active. If a request is active, the scanner, under control of the primary control field in the ICW, performs the bit service operation and updates the ICW content. The scanner signals a character service level 2 interrupt when appropriate. If the scanner does not detect a bit service request, the bit service operation does not occur.

The scan counter furnishes 96 discrete interface addresses to all scanners in parallel. The address substitution mechanism in the attachment base can modify certain addresses before they are sent to the scanners. Each scanner contains an upper scan limit mechanism for modifying the interface address received from the attachment base. Modification only occurs during scan addressing. Address substitution and upper scan limit modification are both under control of the program.

LEVEL 1 INTERRUPTS

Failures in the scanner can affect all communication lines attached to the 3705, or can affect at least a group of lines within a particular LIB. The detection of one or more of the failures is indicated by a type 2 scanner n level 1 interrupt request. Each scanner contains a check register which buffers the condition that causes the level 1 interrupt.

TRANSMIT OPERATION

The program initializes the operation and places the first character into the SDF (serial data field) and the second character into the PDF (parallel data field) of the ICW associated with that line interface. The SDF serializes the character and sends it to the line interface a bit at a time under control of the bit service request from the line interface. The line interface then sends the bits to the modem or transmission line under control of the transmit oscillator located in the scanner or external clock in the modem. The control program must furnish all the data to be transmitted (such as line control, initial SYN and PAD, and response characters). The scanner only adds the start and stop bits for start-stop operations.

When the character has been transmitted, the scanner requests a level 2 interrupt to signal the control program that another character can be sent to the scanner. The scanner transfers the next character from the PDF to the SDF so transmission can continue while the control program (1) loads the next character into the PDF, or (2) signals the scanner that the last character has been transmitted by changing to transmit turnaround mode.

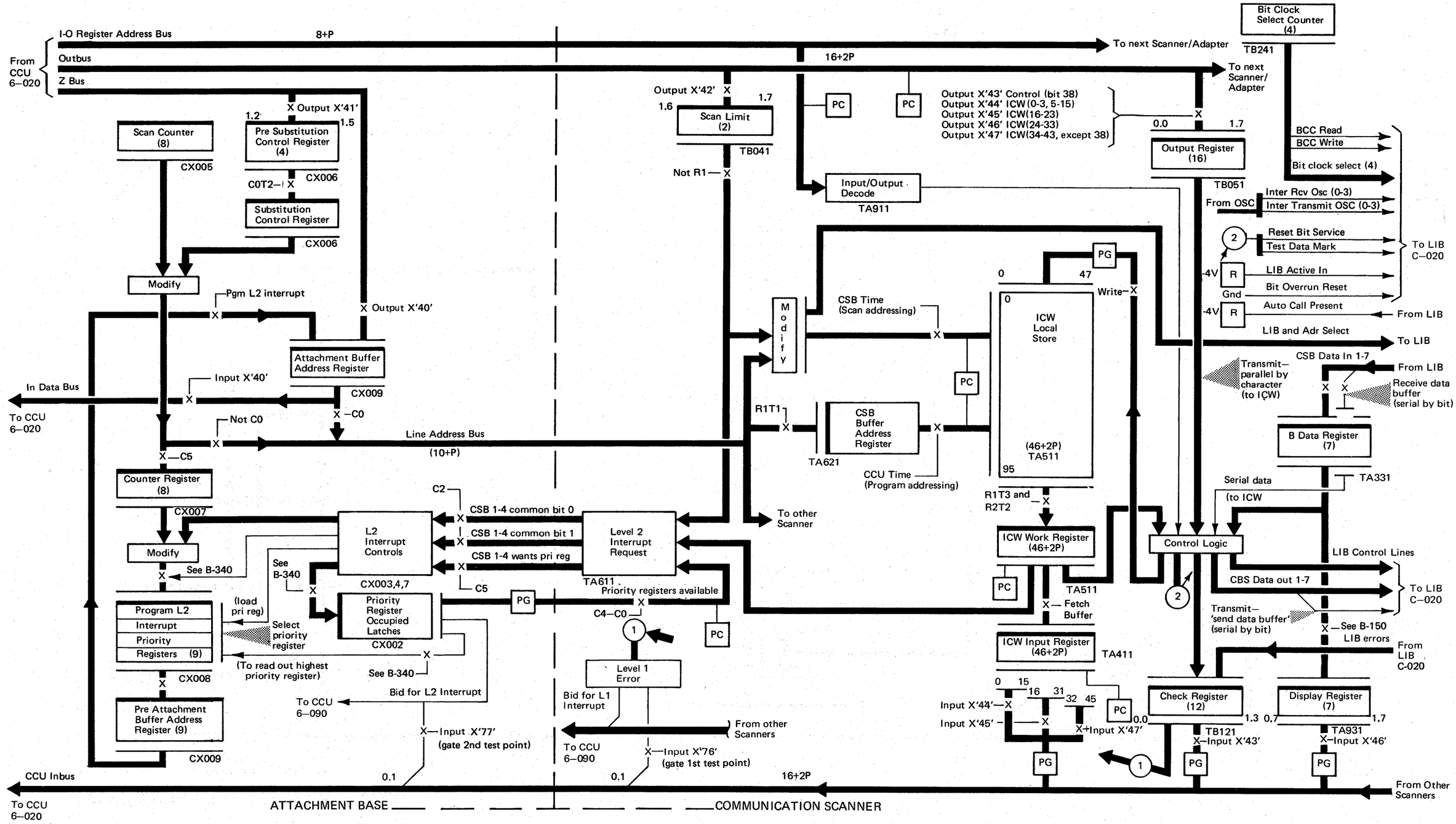
RECEIVE OPERATION

The line interface receives the bits from the modem or transmission line. The line interface strobes the bits into its receive buffer. The strobe is under control of the bit clock control (located in the LIB) for business machine clocking. The scanner contains the receive oscillator that controls the bit clock circuit in the LIB. The modem receive clock pulses generate the strobe pulses when external clocking is specified by the control program for synchronous operation. In either case, the strobe generates a bit service request in the line interface which signals the scanner that the receive buffer contains the received bit. The scanner places the bits into the SDF until a character has been assembled and then transfers the character to the parallel data field. The scanner strips the start and stop bits off the character and then causes a program level 2 interrupt. The control program can execute an input instruction to obtain the character in the PDF.

The only character the scanner recognizes is the first SYN character used for phase initialization in synchronous operation. The second SYN character must be recognized by the control program before 'character phase' is identified by the program. If the second character is not the SYN character, the control program changes the operating mode from receiving to monitoring, and the search for character phase resumes.

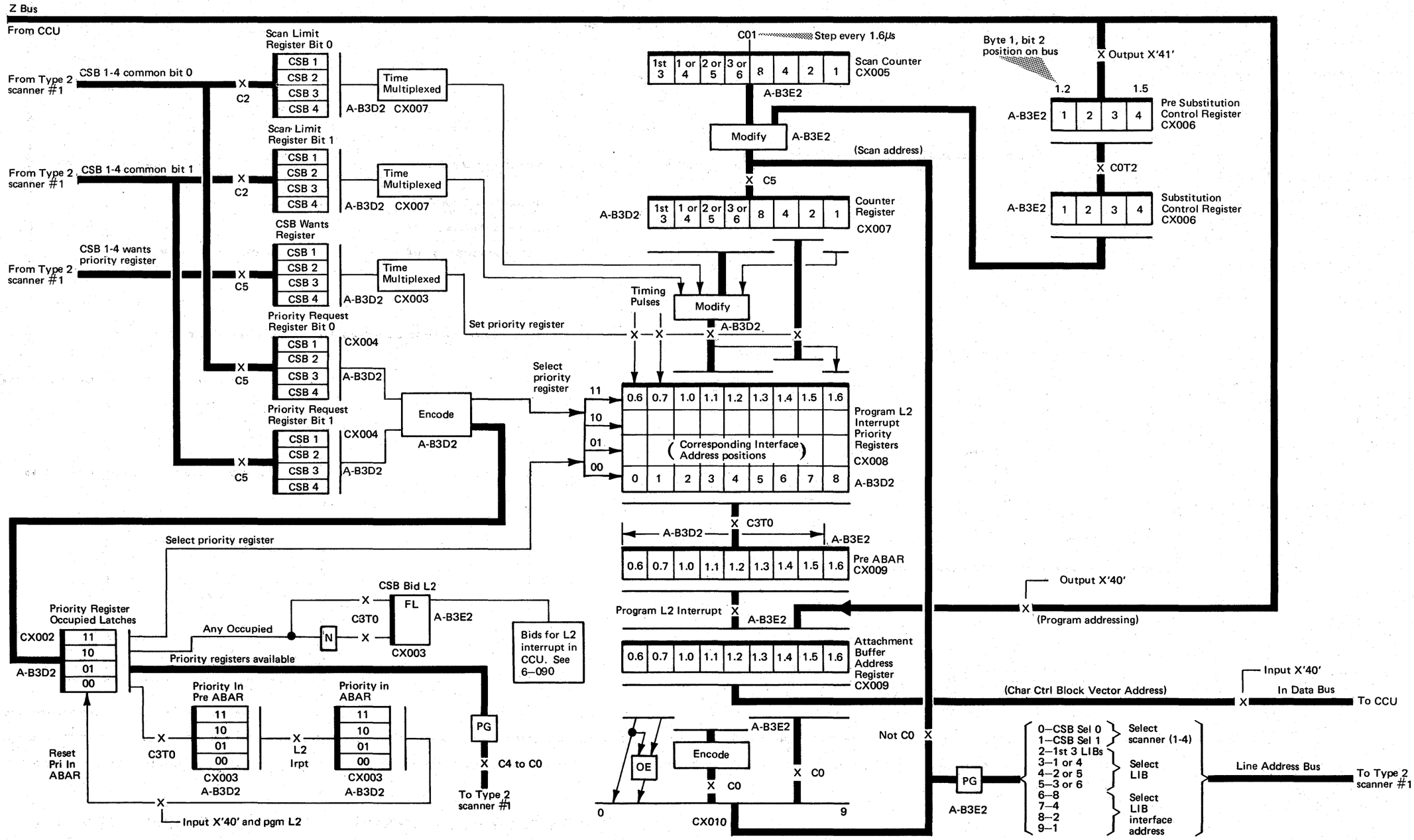
The control program determines when an ending character or sequence has been received and changes the operating mode accordingly.

TYPE 2 ATTACHMENT BASE AND COMMUNICATION SCANNER DATA FLOW



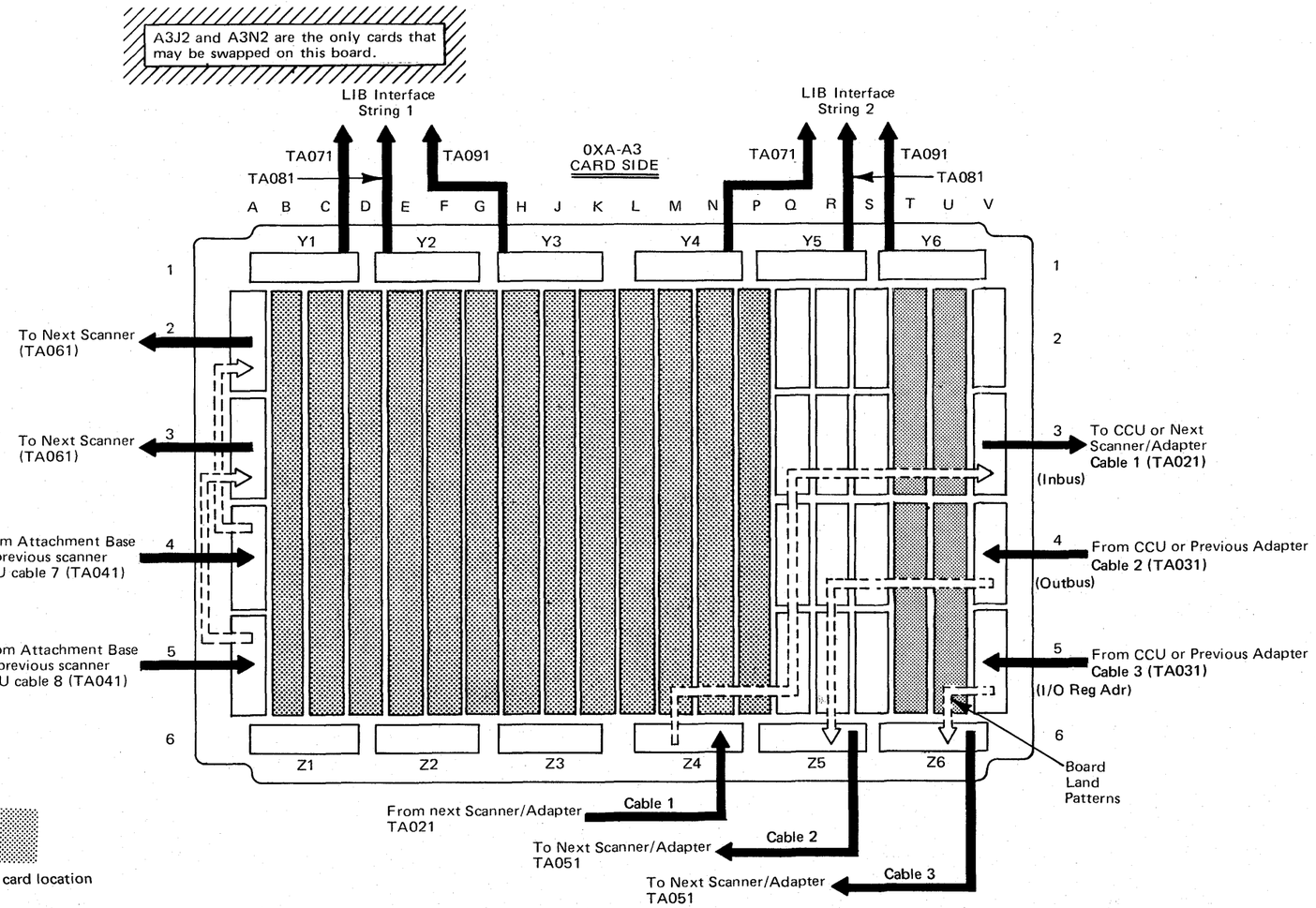
TYPE 2 ATTACHMENT BASE DATA FLOW

The logic for the attachment base is located on two MST cards A-B3D2 and A-B3E2. The logic is distributed between the cards as indicated on this page.



TYPE 2 COMMUNICATION SCANNER BOARD LAYOUT

Card Location	ALD Page	Function
A3B2	TB211	Inbus powering
	TB231	Dial inputs to SDF
	TB231	Work register gate
	TB241	BCC Drive
A3C2	TB111	Mask LIB errors
	TB121	BCC errors
	TB131	Check register
	TB141	Ser L1 interrupt
	TB141	POR latch
	TB141	POR or sel LIB reset
	TB151	Gate test points CSB errors
	TB161	Check register parity
	TB161	Inbus parity bit
A3D2	TA911	Input-Output decode
	TA921	I.W. output remember latches
	TA931	Display register
	TA941	CSB clock
A3E2	TA311	Data out 7
	TA311	Test data
	TA321	Ctrl out A and B
	TA321	Ctrl in A and C
	TA331	B data register
	TA341	Feedback check
	TA341	Data in 1-7
	TA341	Modem rec space/DPR
	TA361	Bit service reset
	TA371	Ctrl in/out termination
A3F2	TA811	New PCF
	TA811	PCF decode
	TA821	Set PCF states 0-4-5-6-9-C
	TA831	Interrupt Go
	TA841	Set LCD C, D
	TA841	Set PCF state 7
	TA851	SDF 0-8 is empty
A3G2	TB011	Ones CTR & last line state
	TB011	Insert/Delete 0
	TB011	Flag/Abort detect
	TB011	NRZI encode
	TB031	Outreg
	TB041	Upper scan limit latches
	TB051	New bit
	TB061	Display request
A3H2	TA211	SDF update controls
	TA221	SDF direct update
	TA221	SDF shift update
	TA231	SDF output update
	TA231	PDF update
	TA261	Tag generation
	TA261	Tag detection
	TA271	New SDF
A3J2	TA545	ICW local store 23-44, P2
	TA565	ICW local store parity error
	TA571	ICW local store parity generation
A3K2	TA411	Input register
	TA451	Parity generation and check
A3L2	TA611	Interrupt generation
	TA611	Priority Available
	TA621	CSB BAR and parity check
	TA631	LIB select
	TA621	Address select
	TA651	Address parity and check



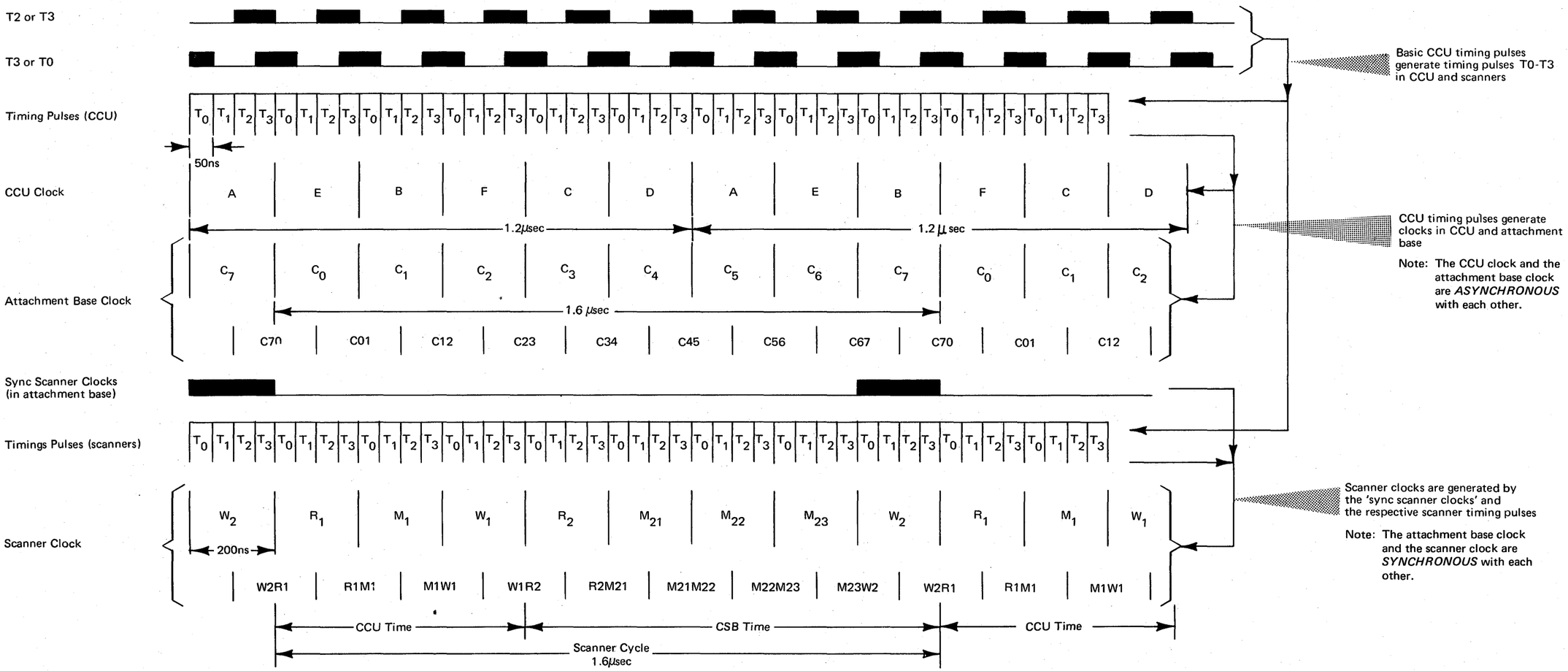
Card Location	ALD Page	Function
A3M2	TA711	SDF to PDF 4-5-6-7-8 bit transfer
	TA731	PDF direct
	TA731	Out reg to PDF
	TA741	New PDF
	TA761	Data out 1-2-3-4-5-6

Card Location	ALD Page	Function
A3N2	TA511	ICW local store 0-22, P1
	TA531	ICW local store parity error
	TA535	ICW local store parity generation
A3P2	TA111	LCD decode and update
	TA121	New SCF 0-7
	TA121	Sw-line security
	TA151	LCD, PCF powering

Card Location	ALD Page	Function
A3T2	TB411*	Internal Xmt-Rcv Oscillator 0
A3T4	TB412*	Internal Xmt-Rcv Oscillator 1
A3U2	TB413*	Internal Xmt-Rcv Oscillator 2
A3U4	TB414*	Internal Xmt-Rcv Oscillator 3

*Contains card P/N by bit rate

CLOCK AND TIMINGS – BRIDGE STORAGE



CCU Time – Program addressing occurs as described on B-010 and B-290. ABAR supplies the address of the ICW that the control program wants to input or output.

R1 – ICW local store read out

M1 – ICW content modified as required by an Input or Output instruction.

W1 – Modified ICW contents written into ICW local store

CSB Time – Scan addressing occurs as described on B-010 and B-220. Each scanner uses the address from the scan counter to determine the state of a line on that scanner and to modify the contents of the associated ICW, if required, if bit service request is active.

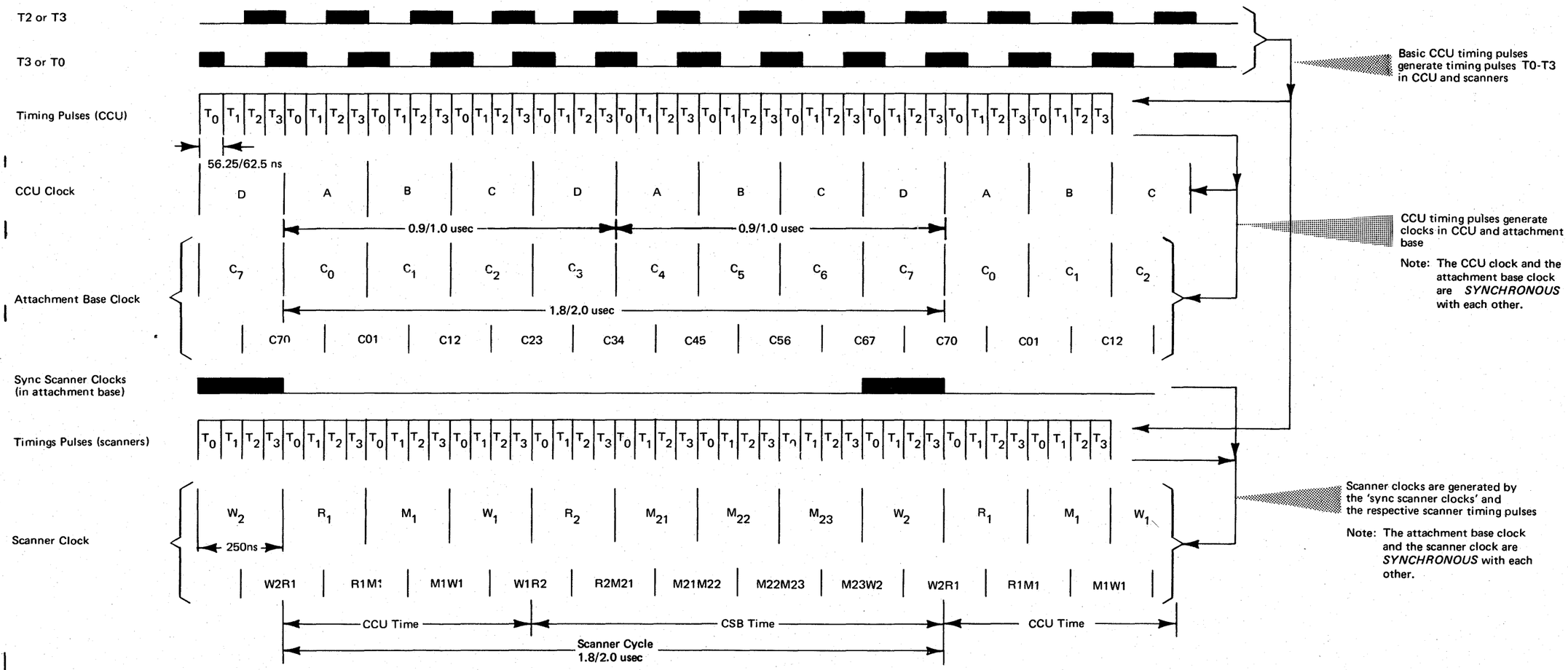
R2 – ICW local store read out

M21, M22, M23 – ICW contents modified as required if bit service request is active from the interrogated line.

W2 – Modified ICW contents written into ICW local store

CLOCK AND TIMINGS – FET STORAGE

Models J-L/E-H



CCU Time – Program addressing occurs as described on B-010 and B-290. ABAR supplies the address of the ICW that the control program wants to input or output.

- **R1** – ICW local store read out
- **M1** – ICW content modified as required by an Input or Output instruction.
- **W1** – Modified ICW contents written into ICW local store

CSB Time – Scan addressing occurs as described on B-010 and B-220. Each scanner uses the address from the scan counter to determine the state of a line on that scanner and to modify the contents of the associated ICW, if required, if bit service request is active.

- **R2** – ICW local store read out
- **M21, M22, M23** – ICW contents modified as required if bit service request is active from the interrogated line.
- **W2** – Modified ICW contents written into ICW local store

ICW CONTROL AND DATA FIELDS

See B-090 for the ICW associated with the autocall interface.

The ICW (interface control word) is the link between the control program and the type 2 scanner, and between the type 2 scanner and the interface hardware. In addition, certain fields within the ICW are used to buffer information about the interface between successive scans.

The ICW is made up of 46 information bits and 2 parity bits and is physically located in the scanner local store. Each scanner contains one ICW for each possible interface that can be attached. The ICW local store contains 96 ICWs, however, only those ICWs associated with an attached interface should be addressed by the control program. The scanner still scans those ICWs that are not associated with an attached interface but are within the range of addresses controlled by the upper scan limit and substitution control register.

PDF (Parallel Data Field)

An eight bit character buffer in the data flow between the program and the ICW serial data field.

SCF (Secondary Control Field)

See B-061 for bit definitions

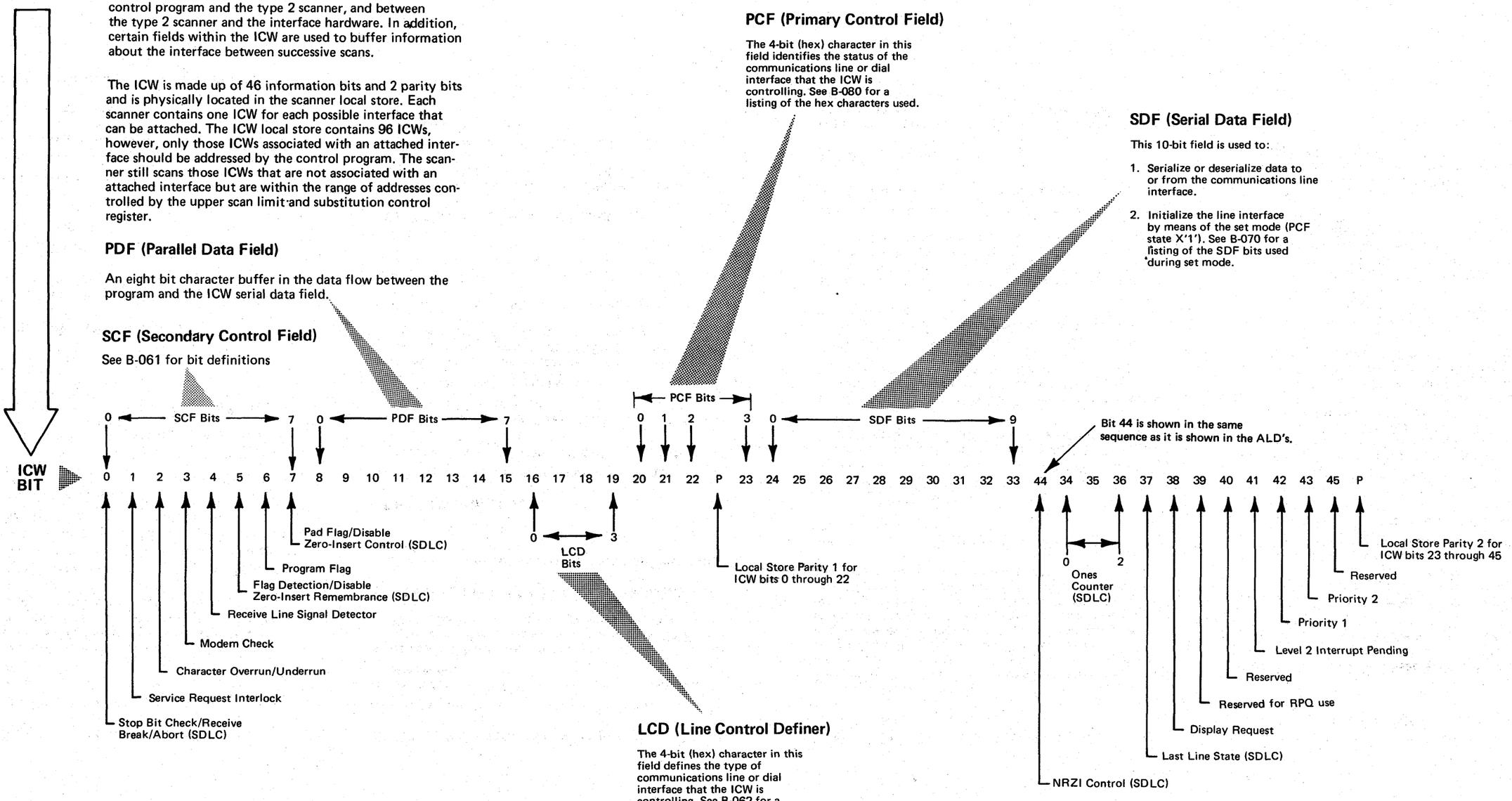
PCF (Primary Control Field)

The 4-bit (hex) character in this field identifies the status of the communications line or dial interface that the ICW is controlling. See B-080 for a listing of the hex characters used.

SDF (Serial Data Field)

This 10-bit field is used to:

1. Serialize or deserialize data to or from the communications line interface.
2. Initialize the line interface by means of the set mode (PCF state X'1'). See B-070 for a listing of the SDF bits used during set mode.



LCD (Line Control Definer)

The 4-bit (hex) character in this field defines the type of communications line or dial interface that the ICW is controlling. See B-062 for a listing of the hex characters used.

ICW–SECONDARY CONTROL FIELD

SCF 0 (Stop Bit Check/Receive Break/Abort)

The scanner sets this bit to a 1 when the scanner detects:

- a space for the stop bit on a start-stop line in the receive state (PCF X'7').
- a 'modem receive space' at 'tag detect' on a start-stop line in the transmit data state (PCF X'9'). When the control program detects this bit set for two consecutive characters, this condition should be interpreted as a 'receive break' signal.
- A 'modem receive space' on line sets 12A and 12B in the transmit data state (PCF X'9'). When the control program detects this bit set for five consecutive characters, this condition should be interpreted as a 'break' signal.
- seven consecutive one bits (SDLC abort) in the receive data stream on a SDLC line in the receive information state (PCF X'6 or 7').

SCF 0 set to a 1 resets SCF 1 (service request interlock).

The service routine executes an Output X'44' with byte 0.0 set to a 1 to reset this bit to 0.

SCF 1 (Service Request Interlock)

The scanner sets this bit to 1 when the scanner signals for a level 2 interrupt request by raising 'interrupt go' except when:

- SCF bits 0, 2, or 3 are set or being set.
- a SDLC Flag is detected.
- a SDLC abort is detected.

This bit is reset to 0 when:

- a SDLC abort is detected.
- the service routine executes an Output X'44' with byte 0.1 set to a 1.
  SCF bits 0, 2, or 3 are set to 1.

The scanner uses this bit for overrun/underrun detection.

SCF 2 (Character Overrun/Underrun)

The scanner sets this bit to 1 when the scanner:

- attempts to set SCF 1 (service request interlock) and it is already set.
- detects a SDLC Flag in other than the predicted position in the SDF when in receive information state (PCF X'7'). See B-530 for information on predicted position.

SCF 2 set to a 1 resets SCF 1 (service request interlock)

The control program executes an Output X'44' with byte 0.2 set to 1 to reset this bit to 0.

SCF 3 (Modem Check)

The scanner sets this bit to 1 if the scanner detects:

- Data Set Ready is inactive during PCF states 5 through D for start-stop, BSC, or SDLC.
- Clear To Send is inactive during PCF states 9, A, B, or D for start-stop, BSC, or SDLC.
- a TTY echo check for start-stop.
- receive line signal detect (carrier detect) inactive on a start-stop line in receive state (PCF X'7') when the pad flag (SCF 7) is a 1 (switched line security).

SCF 3 set to a 1 resets SCF 1 (service request interlock).

The control program executes an Output X'44' with byte 0.3 set to a 1 to reset this bit to 0.

SCF 4 (Receive Line Signal Detector)

The scanner sets this bit to 1 if the modem is receiving a carrier signal for a start-stop, BSC, or SDLC line interface.

The scanner resets this bit to 0 when the carrier signal becomes inactive.

SCF 5 (Flag Detection/Disable Zero-Insert Remembrance)

SDLC Receive Operation
The scanner sets this bit to 1 when a Flag is detected in the receive data stream when in PCF states X'4, 5, 6, or 7' and when using LCD codes X'8, 9'. This bit set to 1 does not cause a level 2 interrupt but a level 2 interrupt may be generated because of the change of PCF states caused by detecting the Flag. For example; a Flag detected in PCF X'7' sets PCF state 6 and this activates the signal 'interrupt go' which starts the level 2 interrupt request.

The control program executes Output X'44' with bit 0.5 set to 1 to reset SCF 5.

SDLC Transmit Operation
The scanner sets this bit to 1:

- as a character is transferred from the PDF to the SDF (tag detected) while in PCF state X'8, 9, A, C, or D and using SDLC code if SCF 7 (disable zero-insert control) is set to 1.
- when the scanner is in PCF X'8' (initial transmit) using SDLC code when Clear To Send becomes active. The scanner sets PCF X'9' at the same time.

While SCF 5 is a 1, the ones counter is forced to a state of 001 which disables the automatic insertion of a zero after five consecutive one bits.

The scanner resets this bit to 0 on a transmit operation as the tag is detected if SCF 7 is a 0. While SCF 5 is a 0, the ones counter controls inserting a zero bit in the data stream after the transmission of 5 consecutive one bits.

The control program must *never* reset SCF 5 (Output X'44' with bit 0.5 set to 1) when in transmit mode.

SCF 6 (Program Flag)

The control program executes Output X'44' with byte 0.6 set to a 1 to set this bit to a 1. This bit is used for program test and skip purposes.

The control program executes Output X'44' with byte 0.6 set to a 0 to reset this bit to a 0.

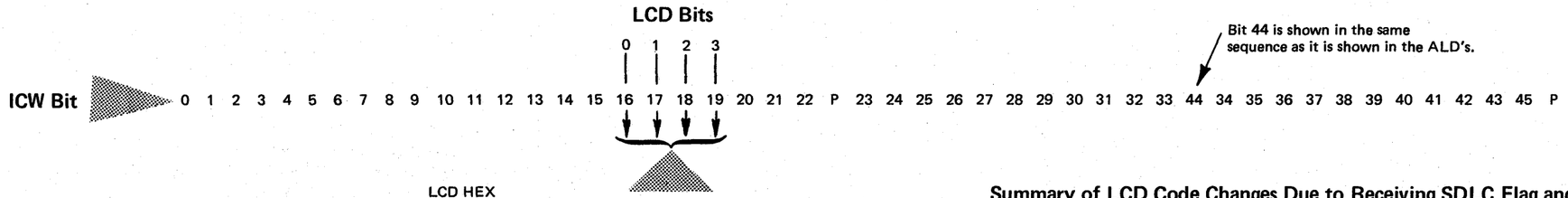
SCF 7 (Pad Flag/Disable Zero-Insert Control)

This bit is set to a 1 by the service routine (Output X'44' with byte 0.7 set to 1) when:

- the 'send data' line must be held at a mark level for the complete character time for a start-stop transmission. When this bit is set to a 1, the scanner forces a mark for the start bit. The other mark bits deserialize normally from a X'FF' simultaneously set in the PDF.
- it is desired to monitor 'receive carrier detect' on a start-stop line in receive state (PCF X'7') for switched line security reasons. If 'receive carrier detect' becomes inactive, the scanner sets SCF 3 (modem check) to a 1.
- a Flag or Abort character is set into the PDF on a transmit operation when using SDLC code.
  This 1 state is transferred to SCF 5 (disable zero-insert remembrance) as the next transmit tag is detected. When SCF 5 is a 1, the scanner forces the ones counter to a state of 001 thus blocking the automatic insertion of zero bits after 5 consecutive one bits. This allows the transmission of the Flag or the Abort (X'7F') characters.
- handling the level 2 interrupt for the address character on a receive operation (PCF X'7') when using SDLC code.
  The 1 state is not transferred to SCF 5 during the receive operation. When SCF 7 is a 1, the active level of receive 'tag detected' forces a '7 bit xfer' which insures transferring the entire 8-bit control character to the PDF.

The service routine executes Output X'44' with byte 0.7 set to 0 to reset this bit after the desired action has been completed.

ICW—LCD FIELD



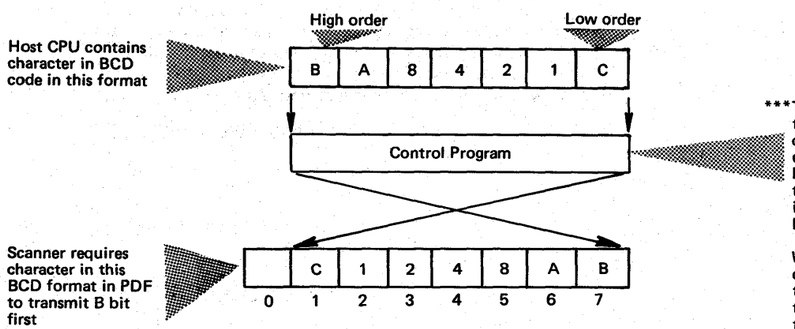
LCD (Line Control Definer)

The LCD is used during transmit and receive operations to define the line control used by the line set type. The scanner uses the LCD field to determine the position of the character within the PDF (parallel data field) and SDF (serial data field), and to set up the proper PDF—to—SDF transfer during a transmit operation, and the proper SDF—to—PDF transfer during a receive operation.

LCD HEX CHARACTER	EXAMPLE OF TERMINAL TYPE
5	IBM 1030
4	IBM 1050, 1060, 2740, and 2741
6	IBM 2845/2848
C	IBM BSC System with EBCDIC CODE
D	IBM BSC System with USASCII CODE
3	Autocall
9	IBM 3705 (with Remote Program Loader)

LCD HEX CHARACTER		TYPE OF LINE CONTROL
0	***	Start-Stop 9 bits per character—6 data bits—1 start bit 2 stop bits on transmit
1		Not Used
2	***	Start-Stop 8 bits per character—5 data bits—1 start bit 2 stop bits on transmit
3		Dial (Auto-Call Unit)
4	***	Start-Stop 9 bits per character—7 data bits—1 start bit 1 stop bit
5	***	Start-Stop 10 bits per character—7 data bits—1 start bit 2 stop bits on transmit
6	***	Start-Stop 10 bits per character—8 data bits—1 start bit 1 stop bit
7	***	Start-Stop 11 bits per character—8 data bits—1 start bit 2 stop bits on transmit
8		Monitor Flag
9		SDLC 8 bit byte length
A		Reserved
B		Reserved
C		EBCDIC
D		USASCII
E		Reserved
F	****	Feedback Error

Example—LCD X'4'



***These LCD states require the control program to reverse the character before executing Output X'44' (to place the character in the PDF for transmit operations), or after executing Input X'44' (to obtain the character from the PDF for receive operations). This only occurs if the terminal requires the high order bit of the data character in the host CPU to be the first data bit on the transmission line. This is shown as the B bit in the LCD X'4' example.

When the terminal requires the low order bit of the data character in the host CPU to be the first data bit on the transmission line, the control program should not reverse the character as above. For example: LCD X'6' when the terminal is the IBM 2848.

Summary of LCD Code Changes Due to Receiving SDLC Flag and BSC SYN Characters

LCD State	Flag* Detected During PCF X'4, 5, or 7'	Flag* Detected During PCF X'6'	EBCDIC SYN (X'32') Character Detected During PCF X'4 or 5'	USASCII SYN (X'16') Character Detected During PCF X'4 or 5'
LCD X'9' (SDLC 8)	• Sets LCD X'9' • Resets SDF** • Inserts 'tag' bit in SDF 2 • Sets PCF X'6' • Causes a level 2 interrupt request • Sets SCF 5 bit • Inhibits set of SCF 1 • Inhibits SDF-to-PDF transfer • Checks that Flag was received on 'boundary' (state 7 only)	• Sets LCD X'9' • Resets SDF** • Inserts 'tag' bit in SDF 2 • Leave in PCF X'6' • Inhibits level 2 interrupt request • Sets SCF 5 bit • Inhibit set of SCF 1 • Inhibits SDF-to-PDF transfer	• Sets LCD X'C' • Sets PCF X'7' • Resets SDF** • Inserts 'tag' bit in SDF 2	• Sets LCD X'D' • Sets PCF X'7' • Resets SDF** • Inserts 'tag' bit in SDF 2

LDC State	Flag* Detected During PCFX'5'
LCD X'8' (Monitor Flag)	• Sets LCD X'9' • Resets SDF** • Inserts 'tag' bit in SDF 2 • Sets PCF X'6' • Causes a level 2 interrupt request • Sets SCF 5 bit • Inhibits set of SCF 1 • Inhibits SDF-to-PDF transfer

*'SDLC Frame Detect' is the notation used in the ALD logic for 'Flag Detect'.
**The scanner resets the SDF by inhibiting 'shift' and leaving 'SDF direct' inactive.

****A Feedback error can be forced by the 3705 Emulation Program to set up presentation of Equipment check sense for some level 1 errors. See Emulation Program Logic Manuals SY30-3001 and SY30-3031.

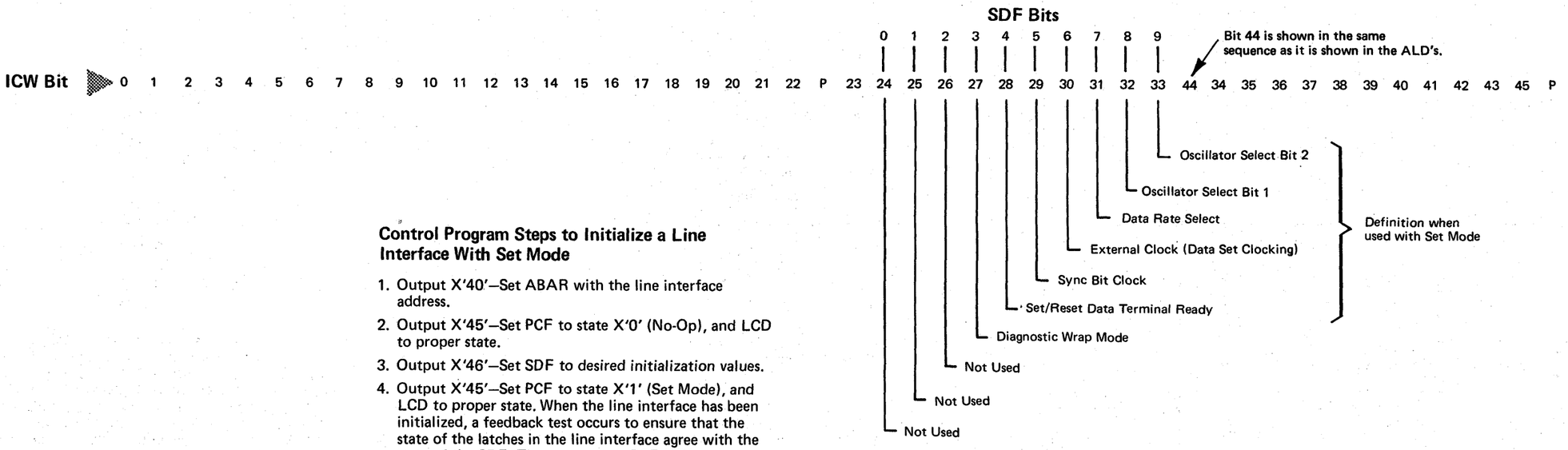
ICW–SDF FIELD

See B-090 for autocall interface

SDF (Serial Data Field)

The SDF is primarily used as a character serializer/deserializer field. On receive operations, the data coming from the line interface is placed in the SDF bit-by-bit to assemble a character. The character transfers to the PDF after the character has been assembled. The program must execute Input X'44' to obtain the character. When transmitting, the character transfers from the PDF to the SDF under hardware control. The SDF sends a bit at a time to the line interface where the bits are sent to the line or modem.

Set Mode (PCF X'1') uses the SDF to initialize the line interface. The definition of the SDF bits, when used for Set Mode, is shown below.



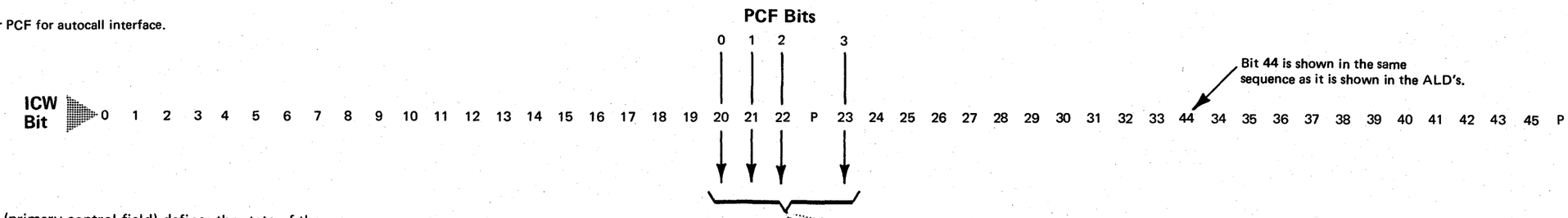
Control Program Steps to Initialize a Line Interface With Set Mode

1. Output X'40'–Set ABAR with the line interface address.
2. Output X'45'–Set PCF to state X'0' (No-Op), and LCD to proper state.
3. Output X'46'–Set SDF to desired initialization values.
4. Output X'45'–Set PCF to state X'1' (Set Mode), and LCD to proper state. When the line interface has been initialized, a feedback test occurs to ensure that the state of the latches in the line interface agree with the state of the SDF. The scanner sets PCF X'0' and generates a level 2 interrupt request.

   If a feedback check occurred, the scanner sets the LCD to state F (Feedback Error).

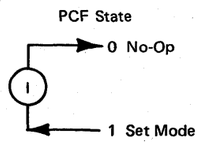
ICW—PRIMARY CONTROL FIELD

See B-090 for PCF for autocall interface.



- The PCF (primary control field) defines the state of the line interface at any particular time. It is used to buffer the operation being performed on that line interface between successive scans.
- The control program initially sets the status of the PCF.
- The control program executes Output X'45' to set or change the PCF state.
- The type 2 scanner automatically changes PCF status under certain conditions (see diagrams).
- The control program executes Input X'45' to determine the PCF status.
- The scanner interpretation of the PCF depends upon the state of the LCD field. The interpretations for a binary synchronous interface, a start-stop interface, and a synchronous data link control interface are shown on this page. See B-090 for the interpretation of the PCF for an autocall interface.

Explanation of diagrams.

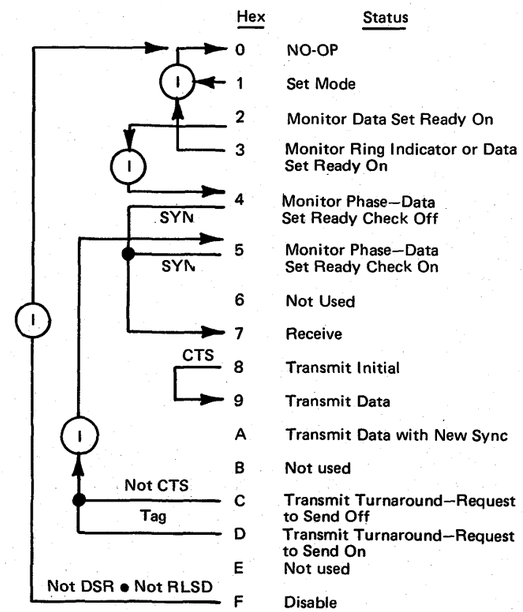


The control program sets PCF X'1'. This is indicated by no line going toward 1.

Once the scanner executes set mode (PCF X'1'), the scanner automatically sets PCF X'0' (No-Op). This is indicated by the line leaving 1 and going to 0. A level 2 interrupt request occurs and is indicated by the (1) inserted within the line.

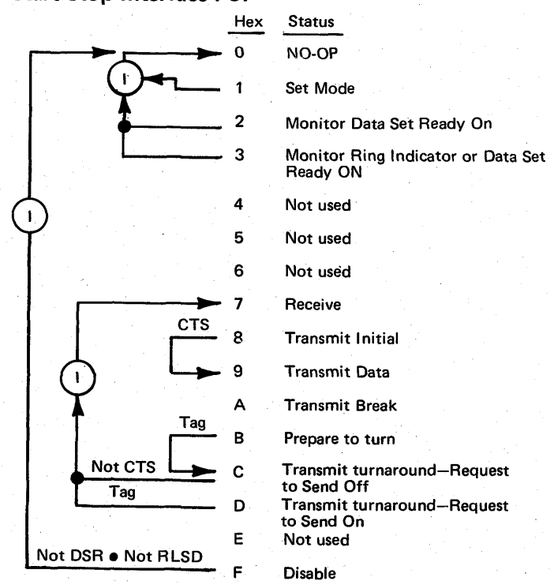
Note: See B-310 for the logic circuits that cause 'interrupt go'. This causes the level 2 interrupt request.

BSC (Binary Synchronous) Interface PCF

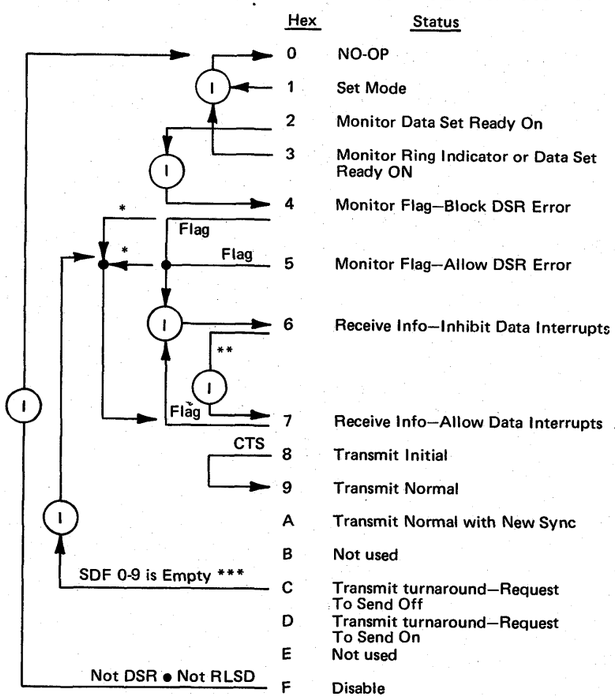


For a complete description of these PCF states and the conditions under which they are used, see the IBM 3704 and 3705 Communications Controllers Principles of Operation, GC 30-3004.

Start-Stop Interface PCF



SYNCHRONOUS DATA LINK CONTROL Interface PCF



*EBCDIC or USASCII 'SYNC' character received in LCD X'9' (SDLC 8).
**Tag • non-Flag character
*** When PCF state C is executed in SDLC mode, the normal 'tag detected' (SDF 0-8 is empty and SDF 9=1) is delayed until a zero is shifted into SDF 9. During the next gated bit service, the 'SDF 0-9 is empty' condition generates the 'tag' line that (1) resets the RTS and transmit mode latches in the line interface, (2) sets PCF state X'5' (Monitor Flag-Allow DSR Error), and (3) places the line in a level 2 interrupt pending state.

ICW-BITS 34-37 AND 44 (SDLC)

ICW Bits 34-36 (SDLC Ones Counter)

SDLC Receive Operation
The ones counter is used to detect:

- inserted zeros to be deleted from the bit stream during PCF X'6 or 7'. 1
- Flag sequences during PCF X'4, 5, 6, or 7'. 2
- seven consecutive ones sequence (Abort) during PCF X'6 or 7'. 3

SDLC Transmit Operation
The ones counter is used to insert a zero after five consecutive one bits during PCF X'8, 9, A, C, or D' when SCF 5 (disable zero-insert remembrance) is a 0. 4

Ones Counter Controls
The scanner adds 1 to the ones counter at 'SDLC bit time' when the ones counter is not zero and a 1 was transmitted 5 or received provided SCF 5 bit is 0 when in the transmit state. Adding 1 with the count at 7 causes the ones counter to go to 000 which stops the counting. This occurs when the Abort sequence is detected.

The scanner resets the ones counter to 001 at 'SDLC bit time' when:

- 'Xmt data' is 0 when in PCF states X'8, 9, A, C, or D'. 6
- the received bit is 0 (normal mode) when in PCF states X'4, 5, 6, or 7'.
- the received bit differs from the last line state (NRZI mode) when in PCF states X'4, 5, 6, or 7'. 7
- 'new SCF 5' (disable zero-insert remembrance) is a 1 when in PCF states X'8, 9, A, C, or D'. 8

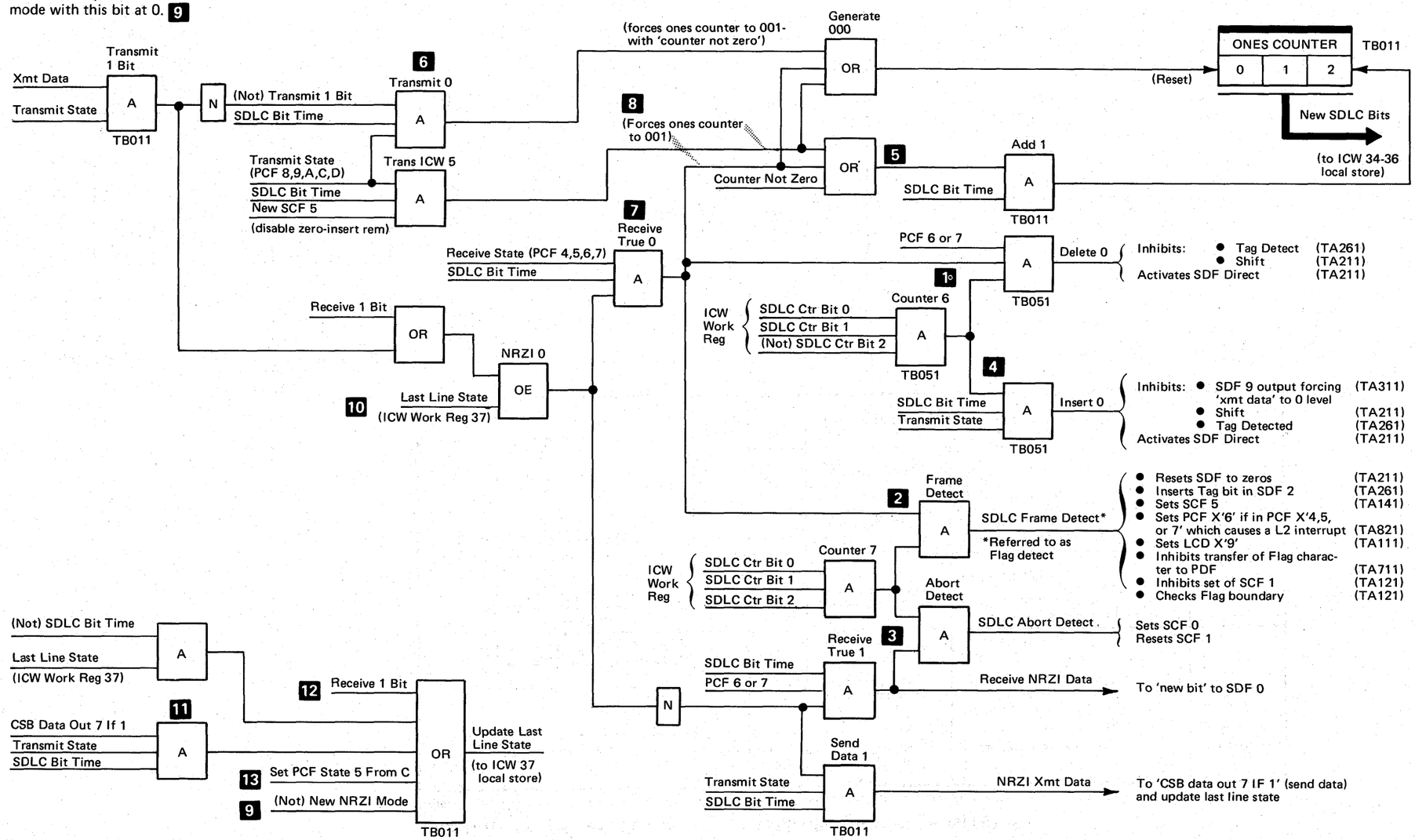
ICW Bit 37 (Last Line State)

- The scanner holds this bit at a 1 during normal mode (ICW bit 44=0). When this bit is a 1, it conditions the Exclusive OR circuit to pass the transmitted and received bits unchanged. 10
- During a NRZI mode transmit operation, the scanner sets this bit to the state of the bit being sent to the LIB. 11
  - When Clear To Send is inactive and the line interface is in PCF state 8, 'xmt data' is at the 1 (mark) level and the scanner sets this bit to 1.
  - When Clear To Send is active, the scanner sets this bit to 1 if the 'xmt data' state is the same as the old last line state. If different, the scanner resets this bit to 0.
- During a NRZI mode receive operation, the scanner sets this bit to 1 when the received bit from the LIB is a 1 and resets this bit to 0 when the received bit is a 0. 12
- The scanner sets this bit to 1 when PCF state 5 is set from PCF state C when Clear To Send becomes active. 13
- Control program sets this bit to 1 by executing Output X'47' with byte 1.1 set to 1 for diagnostic purposes.
- Control program resets this bit to 0 by executing Output X'47' with byte 1.1 set to 0.

ICW Bit 44 (NRZI Control)

Control program sets this bit to 1 by executing Output X'46' with byte 0.0 set to 1. This causes the data to be transmitted in NRZI mode when in PCF state X'9, A, C, or D'. In NRZI mode the 'send data buffer' in the line interface is complemented when a zero is transmitted and unchanged when a one is transmitted.

Control program resets this bit to 0 by executing Output X'46' with byte 0.0 set to 0. Data is transferred in normal mode with this bit at 0. 9



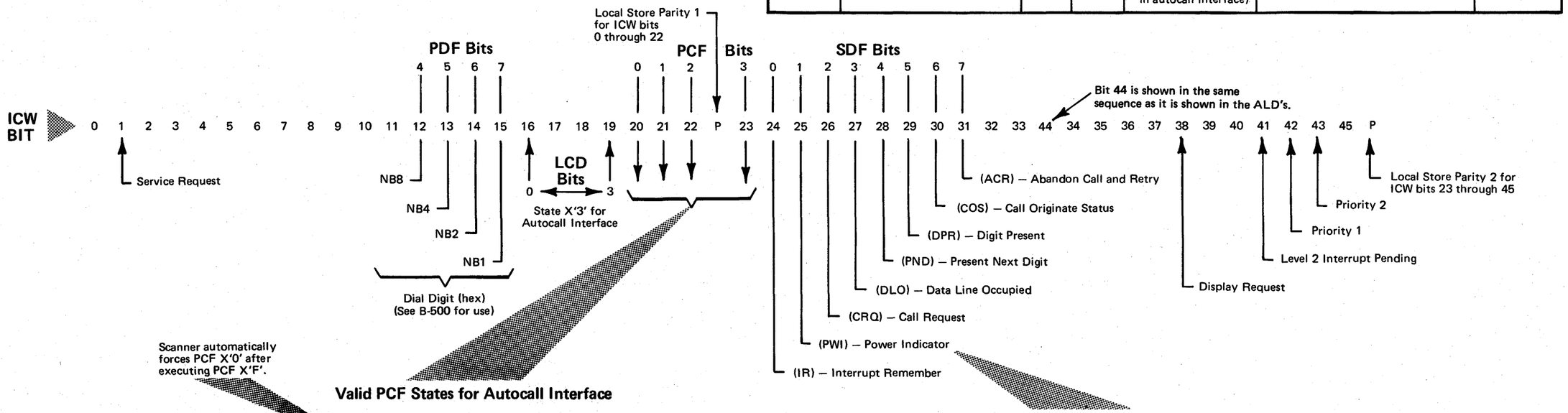
ICW FOR AUTOCALL INTERFACE

- The bits/fields shown below are the only positions of the ICW defined for autocall interfaces.
- For proper autocall interface operation, the LCD field of the ICW associated with an autocall interface must be set to X'3'. Autocall interface operation is then controlled by the state of the PCF field of the ICW associated with the interface.
- The lowest speed internal clock installed in each scanner (OSC 0) generates bit service requests for all autocall interfaces installed in the LIBs supported by the scanner.

SUMMARY OF THE EFFECT OF PCF STATES UPON ICW BIT POSITIONS

Note: To be effective, LCD state must be X'3' during the scan of the autocall interface and a bit service request must be detected.

PCF State (Hex)	Conditions To Set PCF	CRQ (SDF 2)	DPR (SDF 5)	NB 1,2,4,8 (Dial Digit-hex)	Level 2 Interrupt Request	IR (SDF 0)
0	1 — By control program 2 — From PCF X'F' when ACR, COS,PND' and DLO inactive	Reset	Reset	Zeros (resets digit buffer in autocall interface)	1— Yes, after PCF changes state to 0 2— See state 'F'	No Change
4	By control program PND falls in PCF X'8'	Set	Reset	Zeros (resets digit buffer in autocall interface)	Yes—if IR is reset and ACR, COS, or PND lead is active No—if IR bit is set	Set No Change
5	By control program	Set	Reset	Zeros (resets digit buffer in autocall interface	Yes—if IR is reset and COS or ACR lead is active No— if IR bit is set	Set No Change
8	By control program	Set	Set	Dial digit from PDF 4—7	No	No
F	By control program	Reset	Reset	Zeros (resets digit buffer in autocall interface)	Yes— when ACR,DLO,COS, and PND leads are all inactive	No



- If an autocall interface has a bit service request when scanned, the following lines from the ACU (Automatic Calling Unit) set the SDF as long as the LCD state is X'3' (autocall interface):

  'Power Indicator'

  'Data Line Occupied'

  'Present Next Digit'

  'Call Originate Status'

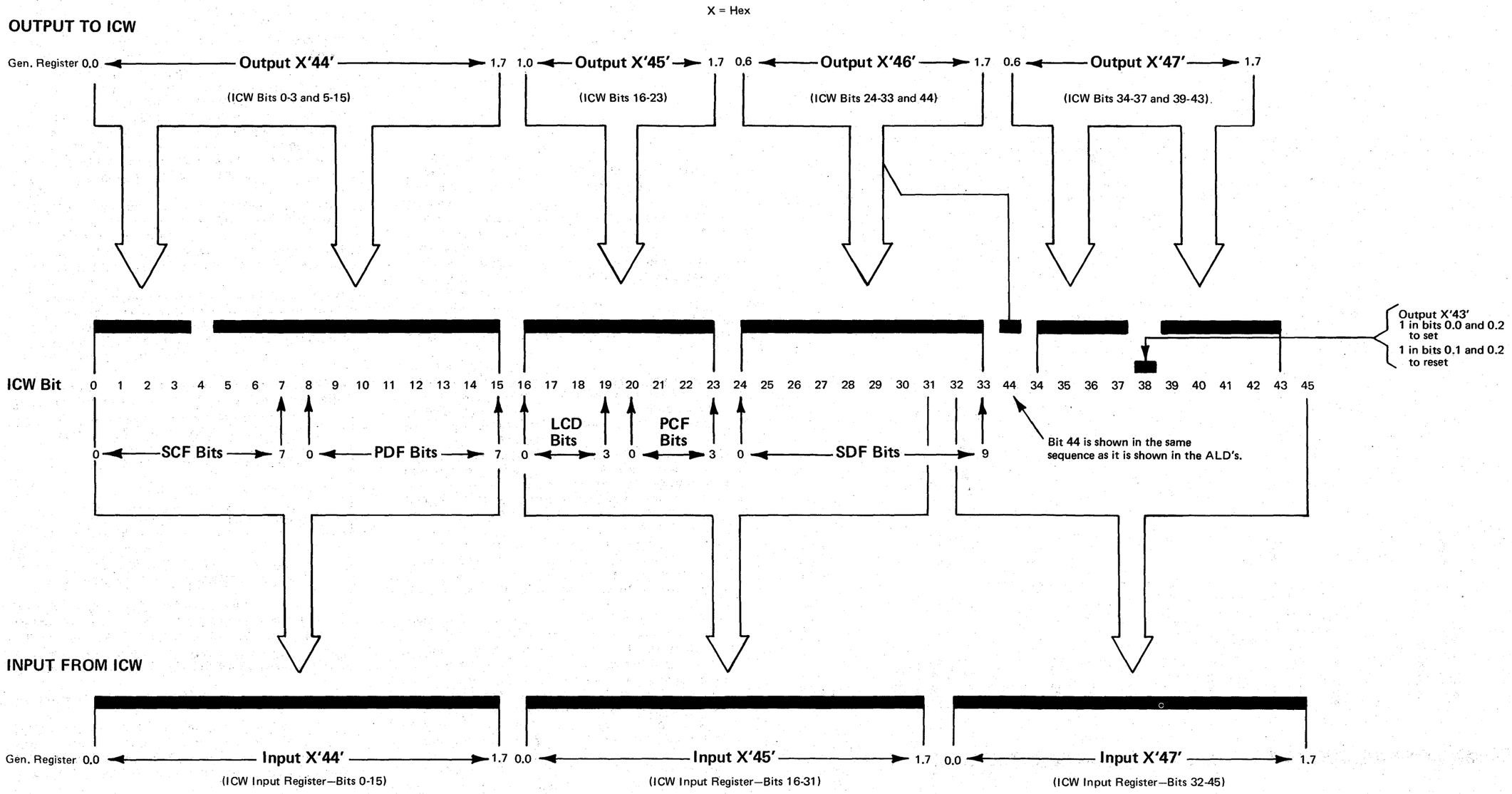
  'Abandon Call and Retry'

- The states of SDF bits 1-9 have no effect on the autocall interface operation.
- SDF 0 (Interrupt Remember) is the only SDF bit that affects the interface operation.
- See B-500 for the use of CRQ and PND.

ACCESS OF ICW BY INPUT/OUTPUT INSTRUCTION

X = Hex

OUTPUT TO ICW



INPUT FROM ICW

Note: The ICW parity bits are not included in the data transferred by the input instruction. The scanner generates parity for the data placed on the CCU inbus.

INPUT AND OUTPUT INSTRUCTIONS

The type 2 scanner input/output instructions enable the program to communicate with the line interface bases (LIBs), program interrupt levels, interface control words (ICWs), and type 2 scanner registers.

I/O Programming Considerations

As a general rule, input/output instructions should be issued only when the status of ABAR (attachment buffer address register) and the particular scanner ICW input register is known. An understanding of how those registers are set or loaded is needed for correct execution.

The following chart shows the program levels that can set the ABAR in the attachment base and the ICW input register in the selected scanner.

Program Level	ABAR	ICW Input Register
1	Output X'40'	Cannot set
2	L2 Interrupt	L2 Interrupt
3 or 4	Output X'40'	Output X'40'

The following considerations are recommended for executing input/output instrucitons in the different program levels.

Program Level 1- (Error Routines)

1. Input X'40' can be executed to obtain the interface address in the attachment buffer address register. This old interface address should be saved if a different address is required to select the scanner that has its 'L1 interrupt request' set.
2. Output X'40' can be executed to select the appropriate scanner if needed. Only the selected scanner can decode the input/output instructions.
   Note: The selected scanner ICW input register is not changed if an Output X'40' is executed at program level 1.
3. After the scanner is selected, other input and output instructions may be executed as needed. Output instructions may be executed in any order, but all output instructions (Outputs X'43, 44, 45, 46, 47') that set a portion of the ICW *must* beseparated by at least one cycle. This is required because the output register in the scanner buffers the data from the general register andrequires time to store the data in the ICW.
4. Before exiting from program level 1, Output X'40' may be executed to place the old interface address back in ABAR if it had been saved. However, one instruction cycle must separate Output X'40' from any Output X'43-47'. The selected scanner ICW input register is not changed as a result of Output X'40'.

Program Level 2- (Character Service)-

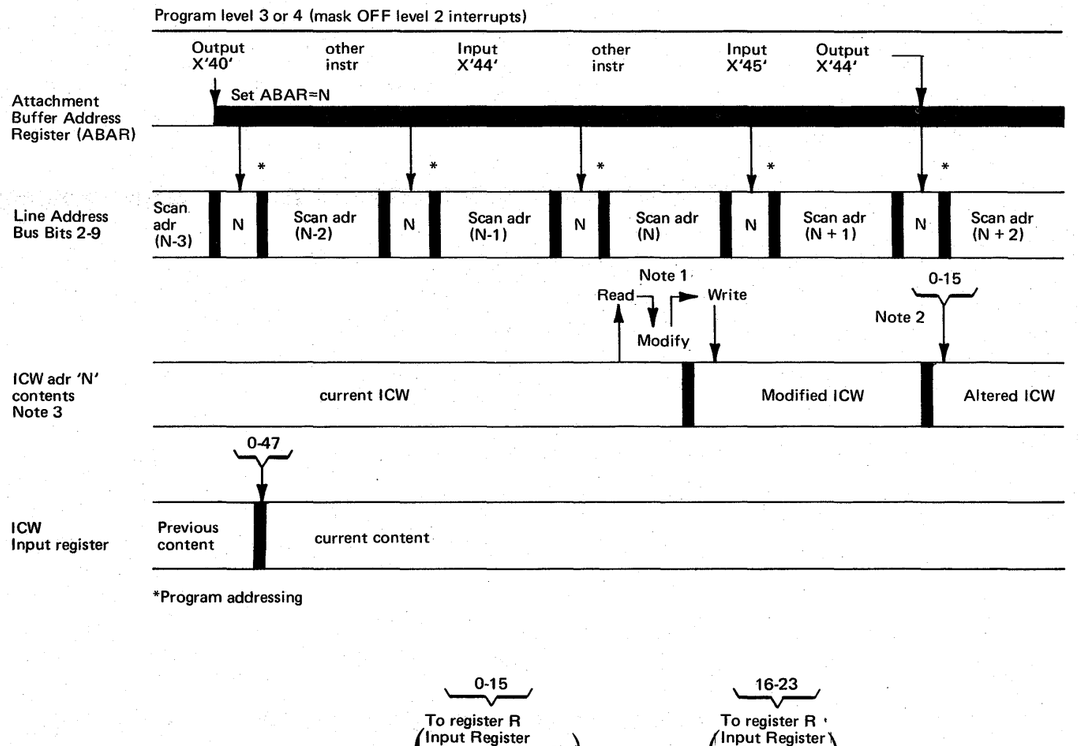
1. Input X'40' may be executed to obtain the interface address.
2. Inputs X'44, 45, or 47' may be executed whenever necessary to obtain a portion of the ICW from the scanner ICW input register; or Outputs X'43, 44, 45, 46, or 47' may be executed to set a portion of the ICW.
3. Output instructions may be executed in any order, but all subsequent Output X'43, 44, 45, 46, or 47' instructions must be separated by at least one cycle. These outputs must also be separated from an Output X'40' by at least one instruction.

Program Levels 3 and 4- (Lower Level Routines)

1. Output X'7E' may be executed with a 1 in byte 1 bit 2 of the register specified by the R field. This will 'mask off' program level 2 interrupts that could change the contents of ABAR by a character service L2 interrupt.
2. Output X'40' may be executed to load ABAR with the interface address of a line to be acted upon. The scanner places the contents of the ICW associated with this interface address in that scanner's ICW input register.
3. After the scanner is selected, (a) Output X'43, 44, 45, 46, or 47' may be executed (to alter the associated portion of the ICW) followed by some other instruction, or (b) some other instruction must be executed, followed by Input X'44, 45, 46, or 47' (to obtain the associated portion of the ICW that was loaded by the Output X'40' into the ICW input registers).

   Note: If Output X'43, 44, 45, 46, or 47' was executed as in (a) above, the ICW content was altered, but the ICW input register still contains the contents of the ICW as it was before the alteration.
4. Output instructions may be executed in any order, but all subsequent Output X'43, 44, 45, 46, or 47' instructions must be separated by at least one cycle.
5. All lines in the addressed type 2 scanner should be disabled before executing an Output X'42' to change the scan limit.
6. Output X'7F' may be executed with a 1 in byte 1, bit 2 of the register specified in the R field. This unmasks the program level 2 interrupts.

Example of Input/Output Instruction Sequence During Program Levels 3 and 4.



Note 1: Current content of the ICW is read out, examined, and modified if needed, then written back into ICW. Modification example: During PCF state 8, 'clear to send' became active, so the scanner sets PCF state 9. The ICW input register will not reflect this modification.
Note 2: Output X'44' alters the ICW content for address N. The ICW input register will not reflect this modification.
Note 3: The scan limit for the selected scanner modifies the interface address on the line address bus to form the ICW address. Scan addressing is modified by the upper scan limit. This example assumes an upper scan limit of 00 (96 lines), therefore no modification occurs.

INPUT X'40' (INTERFACE ADDRESS)

Input X'40' is used to obtain the interface address from ABAR (attachment buffer address register) in the attachment base. When Input X'40' is executed, the attachment base gates the interface address in ABAR to the 0.6 through 1.6 bit positions of the general register specified by the R field. The attachment base also gates a 1 to position 0.4 and a 0 to each of the remaining positions in the general register.

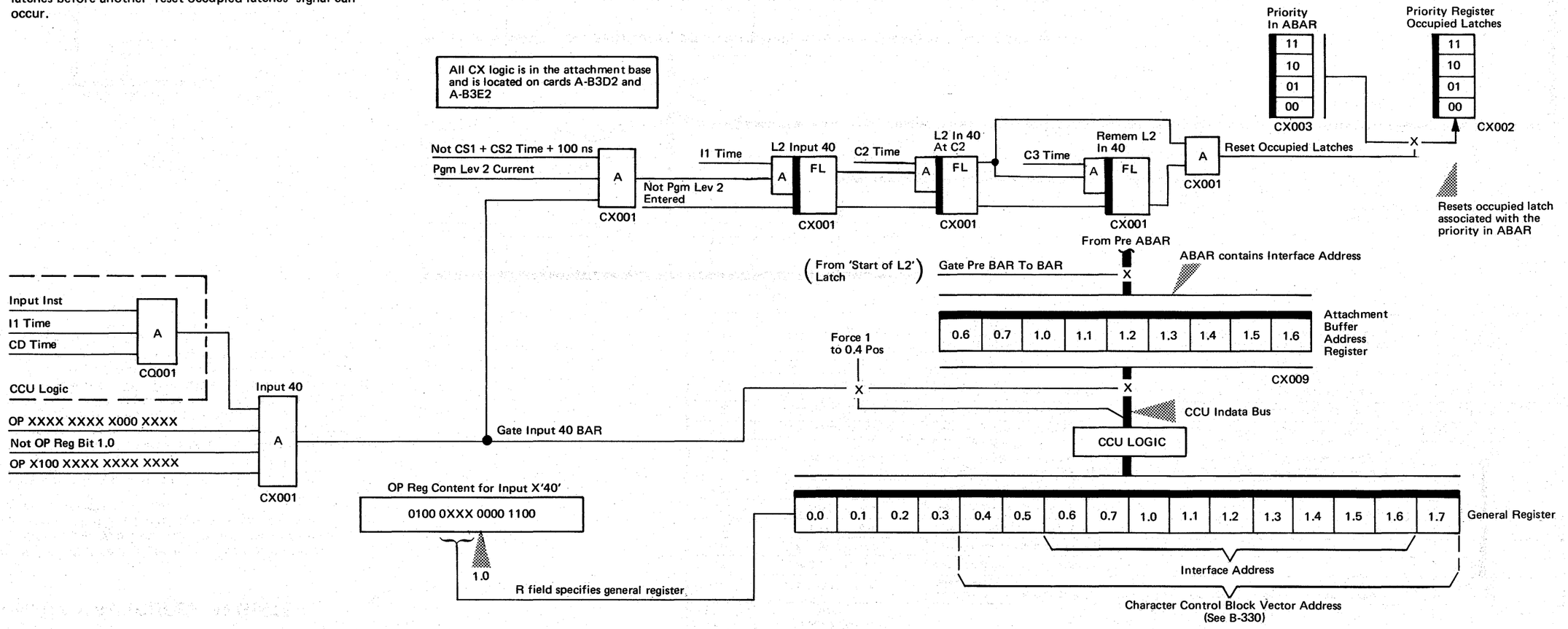
If Input X'40' is executed during program level 2, the attachment base resets the 'priority register occupied' latch associated with the interface address in ABAR. This indicates that (1) the character service request is being serviced by the control program and (2) the 'program level 2 interrupt priority register', from which the ABAR was loaded, is now available for another level 2 interrupt of the same priority. Subsequent Input X'40' instructions within the same character service interrupt do not reset the 'priority register occupied' latches. An exit instruction must be executed in program level 2 to reset the L2 input 40 latches before another 'reset occupied latches' signal can occur.

INPUT X'40' TIMINGS

CCU CLock (*)	A	E	B	F	C	D	A	E	B	F	C	D	B	F	C	D	A
I1 Time of Input X'40'									(Next Instruction)				Exit Instr				
Gate Input 40 BAR																	
Write LS (in CCU)																	
Pgm Lev 2 Entered															Exit		
Pgm Lev 2 Current																Exit	
L2 Input 40 FL																	
Attachment Base Clock (*)	C3	C4	C5	C6	C7	C0	C1	C2	C3	C4	C5	C6	X	X	X	X	
L2 In 40 AT C2 FL																	
Remem L2 In 40 FL																	
Reset Occupied Latches																	

*The CCU clock and attachment base clock are asynchronous, and the relationship shown is assumed for this example.

All CX logic is in the attachment base and is located on cards A-B3D2 and A-B3E2



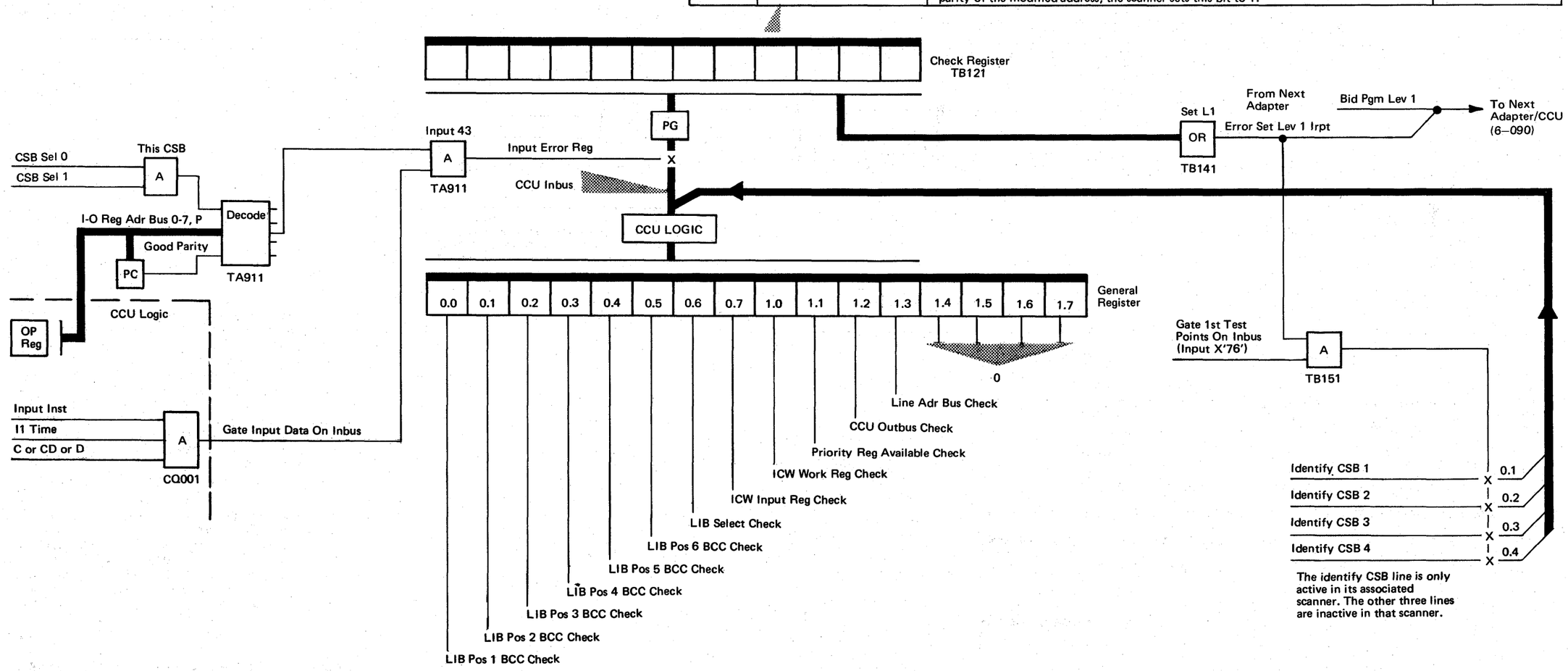
INPUT X'43' (CHECK REGISTER)

Input X'43' is used to obtain the status of the check register in the type 2 scanner. The interface address in the attachment buffer address register selects the scanner that contains the check register.

LEVEL 1 INTERRUPT

If any of the check register bits in a scanner are set to 1, the scanner sets the level 1 interrupt request that bids for a program level 1 interrupt in the CCU. The level 1 routine determines which scanner caused the level 1 interrupt by executing Input X'76'. The control program can set ABAR with an interface address associated with that scanner, and then execute Input X'43' to determine the specific cause for the level 1 interrupt.

General Register (R)	Check Register Position	Cause Of Check	Reference
0.0	LIB 1 BCC Check	Set to 1 if the scanner detects a LIB 1 BCC local store parity error during a bit clock selection.	C-020 C-120
0.1	LIB 2 BCC Check	Same as above for LIB position 2.	
0.2	LIB 3 BCC Check	Same as above for LIB position 3.	
0.3	LIB 4 BCC Check	Same as above for LIB position 4.	
0.4	LIB 5 BCC Check	Same as above for LIB position 5.	
0.5	LIB 6 BCC Check	Same as above for LIB position 6.	
0.6	LIB Select Check	Set to 1 if more than one LIB was selected, or more than one line was accessed on the selected LIB, or no line was accessed on the selected LIB, or a line was accessed on a LIB that was not selected.	
0.7	ICW Input Reg Check	Set to 1 if the scanner detects a parity error (odd) in the ICW input register (46 + 2P).	B-020
1.0	ICW Work Reg Check	Set to 1 if the scanner detects a parity error (odd) in the ICW work register (46 + 2P).	B-020
1.1	Priority Reg Avail Check	Set to 1 if the scanner detects a parity error (even) in the priority register available lines (4 + P).	B-020
1.2	CCU Outbus Check	Set to 1 if the scanner detects a parity error (even) on the Outbus (16 + 2P).	B-020, B-170
1.3	Line Adr Bus Check	The line adr bus parity is used to predict the parity of the address as modified by the scanner's upper scan limits. If this predicted parity does not compare with the actual parity of the modified address, the scanner sets this bit to 1.	B-020 B-(180-210)

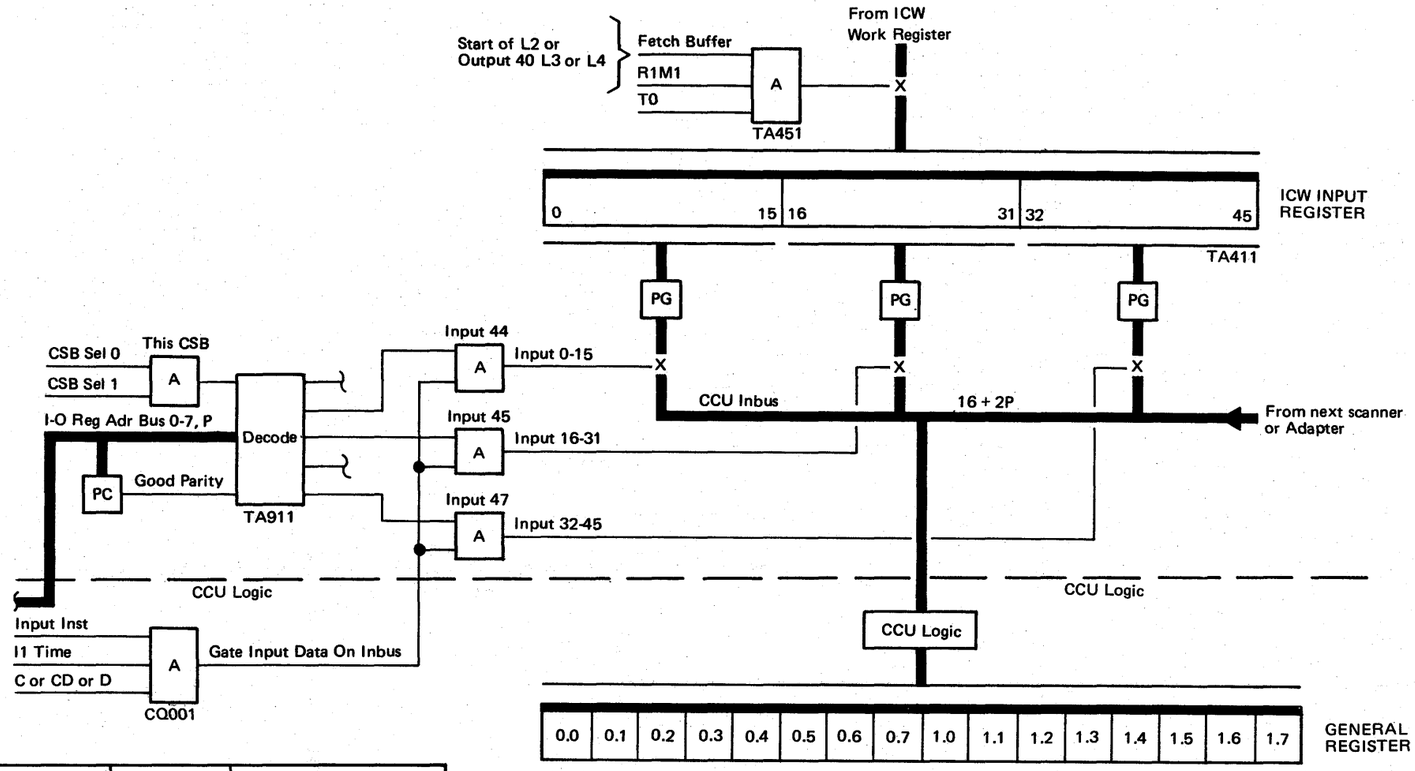


INPUT X'44', X'45', AND X'47'

Input X'44' (ICW Input Register—Bits 0-15). When the scanner decodes Input X'44', the scanner gates the contents of the SCF (secondary control field), and the PDF (parallel data field) to the general register specified by the R field.

Input X'45' (ICW Input Register—Bits 16-31). When the scanner decodes Input X'45', the scanner gates the contents of the LCD (line control definer), PCF (primary control field), and SDF (serial data field) bits 0-7 to the general register specified by the R field.

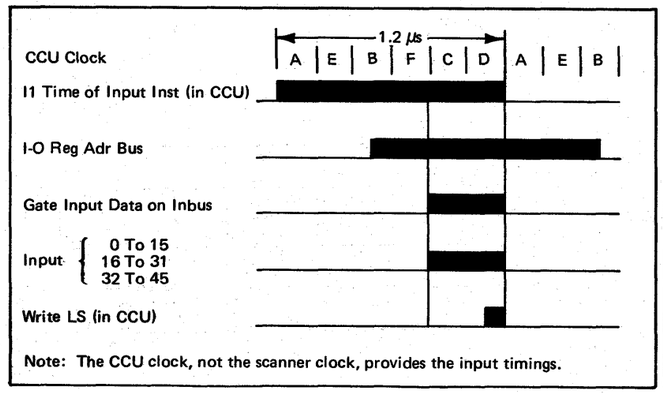
Input X'47' (ICW Input Register—Bits 32-45). When the scanner decodes Input X'47', the scanner gates the contents of SDF bits 8-9, NRZI control bit, ones counter bits 0-2, last line state bit, display request bit, L2 interrupt pending bit, priority bits 1-2, and reserved bits to the general register specified by the R field.



See B-061 for SCF bit definitions

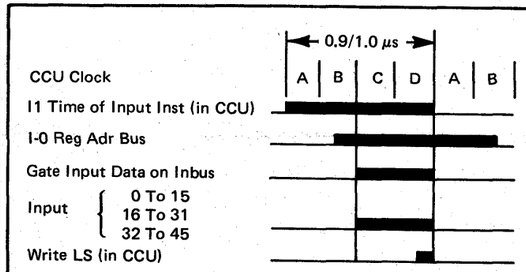
General Register Bit Pos.	Input X'44'	Input X'45'	Input X'47'
0.0	SCF 0 (Stop Bit Check/Receive Break/Abort)	LCD Bit 0	SDF Bit 8
0.1	SCF 1 (Service Request Interlock)	LCD Bit 1	SDF Bit 9
0.2	SCF 2 (Character Overrun/Underrun)	LCD Bit 2	Reserved
0.3	SCF 3 (Modem Check)	LCD Bit 3	Reserved
0.4	SCF 4 (Received Line Signal Detector)	PCF Bit 0	Reserved
0.5	SCF 5 (Flag Detection/Disable Zero-Insert Rem)	PCF Bit 1	Reserved
0.6	SCF 6 (Program Flag)	PCF Bit 2	Display Request
0.7	SCF 7 (Pad Flag/Disable Zero-Insert Control)	PCF Bit 3	Reserved
1.0	PDF Bit 0	SDF Bit 0	Reserved
1.1	PDF Bit 1	SDF Bit 1	L2 Interrupt Pending
1.2	PDF Bit 2	SDF Bit 2	Priority Bit 1
1.3	PDF Bit 3	SDF Bit 3	Priority Bit 2
1.4	PDF Bit 4	SDF Bit 4	NRZI
1.5	PDF Bit 5	SDF Bit 5	Reserved
1.6	PDF Bit 6	SDF Bit 6	Bit is always 0
1.7	PDF Bit 7	SDF Bit 7	Bit is always 0

Input Timing—Bridge Storage



Note: The CCU clock, not the scanner clock, provides the input timings.

Input Timing—FET Storage

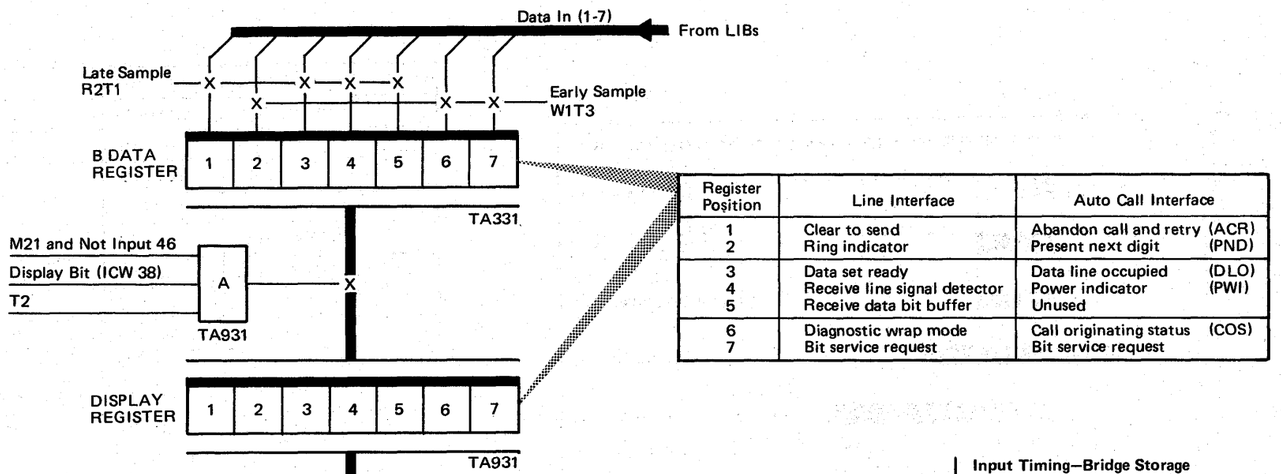


Note: The CCU clock, not the scanner clock, provides the input timings

INPUT X'46' (DISPLAY REGISTER)

This page shows the implementation of Input X'46' within the type 2 scanner, and how the display request bit (ICW bit 38) controls the display register.

When the scanner decodes Input X'46', the scanner gates the contents of the display register to the general register specified by the R field.



Register Position	Line Interface	Auto Call Interface
1	Clear to send	Abandon call and retry (ACR)
2	Ring indicator	Present next digit (PND)
3	Data set ready	Data line occupied (DLO)
4	Receive line signal detector	Power indicator (PWI)
5	Receive data bit buffer	Unused
6	Diagnostic wrap mode	Call originating status (COS)
7	Bit service request	Bit service request

DISPLAY REQUEST OPERATION

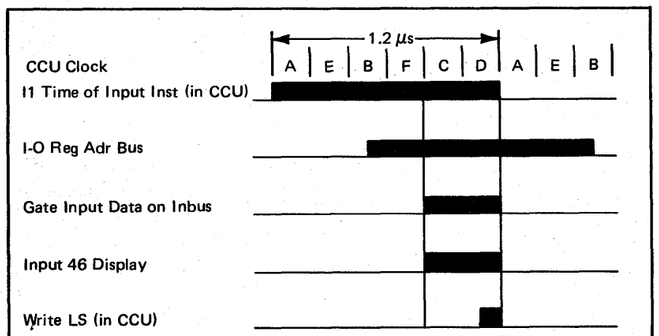
After the attachment base address register (ABAR) has been set to the proper interface address, the control program executes an Output X'43' to set the display request bit (ICW bit 38). As long as the display request bit is on, every scan of that interface causes the display register to trap the contents of the B data register. The display register traps the forced states of 'clear to send', 'data set ready', and 'receive line signal detector' when diagnostic wrap mode is on because these bits are not on in the B data register.

For the display register contents to be meaningful, only one display request bit may be on in an ICW associated with a scanner. Because each scanner contains a display register, each scanner may contain one ICW that uses the display request bit. Input X'46' should not be executed within 153.6 microseconds of the setting of the display bit. This ensures that the data in the display register is valid for the interface just selected and is not the result of a former display trap operation.

General Register Position	Line Interface	Autocall Interface
0.0	Clear To Send: 1 if the CTS line from the modem is on, or if diagnostic wrap forces CTS on.	Abandon Call and Retry: 1 if the ACR line from the autocall unit is on.
0.1	Ring Indicator: 1 if the ring indicator line from the modem is on.	Present Next Digit: 1 if the PND line from the autocall unit is on.
0.2	Data Set Ready: 1 if the DSR line from the modem is on, or if diagnostic wrap forces DSR on.	Data Line Occupied: 1 if the DLO line from the autocall unit is on.
0.3	Receive Line Signal Detector: 1 if the RLSD line from the modem is on, or if diagnostic wrap mode forces RLSD on*.	Power Indicator: 1 if the PWI line from the autocall unit is on.
0.4	Receive Data Bit Buffer: 1 if the line interface receive data bit buffer contains a mark (1). This bit is 0 if the bit buffer contains a space (0).	Bit is always 0.
0.5	Diagnostic Wrap Mode: 1 if the line interface is in diagnostic wrap mode.	Call Originating Status: 1 if the COS line from the autocall unit is on.
0.6	Bit Service Request: 1 if the line interface bit service request is on.	Bit Service Request: 1 if the autocall interface bit service request is on.

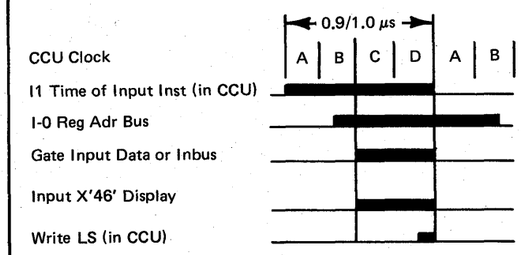
* Diagnostic wrap mode forces Receive Line Signal Detector to a 1 for any line interface under test unless (1) the 3705 has a LIB type 5, 6, 7, 8, 9, 10, or 11 installed or (2) the 3705 was built after October 26, 1973. In both cases, diagnostic wrap mode does not force RLSD to a 1 for any line interface under test in the 3705 and RLSD is controlled by the modem (integrated or external) on the line interface.

Input Timing—Bridge Storage



Note: The CCU clock, not the scanner clock, provides the input timings.

Input Timing—FET Storage



Note: The CCU clock, not the scanner clock, provides the input timings.

OUTPUT X'40', AND X'41'

Output X'40' loads an interface address in ABAR (attachment buffer address register) to the attachment base. When Output X'40' is executed in program levels 3 or 4, the attachment base gates the contents of the ICW work register to the ICW input register where it is available to the control program by means of Input instructions X'44', '45', and '47'.

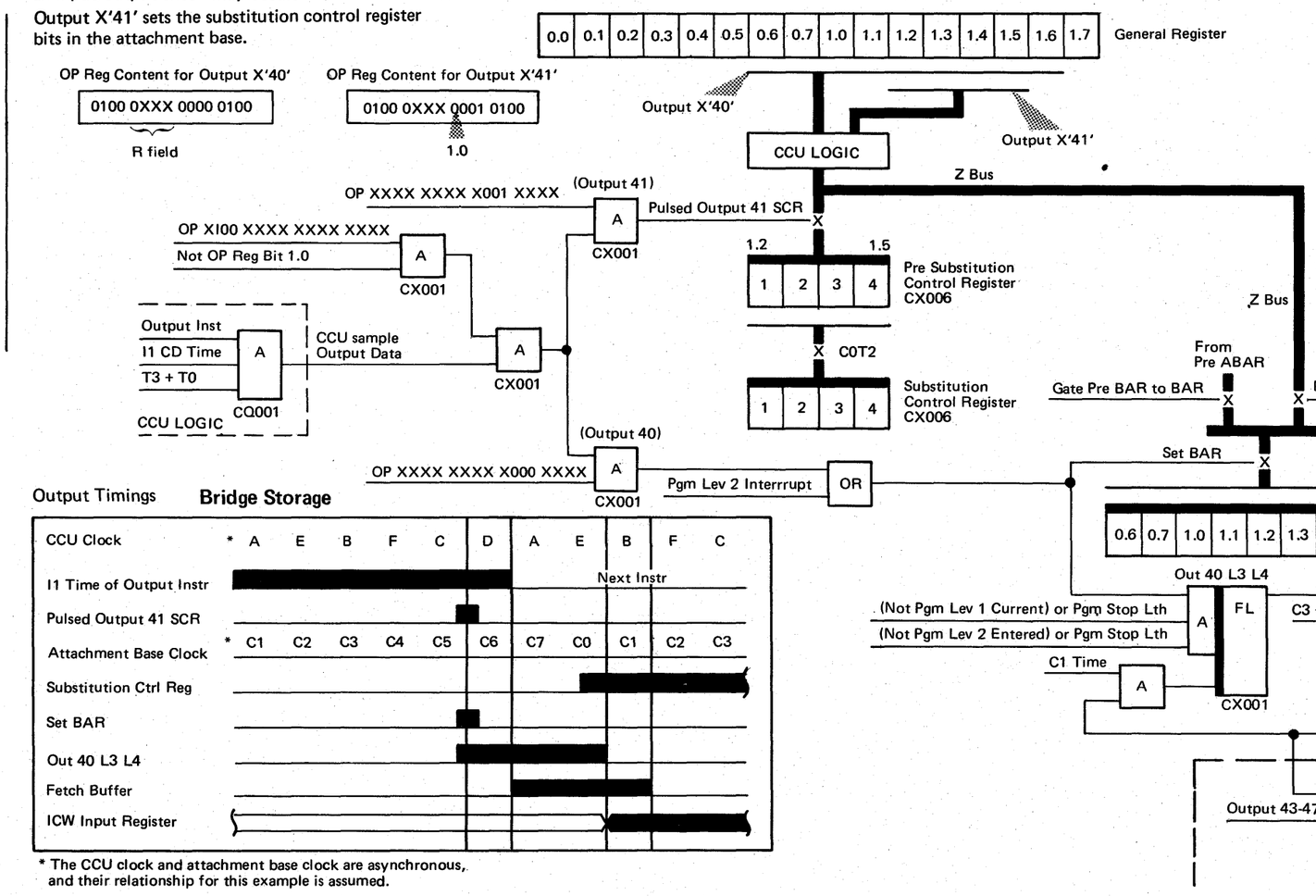
The control program must execute Output X'40' to initialize ABAR with an interface address associated with an installed type 2 scanner after the 3705 is powered on and before other inputs and outputs are issued to the scanner. Otherwise, an input/output check may occur.

Output X'41' sets the substitution control register bits in the attachment base.

General Register (R)	Output X'40'
0.0 – 0.5	*
0.6 – 0.7	Interface Address Bit 0 – Bit 1 ▸ Scanner: 00 = 1, 01 = 2, 10 = 3, 11 = 4
1.0 – 1.2	Bit 2 – Bit 4 ▸ LIB: 010 = LIB 1, 011 = LIB 2, 100 = LIB 3, 101 = LIB 4, 110 = LIB 5, 111 = LIB 6
1.3 – 1.6	Bit 5 – Bit 8 ▸ Line: 0 - F (hex)
1.7	*

*Bit Position Unused

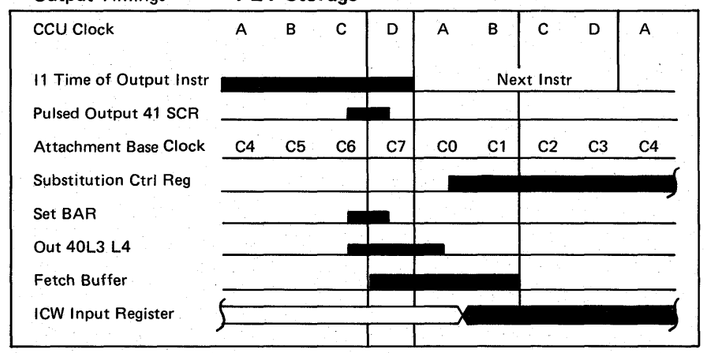
General Register (R)	Output X'41'
0.0 – 1.1	*
1.2 – 1.5	Substitution Ctrl Reg Bit 1, Bit 2, Bit 3, Bit 4
1.6 – 1.7	*



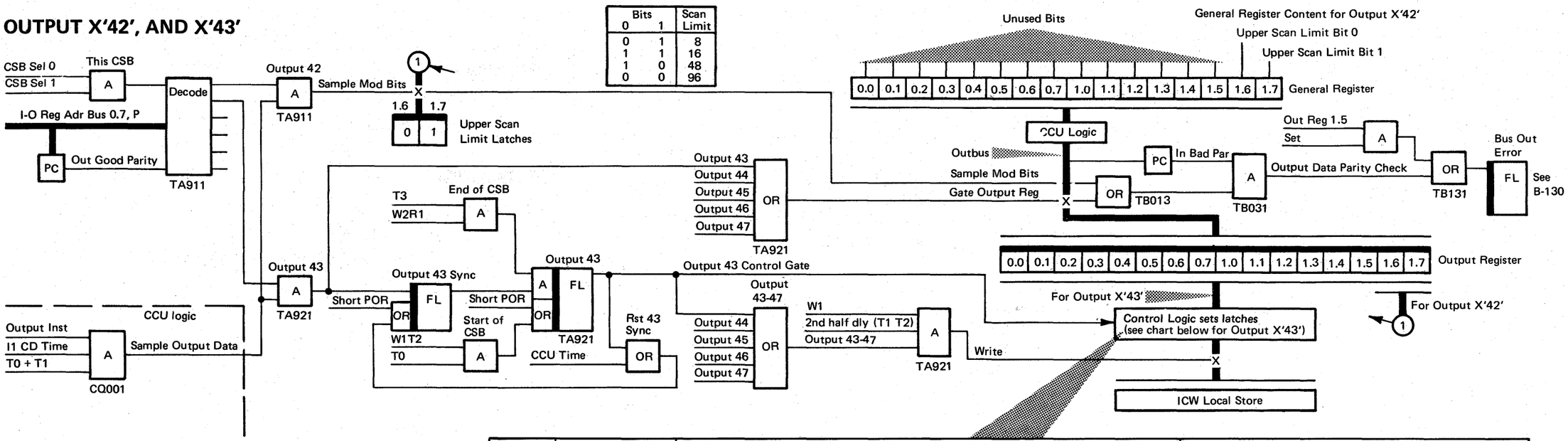
Output Timings **Bridge Storage**

* The CCU clock and attachment base clock are asynchronous, and their relationship for this example is assumed.

Output Timings **FET Storage**



OUTPUT X'42', AND X'43'



Output Reg Pos	Position Name	Set Function (0.0 = 1)	Reset Function (0.1= 1)
0.0	Set Function	A 1 causes the set function for output positions 0.2 through 1.6 when the corresponding bit is 1. This bit should not be 1 if 0.1 is 1.	Must be a 0 if the reset function is on (bit 0.1 = 1).
0.1	Reset Function	A 1 causes the reset function for output positions 0.2 through 1.6 when the corresponding bit is 1. This bit should not be 1 if 0.0 is 1.	Must be a 0 if the set function is on (bit 0.0 = 1).
0.2	Display Request	A 1 sets ICW bit 38. A 0 does not change ICW bit 38.	A 1 resets the ICW bit 38. A 0—no change.
0.3 | 0.6	Not used	No effect.	No effect.
0.7	Disable LIB pos 1	A 1 disables LIB 1. To do this, the scanner: ● Forces 'control out A' and 'control in A'. } This resets the line/autocall ● Forces 'control out B' and 'control in C'. } interface latches in all line ● Holds CSB data out lines 1-7 (IF 1 and 2) to 0. } sets when LIB 1 IF 1 is selected ● Resets PCF 0-3 to X'0' (NO-op). ● Inhibits 'CSB wants a priority register'. ● Resets ICW bit 41 (L2 interrupt pending). ● Inhibits the set of the 'work register error' latch in the check register. ● Forces 'write' at W2 (T3 + T0) to write into ICW local store. ● Masks BCC 1-6 errors from setting corresponding check register latches. A 0 has no effect.	A 1 *enables* LIB 1. A 0 has no effect.
1.0	Disable LIB pos 2	Same as 0.7 for LIB 2.	Same as 0.7 for LIB 2.
1.1	Disable LIB pos 3	Same as 0.7 for LIB 3.	Same as 0.7 for LIB 3.
1.2	Disable LIB pos 4	Same as 0.7 for LIB 4.	Same as 0.7 for LIB 4.
1.3	Disable LIB pos 5	Same as 0.7 for LIB 5.	Same as 0.7 for LIB 5.
1.4	Disable LIB pos 6	Same as 0.7 for LIB 6.	Same as 0.7 for LIB 6.
1.5	Type 2 Scanner N L1 Request	A 1 sets all 12 latches in the check register and causes a level 1 interrupt. A 0 has no effect.	A 1 resets the check register latches and the level 1 interrupt. A 0 has no effect.
1.6	Disable Interrupt Requests	A 1: ● Sets the 'CSB disable' latch that forces the same disable actions as described in 0.7 for all LIBS. ● Resets the upper scan limits. ● Resets the display request bit (ICW bit 38). ● Masks the setting of BCC 1-6 latches in the check register. ● Inhibits the setting of 'line sel error', 'in reg', 'work reg error', 'avail error', and 'BAR error' latches in the check register. Note: Output X'43' can still set the 'line sel error' latch. A 0 has no effect.	A 1 resets the 'CSB disable' latch to *enable the scanner.* A 0 has no effect. Note: The 'CSB disable' latch may also be set during a power on, during IPL 1, or by a reset switch operation. The program *must* reset this latch in each scanner before the scanner can be initialized.
1.7	Not Used	No effect.	No effect

Output X'42' sets the upper scan limit in the selected scanner. The interface address in the attachment buffer address register selects the scanner.

Output X'43' is executed to set or reset various control functions in a type 2 scanner. The interface address in the attachment buffer address register selects the scanner. When Output X'43' is executed, the bit configuration in the general register specified by the R field determines which control functions are set or reset.

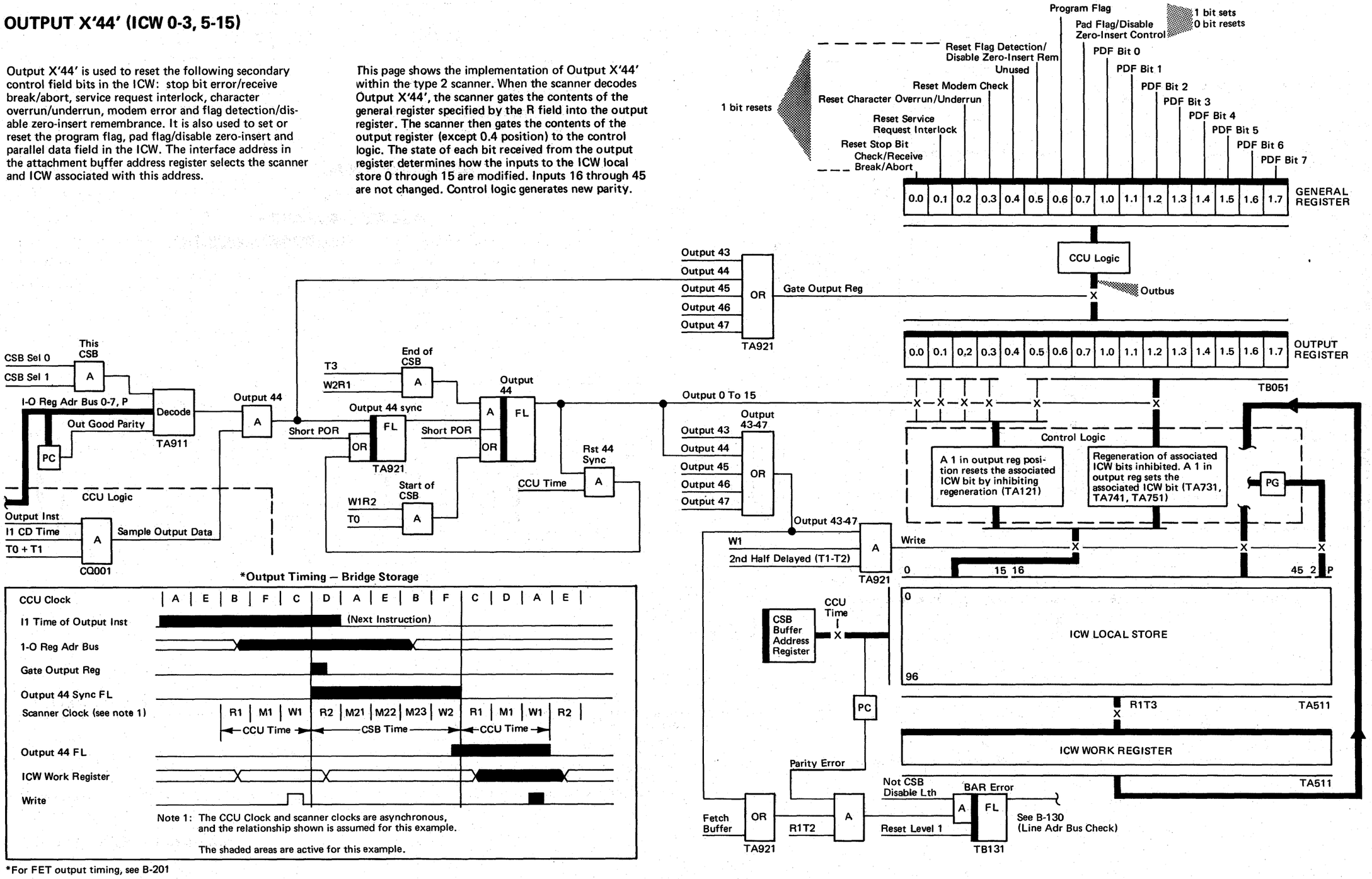
Selective LIB reset is caused by the set function. The scanner sets the 'mask LIB X errors' latch that causes the functions specified in the disable LIB 1 row. The scanner resets each line at that line's bit service request. The reset continues until the 'mask LIB X errors' latch is reset by the reset function (0.1 = 1 and a 1 in the associated disable LIB position) leaving LIB X *enabled.*

A minimum of one scan period (153.6 microseconds) is required between the time the 'CBS disable' latch is turned on to cause a reset (1.6 = 1 when 0.0 = 1), and when the 'CSB disable' latch is turned off to end the reset (1.6 = 1 when 0.1 = 1). The scanner is *enabled* when the 'CSB disable' latch is off.

OUTPUT X'44' (ICW 0-3, 5-15)

Output X'44' is used to reset the following secondary control field bits in the ICW: stop bit error/receive break/abort, service request interlock, character overrun/underrun, modem error and flag detection/disable zero-insert remembrance. It is also used to set or reset the program flag, pad flag/disable zero-insert and parallel data field in the ICW. The interface address in the attachment buffer address register selects the scanner and ICW associated with this address.

This page shows the implementation of Output X'44' within the type 2 scanner. When the scanner decodes Output X'44', the scanner gates the contents of the general register specified by the R field into the output register. The scanner then gates the contents of the output register (except 0.4 position) to the control logic. The state of each bit received from the output register determines how the inputs to the ICW local store 0 through 15 are modified. Inputs 16 through 45 are not changed. Control logic generates new parity.



*Output Timing — Bridge Storage

Note 1: The CCU Clock and scanner clocks are asynchronous, and the relationship shown is assumed for this example.

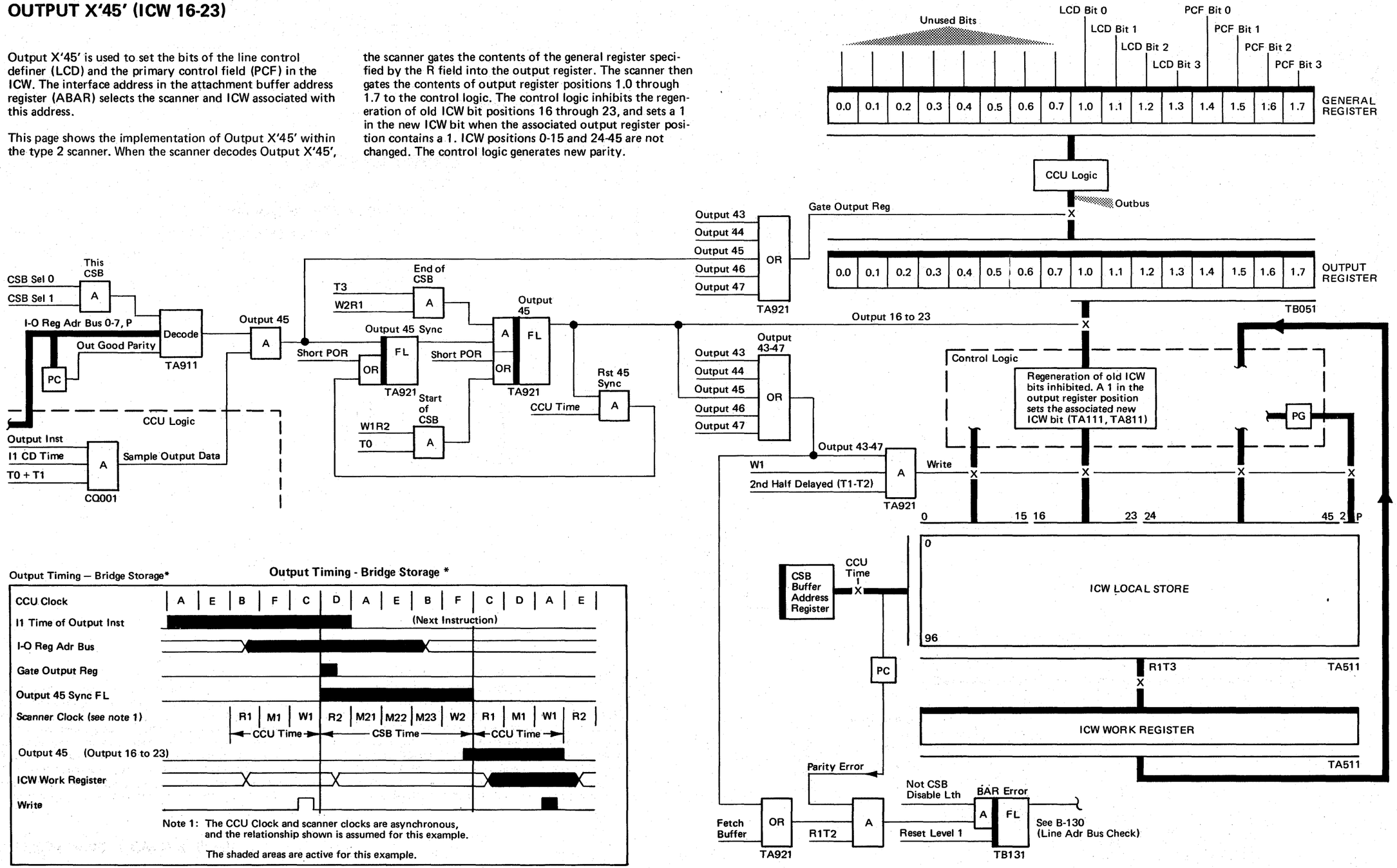
The shaded areas are active for this example.

*For FET output timing, see B-201

OUTPUT X'45' (ICW 16-23)

Output X'45' is used to set the bits of the line control definer (LCD) and the primary control field (PCF) in the ICW. The interface address in the attachment buffer address register (ABAR) selects the scanner and ICW associated with this address.

This page shows the implementation of Output X'45' within the type 2 scanner. When the scanner decodes Output X'45', the scanner gates the contents of the general register specified by the R field into the output register. The scanner then gates the contents of output register positions 1.0 through 1.7 to the control logic. The control logic inhibits the regeneration of old ICW bit positions 16 through 23, and sets a 1 in the new ICW bit when the associated output register position contains a 1. ICW positions 0-15 and 24-45 are not changed. The control logic generates new parity.



Output Timing — Bridge Storage*

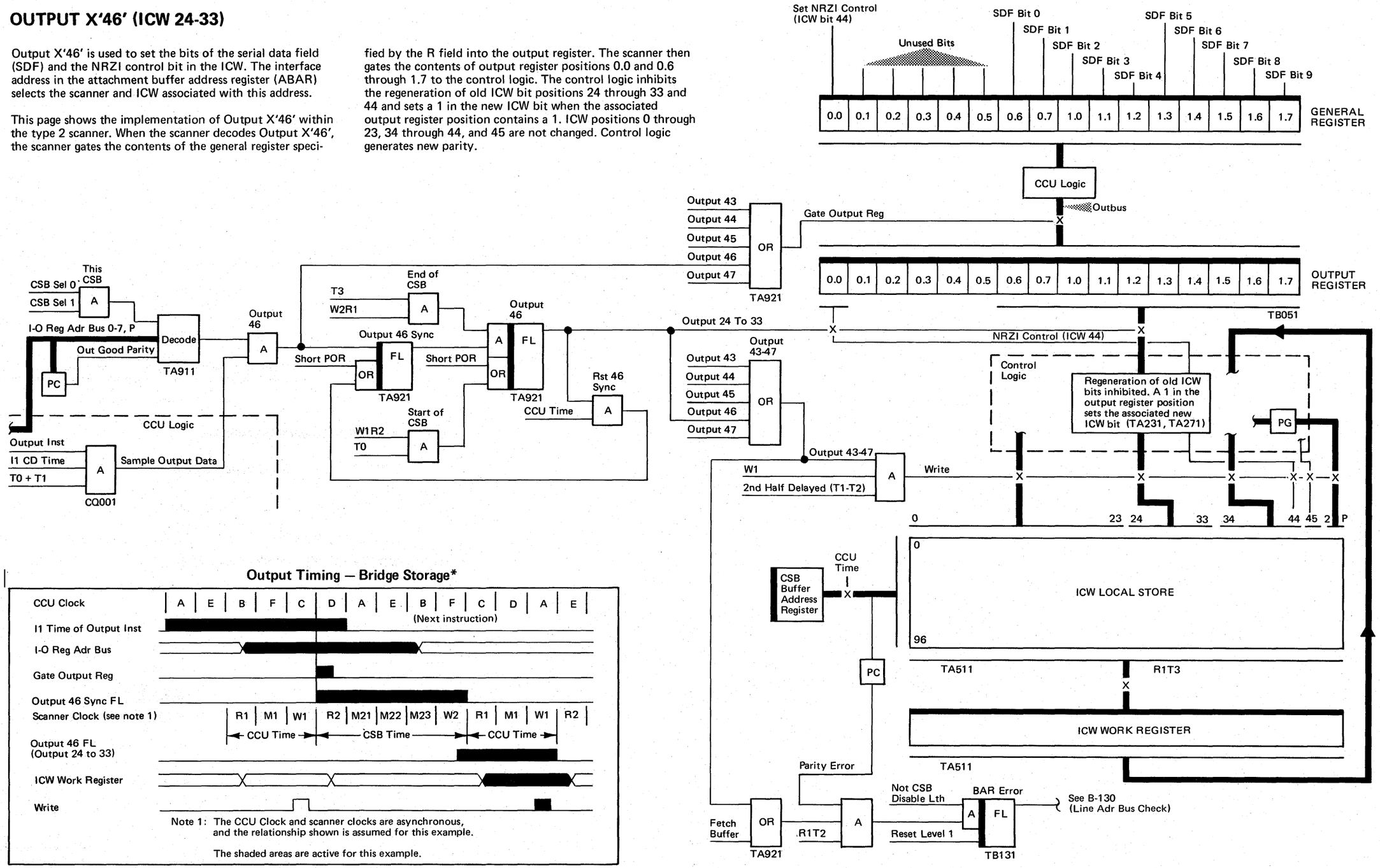
Output Timing - Bridge Storage *

*For FET output timing, see B-201

OUTPUT X'46' (ICW 24-33)

Output X'46' is used to set the bits of the serial data field (SDF) and the NRZI control bit in the ICW. The interface address in the attachment buffer address register (ABAR) selects the scanner and ICW associated with this address.

This page shows the implementation of Output X'46' within the type 2 scanner. When the scanner decodes Output X'46', the scanner gates the contents of the general register specified by the R field into the output register. The scanner then gates the contents of output register positions 0.0 and 0.6 through 1.7 to the control logic. The control logic inhibits the regeneration of old ICW bit positions 24 through 33 and 44 and sets a 1 in the new ICW bit when the associated output register position contains a 1. ICW positions 0 through 23, 34 through 44, and 45 are not changed. Control logic generates new parity.



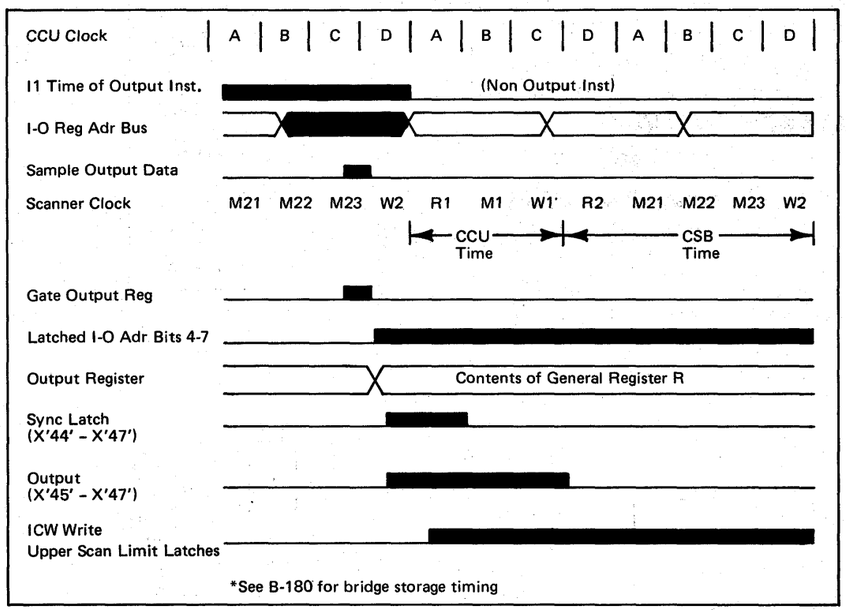
Output Timing — Bridge Storage*

*For FET output timing, see B-201.

FET STORAGE TIMING
OUTPUT X'44', X'45', X'46', AND X'47'

FET storage timings for Output instructions X'44' through X'47' are shown on this page. For bridge storage timing, refer to the description of each output instruction.

Output Timings—FET Storage*



*See B-180 for bridge storage timing

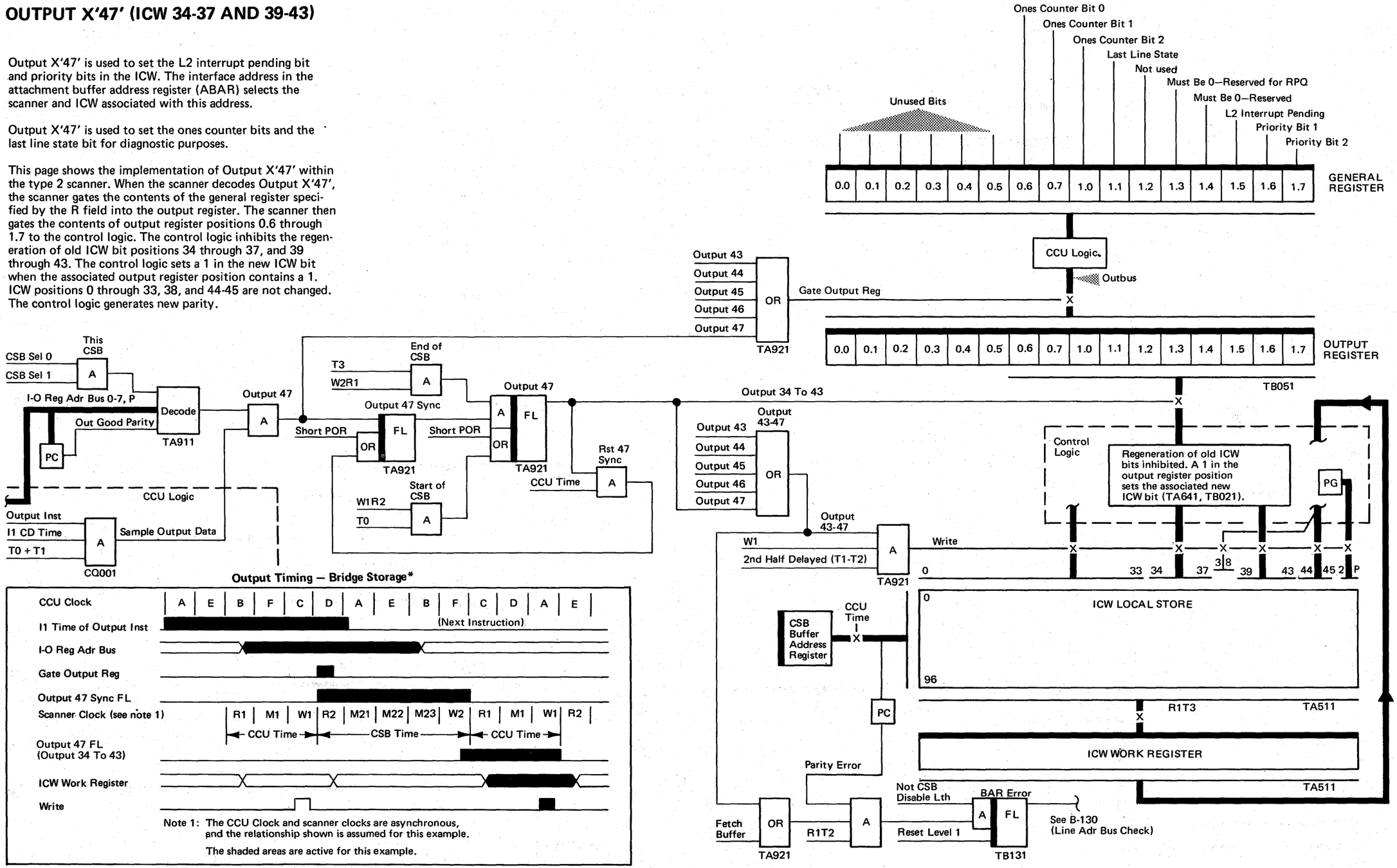
*The scanner sets the sync latch whenever the scanner decodes an Output X'41' thru X'4F' instruction. When set, the sync latch allows the scanner to execute the Output X'4X' instruction the next CCU time.

OUTPUT X'47' (ICW 34-37 AND 39-43)

Output X'47' is used to set the L2 interrupt pending bit and priority bits in the ICW. The interface address in the attachment buffer address register (ABAR) selects the scanner and ICW associated with this address.

Output X'47' is used to set the ones counter bits and the last line state bit for diagnostic purposes.

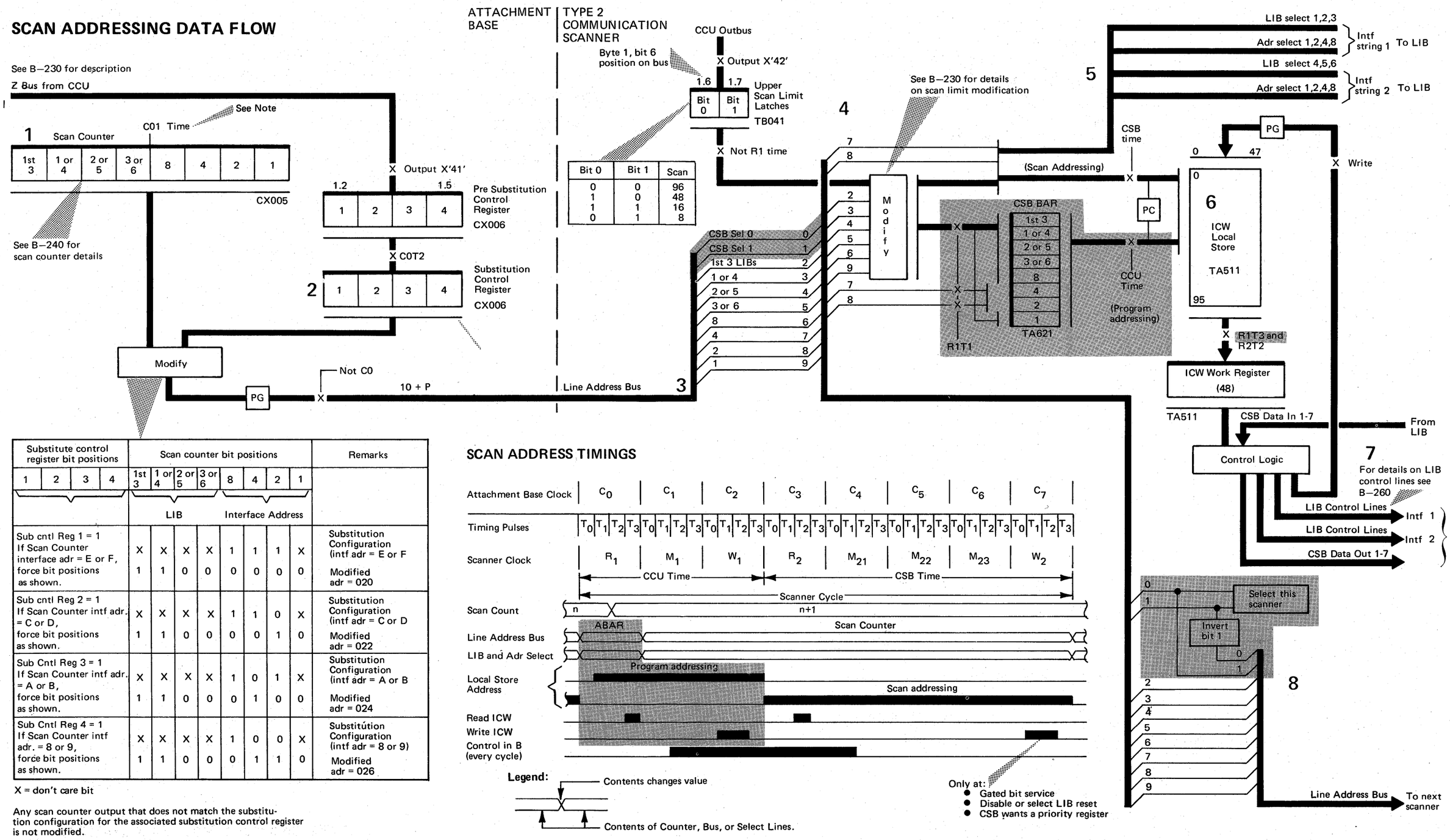
This page shows the implementation of Output X'47' within the type 2 scanner. When the scanner decodes Output X'47', the scanner gates the contents of the general register specified by the R field into the output register. The scanner then gates the contents of output register positions 0.6 through 1.7 to the control logic. The control logic inhibits the regeneration of old ICW bit positions 34 through 37, and 39 through 43. The control logic sets a 1 in the new ICW bit when the associated output register position contains a 1. ICW positions 0 through 33, 38, and 44-45 are not changed. The control logic generates new parity.



Output Timing — Bridge Storage*

*For FET output timing, see B-201.

SCAN ADDRESSING DATA FLOW



Substitute control register bit positions				Scan counter bit positions								Remarks
1	2	3	4	1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1	
				LIB				Interface Address				
Sub cntl Reg 1 = 1 If Scan Counter interface adr = E or F, force bit positions as shown.				X	X	X	X	1	1	1	X	Substitution Configuration (intf adr = E or F
				1	1	0	0	0	0	0	0	Modified adr = 020
Sub cntl Reg 2 = 1 If Scan Counter intf adr. = C or D, force bit positions as shown.				X	X	X	X	1	1	0	X	Substitution Configuration (intf adr = C or D
				1	1	0	0	0	0	1	0	Modified adr = 022
Sub Cntl Reg 3 = 1 If Scan Counter intf adr. = A or B, force bit positions as shown.				X	X	X	X	1	0	1	X	Substitution Configuration (intf adr = A or B
				1	1	0	0	0	1	0	0	Modified adr = 024
Sub Cntl Reg 4 = 1 If Scan Counter intf adr. = 8 or 9, force bit positions as shown.				X	X	X	X	1	0	0	X	Substitution Configuration (intf adr = 8 or 9)
				1	1	0	0	0	1	1	0	Modified adr = 026

X = don't care bit

Any scan counter output that does not match the substitution configuration for the associated substitution control register is not modified.

Note: For 1.2 microsecond cycle times (3705-1), C01 steps every 1.6 microseconds; for 1.0 microsecond cycle times (3705-II Models E-H), C01 steps every 2.0 microseconds; and for 900 nanosecond cycle times (3705-II Models J-L) C01 steps every 1.8 microseconds.

SCAN ADDRESS TIMINGS

SCAN ADDRESSING

Description for B-220. The numbers refer to corresponding numbers on the data flow.

1 Scan Counter

The scan counter runs continuously, stepping through 96 different states. See B-240 for details on the scan counter positions and sequence of interface address outputs.

If the scan counter output is not modified, each type 2 scanner scans 96 different interface addresses in a period of 153.6 microseconds. Without modification, the scanner can not handle line speeds higher than 4,800 bps without the possibility of undetected bit overrun/underrun conditions.

Two modifications can be made to the scan counter output to allow the scanner to handle line speeds of up to 56,000 bps. These modifications are made in conjunction with the substitution control register and the upper scan limit latches.

2 Address Substitution

The bit configuration in the substitution control register determines how the scan counter output is modified. The chart on B-220 shows which scan counter bit positions are modified for each substitution control register position. This modification causes certain fixed interface addresses assigned to line interface base (LIB) position 1 to be substituted on the line address bus for certain normal scan counter output states. When operating in this manner, *all* type 2 scanners are forced to scan the fixed address, or addresses, with an effective scan period of 12.8 microseconds. This is because address substitution occurs every eighth time the scan counter changes state (see B-240 for the scan counter sequence). This allows the fixed address, or addresses, in each scanner to handle line speeds up to 56,000 bps, independent of the state of the upper scan limit latches in the scanner.

The following table shows which addresses are substituted, and which addresses are not scanned as a result of that substitution when the different substitution control register bits are on.

Substitution Ctrl Reg Bit	Fixed Address Substituted In Each Type 2 Scanner If substitution Ctrl Reg Bit is ON	Addresses Not Scanned In Each Type 2 Scanner If Substitution Ctrl Reg Bit is ON
1	Adr 0 in LIB position 1	Adr E and F in LIB positions 1-6
2	Adr 2 in LIB position 1	Adr C and D in LIB positions 1-6
3	Adr 4 in LIB position 1	Adr A and B in LIB positions 1-6
4	Adr 6 in LIB position 1	Adr 8 and 9 in LIB positions 1-6

3 Line Address Bus

Ten address bits plus a parity bit are on the line address bus, but for scan addressing, CSB sel 0 and CSB sel 1 are ignored. Parity is generated over the eight bit address on line address bus positions 2-9.

4 Upper Scan Limit Modification

Each type 2 scanner has two upper scan limit latches. Each scanner modifies the address on the line address bus according to the state of its upper scan limit latches. See the chart to the right for the actual line address bit positions modified by the four states of the upper scan limit latches. The line address bus output may be modified in some form as shown in the chart. A zero in the '1st 3' position of the ICW local store address selects ICWs associated with LIBs 1, 2, 3 and also combines with a one in the '1 or 4', '2 or 5', or '3 or 6' positions for LIB select 1, 2, or 3.

If the scan counter output is not modified by address substitution, the four states of the upper scan limit latches create the following effective scan periods:

3705-I

Upper Scan Limit State	Actual Scan Counter Period	Number of Interfaces actually scanned by Scanner	Number of times each Interface is scanned in Scan Counter Period	1.2 usec Cycle Time Effective Scan Period
00	153.6 usec	96	1	*153.6 usec
10	153.6 usec	48	2	76.8 usec
11	153.6 usec	16	6	25.6 usec
01	153.6 usec	8	12	12.8 usec

3705-II

Upper Scan Limit State	Actual Scan Counter Period	Number of Interfaces actually scanned by Scanner	Number of times each Interface is scanned in Scan Counter Period	1.0 usec Cycle Time Effective Scan Period	0.9 usec Cycle Time Effective Scan Period
00	192 usec	96	1	*192 usec	172.8
10	192 usec	48	2	96 usec	86.4
11	192 usec	16	6	32 usec	28.8
01	192 usec	8	12	16 usec	14.4

*The effective scan period is for 96 addresses since the type 2 attachment base step through 96 addresses.

5 LIB Select and Address Select

Every 1.6 microseconds, the scanner selects a line interface, or auto call interface, by sending the modified line address bus output to the LIB and interface by means of the LIB select and address select lines. LIBS 1,2, and 3 are on interface string 1, and LIBs 4, 5, and 6 are on interface string 2.

6 ICW Local Store

Each type 2 scanner contains a local store array that contains 96 addressable interface control words (ICW). Each ICW contains 46 bits plus 2 parity bits. A distinct ICW is associated with each line interface, or autocall unit interface, attached to the scanner through a LIB. See chart on B-250 for the relationships between the modified line address bus output, ICW array selection, and interface address selected for each scanner.

See B-220 for scan address timings to read out and write into the ICW associated with the selected interface address. CSB time gates the address to the local store, and the contents of the selected ICW are placed in the ICW work register at R2T2 time. The scanner control logic examines the contents of this ICW and the 'control in B' status.

When a hardware interface bit service or a program service level 2 interrupt is required, the ICW contents are modified and written back into the local store at W2T1T2 time. If the ICW contents are not modified, they normally are not written into the local store array because the original contents are not destroyed during read-out.

7 LIB Control

The scanner control logic sends a 'control in B' signal to the selected interface which gates the status of certain data communications equipment lines and certain latches in the interface hardware back to the scanner. See B-260 for details.

8 Line Address Bus to Next Scanner

Line address bus positions 2-9 pass directly to the next scanner. Position 0 reverses position with the inverted position 1; however, these two positions are not used during scan addressing.

UPPER SCAN LIMIT MODIFICATION OF LINE ADDRESS BUS

Upper Scan Limit	Position	Address Bit Positions: 1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1	Interface Lines Selected	Modification Performed
00 (96 lines)	Line adr bus	1	↓	↓	↓	↓	↓	↓	↓	LIB sel x-intf 1	Invert '1st 3' bit
	Local store adr	0	↓	↓	↓	↓	↓	↓	↓	Adr sel y-intf 1 & 2	
	Line addr bus	0	↓	↓	↓	↓	↓	↓	↓	LIB sel x-intf 2	Invert '1st 3' bit
	Local store adr	1	↓	↓	↓	↓	↓	↓	↓	Adr sel y-intf 1 & 2	
10 (48 lines)	Line adr bus	X	↓	↓	↓	↓	↓	↓	↓	LIB sel x-intf 1	Force '1st 3' bit to 0
	Local store adr	0	↓	↓	↓	↓	↓	↓	↓	Adr sel y-intf 1 & 2	
11 (16 lines)	Line adr bus	X	X	X	X	↓	↓	↓	↓	LIB sel x-intf 1	Force '1 or 4' bit to 1 and '1st 3', '2 or 5', '3 or 6' to 0.
	Local store adr	0	1	0	0	↓	↓	↓	↓	Adr sel y-intf 1 & 2	
01 (8 lines)	Line adr bus	X	X	X	X	1	↓	↓	X	LIB sel x-intf 1	If bit 8 = 1, force it to 0 and force bit 1 to 1. If bit 8 = 0, do not modify it, but force bit 1 to 0. In both cases, force bit '1 or 4' to 1, and bits '1st 3', '2 or 5', or '3 or 6' to 0.
	Local store adr	0	1	0	0	0	↓	↓	1	Adr sel y-intf 1 & 2	
	Line adr bus	X	X	X	X	0	↓	↓	X	LIB sel x-intf 1	
	Local store adr	0	1	0	0	0	↓	↓	0	Adr sel y-intf 1 & 2	

↓ indicates no modification

X indicates don't care

Upper scan limit = 01 forces this interface line selection sequence if address substitution has not modified the scan counter sequence.

Modified Line Adr Bus Position 8	4	2	1	Line selected within LIB 1
0	0	0	0	0
0	0	1	0	2
0	1	0	0	4
0	1	1	0	6
0	0	0	1	1
0	0	1	1	3
0	1	0	1	5
0	1	1	1	7

SCAN COUNTER

- Stepped every 1.6 microseconds (see Note) at C01 time (see B-220).

  Note: Every 1.6 microseconds for the 3705-I only. For the 3705-II, the scan counter is stepped every 2.0 microseconds if the cycle time is 1.0 microseconds and every 1.8 microseconds if the cycle time is 900 nanoseconds.

- There are 96 different states—one for each interface address in the communication scanner.

- The relationship of the output state of the scan counter with respect to the line address bus bit positions is shown in the chart.

  Position '1st 3' — A one indicates LIB 1,2 or 3 is selected.

  A zero indicates LIB 4,5 or 6 is selected.

  Position '1 or 4' — A one selects LIB 1 if position '1st 3' is a one, or LIB 4 if position '1st 3' is a zero.

  Position '2 or 5' — A one selects LIB 2 if position '1st 3' is a one, or LIB 5 if position '1st 3' is a zero.

  Position '3 or 6' — A one selects LIB 3 if position '1st 3' is a one, or LIB 6 if position '1st 3' is a zero.

  Only one position, from among '1 or 4', '2 or 5', and '3 or 6', can be active at a time.

  These four positions define the LIB to be selected.

  Positions 8,4,2,1 form the hex representation for the line address within the selected LIB.

- The scan counter generates interface addresses in the sequence shown in the chart. The LIBs are selected in sequence—however, the even interface addresses within each LIB are generated consecutively, followed by the odd interface addresses.

SEQUENCE OF INTERFACE ADDRESSES GENERATED BY SCAN COUNTER

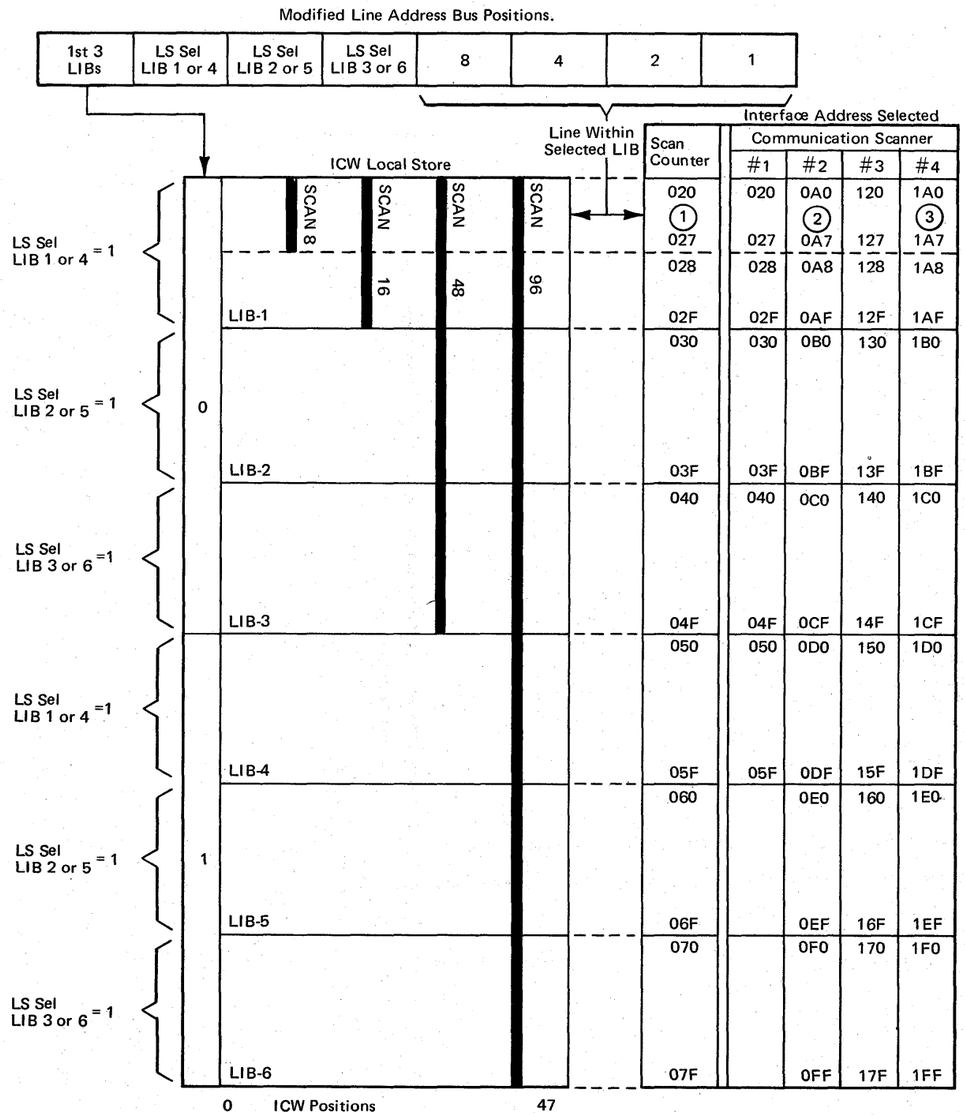
Interface Address (Hex)	Scan Counter Bit Positions								LIB Interface String	LIB Selected	Interface Line Selected
	1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1			
	← LIB Address →				← Interface line within selected LIB →						
020	1	1	0	0	0	0	0	0	1	1	0
022	1	1	0	0	0	0	1	0			2
024	1	1	0	0	0	1	0	0			4
026	1	1	0	0	0	1	1	0			6
028	1	1	0	0	1	0	0	0			8
02A	1	1	0	0	1	0	1	0			A
02C	1	1	0	0	1	1	0	0			C
02E	1	1	0	0	1	1	1	0			E
021	1	1	0	0	0	0	0	1			1
023	1	1	0	0	0	0	1	1			3
025	1	1	0	0	0	1	0	1			5
027	1	1	0	0	0	1	1	1			7
029	1	1	0	0	1	0	0	1			9
02B	1	1	0	0	1	0	1	1			B
02D	1	1	0	0	1	1	0	1			D
02F	1	1	0	0	1	1	1	1			F
030	1	0	1	0	0	0	0	0			0
↓	↓	↓	↓	↓	Even lines then odd lines						
03F	1	0	1	0	1	1	1	1			F
040	1	0	0	1	0	0	0	0			0
↓	↓	↓	↓	↓	Even lines then odd lines						
04F	1	0	0	1	1	1	1	1			F
050	0	1	0	0	0	0	0	0			0
↓	↓	↓	↓	↓	Even lines then odd lines						
05F	0	1	0	0	1	1	1	1			F
060	0	0	1	0	0	0	0	0			0
↓	↓	↓	↓	↓	Even lines then odd lines						
06F	0	0	1	0	1	1	1	1			F
070	0	0	0	1	0	0	0	0			0
↓	↓	↓	↓	↓	Even lines then odd lines						
07F	0	0	0	1	1	1	1	1			F

SCAN ADDRESSING EXAMPLES

Position	Address Positions: 1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1	Interface Lines Selected	ICW Local Store Adr Selected	Modification Performed
EXAMPLE 1: All Substitution Ctrl Registers = 0, Upper Scan Limit = 00 (96 lines), Scanner #1											
Scan Counter	1	1	0	0	0	1	1	1			See B-240
Line Address Bus	1	1	0	0	0	1	1	1			No Adr Substitution
Modified Local Store Adr	0	1	0	0	0	1	1	1	LIB sel 1-intf 1 Adr sel 7-intf 1 & 2	027 (1)	Upper Scan Limit
EXAMPLE 2: Substitution Ctrl Reg Bit 1 = 1, Upper Scan Limit = 11 (16 lines), Scanner #1											
Scan Counter	1	1	0	0	1	1	1	0			See B-240
Line Address Bus	1	1	0	0	0	0	0	0			Adr Substitution
Modified Local Store Adr	0	1	0	0	0	0	0	0	LIB sel 1-intf 1 Adr sel 0-intf 1 & 2	020	Upper Scan Limit
EXAMPLE 3: Substitution Ctrl Reg Bit 4 = 1, Upper Scan Limit = 00 (96 lines), Scanner #2											
Scan Counter	0	0	0	1	1	0	0	1			See B-240
Line Address Bus	1	1	0	0	0	1	1	0			Adr Substitution
Modified Local Store Adr	0	1	0	0	0	1	1	0	LIB sel 1-intf 1 Adr sel 6-intf 1 & 2	0A6 (2)	Upper Scan Limit
EXAMPLE 4: Substitution Ctrl Reg Bit 2 = 1, Upper Scan Limit = 01 (8 lines), Scanner #1											
Scan Counter	1	1	0	0	1	0	0	0			See B-240
Line Address Bus	1	1	0	0	1	0	0	0			No Adr Substitution
Modified Local Store Adr	0	1	0	0	0	0	0	1	LIB sel 1-intf 1 Adr sel 1-intf 1 & 2	021	Upper Scan Limit
EXAMPLE 5: Substitution Ctrl Reg Bit 3 = 1, Upper Scan Limit = 10 (48 lines), Scanner #3											
Scan Counter	0	1	0	0	1	1	1	0			See B-240
Line Address Bus	0	1	0	0	1	1	1	0			No Adr Substitution
Modified Local Store Adr	0	1	0	0	1	1	1	0	LIB sel 1-intf 1 Adr sel E-intf 1 & 2	12E	No Upper Scan Limit
EXAMPLE 6: All Substitution Ctrl Registers = 0, Upper Scan Limits = 01 (8 lines), Scanner #4											
Scan Counter	0	0	0	1	0	1	1	1			See B-240
Line Address Bus	0	0	0	1	0	1	1	1			No Adr Substitution
Modified Local Store Adr	0	1	0	0	0	1	1	0	LIB sel 1-intf 1 Adr sel 6-intf 1 & 2	1A6 (3)	Upper Scan Limit

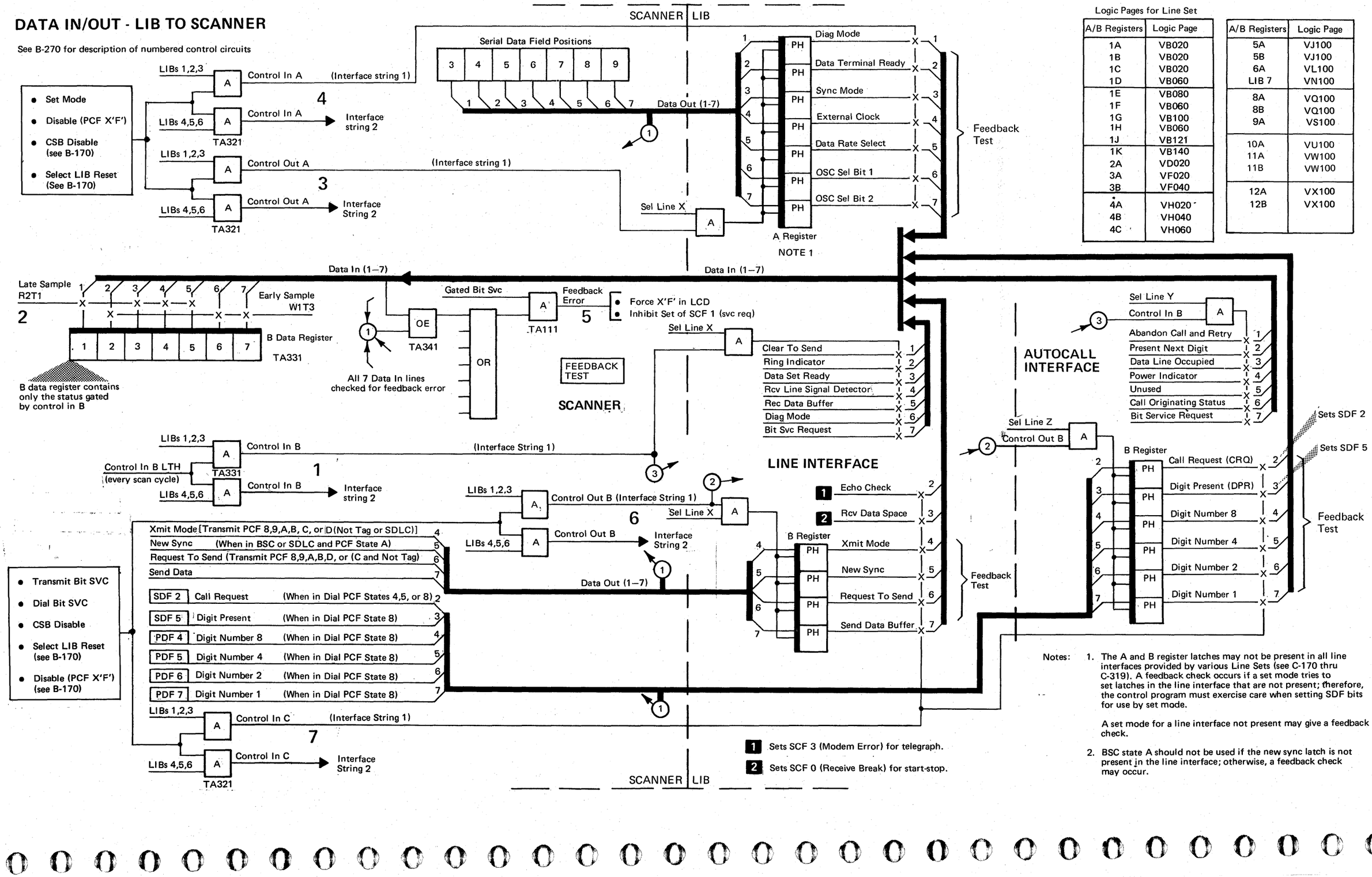
These addresses do not appear as such during scan addressing, but are seen in ABAR during a program level 2 interrupt as shown on B-330.

ICW LOCAL STORE/SELECTED INTERFACE ADDRESS RELATIONSHIP TO SCAN ADDRESSING



DATA IN/OUT - LIB TO SCANNER

See B-270 for description of numbered control circuits



Logic Pages for Line Set

A/B Registers	Logic Page
1A	VB020
1B	VB020
1C	VB020
1D	VB060
1E	VB080
1F	VB060
1G	VB100
1H	VB060
1J	VB121
1K	VB140
2A	VD020
3A	VF020
3B	VF040
4A	VH020
4B	VH040
4C	VH060

A/B Registers	Logic Page
5A	VJ100
5B	VJ100
6A	VL100
LIB 7	VN100
8A	VQ100
8B	VQ100
9A	VS100
10A	VU100
11A	VW100
11B	VW100
12A	VX100
12B	VX100

Notes:

1. The A and B register latches may not be present in all line interfaces provided by various Line Sets (see C-170 thru C-319). A feedback check occurs if a set mode tries to set latches in the line interface that are not present; therefore, the control program must exercise care when setting SDF bits for use by set mode.

   A set mode for a line interface not present may give a feedback check.

2. BSC state A should not be used if the new sync latch is not present in the line interface; otherwise, a feedback check may occur.

DATA IN/OUT LIB INTERFACE, PART 2

Description for B-260. The numbers refer to control circuits shown on B-260.

1 Every 1.6 (3705-I) microseconds during scan addressing, the type 2 scanner selects a line interface, or auto call interface, by sending that interface address to the LIB and interface over the 'LIB select' and 'address select' lines (See Note). The scanner sends a 'control in B' signal to the interface that gates the status of certain data communication equipment lines and certain latches in the interface hardware back to the scanner.

2 This status is stored in the B data register and is available to the control logic and the display register. See B-150 for the status bits buffered in the B data register.

3 PCF state X'1' (set mode) gates the set mode SDF bit configuration over the data out lines and gates this data into the 'A register' of the scanned interface by sending the 'control out A' signal. Bit service request is not required to set the 'A register'.

4 The scanner ensures the latches are set to the correct value by sending 'control in A' to the interface hardware which gates feedback signals (from those latches just set) over the data-in lines to the scanner.

5 At gated bit service, if any latch does not agree with the value to which it was to have been set, a feedback error results which sets the LCD field to hex 'F'. This temporarily suspends scanner-to-interface action for that line. Level-2 interrupts for the faulty interface are also suppressed except for set mode. These errors must be recognized by a periodic scan of the LCD fields for all interfaces. The 3705 interval timer is used to provide this periodic scan of the LCD fields. Line and autocall interface feedback error detection is at the interface level; but if failures are detected in a group of interfaces, the interface hardware, type 2 scanner hardware or program logic may be at fault.

6 With 'bit service' on, a transmit or autocall operation sends 'control out B' to the interface and control logic places the appropriate bits on the data out lines.

7 The 'control in C' signal, sent to the interface, causes a feedback test.

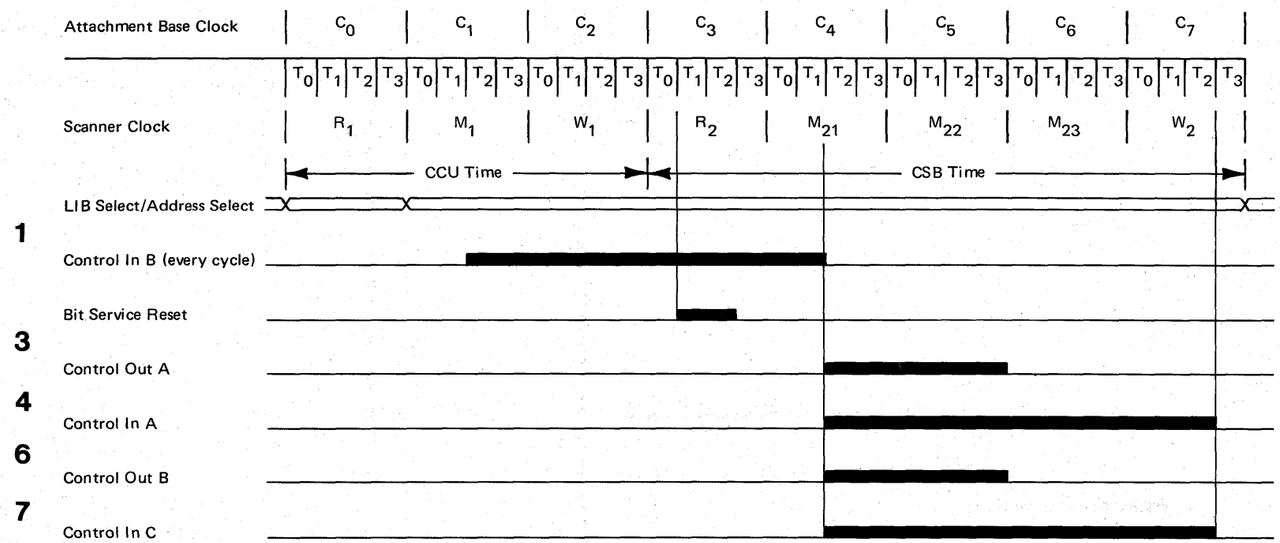
3 & 6 The CSB disable latch turns on by executing Output X'43' (1 in byte 0, bit 0 and 1 in byte 1, bit 6), by an IPL reset, by the control panel Reset pushbutton, or by power on/off reset. When the CSB disable latch is on, the data out lines are held off while 'control out A' and 'control out B' are sent to the interface to reset the hardware latches. A feedback test then occurs (See B-170).

3 With bit service on, a disable (PCF state F) sends 'control out A' and 'control out B', to the interface with data out lines held off to reset the control latches in the LIB. The fall of 'data terminal ready' signals the data communications equipment that the interface is disabled and for the data communications equipment to terminate that connection. A feedback test then occurs. (See B-460).

3 & 6 When Output X'43' is executed with the set function on (1 in 0.0) and any 'disable LIB position 1-6' on (1 in corresponding byte and bit position), the line 'select LIB reset' is active while scanning the interface/autocall lines on the disabled LIB. At this time the data out lines are held off while 'control out A' and 'control out B' are sent to the interface to reset the hardware latches. A feedback test then occurs. (See B-170).

- Two signals are sent from the type 2 scanner to the interface without any control signals to gate them. These are the 'reset bit service' and 'test data' lines.
  - The 'reset bit service' line resets the 'bit service' latch in the interface hardware on the cycle in which it is sensed. This notifies the interface hardware that the service request has just been honored. A feedback check then occurs.
  - When diagnostic wrap mode is used, the scanner places the transmitted data of the diagnostic transmit line in a 'test data' latch in the type 2 scanner hardware. The receive lines sample the state of this 'test data' latch and use it as received data.
- Bit Overrun Reset
  Grounded in the scanner
- LIB Active In
  Held at the down level in the scanner
- Auto Call Present
  Terminated in the scanner but not used.

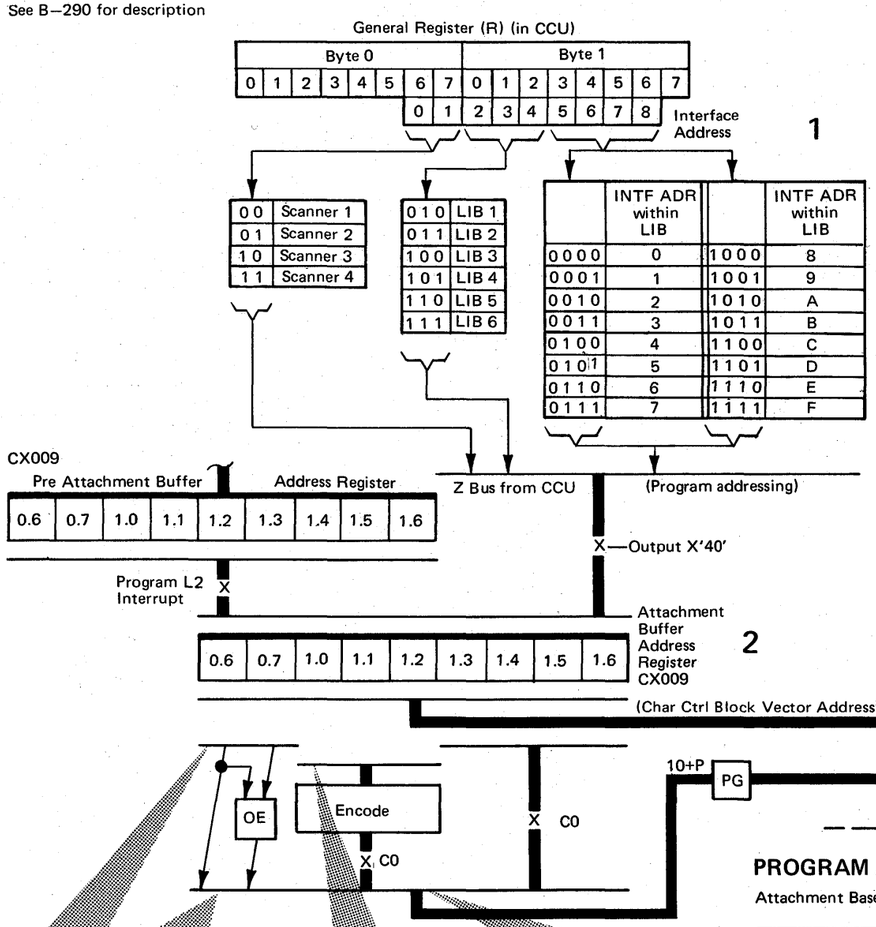
SCANNER INTERFACE TIMING TO LIBS



Note: For the 3705-II, every 2.0 microseconds if the cycle time is 1.0 microseconds and every 1.8 microseconds if the cycle time is 900 nanoseconds.

PROGRAM ADDRESSING DATA FLOW

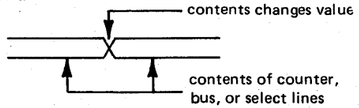
See B–290 for description



0.6	0.7	Line ADR 0	Line ADR 1	Select Scanner
0	0	0	0	1
0	1	0	1	2
1	0	1	1	3
1	1	1	0	4

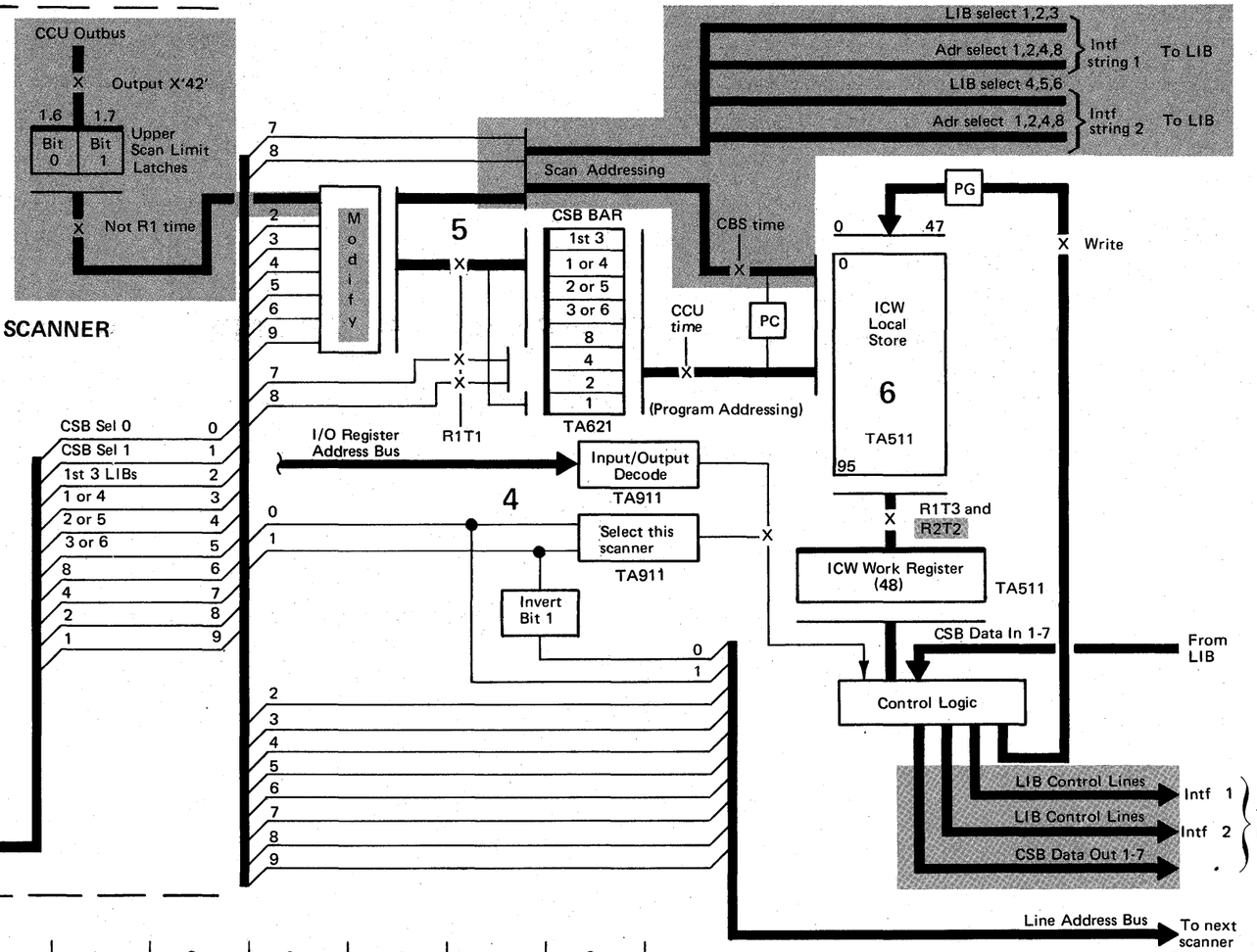
ABAR Positions 1.0 1.1 1.2	Significance At ABAR/Line Address Bus	1st 3	1 or 4	2 or 5	3 or 6
0 1 0	LIB 1	1	1	0	0
0 1 1	LIB 2	1	0	1	0
1 0 0	LIB 3	1	0	0	1
1 0 1	LIB 4	0	1	0	0
1 1 0	LIB 5	0	0	1	0
1 1 1	LIB 6	0	0	0	1

Legend:

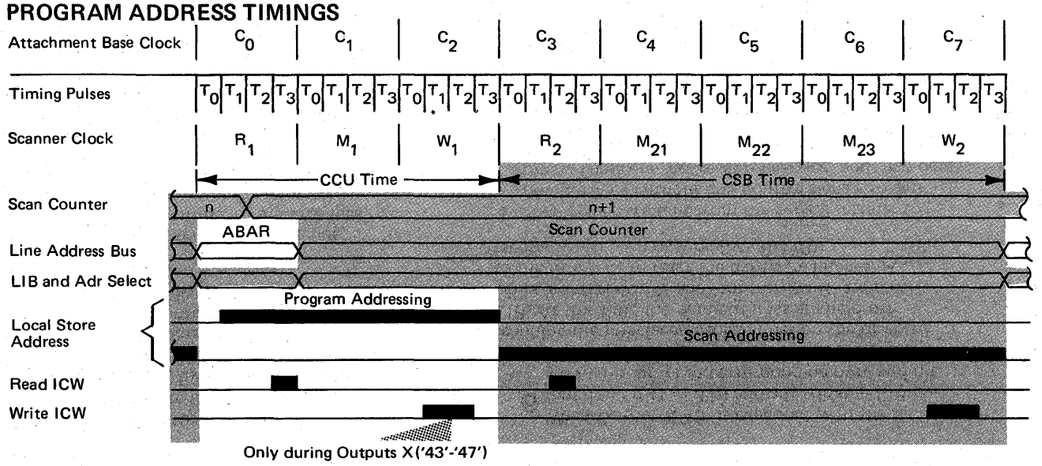


ATTACHMENT BASE

SCANNER



PROGRAM ADDRESS TIMINGS



PROGRAM ADDRESSING

Description for B-280. The numbers refer to corresponding numbers on the data flow.

The control program handles the service requirements of the line interfaces—one at a time. The control program does this by executing input and output instructions. Program addressing refers to the period of the scanner cycle during which the input and output instructions are implemented in the attachment base and scanners. This occurs during CCU time of the scanner cycle.

Before the program can examine or modify fields in an interface control word (ICW) associated with a particular interface, the address of that interface must be placed in the attachment buffer address register (ABAR) of the type 2 attachment base. Similarly, before the program can access certain registers in a particular type 2 scanner, or perform control functions in that scanner, the interface address in the ABAR must be one of those assigned to that scanner. Two distinct events cause the contents of the ABAR to change:

(1) When a program level 2 interrupt occurs, the ABAR contents are automatically set by the attachment base with the interface address from the highest priority register occupied. The interrupt program executes Input X'40' to determine the interface address in ABAR. The program can then examine and/or modify fields in the ICW associated with this interface.

(2) In program levels 1, 3, and 4, the program may have to examine certain registers in a specific scanner or perform miscellaneous control functions in that scanner. Furthermore, in program level 3 or 4, the program may need to access the ICW associated with a specific interface. By executing Output X'40' under such circumstances, the program can cause the ABAR to be set according to the interface address in the general register specified by R.

Note: To avoid conflicts with the automatic mechanism which sets ABAR when a program level 2 interrupt occurs, programs executing at program level 3 or 4 should mask program level 2 interrupts before executing Output X'40'. If more than one program level is likely to execute Output X'40', additional program interlocks should be established between those levels by the user.

The following numbered items pertain to the program addressing data flow on B-280.

1 Interface Addresses

The lines attached to the 3705 are assigned interface addresses at installation time. The interface address assigned to a given line is determined by the physical position of the line interface hardware in the LIB through which the line is attached. The control program identifies each line by means of the nine-position interface address. The nine bits define the scanner position, LIB position, and the line within the selected LIB as shown in the charts on B-280.

2 ABAR (Attachment Buffer Address Register)

ABAR buffers the nine interface address bits for program addressing all scanners.

3 Line Address Bus

Three ABAR positions (1.0-1.2) are encoded to four bits and then gated to the line address bus for 200 nanoseconds (C0 time). C0 time also gates ABAR positions 1.3-1.6 to the line address bus. ABAR positions 0.6-0.7 (interface address bits 0-1) are placed on the line address bus continuously. Since they can be changed by an Output X'40', or a program level 2 interrupt during the scanner cycle, they are not included in the line address bus parity.

4 Scanner Select

Line address bus positions 0-1 determine which scanner is selected. The selected scanner is the only scanner that decodes the input and output instructions and performs the required function. The accompanying diagram shows how the scanner select bits propagate from scanner to scanner, and the conditions under which a feedback error can occur during scanner selection.

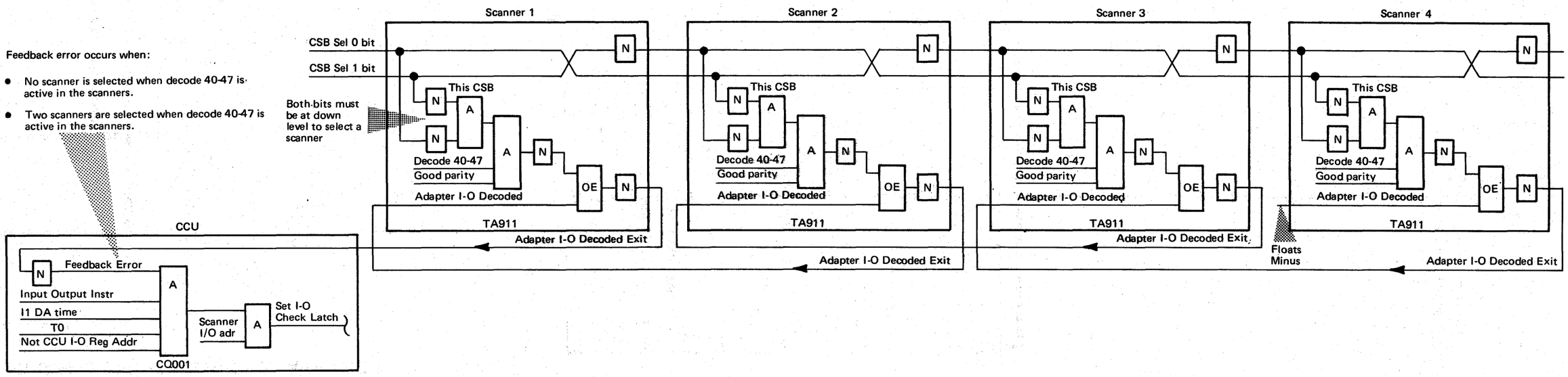
5 CSB BAR (Buffer Address Register)

The line address bus is gated into the CSB BAR at R1T1 time. The line address passes through the upper scan limit modify logic but the upper scan limit latch output is degated at R1 time, and no modification occurs.

6 ICW Local Store

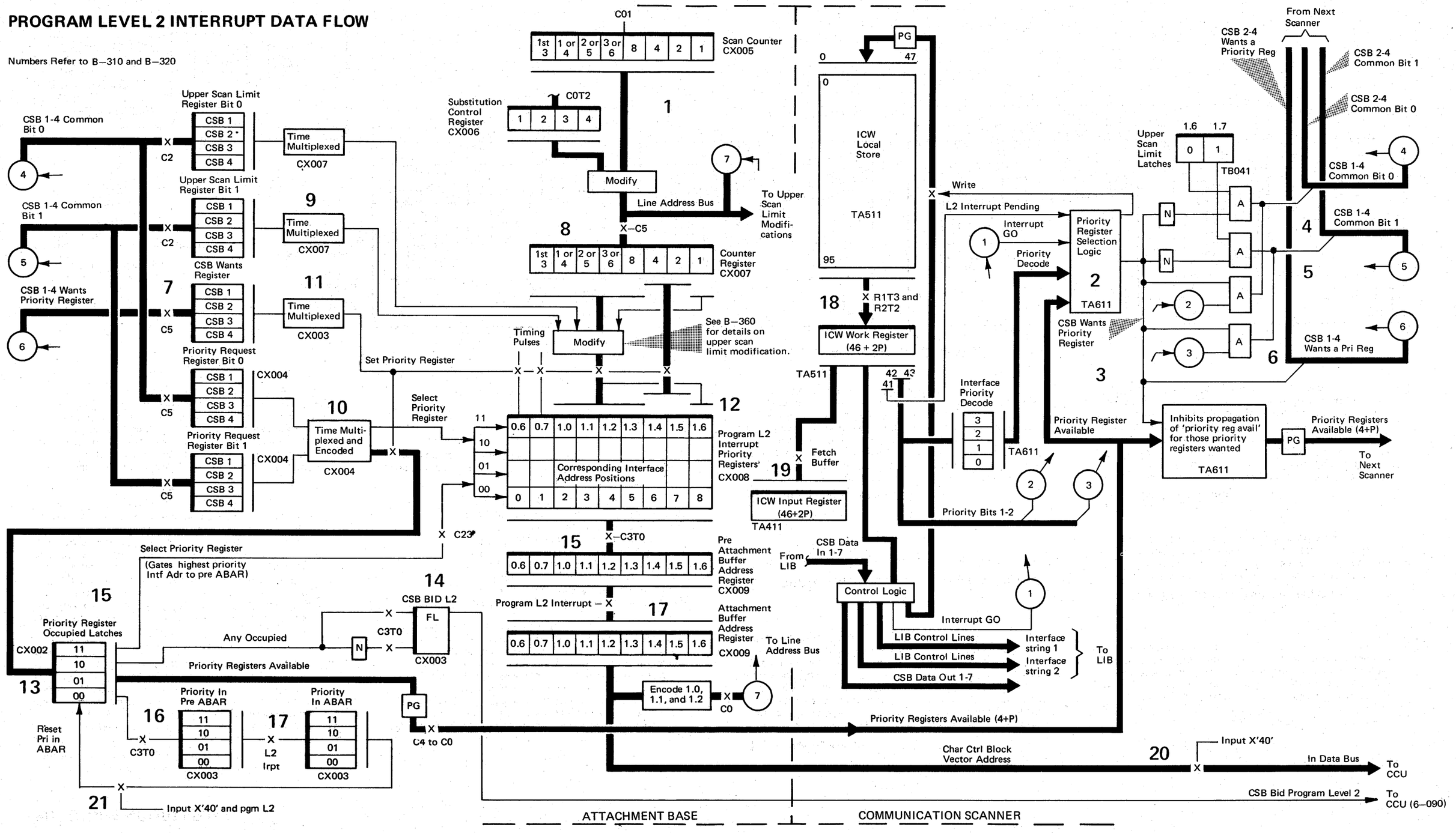
At CCU time, the line address in the CSB BAR selects the associated ICW from the ICW local store. The content of the ICW is read into the ICW work register at R1T3 time. All scanners are addressed and the contents of the selected ICW read out during CCU time, but only the selected scanner decodes the input and output instruction. New data is written into the ICW associated with the line address when OUTPUT X'43-47' instructions are decoded.

Scanner Selection And I/O Check Detection



PROGRAM LEVEL 2 INTERRUPT DATA FLOW

Numbers Refer to B–310 and B–320



PROGRAM LEVEL 2 INTERRUPT

Numbers refer to B–300

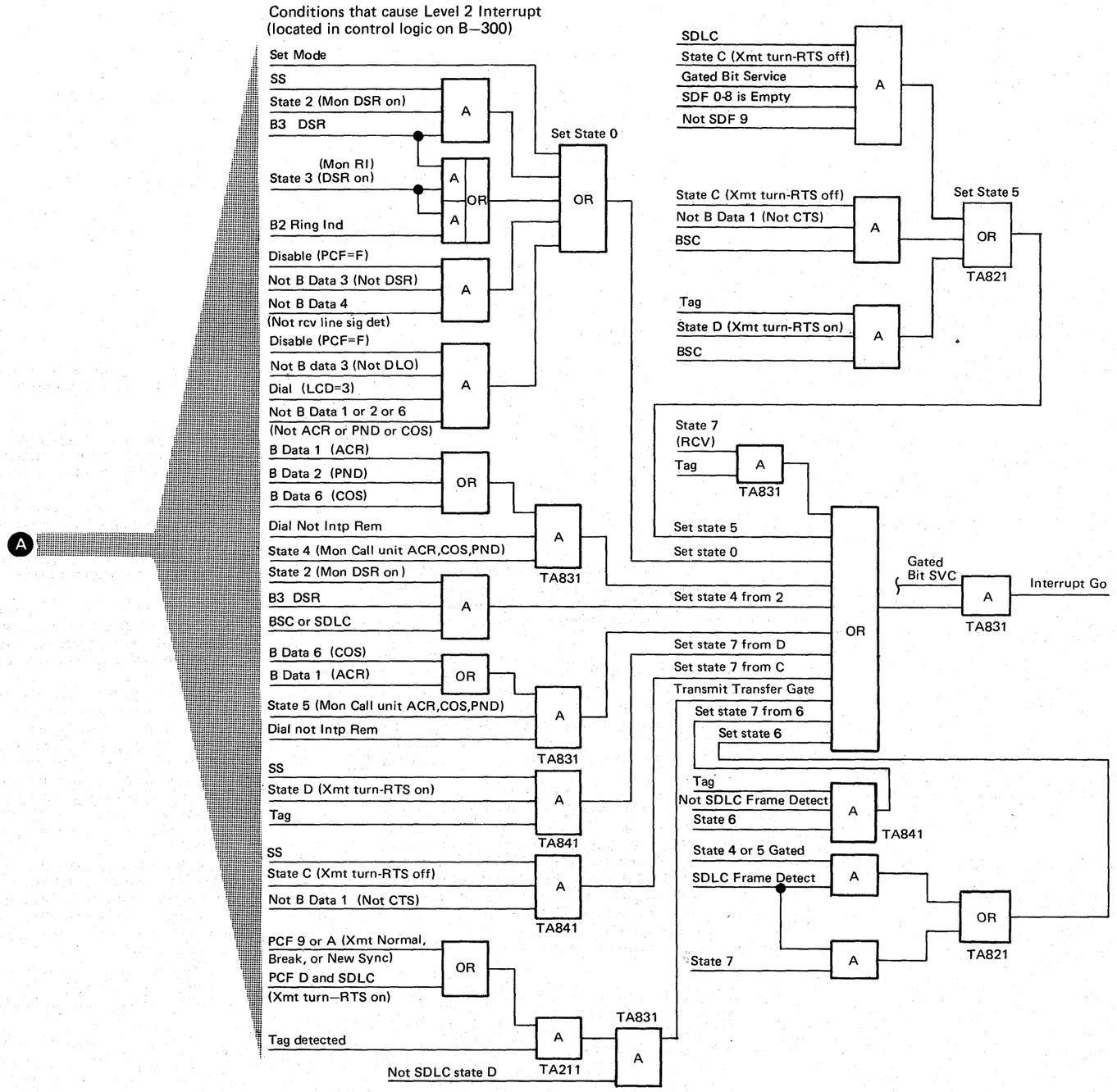
1 During scan addressing, the scan counter output, modified as required by the substitution control register, selects an interface address and a LIB in each type 2 scanner. The ICWs associated with these selected interface addresses are read into their respective scanner ICW work registers.

2 The availability of the priority registers in the type 2 attachment base are sent to the first scanner. If control logic determines that a condition requiring a level 2 interrupt is present (A), it signals 'interrupt go' to the priority register selection logic. Likewise, if a level 2 interrupt is pending from a previously sensed 'interrupt go' condition, this is signaled to the priority register selection logic.

3 The interface priority is decoded from ICW bits 42 and 43. This priority selects the corresponding register from the 'priority registers available' from the attachment base when 'interrupt go' or 'level 2 interrupt pending' is signaled, and activates the line 'CSB wants a priority register' with the following results:

- Write gate causes the unmodified ICW work register contents and all modified bit positions to write into the ICW local store address selected during this CSB time.
  - 'Interrupt go' sets SCF 1 (service request) if there were no feedback errors and if SCF 0 (stop bit check/rcv break), SCF 2 (char overrun/underrun), and SCF 3 (modem check) are not set.
  - L2 interrupt pending bit (ICW bit 41) is set if the priority register wanted is not available from the attachment base.
  - ICW parity bits are changed accordingly.

4 - The state of the upper scan limit bits 0 and 1 were returned to the attachment base over the common bit 0 and 1 buses at C2 time, before the 'CSB wants a priority register' signal. Each scanner places the 0 and 1 bits associated with its upper scan limit on the scanner 1 position of the common bit 0 and common bit 1 buses. There is a one position skew of all bus positions as the bus chains through all scanners. Therefore, a bit placed on the scanner 1 position by scanner 4 will be in the scanner 4 position in the upper scan limit register in the attachment base. The upper scan limit states from all scanners are thus placed in their respective upper scan limit bit 0 and 1 registers at C2 time.



NOTE: The relationship of the conditions that cause 'interrupt go' and the PCF states is shown on B–080

PROGRAM LEVEL 2 INTERRUPT, PART 2

5 The scanner inhibits the propagation of 'priority register available' for the priority register specified by the priority decode. This makes that priority register not available to the following scanners. These scanners may select priority registers from the remaining 'priority registers available' lines coming into their scanners.

See B—340 for the following example. All priority registers are available to scanner I which wants priority register 3 (I I). Scanner 2 also wants priority register 3 but it is not available, so scanner 2 sets L2 interrupt pending bit 4I in the ICW and waits for priority register 3 to become available on a future scan. Scanner 3 wants priority register 2 while scanner 4 wants priority register 0. Because
6 scanners I, 3, and 4 want priority registers that are available, the scanners gate their respective priority bits to the scanner I position of common bit 0 and common bit I buses as they chain through the scanners. These are the same skewed buses described in the preceding paragraph. The priority bits for all scan-
7 ners are gated into the priority request bit 0 and priority request bit I registers at C5 time.

8 The scan counter output (modified as required by the substitution control register) is placed into the counter register and buffered. It is modified by the upper scan limits from each scanner that requested a priority register according to the corresponding chart on B—360. This modification is required since each scanner's upper-scan limits modified the scan counter output in selecting the interface address and associated ICW. The same modification must be made in the attachment base for each scanner to return to the program the interface address that caused the level 2 interrupt.

9 The upper scan limit register bits 0 and 1 are time-multiplexed by scanner number as shown on B—340. Scanner 4 modification occurs at C56 time, followed by scanner 3 at C67 time, scanner 2 at C70, and scanner 1 at C01 time.

10 The priority request register bits 0 and 1 are time-multiplexed by scanner number in the same way (See B—340). The 0 and 1 bits are encoded to select one of the associated priority registers at each time.

11 The 'CSB wants register' output is likewise time-multiplexed by scanner number to generate the set priority register pulses. These pulses set the modified counter register contents (interface address) into the priority register selected by the associated select priority pulses. In addition, the scanner identification code is gated into priority register positions 0.6 and 0.7. This code is formed by timing pulses as shown on B—340 and identified as 'bits 0.6 and 0.7 to priority reg'.

12 Four program level 2 interrupt priority registers are in the type 2 attachment base. These four registers are shared by all four scanners. Each priority register has a different priority, with priority 11 (3) the highest. Each interface address is assigned to one of these four priorities via the priority select bits 1-2 (ICW bits 42-43). The higher speed lines should be assigned a higher priority than the lower speed lines to avoid a character overrun (receiving), or underrun (transmitting).

13 At the same time the interface address is set into the selected priority register, the selecting priority is set into the associated 'priority register occupied' latch. This results in the following:

14 • As long as any occupied latch is set, the CSB bid level 2 latch is set. This causes the type 2 attachment base to bid for a program level 2 interrupt in the CCU. The State of the CSB bid L2 latch may be inspected by the program executing Input X'77'.

15 • The highest priority in the occupied latches selects that priority register and causes its contents to read into the pre ABAR (attachment buffer address register).

16 • The highest priority value is also set in the corresponding 'priority in pre ABAR' latch.

17 When the CCU accepts the program level 2 bid, the line 'prog lev 2 next' turns on the 'start of L2' latch in the attachment base (CX001). This gates the interface address that caused the interrupt from the pre ABAR to the ABAR, and gates the priority value from the 'priority in pre ABAR' latch into the corresponding 'priority in ABAR' latch.

18 The 10-bit interface address in ABAR is gated to the line address bus at C0 time; then program addressing occurs as explained on B—290. Each scanner gates the ICW associated with this interface address into its ICW work register at R1T3 time. The 'start of L2' causes the line 'fetch buffer' to gate the ICW working registers into their
19 respective ICW input registers at R1M1T0 time. The CSB select bits determine which ICW input register contents are used when the control program executes the appropriate input instructions.

20 When Input X'40' is executed in program level 2, the character control block (CCB) vector address associated with the interface address that caused the interrupt is sent to the general register. Then the interrupt handling program can identify which interface wants service. B—330 contains a summary of all the character control block vector assignments.

21 Input X'40' executed in program level 2 also resets the 'priority register occupied' latch associated with the priority in the 'priority in ABAR' latch. This makes that priority register available to the scanners.

CHARACTER CONTROL BLOCK VECTOR ADDRESS

During a program level 2 interrupt, when the program executes an Input X'40', the interface address that caused the program level 2 interrupt is gated from the ABAR to a general register in the CCU. The relationship between the ABAR positions and the general register is shown at **1** .

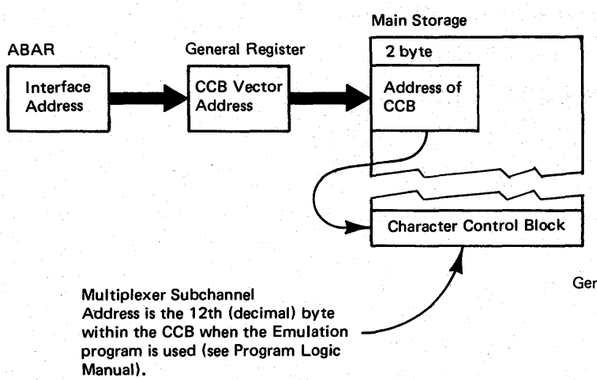
The output of ABAR forms the 'interface address'; for this example it is interface address 020 (hex). The contents of the general register form the character control block (CCB) vector address—in this example, 840 (hex).

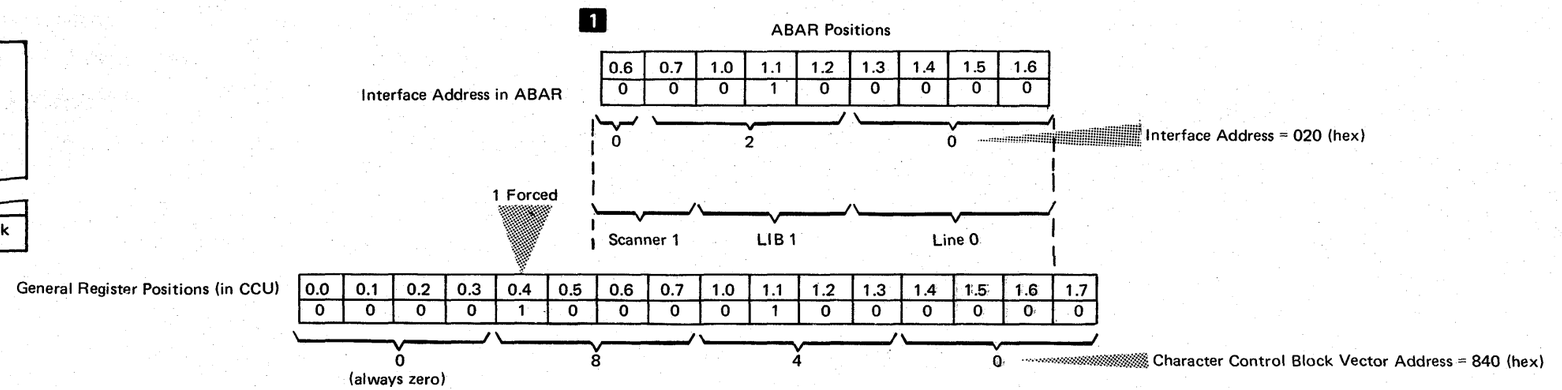
Each interface address has a two-byte permanent storage location that is addressed by its associated character control block vector address. See the accompanying chart for the CCB vector address assigned to each interface address.

The two-byte storage location contains an address pointing to status information concerning that line. This information is used by the routine that handles the program level 2 interrupt. The status information depends upon the program used, such as an emulation program, network control program, or customer-written program. This status information resides in the character control block when the network control program is used.

Type 2 Communication Scanner — LIB Position Interface Address Assignments and CCB Vector Storage Addresses

Frame and LIB Position		INTERFACE ADDRESS ASSIGNMENTS (HEX) 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		Character Control Block Vector Storage Addresses (Hex)															
3705																	
LIB position	1	0 2 _	840	842	844	846	848	84A	84C	84E	850	852	854	856	858	85A	85C	85E
	2	0 3 _	860	862	864	866	868	86A	86C	86E	870	872	874	876	878	87A	87C	87E
	3	0 4 _	880	882	884	886	888	88A	88C	88E	890	892	894	896	898	89A	89C	89E
	4	0 5 _	8A0	8A2	8A4	8A6	8A8	8AA	8AC	8AE	8B0	8B2	8B4	8B6	8B8	8BA	8BC	8BE
Expansion Frame 1																		
LIB position	1	0 A _	940	942	944	946	948	94A	94C	94E	950	952	954	956	958	95A	95C	95E
	2	0 B _	960	962	964	966	968	96A	96C	96E	970	972	974	976	978	97A	97C	97E
	3	0 C _	980	982	984	986	988	98A	98C	98E	990	992	994	996	998	99A	99C	99E
	4	0 D _	9A0	9A2	9A4	9A6	9A8	9AA	9AC	9AE	9B0	9B2	9B4	9B6	9B8	9BA	9BC	9BE
	5	0 E _	9C0	9C2	9C4	9C6	9C8	9CA	9CC	9CE	9D0	9D2	9D4	9D6	9D8	9DA	9DC	9DE
	6	0 F _	9E0	9E2	9E4	9E6	9E8	9EA	9EC	9EE	9F0	9F2	9F4	9F6	9F8	9FA	9FC	9FE
Expansion Frame 2																		
LIB position	1	1 2 _	A40	A42	A44	A46	A48	A4A	A4C	A4E	A50	A52	A54	A56	A58	A5A	A5C	A5E
	2	1 3 _	A60	A62	A64	A66	A68	A6A	A6C	A6E	A70	A72	A74	A76	A78	A7A	A7C	A7E
	3	1 4 _	A80	A82	A84	A86	A88	A8A	A8C	A8E	A90	A92	A94	A96	A98	A9A	A9C	A9E
	4	1 5 _	AA0	AA2	AA4	AA6	AA8	AAA	AAC	AAE	AB0	AB2	AB4	AB6	AB8	ABA	ABC	ABE
	5	1 6 _	AC0	AC2	AC4	AC6	AC8	ACA	ACC	ACE	AD0	AD2	AD4	AD6	AD8	ADA	ADC	ADE
	6	1 7 _	AE0	AE2	AE4	AE6	AE8	AEA	AEC	AEE	AF0	AF2	AF4	AF6*	AF8	AFA	AFC	AFE
Expansion Frame 3																		
LIB position	1	1 A _	B40	B42	B44	B46	B48	B4A	B4C	B4E	B50	B52	B54	B56	B58	B5A	B5C	B5E
	2	1 B _	B60	B62	B64	B66	B68	B6A	B6C	B6E	B70	B72	B74	B76	B78	B7A	B7C	B7E
	3	1 C _	B80	B82	B84	B86	B88	B8A	B8C	B8E	B90	B92	B94	B96	B98	B9A	B9C	B9E
	4	1 D _	BA0	BA2	BA4	BA6	BA8	BAA	BAC	BAE	BB0	BB2	BB4	BB6	BB8	BBA	BBC	BBE
	5	1 E _	BC0	BC2	BC4	BC6	BC8	BCA	BCC	BCE	BD0	BD2	BD4	BD6	BD8	BDA	BDC	BDE
	6	1 F _	BE0	BE2	BE4	BE6	BE8	BEA	BEC	BEE	BF0	BF2	BF4	BF6	BF8	BFA	BFC	BFE



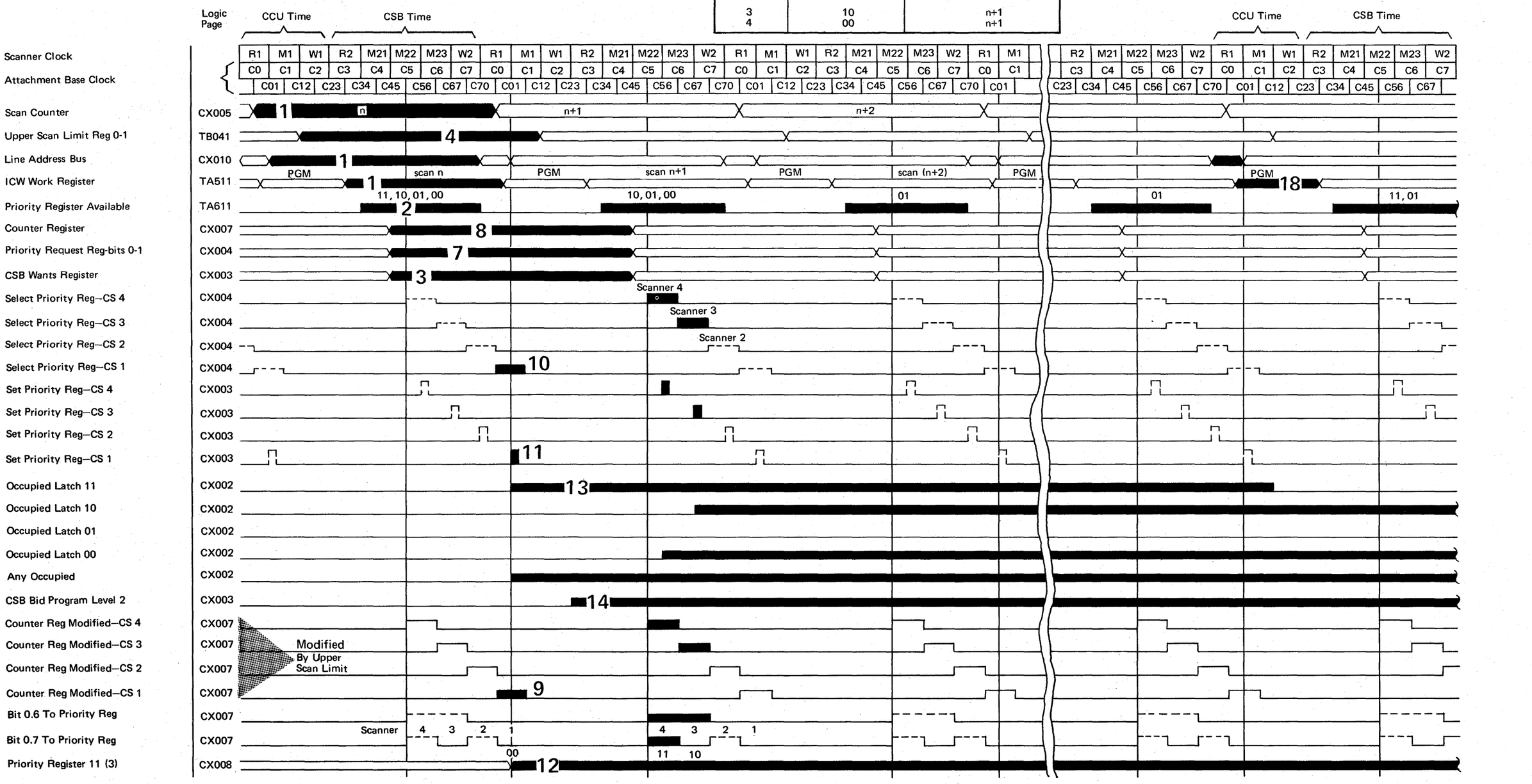


PROGRAM LEVEL 2 INTERRUPT TIMINGS

Numbers refer to B—300 and B—310

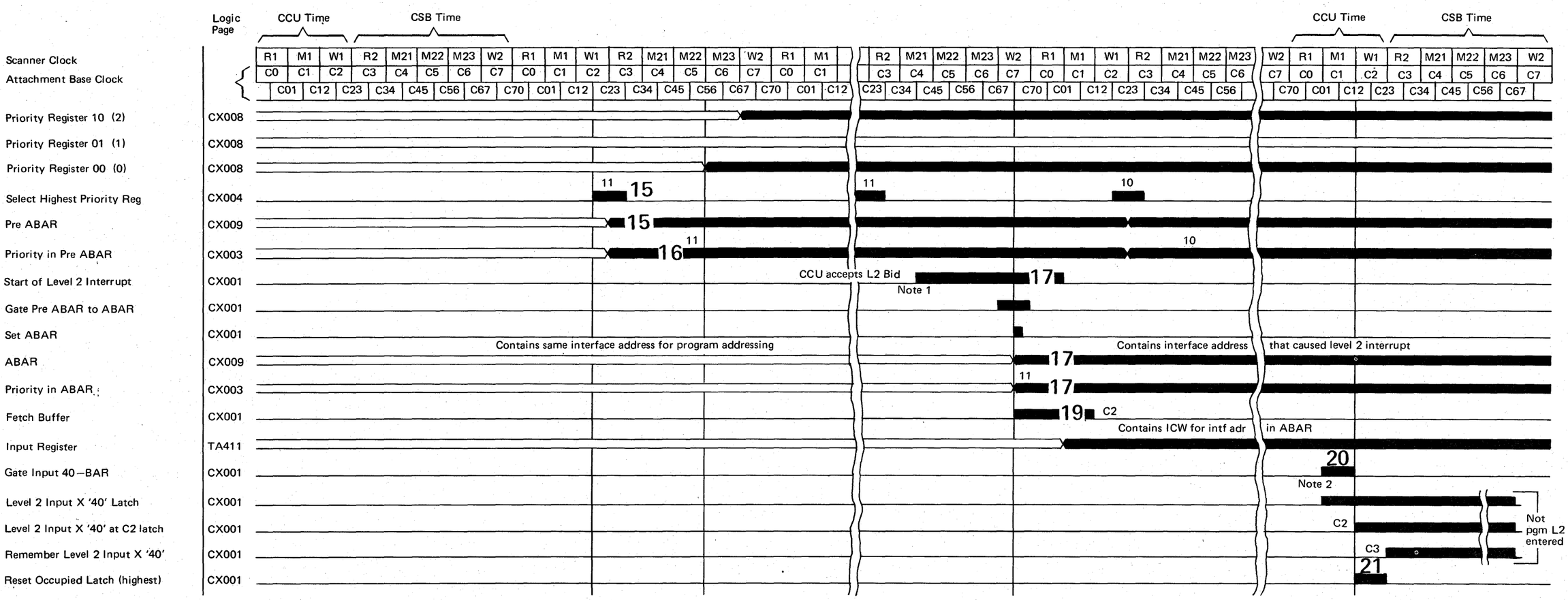
EXAMPLE ILLUSTRATED

Scanner #	Priority in ICW When Scanned	Scan Counter Value When 'Interrupt Go' Is Sensed
1 2	11 11	n n+1
3 4	10 00	n+1 n+1

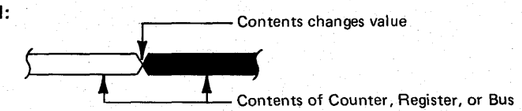


PROGRAM LEVEL 2 INTERRUPT TIMINGS, PART 2

Numbers refer to B–300 and B–310



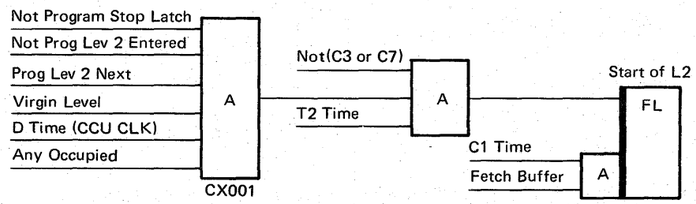
Legend:



Shaded areas indicate the contents apply to the example illustrated

Timing would occur here if conditions were applicable

Timing occurs here



NOTES:
1. This timing varies because it depends upon CCU 'D time' and 'not (C3 or C7) time', and these clocks are asynchronous.
2. Gate Input 40 is independent of the attachment base clock–gated by the CCU clock at CD time.

PROGRAM LEVEL 2 INTERRUPT EXAMPLES

EXAMPLE 1: Substitution ctrl reg 1 = 1, Scanner #1 upper scan limit = 11 (16 lines)

	Position	1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1	Action Performed—Comments
1	Scan Counter	1	0	1	0	1	1	1	0	
	Counter Register/Line Address Bus	1	1	0	0	0	0	0	0	Adr substitution—(See B–220) Interface Address 020
	ICW Local Store Address	0	1	0	0	0	0	0	0	Modified by upper scan limit = 11 (See B–230) Selected—LIB 1, adr = 0, ICW = 020

Interface address 020 requests level 2 interrupt (priority = 11)

	Position	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	
12	Priority Register 11	0	0	0	1	0	0	0	0	0	Modify counter reg according to accompanying charts 1 and 2.
17	ABAR	0	0	0	1	0	0	0	0	0	ABAR loaded by pgm lev 2 interrupt

Force 1 — Scanner 1 (2) — LIB 1 (3) — Line Adr 0 (Hex) — Interface address = 020 on In Data Bus

	In Data Bus position	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	
20	General Reg. in CCU	1	0	0	0	0	1	0	0	0	0	0	0	Character Control Block Vector

8 4 0 — Address = 840 (See B–330)

EXAMPLE 2: Substitution ctrl reg 1 = 1, Scanner #3 upper scan limit = 01 (8 lines)

	Position	1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1	Comment
1	Scan Counter	1	0	1	0	1	1	0	1	
	Counter Register/Line Address Bus	1	0	1	0	1	1	0	1	No adr substitution—(See B–220) Interface Address 13D
	ICW Local Store Address	0	1	0	0	0	1	0	1	Modified by upper scan limit = 01 (See B–230) Selected—LIB 1, adr 5, ICW = 125

Interface address 125 requests level 2 interrupt (priority = 10)

	Position	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	
12	Priority Register 10	1	0	0	1	0	0	1	0	1	Modify counter reg according to accompanying charts 1 and 2.
17	ABAR	1	0	0	1	0	0	1	0	1	ABAR loaded by pgm lev 2 interrupt

Force 1 — Scanner 3 (2) — LIB 1 (3) — Line Adr 5 (Hex) — Interface address = 125 on In Data Bus

	In Data Bus position	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	
20	General Reg in CCU	1	0	1	0	0	1	0	0	1	0	1	0	Character Control Block Vector

A 4 A — Address = A4A (See B–330)

Numbers to the left of the examples refer to B–300, B–310 and B–320.

1 UPPER SCAN LIMIT MODIFICATION OF THE COUNTER REGISTER

Upper Scan Limits Bit 0	Bit 1	Counter Register bit positions 1st 3	1 or 4	2 or 5	3 or 6	8	4	2	1	Priority Register bit positions 1.0	1.1	1.2	1.3	1.4	1.5	1.6	Significance
0	0	1	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB 1
(96 lines)		1	0	1	0	X	X	X	X	0	1	1	X	X	X	X	LIB 2
		1	0	0	1	X	X	X	X	1	0	0	X	X	X	X	LIB 3
		0	1	0	0	X	X	X	X	1	0	1	X	X	X	X	LIB 4
		0	0	1	0	X	X	X	X	1	1	0	X	X	X	X	LIB 5
		0	0	0	1	X	X	X	X	1	1	1	X	X	X	X	LIB 6
1	0	1	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB 1
(48 lines)		1	0	1	0	X	X	X	X	0	1	1	X	X	X	X	LIB 2
		1	0	0	1	X	X	X	X	1	0	0	X	X	X	X	LIB 3
		0	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB 1
		0	0	1	0	X	X	X	X	0	1	1	X	X	X	X	LIB 2
		0	0	0	1	X	X	X	X	1	0	0	X	X	X	X	LIB 3
1	1	1	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB 1
(16 lines)		1	0	1	0	X	X	X	X	0	1	0	X	X	X	X	LIB 1
		1	0	0	1	X	X	X	X	0	1	0	X	X	X	X	LIB 1
		0	1	0	0	X	X	X	X	0	1	0	X	X	X	X	LIB 1
		0	0	1	0	X	X	X	X	0	1	0	X	X	X	X	LIB 1
		0	0	0	1	X	X	X	X	0	1	0	X	X	X	X	LIB 1
0	1	1	1	0	0	0	X	X	0	0	1	0	0	X	X	0	LIB 1 even lines
(8 lines)		1	0	1	0	1	X	X	0	0	1	0	0	X	X	1	LIB 1 odd lines
		1	0	0	1	1	X	X	1	0	1	0	0	X	X	1	LIB 1 odd lines
		0	1	0	0	0	X	X	0	0	1	0	0	X	X	0	LIB 1 even lines
		0	0	1	0	0	X	X	1	0	1	0	0	X	X	0	LIB 1 even lines
		0	0	0	1	1	X	X	1	0	1	0	0	X	X	1	LIB 1 odd lines

2 SCANNER CODE SET IN PRIORITY REGISTERS

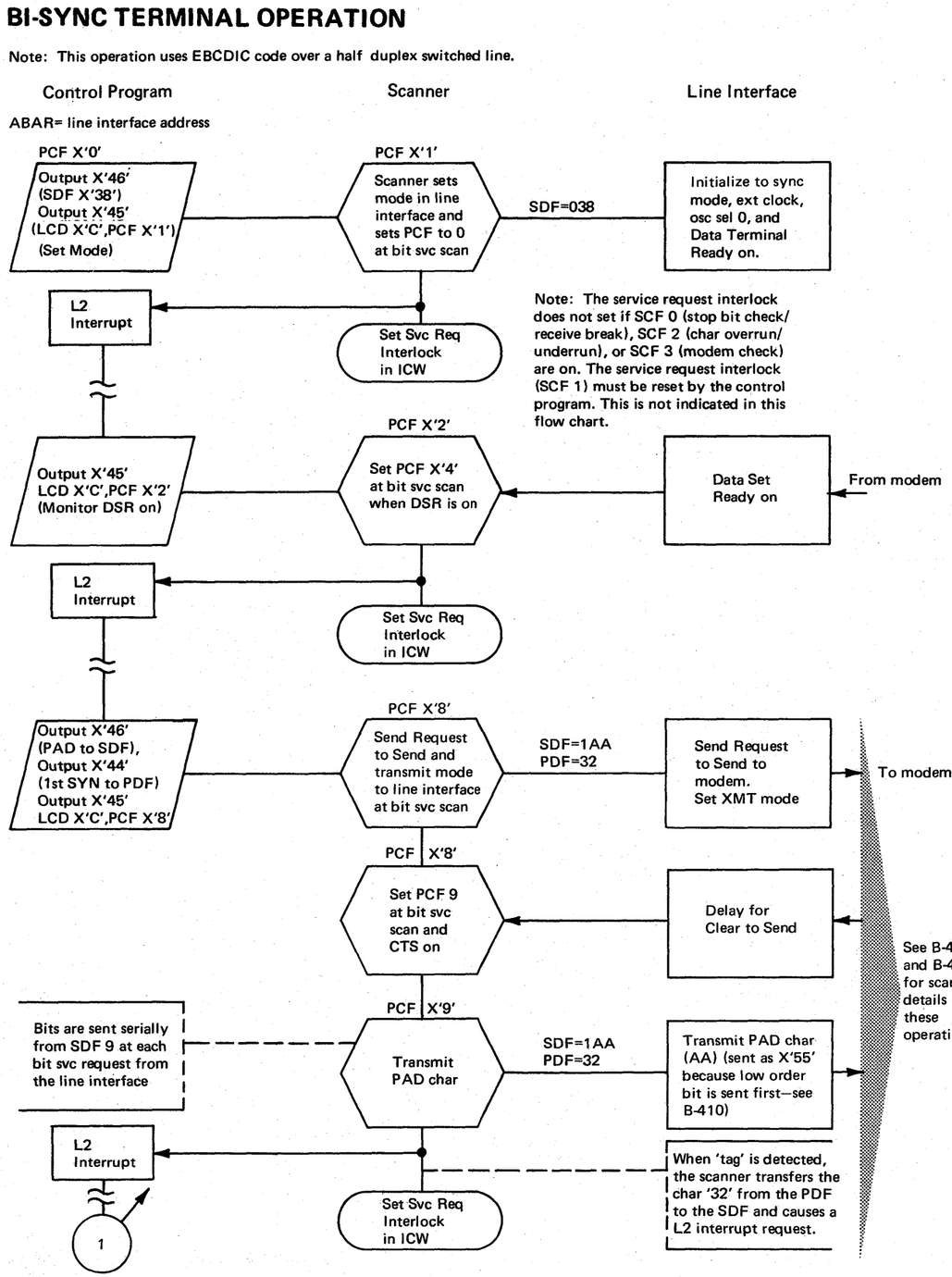
Scanner	Pri Reg bit pos. 0.6	0.7
1	0	0
2	0	1
3	1	0
4	1	1

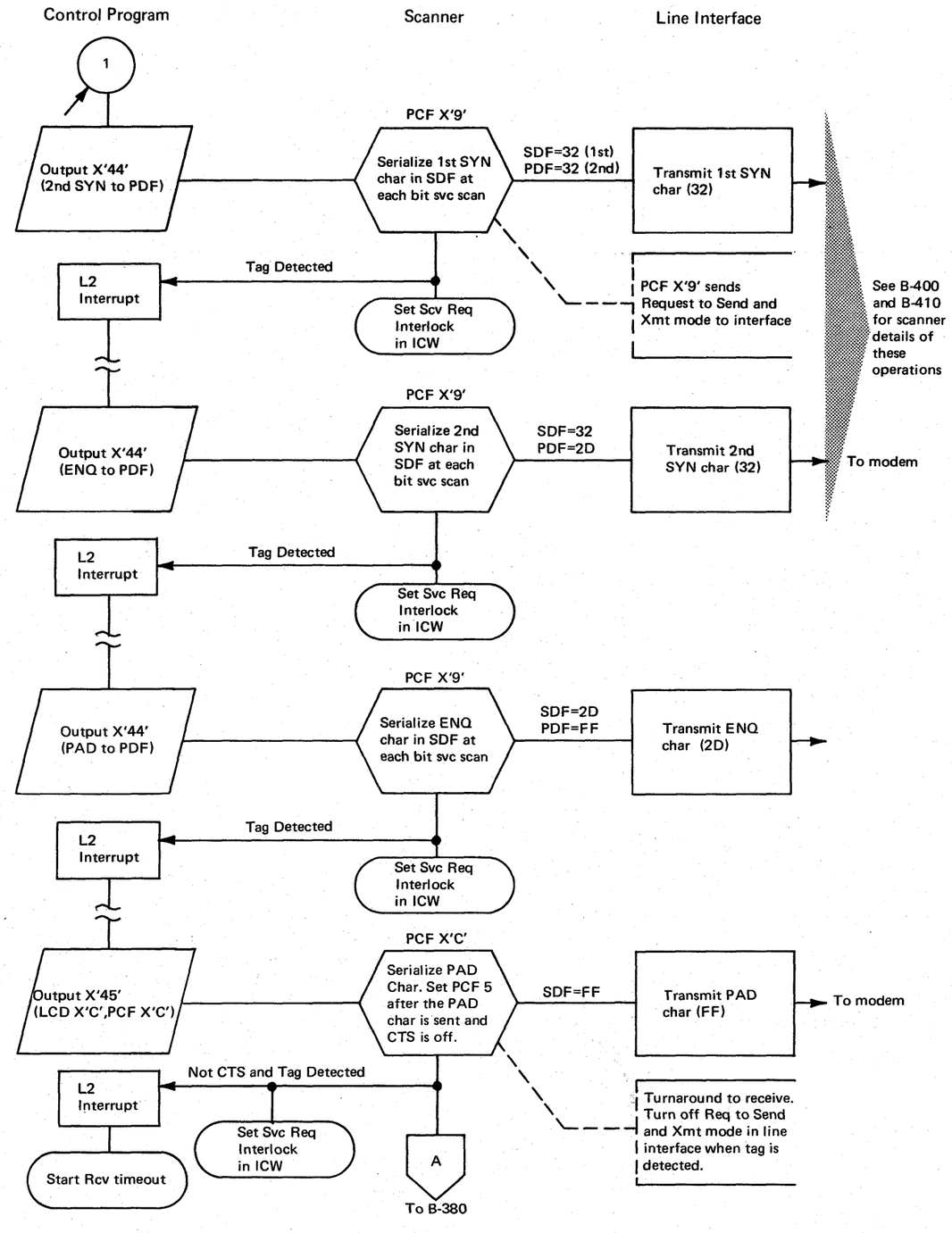
3 LIB IDENTIFICATION

ABAR Positions 1.0	1.1	1.2	Significance of ABAR content
0	1	0	LIB 1
0	1	1	LIB 2
1	0	0	LIB 3
1	0	1	LIB 4
1	1	0	LIB 5
1	1	1	LIB 6

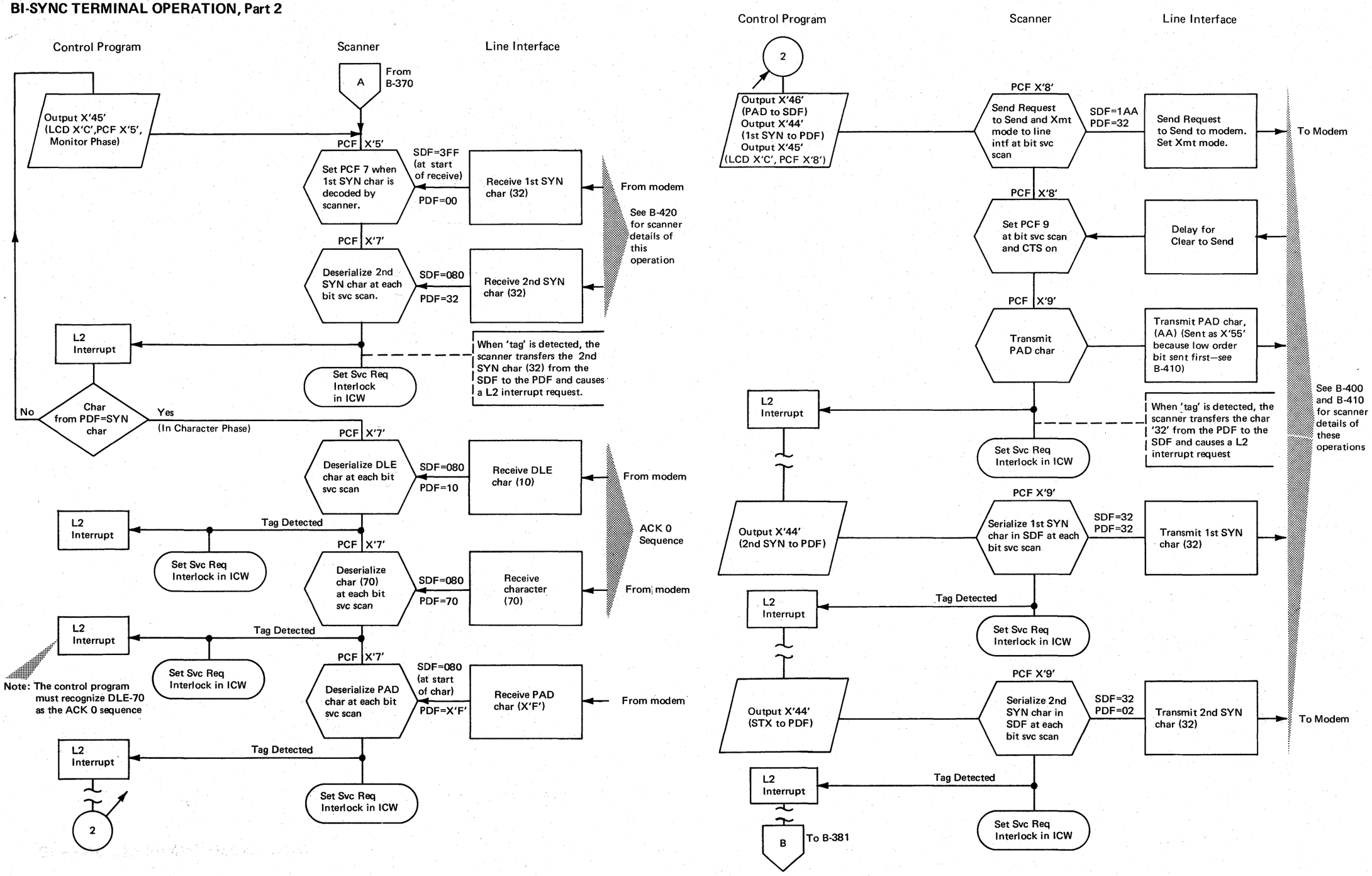
BI-SYNC TERMINAL OPERATION

Note: This operation uses EBCDIC code over a half duplex switched line.

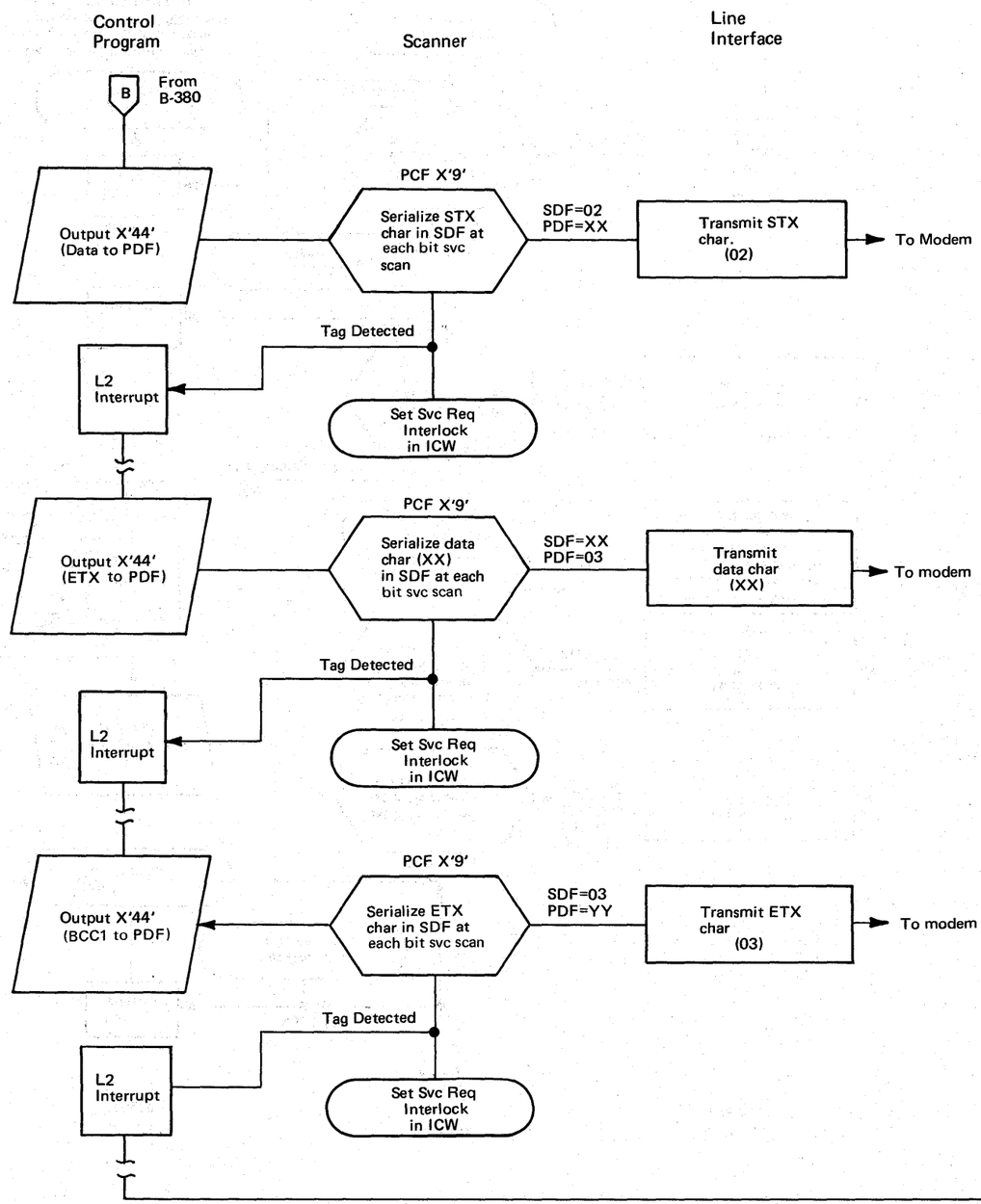


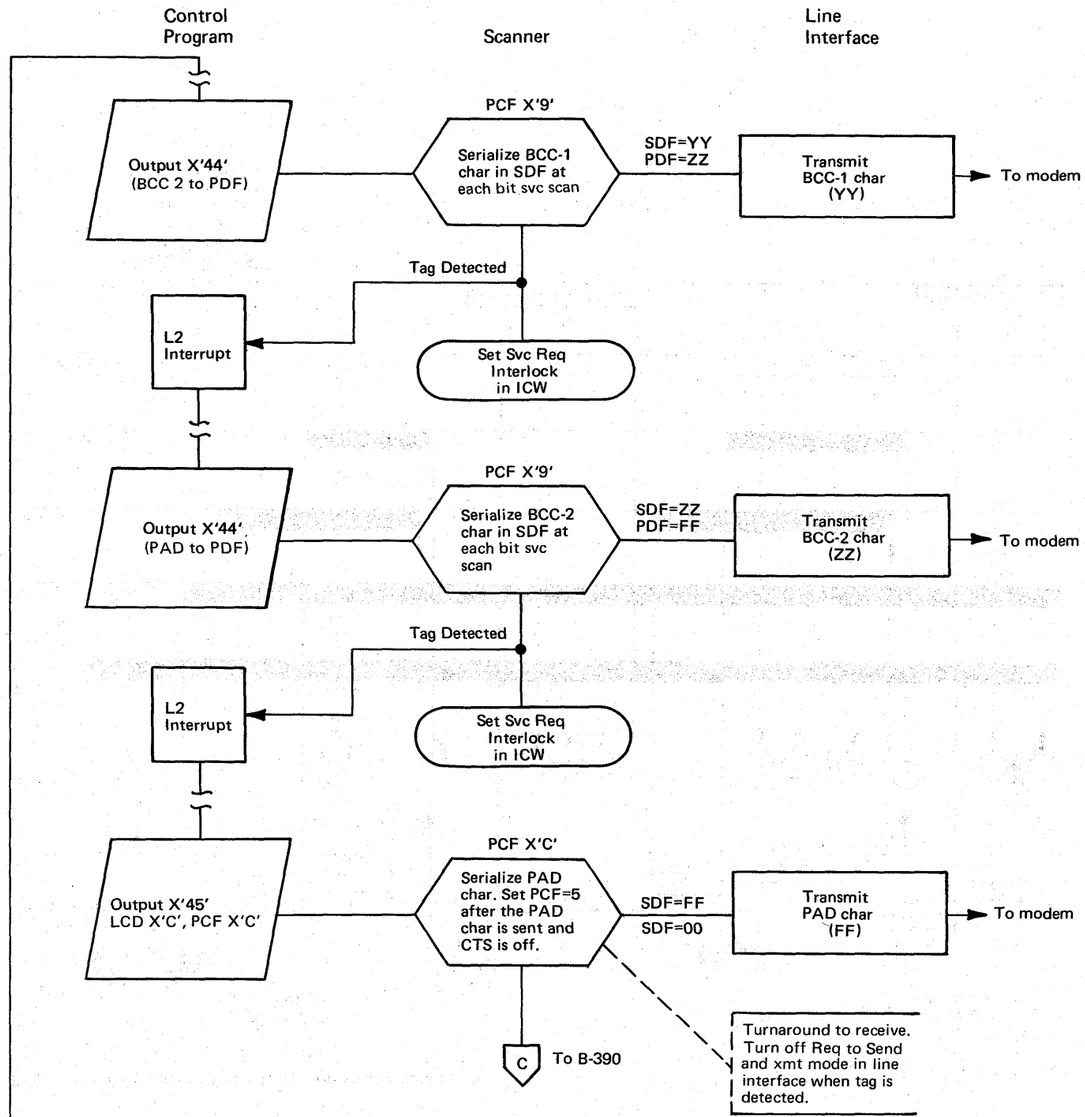


BI-SYNC TERMINAL OPERATION, Part 2

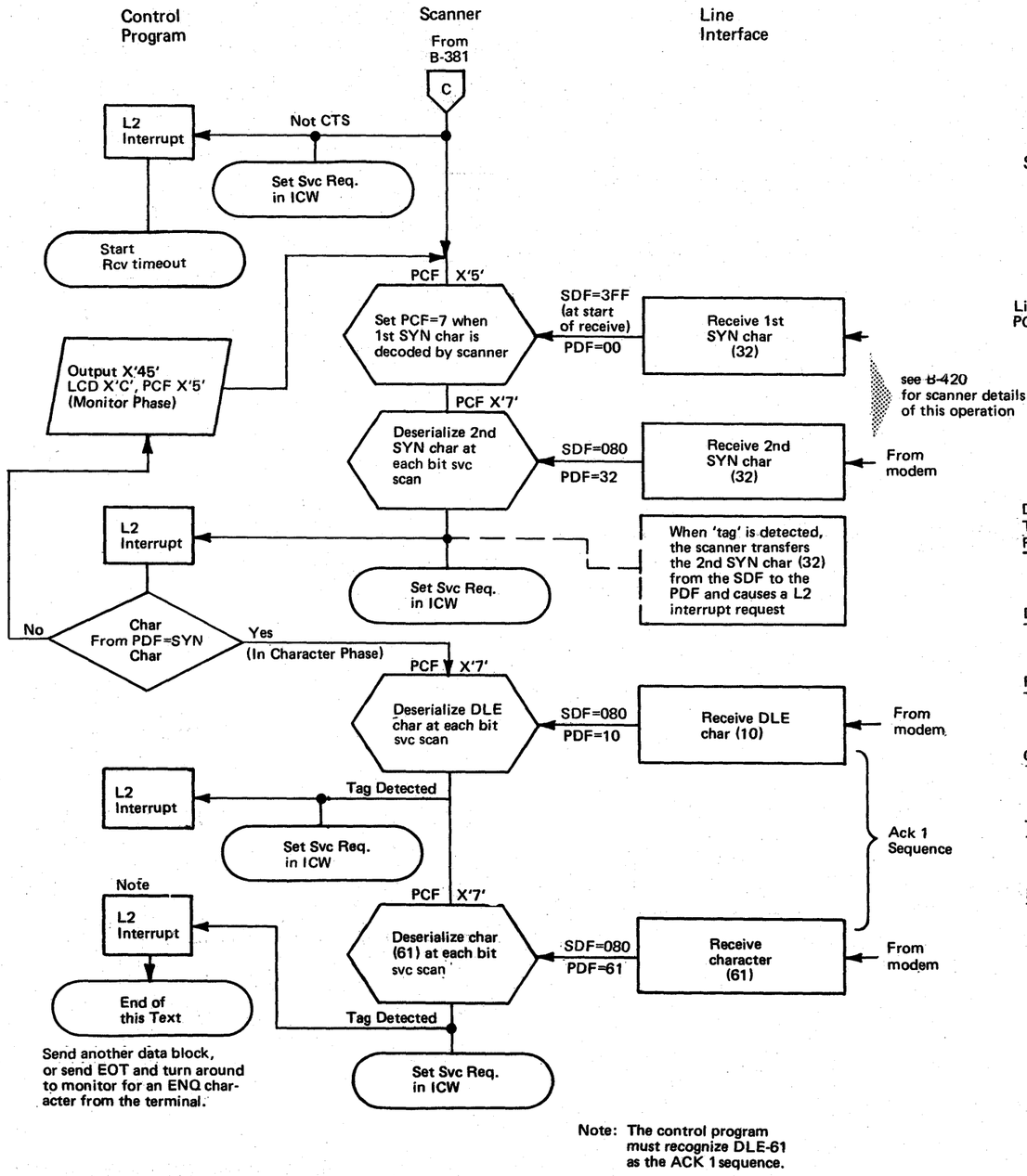


BI-SYNC TERMINAL OPERATION, Part 3



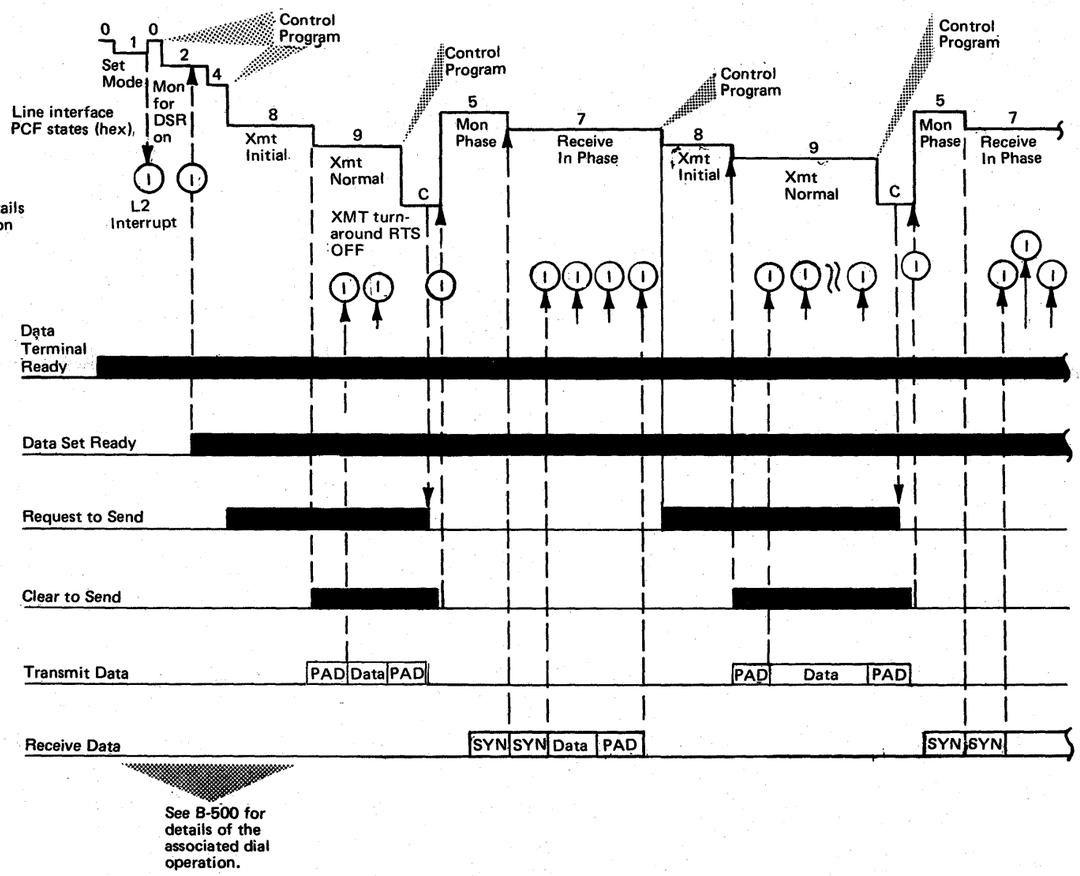


BI-SYNC TERMINAL OPERATION, Part 4



Note: The control program must recognize DLE-61 as the ACK 1 sequence.

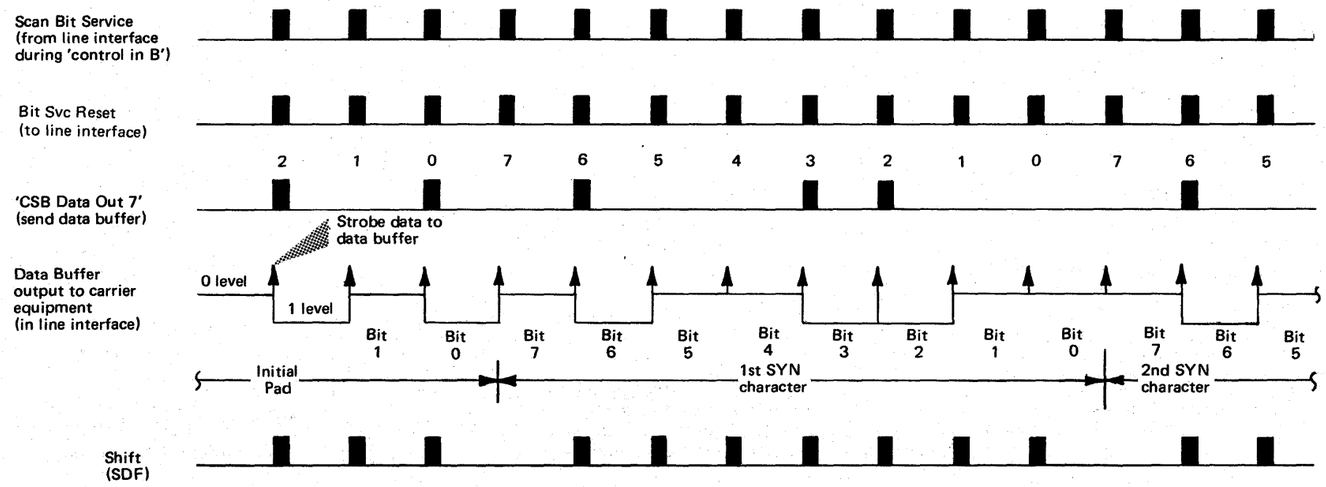
Sequence of Operation For a Half-Duplex Switched Line

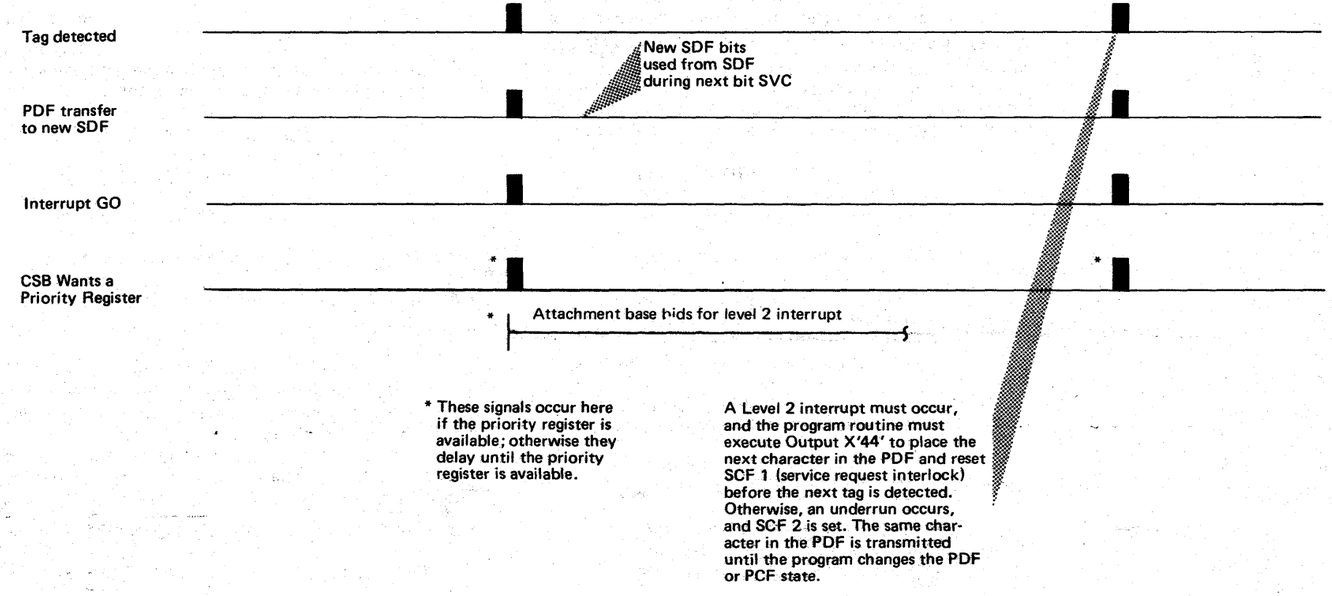


See B-500 for details of the associated dial operation.

BSC TRANSMIT SEQUENCE

See B-410 for details associated with this sequence.





* These signals occur here if the priority register is available; otherwise they delay until the priority register is available.

A Level 2 interrupt must occur, and the program routine must execute Output X'44' to place the next character in the PDF and reset SCF 1 (service request interlock) before the next tag is detected. Otherwise, an underrun occurs, and SCF 2 is set. The same character in the PDF is transmitted until the program changes the PDF or PCF state.

BSC TRANSMIT DETAILS

Note: This example uses LCD = C (EBCDIC code).

The scanner holds 'CSB data out 7' (send data buffer) at the mark level while CTS (clear to send) is off (TA311). 1 While CTS is off, 'SDF direct' regenerates the data in the SDF and 'shift' is inhibited (TA211).

When CTS turns on, the scanner sets PCF=9 (TA831). 2 State 9 becomes the active PCF state at the next 'bit service request' for that interface. The scanner then:

- Removes the mark hold and sends the bit in SDF 9 to the LIB at 'bit service request' time (TA311). 3
- Shifts SDF 0-9 under control of 'bit service request'. 4

  During this shift, the scanner:

  —Inhibits 'SDF direct'.

  —Places a zero in SDF 0. 5

The scanner detects the transmit tag during 'gated bit service' when SDF 0-8 contains all zeros and SDF 9 is 1 (TA261). 6
The scanner:

- Sends the next bit from PDF 7 instead of SDF 9. 7
- Brings up 'sync xmt xfer' that gates PDF 0-6 contents to the SDF (TA231). 8 During this PDF to SDF transfer, the scanner:

  —Sets SDF 2 for the transmit tag. 9 The LCD state determines that this bit is set into SDF 2. This applies to LCD = D (USASCII) also.

  —Forces SDF bits 0-1 to zeros 10 (also under control of LCD C or D).

- Inhibits 'shift' to prevent shifting the new character in the SDF (TA211).
- Brings up 'interrupt go' (TA831) that:

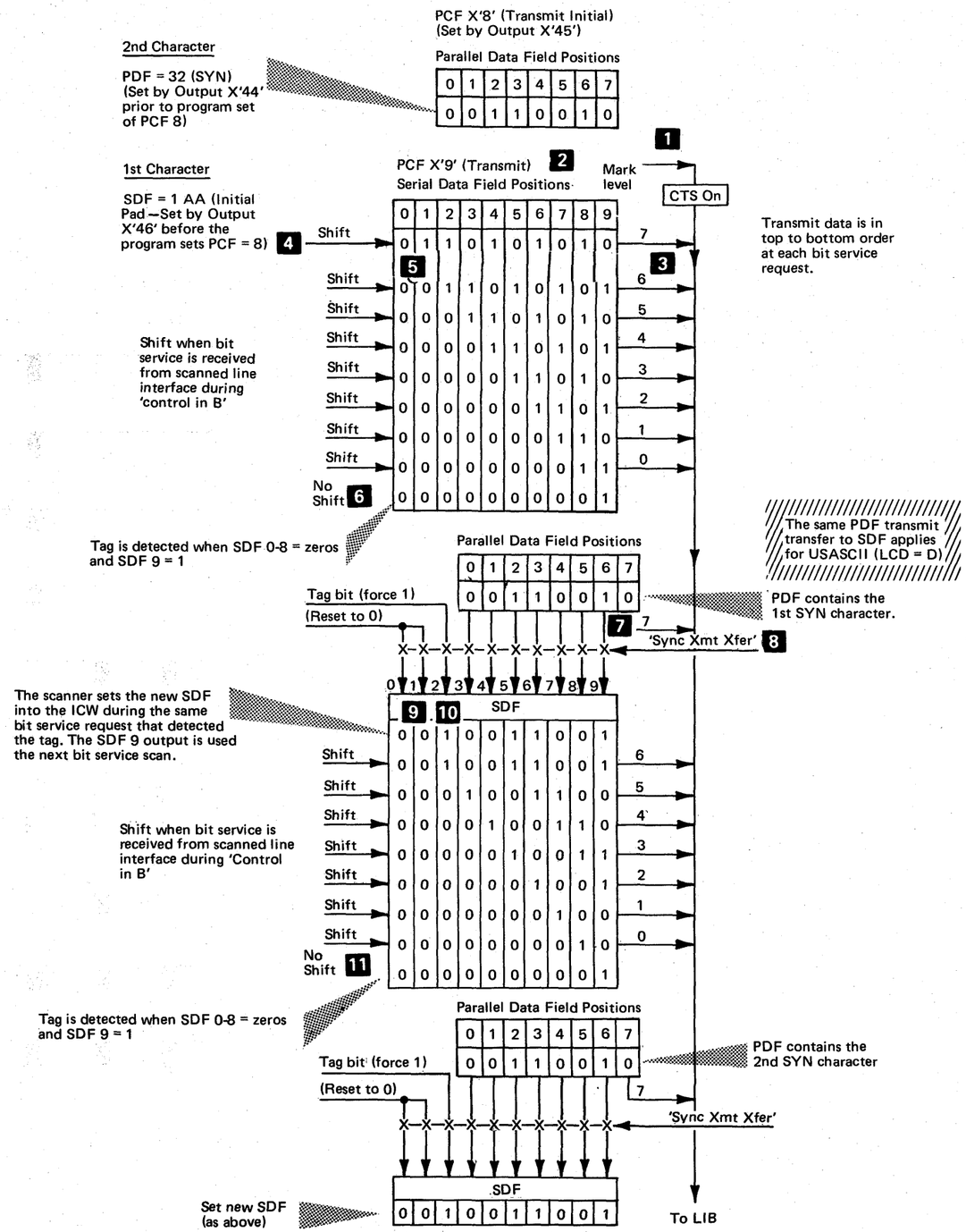
  —Sets SCF 1 (service request interlock) if SCF 0, SCF 2, or SCF 3 are not set (TA121).

  —Causes a L2 interrupt request (TA831).

  —Brings up 'fetch buffer' that gates the ICW content to the input register when the CCU accepts the L2 interrupt (CX001).

The control program executes an Output X'44' to place the next character in the PDF, and to reset SCF 1 (service request interlock). The scanner detects transmit tag (SDF 0-8 = zeros and SDF 9 = 1) for each character sent to the LIB. 11 In addition to the action previously described, the scanner checks to ensure that SCF 1 is off. If on, an underrun has occurred and the scanner sets SCF 2 (overrun/underrun), and resets SCF 1 (TA 121).

The scanner sends characters to the LIB using the above sequence until the control program changes the PCF state to C (transmit turnaround-RTS off), or D (transmit turnaround-RTS on).



BSC RECEIVE DETAILS

Note: Example uses LCD = C (EBCDIC code).

The scanner shifts the received data through the SDF (serial data field) at each bit service request looking for the sync configuration. Once the scanner recognizes the sync configuration (TA841), **1** the scanner:

- Sets PCF = 7 (TA811). **2**
- Inhibits 'gate direct' that prevents regenerating the old PCF 0-3 bits (TA831).
- Generates 'initiate sync 8 rcv tag' (TA841) that:

  —Sets the tag bit in the 'new SDF 2' (TA261) **3**

  —Inhibits 'shift' (TA211). **4**
  With 'gate direct' and 'shift' inhibited, the scanner places zeros in new SDF 0-1 and SDF 3-9 positions. **5**

The scanner shifts the received data through the SDF at each bit service request until the tag bit is detected in SDF 9 (TA261) **6** . When the receive tag is detected, the scanner:

- Initiates 'rcv xfer' (TA711) that:

  —Causes '7 bit xfer' of the SDF contents to the new PDF (TA711) **7** .

  —Gates the new bit to PDF 0 **8** .

  —Inhibits 'PDF direct' (0-7). This prevents the regeneration of the old PDF (TA211).

  —Sets a tag bit in new SDF 2 (TA261) **9** .

  —Inhibits 'shift' and 'SDF direct' (TA211). This resets SDF 0-1 and SDF 3-9 by preventing the regeneration of the old SDF **10** .

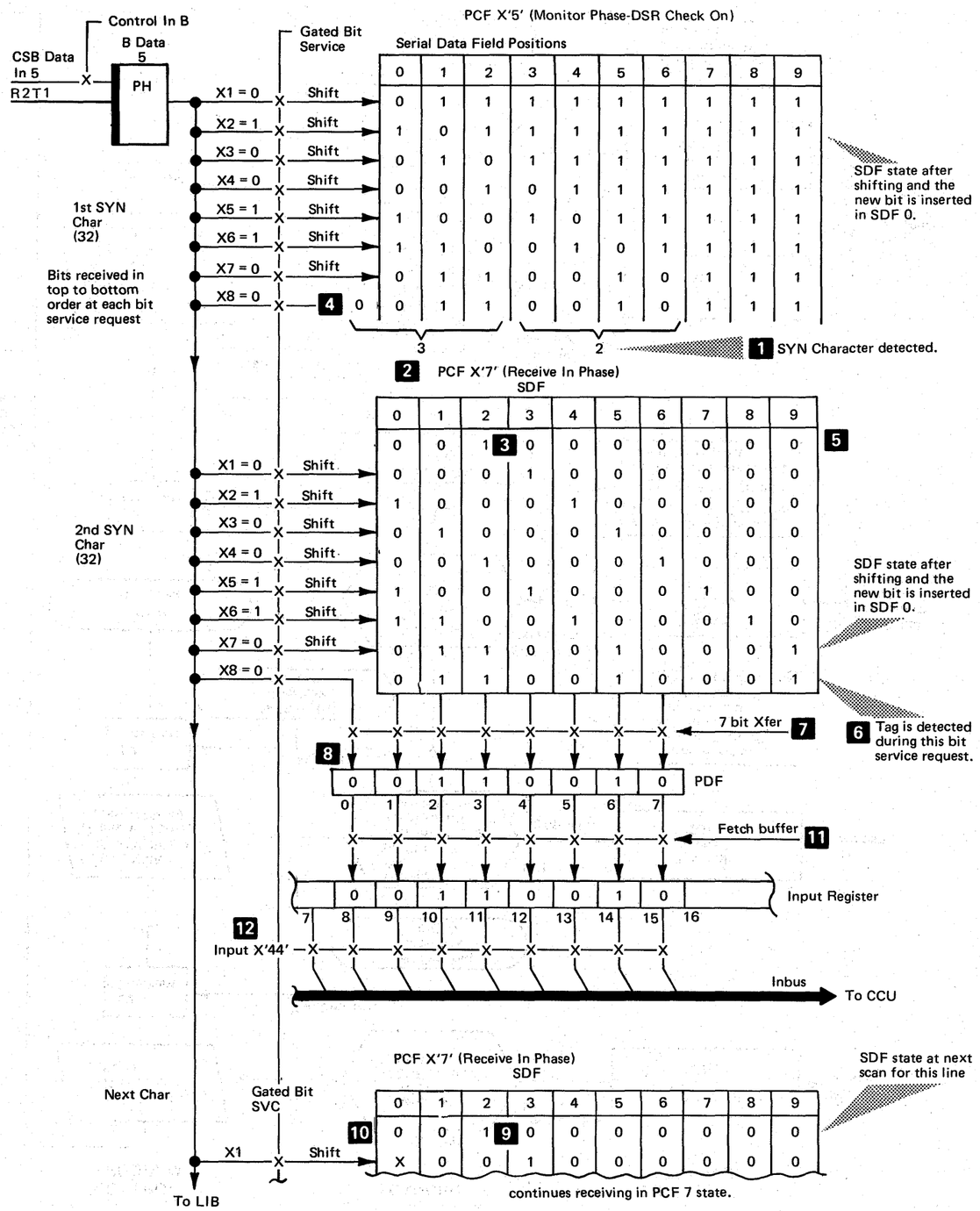
  —Checks for overrun (TA121). If SCF 1 (service request interlock) is on, an overrun has occurred. The scanner sets SCF 2 (overrun/underrun), and resets SCF 1.

  —Brings up 'interrupt go' (TA831) that:

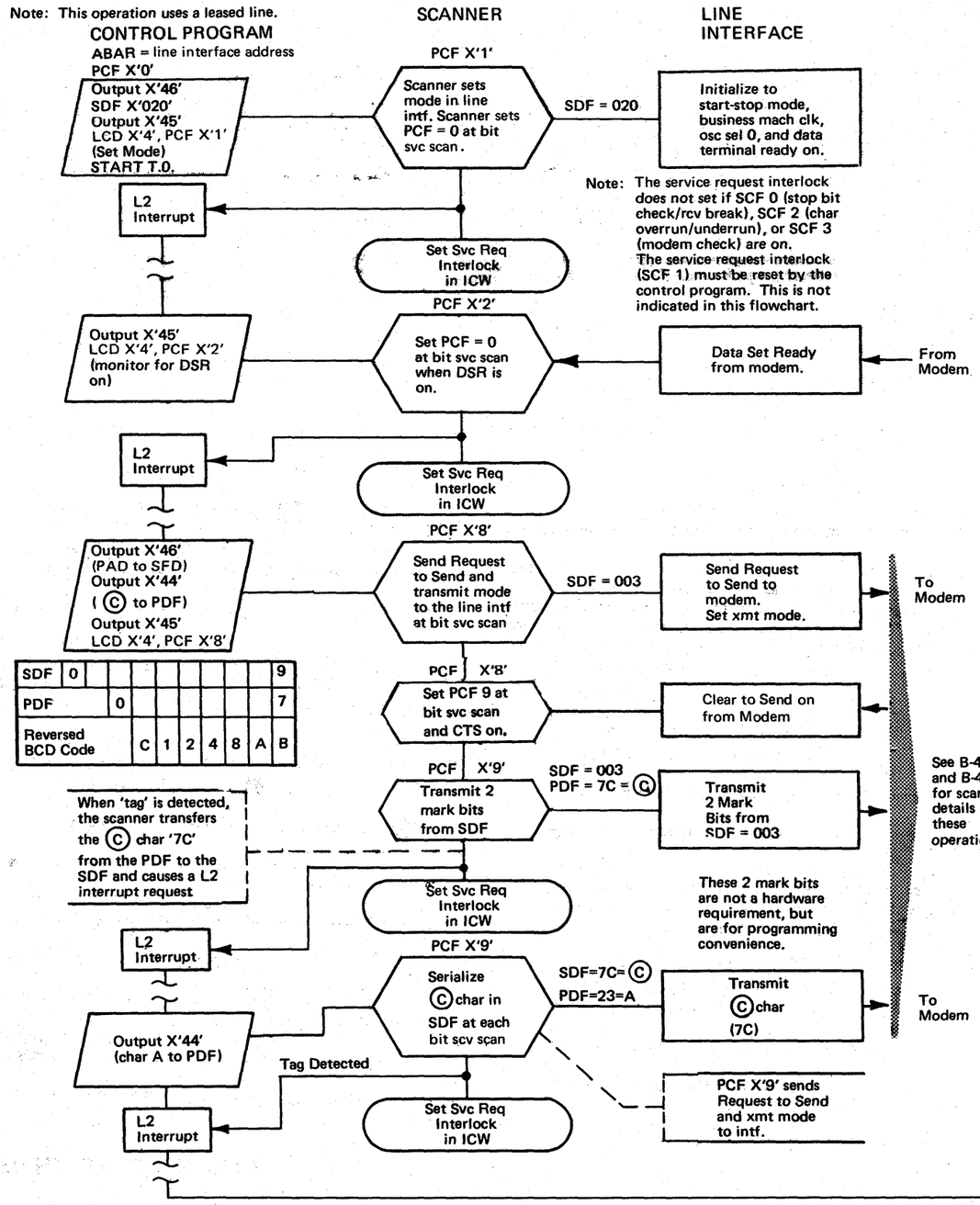
  1. Causes a L2 interrupt request (CX003).
  2. Brings up 'fetch buffer' when the CCU accepts the L2 interrupt (CX001) **11** .

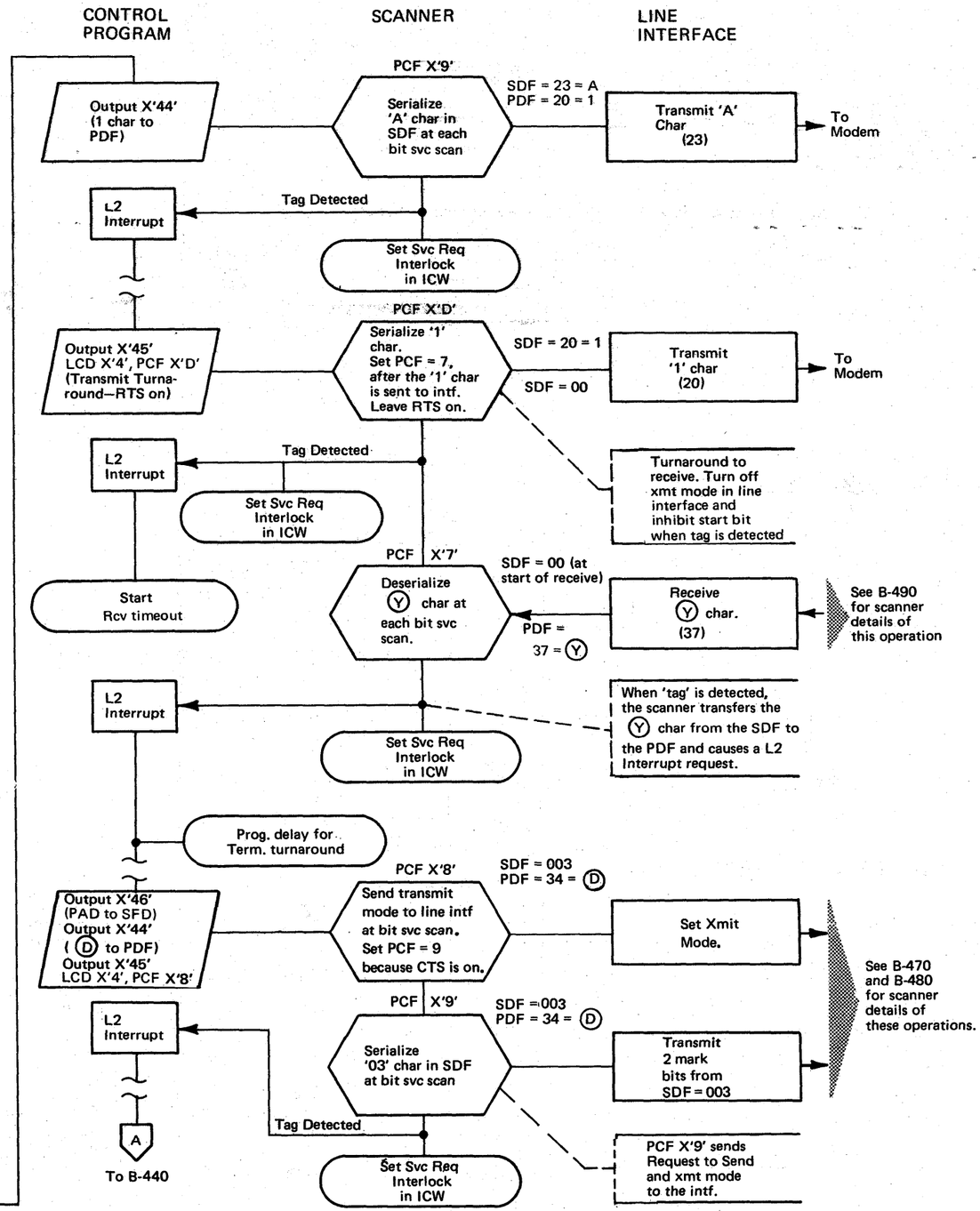
The control program executes Input X'44' to obtain the receive character **12** . If the second character is the SYN character while in PCF X'7', character phase has been established and the program keeps the PCF in state 7. If the second character is not the SYN character, the program sets PCF = 5 (for this example) to resume monitoring for phase.

The same sequence occurs for each character received.

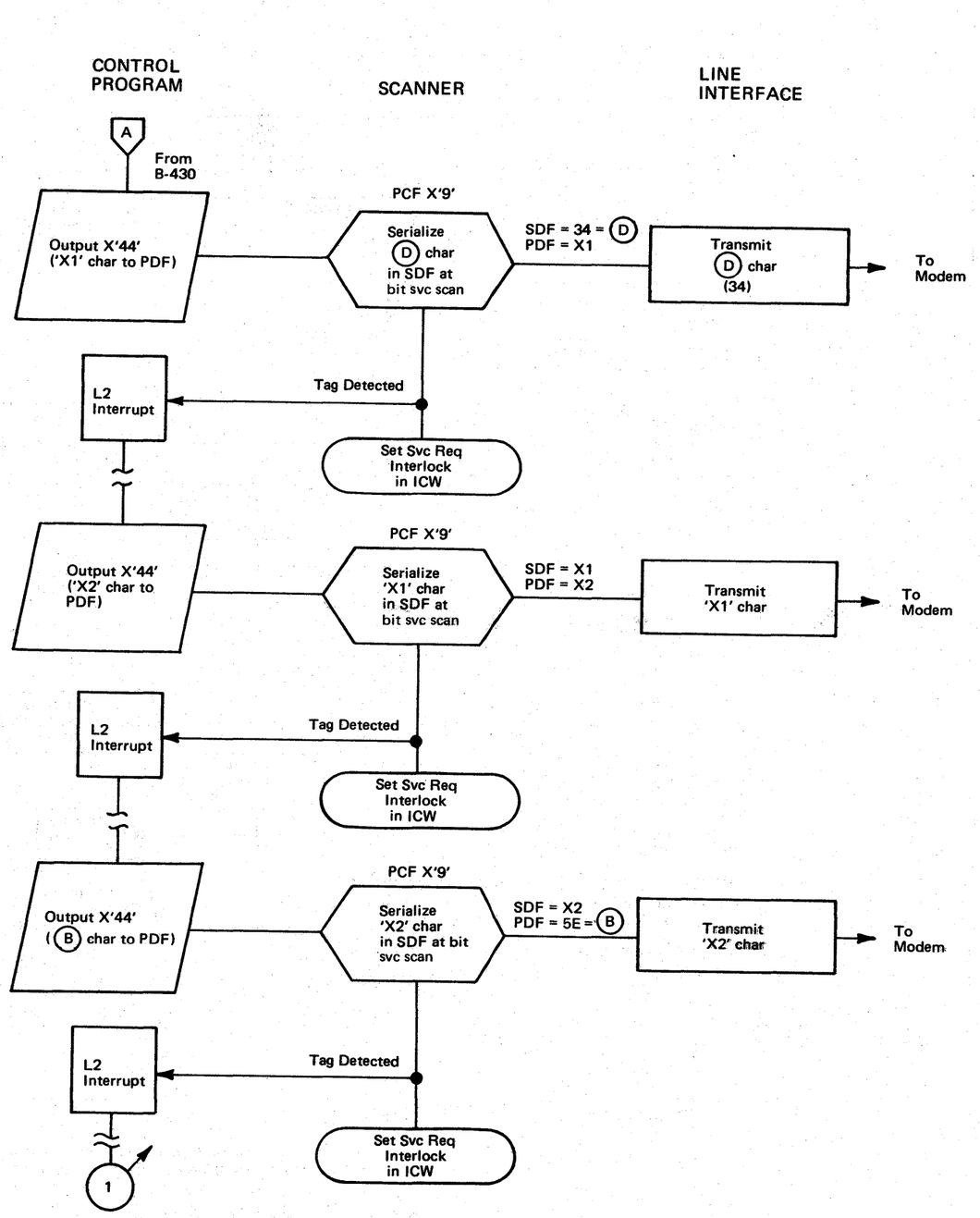


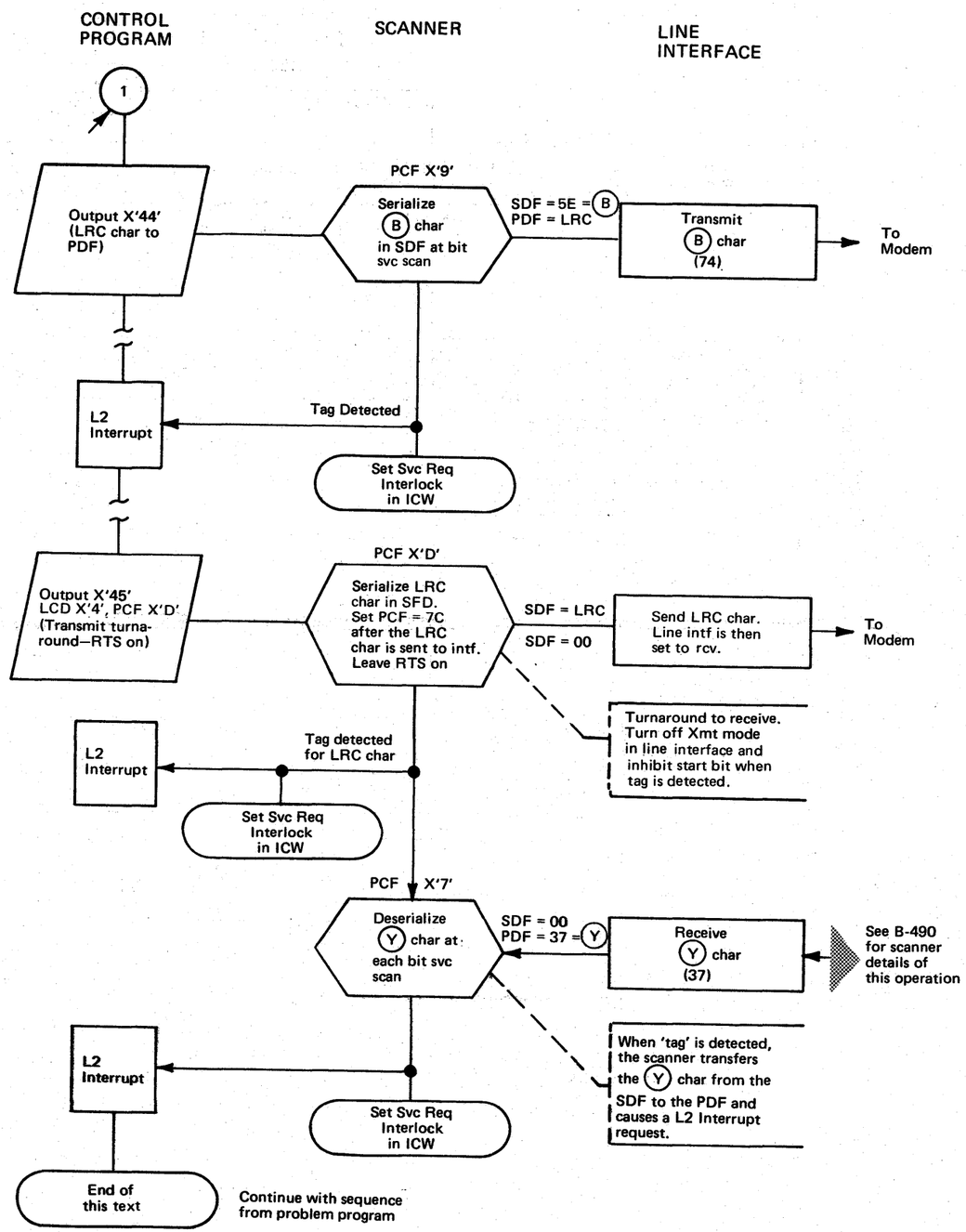
1050 TYPE TERMINAL OPERATION





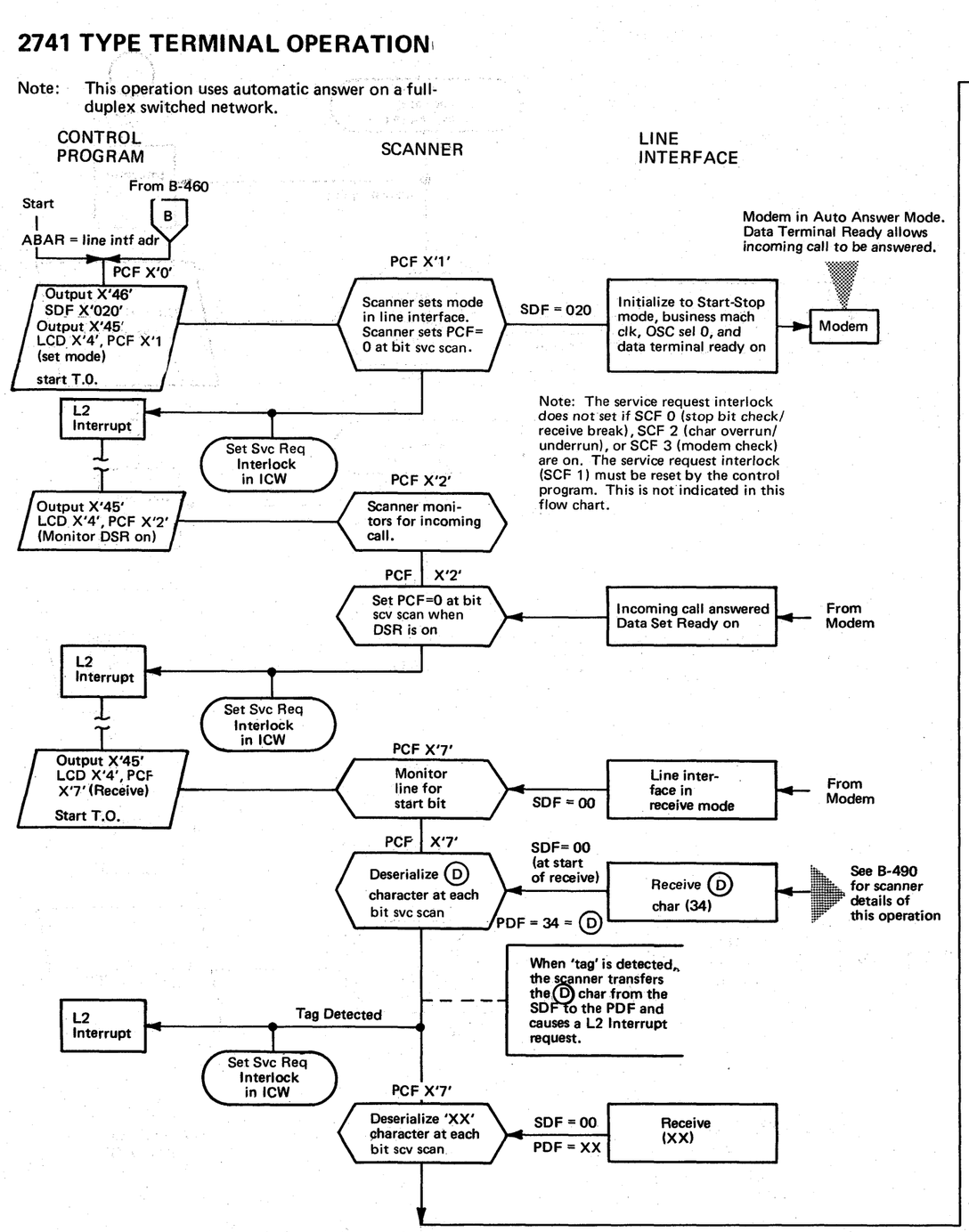
1050 TYPE TERMINAL OPERATION, PART 2



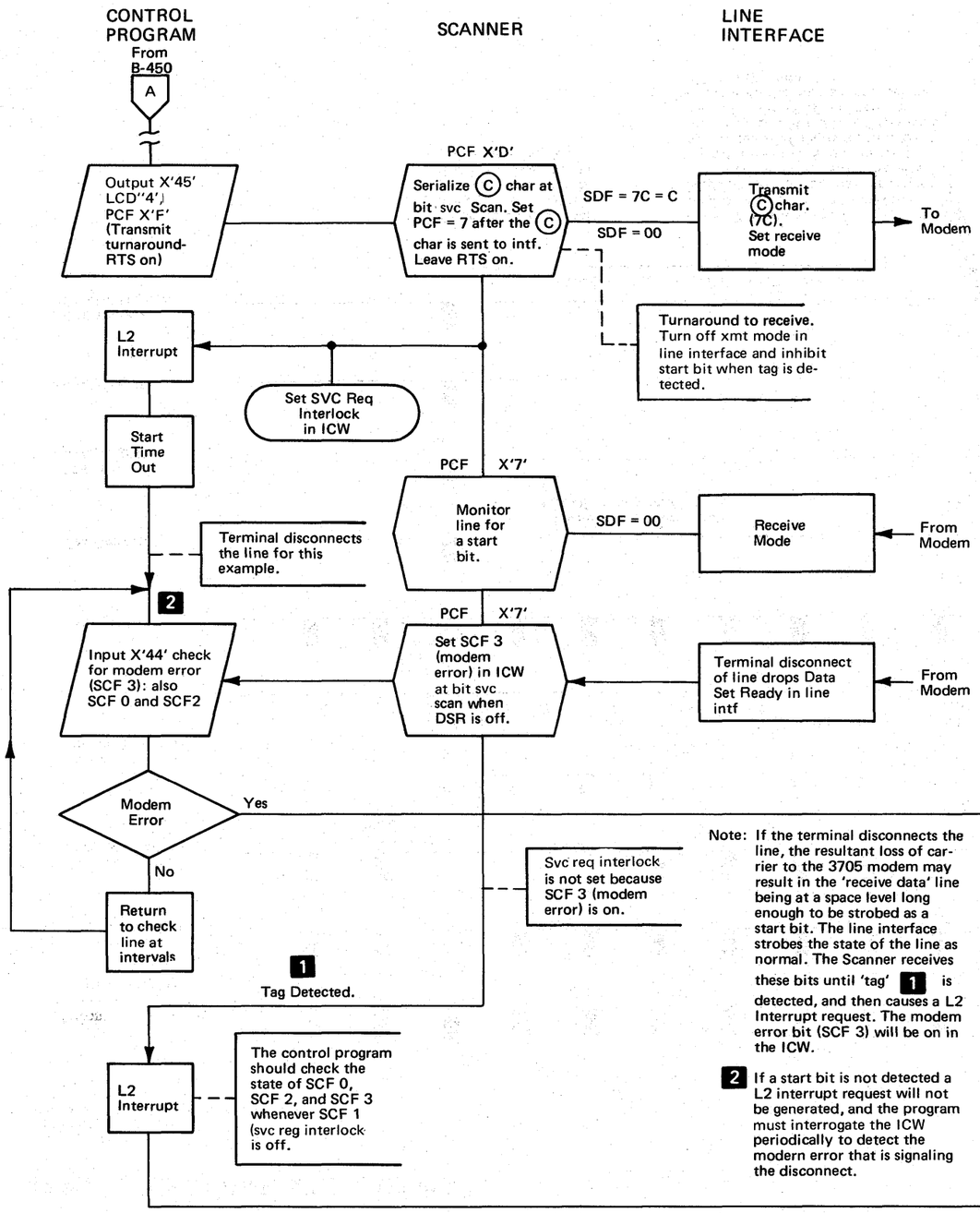


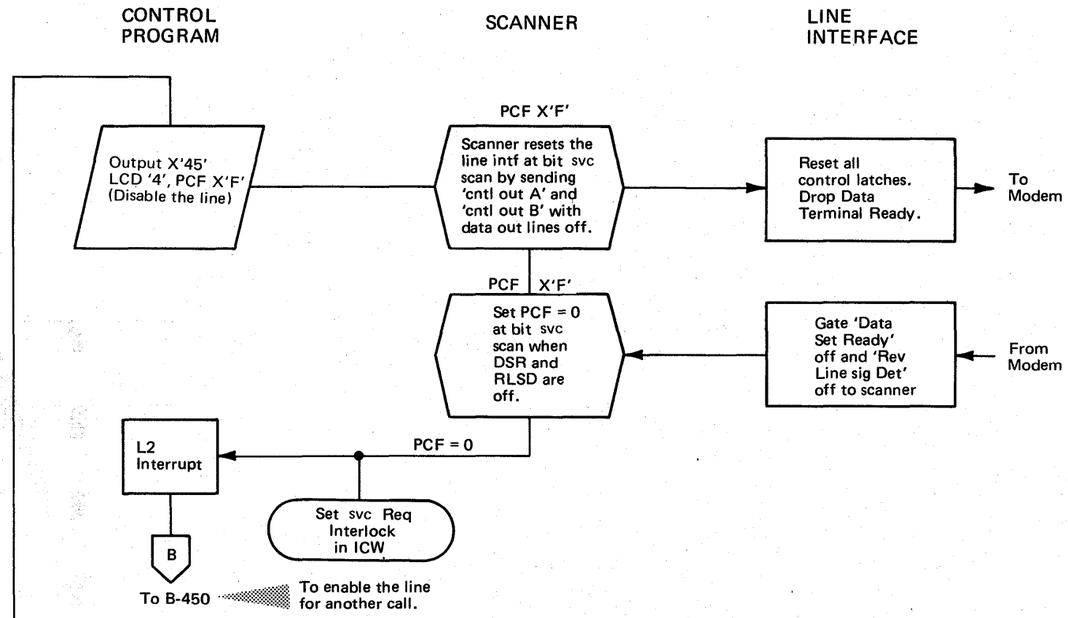
2741 TYPE TERMINAL OPERATION

Note: This operation uses automatic answer on a full-duplex switched network.

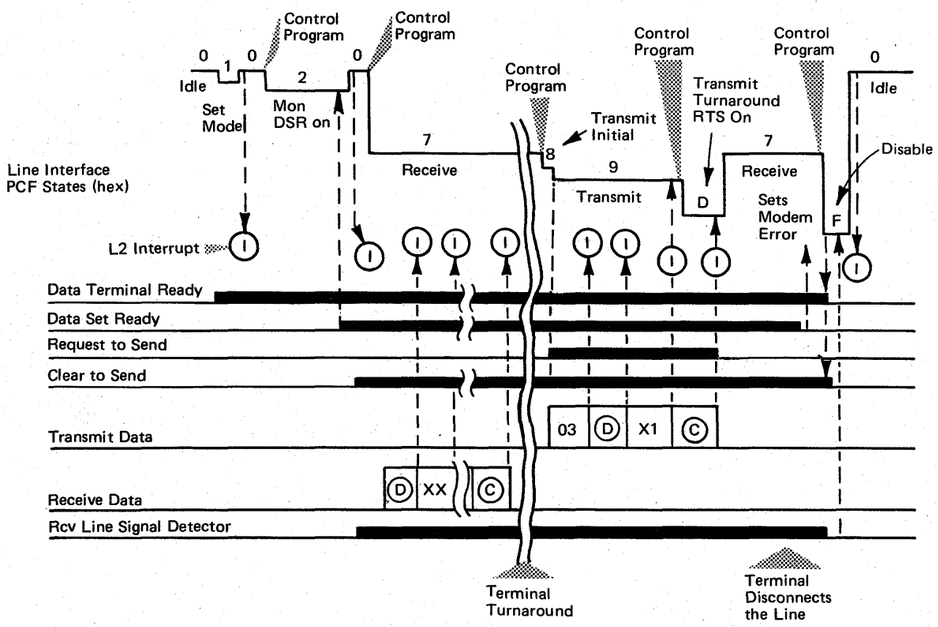


2741 TYPE TERMINAL OPERATION, PART 2



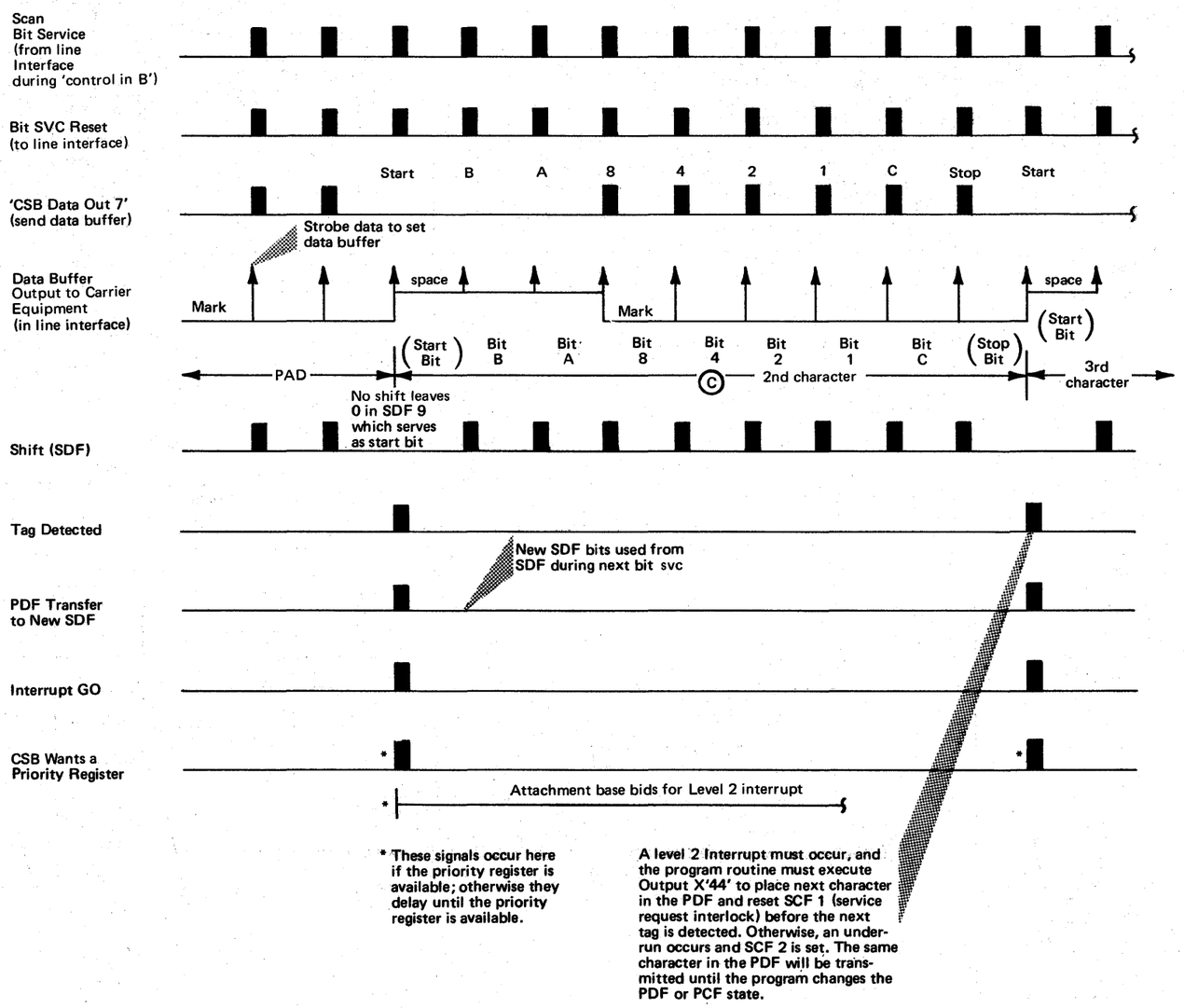


START-STOP OPERATION: AUTOMATIC ANSWER ON A FULL-DUPLEX SWITCHED NETWORK



START-STOP TRANSMIT SEQUENCE

See B-480 for details associated with this sequence.



START-STOP TRANSMIT DETAILS

This example uses LCD = 4 (start-stop 9/7—7 data bits, 1 start bit, and 1 stop bit).

The scanner holds 'CSB data out 7' (send data buffer) at the mark level while CTS (clear to send) is off (TA311). 1 While CTS is off, 'SDF direct' regenerates the data in the SDF and 'shift' is inhibited (TA211).

When CTS turns on, the scanner sets PCF = 9 (TA831). 2 State 9 becomes the active PCF state at the next bit service request for that interface address. The scanner then:

- Removes the mark hold and sends the bit in SDF 9 to the LIB at 'bit service request' time (TA311). 3
- Shifts SDF 0-9 under control of 'bit service request'. 4 During this shift, the scanner:

  —Inhibits 'SDF direct'.

  —Places a zero in SDF 0. 5

The scanner detects the transmit tag during 'gated bit service' when SDF 0-9 contains all zeros (TA261). 6 The scanner:

- Checks the 'modem receive space' line during 'control in C' for an active level. If the line is active, the scanner sets SCF 0 (receive break). SCF 0 on prevents setting SCF 1 (service request interlock) (TA121). This check occurs for every character transmitted.
- Sends the start bit for the Ⓒ to the LIB. 7
- Brings up 'SS xmt xfer' that gates the PDF contents to the SDF (TA231). 8 During this PDF to SDF transfer, the scanner:

  —Sets SDF 2 for the transmit tag (also supplies the mark for the stop bit). The LCD state determines where and how many stop bits are set in the SDF (See the accompanying diagrams). 9

  —Forces SDF 0-1 to zero (also under control of the LCD state). 10

- Inhibits 'shift' to prevent shifting the new character in the SDF (TA211).
- Brings up 'interrupt go' (TA831) that:

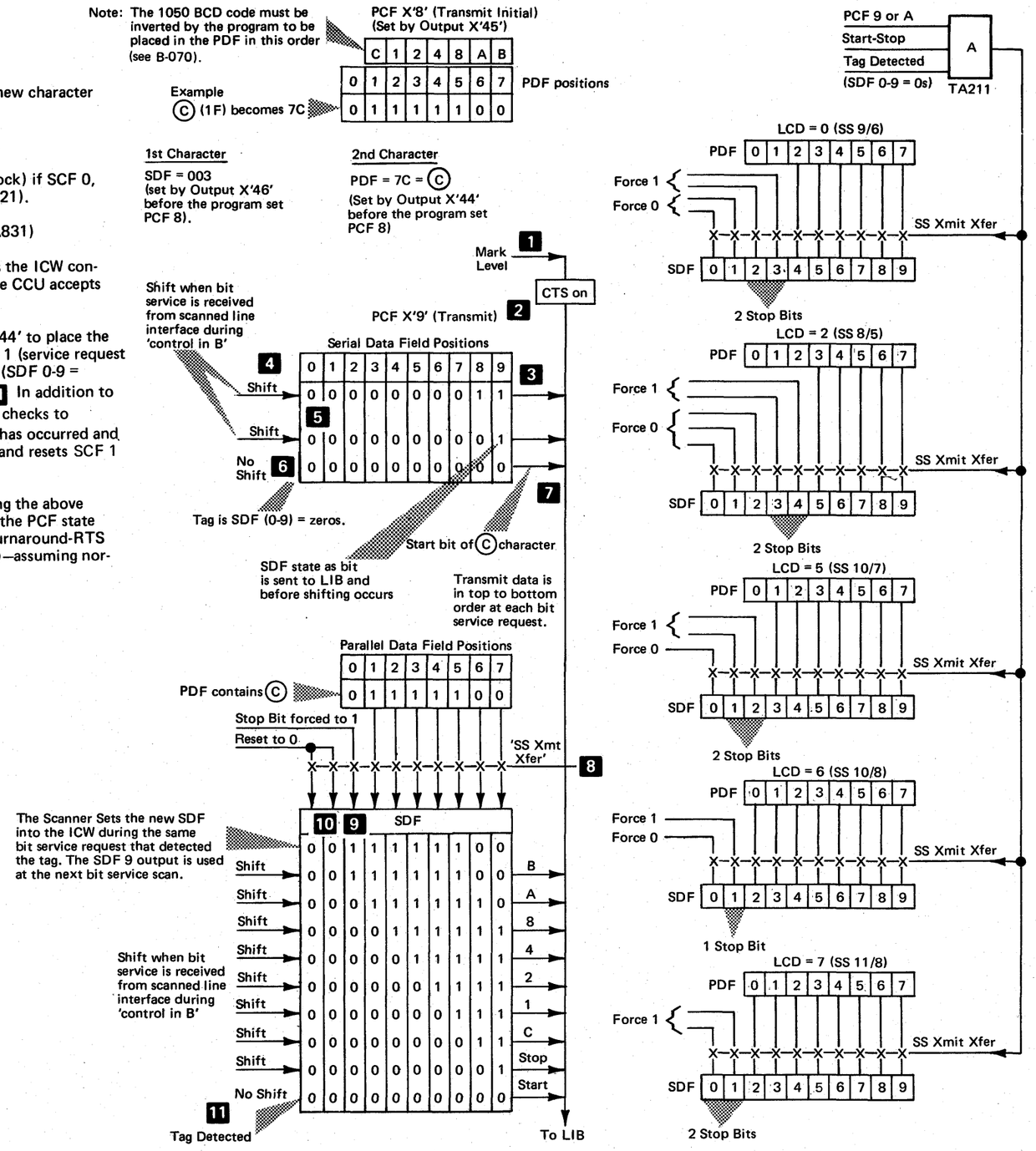
  —Sets SCF 1 (service request interlock) if SCF 0, SCF 2, or SCF 3 are not set (TA121).

  —Causes a L2 interrupt request (TA831)

  —Brings up 'fetch buffer' that gates the ICW content to the input register when the CCU accepts the L2 interrupt (CX001).

The control program executes an Output X'44' to place the next character in the PDF, and to reset SCF 1 (service request interlock). The scanner detects transmit tag (SDF 0-9 = zeros) for each character sent to the LIB. 11 In addition to the action previously described, the scanner checks to ensure that SCF 1 is off. If on, an underrun has occurred and the scanner sets SCF 2 (overrun/underrun), and resets SCF 1 (TA121).

The scanner sends characters to the LIB using the above sequence until the control program changes the PCF state to (1) B (prepare to turn), (2) C (transmit turnaround-RTS off), or (3) D (transmit turnaround-RTS on)—assuming normal operation.



START-STOP RECEIVE DETAILS

Note: Example uses LCD = 4 (start-stop 9/7— 7 data bits, 1 start bit, and 1 stop bit)

The scanner monitors the received data for a start bit (space) at bit service request time when the PCF state is 'receive' and the SDF is empty. The scanner inhibits 'shift' until the start bit is detected. At this time, the scanner inserts a tag bit in SDF 2 **1** .

The scanner detects tag when SDF 9 = 1 at bit service scan **2** .

When tag is detected, the scanner:

- Inhibits shift (TA211) **3** .
- Checks the stop bit in the B data 5 position for a mark level (TA121).

  —If stop bit is at a space level, the scanner sets SCF 0 to 1 (stop bit error).

- Checks for overrun (TA121).

  —If SCF 1 (service request interlock) is on, the scanner sets SCF 2 (overrun), and resets SCF 1.

- Generates 'receive transfer' that:

  —Causes '7 bit xfer' of SDF contents to the PDF (TA711) **4** .

  — Inhibits 'PDF direct' (0-7). This forces PDF 0 to zero, and inhibits the regeneration of the old PDF (TA731).

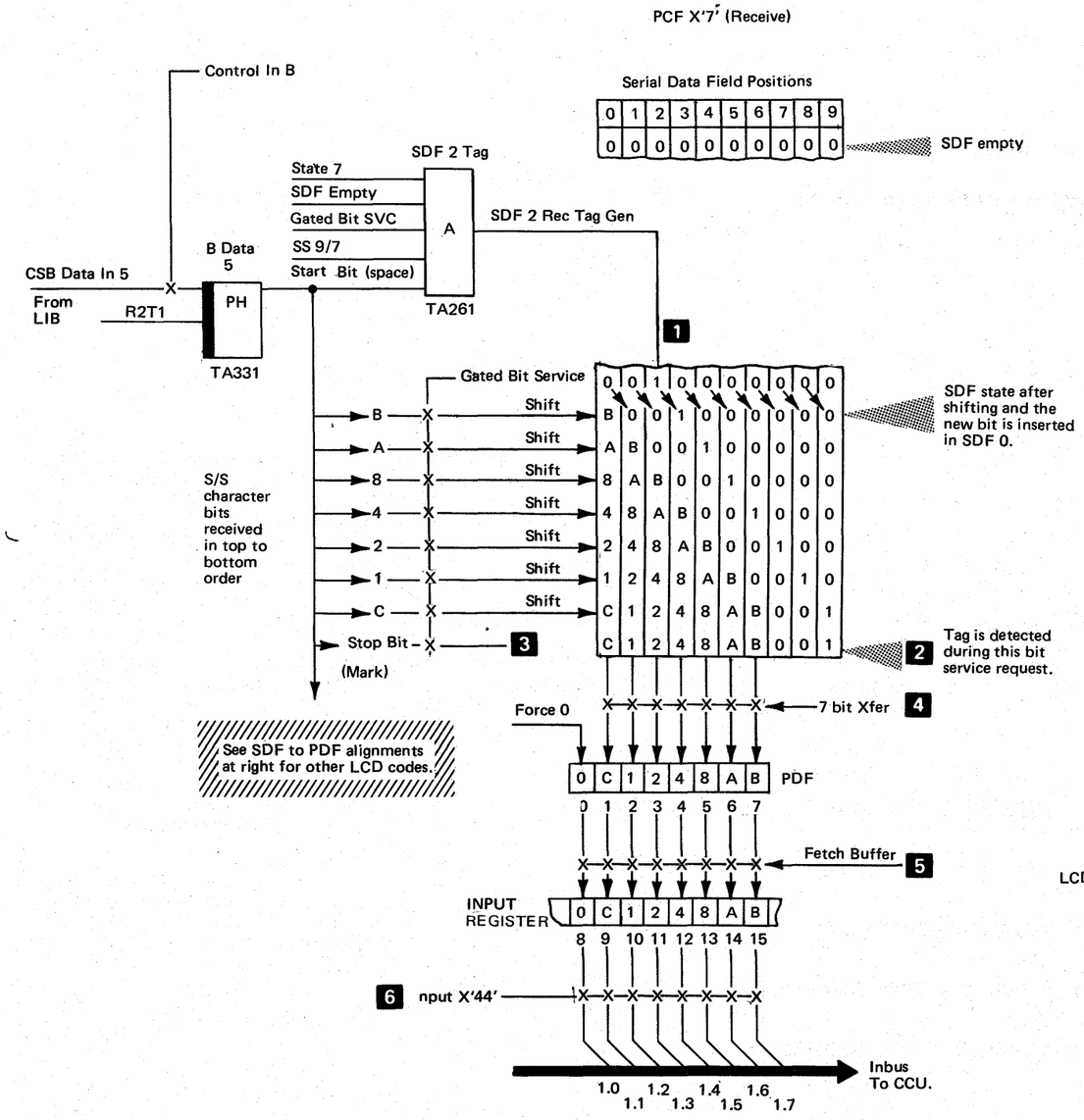
- Brings up 'interrupt go'. This causes:

  —A L2 interrupt request (TA831).

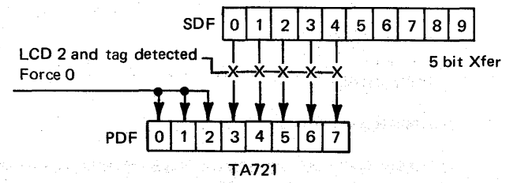
  —'Fetch buffer' that gates the ICW content to the input register (CX001) **5**

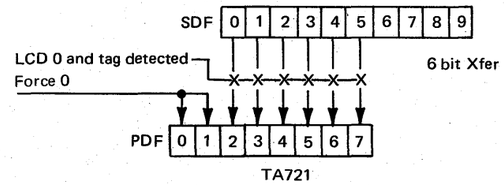
The control program executes Input X'44' to obtain ICW bits 0-15. **6**

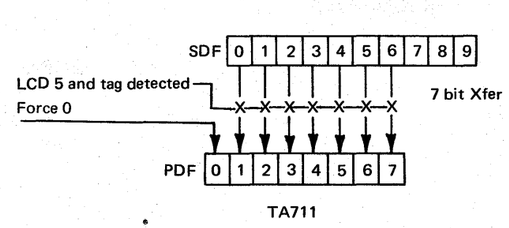
The same sequence occurs for each character received.

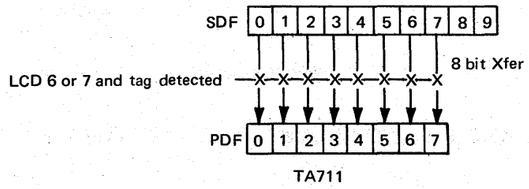


START-STOP SDF TO PDF TRANSFERS BY LCD CODES.









DIAL OPERATION

See B–510 for a flow chart of this dial operation.

The following sequence outlines a suggested procedure which may be taken to perform a dialing function.

Lower Level Disabled Code (L2 Masked)

Address the *autocall interface* and execute Input X'45' to input SDF bits 0-7. DLO must be inactive to proceed with the dial operation (If DLO is active either a dial operation has already been started, the line interface has not been disabled and has auto answered an incoming call, or a failure has occurred). If the IR bit is on, reset it by executing Output X'46'. Set the PCF state to X'4'. (Monitor Call ACR, COS, PND) to cause the CRQ latch to set in the autocall interface, and initiate a timeout.

Address the associated *line interface*. Set the PCF to X'0' (NO-OP), set SDF to turn DTR on, and set the PCF to X'1' (Set Mode).

1. L2 interrupt for associated *Line Interface*
   Reset service request (ICW Bit 1), and set PCF to X'2' (Monitor DSR).

2. First L2 interrupt for *autocall interface* (assuming the timeout did not complete)
   The PCF state should be X'4' (Monitor Call ACR, COS, PND). Input SDF Bits 0-7. Check to see that ACR and COS are OFF and PND is on. Place the proper dial digit in PDF Bits 4-7, and after resetting ICW Bit 1, place the PCF in state X'8' (Valid Digit) to cause the DPR latch to be set in the autocall interface. Reset the IR bit by executing Output X'46', and initiate a timeout.

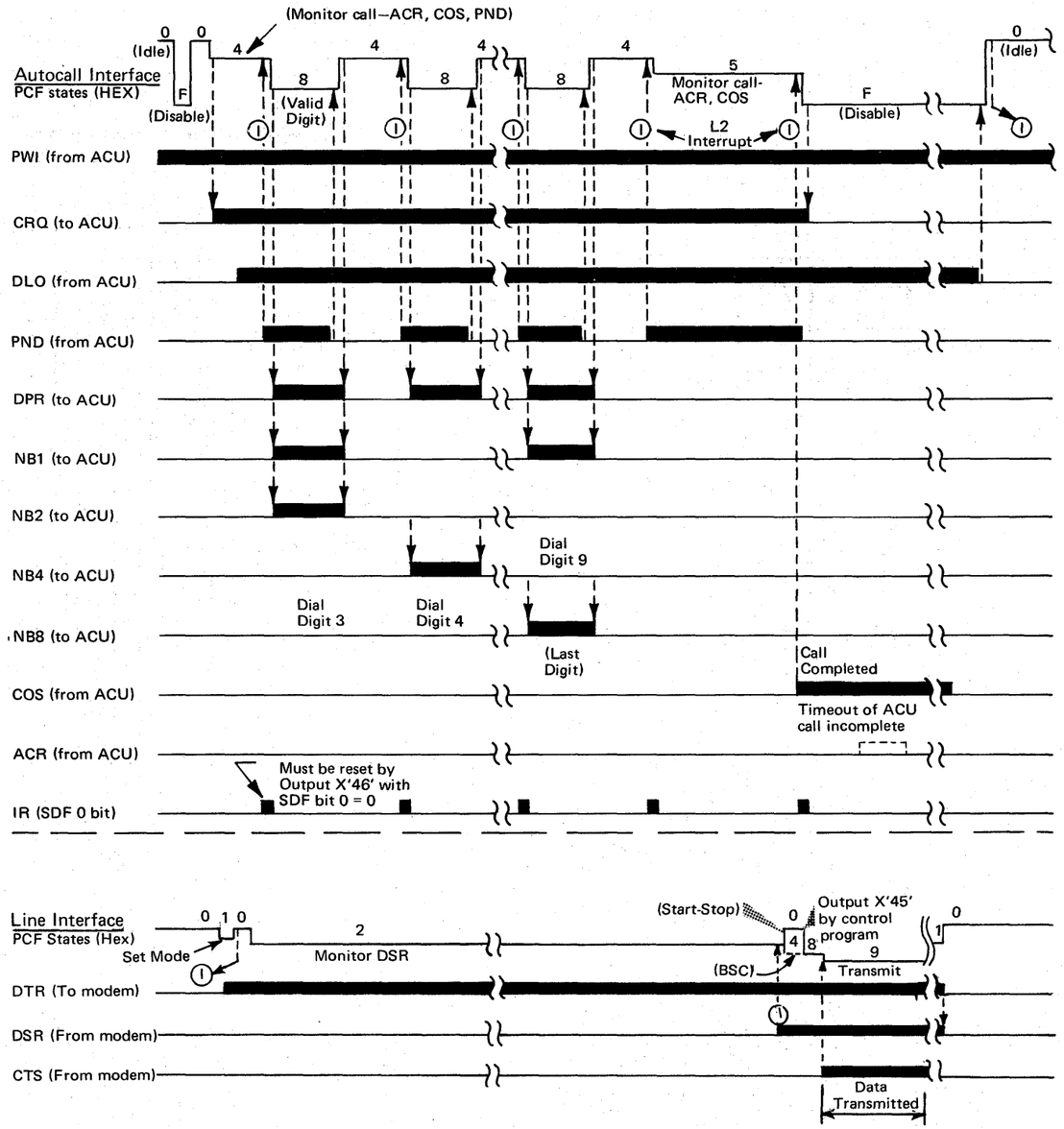
3. L2 interrupts for *autocall interface* for all but the last digit (assuming the timeout did not complete).
   Same action as in 2.

4. Last digit L2 interrupt for *autocall interface* (assuming timeout did not complete).
   The PCF state should be X'4'. Check to see if COS is on.

If COS is off, check to see if ACR is on. If ACR is on, the connection has not been established before ACR timeout and retry is suggested. If ACR and COS are off, reset ICW bit 1, place the PCF in state X'5' (Monitor ACR, COS), reset the IR bit by executing Output X'46', and initiate a timeout. When the next interrupt occurs, either ACR or COS, or both, should be on. If COS is off, appropriate retry action should be taken. If COS is on, the same action should be taken as described in the following paragraph.

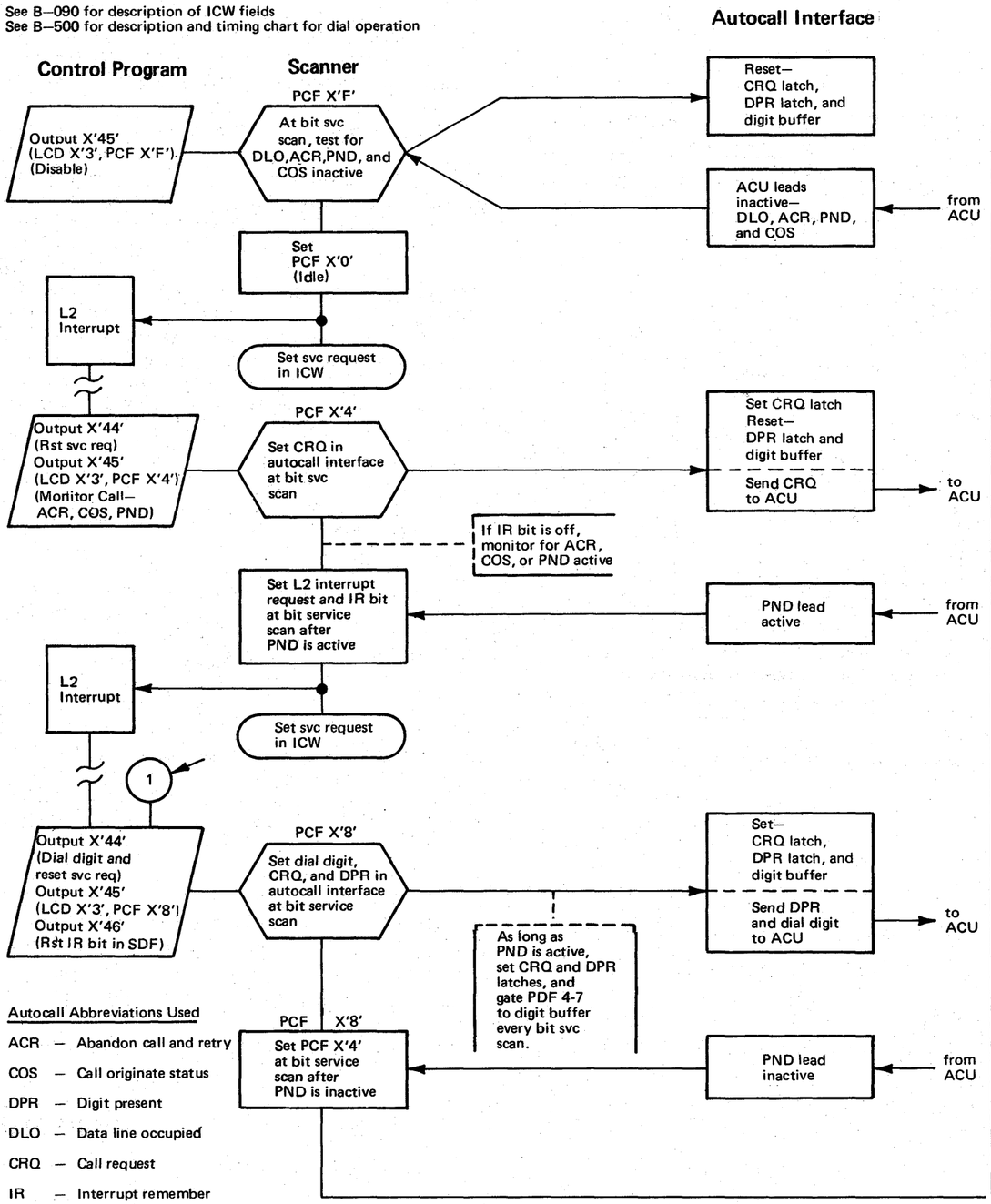
If COS is on, the connection has been established. After resetting ICW Bit 1, place the PCF in state X'F' (Disable) and reset the IR bit by executing Output '46'. When the call completes, a timeout should be initiated on the autocall interface. If DLO, COS, PND and ACR all become inactive, causing the interface to request a L2 interrupt, the timeout should not complete. If the timeout completes before the L2 interrupt, appropriate error recovery procedures should be invoked.

SEQUENCE CHART FOR DIAL OPERATION



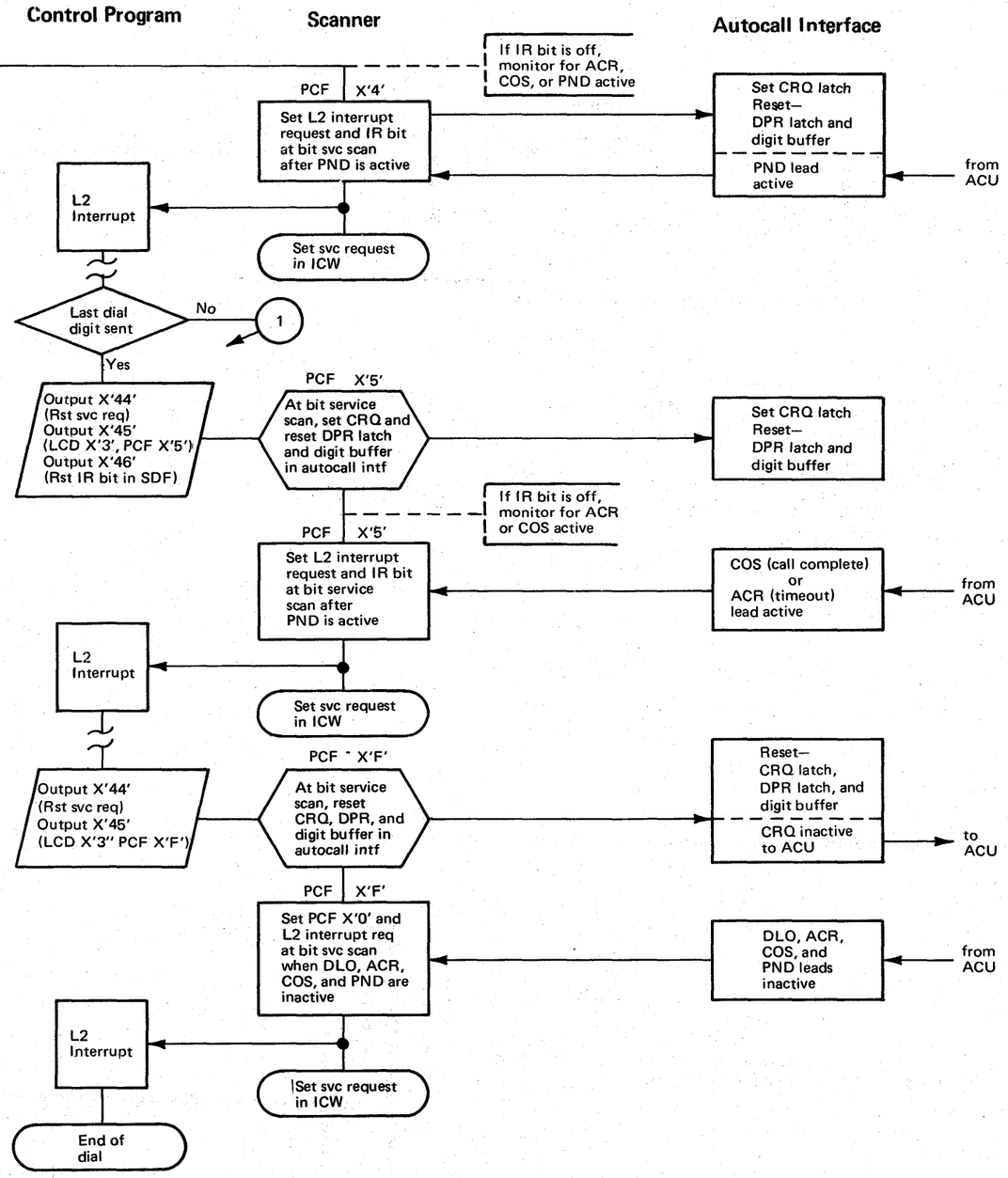
DIAL OPERATION, PART 2

See B–090 for description of ICW fields
See B–500 for description and timing chart for dial operation



Autocall Abbreviations Used

ACR – Abandon call and retry
COS – Call originate status
DPR – Digit present
DLO – Data line occupied
CRQ – Call request
IR – Interrupt remember



DIAGNOSTIC WRAP

DIAGNOSTIC WRAP

- Provides a means of testing and locating troubles in the type 2 scanner line control logic and line-interface receive logic.
- Provides a method of on-line program testing.
- Can be performed on-line without affecting the operation of lines *not* in diagnostic mode.

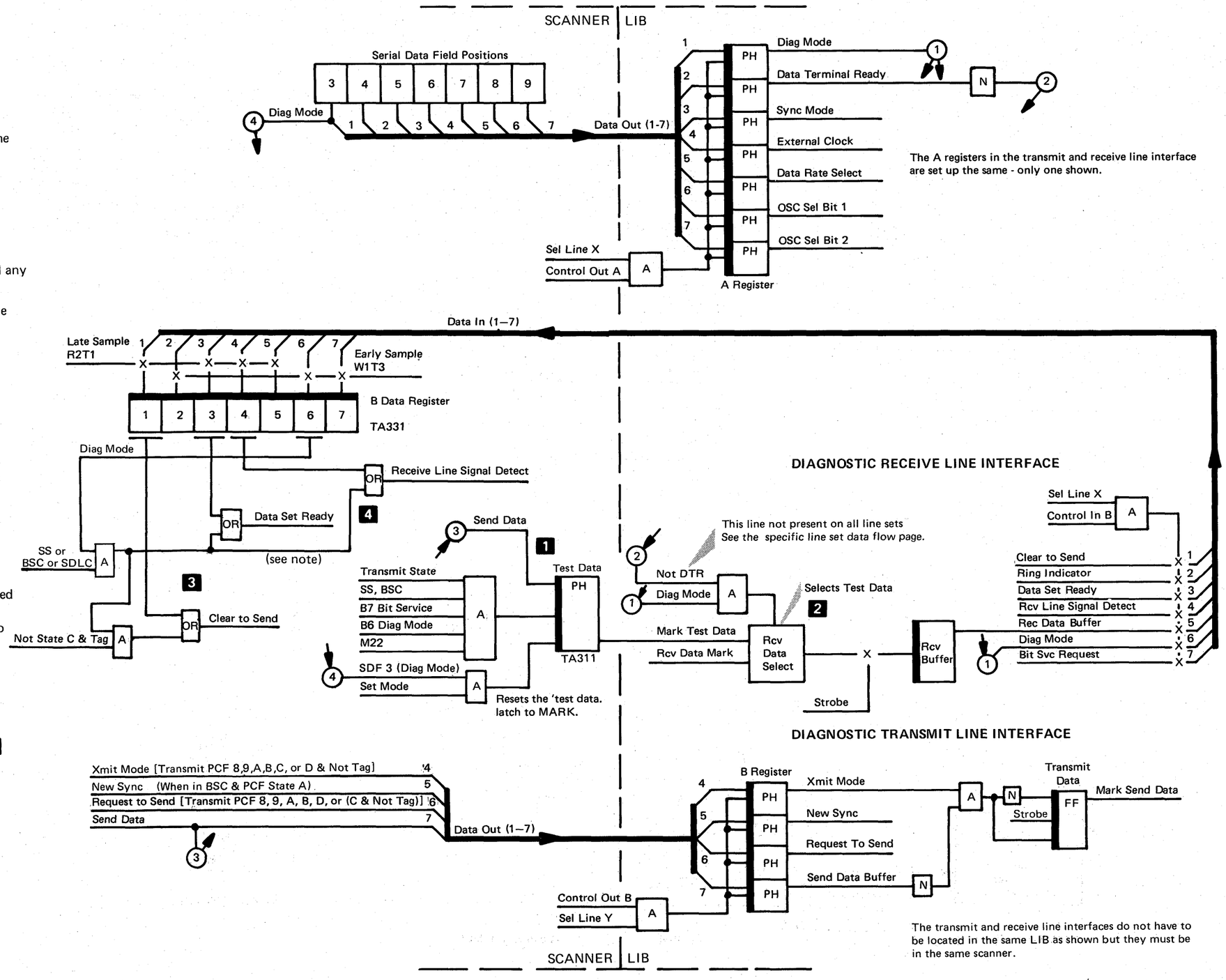
SETUP

- Set any one line interface per type 2 scanner to act as a transmit line and any one or more line interfaces in the same scanner to act as receive lines.
- Set Mode is issued to all diagnostic receive line interfaces first, then to the diagnostic transmit line. The SDF field must be set as follows:
  - –SDF 3 (Diagnostic Mode) - set to 1.
  - –SDF 4 (Data Terminal Ready) - reset to 0.
  - –SDF 5 (Sync Mode) - set to 1 for BSC.
    - reset to 0 for start-stop.
    - Must be 0 for line sets 1A, 1B, 1C, 2A, 3A, 3B, 4A, 4B, 4C, 8A, 9A.
  - –SDF 6 (External Clock) - reset to 0.
  - –SDF 7 (Data Rate Select) - Must be 0 for line sets 1A, 1B, 1C, 2A, 3A, 3B, 4A, 4B, 4C, 8A, 8B, 9A. May be 1 or 0 for all other line sets.
  - –SDF 8 and 9 (Oscillator Select 1,2) - Select an available internal oscillator bit rate. The rate must be the same for the transmit and receive line interfaces.

OPERATION

1. After the Set Modes are issued, the affected line interfaces can be exercised through any sequence of point-to-point or multipoint operations.
2. Data bits clocked to the transmit line interface 'send data buffer' are also clocked into the 'test data' latch in the type 2 scanner. 1
3. As each receive line interface (in diagnostic mode) is scanned, the 'test data' bit is strobed into the 'receive buffer' instead of the 'receive data mark'. 2
4. When the 'diagnostic mode' bit is a 1 in the B data register (B6) during scan time, the type 2 scanner simulates the active states of :
   - 'Data Set Ready' and 'Clear to Send'. Clear to Send is not simulated 3 active if PCF=X'C' and the 'tag' is on (scanner has completely serialized the character in the SDF).
   - 'Receive Line Signal Detect' to turn on ICW bit 4. 4

Note: If a LIB type 5, 6, 7, 8, or 9 is installed, diagnostic mode does not force RLSD to a 1 for any line interface under test in the 3705 and RLSD is controlled by the modem on the line interface. Also diagnostic mode does not force RLSD to a 1 on those 3705s that were built after October 26, 1973.



MODEM WRAP FOR LIBs 5, 6, AND 7

MODEM WRAP TEST (also known as Modem Self Test)

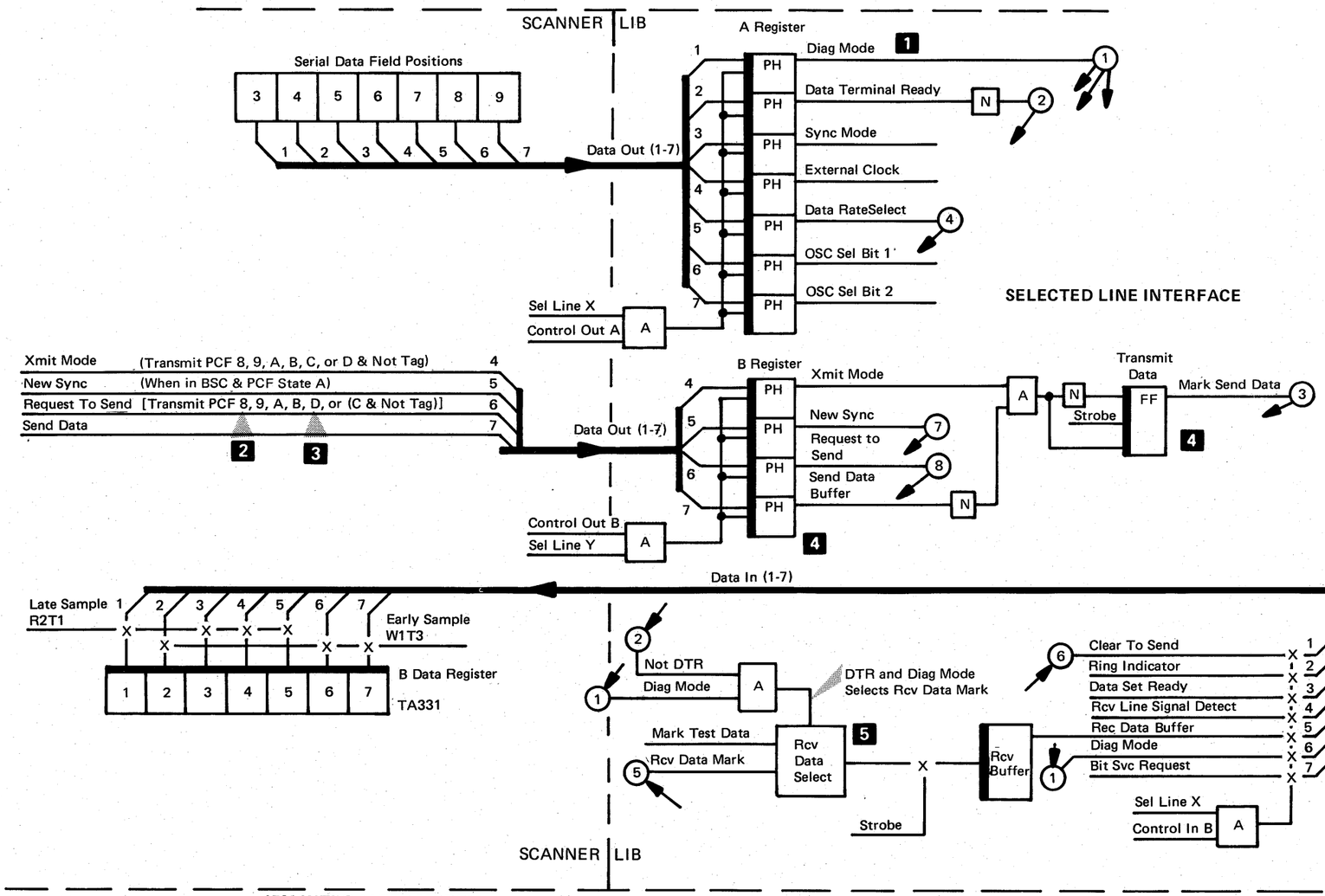
- Provides the capability of testing the modem transmission path of the integrated modems provided by line sets 5A, 5B, 6A, LIB 7, as well as for IBM 3872 or 3875 modems that are externally attached to line set 1D.
- Can be performed on-line without affecting the normal operation of other lines.
- Can not be performed simultaneously with a diagnostic wrap operation for line interfaces attached to the same scanner. It is possible to simultaneously perform diagnostic wrap operations through one scanner and the modem wrap operations through another scanner.

SETUP

1. The line control must be EBCDIC or USASCII—LCD states X'C' or 'D'.
2. Set Mode is issued to the line interface to be tested with the SDF set as follows:
   - SDF 3 (Diagnostic Mode) - set to 1. This sets the diagnostic mode latch in the line interface which picks the modem wrap relay to condition the modem for test. **1**
   - SDF 4 (Data Terminal Ready) - set to 1.
   - SDF 5 (Sync Mode) - set to 1.
   - SDF 6 (External Clock) - set to 1.
   - SDF 7 (Data Rate Select) - set to 0 for 1200 bps. - set to 1 for 2400 bps.
   - SDF 8 and 9 (Oscillator Select 1, 2) - select an internal oscillator whose speed is less than one half the clock speed provided by the IBM modem.
3. Set the PDF and SDF fields to all ones to transmit continuous marks.
4. Set PCF=X'8' (Transmit Initial) to raise Request To Send. **2**
5. When the first interrupt occurs in PCF X'9', set PCF=X,D' to cause the line interface to turn around with Request to Send on. **3** When the turn around is completed, the scanner sets the line interface to PCF X'5' (Monitor Phase-RTS On). A mark bit will be in the 'transmit data' latch and the 'send data' buffer of the line interface. **4**
6. Set PCF=X'7' (receive)

OPERATION

With 'Data Terminal Ready' and 'diagnostic mode' active and the PCF set to receive, the line interface strobes the state of the 'receive data mark' line into the 'receive buffer' instead of the state of the scanner 'test data' latch. **5** All marks should be received because marks are being transmitted continuously to the modem and the modem wrap relay has connected the scrambler back-to-back with the descrambler.



MODEM WRAP TEST FOR LIBs 8, 9, AND 12

- Provides the capability of testing the modem transmission path of the integrated modems provided by line sets 8A, 8B, 12A, 12B, and LIB 9.
- Can be performed online without affecting the normal operation of other lines except the required transmit line.
- Can not be performed simultaneously with a diagnostic wrap operation for line interfaces attached to the same scanner. It is possible to simultaneously perform diagnostic wrap operations through one scanner and the modem wrap operations through another scanner.

SETUP

- Set Mode is issued to both the transmit line interface and the receive line interface to be tested. The SDF is set as follows:

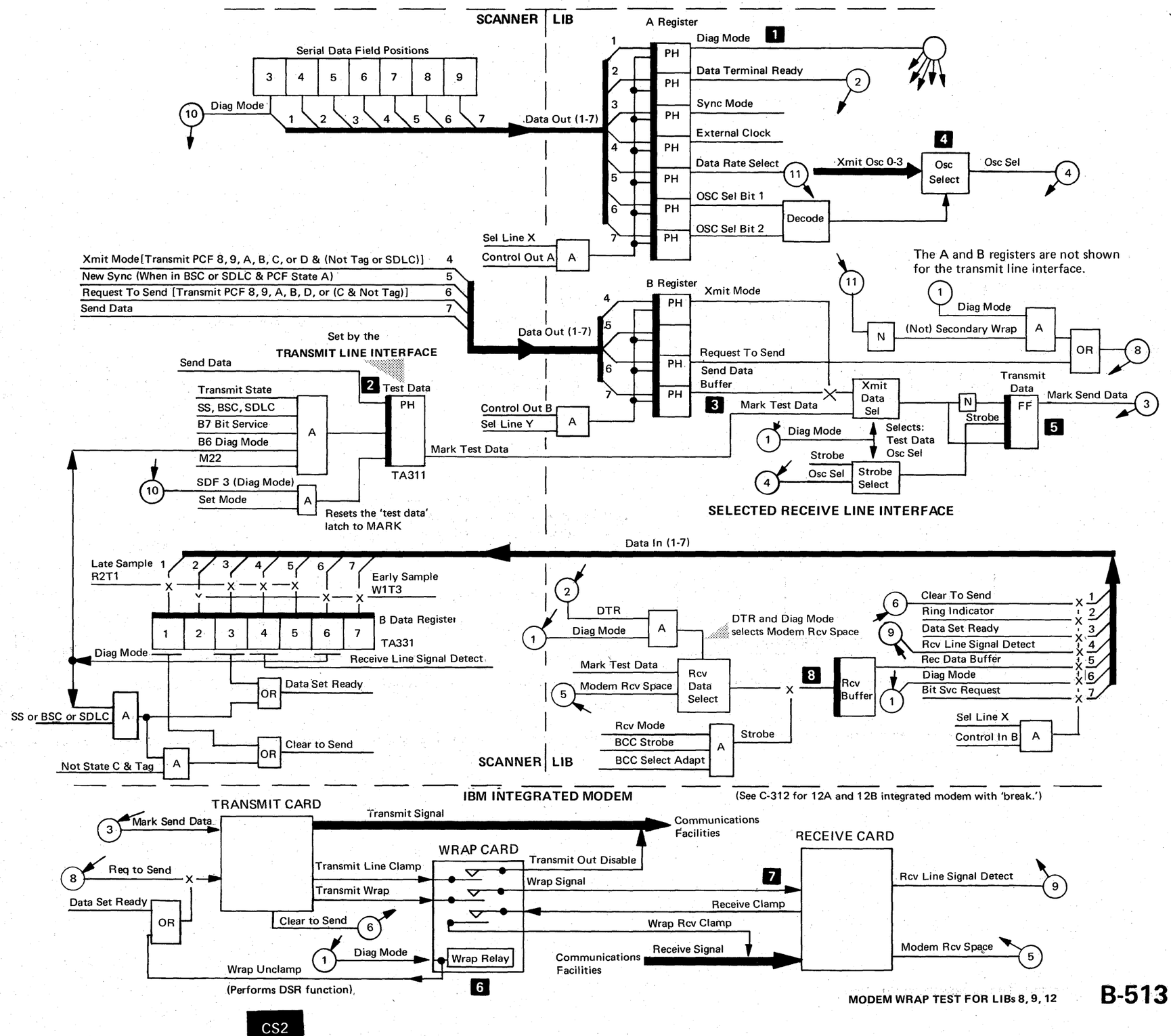
  Receive Line Interface
  - SDF 3 (Diagnostic Mode) - set to 1. This sets the diagnostic mode latch **1** in the line interface which picks the modem wrap relay to condition the modem for test.
  - SDF 4 (Data Terminal Ready) - set to 1. (Enables the break on 12A, 12B)
  - SDF 5 (Sync Mode) - set to 0 for start-stop
    - set to 1 for synchronous
  - SDF 6 (External Clock) - set to 0.
  - SDF 7 (Data Rate Select) - set to 0.
  - SDF 8 and 9 (Oscillator Select 1, 2) - select an internal oscillator.

  Transmit Line Interface
  - SDF 3 (Diagnostic Mode) - set to 1. This sets the diagnostic mode latch in the line interface which sets 'send data' into the scanner 'test data' latch **2** during the scan cycle of the transmit line interface.
  - SDF 4 (Data Terminal Ready) - set to 0.
  - SDF 5 (Sync Mode) - set to 0 for start-stop.
    - set to 1 for synchronous.
  - SDF 6 (External Clock) - set to 0.
  - SDF 7 (Data Rate Select) - set to 0.
  - SDF 8 and 9 (Oscillator Select 1, 2) - select the same internal oscillator as the receive line interface.

- Set PCF=X'7' for start-stop and X'5' for synch. for the LIB 8, 9, or 12 line being tested.
- Set PCF=X'8' (transmit initial) for the transmit line and wait for the CTS and RLSD delays.
- The desired data may now be transmitted by means of the 'test data' latch **2**

OPERATION

Diagnostic mode selects 'mark test data' **3** from the scanner 'test data' latch **2** and the strobe from the selected transmit oscillator **4** to set the 'transmit data' latch. **5** Diagnostic mode picks the wrap relay **6** in the integrated modem which wraps the transmitted data to the receive card. **7** The active states of 'Data Terminal Ready' and 'diagnostic mode' select the 'modem rcv space' output from the receive card. 'Receive mode' gates 'strobe' to set the data into the 'receive buffer', **8**



SDLC TRANSMISSION FRAME FORMAT

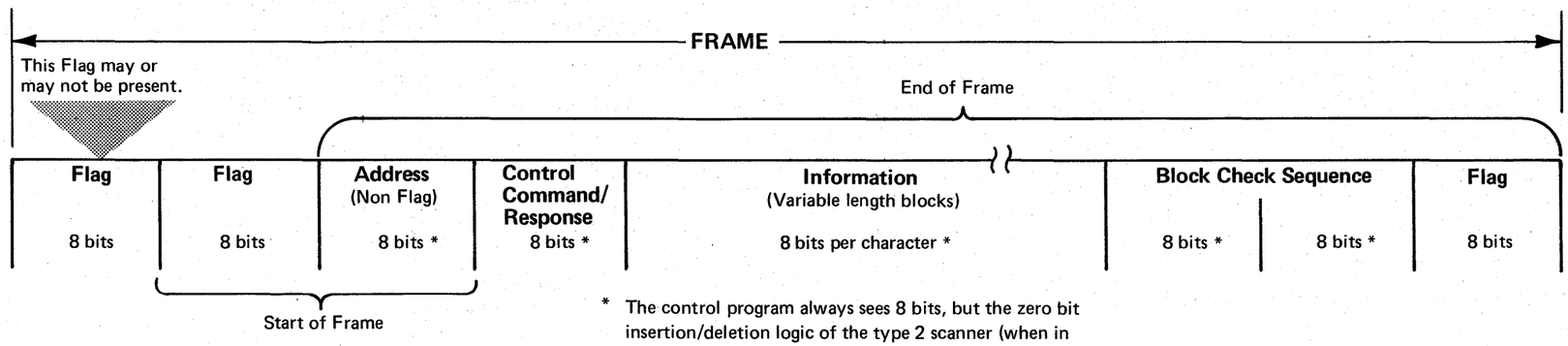
Flag

The Flag is a unique sequence of bits that cannot inadvertently be duplicated in the data stream that is used to signal the start and end of each frame.

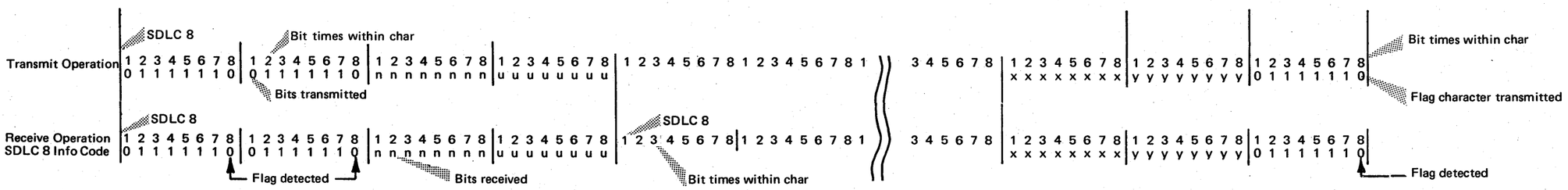
- The bit sequence is 0111 1110
- A minimum of one Flag precedes each frame.
- The End Flag may serve as the Start Flag of the next frame.
- When in receive mode, the scanner continuously monitors the line for the appearance of a Flag.

Abort

The scanner interprets a binary zero followed by a sequence of seven binary ones (01111111) as Abort and sets SCF 0 to a 1 and resets SCF 1 to 0.



* The control program always sees 8 bits, but the zero bit insertion/deletion logic of the type 2 scanner (when in NRZI mode) may transmit/receive more than 8 bits over the communications facility.



SDLC MODES OF OPERATION

NRZI Mode

When receive timing is derived from bit transitions in the data, the transmission technique is inherently sensitive to transitionless data; a series of consecutive binary one bits or binary zero bits. The zero bit insertion technique, to preclude the appearance of Flag sequences within the frame, assures that sequences of consecutive one bits longer than 5 will not occur in the transmission, except for the transmission of the Flag (6 ones) or the Abort (7 ones). In order to prevent the occurrence of extended periods of transitionless data due to consecutive zero bits, zero complemented differential coding (NRZI) is used when SDLC transmission utilizes non-synchronous type modems, equivalent free standing modems, or synchronous modems with data derived clocks.

The control program sets ICW bit 44 (NRZI control) when transmission is to occur in NRZI mode.

Transmit Operation
When transmitting in NRZI mode, the scanner:

- Complements the state of the 'send data' ('CSB data out 7') line to the 'send data' buffer in the selected line interface to transmit a zero bit.
- Does not change the state of the 'send data' line to transmit a 1 bit. This results in continuous transitions (one per bit service request) in the event of consecutive zero bits and no transitions for the case of consecutive one bits.
- Holds the 'send data' line to a steady binary on (Mark) level when PCF state X'8' (initial transmit) is active.
- Sets PCF X'9' (transmit normal) when Clear To Send becomes active and begins transmitting the bit synchronizing pattern, Flag sequences, data, and so forth.

Receive Operation
When receiving in NRZI mode, the scanner:

- Makes the new bit a complement of the 'last line state' if the 'receive data buffer' receives a 1 (Mark).
- Makes the new bit the same as the 'last line state' if the 'receive data buffer' receives a 0 (Space).

When a 6th binary one is received, the scanner inspects the next data bit and if it is a binary zero, the total combination (0111 1110) is the Flag. The scanner recognizes the Flag character and automatically changes from PCF X'5' (monitor Flag) to PCF X'6' (receive info-inhibit data interrupts) to monitor for a non Flag character. The scanner recognizes the 'start of frame' when a Flag character is followed by an eight-bit non-Flag character and automatically changes the PCF state from X'6' to X'7'.

The Flag should be detected on the normal boundary. The following chart shows the predicted position of the Flag bits in the SDF at the time the Flag should be detected. If the flag is detected at other than this configuration of the tag bit, the scanner sets SCF 2 bit to 1.

Flag Detect Predicted Position

	SDLC Code	New Bit Pos.	SDF Positions 0 1 2 3 4 5 6 7 8 9
Normal boundary	8	0	1 1 1 1 1 1 0 0 0 1*

*Receive Tag bit

The bits in the shaded area are the remaining Flag bits when the Flag should be detected (see B-520) with the last 0 bit received in the new bit position. The 1* is the receive Tag bit shifted right.

When 'end of frame' is sensed by the control program, the control program performs a block check.

Non-Synchronous Communication Channel Bit Synchronous Requirements

When business machine clocking is being used and the remote clock is not in phase (for example - half duplex operation or the first transmission following a line turnaround) the first two characters must be X'100' and X'00' respectively. The first two characters transmitted are X'00'; the 1 bit in the initial character X'100' is not transmitted but is used as the tag bit. These two characters, in conjunction with the NRZI encoder, provide the remote business machine 16 transitions for clock synchronization. When using modem clocking or the remote clock is in bit phase, these two leading characters are not required.

Zero Bit Insertion/Deletion

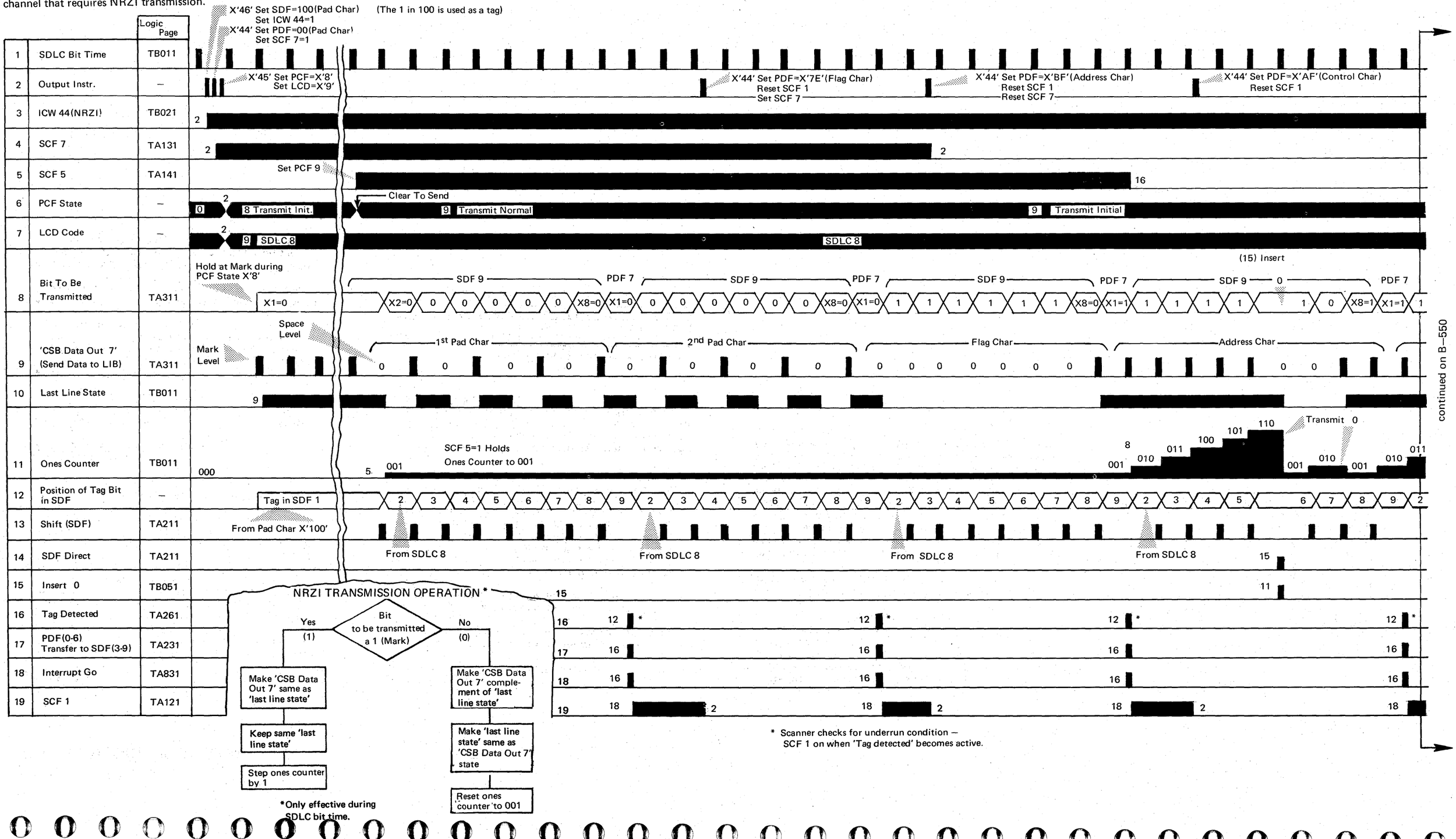
Transmit Mode
The scanner monitors the sequence of transmit data bits and when a consecutive sequence of 5 binary ones is noted, the scanner automatically inserts a binary zero bit before transmitting the next data bit. This includes the transmission of block check characters. Thus there will never be a consecutive sequence of transmitted binary one digits exceeding 5 within the frame except the Flag or Abort.

Receiving Mode
The scanner monitors the stream of received data bits and inspects the bit following any consecutive sequence of 5 binary one bits. If this bit is a binary zero, the scanner deletes it from the data stream.

SDLC TRANSMIT SEQUENCE

This example is for a non synchronous type communication channel that requires NRZI transmission.

		Logic Page
1	SDLC Bit Time	TB011
2	Output Instr.	–
3	ICW 44(NRZI)	TB021
4	SCF 7	TA131
5	SCF 5	TA141
6	PCF State	–
7	LCD Code	–
8	Bit To Be Transmitted	TA311
9	'CSB Data Out 7' (Send Data to LIB)	TA311
10	Last Line State	TB011
11	Ones Counter	TB011
12	Position of Tag Bit in SDF	–
13	Shift (SDF)	TA211
14	SDF Direct	TA211
15	Insert 0	TB051
16	Tag Detected	TA261
17	PDF(0-6) Transfer to SDF(3-9)	TA231
18	Interrupt Go	TA831
19	SCF 1	TA121

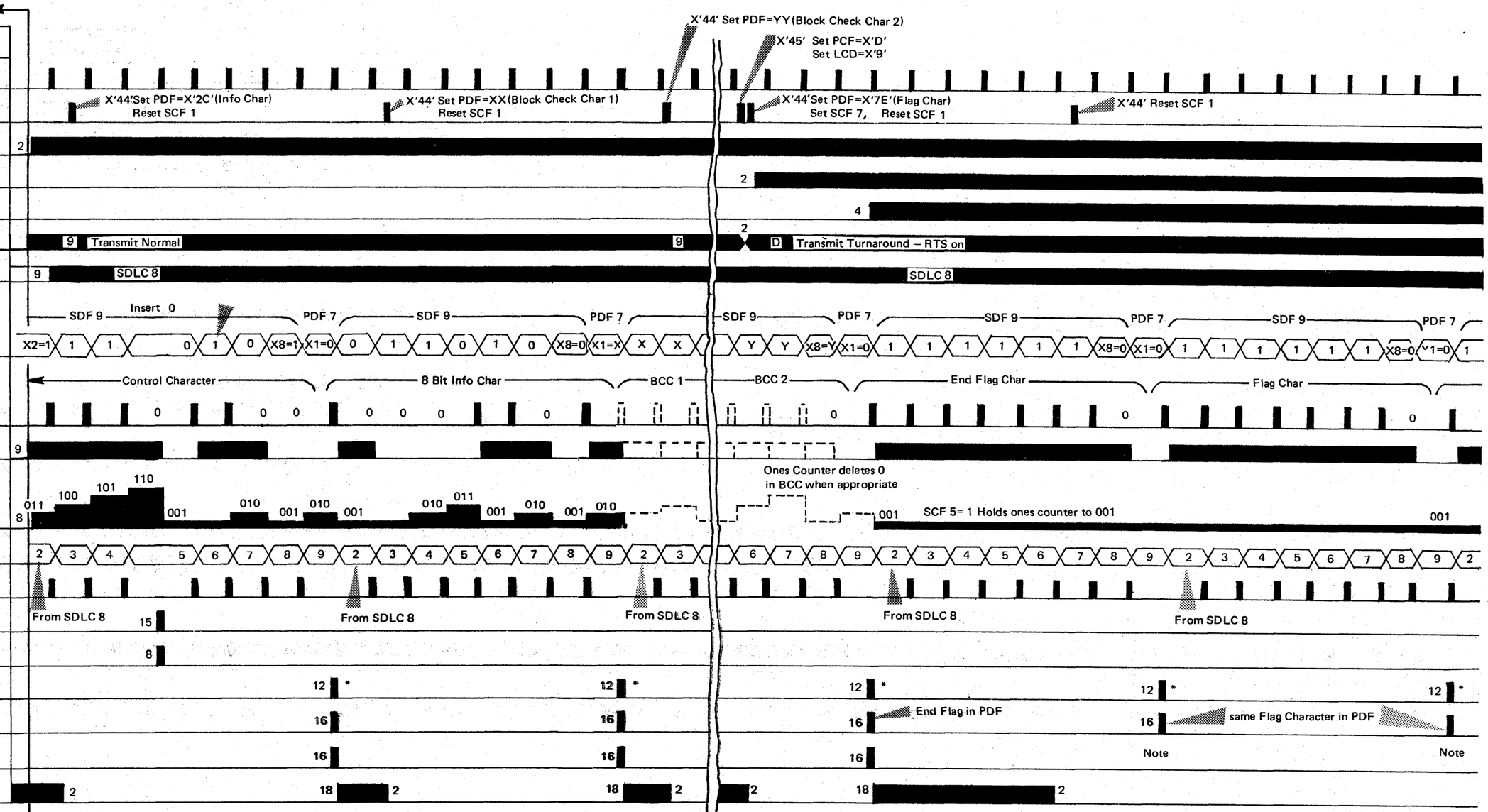


continued on B–550

SDLC TRANSMIT SEQUENCE, PART 2

continued from B-540

		Logic Page
1	SDLC Bit Time	TB011
2	Output Instruction	–
3	ICW 44(NRZI)	TB021
4	SCF 7	TA131
5	SCF 5	TA141
6	PCF State	–
7	LCD Code	–
8	Bit To Be Transmitted	TA311
9	'CSB Data Out 7' (Send Data to LIB)	TA311
10	Last Line State	TB011
11	Ones Counter	TB011
12	Position of Tag Bit in SDF	–
13	Shift (SDF)	TA211
14	SDF Direct	TA211
15	Insert 0	TB051
16	Tag Detected	TA261
17	PDF (0-6) Transfer To SDF (3-9)	TA231
18	Interrupt Go	TA831
19	SDF 1	TA121

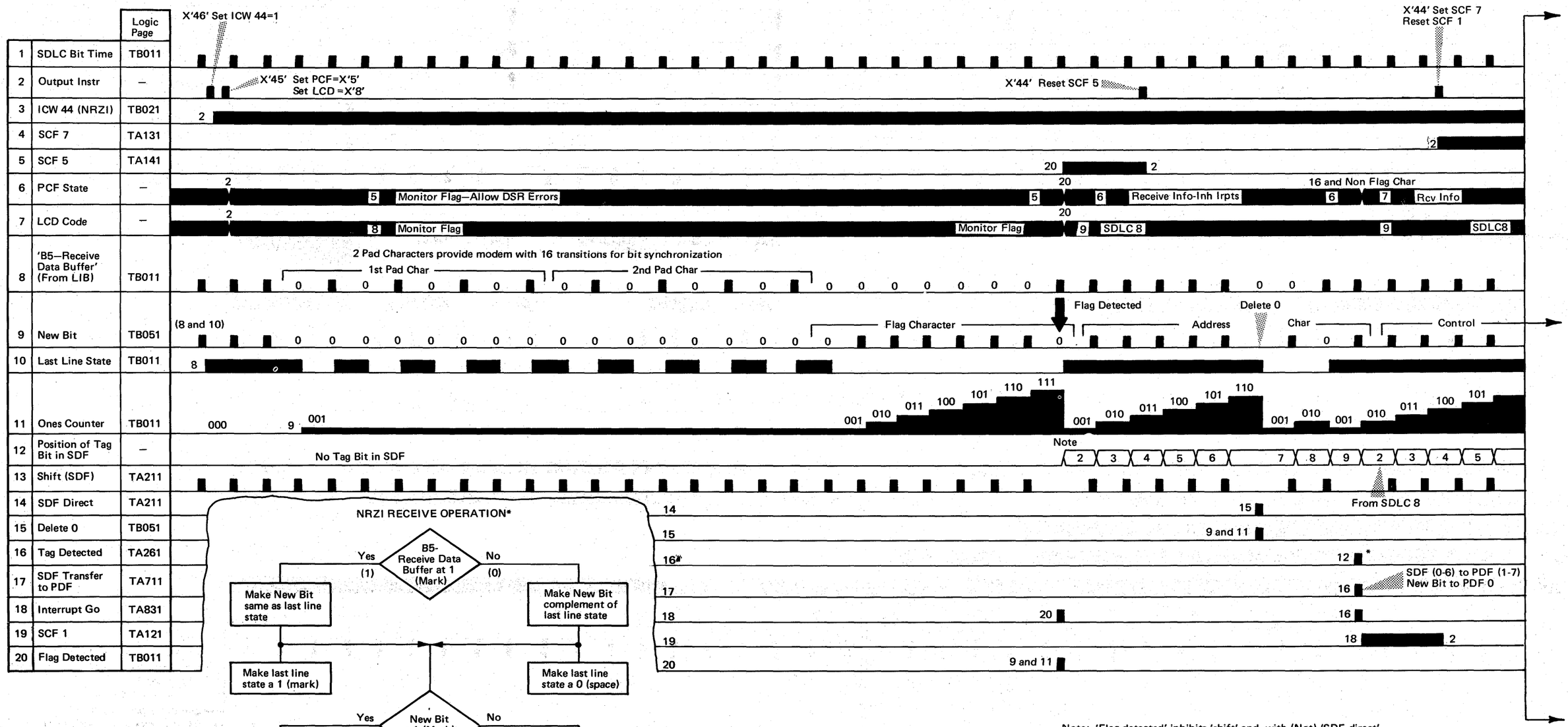


* Scanner checks for underrun condition— SCF 1 on when 'Tag detected' becomes active.

Note: When in PCF state X'D', the scanner continuously serializes the Flag Character to the line interface without further interrupts until the service routine ends it – normally by setting PCF X'9'. This PCF state sequence is used for duplex operation where this SDLC transmit operation occurs on a low order line interface address while the corresponding receive operation occurs on a high order line interface address.

SDLC RECEIVE SEQUENCE

This example is for a non-synchronous type communication channel that requires NRZI receiving. The characters received are those transmitted in the sequence shown on B-540.



NRZI RECEIVE OPERATION*

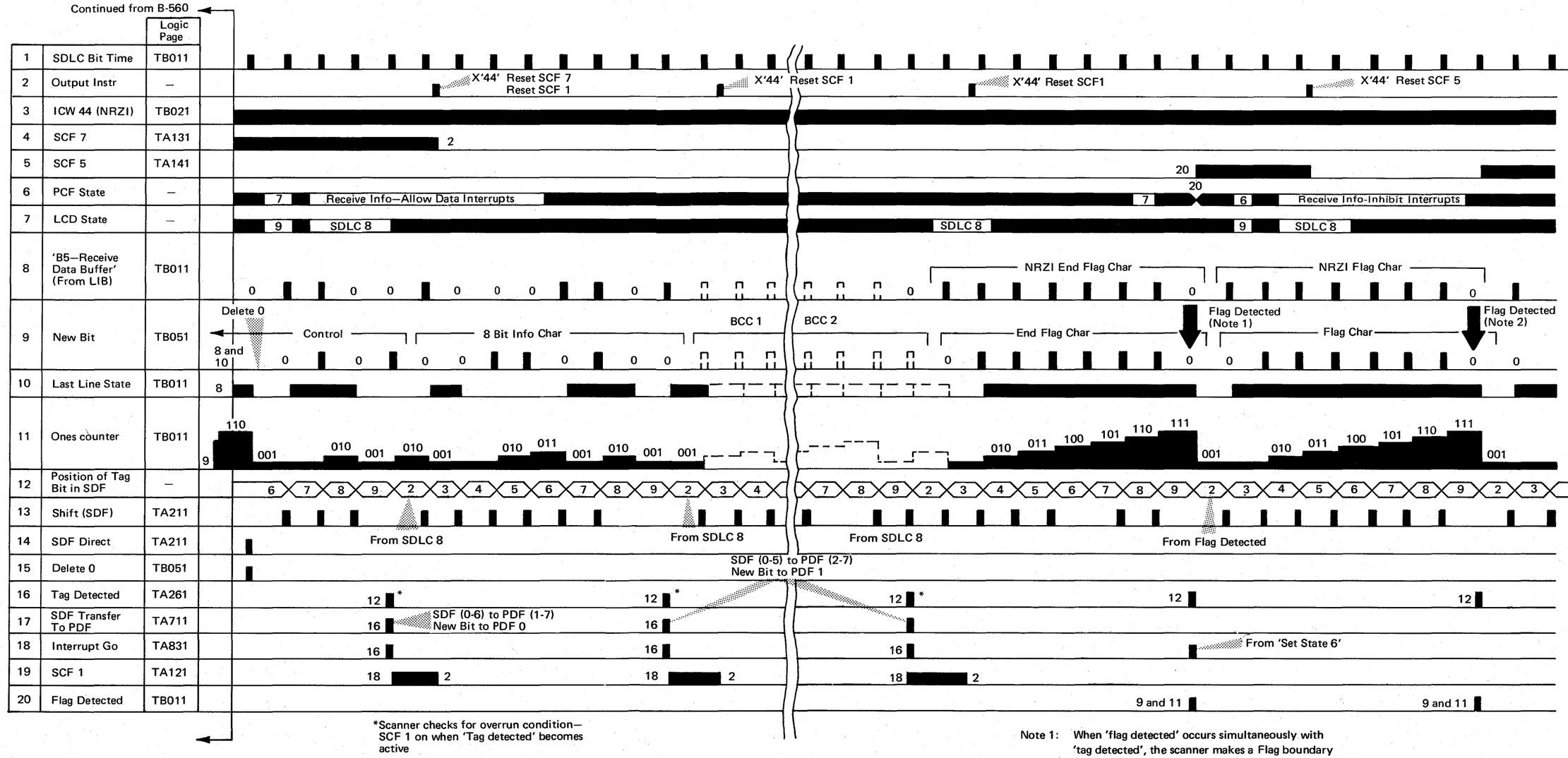
*Scanner checks for overrun condition—SCF 1 on when 'Tag detected' becomes active.

Note: 'Flag detected' inhibits 'shift' and, with (Not) 'SDF direct', resets the SDF to zeros and inserts the receive Tag bit in SDF 2. The scanner does not make a Flag boundary check in PCF state X'6'

*Only effective during SDLC bit time.

SDLC RECEIVE SEQUENCE, PART 2

Continued from B-560



*Scanner checks for overrun condition—SCF 1 on when 'Tag detected' becomes active

Note 1: When 'flag detected' occurs simultaneously with 'tag detected', the scanner makes a Flag boundary check in PCF state X'7' but does not check the overrun condition, therefore, SCF 2 on would indicate a Flag boundary check-not an overrun condition. The SDF does not transfer the Flag char to the PDF.
'Flag detected' inhibits 'shift' and, with (Not) 'SDF direct', resets the SDF to zeros and inserts the receive Tag bit in SDF 2.

Note 2: When 'Flag detected' occurs simultaneously with 'Tag detected', the overrun condition is not checked. The scanner does not make a Flag boundary check in the PCF state X'6'. The SDF does not transfer the Flag char to the PDF.

LIB-Lins Set Configuration Chart

Line Interface Address On LIB	Partition Within LIB	Line Set Type: LIB Type 1 — 1A-Low Speed External Modem	1B-Low Speed Duplex External Modem	1C-Low Speed Local Attachment	1D-Low Speed External Modem	1D-Medium Speed External Modem	1D-Low Speed Duplex External Modem	1D-Medium Speed Duplex External Modem	1D-Low Speed Local Attachment	1D-Medium Speed Local Attachment	1E - Auto Call Unit	1F-Medium Speed Local Attachment	1G-High Speed External Modem	1GA - High Speed External Modem	1H-Medium Speed Duplex External Modem	1J - External Mil std 188 Modem	1K-CCITT V.35 Interface	1N Medium Speed CCITT X.21 Interface Half-Duplex Nonswitched	1N High Speed CCITT X.21 Interface Half-Duplex Nonswitched	1N Medium Speed CCITT X.21 Duplex Nonswitched	1N High Speed CCITT X.21 Interface Duplex Nonswitched	1R-Medium Speed CCITT X.21 Duplex Switched	1R High Speed CCITT X.21 Interface Duplex Switched	1S - Common Carrier 56000 bps Attachment	1T - High Speed Duplex External Modem	1TA - High Speed Duplex External Modem	1U - High Speed Duplex CCITT V.35 Interface	1W - High Speed Local Attachment CCITT V.35 Interface	1Z - High Speed Local Attachment Duplex CCITT V.35 Interface
0 / 1	1	X / X	T / R	X / X	X / X	X / X	T / R	T / R	X / X	X / X	A / A	X / X	X / *	X / *	T / R	X / *	X / *	X / X	Y / *	T / R	T / *	T / R	T / *	X X / X *	T / *	T / *	T / *	X / *	T / *
2 / 3	2	X / X	T / R	X / X	X / X	X / X	T / R	T / R	X / X	X / X	A / A	X / X	X / *	X / *	T / R	X / *	X / *	X / X	Z / *	T / R	R / *	T / R	R / *	X / *	R / *	R / *	R / *	X / *	R / *
4 / 5	3	X / X	T / R	X / X	X / X	X / X	T / R	T / R	X / X	X / X	A / A	X / X	X / *	– / –	T / R	X / *	X / *	X / X	Y / *	T / R	T / *	T / R	T / *	X / *	T / *	– / –	T / *	X / *	T / *
6 / 7	4	X / X	T / R	X / X	X / X	X / X	T / R	T / R	X / X	X / X	A / A	X / X	X / *	– / –	T / R	X / *	X / *	X / X	Z / *	T / R	R / *	T / R	R / *	X / *	R / *	– / –	R / *	X / *	R / *
8 / 9	5	X / X	T / R	X / X	X / X	X / X	T / R	T / R	X / X	X / X	A / A	X / X	X / *	– / –	T / R	X / *	X / *	X / X	Y / *	T / R	T / *	T / R	– / –	X / *	T / *	– / –	T / *	X / *	T / *
A / B	6	X / X	T / R	X / X	X / X	X / X	T / R	T / R	X / X	X / X	A / A	X / X	X / *	– / –	T / R	X / *	X / *	X / X	Z / *	T / R	R / *	T / R	– / –	X / *	R / *	– / –	R / *	X / *	R / *
C / D	7	X / X	T / R	X / X	X / X	X / X	T / R	T / R	X / X	X / X	A / A	X / X	X / *	– / –	T / R	X / *	X / *	X / X	Y / *	T / R	T / *	T / R	– / –	X / *	T / *	– / –	T / *	X / *	T / *
E / F	8	X / X	T / R	X / X	X / X	X / X	T / R	T / R	X / X	X / X	A / A	X / X	X / *	– / –	T / R	X / *	X / *	X / X	Z / *	T / R	R / *	T / R	– / –	X / *	R / *	– / –	R / *	X / *	R / *

Note: Line sets 1A, 1B, 1C, 1F, and 1H are no longer available for the IBM 3705. The functions these line sets provided are now performed by line set 1D. The cables provided by IBM for the 1D line set depend on the type of communications terminal and its intended use. Refer to *IBM Remote Communications Multiplexers and Terminals Installation Manual—Physical Planning* (GA27-3006) or *IBM Input/Output Equipment Installation Manual—Physical Planning: System/360, System/370, 4300 Processors* (GC22-7064) for information on cables.

Note: If the line speed is 40,800 bps or greater and this line set is serviced by a type 2 scanner, or a type 3 scanner when not using high-speed select, the line set must reside in line address positions 0, 2, 4, or 6. If the line set is serviced by a type 3 scanner and high-speed select is used for speeds of 40,800 bps or greater, the line set may be installed in line address positons 0, 2, 4, 6, 8, A, C, or E.

to note under 1G, 1J, 1K and 1S

to note under 1T and 1U

Note: If the line speed is 40,800 bps or greater and this line set is serviced by a type 2 scanner, or a type 3 scanner when not using high-speed select, the line set must reside in line address positons 0 or 4. If the line set is serviced by a type 3 scanner and high-speed select is used for speeds of 40,800 bps or greater, the line set may be installed in line address positions 0, 4, 8, or C.

Legend

Symbol	Meaning
X / X	Denotes a pair of addresses used for a two line interface line set if installed.
A / A	Denotes a pair of addresses used for a two autocall interface line set if installed.
–	Denotes an unused address for this line set.
X / *	Denotes a pair of addresses required for this line set if installed. * is an unused address.
T / R	Denotes a pair of addresses used for a single duplex data line set if installed. Low order addresses are transmit addresses. High order addresses are receive addresses.
X	Denotes an address used for a single line interface line set if installed.
X / A	Denotes a pair of addresses used for a single line interface line set with ACO if installed. A is the auto call interface address for ACO.
T / * / R / *	Denotes four addresses required for this line set. These line sets use two line-interfaces cabled into a single modem. The line sets must have adjacent addresses. The transmit address must be the low order address. The receive address must be the high order address. * is an unused address.
Y / * / Z / *	Denotes a pair of addresses for this line set. * is an unused address.

LIB'S AND LINE SETS (PART 2)

LIB-Line Set Configuration Chart

Line Interface Address On LIB	Partition Within LIB	Line Set Type	LIB Type 2	LIB Type 3		LIB Type 4			LIB Type 5		LIB Type 6	LIB Type 7	LIB Type 8		LIB Type 9	LIB Type 10	LIB Type 11	LIB Type 12	
			2A-Telegraph Single Current	3A - Limited Distance Type 1 Line Adapter - 2 wire	3B - Limited Distance Type 1 Line Adapter - 4 wire	4A-Limited Distance Type 2 Line Adapter	4B - Leased Line, Line Adapter - 2 wire	4C - Leased Line, Line Adapter - 4 wire	5A - 2400 bps Leased Pt-Pt Integrated Modem	5B - 2400 bps Leased Multipoint Control, Integrated Modem	6A - 2400 bps Switched Network Integrated Modem	2400 bps Switched Network Integrated Modem w/ ACO	8A - 1200 bps Leased Integrated Modem	8B - 1200 bps Switched Network Integrated Modem	9A - 1200 bps Switched Network Integrated Modem w/ ACO	10A - 1200 bps Leased Duplex Data Integrated Modem	11A - 2400 bps Leased Pt-Pt Duplex Data Integrated Modem	11B - 2400 bps Leased Multipoint, Control, Duplex Data Integrated Modem	12A - 1200 bps Leased Integrated Modem w/Bi-directional Interrupt Signal	12B - 1200 bps Switched Integrated Modem w/Bi-directional Interrupt Signal
0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	T	T	T	X	X
1		X	X	X	X	X	X	X	–	A	X	X	A	R	R	R	X	X	
2	2	X	X	X	X	X	X	X	X	–	X	X	X	T	T	T	X	X	
3		X	X	X	X	X	–	–	–	–	X	X	A	R	R	R	X	X	
4	3	X	X	X	–	–	–	–	–	–	X	X	–	T	–	–	–	–	
5		X	X	X	–	–	–	–	–	–	X	X	–	R	–	–	–	–	
6	4	X	X	X	–	–	–	–	–	–	–	–	–	T	–	–	–	–	
7		X	X	X	–	–	–	–	–	–	–	–	–	R	–	–	–	–	
8	5	X	X	X	–	–	–	–	–	–	–	–	–	T	–	–	–	–	
9		X	X	X	–	–	–	–	–	–	–	–	–	R	–	–	–	–	
A	6	X	X	X	–	–	–	–	–	–	–	–	–	T	–	–	–	–	
B		X	X	X	–	–	–	–	–	–	–	–	–	R	–	–	–	–	
C	7	X	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
D		X	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
E	8	X	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
F		X	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	

Equivalent IBM		
Line Set Type		External Modem
3705	3704	
5A	1L	3872
5B	1M	3872
6A	1P	3872
LIB 7	1Q	3872
8A	8A	
8B	8B	
9A	LIB 9	
10A	10A	
11A	1X	3872
11B	1Y	3872
12A	8C	
12B	8D	

3705 Line Set Type	Works With IBM				Communication Facility
	Line Set Type		External Modem	Sync Terminal Equipped With (note 3)	
	3705	3704			
5A	5A	1L	3872 (note 2)	2400 bps Integrated Modem	Point-to-point
5B (control)			3872 (note 1)	2400 bps Integrated Modem (tributary)	Multipoint
6A, LIB 7	6A, LIB 7	1P, 1Q	3872 (note 2)	2400 bps Integrated Modem	Switched
8A	8A	8A		1200 bps Integrated Modem	Pt-to-pt or Multipoint
8B, 9A	8B, 9A	8B, LIB 9		1200 bps Integrated Modem	Switched
10A	10A	10A		1200 bps Integrated Modem	Duplex
11A	11A	1X	3872(Note 2)	2400 bps Integrated Modem	Duplex Point-to-Point
11B (control)			3872(Note 1)	2400 bps Integrated Modem (tributary)	Duplex Multipoint
12A				1200 bps Int. Modem (Note 4)	Two-Wire Point-to-Point
12B				1200 bps Int. Modem (Note 4)	Switched

Notes:

1. The modem must have receive and transmit equalization (tributary modem). Line sets with receive and transmit equalization are not offered on the 3704 and 3705.
2. The 3872 must be equipped similarly to the line set types indicated.
3. The terminal's integrated modem must be equipped similarly to the line set types indicated.
4. The break capability of line sets 12A and 12B is only supported for start-stop operation at 300 bps.

LIB'S AND LINE SETS, PART 3

Lines are attached to the 3705 through LIBs (Line Interface Bases). Twelve different LIB types are available for the 3705 to meet the needs of a wide variety of line and terminal types. Each LIB type operates identically, and is controlled by the communication scanner to which it is attached. The main difference between the LIB types is the physical space required by their associated line sets.

Lines are attached to the LIB through line sets. Each LIB is divided into physical locations corresponding to line addresses. Two line address locations make up a partition. LIB types 1, 3, 4, 5, 8, 11 and 12 can contain multiple line set types, but LIB types 2, 6, 7, 9 and 10 can only contain one line set type. (See the LIB-line set configuration chart on C-000 for the line sets that apply to each LIB.) The line sets associated with a given LIB type may be intermixed and placed in any valid partition with the exception of line sets 1G, 1J, 1K, 1S, 1T and 1U (see note following the LIB-line set configuration chart).

The LIB consists of one MST board, a BCC (bit clock control) card, and an isolation card. The LIB provides the following general functions.

- Drives and terminates all signals from the scanner to the line set interface
- Terminates, logically ORs, and redrives all feedback signals from the line set interfaces to the scanner
- Provides bit clocking
  - Controls bit sampling for lines driven by business machine clocks
  - Causes pseudo bit-service requests for lines driven by external data set clocks during periods when the data set clock is not running
  - Provides signals to monitor the autocall operation for autocall interfaces.

Note: In this manual, INTERNAL CLOCK means business machine provided clock, and EXTERNAL CLOCK means modem provided clock.

HIGH-SPEED LOCAL ATTACHMENT

The high-speed local attachment is a special feature of the 3705-II. It allows communication without modems over directly attached cables connecting two 3705s or a 3705 and batch oriented terminals. Two 3705s can communicate at a line speed of 57,600 bps, and a 3705 can communicate with a terminal at a line speed of 14,400 bps.

LIB TYPE 1

LIB Type 1 provides for the attachment of up to eight of the following line set types in any combination (see C-070).

*Line Set 1A (Low Speed External Modem)**

Provides for the attachment of two half-duplex start-stop leased or switched lines at speeds up to 1200 bps, each of which attaches to an external modem. The control program must condition these line interfaces for business machine clock control.

*Line Set 1B (Low Speed Duplex Data External Modem)**

Provides for the attachment of one full-duplex data start-stop leased or switched line at speeds up to 1200 bps. Line set 1B is a line set 1A where both interfaces share a common external cable for attaching to a single external modem. The control program must condition these line interfaces for business machine clock control.

This line set pair consists of 2 addresses. The low-order address is the transmit line and the high-order address is the receive line.

*Line Set 1C (Low Speed Local Attachment)**

Provides for the local attachment of two half-duplex start-stop terminals at speeds up to 1200 bps by means of IBM provided cables (see C-190). The attached terminals provide standard external data set cables to attach to the external cables which are ordered with the line set. Total cable length to each terminal must not exceed 200 feet. The control program must condition these line interfaces for business machine clock control. No external modems are required.

For terminals such as IBM 2740 Mod 1, 2740 Mod 2, 2741, and 1050.

Line Set 1D.

When installed in the IBM 3705, the 1D line set provides for the attachment of an external modem or the direct attachment of a terminal. The line set may be used at line speeds up to 9600 bps. Mode of operation may be start-stop, binary synchronous (BSC), or synchronous data link control (SDLC). (See Note.)

Note: The cables provided by IBM for the 1D line set depend on the type of communications terminal and its intended use. Refer to *IBM Remote Communications Multiplexers and Terminals Installation Manual—Physical Planning:* (GA27-3006) or *IBM Input/Output Equipment Installation Manual—Physical Planning: System/360, System/370, 4300 Processors* (GC22-7064) for information on cables.

With appropriate cables, the 1D line set in a 3705 can provide for:

1. The direct attachment of two half-duplex IBM terminals at line speeds up 2400 bps. This line set can operate in start-stop mode at line speeds up 1200 bps or in synchronous mode (BSC or SDLC) at line speeds up to 2400 bps. However, line protocols for an individual line set cannot be mixed. Modems are not required. Therefore, the attached communications terminal must provide its own clocking and a standard cable for attachment to each interface cable.
2. The attachment of one start-stop or synchronous (BSC or SDLC) communication line. This line set can operate in start-stop mode at line speeds up to 1200 bps or in synchronous mode at line speeds up to 9600 bps. The 1D line set allows duplex transmission of data over non-switched, 4-wire facilities and provides an EIA RS-232C/CCITT V.24 interface to an external modem. The external modem must provide the clocking required for synchronous operation above 2400 bps and an EIA RS-232C/CCITT V.24 interface for attachment to the communication line.
3. The attachment of two start-stop or synchronous (BSC or SDLC) communication lines. This line set can operate in start-stop mode at line speeds up 1200 bps or in synchronous mode at line speeds up to 9600 bps. The 1D line set allows half-duplex transmission of data over switched or nonswitched facilities and provides an EIA RS-232C/CCITT V.24 interface to an external modem. The external modem must provide an EIA RS-232C/CCITT V.24 interface for attachment to each communication line and the clocking required for synchronous operation above 2400 bps.

Line Set 1E (Auto Call Unit)

Provides two independent interfaces for attachment to external ACUs (automatic calling units). Each interface and attached ACU can be associated by external cabling with any of the line interfaces provided by Line Sets 1A, 1D, or 1G.

*Line Set 1F (Medium Speed Local Attachment)**

Provides for the local attachment of two half-duplex synchronous terminals or devices at speeds up to 2400 bps (limited by internal clock speed) by means of IBM provided cables (see C-190). The control program must condition these line interfaces for business machine clock control. External modems are not required. The attached terminal provides a standard external modem cable to attach to the external cables which are ordered with the line set. The total cable length to each terminal must not exceed 100 feet. The attached terminals must provide their own clocking.

For terminals such as IBM 2270, 2780, and S/360 Mod 20.

Note: The control program must activate the 'data rate select' signal since this signal drives the terminal's 'received line signal detector' circuit.

Line Set 1G (High Speed External Modem)

Provides for the attachment of one half-duplex synchronous line for operation at speeds up to 50,000 bps. This line set has a digital interface for attachment to a switched or leased wideband external modem. The control program must condition this line interface for external clock control.

This line set may not be installed with the Type 1 Communication Scanner and must only reside in LIB position 1.

If the line speed is 40,800 bps or greater and the line set is serviced by a type 2 scanner, or a type 3 scanner when not using high-speed select, the line set must reside in line address positions 0, 2, 4, or 6. If the line set is serviced by a type 3 scanner and high-speed select is used for speeds of 40,800 bps or greater, the line set may be installed in line address positions 0, 2, 4, 6, 8, A, C, or E.

Line Set 1GA (High Speed External Modem)

Provides for the attachment of one synchronous communication line for operation at speeds up to 230,400 bps. It has a digital interface for attachment to a nonswitched wideband external modem.

This line set can be attached only to a LIB Type 1 in a 3705-II. A Type 3HS Communication Scanner is required to operate the 1GA line set at line speeds above 57,600 bps, and no more than two line sets may be attached to a scanner that is conditioned for external clocking.

*Line Set 1H (Medium Speed Duplex External Modem)**

Provides for the attachment of one duplex leased line at speeds up to 9600 bps. Line set 1H is a line set 1D where both interfaces share a common external cable for attaching to a single external modem. The control program may condition these line interfaces for either external clock or business machine clock control (if the speed does not exceed 2400 bps).

This line set pair consists of two addresses. The low-order address is the transmit line and the high-order address is the receive line.

The interface for this line set enables modem tests to be performed.

Line Set 1J (External Mil Std 188 Modem)

Provides for the attachment of one half-duplex line at speeds up to 56,000 bps. The control program may condition this line interface for either external clock control or business machine clock control (if the line speed does not exceed 2400 bps).

If the line speed is 40,800 bps or greater and the line set is serviced by a type 2 scanner, or a type 3 scanner when not using high-speed select, the line set must reside in line address positions 0, 2, 4, or 6. If the line set is serviced by a type 3 scanner and high-speed select is used for speeds of 40,800 bps or greater, the line set may be installed in line address positions 0, 2, 4, 6, 8, A, C, or E. This line set does not include an external cable.

Line Set 1K (CCITT V.35 Interface)

Provides for the attachment of one half-duplex line that has a CCITT V.35 interface to an external modem for use on World Trade communications facilities with speeds up to 48,000 bps. The control program must condition this line interface for external clock control.

*Line sets 1A, 1B, 1C, 1F, and 1H are no longer available for the IBM 3705. The functions these line sets provided are now performed by line set 1D. However, appropriate cables must be attached to the 1D line set. Refer to "Line Set 1D".

LIB'S AND LINE SETS, PART 4

If the line speed is 40,800 bps or greater and the line set is serviced by a type 2 scanner, or a type 3 scanner when not using high-speed select, the line set must reside in line address positions 0, 2, 4, or 6. If the line set is serviced by a type 3 scanner and high-speed select is used for speeds of 40,800 bps or greater, the line set may be installed in line address positions 0, 2, 4, 6, 8, A, C, or E. This line set may not be installed with the Type 1 Communication Scanner.

Line Set 1N (Nonswitched CCITT X.21 Interface)

Provides for the attachment of two half-duplex nonswitched synchronous lines or one duplex nonswitched synchronous line with a CCITT X.21 interface to Data Circuit-Terminations Equipment (DCE). This line set is for use on World Trade communication facilities that can operate at line speeds of 2400, 4800, 9600, or 48,000 bits per second. The 1N line set operates with a Type 2 or Type 3 Communication Scanner only.

Line Set 1R (Switched CCITT X.21 Interface)

Provides for the attachment of one duplex switched synchronous line with a CCITT X.21 interface to Data Circuit-Termination Equipment (DCE). This line set is for use on communication facilities that can operate at line speeds of 2400, 4800, 9600, or 48,000 bps. The 1R line set operates with a Type 2 Communication Scanner only.

Line Set 1S (Common Carrier 56,000 bps Attachment)

Provides for the attachment of one half-duplex line that has a CCITT V.35 interface to an external modem for use in the United States and Canada at speeds at 56,000 bps. The control program must condition this line interface for external clock control. This line set may not be installed with the Type 1 Communication Scanner.

Line Set 1T (High Speed Duplex External Modem)

Provides for the attachment of one duplex synchronous line for operation at speeds up to 50,000 bps. This line set consists of two 1G line sets that share a common external cable for attachment to a switched or leased wideband external modem. The control program must condition the line interfaces for external clock control.

This line set may not be installed with the Type 1 Communication Scanner. It requires two adjacent partitions. If the line speed is 40,800 bps or greater and the line set is serviced by a type 2 scanner, or a type 3 scanner when not using high-speed select, the line set must reside in line address positions 0 or 4. If the line set is serviced by a type 3 scanner and high-speed select is used for speeds of 40,800 bps or greater, the line set may be installed in line address positions 0, 4, 8, or C.

Line Set 1TA (High Speed Duplex External Modem)

Provides for the attachment of one duplex synchronous line that has a digital interface for attachment to an external modem for up to 230,400 bps nonswitched wideband facilities. The control program must condition this line interface for external clock control. This line set can only be attached to a LIB Type 1 in a 3705-II. A Type 3HS Communication Scanner is required to operate the 1TA line set at line speeds above 57,600 bps, and no more than one line set may be attached to a scanner that is conditioned for external clocking.

Line Set 1U (High Speed Duplex External Modem)

Provides for the attachment of one duplex line that has a CCITT V.35 interface. This line is two 1K/1S line sets which share a common external cable for attachment to an external modem for use on communciations facilities at speeds up to 56,000 bps. The control program must condition the line interfaces for external clock control.

This line set may not be installed with the Type 1 Communication Scanner. It requires two adjacent partitions. If the line speed is 40,800 bps or greater and the line set is serviced by a type 2 scanner, or a type 3 scanner when not using high-speed select, the line set must reside in line address positions 0 or 4. If the line set is serviced by a type 3 scanner and high-speed select is used for speeds of 40,800 bps or greater, the line set may be installed in line address positions 0, 4, 8, or C.

Line Set 1W (High Speed Local Attachment)

Provides for the attachment of one half-duplex locally attached line at speeds of 14,400 or 57,600 bps. This line set has a CCITT V.35 interface for attachment to another V.35 interface in a terminal or another 3705 containing a 1K or 1S line set. The control program must condition this line interface for external clock.

Line Set 1Z (High Speed Duplex Local Attachment)

Provides for the attachment of one full duplex locally attached line at speeds of 14,400 or 57,600 bps. This line set consists of two 1W line sets cabled in a local attachment configuration. The line set has a CCITT V.35 interface for attachment to another V.35 interface in a terminal or another 3705 containing a 1U line set. The control program must condition this line interface for external clock.

LIB TYPE 2

LIB Type 2 provides for the attachment of up to eight line sets for telegraph termination (see C-080).

Line Set 2A (Telegraph Single Current)

Provides for the attachment of two telegraph lines at speeds up to 200 bps, each of which can be wired for 20, 40, or 62.5 ma single current termination. The maximum allowable receive distortion is 40 percent. The control program must condition these line interfaces for business machine clock control.

LIB TYPE 3

LIB Type 3 provides for the attachment of up to six of the following line set types in any combination (see C-090).

Line Set 3A (Limited Distance Type 1 Line Adapter—two wire)

Provides for the attachment of two half-duplex start-stop lines at speeds up to 134.5 bps. The line interface includes IBM Limited Distance Type 1 (two wire) Line Adapters. The control program must condition these line interfaces for business machine clock control. No external modems are required. Total wire length of each line may not exceed 4.75 miles. See *Planning and Installation of a Data Communications System Using IBM Line Adapters,* GA24-3435 for more information on this Line Adapter.

Line Set 3B (Limited Distance Type 1 Line Adapter—four wire

Same as 3A except 3B is four wire instead of two wire.

LIB TYPE 4

LIB Type 4 provides for the attachment of up to two of the following line set types in any combination (see C-100).

Line Set 4A (Limited Distance Type 2 Line Adapter)

Provides for the attachment of two half-duplex start-stop lines at speeds up to 600 bps. The line interface hardware includes IBM Limited Distance Type 2 Line Adapters. The control program must condition these line interfaces for business machine clock control. External modems are not required. Total wire length of each line may not exceed 8.25 miles. See *Planning and Installation of a Data Communications System Using IBM Line Adapters,* GA24-3435 for more information on this Line Adapter.

Line Set 4B (Leased Line, Line Adapter—two wire)

Provides for the attachment of two half-duplex start-stop leased lines at speeds up to 600 bps. The line interface hardware includes IBM Leased Line Adapters. The control program must condition these line interfaces for business machine clock control. No external modems are required. See *Planning and Installation of a Data Communications System Using IBM Line Adapters,* GA24-3435 for more information on this Line Adapter.

Line Set 4C (Leased Line, Line Adapter—four wire)

Same as 4B except 4C is four wire instead of two wire.

LIB TYPE 5

LIB Type 5 provides for the attachment of up to two of the following line set types in any combination (see C-101). It may only be installed in the 3705 basic frame; not the expansion frames.

Line Set 5A (2400 bps Leased Point-to-Point Integrated Modem)

Provides for the attachment of one half-duplex synchronous leased line at 2400/1200 bps. The line interface hardware includes an integrated modem with receive equalization that is compatible with an equivalent IBM 3872 modem. The control program must condition this line interface for external clock control because the modem provides the clock pulses. No external modem is required.

Line Set 5B (2400 bps Leased Multipoint, Control, Integrated Modem)

Provides for the attachment of one half-duplex synchronous leased line at 2400/1200 bps. The line interface hardware includes an integrated modem without equalization that is compatible with a tributary IBM 3872 modem. The control program must condition this line interface for external clock control because the modem provides the clock pulses. No external modem is required.

LIB TYPE 6

LIB Type 6 provides for the attachment of up to two Line Set 6A's (see C-102).

Line Set 6A (2400 bps Switched Network Line Integrated Modem)

Provides for the attachment of one half-duplex synchronous switched line at 2400/1200 bps. The line interface hardware includes an integrated switched line modem with auto-answer capability and automatic equalization compatible with a switched network IBM 3872 modem. The control program must condition this line interface for external clock because the integrated modem provides the clock pulses. No external modem is required. This line interface is connected to the switched network through a Data Access Arrangement.

LIB TYPE 7

LIB Type 7 provides a single line set for the attachment of one half-duplex synchronous switched line at 2400/1200 bps with Automatic Call Originate and Auto-Answer (see C-103).

Two interfaces are provided—a line interface and an auto-call interface. The line interface hardware includes an integrated switched-line modem with auto-answer capability and with automatic equalization. The auto call interface hardware includes an IBM Automatic Call Originate (ACO) feature for the modem. The control program must condition the line interface for external clock control because the integrated modem provides the clock pulses. No external modem or Automatic Calling Unit is required. These interfaces are connected to the switched network through an automatic Data Access Arrangement (CBS Data Coupler, for example). LIB Type 7 can only be used with a rotary dial system.

LIB TYPE 8

LIB Type 8 provides for the attachment of up to three of the following line sets in any combination (see C-104).

Line Set 8A (1200 bps Leased Line Integrated Modem)

Provides for the attachment of two half-duplex start-stop leased lines at speeds up to 600 bps or two synchronous leased lines at speeds up to 1200 bps. The line interface hardware includes a 1200 bps Integrated Modem for each interface. The control program must condition these line interfaces for business machine clock control because the modems do not provide clock pulses. No external modems are required.

Line Set 8B (1200 bps Switched Network Integrated Modem)

Provides for the attachment of two half-duplex start-stop switched lines at speeds up to 600 bps or two synchronous switched lines at speeds up to 1200 bps. The line interface hardware includes a 1200 bps Integrated Modem with auto-answer capability for each interface. The control program must condition these line interfaces for business machine clock control because the integrated modems do not provide clock pulses. No external modems are required. Each line interface is connected to the switched network through an automatic Data Access Arrangement (CBS Data Coupler, for example).

LIB TYPE 9

LIB Type 9 provides for the attachment of up to two Line Set 9A's (see C-105).

Line Set 9A (1200 bps Switched Network Integrated Modem with ACO)

Provides for the attachment of one half-duplex start-stop or synchronous switched line at speeds up to 1200 bps with Automatic Call Originate and Auto-Answer. Two interfaces are provided—a line interface and an auto call interface. The line interface hardware includes a 1200 bps Integrated Modem with auto-answer capability. The auto call interface hardware includes an IBM Automatic Call Originate (ACO) feature for the modem. The control program must condition this line interface for business machine clock control because the integrated modem does not provide clock pulses. No external modems are required. These interfaces are connected to the switched network through an automatic Data Access Arrangement (CBS Data Coupler, for example). LIB Type 9 can only be used with a rotary dial system.

LIB TYPE 10

LIB Type 10 provides for the attachment of up to six Line Set 10A's (see C-106).

Line Set 10A (1200 bps Leased Duplex Data Integrated Modem)

Provides for the attachment of one duplex synchronous leased line at speeds up to 1200 bps. The line interface hardware is similar to that of line set 1D but includes a 1200 bps integrated modem. The modem transmitter is board wired to the low order address while the modem receiver is board wired to the adjacent high order address. The control program must condition this line interface for business machine clock control because the modem does not provide clock pulses.

LIB TYPE 11

LIB Type 11 provides for the attachment of up to two of the following line set types in any combination (see C-107). It may only be installed in the 3705 basic frame, not in the expansion frames.

Line Set 11A (2400 bps Leased Point-to-Point Duplex Data Integrated Modem)

Provides for the attachment of one duplex synchronous leased line at 2400/1200 bps. The line interface hardware is similar to that of line set 1D but includes an integrated modem with receive equalization. The modem transmitter is board wired to the low order address while the modem receiver is board wired to the adjacent high order address. The control program must condition this line interface for external clock control because the modem provides the clock pulses.

Line Set 11B (2400 bps Leased Multipoint, Control, Duplex Data Integrated Modem)

Provides for the attachment of one duplex synchronous leased line at 2400/1200 bps. The line interface hardware is similar to that of the line set 1D but includes an integrated modem with no equalization. The modem transmitter is board wired to the low order address while the modem receiver is board wired to the adjacent high order address. The control program must condition this line interface for external clock control because the modem provides the clock pulses.

LIB TYPE 12

LIB type 12 provides for the attachment of up to two of the following lines sets in any combination (see C-108).

Line Set 12A (1200 Leased Integrated Modem with Bi-directional Interrupt Signal)

Provides for the attachment of two two-wire leased lines at speeds up to 1200 bps for start-stop or synchronous half-duplex operation. The line interface hardware has the same functional capabilities as the two-wire line set 8A. However, a bi-directional interrupt signal (break) has been added to each of the two 1200 bps leased integrated modems. This break capability is only supported for start-stop operation. The break operation requires the customer to specify the 'No Echo Suppression' option for the two-wire facility from the common carrier. Line set 12A can be used for communication with the IBM 3767 Communication Terminal (operating in 2741 Line Control) at a line speed of 300 bps using two-wire leased common carrier facilities.

When the break capability is not used, line set 12A functions as a line set 8A and can be used for synchronous half-duplex operation.

The control program must condition these line interfaces for business machine clock control because the modems do not provide clock pulses. No external modems are required.

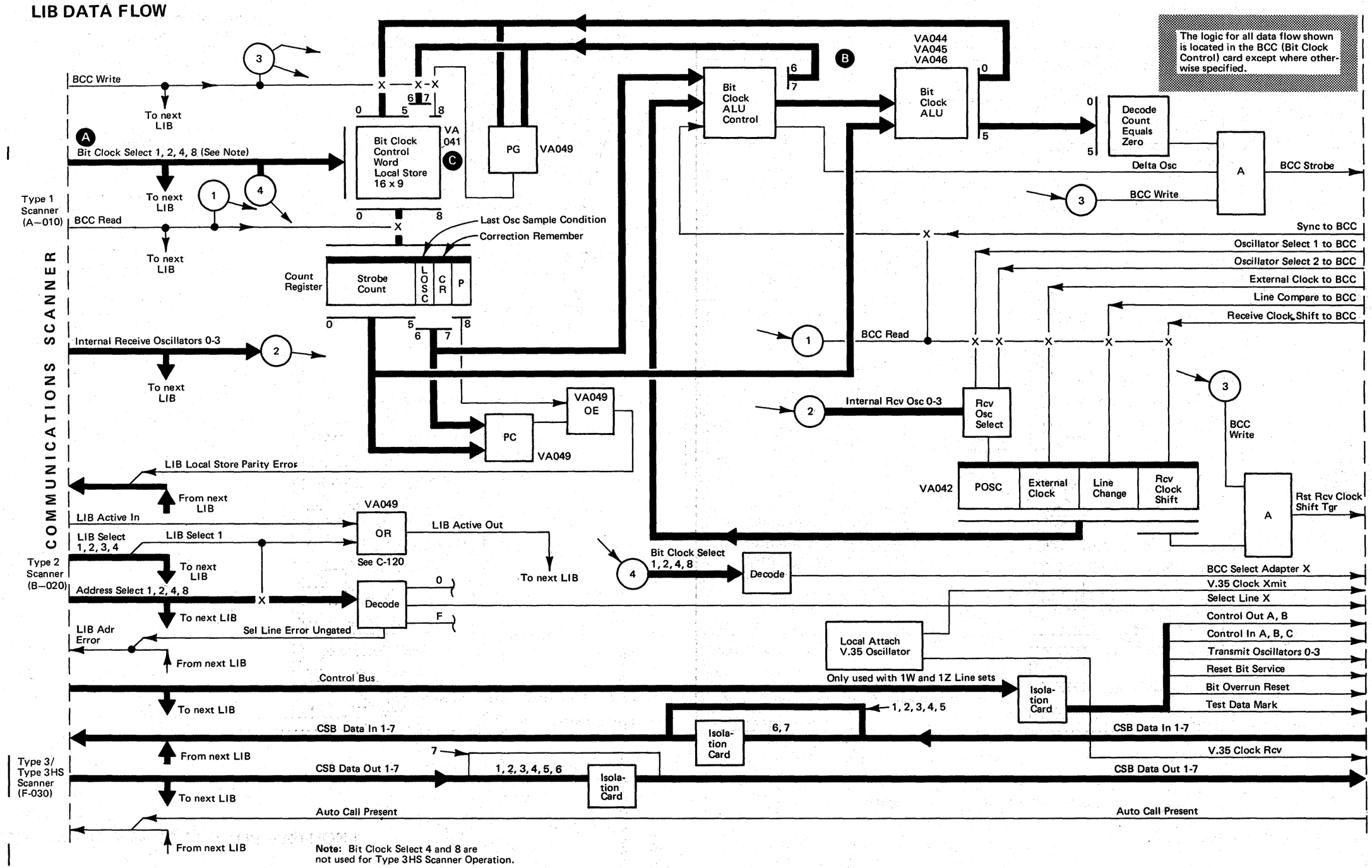
Line Set 12B (1200 bps Switched Integrated Modem with Bi-directional Interrupt Signal)

Provides for the attachment of two switched lines at speeds up to 1200 bps for start-stop or synchronous half-duplex operation. The line interface hardware has the same functional capabilities as line set 8B. However, a bi-directional interrupt signal (break) has been added to each of the two 1200 bps switched integrated modems (with auto-answer capability). This break capability is supported only for start-stop operation. Line set 12B can be used for communication with the IBM 3767 Communication Terminal (operating in 2741 Line Control) at a speed of 300 bps using common carrier switched facilities.

When the break capability is not used, line set 12B functions as a line set 8B and can be used for synchronous half-duplex operation.

The control program must condition these line interfaces for business machine clock control because the modems do not provide clock pulses. No external modems are required. Each line interface is connected to the switched network through an automatic Data Access Arrangement (CBS Data Coupler, for example).

LIB DATA FLOW



LIB DATA FLOW, PART 2

A Interface Bit Clock Addressing

In addition to line scanning for service requests, the scanner controls the sequential selection of the 16 BCC (bit clock control) words in each LIB. During each selection, one BCC word is addressed, read out, updated, and written back into the LIB BCC local store.

B LIB Receive—Bit Clock Control

The BCC provides bit strobing pulses to the associated line interface to sample the received data if that line is business machine clocked. Controls are provided to strobe start-stop data and/or binary synchronous (or equivalent) business machine clocked data. Corrections are continuously made for synchronous data clocking to assure that strobing occurs in the center of the data bit.

When external clocking is provided by the modem, the internal clocking of the bit clock control is used to determine if the modem clock is providing receive clocking pulses. If clocking pulses are not received from the modem, the bit clock control provides the strobe pulses for both the received data and for pseudo bit service requests so the receive operation can continue. The bit clock control uses a program selectable internal clock that runs at less than one half the line speed. Because strobing occurs at a slower rate than the transmission of data, some data bits are lost and the control program would not recognize the characters received. The control program must detect this condition.

Each LIB has a bit clock control that controls the bit clocking and strobing function for up to 16 interfaces.

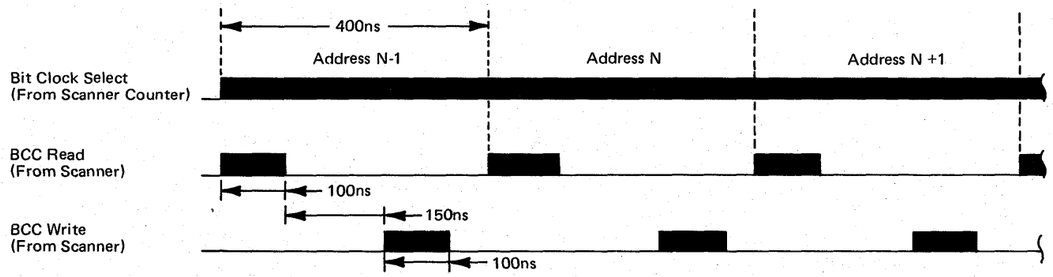
C Bit Clock Control Word Local Store

Within the BCC card in each LIB is a bit clock control word local store. There is a nine bit BCC word for each interface. The format of the BCC word is:

- Bits 0-5 contain a count field that buffers the count of the internal clock oscillator transitions.
- Bit 6 contains the LOSC (last oscillator sample condition) from the previous interface scan.
- Bit 7 contains a correction remember bit. The correction remember bit on indicates:
  - The count has been forced to 32 at a bit boundary for start-stop receive operations.
  - The count has been adjusted at a line transition for synchronous receive operation with business machine clocking.

  In both cases, the count can only be incremented by one (no additional corrections) until BCC strobe, at which time the correction remember bit is reset.
- Bit 8 is a parity bit.

BIT CLOCK CONTROL TIMINGS



- Bit Clock Select
  - Output of the bit clock select counter which runs continuously in the attached scanner.
  - Each bit clock selection cycle is 400 ns during which one line interface address in each LIB and the associated BCC word are selected.
  - Sequentially selects 1 of 16 BCC words in each LIB.
  - The same BCC word is selected every 6.4 microseconds.
- BCC Read
  - Gates the contents of the BCC word to the count register
  - Gates the status of line interface lines to BCC latches for use by the bit clock ALU control
- BCC Write
  - Gates the updated contents of the strobe count, LOSC, correction remember, and parity bit to the selected BCC word in local store.

BUSINESS MACHINE CLOCKS

Up to four business machine clocks may be installed in each communication scanner. The business machine clocks for a given scanner may be selected from the following list. Also shown is the power-on warm-up period associated with each business machine clock.

Business Machine Clock	Power-on Warm Up Period (seconds)
45.5 bps	5
50.0 bps	4
56.89 bps	20
74.2 bps	5
75.0 bps	5
100.0 bps	4
110.0 bps	3
134.5 bps	2
150.0 bps	<1
200.0 bps	<1
300.0 bps	<1
600.0 bps	<1
950.0 bps	<1
1050.0 bps	<1
1200.0 bps	<1
2000.0 bps	<1
2400.0 bps	<1

At least one of the above business machine clocks whose speed is less than one half the speed of the lowest speed external clocked line interface must be installed in each scanner. Which installed business machine clock is used for a given line interface is set under program control. For line attachment at speeds greater than above, the external modem or V.35 Local Attachment Clock must provide the clock pulses.

V.35 LOCAL ATTACHMENT CLOCK

A special oscillator, located in LIB position 1 of the LIB Type 1 board, provides 14,400 or 57,600 bps clock pulses for the 1W and 1Z line sets. Oscillator speed is selectable using a LIB Type 1 board jumper. The V.35 Local Attachment Clock also provides pulses for use by the distant locally attached device.

Power-on warm up time for the V.35 Local Attachment Clock is one second.

LIB BCC SEQUENCE OF OPERATION

The bit clock select lines from the attached scanner sequentially select each BCC word in the BCC local store of each LIB. Four bit-clock select lines (1, 2, 4, 8) are decoded to address the BCC word in the local store (located in the BCC card).

The BCC word is read out of BCC local storage and placed in the clock register at BCC read time.

Since a BCC word is read into the clock register in each LIB every 400 nanoseconds, each bit is sampled at least 64 times for each of the 16 lines operating at 2400 bps -- the highest bit rate for business machine clocking. Received data is sampled at a higher rate as the bit rate decreases (see C-050).

At the same time the LIB selects a BCC word from the BCC local store, the associated interface is also selected.

BCC select adapter X gates the following applicable lines from the selected line adapter (see individual line set pages).

'Sync to BCC'
'External clock to BCC'
'Oscillator select bits 1 and 2 to BCC'
'Line compare to BCC'
'Receive clock shift to BCC'

Up to 4 business machine oscillators may be in the attached scanner. For a given bit rate, the same physical oscillator generates the internal receive oscillator and the internal transmit oscillator, but the internal receive oscillator rate is 32 times as fast as the internal transmit oscillator. The receive oscillator gives 64 oscillator changes for every bit time. The internal receive oscillator chart gives the time-per-cycle for each internal clock bit rate. A cycle is the time between consecutive positive going pulses as shown on C-050.

One of the four internal receive oscillators is selected according to the state of the oscillator select bits 1 and 2. The state of that selected receive oscillator is placed in the POSC

Internal Transmit Osc

Bit Rate BPS	MS/cycle
45.5	21.978
50.0	20.000
56.9	17.574
74.2	13.477
75.0	13.333
100.0	10.000
110.0	9.091
134.5	7.435
150.0	6.667
200.0	5.000
300.0	3.333
600.0	1.667
950.0	1.052
1050.0	0.952
1200.0	0.833
2000.0	0.500
2400.0	0.416

Internal Receive OSC

Bit Rate BPS	MS/cycle
45.5	0.687
50	0.625
56.9	0.549
74.2	0.421
75	0.417
100	0.313
110	0.284
134.5	0.232
150	0.208
200	0.156
300.0	0.104
600	0.052
950.0	0.033
1050.0	0.030
1200	0.026
2000	0.0156
2400	0.013

(present oscillator sample condition) latch at BCC read gate time. The states of the external clock, line compare, and receive clock shift are also gated into their respective latches at BCC read gate time.

The bit clock ALU control logic determines whether there has been an oscillator transition since the last BCC scan of that interface. This is done by comparing the present state of the oscillator (POSC) to the last oscillator sample condition from the bit clock control word for that interface. If the oscillator has not changed state since the last bit clock control scan, the bit clock control word is restored to the bit clock control word local store and the bit clock controls wait until the next BCC scan. If the oscillator has changed state, the POSC state is written into the LOSC position of the BCC word in local store. A sequence of decisions is then made to determine what action is to be taken (see Bit Clock ALU Control Flow Chart on C-050.

START-STOP OPERATION

If the line interface is attached to a start-stop line, and if a transition has occurred on the receive data line, and if the correction remember bit is off, then the count field in the BCC word is set to a pseudo reset value of 32. The correction remember bit is also set on, and the BCC word is restored to the BCC local store.

If a transition has not occurred, or if a transition has occurred but the correction remember bit is on, a one is added to the count by means of the bit clock ALU; the ALU count is then tested. If the count is zero, the BCC strobe is signaled to the line interface, the correction remember bit is reset, and the updated BCC word returns to the BCC local store. If the count is not zero, the only action taken is the updated BCC word returns to the BCC local store.

The count field in the BCC word is six bits (bits 0-5) and can contain a count ranging from 0 to 63. The count starts at 32 on a bit boundary. The count is then incremented by one every 1/64 of a bit time as determined by the change in the internal receive oscillator. The count eventually increments past 63 to 0. A count of zero causes a BCC strobe to be signaled to the interface where a strobe occurs. The strobe is positioned in the virtual center of the bit.

SYNCHRONOUS OPERATION (BUSINESS MACHINE CLOCKING)

If the selected interface is a line interface attached to a synchronous line that requires business machine clocking, a clock correction technique is used. A test is made to determine if a transition has occurred on the receive data line. If a transition has not occurred, the action is the same as for the start-stop operation—no correction takes place.

If a transition has occurred, the correction remember bit is tested. If the correction remember bit is on, a correction has already been made for that strobe period and the transition of the line is ignored. (Note: A transition occurring with the correction remember bit on indicates a noisy or erratic action on the receive data line). Under normal conditions, the correction remember bit in the BCC word is off when the receive data line transition occurs. The two high-order bits of the count field, bits 0 and 1, are examined to determine what correction to make to the count field. The farther the count is from 32 the larger the correction, as indicated in the following chart:

Count Bits 0	1	Corrective Action	Count Between
0	0	Add 5 to count	0-15
0	1	Add 3 to count	16-31
1	0	Subt 2 from count	32-47
1	1	Subt 4 from count	48-63

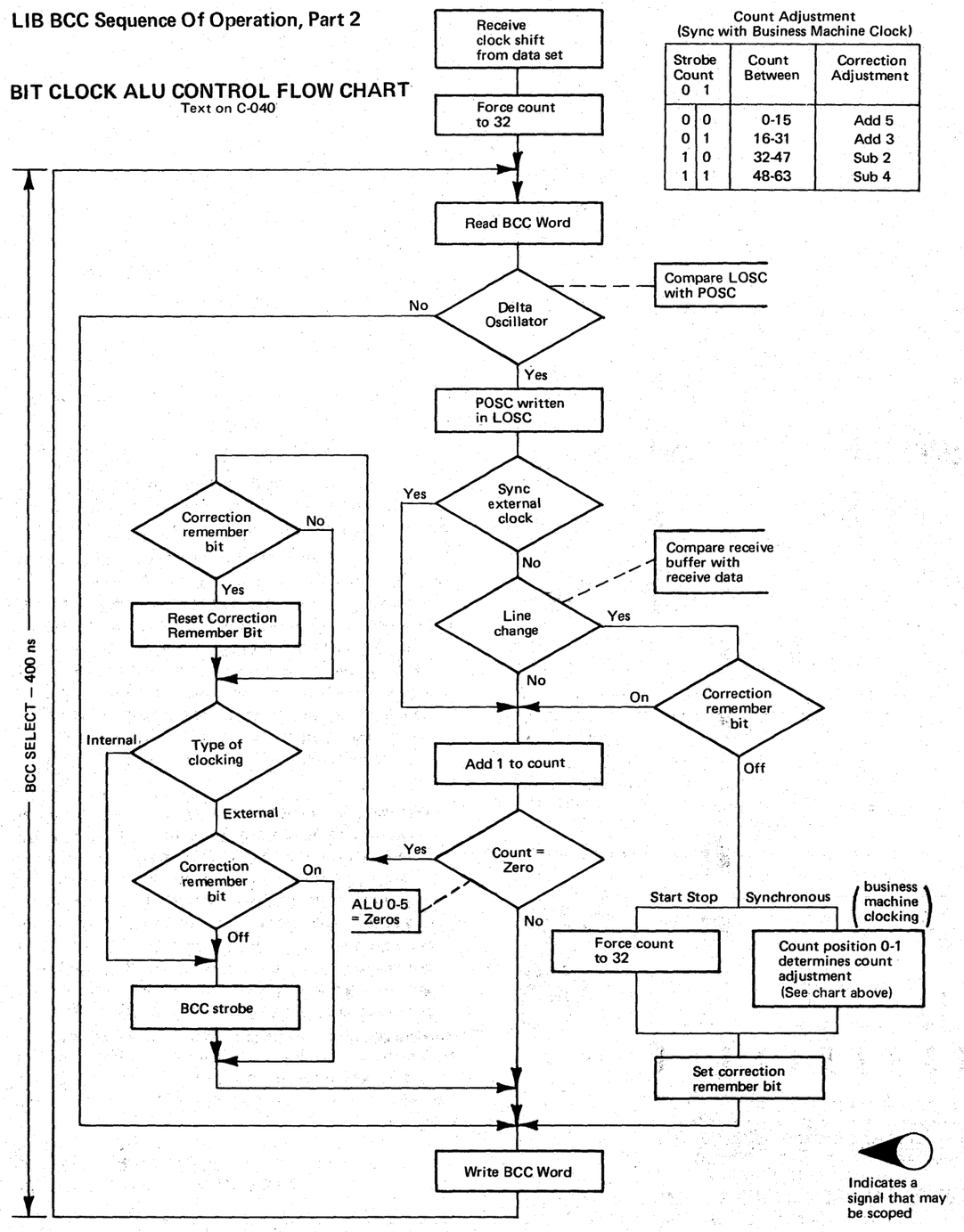
Ideally, the count should be exactly 32 at each data transition. If low, the count is increased in order to advance the strobe time. If high, the count is decreased to delay the strobe time.

The correction is made at the first change in oscillator that occurs when the correction remember bit is off, and when a transition occurs on the receive data line. Corrections are not made when consecutive bits are at the same data level. The count continues to increment by one until it becomes zero at which time the BCC strobe is signaled to the line interface.

LIB BCC Sequence Of Operation, Part 2

BIT CLOCK ALU CONTROL FLOW CHART

Text on C-040

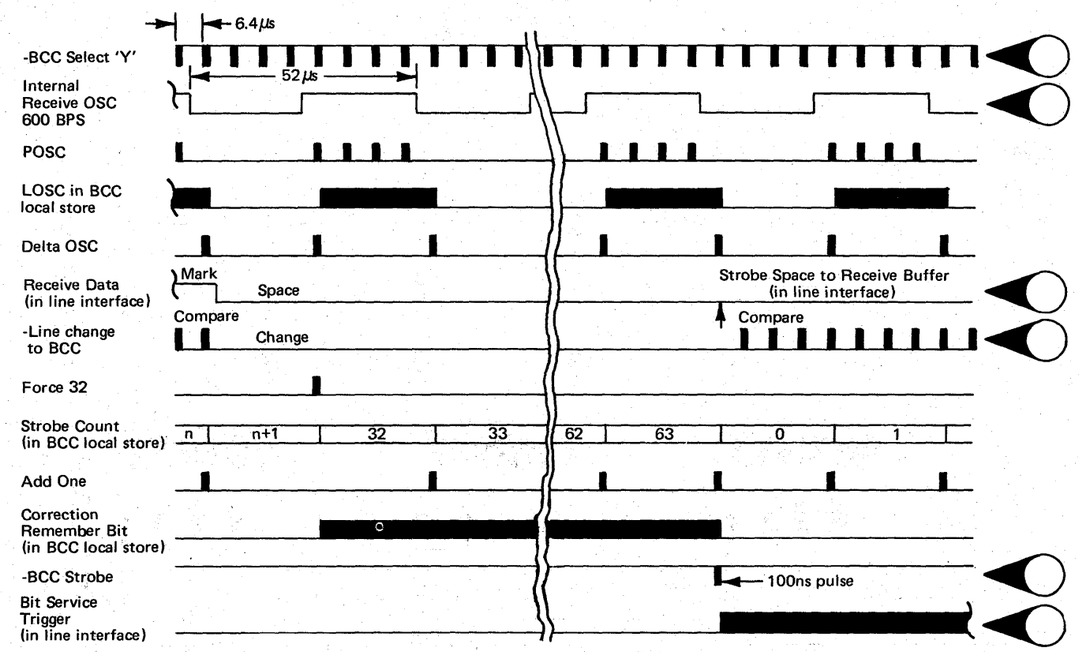


Count Adjustment
(Sync with Business Machine Clock)

Strobe Count 0	1	Count Between	Correction Adjustment
0	0	0-15	Add 5
0	1	16-31	Add 3
1	0	32-47	Sub 2
1	1	48-63	Sub 4

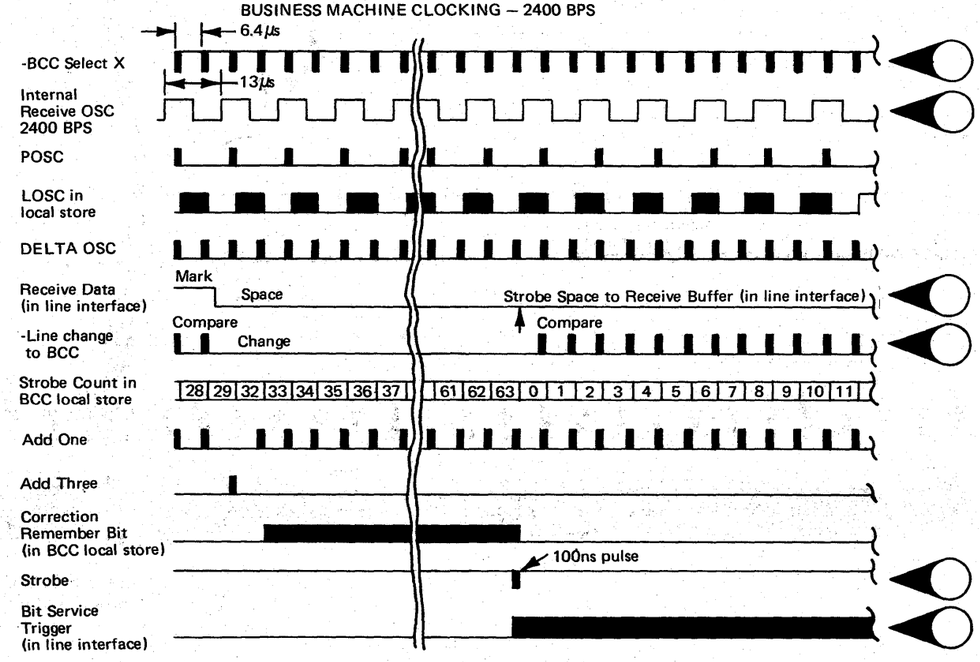
BIT CLOCK CONTROL SEQUENCE FOR START-STOP OPERATION

BUSINESS MACHINE CLOCKING – 600 BPS



BIT CLOCK CONTROL SEQUENCE FOR SYNCHRONOUS OPERATION

BUSINESS MACHINE CLOCKING – 2400 BPS



LIB BCC SEQUENCE OF OPERATION, PART 3

SYNCHRONOUS OPERATION (MODEM CLOCKING)

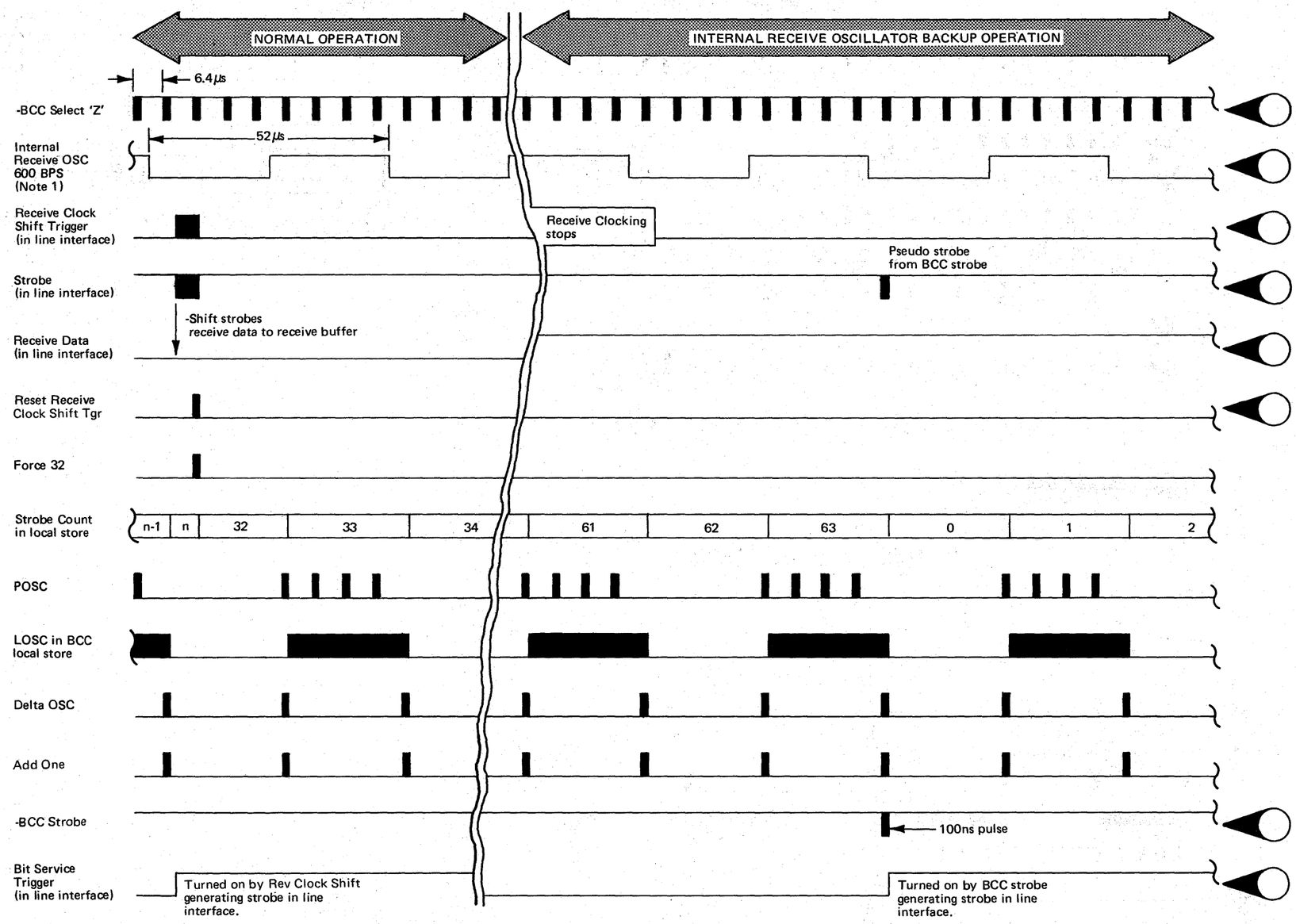
The count is forced to 32 during the BCC select cycle that senses the receive clock shift from the associated line interface. This receive clock shift originated from the negative going transition on the receive clock line from the modem.

A change in oscillator is not required to force the count to 32---however, a delay may exist between the negative transition of the receive clock from the modem and the BCC select cycle. The count is then incremented by one at every change in internal receive oscillator. The internal receive oscillator must run at less than one-half the line bit rate, so that the count will never reach 63 before the next negative transition of the receive clock from the modem repeats the above cycle by forcing the count to 32. The receive data is thus strobed from the modem receive clocking.

If the receive clock from the modem stops, the count eventually increments past 63 to 0. A BCC strobe is signaled to the interface where a pseudo strobe will sample the receive data and cause a bit service request. Because the internal receive oscillator runs at less than half the rate at which the data was transmitted, some data bits are missed. The assembled character is not the character that was transmitted, and as a result, the control characters are not recognized. The control program must detect this condition and take appropriate action.

This internal receive oscillator backup operation is needed to generate pseudo bit service requests to prevent the interface from getting into a 'hung' condition.

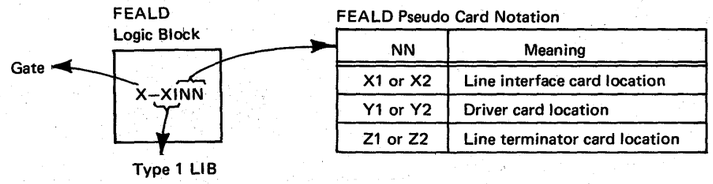
BIT CLOCK CONTROL SEQUENCE FOR SYNCHRONOUS OPERATION MODEM CLOCKING—2400 bps



Note 1 — The internal receive oscillator must run at less than one half the line baud rate.

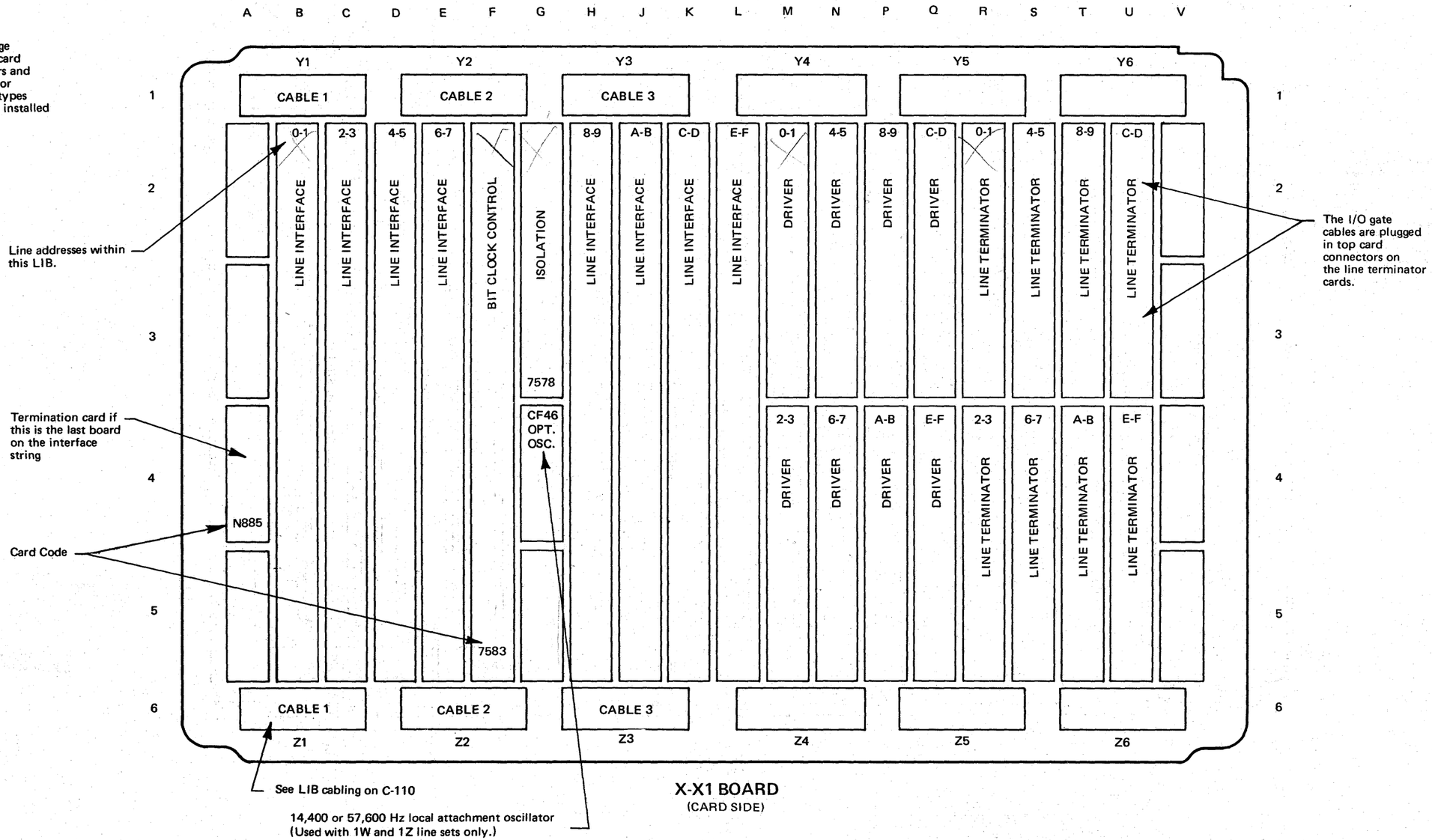
Indicates a signal that may be scoped.

TYPE 1 LIB CARD POSITIONS



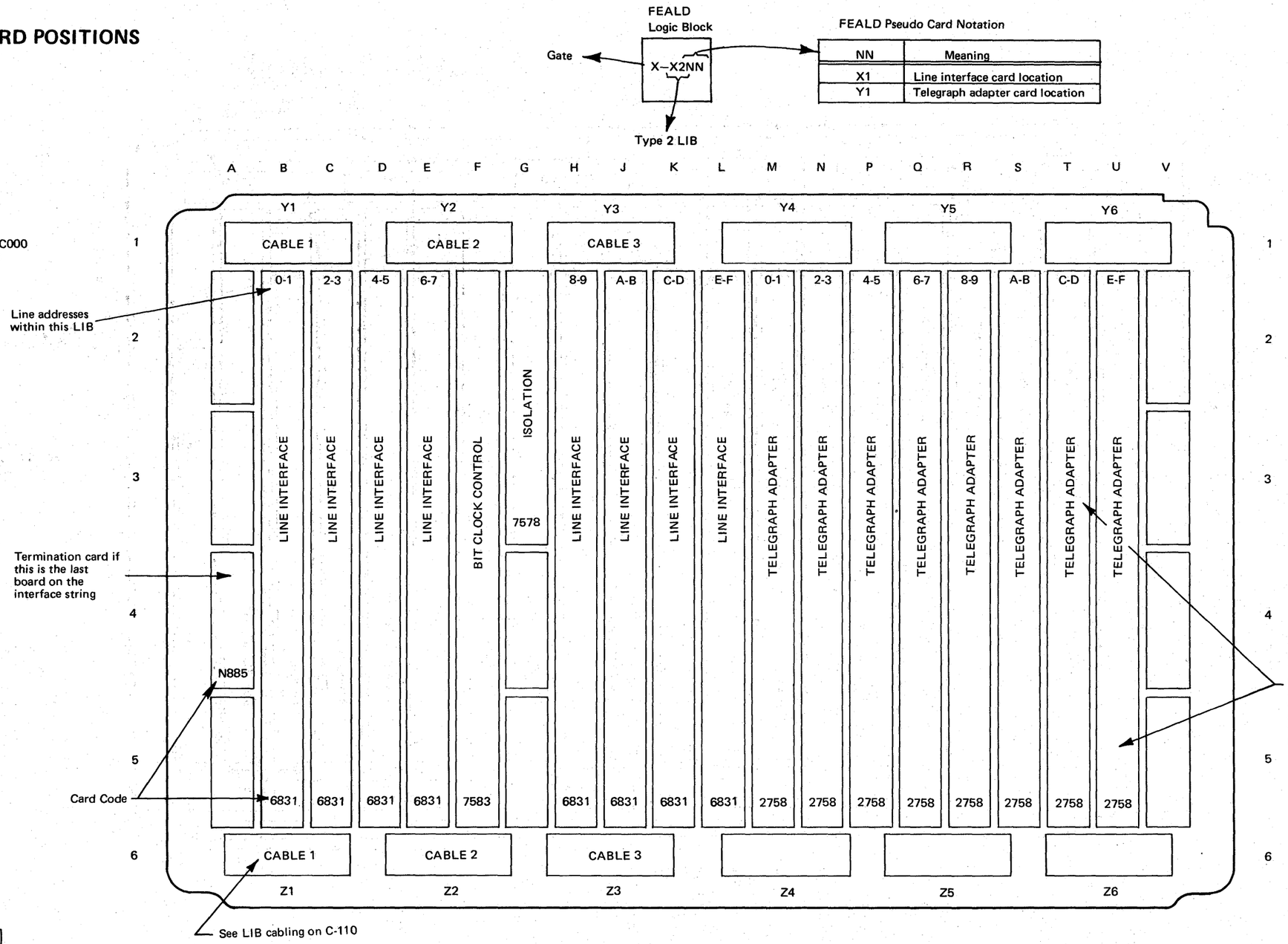
FEALD Pseudo Card Notation

NN	Meaning
X1 or X2	Line interface card location
Y1 or Y2	Driver card location
Z1 or Z2	Line terminator card location



X-X1 BOARD
(CARD SIDE)

TYPE 2 LIB CARD POSITIONS

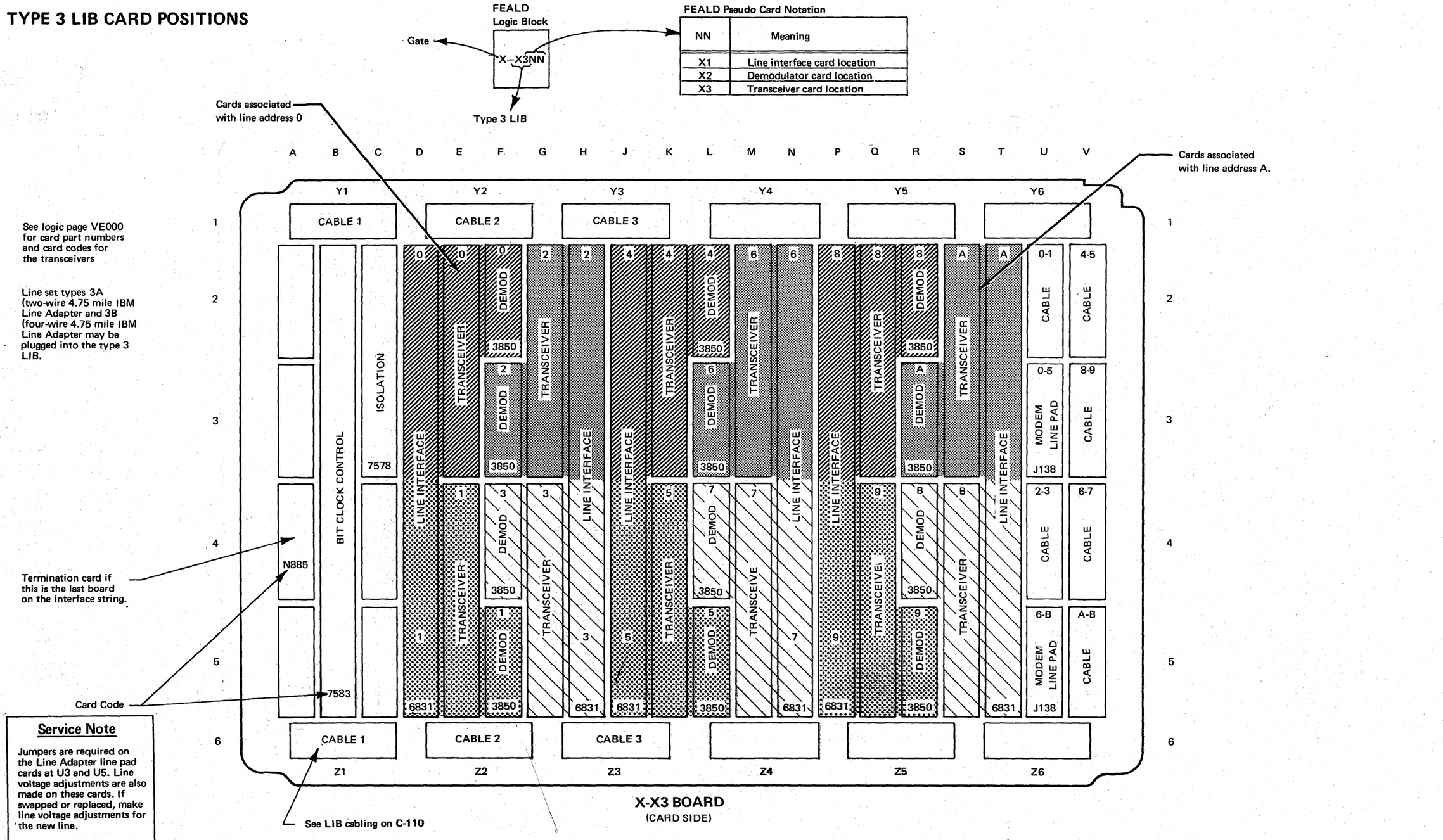


X-X2 BOARD
(CARD SIDE)

Service Note

Jumpers are required on the telegraph adapter card. Refer to logic page VC004.

TYPE 3 LIB CARD POSITIONS



Service Note

Jumpers are required on the Line Adapter line pad cards at U3 and U5. Line voltage adjustments are also made on these cards. If swapped or replaced, make line voltage adjustments for the new line.

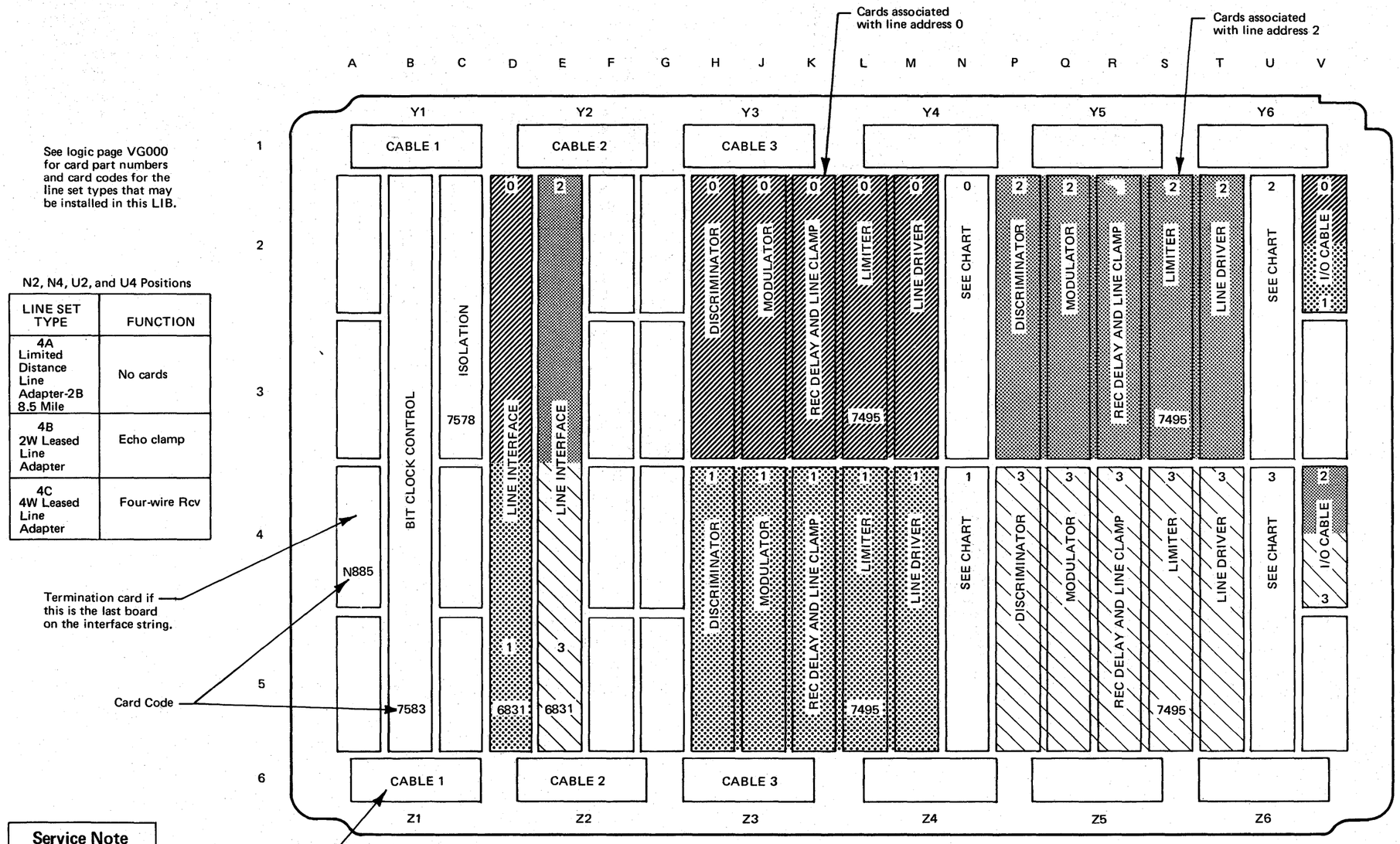
Refer to logic page VE004.

TYPE 4 LIB CARD POSITIONS

See logic page VG000 for card part numbers and card codes for the line set types that may be installed in this LIB.

N2, N4, U2, and U4 Positions

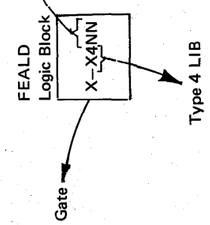
LINE SET TYPE	FUNCTION
4A Limited Distance Line Adapter-2B 8.5 Mile	No cards
4B 2W Leased Line Adapter	Echo clamp
4C 4W Leased Line Adapter	Four-wire Rcv



X-X4 BOARD
(CARD SIDE)

FEALD Pseudo Card Notation

NN for 4A	NN for 4B	NN for 4C	Meaning
X1	X1	X1	Line interface card location
X3 or Y5	X6 or Y6	X6 or Y6	Discriminator card location
X2 or Y3	X4 or Y4	X4 or Y4	Modulator card location
X2 or Y4	X5 or Y5	X5 or Y5	Rcv delay and line clamp card
X2 or Y2	X2 or Y2	X2 or Y2	Limiter card location
X4 or Y6	X7 or Y7	X7 or Y7	Line driver card location
	X3 or Y3		Echo clamp card (N2 or N4)
		X3 or Y3	Wrap test card (N2 or N4)



Service Note

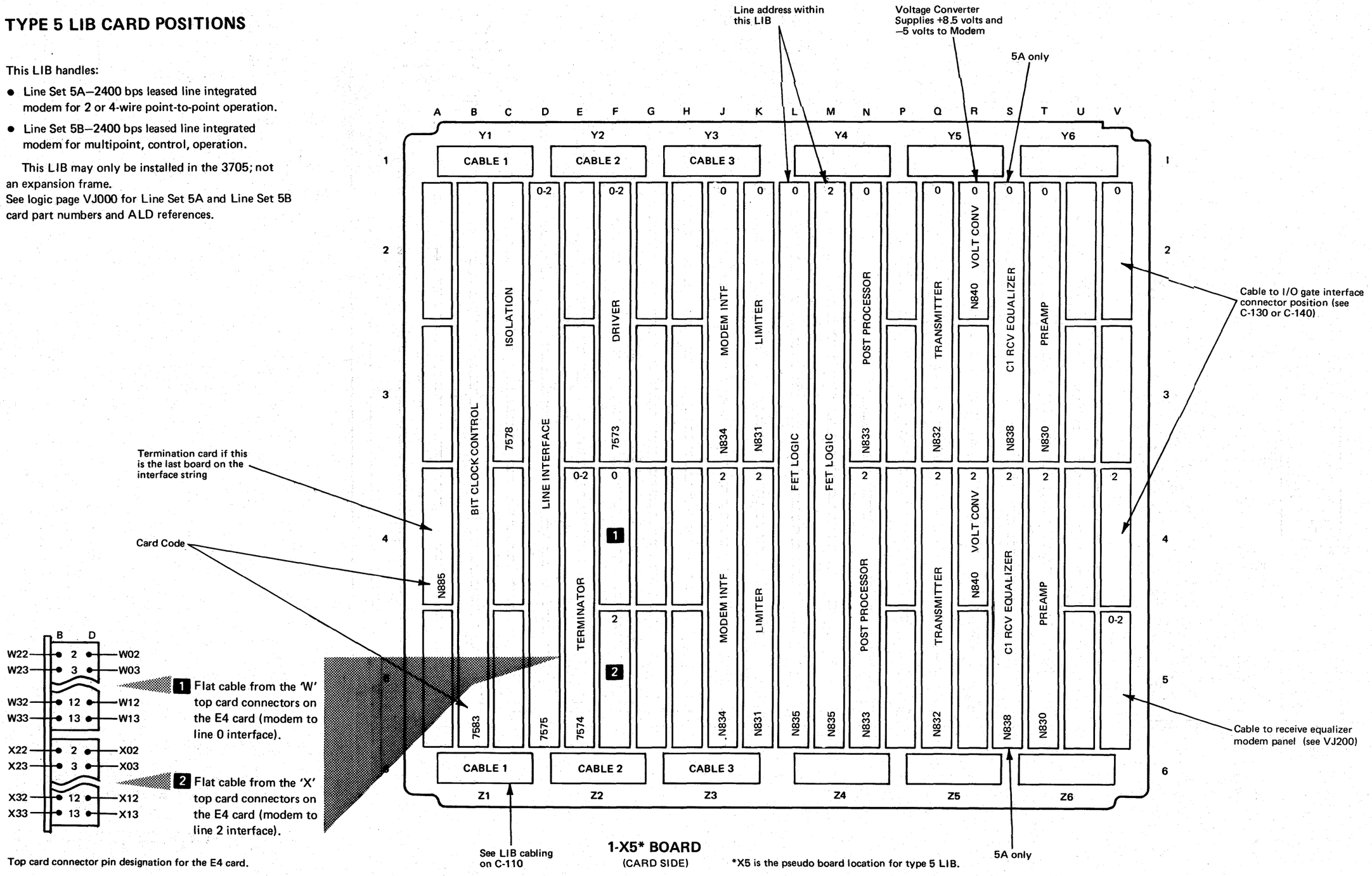
Jumpers are required on certain cards. Refer to logic pages VG006, VG007, and VG008.

TYPE 5 LIB CARD POSITIONS

This LIB handles:

- Line Set 5A—2400 bps leased line integrated modem for 2 or 4-wire point-to-point operation.
- Line Set 5B—2400 bps leased line integrated modem for multipoint, control, operation.

This LIB may only be installed in the 3705; not an expansion frame.
See logic page VJ000 for Line Set 5A and Line Set 5B card part numbers and ALD references.

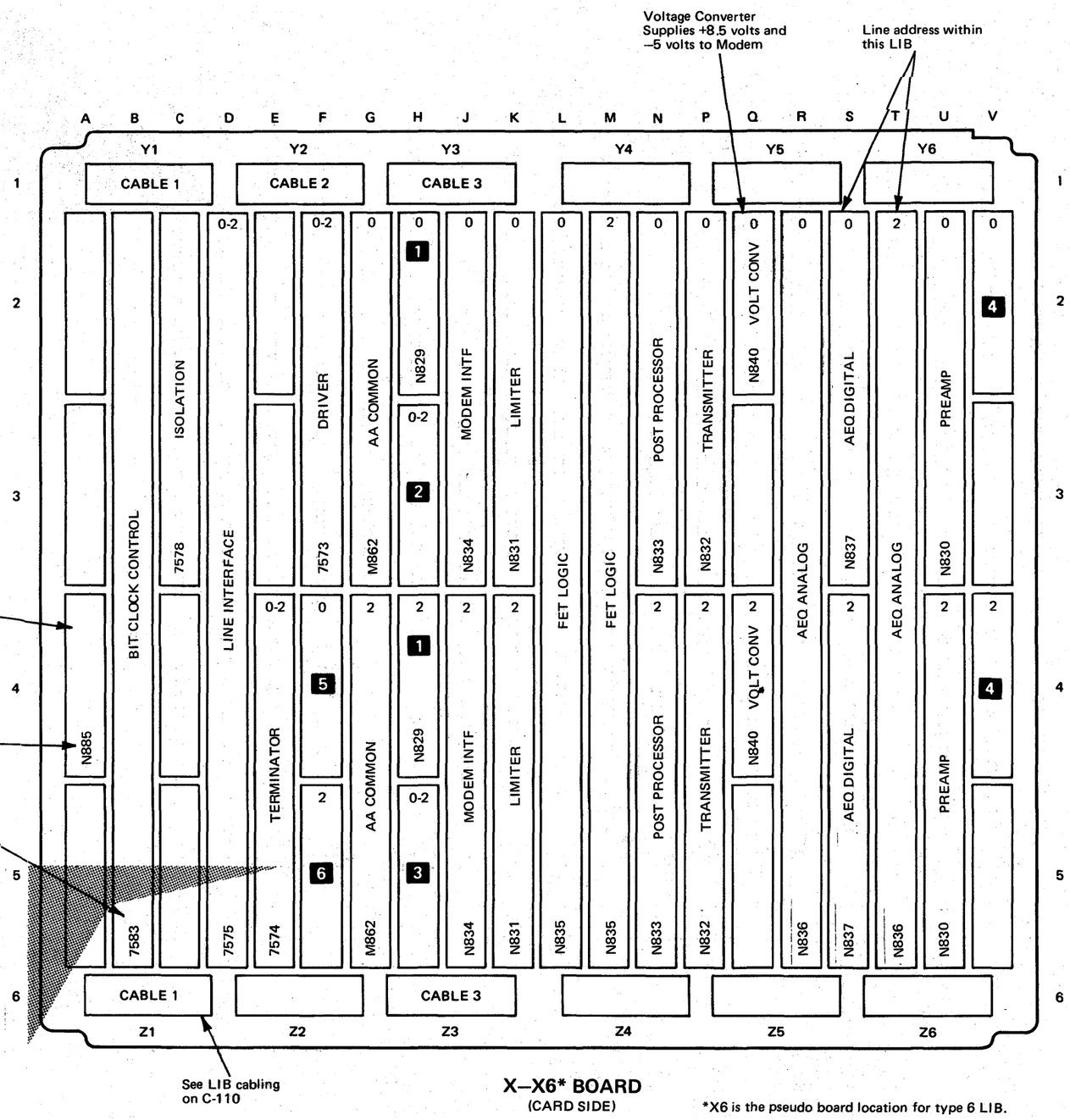


Top card connector pin designation for the E4 card.

TYPE 6 LIB CARD POSITIONS

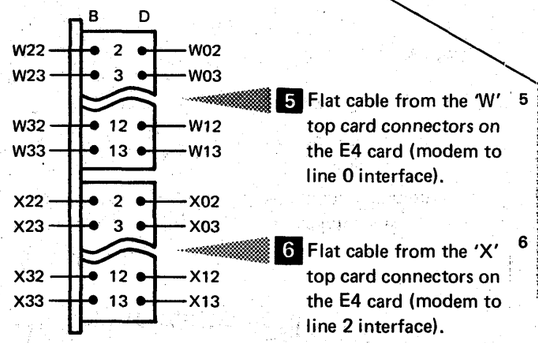
This LIB handles Line Set 6A—2400 bps switched network integrated modem with auto-answer capability and automatic equalization.

See logic page VL000 for Line Set 6A card part numbers and ALD references.



X–X6* BOARD
(CARD SIDE)

*X6 is the pseudo board location for type 6 LIB.



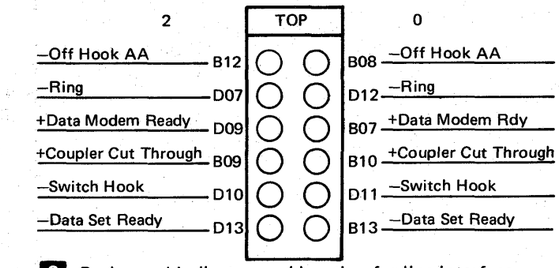
5 Flat cable from the 'W' top card connectors on the E4 card (modem to line 0 interface).

6 Flat cable from the 'X' top card connectors on the E4 card (modem to line 2 interface).

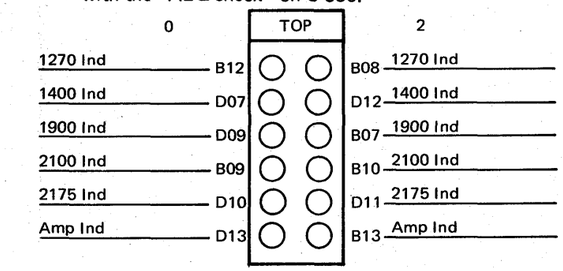
Top card connector pin designation for the E4 card.

1 Auto-Answer without ACO.

2 Back panel indicator card location for line interface addresses 0 and 2 for the following auto-answer lines (see VL026).



3 Back panel indicator card location for line interface addresses 0 and 2 for the following automatic equalizer lines (see VL026). This indicator position is used with the "AEQ check" on C-530.



Indicator Card P/N 5801645

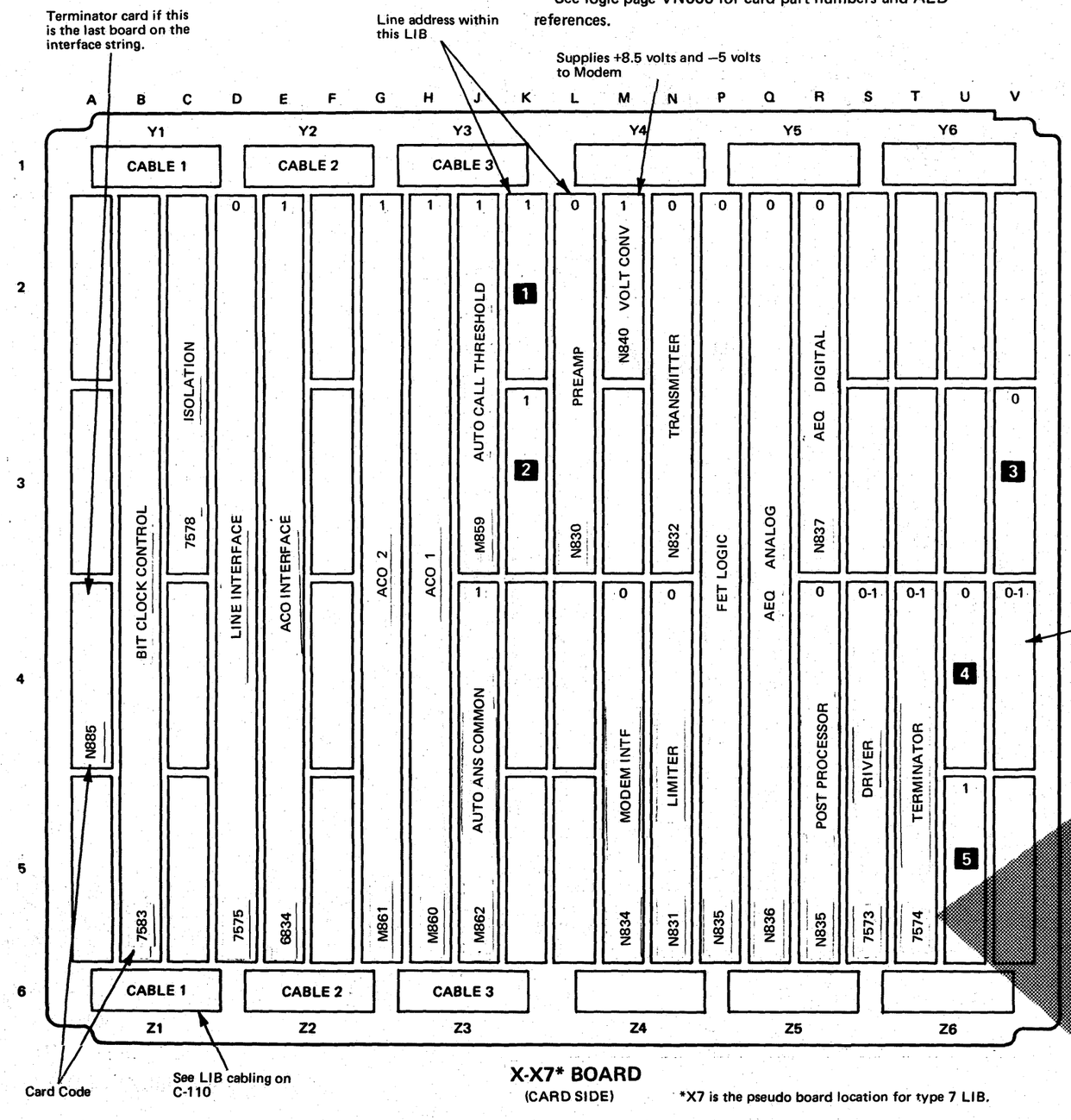
Note: Indicator is on if the input pin is – (ground)
Indicator is off if the input pin is + (toward +12V).

4 Cable to the I/O gate interface connector position (see C-130 or C-140).
Line Set 6A includes an external cable to a CBS Data Coupler.

TYPE 7 LIB CARD POSITIONS

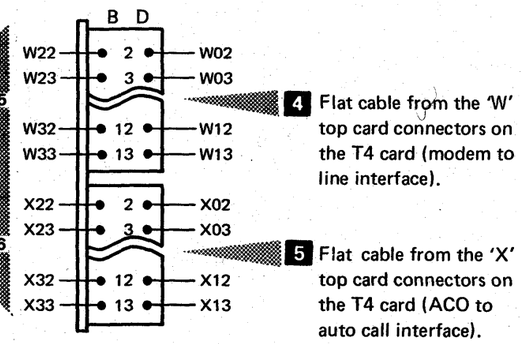
This LIB includes a 2400/1200 bps integrated switched modem with Automatic Call Originate and Auto-Answer capability as well as the line set.

See logic page VN000 for card part numbers and ALD references.



X-X7* BOARD
(CARD SIDE)

*X7 is the pseudo board location for type 7 LIB.



4 Flat cable from the 'W' top card connectors on the T4 card (modem to line interface).

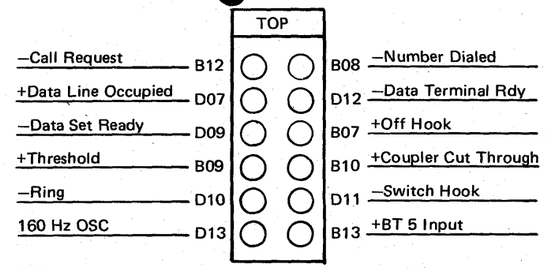
5 Flat cable from the 'X' top card connectors on the T4 card (ACO to auto call interface).

Top card connector pin designation for the T4 card.

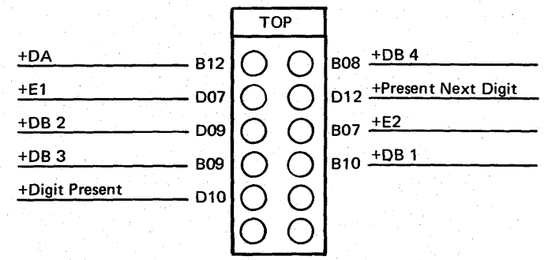
A *Notes:*

1. These ACO indicators are *off* when the indicated function is active, as follows:
   a. DB1, 2, 3, and 4 represent the digit signal bus (1, 2, 4, and 8, respectively). The indicators display the complement of the bus, which sets into the dialer counter. The display is continuous from the DTE interface.
   b. E1 represents the gate for 160Hz to set the dialer counter.
   c. E2 represents the end of dial counter set.
   d. Digit Present is the DTE interface function.
2. Take note of the following:
   a. Without '160Hz Osc', the ACO will not work.
   b. The *not* indicators are *off* when the function is active.
   c. Threshold represents 'dial tone and not number dialed' OR 'answer tone' above threshold.
3. When an automatic equalizer segment is *not* selected, its control line is at ground and the indicator is on.

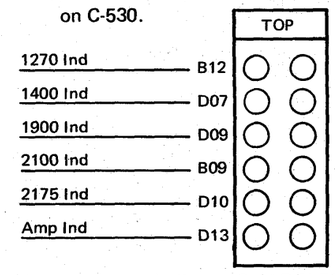
1 Back panel indicator card location for auto call interface address 1 for the following ACO lines (see VN027). See note **A**



2 Back panel indicator card location for auto call interface 1 for the following ACO lines (see VN027). See note **A**



3 Back panel indicator card location for line interface 0 for the following automatic equalizer lines (see VN027). This indicator position is used with the "AEQ check" on C-530.



Indicator Card P/N 5801645

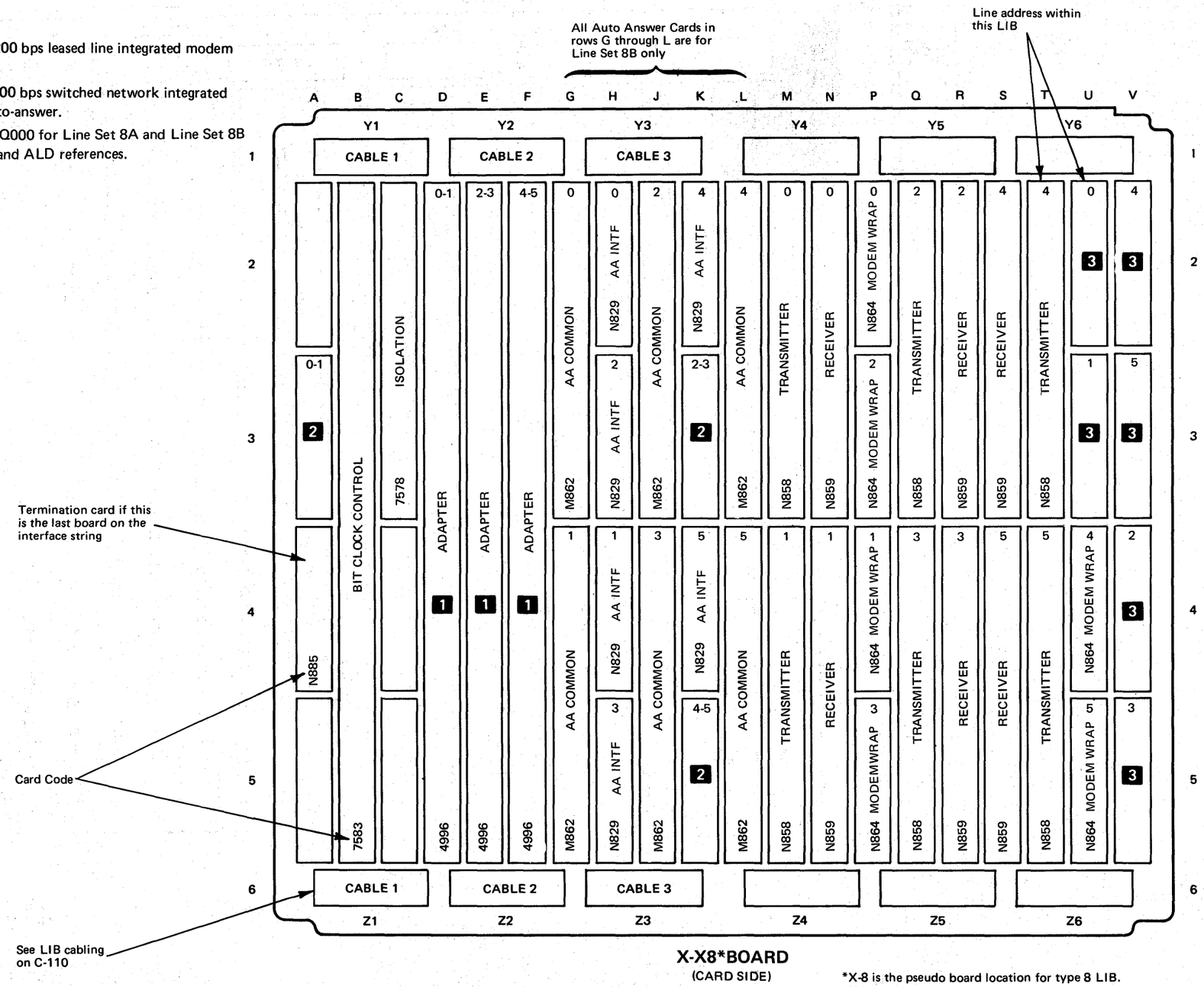
Note: Indicator is on if the input pin is – (ground). Indicator is off if the input pin is + (toward +12).

TYPE 8 LIB CARD POSITIONS

This LIB handles:

- Line Set 8A—1200 bps leased line integrated modem (2 or 4 wire).
- Line Set 8B—1200 bps switched network integrated modem with auto-answer.

See logic page VQ000 for Line Set 8A and Line Set 8B card part numbers and ALD references.

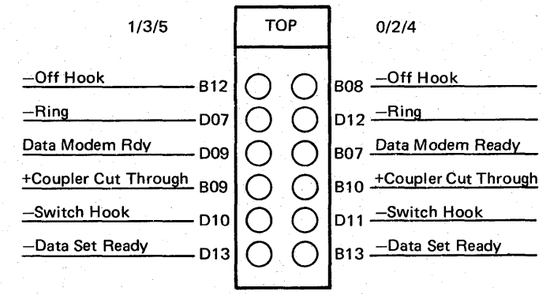


X-X8*BOARD
(CARD SIDE)

*X-8 is the pseudo board location for type 8 LIB.

1 Adapter Card Includes:
- Line Interface
- MST-SLT Drivers
- SLT-MST Terminators

2 Back panel indicator card locations for use with Line Set 8B (switched with auto answer). See VQ025.



Indicator Card P/N 5801645

Note: Indicator is on if the input pin is — (ground).
Indicator is off if the input pin is + (toward +12V).

3 Cables to the I/O gate interface connector positions (see C-130 or C-140).

Line Set 8A includes an external cable assembly that provides a cable to a 4 wire telephone connector for each of its two line interface addresses—(0-1), (2-3) or (4-5).

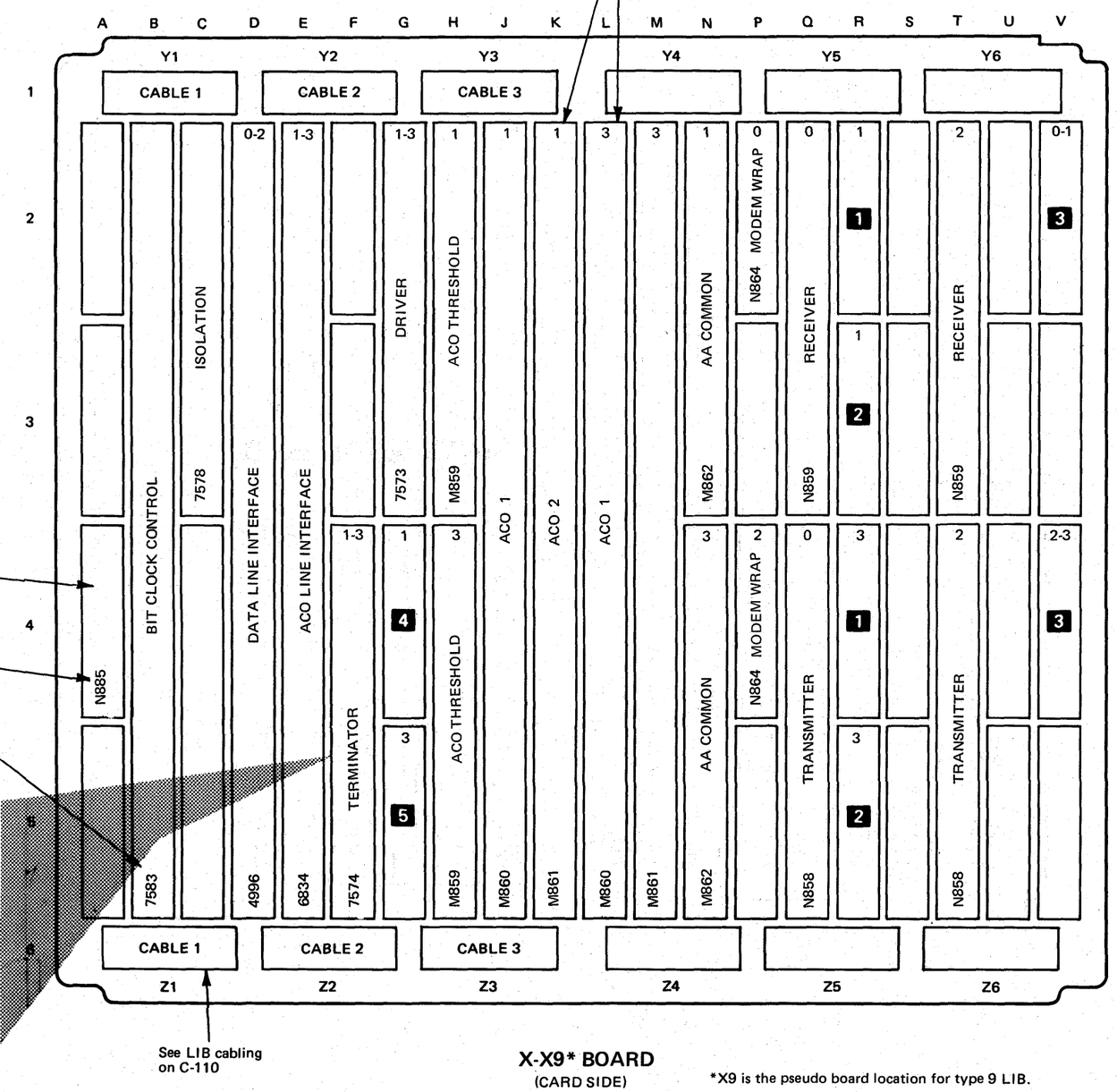
Line Set 8B includes an external cable assembly that provides a cable to a CBS Data Coupler for each of its two line interface addresses.

TYPE 9 LIB CARD POSITIONS

This LIB handles Line Set 9A—1200 bps switched network integrated modem with Automatic Call Originate and Auto-Answer capability.

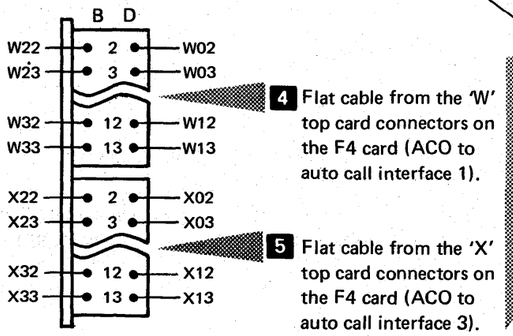
See logic page VS000 for Line Set 9A card part numbers and ALD references.

Line address within this LIB



Termination card if this is the last board on the interface string.

Card Code



Top card connector pin designation for the F4 card.

4 Flat cable from the 'W' top card connectors on the F4 card (ACO to auto call interface 1).

5 Flat cable from the 'X' top card connectors on the F4 card (ACO to auto call interface 3).

See LIB cabling on C-110

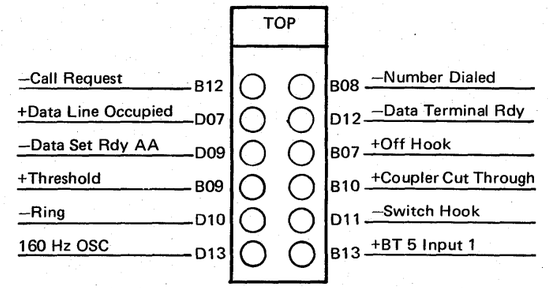
X-X9* BOARD
(CARD SIDE)

*X9 is the pseudo board location for type 9 LIB.

(A) *Notes:*

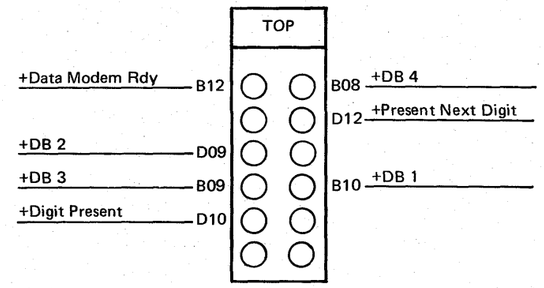
1. These ACO indicators are *off* when the indicated function is active, as follows:
   a. DB1, 2, 3, and 4 represent the digit signal bus (1, 2, 4, and 8, respectively). The indicators display the complement of the bus, which sets into the dialer counter. The display is continuous from the DTE interface.
   b. Digit Present is the DTE interface function.
2. Take note of the following:
   a. Without '160Hz Osc', the ACO will not work.
   b. The *not* indicators are *off* when the function is active.
   c. Threshold represents 'dial tone and not number dialed' OR 'answer tone' above threshold.
3. When an automatic equalizer segment is *not* selected, its control line is at ground and the indicator is on.

1 Back panel indicator card locations for auto call interface addresses 1 or 3 for the following ACO lines (see VS025). See note (A)



Indicator Card P/N 5801645

2 Back panel indicator card locations for auto call interface addresses 1 or 3 for the following ACO lines (see VS025). See note (A).



Note: Indicator is on if the input pin is — (ground).
Indicator is off if the input pin is + (toward +12V).

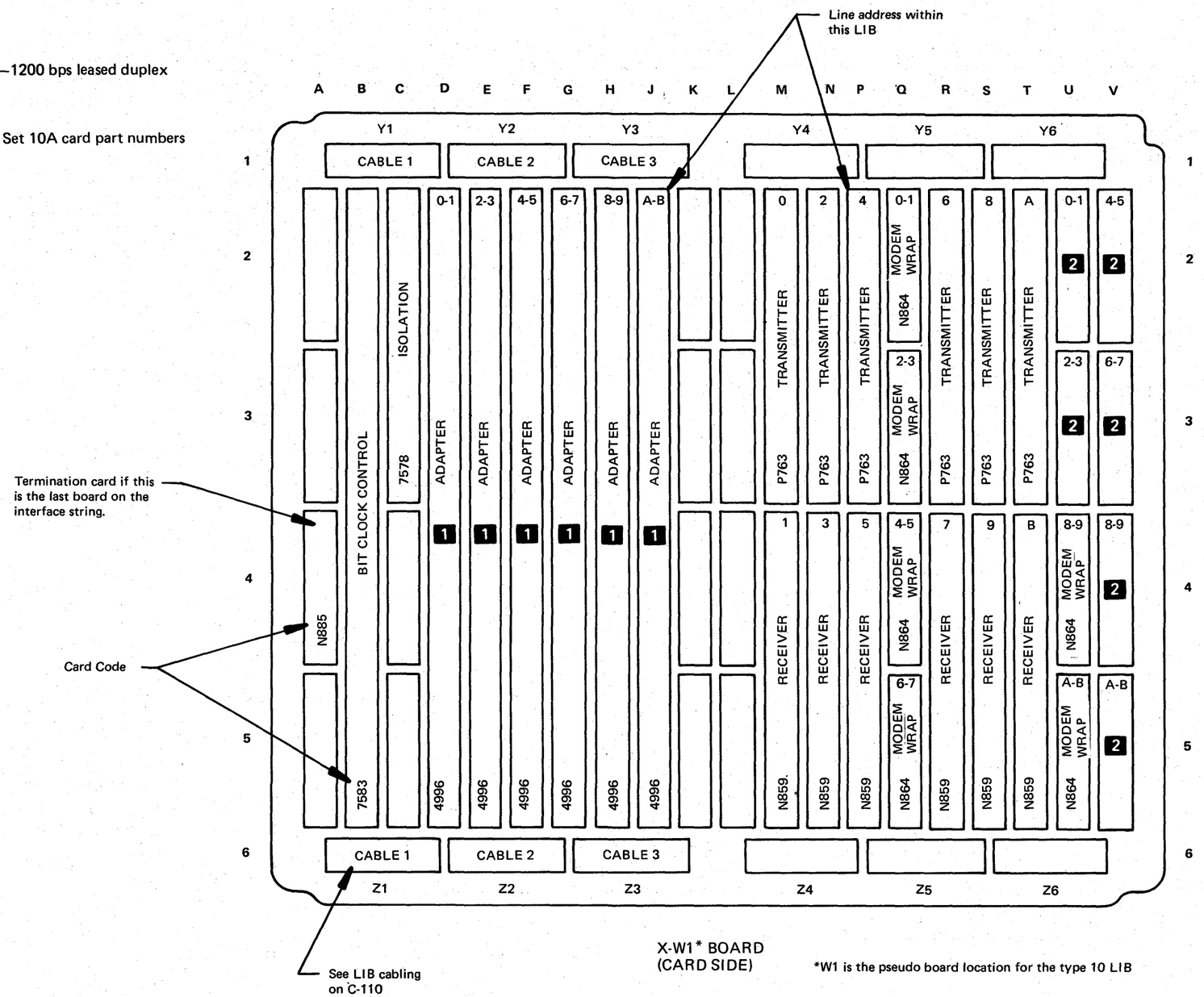
3 Cable to the I/O gate interface connector position (see C-130 or C-140).

Line Set 9A includes an external cable to a CBS Data Coupler for line pairs 0-1 or 2-3.

TYPE 10 LIB CARD POSITIONS

This LIB handles Line Set 10A—1200 bps leased duplex data integrated modem.

See logic page VU000 for Line Set 10A card part numbers and ALD references.



X-W1* BOARD
(CARD SIDE)

*W1 is the pseudo board location for the type 10 LIB

1 Adapter Card Includes:
- Line Interface
- MST-SLT Drivers
- SLT-MST Terminators

2 Cables to the I/O gate interface connector positions (see C-130 or C-140).

Line set 10A includes one external cable to a 4-wire telephone connection for its line pair—(0-1)----(A-B).

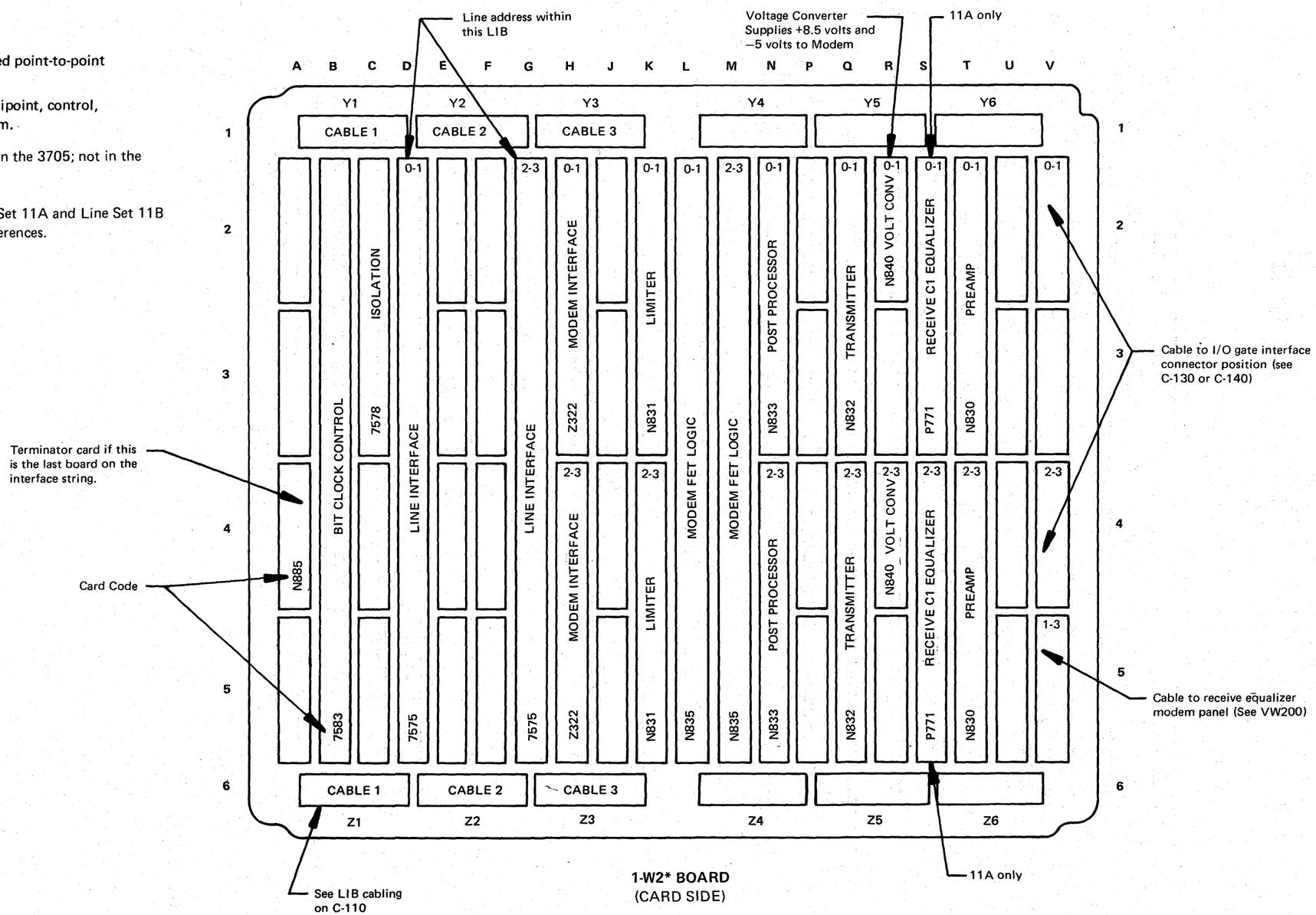
TYPE 11 LIB CARD POSITIONS

This LIB handles:

- Line Set 11A—2400 bps leased point-to-point duplex integrated modem.
- Line Set 11B—2400 bps multipoint, control, duplex data integrated modem.

This LIB may only be installed in the 3705; not in the expansion frames.

See logic page VW000 for Line Set 11A and Line Set 11B card part numbers and ALD references.



1-W2* BOARD
(CARD SIDE)

*W2 is the pseudo board location for the type 11 LIB.

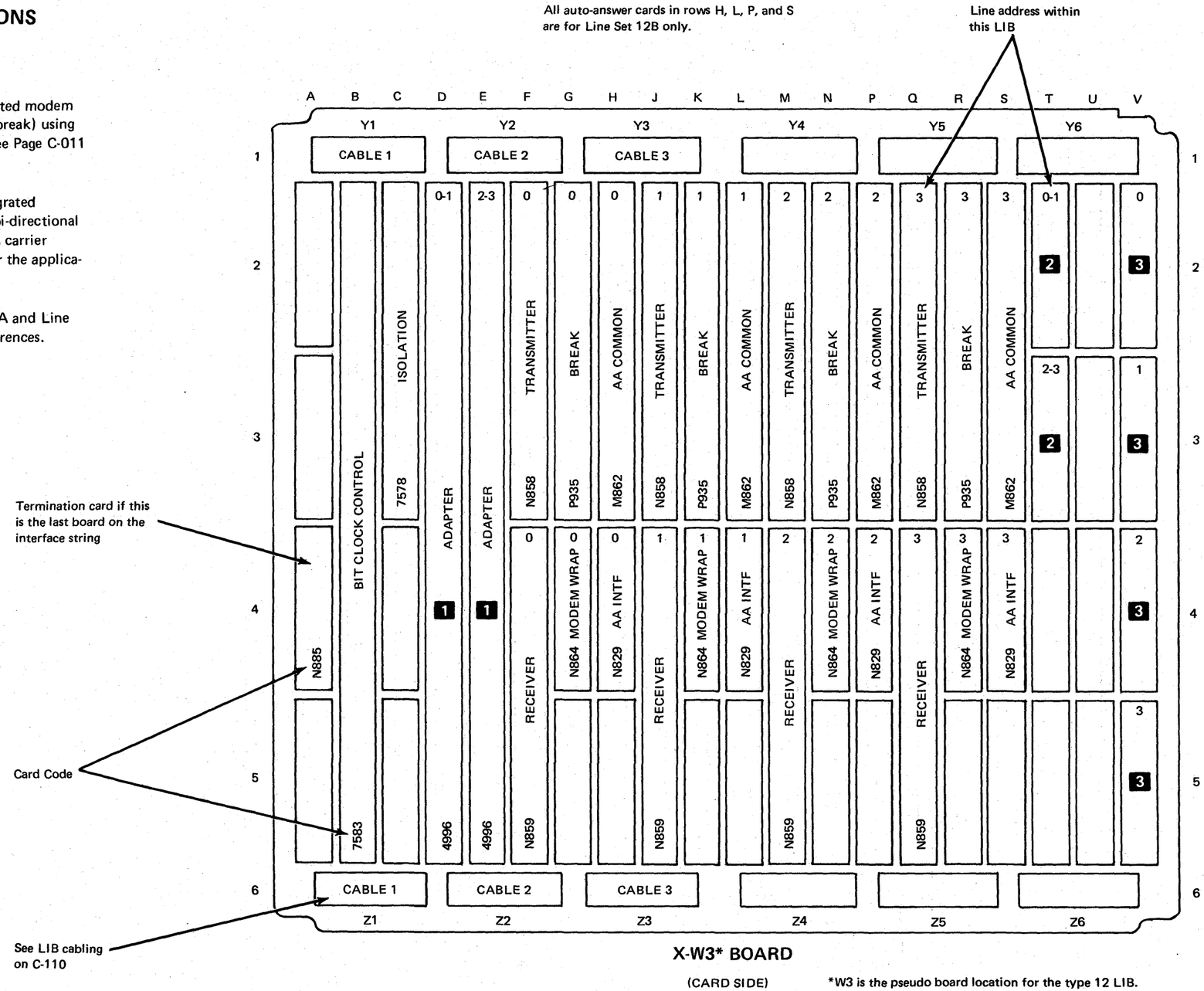
TYPE 12 LIB CARD POSITIONS

This LIB handles:

Line Set 12A—1200 bps leased integrated modem with a bi-directional interrupt signal (break) using two-wire common carrier facilities. See Page C-011 for the application for this line set.

Line Set 12B—1200 bps switched integrated modem with auto-answer and with a bi-directional interrupt signal (break) using common carrier switched facilities. See Page C-011 for the application for this line set.

See logic page VX000 for Line Set 12A and Line Set 12B card part numbers and ALD references.



X-W3* BOARD

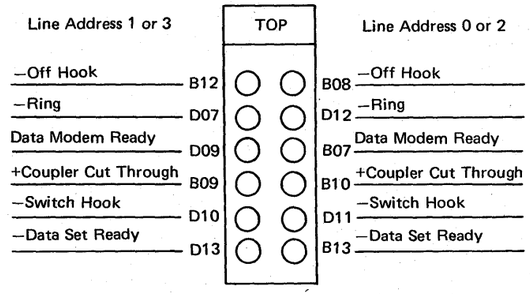
(CARD SIDE)

*W3 is the pseudo board location for the type 12 LIB.

1 Adpater Card Includes:

- Line Interface
- MST-SLT Drivers
- SLT-MST Terminators

2 Back panel indicator card locations for use with Line Set 12B (switched with auto-answer). See VX000.



Indicator Card P/N 5801645

Note: Indicator is on if the input pin is — (ground). Indicator is off if the input pin is + (toward +12V).

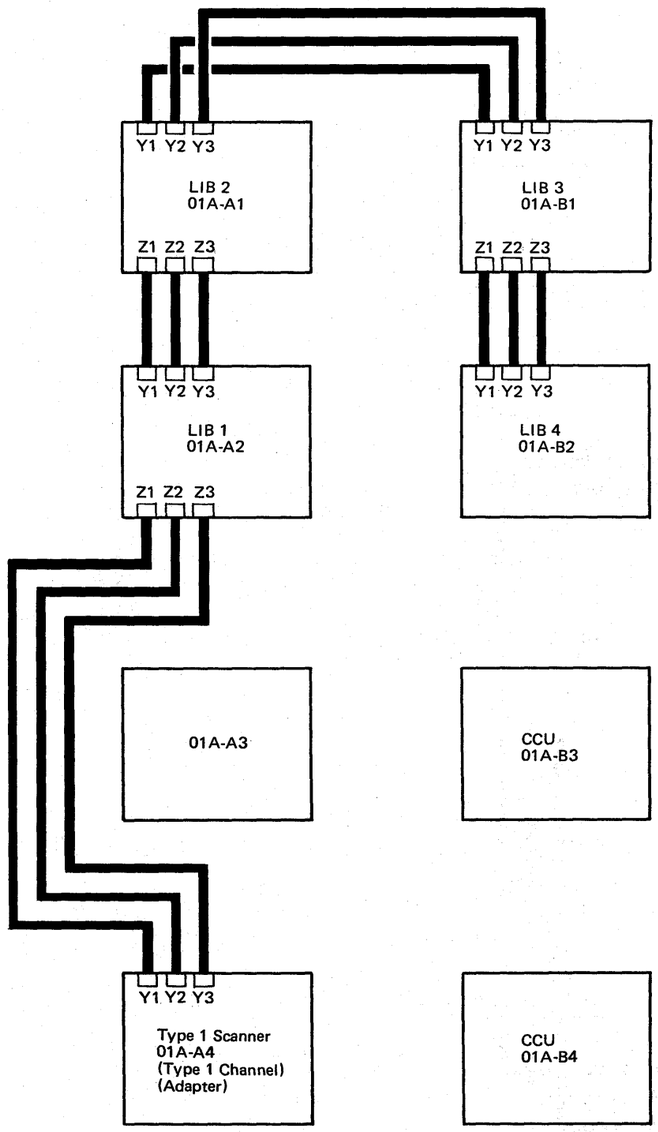
3 Cables to the I/O gate interface connector positions (see C-130 or C-140).

Line Set 12A includes an external cable assembly that provides a cable to a telephone connector for each of its two line interface addresses— (0-1) or (2-3).

Line Set 12B includes an external cable assembly that provides a cable to a CBS Data Coupler for each of its two line interface addresses.

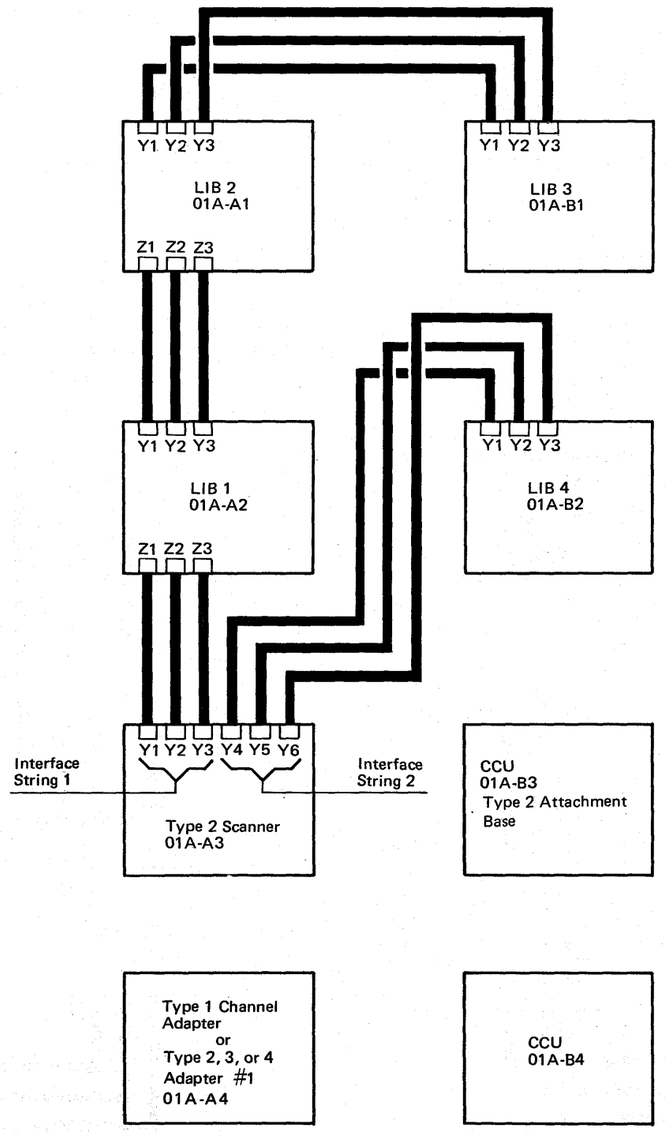
LIB CABLING

TYPE 1 SCANNER



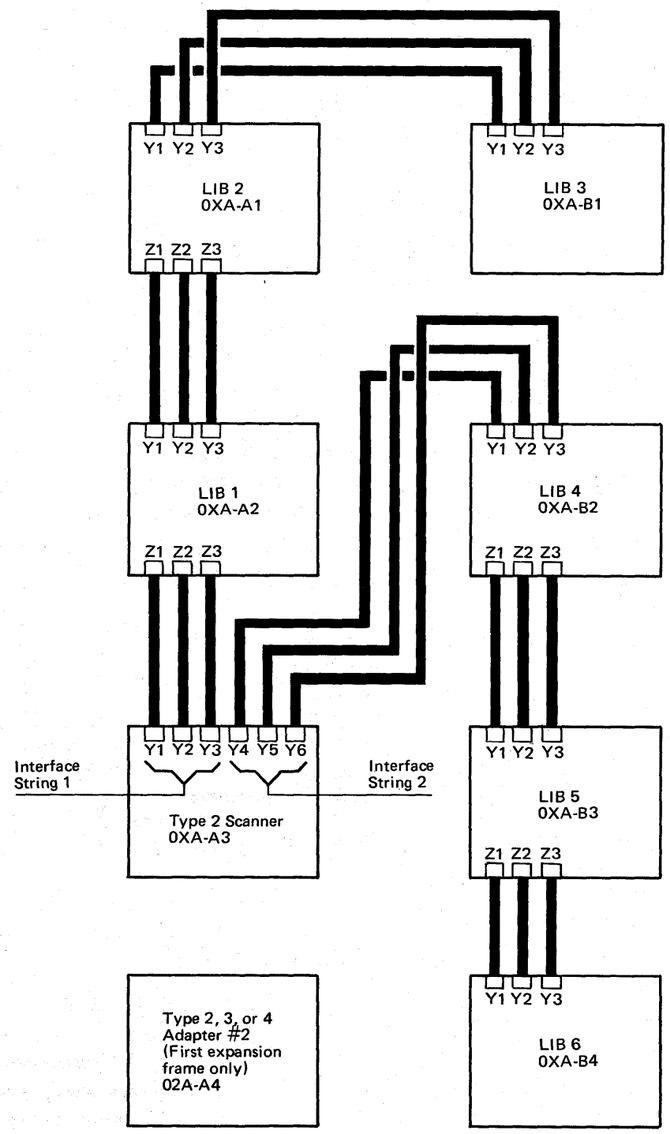
BASIC FRAME
Facing card side of boards.

TYPE 2 SCANNER 1



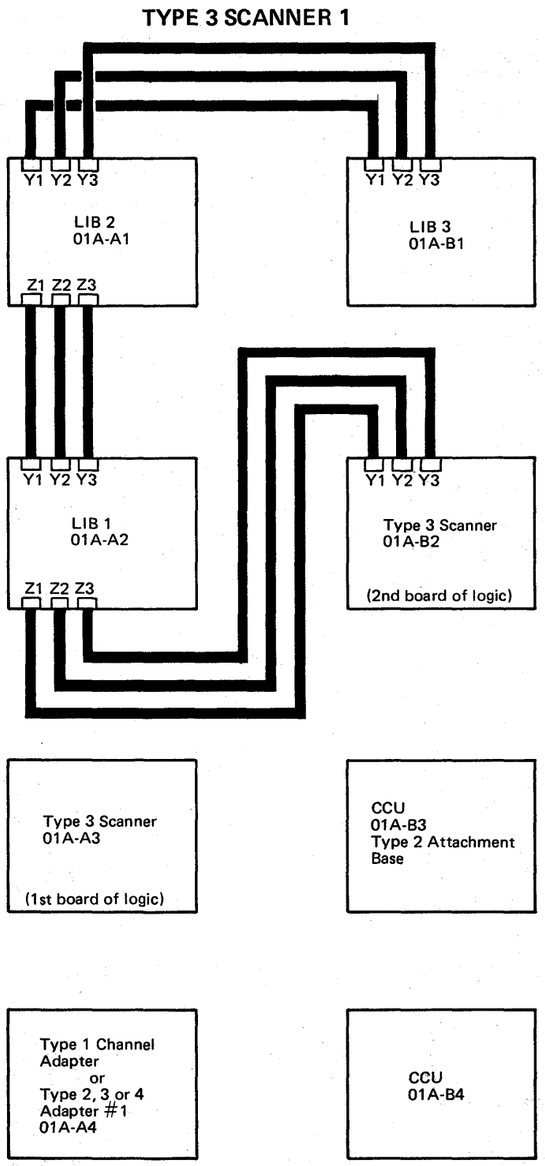
BASIC FRAME
Facing card side of boards.

TYPE 2 SCANNERS 2, 3, 4



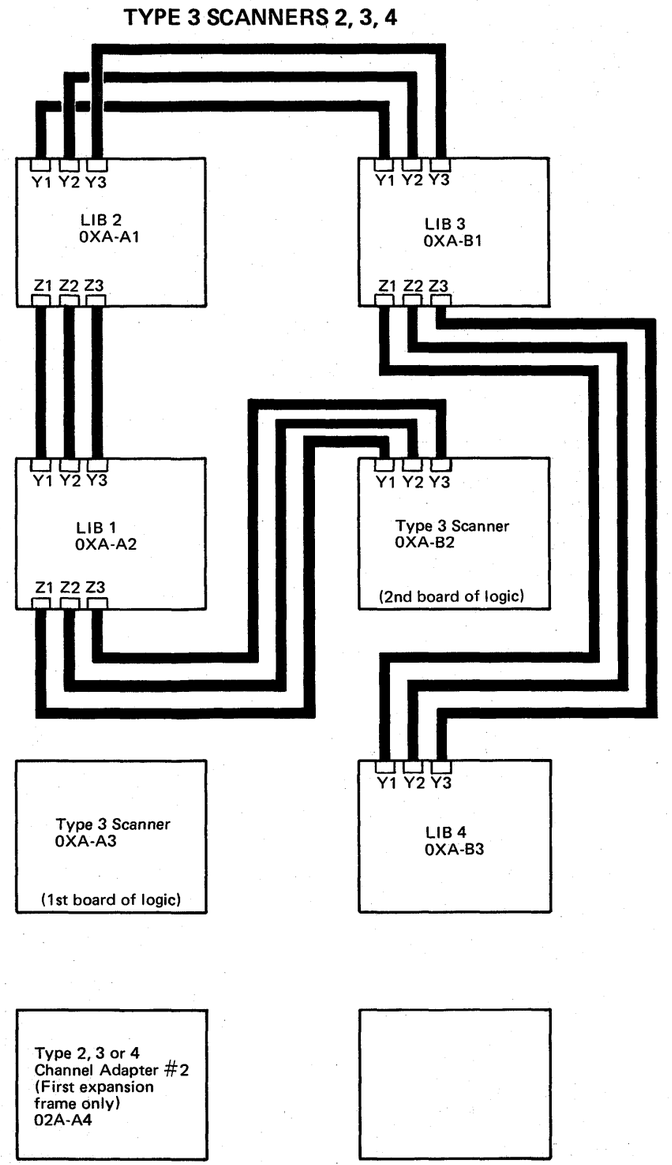
EXPANSION FRAMES
Facing card side of boards.

LIB CABLING (PART 2)



BASIC FRAME

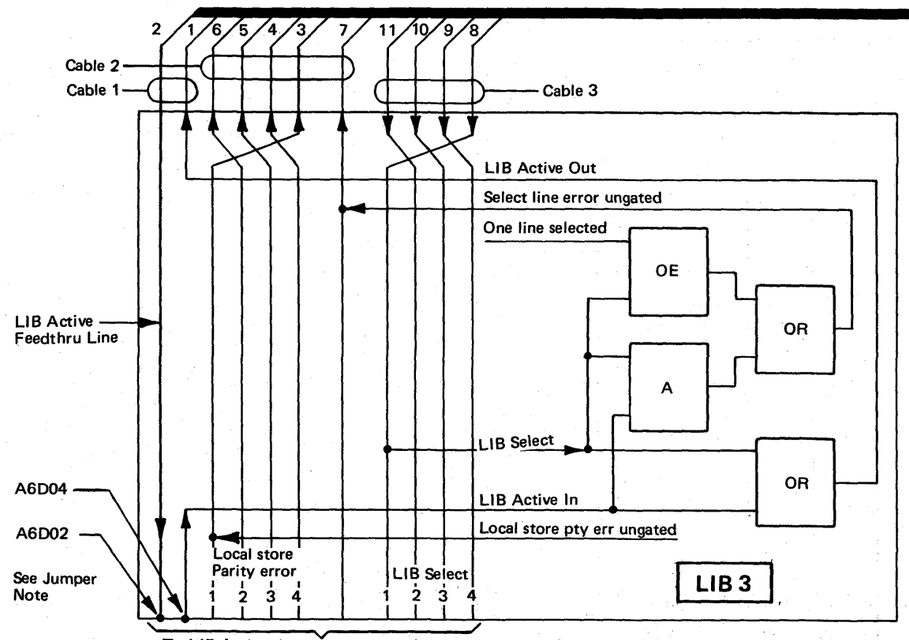
Facing card side of boards.



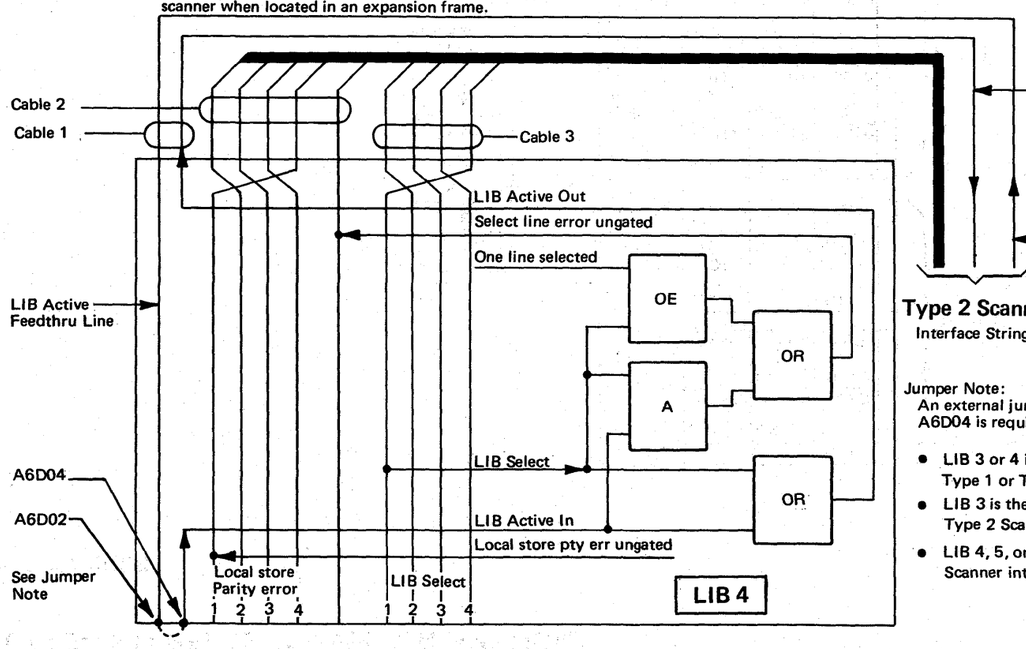
EXPANSION FRAMES

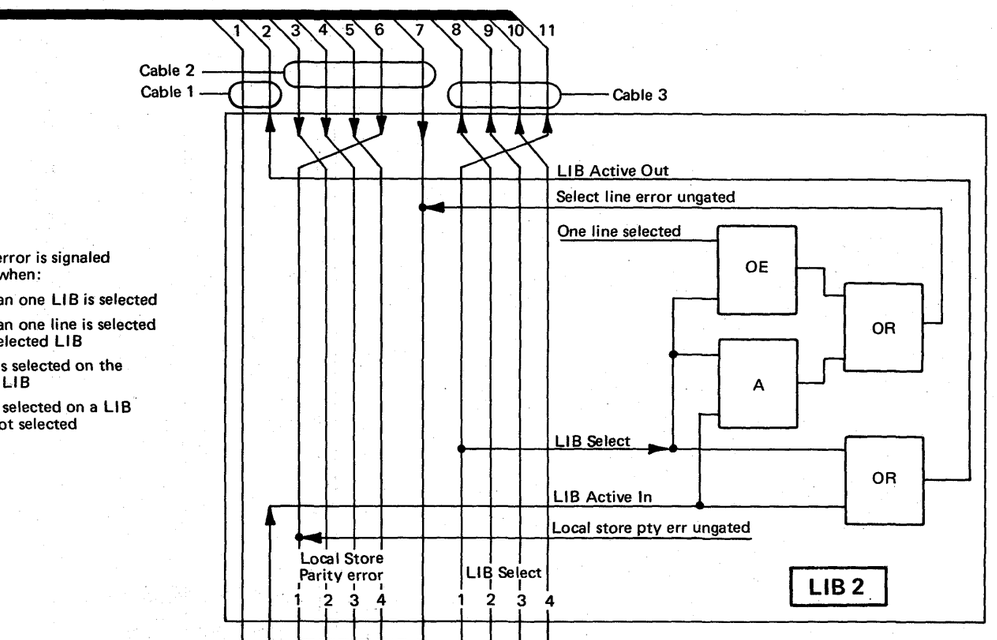
Facing card side of boards.

LIB ADDRESS ERROR AND LOCAL STORE PARITY ERROR



To LIB 4 when it supports a type 1 scanner or a type 3 scanner when located in an expansion frame.





A line address error is signaled to the scanner when:

- More than one LIB is selected
- More than one line is selected on the selected LIB
- No line is selected on the selected LIB
- A line is selected on a LIB that is not selected

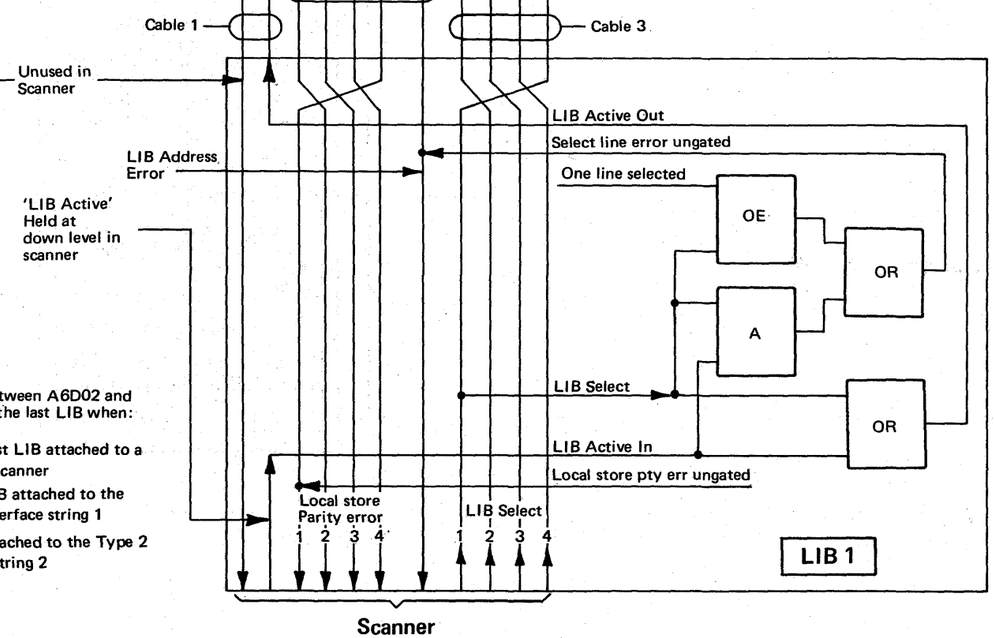
Unused in Scanner

'LIB Active' Held at down level in scanner

Type 2 Scanner
Interface String 2

Jumper Note:
An external jumper between A6D02 and A6D04 is required on the last LIB when:

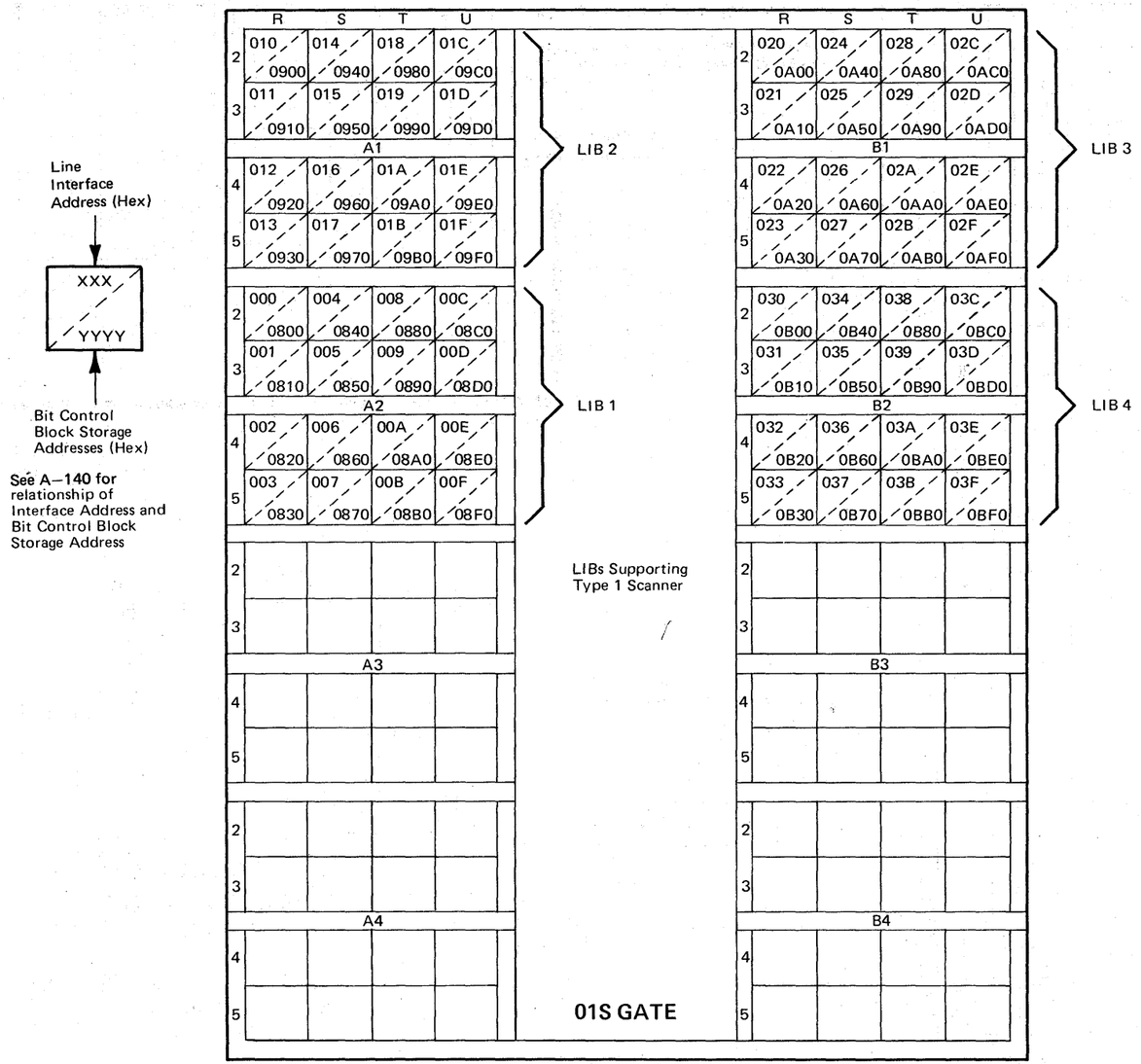
- LIB 3 or 4 is the last LIB attached to a Type 1 or Type 3 Scanner
- LIB 3 is the last LIB attached to the Type 2 Scanner interface string 1
- LIB 4, 5, or 6 is attached to the Type 2 Scanner interface string 2



Scanner
(type 1, type 2, or type 3)

I/O GATE–INTERFACE CONNECTOR POSITIONS

TYPE 1 SCANNER

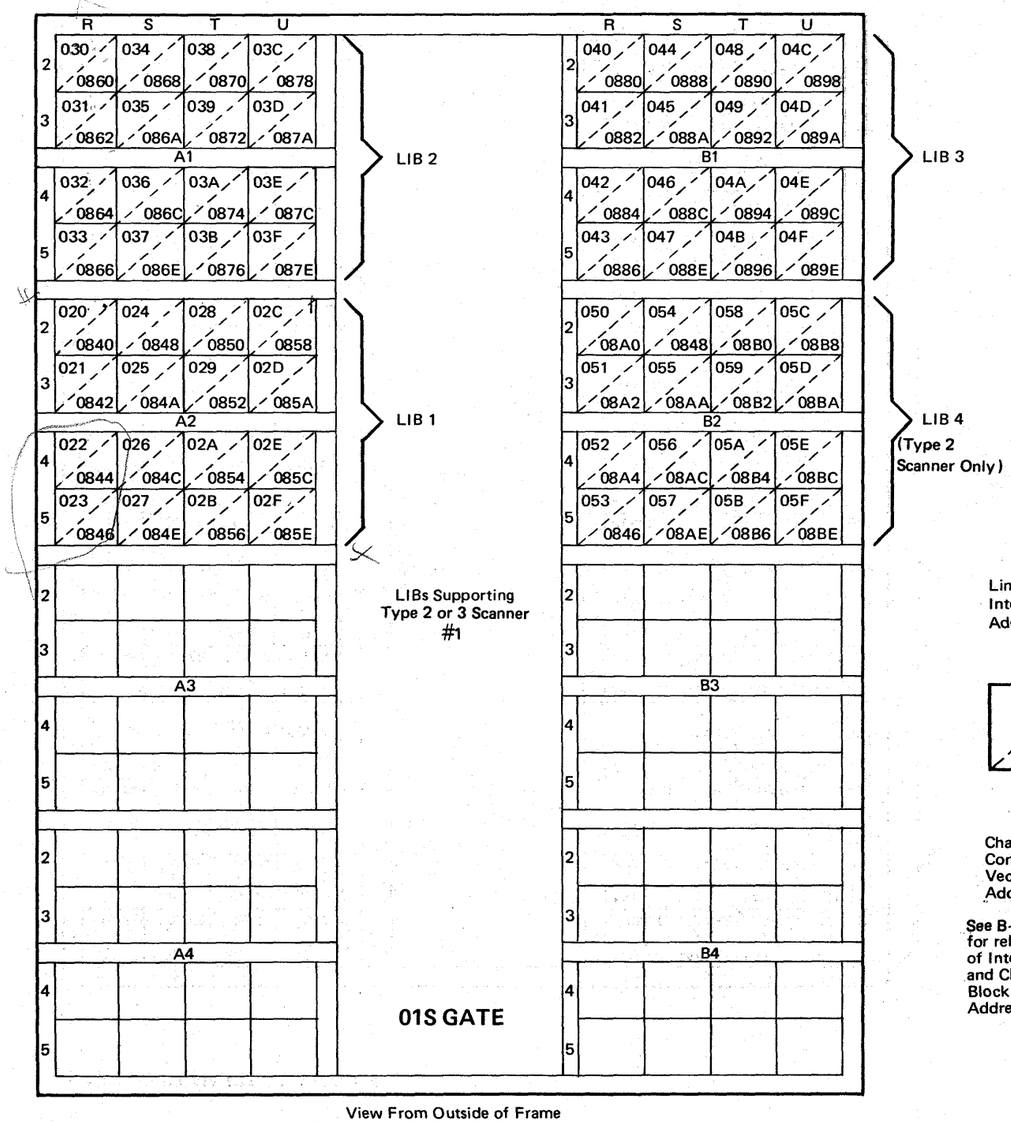


View From Outside of Frame

BASIC FRAME

I/O GATE—INTERFACE CONNECTOR POSITIONS

TYPE 2 OR 3 SCANNER # 1 AND # 2



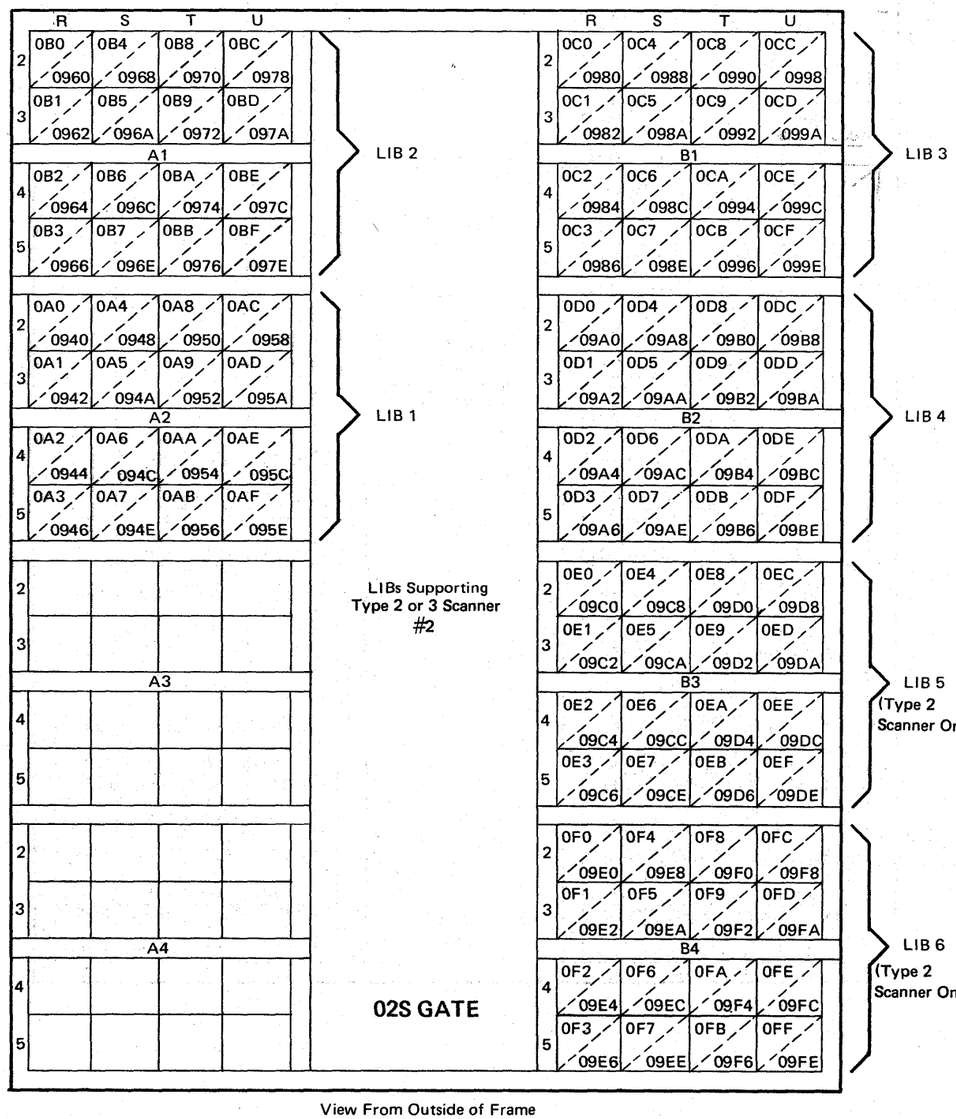
Line Interface Address (Hex)

XXX / YYYY

Character Control Block Vector Storage Address (Hex)

See B—330 for relationship of Interface Address and Character Control Block Vector Storage Address.

View From Outside of Frame
BASIC FRAME



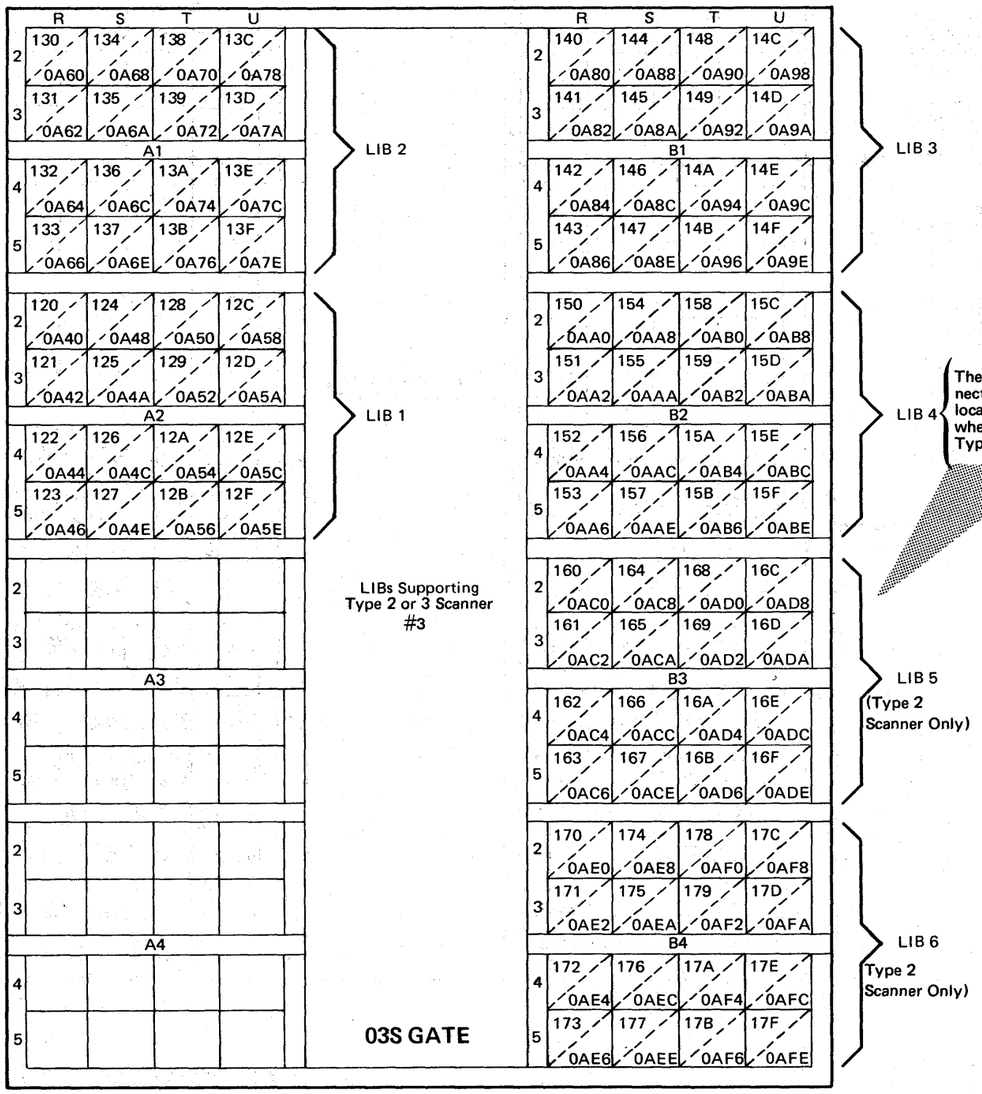
These interface connector positions are located at 02S-B3 when attached to a Type 3 scanner.

Location of the LIB 4 connectors shown above when attached to a Type 3 scanner.

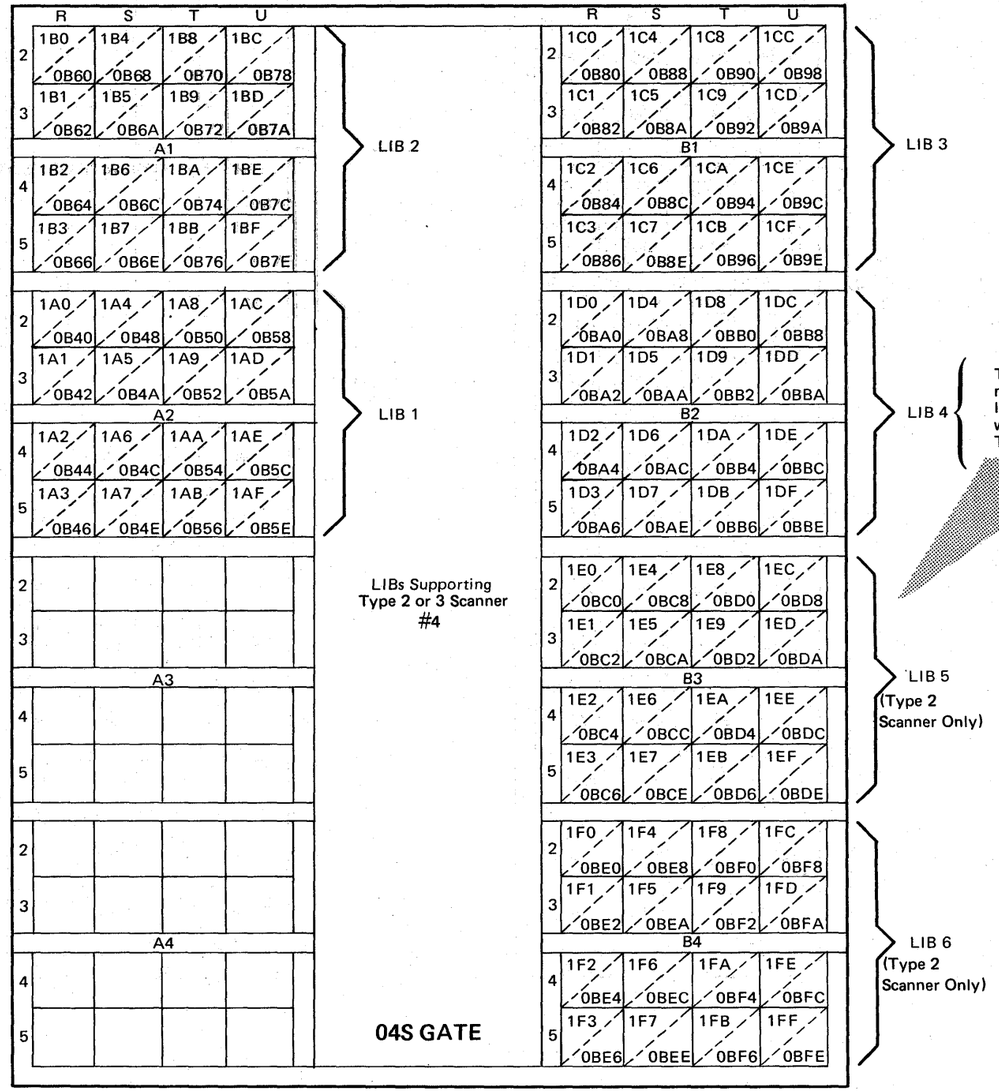
View From Outside of Frame
EXPANSION FRAME 1

I/O GATE—INTERFACE CONNECTOR POSITIONS

TYPE 2 SCANNER #3 AND #4



View From Outside of Frame
EXPANSION FRAME 2



View From Outside of Frame
EXPANSION FRAME 3

LINE SET INDEX

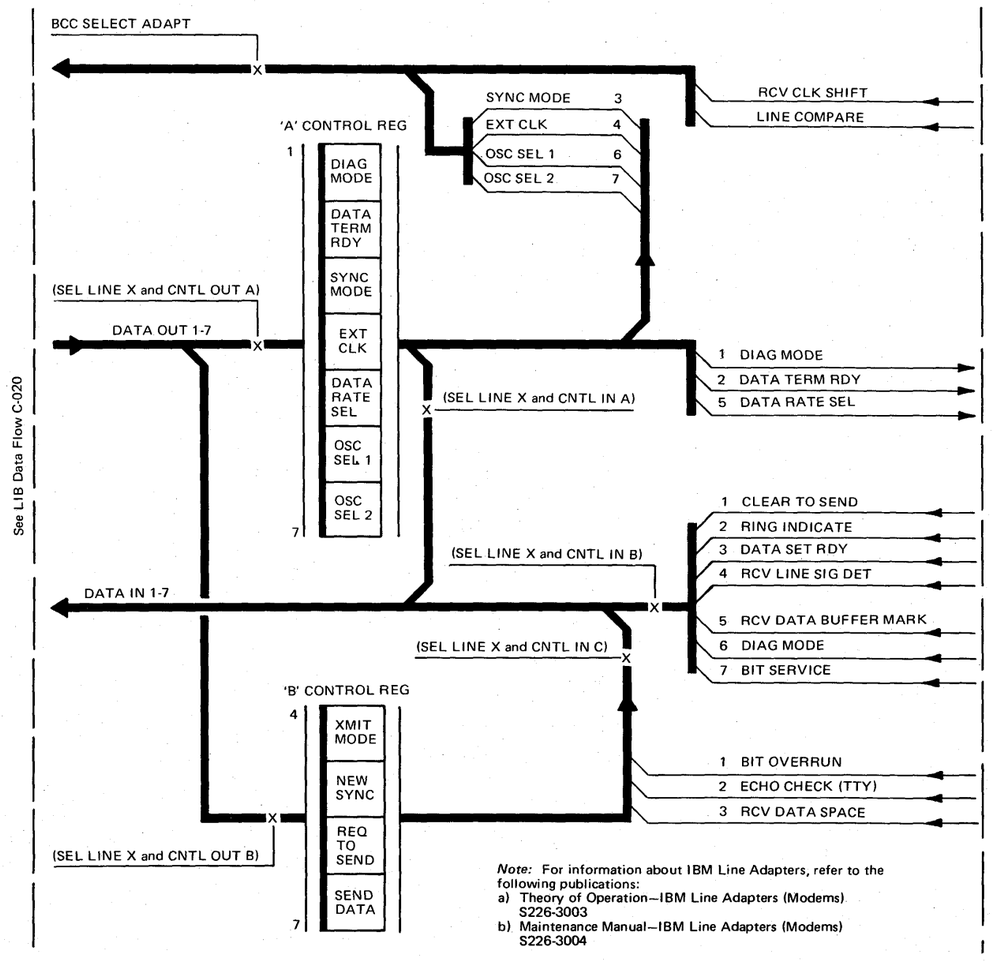
Note: Line sets 1A, 1B, 1C, 1F, and 1H are no longer available for the IBM 3705. The functions these line sets provided are now performed by line set 1D. The cables provided by IBM for the 1D line set depend on the type of communications terminal and its intended use. Refer to *IBM Remote Communications Multiplexers and Terminals Installation Manual—Physical Planning* (GA27-3006) or *IBM Input/Output Equipment Installation Manual—Physical Planning: System/360, System/370, 4300 Processors* (GC22-7064) for information on cables.

LINE SET PAGE REFERENCES

ALD REFERENCES

Line Set	Type	Line Interface Data Flow	Modem/Line Adapter Data Flow	ALD Page	Card Location Chart	Pin Location Chart	Card Jumper Options
1A	Low Speed External Modem Attachment	C–170	——	VB020	VA000	VA003	——
1B	Low Speed Duplex External Modem	C–170	——	VB020	VA000	VA011	——
1C	Low Speed Local Attachment	C–170	C–190	VB020	VA000	VA009	——
1D	Medium Speed External Modem	C–200	——	VB060	VA000	VA004	——
1E	Autocall Unit	C–220	——	VB080	VA000	VA005	——
1F	Medium Speed Local Attach.	C–200	C–190	VB060	VA000	VA010	——
1G	High Speed External Modem	C–230	——	VB100	VA000	VA006	——
1GA	High Speed External Modem	C–232	——	VB160	VA000	VA006	——
1H	Medium Speed Duplex External Modem	C-200	——	VB060	VA000	VA012	——
1J	MIL 188C Modem	C–241	——	VB121	VA000	VA007	VA007
1K	CCITT V.35 Modem	C–243	——	VB140	VA000	VA008	——
1N	Nonswitched Half-Duplex/ Duplex CCITT X.21 Interface	C–245	——	VB200	VA000	VA017	VA017
1R	Switched Duplex CCITT X.21 Interface	C–247	——	VB200	VA000	VA017	VA017
1S	Common Carrier 56,000 bps Attachment	C–243	——	VB140	VA000	VA008	——
1T	High Speed Duplex External Modem	C–230	——	VB100	VA000	VA013	VA013
1TA	High Speed Duplex External Modem	C–232	——	VB160	VA000	VA013	VA013
1U	High Speed Duplex CCITT V.35 Interface	C–243	——	VB140	VA000	VA014	——
1W	High Speed Local Attach, Half-Duplex CCITT V.35 Interface	C–248	——	VB150	VA000	VA015	VA070 (Board Jumper)
1Z	High Speed Local Attach, Duplex CCITT V.35 Interface	C–248	——	VB150	VA000	VA016	VA070 (Board Jumper)
2A	Telegraph (Single Current)	C–250	C–270	VD020	VC000	VC003	VC004
3A	Limited Distance Type 1 Line Adapter — Two-Wire	C–250	Note 1	VF020	VE000	VE003	VE004
3B	Limited Distance Type 1 Line Adapter — Four-Wire	C–250	Note 1	VF040	VE000	VE003	VE004
4A	Limited Distance Type 2 Line Adapter	C–250	Note 1	VH020	VG000	VG003	VG006
4B	Leased Line, Line Adapter—Two-Wire	C–250	Note 1	VH040	VG000	VG004	VG007
4C	Leased Line, Line Adapter—Four-Wire	C–250	Note 1	VH060	VG000	VG005	VG008
5A	2400 bps Leased pt-pt Integrated Modem	C–280	C–380	VJ100	VJ000	VJ003	VJ004
5B	2400 bps Multipoint Control Integrated Modem	C–280	C–380	VJ100	VJ000	VJ003	VJ004
6A	2400 bps Switched Integrated Modem	C–280	C–380	VL100	VL000	VL003	VL004-5
LIB 7	2400 bps Switched Integrated Modem with ACO	C–280	C–380	VN100	VN000	VN003	VN004-5
8A	1200 bps Leased Integrated Modem	C–300	——	VQ100	VQ000	VQ003	VQ005
8B	1200 bps Switched Integrated Modem	C–300	——	VQ100	VQ000	VQ003	VQ005
9A	1200 bps Switched Integrated Modem with ACO	C–300	——	VS100	VS000	VS003	VS004-5
10A	1200 bps Leased Duplex Data Integrated Modem	C–314	——	VU100	VU000	VU003	VU000
11A	2400 bps Leased pt-pt Duplex Data Integrated Modem	C–318	C–380	VW100	VW000	VW003	VW000
11B	2400 bps Multipoint Control Duplex Data Integrated Modem	C–318	C–380	VW100	VW000	VW003	VW000
12A	1200 bps Leased Integrated Modem w/Bi-directional Interrupt Signal	C–300	——	VX100	VX000	VX005	VX003–4
12B	1200 bps Switched Integrated Modem w/Bi-directional Interrupt Signal	C–300	——	VX100	VX000	VX005	VX003–4

LINE SET GENERAL DATA FLOW



Note: For information about IBM Line Adapters, refer to the following publications:
a) Theory of Operation—IBM Line Adapters (Modems) S226-3003
b) Maintenance Manual—IBM Line Adapters (Modems) S226-3004

LINE SET 1A, 1B, 1C, 1D

Note: Line sets 1A, 1B, and 1C are no longer available for the IBM 3705. The functions these line sets provided are not performed by line set 1D. The cables provided by IBM for the 1D line set depend on the type of communications terminal and its intended use. Refer to *IBM Remote Communications Multiplexers and Terminals Installation Manual—Physical Planning* (GA27-3006) or *IBM Input/Output Equipment Installation Manual—Physical Planning: System/360, System/370, 4300 Processors* (GC22-7064) for information on cables.

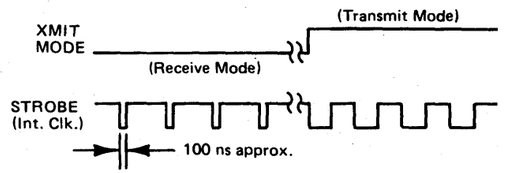
LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the communication line adapter (modem, IBM Line Adapter, telegraph adapter).

1. The communication line adapter status, RCV buffer status, and 'bit service trigger' status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication line adapter, and 'xmit data' bits to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C.

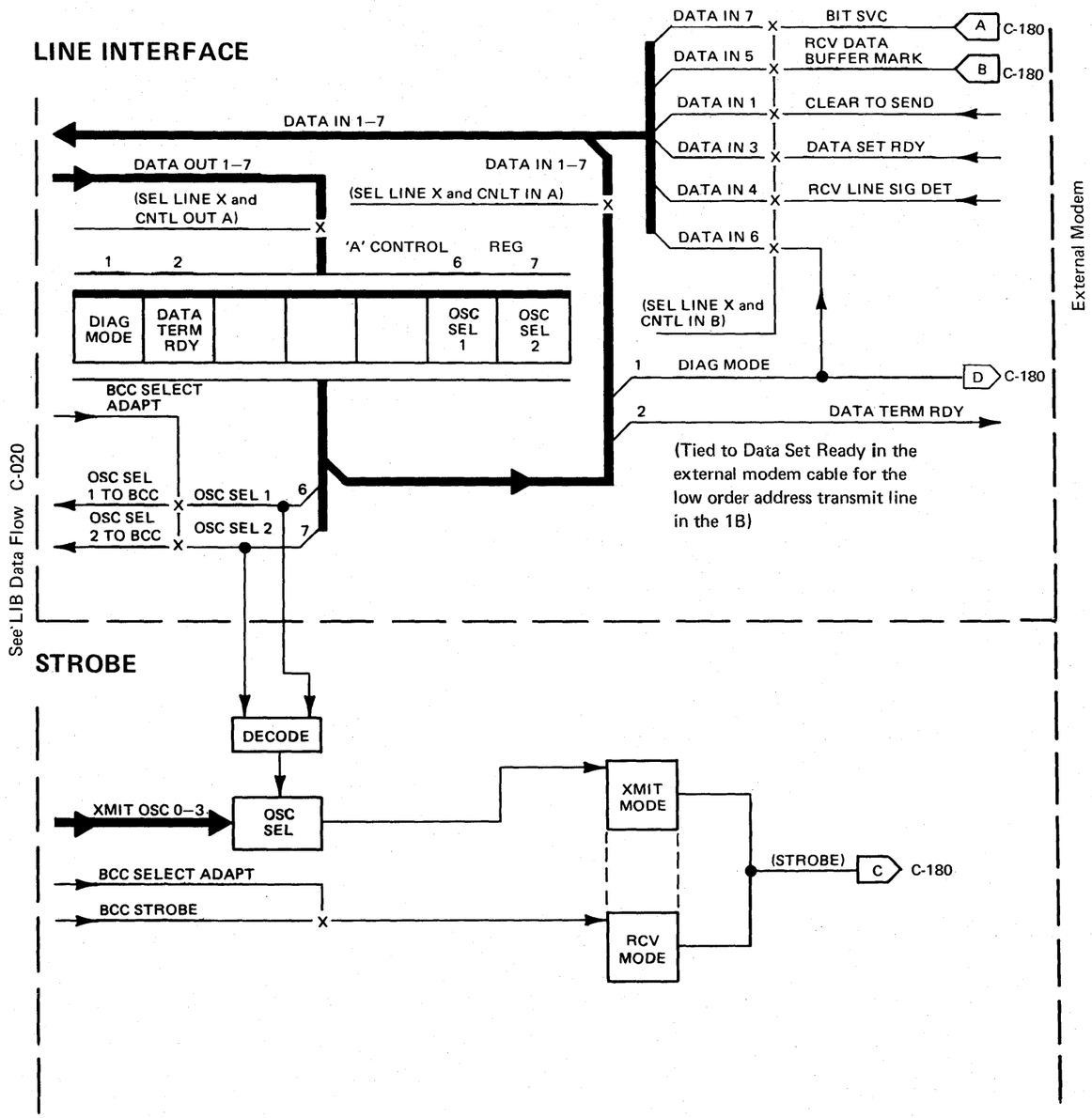
STROBE

1. When Xmit Mode is not set, receive mode is assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

Line Set 1B consists of 2 addresses. The low order address is the transmit line and the high order address is the receive line. Both interfaces share a common external cable for attaching to a single full-duplex modem. See VA011 for the external cable pin connections.



LINE SET 1A, 1B, 1C, 1D (PART 2)

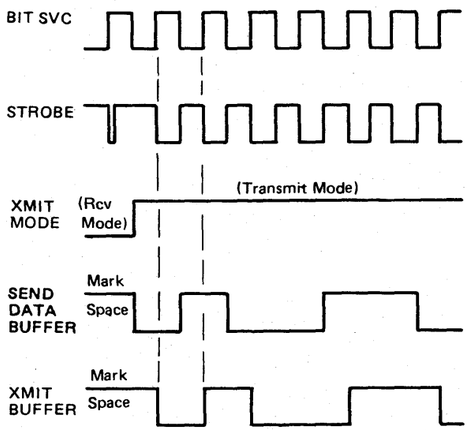
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

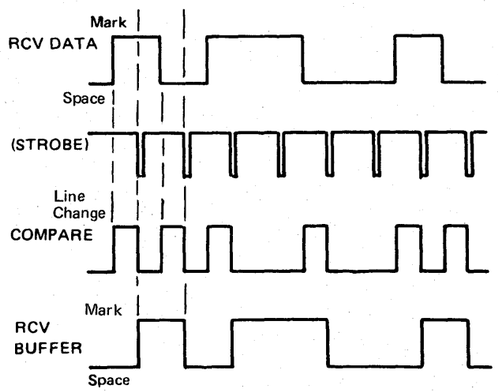
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the EIA level of the communication line.



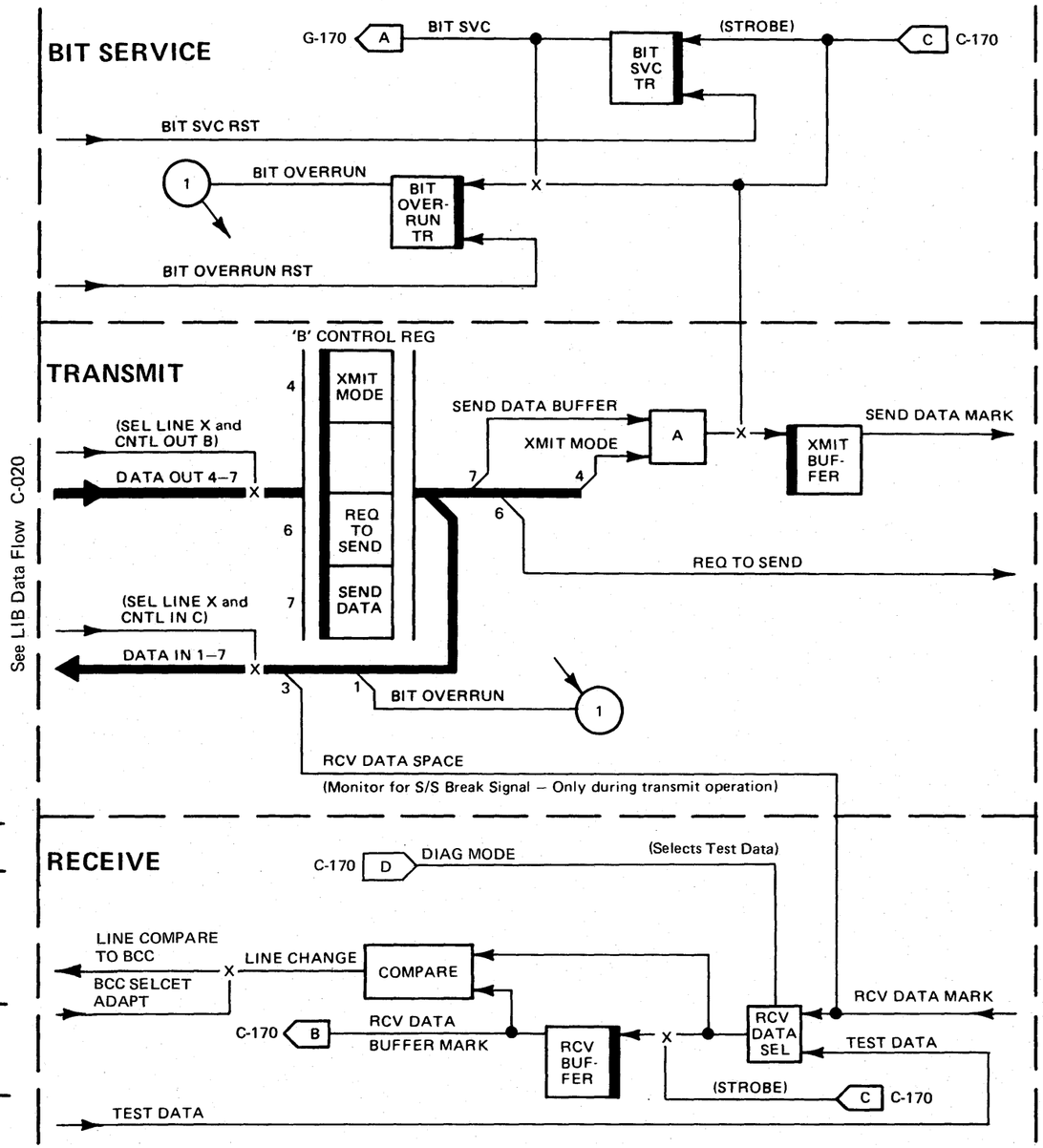
Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



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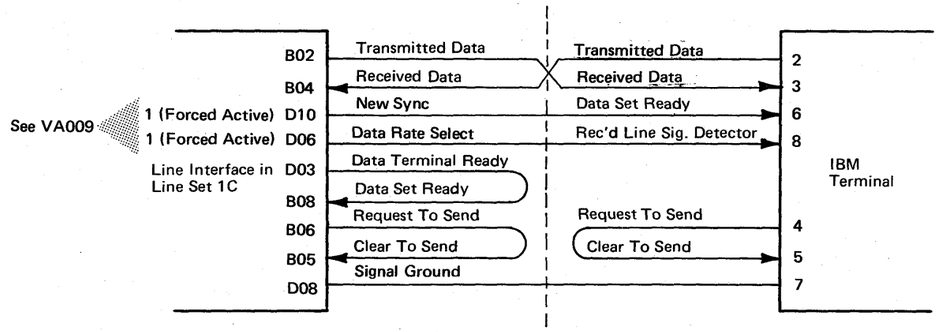
LOCAL ATTACHMENT INTERFACE

Note: Line sets 1C and 1F are no longer available for the IBM 3705. The functions these line sets provided are now performed by line set 1D. The cables provided by IBM for the 1D line set depend on the type of communications terminal and its intended use. Refer to *IBM Remote Communications Multiplexers and Terminals Installation Manual—Physical Planning* (GA27-3006) or *IBM Input/Output Equipment Installation Manual—Physical Planning: System/360, System/370, 4300 Processors* (GC22-7064) for information on cables.

LINE SET 1C OR 1D

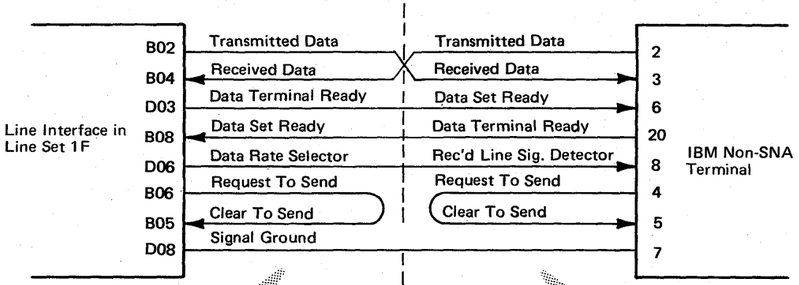
Data flow for line set 1C is the same as line set 1A.

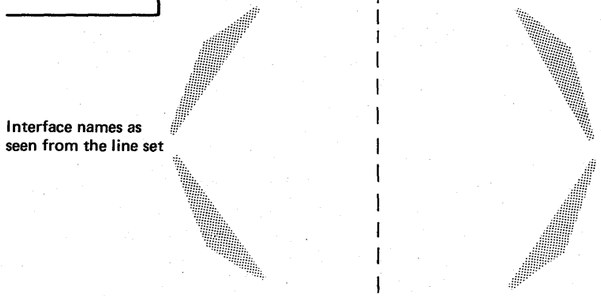


LINE SET 1F OR 1D (Non-SNA Terminals)

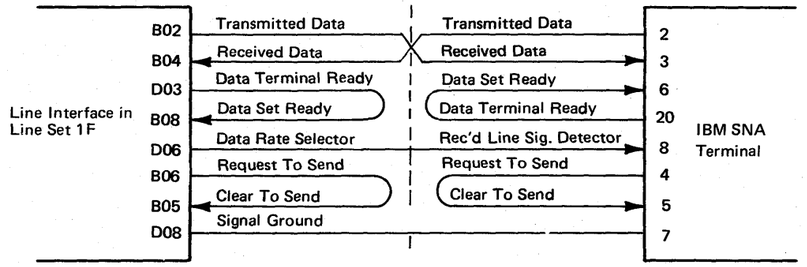
Data flow for line set 1F is the same as line set 1D.

The control program must activate Data Rate Select since this signal drives the terminal's Received Line Signal Detector circuit.





LINE SET 1F OR 1D (SNA Terminals)



LINE SET 1D, 1F, 1H

Note: Line sets 1F and 1H are no longer available for the IBM 3705. The functions these line sets provided are now performed by line set 1D. The cables provided by IBM for the 1D line set depend on the type of communications terminal and its intended use. Refer to *IBM Remote Communications Multiplexers and Terminals Installation Manual—Physical Planning* (GA27-3006) or *IBM Input/Output Equipment Installation Manual—Physical Planning: System/360, System/370, 4300 Processors* (GC22-7064) for information on cables.

LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the communication adapter (external modem—1D and 1H, or the local attachment—1F).

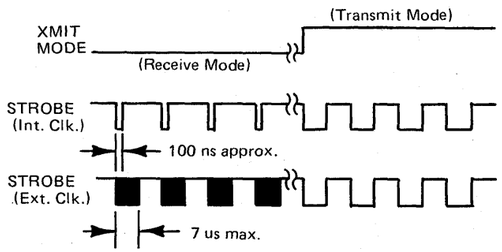
Line Set 1H (Duplex with an External Modem)

This line set consists of a transmit line interface on an even address and a receive line interface on an odd address. Hardware is present in this line set for the transmit address where the modem interface lines are marked with 20 . Hardware is present in this line set for the receive address where the modem interface lines are marked with 18 .

1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter, during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A, is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication adapter, and xmit data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B, is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line, are also transferred to the scanner during a CNTL IN C.

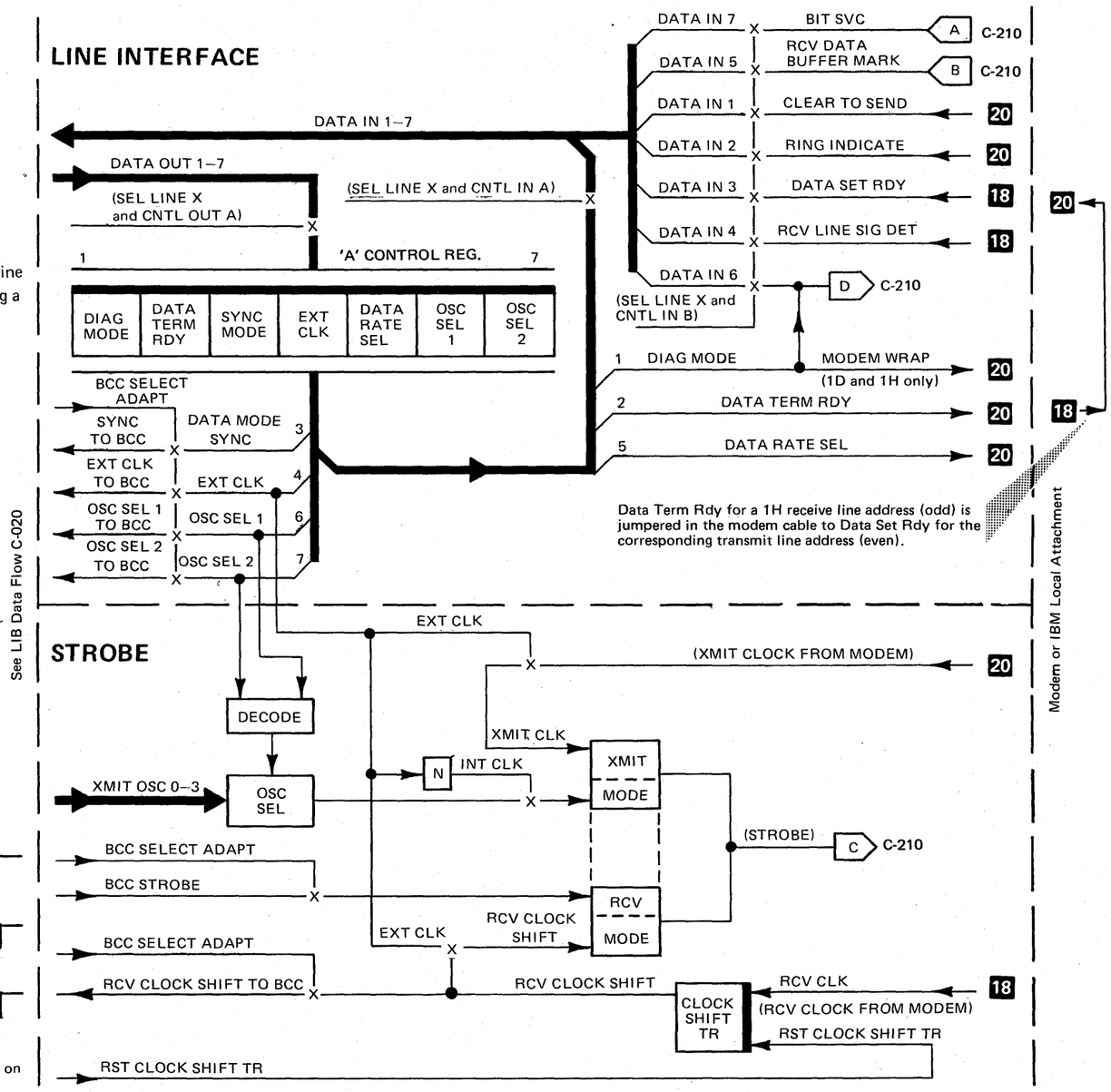
STROBE

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the modem clock (external clocking).



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

See C-190 for line set 1F jumper configurations in the local attachment cable.



LINE SET 1D, 1F, 1H (PART 2)

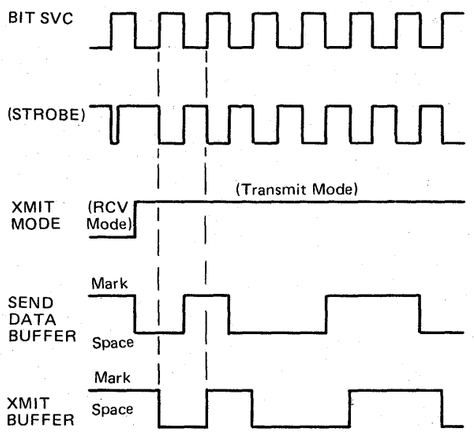
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

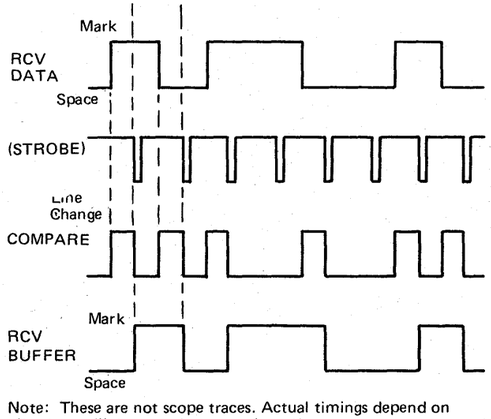
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the EIA level of the communication line.



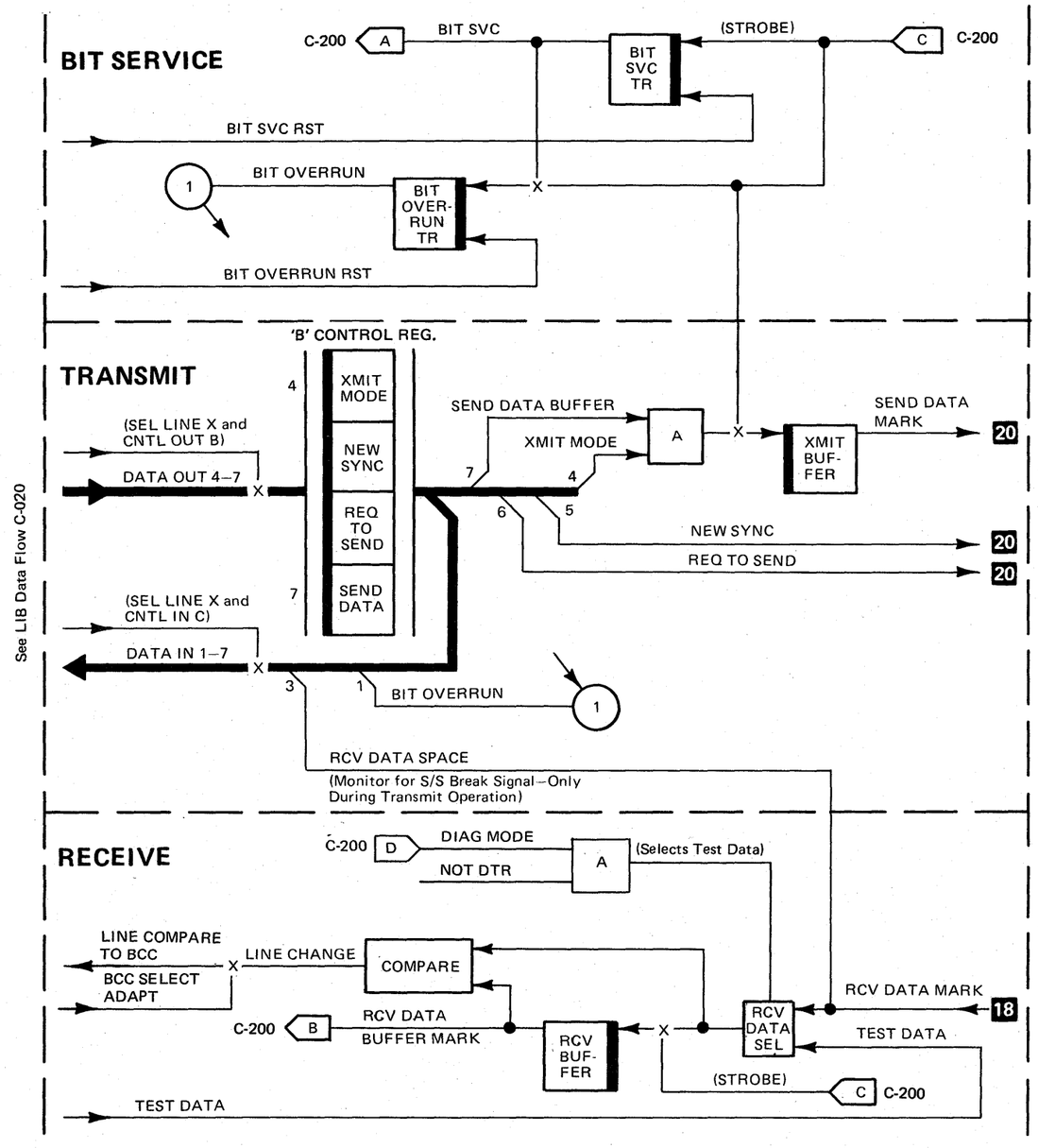
Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



0 0 0

LINE SET 1E

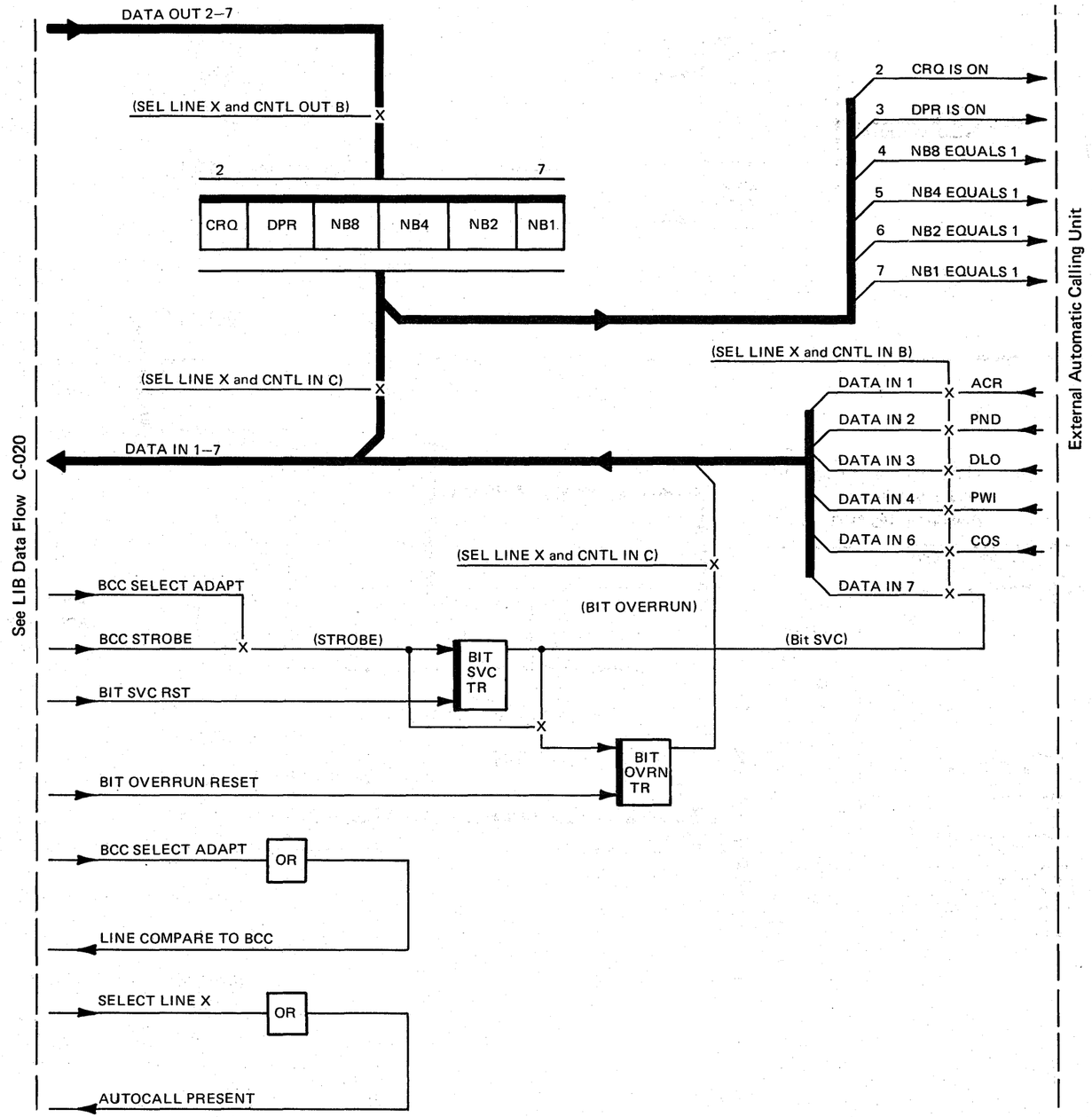
The Auto Call interface is a buffer for status and data transferred between the scanner and the external Automatic Calling Unit (ACU).

1. ACU status is transferred to the scanner during a CNTL IN B.
2. The scanner transfers information to the ACU during a CNTL OUT B (after a 'bit service' request).
3. The information, transferred during the previous CNTL OUT B, is verified during a CNTL IN C.

BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the Auto Call interface. 'Bit service' is the Auto Call interface request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger. 'Strobe' pulses are obtained from the 'BCC strobe' pulses (derived from internal oscillator 0).
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.



LINE SET 1G, 1T

LINE SET 1T (High Speed Duplex External Modem)

Line Set 1T consists of two 1G line sets cabled to a single external modem. Each line interface requires a single partition. Partitions must have adjacent addresses (0 and 2, 4 and 6, 8 and A, C and E). The transmit address must be the low order address (0, 4, 8 or C) and the receive address must be the high order address (2, 6, A or E).

The hardware for transmit and hardware for receive are identical, and for this illustration they are shown combined, but actually they are independent of each other, both in hardware and operation. Hardware used for transmit operations is marked with T, and hardware used for receive operations is marked with R.

See VA013 for how the modem signal lines are connected to the line interfaces.

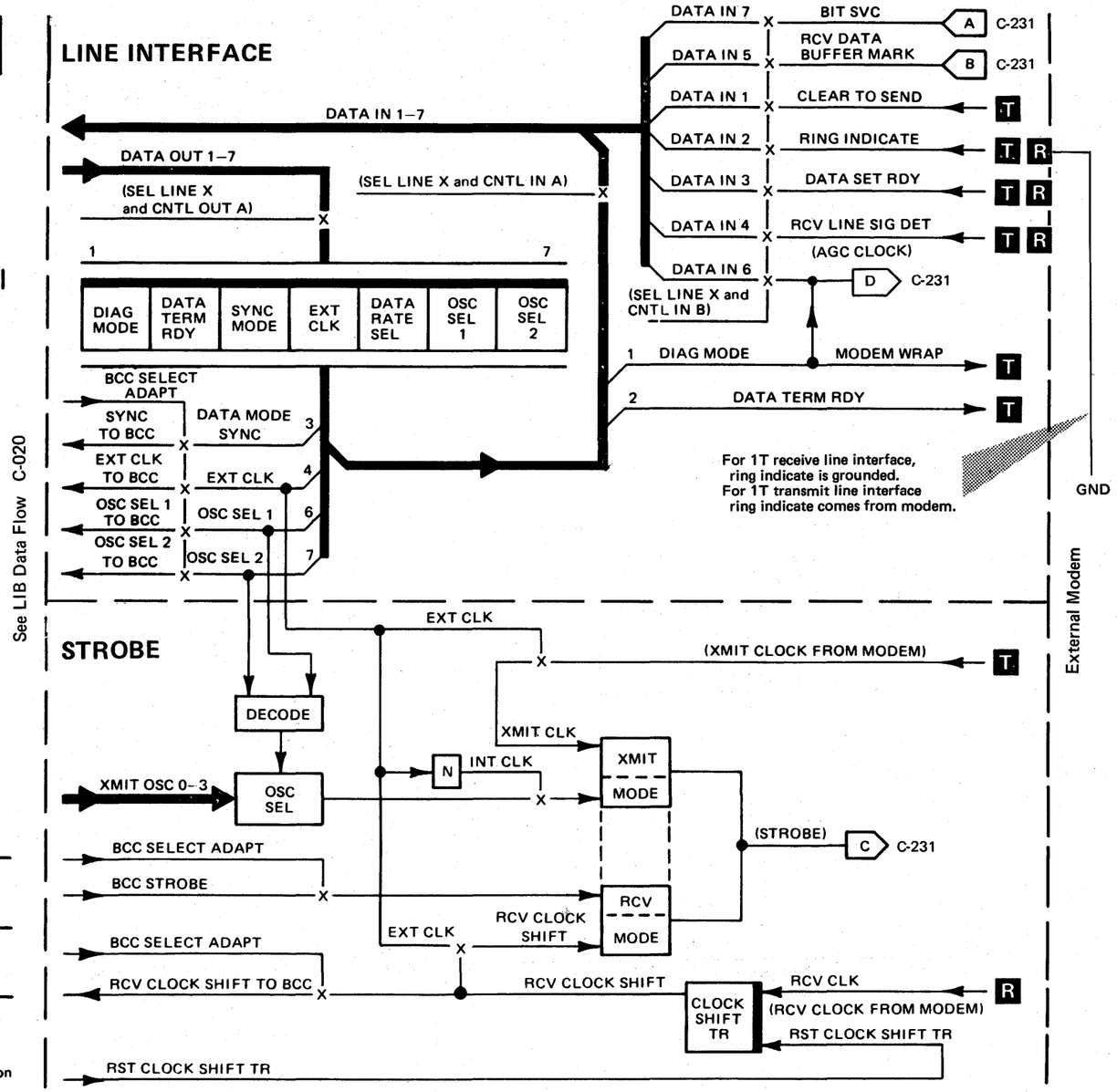
LINE INTERFACE

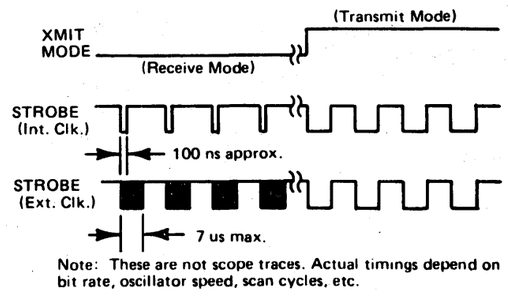
The line interface is a buffer to status and data, transferred between the scanner and the modem.

1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication line adapter, and 'xmit data' bits to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C.

STROBE

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the modem clock (external clocking).





Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

LINE SET 1G, 1T (PART 2)

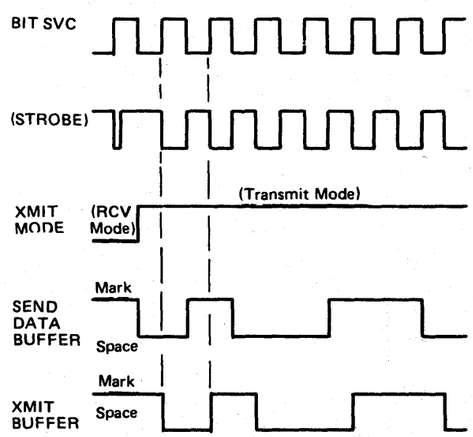
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

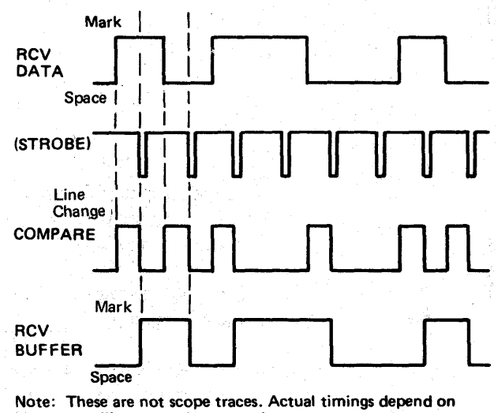
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE)
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the Digital level of the communication line.



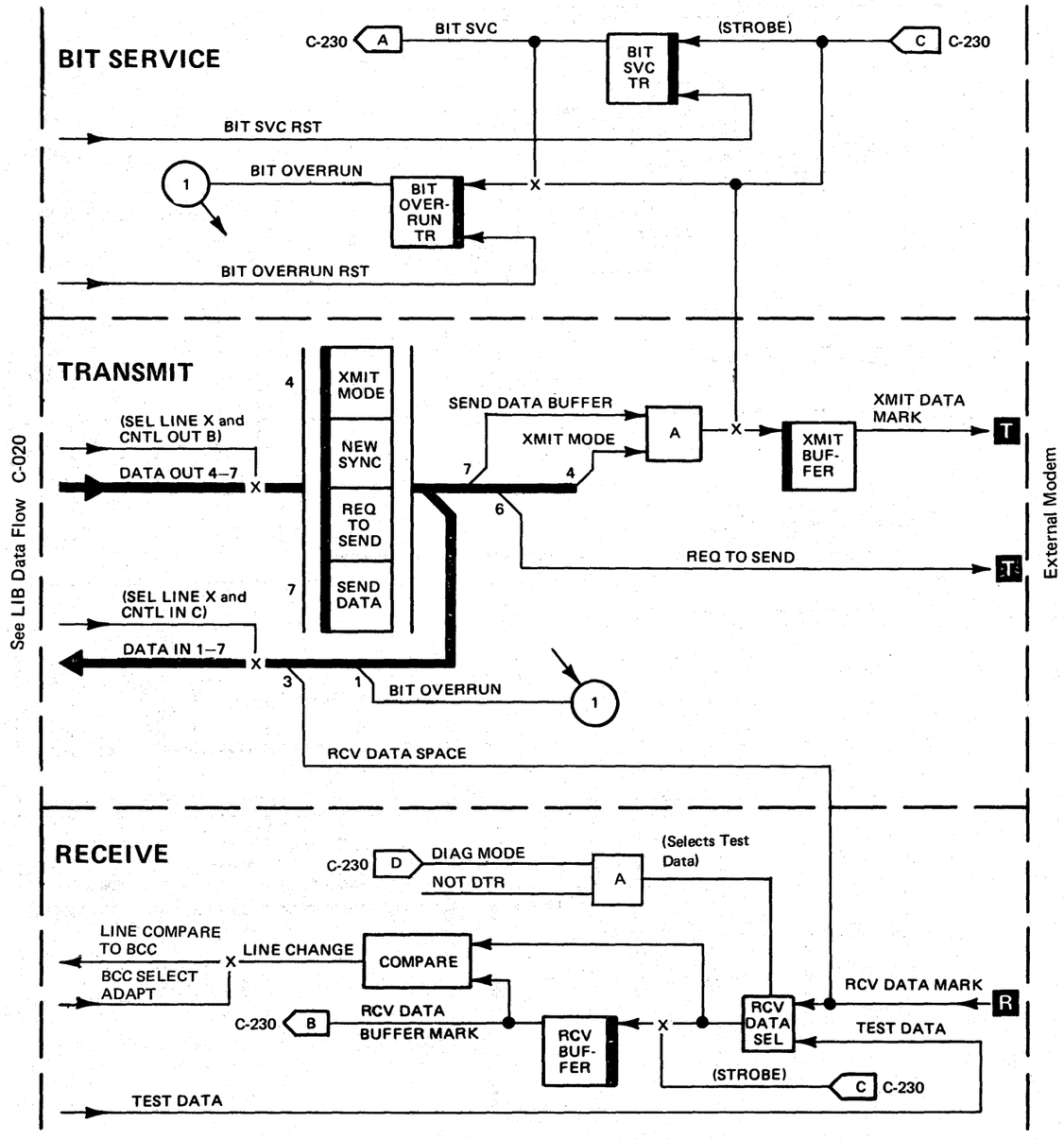
Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 1GA, 1TA

LINE SET 1TA (High Speed Duplex External Modem)

Line Set 1TA consists of two 1GA line sets cabled to a single external modem. Each line interface requires a single partition. Partitions must have adjacent addresses (0 and 2). The transmit address must be the low order address (0) and the receive address must be the high order address (2).

The hardware for transmit and hardware for receive are identical, and for this illustration they are shown combined, but actually they are independent of each other, both in hardware and operation. Hardware used for transmit operations is marked with T, and hardware used for receive operations is marked with R.

See VA013 for how the modem signal lines are connected to the line interfaces.

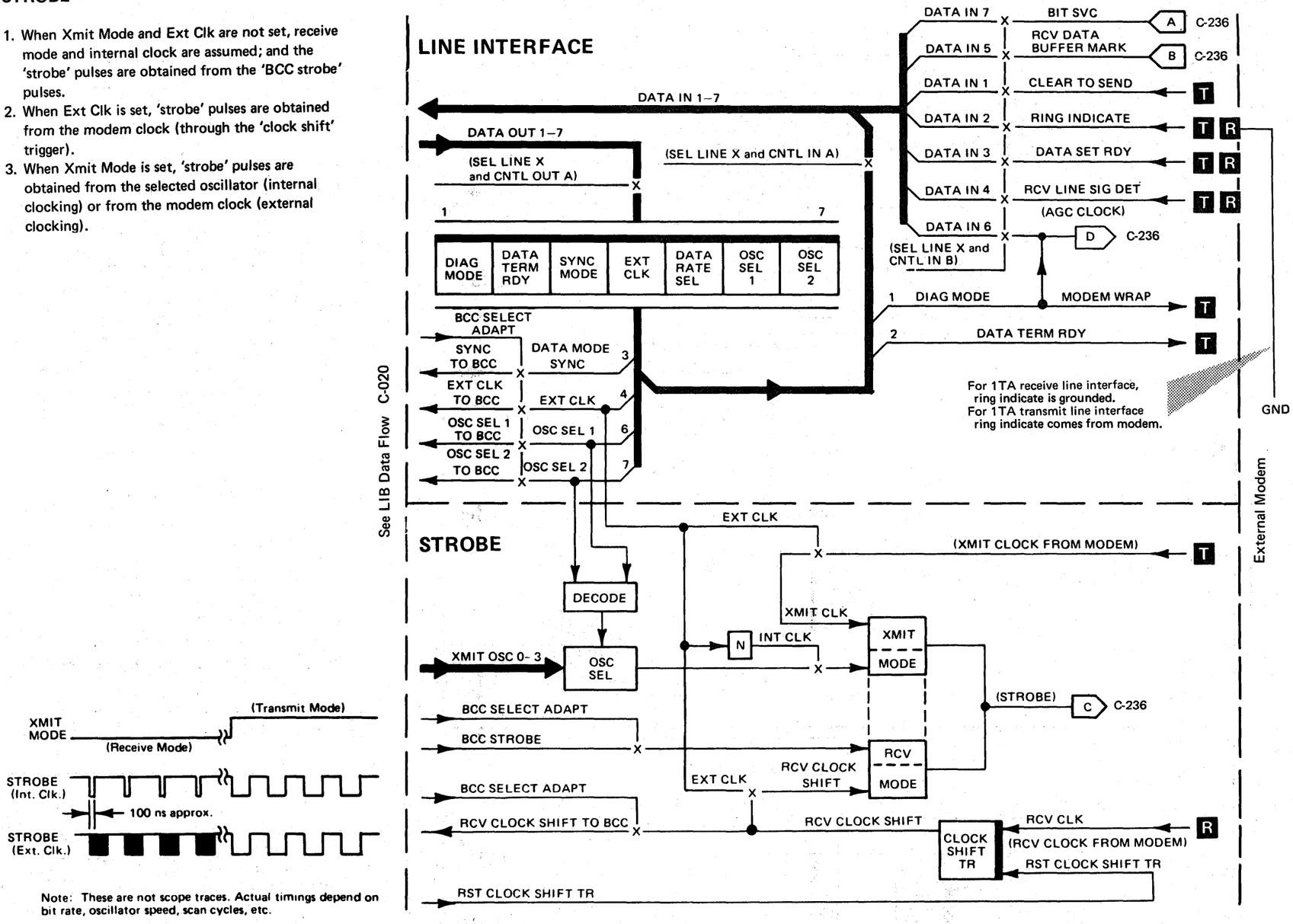
LINE INTERFACE

The line interface is a buffer to status and data, transferred between the scanner and the modem.

1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication line adapter, and 'xmit data' bits to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C.

STROBE

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the modem clock (external clocking).



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

LINE SET 1GA, 1TA (PART 2)

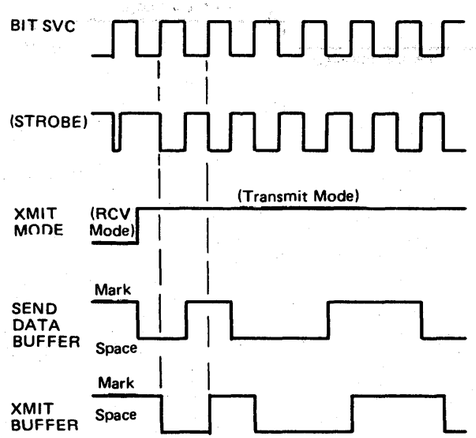
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. The additional stage of bit buffering used in the transmit and receive lines of the 1GA and 1TA line sets is not used on the 1G and 1T line sets.

TRANSMIT

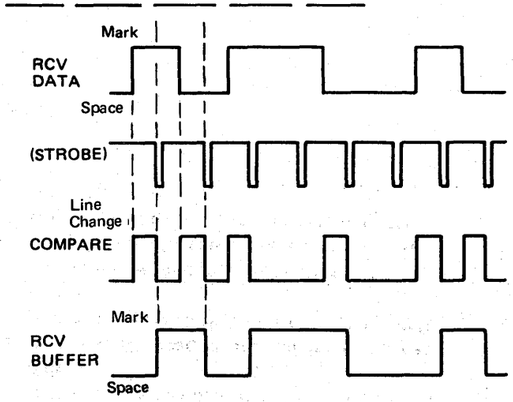
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE)
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the Digital level of the communication line.



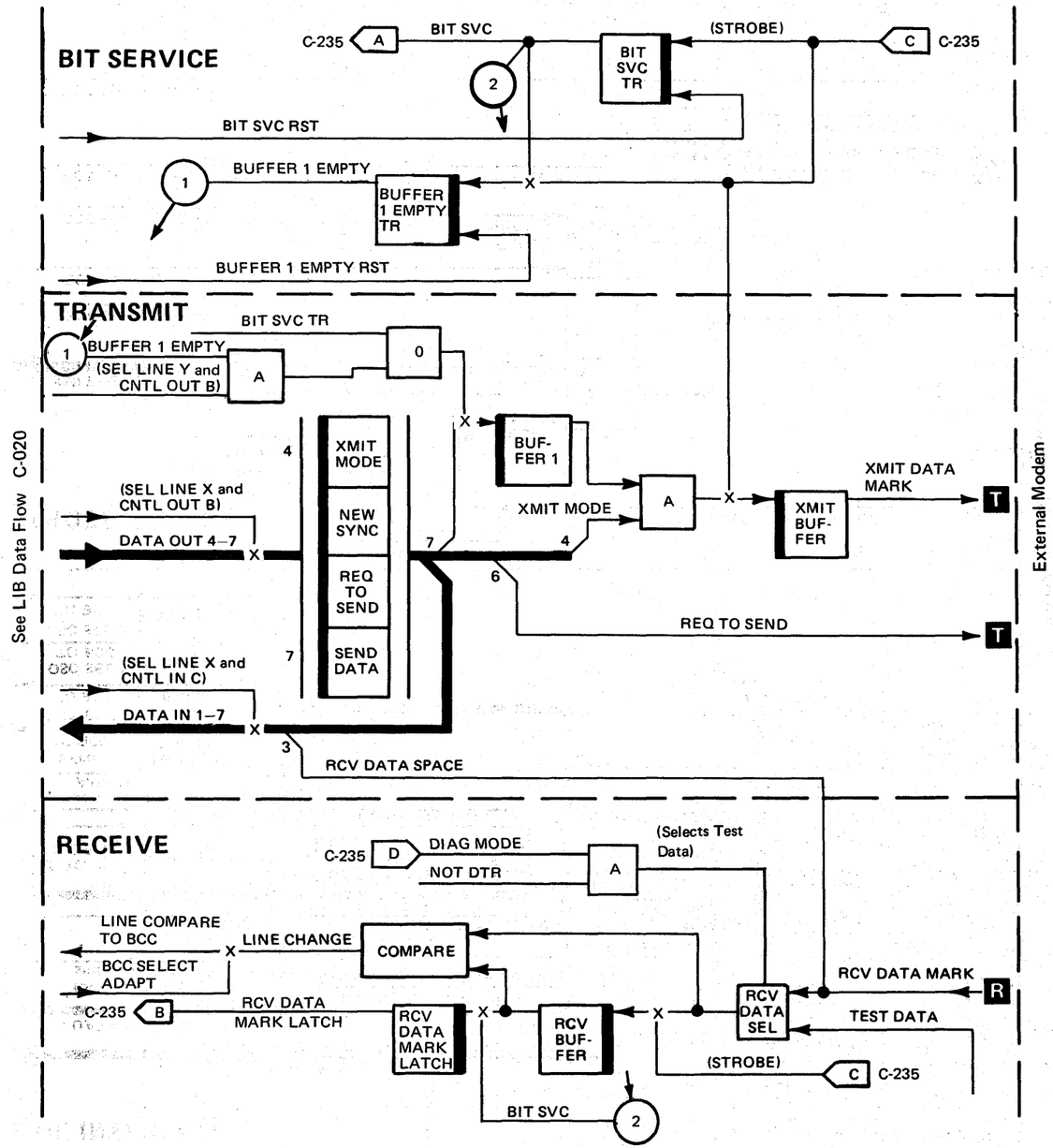
Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 1J

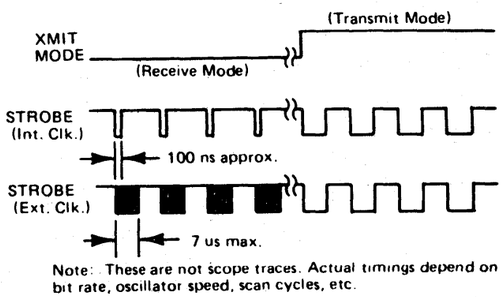
LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the communication line adapter or modem.

1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and transmits a data bit to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C. (The type 2 scanner ignores 'bit overrun' and holds 'bit overrun reset' on solid.)

STROBE

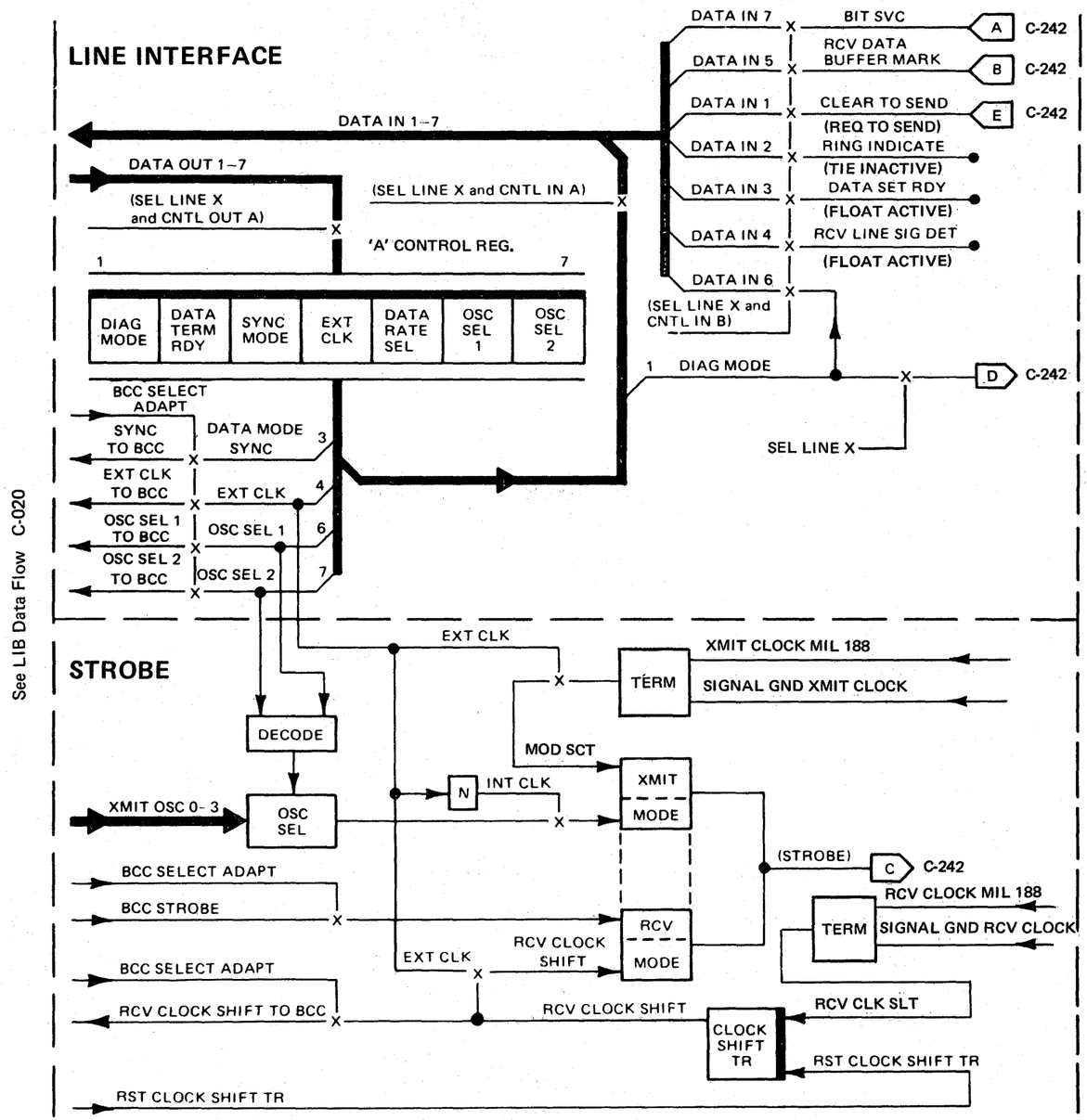
1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the modem clock (external clocking).



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

EXTERNAL CAPACITOR JUMPER

Each line set 1J must have an external capacitor installed. The value of the capacitor is determined by the speed of the line. Refer to VA007 for the capacitor value and plugging location.



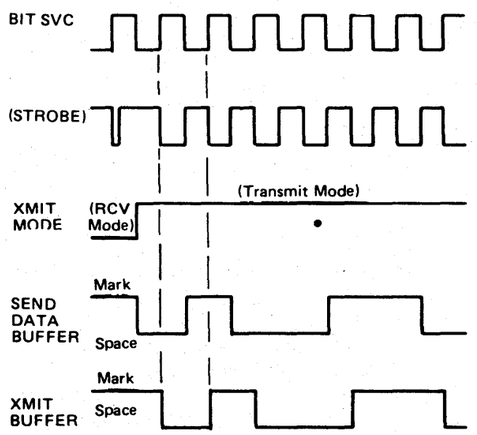
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

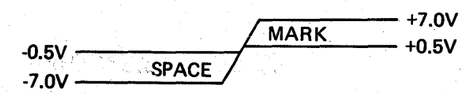
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE)
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the MIL 188C level of the communication line. The driver circuit outputs are:

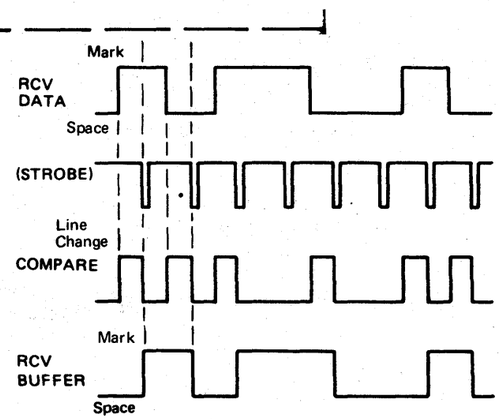


Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

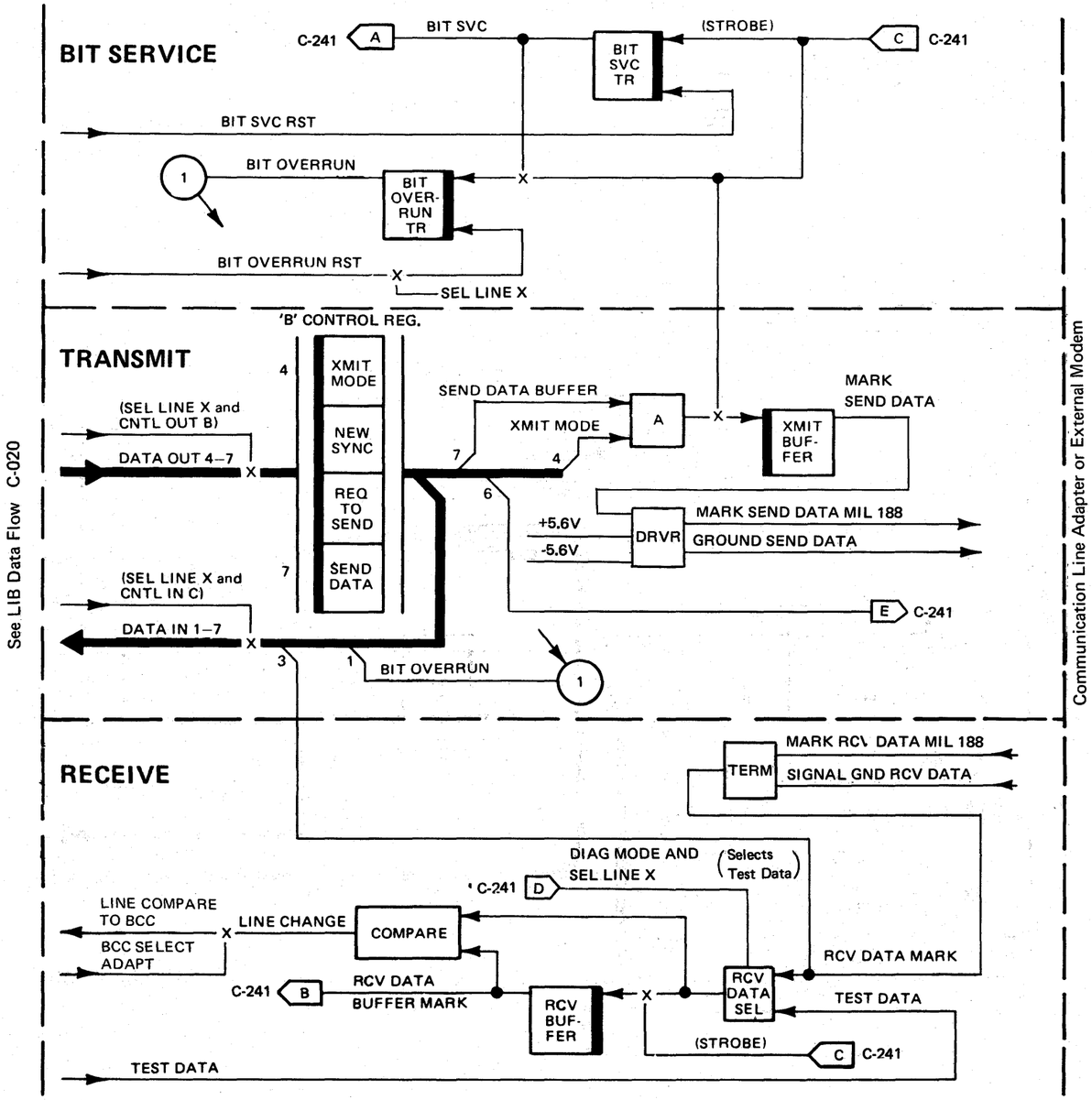
RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit. The MIL 188 *differential* voltage levels referenced to signal gound for RCV DATA, RCV CLOCK, and XMIT CLOCK should be within this range.





Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 1K, 1S, 1U

LINE SET 1U (High Speed Duplex CCITT V.35 Interface)

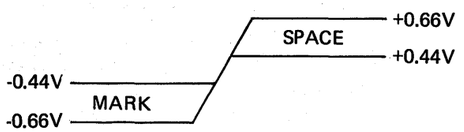
Line set 1U consists of two 1K/1S line sets cabled to a single external modem. Each line interface requires a single partition. Partitions must have adjacent addresses. (0 and 2, 4 and 6, 8 and A, C and E). The transmit address must be the low order address (0, 4, 8, or C) and the receive address must be the high order address (2, 6, A or E).

The hardware for transmit and hardware for receive are identical and for this illustration they are shown combined, but actually they are independent of each other, both in hardware and operation. Hardware used for transmit operations is marked with **T**, and hardware used for receive operations is marked with **R**. See VA014 for how the modem signal lines are connected to the line-interfaces.

STROBE

1. If the receive clock shift is not received from the modem when in receive mode, the backup 'strobe' pulses are obtained from the 'BCC strobe' pulses (see C-060).
2. During receive mode, when Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the modem clock (external clocking).

The modem clock pulses (Xmt clock and RCV clock) are received at the CCITT V35 levels. The range of levels is as follows:

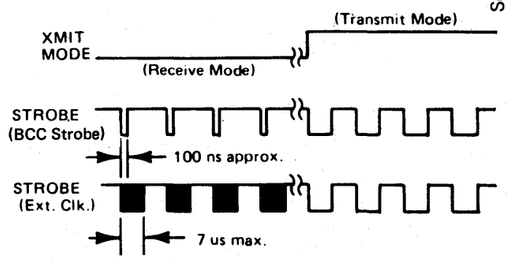


These levels *are differential* voltage levels measured between each side of the balanced line.

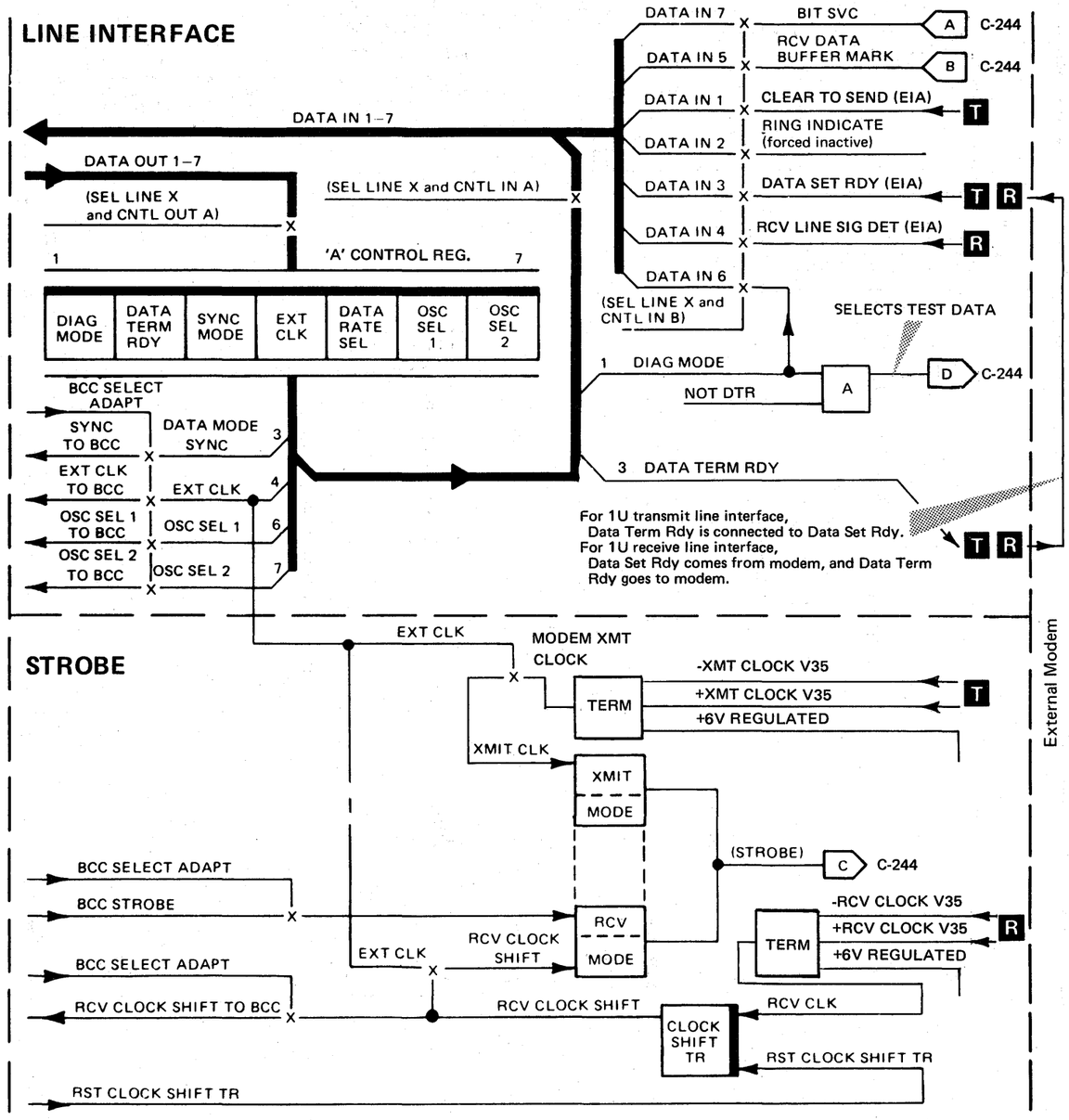
LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the modem.

1. The modem status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL in B.
2. The scanner transfers status information to the line interface during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and transmits a data bit to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C. (The type 2 and 3 scanner ignores 'bit overrun' and holds 'bit overrun reset' on solid.)



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 1K, 1S, 1U (PART 2)

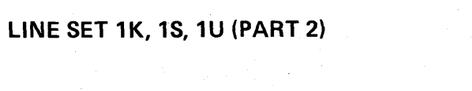
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

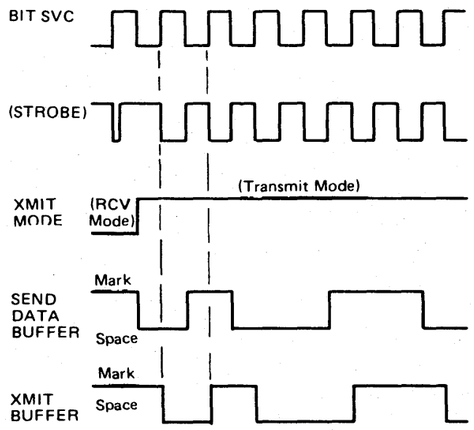
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE)
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the CCITT V.35 level of the communication line. The range of levels is as follows:



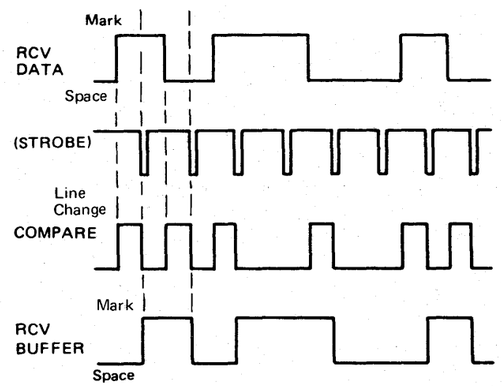
These levels are *differential* voltage levels measured between each side of the balanced time.

RECEIVE

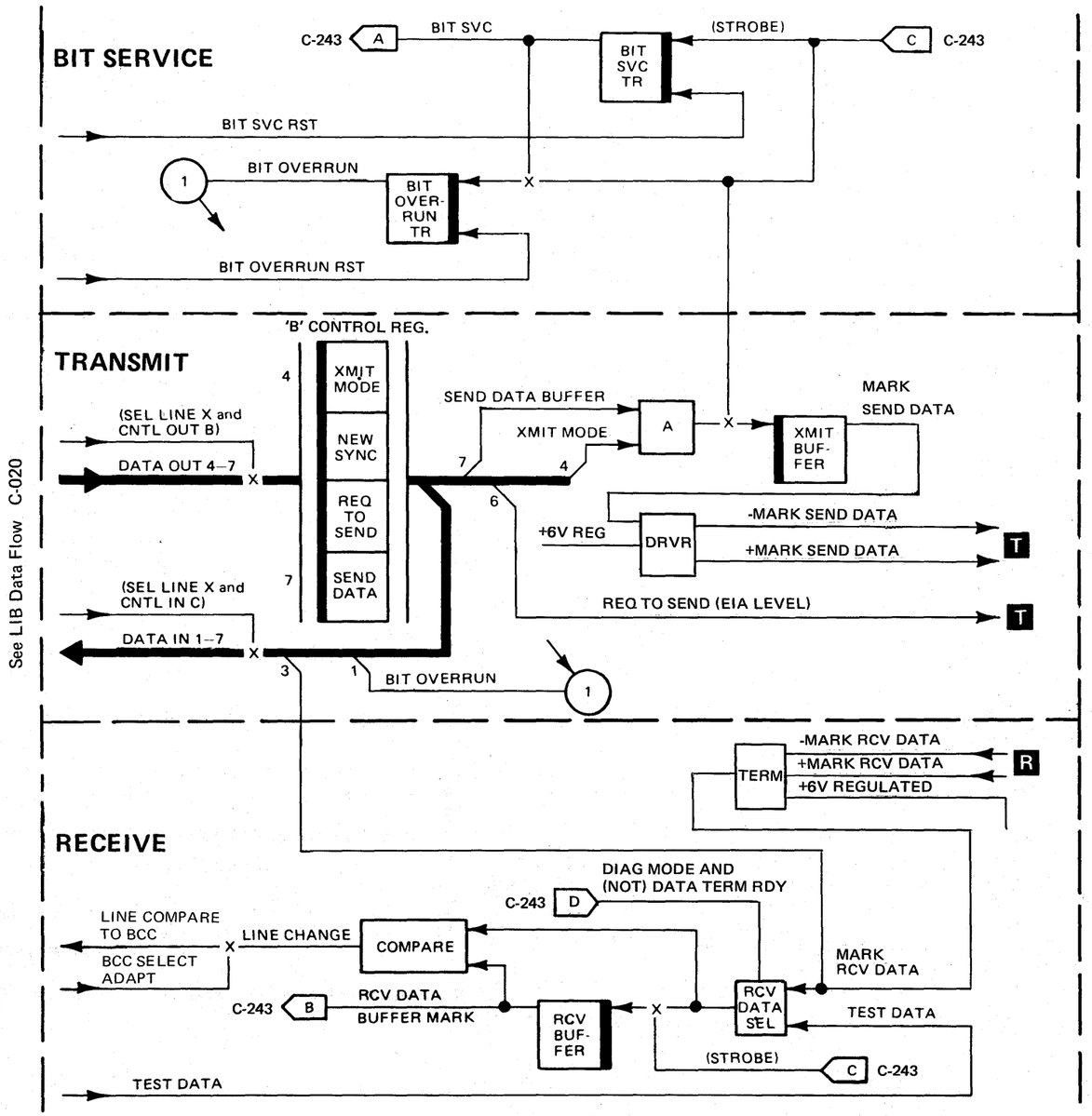
1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit. The received data is at the CCITT V.35 levels as described above.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 1N (CCITT X.21 Interface - Duplex or Half - Duplex Nonswitched)

LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the communication adapter (data circuit-terminating equipment-DCE).

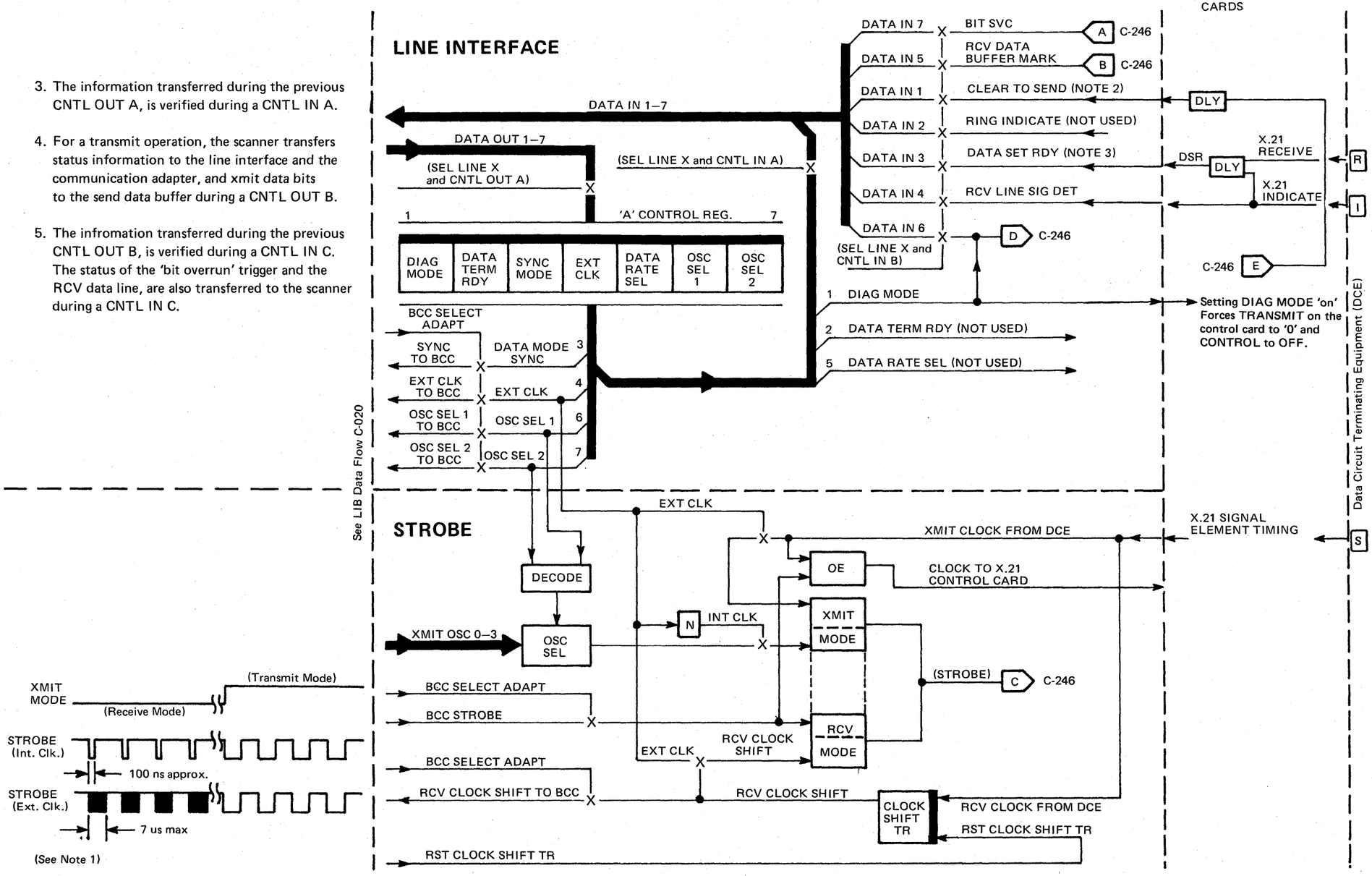
1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter, during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A, is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication adapter, and xmit data bits to the send data buffer during a CNTL OUT B.
5. The infromation transferred during the previous CNTL OUT B, is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line, are also transferred to the scanner during a CNTL IN C.

STROBE

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the DCE clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the DCE clock (external clocking).

Notes:

1. These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.
2. Approximately 26 bit times after it is activated, CLEAR TO SEND becomes effective.
3. Approximately 17 bit times after RECEIVE drops to '0' and INDICATE turns OFF, DATA SET READY becomes inactive.



LINE SET 1N (PART 2)
(CCITT X.21 Interface - Duplex or Half - Duplex Nonswitched)

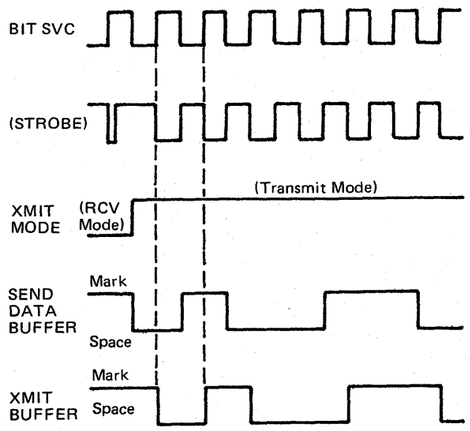
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

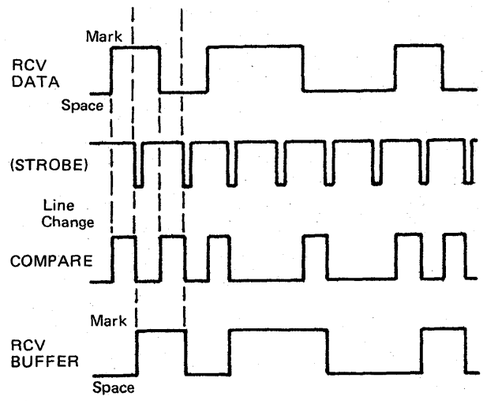
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the CCITT level of the communication line.



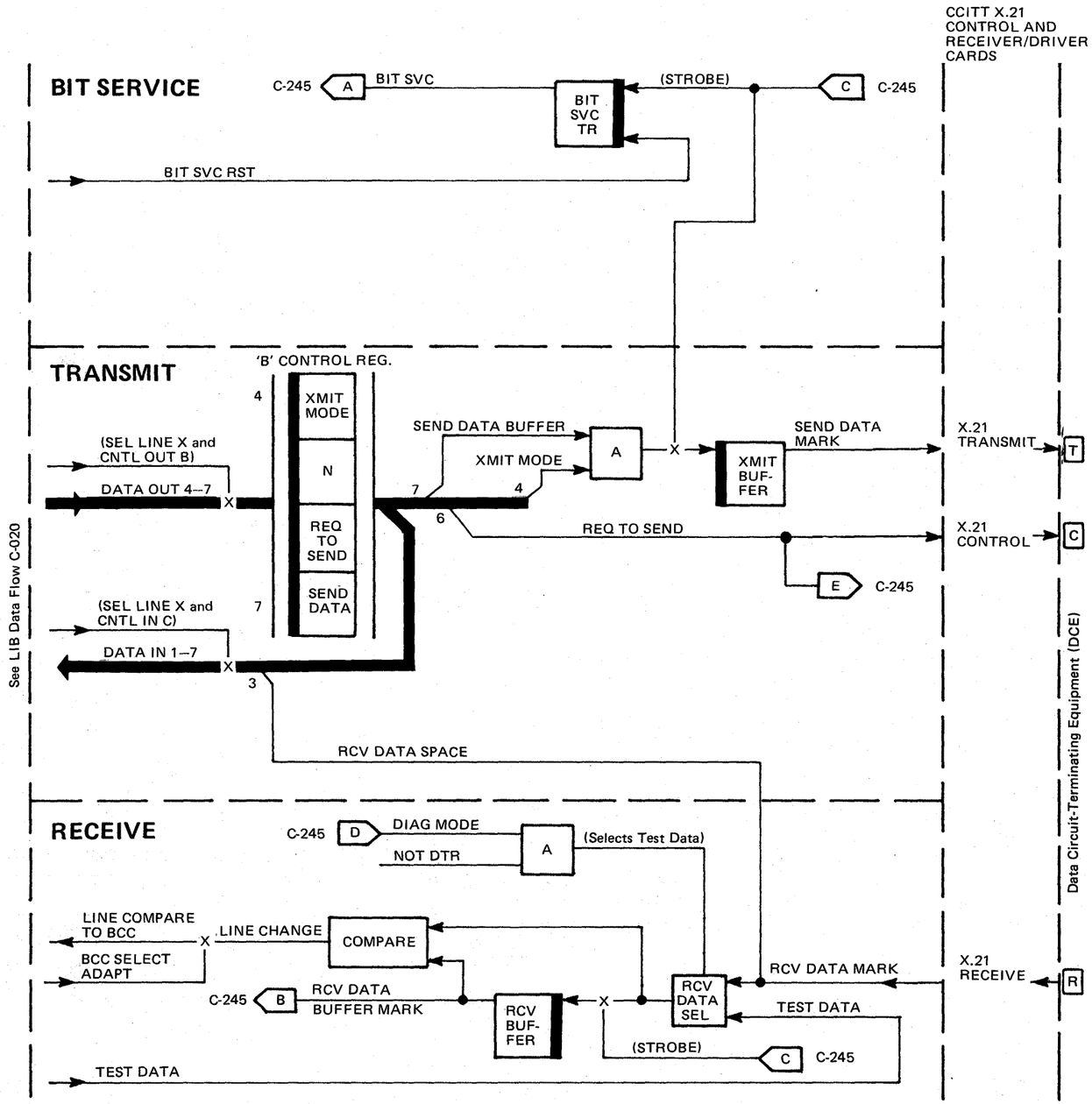
Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 1R (CCITT X.21 Interface - Duplex Switched)

LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the communication adapter (data circuit-terminating equipment-DCE).

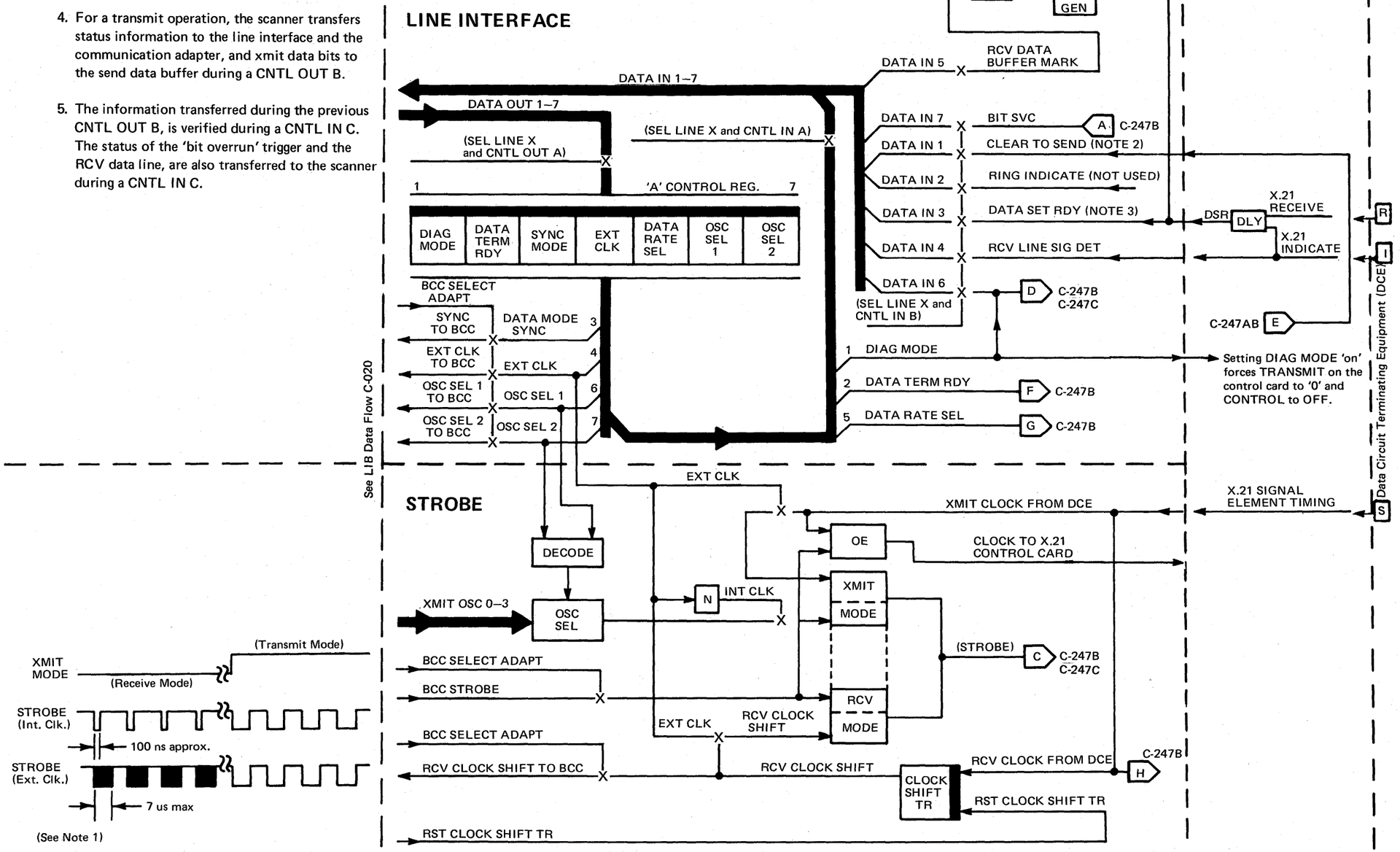
1. The communication line adapter status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the communication adapter, during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A, is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the communication adapter, and xmit data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B, is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line, are also transferred to the scanner during a CNTL IN C.

STROBE

1. When Xmit Mode and Ext Clk are not set, receive mode and internal clock are assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Ext Clk is set, 'strobe' pulses are obtained from the DCE clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking) or from the DCE clock (external clocking).

Notes:

1. These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.
2. With this line set, the NCP and basic machine timing use an internal clock (operating at 1/24 or less of the data rate) to delay a change in state of the CLEAR TO SEND line. The CLEAR TO SEND line changes state approximately 24 bit times after REQUEST TO SEND is activated.
3. Approximately 17 bit times after RECEIVE drops to '0' and INDICATE turns OFF, DATA SET READY becomes inactive.



LINE SET 1R (PART 2)
(CCITT X.21 Interface - Duplex Switched)

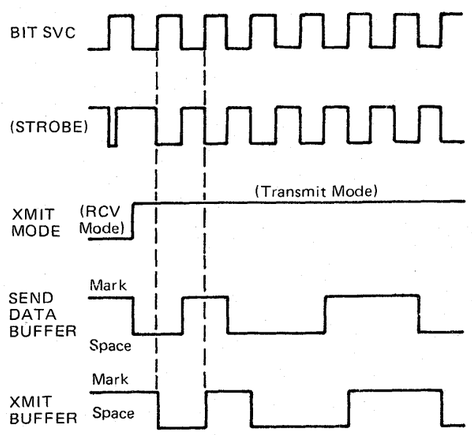
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

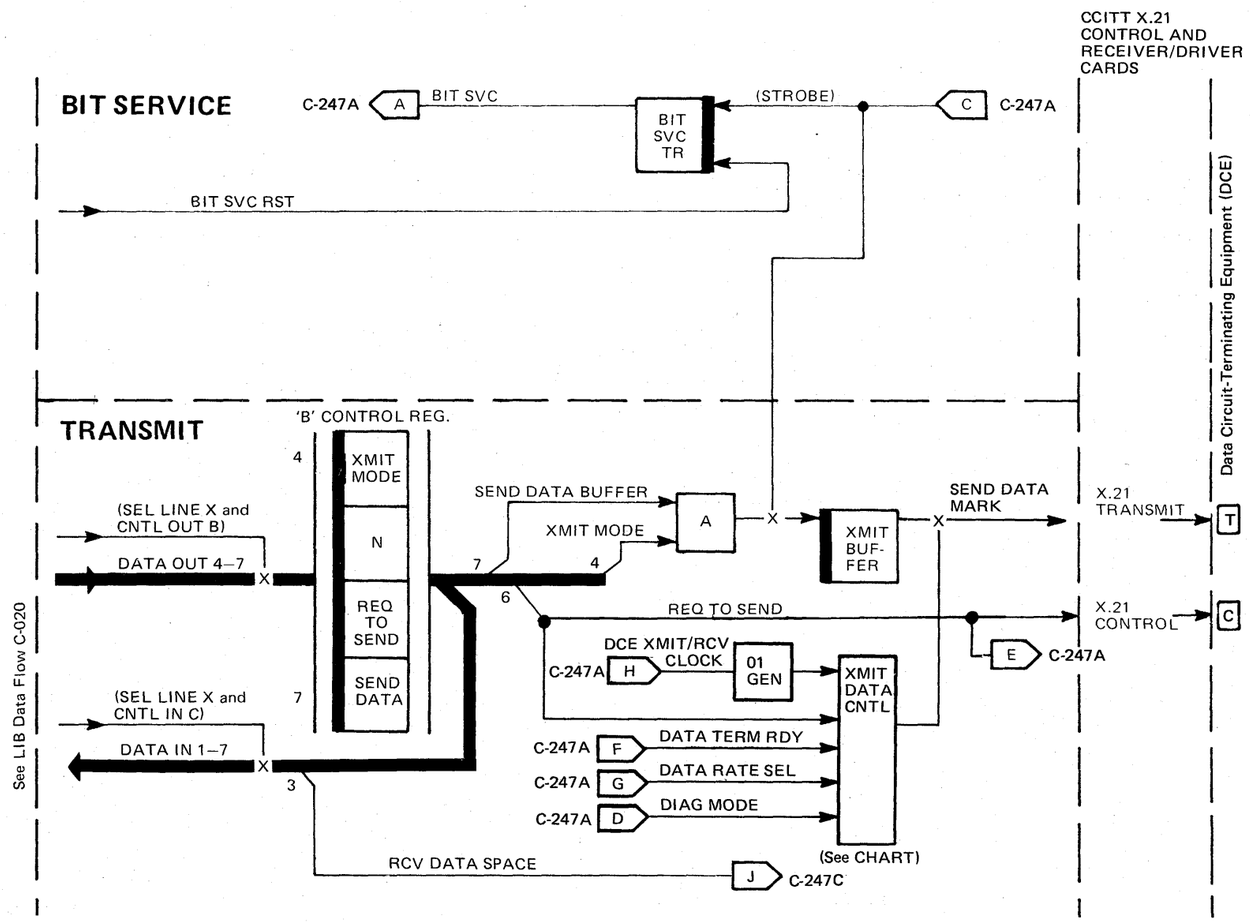
1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the CCITT level of the communication line.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



With a 1R line set, the *on* or *off* state of several latches determines the status of the CCITT X.21 interface and the condition of the transmit and control signal lines. The following chart shows how to use the latch conditions to determine the status of the interface.

Latch Conditions				Interface Signals		
Diag Mode	Data Term Rdy	Data Rate Sel	Req To Send	Control (C)	Transmit (T)	CCITT X.21 Status
Off	Off	**	Off	Off	0101...	DTE Controlled Not Ready
On	**	**	**	Off	0000...	DTE Uncontrolled Not Ready
Off	On	**	Off	Off	1111...	DTE Ready
Off	On	On	On	On	0000...	Call Request
Off	On	Off	On	On	*	Call Accepted or Data Transfer

* Data is transmitted from the Send Data Buffer.

** Of no concern

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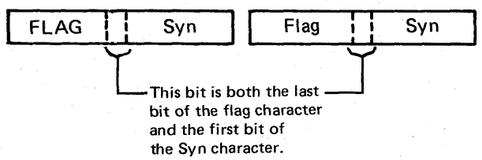
LINE SET 1R (PART 3)
(CCITT X.21 Interface - Duplex Switched)

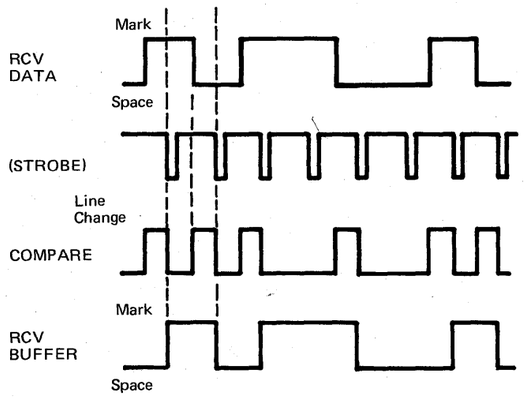
RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.

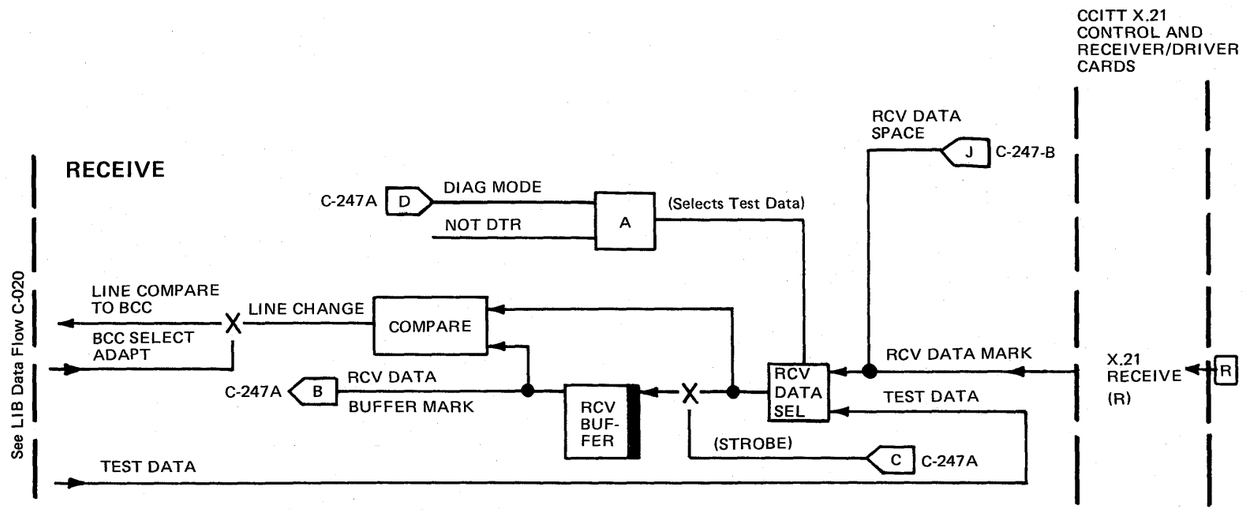
If a DCE not ready conditon occurs (data set ready becomes inactive), a continuous pattern of fixed data appears on the addressed receive data lead. This fixed data pattern consists of an SDLC flag character and a USASCII syn character. If the scanner associated with the CCITT X.21 interface is in a monitor flag or monitor phase state, the continuously generated data pattern produces a level 2 interrupt with a modem check indication. This level 2 interrupt indicates to the controller that a DCE not ready condition exists. The data pattern that appears on the receive data lead is shown below.

X011111101101000X011111101101000 . . . . . .





Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 1W, 1Z

LINE SET 1Z (High Speed Duplex CCITT V.35 Interface)

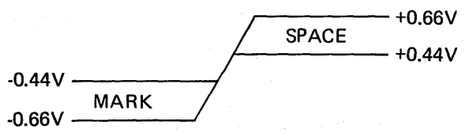
Line set 1Z consists of two 1W line sets cabled in a local attachment configuration. Each of the two 1 line interfaces require a single partition. Partitions must have adjacent addresses (0 and 2, 4 and 6, 8 and A, C and E). The transmit address must be the low order address (0, 4, 8, or C) and the receive address must be the high order address (2, 6, A or E).

The hardware for transmit and hardware for receive are identical and for this illustration they are shown combined, but actually they are independent of each other, both in hardware and operation. Hardware used for transmit operations is marked with T, and hardware used for receive operations is marked with R. See VA016 for how the local attachment signal lines are connected to the line-interfaces.

STROBE

1. If the receive clock shift is not received from the V.35 local oscillator, when in receive mode, the backup 'strobe' pulses are obtained from the 'BCC strobe' pulses (see C-060).
2. During receive mode, when Ext Clk is set, 'strobe' pulses are obtained from the V.35 local oscillator, (through the 'clock shift' trigger).
3. When XMIT Mode is set, 'strobe' pulses are obtained from the V.35 XMIT clock (external clocking).

The clock pulses for a distant terminal or 3705 are transmitted at CCITT V35 levels. The range of levels is as follows:

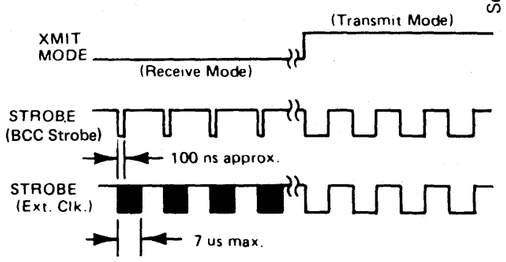


These levels *are differential* voltage levels measured between each side of the balanced line.

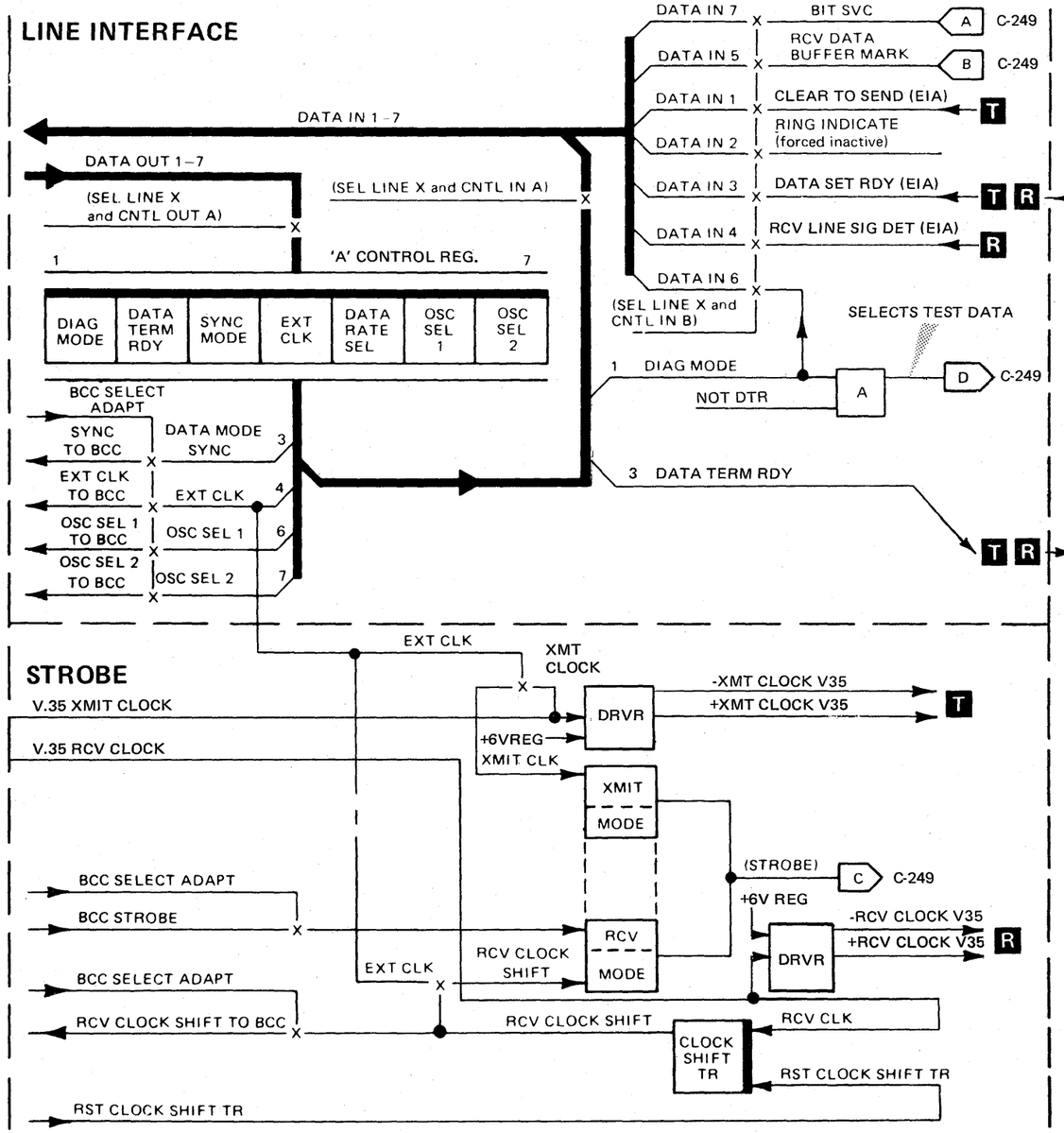
LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the modem.

1. The modem status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL in B.
2. The scanner transfers status information to the line interface during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and transmits a data bit to the 'send data buffer' during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C. (The type 2 and 3 scanner ignores 'bit overrun' and holds 'bit overrun reset' on solid.)



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



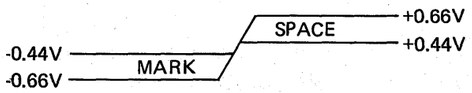
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

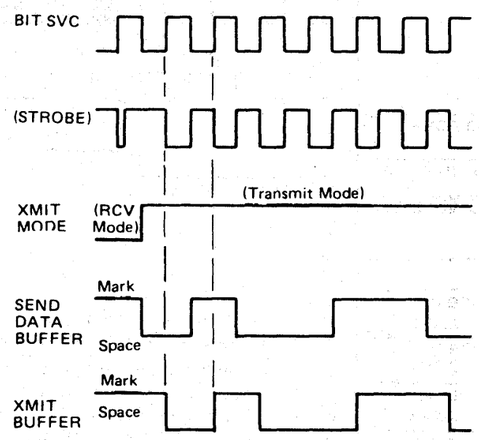
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE)
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the CCITT V.35 level of the communication line. The range of levels is as follows:



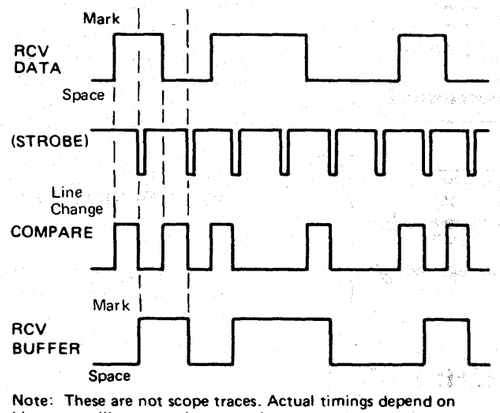
These levels are *differential* voltage levels measured between each side of the balanced time.

RECEIVE

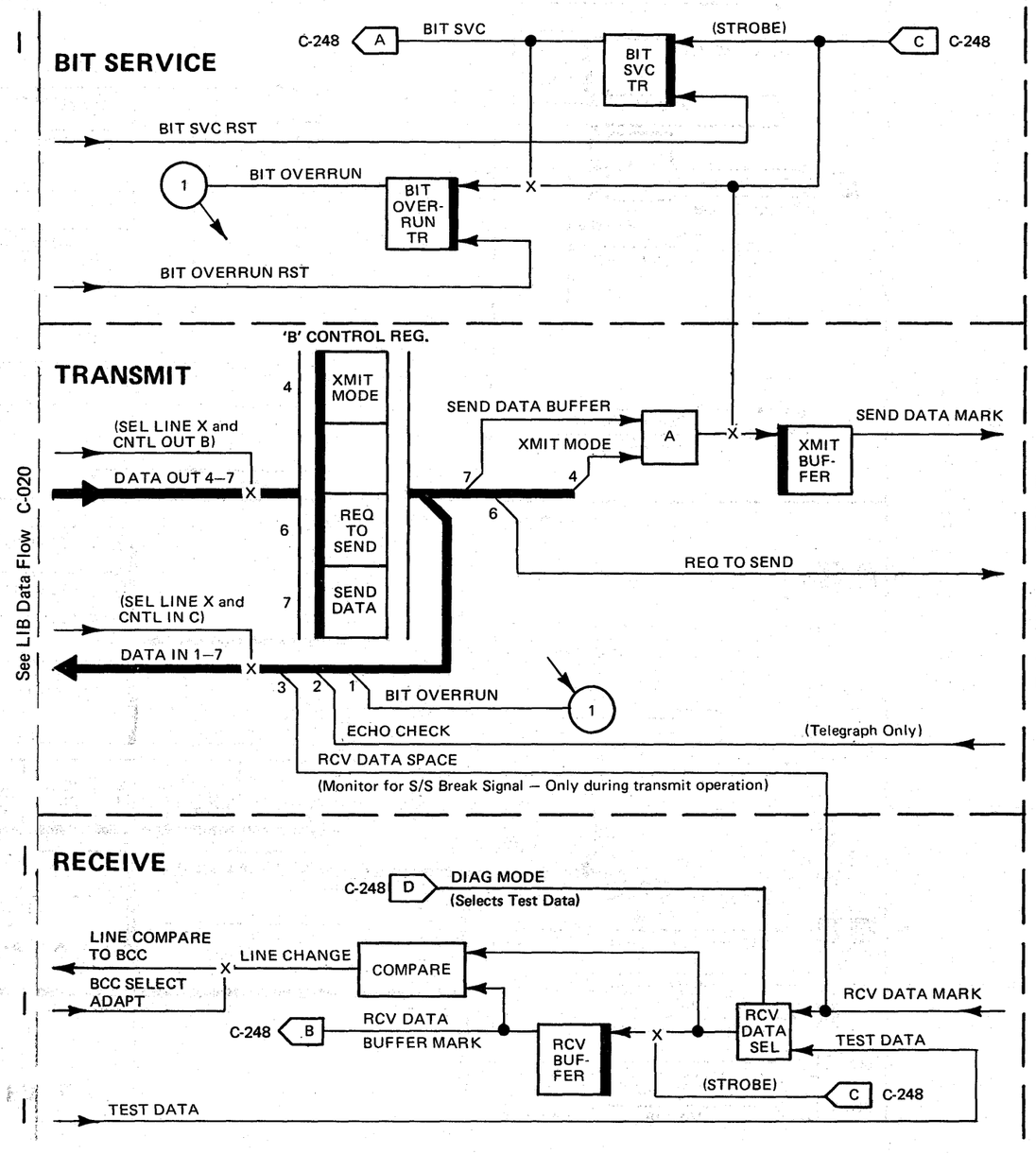
1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit. The received data is at the CCITT V.35 levels as described above.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 2A, 3A, 3B, 4A, 4B, 4C

LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the communication line adapter (modem, IBM Line Adapter, telegraph adapter).

1. The communication line adapter status, RCV buffer status, and 'bit service trigger' status are transferred to the scanner during a CNTL IN B.

2. The scanner transfers status information to the line interface and the communication adapter during a CNTL OUT A.

3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.

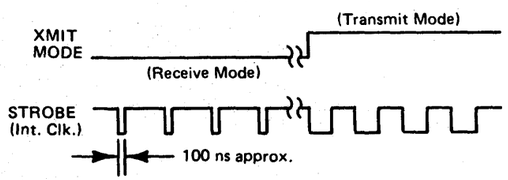
4. For a transmit operation, the scanner transfers status information to the line interface and the communication line adapter, and xmit data bits to the send data buffer during a CNTL OUT B.

5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C.

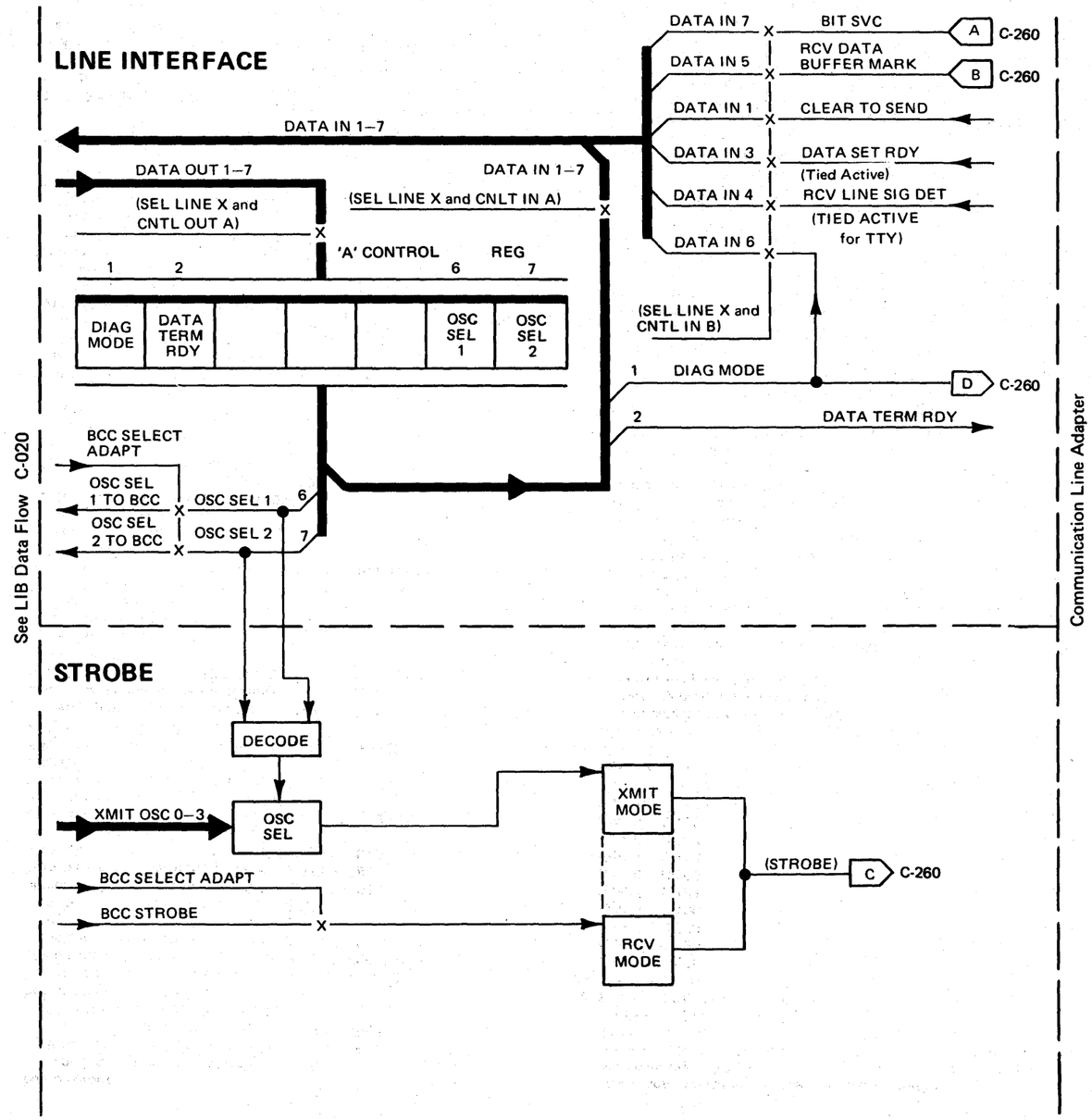
STROBE

1. When Xmit Mode is not set, receive mode is assumed; and the 'strobe' pulses are obtained from the 'BCC strobe' pulses.

2. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 2A, 3A, 3B, 4A, 4B, 4C (PART 2)

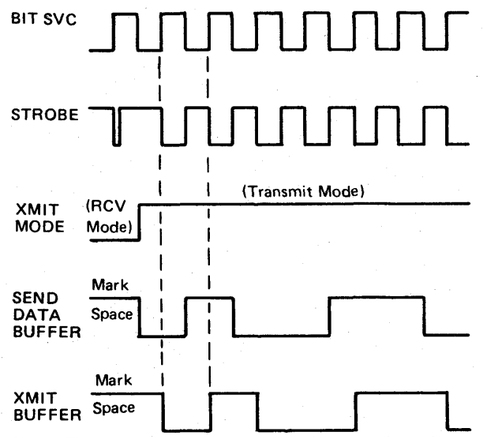
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

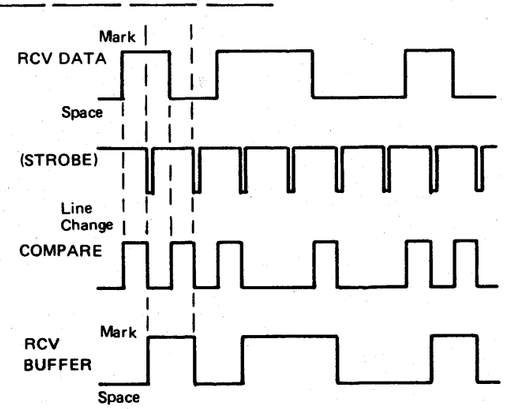
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the EIA level of the communication line.



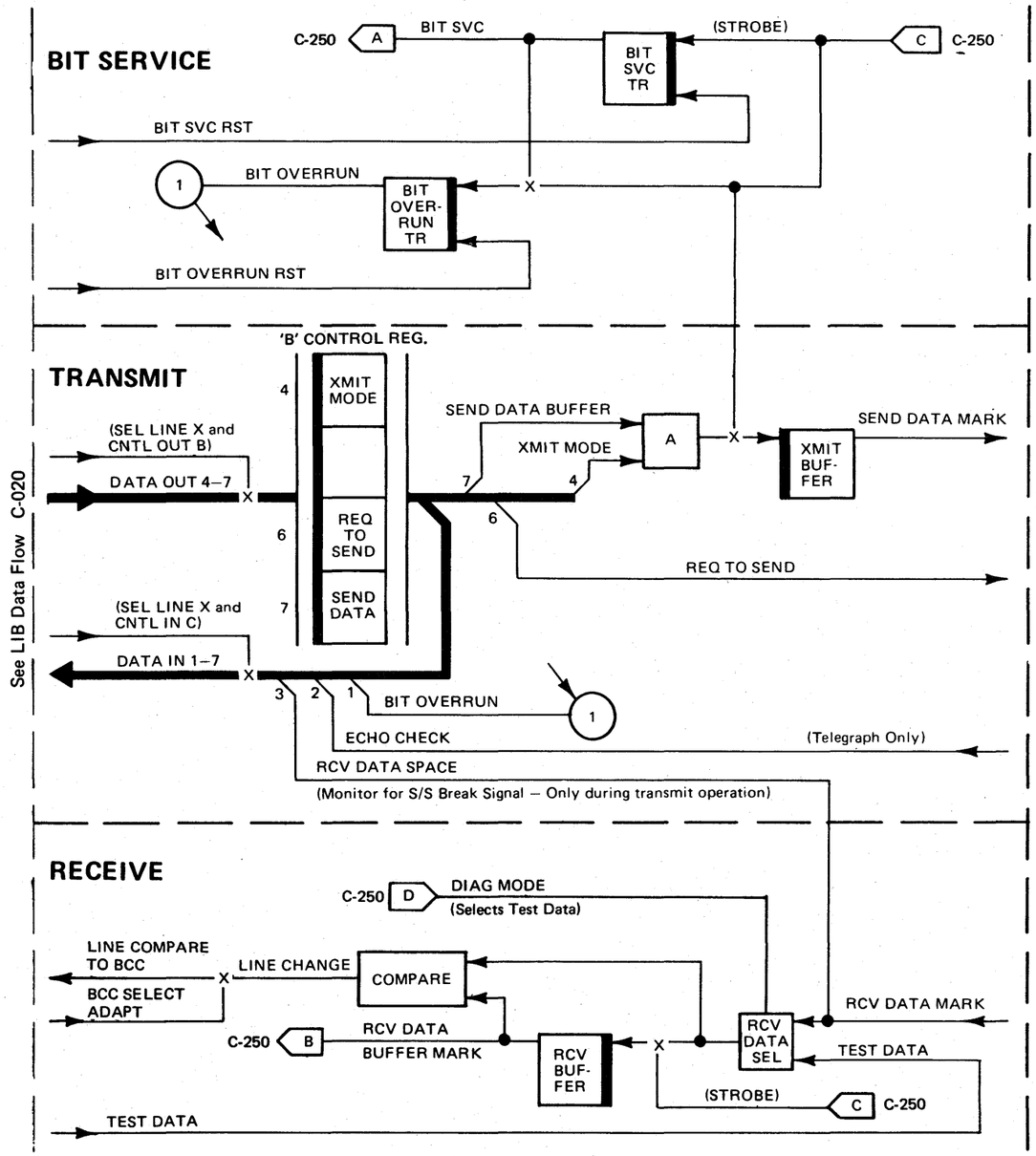
Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



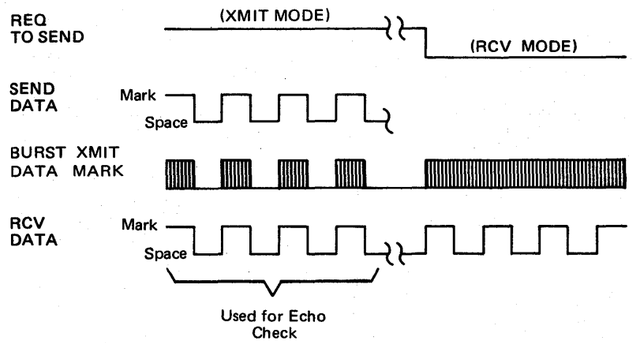
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

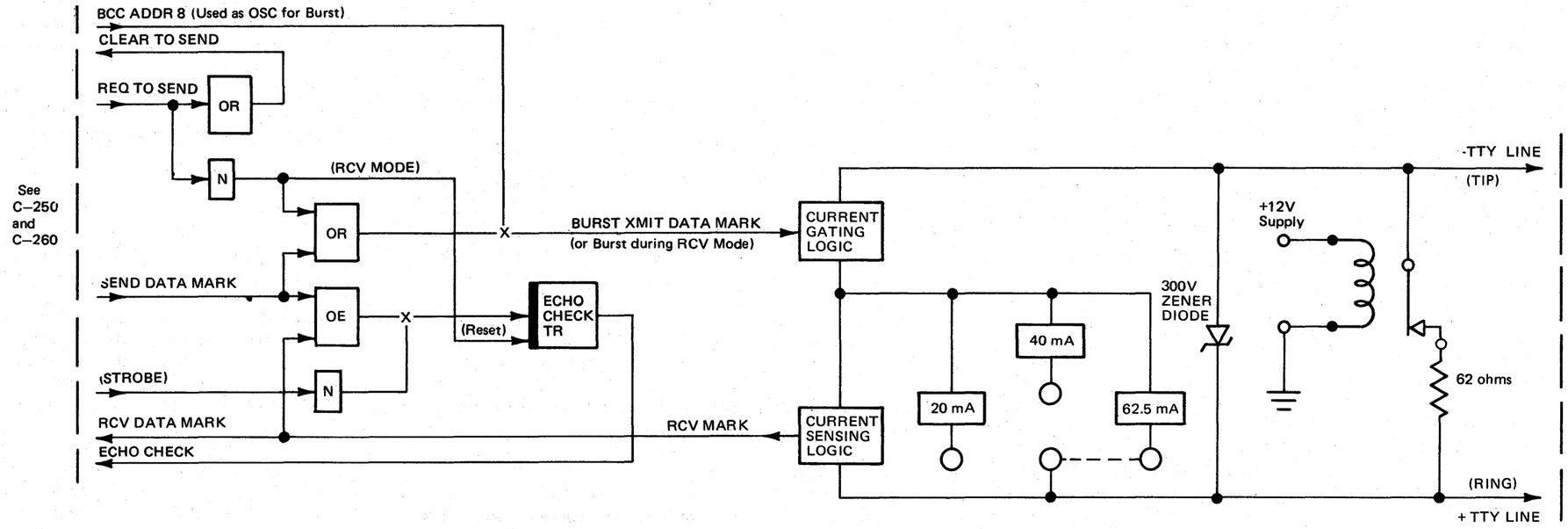
TELEGRAPH ADAPTER (SINGLE CURRENT)

The telegraph adapter transmits data and receives data on the telegraph line. Current in the loop indicates a 'mark'. No current indicates a 'space'.

During a transmit operation, the telegraph adapter controls the current in the loop. Each 'mark' bit gates a burst of oscillator pulses that allows current in the loop.

During a receive operation, the remote terminal controls current in the loop. The telegraph adapter uses oscillator pulses to allow current in the loop under the control of the remote terminal. The current sensing logic detects 'marks' and 'spaces'.





LINE SET 5A, 5B, 6A, AND LIB7

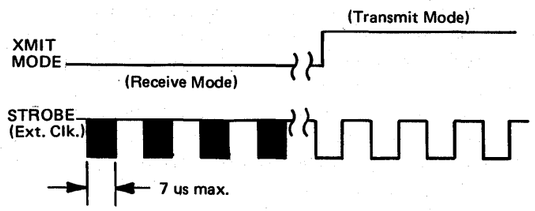
LINE INTERFACE

The line interface is a buffer for status and data transferred between the scanner and the integrated modem.

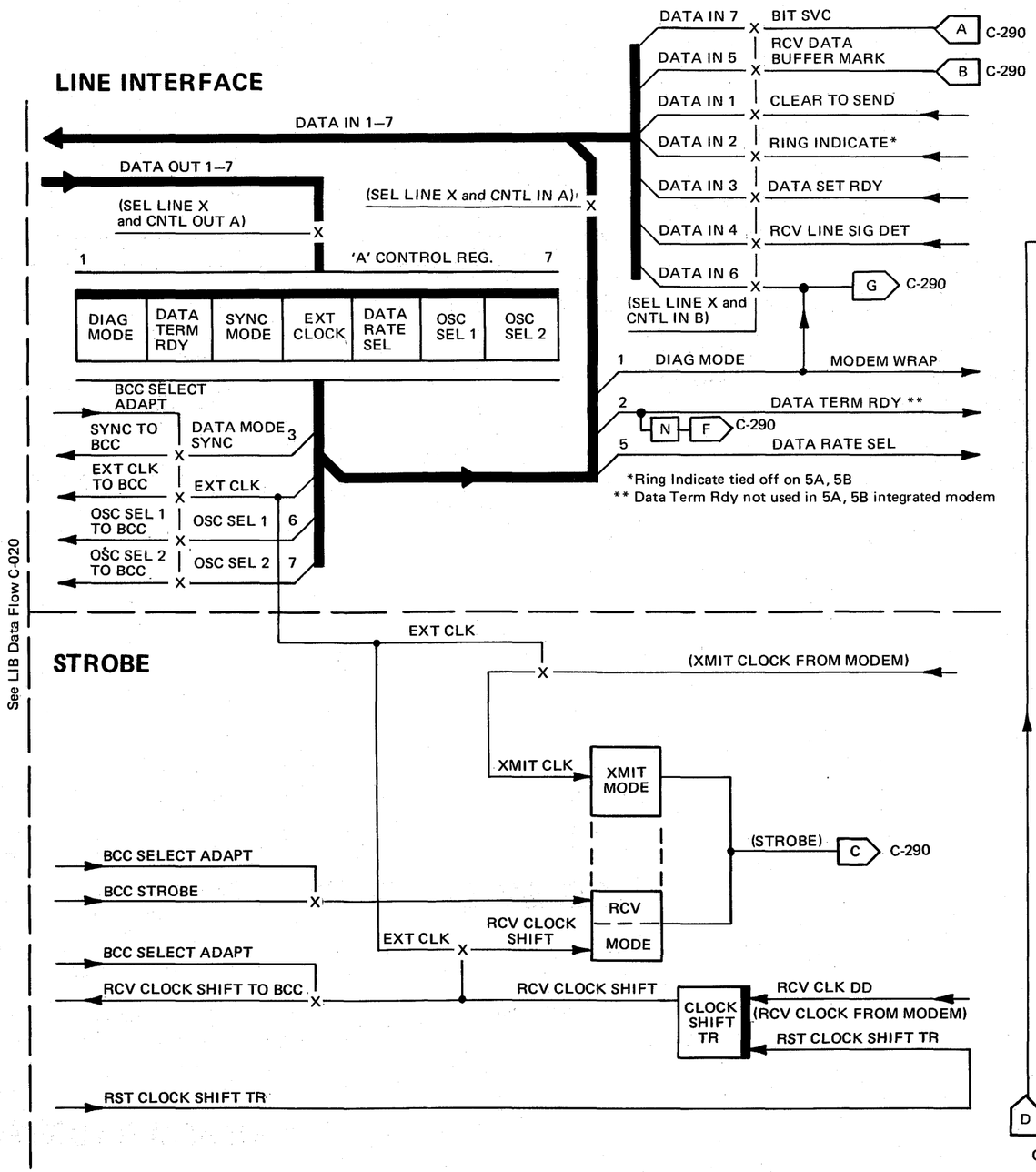
1. The integrated modem status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the integrated modem during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the integrated modem, and transmits data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner.

STROBE

1. If the receive clock shift is not received from the integrated modem, when in receive mode, the backup 'strobe' pulses are obtained from the 'BCC strobe' pulses (see C-060).
2. During receive mode when Ext Clk is set, 'strobe' pulses are obtained from the modem clock (through the 'clock shift' trigger).
3. When Xmit Mode is set, 'strobe' pulses are obtained from the integrated modem clock (external clocking).



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 5A, 5B, 6A AND LIB7 (PART 2)

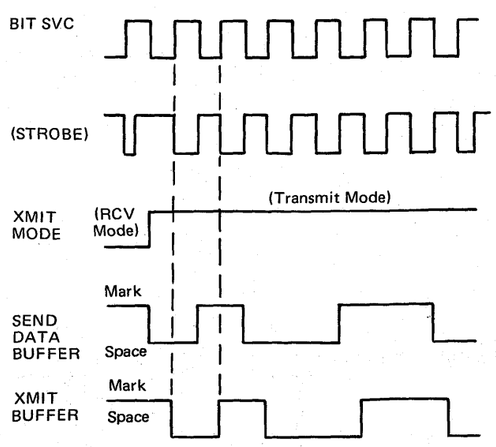
BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

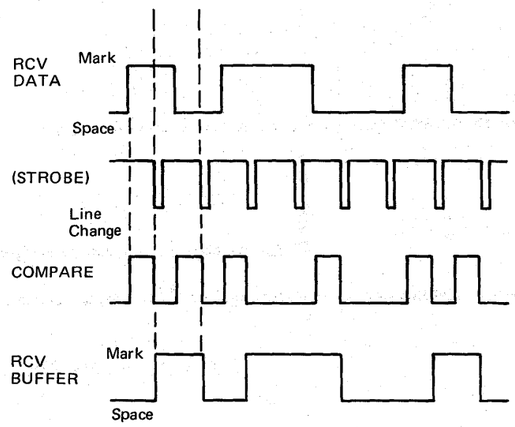
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, New Sync, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. The output of the transmit buffer is converted to the EIA level.



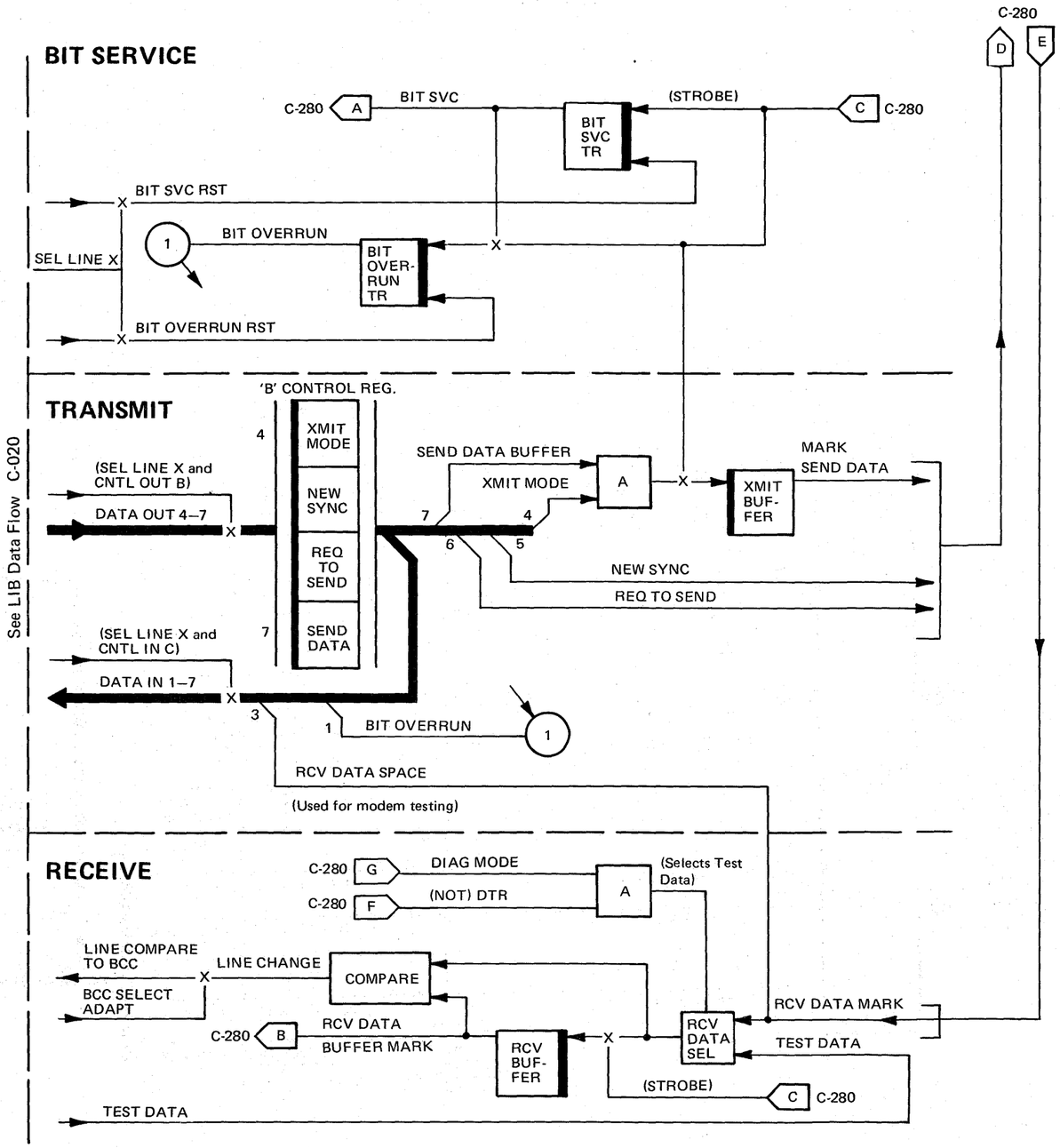
Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 8A, 8B, 9A, 12A, 12B

LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the integrated modem.

1. The modem status, RCV buffer status, and 'bit service' trigger status are transferred to the scanner during a CNTL IN B.
2. The scanner transfers status information to the line interface and the integrated modem during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For a transmit operation, the scanner transfers status information to the line interface and the integrated modem, and transmits data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger and the RCV data line are also transferred to the scanner during a CNTL IN C.

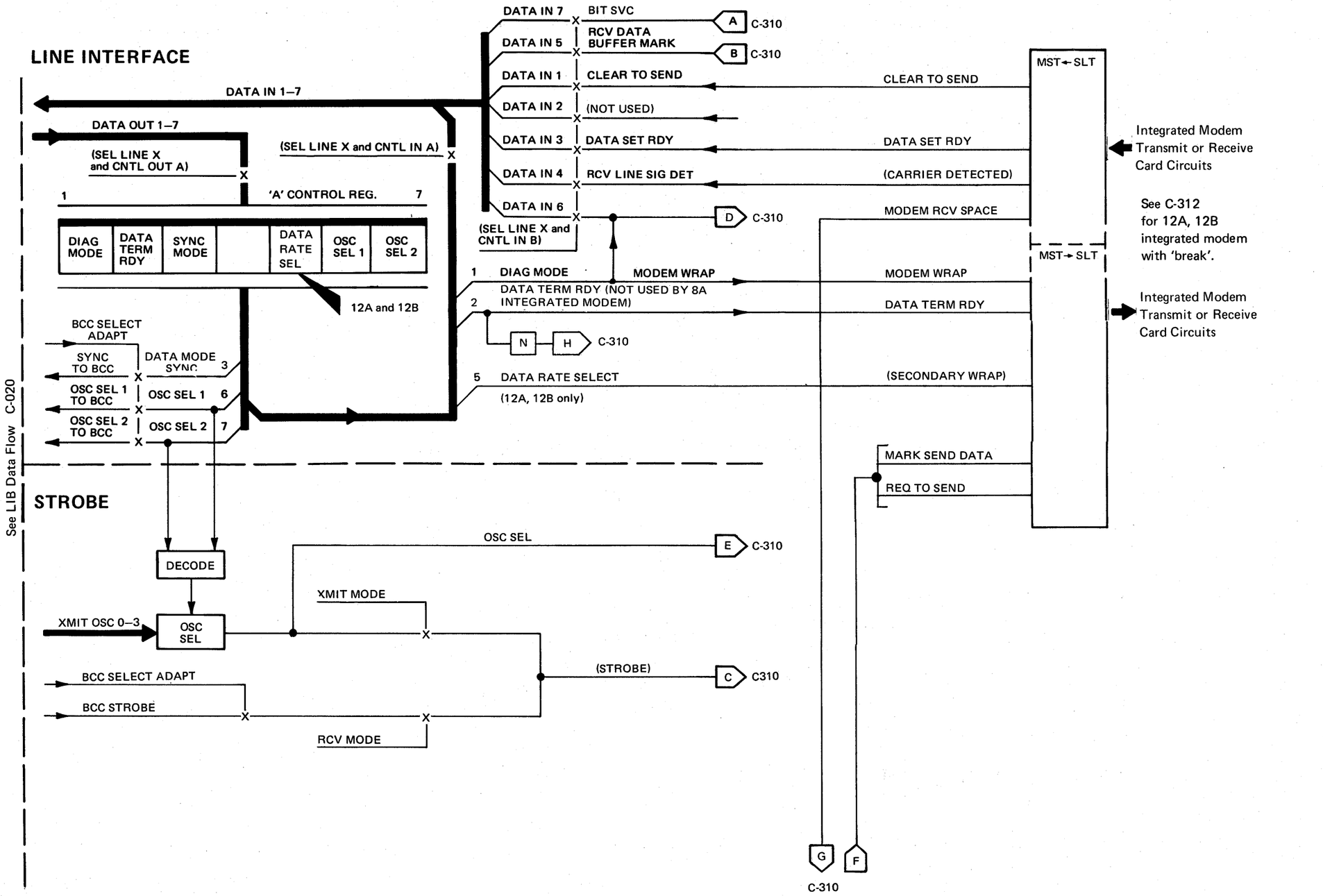
STROBE

1. When Receive Mode is set, the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. When Xmit Mode is set, 'strobe' pulses are obtained from the selected oscillator (internal clocking).

BREAK (12A, 12B)

When line set 12A or 12B is transmitting, the 3767 operator can interrupt the transmission by pressing the ATTENTION key causing the IBM 3767 to send a 450 Hz break signal for six character times. The 12A or 12B line set break card detects this 450 Hz and holds the 'received data' to a SPACE level. The 3705 control program detects the multiple 'stop bit errors' and stops transmitting. Line set 12A or 12B stops IBM 3767 transmission by a similar operation in the opposite direction but only sends the 450 Hz break signal for three character times.

Switched facilities must have their echo suppressors disabled for the break to operate properly. The 12B line set sends a 390 Hz tone to disable the echo suppressors while in receive mode whenever the break is 'enabled'. The 3767 never sends 390 Hz. Leased 2-wire facilities must not have echo suppressors therefore the 390 Hz tone is not used.



LINE SET 8A, 8B, 9A, 12A, 12B (PART 2)

BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

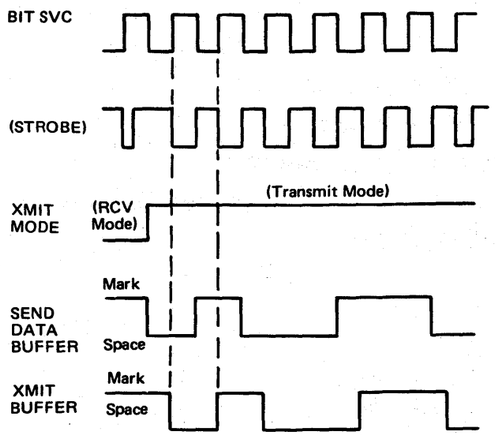
1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

TRANSMIT

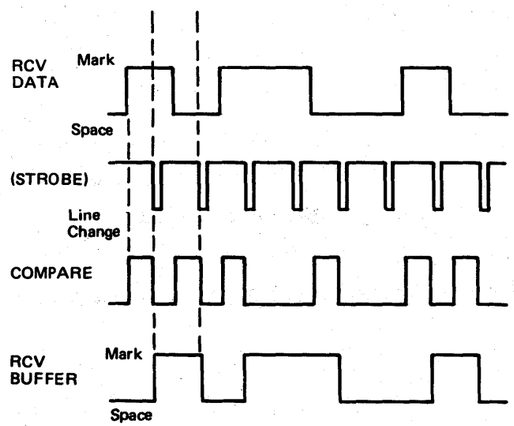
1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. During a modem wrap, another interface address sets the test data latch in the scanner (common to all attached lines). The transmit buffer sends the test data to the modem transmitter where it is wrapped to the receiver. The received data returns to the scanner through the receive buffer because DTR is on.

RECEIVE

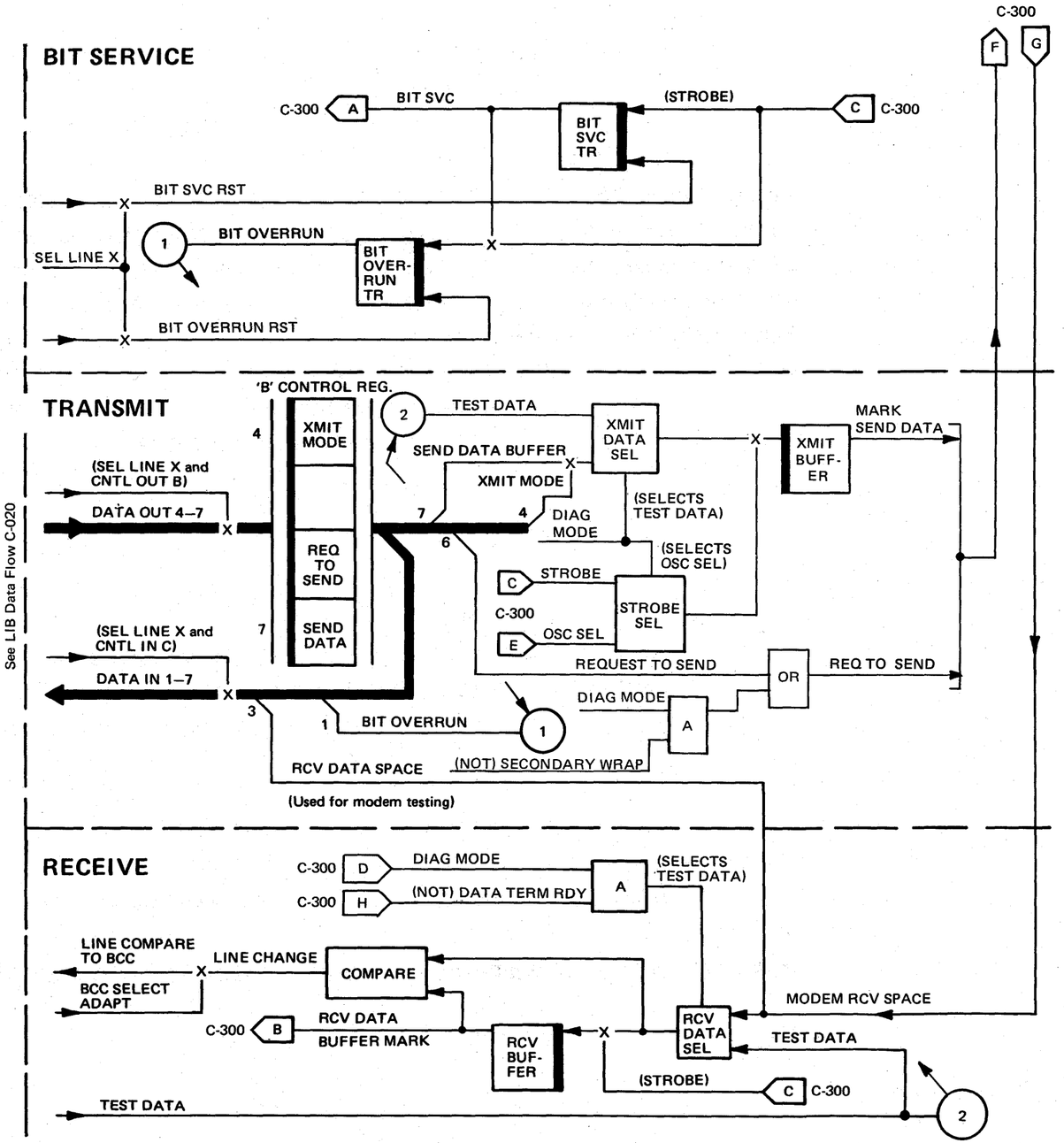
1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



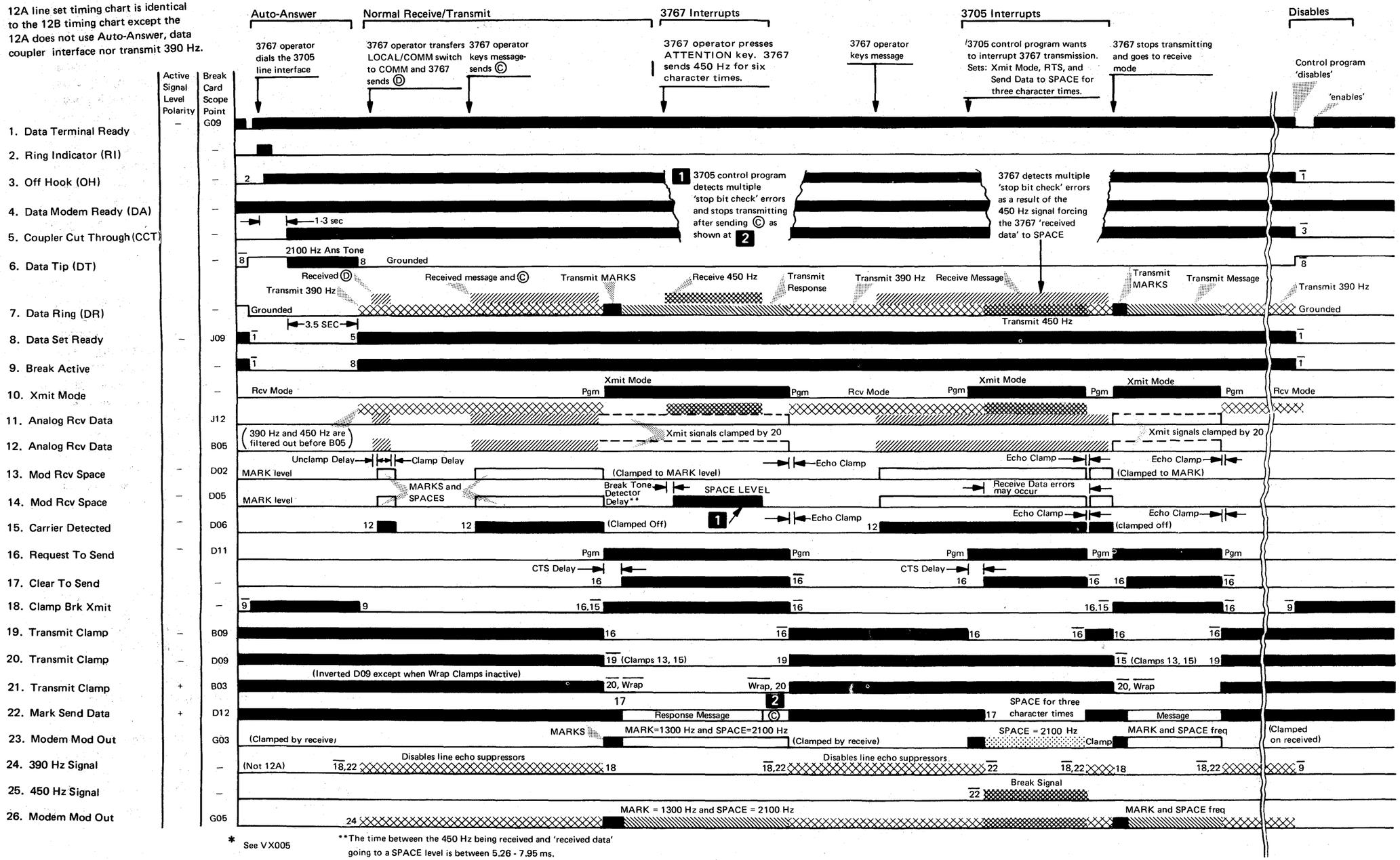
Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



12A, 12B BREAK TIMING CHART

The IBM 3767 Communication Terminal is used as the terminal in this example.

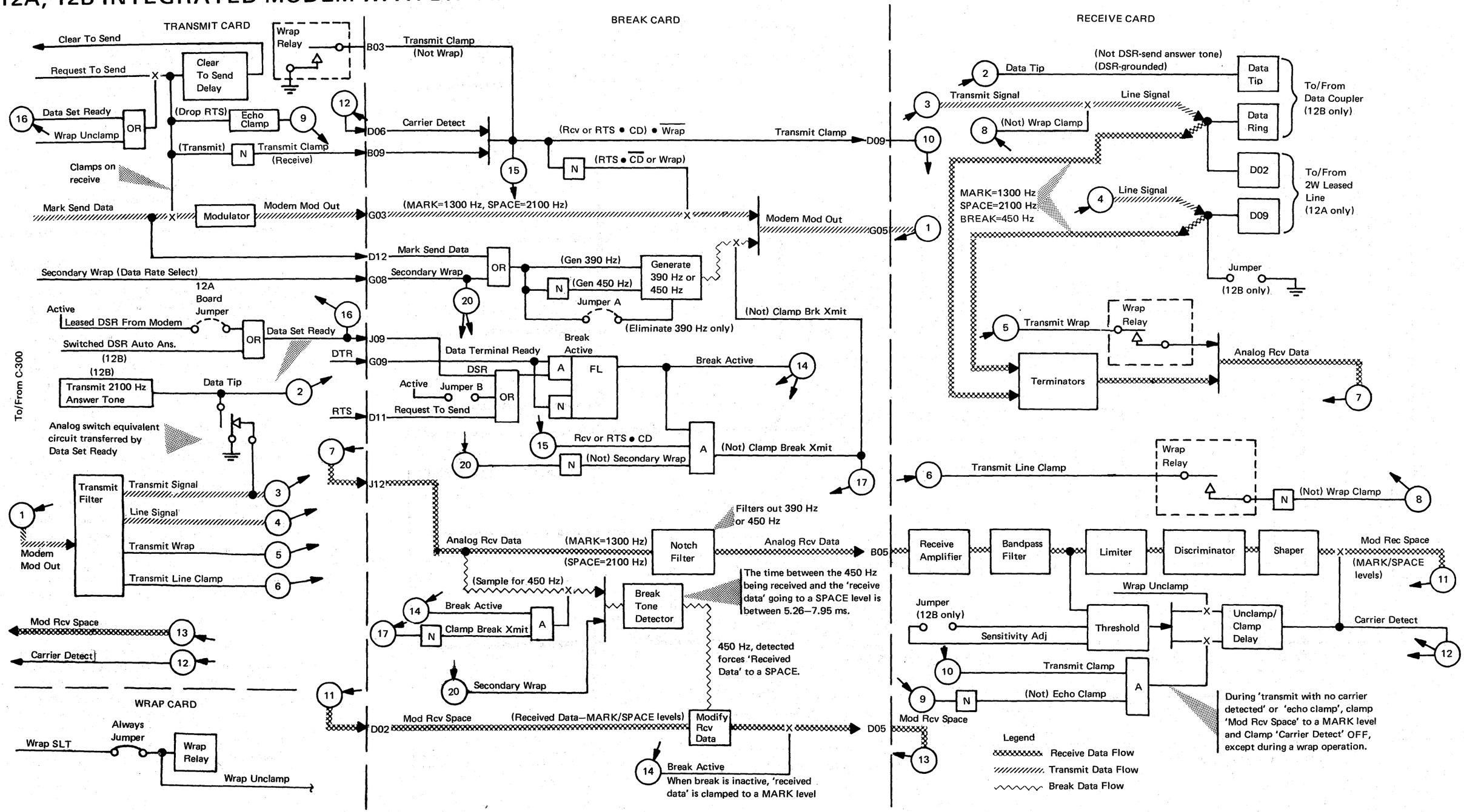
12A line set timing chart is identical to the 12B timing chart except the 12A does not use Auto-Answer, data coupler interface nor transmit 390 Hz.



* See VX005

**The time between the 450 Hz being received and 'received data' going to a SPACE level is between 5.26 - 7.95 ms.

12A, 12B INTEGRATED MODEM WITH BREAK



LINE SET 10A

Line set 10A is an IBM 1200 bps leased *duplex* data integrated modem. The modem transmitter is board wired to the low order address (X) while the modem receiver is board wired to the adjacent high order address (Y) of a modified 1D line set. The transmit address hardware is independent of the receive address hardware with each developing its own 'bit service' and 'strobe'; however, they share the same duplex integrated modem.

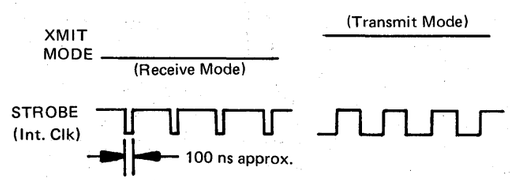
LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the integrated modem.

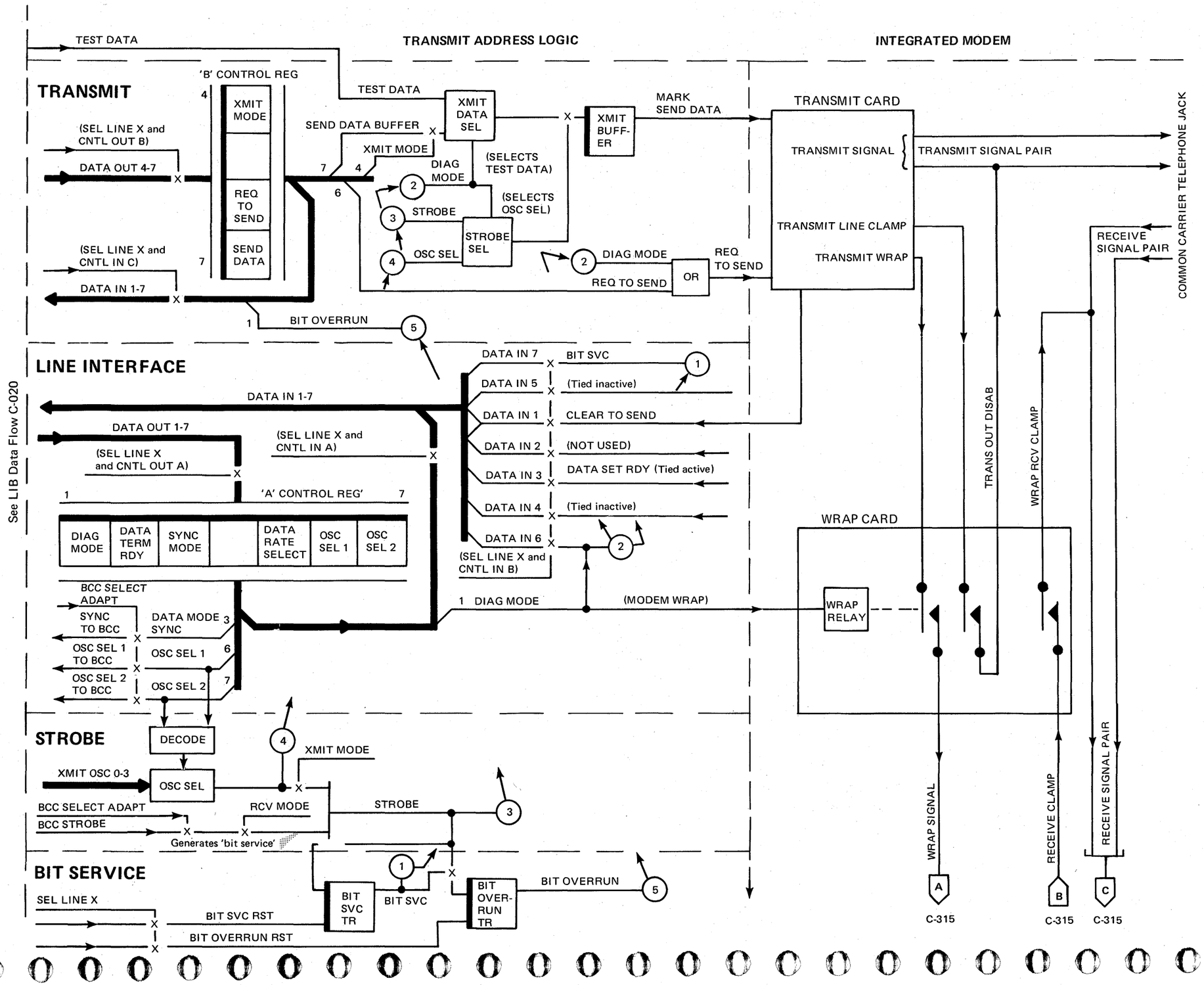
1. The modem status, receive buffer status, and 'bit service' trigger status are transferred to the scanner during their respective address CNTL IN B times.
2. The scanner transfers status information to the line interface and the integrated modem during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For the transmit address, the scanner transfers status information to the line interface and the integrated modem, and transmits data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger is also transferred to the scanner during a CNTL IN C.
6. For the receive address, the scanner resets the 'xmt mode' latch (to force RCV Mode) during its CNTL OUT B. The status of the 'bit overrun' trigger and the RCV data line is transferred to the scanner during CNTL IN C.

STROBE

1. Receive address — the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. Transmit address — the 'strobe' pulses are obtained from the selected oscillator (business machine clocking).



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 10A (PART 2)

BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

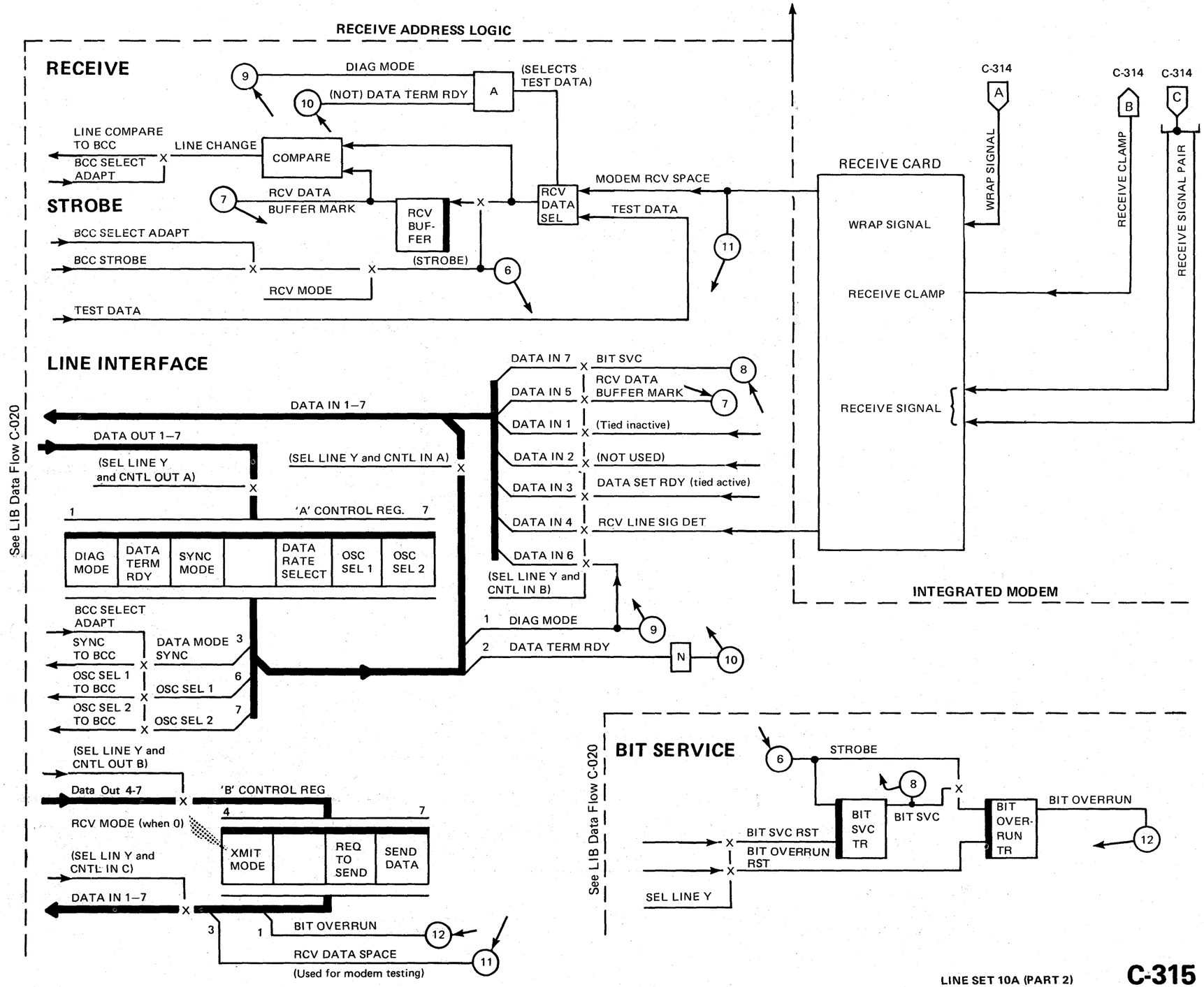
TRANSMIT

1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req to Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. During a modem wrap, another interface address sets the test data latch in the scanner (common to all attached lines). The transmit buffer sends the test data to the modem transmitter where it is wrapped to the receiver. The received data returns to the scanner through the receive buffer because DTR is on.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.

The timing charts on C-310 also apply to line set 10A.



LINE SET 11A, 11B

Line set 11A is a 2400 bps leased point-to-point duplex data integrated modem and line set 11B is a 2400 bps leased multipoint, control, duplex data integrated modem. The modem transmitter is board wired to the low order address (X) while the receiver is board wired to the adjacent high order address (Y) of a modified 1D line set. The transmit address hardware is independent of the receive address hardware with each developing its own 'bit service' and 'strobe'; however, they share the same duplex integrated modem.

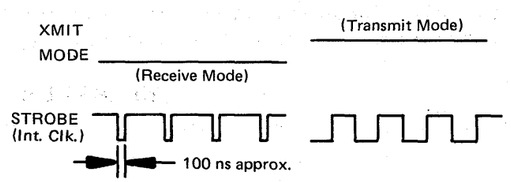
LINE INTERFACE

The line interface is a buffer for status and data, transferred between the scanner and the integrated modem.

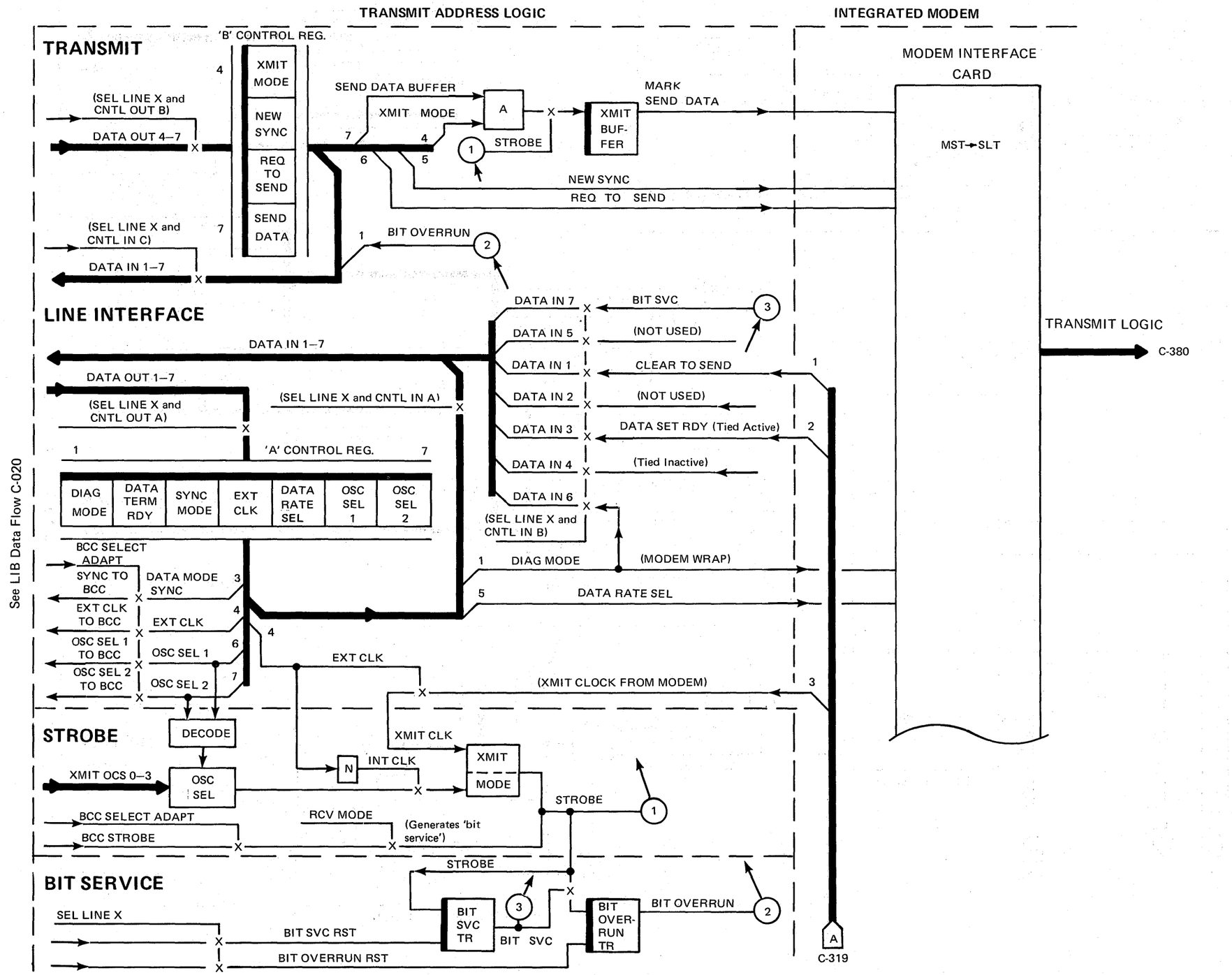
1. The modem status, receive buffer status, and 'bit service'. trigger status are transferred to the scanner during their respective address CNTL IN B times.
2. The scanner transfers status information to the line interface and the integrated modem during a CNTL OUT A.
3. The information transferred during the previous CNTL OUT A is verified during a CNTL IN A.
4. For the transmit address, the scanner transfers status information to the line interface and the integrated modem, and transmits data bits to the send data buffer during a CNTL OUT B.
5. The information transferred during the previous CNTL OUT B is verified during a CNTL IN C. The status of the 'bit overrun' trigger is also transferred to the scanner during a CNTL IN C.
6. For the receive address, the scanner resets the 'xmt mode' latch (to force RCV Mode) during its CNTL OUT B. The status of the 'bit overrun' trigger and the RCV data line are transferred to the scanner during CNTL IN C.

STROBE

1. Receive address – the 'strobe' pulses are obtained from the 'BCC strobe' pulses.
2. Transmit address – the 'strobe' pulses are obtained from the selected oscillator (business machine clocking).



Note: These are not scope traces. Actual timings depend on bit rate, oscillator speed, scan cycles, etc.



LINE SET 11A, 11B (PART 2)

BIT SERVICE

'Bit service' and 'bit service reset' are the interlock controls between the scanner and the line interface. 'Bit service' is the line interface's request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger.
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.

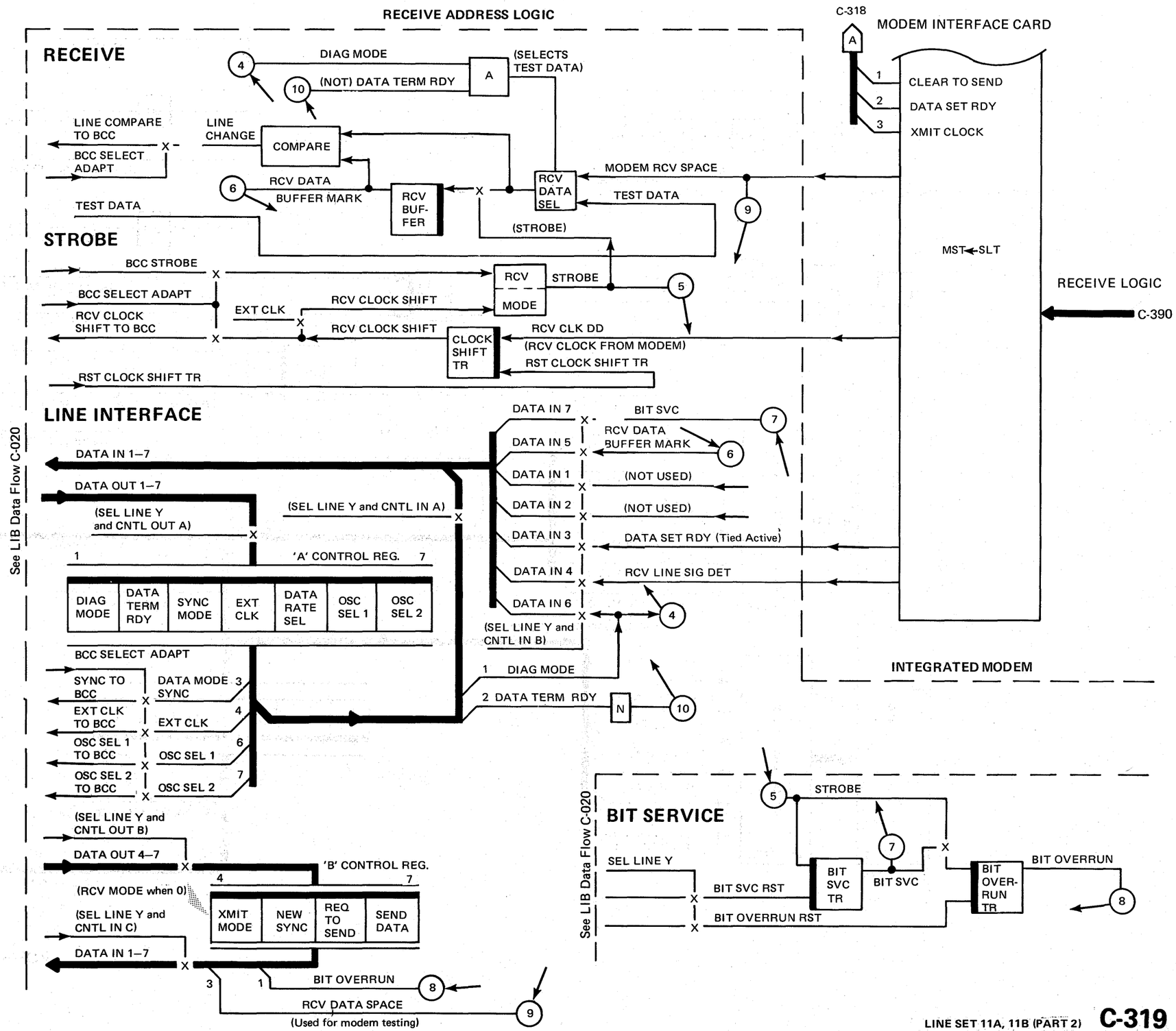
TRANSMIT

1. 'Bit service' is set by the negative going shift of the 'strobe' pulse (see BIT SERVICE).
2. Upon receipt of bit service, the scanner sets Xmit Mode, Req To Send, or Send Data; or a combination of them (depending on the operation).
3. The data is gated into the transmit buffer by the negative going shift of the 'strobe' pulse.
4. During a modem wrap, another interface address sets the test data latch in the scanner (common to all attached lines). The transmit buffer sends the test data to the modem transmitter where it is wrapped to the receiver. The received data returns to the scanner through the receive buffer because DTR is on.

RECEIVE

1. Select receive data or test data.
2. Compare the incoming bit with the status of the receive buffer. If the compare is equal (for example, the incoming bit is a 'mark', and the status of the receive buffer is a 'mark'), the compare output is inactive (not 'line change'). If the compare is not equal (for example, the incoming bit is a 'mark' and the status of the receive buffer is a 'space'), the compare output is active ('line change').
3. The incoming bit is gated into the receive buffer by the negative going shift of the 'strobe' pulse. This occurs at the approximate center of the bit.

The timing charts on C-310 also apply to line sets 11A and 11B.



LIB TYPE 7 AND LINE SET 9A AUTO CALL INTERFACE

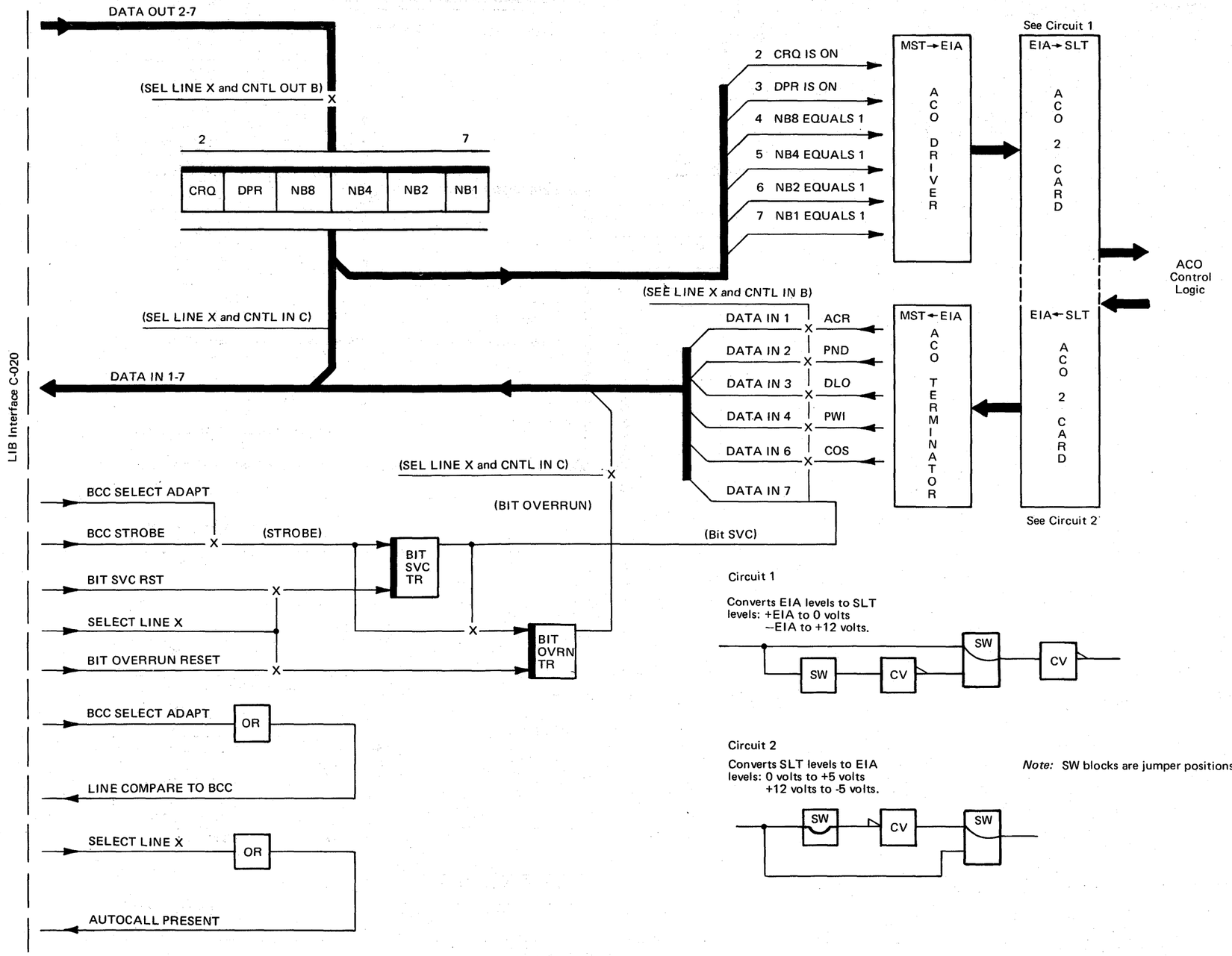
The Auto Call interface is a buffer for status and data transferred between the scanner and the integrated ACO (Automatic Call Originate) feature.

1. ACO status is transferred to the scanner during a CNTL IN B.
2. The scanner transfers information to the ACO during a CNTL OUT B (after a 'bit service' request).
3. The information, transferred during the previous CNTL OUT B, is verified during a CNTL IN C.

BIT SERVICE

'Bit service' and 'Bit service reset' are the interlock controls between the scanner and the Auto Call interface. 'Bit service' is the Auto Call interface request to receive service from the scanner. 'Bit service reset' is the scanner's acknowledgement of the request.

1. The negative going shift of the 'strobe' pulse turns on the 'bit service' trigger. 'Strobe' pulses are obtained from the 'BCC strobe' pulses (derived from internal oscillator 0).
2. The scanner must reset the 'bit service' trigger before the next 'strobe' pulse.
3. If the 'bit service' trigger is not reset, the next 'strobe' pulse gates the output of the 'bit service' trigger to turn on the 'bit overrun' trigger.



Circuit 1

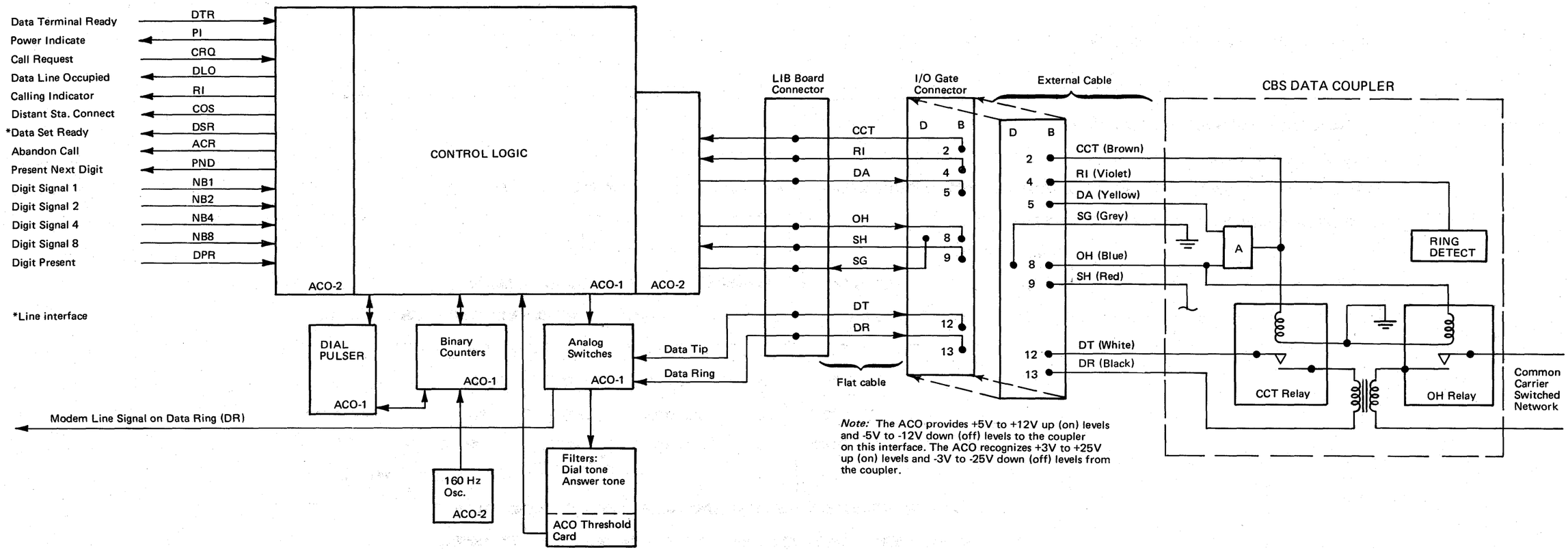
Converts EIA levels to SLT levels: +EIA to 0 volts
−EIA to +12 volts.

Circuit 2

Converts SLT levels to EIA levels: 0 volts to +5 volts
+12 volts to -5 volts.

Note: SW blocks are jumper positions.

AA–ACO INTERFACES



Note: The ACO provides +5V to +12V up (on) levels and -5V to -12V down (off) levels to the coupler on this interface. The ACO recognizes +3V to +25V up (on) levels and -3V to -25V down (off) levels from the coupler.

AUTO CALL LINE INTERFACE LINES

'Data terminal ready' - the autocall interface turns on this line to allow a switched network call to be connected. When this line turns off, 'OH' is turned off. 'DSR' and 'DLO' must go off before DTR can be turned on again.

'Power indicate' - the AA/ACO feature has power.

'Call request' - the autocall interface turns on this line to start a calling sequence.

'Data line occupied' - ACO turns on this line when a calling sequence begins and turns it off 1.5 seconds after disconnection.

'Distant station connected' ('call originate status') ACO turns on this line when answer tone has ended. 'DSC' turns off when the line is disconnected.

'Data set ready' - this line turns on when the call is connected and 'CCT' is on. 'DSR' turns off when the line is disconnected.

'Abandon call' - ACO turns on this line if it receives a nonvalid dial digit or an excessive inter-digit interval from the DTE, or if dialing fails to result in an answered call. 'Call request' and 'data terminal ready' should be dropped and raised again to attempt another call. Optional abandon-call timeouts of 20, 40, or 60 seconds are available by strapping. If ACO is strapped to require EON, the inter-digit timeout is 20 seconds; otherwise, the abandon-call timeout applies.

DATA COUPLER INTERFACE LINES

'OH' - ACO turns on this line to sense dial tone on 'DT' and 'DR'. ACO pulses this line on and off repeatedly to dial a digit. At the end of data transfer, 'OH' turns off to disconnect the line.

'DA' - normally on when the modem and auto answer have power and are ready, ACO turns off this line during dial pulsing.

'SH' - the coupler turns on this line when the telephone set is lifted and the exclusion key is operated.

'RI' - this line from the coupler pulses when the ringing signal is on the telephone line.

'CCT' - the coupler turns on this line when it is ready to accept dial pulsing or signals on 'DT' and 'DR'. 'CCT' is off during dialing and comes on again after a delay.

'SG' - this line is common ground and is the reference level on the interface.

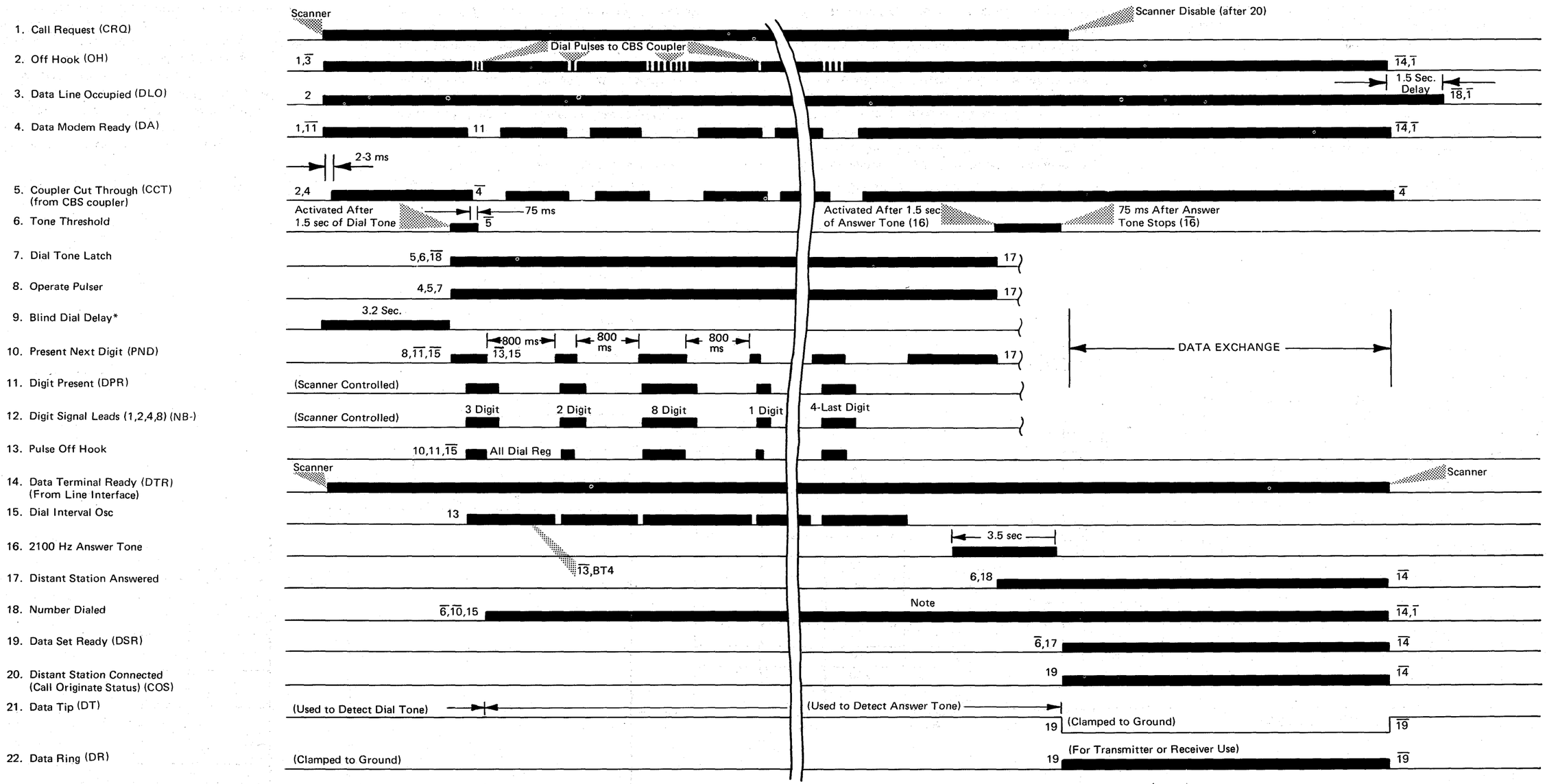
'DT' and 'DR' - analog signals to and from the coupler are on these lines, including dial tone, answer tone, and data.

Valid Digits	1	2	3	4	5	6	7	8	9	0	EON	SEP
Digit Signal 8	0	0	0	0	0	0	0	1	1	0	1	1
Digit Signal 4	0	0	0	1	1	1	1	0	0	0	1	1
Digit Signal 2	0	1	1	0	0	1	1	0	0	0	0	0
Digit Signal 1	1	0	1	0	1	0	1	0	1	0	0	1

Note: Using SEP resets ACO to listen for the dial tone again, which must be recognized within 20 seconds, to allow processing of further dial digits.

AUTOMATIC CALL ORIGINATE TIMING CHART

(Not Using 'Separator' or 'End of Number' Character in Dial Sequence)

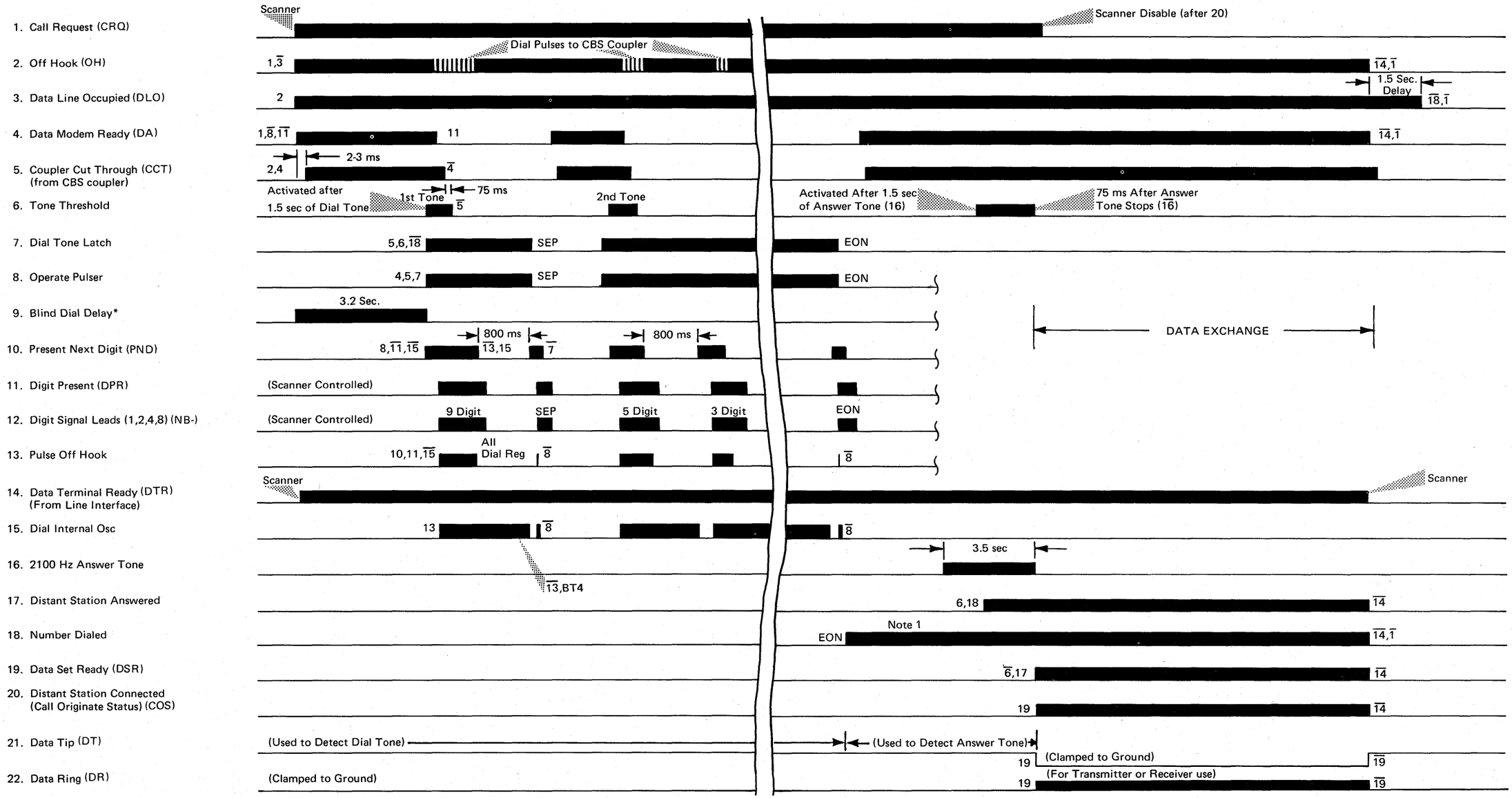


*Instead of a dial tone, an optional 3.2-second 'blind dial' can be used. Use of the delay is controlled by strapping.

Note: The active state of 'number dialed' degates the low-pass filter (used to detect the dial tone threshold). The band-pass filter is then used to detect the 2100 Hz answer-tone threshold.

AUTOMATIC CALL ORIGINATE TIMING CHART, PART 2

(Using 'Separator' and 'End of Number' Character in Dial Sequence)

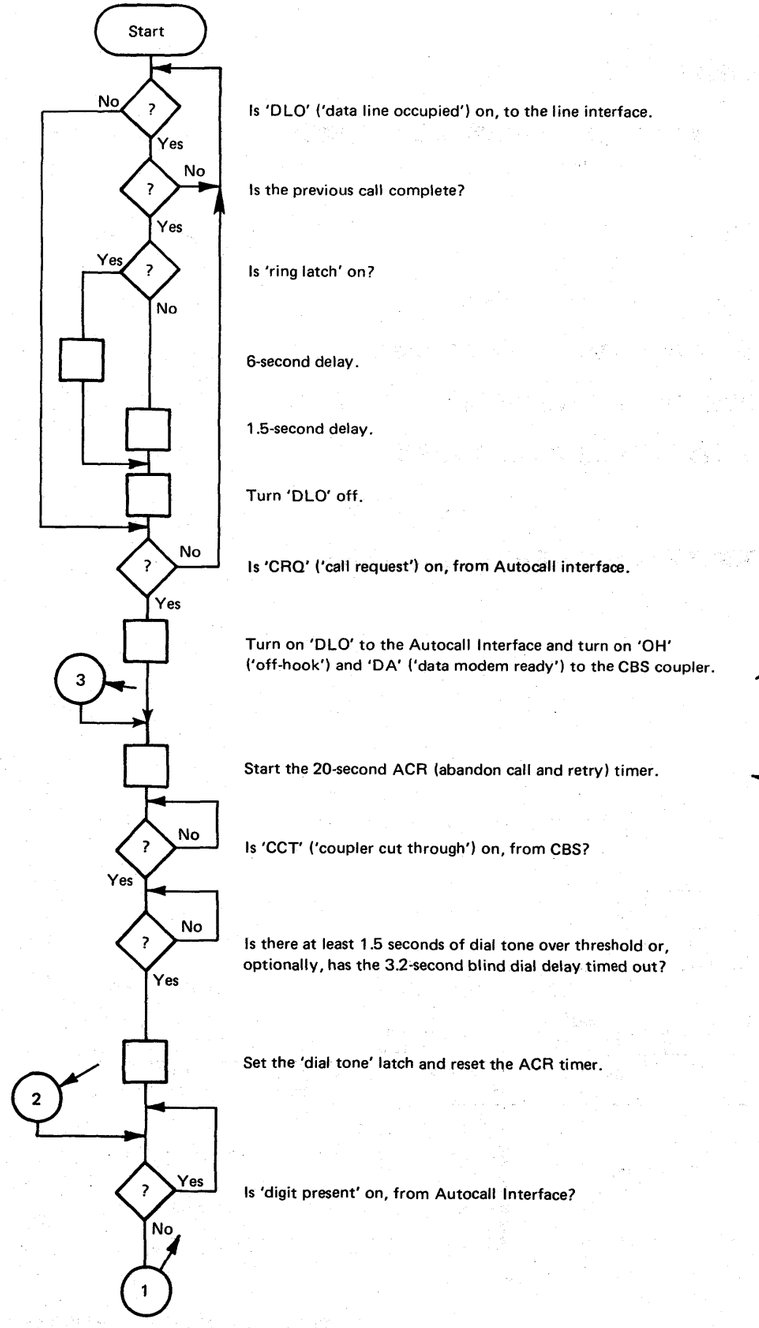


*Instead of a dial tone, an optional 3.2-second 'blind dial' can be used. Use of the delay is controlled by strapping.

Note 1: The active state of 'number dialed' degates the low-pass filter (used to detect the dial tone threshold). The band-pass filter is then used to detect the 2100 Hz answer-tone threshold.

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

AUTOMATIC CALL ORIGINATE OPERATION



Is 'DLO' ('data line occupied') on, to the line interface.

Is the previous call complete?

Is 'ring latch' on?

6-second delay.

1.5-second delay.

Turn 'DLO' off.

Is 'CRQ' ('call request') on, from Autocall interface.

Turn on 'DLO' to the Autocall Interface and turn on 'OH' ('off-hook') and 'DA' ('data modem ready') to the CBS coupler.

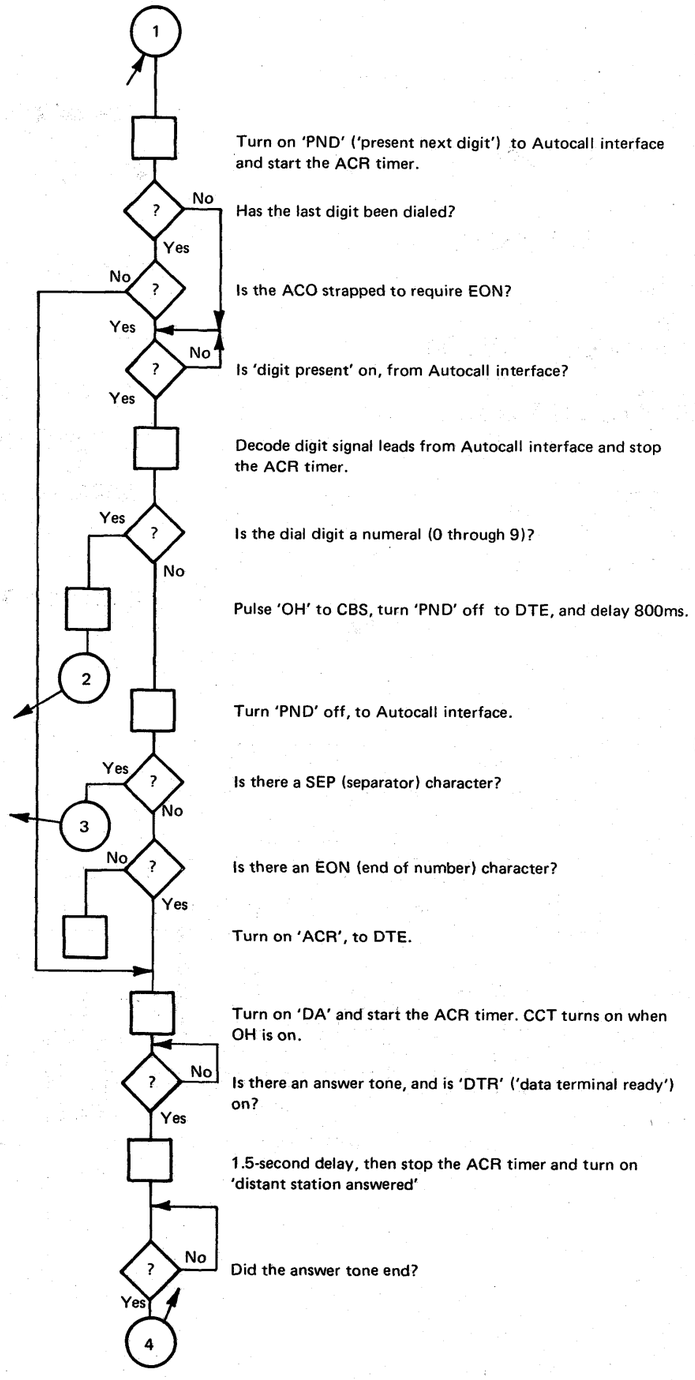
Start the 20-second ACR (abandon call and retry) timer.

Is 'CCT' ('coupler cut through') on, from CBS?

Is there at least 1.5 seconds of dial tone over threshold or, optionally, has the 3.2-second blind dial delay timed out?

Set the 'dial tone' latch and reset the ACR timer.

Is 'digit present' on, from Autocall Interface?



Turn on 'PND' ('present next digit') to Autocall interface and start the ACR timer.

Has the last digit been dialed?

Is the ACO strapped to require EON?

Is 'digit present' on, from Autocall interface?

Decode digit signal leads from Autocall interface and stop the ACR timer.

Is the dial digit a numeral (0 through 9)?

Pulse 'OH' to CBS, turn 'PND' off to DTE, and delay 800ms.

Turn 'PND' off, to Autocall interface.

Is there a SEP (separator) character?

Is there an EON (end of number) character?

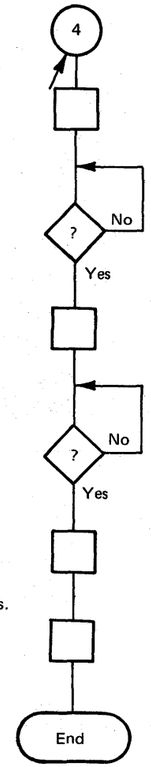
Turn on 'ACR', to DTE.

Turn on 'DA' and start the ACR timer. CCT turns on when OH is on.

Is there an answer tone, and is 'DTR' ('data terminal ready') on?

1.5-second delay, then stop the ACR timer and turn on 'distant station answered'

Did the answer tone end?



Turns on 'DSR' ('data set ready') to enable the modem to use 'DR' ('data ring'). Turn on DSR and DSC to autocall interface.

Is 'CRQ' off, from autocall interface? (dropped by scanner after COS active.)

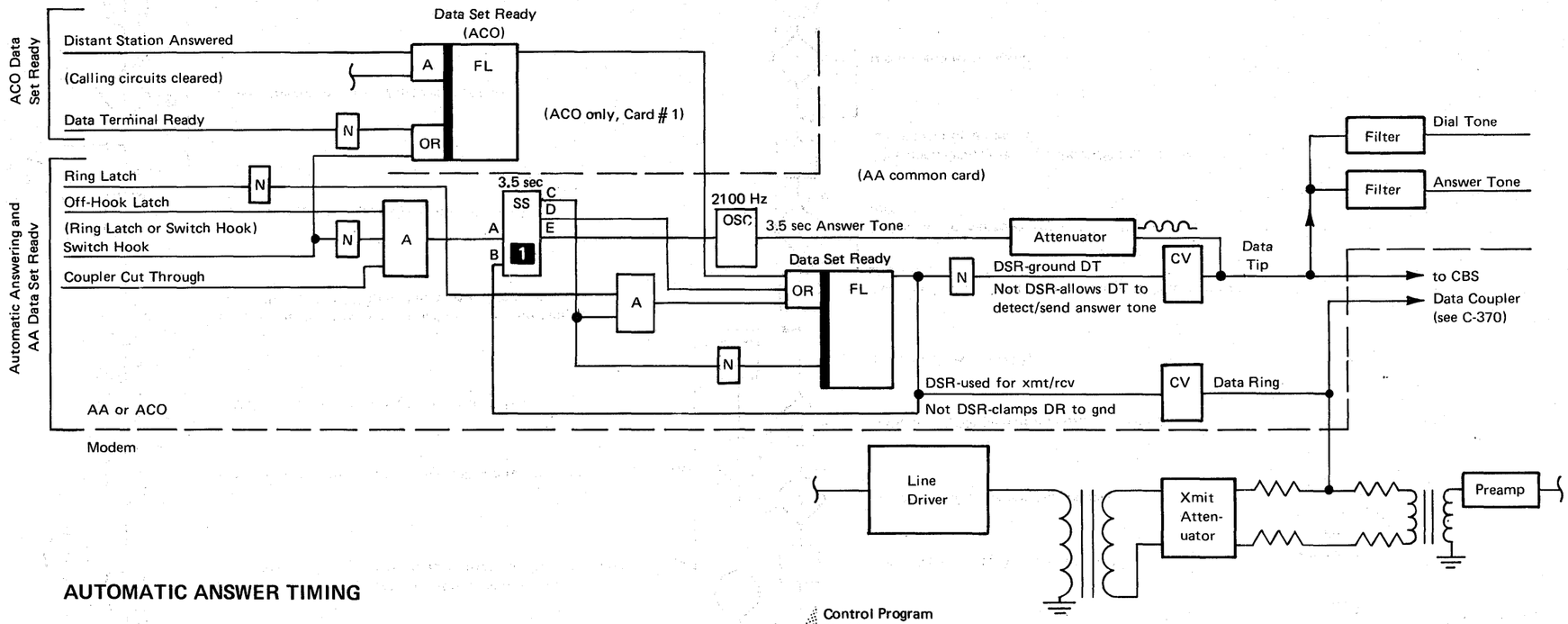
Call is complete and data exchange begins.

Is 'DTR' off, from line interface?

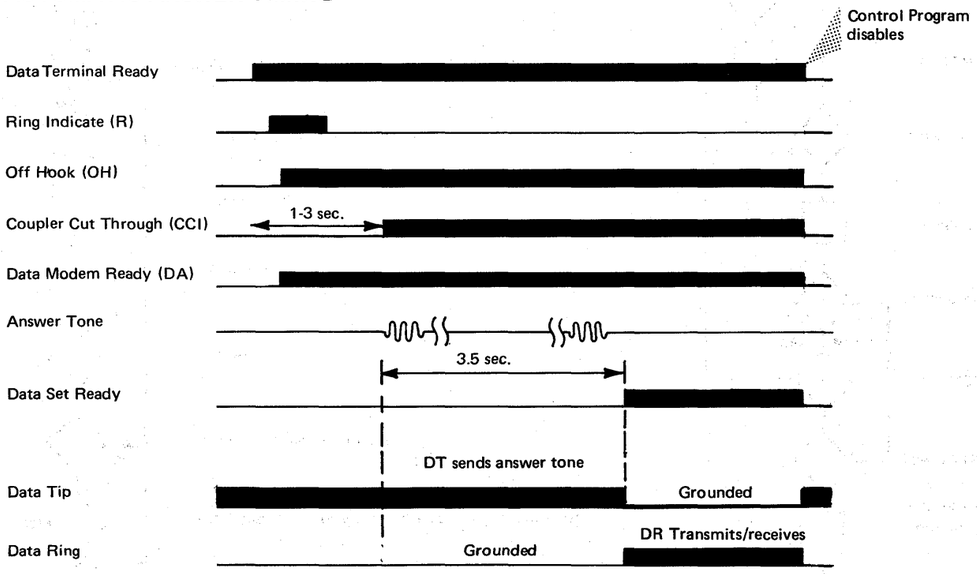
Turn off 'OH', to CBS, and turn off 'DSC' to autocall interface and 'DSR' to line interface.

1.5-second delay, then turn off 'DLO', to autocall interface.

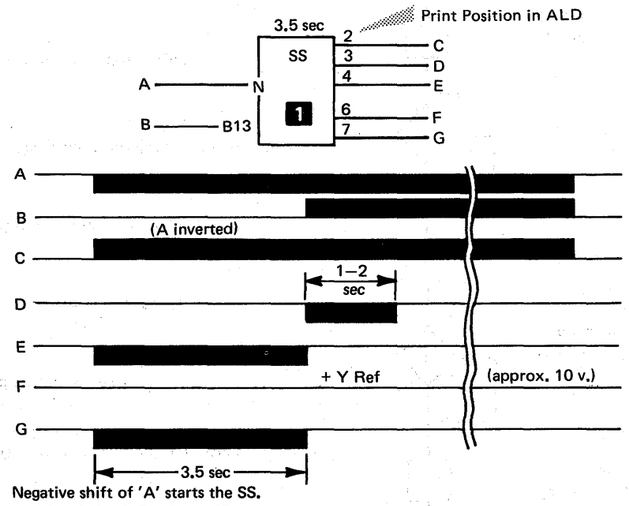
AUTOMATIC ANSWERING



AUTOMATIC ANSWER TIMING

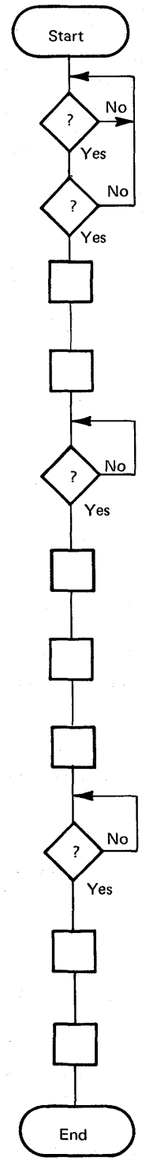


1 Circuit Timing for 3.5 sec SS
(+ and – SLT levels are shown in the timing chart below)



Negative shift of 'A' starts the SS.
Positive shift of 'E' triggers 'D'.
Positive shift of 'A' causes 'B' and 'C' to go negative.

AUTOMATIC ANSWERING OPERATION



Is 'DTR' ('data terminal ready') on?

Is 'ring indicate' on, from data coupler?

Turn 'OH' ('off-hook') and 'DA' ('data modem ready') on, to CBS. (With AA and not ACO, 'DA' is always on.)

1- to 3-second delay by data coupler.

Is 'CCT' ('coupler cut through) on, from data coupler?

Transmit a 3.5-second answer tone.

Turn 'DSR' ('data set ready') on and enable the modem to use 'DR' ('data ring').

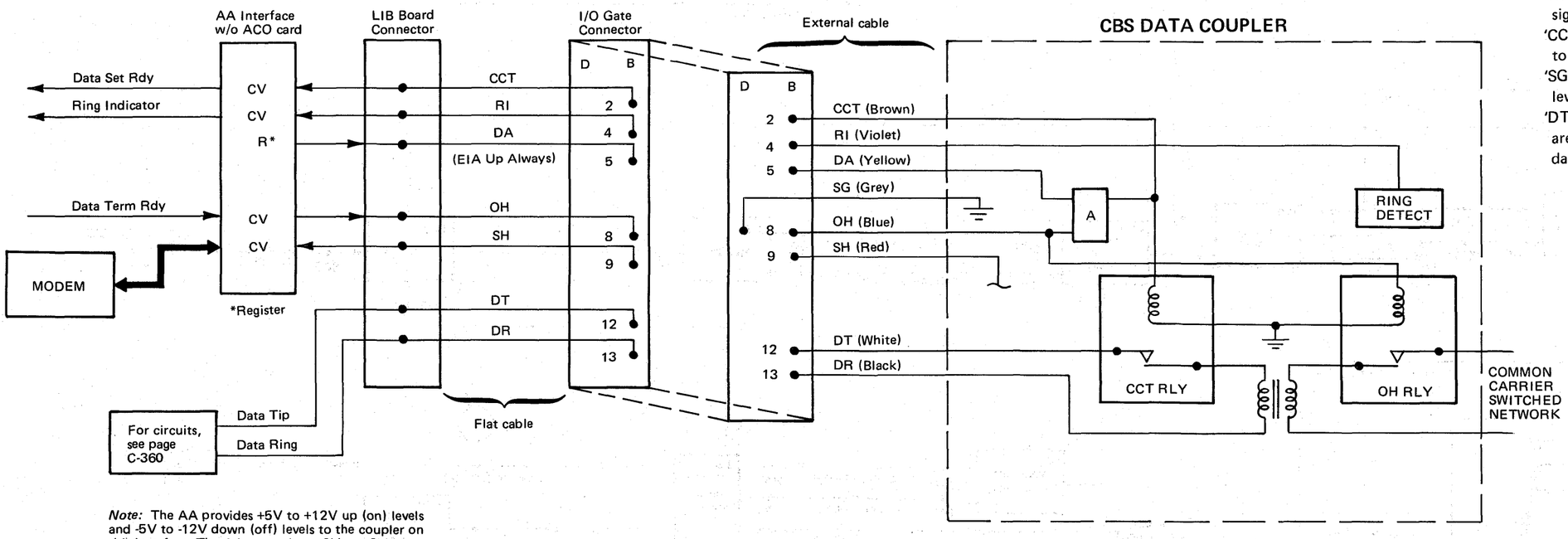
Data communication takes place.

Is 'DTR' off, from line set?

Turn off 'OH', to data coupler, and 'DSR', to line set. Data coupler disconnects the line.

With ACO, 'DLO' ('data line occupied') turns off after 1.5 seconds.

AUTOMATIC ANSWERING (PART 2)



Note: The AA provides +5V to +12V up (on) levels and -5V to -12V down (off) levels to the coupler on this interface. The AA recognizes +3V to +25V up (on) levels and -3V to -25V down (off) levels from the coupler.

'Data terminal ready' - the line set turns on this line to allow a switched network call to be connected. When this line drops, 'OH' is turned off and the call is disconnected.

'Ring indicator' - this logic level is a conversion of 'RI' from the coupler.

'Data set ready' - when answer tone has been sent and CCT is on, the AA feature turns on this line to the line set.

'OH' - the AA feature turns on this line to answer an incoming call, and to clear a path through the data coupler for answer tone. At the end of data transfer, 'OH' turns off to disconnect.

'DA' - this line is on when the modem and AA feature (without ACO) have power and are ready to use DT and DR.

'SH' - the coupler turns on this line when the telephone set is not cradled and the exclusion key is operated.

'RI' - this line from the coupler pulses when the ringing signal is on the telephone line.

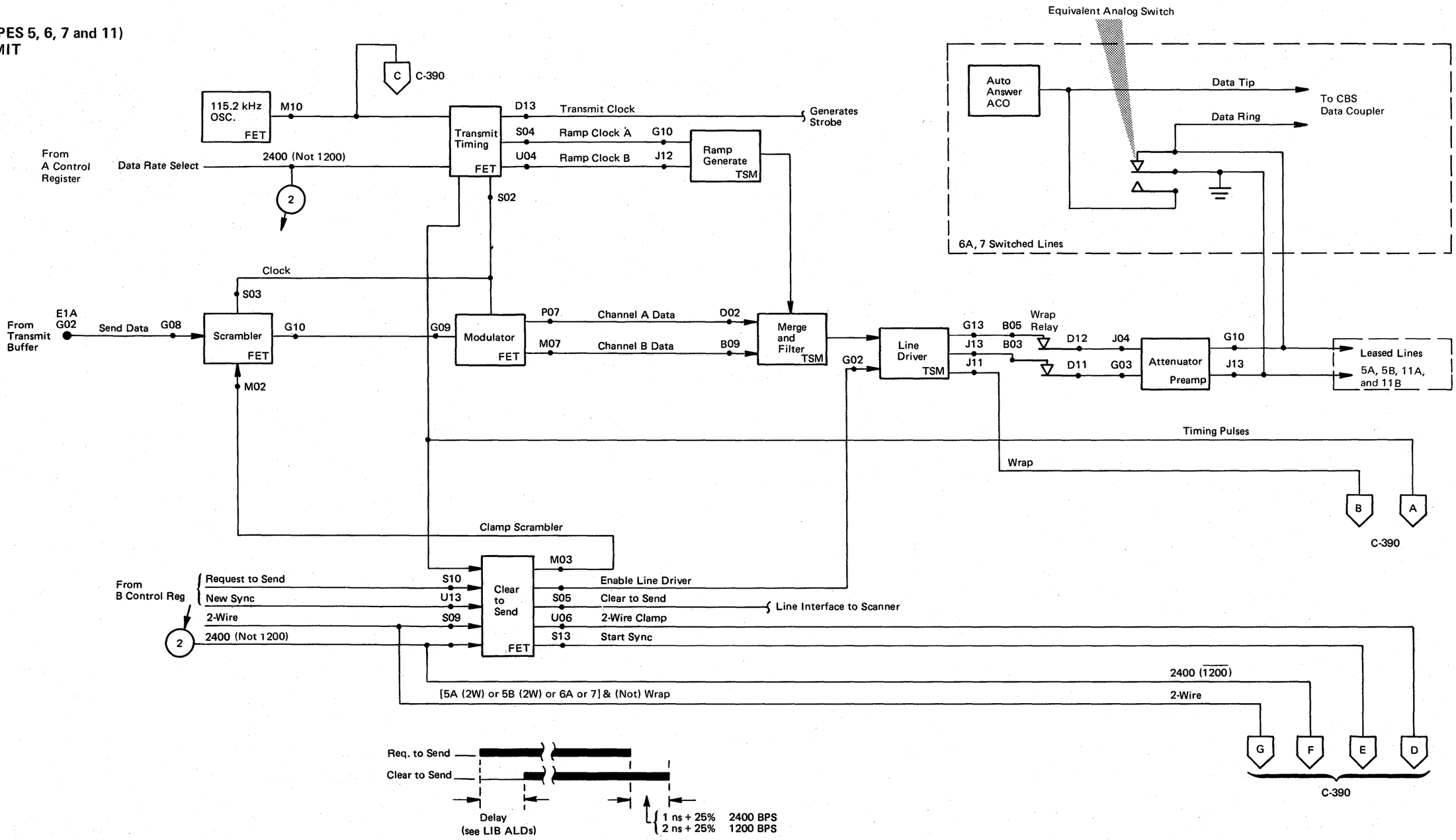
'CCT' - the coupler turns on this line when it is ready to accept signals on DT and DR.

'SG' - this line is common ground and is the reference level on the interface.

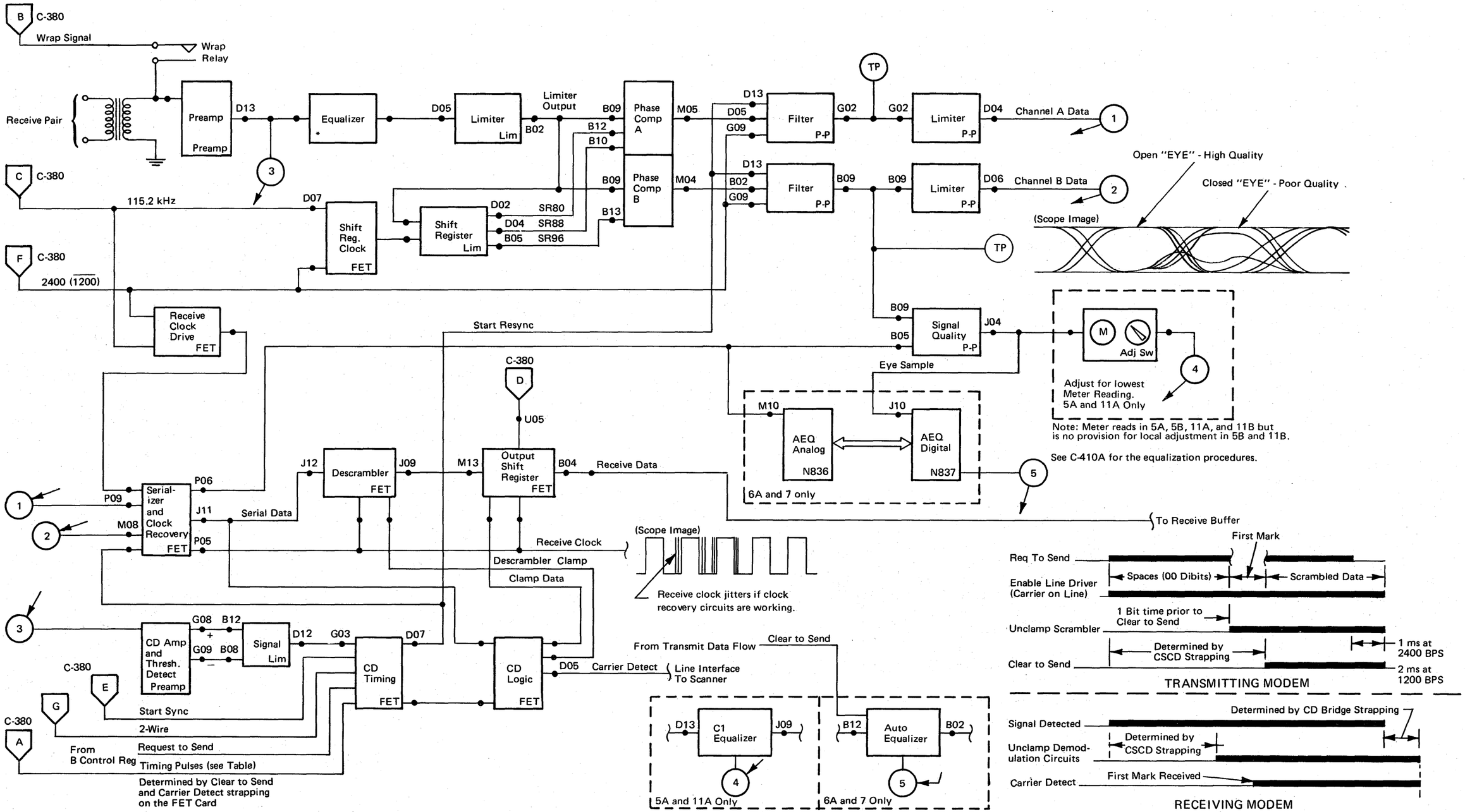
'DT' and 'DR' - analog signals to and from the coupler are on these lines, including the answer tone and data.

MODEM DATA FLOW

(LIB TYPES 5, 6, 7 and 11) TRANSMIT



MODEM DATA FLOW, PART 2 RECEIVE (LIB TYPES 5, 6, 7, AND 11)



SERVICE TECHNIQUES AND SPECIAL TOOLS

SCOPING HINTS AND PRECAUTIONS (LIB TYPES 5, 6, 7, and 11)

The amplitude of some analog signals in the integrated modem is quite small. Try a greater vertical gain on the scope before believing that there is no signal at a test point. Two sync points suffice for tracing signal flow in Test 2 by the observation of analog signals: for transmit signals, use 'ramp clock A', S04; for received signals, use 'sample pulse', B05 (see page C-420A). All scoping described in LIBs 5, 6, 7, and 11 is done with a X10 probe.

In the case of apparent integrated modem malfunction, it may be found that the trouble is with the communications channel, rather than the modem. It is advantageous to know how to scope the line signal in this case and to be familiar with the appearance of the line signal and eye pattern characteristic of a reasonably usable line. Therefore, take every opportunity to view these signals in relation to each other. Refer to the procedure given later for scoping line signals, and to Waveform #030.

dB METER AND USES

The dB meter is used to make benchmark measurements and later to compare existing characteristics of the integrated modem and line to the benchmarks. The dB meter is also used in problem determination in the Line-Side Diagnostic. The dB meter (P/N 453545) has these main characteristics: measurable levels, +3 dBm to -60 dBm; frequency response, 200 Hz to 200 kHz; bridging or terminating input impedance; and an internal variable attenuator for simulating line losses. The meter contains a booklet of instructions for its use.

ADJUSTMENTS (LIB TYPES 5, 6, 7, and 11)

There are three adjustments on the integrated modem. Two of them (transmit signal level and receive sensitivity) are made by strapping at the time of installation and the third (signal quality) is made when the post-processor card is replaced for any reason.

Transmit Signal Level

Preamp card:

- Switched network (jumper for requirements of the DAA—see VL004, VN004)
- 4 wire leased line (jumper for 0 dBm—see VJ004 or VW000)
- 2 wire leased line (jumper for 0 dBm—see VJ004)

Receive Sensitivity

Transmit card:

- -27 dBm (jumper 'A'—see VJ004 for LIB 5 or VW000 for LIB 11)
- -40 dBm for LIB 6 and LIB 7 (no jumper—see VL004 or VN004)

Signal Quality Meter (LIB 5 or LIB 11 only)

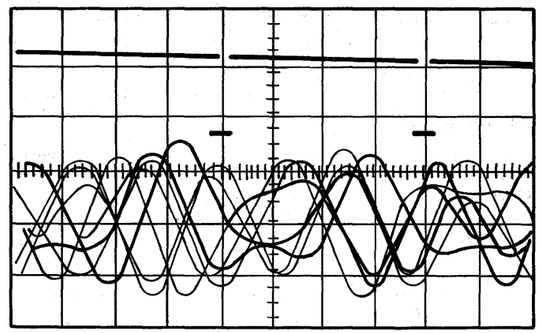
See adjustment procedure on VJ005 for LIB 5 or VW004 for LIB 11.

BENCHMARK REFERENCE (LIB 5 and LIB 11 ONLY)

When the modem is installed, benchmark measurements (transmit signal level and receive sensitivity) are made and recorded for future reference. In case the diagnostic procedures given later do not locate the source of a trouble, compare the existing characteristics to the benchmarks. When line problems may be involved, comparison to benchmark measurements is essential.

LINE SCOPING PROCEDURE

Observe line signals at every opportunity, particularly when the existing measurements differ from benchmarks. Check both transmit and receive signals when scoping line signals. Rapid and irregular horizontal shifting of a signal pattern indicates frequency distortion; rapid and irregular vertical amplitude variations indicate noise. The signal illustrated below contains a mix of transmission impairments, but is a legible signal when received by the modem.



Scoping line signals requires use of the Line Scoping Transformer (P/N 453646) because this device has a 1:1 coupling ratio, has negligible bridging loss, and has negligible insertion loss. Other methods of scoping line signals may cause imbalances in the common carrier equipment. The line scoping transformer has a cable and fitting for coupling directly to the oscilloscope input. It also has banana plug jacks for use of the CE test leads to connect the line scoping transformer to the line. Do not use the line scoping transformer to simulate a C-message-weighted filter for noise measurements; although the frequency response of the device is specified as 300 Hz to 3500 Hz, its actual bandwidth does not discriminate sufficiently for voiceband noise measurements.

Use the following scope setup for scoping 2400 bps line signals (LIB types 5, 6, 7, and 11):

Transmit
Sync on 'ramp clock A', (FET)S04
1V/div. vertical
0.2 ms/div. horizontal

Receive
Sync on 'ramp clock A', (FET)S04
0.005V/div. (-33 dB receive level) vertical
0.05V/div. (-16 dB receive level) vertical
0.2 ms/div. horizontal

Note: At the slow sweep speed, the oscilloscope creates some distortion on the right side of the screen, so observe mainly the first few cycles of the display. Ignore the phase-change areas; they cannot be visually deciphered.

The purpose of using 'ramp clock A' as a sync point for scoping received line signals is to observe the drift of the signal (due to channel distortion or oscillator frequency difference). The drift and jitter of the receive clock, B07 (modem interface card), can also be observed using the 'ramp clock A' sync. (Clock correction circuits are not working if the receive clock does not jitter.)

Scoping of the received line signal may be repeated, using 'sample pulse' (P-P) as the sync point. Both signals should be steady horizontally; otherwise, the oscillator frequencies of the two modems differ beyond the correction capability of the receive clock recovery circuits and the FET card should be replaced in the local and/or remote modem.

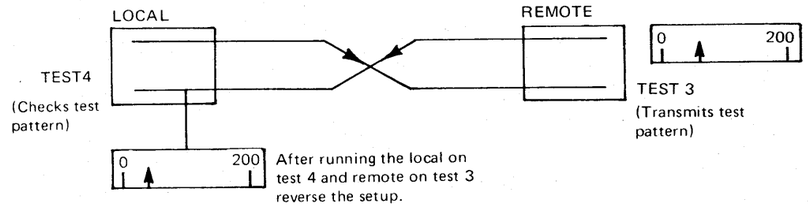
EQUALIZATION PROCEDURE

FOR LIB 5 AND LIB 11

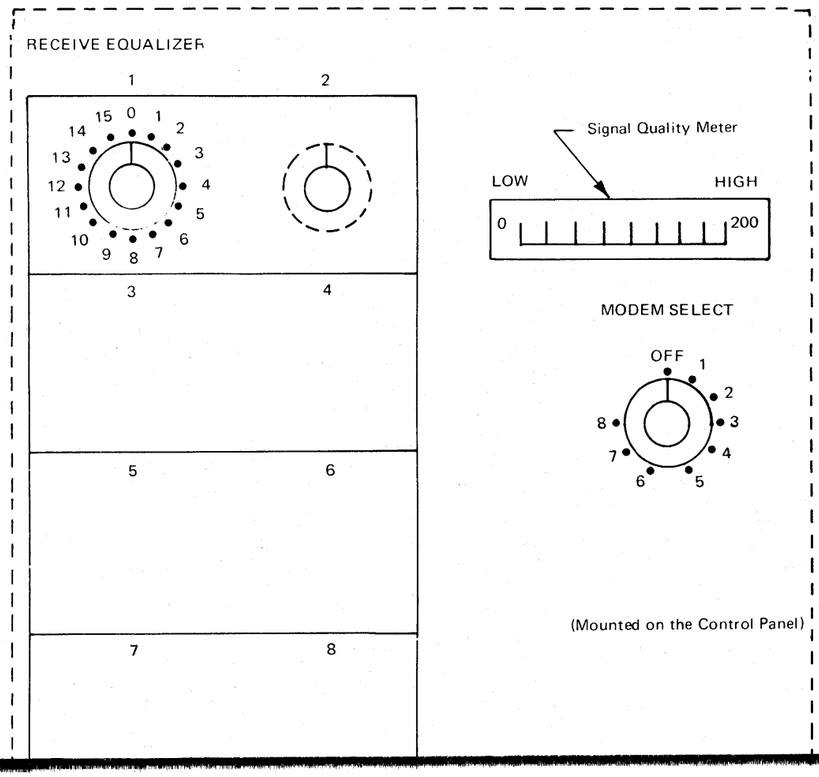
The channel distortions that can be compensated by equalization do not significantly affect 1200 bps speed on the 3705 modem or the 3872. Therefore, successful operation at 1200 bps indicates that equalization may allow successful 2400 bps operation. Failures at 1200 bps usually indicate a need for line maintenance. To adjust equalization, first establish the appropriate equalization set up (see Figure) then, turn the Equalizer switch to each marked position successively, noting the meter reading at each position. For the best operation, select the position that has the lowest meter reading. Normal, meter readings vary according to the distortion and incidence of noise on a particular channel. Use the meter reading during normal, satisfactory operation as a reference to identify abnormally high, troublesome readings. If a change of equalization does not result in satisfactory operation, line maintenance is required and should be followed by re-equalization.

POINT TO POINT SETUP

Select the desired modem with the modem select switch.



Note: The unit that is in test 4 must make the equalizing adjustment on a point to point setup.

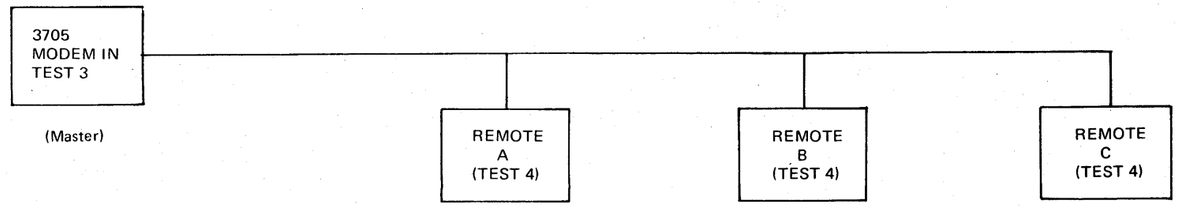


MULTIPOINT TRIBUTARY SETUP

Select the desired modem with the modem select switch

RECEIVE EQUALIZATION

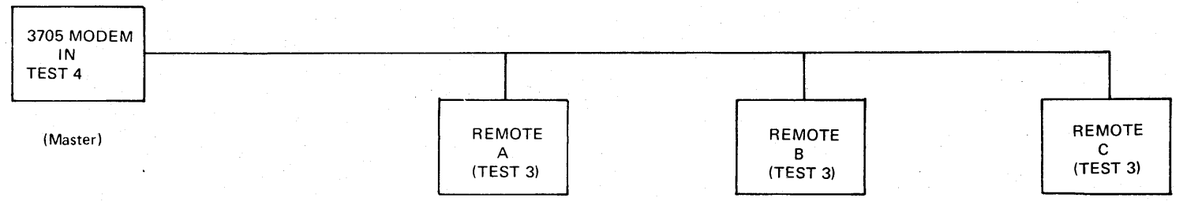
Transmit from the 3705 modem in test 3 to the remote units set to test 4. Adjust the receive equalizer in each remote. Use the lowest EQUALIZER switch setting as read on the remote meter.



TRANSMIT EQUALIZATION

Transmit from one remote at a time to the master station and adjust the transmit equalizer at the remote.

The meter readings for multipoint tributary transmit equalization must be obtained (by separate voice connection) from the operator at the controlling (master) station. There is no equalizer at the controlling (master) station, the adjustment must be made at the remote. The transmit and receive equalizers are at the remote stations.



IFT Routines:

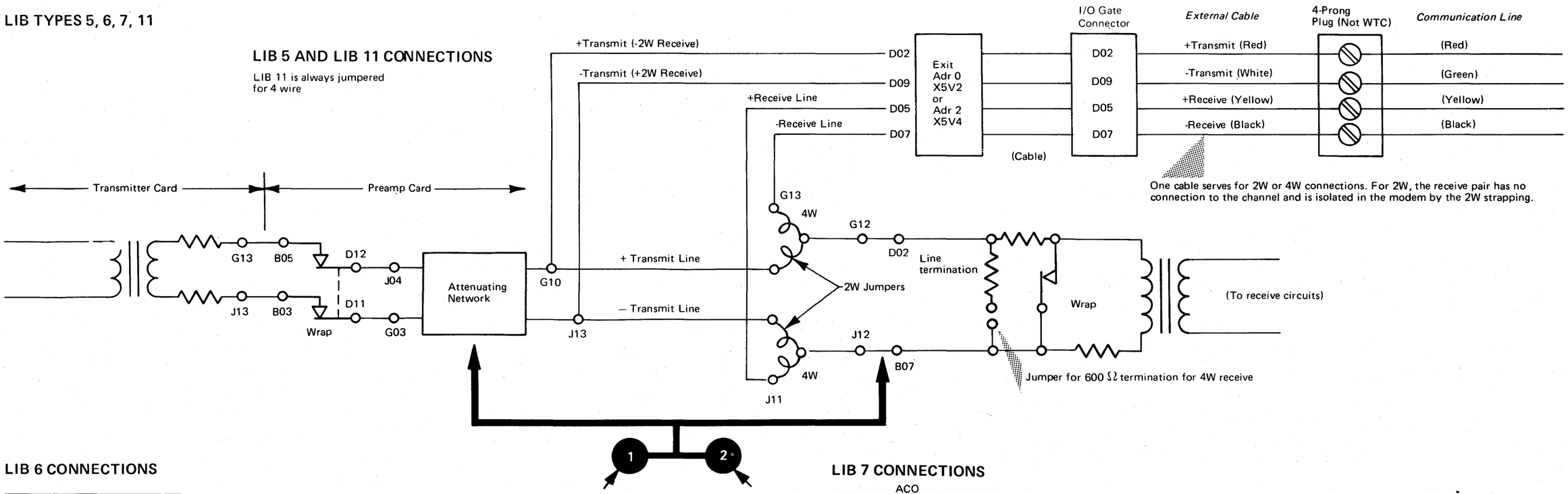
Type 1 Commications Scanner = 15C8 Test 3
Type 1 Commications Scanner = 15CA Test 4

LINE CONNECTION CONTINUITY

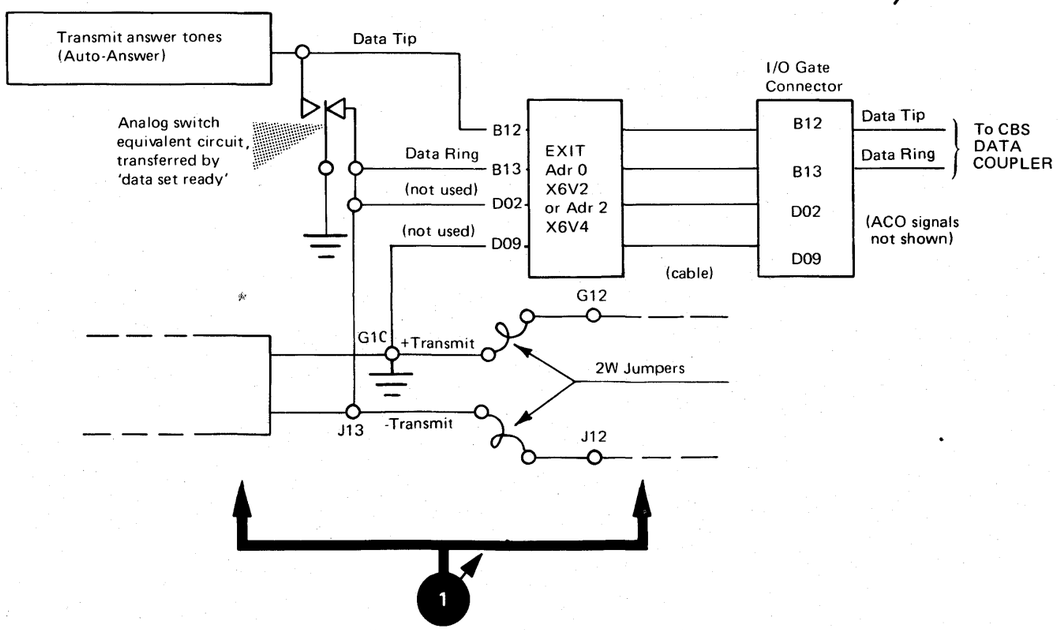
LIB TYPES 5, 6, 7, 11

LIB 5 AND LIB 11 CONNECTIONS

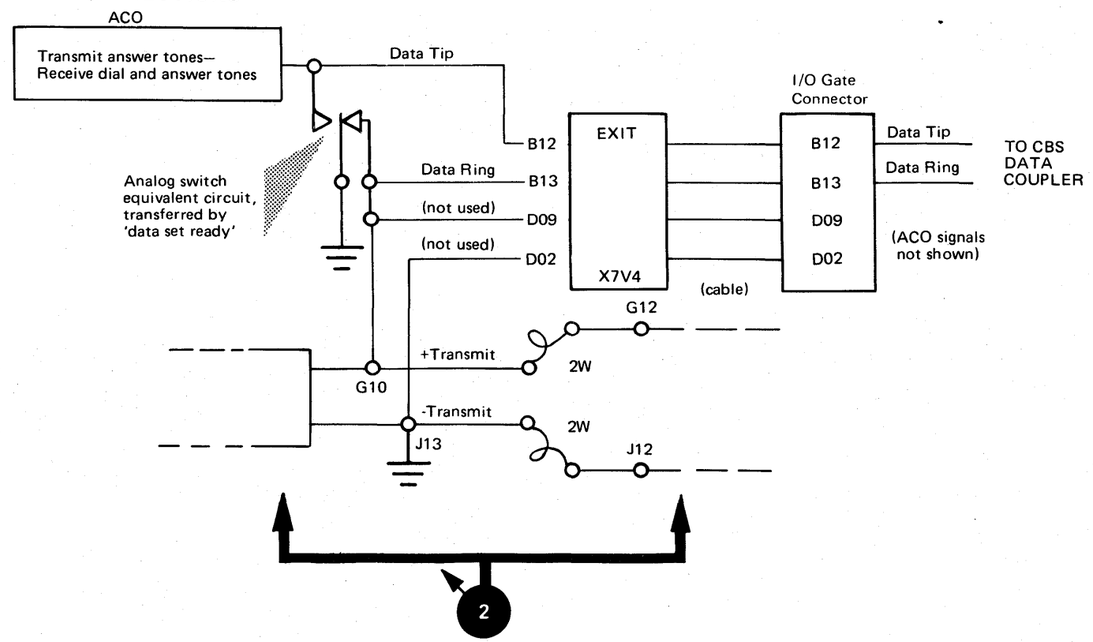
LIB 11 is always jumpered for 4 wire



LIB 6 CONNECTIONS



LIB 7 CONNECTIONS

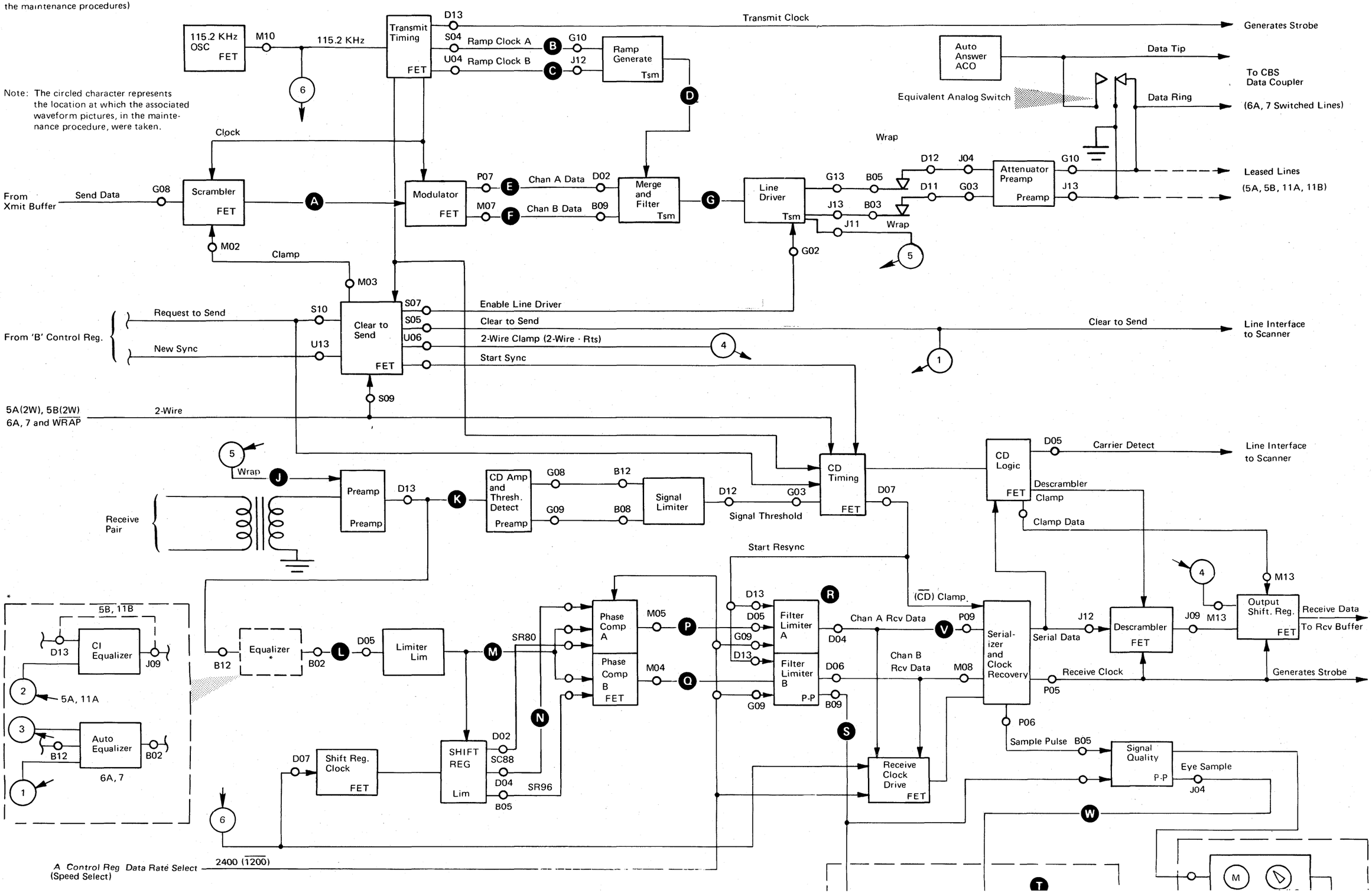


MODEM COMPREHENSIVE DATA FLOW

LIB TYPES 5, 6, 7, 11

(Fold out for use with the maintenance procedures)

Note: The circled character represents the location at which the associated waveform pictures, in the maintenance procedure, were taken.



PANEL PROCEDURES FOR IBM INTEGRATED MODEMS — EMULATION PROGRAM

The panel test (integrated modem) procedures must be selected for the control program at system generation time.

The integrated modem tests check for errors in data transfer that may be caused by a failing modem unit.

The term "remote" refers to the modem at the other end.

Integrated Test 2 (Modem Internal Wrap) with EP
(Line Sets 5A, 5B, 6A, 8A, 8B, 9A, 12A, 12B, LIB 7)

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set up			
FUNCTION 5	0 0 0	Press INTERRUPT	Loads test character in transmit buffer 1, position 0
FUNCTION 5	0 0 0 9 9	Press INTERRUPT	Loads test character in transmit buffer 1, position 0
FUNCTION 5	0 8 9 Subchannel Address	Press INTERRUPT	Transmit test character and repeat
FUNCTION 5	0 8 A Subchannel Address	Press INTERRUPT	Set receive state, PCF 7.
Part 2: Observations			
FUNCTION 6	0 0 0 Subchannel Address See Note 1	Do not press INTERRUPT. Set the function and the subchannel address.	ICW is displayed in DISPLAY A and DISPLAY B
FUNCTION 5	0 8 A Subchannel Address See Note 2	Press INTERRUPT	DISPLAY B = Space counter
Part 3: End of Test			
FUNCTION 5	0 8 F Subchannel Address	Press INTERRUPT	Ends Test 2.

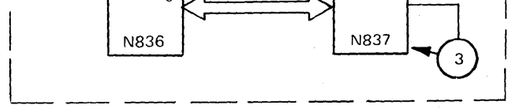
Note 1: Modem line bits 0, 2, and 3 should be on; any one or all being off indicates a Test 2 failure.

Note 2: Observe the space counter in DISPLAY B; if it is incrementing, this is a Test 2 failure.

DISPLAY A, BYTE 1 LIGHTS

The modem lines are displayed in DISPLAY A for EP and DISPLAY B for NCP or PCP

Bit	Modem Lines
0	Clear to Send
1	Ring Indicator
2	Data Set Ready
3	Receive Line Signal
4	Receive Data Bit Buffer
5	Diagnostic Wrap Mode
6	Bit Service Request
7	Zero (not used)



Adjust for lowest meter reading.
Only 5A and 11A. See C-410A.

Integrated Modem Test 3 (Transmit all Marks)
with EP (Line Sets 5A, 5B, 6A, 8A, 8B, 9A,
12A, 12B, LIB 7)

For switched line sets, the auto-call or auto-answer test is used to establish the line connection.

When using this test, place the remote modem in Test 4.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set up			
FUNCTION 5	0 8 9 Subchannel Address	Press INTERRUPT	Transmit test character and repeat (transmits all marks).
Part 2: Observations			
FUNCTION 6	0 0 0 Subchannel Address	Do not press INTERRUPT	ICW displayed (See Note 1)
FUNCTION 5		Do not press INTERRUPT	DISPLAY A=00XX DISPLAY B= FC (TEST) (See Note 2)
Part 3: End of Test			
FUNCTION 5	0 8 F Subchannel Address	Press INTERRUPT	Ends test 3.

Note 1: Modem line bits 0 and 2 should be on; if either bit is off, a local integrated modem failure is indicated.

Note 2: If setmode is accepted, this display indicates the test has been accepted.

Integrated Modem Test 4 (Receive All Marks)
with EP (Line Sets 5A, 5B, 6A, 8A, 8B, 9A,
12A, 12B, LIB 7)

For switched line sets, the auto-call or auto-answer test is used to establish the line connection.

When using this test, place the remote modem in Test 3.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set up			
FUNCTION 5	0 8 A Subchannel Address	Press INTERRUPT	Initializes the test.
Part 2: Observations			
FUNCTION 6	0 0 0 Subchannel Address See Note 1	Do not press INTERRUPT	ICW is displayed in DISPLAY A and DISPLAY B.
FUNCTION 5	See Note 2		DISPLAY B = Space counter
PART 3: END OF TEST			
FUNCTION 5	0 8 F Subchannel Address	Press INTERRUPT	Ends Test 4.

Note 1: Modem line bits 2 and 3 should be on; either or both off, indicates a Test 4 failure. If the failure indication is bit 2, end Test 4 and restart at Test 2. If you return to this point, you have a local integrated modem problem. If the failure is bit 3, recheck both local and remote modem cables and run Test 2; if it runs successfully, you probably have a common carrier problem and should end Test 4. If both bits are on, go on to the next part.

Note 2: Display the space counter in DISPLAY B, if the counter is incrementing, this is a failure and you should [illegible] the remote modem (leased lines) [illegible] the space counter is not incrementing, Test 4 has [illegible] successfully.

PANEL PROCEDURES FOR IBM INTEGRATED MODEMS — EMULATION PROGRAM

The panel test (integrated modem) procedures must be selected for the control program at system generation time.

The integrated modem tests check for errors in data transfer that may be caused by a failing modem unit.

The term "remote" refers to the modem at the other end.

Integrated Test 2 (Modem Internal Wrap) with EP
(Line Sets 5A, 5B, 6A, 8A, 8B, 9A, 12A, 12B, LIB 7)

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set up			
FUNCTION 5	0 0 0 Test Character	Press INTERRUPT	Loads test character in transmit buffer 1, position 0
FUNCTION 5	0 0 0 9 9	Press INTERRUPT	Loads test character in transmit buffer 1, position 0
FUNCTION 5	0 8 9 Subchannel Address	Press INTERRUPT	Transmit test character and repeat
FUNCTION 5	0 8 A Subchannel Address	Press INTERRUPT	Set receive state, PCF 7.
Part 2: Observations			
FUNCTION 6	0 0 0 Subchannel Address See Note 1	Do not press INTERRUPT. Set the function and the subchannel address.	ICW is displayed in DISPLAY A and DISPLAY B
FUNCTION 5	0 8 A Subchannel Address See Note 2	Press INTERRUPT	DISPLAY B = Space counter
Part 3: End of Test			
FUNCTION 5	0 8 F Subchannel Address	Press INTERRUPT	Ends Test 2.

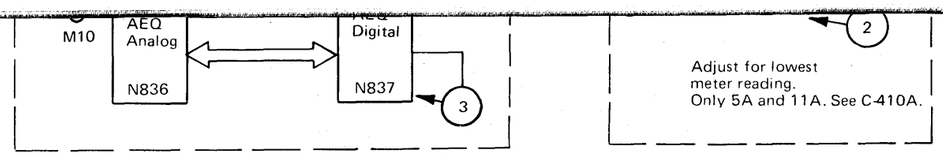
Note 1: Modem line bits 0, 2, and 3 should be on; any one or all being off indicates a Test 2 failure.

Note 2: Observe the space counter in DISPLAY B; if it is incrementing, this is a Test 2 failure.

DISPLAY A, BYTE 1 LIGHTS

The modem lines are displayed in DISPLAY A for EP and DISPLAY B for NCP or PCP

Bit	Modem Lines
0	Clear to Send
1	Ring Indicator
2	Data Set Ready
3	Receive Line Signal
4	Receive Data Bit Buffer
5	Diagnostic Wrap Mode
6	Bit Service Request
7	Zero (not used)



Integrated Modem Test 3 (Transmit all Marks)
with EP (Line Sets 5A, 5B, 6A, 8A, 8B, 9A,
12A, 12B, LIB 7)

For switched line sets, the auto-call or auto-answer test is used to establish the line connection.

When using this test, place the remote modem in Test 4.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set up FUNCTION 5	0 8 9 Subchannel Address	Press INTERRUPT	Transmit test character and repeat (transmits all marks).
Part 2: Observations FUNCTION 6	0 0 0 Subchannel Address	Do not press INTERRUPT	ICW displayed (See Note 1)
FUNCTION 5		Do not press INTERRUPT	DISPLAY A=00XX DISPLAY B= FC (TEST) (See Note 2)
Part 3: End of Test FUNCTION 5	0 8 F Subchannel Address	Press INTERRUPT	Ends test 3.

Note 1: Modem line bits 0 and 2 should be on; if either bit is off, a local integrated modem failure is indicated.

Note 2: If setmode is accepted, this display indicates the test has been accepted.

Integrated Modem Test 4 (Receive All Marks)
with EP (Line Sets 5A, 5B, 6A, 8A, 8B, 9A,
12A, 12B, LIB 7)

For switched line sets, the auto-call or auto-answer test is used to establish the line connection.

When using this test, place the remote modem in Test 3.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set up FUNCTION 5	0 8 A Subchannel Address	Press INTERRUPT	Initializes the test.
Part 2: Observations FUNCTION 6	0 0 0 Subchannel Address See Note 1	Do not press INTERRUPT	ICW is displayed in DISPLAY A and DISPLAY B.
FUNCTION 5	See Note 2		DISPLAY B = Space counter
PART 3: END OF TEST FUNCTION 5	0 8 F Subchannel Address	Press INTERRUPT	Ends Test 4.

Note 1: Modem line bits 2 and 3 should be on; either or both off, indicates a Test 4 failure. If the failure indication is bit 2, end Test 4 and restart at Test 2. If you return to this point, you have a local integrated modem problem. If the failure is bit 3, recheck both local and remote modem cables and run Test 2; if it runs successfully, you probably have a common carrier problem and should end Test 4. If both bits are on, go on to the next part.

Note 2: Display the space counter in DISPLAY B, if the counter is incrementing, this is a failure and you should [illegible] the remote modem (local lines) if the space counter is not incrementing, Test 4 has run successfully.

PANEL PROCEDURES FOR IBM INTEGRATED MODEMS—EMULATION PROGRAM, PART 2

Integrated Modems
Auto-answer Test with EP
(Line Sets 6A, 8B, 9A, 12B, LIB 7)

All test functions are preceded by an auto-answer or auto-call initialization. Any 2X or 4X function can be used to test a line with an auto-answer or auto-call interface. See 'Line Test Function (Panel Test) in *Guide to Using the IBM 3705 Communications Controller Control Panel,* GA27-3087 for setting of switch C. Use a 4X function when receiving data and a 2X function when transmitting data. Determine how data is to be handled (CCBOPT field of the CCB) for the line before selecting the appropriate function. Proper consideration should be given to compare characters and buffer load operations although the tests execute without any preliminary setup.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set up FUNCTION 5	0 2/4 X Subchannel Address	Press INTERRUPT	Initializes the test.
Part 2: Observations FUNCTION 5	(See Note 1) (Display is lost if not in in FUNCTION 5)		Level 2 codes displayed.
FUNCTION 6	0 0 0 Subchannel Address (See Note 2)	Do not press INTERRUPT	ICW is displayed in DISPLAY A and DISPLAY B
Part 3: End of Test FUNCTION 5	0 8 F Subchannel Address	Press INTERRUPT	Ends auto-answer test.

Note 1: Auto-answer/auto-call errors: DISPLAY A = 3XYY; DISPLAY B = (CCBSTMOD) (Test); Description: Feedback check. See 'Line Test Function (Panel Test) level 2 display codes in *Guide to Using the IBM 3705 Communications Controller Control Panel,* GA27-3087.

If no errors occur during the test, DISPLAY A = 0XYY, DISPLAY B = (FC) (Test).

Note 2: Modem lines bit 1 (Ring Indicator) should be on momentarily. Then bit 2 (Data Set Ready) should come on indicating that the call has been answered. If data follows, display the CCB or BCB for data information. See 'Dynamic Display of an ICW, CCB, or BCB' in *Guide to Using the IBM 3705 Communications Controller Control Panel,* GA27-3087 for switch settings to display other information.

DISPLAY A, BYTE 1 LIGHTS

Bit	Modem Lines	Autocall Line
0	Clear to Send	Abandon Call and Retry
1	Ring Indicator	Present Next Digit
2	Data Set Ready	Data Line Occupied
3	Receive Line Signal	Digit Present
4	Receive Data Bit Buffer	Call Request
5	Diagnostic Wrap Mode	Call Originating Status
6	Bit Service Request	Bit Service Request
7	Zero (not used)	Interrupt Remember

Integrated Modems
Auto-Call (ACO) Test with EP
(Line Set 9A, LIB 7)

The dial digits are manually entered to test the auto-call unit. By observing the displays, you can see the dialing sequence and the state of the data set leads.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set Up			
FUNCTION 5	0 0 3 0 X See Note 1	Press INTERRUPT	Loads the dial digit from switch E.
FUNCTION 5	0 0 3 9 9	Press INTERRUPT	Identifies the end of the dial digits in the buffer.
FUNCTION 5	0 2/4 X Subchannel See Note 2 Address	Press INTERRUPT	Performs auto dial operation.
Part 2: Observations			
FUNCTION 6	0 1 0 Subchannel Address See Note 3	Do not press INTERRUPT. Set the function and the subchannel (auto-call) address.	ICW is displayed in DISPLAY A and DISPLAY B.
Part 3: End Of Test			
FUNCTION 5	0 8 F Subchannel Address	Press INTERRUPT	Ends the ACO Test.

Note 1: X is the dial digit. Enter each dial digit in sequence and press INTERRUPT for each digit to be entered. In applicable cases enter SEP characters (X'D') in the dial sequence when needed for time-outs. If the auto-call unit is wired for End of Number (EON), enter the EON character (X'C') after the dial digits. A maximum of 15 characters and dial digits can be entered for this test.

Note 2: The test digit X'FF' may be entered anywhere in the dial digit buffer. When detected by the auto-call function, it immediately ends the auto-call operation.

Example: Dial Buffer Load

Enter 0807060504030201FF0199
Results 87654321 - end without sending 01

Enter 010301FF0206040199
Results 131 - end without sending 2641

Note 3: Refer to the line test auto-call displays or observe the modem lines in DISPLAY A, byte 1. If you are in the dial sequence, display the auto-call lines; if in data, display the modem lines. See 'Dynamic Display of an ICW, CCB, or BCB, in *Guide to Using the IBM 3705 Communications Controller Control Panel,* GA27-3087.

PANEL PROCEDURES FOR IBM INTEGRATED MODEMS–NCP OR PEP

The panel test (integrated modem tests) procedures must be selected for the control program at system generation time.

The integrated modem tests check for errors in data transfer that may be caused by a failing modem unit.

Integrated Modem Test 2 (Modem Wrap) with NCP or NCP/PEP (Line Sets 5A, 5B, 6A, 8A, 8B, 9A, 10A, 11A, 11B, 12A, 12B, LIB 7)

When operating in a PEP environment, place the control panel in NCP mode.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set Up			
FUNCTION 2	0 2 NCP Line Address or 0 2 E EP Subchannel Address	Press INTERRUPT	Initializes the test.
FUNCTION 2	0 4 1 7 C/8/0*	Press INTERRUPT	Set mode test.
FUNCTION 2	0 4 2 7 C/8/0*	Press INTERRUPT	Transmit initial (sends synchronization characters)
FUNCTION 2***	0 5 C 0 4	Press INTERRUPT	Set receive mode byte to indicate modem test in progress
FUNCTION 2	0 4 4/E** F F	Press INTERRUPT	Transmit test character and repeat (transmits the character in switches D and E).
FUNCTION 2	0 4 A F F	Press INTERRUPT	Sets the receive state.
Part 2: Observations			
FUNCTION 2	See Note 1.	Do not press INTERRUPT. Set the subchannel address.	ICW is displayed in DISPLAY A and DISPLAY B.
FUNCTION 2	0 4 C 1 8 See Note 2.	Press INTERRUPT	LTS field displayed.
Part 3: End of Test			
FUNCTION 2	0 5 0 X X	Press INTERRUPT	Ends Test 2.

*For line sets 5A, 5B, 6A, 11A, 11B and LIB 7 set switch E to: C for 2400 bps
8 for 1200 bps

For line sets 8A, 8B, 9A, 10A, 12A and 12B set switch E to 0.

**Set switch C to: E for SDLC operation
4 for non-SDLC operation

***For NCP 5

Note 1: The modem line bits 0, 2, and 3 in the ICW should be on; any one or all being off indicates a Test 2 failure.

Note 2: This setting is the displacement (X'18') into the Line Test Control Block (LTS) to the counter for non-X'FF' data characters when receiving. Observe the space counter in DISPLAY A, Bytes 0 and 1. If the counter is incrementing, Test 2 has failed. If the counter is not incrementing, Test 2 ran successfully.

DISPLAY B, BYTE 1 LIGHTS

The modem lines are displayed in DISPLAY A for EP and DISPLAY B for NCP or PEP.

Bit	Modem Lines
0	Clear to Send
1	Ring Indicator
2	Data Set Ready
3	Receive Line Signal
4	Receive Data Bit Buffer
5	Diagnostic Wrap Mode
6	Bit Service Request
7	Zero (not used)

Integrated Modem Test (Transmit All Marks) with NCP or NCP/PEP (Line Sets 5A, 5B, 6A, 8A, 8B, 9A, 10A, 11A, 11B, 12A, 12B, LIB 7)

For switched line sets, use the auto-call or auto-answer test to establish the line connection. Do not end the test. Following the line connection, start Test 3 at the *set mode* test for line set 6A and LIB 7 and at the *transmit initial* test for line sets 8B and 9A.

When using this test, place the modem located at the other end of the line in Test 4.

When operating in a PEP environment, place the control panel in NCP mode.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set Up			
FUNCTION 2	0 2 NCP Line Address or 0 2 E EP Subchannel Address	Press INTERRUPT	Initializes the test.
FUNCTION 2**	0 4 0 0 0 or	Press INTERRUPT	Set mode test.
FUNCTION 2	0 4 1 3 C/8*	Press INTERRUPT	Set mode test.
FUNCTION 2	0 4 2 X X	Press INTERRUPT	Transmit initial (sends synchronization characters).
FUNCTION 2	0 5 C 0 4	Press INTERRUPT	Set receive mode byte to indicate modem test in progress
FUNCTION 2 (omit for start-stop terminals)	0 4 4/E*** F F	Press INTERRUPT	Transmit test character and repeat (transmits the character in switches D and E).
Part 2: Observations			
FUNCTION 2	See Note 1	Do not press INTERRUPT	ICW is displayed in DISPLAY A and DISPLAY B.
Part 3: End of Test			
FUNCTION 2	0 5 0 0 0	Press INTERRUPT	Ends Test 3.

*Set switch E to: C for 2400 bps. These settings do not set the diagnostic wrap bit.
8 for 1200 bps.

**Set switches B and C to 40 for line sets 8A or 12A. Set switches B and C to 41 for line sets 5A, 5B, 6A, 11A, 11B, and LIB 7. Do not set switches B and C with line sets 8B, 9A, 10A, and 12B.

***Set switch C to: E for SDLC operation
4 for non-SDLC operation

Note 1: Modem line bits 0 and 2 should be on; if either bit is off, a local modem failure is indicated. If both bits are on, go to the next step to end the test.

PANEL PROCEDURES FOR IBM INTEGRATED MODEMS—NCP OR PEP, PART 2

**Integrated Modem Test 4 (Receive All Marks)
with NCP or NCP/PEP
(Line Sets 5A, 5B, 6A, 8A, 8B, 9A, 10A,
11A, 11B, 12A, 12B, LIB 7)**

For switched line sets, use the auto-call or auto-answer test to establish the line connection. Do not end the test. Start Test 4 at the *set mode* test for line set 6A and LIB 7 and at the *transmit initial* test for line sets 8B and 9A.

When using this test, place the modem located at the other end of the line in Test 3.

When operating in a PEP environment, place the control panel in NCP mode.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
PART 1: SET UP			
FUNCTION 2	0 2 NCP Line Address***	Press INTERRUPT	Initializes the test.
	or		
	0 2 E EP Subchannel Address		
FUNCTION 2**	0 4 0 0 0	Press INTERRUPT	Set mode test.
	or		
FUNCTION 2	0 4 1 3 C/8*	Press INTERRUPT	Set mode test.
FUNCTION 2	0 4 2 X X	Press INTERRUPT	Transmit initial (sends synchronization characters).
FUNCTION 2****	0 5 C 0 4	Press INTERRUPT	Set receive mode byte to indicate modem test in progress.
FUNCTION 2	0 4 5 F F	Press INTERRUPT	Transmits test character and turns to receive.
PART 2: OBSERVATIONS			
FUNCTION 2	See Note 1	Do not press INTERRUPT	ICW is displayed in DISPLAY A and DISPLAY B.
FUNCTION 2	0 4 C 1 8 See Note 2.	Press INTERRUPT	LTS field displayed.
PART 3: END OF TEST			
FUNCTION 2	0 5 0 0 0	Press INTERRUPT	Ends Test 4.

*Set switch E to: C for 2400 bps. These settings do not set the diagnostic wrap bit.
8 for 1200 bps.

**Set switches B and C to 40 for line sets 8A or 12A. Set switches B and C to 41 for line sets 5A, 5B, 6A, 11A, 11B and LIB 7. Do not set switches B and C for line sets 8B, 9A, 10A, or 12B.

***For duplex line sets 10A, 11A and 11B set switches C, D, and E to the NCP transmit line address.

****For NCP 5

Note 1: Modem linet bits 2 and 3 should be on; if either or both are off, this indicates a Test 4 failure. If the failure indication is modem line, bit 2, end Test 4 and restart at Test 2. If you return to this point, you have a local modem problem. If the failure is modem line, bit 3, recheck both local and remote modem cables and run Test 2 for integrated modems; if it runs successfully, you probably have a common carrier problem and should end Test 4. If both bits are on, go on to the next step.

Note 2: This setting is the displacement (X'18') into the Line Test Control Block to the counter for non-X'FF' data characters when receiving. Observe the space counter in DISPLAY A, Bytes 0 and 1. If the counter is incrementing, Test 4 has failed and equalization is required for the remote modem (leased lines). If the counter is not incrementing, Test 4 ran successfully.

**Integrated Modems
Auto-Answer Test with
NCP or NCP/PEP
(Line Sets 6A, 8B, 9A, 12B, LIB 7)**

When operating in a PEP environment, place the control panel in NCP mode.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set up			
FUNCTION 2	0 2 NCP Line Address	Press INTERRUPT	Initializes the test.
	or		
	0 2 E EP Subchannel Address		
FUNCTION 2	0 4 6 0 0	Press INTERRUPT	Auto-answer test.
Part 2: Observations	See Note 1	Do not press INTERRUPT	ICW is displayed in DISPLAY A and DISPLAY B.
FUNCTION 2	0 4 C 0 8 See Note 2	Press INTERRUPT	LTS field displayed.
Part 3: End of Test			
FUNCTION 2	0 5 0 X X	Press INTERRUPT	Ends the Auto-answer Test.

Note 1: Modem line bit 1 (Ring Indicator) should be on momentarily. Then bit 2 (Data Set Ready) should come on indicating that the call has been answered.

Note 2: This setting is the displacement (X'08') into the Line Test Control Block to the buffer for receive data characters. If the line is attached to a type 3 scanner, this setting points to the buffer address of the received data.

DISPLAY B, BYTE 1 LIGHTS

The modem lines and auto call lines are displayed in DISPLAY A for EP and DISPLAY B for NCP or PEP.

Bit	Modem Lines	Autocall Line
0	Clear to Send	Abandon Call and Retry
1	Ring Indicator	Present Next Digit
2	Data Set Ready	Data Line Occupied
3	Receive Line Signal	Digit Present
4	Receive Data Bit Buffer	Call Request
5	Diagnostic Wrap Mode	Call Originating Status
6	Bit Service Request	Bit Service Request
7	Zero (not used)	Interrupt Remember

**Integrated Modems
Auto Call (ACO) Test with
NCP or NCP/PEP
(Line Set 9A, LIB 7)**

The dial digits are manually entered to test the ACO unit. By observing the displays, you can see the dialing sequence and the state of the data set leads.

When operating in a PEP environment, place the control panel in NCP mode.

DISPLAY/FUNCTION SELECT Switch	ADDRESS/DATA Switches A B C D E		Descriptions
Part 1: Set Up			
FUNCTION 2	0 2 NCP Line Address	Press INTERRUPT	Initializes the test.
	or		
	0 2 E EP Subchannel Address		
FUNCTION 2	0 4 7 0 X See Note 1	Press INTERRUPT	Loads the dial digit from switch E.
FUNCTION 2	0 4 7 0 F	Press INTERRUPT	Identifies the end of the dial digits in the buffer.
FUNCTION 2	0 4 8 0 Y See Note 2	Press INTERRUPT	Transmits the dial digits previously loaded to the auto-call unit.
Part 2: Observations			
FUNCTION 2	See Note 3	Do not press INTERRUPT. Set the function and the subchannel address.	ICW is displayed in DISPLAY A and DISPLAY B.
Part 3: End Of Test			
FUNCTION 2	0 5 0 X X	Press INTERRUPT	Ends the ACO test.

Note 1: X is the dial digit. Enter each dial digit in sequence and press INTERRUPT for each digit to be entered. In applicable cases enter SEP (X'D') characters in the dial sequence when needed for time-outs. If the auto-call unit is wired for End of Number (EON), enter the EON character (X'C') after the dial digits. A maximum of 15 characters and dial digits can be entered for this test.

Note 2: Switch E determines how many dial digits and characters are sent to the ACO. The value of Y has the following meanings:
0-Send all digits and characters entered.
1-Send the first dial digit entered then stop.
2-Send the first two entries (two dial digits or one dial digit and the SEP character), then stop.
↓
etc:
↓
9-Send the first nine entries then stop.
Example: Enter 8 (SEP) 7654321 (EON).
Set switch E to 9
Result: Send 8 (SEP) 7654321 then stop without sending EON.
Switch E values other than 0 result in Abandon Call and Retry.
You can observe DISPLAY A and DISPLAY B to see the dialing sequence and to determine how far the test proceeds if it does not run to completion.

Note 3: Observe the auto call lines in DISPLAY B, Byte 1. The LCD field in DISPLAY B, Byte 0 displays X'3' (auto call) when the auto call lines is displayed in DISPLAY B, Byte 1.

MAINTENANCE PROCEDURES

FOR LIB TYPES 5, 6, 7, AND 11

Modem Diagnostic

This test checks the basic transmit and receive circuits of the integrated modem. The mainstream of the test is brief, with branches to the following sub-tests as necessary:

A. Signal indicator off (010-020)
B. Meter reads high (030-047)
C. Not receiving marks (057-063)
D. Transmit test (070-120)
E. Carrier detect test (130-150)
F. Receive test (160-193)
G. Receive equalizer test (200-232)
H. Automatic equalizer test (240-286)

Note: Use the following rules when scoping in the procedures that follow:

1. Sync internal is always "minus" on Channel 1.
2. Channel 1 is displayed above Channel 2 in all cases where both are used. When displaying both channels, use chopped mode.
3. A X10 probe is used for all signals.
4. When comparing waveforms, minor differences in amplitude are not noncomparisons. A radical amplitude difference, unless specified, indicates a failure to compare.

Note 1: Unless instructions specify otherwise, always remove grounding jumpers before performing the next step in any procedure. The pins used for grounding are D08, J08, P08, or U08 (except in card row 1).

Note 2: When instructions state "replace" a card, put in a new one. When "return" the card is instructed, put the same one back in the socket.

Note 3: The flowchart blocks of the diagnostics are sequentially numbered. Off-page connectors indicate the "go to" block number.

Note 4: Many of the scope waveforms and other measurements in the following procedures are made with a special setup. If you do not follow the procedures, but wish to make the observation or measurement, be sure to check in preceding blocks for the possibility of a special setup.

When a card services two *addresses,* the pins are identified as XXX/YYY where XXX refers to the lowest address pin and YYY refers to the highest address pin. When a card services only one *address* and two pins are given as XXX/YYY, the XXX pin applies.

Refer to the card location chart for the card location for your LIB type.

CARD LOCATION CHART

	Function	Card Code	LIB 5 Adr position 0/2	LIB 6 Adr position 0/2	LIB 7 Adr position 0/1	LIB 11 Modem 0/1
LINE SET	Driver	7573	F2	F2	S4	——
	Terminator	7574	E4	E4	T4	——
	Line Interface	7575	D2	D2	D2	D2/G2
	Isolation	7578	C2	C2	C2	C2
	Bit Clock Control	7583	B2	B2	B2	B2
	Board Entry from Top Card Conn.	——	F4-F5	F4-F5	U4-U5	—
MODEM	Preamp	N830	T2/T4	U2/U4	L2	T2/T4
	Limiter	N831	K2/K4	K2/K4	N4	K2/K4
	Transmitter	N832	Q2/Q4	P2/P4	N2	Q2/Q4
	Post Processor (PP)	N833	N2/N4	N2/N4	R4	N2/N4
	Modem Interface	**	J2/J4	J2/J4	M4	H2/H4
	Modem Digital Logic (FET)	N835	L2/M2	L2/M2	P2	L2/M2
	C1 Receive Equalizer (external)	***	*S2/S4	——	—	*S2/S4
	AEQ Digital	N837	——	S2/S4	R2	
	AEQ Analog	N836	——	R2/T2	Q2	
	Voltage Converter	N840	R2/R4	Q2/Q4	M2	R2/R4
	I/O Gate Cable Connector	——	V2/V4	V2/V4	V4	V2/V4
	External Receive Equalizer Cable	——	V5	——	—	V5
AUTOCALL AUTO-ANS	ACO Interface	6834	——	——	E2	——
	ACO Threshold	M859	——	——	J2	——
	ACO-1	M860	——	——	H2	——
	ACO-2	M861	——	——	G2	——
	AA Common	M862	——	G2/G4	J4	——
	AA Interface W/O ACO	N829	——	H2/H4	—	——

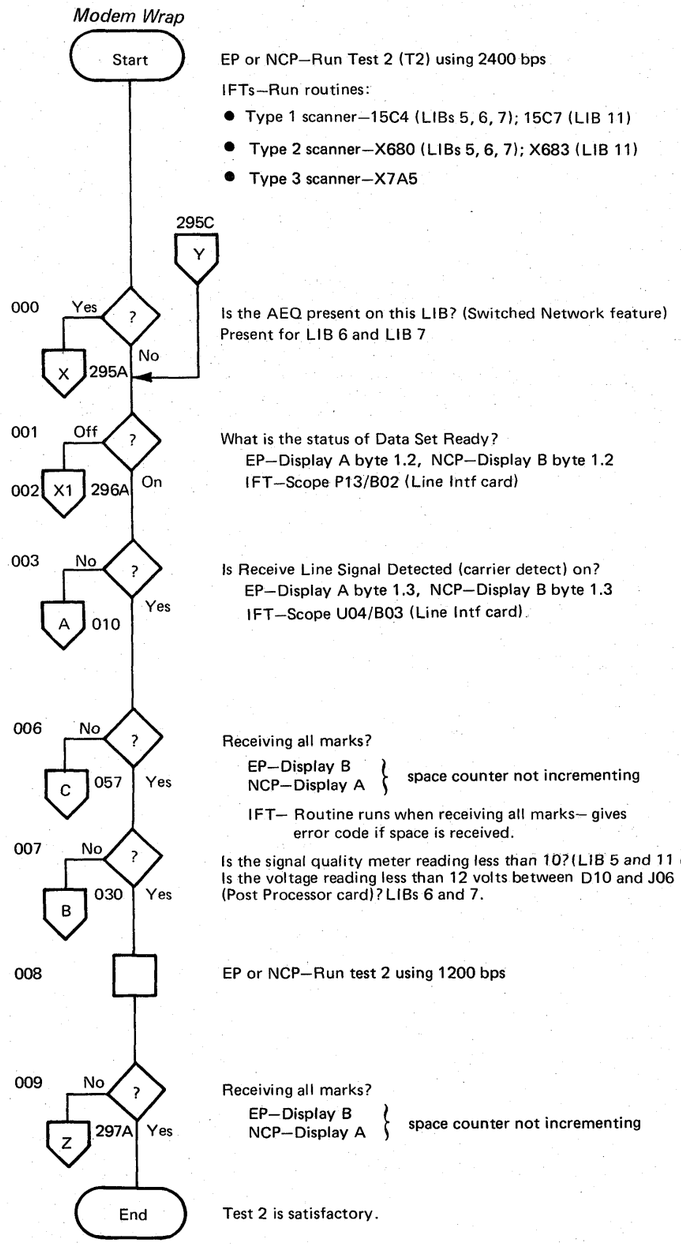
* External receive equalizers are present for line sets 5A and 11A (point-to-point). For line sets 5B and 11B (multipoint control) no receive equalizers are present because the tributary does the equalizing, however the signal quality meter is on the 3705.
**Card code N834 for LIBs 5, 6, 7 and card code Z322 for LIB 11.
***Card code N838 for line set 5A and card code P771 for line set 11A.

Summary of IFT Routines and Panel Procedures to Simulate the Modem Tests

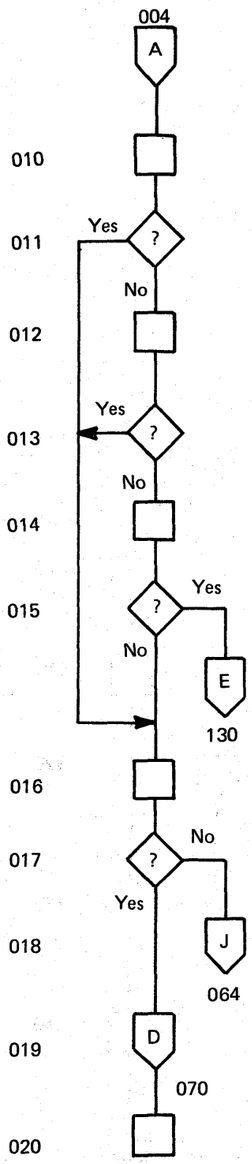
Modem Test	IFT Routines			EP or NCP Panel Procedures
	Type 1 Scanner	Type 2 Scanner	Type 3 Scanner	
Test 2	15C4*	X680**	X7A5	Test 2
Test 3	15C8	X6CE	X7A5	Test 3
Test 4	15CA	X6CE	X7A5	Test 4
Auto-Ans.	15CA	X6CE	X7A5	Auto-Ans.
Auto Call	15C8	X6CE	X7A5	ACO Test

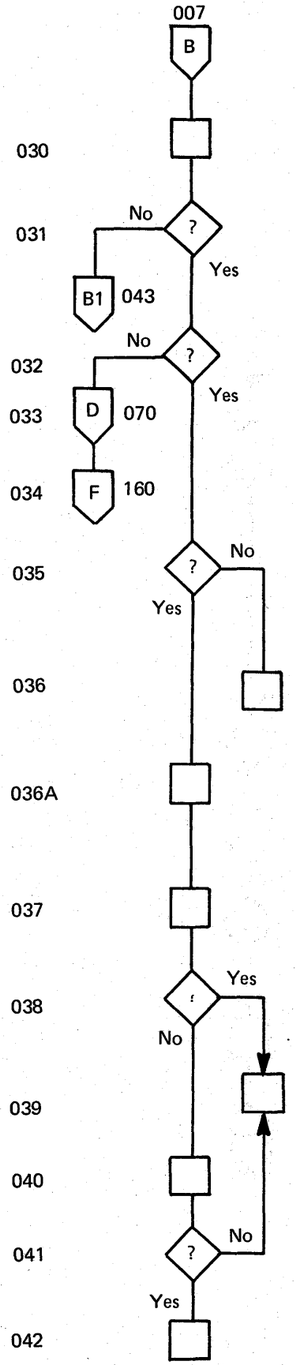
*Line sets 11A and 11B use routine 15C7.
**Line sets 11A and 11B use routine X683.

Note: Before removing any modem cards, check the LIB card position page for that LIB to determine if the card controls two modems.

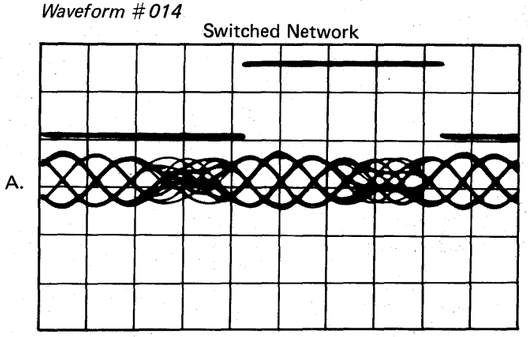


MAINTENANCE PROCEDURES, PART 2

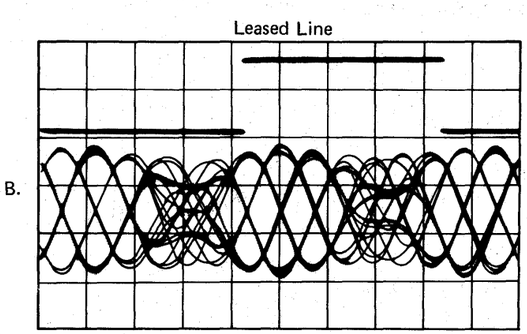




Waveform #014

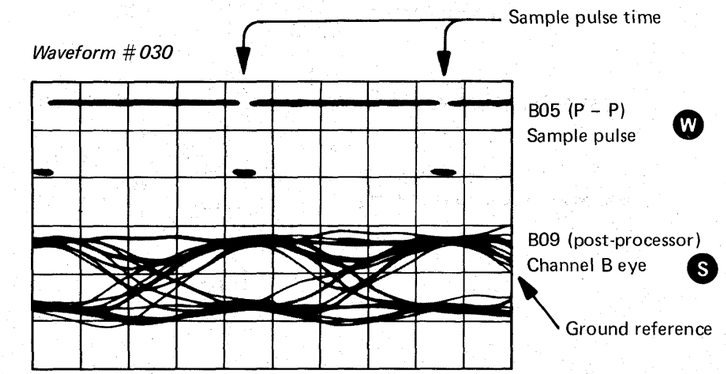


Sync -internal, 0.2ms/div.
Channel 1, 0.5V/div.
Channel 2, 50mV/div.



Sync -internal, 0.2ms/div.
Channel 1, 0.5V/div.
Channel 2, 100mV/div.

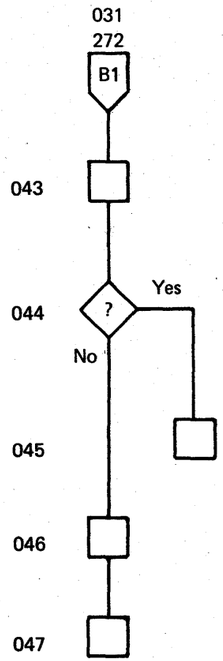
Waveform #030



Sync -internal, 0.2ms/div.
Channel 1, 0.5V/div.
Channel 2, 2V/div.

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

MAINTENANCE PROCEDURES, PART 3



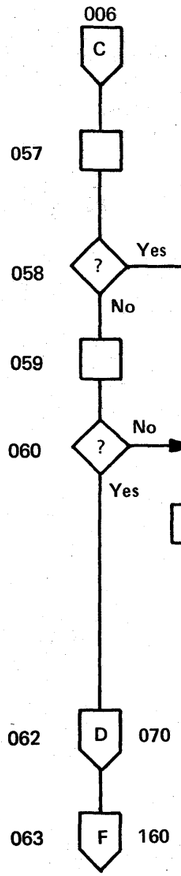
Remove post-processor and scope B05 (post-processor position). See Waveform #30.

Is the waveform at B05 the same except amplitude >+3V?

Replace post-processor card, recalibrate the signal quality meter (see VJ005 or VW004), and restart Test 2.

Plug the post-processor card back in the socket.

Replace the FET card and restart Test 2.



Not receiving all marks

Scope B04, ('receive data' on FET card).

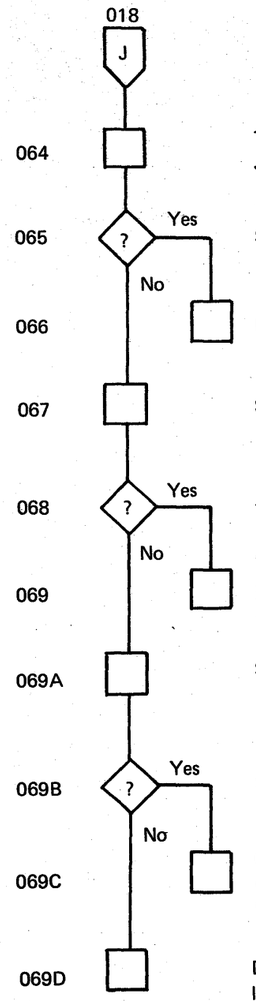
Steady "down" (space) level?

Scope G08 ('scrambler input' on the FET card).

Steady "up " level >+4.2V (mark)?

Marks come from the transmit data trigger in the line interface card. Scope at U11/D10 to ensure the trigger is at an MST up level (mark). Scope the signal through the modem to find the problem by referring to logic. Be sure you have followed all the steps to here and are executing Test 2.

Execute the transmit test. If no trouble is found, execute the receive test.



The wrap relay is not picked-scope JO9 (limiter card).

Steady "down" level <+0.3V?

Replace limiter card

Scope J13 (modem intf card)

+EIA level >+3V?

Replace modem interface card.

Scope B09 (driver card)

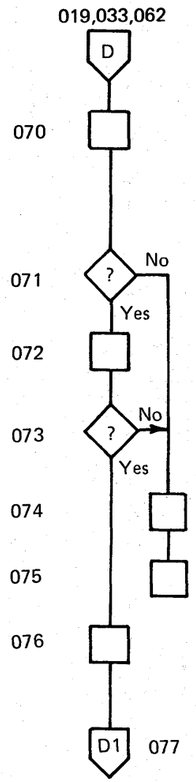
Steady - MST voltage?

Check cable from top card connector (not on LIB 11).
If all right, replace driver card.

Diagnostic Mode should be set in the line interface card by a set Mode operation - check.

See C-101 for LIB 5 card positions.
See C-102 for LIB 6 card positions.
See C-103 for LIB 7 card positions.
See C-107 for LIB 11 card positions.

MAINTENANCE PROCEDURES, PART 4



Transmit test

End test 2 (abort). Tie '+EIA data sig rate sel' to +8.5V for 2400 bps operation (See V*090 to V*095). Remove transmitter card and scope J12 and G10 (ramp clocks A and B on the transmitter card; see Waveform #070).

Are the waveforms correct?

Scope B09 and D02 (Channel A and B transmit on the transmitter card; see Waveform #072).

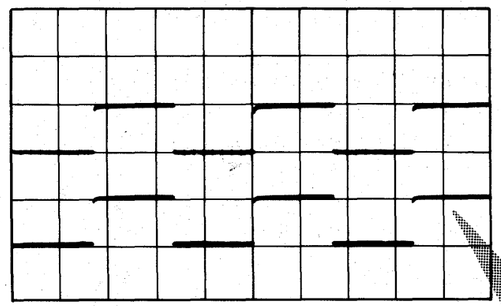
Are the waveforms correct?

Return transmitter card to its socket.

Remove jumper for 2400 bps operation. Replace FET card and restart Test 2.

Return transmitter card to its socket and scope D11 (ramp test point on the transmitter card; see Waveform #076).

Waveform # 070



J12 (transmit card) Ramp clock A (B)

G10 (transmit card) Ramp clock B (C)

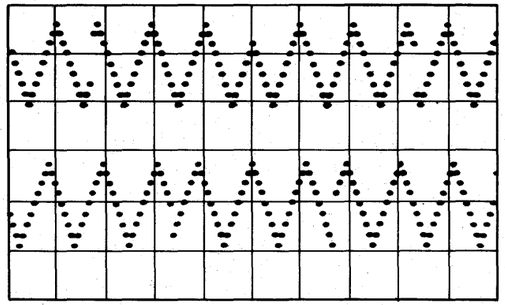
Sync - internal, 0.5ms/div.
Channel 1, 10V/div.
Channel 2, 10V/div.

If 'ramp clock B' is 180 ° out-of-phase you are running at 1200 bps — should be running at 2400 bps.

Waveform # 072

Note: **Observe the oscilloscope carefully. Depending upon how sync actually triggers the sweep, waveform A, B, C, or D may be displayed. A correct waveform always has nine dots vertically, and phase changes always appear as a compressed waveform with four dots omitted. At 2400, three full cycles appear between phase changes; at 1200, six cycles appear between changes. Phase changes are staggered.**

A.

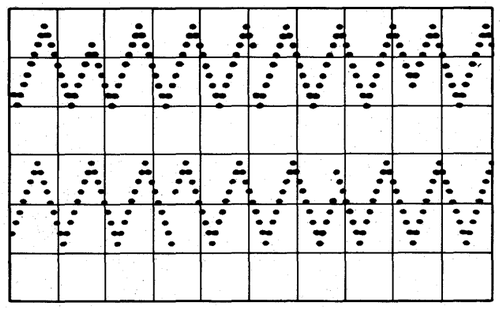


B09 (FET) Chan B transmit (F)

D02 (FET) Chan A transmit (E)

Sync - S04 (FET), 0.5ms/div.
Channel 1, 0.5V/div.
Channel 2, 0.5V/div.

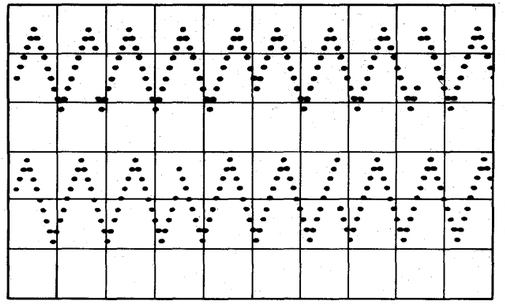
B.



B09 (FET) Chan B transmit (F)

D02 (FET) Chan A transmit (E)

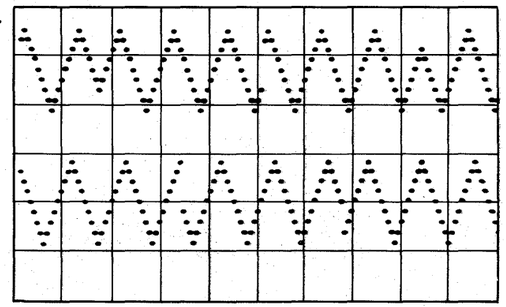
C.



B09 (FET) Chan B transmit (F)

D02 (FET) Chan A transmit (E)

D.

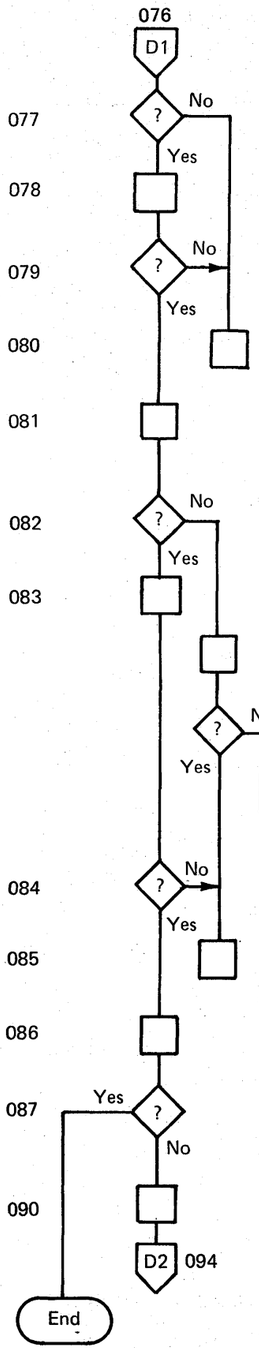


B09 (FET) Chan B transmit (F)

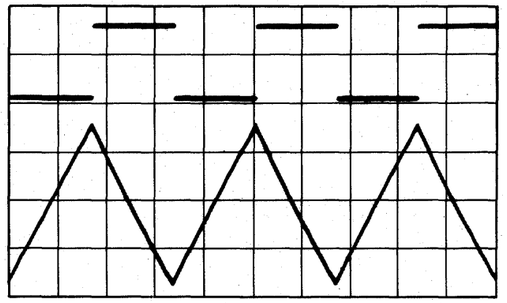
D02 (FET) Chan A transmit (E)

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

MAINTENANCE PROCEDURES, PART 5



Waveform # 076

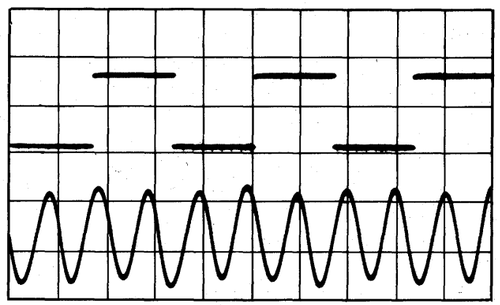


S04 (FET) Ramp clock A (B)

D11 (TSM) Ramp test point (D)

Sync - internal, 0.5ms/div.
Channel 1, 0.5V/div.
Channel 2, 0.1V/div.

Waveform # 078

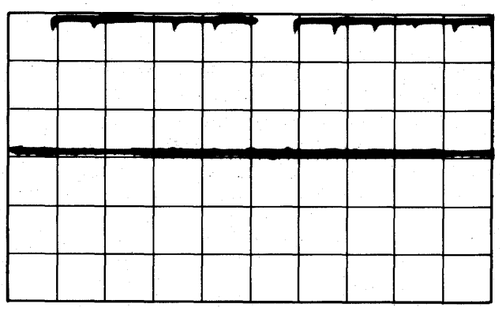


S04 (FET) Ramp clock A (B)

D05 (TSM) Analog transmit signal (G)

Sync - internal, 0.5ms/div.
Channel 1, 0.5V/div.
Channel 2, 1V/div.

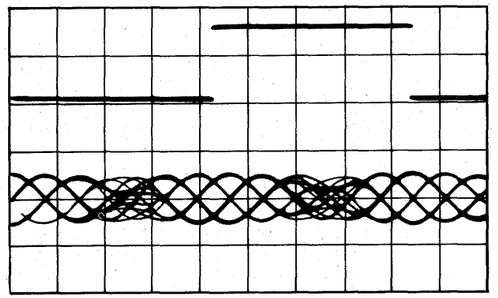
Waveform # 081



G09 (FET) Scramble output (A)

Sync - internal, 0.5ms/div.
Channel 1, 2V/div.

Waveform # 088

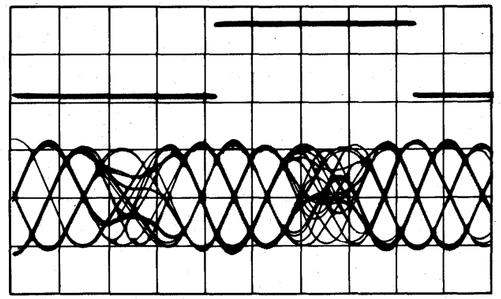


S04 (FET) Ramp clock A (B)

G09 (TSM) Line driver input (H)

Sync - internal, 0.2ms/div.
Channel 1, 0.5V/div.
Channel 2, 2Vac/div.

Waveform # 090



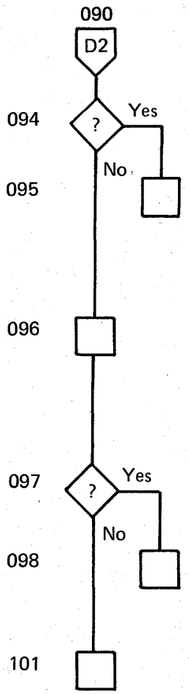
S04 (FET) Ramp clock A (B)

B02 (Preamp) Preamp wrap Signal input (J)

Sync - internal, 0.2ms/div.
Channel 1, 0.5V/div.
Channel 2, 5V/div.

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

MAINTENANCE PROCEDURES, PART 6



094 Is the waveform at B02 (preamp card) correct?

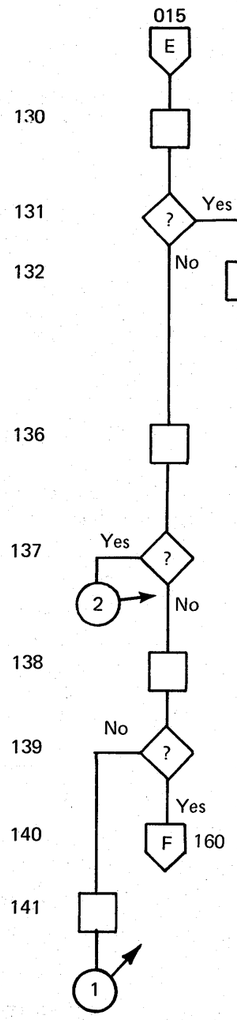
095 Replace preamp card and restart Test 2.

096 Return the preamp card to its socket, remove transmitter card, and scope G02 (-enable line driver on the transmitter card).

097 Steady "down" level < +0.3V?

098 Replace transmitter card and restart Test 2.

101 Replace the FET card and restart Test 2.



Carrier detect test

130 Scope D05 ('+carrier detect' on the FET card).

131 Steady "up" level > +3V?

132 Receive line signal detected (carrier detected) is gated to the scanner by 'control in B' in the line interface card. Refer to V*003 to trace the signal to the line interface card.

136 Scope J11 ('- serial data' on the FET card).

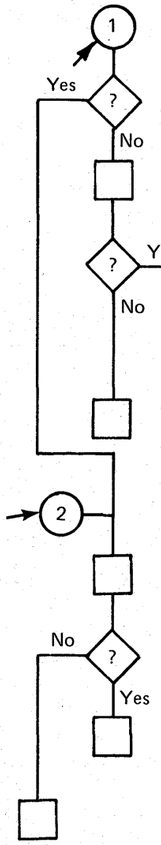
137 Is J11 switching from "down" levels < +0.3V to "up" levels > +3.5V?

138 Scope D07 ('+ clamp - start resync' on the FET card).

139 Steady "down" level (- start resync) < +0.3V?

140 Execute the receive test.

141 Scope G03 (-signal threshold on the FET card).



142 Is G03 switching from ground to > +3.5V?

143 Scope D09 ('-2 wire' on the limiter card).

144 Steady "up" level (+4 wire) > +3V?

145 Replace the limiter card and restart Test 2.

146 Internal four-wire operation is not being forced by Test 2. Set mode sets the diagnostic mode latch in the line interface card for a wrap operation. Refer to V*003 to ensure S09/D02 is at a steady MST downlevel and to trace the wrap signal.

147 Scope U13 ('+new sync' on the FET card).

148 Steady "up" level > +4.2V?

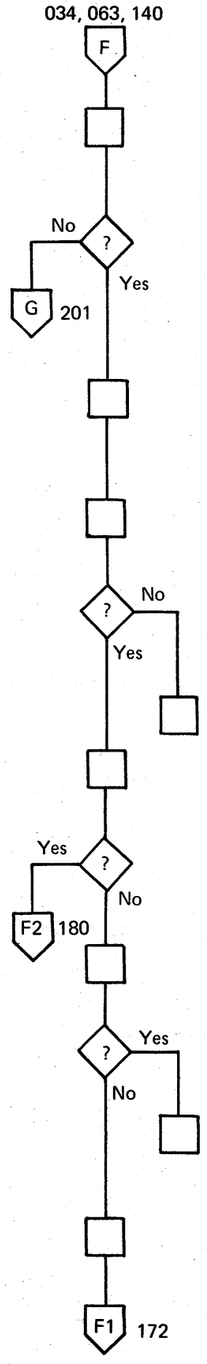
149 Replace the FET card and restart Test 2.

150 New sync is not being clamped off in Test 2. New sync comes from its latch in the line interface card. Refer to V*003 to ensure that new sync is off in the line interface card and to trace the signal to the FET card.

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

LIB

MAINTENANCE PROCEDURES, PART 7



Receive test

Scope D13 (preamp output) and D05 (limiter input). If this is LIB 6 or 7, jumper G05 (AEQ analog) to ground. (See Waveform # 160.)

Do the waveforms compare? Remove ground jumper.

Note: Line Set 5B and 11B jumpers the preamp output to the limiter input.

Execute the receive equalizer test.

Start Test 2 and jumper G02 ('-enable line driver' on the transmitter card) to ground. Also, jumper G07 ('RTS' on the driver card) to ground. Leave the jumpers on.

Scope D05 (limiter input) and B02 (limiter output; see Waveform # 163).

Are the waveforms correct?
(Ignore the phasing of limiter input; however, the up and down levels of limiter output should have about equal duration and should be in phase with limiter input.)

Replace limiter card, remove the jumpers, and restart Test 2.

Scope D05 and B02 ('Chan A and B filters' on the post-processor card; see Waveform # 166).

Are the waveforms correct?

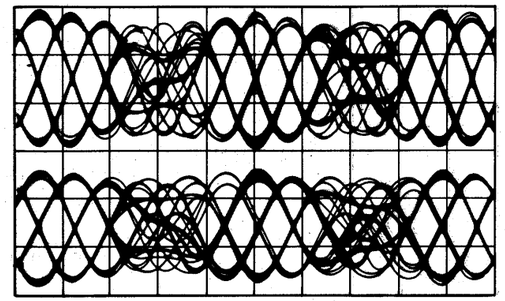
Remove the post-processor card.

Are the waveforms now correct except amplitude > +6V? (see Waveform # 166)

Replace post-processor card, remove the jumpers, recalibrate the signal quality meter (see VJ005 or VW004), and restart Test 2.

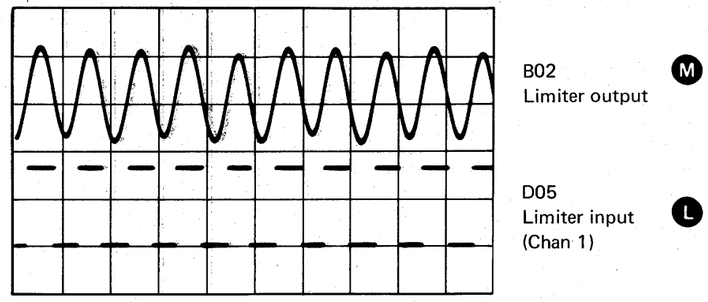
Return post-processor card to its socket.

Waveform # 160



Sync - S04 (FET), 0.2ms/div.
Channel 1, 100mV/div. for LIBs 5 and 11 (50mV and 2/5 amplitude for LIB 6 or 7)
Channel 2, 100mV/div. (for line sets 5A or 11A or LIBs 6 or 7)

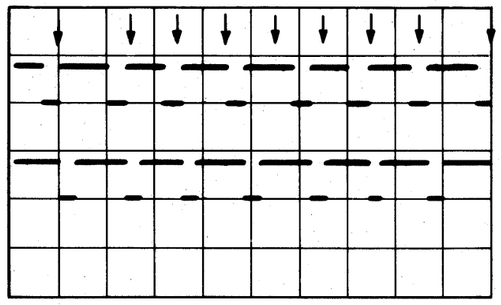
Waveform # 163



Sync - S04(FET), 0.5ms/div.
Channel 1, 100mV/div. for LIBs 5 and 11 (50mV and 2/5 amplitude for LIB 6 or 7)
Channel 2, 5V/div.

Waveform # 166

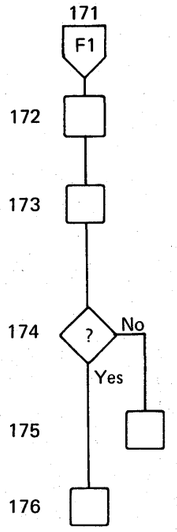
Note: Both signals are more up than down; transitions marked with arrows line up vertically.



Sync S04(FET), 0.2ms/div.
Channel 1, 1V/div.
Channel 2, 1V/div.
Scope in Alternate Mode

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

MAINTENANCE PROCEDURES, PART 8



172 Remove the jumpers and start T2.

173 Scope B02 (limiter output) and compare with D02, B05, and D04 (limiter output delayed through shift register; see Waveform # 173).

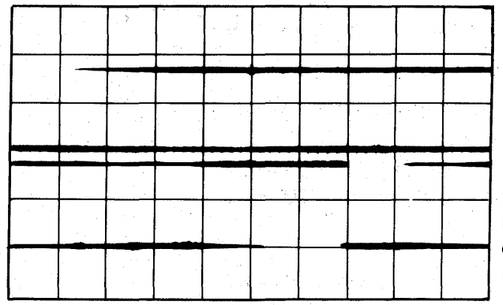
174 Are the waveforms correct and correctly delayed?

175 Replace limiter card and restart Test 2.

176 Replace the FET card and restart Test 2.

Waveform # 173

A.

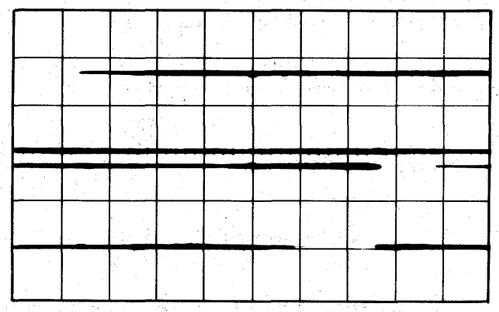


B02 (M) Limiter output

D02 (N) Limiter output delayed 450° (2400) (shift reg. Bit 80)

Sync -internal, 0.1ms/div.
Channel 1, 5V/div.
Channel 2, 5V/div.

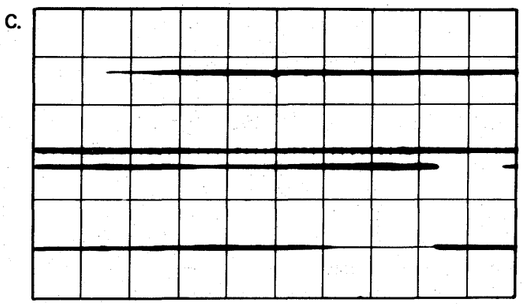
B



B02 (M) Limiter output

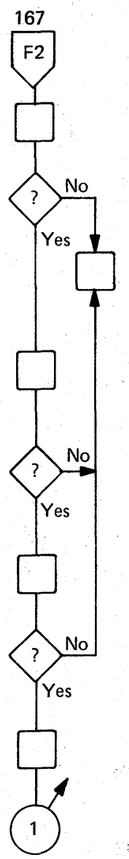
D04 (N) Limiter output delayed 990° (1200) (shift reg. Bit 88)

C.



B02 (M) Limiter output

B05 (N) Limiter output delayed 540° (2400) or 1080° (1200) (shift reg. Bit 96)



180 Scope D04 and D06 ('Channels A and B data' on the post-processor card).

181 Steady "up" level (about +8V) on both?

182 Replace post-processor card, remove the jumpers, recalibrate the signal quality meter (see VJ005 or VW004) and restart Test 2.

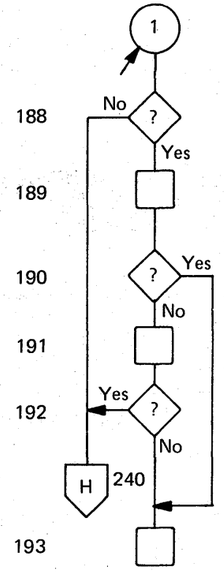
183 Remove the jumpers and scope D04 ('chan A receive data') and G02 (chan A Eye TP) on the post-processor card (see Waveform # 183).

184 Are the waveforms correct?

185 Scope D06 (Chan B rcv data) and B09 (Chan B eye) (See Waveform # 183.)

186 Are the waveforms similar to D04 and G02 (above)?

187 Scope M09 ('-resync AEL' on FET card).



188 Steady "down" level < +0.3V?

189 Scope M13 ('+clamp data AEL' on FET card).

190 Steady "down" level < +0.3V?

191 Scope B07 ('+clamp data' on FET card).

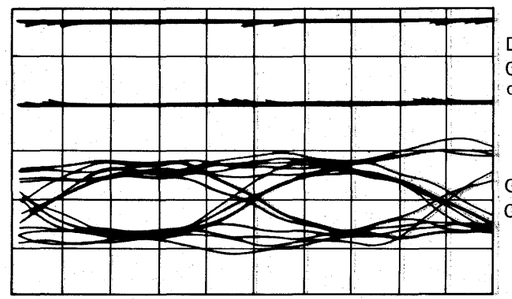
192 Steady "down" level < +0.3V?

240 Execute the AEQ test.

193 Replace FET card and restart Test 2.

Waveform # 183

Note: Maladjust scope probe compensation to observe the blips on the receive data trace. Recompensate the probe before proceeding.



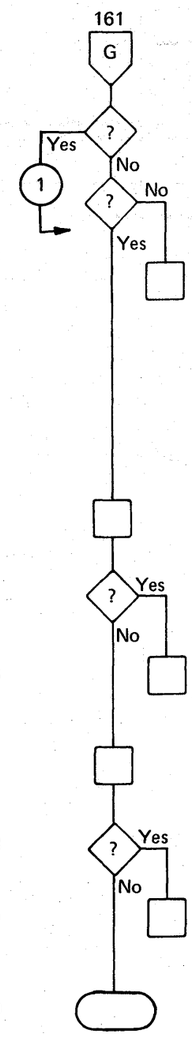
D04 (P – P) (V) Chan A receive data

G02 (P – P) (R) Chan A eye

Sync - S04 (FET), 0.2ms/div.
Channel I, 5V/div.
Channel 2, 2V/div.

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

MAINTENANCE PROCEDURES, PART 9



201 Is the AEQ present (LIBs 6 – 7)?

202 Is the C1 receive equalizer present (Line Sets 5A or 11A)?

203 At this point, your decisions indicate that the modem has no receive equalizer (Line Sets 5B or 11B), yet the preamp output is good and the limiter input is bad. This is the same line, so unless the backpanel wire-wrapped jumper from D13 to J09 (empty C1 rcv equalizer position) is bad, you have made a mistake and should start over.

204 Scope J02, G03, G02, B07, and D04 (C1 equalizer control lines).

205 All steady "down" levels < +0.3V?

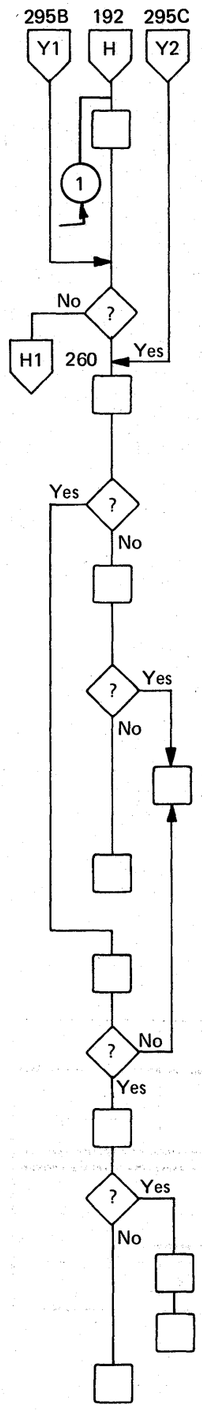
206 Replace C1 equalizer card and restart Test 2.

207 Scope J02 ('+equalizers out' on the post-processor card).

208 Steady "up" level > +3.5V?

209 **Replace post-processor card, recalibrate the signal quality meter (see VJ005 or VW004), and restart Test 2.**

210 The '+equalizers out' line is not being forced on Test 2. Diagnostic mode (wrap) forces '+ equal out' on VJ302. Scope to locate the trouble.



AEQ Test (LIB 6–7)

240 Plug the indicator card on the back panel in the indicator location (see C- 102 for LIB 6 or C-103 for LIB 7). Observe the indicators while starting Test 2 from a reset state. AEQ equalizes on the first start character after carrier is detected. Jumpering G07 (driver card) to ground simulates starting and resetting Test 2 when Test 2 is running.

241 Did any of the lights blink?

242 Jumper G05 ('– TP' on the AEQ analog card) and G07 ('+AEL ready' on the AEQ digital card) to ground and scope B02 and B12 (AEQ analog card). (Sync J10-AEQ digital, 0.2ms/div.) Leave the jumpers on.

243 Do the waveforms compare (similar to Waveform # 160)?

244 Remove the AEQ analog card and scope D02, B02, D04, J12, G12, and J13 (AEQ digital card).

245 All at steady levels more negative than -1.75V?

246 Replace the AEQ analog card, remove jumpers, and restart Test 2.

247 Return the AEQ analog card to its socket, replace the AEQ digital card, remove jumpers, and restart Test 2.

248 Scope U05 ('rectified eye' on the AEQ analog card, see Waveform # 248).

249 Is the waveform correct?

250 Scope J06 ('-2400' on the AEQ digital card).

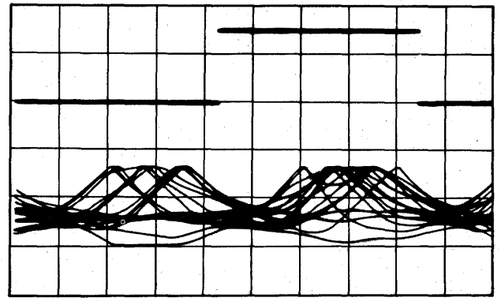
251 Steady "down" level < +0.3V?

252 Replace the AEQ digital card and restart Test 2. Of you return here, replace the AEQ analog card, instead, and restart Test 2.

253

254 Speed control is incorrect. Correct speed control then restart Test 2.

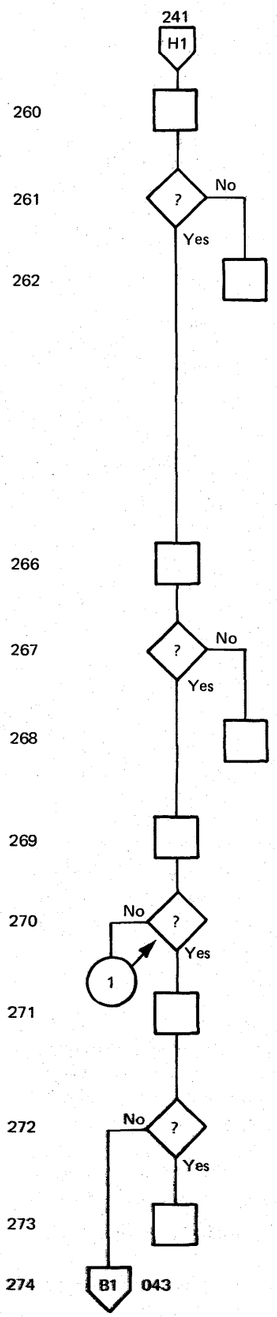
Waveform # 248

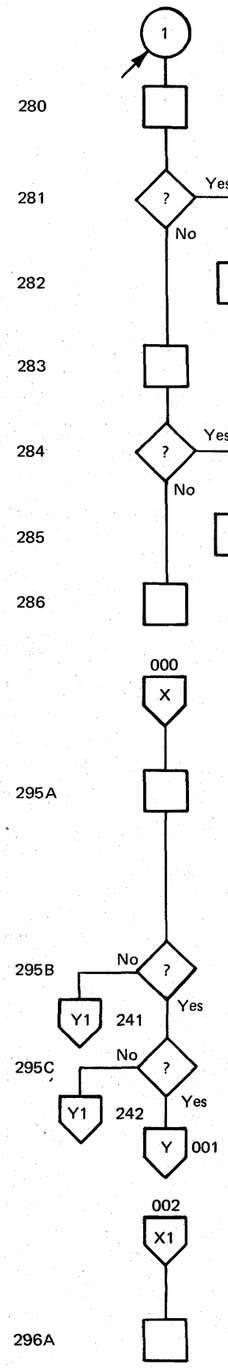


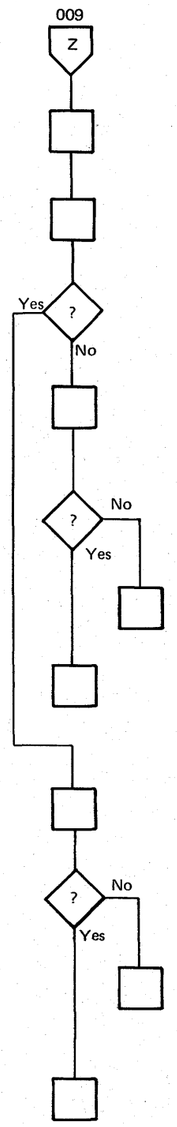
Sync -internal, 0.2ms/div.
Channel 1, 0.5V/div.
Channel 2, 5V/div.

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

MAINTENANCE PROCEDURES, PART 10







See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

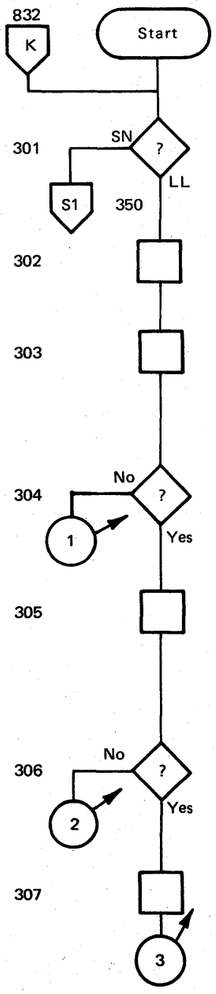
LIB

MAINTENANCE PROCEDURES, PART 11

Line-Side Diagnostic

This test checks the basic circuits of the modem between the communications line and the circuits exercised by the Test 1 Diagnostic.

This test uses a remote modem. The T3 and T4 capabilities are used on both modems, in addition to continuity checking in some cases. Test equipment required, in addition to an oscilloscope, include the CE meter and the dB meter.



Is the problem on leased line or switched network?

Have the remote modem(s) set to T4; start Test 3 at the local modem end.

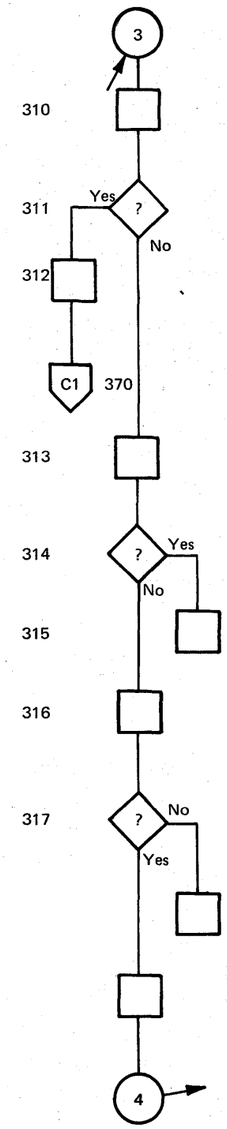
Set the dB meter to BRIDGING and measure the local modem transmit level at the 283-B plug. Either remove the plug cover and clip to the screwheads or partially remove the plug from the receptacle and clip to the prongs.

Is the transmit level correct? (Refer to the benchmark chart—LIBs 5 and 11 only.)

Scope the transmit signal at the 283-B plug. (Refer to the line-scoping procedure under "Scoping Hints and Precautions" on C-400.)

Is the waveform normal (similar to the one on page C-400, but "clean" and undistorted)?

Have a remote modem set to T3 and run Test 4 at the local modem.



Set the dB meter to BRIDGING and measure the receive level at the 283-B plug.

Is the receive level correct?
(Refer to the benchmark chart—LIBs 5 and 11 only.)

Scope the receive line signal at the 283-B plug (see the line-scoping procedure under "Scoping Hints and Precautions") and compare it with preamp output D13 (see Waveform #014).

Unplug the 283-B plug and plug the dB meter into the receptacle. Set the dB meter to 600-ohm termination and measure the receive level.

Is the receive level still wrong? (See block 311.)

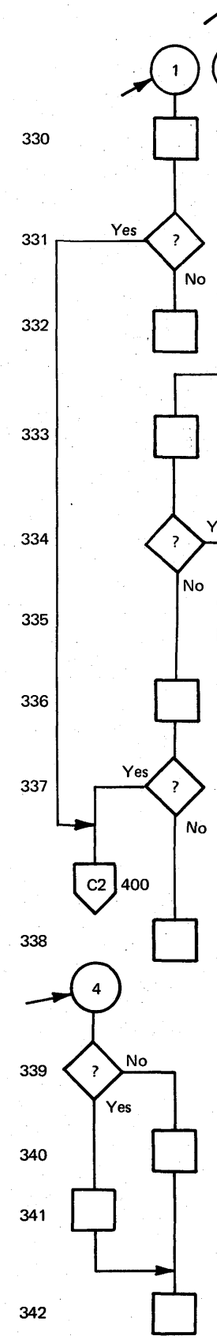
The problem is not in this modem.

Scope B08 ('-wrap relay' on the preamp card).

Steady level ⟩ +10.5V?

Use V*003 for points to scope in determining why the wrap relay doesn't pick.

Abort the test. Using the Line Connection Continuity drawing C-410B, check the continuity of the line connections.



Unplug the 283-B plug from the line and plug it into the dB meter. Set the dB meter to 600-ohm termination.

Is the transmit level still wrong?
(See block 304.)

The problem is not in this modem.

Unplug the 283-B plug from the line and plug it into the dB meter. Set the dB meter to 600-ohm termination.

Is the waveform on the oscilloscope now correct?

The problem is not in this modem.

Scope J11 ('wrap signal' on the transmitter card).

Is the waveform correct (like Waveform #090 if the transmit C1 equalizer is switched out or not present)?

Go to the Test 2 Diagnostic, Transmit Test (block 070).

Is the continuity check good?

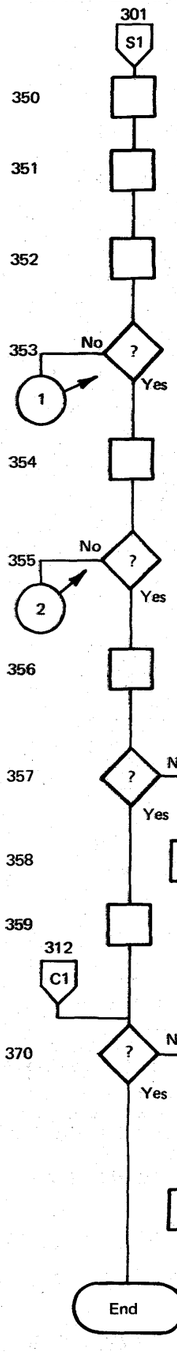
Repair or replace the faulty part.

Replace preamp card.

Reconnect the 283-B plug to the line and restart the line-side test.

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-107 for LIB 11 card positions

MAINTENANCE PROCEDURES, PART 12



Switched network problem

Establish a telephone line *connection* to an IBM 3872 Modem or appropriate IBM integrated modem.

Have the Test/Operate switch of the remote modem set to T4; start Test 3.

Using the dB meter set to BRIDGING, clip to the 'DT' and 'DR' spade lugs at the local data coupler and measure the transmit level.

Is the transmit level correct? (Refer to the benchmark chart.)

Scope the transmit signal at the 'DT' and 'DR' spade lugs. (Refer to the line-scoping procedure under "Scoping Hints and Precautions".)

Is the waveshape correct?

Have the remote modem set to T3; start Test 4 at the local modem, and use the dB meter set to BRIDGING to measure the receive level between 'DT' and 'DR'.

Is the receive level correct? (Refer to the benchmark chart.)

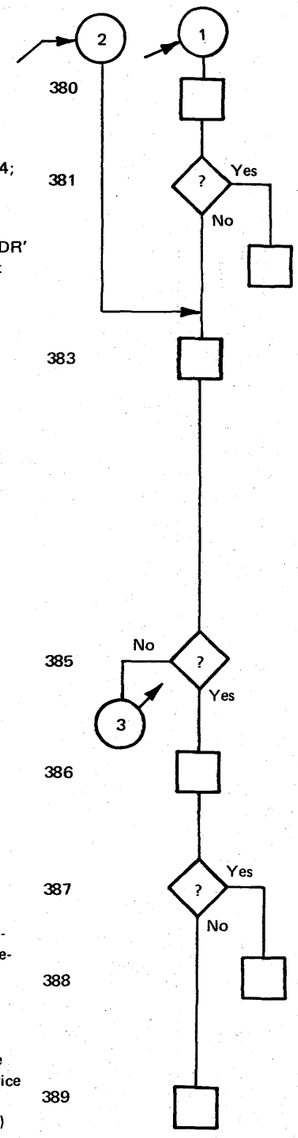
The problem is not in this modem.

Scope the receive line signal at the 'DT' and 'DR' spade lugs (see the line-scoping procedure under "Scoping Hints and Precautions") and compare it with preamp output D13 (see Waveform #014).

Is preamp output the same basic waveshape as the receive line signal? (The amplitude of preamp output should be nearly twice as great. Also, because the preamp attenuates low- and high-frequency noise, preamp output should appear "cleaned up".)

Replace preamp card and restart the line-side test.

The line-side test is satisfactory.



Jumper G10 ('- DSR' on the limiter card) to ground.

Is the transmit level now correct?

There is an auto-answer problem. Go to the AA/ACO Diagnostics (page C-560). Remove jumper.

Disconnect the telephone call and disconnect the cable to the coupler from the I/O gate connector and measure the transmit level between B12 and B13 ('data tip' and 'data ring' on the I/O gate connector). Use the dB meter, set to 600-ohm termination. B12 should be grounded by the analog switch circuit. If the transmit level is not correct, check it at the appropriate V2 or V4 connector position.

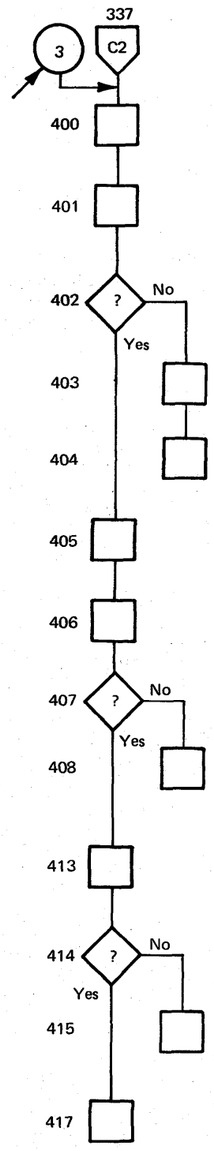
Is the transmit level now correct?

Check for continuity in the cable to the data coupler between B12 and the 'DT' spade lug, and between B13 and the 'DR' lug.

Is the continuity check good?

The problem is not in this modem or external cable.

Repair or replace the cable and restart the line-side test.



Remove preamp card from its socket.

Scope differentially G13 and J13 (±line driver output on the transmitter card). Sync on S04 ('ramp clock A' on the FET card).

Is the signal within the range of 46.3V–57.7V, peak-to-peak?

Return preamp card to its socket.

Replace transmitter card and restart the line-side test.

Return preamp card to its socket.

Scope B08 ('-wrap relay' on the preamp card).

Steady level ⟩+10.5?

See V*003 for points to scope to determine why the wrap relay does not pick. Remove jumper.

Abort Test 2. Using the 'line connection continuity' drawing, check the continuity of the line connections.

Is the continuity check good?

Repair or replace the faulty part, remove jumper and restart the line-side test.

Replace preamp card, remove jumper, and restart the line-side test.

See C-101 for LIB 5 card positions
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions

MAINTENANCE PROCEDURES, PART 13

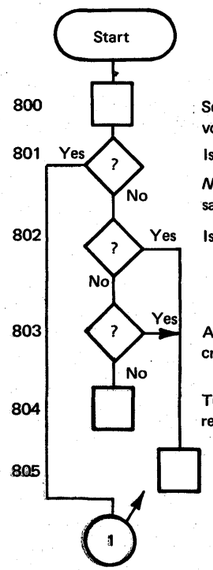
AA FAULT LOCATION

CIRCUIT CARDS INVOLVED WITH AUTO-ANSWER

CARD NAME	CARD CODE	LINE SET 6A	LIB 7	LINE SETS 8B, 12B	LINE SET 9A
AA Common	M862	YES	YES	YES	YES
AA interface w/o ACO	N829	YES	—	YES	—
ACO-2	M861	—	YES	—	YES

Use the following procedure to locate the source of auto answer problems.

1. Use the back panel indicator to answer the questions asked in this section before scoping. See the appropriate "Type X LIB CARD POSITIONS" page for the location in which to plug the indicator card. The indicator card plugs onto the back panel pins with the end of the indicator block marked TOP at the top so the lights are vertical.
2. Scope those signals that do not affect the indicator. Always scope pulsing signals.
3. See C-430 (EP) or C-432 (NCP) for panel procedures for the AA Test.



800 Set up the AA Test and dial the modem's number from a nearby voice telephone.

801 Is there a remote ringing sound?

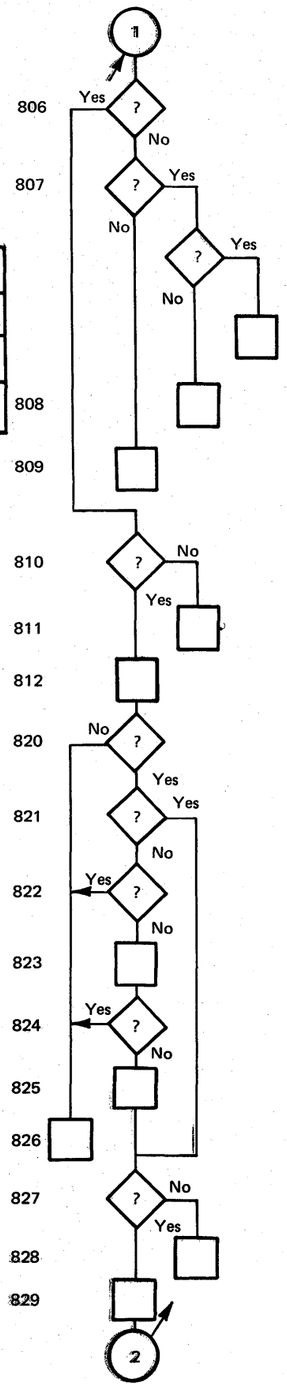
Note: Sound may be brief or unheard. Check decision 806 before saying "no".

802 Is there a busy signal?

803 Are the CBS coupler switches and indicators off and the handset cradled?

804 Turn off the switches, put the handset in the cradle, and restart.

805 Have the common carrier check the CBS coupler and loop. Restart.



806 Is 'OH' ('off hook') up? [Without ACO, B12 (AA intf); with ACO, S09 (ACO-2)].

807 Is 'RI' ('ring indicate') pulsing? [Without ACO, B07 (AA intf); with ACO, S02 (ACO-2)].

Is '-force DTR off' down? [With and without ACO, J13 (AA common)].

808 Wrap keeps this line down, but ACO Test does not wrap. Scope to determine problem.

Replace the AA common card and restart.

809 Recheck decisions 806 and 807 with the oscilloscope at the spade lugs attached to the data coupler. Repair or replace the cable if there is a discrepancy; if not, call the common carrier.

810 Is 'DA' ('data modem ready') up? [Without ACO, D12 (AA intf); with ACO, S07 (ACO-2)].

811 Replace the AA interface card (without ACO) or the ACO-2 (with ACO) and restart.

812 1- to 3-second delay by CBS.

820 Is 'CCT' ('coupler cut through') up? [Without ACO, B10 (AA intf); with ACO, U02 (ACO-2)].

821 Is the answer tone (2100Hz) heard?

822 Is 'SH' ('switch hook') up? [Without ACO, (AA intf); with ACO, U05 (ACO-2)].

823 Hang up the calling telephone, jumper B05 (AA common card) to ground and scope G02 (AA common) for a 2100Hz sine wave signal.

824 Is the answer tone signal present?

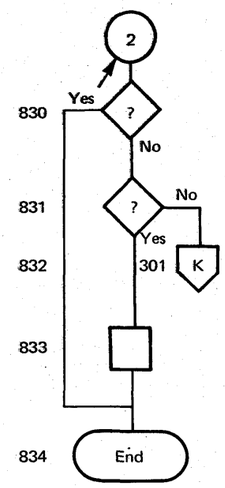
825 Replace the AA common card and restart. Remove jumper.

826 Recheck decisions 810 and 820 or 822 with the oscilloscope at the spade lugs attached to the data coupler. Repair or replace the cable if there is a discrepancy; if not, call the common carrier. Remove jumper.

827 Does the answer tone end and does 'DSR' ('data set ready') come on? [Without ACO, D09 (AA intf); with ACO, M13 (ACO-2)].

828 Replace the AA interface card (without ACO) or the ACO-2 (with ACO) and restart.

829 Set up the AA Test. Without ACO, scope 'data tip' at B02 (AA intf) for ground level, and scope 'data ring' at D06 (AA intf) for data signals. With ACO, scope 'data tip' at B02 (ACO threshold) for ground level, and scope 'data ring' at D06 (ACO threshold) for data signals.



830 Are both signals OK?

831 Is the data signal on 'DR' D06?

832 Local modem problem.

833 Replace the AA interface card (without ACO) or the ACO threshold card (with ACO) and restart.

834 No trouble found. Check cables and wiring.

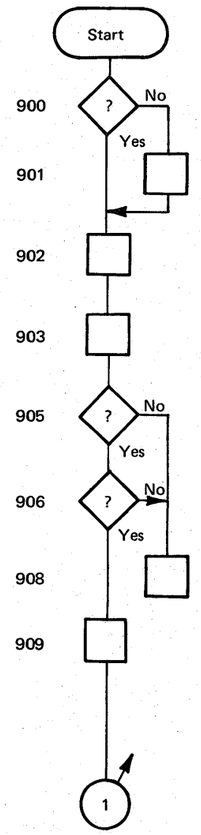
See C-102 for LIB 6 card positions
See C-103 for LIB 7 card positions
See C-104 for LIB 8 card positions
See C-105 for LIB 9 card positions
See C-108 for LIB 12 card positions

MAINTENANCE PROCEDURES, PART 14
ACO FAULT LOCATION

Use the back-panel indicator card to observe the status of the test points in the following procedure. See C-430 (EP) or C-432 (NCP) for the panel procedures for the ACO TEST

CIRCUIT CARDS INVOLVED WITH ACO

CARD NAME	CARD CODE	LIB 7	LINE SET 9A
ACO Interface	6834	YES	YES
ACO Threshold	M859	YES	YES
ACO-1	M860	YES	YES
ACO-2	M861	YES	YES
AA Common	M862	YES	YES



900 Are the CBS coupler switches off and is the telephone handset cradled?

901 Turn off the switches and put the handset in the cradle.

902 Plug the back-panel indicator card onto the pins of the appropriate card socket. See appropriate "LIB CARD POSITIONS" page.

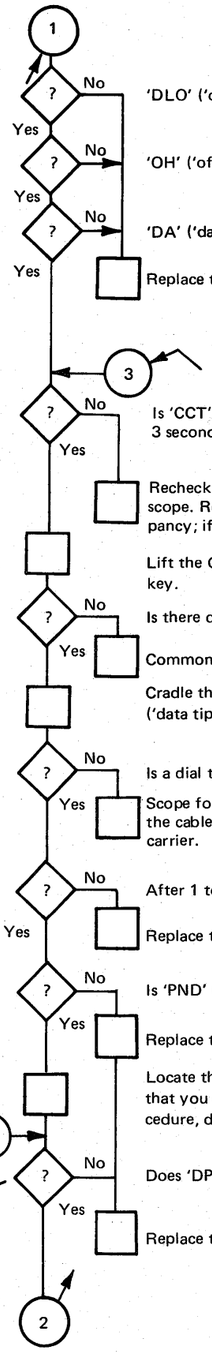
903 Set up Test 3 for the modem interface. Set up the ACO TEST for the autocall interface but do not activate it.

905 Is '160Hz Osc' functioning? (ACO will not work without '160Hz Osc.').

906 Is 'call request' or 'data terminal ready' active?

908 Replace card ACO-1 and restart.

909 *Note:* Normally, the next three decisions are almost simultaneous. See block 920.



910 'DLO' ('data line occupied') active?

911 'OH' ('off-hook') active?

912 'DA' ('data modem ready'), S07 (ACO-2) active?

913 Replace the ACO-1 card and restart.

920 Is 'CCT' ('coupler cut through') active after 1 to 3 seconds ?

921 Recheck decisions 911, 912, and 920 with the oscilloscope. Repair or replace the cable if there is a discrepancy; if not, call the common carrier.

924 Lift the CBS coupler handset and operate the exclusion key.

925 Is there dial tone on the CBS handset?

925A Common carrier problem.

926 Cradle the CBS handset and scope for dial tone at B02 ('data tip' on the ACO threshold card).

927 Is a dial tone present?

928 Scope for dial tone at the DT or DR. Repair or replace the cable if dial tone is present; if not, call the common carrier.

930 After 1 to 2 seconds of dial tone, is threshold active?

931 Replace the ACO threshold card and restart.

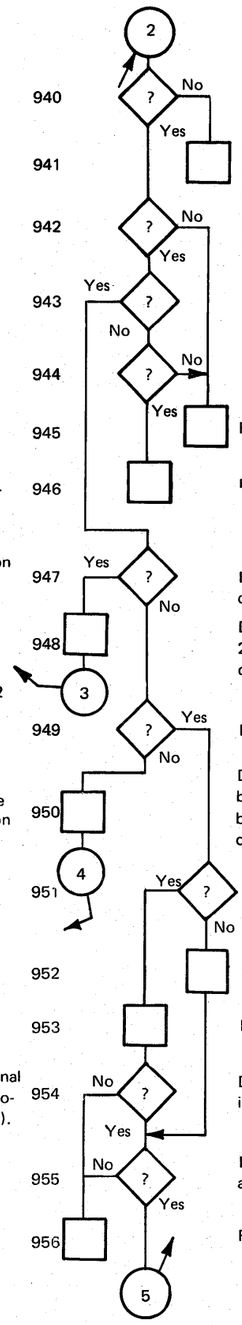
932 Is 'PND' ('present next digit') active?

933 Replace the ACO-1 card and restart.

934 Locate the telephone number of an auto answer terminal that you can have made ready. Using the ACO Test procedure, dial the first digit (set Adr/Data Switch E to 1).

935 Does 'DP' ('digit present') become active?

936 Replace the ACO-2 card and restart.



940 If an audio monitor feature is in operation at your Data Coupler, listen to the dial pulses. Was the number of dial pulses correct?

941 Replace the ACO-1 card and restart. If the trouble persists, replace the ACO-2 card instead and restart again.

942 Did 'PND' become inactive during dial pulsing?

943 Did 'PND' become active again?

944 Is 'DP' active?

945 Replace the ACO-1 card and restart.

946 Replace the ACO-2 card and restart.

947 Is SEP (separator) required for a second dial tone? (only after the first dial digit.)

948 Dial SEP by moving Adr/Data Switch E to 2 and pressing INTERRUPT. This *must* be done before the timeout sets ACR.

949 Have all digits been dialed?

950 Dial the next digit by incrementing switch E by 1 for each digit. This must be done before the timeout sets ACR. To dial all the digits automatically, set switch E to 0.

951 Is card strapped to require EON (end of number)?

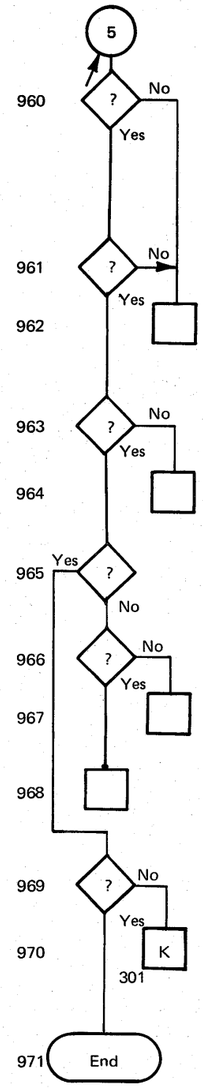
952 'PND' remains on.

953 Dial EON.

954 Does 'PND' become inactive and remain inactive?

955 Is S07 ('data modem ready' on ACO-2) active?

956 Replace the ACO-1 card and restart.



960 Is 'CCT' active?

961 Can ringing or answer tone be heard on the call audio monitor feature?

962 Common-carrier problem.

963 Is the answer tone (2100 Hz) heard, ending after about 3 seconds?

964 Have the distant-end modem checked for an auto answer problem.

965 Does 'DSC' (Distant Station Connected) become active?

966 Is 'threshold' active?

967 Replace the ACO threshold card and restart.

968 Replace the ACO-1 card and restart.

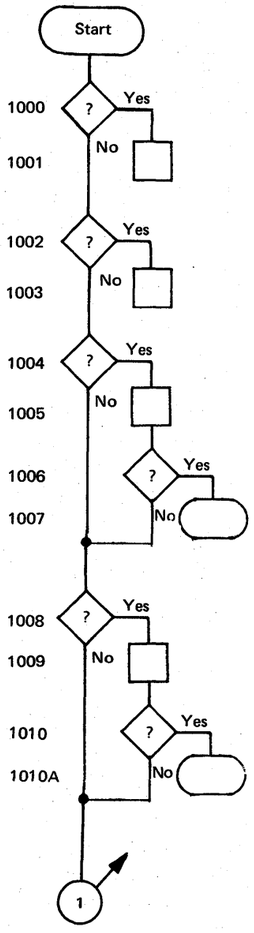
969 Is data audible on the audio monitor feature?

970 Local modem problem.

971 If the trouble persists, check cables and connections.

See C-103 for LIB 7 card positions
See C-105 for LIB 9 card positions

MAINTENANCE PROCEDURE, PART 15
LIB TYPES 8, 9, 10, AND 12 MODEM PROBLEMS



Auto Answer problem?

See AA fault location procedures on C-560.

Automatic call originate problem?

See ACO fault location procedures on C-570.

Integrated modem receiver problem?

Swap receiver card— see C-104, C-105, C-106, or C-108.

Proper operation?

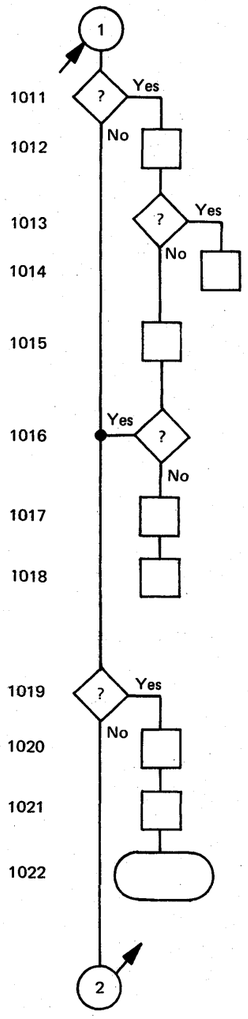
Replace bad receiver card.

Line set 12A or 12B 'break' problem?

Swap break card—see C-108.

Proper operation?

Replace bad break card.



Integrated modem transmitter problem?

Swap transmit card-see C-104, C-105, C-106, or C-108.

Proper operation?

Replace bad transmit card.

Check transmit level of transmit card with FE db meter and adjust if necessary. See C-400 for db meter P/N.

Strobe pulses available? (see C-300).
('Transmit data mark' is alternating 1's and 0's)

Swap bit clock control card—see C-104, C-105, C-106, or C-108.

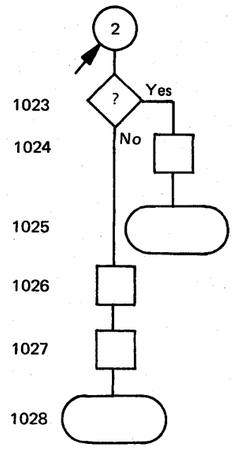
Swap adapter/data line interface card.

Scanner interface problem?

Swap bit clock control card—see C-104, C-105, C-106, or C-108.

Swap isolation card—see C-104, C-105, C-106, or C-108.

Scope lines from scanner—see C-020.



LIB interface problem?

Swap adapter/data line interface card—see C-104, C-105, C-106, or C-108.

Scope lines from LIB.

Check card and board jumper options.

Swap adapter/data line interface card—see C-104, C-105, C-106, or C-108.

Scope lines to integrated modem.

Summary of IFT Routines and Panel Procedures to Simulate the Modem Tests

Modem Test	IFT Routines		EP or NCP Panel Procedures
	Type 1 Scanner	Type 2 Scanner	
Test 2	15C6	X681 *	Test 2
Test 3	15C8	X6CE	Test 3
Test 4	15CA	X6CE	Test 4
Auto-Ans.	15CA	X6CE	Auto-Ans.
Auto Call	15C8	X6CE	ACO Test

*Line set 10A uses routine X684

See C-104 for LIB 8 card positions
See C-105 for LIB 9 card positions
See C-106 for LIB 10 card positions
See C-108 for LIB 12 card positions

INDEX

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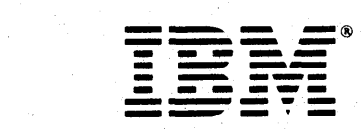

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