FAA–2371 (Revision B)

DATA PROCESSING SYSTEM MAINTENANCE DIAGNOSTIC PROGRAMS DESCRIPTIONS: 1003–2740

9020D and E

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Airway Facilities Service
Radar/Automation Engineering Division
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REVISION HISTORY

Revision Level	Date	IBM or CCD/PTR Number	Comments
A	1 December 1979		
B	1 December 1980	08099723F	

Archival Note

This is Volume II as shown in the 'Vol' column of the index.

The original document was retained to support only the 9020 CE. Pages supporting other units were discarded in the 1980s. Hence only the pages for programs D1101 to D1DA3 are included.

Mark Triggers March 2024

IBM 9020D AND 9020E DATA PROCESSING SYSTEM
INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS

These volumes of Maintenance Diagnostic Programs contain diagnostic program descriptions and listings needed for off–line maintenance of the 9020D and 9020E Systems. The descriptions are contained in Volumes I through V; the listings are contained in Volumes VI through XXX. The programs are in program identity sequence within each of these two categories.

This index provides the following information for each identifiable program:

Identity, $P_1P_2P_3S_1S_2$, of each utility, diagnostic monitor, and diagnostic section. The overlay number, A_1A_2, is also given for each overlay subsection.

Name of utility, diagnostic monitor, diagnostic section, or overlay subsection (hereafter, all called programs).

CPU (IOCE, CE) that can execute the program in the 9020 System, as denoted by an X under the appropriate heading(s). For example D0040, Hardcore, can be run in only the CE; D0B01, IDM, can be run in only the IOCE; and D0C00, SDM, can be run in either the IOCE or CE.

Monitor (IDM, SDM, MDM–D/E) required to execute the diagnostic section or overlay subsection, as denoted by an X under the appropriate heading(s). For example D0010, Go/No–Go requires no monitor because it is self–controlled; D1003–D1077, the IOCE bring–up or functional tests, require either IDM or SDM; and DE0A3–DE5CA, SEVA, requires MDM–D/E.

System Model Only (D or E for 9020D or 9020E System, respectively) denotes system–dependent sections. For example, D6CA4, 7265–02 System Console, applies only to a 9020D System and D6CA6, 7265–03 Configuration Console, applies only to a 9020E System. Testing by sections identified by a D or E is bypassed if the model requirement is not met.

Multiprogramming is possible under control of MDM–D/E for sections denoted by M. For example, D1111–D1115, CEDA, can be multiprogrammed.

Operator Intervention is normally required by sections denoted by O. For example, D13A0, CE Interval Timer, requires the activation and de–activation of the DISABLE INTERVAL TIMER switch.

Section Sense Switches are provided in sections denoted by S. For example, one of several section sense switches in D1111–D1115, CEDA, causes the printing of lengthier error messages when it is set to 1.

Additional Units, in addition to those needed by the monitor, are required by sections denoted by A. In some cases the unit under test is the additional unit required.

IBM 9020D AND 9020E DATA PROCESSING SYSTEM (Continued)
INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS

Description reference and volume numbers in which additional information regarding the program can be found. For example DMMM I refers to the "Maintenance Monitor Manual" in Volume I. Also, for section D1003 (LA Instruction), 1003 II refers to description D1003 in Volume II. Notice that D1004 through D100C also refer to description D1003; this is because all RX–format, fixed–point, IOCE–instruction functional tests are included in description D1003.

Listing volume number in which the listing for the program can be found. If no volume number is listed, the listing is not provided.

Two descriptions not included in the index are "Maintenance Monitor Flowcharts", which is in Volume I, and "PAM Appendices", which is in Volume IV.

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PREFACE

Revision B of FAA–2371 modifies a sample print message in the description of D22A0. Also, a sentence has been added to paragraph 3.0 of D22A0 to warn the user that the executing CE must have its own SCON bit set (PTR 08099723F).

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Identity PPPSSSAA 12312r12	Name	CPU		Monitor			System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description		Listing
		IOCE	CE	IDM	SDM	MDM–D/E		Ref	Vol	Vol
D0000	IPL Card Deck Loader	X	X					DMMM	I	None
D0001	Utility Library Loader	X	X					DMMM	I	VI
D0010	Go/No–Go	X	X					DMMM	I	VI
D0020	Basic Storage Test	X	X					DMMM	I	VI
D0040	Hardcore		X					DMMM	I	VI
D0B01	Initial Diagnostic Monitor	X						DMMM	I	VI
D0C00	Subsystem Diagnostic Monitor	X	X					DMMM	I	VI
D0CF0	Storage Dump	X	X					DMMM	I	VI
D0D10	Formatted Logout	X			X			DMMM	I	VI
D0D50	Multiprocessing Diagnostic Monitor D/E		X					DMMM	I	VII
D0D60	Short Logout Formatter	X	X		X	X		DMMM	I	VII
D0D70	Formatted Logout		X		X	X		DMMM	I	VII
D1003	LA	X		X	X			1003	II	VIII
D1004	L	X		X	X			1003	II	VIII
D1005	ST	X		X	X			1003	II	VIII
D1006	A	X		X	X			1003	II	VIII
D1007	S, C	X		X	X			1003	II	VIII
D1008	CL	X		X	X			1003	II	VIII
D1009	N, O, X	X		X	X			1003	II	VIII
D100C	AL, SL	X		X	X			1003	II	VIII

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE CE	Monitor IDM SDM MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref Vol	List–ing Vol
D1010	LR Part 1	X	X X		1010 II	VIII
D1011	LR Part 2	X	X X		1010 II	VIII
D1012	LR Part 3	X	X X		1010 II	VIII
D1013	LR Part 4	X	X X		1010 II	VIII
D1014	AR	X	X X		1010 II	VIII
D1015	SR, CR	X	X X		1010 II	VIII
D1016	CLR	X	X X		1010 II	VIII
D1017	NR	X	X X		1010 II	VIII
D1018	OR	X	X X		1010 II	VIII
D1019	XR	X	X X		1010 II	VIII
D101A	LPR, LNR, LTR, LCR	X	X X		1010 II	VIII
D101B	ALR, SLR	X	X X		1010 II	VIII
D101F	BCR, BC	X	X X		101F II	IX
D1020	BAL, BALR	X	X X		101F II	IX
D1021	BCT, BCTR	X	X X		101F II	IX
D1022	BXH, BXLE	X	X X		101F II	IX
D1023	Branch Instructions	X	X X		101F II	IX
D1027	LH, STH, AH, SH, CH	X	X X		1027 II	IX
D102A	SRL, SRA, SLL, SLA	X	X X		102A II	IX
D102D	TM	X	X X		102D II	IX
D102E	CLI	X	X X		102D II	IX
D102F	MVI	X	X X		102D II	IX
D1030	NI	X	X X		102D II	IX
D1031	OI	X	X X		102D II	IX
D1032	XI	X	X X		102D II	IX
D1037	STM	X	X X		1037 II	IX
D1038	STM, LM	X	X X		1037 II	IX

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Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D103C	SVC, LPSW, SPM, SSM	X		X	X			103C	II	IX
D103F	MH	X		X	X			103F	II	IX
D1040	M	X		X	X			103F	II	IX
D1041	MR	X		X	X			103F	II	IX
D1042	D	X		X	X			103F	II	IX
D1043	DR	X		X	X			103F	II	IX
D1045	IC, STC	X		X	X			1045	II	IX
D1047	SRDL, SRDA, SLDL, SLDA	X		X	X			1047	II	IX
D104A	CLC	X		X	X			104A	II	X
D104B	CLC	X		X	X			104A	II	X
D104C	CLC, MVC	X		X	X			104A	II	X
D104D	NC	X		X	X			104A	II	X
D104E	OC	X		X	X			104A	II	X
D104F	XC	X		X	X			104A	II	X
D1050	MVO	X		X	X			104A	II	X
D1051	MVN	X		X	X			104A	II	X
D1052	MVZ	X		X	X			104A	II	X
D1053	MVW	X		X	X			1053	II	X
D105A	CVB, CVD	X		X	X			105A	II	X
D105C	TR	X		X	X			105A	II	X
D105D	TRT	X		X	X			105A	II	X
D105E	PACK, UNPK	X		X	X			105A	II	X
D105F	PACK, UNPK	X		X	X			105A	II	X
D1060	Boundary Test of NC, OC, XC, MVO, MVN, MVZ	X		X	X			1060	II	X

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	 CE	Monitor IDM	 SDM	 MDM–D/E	System Model Only Multiprogram Op Intervention Section Sense Sw Additional Units	Description Ref	 Vol	Listing Vol
D1063	EX, Small Binary Set; Part 1	X		X	X			1063	II	X
D1064	EX, Small Binary Set; Part 2	X		X	X			1063	II	X
D1065	EX, Small Binary Set; Part 3	X		X	X			1063	II	X
D1066	EX, Standard Set; Part 1	X		X	X			1063	II	X
D1067	EX, Standard Set; Part 2	X		X	X			1063	II	X
D1068	LDA, LI, TS, WRD; Part 1	X		X	X			1068	II	X
D1069	LDA, LI, TS, WRD; Part 2	X		X	X			1068	II	X
D106B	Program Interrupts, Part 1	X		X	X			106B	II	XI
D106C	Program Interrupts, Part 2	X		X	X			106B	II	XI
D106D	Program Interrupts, Part 3	X		X	X			106B	II	XI
D106E	Operation Exceptions	X		X	X			106E	II	XI
D1071	EX, Program Interrupts; Part 1	X		X	X			1071	II	XI
D1072	EX, Program Interrupts; Part 2	X		X	X			1071	II	XI
D1075	Pair Instruction Scrambler	X		X	X			1075	II	XI

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Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D1076	Diagnose Kernels, Part 1	X		X	X			1076	II	XI
D1077	Diagnose Kernels, Part 2	X		X	X			1076	II	XI
D1101	Basic CE Test, Part 1		X		X	X	M S	1101	II	XII
D1102	Basic CE Test, Part 2		X		X	X	M S	1101	II	XII
D1103	Basic CE Test, Part 3		X		X	X	M S	1101	II	XII
D1108	Basic Diagnose and Logout		X		X	X	M S	1108	II	XII
D1111	CEDA, Part 1		X		X	X	M S	1111	II	XIII
D1112	CEDA, Part 2		X		X	X	M S	1111	II	XIII
D1113	CEDA, Part 3		X		X	X	M S	1111	II	XIII
D1114	CEDA, Part 4		X		X	X	M S	1111	II	XIII
D1115	CEDA, Part 5		X		X	X	M S	1111	II	XIII
D1151	LA		X		X	X	M	1151	II	XIV
D1152	L		X		X	X	M	1151	II	XIV
D1153	ST		X		X	X	M	1151	II	XIV
D1154	A		X		X	X	M	1151	II	XIV
D1155	S, C		X		X	X	M	1151	II	XIV
D1156	CL		X		X	X	M	1151	II	XIV
D1157	N, O, X		X		X	X	M	1151	II	XIV
D115A	AL, SL		X		X	X	M	1151	II	XIV
D115C	LR, Part 1		X		X	X	M	115C	II	XIV
D115D	LR, Part 2		X		X	X	M	115C	II	XIV

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D115E	LR, Part 3		X		X	X	M	115C	II	XIV
D115F	LR, Part 4		X		X	X	M	115C	II	XIV
D1160	AR		X		X	X	M	115C	II	XIV
D1161	SR, CR		X		X	X	M	115C	II	XIV
D1162	CLR		X		X	X	M	115C	II	XIV
D1163	NR		X		X	X	M	115C	II	XIV
D1164	OR		X		X	X	M	115C	II	XIV
D1165	XR		X		X	X	M	115C	II	XIV
D1166	LPR, LNR, LTR, LCR		X		X	X	M	115C	II	XIV
D1167	ALR, SLR		X		X	X	M	115C	II	XIV
D1169	BCR, BC		X		X	X	M	1169	II	XV
D116A	BALR		X		X	X	M	1169	II	XV
D116B	BCT, BCTR		X		X	X	M	1169	II	XV
D116C	BXH, BXLE		X		X	X	M	1169	II	XV
D116D	Branch Instructions		X		X	X	M	1169	II	XV
D116F	LH, STH, AH, SH, CH		X		X	X	M	116F	II	XV
D1171	SRL, SRA, SLL, SLA		X		X	X	M	1171	II	XV
D1173	TM		X		X	X	M	1173	II	XV
D1174	CLI		X		X	X	M	1173	II	XV
D1175	MVI		X		X	X	M	1173	II	XV
D1176	NI		X		X	X	M	1173	II	XV
D1177	OI		X		X	X	M	1173	II	XV
D1178	XI		X		X	X	M	1173	II	XV
D1179	TS		X		X	X	M	1179	II	XV
D117B	STM		X		X	X	M	117B	II	XV

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Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D117C	STM, LM		X		X	X	M	117B	II	XV
D117E	SVC, LPSW, SPM, SSM		X		X	X		117E	II	XV
D1180	MH		X		X	X	M	1180	II	XV
D1181	M		X		X	X	M	1180	II	XV
D1182	MR		X		X	X		1180	II	XV
D1183	D		X		X	X	M	1180	II	XV
D1184	DR		X		X	X	M	1180	II	XV
D1186	SRDL, SRDA, SLDL, SLDA		X		X	X	M	1186	II	XVI
D118A	CLC, MVC		X		X	X	M	118A	II	XVI
D118B	NC		X		X	X	M	118A	II	XVI
D118C	OC		X		X	X	M	118A	II	XVI
D118D	XC		X		X	X	M	118A	II	XVI
D118E	MVO		X		X	X	M	118A	II	XVI
D118F	MVN		X		X	X	M	118A	II	XVI
D1190	MVZ		X		X	X	M	118A	II	XVI
D1191	MVW		X		X	X	M	1191	II	XVI
D1192	IC, STC, ISK, SSK		X		X	X	M	1192	II	XVI
D1196	CVD, CVB		X		X	X	M	1196	II	XVI
D1197	TR		X		X	X	M	1196	II	XVI
D1198	TRT		X		X	X	M	1196	II	XVI
D1199	PACK, UNPK; Part 1		X		X	X	M	1196	II	XVI
D119A	PACK, UNPK; Part 2		X		X	X	M	1196	II	XVI
D119B	Boundary Test of NC, OC, XC, MVN, MVZ, TR, TRT		X		X	X	M	1196	II	XVI

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Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D119C	SPSB, LPSB, LI; Part 1		X		X	X		119C	II	XVI
D119D	SPSB, LPSB, LI; Part 2		X		X	X		119C	II	XVI
D11A2	LE, STE, LD, STD, CE, CD		X		X	X	M	11A2	II	XVI
D11A6	LER, CER, LDR, CDR, LTER		X		X	X	M	11A2	II	XVI
D11A9	LTDR, LCER, LCDR		X		X	X	M	11A2	II	XVI
D11AC	LPER, LPDR, LNER, LNDR		X		X	X	M	11A2	II	XVII
D11B0	AER, ADR, AE, AD		X		X	X	M	11A2	II	XVII
D11B4	AUR, AWR, AU, AW		X		X	X	M	11A2	II	XVII
D11B8	SER, SDR, SE, SD		X		X	X	M	11A2	II	XVII
D11BC	SUR, SWR, SU, SW		X		X	X	M	11A2	II	XVII
D11C0	HER, HDR		X		X	X	M	11A2	II	XVII
D11C2	MER, MDR, ME, MD		X		X	X	M	11A2	II	XVII
D11C6	DER, DDR, DE, DD		X		X	X	M	11A2	II	XVII
D11CA	Multiply and Divide Reliability		X		X	X	M	11A2	II	XVII
D11CD	AP, Part 1		X		X	X	M	11CD	II	XVII
D11CE	AP, Part 2		X		X	X	M	11CD	II	XVII
D11CF	SP		X		X	X	M	11CD	II	XVII
D11D0	CP		X		X	X	M	11CD	II	XVII
D11D1	ZAP		X		X	X	M	11CD	II	XVII
D11D3	MP, Part 1		X		X	X	M	11CD	II	XVII
D11D4	MP, Part 2		X		X	X	M	11CD	II	XVII
D11D5	DP, Part 1		X		X	X	M	11CD	II	XVII
D11D6	DP, Part 2		X		X	X	M	11CD	II	XVII

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Identity PPPSSSAA 12312r12	Name	CPU IOCE	 CE	Monitor IDM	 SDM	 MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	 Vol	List–ing Vol
D11D7	ED		X		X	X	M	11CD	II	XVII
D11D8	EDMK		X		X	X	M	11CD	II	XVII
D11DA	EX, Small Binary Set; Part 1		X		X	X	M	11DA	II	XVIII
D11DB	EX, Small Binary Set; Part 2		X		X	X	M	11DA	II	XVIII
D11DC	EX, Small Binary Set; Part 3		X		X	X	M	11DA	II	XVIII
D11DD	EX, Standard Set; Part 1		X		X	X	M	11DA	II	XVIII
D11DE	EX, Standard Set; Part 2		X		X	X	M	11DA	II	XVIII
D11DF	EX, Floating Point Set; Part 1		X		X	X	M	11DA	II	XVIII
D11E0	EX, Floating Point Set; Part 2		X		X	X	M	11DA	II	XVIII
D11E1	EX, Decimal Set		X		X	X	M	11DA	II	XVIII
D11E4	Program Interrupts, Small Binary Set		X		X	X		11E4	II	XVIII
D11E5	Program Interrupts, Standard Set		X		X	X		11E4	II	XVIII
D11E6	Program Interrupts, Floating Point Set		X		X	X		11E4	II	XVIII
D11E7	Program Interrupts, Decimal Set		X		X	X		11E4	II	XVIII
D11E8	Program Interrupts, Suppression Completion		X		X	X		11E4	II	XVIII

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Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multiprogram Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D11E9	Operation Exception		X		X	X	M	11E9	II	XVIII
D11EB	Execute Pgm Irpt, Small Binary Set		X		X	X		11EB	II	XVIII
D11EC	Execute Pgm Irpt, Standard Set		X		X	X		11EB	II	XVIII
D11ED	Execute Pgm Irpt, Floating Point Set		X		X	X		11EB	II	XVIII
D11EE	Execute Pgm Irpt, Decimal Set		X		X	X		11EB	II	XVIII
D13A0	Interval Timer		X		X	X	O	13A0	II	XVIII
D13A5	360/9020 Mode Differences of Operation		X		X	X	S	13A5	II	XVIII
D13B0	SPSB, LPSB, LI, SCON, IATR, SATR, DLY, MVW		X		X	X	O	13B0	II	XVIII
D13BA	Diagnose, Scan–In, and Logout		X		X	X	O	13BA	II	XIX
D13C0	CSS, LC		X		X	X	S	13C0	II	XIX
D13C1	CVWL		X		X	X	S	13C1	II	XIX
D13C2	RPSB		X		X	X	S	13C2	II	XIX
D13C8	Interrupt Priority Test		X		X	X	O S	13C8	II	XIX
D13CD	Random		X		X	X	S	13CD	II	XIX
D1401	Interval Timer	X			X		O	1401	II	XIX
D1403	DLY Instruction	X			X		O	1403	II	XIX
D1501	Diagnose Kernels, Part 3	X			X		A	1501	II	XIX

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Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	List–ing Vol
D1DA3	Direct Control		X		X	X	O S	1DA3	II	XX
D2101	Local Storage	X			X			2101	II	XX
D22A0	Storage and Display Storage Diagnostic		X		X	X	S	22A0	II	XX
D22A4	Storage and Display Storage Error Checks		X		X	X	S	22A4	II	XX
D22AA	Storage and Display Storage Protection		X		X	X	M S	22AA	II	XX
D2308	MACH–TO–SE Diagnostic	X			X		S A	2308	II	XX
D24A0	DE/DG Interface Functions		X			X	E S	24A0	II	XX
D2740	MACH Storage Diagnostic	X			X		S	2740	II	XX
D3051	Multiplexor Channel Functional, Part 1	X	X		X	X	A	3051	III	XXI
D3052	Multiplexor Channel Functional, Part 2	X	X		X	X	A	3051	III	XXI
D3053	Multiplexor Channel Functional, Part 3	X	X		X	X	A	3051	III	XXI
D3054	Multiplexor Channel Invalid Specifications	X	X		X	X	A	3054	III	XXI
D3055	Multiplexor Channel SPCI	X	X		X	X	A	3055	III	XXI

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D3151	Selector Channel Functional, Part 1	X	X		X	X	A	3151	III	XXI
D3152	Selector Channel Functional, Part 2	X	X		X	X	A	3151	III	XXI
D3153	Selector Channel Functional, Part 3	X	X		X	X	A	3151	III	XXI
D3154	Selector Channel Invalid Specifications	X	X		X	X	A	3154	III	XXI
D3155	Selector Channel SPCI	X	X		X	X	A	3055	III	XXI
D4050	2400/2800 Tape; Sense, Read, Write	X	X		X	X	S A	4050	III	XXII
D4051	2400/2800 Tape; Backspace, Forward Space	X	X		X	X	S A	4050	III	XXII
D4052	2400/2800 Tape; Characters as Tape Marks	X	X		X	X	S A	4050	III	XXII
D4053	2400/2800 Tape; TIO, Count 5, CU Busy	X	X		X	X	S A	4050	III	XXII
D4054	2400/2800 Tape; SIO, TIO, Clear Status	X	X		X	X	S A	4050	III	XXII
D4055	2400/2800 Tape; Flags, CAW Valid and Invalid	X	X		X	X	S A	4050	III	XXII

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D4056	2400/2800 Tape; SIO, HIO	X	X		X	X	S A	4050	III	XXII
D4057	2400/2800 Tape; Data Chaining	X	X		X	X	S A	4050	III	XXII
D4058	2400/2800 Tape; 7 Track Mode Density	X	X		X	X	S A	4050	III	XXII
D4059	2400/2800 Tape; 7 Track Mode	X	X		X	X	S A	4050	III	XXII
D405A	2400/2800 Tape; Translator	X	X		X	X	S A	4050	III	XXII
D405B	2400/2800 Tape; Data Converter	X	X		X	X	S A	4050	III	XXII
D405C	2400/2800 Tape; Data Converter	X	X		X	X	S A	4050	III	XXII
D405D	2400/2800 Tape; Data Converter Set	X	X		X	X	S A	4050	III	XXII
D405E	2400/2800 Tape; Rewind, Unload, End of Tape	X	X		X	X	O S A	4050	III	XXII
D405F	2400/2800 Tape; Interchangeability	X	X		X	X	O S A	4050	III	XXII
D4060	Tape Motion Test	X	X		X	X	S A	4060	III	XXII
D46A0	TCU Dual Interface		X			X	S A	46A0	III	XXII
D6251	2540 Punch	X	X		X	X	O S A	6251	III	XXIII
D6261	2540 Reader, Part 1	X	X		X	X	O S A	6261	III	XXIII
D6262	2540 Reader, Part 2	X	X		X	X	O S A	6261	III	XXIII

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multiprogram Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D6351	Printer Functional, Part 1	X	X		X	X	M O S A	6351	III	XXIII
D6352	Printer Functional, Part 2	X	X		X	X	M S A	6351	III	XXIII
D6353	Printer Functional, Part 3	X	X		X	X	M S A	6351	III	XXIII
D6354	Printer Ripple, Print Test	X	X		X	X	M S A	6354	III	XXIII
D6355	Printer Functional, Part 4	X	X		X	X	M O S A	6355	III	XXIII
D6356	Printer Carriage	X	X		X	X	M O S A	6356	III	XXIII
D6651	1052, Basic Operation, and Write Tests	X	X		X	X	M O S A	6651	III	XXIII
D6652	1052, Mechanical Test	X	X		X	X	M O S A	6651	III	XXIII
D6653	1052, Read Test	X	X		X	X	M O S A	6651	III	XXIII
D6A51	2821/2540 Channel Register Test	X	X		X	X	S A	6A51	III	XXIII
D6A52	2821/2540 Control Program	X	X		X	X	S A	6A52	III	XXIII
D6A53	2821/2540 Buffer Addressing Test	X	X		X	X	S A	6A53	III	XXIII
D6A54	2821/1403 Print Buffer	X	X		X	X	S A	6A54	III	XXIII
D6A55	2821/1403 UCS Buffer	X	X		X	X	S A	6A54	III	XXIII

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D6A56	2821/1403 Print Buffer Data Reg FLT	X	X		X	X	S A	6A54	III	XXIII
D6A57	2821/1403 UCB Data Reg FLT	X	X		X	X	S A	6A54	III	XXIII
D6A58	2821/1403 UCB Restore	X	X		X	X	S A	6A54	III	XXIII
D6AA0	2821 Dual Interface		X			X	S A	6AA0	III	XXIII
D6CA4	7265–02 System Console		X			X	D O S A	6CA4	IV	XXIII
D6CA6	7265–03 Configuration Console		X		X	X	E O S A	6CA6	IV	XXIII
D8050	DASF Pack Initializer	X	X		X		D O S A	8050	IV	XXIIIA
D8051	DASF SCU; TIO, Sense, Seek	X	X		X	X	D S A	8051	IV	XXIIIA
D8052	DASF SCU; Search Part 1	X	X		X	X	D S A	8051	IV	XXIIIA
D8053	DASF SCU; Search Part 2	X	X		X	X	D S A	8051	IV	XXIIIA
D8054	DASF SCU; Search Part 3	X	X		X	X	D S A	8051	IV	XXIIIA
D8055	DASF SCU; File Protect	X	X		X	X	D S A	8051	IV	XXIIIA
D8056	DASF SCU; CU Busy & End, Excep	X	X		X	X	D S A	8051	IV	XXIIIA
D8057	DASF SCU; Inval Sequences Part 1	X	X		X	X	D S A	8051	IV	XXIIIA
D8058	DASF SCU; Inval Sequences Part 2	X	X		X	X	D S A	8051	IV	XXIIIA

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D8059	DASF SCU; Sense Bits 5–7, 10–12	X	X		X	X	D S A	8051	IV	XXIIIA
D805A	DASF SCU; Trunc Read, MT, Long	X	X		X	X	D S A	8051	IV	XXIIIA
D805B	DASF SCU; Erase, Sp, Read IPL, EOF	X	X		X	X	D S A	8051	IV	XXIIIA
D805C	DASF SCU; Over/ Under Truncation	X	X		X	X	D S A	8051	IV	XXIIIA
D805D	DASF SCU; HIO Address Mark	X	X		X	X	D S A	8051	IV	XXIIIA
D805E	DASF SCU; File Interaction	X	X		X	X	D S A	8051	IV	XXIIIA
D805F	DASF SCU; Search Part 4	X	X		X	X	D S A	8051	IV	XXIIIA
D8060	DASF SCU; Overflow Part 1	X	X		X	X	D S A	8051	IV	XXIIIA
D8061	DASF SCU; Overflow Part 2	X	X		X	X	D S A	8051	IV	XXIIIA
D8062	DASF SCU; 6th Sense Byte Part 1	X	X		X	X	D S A	8051	IV	XXIIIA
D8063	DASF SCU; 6th Sense Byte Part 2	X	X		X	X	D S A	8051	IV	XXIIIA
D8064	DASF SCU; 6th Sense Byte Part 3	X	X		X	X	D S A	8051	IV	XXIIIA
D8065	DASF DSU Part 1	X	X		X	X	D S A	8065	IV	XXIIIA
D8066	DASF DSU Part 2	X	X		X	X	D S A	8065	IV	XXIIIA
D8067	DASF DSU Part 3	X	X		X	X	D S A	8065	IV	XXIIIA
D8068	DASF DSU Part 4	X	X		X	X	D S A	8065	IV	XXIIIA

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
D8069	DASF Random Access Timing	X	X		X	X	D O S A	8069	IV	XXIIIA
D806A	DASF Pack Data Integrity	X	X		X	X	D O S A	806A	IV	XXIIIA
D80A0	DASF Two Channel Switch		X			X	D S A	80A0	IV	XXIIIA
D9051	Reconfiguration Cntl Unit	X	X		X	X	E M S A	9051	IV	XXIV
DA051	Channel–to–Channel Adapter	X	X		X	X	A	A051	IV	XXIV
DB051	2701 DAU, Part 1	X	X		X	X	E S A	B051	IV	XXIV
DB052	2701 DAU, Part 2	X	X		X	X	E S A	B051	IV	XXIV
DB0A1	2701 DAU Two Proc Switch		X			X	E O S A	B0A1	IV	XXIV
DCC51–00	PAM, Control Section	X	X		X	X	D A	CC51	IV	XXV
DCC51–02	Adapter Common Test	X	X		X	X	D A	CC51	IV	XXV
DCC51–04	GPO Adapter	X	X		X	X	D A	CC51	IV	XXV
DCC51–06	GPI Adapter	X	X		X	X	D A	CC51	IV	XXV
DCC51–08	RVDP Adapter	X	X		X	X	D A	CC51	IV	XXV
DCC51–09	CD Adapter	X	X		X	X	D A	CC51	IV	XXV
DCC51–0A	INTI Adapter	X	X		X	X	D A	CC51	IV	XXV
DCC51–0C	INTO Adapter	X	X		X	X	D A	CC51	IV	XXV
DCC51–0E	TTYLL Adapter, Read	X	X		X	X	D A	CC51	IV	XXV
DCC51–0F	TTYLL Adapter, Write	X	X		X	X	D A	CC51	IV	XXV
DCC51–10	1052 Adapter	X	X		X	X	D A	CC51	IV	XXV

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
DCC51–12	FDEP Adapter, Part 1	X	X		X	X	D A	CC51	IV	XXV
DCC51–13	FDEP Adapter, Part 2	X	X		X	X	D A	CC51	IV	XXV
DCC51–14	PAM Common Test, Part 1	X	X		X	X	D A	CC51	IV	XXV
DCC51–15	PAM Common Test, Part 2	X	X		X	X	D A	CC51	IV	XXV
DCC51–16	BP Adapter	X	X		X	X	D A	CC51	IV	XXV
DCC61–00	FSP/FSPCU, Control Section	X	X		X	X	D A	CC61	IV	XXVI
DCC61–01	Automatic Functions	X	X		X	X	D A	CC61	IV	XXVI
DCC61–02	Timing	X	X		X	X	D S A	CC61	IV	XXVI
DCC61–03	Manual Functions	X	X		X	X	D O A	CC61	IV	XXVI
DCCA0	PAM Dual Interface		X			X	D S A	CCA0	IV	XXVI
DD6A2	DAR and DAR Mask Register		X			X	O	D6A2	V	XXVI
DD8A0–00	Configuration Control, Control		X			X	S A	D8A0	V	XXVI
DD8A0–01	Overlay		X			X		D8A0	V	XXVI
DD9A0	ATR		X			X	O S A	D9A0	V	XXVII
DDAA0	SSU Multi–Element Test		X		X	X	S	DAA0	V	XXVII
DDDA1	IOCE Processor Test, CE Control		X			X	M O S	DDA1	V	XXVII
DDDA2	IOCE Processor Test, IOCE Control	X					M	DDA1	V	XXVII
DE0A3	SEVA Control Section		X			X	S	E0A3	V	XXVII

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
DE0B2	SEVA SE Random		X			X	M	E0B2	V	XXVII
DE0B6	SEVA 1052		X			X	M S A	E0B6	V	XXVII
DE0B8	SEVA Card Reader–Punch		X			X	M A	E0B8	V	XXVII
DE0C1	SEVA CE Super Scramble		X			X	M S	E0C1	V	XXVIII
DE0C3	SEVA Read/Write Direct Data		X			X	M A	E0C3	V	XXVIII
DE0C5	SEVA ELC Generate and Receive		X			X	M	E0C5	V	XXVIII
DE0C7	SEVA Acceptance Automatic Reconfig Demonstration		X			X	M O A	E0C7	V	XXVIII
DE0C8	SEVA Channel–to–Channel Adapter		X			X	M S	E0C8	V	XXVIII
DE0C9	SEVA CE Random		X			X	M	E0C9	V	XXVIII
DE1B3	SEVA PAM 1		X			X	D M A	E1B3	V	XXVIII
DE1B5	SEVA IOCE Processor 1		X			X	M	E1B5	V	XXVIII
DE1C4	SEVA Sel Chan, TCU 1, and Tapes		X			X	M S A	E1C4	V	XXVIII
DE1C6	SEVA RCU and DAU (IOCE 1)					X	E M A	E1C6	V	XXIX
DE1C7	SEVA Printer 1		X			X	M A	E1C7	V	XXIX
DE1CA	SEVA DE 1		X			X	M	E1CA	V	XXIX
DE1CC	SEVA DASF 1		X			X	D M S A	E1CC	V	XXIX
DE2B3	SEVA PAM 2		X			X	D M A	E1B3	V	XXIX

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	Monitor MDM–D/E	System Model Only Multiprogram Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
DE2B5	SEVA IOCE Processor 2		X			X	M	E1B5	V	XXIX
DE2C4	SEVA Sel Chan, TCU 2, and Tapes		X			X	M S A	E1C4	V	XXIX
DE2C6	SEVA RCU and DAU (IOCE 2)					X	E M A	E1C6	V	XXIX
DE2C7	SEVA Printer 2		X			X	M A	E1C7	V	XXIX
DE2CA	SEVA DE 2		X			X	E M A	E1CA	V	XXIX
DE2CC	SEVA DASF 2		X			X	D M S A	E1CC	V	XXIX
DE3B3	SEVA PAM 3		X			X	D M A	E1B3	V	XXIX
DE3B5	SEVA IOCE Processor 3		X			X	D M	E1B5	V	XXX
DE3C4	SEVA Sel Chan, TCU 3, and Tapes		X			X	D M S A	E1C4	V	XXX
DE3CA	SEVA DE 3		X			X	E M A	E1CA	V	XXX
DE3CC	SEVA DASF 3		X			X	D M S A	E1CC	V	XXX
DE4CA	SEVA DE 4		X			X	E M A	E1CA	V	XXX
DE5CA	SEVA DE 5		X			X	E M A	E1CA	V	XXX
DF0A1	Safe Store Tests (Acceptance Only)		X					F0A1	V	XXX
DF0B0–00	Computing Time Adjustment Factor (Acceptance Only)		X			X	M	F0B0	V	XXX
DF0B0–01	Time Sample Problem 1		X			X		F0B0	V	XXX
DF0B0–02	Time Sample Problem 2		X			X		F0B0	V	XXX

INDEX OF MAINTENANCE DIAGNOSTIC PROGRAMS (Continued)

Identity PPPSSSAA 12312r12	Name	CPU IOCE	CPU CE	Monitor IDM	Monitor SDM	MDM–D/E	System Model Only Multi–program Op Intervention Section Sense Sw Additional Units	Description Ref	Description Vol	Listing Vol
DF0B0–03	Time Sample Problem 3		X			X		F0B0	V	XXX
DF0B0–04	Time Sample Problem 4		X			X		F0B0	V	XXX
DF0B0–05	Time Sample Problem 5		X			X		F0B0	V	XXX
DF0B0–06	Time Sample Problem 6		X			X		F0B0	V	XXX
DF0B0–07	Time Sample Problem 7		X			X		F0B0	V	XXX
DF0B0–08	Time Sample Problem 8		X			X		F0B0	V	XXX
DF0C0	Display Instr Performance Test (Acceptance Only)		X			X	E A	F0C0	V	XXX
DFFFF	Dummy Section	X	X		X	X		DMMM	I	None

BASIC COMPUTING ELEMENT TEST (D1101–D1103)

1.0 PURPOSE

Basic Computing Element Test performs a functional and diagnostic test of the System/360 standard instructions (with the exception of the HIO, RDD, and WRD instructions) not tested by Hardcore, D0040. Basic CE Test is an extension of Hardcore and uses the same CAS (Control Automated System) building–block approach. No instruction is used as part of a test until it has been tested. Errors are indicated by messages under the control of the diagnostic monitor.

Basic CE Test consists of three sections:

D1101 tests RR, RX and SI instructions not tested by Hardcore.

D1102 tests SS–type and Decimal instructions.

D1103 tests floating–point instructions, the Execute instruction, floating–point register interaction, and special protection interruptions.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections are loaded by and run under the control of SDM or MDM–D/E. The DM must be loaded via a CE.

2.2 EQUIPMENT

These sections require a 9020D or 9020E System. Only those units required by DM are needed to run these sections.

3.0 OPERATING PROCEDURES

3.1 LOADING

Standard DM loading procedures are used. It is recommended that the CHECK CONTROL switch be in the PROC position.

3.2 OPERATION

The following section sense switches are available:

Bit	State	Meaning
0	0	Bypass Scope Loop
	1	Scope Loop

Bit 0 is tested when an error occurs during testing or when bit 6 is found set to 1. When bit 0 is found set to 1, the routine is cycled, error printing is inhibited, and PMT subroutine is bypassed.

1	0	Perform PMT
	1	Bypass PMT

Bit 1 is tested when bit 0 is set to 0 and either an error occurs or bit 6 is found set to 1. If bit 1 is set to 1, the PMT subroutine is bypassed. If bit 1 is set to 0, the PMT subroutine is entered for each test.

2	0	Print Short PMT Format
	1	Print Long PMT Format

See heading 4.0.

3	0	Bypass Lock on Error
	1	Lock on Error

Bit 3 is tested under the same conditions as bit 1. If bit 3 is set to 1, the routine being performed is cycled, printing is enabled, and PMT subroutine is performed.

5	0	Intermittent Mode
	1	Single Trace

If bit 5 is set to 0, PMT successively tests each ROS microword 2000 times, printing the first logout and any differing logout of each microword tested. If bit 5 is set to 1, PMT tests each ROS microword once, printing the logout of each microword.

6	0	Normal Mode
	1	Force PMT

Bit 6 is checked when a test is successful. If bit 6 is set to 0 and not in the scope loop, the next test is performed. If bit 6 is set to 1, section sense switch 0, 1, 2, 3, and 5 are interrogated as if an error had occurred.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Standard DM termination procedures are used.

4.0 PRINTOUTS

Printouts consist of error messages followed by a microtrace of the instruction. The list of error messages are too numerous for all to be shown here, but they may be obtained by running the sections with section sense switch 6, force PMT, set to 1. Figure 4–1 is an example of one printout obtained by that means. When setting 6 to 1, however, the REC (received) and EXP (expected) results that are printed are not valid and should be ignored.

```
*  SD0 D11010 02 10ADDA
 LOC 10E172     REC RESULTS          00 00 00 00
                EXP. RESULTS         00 00 00 00
                INST WAS             48 30 F 210
                SUBTRACT HALF-WORD INSTRUCTION FAILED
*  MICROTRACE STARTING *
     ROSAR          Q REG          R     E     IC      D       S        T        STC  A         B         ABC  WORK REG  F  STAT TRG
21B  5CD  838  F21C9200F00F47E0  4B30  9208  10E15E  10A00F  0010B162 0010E108 7    0010A00F  00000008  7    0010E14E  01
10B  21B  5CD  F21C9200F00F47E0  4B30  4B30  10E15E  10A00F  0010E162 0010A000 7    0010A00F  00000008  7    0010208A  01
680  108  21B  F21C9200F00F47E0  9200  4B30  10E15A  10A21C  7FFF8000 7FFF8000 0    0010A00F  00000008  0    0010208A  01
681  680  10B  F21C9200F00F47E0  9200  4B30  10E15A  10A21C  7FFF8000 7FFF8000 0    0010A00F  7FFF8000  0    0010208A  01
682  681  680  F21C9200F00F47E0  9200  4B30  10E15A  10A21C  7FFF8000 7FFF8000 0    FFFFFF00  7FFF8000  0    0010208A  01
684  682  681  F21C9200F00F47E0  9200  4B30  10E15A  10A21C  7FFF8000 80000000 0    FFFFF000  7FFF8000  0    0010208A  01
198  684  682  F21C9200F00F47E0  9200  4B30  10E15A  10A21C  7FFF8000 80000000 0    FFFF0000  7FFF8000  0    0010208A  01
490  19B  684  F21C9200F00F47E0  9200  4B30  10E15A  10A21C  7FFF8000 FFFF8000 0    FFFF0000  7FFF8000  0    0010208A  01
221  490  198  F21C9200F00F47E0  9200  4B30  10E15A  10A21C  7FFF8000 80000000 0    FFFF0000  7FFF8000  0    0010208A  01  B
034  221  490  F21C9200F00F47E0  9200  9200  10E15A  10A21C  7FFF8000 0010A000 0    FFFF0000  7FFF8000  0    0010208A  01  B
*  MICROTRACE COMPLETED *
```

FIGURE 4–1. PRINTOUTS

Line 1 contains the section identity (D11010) and the routine number (02). The address that follows is the location of the supervisor D0 call to the diagnostic monitor.

Line 2 displays the address of the print call within the test, followed by the results received from executing the test instruction.

Line 3 contains the results expected from executing the test instruction.

Line 4 contains the test instruction, printed in hex.

Line 5 is a brief description of the test instruction.

This is followed by a microtrace in the short PMT format.

5.0 COMMENTS

5.1 SUBROUTINES

PMT (Programmed Micro–Instruction Trace) subroutine attempts to isolate the failing machine cycle within the failing instruction. Entry into this subroutine initiates a microtrace of the failing instruction using the Diagnose instruction with a log–on–count. A message is printed that the PMT analysis has begun. The failing instruction is then progressively exercised for each of its machine cycles and all pertinent data is printed for each cycle. An asterisk will identify the reception of a machine check.

The PMT subroutine is bypassed if the Basic CE Test sections are running in multiprogramming or multiprocessing mode or if DM sense switch 27, inhibit all printing, is set to 1. A single, solid failure is assumed. However, RTLP (Routine Looper) subroutine normally cycles each routine a number of times before proceeding to the next test, to detect possible intermittent failures.

5.2 ROUTINES

The routines test all the CAS blocks for each instruction. Every CAS block that is tested for the first time is shown in the upper right–hand corner of the listings as an aid to the operator. The results of the instruction being tested are predetermined. The instruction is tested for a wrong result or a machine check. If a machine check occurs while the instruction other than the one being tested, the diagnostic monitor returns control to the section and the TMCK subroutine prints an error message and the logout.

5.2.1 Section 1

The following instructions are tested in section 1:

AH	ALR	XI	SLDA
SH	SLR	TS	M
C	BXH	SPM	MR
CLR	BXLE	SRA	MH
LPR	SL	SRDL	D
LTR	AL	SDRA	DR
LNR	XR	SLA	CVD
LCR	X	SLDL	CVB

5.2.2 Section 2

The following instructions are tested in section 2:

MVC	MVZ	PACK	SP
NC	MVN	UNPK	CP
XC	TR	ED	ZAP
OC	TRT	EDMK	MP
CLC	MVO	AP	DP

5.2.3 Section 3

The following instructions and operations are tested in section 3:

STD	SW		DD
LD	MDR	LTER	DE
FPR Interaction	MD	LCER	EX
	LE	AER	Special Protection
HER	ME	AE	Interruptions
HDR	MER	AUR	
ADR	LDR	AU	
AD	LER	CER	
AWR	LPDR	CE	
AW	LNDR	SER	
CDR	LTDR	SE	
CD	LCDR	SUR	
SDR	LPER	SU	
SD	LNER	STE	
SWR		DDR	
		DER	

FLOATING POINT DIVIDE TESTS WITH PMT (D1106)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each of the four floating divide instructions DE, DD, DDR and DER.

1.2 MODIFICATIONS

This CE program differs from D1106 in that it includes Program Micro Trace (PMT), Program interrupt and Machine Check handlers, Condition Code tests and underflow tests with program interrupts allowed plus overflow tests.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under SDM or MDM D/E

2.2 EQUIPMENT

This section requires a 9020 Simplex consisting of a CE, IOCE and SE plus I/O devices for program loading and communication. The CE must be in state Ø in order to run PMT. If sense switch 1 is set (bypass PMT) then the CE can be in any state.

3.0 OPERATING PROCEDURES

3.2 LOADING

Refer to the 9020 System Maintenance Monitor Manual FAA 2000 for loading procedures.

3.2 OPERATION

The following section sense switches are available:-

BIT	STATE	MEANING
Ø	Ø	Run from SE
	1	Run from DE
1	Ø	Perform PMT
	1	Bypass PMT
2	Ø	Short PMT format
	1	Long PMT format
4	Ø	Trace Instruction at Address C
	1	Trace instructions at address B thru C
5	Ø	Intermittent mode
	1	Not Intermittent mode
18	Ø	Normal run
	1	Force error print

3.3 HALTS OR WAITS

None

3.4 TERMINATION

Standard DM termination procedures are used.

3.5 RUN TIME

Run times depend on sense switch settings and the amount of printing, some sample times are as follows:-

No sense switches set and no error printout - less than 10 seconds.
Sense switch 1 (Bypass PMT) and 18 (Force error print) set - approximately 1.5 minutes.
Sense switch 5 (Not intermittent mode) and 18 (Force error print) set - approximately 18 minutes.
Sense switch 2 (Long PMT format), 5 (Not intermittent mode) and 18 (Force error print) set - approximately 2 hours 20 minutes.
Sense switch 2 (Long PMT format) and 18 Force error print) set - approximately 24 hours.

3.6 RUN MODE

If an attempt is being made to trace an intermittent CE fault the section could be cycled with the CE in state Ø and no section sense switches set. Under these conditions the program will run continuously and no printing will result unless an error occurs. Following an error the expected and actual results will be printed and PMT will be called. Unless the error re-occurs PMT will not show any discrepancies and also the conditions leading up to the error will be lost.

An alternative method would be to run the section with sense switches 2 and 18 set. The section would then print the results of all tests and run PMT in intermittent mode using long format printout. If an error does occur the data will be available for events both preceding and following the error. The amount of printout in this mode is considerable (around 800 pages) but it is spread over a period of 24 hours and thus is at the fairly low rate of 33 pages per hour.

4.0 PRINTOUTS

Since this section can output a considerable amount of printout (up to approximately 800 pages) it is recommended that a HSP is added and initialised as the secondary output device.

Appendices A, B and C show sample program outputs as a result of different sense switch settings:-

Appendix A shows part of a run with sense switches 1(bypass PMT) and 18 (force error print) set.

Appendix B shows part of a run with sense switches 2 (long PMT format), 5(not intermittent mode) and 18 (force error print) set.

Appendix C shows a similar run to that in appendix B but short format PMT has been specified by leaving sense switch 2 reset.

Appendix D shows a sample printout as a result of an expected program interrupt not being received. If a program interrupt occurs but has the wrong code then the printout is as shown in appendix E.

Appendix E shows sample printouts of unexpected program interrupts and machine checks, note that in the case of machine checks within the test instruction a PMT format printout occurs with long format forced. If a machine check occurs outside the test instruction output is in the usual logout format. If an unexpected machine check occurs while an instruction is being micro-traced an asterisk is placed at the beginning of the line in the PMT printout.

5.0 COMMENTS

5.1 PROGRAM MICRO TRACE

PMT attempts to isolate the failing machine cycle within the failing instructions. Entry into this subroutine initiates a micro-trace of the failing instruction using the Diagnose instruction with a log-on-count. A message is printed indicating that the PMT analysis has started. The failing instruction is then progressively exercised for each of its machine cycles and all pertinent data is printed for each cycle. Refer to FAA 2000 for a full description of PMT.

5.2 TEST ROUTINES

All tests verify:-

a) The actual result of the divide is same as the expected result.

b) The condition code remains unchanged.

c) No unexpected program interrupts.

d) No machine checks.

Some tests also verify:-

a) Floating point registers not used in the divide instruction remain unchanged.

b) Expected program interrupts occur

c) The divide can take place from any valid address boundary.

Failure to pass all of these checks, or if sense switch 18 is set, results in the appropriate error printout. After the printout PMT is called to micro-trace the failing instruction.

APPENDIX A

```
L11C6/SS.1.18/B/
START   D11060
* D11C60 01 2935E2 3
  EXPECTED RESULTS 41400000 00000000
  ACTUAL   RESULTS 414CC000 CCC00C00
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN CCCO
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 0 RECEIVED,EXPECTED 0
* D11060 02 29364C 3
  EXPECTED RESULTS 41400000 00000000
  ACTUAL   RESULTS 414CC000 CCC00C00
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 0010
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 1 RECEIVED,EXPECTED 1
* D11060 03 2936AE 3
  EXPECTED RESULTS 414CC000 00000000
  ACTUAL   RESULTS 41400000 00000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 0100
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 2 RECEIVED,EXPECTED 2
* D11060 04 293710 3
  EXPECTED RESULTS 414CC000 C0000000
  ACTUAL   RESULTS 414CC000 00000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 1110
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 3 RECEIVED,EXPECTED 3
* D11060 05 293772 3
  EXPECTED RESULTS 41400000 00000000
  ACTUAL   RESULTS 414CC000 00000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 1000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 0 RECEIVED,EXPECTED 0
* D11060 06 2937D4 3
  EXPECTED RESULTS 41400000 00000000
  ACTUAL   RESULTS 414CC000 00000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 1010
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 1 RECEIVED,EXPECTED 1
* D11C60 07 293836 3
  EXPECTED RESULTS 41400000 00000000
  ACTUAL   RESULTS 41400000 00000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 1100
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 2 RECEIVED,EXPECTED 2
* D11C60 08 293898 3
  EXPECTED RESULTS 41400000 00000000
  ACTUAL   RESULTS 41400000 00000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 0110
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 3 RECEIVED,EXPECTED 3
* D11C6C 09 2938FC 3
  EXPECTED RESULTS 45671000 00000000
  ACTUAL   RESULTS 45671000 00000000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 0 RECEIVED,EXPECTED 0
```

APPENDIX B

```
  LI.../SS.18.2.5/B/
START   D11060
* D11060 01 2935E2 3
  EXPECTED RESULTS 414CCCOO COOOOOOO
  ACTUAL   RESULTS 414CCCOO OOOOOOOO
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 0000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 0 RECEIVED,EXPECTED 0
  * MICROTRACE STARTING *
   RSR PSR       LM           N    E    IC     D       S       T    STC   A       B    ABC   X       ATR       Y     F STT
   200 490 OOOOOOOOOO1ECOOO C000 9100 2935C8 2935BC 9228F00F 0000F5BC 4 002935BC OOOOOOOO 7 20000000 0000067000 00000000 00 01
   A51E1FFF FF7E4FFF 3ECCORFF 07AF1FFF 003F8400 OCOOOCOO CCCCC67C C2CCCCCC C0551ECC 480C0C00 60000000 005F8040
   C03CCCC6 COC40704 002935BC OOOOOOOO 6BA800F0 38060201 08100105 002935C8 3D269100 002935BC 3D269200 F00F0510
   CCOOOOOO OOOOOCOO B03CAAFF CC2935CC CCCCCOOO OOOOOCOO OOOOOOOO 00021000 00000000 0010010A 00000000 0080EBE0
   FDFFFFFF 40I28438 F7FECCCO 11100F03 00281AB2 OCOOOCCC CCCCCCCO C01ECCCC 2CCCCCCC CCCOOCOO 9228F00F 0000F5BC
  GPRO-7 OOCCOOOO OCCCCOOO OOOOOOOO 002935EA 00000000 00000000 00000000 00000000
  GPR8-15 00000000 00CCCOOO OC296C00 CC295CCO 9F2935F0 00297000 00294000 4F293000
  FPRO- 7 00000000 00000000 41800000 00000000 41400000 CCCCCCCO 412CCCCC CCCCCCCC
   RSR PSR       LM           N    E    IC     D       S       T    STC   A       B    ABC   X       ATR       Y     F STT
   1BD 200 OOOOOOOOOO1EOOOO OCOO 3D26 2935C8 2935BC 9228F00F 41800000 4 002935BC 00000000 7 20000000 0000067000 00000000 00 01
   A71E1FFF FF7B4FFF 3E000RFF 07AF0FFF 003F8400 00C00000 00000C70 C2CCCCCC C0551ECC 480CC000 60000C00 005F8040
   CC3CCCC6 CCC4C7C4 CC2935BC 00000000 6BA800F0 38060201 08100105 002935C8 3D263D26 002935BC 3D269200 F00F0510
   CCCCOCOO 00000000 B03CAAFF C02935C0 CCCCCOOO 80000000 00000000 00020E00 00000000 500C3338 00000000 01DE7431
   FDFFFFFF 37528100 F7FE0000 44100F93 00281AB2 OOCOOCCO OOCOCOOO 001E0000 2CCCCCCC CCCCOCOO 9228F00F 41800000
  GPRO-7 CCCCCCCC CCCCCCOO CCOOOOOO 002935EA C0000000 00000000 00000000 00000000
  GPR8-15 OOCCCOOO CCCCCOOO OC296C00 CC295CCO 9F2935F0 00297000 00294000 4F293000
  FPRO- 7 00000000 00000000 41800000 OC000000 41400000 00000000 41200000 00000000
   RSR PSR       LM           N    E    IC     D       S       T    STC   A       B    ABC   X       ATR       Y     F STT
   CC9 1BD CCOOOOCCCO1ECOOO 0000 3D26 2935CA 800000 41200000 41200000 4 41800000 41800000 0 20000000 0000067000 00000000 00 00
   B51E1FFF FFBB4FFF 3E000RFF 07BB4FFF 003F8400 OOCOOCOO 00000670 00000000 00551E00 480C0000 60000000 005F8040
   CC3CCCC6 CCC4CC04 418C0CC0 41800000 6BA800F0 38060201 C81CC1C5 CC2935CA 92CC3D26 C0800000 3D269200 F00F0510
   COCCOCCO OCCOOCCO B03CABFF 002935C0 00000000 80000000 0D000000 76001E00 00000000 0006BE08 00000000 001F80C0
   FDFFFFFF 194800BD F7FECCCO 12000FB3 00281AB2 OCCOOCCO C0000C000 001E0000 20000000 00000000 41200000 41200000
  GPRO- 7 CCCCCCCC CCCCCCCO 00000000 002935EA 0000000C CCCCCCCC CCCCCCCC CCCCCCCC
  GPR8-15 OCCCCOOO OCCCCOOO 00296000 00295000 9F2935F0 00297000 00294000 4F293000
  FPRO- 7 00000000 OCCCCOOO 41800CCC CCCCCCCO 41400000 00000000 41200000 00000000
   RSR PSR       LM           N    E    IC     D       S       T    STC   A       B    ABC   X       ATR       Y     F STT
   CC0 0C9 OCC000CC001ECOOO 0000 3D26 2935CA 200000 41200000 41200000 4 41800000 41800000 0 20000000 0000067000 00000000 00 00
   B51E1FFF FFBB4FFF 3EC00RFF 07BB4FFF 003F8400 OCOOOOOO 00000670 00000000 00551E00 480C0000 60000000 005F8040
   CC300006 00C40004 41800CC0 41800000 6BA800F0 38060201 081CC1C5 CC2935CA 92CC3D26 CC2C0CC0 3D269200 F00F0510
   CCCCCCCC CCCCCCOO B03CABFF 002935C0 00000000 00000000 00000000 38030000 00000000 000601D8 00000000 000980E0
   FDFFFFFF 1806E8C9 F7FE0CC0 27180FC3 C0281AB2 OCOOOCOO 00000000 001E0000 20000000 00000000 41200000 41200000
  GPRO- 7 00000000 00000000 00000000 002935EA C0000000 OCCCCCCO CCCCCCCC CCCCCCCC
  GPR8-15 CCCCCCCC CCCCCCOO 00296000 00295000 9F2935F0 00297000 00294000 4F293000
  FPRO- 7 00000000 OCOCCOOO 4180CCCC CCCCCCCO 41400000 00000000 41200000 00000000
   RSR PSR       LM           N    E    IC     D       S       T    STC   A       B    ABC   X       ATR       Y     F STT
   3C7 CCC CCCCCCCCCC1ECOOC 0000 3D26 2935CA 2C0000 41200000 00000000 4 41800000 00000000 0 20000000 0000067000 00000000 C0 00
   B11E1FFF FFBF4FFF 3ECCORFF 07BF4FFF C03F8400 00C00000 00000670 00000000 00551E00 480C0000 60000000 005F8040
   00300006 00C40004 41800000 00000000 6BA800F0 38060201 0810C105 002935CA 92003D26 C0200000 3D269200 F00F0510
   CCCCCCCO CCCCCCCO B03CABFF 002935C0 000C0000 40C06CC0 CCCCCCCC CC00CC00 00000000 001E420A 00000000 02004360
   FDFFFFFF 78C3C0C9 F7FE0000 44024F03 00281AB2 COC00000 00000000 001E0000 20000000 00000000 41200000 00000000
  GPRO-7 00000000 00000000 00000000 002935EA 00000CCO CCCOCCCO 00000000 00000000
  GPR8-15 CCCCCCCC CCCCCCOO 00296000 00295000 9F2935F0 C0297CC0 CC294CC0 4F293CCC
  FPRO- 7 OCCCCOOO CCCCCOOO 41800000 00000000 41400000 00000000 41200000 00000000
   RSR PSR       LM           N    E    IC     D       S       T    STC   A       B    ABC   X       ATR       Y     F STT
   14F 3C7 CCCCCCCCCC1ECOOO 0000 3D26 2935CA 200000 412CCCCC CCCCCCCC C CC6CCCCC CCCCCC00 0 20000000 0000067000 00000000 C0 00
   B51E1FFF FFBF4FFF 3EC00FFF 07FF4FFF 003F8400 00000000 00000670 00000000 00551E00 480C0000 60000000 005F8040
   00300006 00C40000 006C0CC0 COCCCCC0 6BA8C0FC 38060201 08100105 002935CA 92003D26 C0200000 3D269200 F00F0510
   C0000000 00000000 B03CABFF 002935C0 000C0000 00000C00 CCCCCCCC 5CC1CCCC CCCCCCCC C00AC3B2 CC000C00 001DA2A0
```

```
  L11C   .5.18/B/
START   D11060
* D11060 01 2935E2 3
  EXPECTED RESULTS 41400000 00000000
  ACTUAL   RESULTS 414CC000 CC000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 0000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE C RECEIVED,EXPECTED 0
  * MICROTRACE STARTING *
   RSR PSR       LM              N    E    IC     D       S       T       STC  A       B       ABC  X       ATR       Y       F STT
   200 490 CCCCCCCCC01EC000 0000 91C0 2935C8 2935BC 9228F00F 0000F5BC 4 002935BC 00000000 7 20000000 0000067000 00000000 00 01
   1BD 200 000000000001E0000 0000 3D26 2935C8 2935BC 9228F00F 41800000 4 002935BC 00000000 7 20000000 0000067000 00000000 00 01
   CC9 1BD CCCCCCCCCC1ECC00 0000 3D26 2935CA 800000 412CCCCC 412CCCCC 4 41800000 41800000 0 20000000 0000067000 00000000 00 00
   CC0 0C9 CCCCCCCCC01EC000 C000 3D26 2935CA 2C0000 41200000 41200000 4 41800000 41800000 0 20000000 0000067000 00000000 00 00
   3C7 0C0 000000C0001E0000 0000 3D26 2935CA 2C0000 412C0000 00000000 4 41800000 00000000 0 20000000 0000067000 00000000 C0 00
   14F 3C7 CCCCCCCCCC1ECCC0 0000 3D26 2935CA 2C0000 412CCCCC CCCCCCCC C CC6CCCCC CCCC0000 0 20000000 0000067000 00000000 C0 00
   788 14F 0CCCCCCCCC1EC000 C000 3D25 2935CA 200000 40200000 00000000 0 00600000 00000000 0 20000000 0000067000 00000000 40 00
   24C 788 000000C0D01EC000 CCC0 3D25 2935CA 200000 412C0000 00000000 0 00080000 00000000 0 20000000 0000067000 00000000 41 00
   9C9 24C CCCCCCCCCC1ECCC0 0000 3D25 2935CA 2C0000 412CCCCC CCCCCCCC 1 CFECCCCC CCCCCCC0 1 20000000 0000067000 00000000 41 00
   CCD 9C9 CCCCCCCCC01EC000 0000 3D25 2935CA 200000 41200000 00000000 1 00000000 00000000 1 20000000 0000067000 00000000 00 00
   9C9 0CD 000000C0001EC000 CCC0 3D26 2935CA 200000 41200000 C0000000 1 0FC00000 00000000 1 20000000 0000067000 00000000 40 00
   CCD 9C9 000000000001EC000 0000 3D26 2935CA 200000 412CCCCC CCCCCCCC 1 CFECCCCC CCCCCCC0 2 2C000000 0000067000 00000000 40 00
   9C9 0CD CCCCCCCCC01EC000 0000 3D27 2935CA 200000 41200000 00000000 1 0FC00000 00000000 2 20000000 0000067000 00000000 40 00
   0CC 9C9 000000000001E0000 CCC0 3D27 2935CA 2C0000 41200000 00000000 1 0FE00000 00000000 3 20000000 0000067000 00000000 40 00
   0CF 0CC 000000000001E0000 0000 3D28 2935CA 2C0000 412CCCCC CCCCCCCC 1 CFCCCCCC CCCCCCC0 3 2C000000 0000067000 00000000 40 00
   83E CCF CCCCCCCC001EC000 0000 3D28 2935CA 200000 41200000 00000000 1 0FE00000 00000000 0 20000000 0000067000 00000000 40 00
   9C9 83E 0000000C001EC000 CCC0 3D29 2935CA 2C0000 41400000 00000000 2 0FC00000 00000000 0 20000000 0000067000 00000000 40 00
   0CD 9C9 000000000001E0000 0000 3D29 2935CA 2C0000 414CCCCC CCCCCCCC 2 0FECCCCC CCCCCCC0 1 2C000000 0000067000 00000000 00 00
   5C9 CCD CCCCCCCCCC1ECC00 0000 3D2A 2935CA 200000 41400000 00000000 2 0FC00000 00000000 1 20000000 0000067000 00000000 00 00
   0CD 9C9 000000C0001EC000 CCC0 3D2A 2935CA 2C0000 41400000 00000000 2 0FE00000 00000000 2 20000000 0000067000 00000000 00 00
   9C9 0CD 000000000001E0000 0000 3D2B 2935CA 2C0000 41400000 00000000 2 0FCCCCCC CCCCCCC0 2 2C000000 0000067000 00000000 00 00
   CCC 9C9 CCCCCCCCCC1ECC00 0000 3D2B 2935CA 200000 41400000 00000000 2 0FE00000 00000000 3 20000000 0000067000 00000000 00 00
   0CF 0CC CCCCC0C0001ECC00 C000 3D2C 2935CA 2C0000 41400000 00000000 2 0FC00000 00000000 3 20000000 0000067000 00000000 00 00
   83E 0CF 000000000001E0000 0000 3D2C 2935CA 2C0000 41400000 00000000 2 0FE00000 0CCCCCC0 0 2C000000 0000067000 00000000 00 00
   5C9 83E CCCCCCCCCC1ECCC0 C000 3D2D 2935CA 2C0000 41400000 00000000 3 0FC00000 00000000 0 20000000 0000067000 00000000 00 00
   0CD 9C9 0CCCCCCCC01EC000 0000 3D2D 2935CA 2C0000 41400000 00000000 3 0FE00000 00000000 1 20000000 0000067000 00000000 00 00
   9C9 0CD 000000000001E0000 0000 3D2E 2935CA 2C0000 414CC000 00000000 3 0FC00000 00000000 1 20000000 0000067000 00000000 00 00
   CCD 9C9 CCCCCCCCCC1ECCC0 0000 3D2E 2935CA 2C0000 414CCCCC CCCCCCCC 3 0FE00000 00000000 2 20000000 0000067000 00000000 00 00
   9C9 0CD CCCCCCCCC01ECC00 C000 3D2F 2935CA 2C0000 41400000 00000000 3 0FC00000 00000000 2 20000000 0000067000 00000000 00 00
   0CC 9C9 000000000001E0000 0000 3D2F 2935CA 2C0000 414CC000 00000000 3 0FE00000 00000000 3 20000000 0000067000 00000000 00 00
   CCE CCC CCCCCCCCCC1ECCC0 0000 3D20 2935CA 2C0000 414CCCCC CCCCCCCC 3 CFCCCCCC CCCC0000 3 20000000 0000067000 00000000 00 00
   781 0CE 0CCCCCCCCC01EC000 0000 3D20 2935CA 200000 41400000 00000000 3 0FE00000 00000000 0 20000000 0000067000 00000000 00 00
   9A4 781 000000000001ECC00 CCC0 3D21 2935CA 2C0000 41400000 C0000000 0 0FC00000 00000000 0 20000000 0000067000 00000000 00 00
   221 9A4 CCCCCCCCCC1ECCC0 0000 3D21 2935CA 2C0000 414CCCCC 414CCCCC C CFCCCCCC CCCCCCC0 0 20000000 0000067000 00000000 00 00
   C34 221 0CCCCCCCCC1EC000 C000 9200 2935CA 200000 41400000 00293000 0 0FC00000 00000000 0 20000000 0000067000 00000000 00 00
  * MICROTRACE COMPLETED *
* D11060 02 29364C 3
  EXPECTED RESULTS 414CC000 00000000
  ACTUAL   RESULTS 414CC00C CCC00CC0
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN C010
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 1 RECEIVED,EXPECTED 1
  * MICROTRACE STARTING *
   RSR PSR       LM              N    E    IC     D       S       T       STC  A       B       ABC  X       ATR       Y       F STT
   201 725 000000000001E0000 0000 4700 293632 000000 00000000 00000000 0 CC293622 CCCCC0F0 0 20000000 0000067000 00000000 A0 00
   1BD 2C1 CCCCCCCCCC1ECCC0 0000 3D26 293632 000000 00000000 41800000 0 00293622 000000F0 0 20000000 0000067000 00000000 A0 00
   CC9 1BD CCCC0CCCC01EC000 CCC0 3D26 293634 800000 41200000 41200000 4 41800000 41800000 0 20000000 0000067000 00000000 A0 00
   CC0 0C9 000000000001E0000 0000 3D26 293634 200000 412C0000 41200000 4 41800000 4180CC00 0 2C000000 0000067000 00000000 00 00
   3C7 0CC CCCCCCCCCC1ECCC0 0000 3D26 293634 2000CC 412CCCC0 00000000 4 41800000 00C00000 0 20000000 0000067000 00000000 C0 00
```

APPENDIX C

APPENDIX D

```
START   D11060
  D11060 21 293DFA 3
  EXPECTED PROGRAM INTERRUPT CODE 00D DID NOT OCCUR
* D11060 21 293E2A 3
  EXPECTED RESULTS 618BA2E8 00000000
  ACTUAL   RESULTS 00000000 00000000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 3 RECEIVED,EXPECTED 3
  D11060 22 293EEE 3
  EXPECTED PROGRAM INTERRUPT CODE 00D DID NOT OCCUR
* D11060 22 293F1E 3
  EXPECTED RESULTS D8A00000 00000000
  ACTUAL   RESULTS 00000000 00000000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 2 RECEIVED,EXPECTED 2
  D11060 34 2945F8 3
  EXPECTED PROGRAM INTERRUPT CODE 00C DID NOT OCCUR
* D11060 34 294628 3
  EXPECTED RESULTS 3FEF0000 00000000
  ACTUAL   RESULTS 41EF0000 00000000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 0 RECEIVED,EXPECTED 0
  D11060 5E 295618 3
  EXPECTED PROGRAM INTERRUPT CODE 00C DID NOT OCCUR
* D11060 5E 295648 3
  EXPECTED RESULTS 33558000 00000000
  ACTUAL   RESULTS 41558000 00000000
  FLOATING POINT DIVIDE - OP CODE DDR
  CONDITION CODE 1 RECEIVED,EXPECTED 1
  D11060 7A 29646E 3
  EXPECTED PROGRAM INTERRUPT CODE 00C DID NOT OCCUR
* D11060 7A 29649E 3
  EXPECTED RESULTS 41F0F0F0 00000000
  ACTUAL   RESULTS 43F0F0F0 00000000
  FLOATING POINT DIVIDE - OP CODE DE
  CONDITION CODE 2 RECEIVED,EXPECTED 2
  D11060 9E 29746E 3
  EXPECTED PROGRAM INTERRUPT CODE 00C DID NOT OCCUR
* D11060 9E 29749E 3
  EXPECTED RESULTS 41F00000 000000EF
  ACTUAL   RESULTS 43F00000 000000EF
  FLOATING POINT DIVIDE - OP CODE DD
  CONDITION CODE 3 RECEIVED,EXPECTED 3
T CE3  123      D11060
  EOJ  MDM JOB COMPLETE
```

APPENDIX E

```
START   D11060
* D11060 01 293388 3
  A PROGRAM INTERRUPT OCCURED WITHIN THE TEST INSTRUCTION
* PROGRAM OLD PSW FF55F0014F2935B2
* GPR 0-15,   AT TIME OF INTERRUPT
* 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
* 0CC00000 00000000 00000000 8E2933AC 4E293266 00293378 00294000 4E293000
* FPR 0-7,    AT TIME OF INTERRUPT
* 00000000 00000000 41800000 00000000 41400000 00000000 41200000 00000000
* D11060 01 2935D2 3
  EXPECTED RESULTS 41400000 00000000
  ACTUAL   RESULTS 41800000 00000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 0000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 0 RECEIVED,EXPECTED 0


START   D11060
* D11060 01 29349C 3
  A MACHINE CHECK OCCURED UNDER THE FOLLOWING CONDITIONS
   RSR PSR       LM            N    E    IC     D       S       T    STC  A        B    ABC  X        ATR       Y     F STT
   890 88C 22D14141641C4812 0000 9100 2935C8 2935C0 00000000 00000000 4 41800000 41800000 0 FFFFFFFF 00000670 00 FFFFFFFF 00 00
   B51E1FFF FFFF4FFF 3EC00FFF 07BB1FFF 003FAC00 00000000 00000670 0CC0C000 FF651ECC 481C0020 60000000 005FB840
   00300006 00C40004 41800000 41800000 6BA800F0 38060201 08100105 002935C8 3D269100 002935C0 3D269200 F00F0510
   C0C00000 00000000 B03CAAFF 002935C0 00000000 00000000 00000000 00001000 00000000 004401A8 00000000 00004000
   FBFFFFFF 1220346C 3FFE0CC0 80200F03 002953C0 00000000 22D14141 641C4812 FFFFFFFF FFFFFFFF 0CC0CC00 00000000
  GPR0- 7 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
  GPR8-15 802934AC 00000000 00296000 00295000 4F29329E 00299000 00298000 4F293000
  FPR0- 7 00000000 00000000 41800000 00000000 41400000 00000000 41200000 00000000
  D11060 01 29890C 3

* D11060 01 2935E2 3
  EXPECTED RESULTS 414CCCOC 0CC0C000
  ACTUAL   RESULTS 41800000 00000000
  THIS HAS BEEN AN I-FETCH FROM AN ADDRESS ENDING IN 0000
  FLOATING POINT DIVIDE - OP CODE DER
  CONDITION CODE 0 RECEIVED,EXPECTED 0
T CE3  123      D11C62
  EOJ  MDM JOB COMPLETE
```

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BASIC DIAGNOSE AND LOGOUT (D1108)

1.0 PURPOSE

This section tests the basic functions of the Diagnose instruction including Reset MCW, Log on Count, Scan–In, and Logout.

2.0 REQUIREMENTS

2.1 PROGRAM

This section must be loaded by and run under the control of SDM or MDM–D/E. The DM must be loaded via a CE.

2.2 EQUIPMENT

This relocatable section requires a 9020D or 9020E System in state zero. Only those units required by DM are needed to run this section.

3.0 OPERATING PROCEDURES

3.1 LOADING

Standard DM loading procedures are used.

3.2 OPERATION

Set section sense switch 0 to a 1 if looping on the first failing test (without printing) is desired.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Standard DM termination procedures are used.

4.0 PRINTOUTS

4.1 INFORMATION PRINTOUTS

None.

4.2 ERROR PRINTOUTS

* NO MACHINE CHECK INTERRUPT OCCURRED AT XXXXXX appears when an expected machine check interrupt fails to occur. The location in the routine where the machine check was expected is printed.

* ERROR – TESTING LOG ON COUNT – COUNT WAS XXX.
  DIAGNOSE WAS LOCATED AT XXXXXX.

After a Diagnose Log on Count was issued, a machine check prematurely occurred. The actual count is printed in addition to the location of the Diagnose instruction.

* XXXXXX FAILED TO LOGOUT CORRECTLY AFTER SCANNING IN indicates that the printed register, trigger, or counter failed to logout with expected results.

* EXPECTED XXXXXXX
  RECEIVED XXXXXXX
  COULD BE LOGOUT OR SCAN IN ERROR

The message indicates that the error occurred either from a scan–in or logout. Inspecting the expected and the received data will usually determine which was at fault.

* XXXXXXXX LOGGED OUT INCORRECTLY indicates that the ROS data register or the working register failed to logout correctly.

* NOW LOOPING ON ERROR is printed when section sense switch 0 is set to 1 and an error is detected.

* MACHINE CHECK OLD PSW INCORRECT is printed when an expected machine check interrupt occurs and the location at which the interrupt happened is not as expected.

* DIAGNOSE RESET MCW FAILED is self–explanatory.

* MCW BIT 20 DID NOT DISABLE TIMER, RTN TERMINATED is printed if, after executing a Diagnose Disable Interval Timer, the timer continued to step.

5.0 COMMENTS

5.1 ROUTINES

Routine 1 – Test Diagnose Reset MCW.

This routine checks the Diagnose Reset MCW to insure that this basic instruction can be properly executed and that no logout occurs.

Routine 2 – Test Diagnose Log on Count with Count of Zero.

This routine insures that Diagnose Log on Count with a zero count immediately causes machine check interruption.

Routine 3 – Test Diagnose Log on Count.

Various counts are moved in the MCW and a set of test instructions are executed on different boundary alignments in order to test the accuracy of Log on Count.

Routine 4 – Test Scan–In and Logout of ST Register and Counter.

A Diagnose Scan–In is issued and the ST register and ST counter are checked for expected values. Two different data patterns are scanned in and tested.

Routine 5 – Test Scan–In and Logout of AB Register and Counter.

A Diagnose Scan–In/Logout is issued and the AB register and AB counter are checked for expected results. Two different data patterns are scanned in and tested.

Routine 6 – Test Scan–In and Logout of Q–Register.

Two different data patterns are scanned into the Q–register and the logged out values are checked against expected results.

Routine 7 – Test Scan–In and Logout of IC and D–Register.

A Diagnose Scan–In/Logout is issued to check the IC and D–register. Two data patterns are tested.

Routine 8 – Test Scan–In and Logout of R–, E–, and F–Register and Status Triggers.

A Diagnose Scan–In/Logout is issued to check R, E, and F and the STAT triggers. Two passes are made with different data patterns and the logged out results are checked with expected results.

Routine 9 – Test Logout of Working Register.

A Diagnose Log on Count is issued to test proper logout of the working register. Two different counts are used to check desired results.

Routine 10 – Test Logout of ROSAR, PROSA, and PROSB Registers.

This routine tests the logout of the ROS address, previous ROS address A, and previous ROS address B registers. A Diagnose Log on Count is issued to ROS address 89A with counts from zero to four. The expected results are checked after each count to insure that the ROS address registers logged out properly.

Routine 11 – Test Logout of All ROS Data Bits.

A Diagnose Log on Count is issued to several ROS addresses for a combination of "one" bits to test logout of ROS Data Register "one" bits and then to ROS address F02 and F03 to test logout of ROS Data Register "zero" bits.

Routine 12 – Test Logout of Gate Control Triggers and I–Fetch Latches.

A Diagnose Log on Count is issued with the count from 1 to 225. A group of test instructions are performed and the logout results are accumulated in a work area. When all the counts have been performed, the I–Fetch latches and gate–control triggers are tested to insure they had been set and also logged out properly.

5.2 SUBROUTINES

No Machine Check Interrupt subroutine is entered when an expected Machine check interruption did not occur. An error message is printed and the routine is terminated unless a loop–on–error option is indicated by section sense switch 0.

Scan–In or Logout Error subroutine is entered when the expected results do not agree with actual results after a logout. An appropriate error message is printed and a return to the routine is made.

Interrogate Sense Switch Zero subroutine is branched to when an error is detected in a routine to determine whether the loop–on–error option is set.

Load Scan Buffers subroutine is entered by those routines that do a scan–in. The scan buffers are loaded and certain important registers are set.

Assure Timer Is Disabled subroutine issues a Diagnose Disable Timer to insure that the timer can be disabled. If not, those routines which require the timer to be off are terminated.

CPU ERROR AND DETECTION ANALYSIS PROGRAM (D1111–D1115)

1.0 PURPOSE

The CPU Error and Detection Analysis (CEDA) Program consists of five sections, D1111 thru D1115. CEDA detects and isolates intermittent CE failures. The isolation of solid failures, although secondary, is also achieved by this program. CEDA stringently exercises the machine using chains of instructions. When a failure is detected, CEDA attempts to isolate the failure by reducing the number of instructions in the chain to the minimum number required to sustain the failure. The Programmed Micro–Instruction Trace (PMT) subroutine is included in CEDA to enable error isolation down to a CAS block. The use of random data in conjunction with various instructions allows isolation of data–dependent intermittent failures. Interruptions are forced to assure that an intermittent interruption condition does not exist. CEDA uses and tests only the System/360 instructions. The multiple CE and display instructions are not used or tested in CEDA.

2.0 REQUIREMENTS

2.1 PROGRAM

CEDA is loaded and runs under the control of SDM or MDM–D/E. The diagnostic monitor must be loaded via CE.

2.2 EQUIPMENT

CEDA requires a 9020D or 9020E system. Only those units required by the DM are needed to run CEDA.

3.0 OPERATING PROCEDURES

3.1 LOADING

Standard DM loading procedures are used. Placing of the CHECK CONTROL switch in the PROC position is recommended.

3.2 OPERATION

The following section sense switch options are available:

Bit	State	Meaning
0	0	Bypass Scope Loop
	1	Scope Loop

Bit 0 is tested when an error occurs during testing. When bit 0 is found set to 1, the routine is cycled, error printing is inhibited, and PMT subroutine is bypassed.

1	0	Perform PMT
	1	Bypass PMT

Bit 1 is tested when bit 0 is set to 0 and an error occurs. If bit 1 is set to 1, the PMT subroutine is bypassed. If bit 1 is set to 0, the PMT subroutine is entered for each test.

2	0	Print Short PMT Format as shown in 4.2.3.
	1	Print Long PMT Format as shown in 4.2.4.

When a 'Machine Error' occurs, the Long PMT Format (Log–Out) will be printed, regardless of setting of sense switch 2.

3	0	Bypass Lock on Error
	1	Lock on Error

Bit 3 is tested under the same conditions as bit 1. If bit 3 is set to 1, the routine being performed is cycled, printing is enabled, and PMT subroutine is performed.

4	0	Microtrace Failing Instruction (Address C)
	1	Microtrace Failing Chain (Address B through C)

See heading 5.1.2.

5	0	Intermittent Mode
	1	Single Trace

If bit 5 is set to 0, PMT successively tests each ROS microword 2000 times, printing the first logout and any differing logout of each microword tested. If bit 5 is set to 1, PMT tests each ROS microword once, printing the logout of each microword.

Sense switch 3 (Lock on Error) as well as switch 0 (Scope loop), will loop the failing chain with the data that caused the failure; no new data will be generated unless a DM cycle routine option is used and section switches 0 and 3 are off.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Standard DM termination procedures are used.

4.0 PRINTOUTS

4.1 INFORMATION PRINTOUTS

None.

4.2 ERROR PRINTOUTS

4.2.1 Error Message

The following error message is an example of one type printed by CEDA:

```
*  SD0 D11150 14 00A6B8
   LOC 0120D2 TEST 514 FAILED. MULTIPLY DECIMAL INSTRUCTION (MP)
 STARTING CHAIN ANALYSIS TO ISOLATE FAILING INSTR.
 THE FAILING INSTRUCTION IS NUMBER 08 IN THE CHAIN
 STORAGE                REC RESULTS 00 00 00 00  00 00 00 00   00 00 00 04  54 08 0C 00  00 00 00 00  00 00
                        EXP RESULTS 00 00 00 00  00 00 00 00  00 00 00 04  54 08 0C 00  00 00 00 00  00 00
                        INST WAS          FC E6 D 128  D 108
```

FIGURE 4–1. ERROR MESSAGE

The first line contains the section identity (D11150) and routine number (14). The address that follows is the location of the supervisor D0 call to the diagnostic monitor.

The second line displays the address of the print call within the test followed by the test number that failed, with a brief description of the test.

The third line informs that the chain analysis subroutine is starting. The run time of this subroutine is variable. It may run several minutes before finding which instruction failed within the chain. The more intermittent the failure, the longer the run time.

The fourth line indicates which of the instructions within the chain failed. The instruction test chain normally contain 16 instructions.

The fifth line contains the actual (received) data generated by the hardware. The sixth line contains the expected data which may be fixed data patterns or generated from simulators using random data patterns.

The seventh line contains the actual instruction that failed, printed in hex.

4.2.2 Error Message

The following is an example of a printout in the third CEDA section:

```
*  SDO D11130 02 00F624
TEST 302 FAILED. UNPACK DECIMAL INSTRUCTION (UNPK)
THE FAILING INSTRUCTION IS NUMBER 01 IN THE CHAIN
INSTRUCTION WAS F38280048018


RECEIVED RESULTS      F0F0F0F0F9FCF7F906
EXPECTED RESULTS      F0F0F0F0F9FCF7F906

OPERAND 1 WAS         A398A5A68723560360

OPERAND 2 WAS         9C7960
```

FIGURE 4–2. ERROR MESSAGE

The first line contains the section identity (D11130) and routine number (02). The address that follows is the location of the supervisor D0 call to the diagnostic monitor.

The second line displays the test number that failed, with a brief description of the test.

The third line indicates which of the instructions within the chain failed. Instruction test chain normally contains 16 instructions.

The fourth line contains the actual instruction that failed, printed in hex.

The fifth line contains the actual result of executing the failing instruction. This is the contents of the operand 1 field after execution of the failing instruction.

The sixth line contains the expected results of executing the instruction that failed. This is derived by program simulating the instruction.

The seventh and eighth lines display the contents of operand 1 and operand 2 fields respectively, before execution of the failing instruction.

4.2.3 Short–Format Microtrace

The following is an example of a successful short–format microtrace for a Move Character (MVC) instruction:

```
STARTING INTERMITTENT MODE TRACK – 20 SECONDS PER PASS.
     ROSAR          Q REG          R    E    IC       D       S        T        STC  A         B         ABC  WORK REG  F STAT TRG
234  5CD  838  D207001000089200  D207 9208 08E020  08A00F  0008E032 0008E008  7   0008A00F  00000008  7    0008E018  01
209  234  5CD  D207001000089200  D207 D207 08E020  08A00F  0008E032 0008E032  7   0008A00F  00000008  7    0008E018  01  D
208  209  234  D207001000089200  D207 D207 08E026  000010  0008E032 0008E032  7   0008A00F  00000008  7    0008E016  01
22A  208  209  D207001000089200  9200 D207 08E020  000010  0008E032 0008E032  7   0008A00F  00000008  7    0008E016  01  D
22F  22A  208  D207001000089200  9200 D207 08E026  000010  0008E032 00000017  7   0008A00F  00000008  7    7FFFFAFE  01  D
3A6  22F  22A  F00F983600081935  9200 D207 08E026  000010  0008E032 00000017  7   0008A00F  00000008  7    0008E016  01  D
397  3A6  22F  F00F983600081935  9200 D207 08E026  000010  0008E032 00000017  7   0008A00F  00000008  7    7FFFFAFE  01  D
292  397  3A6  F00F983600081935  9200 D207 08E026  000010  0008E032 0008E02E  7   0008A00F  00000008  7    0008E02E  01
366  292  397  F00F983600081935  9200 D207 000008  000010  0008E032 00000008  0   0008A00F  00000008  0    0008E02E  01
3AA  3B6  292  F00F983600081935  9200 D207 000008  000010  FFFFFF80 FFFFFF7E  0   0008A00F  00000008  0    0008E02E  01
3AF  3AA  3B6  F00F983600081935  9200 D207 000008  000010  FFFFFF80 FFFFFF7E  0   0008A00F  00000008  0    0008E02E  01
62B  3AF  3AA  F00F983600081935  9200 D207 000008  000010  FFFFFF80 FFFFFF7E  0   0008A00F  00000008  0    0008E02E  01
6A8  62B  3AF  F00F983600081935  9200 D207 000008  000010  00000001 00000000  0   00000001  00000000  0    0008E02E  01
6A9  6A8  62B  F00F983600081935  9200 D2FF 000008  000010  00000001 00000000  0   00000001  00000000  0    0008E02E  01
8B1  6A9  6A8  F00F983600081935  9200 D2FF 000008  000010  00000001 00000000  0   00000001  00000000  0    0008E02E  01
010  8B1  6A9  F00F983600081935  9200 D2FF 000008  000010  00000001 0008E02E  0   00000001  00000000  0    0008E02E  01
223  010  8B1  F00F983600081935  9200 D2FF 08E02E  000010  00000001 0008E02E  0   00000001  00000000  0    0008E02E  01
092  223  010  F00F983600081935  9200 9200 08E02E  000010  00000001 0008A000  0   00000001  00000000  0    0008E02E  01
INTERMITTENT TRACE COMPLETE
* MICROTRACE COMPLETED *
```

FIGURE 4–3. SHORT–FORMAT MICROTRACE

The first line is a notification that the PMT subroutine has started. A "pass" in this message is defined as the time it takes the PMT subroutine to cycle on repetitive diagnose–controlled logouts for each machine cycle of a failing instruction within the chain. The PMT subroutine is checking for discrepancies within the logout of each machine cycle. Any discrepancies found between repetitive logouts of the same machine cycle will be printed in the main body of trace. The time per pass depends on two factors: the number of times PMT tries each block looking for an intermittent error and the instruciton sequence being traced (addresses A, B, and C). If intermittent mode is bypassed, the following message is printed "*MICRO TRACE STARTING*".

The second line is the heading to define the fields (registers and triggers) of the instruction trace data.

The main body (trace) represents the summary of the PMT subroutine. This trace is formatted into fields that correspond to the registers of the machine.

The last line, "MICROTRACE COMPLETED", notifies that the PMT subroutine is complete. PMT subroutine returns to the test and loops the chain or proceeds, depending upon section sense switch 3.

The operator must decide what action should be taken if isolation could not be achieved. Normal program sequece if no action is taken by the operator, is to go to the next test. However, the operator may –

a. loop on the entire test with an input–message, DM cycle routine which will run the test with new random data, or

b. lock on the failing chain with lock on error switch 3. This will "freeze" the random data that caused the initial and only failure. It is recommended that the operator set this switch on as soon as possible. If scope loop switch 0 is used, it should be set after locking on the error with switch 3, (switch 0 overrides switch 3). Both switches must be "off" to continue.

4.2.4 Long–Format Microtrace

The following is an example of the first machine cycle of a long–format microtrace for an Add Halfword (AH) instruction:

```
* MICROTRACE STARTING *
     ROSAR          Q REG            R     E    IC      D      S        T        STC   A        B       ABC WORK REG F STAT TRG
218  5CD  838   4A30F2409200F00F  4A30  9208  10E018  10A00F 0010E024 0010E008  7   0010A00F  00000008 7   0010E010 01
3547FFFF FF98FFF  3F000FFF 078E4FFF 00350000 00000000 00300000 00000000 00040000 40000000 30000000 005F6840
02180805 00040707 0010A00F 00000008 39100000 0A200201 00000000 0010E018 4A309208 0110A00F 4A30F240 9200F00F
00000800 00000000 803AE9FF 0010E010 00000000 00000000 00000000 00021000 00000000 0010010A 00000000 0080E800
F4FFFFF  41376C38 F7FF0000 00100F03 0010C112 00000000 00000000 00000000 20000000 00000000 0010E024 0010E0008
GPRD 7   0010B024 00000000 0010A994 00000001 00000000 00000000 0010EF5  0010E010
GPRB–15  0010B268 0010E000 0010F000 0010AF7C 0010C000 0010B000 00000208 0010A000
GPRO–7   00000000 00000000 00000000 00000000 AAAAAAAA 55555555 AAAAAAAA 55555555
```

FIGURE 4–4. LONG–FORMAT MICROTRACE

For each machine cycle, the contents of the machine's registers, the logout, the contents of the GPR's, and the contents of the FPR's are printed.

5.0 COMMENTS

5.1 SUBROUTINES

5.1.1 Chain Analysis

The Chain Analysis (CAN) subroutine is entered whenever an error is detected within the execution of the instruction chain. This subroutine isolates the failing instruction within the chain by reducing the number of instructions to the minimum that still causes an error. Upon isolating the failing instruction, CAN subroutine relinquishes control to the PMT subroutine.

CEDA section 3 uses a CAN routine mainly for machine check error isolation. Isolation is normally accomplished by direct comparison of expected and received results for all 16 instructions in the chain.

5.1.2 Programmed Micro–Instruction Trace (PMT)

The PMT subroutine is designed to provide a microtrace (cycle by cycle logouts) of the CPU operations including instructions and interruptions. Upon entry from CAN, PMT initiates a microtrace of the failing instruction using the Diagnose instruction with log–on–count.

PMT normal mode of operation is to print the short format, intermittent mode, and address C trace. If any other mode of operation is desired, the section sense switches should be used to make the selection.

The chain analysis subroutine will setup the three required parameter addresses for PMT. The first address called address A specifies the location of the start of the instruction sequence. In the case of CEDA it will be the starting address of a chain. In CEDA section 3 each test sets up these parameters. The second address (B) needed by PMT is the location where the instruction sequence is run under control of the diagnose instruction, using log–on–count. The third address (C) is the location of the instruction being traced. The maximum number of cycles allowed with log–on–count is 2047. If the instruction between addresses B and C exceed this count, address B parameter is moved closer to the address C parameter and the trace attempted again by PMT. If section sense switch 4 is set "on" the operator gets a printout of all instructions within the chain between the addresses of B and C. This may be a very long and time consuming printout and discretion should be used before requesting the option.

5.2 ROUTINES

Testing is done using an instruction chain consisting of the following combinations of instructions:

a. the instruction under test repeated 16 times with different data each time;

b. the instruction under test interspersed with previously–tested instructions and

c. the instruction under test with a specific condition set to force normal interruptions.

The data used by the instruction chain are both fixed and random. The result of each instruction is predetermined using instruction simulators. Thus an expected result table is developed for each chain; each entry in the table is the expected result of each instruction executed. There are tests (such as for branch and compare instructions) where tables are not generated. Also, instruction simulation is accomplished whenever possible but is limited to those instructions previously tested.

The five sections which comprise CEDA perform a complete test of the instruction fetching, decoding, and execution circuits, including the checking of data paths for the system/360 type instructions, but excluding the following:

SVC – Supervisor Call
HIO – Halt I/O
TCH – Test Channel
RDD – Read Direct
Multiple CE Instructions
Display Instructions
SIO – Start I/O
TIO – Test I/O
WRD – Write Direct
Diagnose

5.2.1 CEDA Section 1

MVC – Move Character (SS)
LPSW – Load PSW (SI)
LH – Load Half (RX)
STH – Store Half (RX)
BCR – Branch on Condition (RR)
BC – Branch on Condition (RX)
BALR – Branch and Link (RR)
BAL – Branch and Link (RX)
CL – Compare Logical (RX)
L – Load (RX)
AR – Add (RR)
SR – Subtract (RR)
CR – Compare (RR)
BCT – Branch on Count (RX)
IC – Insert Character (RX)
SLA – Shift Left Algebraic (RS)
SRA – Shift Right Algebraic (RS)
SLL – Shift Left Logical (RS)

SRL – Shift Right Logical (RS)
TM – Test Under Mask (SI)
MVI – Move Immediate (SI)
CLI – Compare Logical Immediate (SI)
STC – Store Character (RX)
A – Add Algebraic (RX)
S – Subtract Algebraic (RX)
ST – Store (RX)
LR – Load (RR)
LA – Load Address (RX)
NR – AND (RR)
OR – OR (RX)
O – OR (RX)
N – AND (RX)
CH – Compare Half (RX)
BCTR – Branch on Count (RR)
SSM – Set System Mask (SI)
ISK – Insert Storage Key (RR)
SSK – Set Storage Key (RR)
EX – Execute (RX)
LM – Load Multiple (RX)
STM – Store Multiple (RX)

5.2.2 CEDA Section 2

– FIXED POINT –

LPR – Load Positive (RR)
LNR – Load Negative (RR)
LCR – Load Compliment (RR)
ALR – Add Logical (RR)
AL – Add Logical (RX)
AH – Add Half (RX)
XI – Exclusive OR (SI)
NI – Exclusive AND (SI)
OI – OR Immediate (SI)
OC – OR (SS)
XC – Exclusive OR (SS)
NC – AND (SS)
C – Compare Algebraic (RX)
CLR – Compare Logical (RR)

– FLOATING POINT LOAD & STORE –

CLC – Compare Logical (SS)
LTR – Load and Test (RR)
XR – Exclusive OR (RR)
X – Exclusive OR (RX)
SH – Subtract Halfword (RX)
SLR – Subtract Logical (RR)
SL – Subtract Logical (RX)
LE – Load Short (RX)
STE – Store Short (RX)
LD – Load Long (RX)
STD – Store Long (RX)
LER – Load Short (RR)
LDR – Load Long (RR)
LPER – Load Positive Short (RR)
LNER – Load Negative Short (RR)
LPDR – Load Positive Long (RR)
LNDR – Load Negative Long (RR)
LCDR – Load Compliment Long (RR)
LCER – Load Compliment Short (RR)
LTDR – Load and Test Long (RR)
LTER – Load and Test Short (RR)
CER – Compare Short (RR)
CE – Compare Short (RX)
CDR – Compare Long (RR)
CD – Compare Long (RX)

5.2.3 CEDA Section 3

– VFL LOGICAL –

MVN – Move Numerics (SS)
MVZ – Move Zones (SS)
TR – Translate (SS)
TRT – Translate and Test (SS)
EDIT – Edit (SS)
EDMX – Edit and Mark (SS)

– BRANCHING –

BXH – Branch on Index High (RS)
BXLE – Branch on Index LO OR EQU (RS)

– VFL DECIMAL –

PACK – Pack (SS)
UNPK – Unpack (SS)
AP – Add Decimal (SS)
SP – Subtract Decimal (SS)
ZAP – Zero and Add (SS)
CP – Compare Decimal (SS)

– STATUS SWITCHING –

TS – Test and Set (SI)

5.2.4 CEDA Section 4

– FLOATING POINT –

AER – Add Normalized Short (RR)
AE – Add Normalized Short (RX)
AWR – Add Unnormalized Long (RR)
AW – Add Unnormalized Short (RX)
AUR – Add Unnormalized Long (RR)
AU – Add Unnormalized Long (RX)
ADR – Add Normalized Long (RR)
AD – Add Normalized Long (RX)
HDR – Halve Long (RR)
HER – Halve Short (RR)

– FLOATING POINT –

SER – Subtract Normalized Short (RR)
SE – Subtract Normalized Long (RX)
SWR – Subtract Unnormalized Long (RR)
SW – Subtract Unnormalized Long (RX)
SUR – Subtract Unnormalized Short (RR)
SU – Subtract Unnormalized Short (RX)
SDR – Subtract Normalized Long (RR)
SD – Subtract Normalized Long (RX)

5.2.5 CEDA Section 5

– FIXED POINT AND DECIMAL –

SLDL – Shift Left Double Logical (RS)
SRDL – Shift Right Double Logical (RS)
SLDA – Shift Left Double Algebraic (RS)
SRDA – Shift Right Double Algebraic (RS)
MH – Multiply Half (RX)
MR – Multiply (RR)
M – Multiply (RX)

– FIXED POINT AND DECIMAL (Continued) –

DR – Divide (RR)
D – Divide (RX)
MP – Multiply Decimal (SS)
DP – Divide Decimal (SS)

– FLOATING POINT –

ME – Multiply Short (RX)
MER – Multiply Short (RR)
MD – Multiply Long (RX)
MDR – Multiply Long (RR)
DE – Divide Short (RX)
DER – Divide Short (RR)
DD – Divide Long (RX)
DDR – Divide Long (RR)

RX FORMAT FIXED–POINT INSTRUCTIONS FUNCTIONAL TESTS (D1151–D1157, D115A)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RX format "fixed–point" class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE plus an input/output device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no sense switch options in these sections.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instructions when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D11' Supervisor Call instructions.

4.2 INFORMATION

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
LA	D1151	5
L	D1152	5
ST	S1153	5
A	D1154	5
S, C	D1155	5
CL	D1156	5
N, O, X	D1157	5
AL, SL	D115A	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RR FORMAT FIXED–POINT INSTRUCTIONS FUNCTIONAL TESTS (D115C–D1167)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RR format "fixed–point" class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal switches in these sections.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
LR	D115C	5
LR	D115D	5
LR	D115E	5
LR	D115F	5
AR	D1160	5
SR, CR	D1161	5
CLR	D1162	10
NR	D1163	5
OR	D1164	5
XR	D1165	5
LPR, LNR, LTR, LCR	D1166	5
ALR, SLR	D1167	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RR, RX, AND RS FORMATS BRANCH INSTRUCTIONS FUNCTIONAL TESTS (D1169–D116D)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RR, RX, and RS formats "branch" class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in these sections.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

RR, RX, AND RS FORMATS BRANCH INSTRUCTIONS FUNCTIONAL TESTS (D1169–D116D) (Continued)

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instruction for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
BC, BCR	D1169	5
BAL, BALR	D116A	5
BCT, BCTR	D116B	5
BXH, BXLE	D116C	5
Unsuccessful Branching, all of the above instructions	D116D	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RX FORMAT HALFWORD INSTRUCTIONS FUNCTIONAL TESTS (D116F)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RX format "halfword" class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

This section requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

RX FORMAT HALFWORD INSTRUCTIONS FUNCTIONAL TESTS (D116F) (Continued)

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, the section number, and the run time involved:

Instruction	Section ID	Run Time in Less Than Seconds
LH, STH, AH, SH, CH	D116F	10

6.0 APPENDIX

6.1 STORAGE MAP

This program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RS FORMAT SINGLE–SHIFT INSTRUCTIONS FUNCTIONAL TESTS (D1171)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RS format "single shifts" class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

This section requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

RS FORMAT SINGLE-SHIFT INSTRUCTIONS FUNCTIONAL TESTS (D1171) (Continued)

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, the section number, and the run time involved:

Instruction	Section ID	Run Time in Less Than Seconds
SRL, SRA, SLL, SLA	D11710	5

6.0 APPENDIX

6.1 STORAGE MAP

This program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

SI FORMAT INSTRUCTIONS FUNCTIONAL TESTS (D1173–D1178)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the SI format class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
TM	D1173	5
CLI	D1174	10
MVI	D1175	5
NI	D1176	5
OI	D1177	5
XI	D1178	5

6.0 APPENDIX

6.1 STORAGE MAP

This program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

'TS' SI FORMAT INSTRUCTION FUNCTIONAL TEST (D1179)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of the SI format test–and–set instruction.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

This section requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instruction tested, its section number, and the run time involved:

Instruction	Section ID	Run Time in Less Than
TS	D1179	1 Minute

6.0 APPENDIX

6.1 STORAGE MAP

This program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

"LM/STM" RS FORMAT INSTRUCTIONS FUNCTIONAL TESTS (D117B – D117C)

1.0 PURPOSE

1.1 INTENT

This CE program is designed to test the functional operation of each instruction in the LM/STM RS format class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATING

Refer to maintenance monitor manual for DM sense switch options. There are no internal sense switches in these sections.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions, their section numbers, and the run time involved:

Instruction	Section ID	Run Time in Less Than Seconds
STM	D117B	5
STM, LM	D117C	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RR AND SI FORMATS STATUS–SWITCHING INSTRUCTIONS FUNCTIONAL TESTS (D117E)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RR and SI formats "status–switching" class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

This section requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time involved:

Instruction	Section ID	Run Time in Less Than Seconds
SVC, LPSW, SPM SSM	D117E	5

6.0 APPENDIX

6.1 STORAGE MAP

This program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RR AND RX FORMATS MULTIPLY/DIVIDE INSTRUCTIONS FUNCTIONAL TESTS (D1180–D1184)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RR and RX formats multiply/divide class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

This section requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
MH	D1180	5
M	D1181	5
MR	D1182	5
D	D1183	5
DR	D1184	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RS FORMAT DOUBLE–SHIFT INSTRUCTIONS FUNCTIONAL TESTS (D1186)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RS format "double–shifts" class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

This section requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

RS FORMAT DOUBLE-SHIFT INSTRUCTIONS FUNCTIONAL TESTS (D1186) (Continued)

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, the section number, and the run time needed:

Instruction	Section ID	Run Time in Less Than Seconds
SRDL, SLDL, SRDA, SLDA	D1186	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

SS FORMAT INSTRUCTIONS FUNCTIONAL TESTS (D118A–D1190)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the SS format class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 system simplex consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in these sections.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
CLC, MVC	D118A	15
NC	D118B	5
OC	D118C	5
XC	D118D	5
MVO	D118E	5
MVN	D118F	5
MVZ	D1190	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

MOVE WORD INSTRUCTION TEST (D1191)

1.0 PURPOSE

1.1 INTENT

This diagnostic program checks functional specifications of the Move Word Instruction and provides good indications when errors are encountered.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, or MDM–D/E.

2.2 EQUIPMENT

This section requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus and I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the maintenance monitor manual for loading procedure.

3.2 OPERATION

a. Refer to the maintenance monitor manual for DM sense switch options.

b. Section sense switches may be used in routines 1, 2, 3, and 4 only.

   Sense switch 0 = 1 loop on failing data in routines 3 and 4.

   Sense switch 1 = 1 loop routine on error. Valid in routines 3 and 4. (Bypasses Monitor.)

   Sense switch 2 = 1 skip section abort in routines 1 and 2.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

3.4.1 Routine Termination

Routines are terminated via SVC X'D6'. If routines 7 and 8 are terminated before normal end of routine, the DM will return to the section to allow housekeeping of storage keys.

3.4.2 Section Termination

This section is terminated via SVC X'D6' if run to completion. If I–fetch in routine 1 or 2 should fail, this section is terminated via SVC X'D5' and the message 'Section Aborted' is printed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

All error messages are outputted by DM via either SVC X'D0' or SVC X'D1'.

4.2 OPERATIONAL MESSAGES: SECTION ABORTED

This message is outputted when a data transfer error is detected in either routine 1 or 2. If it is desired to continue, reload section with section sense switch 2 set to 1. This will bypass section abort.

5.0 COMMENTS

Section D1191 tests the MVW instruction in the CE.

6.0 APPENDIX

6.1 STORAGE MAP

D1191 occupies no more than 8K (8192 decimal) bytes of core storage. The location of the section is determined by the controlling monitor at load time.

"IC/STC & ISK/SSK" RX AND RR FORMAT INSTRUCTIONS FUNCTIONAL TESTS (D1192)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the "IC/STC"RX format class and in the "ISK/SSK" RR format class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

This section requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

"IC/STC & ISK/SSK" RX AND RR FORMAT INSTRUCTIONS FUNCTIONAL TESTS (D1192)

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, the section number, and the run time involved:

Instruction	Section ID	Run Time in Less Than Seconds
IC STC ISK SSK	D1192	5

6.0 APPENDIX

6.1 STORAGE MAP

This program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RX AND SS FORMATS VARIABLE FIELD–LENGTH INSTRUCTIONS FUNCTIONAL TESTS (D1196–D119B)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the RX and SS formats variable field–length class.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
CVD, CVB	D1196	5
TR	D1197	5
TRT	D1198	5
PACK, UNPK	D1199	5
SS BOUNDARY TEST 1	D119A	120
SS BOUNDARY TEST 2	D119B	45

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

SPSB, LPSB AND LI INSTRUCTIONS FUNCTIONAL TESTS (D119C–D119D)

1.0 PURPOSE

1.1 INTENT

These CE programs are designed to test the functional operation of the Store and Load PSBAR, and Load Identity instructions in accordance with IBM 9020 System specifications. These programs are intended to be used for two purposes: they will run under the control of IDM as bring–up programs, and can also be used as maintenance programs under the control of MDM.

1.2 MODIFICATIONS

This is the initial program release.

2.0 REQUIREMENTS

2.1 PROGRAM

All sections must run under control of either IDM or MDM.

2.2 EQUIPMENT

This program requires a 9020 simplex system consisting of a CE, IOCE, and SE, plus an input/output device for program loading.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for IDM and MDM loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no sense switches in these sections.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

The following is a list of instructions tested, and their section numbers, included in the scope of this document:

Instruction	Section ID	Run Time in Less Than Seconds
SPSB, LPSB, LI and PGM INT	D119C0	5
EX, SPSB, LPSB, LI and EX, PGM INT	D119D0	5

These sections check only logical PSBAR, not physical PSBAR that results from ATR.

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

FLOATING POINT FUNCTIONAL TESTS (D11A2–D11CA)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of each instruction in the floating point instruction set. These programs also contain worst case patterns and reliability routines.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch settings. There are no section sense switch options for these sections.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for methods of terminating a section.

4.0 PRINTOUTS

4.1 INSTRUCTIONS TO OPERATOR

4.2 STATUS MESSAGES

When errors are encountered under SDM, MDM, or MDM–D/E control, SVC X'D0' and X'D1' and X'D2' messages will describe the error and give actual and expected results.

Under IDM control, errors result in hang–up loops. Refer to the maintenance monitor manual for identification of these loops.

5.0 COMMENTS

5.1 PROGRAM DESCRIPTION

The following is a list of the instructions tested and the section numbers for the instructions in the Floating Point Set.

Instruction	Section
LE, STE LD, STD DE, CD	D11A2
LER, CER LDR, CDR, LTER	D11A6
LTDR LCER, LCDR	D11A9
LPER, LPDR	D11AC
LNER, LNDR	
AER, ADR AE, AD	D11B0
AUR, AWR AU, AW	D11B4

Instruction	Section
SER, SDR SE, SD	D11B8
SUR, SWR SU, SW	D11BC
HER, HDR	D11C0
MER, MDR ME, MD	D11C2
DER, DDR DE, DD	D11C6
Reliability multi– ply/Divide	D11CA

5.2 APPROXIMATE RUN TIMES

The approximate run time is less than 10 seconds per section.

6.0 APPENDIX

6.1 STORAGE MAP

These sections each occupy 2K (8192 decimal) bytes of main storage.

DECIMAL INSTRUCTIONS FUNCTIONAL TESTS (D11CD–D11D1, D11D3–D11D8)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of the decimal instruction set.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in this section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
AP	D11CD	5
AP	D11CE	5
SP	D11CF	5
CP	D11D0	5
ZAP	D11D1	5
MP	D11D3	5
MP	D11D4	5
DP	D11D5	5
DP	D11D6	5
ED	D11D7	5
EDMK	D11D8	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

RX FORMAT "EX" INSTRUCTION FUNCTIONAL TESTS (D11DA–D11E1)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of the RX format EX instruction.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in these section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
EX of Small Binary Instruction Set	D11DA	5
EX of Small Binary Instruction Set	D11DB	5
EX of Small Binary Instruction Set	D11DC	5
EX of Standard Instruction Set	D11DD	5
EX of Standard Instruction Set	D11DE	5
EX of Floating Point Instruction Set	D11DF	5
EX of Floating Point Instruction Set	D11E0	5
EX of Decimal Instruction Set	D11E1	5

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

PROGRAM INTERRUPTS FUNCTIONAL TESTS (D11E4–D11E8)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of the 9020 CE program interrupt system.

1.2 MODIFICATIONS

This program has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in these section.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or SVC X'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
Program Interrupts, using Small Binary Instruction Set	D11E4	15
Program Interrupts, using Standard Instruction Set	D11E5	15
Program Interrupts, using Floating Point Instruction Set	D11E6	15

Instruction	Section ID	Run Time in Less Than Seconds
Program Interrupts, using Decimal Instruction Set	D11E7	15
Suppression, Completion, and Termination of Program Interrupts, using all Instruction Sets	D11E8	5

All expected interrupts are returned to the sections.

All storage elements configured in the system should be defined to the monitor; otherwise error printouts may occur.

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage, except D11E8, which occupies 8K (8192 decimal) bytes. The location of a section after loading is determined by the controlling monitor.

INVALID OP-CODES, PROGRAM INTERRUPTS AND EX-PROGRAM INTERRUPTS FUNCTIONAL TESTS (D11E9)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of the program interrupt system, in particular the Operation Exception.

1.2 MODIFICATIONS

This program has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

This section operates under IDM, SDM, MDM, or MDM-D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATION

Refer to the maintenance monitor manual for DM sense switch options. Also refer to page 2 of program listing for internal program sense switch options.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

INVALID OP-CODES, PROGRAM INTERRUPTS AND EX-PROGRAM INTERRUPTS FUNCTIONAL TESTS (D11E9) (Continued)

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or 'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

The following is a list of hexadecimal invalid op-codes tested:

00	
0D	81
0E	93
20–3F	99
4D	A2–D0
51	D9–DB
53	DE–F0
60–7F	F4–FF

Approximate run time of D11E9 is less than 5 seconds.

An Operation Exception type program interrupt will be generated for each of the CE invalid op code in the instruction stream. Routine 2 will attempt it with an Execute instruction, the invalid op code being removed from the instruction stream. All expected program interrupts will be returned to the section from just before each test op code until just after each test op code.

6.0 APPENDIX

6.1 STORAGE MAP

This program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

'EX'–PROGRAM INTERRUPTS FUNCTIONAL TESTS (D11EB–D11EE)

1.0 PURPOSE

1.1 INTENT

This CE program tests the functional operation of the program interrupt system, using the RX format EX instruction.

1.2 MODIFICATIONS

This description has been changed to accommodate the 9020D and 9020E Systems, as well as the 9020A System.

2.0 REQUIREMENTS

2.1 PROGRAM

These sections operate under IDM, SDM, MDM, or MDM–D/E.

2.2 EQUIPMENT

These sections require a 9020 simplex system consisting of a CE, IOCE, and SE, plus an I/O device for program loading and communication.

3.0 OPERATING PROCEDURES

3.1 LOADING

Refer to the 9020 System Maintenance Monitor Manual for loading procedures.

3.2 OPERATING

Refer to the maintenance monitor manual for DM sense switch options. There are no internal sense switches in these SE sections.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

Refer to the maintenance monitor manual for possible ways of terminating a section. Normal program termination is by the section issuing an SVC X'D6' Supervisor Call instruction when the section's last routine is completed.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

When a section recognizes an error condition, an error message is conveyed by the monitor from SVC X'D0' and/or 'D1' Supervisor Call instructions.

4.2 INFORMATION PRINTOUTS

These messages are conveyed by the monitor from SVC X'D0' Supervisor Call instructions for the operator's information.

5.0 COMMENTS

Listed below are the instructions tested, their section numbers, and the run time per section:

Instruction	Section ID	Run Time in Less Than Seconds
EX–Pgm Interrupts, of Small Binary Instruction Set	D11EB	15
EX–Pgm Interrupts, of Standard Instruction Set	D11EC	15
EX–Pgm Interrupts, of Floating Point Instruc–tion Set	D11ED	5

Instruction	Section ID	Run Time in Less Than Seconds
EX–Pgm Interrupts, of Decimal Instruction Set	D11EE	15

All expected interrupts are returned to the sections.

6.0 APPENDIX

6.1 STORAGE MAP

Each program section occupies and does not use more than 4K (4096 decimal) bytes of core storage. The location of a section after loading is determined by the controlling monitor.

INTERVAL TIMER TESTS FOR 7201–02 (D13A0)

1.0 PURPOSE

This section tests the 60–Hz interval timer of the IBM 7201–02 Computing Element (CE) for its ability to step, to step within the correct time interval, and to be inhibited from stepping by use of a Diagnose instruction.

2.0 REQUIREMENTS

2.1 PROGRAM

This section must be loaded by and run under control of SDM or MDM–D/E. The DM must be loaded via a CE.

This section assumes that Hardcore, D0040, has run successfully.

2.2 EQUIPMENT

This section requires a 9020D or 9020E system. Only those units required by DM are needed to run this section.

CHECK CONTROL switch must be in PROCESS position. TIMER switch should be ON if no manual intervention is required or OFF if operator wants section to enter initial halt and perform sense switch set up.

3.0 OPERATING PROCEDURES

3.1 LOADING

Standard DM loading procedures are used.

3.2 OPERATION

After initial loading, the section tests if the interval timer is stepping. If it is stepping, the section will proceed with the testing.

If not stepping, an initial wait is entered following a message to the operator. The operator can now set any section sense switch options via the console data keys. (See section 5.2 which describes data

key usage). If no keys are set, a normal section pass is taken. Timer MUST be enabled at this time. If not, the section assumes the timer is inoperative and terminates.

To continue enter a B–message.

3.3 HALTS OR WAITS

None.

3.4 TERMINATIONS

A normal termination occurs after the section has completed one pass.

The operator may terminate the section anytime by entering an F–message.

If routine 01 is entered without the timer stepping, the section terminates following an error printout. If routine 01 is entered when monitor sense switch 21 is set to 1 and the timer is disabled, the section terminates following an operational printout.

4.0 PRINTOUTS

Each printout contains the address of the common print Supervisor Call instruction in the first line and the address of the branch instruction to the common print routine in the second line.

4.1 ERROR PRINTOUTS

*SD0	D13A00	01 0062A8
LOC	00668E	TIMER DID NOT STEP WITHIN 40MS–TURN TIMER SWITCH OFF AND RUN HARD CORE, ID – D0040. HARD CORE ATTEMPTS TO SET THE TCS TRIGGER VIA SCAN IN, THEREFORE IF HARD CORE RUNS THE TROUBLE IS PRIOR TO THE TCS TRIGGER OR THE NORMAL SET INPUT TO THE TCS TRIGGER.
*SD0	D13A00	01 0062A8
LOC	0066B8	TIMER STEPPED UP NOT DOWN.
*SD0	D13A00	01
LOC	0066F8	TIMER STEPPING TOO FAST, STEPPED 000010 TIMES IN APPROXIMATELY 25 I FETCHES IT SHOULD NOT HAVE STEPPED AT ALL IN THE TIME ALLOTED.

INTERVAL TIMER TEST FOR 7201–02 (D13A0) (Continued)

*SDO	D13A00	01 0062A8
LOC	006736	TIMER STEPPING BY WRONG FACTOR SHOULD BE 6 BUT IS 0005.
*SDO	D13A00	01 0062A8
LOC	006752	BYTE 53 HEX WAS MODIFIED BY A TIME CLOCK STEP – ONLY 50–52 SHOULD BE AFFECTED.
*SDO	D13A00	02 0052A8
LOC	005784	COULD NOT SET TIMER TO ALL –F,S–. SEE EXPECTED/ACTUAL PRINTOUT BELOW
		02 005790
		FFFFFFFF EXPECTED
		FFFFFFFF ACTUAL
*SDO	D13A00	02 0052A8
LOC	0057B4	COULD NOT SET TIMER TO ZERO. SEE EXPECTED/ACTUAL PRINTOUT BELOW
		02 0052C8
		00000000 EXPECTED
		00000000 ACTUAL
*SDO	D13A00	02 0052A8
LOC	0057E4	NO EXTERNAL INTERRUPT FROM TIMER OVERFLOW.

INTERVAL TIMER TEST FOR 7201–02 (D13A0) (Continued)

*SDO	D13A00	02 0062A8
LOC	006806	TIMER WAS NOT SET TO ALL –F,S– AFTER IN–TERRUPT. SEE EXPECTED/ACTUAL PRINTOUT BELOW
*	D13A00	02 006812 FFFFFA00 EXPECTED FFFFFB00 ACTUAL

NOTE: Expected contents of timer after interrupt is really zero (value in timer prior to interrupt) minus the stepping factor, not all F's.

*SD0	D13A00	02 0062A8
LOC	006850	UNABLE TO INHIBIT TIMER STEP USING DIAG–NOSE WITH MCW BIT –20– EQUAL TO ONE

*SDO	D13A00	03 0062A8
LOC	006876	AFTER INHIBITING TIMER VIA DIAGNOSE IN–STRUCTION MCW BIT–20,PROGRAM COULD NOT RESET THIS CONDITION AND ALLOW TIMER TO STEP AGAIN.

*SDO	D13A00	04 0062A8
LOC	0068F2	60 CYCLE INTERVAL TIMER SET TIMER TO 800000 AND ALLOWED IT TO STEP ONCE. EXPECTED TIMER CONTENTS AFTER ONE STEP–7FFFFB. ACTUAL TIMER CONTENTS AFTER ONE STEP—7FFFFA.

*SDO	D13A00	05 0052A8
LOC	00599A	60 CYCLE INTERVAL TIMER IS STEPPING EVERY 24.811 MS. LIMITS SHOULD BE 13.333 TO 20.000 WHICH IS A 20 PER CENT TOLERANCE ANY MINOR VARIANCE FROM THE PRECISE TIME OF 16.666 MS, COULD BE DUE TO TOLERANCES IN PROGRAM SYNCING, MACHINE TIMING, ETC. ANY MAJOR VARIANCE IS PROBABLY DUE TO INPUT LINE FREQUENCY BEING OFF.

4.2 OPERATIONAL PRINTOUTS

*SDO	D13A00	01 0052A8
LOC	0055DC	TIMER NOT STEPPING – TURN TIMER SWITCH ON – CPU SWITCH TO PROCESS–SET SENSE SWITCHES VIA KEYS AS DESIRED AS LISTED IN PROGRAM WRITE–UP OR IN FRONT OF LISTING. TO CONTINUE ENTER A B–MESSAGE VIA THE 1052. IF TIMER SWITCH IS ALREADY ON RUN HARD CORE, ID – D0040. HARD CORE ATTEMPTS TO SET THE TCS TRIGGER VIA SCAN IN, THEREFORE IF HARD CORE RUNS THE TROUBLE IS PRIOR TO THE TCS TRIGGER OR THE NORMAL SET INPUT TO THE TCS TRIGGER.
HLT	D13A00	01 FF0400DA400055E8 00DA
SDO	D13A01	01 0052AC
LOC	0055B8	THIS SECTION WILL BE TERMINATED –NO ROUTINES EXECUTED– THE TIMER IS NOT STEPPING AND DM SENSE SWITCH 21 IS ON – BYPASS MANUAL INTERVENTION.

5.0 COMMENTS

5.1 ROUTINE DESCRIPTIONS

5.1.1 Routine 01

Tests for the ability of the clock to step, tests that it does not step continuously, tests that it decrements by the correct value and tests that a timer update only affects the high order bytes of word 80 (decimal).

5.1.2 Routine 02

Tests for the ability of the timer bits to be set to all ones or all zeros. A test is also made that an external interrupt occurs when the timer steps through zero and the contents of the timer are correct after the interrupt.

5.1.3 Routine 03

Testss to see if the timer can be inhibited from stepping by using a feature of the diagnose instruction (MCW bit 20 set to 1). If it can, then an attempt is made to reset this condition using another diagnose instruction (MCW bit 20 set to 0).

5.1.4 Routine 04

Tests that each bit of the timer can step to the next lower bit.

5.1.5 Routine 05

Times the duration between time clock steps. The results are printed if either they are not within a $\pm$20 percent tolerance or if the printout is requested via the consle data keys. All error printouts will be flagged as usual with an asterisk at the beginning of the printout. Slight variations from the nominal of 16.666 ms for 60 Hz timers are to be expected due to program syncing circuit delays or input line frequency being minutely off. Three passes are made in this routine for each pass of the section and all three results should be within .02 milliseconds of each other if the timer is working correctly.

5.2 CONSOLE SENSE SWITCHES AND THEIR USAGE

5.2.1 Sense Switch Definition

Sense Switch	Function
0	Scope loop if ON
1–2	Spare
3	Loop/lock on error if ON
4–6	Spare
7	Enter keys via diagnose if ON
8	Loop active routine if ON
9–19	Spare
20–21	Delay in nanoseconds (in decimal). Only numbers 0–9 are allowed in each half byte; if violated, a program interrupt will occur. If no entry is made at the initial wait, a delay of 375 ns will be used.
32–60	Spare
61	Force printout in RT05 if on
62	Spare
63	Validity bit–if on console switches are active

5.2.2 Sense Switch Usage

Bits 0–31 of keys, if read, are set into section sense switches in the section preface. After the initial halt the console keys will only be read if section sense switch 7 is on and then used only if bit 63 of the keys was a one. At the initial halt, only bit 63 is needed to read the keys. If switch 7 is not set, keys 0, 3, 8, and 61 even though they were read, will not be used. At any other time switch 7 will have to set manually or via the console typewriter. The switches are read if the above conditions are met, anytime printing is done and between routines.

Keys 20–31 (delay in microseconds) are used only after the initial halt.

SYSTEM/360 MODE DIFFERENCES OF OPERATION (D13A5)

1.0 PURPOSE

This section is a functional test of the differences between the 9020 System mode of operation and the System/360 mode of operation within a 9020D or 9020E System CE. Channel mask differences are tested by using the LPSW and SSM instructions and by creating program interruptions. All multiple CE (multiprocessing) instructions (except TS) are performed on various addressing boundaries to ensure that while in System/360 mode an operation exception program interruption occurs.

2.0 REQUIREMENTS

2.1 PROGRAM

This relocatable section must be run under the control of SDM or MDM–D/E. The DM must be loaded via a CE.

2.2 EQUIPMENT

This section requires a 9020D or 9020E System. Only those units required by the DM are needed to run this section.

3.0 OPERATING PROCEDURES

3.1 LOADING

Standard DM loading procedures are used.

3.2 OPERATION

This section forces CE errors, causing check indicators to light. Therefore, if forced CE errors are not desired, set monitor sense switch 15 to 1 to bypass all testing by this section. That is, monitor sense switch 15 must be set to 0 to allow this section to test.

The section sense switch options are as follows.

Switch	Meaning When Set
0	Loop on error detected in routine 01.
1	Loop testing of current or selected op code (routine 03 or 05).
2	Begin routine (03 or 05) with selected op code.

Switch	Meaning When Set
3	Begin routine 03 testing of all op codes on boundary specified in switches 16–23.
8–15	Selected op code referred to in descriptions for switches 1 and 2.
16–23	Boundary of op code to test first in routine 03; must be 00, 02, 04, or 06 when switch 3 is set to 1.

For example, to loop a specific op–code, boundary test: set switches 1, 2 and 3 to 1, set switches 8–15 per the specific op code, and set switches 21 and 22 per the desired boundary. Thus, to loop Load PSBAR (op code A1) on a 6, 8 boundary, enter SS13A5.1.2.3.8.10.15.21.22/.

3.3 HALTS OR WAITS

None.

3.4 TERMINATION

Standard DM termination procedures are used.

4.0 PRINTOUTS

4.1 INFORMATION PRINTOUTS

These messages are conveyed to the monitor by SVC X'D0' for the operator's information.

4.2 ERROR PRINTOUTS

When the section recognizes an error condition, an error message is conveyed to the monitor by SVC X'D0' or X'D1'.

5.0 COMMENTS

Routine 01 tests PSW bits 16–19, making sure they cannot be set while in System/360 Mode.

Routines 02 and 04 are used only to allow the DM to handle any pending I/O interruptions; no testing is done.

Routine 03 tests that all multiple CE op codes (except that for TS) cause an operation exception program interruption when performed in System/360 mode. Each instruction is performed four times, once on each halfword boundary relative to a doubleword; 00, 02, 04 and 06.

Routine 05 is the same as routine 03 except that the Execute instruction is used and there is no boundary variation.

MULTIPLE CE INSTRUCTIONS FUNCTIONAL TESTS (D13B0)

1.0 PURPOSE

This section checks that each multiple CE (or multiprocessing) instruction (except Test and Set) gives results according to architectural specifications. The tests are designed to exercise all ROS paths of the instruction. Test and set instruction is tested in a different section.

2.0 REQUIREMENTS

2.1 PROGRAM

This section must be loaded by and run under the control of SDM or MDM–D/E. The DM must be loaded via a CE. FLT's and Hardcore are assumed to have run successfully.

2.2 EQUIPMENT

This section requires a 9020D or 9020E System. Only those units required by DM are needed to run this section. The length of this relocatable section is about 19,000 decimal bytes.

3.0 OPERATING PROCEDURES

3.1 LOADING

Standard DM loading procedures are used.

3.2 OPERATION

Set monitor sense switch 21 to 1 if bypassing of routines 2 through 10, which require operator intervention, is desired.

The following section sense switch options are as available.

Switch	Function When Set to 1
1	Bypass PMT regardless of errors or other option settings.
2	Use long PMT microtrace format that includes a hex dump of each micro–instruction logout.
4	Print PMT microtrace of instructions from address B through address C instead of just address C

3.3 HALTS OR WAITS

If operator intervention is allowed, a halt in routine 1 allows the operator to set conditions specified by an output message. A similar wait occurs in routine 10.

3.4 TERMINATION

If the CE being tested is not in state zero, the section is terminated in routine 1. Otherwise, standard DM termination procedures are used.

4.0 PRINTOUTS

4.1 ERROR PRINTOUTS

Upon detecting an error, the section prints information concerning suspected problems using SVC X'D0'. Also, except for any problem encountered with the DLY instruction, a PMT microtrace accompanies the error information. Some examples follow:

- AN UNEXPECTED PRIVIL–OP EXCEPTION RESULTED AFTER ISSUING SCON WITH ALL LEGITIMATE BITS SET IN CCR THE EXPECTED RESULT WAS GOOD COMPARE CONFIGURATION MASK— 3EFFCF0E SELECTION MASK— 00000800
  MICROTRACE START
  (The microtrace is printed here.)
  MICROTRACE END
- THE EXPECTED SPECIFICATION INTERRUPT DID NOT OCCUR WHEN SATR WITH NO VALID SE SELECTED.
  ATR MASK AFTER SATR WAS ISSUED— 0000000000000084
  (The microtrace is printed here.)

4.2 INFORMATION PRINTOUTS

If manual intervention is allowed:

- TURN TEST SWITCH ON–ENABLE TIMER–REPLY B/TO CONTINUE
- MANUAL INTERVENTION REQUIRED. INSTRUCTIONS ABOVE.

5.0 COMMENTS

5.1 RUN TIME

Total run time, excluding printouts or halts, is less than 2 seconds.

5.2 INSTRUCTIONS TESTED

The instructions tested by this section are: SCON, SATR, LPSB, IATR, SPSB, LI, DLY, and MVW.

5.3 ROUTINE DESCRIPTIONS

Routine 1 initializes the section by checking for state 0, setting up selection mask for SATR, setting up DE portion of CCR if on a 9020E System, interrogating monitor sense switch 21 for manual intervention bypass, and checking for interval timer and test switch on (if sense switch 21 is set to 0) or skipping routines 2–10 (if sense switch 21 is set to 1).

Routine 2 issues DLY instruction with a maximum value and sets the interval timer to externally interrupt the delay.

Routine 3 repeatedly issues DLY instructions and compares the actual and expected delays.

Routine 4 issues a SCON instruction with the R1 field containing an odd register address. The expected result is a specification interruption.

Routine 5 issues a SCON instruction with the scon field all 0's. The expected result is a specification interruption.

Routine 6 issues a SCON instruction with no IOCE selected. The expected result is a condition code of 2.

Routine 7 issues a SCON instruction with the CE field of 0 in the configuration mask and a valid IOCE selected. The expected result is a condition code of 2.

Routine 8 issues a SCON instruction with an IOCE selected to communicate with 2 CE's. The expected result is a specification interruption.

Routine 9 issues a SCON instruction with an IOCE selected to communicate with CE 4. The expected result is a condition code of 2.

Routine 10 issues a SCON instruction with each legitimate bit set in the configuration mask. The resulting CCR is expected to be the same as the configuration mask. This routine also requests that the TEST switch be turned off or, alternatively, resets CCR and skips routine 11.

Routine 11 issues a SCON instruction if the TEST switch is off. The CCR is used as a configuration mask and the expected result is a condition code of 0. Routine 11 is the first testing routine to be run if manual intervention is bypassed.

Routine 12 issues a SATR instruction with a selection mask of all 0's. The expected result is a condition code of 3.

MULTIPLE CE INSTRUCTIONS FUNCTIONAL TESTS (D13B0) (Continued)

Routine 13 issues a SATR instruction to an element that does not have the executing CE's scon bit on. The expected result is a condition code of 1.

Routine 14 issues a SATR instruction with a parity error. The expected result is a condition code of 2.

Routine 15 issues a SATR instruction with an SE value in the DE half of the ATR mask, and vice versa. The expected result is a specification interruption. This test is skipped in a 9020D System.

Routine 16 issues a SATR instruction without a valid SE selected. The expected result is a specification interruption.

Routine 17 issues a SATR instruction with bits set to all elements of the system. The expected result is a condition code of 0.

Routine 18 issues a SPSB instruction with a valid operand. The value logged out is expected to equal the value stored.

Routine 19 issues LPSB with the operand field pointing to an unreal SE. The expected result is a specification interruption.

Routine 20 issues LPSB with the operand field address not on a full word boundary. The expected result is a specification interruption.

Routine 21 issues LPSB with operand field pointing to 30000 hex and then causes a program interruption. The expected result is a successful load, which will be known by using addresses from new PSA. PSBAR is reset to its original value.

Routine 22 issues IATR with R2 field specifying a different register from the R1 field. The expected result is a good compare between R1 and the first 8 digits of ATR and also a good compare between the first byte of R2 and the last 2 digits of ATR. Routine 22 also issues IATR with the two register fields equal. The expected result is a good compare between R1 and the first 8 digits of ATR.

Routine 23 issues LI and checks that the value returned is a positive integer not greater than 3. Also, this routine issues LI with a test value in the R2 field and checks that the value is undisturbed.

Routine 24 issues MVW with source on a doubleword boundary and destination or doubleword boundary and compares the data in destination against expected. A good compare is the expected result.

Routine 25, 26 and 27 are similar to routine 24, except in 25 source is on a doubleword boundary and destination is on word boundary, and in routine 26 source on word boundary and destination on doubleword boundary, and in routine 27, both source and destination are on word boundaries. In all three routines the expected result is a good compare of data in destination to data in source.

MULTIPLE CE INSTRUCTIONS FUNCTIONAL TESTS (D13B0) (Continued)

Routine 28 issues MVW with source on a doubleword boundary and destination on the first doubleword higher than source. The expected result is a good compare of a propagated doubleword.

Routine 29 issues MVW with source on doubleword boundary and destination on the first word higher than source. The expected result is a good compare of a propagated word.

Routine 30 issues MVW with source on a word boundary and destination on the second word higher than source. The expected result is a good compare of a propagated doubleword.

Routine 31 issues MVW with source on a word boundary and destination on the first doubleword boundary higher than source. The expected result is a good compare of a propagated word.

Routine 32 issues MVW with source and/or destination on halfword boundary. The expected result is a specification interruption.

SCON AND SATR TESTS (D13B1)

1.0 PURPOSE

This section tests the ability of any individual valid 9020D element, as designated by the operator, to accept reset and set configuration masks and if the element is a CE or IOCE all possible valid ATR masks for the installation.

2.0 REQUIREMENTS

2.1 PROGRAM

This section must be loaded by and run under the control of MDM D/E. The section can be cycled but not multiprogrammed. It must run in a CE in state Ø.

2.2 EQUIPMENT

The minimum sub-system required for MDM and this section is one each of the following elements:-

CE IOCE, SE plus a DCU or TCU and drive for the loader device.

Additionally a card reader or 1052 is required for operator input messages. Output messages requiring action by the operator are routed to the MDM primary output device, all other output messages are routed to the MDM secondary output device, Since a considerable amount of printout can occur under error conditions it is advisable to use a HSP as the MDM secondary output device.

The element to be tested must have the appropriate SCON bit set in its CCR for the CE which is to run this section. Since the element will be reset it must not be in use by MDM, that is it must not have been added to the MDM environment by A or U messages.

3.0 OPERATING PROCEDURES

3.1 LOADING

Standard diagnostic loading procedures are used. This program requires A Q messages to define the element to be tested. If the Q message is entered with the load message the short format can be used, if entered after loading the program the long format must be used ie:-

Q.AA/..... Short format Q message.

Q13B1.AA/... Long format Q message

Where AA is one of the 2 digit alphanumerics listed in table 3.1.

ALPHANUMERIC	UNIT DEFINED
1X	CEX where X is 1-4
2X	SEX where X is 1-9 or A
3X	IOCE X where X is 1-3
4X	TCU X where X is 1-3
8X	DCU X where X is 1-3
CX	PAM X where X is 1-3

TABLE 3.1 UNIT DEFINITIONS IN A Q MESSAGE

Sense switch settings are all optional and can be used in any combination, sense switch 1 (Bypass program micro trace) takes precedence over sense switches 2,4,5 and 6. Sense switch functions are listed in table 3.2.

SENSE SWITCH	ROUTINE AFFECTED	FUNCTION WHEN SET
Ø	2	READ CE DATA KEYS 32-63
1	2,3.4,5	BYPASS PMT*
2	2,3,4,5	LONG PMT* FORMAT
4	2,3,4,5	TRACE ADDRESS B THROUGH C
5	2,3,4,5	NOT INTERMITTENT MODE PMT
6	2,3,4,5	DO NOT INHIBIT X 'A34' LOGOUTS
18	2,3,4,5	FORCE ERROR PRINT

TABLE 3.2 SENSE FUNCTIONS

* PMT = PROGRAM MICRO TRACE

3.2 OPERATION

3.2.1 ROUTINE 1 - HOUSEKEEPING

Routine 1 initialises the main print subroutine PRINTA and checks if this is the first entry to routine 1, if the section is being cycled all other functions are bypassed except on the first pass.

First the routine checks whether a Q message has been entered, if not output message 1 is printed (FIG 4-1) and the section halts. When a B message is entered the routine rechecks if a Q message has been entered.

The entered Q message is checked to ensure that two characters have been included and that they define a valid configurable 9020D unit.

If an error is detected output message 2 is printed (FIG 4-2) followed by output message 1 (FIG 4-1). The section then halts waiting for a new Q message to be entered. These checks are repeated until a valid Q message is entered.

Routine 1 then fetches the CCR data for the CE in which it is resident from the MDM section reference table (SRT). If no CCR data is found output message 3 is printed (FIG 4-3), the section then terminates. If CCR data is found the state bits are checked for state Ø. If the CE is not in state Ø output message 4 is printed (FIG 4-4) and the section then terminates. If the CE is in state Ø the MDM SRT is checked to see if the test unit has been added via an A or U message to the MDM environment, if it has output message 5 is printed (FIG 4-5) where AAAA A are the identity letters and number of the test unit eg IOCE 2. The section then terminates.

If the test unit has not been added to the MDM environment routine 1 then sets up an appropriate select mask plus reset and set CCR masks for this unit. The CCR for the master CE is used as the basis for all reset and set CCR masks, bits are extracted from it and used as follows:-

CE reset CCR:- SCON bit(s) only set.
CE set CCR:- all bits used except IOCE bits.
IOCE reset CCR:- SCON and SE bits only set.
IOCE set CCR:- SCON, SE and master CE communication bits (1 CE bit only).
TCU reset CCR:- SCON bit(s) only set.
TCU set CCR:- SCON and IOCE bits set.
DCU reset CCR:- SCON bit(s) only set.
DCU set CCR:- SCON and IOCE bits set.
PAM reset CCR:- SCON bit(s) only set.
PAM set CCR:- SCON and IOCE bits set. Only the lowest numbered IOCE bit is used if more than one is set in the master CE.
SE reset CCR:- SCON bit(s) only set.
SE set CCR:- SCON, CE and IOCE bits set.

NOTES:- All bits other than those shown are reset. No check is made as to whether an IOCE is valid for connection to any particular control unit since this is not significant for these tests. Output messages 1-5, 8 and 10 are all printed on the MDM primary output device, all other printouts are routed to the MDM secondary output device.

Routine 1 then terminates calling routine 2.

3.2.2 ROUTINE 2 - RESET SCON TESTS

Routine 2 first calls subroutine WRD to issue a write direct stop if the test element is a CE. If a program interrupt occurs as a result of the write direct output message 6 is printed, if condition code 3 is set output message 7 is printed, where AAAA A are the identity letters and number of the test unit.

Sense switch Ø is then checked
is printed and the section halts. When a B message is entered routine 2 reads the CE data keys and uses the data from keys 32-63 as a CCR mask, no checking is performed on this data other than to ensure that the SCON bit is set for the resident CE. If bad parity is read from the CE data keys output message 12 (fig 4-12) is printed followed by the logout in long format PMT. Then output message 9 (fig 4-9) is printed where the xxxx --- is replaced with the actual data read. Output message 10 (fig 4-10) is also printed and the section halts to allow the operator the choice of using the data read or the standard reset SCON mask.

Routine 2 then issues a SCON instruction using either the reset CCR mask as defined in 3.2.1 for the element under test or the CCR mask entered by the operator if sense switch Ø is set. If no error is detected the test is repeated 100 times (X'64'). The number of repeats can be varied by E patching location COUNT. this will have the effect of altering the number of repeats in all test routines and the value patched will be reflected in output messages 16 and/or 17 (figures 4-16 and 4-17).

An error is determined if the condition code after the SCON is not Ø or if the select and CCR registers do not contain the expected result. Under either of these conditions output message 11 (fig 4-11) and/or output messages 15 and 16 (figures 4-15 and 4-16) are printed and the PMT subroutine MICRO is called (See 3.2.6).

If no errors are detected but sense switch 18 is set output message 14 (fig 4-14) is printed and this is followed by the printouts described above as if an error had been detected.

If a program interrupt occurs as a result of the SCON instruction output message 13 (figure 4-13) is printed where xxxx---- is replaced by the relevant data followed by the error printout (fig 4-16) and PMT.

If a machine check interrupt occurs as a result of the SCON instruction output message 12 (fig 4-12) is printed followed by the logout in long PMT format, error printout fig 4-16 and PMT.

Whenever the error printouts occur the routine terminates without further repetition of the test.

3.2.3 ROUTINE 3 - ALTERNATE RESET/SET SCON TESTS

This routine is intended to simulate the action of the NAS operational program in that a write direct to stop is issued, if the test element is a CE, followed by a SCON with a reset CCR mask and a SCON with a set CCR mask. If no errors result the test is repeated such that a total of 100 SCON instructions are issued.

An error is determined only if the condition code is not Ø following the SCON. Printouts from routine 3 only occur if an error is detected, sense switch 18 is not tested. Error printouts following write direct and SCON errors are as described in 3.2.2.

3.2.4 ROUTINE 4 - SET SCON TESTS

This routine first calls subroutine WRD to issue a write direct to stop if the test element is a CE. A SCON instruction is then issued with a set CCR mask as defined in 3.2.1 for the test element. If no errors are detected the test is repeated 100 times. Error printouts and the action when sense switch 18 is set in the same as that described for routine 2 at 3.2.2.

3.2.5 ROUTINE 5 - SET ATR TESTS

This routine only runs if the test element is a CE or IOCE. First subroutine WRD is called to issue a write direct to stop if the test element is a CE, then a diagnose is issued to determine the number of SEs installed. From this information an ATR mask is built such that the SEs are in numerical ascending order starting in slot one. The SATR instruction is now issued and if no errors result the test is repeated 100 times. The ATR mask is then changed such that the SE in slot 1 is moved to slot 10 and all other SEs are moved 1 slot lower, the SATR test is then repeated. This process continues until all SEs have been tested in all possible ATR positions, the program then terminates.

An error is determined if following the SATR the condition code is not Ø or if the SATR registers do not contain the expected result. Error printouts for SATR errors, program interrupts and machine checks are the same as those described for routine 2 para 3.2.2 except that output message 17 (fig 4-17) replaces output message 16. An error stops further testing with that ATR mask, testing continues with the next ATR mask.

3.2.6 PROGRAM MICRO TRACE

PMT is described in chapter 5 of FAA 2000, only differences will be described here.

Sense switch options 1,2,4 and 5 are as described at 5.6 in FAA 2000, sense switch 6 is used within PMT but has a different function from that described in FAA 2000 as follows:-

When the test element is an SE the logouts caused by PMT tracing a SCON instruction tend to corrupt CCR data on Storage Data Bus In (SDBI) during the first five micro second timeout (ROS address X'A34' CAS block X'A34' is executed a total of 26 (decimal) times, the corruption occuring during the last few passes. As a result of this corruption the SCON fails as do all subsequent SCON attempts. To prevent the corruption PMT bypasses the next 12 logouts on detecting ROS address X'A34' thus logouts occur on the first and fourteenth pass through this CAS block the remaining 24 being suppressed. If sense switch 6 is set a full microtrace is performed and the SCON will fail. This problem does not affect any other 9020D element type and thus a full microtrace is always performed with sense switch 6 having no effect.

Output message 18 (fig 4-18) is printed at the start of PMT, the time shown in the first line refers to the approximate time for an intermittent mode trace of a SCON instruction with short format printout. This time is changed to 60 seconds when tracing a SATR instruction in routine 5. When sense switches 2 and/or 4 are set the time taken increases substantially. When sense

switch 5 is set the first line is replaced with "MICROTRACE STARTING".

3.3 HALTS OR WAITS

There are two conditions under which routine 1 will halt, if a Q message has not been entered or if a Q message error has been detected.

A further two halts may occur in routine 2 if sense switch Ø is set or if bad parity is detected in the key data.

3.4 TERMINATION

Routine 1 will terminate the section if it is unable to obtain the resident CE CCR field from the SRT of MDM or if the resident CE is not in state Ø. Otherwise standard termination procedures are used.

4.0 PRINTOUTS

ENTER TEST UNIT VIA Q13B1.OPTION/AND B/
FIG 4.1 OUTPUT MESSAGE 1

ERROR DETECTED IN LAST Q MESSAGE
FIG 4-2 OUTPUT MESSAGE 2

CCR DATA UNAVAILABLE - SECTION TERMINATING
FIG 4-3 OUTPUT MESSAGE 3

MASTER CE NOT IN STATE ZERO - TERMINATING
FIG 4-4 OUTPUT MESSAGE 4

AAAA A IN MDM SYSTEM ENTER U MSG. & RELOAD 13B1
FIG 4-5 OUTPUT MESSAGE 5

WRITE DIRECT TO AAAA A FAILED
FIG 4-6 OUTPUT MESSAGE 6

WRITE DIRECT TO AAAA A FAILED, CONDITION CODE 3 OCCURRED
FIG 4-7 OUTPUT MESSAGE 7

SET DESIRED CCR IN CE X DATA KEYS 32-63 THEN ENTER B/
FIG 4-8 OUTPUT MESSAGE 8

BAD PARITY IN DATA KEYS - DATA RECEIVED XXXXXXXXXXXXXXXX
FIG 4-9 OUTPUT MESSAGE 9

ENTER RS13B1.Ø/ TO SKIP KEY DATA AND/OR B/ TO CONTINUE
FIG 4-10 OUTPUT MESSAGE 10

THE RECEIVED AND EXPECTED RESULTS DID NOT COMPARE UNDER THE FOLLOWING CONDITIONS
FIG 4-11 OUTPUT MESSAGE 11

```
A MACHINE CHECK OCCURED UNDER THE FOLLOWING CONDITIONS
```

FIG 4-12 OUTPUT MESSAGE 12

```
A PROGRAM INTERRUPT OCCURED WITHIN THE TEST INSTRUCTION
PROGRAM OLD PSW XXXXXXXXXXXXXXXX
GPR Ø-15, AT TIME OF INTERRUPT
XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX
XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX
```

FIG 4-13 OUTPUT MESSAGE 13

```
FORCE ERROR PRINT
```

FIG 4-14 OUTPUT MESSAGE 14

```
RECEIVED CONDITION CODE X UNDER THE FOLLOWING CONDITIONS
```

FIG 4-15 OUTPUT MESSAGE 15

```
                          EXPECTED              RECEIVED          ISSUED
SCON SELECT REG 8         XXXXXXXX              XXXXXXXX          XXXXXXXX
SCON CCR,S R6/R7      XXXXXXXX/XXXXXXXX     XXXXXXXX/XXXXXXXX XXXXXXXX/XXXXX
LOOP COUNT HEX VALUE:- INITIAL XXXXXXXX  NOW XXXXXXXX
```

FIG 4-16 OUTPUT MESSAGE 16

```
                          EXPECTED              RECEIVED          ISSUED
ATR.S R6/R7           XXXXXXXX/XXXXXXXX     XXXXXXXX/XXXXXXXX XXX XXXX/XXXXX
LOOP COUNT  HEX VALUE:- INITIAL XXXXXXXX   NOW XXXXXXXX
```

FIG 4-17 OUTPUT MESSAGE 17

```
STARTING INTERMITTENT MODE TRACE - 40 SECONDS PER PASS
RSR PSR LM N E IC D S T STC A B ABC X ATR Y F STT
```

FIG 4-18 OUTPUT MESSAGE 18

5.0 COMMENTS

5.1 RUN TIME

Total run time excluding printouts and halts in less than 2 seconds. Maximum run time with sense switches 2,4,5 and 18 set is approximately 45 minutes for a CE or IOCE.

5.2 RECOMMENDATIONS

Since a considerable amount of printout can occur it is recommended that a HSP is initialised as secondary output device only. All outputs requiring operator action are routed to the primary output device, these may be overlooked if this also is the HSP.

If sense switch 6 is set while testing an SE and PMT is called (due to an error or sense switch 18 set) it will be necessary to manually reconfigure the SE or system IPL to recover since the corruption of CCR data usually sets the SE to state 1 and CE4. The logouts at ROS address X'A34' are identical except for the contents of the B register which contains the loop count which is decremented on each pass.

6.0 REFERENCES

FAA 2000