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Systems Reference Library

IBM 7750 Principles of Operation

Preliminary Edition

Presents the operation and use of the 7750 Programmed Transmission Control including: (1) a system summary, (2) detailed description of process storage, control storage, registers, timing, instructions, priority processing, interfaces, modes of operation, operator's panel, types of adapters, and channel operations.

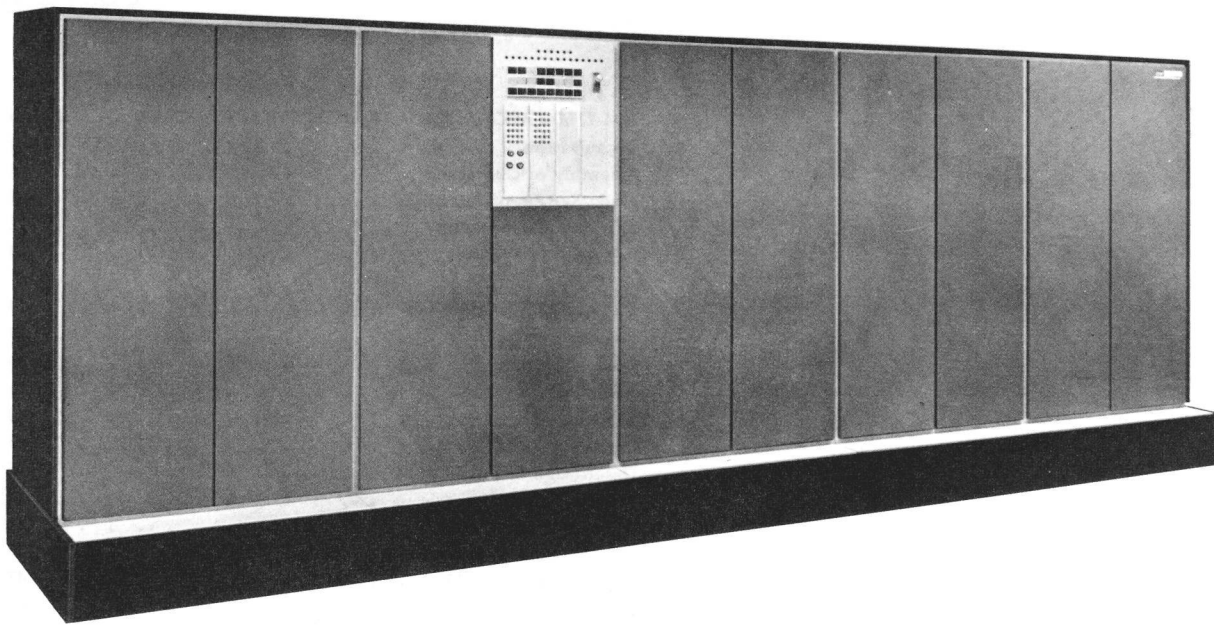
This edition is a complete revision of the former edition. Because of limited interest, no copies have been distributed to the library.

MAJOR REVISION (March, 1963)

This edition, Form A22-6679-1, obsoletes Form A22-6679 and all earlier editions. Significant changes have been made throughout the manual, and this edition should be reviewed in its entirety.

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IBM 7750 Programmed Transmission Control

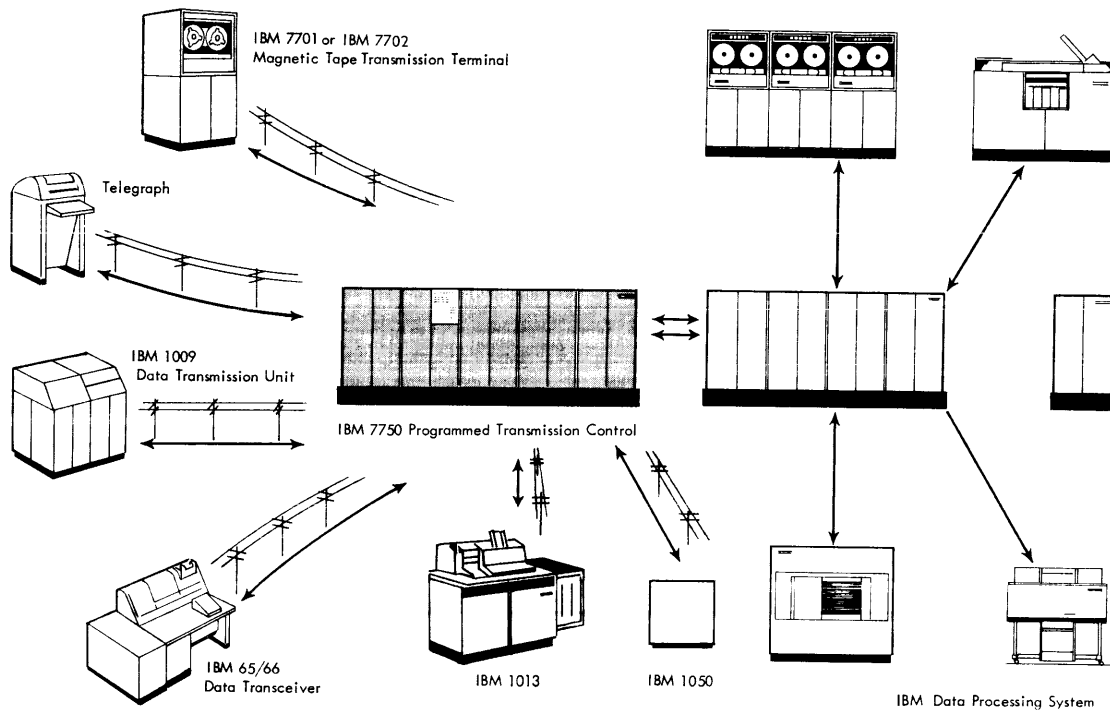


Figure 1. Communication-Based Data Processing System

The IBM 7750 Programmed Transmission Control is a Tele-Processing[®] system component that links a central computer with remote terminals. Telecommunications equipment such as telegraph terminals, IBM 65/66 Telegraph Data Transceivers with IBM 67 Telegraph Signal Units, IBM 7701 or 7702 Magnetic Tape Transmission Terminals, IBM 1013 Card Transmission Terminals, IBM 1009 Data Transmission Units, or IBM 1050 Data Communications System may be connected to the 7750 through appropriate channel adapters. The 7750 is also connected to an IBM Data Processing System through a data channel. The 7750 thus enables computer users to combine data processing capabilities with the transmission capacity of many telecommunications devices (Figure 1).

The 7750 is a stored program unit that serves as a buffer control device, directing and controlling the flow of information between the computer and its communications network. This network may have a variety of standard or specially designed terminals, each operating independently but linked directly to the system. The terminals may have different transmission speeds. The 7750 accepts electrical signals

simultaneously from a number of communications lines, converts these signals into bits, then into characters, then into records and, finally, relays these records at high speed to the computer for processing.

Usually, the prime function of the 7750 is to connect the diverse elements of the network to an associated computer such as the IBM 1410, 7010, 7040, 7044, 7070, 7074, 7080, 7090, or 7094. Tele-Processing systems using the 7750 may be employed for airline reservations, message routing, centralized data processing, production control, or other applications. The system planner can choose the computer and be assured that the communications problem will not be a significant factor in determining his choice.

The IBM 7750 is organized around two magnetic core storages. Control storage is used to control the communications network and to assist in the execution of the programs. This memory contains 128 words; there are 48 bits per word of storage. Process storage is used to hold the message queues and the programs. Process storage may be one of three sizes: 16,384 words, 48 bits per word (sometimes called 16K storage); 8,192 words, 48 bits

per word (8K storage); or 4,096 words, 48 bits per word (4K storage). Specific job applications determine the size of process storage chosen. All important functions of the 7750 are performed in and around these memories. The Tele-Processing system depends on the terminals used, which model of the 7750 is installed, and the traffic volumes of the customer.

Within a Tele-Processing system, the 7750 performs five basic functions:

Data Assembly (and Distribution) proceed automatically with only occasional supervision from the stored program. Data assembly begins when bits are derived from the incoming communications circuits by the channel adapter. The process continues until characters are assembled into complete data messages in the process storage section of the 7750.

Information Conversion from or to the form required by the computer includes changes to both the code and format of the message. Conversion is controlled by the 7750 stored program.

Editing involves omitting and adding special characters (and, sometimes, format changes) under program control.

Monitoring and Supervision checks incoming (or outgoing) traffic to indicate the status of terminals and oversees the data flow in a network. The stored program controls this function.

Data Transfer supplies data to and accepts data from the computer, on a demand and response basis, through linkage connecting the 7750 and the computer.

ORGANIZATION

The 7750 is made of five standard IBM racks.

1. Communications Line Terminator Rack: The major functions of this rack are to adapt communications lines to the 7750 and to aid the customer in isolating troubles in his communications network. The rack contains patch panels (a type of control panel for physically connecting transmission line terminations to internal 7750 channels), signal generation circuitry, and equipment to aid in the running of diagnostic programs on the 7750.

2. Channel Adapter Rack: This rack is designed to hold different types and combinations of channel

adapters. The channel adapters perform a variety of functions such as time-multiplexing a number of low-speed channels into one high-speed output, and recovering bit timings from synchronous data. The design of this rack is modular to match different types of communications networks. For example, two modules are required for handling data on from one through 56 low-speed lines. If 57 through 112 low-speed lines are desired, three modules are required for data handling. For any number of low-speed lines (from one through 112), one of the modules is used for controls. For from one through four high-speed lines, one module is required (and no extra module is needed for controls). Thus, all four modules could be used to accommodate as many as 16 high-speed lines.

3. Process Control Rack: This rack contains the registers and the instruction control circuitry for performing three basic functions: (a) assembly and distribution of data between the communications channels and process storage; (b) processing of assembled data under the control of stored programs; (c) transmission of data from and to the central computer.

4. Core Storage Rack: This rack contains the process storage and control storage. The data and address registers for these storages are in the process control rack.

5. Power Supply Rack: The power supply rack contains all the power supplies necessary to run the 7750.

Communications Terminology

The following communications terms are defined to clarify the explanation of 7750 operation.

Half-Duplex: A channel in which information can be transmitted in either direction, but only one direction of transmission may be employed at any one time.

Full-Duplex: A channel in which information can be transmitted in both directions simultaneously. Full-duplex channels are often made of two half-duplex channels.

Start-Stop Transmission: In this method of transmission the data bits are preceded by a start bit, and are followed by one or more stop bits. The total number of stop bits is not necessarily an integer.

The purpose of this method is to allow the receiving terminal to stay in synchronization with the transmitting terminal. In each character, the start and stop bits are the synchronizing information; thus, the receiver is resynchronized by each character. This method of transmission is used by normal telegraph machines.

Synchronous Transmission: Initially, the receiving terminal is synchronized with the transmitting terminal by the receipt of special synchronizing information (bit pattern), then the transmission of data begins. While data are being transmitted, no special synchronizing information is needed. It is assumed that both terminals stay in step for the duration of the transmission. At intervals, new synchronizing information is transmitted. It can be sent at the beginning of every message, or as infrequently as once a day. Synchronous transmission is generally used on high-speed channels, because it requires fewer bits than start-stop to transmit the same amount of information. For example, the IBM 7702 Magnetic Tape Transmission Terminal employs synchronous transmission.

Modem: The word modem is a contraction of the term modulation-demodulation. It is a device that accepts as input, from IBM equipment, binary-valued electrical signals and gives as output, to the transmission lines, a modulated waveform suitable for transmission over a communications channel. Conversely, the modem receives modulated waveforms from the transmission channel and converts them into binary-valued electrical signal outputs to IBM equipment.

Abbreviations Used in this Manual

<u>Abbreviation</u>	<u>Meaning</u>
ACIF	Adapter Control Interface
AL	Address- and Limit-Moving Instructions
CE	IBM Customer Engineer
CH	Character Manipulating Instructions
Clock-Hold	An instantaneous stopping of the 7750 clock whenever an error occurs, without the clock's continuing to the end of a cycle.
CLT	Communications Lines Terminator
CS	Control Storage
CSAR	Control Storage Address Register
CSDR	Control Storage Data Register
CSR	Channel Service Register
CT	Control Instructions
CWD	Channel Word

<u>Abbreviation</u>	<u>Meaning</u>
DWD	Data Word
ECWD	Error Channel Word
FM	Frequency Modulation
FSB	Fractional Sampling Bit
HSA	High-Speed Adapter
HSA2	High-Speed Adapter, Model 2
ICR	Interface Control Register
IFCR	Interface Control Register
IFDR	Interface Data Register
IR	Instruction Register
IWD	Instruction Word
Jack	A hole on the patch panel into which a cord is inserted (from another jack) to connect a communications channel to a 7750 internal channel.
L	Length-of-Modifier Portion of an Instruction
LCS	Last Clock Sample
LDS	Last Data Sample
LWD	Limit Word
M	Modifier Portion of an Instruction
MCA	Multiplexing Channel Adapter
MRR	Mode Request Register
ms	Millisecond
MS	Multiplexor Storage
MSDR	Multiplexor Storage Data Register
MSR	Mode Status Register
OAR	Operational Address Register
P(word)	Process Word
Patch	Manual connection, by cord on a patch panel, of a communication line termination with a 7750 channel termination.
PC	Process Control
PCR	Process Control Rack
Program Stop	A stop (caused by pushing the stop key) that occurs at a normal end-cycle time. (Note: The program stop light comes on with error stops as well as program stops.)
PS	Process Storage
PSAR1	Process Storage Address Register 1
PSAR2	Process Storage Address Register 2
PSDR	Process Storage Data Register
PWD	Process Word
R	Register to be used in a character-manipulating or control instruction
S	Size-specification portion of an instruction designating the number of bits in R to be operated upon.
SC	Sample Clock
SCC	Status Change Character
SCO	Sample Clock Oscillator
Scratch Words	Functionally unassigned words with predetermined locations in core storage.
S/R	Send/Receive
SS	Storage-to-Storage Data Transfer Instructions
SSDC	Special Sending Delay Character
STR	Synchronous Transmitter-Receiver
usec	Microsecond
W	Address Portion of an Instruction
W _e	Effective Address
W*	Indirect Address

ASSEMBLY OF CHARACTERS

Messages from the network enter the 7750 via one of several types of channel adapters. These adapters perform a variety of functions. One type, the multiplexing channel adapter (MCA) time-multiplexes a number of low-speed communications adapters into one high-speed information channel. It does this by a process of scanning and storing the results in a small core buffer. The high-speed adapter (HSA2) receives its information from an FM modem. All adapters communicate with control storage by means of the adapter control interface.

Adapter Control Interface

The adapter control interface connects the channel adapters to the control storage data register. This interface contains 19 lines. Each adapter is connected in parallel to these 19 lines, and a 16-position scanner selects a particular adapter at a given time. When an adapter is selected, information is transmitted on all 19 lines at once. The scanner does the selecting. The scanner is timed sequentially; there is no addressing of the scanner.

Three types of information pass across the interface: data, control information, and address. Channel adapters only receive and pass on bits; they do not assemble characters. Therefore, data are transferred serially, one bit at a time, across this interface, together with control information. Address information is transferred from the adapters to control storage, each adapter having one or more control storage locations associated with it. Besides information transfer, the interface also indicates to an adapter whether it should be in send or receive status, or indicates to control storage when some type of error has occurred in the adapters. The adapter control interface is controlled by a channel word in control storage.

Channel Word

The control storage operates alternately on scan cycles and process cycles. The process cycle is devoted to message processing and is discussed later. The scan cycle is devoted to receiving bits from or transmitting bits to the channel adapters. During scan cycles, channel words are read from control storage. These channel words have pre-assigned positions in core storage. The address of a channel word is generated in the channel adapter selected by the 16-position scanner in the adapter control interface. There is at least one channel word for each half-duplex channel connected to the

7750, and two channel words for each full-duplex channel, one word for the receive portion of the full-duplex channel and one word for the transmit portion of the full-duplex channel. These channel words completely control the action of the associated communications channel. The general channel word format is:

Address	Control Area	Char Assembly Area	P*
47	32 31	12 11	1

*Parity Bit

The channel word has three major functions: It serves as the assembly area in which bits are assembled into characters, directs the assembled character into the proper queue, and controls the communications channel.

The assembly of bits into characters is done in one 11-bit field of the 48-bit channel word. Character length may be any number of bits from two to 11 for start-stop type of transmission, and from one to 11 for synchronous transmission. As this assembly field is a shift register, bits are accepted one at a time and shifted until a complete character has been received. During transmission, a complete character is put into the assembly area and shifted out one bit at a time. The character length and bit count control fields are associated with the character assembly field. The character length is a four-bit field used to indicate the size of the character being received or transmitted over this particular channel. The bit count is a four-bit field which may be used to indicate how many bits of a given character have been received or transmitted.

The use of these fields differs somewhat in start-stop and synchronous transmission; their exact usage is explained in the "Detailed Description" section. As an example, consider the reception of a synchronous transmission that uses six-bit characters. The character length is set to 6 by the program, and the bit count advances every time a bit is received. Every time the bit count equals the character length, a complete character has been received. Three fields, the character assembly field, the character length, and the bit count, working in conjunction with one another, allow the reception and transmission of variable-length characters, one bit at a time. Within one message, all characters must have the same length.

When the character has been assembled, it must be directed into the proper queue in process storage. Another field in the channel word contains a 16-bit address. This is the address in process storage of

the next character to be sent or received. The assembled character is stored at this location in process storage. Sixteen bits are sufficient to refer to 65,536 locations. Each word in process storage may be divided into four fields; the address in the channel word is sufficient to specify any of them. When the character is complete, it is immediately put into process storage, regardless of what else may be going on in the machine. This process of transferring a complete character from the channel word to the process storage is called character interrupt, and is done automatically without program intervention. After a character has been transferred to process storage, the 16-bit address in the channel word is automatically incremented by one. When transmitting, the reverse procedure takes place. Characters are transferred from process storage into the character assembly field of the channel word, and the address in the channel word is incremented.

The third function of the channel word is to control the communications channels. Bits 12 through 31 in the channel word are used for this purpose. These bits perform such functions as indicating whether a channel is in send or receive status, whether the start-stop or synchronous mode of transmission is being used, whether the initial synchronization pattern has been found or whether the channel should be searching for this pattern, and whether the 7750 is waiting for a response on this channel. The use of these bits in the channel word is further explained in the "Detailed Description" section.

By assigning these functions to the channel word, and by having at least one channel word per communications channel, it is possible to have every channel operating in a different fashion, using different character lengths and different methods of transmission, and still maintain control over the channel by accessing the proper word. The time-shared, control storage data register is the only control register required. Thus, the channel word method provides an economical means of channel control and of character assembly.

Types of Instructions

Although instruction formats are discussed in detail later, it is helpful to the understanding of queue formation to know that there are four types of instructions to the 7750:

1. Character Manipulation: An example of this type of instruction is LOD Z11 POLLWD. This would mean, essentially: load a character into a certain Z register to identify the terminal to be polled.

2. Address and Limit-Moving. An example of this type of instruction is: GTL POLLWD. This means: get the limit portion of the word called POLLWD, a word in process storage. This limit portion goes into the operational address register, where the next instruction does something with it. The next instruction might be a put instruction, moving the limit portion to some part of another word.

3. Storage to Storage. This type of instruction deals with two word locations, one in process storage and one in control storage. An example would be: MWC 27 POLLWD. This means: move to control storage channel word 27, the polling word (in process storage at the symbolic location called POLLWD).

4. Control. An example of this type of instruction would be: BRZ Y11 ZEROS, meaning: branch to a subroutine called zeros if register Y is all zeros (a likely test for the end of a chain of blocks).

Queue Formation

When characters have been assembled in channel words, they are automatically transferred into a queue in process storage. The formation and maintenance of these queues is one of the most important tasks performed by the 7750. A large portion of process storage may be occupied with such queues because there will be an incoming queue for every channel receiving information from a communications terminal, an outgoing queue for every channel transmitting information to a terminal, a queue of information for the computer, and a queue of information coming from the computer. If process storage is to be used efficiently, a good system for assigning queuing space must be used.

Many methods of memory space assignment are possible. For example, a fixed block of storage can be assigned to each channel for its queuing space. This is a relatively inflexible and inefficient method of storage allocation. The storage space required for the queue may overflow the fixed amount of space available, or, only use a small fraction of the space. The problem is made more severe because message lengths are not restricted or in any way controlled. The 7750 therefore assigns its memory space for queues by the process of chaining.

Chaining consists of associating a sufficient number of pieces of storage space to make enough storage locations available to perform a given job. For chaining, process storage is broken into blocks. Each block consists of eight words. Each word is broken into four fields of 11 bits. Therefore, 32 characters may potentially be stored in each block. The 32nd storage location in each block is reserved

for a special character, called the block-control character. Each block has a starting address whose five low-order bits are all zeros. Because there are 32 characters per block, an ending address is one whose five low-order bits are all ones.

The block-control character is the 11 high-order bits of the starting address of the next block in the chain and is the means by which the blocks are chained together. For example, four blocks can be arbitrarily labeled A, B, C, and D. Figure 2 shows these blocks with their starting addresses. Figure 3 shows these blocks chained together, the order of the chain being C-A-B-D. They are chained because the block-control character in block C is composed of the eleven high-order bits of the starting address of block A; the block-control character in block A is composed of the 11 high-order bits of the starting address at block B, and so on. By means of chaining, small pieces of storage have been effectively assembled into a larger portion of storage. The blocks which make up the chain are not necessarily continuous in storage. These blocks may be physically located almost anywhere within process storage; through chaining, they act as a continuous segment of storage.

To make this process work, a certain amount of bookkeeping is required. The following is one method that may be used: First, chain together all the unused blocks of storage. Then maintain as records two addresses, A1, the starting address of the first empty block in the chain, and A2, the address of the block-control character in the last empty block in the chain. Suppose that a message queue has filled its chain and that another block is required. The 11 high-order bits of the starting address of the next block are put into the block-control character of the last block in the message queue and the first empty block from the chain of empty blocks is attached to the message queue. As this block is chained to the rest of the empty blocks, its block-control character is the starting address, A3, of the next empty block in the chain. Now A3 should be stored in the location which formerly held A1, because A3 is now the starting address of the first block in the chain of empty blocks. Thus, the process can be repeated.

When blocks become empty, they must be returned to the chain of empty blocks. Suppose that A4 is the starting address of an empty block which is to be returned to the chain of empty blocks. A4 is then written at the address specified by A2. That is, A4 is written as the block-control character of the last block in the chain of empty blocks. The block whose starting address is A4 is now connected to the end of the chain of empty blocks. To complete the process, A5, the address of the block-control character of

this block, is now written in the location at which A2 was stored.

After both these operations have been completed, a block has been removed from the front of the chain of empty blocks, a block has been added to the end of the chain of empty blocks, and the addresses A3 and A5 have been stored. These addresses are again the starting address of the first empty block in the chain of empty blocks and the address of the block-control character of the last block in the chain of empty blocks.

In the 7750, the chaining process is done under program control. When a particular channel requires more storage space for its queue, the channel service program is automatically brought into operation. The need for this program is sensed by noting when the five low-order bits of the address contained in the channel word are all ones. This indicates that the end of a block has been reached and that channel service is necessary to assign a new block to the chain. Thus far, characters have been assembled and put into queues in process storage. They will next be processed in some way before being sent on to the computer.

MODE SYSTEM OF INTERRUPTS

The 7750 works in an essentially uncontrolled environment. In many applications, the 7750 cannot dictate when messages will occur on the communications network, or what the length of these messages will be. Communication from the associated computer may take place at random intervals. Therefore, the 7750 is equipped with a very flexible interrupt system so that it may quickly and automatically switch from one program to another when various conditions require immediate attention.

This interrupt system has several levels. An interrupt may interrupt an interrupt, and so on. Priorities are assigned to various classes of interrupts so that the machine can decide which interrupt to execute. There are six such classes (or modes) of priorities in the 7750. These modes, listed in order of decreasing priority, are:

- | | |
|--------------------|-----------|
| 1. Service | 4. Out |
| 2. Channel Service | 5. In |
| 3. Copy | 6. Normal |

At the end of every machine cycle, the mode circuitry is examined to determine what modes are requested. The machine will then go into the requested mode with the highest priority and execute the programs associated with that mode. Requests for a mode are stored in the mode request register. This register maintains the requests until they can be serviced.

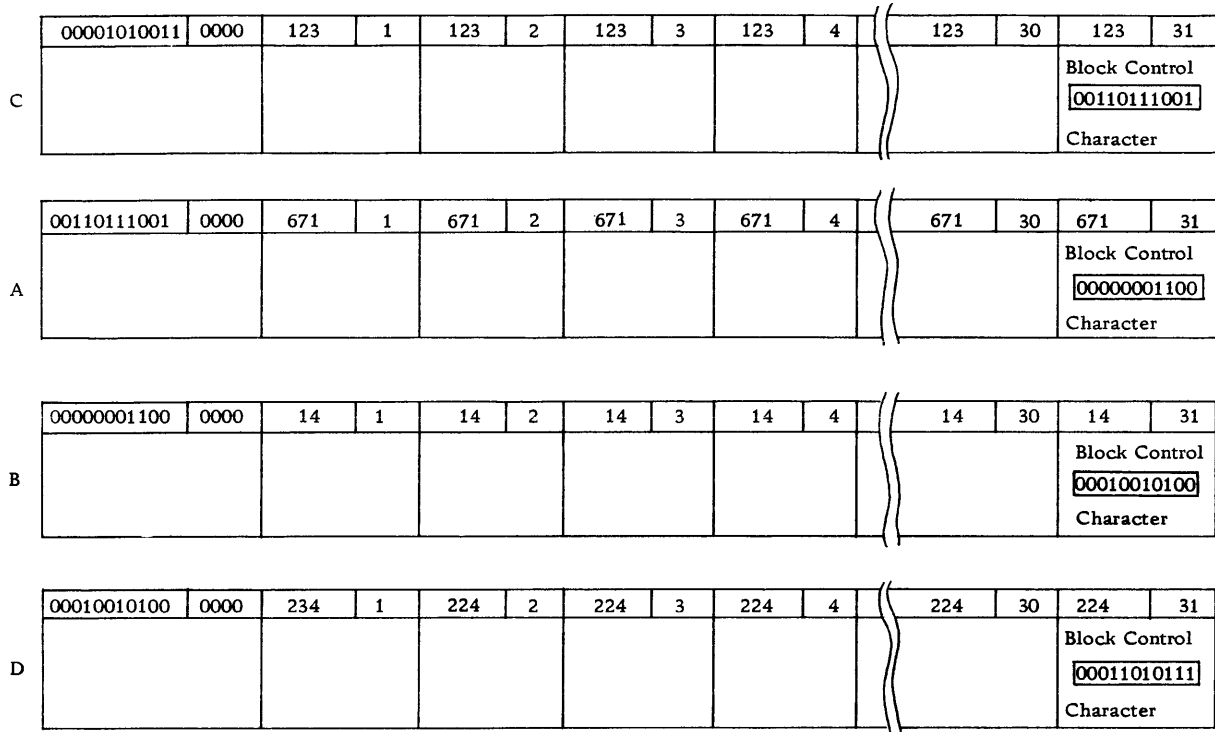


Figure 2. Blocks

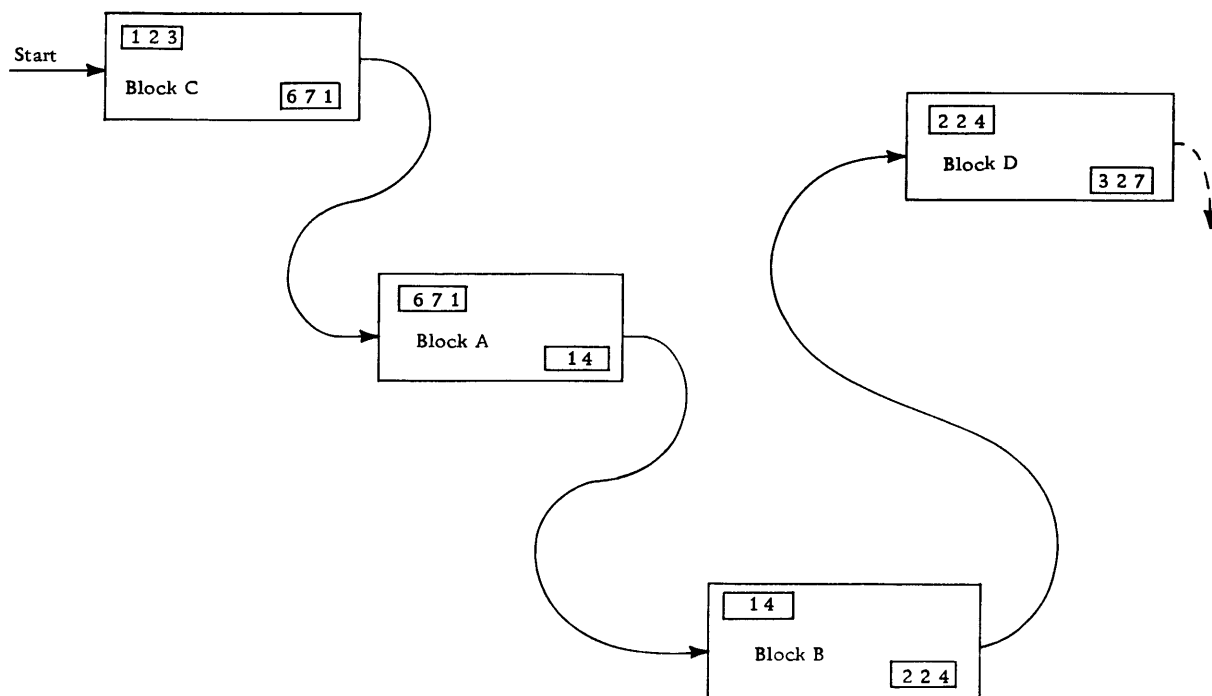


Figure 3. Chain C-A-B-D

Changes in mode can be made without any special preparation on the part of the programmer. It is not necessary to write a number of housekeeping programs to change modes. Instead, the 7750 stores all working registers and the instruction counter at the end of every machine cycle. Instruction counters are stored in control storage in a special format called the process word, or P word. This word contains three working registers as well as the instruction counter. There is one P word for each mode. Therefore, to change modes it is only necessary to access a different P word in control storage. The instruction counter in this P word will then address the programs associated with the new mode.

METHODS OF PROCESSING

The 7750 processes messages in real time, in a wide variety of formats, character sizes, and codes. Methods of processing must be extremely flexible to meet the diverse requirements. Therefore, table look-up is the fundamental processing technique.

Table look-up is used for many purposes in a typical 7750 program including code translations. Any code of up to 11 bits per character may be readily translated into any other arbitrary code of up to 11 bits per character. All shifts are performed by using shift tables. There is no shift instruction. Arithmetic operations are performed by means of multiple table look-ups. Perhaps the most important use of this technique is to control the operation of the normal mode program.

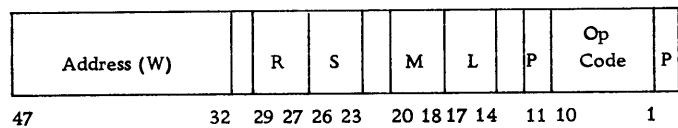
As an example of how the program may be controlled by table look-up, consider a telegraph polling system in which five programs may be required. These programs are: polling, sending data, answer back, header processing, and message processing. Assume there are 20 telegraph channels connected to the 7750. Each channel will require these programs in an unpredictable sequence. A technique for handling this situation requires the use of a program branching table and the assignment of a unique identification number, called a channel number, to each communications channel. The 7750 then uses the channel number to address the program branching table. The program branching table will then cause the program to branch to the correct programs. The last action any one of the programs performs is to update the relevant entry in the program branching table so that the next time the table is addressed by the channel number, the proper program will be selected.

Certain features of the instruction set permit table look-up operations to be performed easily.

These features are an address modification method and a register and size specification method. Each method is described below.

The 7750 is a single address machine. In many instructions, this address can be modified by means of information specified in the instruction. Two fields in an instruction, the M field and the L field, specify this modification. The M field specifies a particular register, and the L field specifies from zero to 11 low-order bits in that register. These bits then replace the L low-order bits in the address before the instruction is executed.

The 7750 is a binary machine. Therefore, it is most convenient to refer to the addresses in octal notation. The general format of the instruction word is:



Notes:

1. The P in the 11th bit position stands for a bit that satisfies a special parity requirement for the operation code and bits 12 and 13 only. The P at the right-most position of the word is the parity bit for the whole instruction.
2. Bits 12 and 13 are discussed later. Briefly, a bit in the 12th position decrements the Z register by one before execution of the instruction; a bit in the 13th position prevents mode change.
3. Bits 21, 22, 30, and 31 are not used in the instruction word.
4. The following is a resume of the symbols used in the instruction word:
 - W -- address (of the character in core storage to be operated upon)
 - R -- register (to be used in the operation)
 - S -- size (the number of bits involved in the operation)
 - M -- modification register (address of one of the seven registers whose bits are to replace the W portion)
 - L -- length (the number of low-order bits in M that are to replace an equal number or low-order bits in W)
 - P -- parity bit (both of which are described in note 1)

Consider as an example an instruction containing the address $(34651-1)_8$, where M specifies the Y register, and L equals 5. The address consists of the 14-bit word address (34651) plus a two-bit character address. Assume the contents of the Y register to be $(3732)_8$. The instruction would then be executed as though the address it contained

were (34656-2)₈; that is, five low-order bits of the Y register have replaced the five low-order bits in the instruction, namely the two-bit character address and three bits of the word address.

The register and size feature of the 7750 instruction set allows the results of many machine instructions to be placed in one of seven addressable registers. The particular register to be used may be selected by setting the proper bits in the R field of the instruction. The number of bits which are to be loaded into the specified register may also be varied by setting the S field of the instruction. This feature allows the programmer the option of loading from zero to 11 bits into the specified register.

The combined use of the register and size feature, and the address modification method allow a table look-up to be performed in one instruction, with the final result stored in a designated register.

Other useful features in the instruction set include the ability to perform most instructions with an indirect address, the ability to complement the operands in an instruction, and the ability to increment the address of the process storage word address by the instruction. Indirect addressing, complementing, and incrementing may be done individually, or they may be done in combination when executing most instructions.

The instruction set makes message processing more efficient. The program operates upon characters and messages which have been automatically stored in the process storage. There will be one queue of data to be processed for each receiving communications channel, and one queue of data to be processed from the computer. The program processes the contents of these queues, character by character, and places the results in other queues. Some of these queues will be transmitted back into the communications network, and one queue will be

transmitted to the computer. Thus, information has been acquired from the communications network, processed, and is now in the format which the associated computer requires.

INFORMATION TRANSFER

The 7750 connects to a host computer through a read bus (nine data lines), a write bus (another nine data lines), and a number of control lines to the proper data channel. The 7750 can be connected to the IBM 1410, 7010, 7040, 7044, 7070, 7074, 7080, 7090, and 7094 Data Processing Systems.

The 7750 operates in three modes to service the computer. These modes are: in, out, and copy. The in mode is used to prepare the 7750 for receipt of information from the computer. The control lines are examined, and the proper responses are made. The in mode program prepares a chain of storage for the incoming information and sets up the proper control word so that the 7750 can determine when all the information has been received from the computer. The out mode prepares the 7750 for the transmission of information to the computer. Its mode program sets the proper signal to inform the computer that the 7750 has information to transmit. In addition, this mode program also prepares the queue of outgoing information and sets up a control word so that the 7750 can determine when all information has been sent to the computer.

The actual transfer of information takes place in copy mode, which has no program. Information is transferred one character at a time, using a request and response system. The copy-mode process word (prepared in the in or out mode) specifies the area in process storage to contain the message.

DETAILED DESCRIPTION

PROCESS STORAGE

The IBM 7750 Process Storage is a magnetic core storage available in three sizes: 4,096 words, 8,192 words, 16,384 words. Each word contains 48 bits, including one parity bit.

Process Storage Word Formats

The contents of a word in process storage may be arranged in several ways, depending on its intended use. Figure 4 shows the word format for data words, instruction words, and limit words. Note that process storage words are words that are in process storage while process words (described later) are located in control storage. Both types of words are shown in Figure 4.

Data Word: The DWD is made up of four 11-bit registers: A, occupying bit positions 47 through 37; B, occupying bit positions 33 through 23; C, occupying bit positions 22 through 12; and D, occupying bit positions 11 through 1. Bit positions 36 through 34 are not used. Bit position P is the parity bit for the entire word.

Instruction Word: The IWD contains a ten-bit operation code in bit positions 1 through 10, an Op code parity in bit position 11, a two-bit flag field in bit positions 12 and 13, a four-bit L field in bit positions 14 through 17, a three-bit M field in bit positions 18 through 20, a four-bit S field in bit positions 23 through 26, a three-bit R field in bit positions 27 through 29, and a 16-bit address in bit positions 32 through 47 (low order in position 32). Bit position P is a parity bit for the word; bits 21, 22, 30 and 31 are not used.

Limit Word: The LWD, shown in Figure 4, contains a 16-bit address in the normal address portion of the word (W). The address occupies bit positions 32 through 47 of the word. In addition, the word contains a limit of 16 bits which fill bit positions 12 through 27. The five high-order bits of the limit occupy bit positions 23 through 27 (the five low-order positions of the B field in the data word); the 11 low-order bits of the limit field occupy positions corresponding to the data-word C field.

CONTROL STORAGE

The IBM 7750 Control Storage is a magnetic core storage with a capacity of 128 words. Each word has 48 bits, including one parity bit.

The control storage operates on alternate scan and process cycles of 11 microseconds and 17 microseconds, respectively. The scan cycle contains four microseconds for manipulation of the data word between read and write, and the process cycle contains ten microseconds for manipulation time.

Data are entered into and read out of the control storage by use of the control storage data register (CSDR).

Control Storage Data Register

The CSDR is a 48-bit register that holds the word to be read out of, or to be written into, storage. (See Figure 4.) The control circuits for this register enable it to be used as:

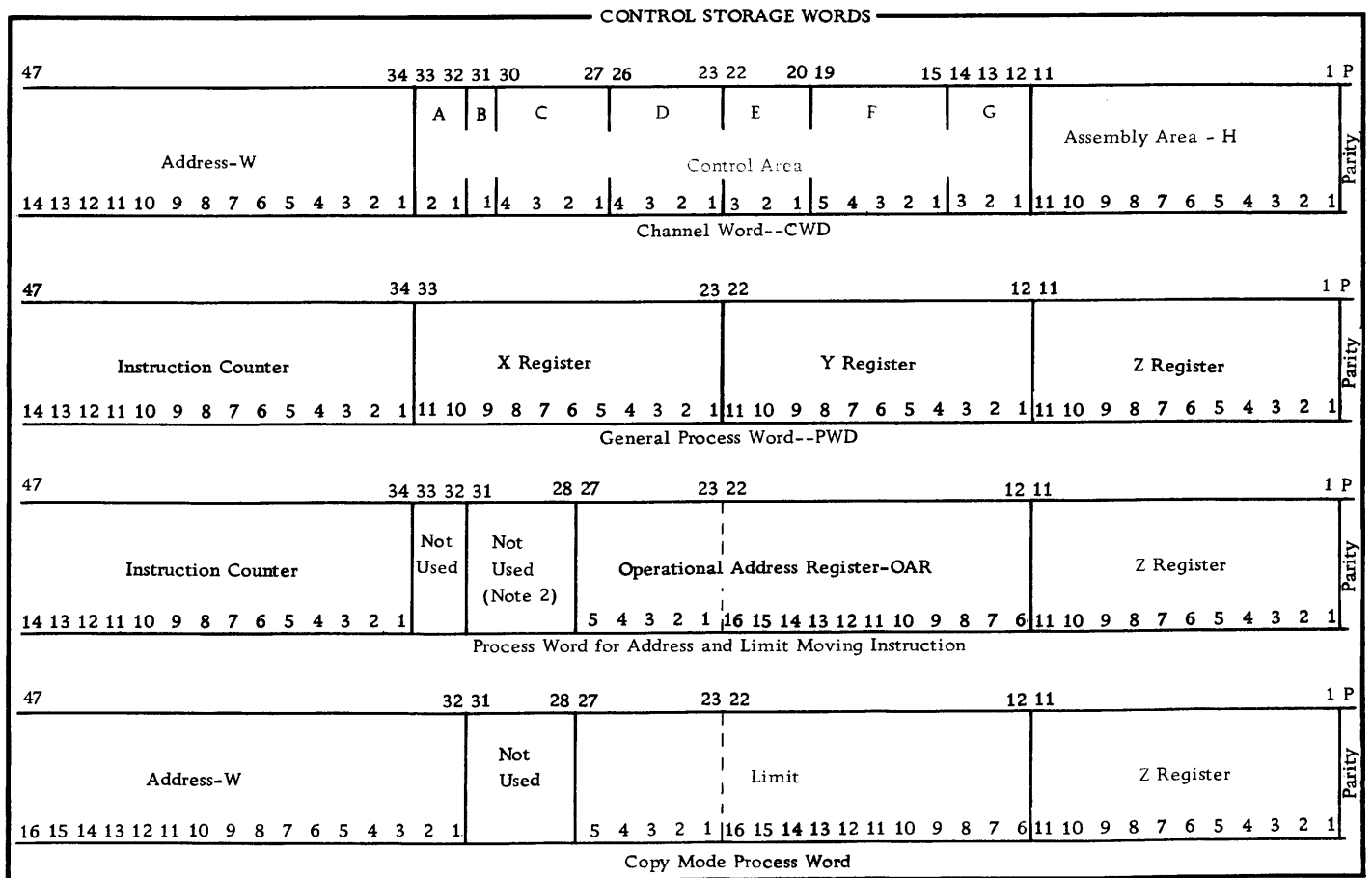
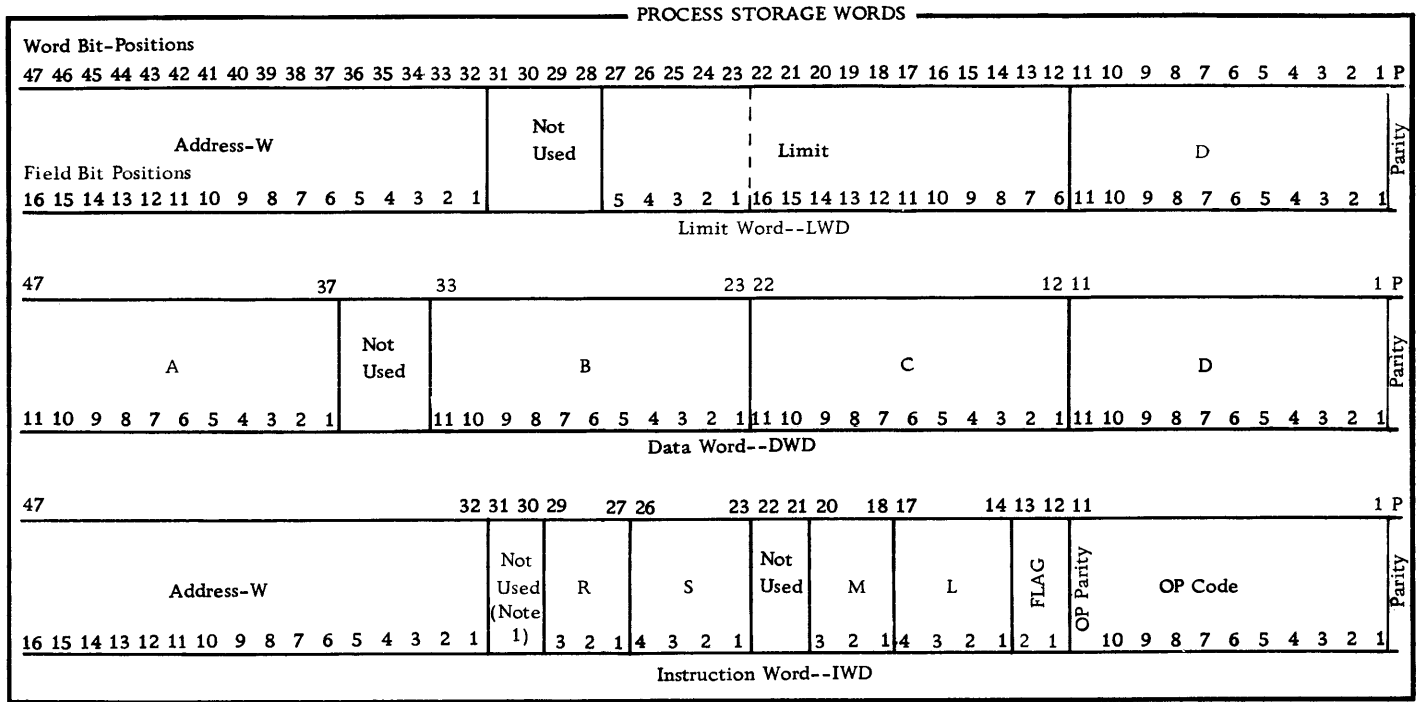
- (1) A single 48-bit register.
- (2) Four independent registers: X, Y, and Z, (11 bits each), and instruction counter (14 bits). See Figure 4, General Process Word.
- (3) Three independent registers: Z (11 bits), an operational address register (16 bits), and an address register (16 bits). See Figure 4, Process Word for Address and Limit-Moving Instruction.

The Z register is a count-down counter which may be decremented under program control.

Control Storage Word Formats

The control-storage word will be arranged in one of four ways, depending on its intended use (See Figure 4).

Channel Word: The CWD is divided into fields as shown in Table I



Note 1: Bits 23-33 are used as a mask in the branch-test instruction.
 Note 2: This not-used portion (bits 28-31) must contain 0 bits.

Figure 4. IBM 7750 Word Formats

<u>Field</u>	<u>CSDR Position No.</u>
W - Word Address	47-34
A - Character Address	33-32
B - Last Timing Bit	31
C - Character Length	30-27
D - Status-Micro*	26-23
E - Action*	22-20
F - Character Control	19-15
G - Status-Macro**	14-12
H - Assembly/Distribution	11-1
P - Word Parity	P

*Includes:

For Start-Stop Transmission (Send or Receive)

<u>Bit No.</u>	<u>Use</u>
26	Not-hold (0 to stop receiving on the channel, 1 to permit scanning)
25	Delay (to permit carriage return or other delays. Field H contains the length of delay, in bit times.)
24	Fractional Sampling (to lengthen last stop bit)
23	Data transfer check (echos the last data bit transferred)
22-20	Always zeros

For Synchronous Transmission (Send)

<u>Bit No.</u>	<u>Use</u>
26-23	Extended assembly area, when looking for character synchronization. Otherwise, the same as for synchronous-receive.
22-20	Always zeros

For Synchronous Transmission (Receive)

<u>Bit No.</u>	<u>Use</u>
26-25	Always zeros
24	On to indicate not-error
23	Data transfer check
22-20	Always zeros

**Includes:

For Any Transmission Activity

<u>Bit No.</u>	<u>Use</u>
14	1 for synchronous transmission 0 for start-stop transmission
13	1 for no error } for start-stop transmission. 0 for error } See note.
12	1 for send 0 for receive

Note: See "Slave-Master Control" under "Type 2 High-Speed Channel Adapter" for use of this bit in synchronous transmission.

Table 1. Channel Word Bits

Process Word: For all modes except the copy mode, the PWD will have one of the following interpretations:

<u>Field Name</u>	<u>No. of Bits</u>	<u>Position</u>
Instruction Counter	14	47-34
X	11	33-23
Y	11	22-12
Z	11	11- 1
Word Parity	1	P

or

<u>Field Name</u>	<u>No. of Bits</u>	<u>Position</u>
Instruction Counter	14	47-34
Operational Address Register	16	27-12
Z	11	11- 1
Word Parity	1	P

The second interpretation is used only with the address- and limit-moving instructions.

Copy Mode Process Word: During the process cycle of the copy mode, the control storage data register is interpreted as follows:

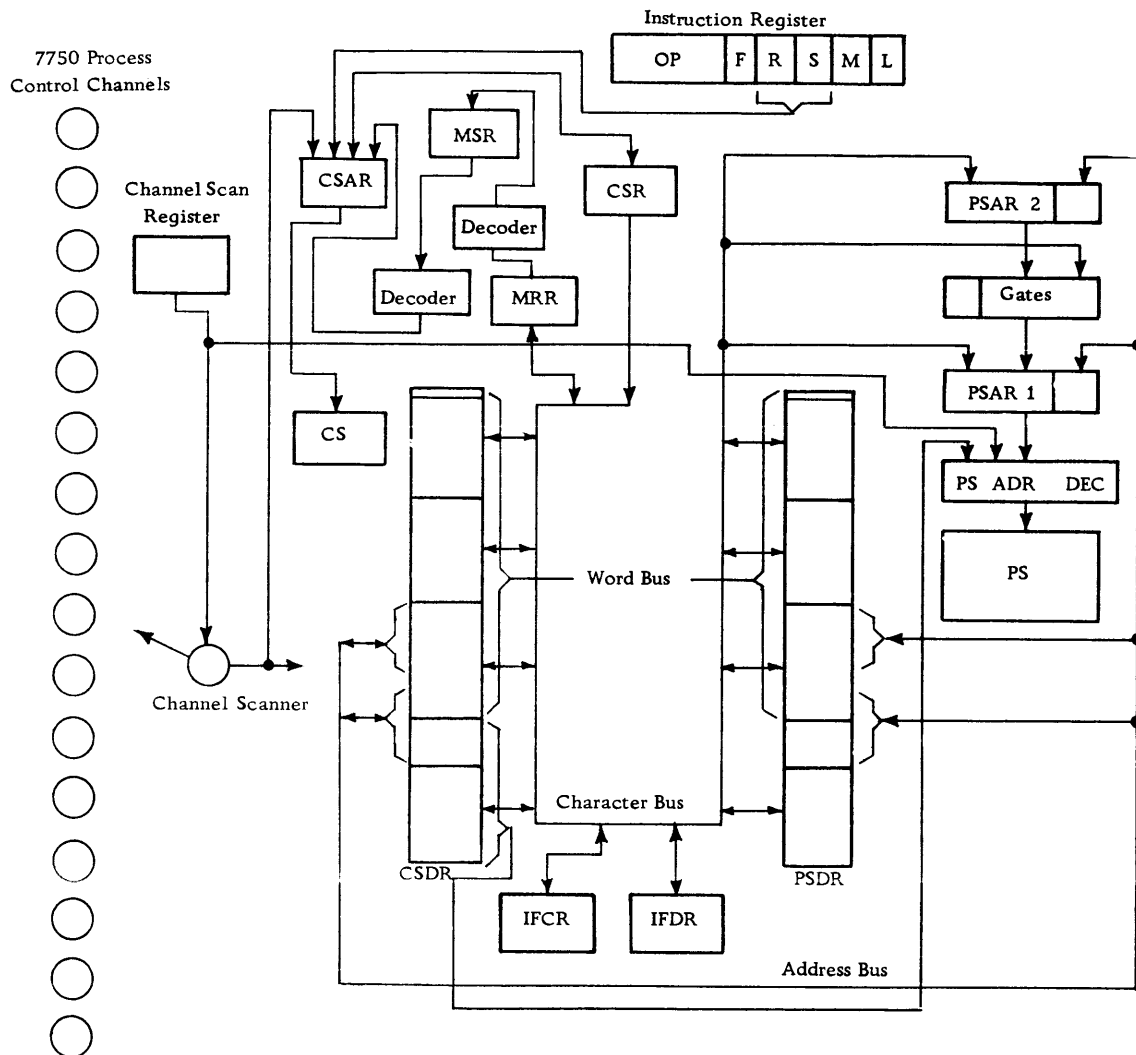
<u>Field Name</u>	<u>No. of Bits</u>	<u>Position</u>
Address	16	47-32
Limit	16	27-12
Z	11	11- 1
Word Parity	1	P

REGISTERS

Registers are temporary storage devices. They may be divided into two general types: addressable and non-addressable. Addressable registers can be addressed by the stored program, that is, an addressable register may be loaded, set, or requested by the programmer. Non-addressable registers cannot be addressed by the stored program. They are set and reset automatically at the proper time. Figure 5 shows the registers of the 7750.

Non-Addressable Registers

Although these registers cannot be manipulated directly by programming, their function affects bits in words that are used by programming.



LEGEND

CS Control Storage
 CSAR Control Storage Address Register
 CSR Channel Service Register
 CSDR Control Storage Data Register
 F Flag Bits
 IFCR Interface Control Register
 IFDR Interface Data Register
 L Length-of-Modification Field
 M Modifier Field
 MRR Mode Request Register

MSR Mode Select Register
 OP Operation Code
 PS Process Storage
 PS-ADR DEC Process-Storage Address Decoder
 PSAR 1 Process Storage Address Register 1
 PSAR 2 Process Storage Address Register 2
 PSDR Process Storage Data Register
 R Register Field (of Character to be Operated Upon)
 S Size Field (No. of Bits in R to be Operated Upon)

Figure 5. IBM 7750 Process Control Registers

Instruction Register: The instruction register is a 26-bit register that holds all of the instruction being executed, except the address. The first ten bit positions contain the operation code, the next two bit positions contain the flag bits, the last 14 bits contain the R, S, M, and L fields.

Mode Status Register: The mode status register is a five-bit-position register. Before the execution of each instruction, this register selects the bit associated with the highest priority mode from the priority requests contained in the mode request register. At any one time, the mode status register may contain only one bit (a logical one) to indicate the highest priority mode selected. If this register contains no logical one, the 7750 is operating in normal mode.

Process Storage Address Register 1: The process storage address register 1 (PSAR 1) contains the current address for addressing the process storage. Address modification takes place as the address is set into this register from the process address register 2 (PSAR 2). This register can hold 16 bits; 14 bits are used to address the correct word in storage, and two bits are used to specify a particular character (0, 1, 2, or 3) within a four-character word.

Process Storage Address Register 2: The process storage address register 2 (PSAR 2) temporarily stores a 16-bit address from the process storage data register or control storage data register. The address is transferred to the PSAR 1 when it is used to address the process storage.

Control Storage Address Register: The control storage address register (CSAR) contains the current address for addressing a channel word or process word in control storage.

Addressable Registers

Process Storage Data Register: The process storage data register is a 48-bit register that holds the word read from, or to be written into, process storage. This register can conform to any one of the three word formats in the process storage: the data word format, the limit word format, or the instruction word format.

Control Storage Data Register: The control storage data register is a 48-bit register that holds the word read from, or to be written into, the control storage. This register can conform to any one of the following word formats: channel word, process word, copy

mode process word, and scratch word (for optional use by the programmer).

Channel Service Register: The channel service register enables a channel requiring new storage space to identify itself to the channel service program. This register has seven bit positions to hold the channel address. When channel service is obtained during a character interrupt or a scan cycle, the channel service register is automatically set with the address of the channel needing service.

During the execution of storage-to-storage instructions while in channel service mode, the 7750 transfers the contents of the channel service register to the control storage address register to address control storage. This transfer is automatically done on the second process cycle of a two-cycle instruction that refers to the control storage while the machine is in channel service mode.

The four high-order bits, 11-8, are used to indicate certain errors to the program. These errors will be discussed in a later section of this manual. The programmer can unload or test bits in the channel service register. He cannot load the register. If a load instruction is executed, bits 11-8 will be reset to zero and bits 7-1 will remain unchanged.

Interface Data Register: The interface data register is a nine-bit-position register (eight bits plus one parity bit) which enables the 7750 to communicate with a computer. This register may be automatically loaded or its contents stored under program control. It may also be loaded or its contents automatically stored when data are transferred to or from the associated computer.

Interface Control Register: The interface control register, an 11-bit position register (Figure 6), controls the data flow between the IBM 7750 and the associated computer. This register may be loaded and its contents stored or modified under program control. Most of these bits may be set or reset automatically when the 7750 is transferring data to or from the associated computer. See Table II for meaning of the bits in the register.

Mode Request Register: The mode request register is a five-bit register that holds requests for priority mode service (Figure 7). The 7750 requests a certain mode by turning on the bit position associated with that mode in the mode request register. If more than one mode is requested, the 7750 will always select the highest mode first. If no mode is requested, the 7750 will execute the normal mode program. To leave a mode and go to a lower mode, the bit in the MRR corresponding to the higher mode must be turned off.

Bit No.	Name	Turned On (to 1) by:	Turned Off (to 0) by:
11	Service Response	Host computer as it responds to a request.	7750 copy mode controls (automatic)
10	Service Request	7750 copy-mode controls (automatic)	Service response (automatic)
9	Interface Reset	Host computer when that computer is reset either manually or by program. (Whenever this bit is on, all other bits in this register go to 0 and remain so until this bit goes off.)	7750 Programming: AND to the IFCR, with a 0 in the 9-bit position of the image character
8	Load	7750 program, or Operator's pressing Load key.	7750 program
7	Attention	7750 program	Receipt of automatic attention-response from host computer
6	Control	Host computer program	7750 program
5	Sense	Host computer program	7750 program
4	Stop	Automatic stop signal from host computer. At end of transmission from computer, it should be on.	7750 program
3	End	The 7750 program at the end of error-free transmission.	Receipt of automatic end-response from host computer
2	Unusual End	The 7750 program, upon sensing an error in the 7750 or transmission line	Receipt of automatic end-response from host computer
1	End Response	Automatically by an end-response signal from the host computer	7750 program

NOTES:

1. All of these bits can be turned on or off by 7750 programming, though in some cases, this would only be done for diagnostic programming.
2. To program bits 9, 10, and 11, use AND instruction with a 0 in the corresponding position of the image word to program the bit OFF, and 1 to leave it ON. To program one of these bits ON, use a LOD or IOR instruction with a 1 in the corresponding position.
3. One way to program the other bits is to use a load instruction with a 0 in the corresponding position of the image word to program the bit OFF, and 1 to program it ON.
4. All of these bits can be set OFF by manually pressing the reset key on the 7750.

Table II. Interface Control Register Bits

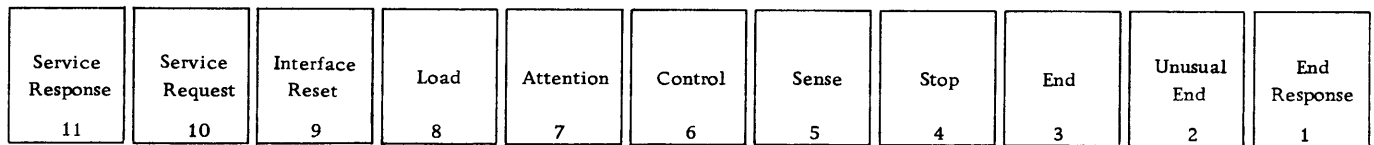


Figure 6. Interface Control Register

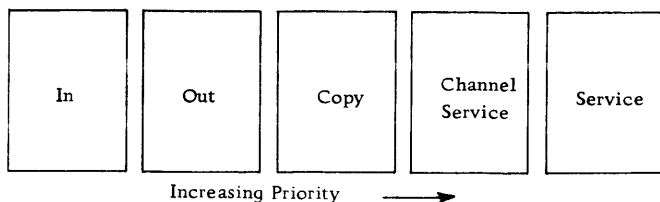


Figure 7. Mode Request Register

TIMING

The basic machine cycle of the 7750 is 28 microseconds. Most 7750 instructions are one-cycle instructions. Two-cycle instructions, which require 56 microseconds for execution, are the instructions used for indirect addressing and storage-to-storage data manipulations. An exception is branch indirect, which is one cycle.

For control storage operations, the basic machine cycle is divided into two storage cycles, scan and process, which are 11 and 17 microseconds long, respectively. During 7750 operation, the control storage goes through alternate cycles during which it performs the following operations:

1. Services one of the channels, assembling bits until a character has been accumulated, or sending bits until a complete character has been sent.
2. Provides the operational registers for the process storage to execute the instructions.

For process storage operations, the basic machine cycle is also divided into two cycles. These two cycles, the instruction cycle and the execute cycle, alternate and are 12 and 16 microseconds long, respectively. During an instruction cycle, the 7750 obtains an instruction; during the execute cycle, it executes the instruction.

The control storage and the process storage cycles overlap, allowing the information in either cycle of either storage to influence the operation of the other. In one machine cycle, the process storage goes through an instruction cycle and an execute cycle, while the control storage goes through a scan cycle and a process cycle. Because the process cycle of the control storage is 17 microseconds long, it overlaps the instruction and execute cycles of the process storage.

Clock Phases

The 7750 clock is composed of a 28-stage ring driven at a one megacycle rate. The clock cycles are divided into six phases, as shown in Figure 8. Four phases are used for single-cycle instructions, and all six are used for two-cycle instructions. During phase 1, the 7750 brings out an instruction from process storage, places it in the instruction register, and decodes it. During phase 2, the address contained in the instruction word is placed in PSAR 2. Later in phase 2, if there is no address modification, the address in PSAR 2 is transferred to PSAR 1 to address the process storage at the beginning of the execute cycle. If there is address modification, the 11 low-order bits of the address are modified as the address is transferred from

PSAR 2 to PSAR 1. The location and length of the modifier is given by the M and L fields of the instruction word. Modification is accomplished by replacing the L low-order bits of the address with L low-order bits from the register specified by the M field. The modified address is used to address the process storage at the beginning of the execute cycle. Because phase 2 is used to test S low-order bits of register R for zeros or ones to determine if the branch takes place, address modification cannot take place during a branch on zero or a branch on ones instruction. The uses of phase 3 through phase 6 are determined by the types of instruction being executed.

One-Cycle Instructions

During phase 1, the 7750 brings out an instruction from process storage, places this instruction in the instruction register, and decodes it (Figure 8). At the beginning of phase 2, the address contained in this instruction is placed in PSAR 2, then moved into PSAR 1 for addressing process storage. At the end of phase 2, the instruction counter is incremented to address the next instruction at the beginning of the next machine cycle. If the instruction being executed is a skip type of instruction (where, under certain conditions, the next instruction is skipped), the instruction counter will be incremented again in phase 3. The use of the remainder of phase 3 and phase 4 depends on the type of one-cycle instructions to be executed.

Branch Instructions

At the beginning of phase 2 of a non-indirect, branch type instruction, the address contained in the process storage data register is not moved to PSAR 2. Therefore, the process storage address is not changed. In phase 3, the address in the process storage data register is placed in the instruction counter of the process word contained in the control storage data register. During phase 4, the instruction counter is put in PSAR 2 and later moved to PSAR 1 to address process storage. At some time in phase 4, the instruction word is read back into process storage and the process word is read back into control storage.

At the beginning of phase 2 of an indirect branch type instruction (Figure 9), the address contained in the process storage data register is placed in PSAR 2. This address is then shifted from PSAR 2 to PSAR 1. The remaining part of the cycle is used in the same manner as described above for non-indirect branch type instructions.

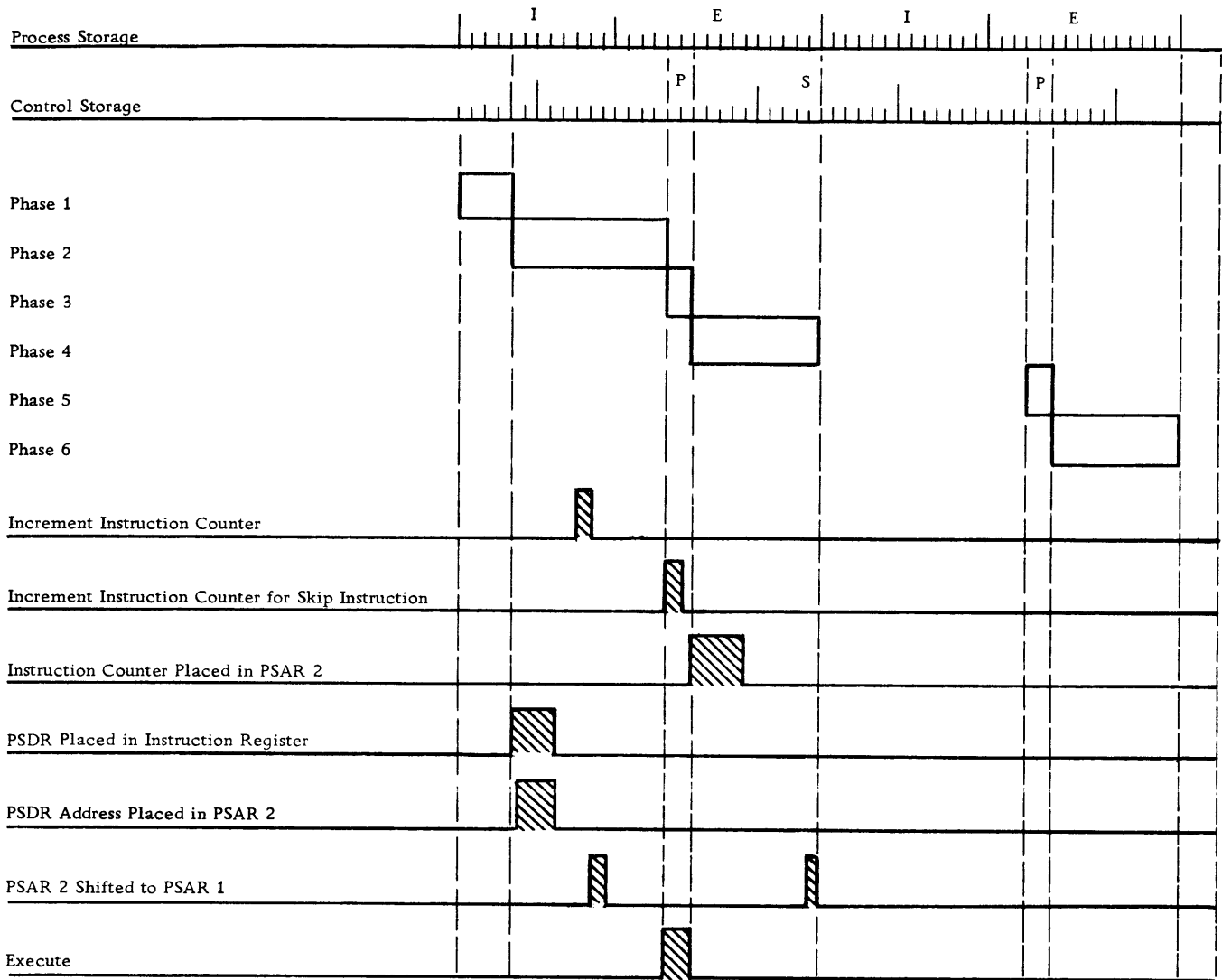


Figure 8. One Cycle Instructions

Compare-Address-to-Limit Instructions

During phase 3 of this type of instruction, the limit of the process storage data register is compared with the address. (In a 7750 with 8K storage, the high-order bit is ignored. In a 4K 7750, the two high-order bits are ignored.) If they are identical, the 7750 takes the next instruction in sequence. If they are not identical, the instruction counter is incremented to skip the next instruction. During phase 4, the instruction counter is placed in PSAR 2 and the data registers are stored.

Character- and Address-Moving Instructions

During phase 3 of a character- or address-moving instruction, the character or address is placed in the

correct register, such as the operational-address register (OAR) or the process storage data register (PSDR). At the beginning of phase 4, the instruction counter is placed in PSAR 2 and the data registers are stored.

Two-Cycle Instructions

Some instructions require more than two process storage cycles for execution. Phases 1 and 2 of these instructions are the same as those for one-cycle instructions. Phases 3 through 6 depend on the specific instruction.

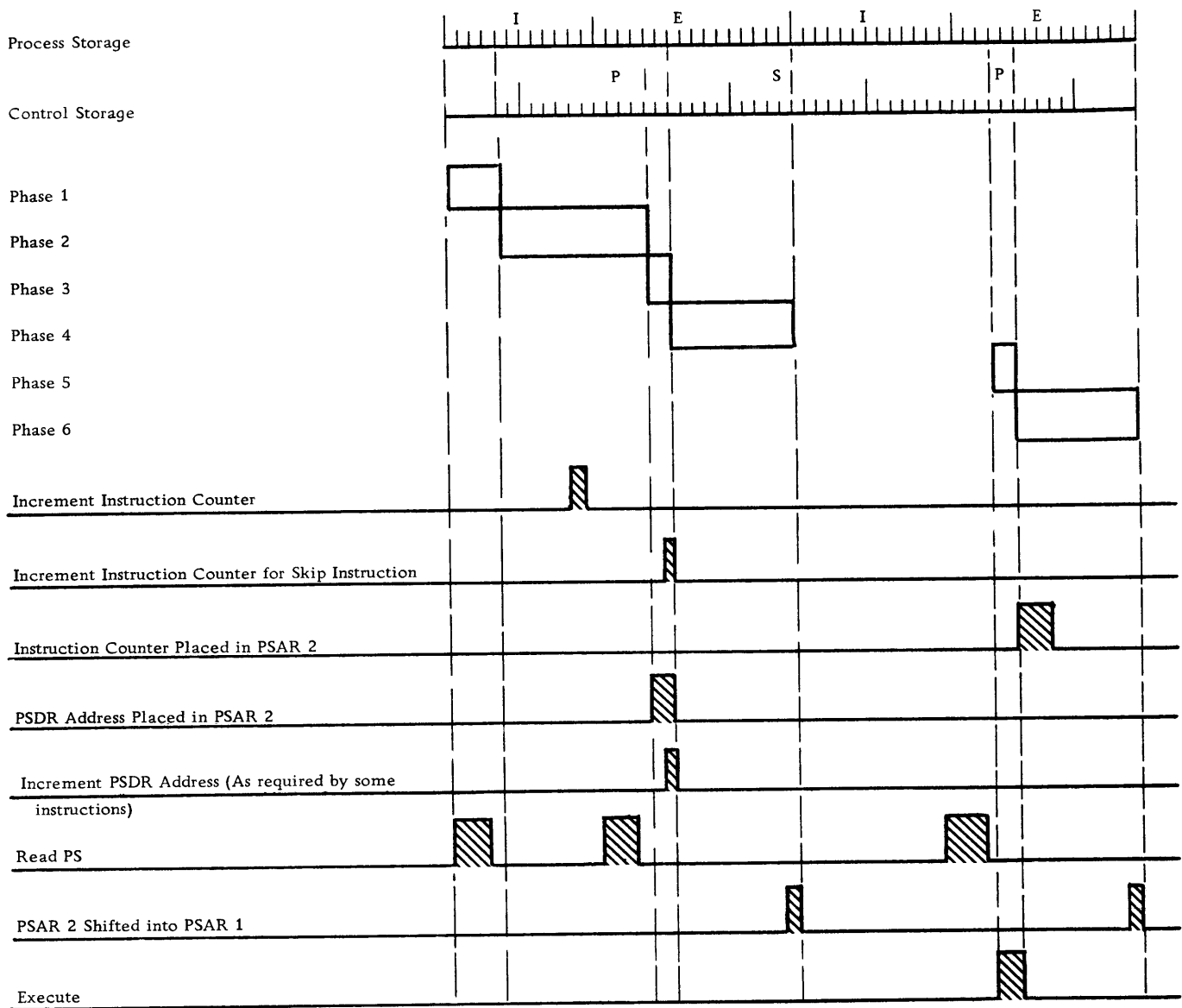


Figure 9. Indirect Instructions Except Storage to Storage

Indirect Instructions (Except Storage-to-Storage Instructions)

During phase 3 of an indirect type instruction other than branch indirect (Figure 9), the address in the PSDR is placed into the process storage address register 2. During phase 4, the address is incremented, if specified in the instruction, and the contents of the PSDR are read back into process storage. Just prior to phase 5, process storage is read using the indirect address. During phase 5, the instruction is executed. Phase 5 of an indirect instruction is similar to phase 3 of a non-indirect in-

struction. During phase 6, the instruction counter is placed in PSAR 2, the data registers are stored, and PSAR 2 is shifted to address the next instruction.

Storage-to-Storage Instructions

Phase 3 of a storage-to-storage instruction is idle (Figure 10). The instruction counter is placed in PSAR 2 during phase 4, as it will not be available from the CSDR for use during phase 6. If the instruction is indirect, the address of the process storage data register is placed in PSAR 1 at the end of phase 4. Since process storage has been written at this time, it is too late to increment the address.

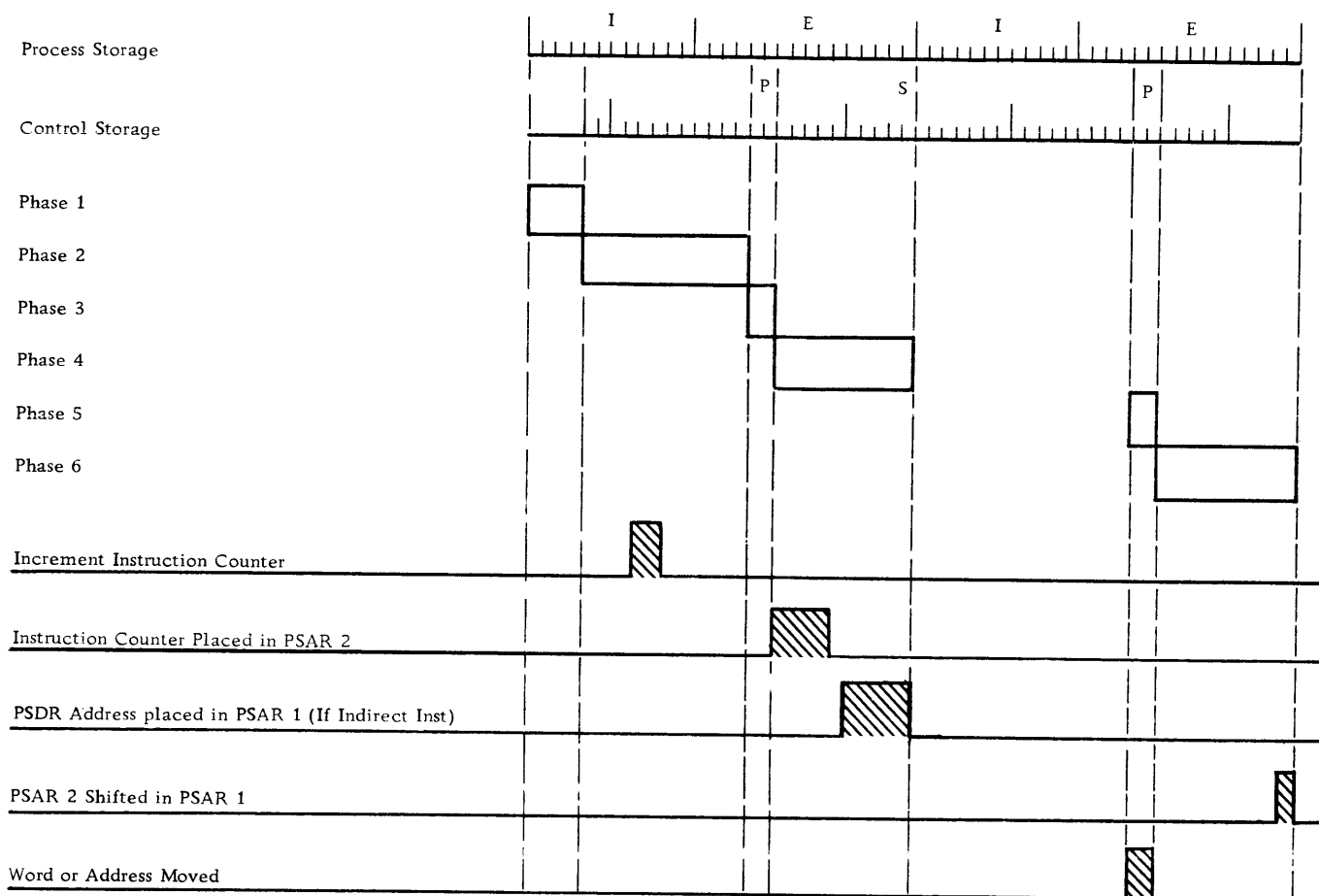


Figure 10. Storage Instructions

Therefore, there can be no indirect and increment storage-to-storage instructions. The appropriate control storage word is read out for the second process cycle prior to phase 5.* During phase 5, the address or word specified by the instruction is moved from one storage area to another. During phase 6, the data registers are stored. The instruction counter in PSAR 2 (placed there during phase 4) is put into PSAR 1 to address the next instruction.

INSTRUCTIONS

All 7750 instructions belong to one of four types:

1. Character-Manipulating Instructions - CH
2. Address- and Limit-Moving Instructions - AL
3. Storage-to-Storage Data Transfer Instructions - SS
4. Control Instructions - CT

* In modes other than channel service, the word is addressed by the seven-bit R and S fields of the instruction. In channel service mode, it is the word addressed by the channel service register.

The basic abbreviations of instructions are:

- A -- logical AND
- B -- BRANCH
- C -- COMPARE (address to limit)
- G -- GET (address or limit) from process storage for the operational address register
- I -- Inclusive OR (to a register)
- L -- LOAD (a character into X, Y, Z, IFOR, IFCR, or MRR register)
- M -- MOVE (a whole word)
- O -- Inclusive OR (to process storage)
- P -- PUT (an address from the operational address register into process storage)
- T -- TRANSMIT (an address)
- U -- UNLOAD (a character)
- X -- Exclusive OR

The pattern into which 7750 instructions fit appears in Table III.

Character Manipulation Instructions

<u>Instruction</u>	<u>Basic Operation</u>	<u>Indirect</u>	<u>Increment Address</u>	<u>Indirect and Increment Address</u>	<u>Complement</u>	<u>Complement Indirect</u>	<u>Complement and Increment Address</u>	<u>Complement Indirect and Increment Address</u>
Load Character	LOD	LOD*	LOI	LOI*	LDC	LDC*	LCI	LCI*
Unload Character	UNL	UNL*		ULI*	ULC	ULC*		UCI*
Exclusive OR	XOR	XOR*	XOI	XOI*	XOC	XOC*	XCI	XCI*
Inclusive OR	IOR	IOR*	IOI	IOI*	IOC	IOC*	ICI	ICI*
OR to Process Storage	ORP	ORP*		ORI*	OCP	OCP*		OCI*
AND	AND	AND*	ANI	ANI*	ANC	ANC*	ACI	ACI*

Address- and Limit-Moving Instructions

<u>Instruction</u>	<u>Address</u>	<u>Address Indirect</u>	<u>Limit</u>	<u>Limit Indirect</u>	<u>OR Address</u>	<u>OR Address Indirect</u>	<u>OR Limit</u>	<u>OR Limit Indirect</u>
Get	GTA	GTA*	GTL	GTL*	GOA	GOA*	GOL	GOL*
Put	PTA	PTA*	PTL	PTL*				

Storage-to-Storage Instructions

<u>Instruction</u>	<u>to Process Storage</u>	<u>to Process Storage Indirect</u>	<u>to Control Storage</u>	<u>to Control Storage Indirect</u>	<u>and OR to Control Storage</u>	<u>and OR to Control Storage Indirect</u>
Transmit Address	TAP	TAP*	TAC	TAC*	TOC	TOC*
Move Word	MWP	MWP*	MWC	MWC*	MOC	MOC*

Control Instructions

<u>Instruction</u>	<u>Unconditional</u>	<u>Indirect</u>	<u>On All Zeros</u>	<u>On Zeros Indirect</u>	<u>On All Ones</u>	<u>On Ones Indirect</u>	<u>On Test</u>	<u>Basic</u>	<u>Increment</u>
Branch	BRA	BRA*	BRZ	BRZ*	BRO	BRO*	BRT		
Compare Address to Limit								CAL	CAI

Table III. 7750 Instruction Set

Addressing

The IBM 7750 is a single-address machine. Each instruction contains one address for addressing storage. However, the addressing format of this machine includes address modification and indirect addressing.

Instruction Word Address - W

All 7750 instructions, except BRT, contain a 16-bit address (W) in bit positions 47 to 32. For direct, unmodified character-manipulating instructions, W

is the location, in process storage, of one of the characters to be manipulated. In the execution of the other three types of direct, unmodified instructions, the 14 high-order bits (47-34) address the word to be used in the execution of the instruction. (Bit 47 is ignored by a 7750 with 8K storage. Bits 47 and 46 are ignored on a 4K 7750.) The two low-order bits of the 16-bit address are not used because these instructions deal with words in storage rather than characters. With character-moving instructions, however, both the word and the specific character (0, 1, 2, or 3) within the word must be specified. Therefore, the complete 16-bit address must be used.

Address Modification

With the exception of all branch instructions other than branch indirect, the address W of any instructions may be modified by specifying a non-zero value for the L field of the instruction word. If L is zero, no modification takes place. If L is non-zero, the M field (bits 20–18) specifies the register containing the modifier; L is a binary number specifying the number of bits of the modifier to be used, counting from the low-order end of the specified register. L cannot be larger than 11. The effective address W_e is formed in the PSAR 1 by replacing the low-order L bits of W by the low-order L bits of the modifier in the register specified by M . The address W is read back into storage as W rather than W_e because modification is done in PSAR rather than PSDR. Figure 11 lists the values of M and the register each value specifies.

<u>R</u>	<u>M</u>	<u>Registers</u>
000	000	No register
001	001	X
010	010	Y
011	011	Z
100	100	Channel Service
101	101	Interface Data
110	110	Interface Control
111	111	Mode Request

Figure 11. Addressable Registers

Indirect Addressing

In executing directly addressed instructions, W_e is the location of one of the operands. When an instruction is executed indirectly, the operand is located at W^* ; W^* is the address (bits 47 through 32) contained in the word addressed by W_e .

Register Addressing - R, S, and OAR

All character-manipulating instructions deal with two character locations, one in process storage specified by W_e or W^* and the other a register specified by R (bits 29–27). S (bits 26–23) is a binary number specifying the size of the character to be operated on, counting from the low-order bit of the register specified by R . In character-manipulating instructions, S cannot be larger than eleven. Figure 11 lists the values of R and the register each value specifies.

Address- and limit-moving instructions automatically specify the OAR because, when such instructions are executed, the 7750 interprets the process word as having an OAR instead of Y and X registers. The OAR is composed of the Y register and five low-order bits of the X register. When an address or limit is moved into the OAR, the five low-order bits of the address or limit go to the five low-order bit positions of the X register; the 11 high-order bits of the address or limit go to the Y register.

Control Storage Addressing

Storage-to-storage instructions deal with two word locations: one in process storage, specified by W_e or W^* , and one in control storage, specified by R and S in all modes except channel service. In channel service mode, storage-to-storage instructions are executed using the contents of the channel service register to address control storage.

Address Incrementing

If the last alphabetic code character of an operation code mnemonic is an I , W^* will be incremented after its use. Address incrementing may occur whether or not W^* is used as an indirect address. Incrementing starts with bit 32 of the word addressed by W_e (bit 1 of W^*) and continue through bit 47. Regardless of the storage size (4K, 8K, or 16K) bits 46 and 47 are included in the incrementing process.

Indirect Addressing with Incrementing -- Skip

All 7750 instructions whose mnemonic codes end in I^* are skip instructions. If, after incrementing, bits 5–1 of W^* are all ones, the IBM 7750 executes the next instruction in sequence. Ones in bit positions 5–1 indicate that the 7750 has reached the last character position of a block. To proceed any further, the 7750 must locate a new empty block of characters when it is receiving data or a new block when it is transmitting data. Therefore, the next instruction in sequence is a branch instruction which enables the 7750 to enter the subroutine for locating the next block of characters to be sent out or the next empty block to be filled.

If bits 5–1 of W^* are not all ones after incrementing, indicating that the last (32nd) character position of the block has not been reached, the 7750 skips the branch instruction and executes the instruction following.

Flags

Bits 12 and 13 of an instruction word are flag bits. Any combination of these two flag bits may be used in an instruction. If bit 12 is a one, the Z register is decremented by one between the address modification and execution times of the instruction. If bit 13 is a one, no mode change can take place between the execution of the instruction containing this flag bit and the next instruction executed.

Operation Code

Bits 10 through 1 of the instruction word form the operation code. It specifies what instruction the 7750 is to do. Bit 11 is the odd parity bit for bits 10 through 1 and the flag bits.

DESCRIPTION OF INSTRUCTIONS

The instruction descriptions are arranged as follows in the text:

Instruction Name and Example:

Load Character Indirect, 2 LOD* W 1312

Where:

<u>2</u>	<u>LOD*</u>	<u>W(W_e)</u>	<u>1312</u>
Execution Length in Cycles	Mnemonic Op Code *Indirect Address	Direct, Unmodified, or Modified Address	Octal Op Code, Not Including Parity or Flags

NOTE: Unless stated otherwise, all instructions may be executed using $W_e = W$ modified by M and L. In all cases where modification is allowed, any of the registers in Figure 11, including no register, may be used.

Character Operations

None of the instructions in this group may be used to alter bits 1 through 7 of the channel service register. Specifying $R = 4$ on a load instruction will reset the error indicators (CSR 8-11), but will not change the rest of the CSR. All instructions whose mnemonic begins with X must specify $R = 1$, the X register. None of the instructions whose mnemonic begins with A can specify $R = 5$, the interface data register.

Load Character, 1 LOD W 1302: All bits of register R are cleared and the lower S bits are replaced by the corresponding bits of the character addressed by W_e . The contents of storage are unchanged.

Load Character Indirect, 2 LOD* W 1312: All bits of register R are cleared and S low-order bits are replaced by the corresponding bits of the character addressed by W^* , where W^* is the address (bits 47 through 32) contained in the word addressed by W_e . The contents of storage are unchanged.

Load Character and Increment, 1 LOI W 1322: The entire contents of register R are cleared. S low-order bits are moved into the low-order portion of register R from the character addressed by W_e . The 16-bit address (W^*) is incremented by one.

Load Character Indirect and Increment, 2 LOI* W 1332: The entire contents of register R are cleared. S low-order bits are moved into the low-order portion of register R from the character addressed by W^* . W^* is incremented by one. If, after incrementing, bits 5-1 of W^* are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The contents of storage location W^* are unchanged.

Load Complemented Character, 1 LDC W 1342: The entire contents of register R are cleared. One's complement of S low-order bits are moved into register R from the character addressed by W_e . The contents of storage location W_e are unchanged.

Load Complemented Character Indirect, 2 LDC* W 1352: The entire contents of register R are cleared. One's complements of S low-order bits are moved into register R from the character addressed by W^* . The contents of storage location W^* are unchanged.

Load Complemented Character and Increment, 1 LCI W 1362: The entire contents of register R are cleared. One's complements of S low-order bits are moved into register R from the character addressed by W_e . The 16-bit address (W^*) is increased by one.

Load Complemented Character Indirect and Increment, 2 LCI* W 1372: The entire contents of register R are cleared. One's complements of S low-order bits are moved into R from the character addressed by W^* . W^* is incremented by one. If, after incrementing, bits 5-1 of W^* are all ones, the 7750 executes the next instruction in sequence. If, after incrementing, bits 5-1 of W^* are not all ones, the 7750 skips the next instruction in sequence and executes the next instruction following. The contents of storage location W^* are unchanged.

Unload Character, 1 UNL W 1202: All 11 bits of the character addressed by W_e are cleared. S low-order bits of register R are moved into the low-order portion of the character field at location W_e . The contents of register R are unchanged.

Unload Character Indirect, 2 UNL* W 1212: All 11 bits of the character addressed by W^* are cleared. S low-order bits of register R are moved into the low-order portion of the character field at location W^* . The contents of register R are unchanged.

Unload Character Indirect and Increment, 2 ULI* W 1232: All 11 bits of the character addressed by W^* are cleared. S low-order bits of register R are moved into the low-order portion of the character field at location W^* . W^* is incremented by one. If, after incrementing, bits 5-1 of W^* are all ones, the 7750 executes the next instruction in sequence. If, after incrementing, bits 5-1 of W^* are not all ones, the 7750 skips the next instruction in sequence and executes the next instruction following. The contents of register R are unchanged.

Unload Complemented Character, 1 ULC W 1242: All 11 bits of the character addressed by W_e are cleared. One's complements of S low-order bits of register R are moved into the low-order portion of the character field at location W_e . The contents of register R are unchanged.

Unload Complemented Character Indirect, 2 ULC* W 1252: All 11 bits of the character addressed by W^* are cleared. One's complements of S low-order bits of register R are moved into the low-order portion of the character field at W^* . The contents of register R are unchanged.

Unload Complemented Character Indirect and Increment, 2 UCI* W 1272: All 11 bits of the character addressed by W^* are cleared. One's complements of S low-order bits of register R are moved into the low-order portion of the character field at W^* . W^* is incremented by one. If, after incrementing, bits 5-1 of W^* are all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The contents of register R are unchanged.

Exclusive OR, 1 XOR W 1101: The S low-order bits of register X are exclusive-OR'ed, bit by bit, with the corresponding bits of the character addressed by W_e . The result replaces the S low-order bits of X. The contents of storage and the 11 minus S high-order bits of X are unchanged. The result of an exclusive-OR between two bits is a one when the two

bits differ (10 or 01), and a zero when they are the same (11 or 00).

Exclusive OR Indirect, 2 XOR* W 1111: The S low-order bits of register X are exclusive-OR'ed, bit by bit, with the corresponding bits of the character addressed by W^* . The result replaces the S low-order bits of the X register. The 11 minus S high-order bits of register X and the contents at location W^* are unchanged.

Exclusive OR and Increment, 1 XOI W 1121: The S low-order bits of register X are exclusive-OR'ed, bit by bit, with the corresponding bits of the character addressed by W_e . The result replaces the S low-order bits of register X. The 11 minus S high-order bits of the X register are unchanged. W^* is incremented by one.

Exclusive OR Indirect and Increment, 2 XOI* W 1131: The S low-order bits of register X are exclusive-OR'ed, bit by bit, with the corresponding bits of the character address by W^* . The result replaces the S low-order bits of the X register. The 11 minus S high-order bits of register X are unchanged. W^* is incremented by one. If, after incrementing, bits 5-1 of W^* are all ones, the 7750 executes the next instruction in sequence. If, after incrementing, bits 5-1 of W^* are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The contents of storage location W^* are unchanged.

Exclusive OR Complemented, 1 XOC W 1141: The S low-order bits of register X are exclusive-OR'ed, bit by bit, with the one's complement of the corresponding bits of the character addressed by W_e . The result replaces the S low-order bits of X. The contents of storage and 11 minus S high-order bits of X are unchanged.

Exclusive OR Complemented Indirect, 2 XOC* W 1151: The S low-order bits of register X are exclusive-OR'ed, bit by bit, with one's complement of the corresponding bits of the character addressed by W^* . The result replaces the S low-order bits of X. The contents of storage location W^* and the 11 minus S high-order bits of register X are unchanged.

Exclusive OR Complemented and Increment, 1 XCI W 1161: The S low-order bits of register X are exclusive-OR'ed, bit by bit, with one's complement of the corresponding bits of the character addressed by W_e . W^* is incremented by one. The 11 minus S high-order bits of register X are unchanged.

Exclusive OR Complemented Indirect and Increment, 2 XCI* W 1171: The S low-order bits of register X are exclusive-OR'ed, bit by bit, with one's complement of the corresponding bits of the character addressed by W*. W* is incremented by one. If, after incrementing, bits 5-1 of W* are all ones, the 7750 executes the next instruction in sequence. If, after incrementing, bits 5-1 are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The contents of storage location W* and the 11 minus S high-order bits of register X are unchanged.

Inclusive OR, 1 IOR W 1102: The S low-order bits of register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W_e. The result replaces the S low-order bits of R. The contents of storage and the 11 minus S high-order bits of R are unchanged. The results of an OR between two bits is a one when either or both of the bits are ones (11, 10, 01) and a zero when they are both zeros (00).

Inclusive OR Indirect, 2 IOR* W 1112: The S low-order bits of register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W*. The result replaces the S low-order bits of R. The contents of storage location W*, the contents of location W_e, and the 11 minus S high-order bits of register R are unchanged.

Inclusive OR and Increment, 1 IOI W 1122: The S low-order bits of register R are OR'ed, bit by bit, with corresponding bits of the character addressed by W_e. The result replaces the S low-order bits of R. W* is incremented by one. The 11 minus S high-order bits of register R are unchanged.

Inclusive OR Indirect and Increment, 2 IOI* W 1132: The S low-order bits of register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W*. The result replaces the S low-order bits of R. W* is incremented by one. The contents of storage location W* and the 11 minus S high-order bits of register R are unchanged. If, after incrementing, bits 5-1 of W* are all ones, the 7750 executes the next instruction in sequence. If bits 5-1 are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following.

Inclusive OR Complemented, 1 IOC W 1142: The S low-order bits of register R are OR'ed, bit by bit, with the one's complement of the corresponding bits of the character addressed by W_e. The result replaces the S low-order bits of R. The contents of

storage and the 11 minus S high-order bits of R are unchanged.

Inclusive OR Complemented Indirect, 2 IOC* W 1152: The S low-order bits of register R are OR'ed, bit by bit, with the one's complement of the corresponding bits of the character addressed by W*. The result replaced the S low-order bits of R. The contents of storage location W* and 11 minus S low-order bits of register R are unchanged.

Inclusive OR Complemented and Increment, 1 ICI W 1162: The S low-order bits of register R are OR'ed, bit by bit, with the one's complement of the corresponding bits of the character addressed by W_e. W* is incremented by one. The result replaces the S low-order bits of R. The 11 minus S high-order bits of register R are unchanged.

Inclusive OR Complemented Indirect and Increment, 2 ICI* W 1172: The S low-order bits of the register R are OR'ed, bit by bit, with the one's complement of the corresponding bits of the character addressed by W*. The result replaces the S low-order bits of R. W* is incremented by one. If, after incrementing, bits 5-1 of W* are all ones, the 7750 executes the next instruction in sequence. If, after incrementing, bits 5-1 are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The contents of storage location W* and the 11 minus S high-order bits of register R are unchanged.

OR to Process Storage, 1 ORP W 1002: The S low-order bits of the register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W_e. The result replaces the S low-order bits of the character in storage. The contents of R and the 11 minus S high-order bits of the character in storage are unchanged.

OR to Process Storage Indirect, 2 ORP* W 1012: The S low-order bits of register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W*. The result replaces the S low-order bits of the character in storage. The contents of register R and the 11 minus S high-order bits of the character in storage location W* are unchanged.

OR to Process Storage Indirect and Increment, 2 ORI* W 1032: The S low-order bits of register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W*. The result replaces the S low-order bits of the character in storage. W* is incremented by one. If, after incrementing, bits 5-1 of W* are all ones, the 7750 executes the next

instruction in sequence. If, after incrementing, bits 5-1 of W^* are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The entire contents of register R and the 11 minus S high-order bits of the character in storage location W^* are unchanged.

OR Complement to Process Storage, 1 OCP W 1042: The one's complements of the S low-order bits of the register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W_e . The result replaces the S low-order bits of the character in storage. The entire contents of R and the 11 minus S high-order bits of the character in storage are unchanged.

OR Complement to Process Storage Indirect, 2 OCP* W 1052: The one's complements of S low-order bits of R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W^* . The result replaces the S low-order bits of the character in storage. The entire contents of register R and the 11 minus S high-order bits of the character in location W^* are unchanged.

OR Complement to Process Storage Indirect and Increment, 2 OCI* W 1072: The one's complements of S low-order bits of R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W^* . The result replaces the S low-order bits of the character in storage. W^* is incremented by one. If, after incrementing, bits 5-1 of W^* are all ones, the 7750 executes the next instruction in sequence. If, after incrementing, bits 5-1 of W^* are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The entire contents of register R and the 11 minus S high-order bits of the character in storage location W^* are unchanged.

AND, 1 AND W 1145: The S low-order bits of the register R are AND'ed, bit by bit, with the corresponding bits of the character addressed by W_e . The result replaces the S low-order bits of R. The contents of storage and the 11 minus S high-order bits of R are unchanged. The result of an AND between two bits is a one when both bits are ones (11) and a zero otherwise (10, 01, 00).

AND Indirect, 2 AND* W 1155: The S low-order bits of register R are AND'ed, bit by bit, with the corresponding bits of the character addressed by W^* . The result replaces the S low-order bits of register R. The contents of storage location W^* and the 11 minus S high-order bits of register R are unchanged.

AND and Increment, 1 ANI W 1165: The S low-order bits of register R are AND'ed, bit by bit, with the corresponding bits of the character addressed by W_e . The result replaced the S low-order bits of register R. W^* is incremented by one. The 11 minus S high-order bits of register R are unchanged.

AND Indirect and Increment, 2 ANI* W 1175: The S low-order bits of register R are AND'ed, bit by bit, with the corresponding bits of the character addressed by W^* . The result replaces the S low-order bits of register R. W^* is incremented by one. If, after incrementing, bits 5-1 of W^* are all ones, the 7750 executes the next instruction in sequence. If, after incrementing, bits 5-1 of W^* are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The contents of storage location W^* and the 11 minus S high-order bits of register R are unchanged.

AND Complemented, 1 ANC W 1105: The S low-order bits of register R are AND'ed, bit by bit, with the one's complement of the corresponding bits of the character addressed by W_e . The result replaces the S low-order bits of R. The contents of storage and the 11 minus S high-order bits of R are unchanged.

AND Complemented Indirect, 2 ANC * W 1115: The S low-order bits of register R are AND'ed, bit by bit, with one's complement of the corresponding bits of the character addressed by W^* . The result replaces the S low-order bits of R. The contents of the character at storage location W^* and the 11 minus S high-order bits of register R are unchanged.

AND Complemented and Increment, 1 ACI W 1125: The S low-order bits of register R are AND'ed, bit by bit, with one's complement of the corresponding bits of the character addressed by W_e . The result replaces the S low-order bits of R. W^* is incremented. The 11 minus S high-order bits of register R are unchanged.

AND Complemented Indirect and Increment, 2 ACI* W 1135: The S low-order bits of register R are AND'ed, bit by bit, with one's complement of the corresponding bits of the character addressed by W^* . The result replaces the low-order bits of R. W^* is incremented by one. If, after incrementing, bits 5-1 of W^* are all ones, the 7750 executes the next instruction in sequence. If, after incrementing, bits 5-1 of W^* are not all ones, the 7750 skips the next instruction in sequence and executes the instruction following. The contents of character location W^* and the 11 minus S high-order bits of register R are unchanged.

Address- and Limit-Moving Operations

Get Address, 1 GTA W 0702: The operational address register (OAR) is cleared, then loaded with the address in the word addressed by W_e . The contents of storage and the two high-order bits (10 and 11) of register X are unchanged. Bits 9-6 of the X register are cleared.

Get Address Indirect, 2 GTA* W 0712: The OAR is cleared, then loaded with the address in the word addressed by W^* . The contents of storage and the two high-order bits (10-11) of register X are unchanged. Bits 9-6 of the X register are cleared.

Get Limit, 1 GTL W 0302: The OAR is cleared, then loaded with the limit in the word addressed by W_e . The contents of storage and the two high-order bits of register X are unchanged. Bits 9-6 of the X register are cleared.

Get Limit Indirect, 2 GTL* W 0312: The OAR is cleared, then loaded with the limit in the word addressed by W^* . The contents of storage location W^* and the two high-order bits of register X are unchanged. Bits 9-6 of the X register are cleared.

Get and OR Address, 1 GOA W 0502: The contents of the OAR are OR'ed into the OAR with the corresponding bits of the address in the word addressed by W_e . The word in the process storage location W_e and the two high-order bits of register X are unchanged.

Get and OR Address Indirect, 2 GOA* W 0512: The contents of the OAR are OR'ed into the OAR with the corresponding bits of the address in the word addressed by W^* . The word in the process storage location W^* and the two high-order bits of register X are unchanged.

Get and OR Limit, 1 GOL W 0102: The contents of the OAR are OR'ed into the OAR with the corresponding bits of the limit in the word addressed by W_e . The word in the process storage location W_e and the two high-order bits of register X are unchanged.

Get and OR Limit Indirect, 2 GOL* W 0112: The contents of the OAR are OR'ed into the OAR with the corresponding bits of the limit in the word addressed by W^* . The word in the process storage location W^* and the two high-order bits of register X are unchanged.

Put Address, 1 PTA W 0602: The address field (bits 47 through 32) in the word addressed by W_e is cleared, then loaded with the contents of the OAR. The OAR is unchanged.

Put Address Indirect, 2 PTA* W 0612: The address field (bits 47 through 32) in the word addressed by W^* is cleared, then loaded with the contents of the OAR. The OAR is unchanged.

Put Limit, 1 PTL W 0202: The limit field (bits 27 through 12) in the word addressed by W_e is cleared, then loaded with the contents of the OAR. The OAR is unchanged.

Put Limit Indirect, 2 PTL * W 0212: The limit field (bits 27 through 12) in the word addressed by W^* is cleared, then loaded with the contents of the OAR. The OAR is unchanged.

Storage-to-Storage Data Moving Operations

Transmit Address to Process Storage, 2 TAP W 0606: The address (bits 47-32) from the control storage word replaces the address in the process storage word addressed by W_e . Control storage is unchanged.

Transmit Address to Process Storage Indirect, 2 TAP* W 0616: The address (bits 47-32) from the control storage word replaces the address in the process storage word addressed by W^* . Control storage is unchanged.

Transmit Address to Control Storage, 2 TAC W 0706: The address field (bits 47-32) of the control storage word referenced is cleared, then loaded with the address in the process storage word addressed by W_e . Process storage is unchanged.

Transmit Address to Control Storage Indirect, 2 TAC* W 0716: The address field (bits 47-32) of the control storage word referenced is cleared, then loaded with the address in the process storage word addressed by W^* . Process storage is unchanged.

Transmit and OR Address to Control Storage, 2 TOC W 0506: The address field (bits 47-32) of the control storage word referenced is OR'ed into itself with the address field of the word addressed by W_e . The word in the process storage location addressed by W_e is unchanged.

Transmit and OR Address to Control Storage Indirect, 2 TOC* W 0516: The address field (bits 47-32) of the control storage word referenced is OR'ed into itself with the address field of the word addressed by W*. The word in the process storage location addressed by W* is unchanged.

Move Word to Process Storage, 2 MWP W 0206: The contents of the control storage word replaces the contents of the process storage word addressed by W_e. The word in the control storage location is unchanged.

Move Word to Process Storage Indirect, 2 MWP* W 0216: The contents of the control storage word replace the contents of the process storage word addressed by W*. The word in control storage is unchanged.

Move Word to Control Storage, 2 MWC W 0306: The control storage word referenced is replaced by the process storage word addressed by W_e. The word in process storage location W_e is unchanged.

Move Word to Control Storage Indirect, 2 MWC* W 0316: The control storage word referenced is replaced by the process storage word addressed by W*. The word in process location W* is unchanged.

Move Word and OR to Control Storage, 2 MOC W 0106: The contents of the control storage word referenced are OR'ed into the control storage word referenced with the contents of the process storage word addressed by W_e. The word at the process storage location addressed by W_e is unchanged.

Move Word and OR to Control Storage Indirect, 2 MOC* W 0116: The contents of the control storage word referenced are OR'ed into the control storage word referenced with the contents of the process storage word addressed by W*. The word at process storage location addressed by W* is unchanged.

Control Operations

Branch type instructions other than branch indirect cannot have their addresses modified by M and L.

Branch, 1 BRA W 0707: This instruction causes the 7750 to take its next instruction from word location W and to proceed from there.

Branch Indirect, 1 BRA* W 0717: This instruction causes the IBM 7750 to take its next instruction from word location W* and to proceed from there. W* is the address at word location W_e. (See the paragraph on indirect addressing.)

Branch on Zero, 1 BRZ W 0704: If the S low-order bits of register R are all zeros, the 7750 takes its next instruction from word location W and proceeds from there. Otherwise, it takes the next instruction in sequence. Register R is unchanged.

Branch on Zero Indirect, 1 BRZ* W 0714: If the S low-order bits of register R are all zeros, the 7750 takes its next instruction from word location W* and proceeds from there. Otherwise, it takes the next instruction in sequence. Register R is unchanged. W* is the word addressed by W.

Branch on Ones, 1 BRO W 0744: If the S low-order bits of register R are all ones, the 7750 takes its next instruction from word location W and proceeds from there. Otherwise, it takes the next instruction in sequence. Register R is unchanged.

Branch on Ones Indirect, 1 BRO* W 0754: If the S low-order bits of register R are all ones, the 7750 takes its next instruction from word location W* and proceeds from there. Otherwise it takes the next instruction in sequence. Register R is unchanged. W* is the word addressed by W.

Branch on Test, 1 BRT W 0544: The contents of positions 33 through 23 of the instruction word are OR'ed with the contents of the register specified by the M field of the instruction word. If the result is all ones, the next instruction will be taken from the location specified in the address field (bits 47-34) of the BRT instruction word. If the result is not all ones, the 7750 executes the next instruction in sequence. The contents of the instruction word and of the register specified by M are unchanged.

Compare Address to Limit, 1 CAL W 0003: If the address and limit fields of the word addressed by W_e are identical, the 7750 executes the next instruction in sequence. If they are not identical, the 7750 skips the next instruction and goes to the instruction following. For an 8K 7750, bits 47 and 22 of the address and limit, respectively, are ignored in the compare operation. For a 4K machine, bits 47-46 and 22-21 of the address and limit, respectively, are ignored in the comparison.

Compare Address to Limit and Increment, 1 CAI W 0023: If the address and limit fields of the word addressed by W_e are identical, the 7750 executes the next instruction in sequence. If they are not identical, the 7750 skips the next instruction and goes to the instruction following. W* is incremented by one after the test. For an 8K 7750, bits 47 and 22 of the address and limit, respectively, are ignored in the

compare operation. For a 4K machine, bits 47-46 and 22-21 of the address and limit, respectively, are ignored in the comparison.

Sense, 1 SNS W 0000: The sense line, as specified by the M field (1 through 5)₈, is raised for 20 microseconds. This instruction is used for diagnostic purposes only.

PRIORITY PROCESSING

When the IBM 7750 is executing a program, the sequence of its operation is controlled by the instruction counter. Because the instruction counter is not an actual register but is a field stored in a control storage process word, a change in the sequence of operation can be accomplished by accessing a different process word and thus a different instruction counter. In the 7750, priority processing is accomplished by the use of six such process words. Each process word has a preassigned priority. The choice of a specific process word is based on the contents of the MSR.

The 7750 is in a particular mode when its sequence of operation is under the control of the process word associated with that mode. A mode is requested by the setting of its associated trigger in the mode request register. The normal mode, however, is always requested although it has no trigger. In all modes except copy mode, the 7750 operates as described below. The operation in copy mode is described in "Transmission Between the 7750 and the Computer." Figure 12 gives the priority, MRR position, and control storage address of each mode.

<u>Mode</u>	<u>Priority</u>	<u>MRR</u>	<u>Control Storage Address</u>
Service	1	1	37 ₈
Channel Service	2	2	77 ₈
Copy	3	3	137 ₈
OUT*	4	4	136 ₈
IN*	5	5	176 ₈
Normal	6	none	177 ₈

*The IN and OUT Modes correspond to the Write and Read operations. They refer to the data transmission relative to the IBM 7750.

Figure 12. Mode and Priority

Service Mode

The service mode has highest priority. In most cases, this mode is used for detecting errors, and the request of this mode is automatic through channel words and machine errors. In addition, the service mode, together with the service mode program, may be used to: (1) isolate or remove mistakes from a program (debugging); (2) locate a faulty component (diagnosing); and (3) obtain a programmed output of error messages when a machine malfunction occurs. Service mode may be entered manually from the operator's panel, automatically on the occurrence of an error condition, or by the program. The 7750 program must reset bit one in the MRR to leave this mode.

Channel Service Mode

Channel service mode has second priority; it causes the execution of the program that assigns blocks to receiving and transmitting communication channels. Channel service request is set automatically when any communication channels need it, and is turned off by the program.

Copy Mode

Copy mode has third priority and is requested by the program of in or out mode. When this mode is operative, data are automatically moved to or from the associated computer. Copy mode is not a program executing mode but is given a mode position because its function ranks in priority above all but service mode and channel service mode.

Out Mode

Out mode has fourth priority. Its mode program executes the necessary instructions to set up the copy mode process word and prepares the 7750 to transmit data to the computer. The out mode request bit is normally turned on by the program of the associated computer and is turned off by the IBM 7750 program. This mode may also be requested by the 7750 program. However, data transfer to or from the central processor can be performed only if the 7750 is placed in out or in mode operation automatically upon receiving a command from the processor.

In Mode

In mode has fifth priority. It is requested by the associated computer when the computer wants the 7750 to accept data from it. The program written

for this mode locates space for the data, sets up the copy mode process word to read the data into this area, and requests copy mode. The in mode request bit is normally turned on by the program of the associated computer and is turned off by the IBM 7750 program.

Normal Mode

Normal mode has lowest priority. It causes the execution of the normal program which performs error checking, code translation, recognition of functional codes, monitoring, queuing, and so on. All 7750 functions not specifically delegated to other modes usually are executed by the normal mode program.

Mode Selector System

The mode selector system enables the 7750 to change modes automatically. This system consists of a mode request register (MRR) and a mode status register (MSR). Both registers have five bit positions. Each bit position in the registers represents a specific mode. Normal mode is indicated when there are no bits appearing in either register. If more than one bit appears in the MRR, indicating more than one mode requested at one time, only the bit corresponding to the highest-requested mode appears in the MSR. Because the control storage is addressed by the mode status register, during the process cycle, the 7750 will always service the mode with the highest priority first.

At the end of the last execute cycle of each instruction, the MSR is checked against the MRR. If the check shows that the MSR is at the highest-requested mode, the next instruction, whose address is supplied by the previous process cycle of the current mode, is executed. If the check shows that the MSR is not at the highest-requested mode, and the instruction executed was not flagged "prevent mode change," the following sequence of events occurs: the MSR is updated to agree with the highest priority in the MRR; the mode change trigger is set to store the fact that a mode change is to occur; the following instruction and execute cycles are not used for a fetch and execute; instead, the updated MSR addresses the process word of the new mode in control storage; the instruction counter is used to address process storage on the second instruction cycle. The mode has now changed with a loss of one machine cycle.

If the instruction just executed had been flagged "prevent mode change," the change in the MSR and the setting of the mode change trigger would not have occurred. The change of mode would not have taken place until after the execution of an instruction not flagged "prevent mode change."

Note:

- (1) A character interrupt occurring at the same time as a mode change merely causes the mode change to be delayed.
- (2) A mode change cannot occur between the first and second cycles of a two-cycle instruction.

CHANNEL INPUT/OUTPUT

In the 7750, the sending and receiving of data is an automatic function controlled by a unique channel word located in the control storage for each communication channel. Receiving and sending of data require only occasional supervision from the program.

Incoming data arrive at the adapters where the data are converted (voltage levels, polarity, etc.) and sent to the control storage via the adapter control interface (Figure 13). Incoming bits are maintained in control storage until a complete character is received. Next, the character is automatically transferred to process storage. Outgoing data are sent to adapters serially by bit from control storage until a complete character has been transmitted. Then the next character is automatically obtained from process storage.

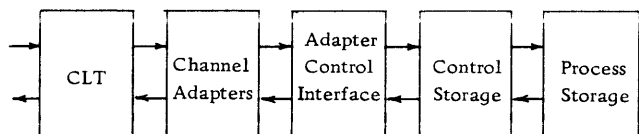


Figure 13. Data Flow

Adapter Control Interface

Figure 14 shows the lines which go between each of the process control channels and the associated adapters. Each line performs specific functions for controlling data flow between a process control channel and its associated adapter. Collectively, these lines form an interface -- the adapter control interface.

Process Control Channel Scanner Operation

The process control channel scanner steps from channel to channel, in sequence. It selects a process control channel every 28 microseconds (one machine cycle). The 7750 can have a maximum of 16 process control channels. Depending on the application, the process control channel scanner is pre-set to count up to the maximum number of process control channels used.

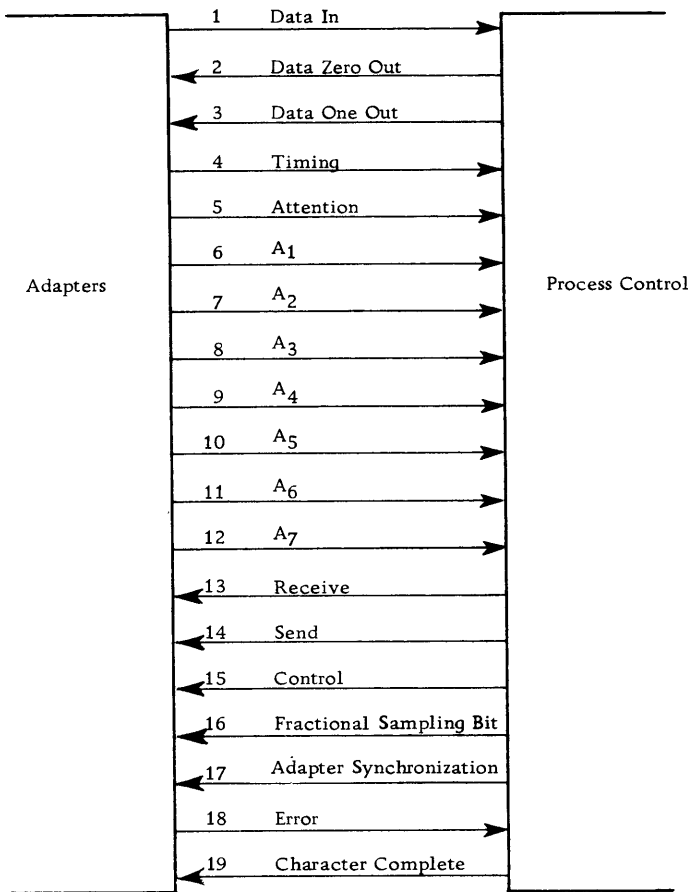


Figure 14. Adapter Control Interface

Channel Word

The channel word, a 48-bit word located in control storage, automatically controls the assembly and distribution of characters to and from the channel adapters. Each communications channel connected to the 7750 has a unique channel word associated with it stored in control storage. High-speed communication channels require the assignment of three or four words of control storage: one (if half-duplex channel) or two (if full-duplex channel) as channel words, and the other two for additional control functions (i.e., indicating high-speed channel errors). At the beginning of each scan cycle, the process control channel scanner selects a channel adapter. The corresponding adapter then provides the address of the correct channel word to the process control. Depending on the contents of this channel word, automatic character assembly and distribution take place. The channel word is then stored and the process control channel scanner incremented to select the next adapter for the following scan cycle. If, in a particular application, there are ten scan points, scan point one would be selected every 280 microseconds (ten machine cycles).

Channel Word Format

The fields composing the channel word are shown in Figure 15.

The assembly/distribution field, H, is an 11-bit shift register and count-down counter which contains all or part of a character being assembled or distributed. Characters are arranged in the H field with the first bit placed in the low-order position. The character length field, C, defines the number of bits per character. Fractional sampling bits are omitted when determining the character length.

Because four characters can be stored in each process storage word, the character field, A, defines the next character position in the process word to be assembled or transmitted. The character address field, A, defines the character location 00, 01, 10, 11 from which the next character is to be obtained during transmission or where the next character received is to be stored.

The word address field, W, defines the process storage word location of the next character position. It is automatically incremented when four character positions have been used.

In the G field, the high-order bit defines the type of character transmission: synchronous or start-stop. The next high-order bit, CSDR 13, is defined later in this manual for start-stop channel words and for synchronous channel words. The lower-order bit indicates whether the 7750 is sending or receiving data.

<u>Position Number</u>	<u>Name</u>	<u>Field</u>
47-34	Word Address	W
33-32	Character Address	A
31	Last Timing	B
30-27	Character Length	C
26-23	Status-Micro	D
22-20	Action	E
19-15	Character Control	F
14-12	Status-Macro	G
11-1	Assembly/Distribution	H
P	Word Parity	---

Figure 15. Channel Word Format

The last timing bit, B, is used in conjunction with the timing line of the adapter control interface to determine whether a new bit is to be transmitted or received by the process control. Following a bit transfer, the last timing bit is automatically set equal to the timing line.

Fields D and F are discussed in the following section. Their functions depend on the type of character transmission and the status of the channel word. The action field, E, is discussed in "Action Delaying Feature."

Character Assembly and Distribution

Characters are automatically loaded into the assembly area (H field) and sent to the channel adapter, serially by bit from the low-order position, at each new bit time.

For start-stop or synchronous data transmission, the four low-order bits in the character control field, F, form a binary counter which increments each time a new bit is sent to the channel adapter. When the bit count equals the character length, signifying that a complete character has been sent to the adapter, the next character is automatically obtained from process storage.

In receiving status, incoming bits are gated into the assembly area, as defined by the character length field, (C), and shifted toward the low-order bit position. For example, if C equals 118, the first bit and all succeeding bits of the character enter at CSDR bit position 9.

For synchronous-receive, the complete character is stored when the four low-order bits of F equal C. On start-stop receive, a different method is used to determine when a complete character is in the assembly area. The detection of the start bit shifting into the CSDR 1 and a stop bit shifting into H, as defined by the character length field (C), causes the character to be stored. Before storing the character, the assembly area is again shifted to strip the start bit from the character. On start-stop receive, the F field is not used as a counter.

Data Transfer Check

An automatic data transfer check is made on the data flow path between the process control and the channel adapter in send status. Each time a data bit is sent to the channel adapter, it is retained in the low-order position of the D field in the channel word. This low-order position of the D field is the transfer check bit (CSDR 23). When the IBM 7750 is sending data to a communication channel, the channel adapter sets the value of the last bit sent to the communication channel on the data-in line. When the next bit

is requested by the channel adapter, the transfer check bit is compared with the data-in line. If they are not equal, a channel error is indicated (see "Channel Error"). The MCA also makes a check on the data flow path between the MCA data bit and the output communications lines of the communications lines terminator (CLT).

Start-Stop Channel Words

Channel words would normally be assembled by the program in process storage and transferred to control storage to initiate character assembly or distribution. The channel word as it is used for start-stop channels is given in Figures 16 and 17. All unused bits must be logical zeros in start-stop channel words.

Certain rules are necessary to insure correct data transmission. One such rule is adapter synchronization. If a channel has been inactive, i. e., in hold status, or the data flow direction has changed, it is necessary to use the first active scan cycle to synchronize the adapter with the process control. This should not be confused with synchronous transmission. In the new channel word the programmer must set the character control field, F, to 14_g. On the first active scan cycle the channel word automatically performs the following functions:

1. The last timing bit is reset to a logical zero.
2. A data transfer check is inhibited and the transfer check bit reset to a logical zero.
3. The adapter synchronizer line is set to a logical one.
4. CSDR bits 11-1 are cleared.
5. The character control field is reset to 00_g for use as a bit counter.
6. If the channel is starting to send, the first character of the message is obtained from process storage.

In send status, for channels having character formats containing non-integer stop bits, the programmer must set the fractional sampling bit (bit 24) in the D field to a logical one. When bit count equals character length, signifying that the last stop bit is being sent to the adapter, the fractional sampling bit line of the adapter control interface is automatically set to a logical one. The adapter will then elongate this last stop bit by a predetermined interval. CSDR 19 in the F field of a start-stop channel word must always be set to a logical zero.

The programmer can automatically initiate a sending delay during the normal transmission of a message. The programmer inserts in the message a special character followed by a delay count equal to the desired delay in binary bit times. The special

character is called special sending delay character (SSDC) and has the following bit pattern: 3777g. During a character interrupt, the recognition of SSDC sets the delay bit in the D field to a logical one. If the channel word is not requesting channel service, character interrupt is initiated the next time this same channel word is accessed and the delay count is loaded into the H field. The maximum delay is 3775g. Each time the channel word is accessed and a new bit time occurs, the H field is decremented.

When the H field is decremented to all zeros, signifying the end of sending delay, the delay bit is turned off, and the next character is obtained from process storage to be transmitted in the normal manner. Neither the SSDC nor the delay count is sent to the channel, and neither can be located in the 32nd position of a block in process storage.

In data transmission, it is sometimes desirable to send a message and then wait for a reply on the same line, e.g., polling on half-duplex lines. The programmer can automatically initiate a status change in the channel word at the end of an outgoing message for this purpose. The recognition of a special character by the logic will place the channel word in a receiving delay status, during which time the logic examines the data-in line for a logical one, i.e., start bit of an incoming character. The recognition of a start bit places the channel word in normal start-stop receive for character assembly. If the delay interval times out, the channel word will be placed in a hold condition. The special character is defined as the status change character (SCC) and has the following bit pattern: 3776g.

To initiate a status change, the programmer inserts the status change character followed by a delay count character equal to the desired delay in binary bit time. The maximum delay count that can be used is 3775g. During a character interrupt, the recognition of SCC

Position Number	Name	Field
47-34	Word Address	W
33-32	Character Address	A
31	Last Timing	B
30-27	Character Length	C
26	Not Hold	D
25	Delay	D
24	Fractional Sampling Bit	D
23	Transfer Check	D
22-20	Action	E
19-15	Character Control	F
14-12	Status-Macro	G
11-1	Assembly/Distribution	H
P	Word Parity	---

Figure 16. Start-Stop Channel Word Format

FIELD	W	A	B	C	D	E	F	G	H	P
Number of Bits per Field	14	2	1	4	4	3	5	3	11	1
CSDR Bit Position Number	47-34	33-32	31	30-27	26-23	22-20	19-15	14-12	11-1	1
SEND*										
1. First Active Scan Cycle	Word Address of 1st Character	Character Address	0	02-13	10	0	14	3	0000	-
2. Normal Without Error	-----	-----	-	02-13	10-11	0	00-13	3	----	-
3. Normal Delay Without Error	-----	-----	-	02-13	14	0	00	3	----	-
RECEIVE*										
1. First Active Scan Cycle	Word Address of 1st Character	Character Address	0	02-13	10	0	14	2	0000	-
2. Normal Without Error	-----	-----	-	02-13	10	0	00	2	----	-
3. Normal Delay Without Error	-----	-----	-	02-13	14	0	00	2	----	-
INACTIVE, Send or Receive	-----	-----	-	-----	00-07	-	-----	0 to 3	----	-
*Without Fractional Sampling Bit Note: All numbers are in octal.										

Figure 17. Detailed Start-Stop Channel Word Format

sets the delay bit (CSDR 25) to a logical one. Character interrupt is again initiated the next time the same channel word is accessed under the following conditions: The data-in line is a logical zero, the channel word is not requesting channel service, and a timing change has occurred. When the data-in line is a logical zero and a timing change has occurred, the last character has been transmitted. The delay count character is loaded into the H field, the F field is set to 14g, and the low-order bit in the G field is set to a logical zero, that is, to receive status. On the next active scan cycle the octal code 14g performs the adapter synchronization function. Each time this channel word is accessed and a new bit time occurs, the H field is decremented. If at any time the data-in line becomes a logical one (the start bit of an incoming character), receiving delay is terminated, the assembly area is cleared, data are entered, and the delay bit turned off. Should the H field be decremented to all zeros, the not-hold bit (CSDR 26) is reset to a logical zero, placing the channel word in an inactive status. Neither the SCC nor the delay count character can be located in the 32nd position of a block of process storage (the block control character).

Synchronous Channel Words

The major difference between start-stop and synchronous transmission is the character format. To establish and maintain character synchronization, synchronous channels use special synchronizing characters instead of start and stop bits. However, once character synchronization has been established, incoming characters are stored regardless of the content of the assembly area. In some applications, it is also desirable to transmit synchronization characters, at predetermined intervals, to aid the maintenance of character synchronization.

In the G field, CSDR 13 is called the control bit. The value of this bit depends upon the type of HSA2, full-duplex or half-duplex. Refer to "Channel Adapter" for the correct use of the control bit.

Two types of character synchronization are available. They are hunt and continuous hunt. The choice of which type to use, or whether a combination of the two should be used, is determined by the particular application. The channel word format used for synchronous channels in receive status and send status is given in Figures 18, 19 and 20.

FIELD	W	A	B	C	D	F	F	G	H	P
Number of Bits per Field	14	2	1	4	4	3	5	3	11	1
CSDR Bit Position Number	47-34	33-32	31	30-27	27-23	22-20	19-15	14-12	11-1	P
SEND*										
1. First Active Scan Cycle	Word Address of 1st Character	Character Address	0	01-13	02	0	14	7	0000	-
2. Normal Without Error	-----	-----	-	01-13	02-03	0	00-13	7	----	-
RECEIVE*										
1. First Active Scan Cycle	Word Address of 1st Character	Character Address	0	01-13	00	0	14	6	0000	-
2. First Active Scan Cycle Going to Continuous Hunt	Word Address of 1st Character	Character Address	0	01-13	00	0	34	6	----	-
3. Normal Continuous Hunt	-----	-----	-	01-13	--	-	10-33	6	----	-
4. First Active Scan Cycle Going to Hunt	Word Address of 1st Character	Character Address	0	01-13	00	0	16	6	0000	-
5. Hunt	Word Address of 1st Character	Character Address	-	01-13	--	0	17	6	0000	-
6. First Active Scan Cycle Going to Hunt then Going to Continuous Hunt	Word Address of 1st Character	Character Address	0	01-13	00	0	36	6	0000	-
ERROR CHANNEL WORD	-----	-----	-	14-17	10-11	-	--	2	----	-
INACTIVE SEND OR RECEIVE	-----	-----	-	--	00-07	-	--	0 to 3	----	-

*Control Bit CSDR 13 Logical One
Note: All numbers are in octal.

Figure 18. Synchronous Channel Word Format

<u>Position Number</u>	<u>Name</u>	<u>Field</u>
47-34	Word Address	W
33-32	Character Address	A
31	Last Timing	B
30-27	Character Length	C
26-23	Extended Assembly Area	D
22-20	Action	E
19-15	Character Control	F
14-12	Status Macro	G
11-1	Assembly/Distribution	H
P	Word Parity	---

<u>Position Number</u>	<u>Name</u>	<u>Field</u>
47-34	Word Address	W
33-32	Character Address	A
31	Last Timing	B
30-27	Character Length	C
26-25	Not Used	D*
24	Not Error	D
23	Data Transfer Check	D
22-20	Action	E
19-15	Character Control	F
14-12	Status-Macro	G
11-1	Assembly/Distribution	H
P	Word Parity	---

Figure 19. Synchronous Channel Word Format--Receive Status

*All unused bits must be logical zeros in synchronous-send channel words.

Figure 20. Synchronous Channel Word Format -- Send Status

Before a channel word can be placed in hunt or continuous hunt status, it is necessary to use the first active scan cycle to synchronize the adapter with the process control. The character control field is used to perform this function. By setting the proper octal code in the F field, the programmer can make one of several sequences take place without further attention from the program. These sequences are:

1. Adapter synchronization going to normal synchronous receive.
2. Adapter synchronization going to continuous hunt.
3. Adapter synchronization going to hunt and then going to normal synchronous receive.
4. Adapter synchronization going to hunt and then going to continuous hunt.

In sequence one, the programmer inserts the octal code 14₈ in the F field. When a channel word containing this octal code is accessed on the first active scan cycle, the following automatic actions take place:

1. The last timing bit is reset to a logical zero.
2. The D field is cleared.
3. The adapter synchronization line is set to a logical one.
4. The four low-order bits in the F field are reset to 00₈ for use as a bit counter.
5. The H field is cleared.

After the adapter synchronization function has been completed, character assembly begins. The channel word is in a normal synchronous receive status.

In sequence two, the programmer inserts the octal code 34₈ in the F field. The high-order bit in

the F field defines continuous hunt. On the first active scan cycle the octal code 34₈ performs the adapter synchronization function as described in the previous paragraph. However, when the adapter synchronization is completed, the channel word is in a continuous hunt status and character assembly begins.

In continuous hunt, a 16-bit end-around shift register is formed using bits 11-1, 26-23, and the data-in line. A new bit is entered into the assembly area, as specified by C, and shifted toward the low-order position. The low-order position is equal to the character length plus one. If C equals 6, the low-order position is control storage data register 7. A maximum of fifteen bits is maintained in the shift register. As each new bit is received, the bit count is incremented and compared with the character length. If an equal comparison occurs, character interrupt is initiated, and those low-order bits in H, as specified by the character length, are transferred to process storage.

In continuous hunt, the 7750 examines the contents of the 16-bit assembly area at each new bit time. Character synchronization is established when the logic indicates that the proper synchronization pattern has been received. The four low-order bits of F are reset to 00₈ in preparation to count succeeding bits. However, the continuous hunt bit is not turned off. When bit count equals character length, those bits, as specified by C, are transferred to process storage. Only one synchronization pattern per process control channel can be used. The selection of the correct decoder is made by the process control channel scanner.

Note: There may be some difficulties inherent in the use of continuous hunt. Bit synchronization data may be transferred to process storage as if they were valid characters.

In sequence three, the programmer inserts the octal code, 16₈, in the character control field. When a channel word containing the octal code 16₈ is accessed on the first active scan cycle, the following action is initiated:

1. The last timing bit is reset to a logical zero.
2. The D field is cleared.
3. The adapter synchronization line is set to a logical one.
4. The four low-order bits of the F field are incremented to 17₈.
5. CSDR bits 11-1 and 26-23 are cleared.

After the adapter synchronization function has been completed, the octal code, 17₈, places the channel word in hunt status.

In hunt, a 16-bit end-around shift register is formed using bits 11-1, 26-23, and the data-in line. A new bit is entered into the assembly area, as specified by C, and shifted toward the low-order position. The low-order position of the 16-bit assembly area is equal to C plus one. For example, if C equals seven, the low-order position is control storage data register 8. A maximum of 15 bits is maintained in the shift register. As each new bit is entered, the F is not incremented and the characters are not transferred to process storage.

In hunt, 7750 examines the contents of the 16-bit assembly area at each new bit time. Character synchronization is established and hunt status is terminated when the logic indicates that the proper synchronization pattern has been received. The four low-order bits of the F field are incremented to 00₈ for use as a bit counter, and the channel word is in a normal synchronous receive status.

Logic is provided for two synchronization patterns. These patterns may be any combination of logical ones and zeros and have maximum lengths of 16 bits. Only one synchronization pattern per process control channel can be used. The selection of the correct decoder is made by the process control channel scanner. Hunt and continuous hunt must use the same synchronization pattern.

To initiate sequence four, the programmer inserts the octal code 36₈ in the F field. Sequence three is performed, followed by sequence two. A second adapter synchronization does not occur.

If a communication channel has been inactive, that is, hold status, or the direction of data flow has changed from receive to send, it is necessary to use the first active scan cycle to synchronize the adapter with the process control. In the new send channel word, the programmer must set the character control field, F, to 14₈ or 34₈. On the first active scan cycle, the channel word automatically performs the following functions:

1. The last timing bit is reset to a logical zero.

2. A data transfer check is inhibited, and the transfer check bit reset to a logical zero.
3. The adapter synchronization line is set to a logical one.
4. CSDR bits 11-1, 26-25 and 23 are cleared.
5. CSDR bit 24 is set to a logical one (not error).
6. The first character of the message is obtained from process storage.
7. The character control field is reset to 00₈ or 20₈ for use as a bit counter.

It is sometimes desirable to place the channel word automatically in a receiving hunt status at the end of an outgoing message. The programmer can change the channel word by placing a special character at the end of the message. This special character is called status change character (SCC), as described in the Start-Stop Channel Word Section, and has the following bit pattern: 3776₈. During a scan cycle, the recognition of SCC automatically sets the four low-order bits of the F field to 16₈ and the low-order bit in the G field to a logical zero, if the data-in line is a logical zero and a timing change has occurred. When data-in line is a logical zero with a timing change the last character has been transmitted. Depending on the high-order bit of the F field (continuous hunt), sequence three or four is initiated as previously described.

Channel Errors

A channel error is defined as an error, detected by the 7750, that occurred between the process control character assembly/distribution area and a remote terminal. The detection of a channel error is automatic, but the indication of the error -- its identity, where it occurred, and the corrective action to be taken -- is the responsibility of the program.

The present components attached to or contained in the 7750 may produce three different types of channel errors on high-speed and two different types of channel errors on low-speed communication channels.

Low-Speed Channel Errors

Data Transfer Error: The detection of this error is based on the same principles described in the "Data Transfer Check" section. The data transfer error can only be detected on channels in sending status.

MCA Parity Error: This type of error can be detected on all low-speed channels, regardless of their status. The multiplexing channel adapter has a storage with 32 control words, subdivided into four 11-bit control characters. Each control character in the storage is checked for odd parity. If, on a

matched scan cycle (i. e., when the MCA control character that is read out contains information for the same channel whose CWD is located in the CSDR at the same time), the MCA detects a parity error, this error is indicated to the process control via the adapter control interface error line.

Indication of Low-Speed Channel Errors to Program:

Control storage data register bit position 13 is used to tag the start-stop channel word when an error occurs. Bit position 13 is called not-error bit, that is, when CSDR 13 is a logical zero, an error condition is indicated. When a channel error occurs, the not-error bit is automatically set to a logical zero. If the start-stop channel word is active (not hold status), the address of the channel word is placed in the channel service register, service mode is requested, the channel error trigger (CSR 8) is set to a logical one, and the channel check trigger on the operator's panel is turned on, provided that:

1. CSDR 13 is a logical zero - indicating an error.
2. Channel service mode has not previously been requested.
3. Service mode has not previously been requested.

High-Speed Channel Errors

Control storage data register bit position 24 is used to tag the synchronous channel word when a data transfer check occurs. Bit position 24 is called the not-error bit, that is, a logical zero in CSDR 24 indicates an error condition. The detection of this error is based on the same principles described in the "Data Transfer Check" section. When a data transfer check occurs, the not-error bit (CSDR 24) is automatically set to a logical zero, the address of the channel word is placed in the channel service register, service mode is requested, the channel error trigger is set to a logical one, and the channel check trigger on the operator's panel is turned on, provided that:

1. CSDR 24 is a logical zero.
2. Channel service mode has not previously been requested.
3. Service mode has not previously been requested.

Time-out tag and interlock errors associated with high-speed adapter 2 (HSA2) for half- and full-duplex channels are discussed later in the HSA section. When a high-speed adapter detects one of the above errors, the adapter changes the address lines of the adapter control interface so that a CWD different from the normal CWD will be accessed the next time the adapter is selected. For each error condition a unique CWD is accessed in control storage. Hereafter, this new CWD is referred to as error channel word and

Position Number	Field	Logical State				
		Interlock		Time-Out Tag		
		HDX	FDX	HDX	FDX	
47-34	Word Address	W	(a)	(a)	(a)	(a)
33-32	Character Address	A	0	0	0	0
31	Last Timing	-	-	-	-	-
30-27	Character Length	C	(b)	(b)	(b)	(b)
26	Not Hold	D	(c)	(c)	(c)	(c)
25-23	Not Used	D	(a)	(a)	(a)	(a)
22-20	Not Used	E	(a)	(a)	(a)	(a)
19	Not Used	F	(a)	(a)	(a)	(a)
18-15	Character Control	F	(d)	(d)	(d)	(d)
14	Start-Stop	G	0	0	0	0
13	Not Error	G	1	1	1	1
12	Send/Receive	G	0	0	0	0
11-1	Assembly Area	H	(a)	(a)	(a)	(a)
HDX	Half Duplex					
FDX	Full Duplex					
(a)	May be used by the programmer					
(b)	Must be 17g - 14g					
(c)	Must be a logical one to activate ECWD					
(d)	Used to clear error condition from adapter					

Figure 21. Error Channel Words

uses a start-stop CWD format with a character length field greater than 13g. See Figure 21. The addresses in control storage are used to identify the type of error and the channel on which the error occurred.

When the ECWD is accessed, CSDR 13 is set to a logical zero, the address of the ECWD is placed in the channel service register, service mode is requested and the channel error trigger (CSR 8) turned on, provided that:

1. CSDR 26 (not hold) is a logical one.
2. CSDR 18-15 contains 00g.
3. Channel service mode has not previously been requested.
4. Service mode has not previously been requested.

In all cases except a time-out tag error, the channel check light on the operator's panel is turned on.

Identification of Channel Errors

Any type of channel error for high- or low-speed channels will automatically turn the operation of the IBM 7750 to the service mode. The program written for the service mode must have efficient routines for the quick identification of the specific error indicated and for the initiation of the corrective actions.

The program must examine the settings of the error bits (bits 11-8) in the channel service register

in order to execute the proper routine. Because each of the three high-order bits in the CSR represents one process control error, and only bit 8 can indicate one of the five different types of system errors, the programmer should check bit 8 first. Next, the programmer examines the contents of the seven low-order bit positions in the channel service register, and through cross references, identifies the channel in error and the type of error. Once the error and the source are identified, the desired action can be initiated without delay.

Corrective Actions for Channel Errors

There are no set rules or methods for handling channel errors; each error condition depends entirely on the configuration and requirements of each individual system application and must be presented in the system specifications. The environment of a communications network sometimes may be the source of conditions resulting in effects recognized as errors, when no error occurred. Therefore, the programmer may try out the error indication first to be sure of the presence of the signal error before initiating a complicated error procedure. To do this, the programmer must eliminate the error indication by resetting channel words to not-error status and keep a count for each error type, by channels, at certain storage locations. If the indicated error has been a legitimate error, the service mode will be requested repeatedly in consecutive scan cycles for that specific channel after each resetting; the count will rapidly reach the predetermined number required to execute certain error routines. At this time, the counter must be reset because it is possible that the same "illegitimate" error counts.

The 7750 machine operation should be kept in the service mode for as short a time as possible. The 7750 should only initiate, not execute, error routines in this mode. Executing error routines in the service mode would block other channels from obtaining service for this or other modes.

When a time-out tag error occurs, the service mode program must load the 14₈ adapter synchronization pattern into bit positions 18-15 of the affected error channel word immediately after the identification of the error. This resets the error condition in the channel adapter.

If a "legitimate" error condition is found, the service mode program must inactivate the channel by setting bit positions 26 and 14 of the error channel word or the regular channel word (depending on which one is used for indicating the error) to logical zeros before turning control over to the error-handling mode. If no provision is made for this action, control will be repeatedly turned over to the service mode for the same error, until the error is corrected.

If the correction of a system error requires a comparatively long time, the traffic of the affected channel probably will be rerouted. Normally, the computer will initiate such an order. The system specifications and the 7750 program must have made provisions for these cases in advance.

The service mode program must turn the channel error bit (bit 8) in the channel service register off before the service mode request bit is turned off in the mode request register. This should be done by the instruction immediately preceding the one that turns the service mode request bit off. If the instruction for turning the channel service register off is given sooner, the contents of the seven low-order bit positions of the channel service register may be destroyed before the service mode program is able to complete the necessary identification procedure.

Each time an end-of-block is recognized in a channel word, the machine logic first examines the status of the channel error bit in the channel service register. If this bit is off (logical zero) and the channel service mode request bit is off in the mode request register at the same time, the control storage address of the channel word requesting service is placed in the seven low-order bit positions of the channel service register. The channel service mode request bit is turned on in the mode request register. This will happen, whether the service mode request bit is on or off. Only the on status of the channel error bit prevents the machine logic from destroying the error-indicating channel-word address or error-channel-word address in the channel service register.

If the service mode program fails to turn the error channel bit off, however, the channel service mode is blocked for all channels until the bit is turned off. The channel error bit can be turned off by a load instruction (LOD) specifying the channel service register (C or 4) as an R register with a blank or zero S field; this instruction resets the four high-order bits (bits 11-8) in the channel service register at the same time.

Action Delaying Feature

In some cases, when working with high-speed lines, it is necessary to take some action relative to this line more rapidly than the normal IBM 7750 program is able to do. It also may be necessary to take this action after a delay of several character times. The sequence of recognizing a character, waiting one or more character times, and then taking some action relative to a high-speed line is called the action delaying feature. An example of its use may be found in 9000 series systems, in which it is necessary to recognize the go ahead character, wait one character time, and then raise the new sync line to the data set.

The action delaying feature enables the programmer to change the E, F, and G fields of the channel word automatically during character transmission. These new fields are stored in predetermined locations in process storage and must be loaded by the program. They are addressed by the position of the process control channel scanner which supplies A and the two low-order bits of W. The new E, F, and G field locations for process control channels 1-16 are permanently wired into addresses 37774, 0_8 to 37777, 3_8 , respectively, in a 7750 with a 16K storage. For an 8K storage, they are 17774, 0_8 , to 17777, 3_8 , respectively, and for 4K, they are 7774, 0_8 , to 7777, 3_8 , respectively.

A channel is put into the action-delaying mode by setting the low-order bit of the E field to a logical one in the appropriate channel word. A count equal to 3 minus the desired number of character delays is inserted into the two high-order bits of the E field. The IBM 7750 then examines in parallel the contents of the H field, searching for the action delay character, during character interrupt. One action delay character decoder is provided for each machine. Therefore, each 7750 with this feature can have just one (arbitrarily chosen) character perform this function.

In send status, the action delay character must be included in the number of character delays. However, in receive status, the action delay character is excluded when counting the number of character delays. When the action delay character is recognized, the low-order bit of the E field is turned off and the two

high-order bits incremented. During each succeeding character interrupt cycle, the two high-order bits are incremented until they change to logical zeros, signifying that the E, F, and G fields are to be changed at this time. The new fields are automatically transferred into the channel word during the E cycle of character interrupt. These fields will contain the bit pattern necessary to effect the desired change in action of this channel.

Character Interrupt

Character interrupt is the interruption of a normal machine cycle for the purpose of transferring a received character to process storage or obtaining a new character from process storage for transmission (Figure 22). The execution of a program is not disturbed at the time character interrupt occurs. However, character interrupt does delay the program by one machine cycle. If a request for a mode change occurs just before character interrupt, the mode change is delayed by one machine cycle.

The character interrupt trigger is set when a complete character has been received or transmitted. The address of the channel word is held at the control storage address register during the interrupted process cycle. The address (W) in the channel word addresses process storage prior to the interrupted I cycle. During the interrupted I cycle, the process storage is read, and the character is transferred via the character bus. In start-stop send, synchronous send, and start-stop receive, 11 bits are transferred.

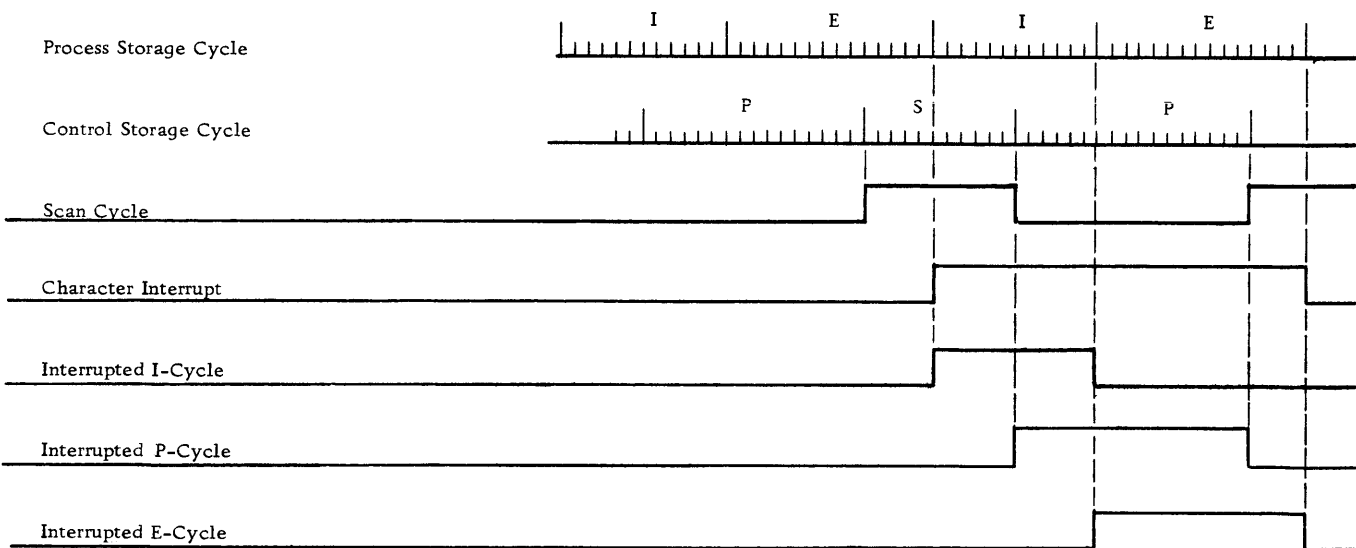


Figure 22. Character Interrupt Timing

In synchronous receive, only those bits specified by the character length in the channel word are transferred to the process storage. At the end of the interrupted I cycle, the word in PSDR is read back into process storage, and the channel word address (W) is incremented. If the five low-order bits of the incremented character address are all ones, channel service is requested. The channel word is re-stored at the end of the interrupted P cycle and character interrupt is terminated.

Channel Service

A channel service program obtains new blocks of storage for receiving channels, and locates the next new block of a sending chain for sending channels. The programmer must prepare a program for this function. The end of a block in storage is detected when the three low-order bits of W and the two bits of A are all ones. These five low-order bits request channel service. If the channel service mode request and channel error bits are off and the channel word does not indicate an error condition, the contents of the control storage address register are transferred to the channel service register. This preserves the address of the channel word requiring service. The channel service mode request trigger is turned on, and a mode change occurs at the appropriate time. The channel service mode select trigger initiates the channel service program and the channel word address is set to the starting address of a new block of storage. When channel service mode is completed, the channel service mode request trigger is reset by the programmer.

The failure of a channel to get service before a complete character has been received will result in the loss of the character. If a complete character is transmitted before channel service is obtained, logical zeros will be transmitted as the next character.

TRANSMISSION BETWEEN THE COMPUTER AND THE 7750

Two registers, the interface control register (IFCR) and the interface data register (IFDR), are used in conjunction with the necessary control circuits to transmit data or control information to the computer from the 7750 or to receive data control information from the computer. These two directions of transmission are the 7750 out and in operations, respectively. The interface control register is shown in Figure 6. The interface data register is a one-character buffer used to facilitate the character transfer.

Interface Control Register

Service Response Bit (Bit 11): This bit is set by the host computer when service request is answered, or by a load or inclusive-OR instruction with a bit in character position 11. When the service response bit is set by the host computer during copy mode, the controls allow the normal continuation of this mode. When this bit is set by the program (7750 not in copy mode), diagnostic testing can determine if it was set by such instructions as branch on test and branch on zero indirect. This bit can be reset automatically by copy mode controls, by the instruction AND to IFCR with no bit in character position 11, or by operator reset.

Service Request Bit (Bit 10): This bit is set automatically by copy mode controls or by the instructions LOAD or inclusive-OR to IFCR with a bit in character position 10. The setting of this bit allows the 7750 to provide service request to the host computer or diagnostic checking by the program. This bit may be reset automatically by copy mode controls on receipt of service response stop, or end response, or by:

1. Instruction AND to IFCR with no bit in character position 10.
2. Load or inclusive-OR to IFCR 11
3. Operator Reset

Computer Reset Bit (Bit 9): This bit is set by the fall of the operation "in" line or the instruction LOAD IFCR with a bit in character position 9. When set, this position resets all positions of the IFCR except IFCR 9. The in/out buffers, command response, copy mode controls, and copy mode request are all reset. This bit is reset by the instruction AND to IFCR with no bit in character position 9 or by operator reset.

Load Bit (Bit 8): This bit is set to a logical one by the 7750 program or manually by depressing the load key to allow the 7750 to differentiate between loading of three-bit bytes and character transfer. It is reset by the 7750 program or 7750 reset key. The output of the load bit is not interrogated by the host computer.

Attention Bit (Bit 7): This bit is set to a logical one by the 7750 program to send an attention signal to the host computer. The program specification must point out the condition permitting this signal to be sent. The attention bit is reset by the attention response signal from the host computer. It is also set when the load key is depressed.

Control Bit (Bit 6): This bit is associated with the in mode. The in mode program must test the status of this bit position to determine if a read or control command was sent. If the bit is on, the program must initiate the action specified for such a case. For example, when the control bit is on, the host computer can indicate that the next transmission is a control message not exceeding 10 characters; therefore, the 7750 in mode program may set a copy word for only one block. This block may represent a different area from the one used for data transmission. Provision can also be made to examine the contents of this control message as soon as its transmission is terminated. If the control bit is off, the host computer indicates normal transmission and the input area must be set up for data transmission. The in mode program may turn off the control bit. The control bit is also reset by the end response signal from the computer.

Sense Bit (Bit 5): This bit is associated with the out mode. The principles of operation for this bit, with reference to a read command, are the same as for the control bit in the in mode. This bit is turned on by the 7750 when it receives a sense signal from the host computer and is turned off by the same conditions that turn off the control bit.

Stop Bit (Bit 4): This bit is set by the host computer whenever it terminates a data transfer operation. Normally, an in operation is terminated by the host computer and an out operation by an equal compare of address and limit in the copy word of the 7750. This bit must be turned off by the 7750 out or in mode program.

End Bit (Bit 3): This bit must be turned on by the IBM 7750 out or in mode program to signal that a valid transmission to or from the host computer after the checking procedure following termination of a copy mode operation is completed. This bit is turned off by the 7750 upon the recognition of an end response signal from the host computer.

Unusual End Bit (Bit 2): This bit is turned on by the 7750 out or in mode program to signal an incomplete or invalid transmission to or from the host computer as a result of the checking procedure after a terminated copy mode operation. For resetting this bit, the same principles apply as for the end bit. The required corrective actions must be described in the host computer program.

End Response Bit (Bit 1): This bit is automatically set up upon reception of a signal from the host computer as a response for an end or unusual end signal.

The 7750 out mode or in mode program must reset all bits in the interface control register before turning the request bit off in the mode request register, causing the machine to leave the out or in mode.

The In Operation: Transmission from the Computer to the IBM 7750

In Mode

Transmission of data from the computer to the IBM 7750 can be initiated by the 7750 program. The program brings up the attention line to the computer via the attention bit in the IFCR. The computer then brings up the attention response line to the 7750 which resets the attention bit.

The computer must be programmed to bring up the control line or write line to the 7750. This may be done with or without a prior attention from the 7750. The control line sets the control trigger of the IFCR and the in trigger of the mode request register; the write line will set only the in trigger of the mode request register. This sets a command response trigger, the output of which is sent to the computer on the command response line. The 7750 then goes into the in mode, and the program examines the IFCR to determine whether write or control was given by the computer. The in mode program turns on the copy trigger of the mode request register (MRR), leaving the in trigger on. At the beginning of the next I cycle, copy mode commences.

Prior to entering copy mode, the program will have set up the copy word with the beginning (W) address and ending (Limit) address of the location where the data are to be stored. It is required that the programmer establish a maximum length for messages received from the computer. This determines the limit of the copy word.

During in mode, it is the responsibility of the programmer to insure that the IFDR is cleared before entering copy mode.

Copy Mode

When transmitting from the computer to the 7750, the latter, by setting the service request trigger on, will ask for a character on an average of every 14 microseconds (without interrupts) provided the computer answers by turning on the service response trigger and by placing a character on the write bus within 5.5 microseconds of the request. When the computer replies with a service response within the required time, the 7750 normally transfers the character to the appropriate location in the process storage data register (PSDR), and proceeds to the next character. When in copy mode, the 7750 increments the W address in

the control storage data register (CSDR-W) after each transfer of a character from the IFDR to the PSDR.

During normal operation of copy mode, the CSDR-W is placed in either process storage address register 2 or PSAR-1 to bring out of process storage the word into which the incoming character will be stored. The address register used is contingent upon the portion of the machine cycle during which the transfer takes place. Address transfer does not take place during character interrupt because the character bus is in use at that time.

Interruption or Termination of the In Operation

The normal transfer of characters into process storage may be interrupted or terminated for several reasons.

When the five low-order positions of CSDR-W become ones, the D character addressed contains the 11 high-order bits of the address of the next block in the chain. These 11 bits are transferred to the high-order positions of the CSDR-W and the 5 low-order bits of CSDR-W are cleared. This procedure sets up the correct process storage location for the next incoming character at the loss of one storage cycle.

In addition to the five ones test, the address and limit of CSDR are compared. If the addresses compare, the allotted storage space has been exhausted and the present or any future character of this message will not be received unless the programmer prepares a new chain for the remainder of the message. If the 7750 leaves copy mode because the address and limit compare equally, a service-request signal has already been issued to the host computer. Normally, the stop command from the host computer would cause the 7750 to leave copy mode. This equal comparison between address and limit is an unusual condition. A successful comparison of the address and limit of the copy word in CSDR sets an address compare trigger, resets the copy mode request trigger, and causes the IBM 7750 to go into the in mode.

The in operation will be terminated if the computer sends the stop signal. Stop resets copy mode request and causes the 7750 to revert to in mode. In this case, the in mode program turns on the end trigger of the IFCR after it has completed the necessary housekeeping which normally follows the termination of copy mode. If the 7750 program detects that an address compare caused termination of the in operation (by the stop trigger being off or service response on), the decision is left to the programmer whether the end trigger or the unusual-end trigger of the IFCR should be set at the end of in mode housekeeping.

The 7750 exits from copy mode with the address contained in the CSDR-W equal to one character location more than the location of the last character

stored. The block control character is not considered a character location in the chain.

The computer may send a service response and a stop signal at the same time. In this case, the 7750 will accept the character from the computer.

No character transfer, address incrementing, or address test can be performed during a character interrupt cycle.

A copy delay trigger is used to control the time at which copy mode operations are initiated and terminated. It delays the start of copy mode operations until a particular cycle time is reached and also delays the termination of copy mode into the next I cycle following the reset of the copy mode request trigger. Prolonging copy mode operations at the termination of copy mode is necessary to complete the character transfer in progress. If either channel service or service mode is requested, the copy delay trigger will delay the in operation until such time as the 7750 returns to copy mode to complete the in operation.

Copy Proceed and Inhibit Triggers

The IBM 7750 proceeds with the in operation by sampling the status of various triggers on an average of every 14 microseconds. The purpose of sampling is to control acceptance of characters from the computer to allow for conditions which interrupt character transfers. A copy proceed gate is used to control the sampling, which in turn determines any of the following conditions:

1. The character interrupt trigger is on.
2. The service request trigger is on. The computer has not answered the last service request.
3. The address compare trigger is on.
4. The five ones trigger is on.
5. The copy mode bit of the MRR is off.
6. The Z time-out trigger is on.
7. The copy mode status bit of the MSR is off.

The existence of one or more of the above conditions will set the inhibit trigger which will be used to stop the generation of various character transfer gates, the generation of the next service request, the incrementing of the CSDR-W, and the generation of various reset pulses. In this manner, the normal transfer of characters to process storage will be controlled.

In order to block incrementing the CSDR-W until the first character is accepted, the inhibit trigger will always be on during the first half-cycle of in or out operations. It can only be reset at copy proceed time during copy mode status if none of the six previously mentioned conditions is present. This prevents the IBM 7750 from proceeding with any character transfers until the condition causing the inhibit has been removed.

If the stop trigger of IFCR is on at copy proceed time, the copy mode request bit of the MRR will be reset.

Method and Conditions for Generating a Service Request

There are three separate conditions in which a service request will be issued during copy mode for the purpose of requesting transmission of a character from the computer.

The 7750 will issue a service request at the start of a message under a different set of conditions from those existing during the message transmission. If the in mode request trigger is on, and the service response trigger is off, the service request trigger will be set on when the copy delay trigger is set on. This and the program are the only circumstances under which a service request may be issued while the inhibit trigger is on.

Service requests will be made by the 7750 after each copy proceed if, at copy proceed, the inhibit trigger was off and the copy delay trigger was on. No service request will be issued at any time if the IFCR stop trigger is on during the time that the in mode request trigger is on.

If the inhibit trigger is off during the time the copy delay trigger is on, service response will be reset immediately after copy proceed, but before another service request is issued.

A service response or a stop signal will reset the service request trigger.

It is desirable to prevent the associated computer from tying up the 7750 in copy mode while the latter is waiting for a service response from the computer. The countdown counter in positions 11 through 1 (Z field) of the CSDR is used to count the number of 7750 cycles that elapse from the time a service request is issued until the computer makes a service response. The program sets all the Z field bits to logical zeros before setting the copy mode request bit of the MRR. The Z counter is decremented and then tested once each copy mode cycle. If all the bits in the Z field become logical zeros before the computer responds with a service response or a stop, the copy mode request trigger of the MRR is reset. The program returns to out or in mode, where it must determine the reason for leaving copy mode. It checks the IFCR for normal completion of the mode. It can also check the copy word for an address compare or a failure of the computer to respond. When the reason for leaving copy mode has been determined, the program takes the desired action.

The Out Operation: Transmission from the IBM 7750 to the Computer

The Out Mode Operation for Entry Into Copy Mode

The out operation is similar to the in operation previously described, although the data flows in the opposite direction. Much of the logical circuitry is common to both operations. The inhibit, copy delay, address compare, and five ones triggers are used for both operations.

Transmission of data from the 7750 to the computer can be initiated by the 7750 program. The program sends an attention signal to the computer via the attention bit in the IFCR. The computer then sends an attention response to the 7750, which resets the attention bit. The computer must be programmed to bring up either the read or sense line to the IBM 7750. The read line sets the out bit of the mode request register. The sense line sets the sense bit of the IFCR and the out bit of the mode request register (MRR) See Figure 7. The program for out mode will examine the IFCR to determine if the sense bit is on. Prior to entering copy mode, the program will have set up the copy word with the address and limit of the chain to be transmitted to the computer. The program then sets the copy bit of the MRR, leaving the out bit on. The copy mode has higher priority than out mode, and consequently the 7750 goes into copy mode at the start of the next I cycle.

Copy Mode Character Transfer

When transmitting from the 7750 to the computer, the 7750 indicates that it has placed a character on the read bus by turning on the service request bit. This is done twice every 28 microseconds, provided the computer accepts characters at this rate, and provided the 7750 is not interrupted by conditions described for the in operation. The 7750 will test the service response trigger every half cycle for the existence of a service response. When the computer responds by accepting a character and giving a service response, the 7750 will transfer the next character from the process storage to the IFDR and issue another service request.

Interruption or Termination of the Out Operation

The out operation is terminated in a similar way to the in operation.

As in the in operation, a test is made on the copy word for five ones in the low-order bits of the CSDR-W. Similarly, the new block location, in the case of a successful test, will be accessed from the PSDR while in copy mode.

A test is made for equality of the address and limit of the CSDR, as in the in operation. If the addresses are equal, the 7750 has transmitted the contents of the current chain and the copy mode request trigger is reset, causing the 7750 to revert to out mode if no higher modes are requested.

If neither the address compare test nor the five ones test is successful, CSDR-W is placed in PSAR2 or PSAR1 in order to access the process storage character which is to be transmitted to the computer. The character is taken from the PSDR, placed in the IFDR via the character bus, and the service request bit is turned on. The CSDR-W is again incremented and the previous two tests repeated.

The computer may terminate the out operation by sending a stop signal which sets the stop bit of the IFCR. The last character is available to the computer on the read bus at this time; the computer has the choice of taking or ignoring this character. The stop signal resets copy mode request, and causes the 7750 to revert to out mode. The end or unusual end trigger then is set as it was for the in operation.

The 7750 will exit from copy mode with the CSDR-W equal to one character location farther in the chain than the location of the last character transmitted. The block control character is not considered a character location in the chain.

After a successful address compare, the 7750 does not exit from copy mode during the out operation until the service response is received. This acknowledges that the computer has accepted the final character, which was on the read bus at the time. The Z field counter previously mentioned prevents the 7750 from becoming stalled in copy mode for lack of a computer service response.

The computer can give either a read or a sense command to the 7750 without the 7750 giving a prior attention signal.

A character interrupt, a mode change to a higher priority mode, or a failure of the computer to provide a service response signal within a specified time will insert delays between transmission of characters.

LOADING THE IBM 7750

Load Trigger and Load Counter

The load trigger in the IFCR controls loading and unloading of complete 48-bit words to and from process storage. This load trigger can be set from the load key on the operator's panel or by the 7750 program. When this trigger is on, the 7750 responds to a read, write, sense, or control command from the computer in a manner different from that previously described.

It executes the out or in operation normally except that 16 characters of three bits each are stored in or transmitted from a single word. A four-bit load counter is used to control the number of characters that can be loaded into each word. The 16 characters, which constitute one word, are placed into or received from the 1, 2, and 3 positions of the IFDR* and are stored in or taken from PSDR positions 47-45, 44-42, 41-39, 38-36, 35-33, 32-30, 29-27, 26-24, 23-21, 20-18, 17-15, 14-12, 11-9, 8-6, 5-3, and 2-P under control of the load counter. When a complete word is assembled into the 7750, position P, the word parity bit, is checked to insure proper loading. The load counter is reset after each 16 count and when the load bit of the IFCR is reset.

Loading Under Program Control

To load or unload the IBM 7750 by program, the 7750 is put into in or out mode in the same manner that was followed in the previous sections. When in out or in mode, however, the appropriate program sets the load trigger of the IFCR. The program then sets up the address and limit and turns on the copy mode request trigger. Loading or unloading starts from the address of the copy control word and continues in sequential storage locations until the computer signals stop or the limit and address of the copy word compare.

After a complete word has been assembled or transmitted from a given word address, the address of the copy control word is incremented by one word location, in order to access the next word in process storage.

The three-bit byte transmission is continued in the normal in or out mode. No test for five ones will be made when the load trigger is on. When loading or unloading is completed, the IBM 7750 proceeds to the program determined by the MRR.

Loading Under Manual Control

The 7750 must be in a program stop status at the time the operator initiates a manual load. All triggers and registers must then be reset by utilizing the reset switch or the clear switch, depending on whether the storages are to be cleared or to remain unchanged.

Pressing the load key will set on:

1. Load trigger of the IFCR
2. Manual load trigger
3. Attention trigger of the IFCR
4. Mode change trigger
5. Stop-start trigger

* Odd parity on these three bits is placed in IFDR 9 by the 7750 during unload.

The manual load trigger is kept on until the first word has been loaded or unloaded.

When the manual load trigger is on and no read or write command is received from the associated computer, the mode change trigger will be kept on. This prevents the 7750 from executing instructions and, consequently, from stopping on an operation code parity error on the words that were previously reset. A write command from the computer sets the in trigger of the MRR. Because the manual load trigger is on, the copy mode request trigger will be set on immediately, allowing the mode change trigger to be reset. When the copy P-word is read out for the first time during manual load, it is reset so that loading starts from address zero in process storage. When the 7750 goes into in mode, the in mode P-word is reset when first read out, causing the in mode program to start at the instruction in address zero of the process storage.

The address compare for the first 16 characters is inhibited by the manual load trigger. This trigger is reset when the first word has been assembled into the PSDR.

When loading of sufficient instructions is completed the IBM 7750 will revert to in or out mode because of a stop signal, address compare, or Z time-out condition. Thereafter, any further loading will be under control of the instructions previously loaded.

During both manual and program loading operation, the 7750 continues its scanning of the process control channels. The programmer must take precautions to insure that the scanning does not interfere with the loading routine. The control storage must be loaded by the 7750 program, which also resets the load trigger of the IFCR on completion of the loading routine. The Z counter operates in the same manner as for normal data transfers. That is, when the Z counter is decremented to all zeros, it causes the 7750 to exit from copy mode. However, the Z counter will not cause the machine to exit from copy mode until the first word has been completely loaded under manual load conditions.

As in the normal data transfer operations while in copy mode only, in mode or out mode, but not both, may be requested at any one time.

PROGRAMMING ASPECTS

Z Time-Out Trigger

During 7750 operation, it is desirable to prevent the computer from setting the stop trigger in the IFCR when the 7750 is not in copy mode. This allows the programmer (by testing the stop trigger) to get a true indication of the reason the machine left copy

mode. Otherwise, the Z-counter may decrement to all zeros and there is the possibility that the stop trigger may be set on after the 7750 leaves copy mode but before the programmer can test it. Then, it might be incorrectly concluded that the computer caused the exit from copy mode. The programmer may, consequently, branch to the wrong place in his program.

To insure correct operation, the output of the stop trigger is gated with the output of the Z time-out trigger. This trigger is set on when a Z-counter has all zeros. It is turned off whenever stop or service response are on during any of the succeeding times when the machine re-enters copy mode. While the trigger is on, the output of the IFCR stop trigger is de-gated to the character bus, thus making it appear to the programmer that the stop trigger is not on.

If the programmer finds the stop trigger off after exiting from copy mode, and that no address compare occurred, then he assumes that the Z-counter decremented out. Should stop come after the copy mode exit, the programmer can do one of two things:

1. He can set copy mode request and the 7750 will accept one character before exiting again.
2. He can give end or unusual end to the computer if he knows by system operation that the "Z-counter = 0" signal means an inoperative computer. (In the 7750 console, the Z-counter may decrement to zero many times between cards even though the card reader is operational.) In this case the computer end response will reset stop trigger and the Z time-out trigger.

He can turn on the interface reset (bit 9 of the IFCR) if the computer is inoperative. This will reset stop and Z time-out triggers and the in and out buffers.

Copy Address Compare Simultaneous with Five-Ones Condition

A problem arises when the programmer wishes to exit from copy mode because of an address compare and wishes to store all 31 characters in the last block. He cannot place an address with five low-order ones in the limit since it is necessary to exit from copy mode with the address one more than the location of the last character stored. (The block control character is not considered to be a position in the block.) Under these conditions, the address at the time the copy mode is finished cannot be predicted.

To solve this problem, place all zeros in the block control character of the last block and make the limit all zeros. When the five-ones condition occurs, the D field will be accessed and will set the address to zero also. The zeros in both addresses give an address compare and cause a correct termination of copy mode.

Interface Parity

The 7750 computer interface uses odd parity. This odd parity is generated in the high-order bit of the IFDR when the 7750 is unloading. When BCD or other character codes are being sent on the read bus, the 7750 program will insert the odd parity bit. No parity check is wired in for incoming characters on the write bus. However, as mentioned in the section on loading, a parity check is made on all 48 bits when the 7750 has completed the loading of a full word.

Continuous Read or Write of One Storage Location

A method exists in the copy mode controls for continuously reading and writing one address in process storage. The programmer may execute this type of operation for diagnostic purposes by setting up a copy P-word so that the Z field contains logical zeros in all but the low-order bit position, which has a logical one. The contents of the address are the storage address to be used. The programmer then sets on the copy bit of the MRR leaving in and out bits off. This forces a Z time-out on the first cycle and the Z time-out trigger can then be used to hold the inhibit trigger on during the subsequent times the program re-enters copy mode. The advantage of this system is that two storage accesses per 28 microsecond cycle are possible, which is significantly faster than the same operation carried by 7750 instructions only. No service request is given to the computer by this method.

Use of Address Compare

This section discusses the use of address compare for copy mode termination. First, for in mode, if the addresses compare and the allotted storage space has been exhausted, the present and any future characters of this message are received unless the programmer prepares a new chain for the remainder of the message. The "present" character means that a service request is issued by the 7750 at the time it finds that the limit and address compare. If the computer sends a service response, then any information sent is not stored by the 7750. This extra service request may be prevented only if the computer or console gives a stop with a delay of no more than four microseconds from the time the previous service response was sent. If this extra service-request signal is sent, and the computer sends a character

and a service-response signal, then the service-response indicator will be on, and the character will be in the IFDR when the 7750 leaves copy mode. It is then up to the program to either store the character or go back to copy mode with another block of space, or else send an unusual-end signal.

It is difficult to terminate the output transfer of characters from the 7750. In order to transmit to computers at a maximum speed of two characters per machine cycle, it becomes necessary to set up the next process storage address before the service request for the previous character has been sent. Consequently, when a computer or console sends a service response followed by a stop, two address increments may take place after the last character is sent. It is, therefore, inadvisable to permit this type of termination of output operations. Alternatively, output operations should be terminated by one of two methods:

1. Address compare.
2. Stop issued during the time service request is on and not accompanied by a service response.

ERROR CHECKING

Checks

Full Word Transfer Check: When full words are transferred between control storage data register and process storage data register, the parity bit P is also transferred. After the transfer, a difference between the CSDR and PSDR indicates an error.

Parity Check: Process storage and control storage have a parity bit P associated with each word. Before writing into either storage, P is generated so that the word has odd parity. An odd parity check is made after reading a word from either storage.

Instruction Register Parity Check: An odd parity check is made on the operation code, bits 1-10, and flag data, bits 12 and 13, of the instruction register and the parity bit. Bit position 11 is the parity bit located in process storage data register, and is generated by the assembly program. When an instruction operation code is changed in the 7750, the operation code parity must be odd.

Clock Check: The clock in the 7750 is checked for (a) multiple pulses or (b) no pulses.

Channel Check: There are 16 channel check lights mounted on the operator's panel, one for each 7750

process control channel. Because each high-speed communication channel is connected to one (or two if full-duplex) 7750 process control channel through a high-speed channel adapter, each light numbered represents a corresponding high-speed communication channel. Therefore, if a channel check light goes on, it means that a channel error has occurred in the high-speed channel associated with that light.

For low-speed operations, when a channel check light goes on, it indicates that a data transfer error has occurred on one of the low-speed communications channels attached to the MCA; or that an MCA storage parity error has occurred. The number of the channel check light is not associated with the low-speed communication channel in error, but with the MCA it is connected to.

Error Procedure

Whenever an error occurs, the 7750 sets the error trigger and either requests service mode or stops the machine, depending upon the setting of the check switch. Two types of errors, clock check and instruction parity check, always stop the machine. A channel check always requests service mode if the channel word is active. The remaining checks, full word transfer check and parity checks (either process storage or control storage), can stop the 7750 or request service mode. Whether to stop the machine or to request service mode depends on the position of the check switch on the operator's panel. If the check switch is set to the service position, the 7750 will go into service mode when any one of the three errors occurs.

The full word transfer, process storage parity, channel check, and control storage parity check triggers are actually part of the channel service register. Program instructions can unload, test, or reset these four positions. The execution of a LOD CSR instruction resets these four positions. If it is desired to bring the 7750 to a program stop status while the check switch is set to service position, the program must execute an instruction which contains an even parity configuration in the op code and flag data field.

If the check switch is set to the stop position, a full word transfer, process storage, control storage, or MCA parity check will stop the 7750 clock from advancing and the error condition will be displayed on the CE panels.

When a clock or instruction parity error is detected, the clock is halted in place and the program stop and check lights will come on. However, since the clock has not completed its cycle, the automatic lights will still be on. The operator's panel check indicator remains on until the reset key or clear key is pushed.

OPERATOR'S PANEL

The operator's panel (Figure 23) contains three groups of switches and lights:

Power Controls and Indicators

Switches and Keys

Power off/Power on
DC on
DC off

Lights

Thermal
Power on
DC on
Circuit breakers
Blower

Control Switches and Keys

The Stop Key sets the stop-start bit to stop status at the end of the execution of a machine cycle. When the stop-start bit is set to stop status, the clock continues to step until the early part of I time of the next machine cycle.

The Start Key starts the clock. The IBM 7750 must be in program-stop or clock-hold status for this key to be effective.

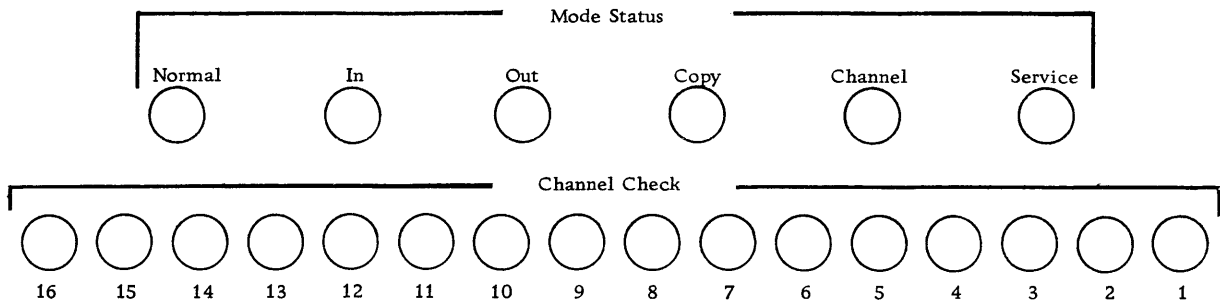
The Load Key sets the load bit and the attention bit in the interface control register, and starts the 7750 clock, enabling the associated computer to load the 7750. The 7750 must be in program-stop status for this key to be effective and reset or clear must have been depressed.

The Channel Reset Key resets all channel check indicators and MCA storage error triggers.

The Reset Key generates a reset to all internal latches and triggers. The 7750 must be in program stop status for this key to be effective and the automatic light must be off.

The Service Mode Key sets the service mode request bit on.

The Service-Stop Check Switch, when set in the service position, causes the 7750 to enter service mode when certain checks occur. When this switch is set to the stop position, the 7750 will go to clock hold status when certain checks occur.



(Light) Circuit Breaker	(Light) Thermal	(Light) Blower	(Light) Check	(Light) CE Test	(Light) CLT Wrap On	(Light) Interface Reset	(Key) Clear
(Light) Power On	(Light) DC On Light		(Key) Service Mode	Service (Switch) Check Stop	(Light) Load	(Light) Automatic	(Light) Program Stop
On (Switch) Power Off	(Key) DC On	(Key) DC Off	(Key) Reset	(Key) Channel Reset	(Key) Load	(Key) Start	(Key) Stop

Figure 23. Operator's Panel

The Clear Key clears both control storage and process storage and resets all registers and triggers. The 7750 must be in program stop or clock-hold status for this key to be effective.

Operation Monitors

Mode Status Lights, one for each mode, indicate which mode the 7750 is in. Each light goes off as the 7750 changes to another mode, i. e., only one light will be on at one time.

Channel Check Lights, one light for each channel, indicate that a channel error has occurred. See "Channel Check" under "Error Checking." It is possible to reset these lights by pressing the channel-reset key without interfering with the process control in the 7750.

The Check Light goes on whenever an error occurs in the process control. It can be turned off only by manual reset. See "Error Checking."

The CE Test Light goes on whenever the IBM 7750 process control or MCA is in customer-engineering test status. It goes off when the customer engineer turns a switch causing the 7750 to return to normal operation.

The CLT Wrap-On Light goes on whenever the communications line terminator is in wrap-around status (the CLT switch has been turned to WRAP). It goes off when the CLT switch (just below the patch panel) is turned to the forward position.

The Interface Reset Light goes on whenever the interface-control-register bit 9 is on. This bit comes on when the host computer has issued a reset instruction or manual reset causing the 7750 to reset: Z time-out, copy five ones, command-response triggers, and remainder of the interface control register (except position 9).

The Load Light indicates that the 7750 is loading information from (or unloading to) the host computer. The light stays on until the program resets the load bit in the interface control register.

The Automatic Light indicates that the 7750 is under the control of its own program, unless it has been halted by a check, in which case the program stop light would also be on. The light goes off when the main timing clock is not advancing (and all operations have halted normally).

The Program Stop Light goes on when the IBM 7750 clock stops or is held by an error condition or single-cycle step. It goes off when the clock starts and the automatic light goes on.

High-Speed Channel Indicators

In addition to the above switches, keys, and lights, a panel of high-speed channel indicators and speed selectors is included for each group of from one through four FM high-speed channels used in the system configuration. The operator sets the switches to the speed (600 or 1200 bits per second) of the transmission capability of the line and the remote equipment for each high-speed line. The lights reflect the operating status of each of the high-speed lines:

Request to Send (1, 2, 3, 4): The appropriate channel light comes on when the 7750 has data to send on this

high-speed line and has sent a request-to-send signal to the data set. It goes off when the channel word is changed to receive.

Clear to Send (1, 2, 3, 4): The appropriate channel light comes on following a clear-to-send signal from the data set (in response to a request-to-send from the 7750). It goes off as soon as the 7750 drops its request to send.

Subset Ready (1, 2, 3, 4): This channel light, when on, indicates that the 7750 is connected to the data set (modem for this channel) and that the data set has power on.

Carrier On (1, 2, 3, 4): This light indicates that either idle signals or data signals are being received from or sent to the remote end of the transmission line. It goes off as soon as an interruption occurs between the two terminals.

Receive Data (1, 2, 3, 4): This light indicates that data signals (binary) 1's are being received from the remote end of the transmission line. It goes off whenever data 1 bits are not being received. Consequently, to the operator it is a dim light, flicking on and off frequently.

Send Data (1, 2, 3, 4): This light indicates that the 7750 is sending data (1 bits) to the transmission line. It goes off whenever 1 bits are not passing out from the high-speed portion of the 7750.

The communications system of a customer may be composed of a number of different types of communications services. For example, there are telegraph machines, operating at 60, 75, and 100 wpm, employing both polar and neutral signaling. A variety of digital data sets, made by communications companies, are used. Few of these devices employ the same signal levels, or bit rates, and they must all be integrated into many Tele-Processing systems. In order to join the IBM 7750 economically to a customer's system, various channel adapters are used.

These channel adapters, according to type, perform a variety of functions. Some types control digital data sets, while others time-multiplex a number of low-speed communication channels into one or more high-speed channels.

The principles underlying the design of the various adapters are those of providing flexibility to meet the needs of the customer, while taking advantage of the power of a stored program processor to reduce the cost and complexity of the equipment per communications channel.

MULTIPLEXING CHANNEL ADAPTER

The Multiplexing Channel Adapter (MCA) is a channel concentrator and speed changing device (Figure 24). It derives data from a number of incoming channels by a scanning and sampling technique, and transfers these data, together with generated timing, to the process control. The MCA accommodates up to 28 low-speed, half-duplex channels plus one test channel and communicates with the process control via one or more high-speed communications channels. The maximum bit rate on a channel connected to an MCA is dependent on the number of low-speed channels into the MCA, the number of high-speed channels into the process control, and the number of process control channels to which the MCA is connected.

The low-speed channels are divided into low-speed line adapter sets of four channels each, and all channels within a set must operate at the same bit rate.

There are a total of seven sets available per MCA. The bit rate per set may be any value up to the limits

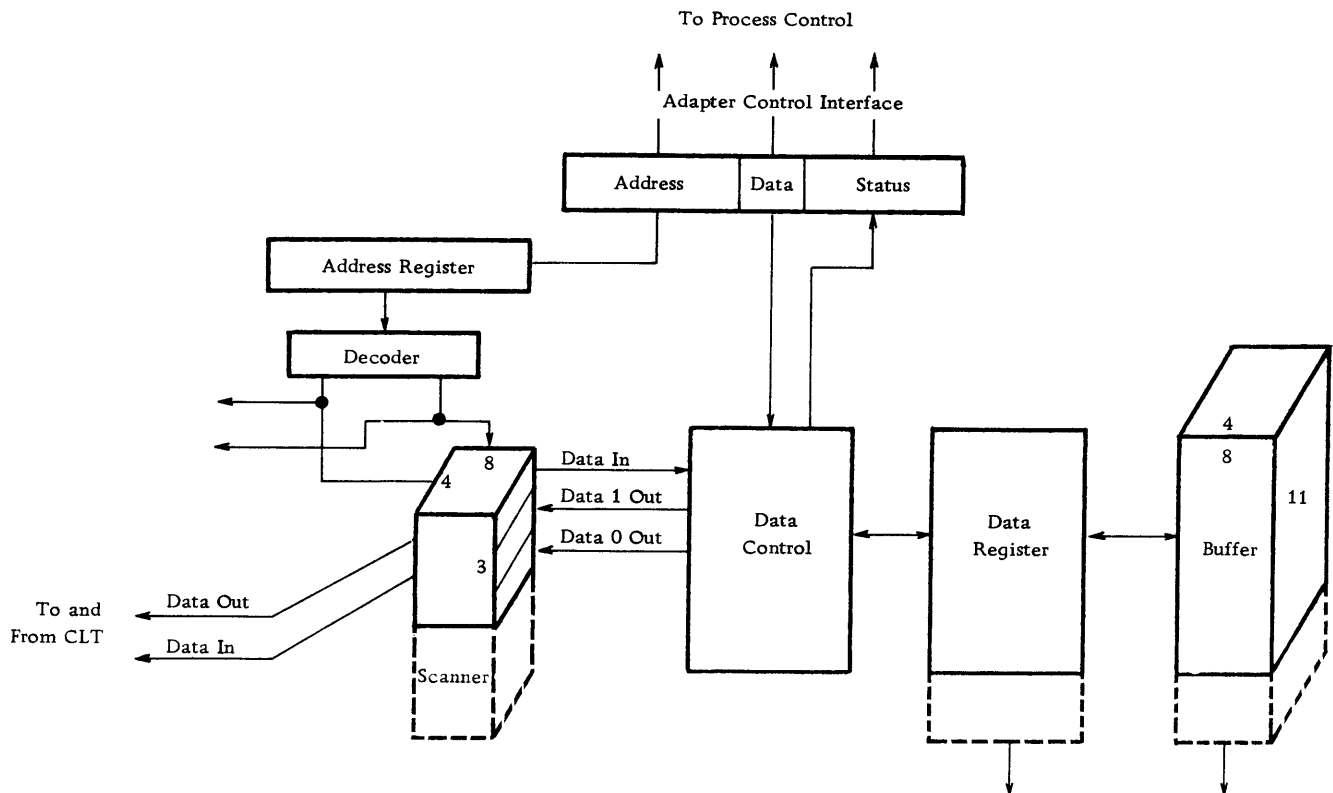


Figure 24. Multiplexing Channel Adapter

imposed. (See Figures 36 and 37.) The bit rate per set is controlled by a sample clock oscillator (SCO) and may be field-changed.

Equipment Configurations

The MCA is made up of several basic pieces of equipment: the low-speed-basic equipment, the multiplexor storage data register with its controls, and the transmit-receiver scanner equipment. The basic equipment contains components used in conjunction with other MCA's. As many as four MCA's can be attached to the basic equipment.

If a second MCA is added to a 7750 already containing one MCA with its basic equipment, some additional circuitry will be required in the basic equipment, plus the addition of a storage data register with its controls and transmit-receive scanner equipment. Each MCA controls seven sets (four communications channels to a set) plus one test channel. Since one 7750 can be connected to four MCA's, it can serve a total of 112 low-speed communications channels and four test channels.

The equipment configuration for the 7750 was chosen to realize the advantages and accompanying cost reduction of using common circuitry in certain portions of all multiplexing channel adapters. All MCA's that share a portion of the low-speed basic equipment package operate in synchronism. Because of this, all such MCA's must scan the same number of channels, although it is not required that all channels be utilized in each MCA. In general, what occurs in one MCA can be assumed to happen in each of the other MCA's that share the basic equipment package.

General Operation

The MCA operates with both the process control rack and the communication channels on a bit-by-bit basis. That is, the MCA sequentially scans the communications channels, obtains bits one at a time from each channel, stores them, and transmits the bits one at a time to the proper remote terminals at the proper scan time for the particular channel. The transfer of bits between the MCA and the process control is by demand from the MCA. Bits are obtained from the channels and transferred to the process control as follows:

The MCA scans each of the communications channels for 14 usec every 14 n usec, where n = number of low-speed channels connected to the MCA. The scanning is done at a rate which insures that at least

ten scans will be taken; thus, ten samples can be taken during a bit time for the fastest bit rate into the MCA. This is the relationship between the number of low-speed channels into an MCA and the maximum bit rate on any low-speed channel. The particular scans during which data samples are to be taken are controlled by a channel timing circuit. Associated with each speed group of low-speed channels is a channel timing circuit whose binary output changes exactly ten times during a bit time for the rated speed of this group of low-speed channels. If, during the scan of a particular channel, the output of the channel timing circuit is different from its state during the previous scan of this channel, a data sample is taken and a sample counter is incremented. Similarly, consecutive scans determine additional samples until sample count 6 is reached. The sample at count 6 is taken as the value for this bit and is stored in the MCA. Also, during sample count 6, a timing bit associated with this low-speed channel is complemented. At some subsequent scan, but prior to the following sample count 6, the process control senses the reversal in the timing bit for this channel, and accepts the bit stored in the MCA for this low-speed channel as the next bit from the channel. The sample counter is reset on either sample count 10, or detection of a level change in the sampled data.

On output, the MCA always transmits to low-speed channels on sample count 6, and the sample counter is reset on count 10, except when elongated stop bits are to be sent. In the latter case, the counter is not reset on ten but on a count equal to the number of tenths desired in the stop bit, e.g., 14 for Baudot code. This number can be assigned any value between 1 and 1.5 integer bit periods by pluggable pins on a circuit card. Between consecutive counts of 6, the MCA obtains a new bit from the process control. The exact scan time depends on the position of the precession of the process control scan with the MCA scan.

Distortion

Receiving distortion is the percentage by which the actual bit width varies from that of the perfect bit width at the communication line terminator interface. In receiving, several types of distortion must be considered. Distortion due to transmitting speed can usually be separated from distortion due to lengthening or shortening of bits. Sampling methods used in the 7750 make speed variations more significant when trying to receive a large number of consecutive identical bits. The following two formulas may be used to

compute the allowable distortion from speed variation and other types of distortion.

$$0.3996 - 0.001N = L$$

$$0.5005 - 0.001N - \frac{2.01P}{B} = S$$

where

N = number of consecutive identical bits.

B = normal bit period.

P = normal scan period for the channel of the MCA.

This is equal to: (number of channels scanned by MCA) x 14 usec.

The first formula gives the percentage of one normal bit period that may be added by distortion to N consecutive identical bits before a sampling error will occur; this percentage is L. The second formula gives the percentage of a normal bit period that may be subtracted by distortion from N consecutive identical bits before a sampling error will occur; this percentage is S. Note that S is dependent upon the number of channels scanned by an MCA and upon the normal bit period. To clarify the use of these formulas, consider the following example:

Transmission rate: 75 bits/second.

MCA scans 25 channels.

Bits may be lengthened or shortened because of bias distortion of 20%.

N = 6

therefore,

$$L = 0.3996 - 0.006 = 0.3936 \approx 0.39$$

$$S = 0.5005 - 0.006 - 2.01 \times 7.5 \times 2.5 \times 1.4 \times 10^{-3}$$

$$S = 0.5005 - 0.006 - 0.0528 \approx 0.44$$

As bias distortion may account for 0.2 bit width variation, this must be subtracted from L and S to find what distortion can be introduced by speed variations.

Therefore:

$$L = 0.39 - 0.2 = 0.19$$

$$S = 0.44 - 0.2 = 0.24$$

The speed tolerance can now be found by dividing L and S by 6, the number of consecutive identical bits that are to be properly sampled. Therefore, each transmitted bit must be written at its normal length altered as follows:

$$1 + \frac{0.19}{6}$$

$$1 - \frac{0.24}{6}$$

or the bit may be varied from 1.03 to 0.96 of its normal width. Regardless of transmitting speed and the number of channels scanned by an MCA, the worst-case condition occurs when P = 0.1 B. This

condition implies that in the worst case, no single bit may be lengthened by more than 40% or shortened by more than 30%. In actual practice, however, P is generally much smaller than 0.1 B.

When transmitting from an MCA, the following distortion formulas give the amount, in fractions of a normal bit width, by which a group of consecutive identical bits may be lengthened or shortened.

Amount group lengthened = 0.001 NB + 1.005 P

Amount group shortened = 0.001 NB - 1.005 P

where:

N = number of consecutive identical bits

B = normal bit period

P = normal scan period for this channel of the MCA.

This is equal to (number of channels scanned by MCA) x 14 usec.

The worst case occurs when P = 0.1 B. In most systems P is much smaller. A single bit may vary from about 90% of its normal length to about 110% of its normal length.

DETAILED DESCRIPTION

The MCA is divided into six functional units (Figure 24):

1. Address Register
2. Channel Scanner
3. MCA Buffer
4. Multiplexor Storage Data Register
5. Data Control
6. Adapter Control Interface

Address Register

The address register is a five-stage binary counter used for sequential addressing of the communications channels. The register's binary output, together with two wired-in bits, supply the seven-bit address sent to process control for addressing control storage during a scan cycle. The value of the wired-in bits depends on which MCA (A, B, C, or D) is being used. When decoded into a 4-out-of-32 output, the address register addresses the MCA buffer. Also when decoded into a 2-out-of-12 output, the register addresses each of the MCA scanners simultaneously. The 2-out-of-12 output is obtained by decoding the first two positions of the counter to determine one of four possible outputs. The remaining three positions are decoded to determine one of eight possible outputs. The 1-out-of-4 output serves as the Y address for the channel scanner matrix; the 1-out-of-8 output serves as the X address for the scanner matrix. The X address also divides the 29 possible channels into sets of four channels each, with the exception of the test channel; thus, the X address gates the appropriate

channel timing circuit into data control. The address of the test channel is always 34 octal in each MCA and the speed of its channel timing circuit is selected by a switch on the communications line terminator (CLT).

Channel Scanner

The channel scanner is a 4 x 8 x 3 matrix of AND gates conditioned by the decoded output of the address register. It is used for routing the input and output data between CLT and the MCA's multiplexor storage data register (MSDR). Figure 25 shows the addressing, and gives an example of channel assignment. If fewer than 28 channels plus one test channel are scanned, the assignment of matrix points may take an even number of sequential addresses beginning with zero. Provisions are made to change the number on which the address register resets and the number to which it resets, according to the number of channels to be scanned. The address register automatically skips to the test channel from the last communications channel scanned and then resets to address zero. Each point in the matrix consists of three AND gates, one for routing Data Out = 1, one for routing Data Out = 0 to CLT via output latches, and one for routing Data In.

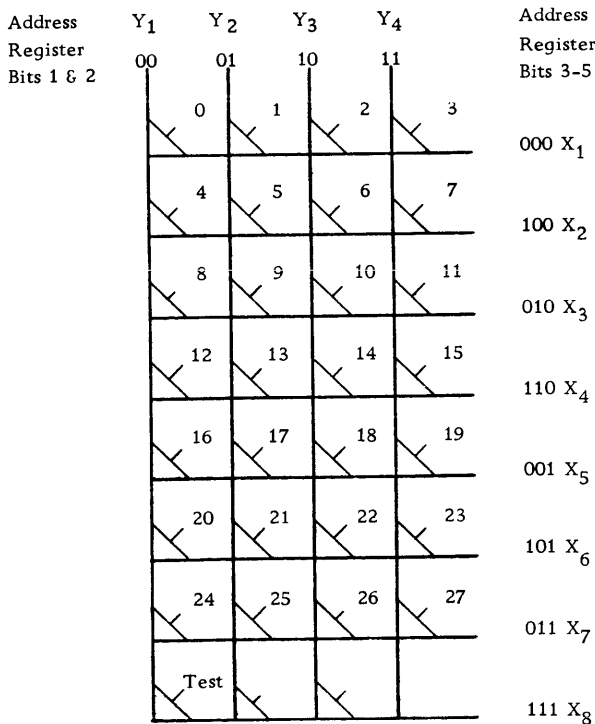


Figure 25. MCA Scanning Matrix

MCA Multiplexor Storage

The MCA multiplexor storage (MS) is a 32 word, four characters per word, 11 bits per character, core storage buffer that stores multiplexor control characters -- one for each communications channel connected to an MCA. The first character of each MS word is reserved for channels connected to MCA-A. The second, third, and fourth characters of each word are reserved for channels connected to the respective second, third, and fourth MCA's possibly associated with a 7750 Programmed Transmission Control System.

Multiplexor Storage Data Register

The buffer data register is an 11-bit register from which multiplexor control characters are accessed. Associated with each of the communications channels connected to the MCA is a multiplexor control character which stores the information required for the data derivation and multiplexing process. The multiplexor control character contains a single bit of data buffering, plus nine control bits used by the MCA to control the transfer of data to and from the communications channel. An eleventh bit provides character parity. Format of the multiplexor control character is as follows:

Bit Name	Number of Bits	Position
Data bit	1	1
Last data sample (LDS) bit	1	2
Send/Receive (S/R) bit	1	3
Last clock sample (LCS) bit	1	4
Sample counter (SC)	4	5-8
Timing bit	1	9
Fractional sampling bit (FSB)	1	10
Parity bit	1	11

The functions of these bits are described below:

1. The data bit is a single bit used to buffer the asynchronous transfer of data into and out of the MCA.
2. The last data sample (LDS) bit in receive operation stores the previous data sample from the channel. In send operation, it is used to store the value of the data in the channel output latch.
3. The send/receive (SR) bit controlled by the process control tells the MCA the transmission status for this particular channel.
4. The last clock sample (LCS) bit stores the status of the channel timing circuit for this line during the previous MCA scan for this channel.
5. The sample counter (SC) is a four-stage binary counter which is incremented upon a detection of a change in status of the channel timing circuit. Reset

of the counter is caused by any of these four conditions:

- (a) change in the send/receive bit
- (b) transition in the sampled data
- (c) count of ten
- (d) count of n

6. The timing bit furnishes line timing status to the process control for the channel associated with this multiplexor control character. In particular, the bit is complemented on each count six of the sample counter.

7. The fractional sampling bit (FSB) is turned on by process control for a channel in send status to cause the MCA to elongate the stop bit being transmitted to the start-stop terminal connected to this channel. The FSB bit is turned on each count six of the sample counter for a channel in receive status to signal process control that the channel has received a new data bit. The FSB is turned off when process control scans the channel.

8. The parity bit provides character parity for checking buffer storage operation. It is used to generate odd parity before writing into storage and is checked at the end of every read time.

Data Control

Data control is the miscellaneous control logic with which the MCA integrates the previous four sections to perform the required functions of channel scanning, channel timing generation, and data transfer to and from the communication channel and the process control.

Of particular significance in data control are the channel timing circuits. Associated with each group of common speed channels is a channel timing circuit whose binary output level changes ten times during a bit time (for the rated speed of the channel). The channel timing circuit consists of a highly stable oscillator connected to a driver that drives a binary trigger whose output is changing at a constant rate -- exactly ten times per bit period. Each level change in the trigger's output is interpreted as a sample time and ten samples are counted as a bit time. Thus, if the channel is operating at exactly its rated speed, there will be exactly ten samples taken during a bit time. Should the channel be operating at some speed slightly slower than its rating, the ten samples per bit would be taken in a bit period of time less than the actual bit time. If several consecutive identical bits, say 14, were transmitted at this slower speed, it is possible that 15 bits would be derived from the channel instead of the correct number (14). To pre-

vent such occurrence, the 7750 must perform within certain transmission speed tolerances. See section 4, "Communications Systems Design," on distortion.

MCA OPERATION

The MCA derives bits from the lines by a scanning and sampling technique. The scanning operation is performed synchronously with the process control and asynchronously with the communications channels; however, the sampling operation is asynchronous with both the process control and the communications channels. Sampling is done at a rate that insures that ten samples will be taken with sufficient accuracy to permit terminal distortions. Since sampling is performed asynchronously, the data transferred to and from the MCA are asynchronous; thus, a multiplexor storage is needed.

To explain the detailed operation of the MCA, the following symbols are defined:

- I Number of scan points connected to the process control (PC).
- N Number of PC scan points to which an MCA is connected.
- i Number of consecutive PC scan points between scan points used for a particular MCA.
- n Number of low-speed channels connected to MCA.

Two 14-usec scan cycles of the MCA are performed during one scan process cycle sequence of control storage. The relationship of these cycles is shown in Figure 26. It can be seen that on alternate scan of the MCA, the control storage is in a scan cycle. On each i^{th} scan cycle of the control storage, one of the N channels to which the MCA is attached is being scanned by the process control. It is during these coincidences of scan cycles that data may be transferred to (or from) the process control from (or to) the multiplexor control character associated with the communications channel being addressed by the MCA channel scanner. For simplification, i is assumed to be constant in this section; that is, the MCA is connected to the process control channels which are evenly spaced.

The 14-usec scan cycle per line is divided into three phases, as shown in Figure 26. In general, phase 1 consists of reading out the multiplexor control character for a particular MCA channel address. Phase 2 consists of modifying the control character as required and initiating data transfers to and from CLT and PC. Phase 3 consists of writing the modified control character into multiplexor storage.

TIMING

The PC performs a ten-usec scan every 28 usec. The MCA performs two 14-usec scan cycles every 28 usec. Thus, the MCA scans two low-speed channels while the PC is scanning one high-speed channel. In addition, the MCA is connected to N scan points of the PC and these N scan points are spaced i scan points apart in the scanning sequence.

To facilitate explanation of the timing relationships between the PC, MCA, and communications channels, a specific example will be used where $I = 15$, $N = 3$, $i = 5$, and $n = 29$. It will also be assumed that the maximum bit rate on any communication channel into the MCA is 200 bits per second (bit period of five ms). See Figure 27.

It can be seen from Figure 28 that the MCA goes through ten complete scanning sequences of the 29 channels between the times that the PC sees a particular MCA channel.

With the maximum bit rate of 200 bps or the minimum pulse width of five ms, with ten channel timing circuit transitions taken within each bit time, and with the relationships given in Figure 27 showing that the MCA scans a particular communications channel every 406 usec, it is assured that a scan, and thus a sample, can be taken at least once during each channel timing circuit period of 500 usec.

Furthermore, it can be seen that the PC scans a particular low-speed channel at least every 4.06 ms and that every channel will be scanned by the PC at least once during every bit time.

Since transmission is asynchronous to the 7750, the beginning of a bit time can occur at any point with respect to the beginning of the timing chart. See Figure 28. For purposes of explanation, it will be assumed that the beginning of a bit time for low-speed channel 10 occurred at microsecond 105. This new bit will be recognized at time 140 when the MCA next scans channel 10, and sample 1 will be counted. Succeeding samples are counted at times 546, 1358, 1764, and 2170 until sample 6 is counted at time 2576. At sample 6, data are taken from the channel and stored in the data bit of the multiplexor control character and its timing bit is complemented and the FSB bit is turned on. At time 3794, the PC is scanning this MCA and the MCA is scanning low-speed channel 10. Thus, the PC sees low-speed channel 10. Since the timing bit for this channel is different from the last timing bit in the channel control word for this channel, the PC knows that a new data bit is stored in bit 1 of the multiplexor control character and it accepts this as a new bit from this channel and turns off the FSB bit. Since the PC sees a given

low-speed channel every 4.06 ms (less than minimum bit time), it is possible, by virtue of the asynchronism just explained, to see a particular bit twice. However, the bit is not accepted the second time because the timing line is not reversed, and the FSB bit is off. All clock timing signals needed in the MCA, other than the channel timing circuits, are supplied by the central clock in the PC.

ERROR CHECKING

A feedback loop from the communications channels to the MCA is provided to check for the correct transmission of data to the communications channel.

In send status, when the MCA transfers a bit to a channel's output latch, the last data sample (LDS) bit is made to match the bit in the output latch. Checking for correct line transmission of the bit in the output latch is done just prior to changing the output latch for the next bit. The status of the LDS bit and the status of the sending channel fed back through the MCA input scanner are compared. If they do not compare, an error latch is set. This causes the MSDR data bit to be different than the last data bit transferred from the PCR. The PCR detects this difference as an error during the next coincident scan in which a timing line reversal is detected and activates its error circuitry.

This comparison gives an error check on the operation of transferring bits from the control storage distribution area to the MCA and subsequently to the communications channels. In addition, the operation of the input scanner is checked.

TYPE 2 HIGH-SPEED CHANNEL ADAPTER

The Type 2 High-Speed Channel Adapter (HSA2) adapts one or two 7750 scan points, depending on half-duplex or full-duplex service, to an IBM terminal provided with a synchronous transmitter-receiver (STR), such as the IBM 7702 Magnetic Tape Transmission Terminal or the IBM 1009 Data Transmission Unit. The HSA2 requires no clocking information from the data set provided by the communications company and generates its own bit synchronization from a crystal-controlled oscillator and bit clock that corrects its own strobe on received data. No character assembly is done by HSA2 because the data-moving operation is serial by bit between the process control and the communications line terminator (CLT). HSA2 accepts bits from the process control and transmits

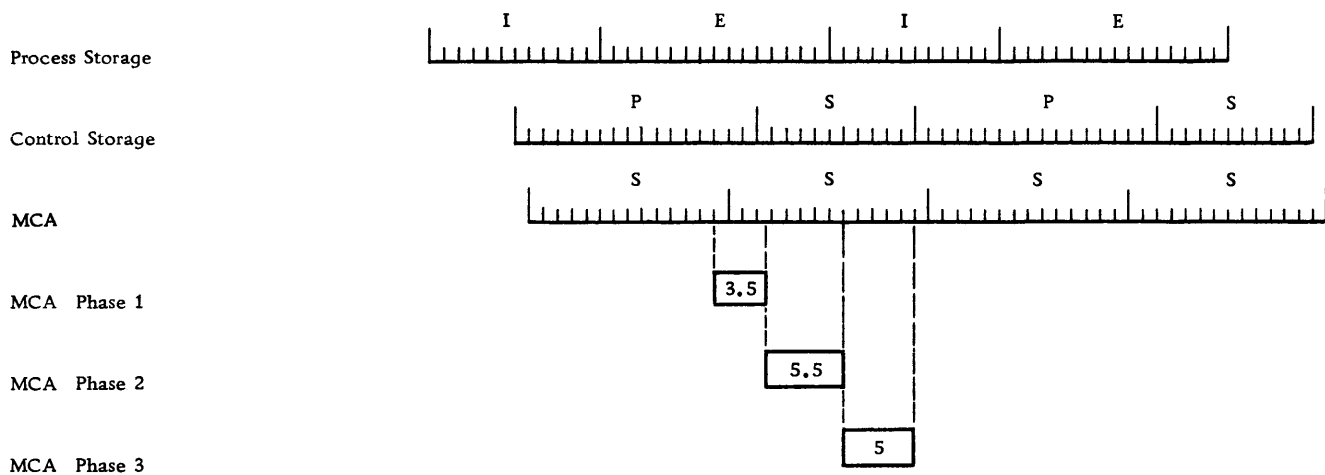


Figure 26. Process Control Rack -- MCA Cycle Relationships

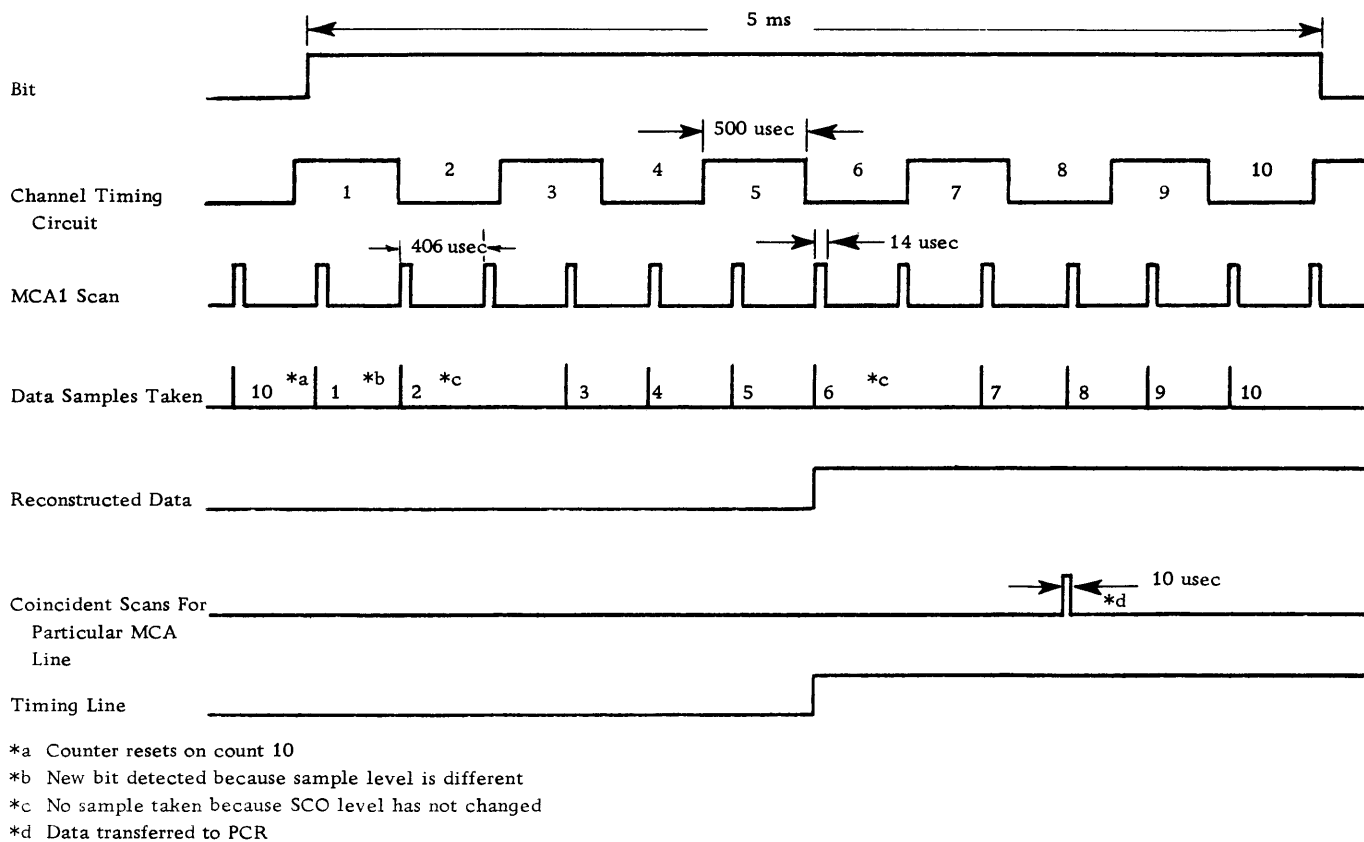


Figure 27. Timing Relationships for a Channel in Receive Status

A	B	C		A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C														
1	14	1	OX#	1	420		1	826	15	1	1232		1	1638	14	1	2044		1	2450	13	1	2856		1	3262	12	1	3668		1	4074	11	OX#										
2	28			2	434	1	X	2	840		2	1246	15	2	1652		2	2058	14	2	2464		2	2870	13	2	3276		2	3682	12	2	4088											
3	42	2		3	448			3	854	1	X	3	1260		3	1666	15	3	2072		3	2478	14	3	2884		3	3290	13	3	3696		3	4102	12									
4	56			4	462	2		4	868			4	1274	1	X	4	1680		4	2086	15	4	2492		4	2898	14	4	3304		4	3710	13	4	4116									
5	70	3		5	476			5	882	2		5	1288			5	1694	1	X	5	2100		5	2506	15	5	2912		5	3318	14	5	3724		5	4130	13							
6	84			6	490	3		6	896			6	1302	2		6	1708		6	2114	1	X	6	2520		6	2926	15	6	3332		6	3738	14	6	4144								
7	98	4	∅	7	504			7	910	3		7	1316			7	1722	2		7	2128		7	2534	1	X	7	2940		7	3346	15	7	3752		7	4158	14						
8	112			8	518	4		8	924			8	1330	3		8	1736		8	2142	2		8	2548		8	2954	1	X	8	3360		8	3766	15	8	4172							
9	126	5		9	532			9	938	4		9	1344			9	1750	3		9	2156		9	2562	2		9	2968		9	3374	1	X	9	3780		9	4186	15					
10	140		Δ	10	546	5	Δ	10	952		Δ	10	1358	4	Δ	10	1764		Δ	10	2170	3	Δ	10	2576		Δ	10	2982	2	Δ	10	3388		Δ	10	3794	1	X	●	10	4200		Δ
11	154	6	X	11	560			11	966	5		11	1372			11	1778	4		11	2184		11	2590	3		11	2996		11	3402	2		11	3808		11	4214	1	X				
12	168			12	574	6	X	12	980			12	1386	5		12	1792		12	2198	4		12	2604		12	3010	3		12	3416		12	3822	2		12	4228						
13	182	7		13	588			13	994	6	X	13	1400			13	1806	5		13	2212		13	2618	4		13	3024		13	3430	3		13	3836		13	4242	2					
14	196			14	602	7		14	1008			14	1414	6	X	14	1820		14	2226	5		14	2632		14	3038	4		14	3444		14	3850	3		14	4256						
15	210	8		15	616			15	1022	7		15	1428			15	1834	6	X	15	2240		15	2646	5		15	3052		15	3458	4		15	3864		15	4270	3					
16	224			16	630	8		16	1036			16	1442	7		16	1848		16	2254	6	X	16	2660		16	3066	5		16	3472		16	3878	4		16	4284						
17	238	9		17	644			17	1050	8		17	1456			17	1862	7		17	2268		17	2674	6	X	17	3080		17	3486	5		17	3892		17	4298	4					
18	252			18	658	9		18	1064			18	1470	8		18	1876		18	2282	7		18	2688		18	3094	6	X	18	3500		18	3906	5		18	4312						
19	266	10		19	672			19	1078	9		19	1484			19	1890	8		19	2296		19	2702	7		19	3108		19	3514	6	X	19	3920		19	4326	5					
20	280			20	686	10		20	1092			20	1498	9		20	1904		20	2310	8		20	2716		20	3122	7		20	3528		20	3934	6	X	20	4340						
21	294	11	X	21	700			21	1106	10		21	1512			21	1918	9		21	2324		21	2730	8		21	3136		21	3542	7		21	3948		21	4354	6	X				
22	308			22	714	11	X	22	1120			22	1526	10		22	1932		22	2338	9		22	2744		22	3150	8		22	3556		22	3962	7		22	4368						
23	322	12		23	728			23	1134	11	X	23	1540			23	1946	10		23	2352		23	2758	9		23	3164		23	3570	8		23	3976		23	4382	7					
24	336			24	742	12		24	1148			24	1554	11	X	24	1960		24	2366	10		24	2772		24	3178	9		24	3584		24	3990	8		24	4396						
25	350	13		25	756			25	1162	12		25	1568			25	1974	11	X	25	2380		25	2786	10		25	3192		25	3598	9		25	4004		25	4410	8					
26	364			26	770	13		26	1176			26	1582	12		26	1988		26	2394	11	X	26	2800		26	3206	10		26	3612		26	4018	9		26	4424						
27	378	14		27	784			27	1190	13		27	1596			27	2002	12		27	2408		27	2814	11	X	27	3220		27	3626	10		27	4032		27	4438	9					
28	392			28	798	14		28	1204			28	1610	13		28	2016		28	2422	12		28	2828		28	3234	11	X	28	3640		28	4046	10		28	4452						
29	406	15		29	812			29	1218	14		29	1624			29	2030	13		29	2436		29	2842	12		29	3248		29	3654	11	X	29	4060		29	4466	10					

Key: A - MCA scans low-speed channel.
 B - Time in microseconds.
 C - Process control rack (PCR) scans high-speed channel or MCA.

○ - MCA scans low-speed channel 1.
 X - PCR scans MCA.
 # - PCR and MCA have coincident scans on channel 1.
 ▲ - Data sample 6 taken from low-speed channel 10; timing bit complemented.

∅ - Data transition occurs on low-speed channel 10.
 Δ - Data sample taken from low-speed channel 10.
 ● - Data bit transferred to PCR, from MCA for channel 10.

Figure 28. Process Control Rack--MCA Scanning Relationships

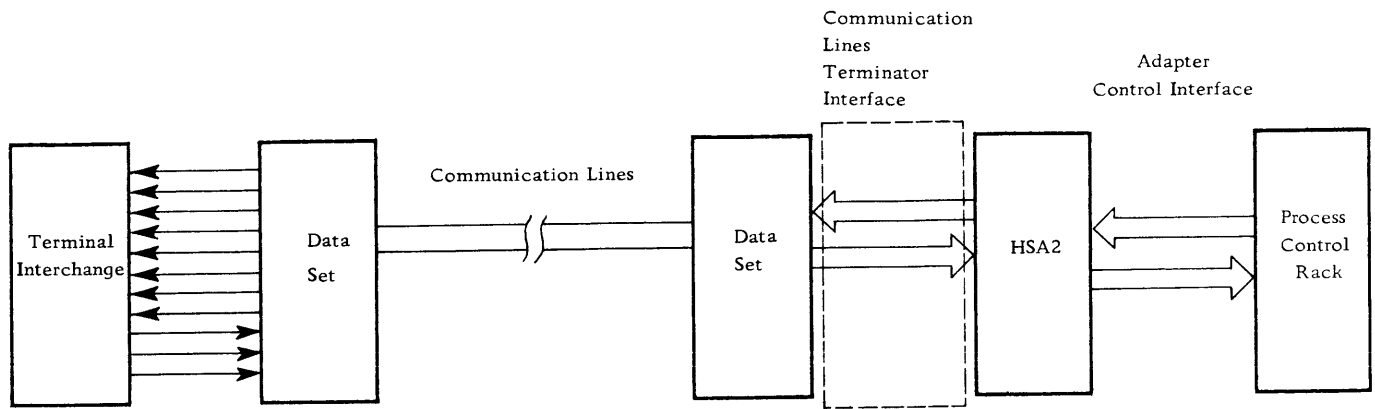


Figure 29. HSA2 Connections

them through the CLT to the remote terminal. On receiving, HSA2 samples information serially to the process control, Figure 29. HSA2 is capable of operating at 600 or 1200 bits per second. The operating speed of an HSA2 may be selected from the 7750 operator's panel subassembly by the customer. Each HSA2 may operate at either of the two speeds.

HSA2 may operate half-duplex or full-duplex. When operating half-duplex, HSA2 requires only one 7750 scan point. However, two scan points are required for full-duplex operation -- one each for the send-only and receive-only channels. HSA2 may be changed from half-duplex to full-duplex.

HSA2 provides one bit buffering and speed changing between two interfaces in both directions. On the one side, HSA2 exchanges information with the process control via the adapter control interface. On the other side, HSA2 transmits or receives information to CLT which in turn relays this information to the communications line.

ACIF Operation

Each time that the process control channel scanner is incremented, a new select signal is generated. This select signal comes from one of the IBM 7750 scan points. When HSA2 becomes selected, its seven-bit control storage address is sent to the ACIF. The process control uses this address to access the channel word, CWD, for HSA2 from control storage. Once the CWD is in place in the CSDR, a transfer of information occurs across the ACIF, causing HSA2 and the process control to take different actions. The channel word is written back into control storage and the channel scanner is incremented to scan the next scan point. During this select period, the bit derived by HSA2 is transferred to the process control.

Transmitting

To transmit a message, the programmer first sets up an output chain in process storage and moves the CWD to its proper location in control storage. The format of this CWD will be synchronous send. When HSA2 is selected, it will raise the "request to send" line of the CLT interface and initialize the "timing" and "data in" lines of the ACIF in response to adapter synchronization. Timing changes cannot happen until the character phase counter counts through zero. The next time HSA2 is selected there will be a logical difference between the timing line of ACIF and bit 31 of CSDR, last timing bit. On such a difference the process control will transfer the first bit to HSA2. HSA2 accepts this bit and buffers it until transmit strobe time, when it is placed on the "transmit data" line of the CLT interface for transmission. At transmit strobe time the "timing" line of ACIF is complemented and the logical value of the "transmit data" line is fed back to the "data in" line of ACIF. The next time HSA2 is selected, the process control recognizes another change of the timing line and sends the next bit to the HSA2 and checks the value of the "data in" line with the previous bit sent to HSA2. If value of the data-in does not agree with the value of the last bit sent to HSA2, a data transfer check occurs. This process continues until the last bit of the last character has been transferred to HSA2 via the ACIF. Then the process control performs a character interrupt to get the next character to be sent. The next character is the status change character (SCC). When the SCC is placed into the assembly area of the CWD as the next character to be sent, it is recognized by the process control, and preparations are made to turn the channel around to receive status. After sufficient time has elapsed for the last bit to be fully transmitted, HSA2 is

changed to receiving hunt status and an adapter synchronization is given to HSA2 via the ACIF.

This description holds for both full-duplex and half-duplex operation of HSA2, with the exception that when the send-only channel of HSA2 is placed in receiving hunt status on full-duplex, it is placed in an inactive state and is not capable of receiving data.

Receiving

When the IBM 7750 program is started, the channel words are moved from process storage to control storage, making the channels active. Normally the format of the CWD moved to the control storage location assigned to an HSA2 is synchronous send. After the sending of the synchronization information, a status change character is used to put the channel into synchronous receive hunt status.

With the CWD in receiving hunt, the process control will shift bits as they are transferred from HSA2 through the extended assembly area of the CSDR looking for the character sync pattern. HSA2, however, will not be transferring bits to the process control rack until it starts receiving data through the CLT interface. When data are received from the communications channel, the "carrier on" line of the CLT interface becomes a logical one. This line is then used to start allowing changes to occur to the timing line of ACIF. The timing line is also complemented at receive strobe time. When HSA2 is selected by the process control channel scanner, a difference occurs between the timing line of ACIF and bit 31 of CSDR, last timing bit. The process control knows from this difference that a new bit has arrived on the "data in" line and gates it into the assembly area of CSDR. Process control also updates the value of bit 31 of CSDR to agree with the timing line of ACIF so that the same bit will not be sampled twice. Bits are transferred to the process control in this manner. When the character sync pattern has been recognized by the process control, the CWD falls out of receiving hunt and starts receiving bits. When the number of bits equals the character length specified in the CWD, the character assembled is moved to the receiving chain in storage for communications channel.

Slave-Master Control

When using HSA2 on a half-duplex communication facility, the 7750 makes special use of the control bit, CSDR 13, of the normal synchronous channel word. If the control bit is set to a logical one, HSA2 assumes a slave status. Slave status is required, on half-duplex transmission, when the 7750 is receiving a tape record from a 7701 or 7702, or receiving card transmission

from a 1013. The adapter must remain in this slave status even though its status changes from send to receive or receive to send via CSDR 12 of its channel word. If, however, the 7750 is transmitting tape records or card images to an STR device (1009, 1013, 7701, or 7702) the control bit must be reset to logical zero and the HSA2 will assume master status.

Error Indication

HSA2 is capable of calling program attention to two types of channel errors via a service mode request and interrupt of all lower priority modes. When indicating channel errors, HSA2 will change two bits of the seven-bit control storage address to which it is assigned in order to access a channel word other than that used for normal operation. At the same time, the attention line of ACIF is brought to logical one and the error line of ACIF may or may not be brought to logical one, depending on the type of error. The next time HSA2 is selected by the process control channel scanner, the error channel word is read into the CSDR. The error is recognized and service mode is requested. Also, the address of the channel in error is moved to the channel service register for the program to interrogate. For details of this operation, read "Channel Errors."

Interlock Error

The interlock line of the CLT interface is at logical one whenever the data set at the local end of the communications channel of HSA2 has power on and it is functioning properly. If the interlock line drops to a logical zero, an interlock error will be signaled to the attention of the program. HSA2 places logical ones on both the attention and error lines of the ACIF. The channel check light associated with the scan point to which HSA2 is connected will be turned on by the interlock error.

Time-Out Tag for Half-Duplex HSA2

When HSA2 has completed transmission of a message to a remote terminal, it will be placed in receiving hunt by the SCC. From the time that HSA2 is placed in receive status to the time that the process control recognizes the received character sync pattern and starts assembling characters and moving them to the receiving chain in process storage, HSA2 is timing out. The duration of this time-out cycle is three seconds. If the process control has not recognized the character sync pattern and assembled at least one character before the HSA2 times out, a time-out tag will be signaled to the attention of the program. However, if a character has been assembled

before the HSA2 times out, HSA2 will receive logical ones on the "character complete" line of the ACIF each time a new character is assembled. HSA2 uses these logical ones to prevent the time-out tag.

The 7750 program will use this time-out tag as a special signal that bit synchronization must be re-established with the remote terminal before proceeding with transmission. To reset the time-out-tag error condition, the programmer must put a 14₈ in the F field (bits 15-19) of the time-out-tag error channel word and put a synchronous send channel word in the normal channel word to send synchronization information.

Time-Out Tag for Full-Duplex HSA2

With full-duplex operation of HSA2, idle characters will always be received on the receive-only channel when messages are not being received. When the 7750 sends a message on the send-only channel and expects a reply, a time limit for that reply is imposed. This time limit is three seconds, the same limit as for time-out tag on half-duplex. Again, HSA2 keeps track of this time.

Time out is initiated by placing an active channel word in control storage containing an adapter-synchronization and the control-bit (CSDR 13) reset. The programmer may do this whichever way he wishes: by using action delay, by moving a new channel word to control storage, or by any other techniques at his disposal. The time-out tag is controlled by the transmitting portion of the full-duplex adapter. It is the send-only channel word through which time out is initiated. Time out can be blocked at any time by setting the control bit (CSDR 13) of the send-only channel word to a logical zero. A time-out tag will occur approximately three seconds after time out is initiated. The send-only channel word will no longer be accessed by the adapter when it contains a time-out tag. The time-out-tag error channel word must be given the adapter-synchronization 14₈ to reset the time-out tag.

The 7750 program will use this time-out tag as a signal that an inquiry must be sent to the remote terminal asking for the reply to the transmitted record.

Control Storage Address Assignments

Each of HSA2 requires three or four pre-assigned addresses in control storage, depending on whether HSA2 is operating half-duplex or full-duplex, respectively. Assignment of control storage words is

made according to Figure 34. If the HSA2 is half-duplex, the fourth address can only be used for a scratch word. The address assignment depends on the customer's channel adapter configuration. This section describes the arrangement within the sequential block assigned to an HSA2 of the normal channel word and error channel words. For either half-duplex or full-duplex there may be either a horizontal or vertical assignment of words to HSA2.

Half-Duplex Vertical Assignment:

-----00 is assigned to the normal CWD.

-----01 is assigned to the error CWD for interlock error.

-----10 is assigned to the error CWD for time-out tag.

Half-Duplex Horizontal Assignment:

00-----is assigned to the normal CWD.

01-----is assigned to the error CWD for interlock error.

10-----is assigned to the error CWD for time-out tag.

Full-Duplex Vertical Assignment:

-----00 is assigned to the receive-only CWD.

-----01 is assigned to the error CWD for interlock error.

-----10 is assigned to the send-only CWD.

-----11 is assigned to the error CWD for time-out tag.

Full-Duplex Horizontal Assignment:

00-----is assigned to the receive-only CWD.

01-----is assigned to the error CWD for interlock error.

10-----is assigned to the send-only CWD.

11-----is assigned to the error CWD for time-out tag.

In this discussion address bits represented by (-) are fixed and equal for each word address assigned to a particular HSA2.

Operator's Switches and Data Lights

The operator's panel sub-assembly contains four sets of data lights and four rotary speed select switches. Each set of data lights indicates the six lines of the CLT interface. The operator can see at a glance the state of any one of four HSA2's indicated on the sub-assembly. The operator may also change the operating speed of any one of four HSA2's in accordance with the speed of operation on the communication line.

FM-STR Distortion

For FM-STR operations, the receiving distortion is the absolute difference between a consecutive marking bit and a spacing bit (or spacing bit and marking bit) divided by four normal bit periods. This ratio is expressed as a percentage.

Example: In two consecutive bits, a marking bit is 750 usec and a space bit is 250 usec. If a normal bit is 500 usec (2,000 bits/sec), the distortion is:

$$D = \frac{750 - 250}{4(500)} = 0.25 = 25\%$$

Distortion discussed does not include the effects of speed variation or drift between the controlling oscillators at each end of the communications facility. This is a separate subject that will be considered by itself.

Once bit synchronization has been established, distortion can be increased gradually and the STR clock will maintain the bit synchronization. However, if this highly distorted signal were transmitted to a clock not in bit synchronization, it might possibly never synchronize. Therefore, the limiting point for distortion is that limit beyond which bit synchronization will not be established.

In operation with the STR, it is the idle character that is used to establish bit synchronization, and hence character phase. The idle character is of the form: mark, space, space, 3 marks, space, space. Synchronization can be established and maintained while receiving idle characters with up to 25% distortion. With over 25% distortion the HSA2 bit clock will start sampling the distorted bit twice, deriving false information. With exactly 25% distortion, reliable operation cannot be guaranteed.

COMMUNICATIONS LINES TERMINATOR

The communications lines terminator connects common carrier equipment to the 7750. It changes common carrier voltage levels to those used in IBM circuits and changes IBM voltage levels to those used in communications channels. The CLT contains equipment to convert IBM signal levels to certain telegraph signal levels. To perform these functions efficiently, the CLT:

1. Provides a standardized interface to the common carrier.
2. Is capable of switching off to permit testing the processor without disturbing the communications lines.
3. Permits customer reassignment of channels for service fault location.

4. Permits customer selection and speed control of an extra low-speed channel for fault location or temporary usage.
5. Facilitates a diagnostic wrap-around of the entire machine under one control, including the necessary line isolation.
6. Provides a test pattern generator for testing individual high-speed lines.

General Characteristics

The CLT consists of one rack-and-panel module with appropriate covers and associated equipment.

Low-Speed Line Termination: At transistor level the CLT can terminate a maximum of 112 lines at speeds up to 200 bps. The lines are half-duplex and consist of one send circuit, one receive circuit, one signal ground, and one frame ground for each low-speed communication line. When telegraph lines feed directly into the CLT, maximum line speed is 75 bps. The lines are half-duplex and consist of two conductors of the telegraph line.

High-Speed Line Termination: The CLT can operate with high-speed data sets conforming to EIA Standards No. 232, at speeds of 1,200 bits per second or less.

Off-Line and Diagnostic Status: All high- and low-speed channels can be functionally disconnected from the communication lines and data sets by depressing the wrap-around switch. When in the off-line status, the send circuits of the odd-numbered channels are connected to the receive circuits of the next higher order channels to effect a paired wrap-around of two adjacent like channels for diagnostic test purposes. The wrap-around of the adjacent like channels causes an echo to be simulated on each low-speed line. Depressing the simulation switch generates a test pattern for testing individual high-speed channels.

Customer Facilities

The CLT has a patch panel by which the customer can alter the line-to-channel assignment in order to localize a trouble fault, i.e., IBM equipment or common carrier.

Low-Speed Patch Panel

The low-speed patch panel has a two-circuit-line jack and a two-circuit-channel jack. The line jack refers to the common carrier and the channel jack refers to the 7750. The two jacks are internally connected in such a way that no plug is needed in either

jack. Line 1 is connected with channel 1, line 2 is connected to channel 2, etc. Under normal operating conditions, therefore, no patch cords are plugged into any of the jacks.

High-Speed Patch Panel

The high-speed patch panel has two multi-pin connectors. One connection refers to the common carrier and the other refers to the 7750. Connection between the two is established by a multi-wire patch cord. For the high-speed circuits to be operational, this patch cord must be externally connected by the customer.

Low-Speed Test Channels

One low-speed test channel is provided for each MCA group specified in the 7750. By switching, the customer can select the speed of the test channel to match the speed of the line to which the test channel is patched.

Low-Speed Test Circuits

The basic machine will have two test circuits. Each circuit can operate on telegraph and transistor levels.

High-Speed Test Jack

One high-speed test jack is provided. It will emit a test pattern when the request-to-send line is inoperative and it will provide a feedback from the transmit-data line to the receive data line when the request-to-send line is operated. The feedback will facilitate a single-channel wrap-around on a full-duplex system. On a half-duplex system, the send and receive lines must be tested separately.

Effect of Patch Panel on Programming

If any change is made in the patch panel, the program must be altered to reflect the change. This applies to a diagnostic wrap-around as well as on-line operation.

Diagnostic Facilities

The CLT contains five sense lines. The lines, controlled by the computer, perform the following functions:

1. Simulate carrier failure
2. Restore carrier or interlock
3. Simulate interlock failure
4. Master reset
5. Simulate echo failure

The first three lines are used in diagnostic programming to simulate high-speed data set carrier or interlock failures. The last two are used to control echo checks on the low-speed circuits during transmitting. All of the above sense instructions operate as stated in the wrap-around status. In normal operation, the carrier-failure and the interlock-failure sense instructions operate at the high-speed test jack only.

LOW-SPEED OPERATION (ON LINE)

In the event of apparent trouble on a communication line, it is particularly important that the customer be able to determine whether the trouble lies in IBM equipment or in the communications network, so that the proper service representative may be called. The CLT provides a means by which the customer may determine where the trouble lies. If these facilities are not used, 7750 availability will be decreased.

If trouble is experienced on a low-speed line, the customer can perform the following tests:

1. Cross the line-channel assignment; connect line 1 to channel 2, line 2 to channel 1, etc. Any crossing assignment may be made as long as line and channel speeds are matched. From the result, the customer can predict whether the common-carrier line or IBM channel is at fault.
2. Patch the faulty line into an unused channel of the same speed. From the results, the customer can predict the source of trouble.
3. Patch the faulty line into a test channel. The speed of the test channel can be adjusted by a switch to match the line speed. From these results, the customer can also predict the source of the trouble. If the trouble is in a channel rather than in a line, the customer can continue operation temporarily, using the test channel.
4. Wrap any two channels, including the test channel, with a special patch cable.
5. Use the low-speed test circuits. The use of these circuits will be the customer's best tool for trouble isolation. So that their use may be understood, the common-carrier termination will be reviewed.

The common-carrier termination (interface) is as follows:

1. Low-Speed Telegraph (Electromechanical) Mode -- The common carrier terminates all telegraph lines with WE 303 telegraph jacks located on a panel at a convenient location in the same room as the 7750. The 7750 circuitry terminates all telegraph channels, including the low-speed test circuits, with WE 347 male telegraph plugs on cables not more than 50 feet long.

2. Low-Speed Electronic Mode--The common-carrier supplies a data set for operation in the electronic mode and terminates its circuits at the male input to the data set (DB-19604-433). The 7750 circuitry terminates all channels, including the low-speed test circuits with a female plug (DB-19604-432) on cables not over 50 feet long.

The above format permits substitution of channels at the interface and enables the customer to differentiate between IBM and common-carrier responsibilities. The 7750 contains two additional low-speed telegraph circuits and two additional low-speed electronic circuits to facilitate these tests without interrupting other machine functions.

Each low-speed test circuit begins at the common carrier interface and terminates at a jack on the patch panel. This jack can be patched to a test channel to establish an alternate path from the common-carrier interface to the MCA. When a particular line is failing and other lines are working properly, the first customer test should be to substitute a test circuit and channel for the questionable one and modify the program accordingly. Figure 30 shows diagrammatically various ways of using the test circuits. See "Program Considerations" for further details. Substituting a test circuit and channel for the questionable one provides an alternate path from the common-carrier interface to the MCA, and enables the customer to determine whether he should call for common-carrier service or for IBM service. If both channels react in the same manner, the common-carrier line can be assumed to be at fault and requiring service. However, if the connection combinations work properly on one channel but continue to fail on the questioned channel, the faulty 7750 channel requires service.

HIGH-SPEED OPERATION (ON LINE)

Any two channel combinations may be crossed and analyzed in a manner similar to that described for tests 1, 2, and 3 under "Low-Speed Operation."

DIAGNOSTIC OPERATION (OFF LINE)

Low-Speed Wrap-Around

The wrap-around switch, when ON, causes an echo to be generated for each low-speed transmission channel. The diagnostic program transmits on a channel and receives on the paired channel. The program can compare the transmitted data and the received data to verify the operation. If any patching appears in the patch panel, it will alter the wrap-around combinations.

Low-Speed Sense Line Control

The diagnostic program can impulse the "simulate echo failure" sense line and thus inhibit the echo. The program can then transmit on each channel and expect to get an echo failure on each channel. The echo can subsequently be uninhibited by pulsing the master reset sense line. Whenever either of these sense lines is pulsed, a 10-millisecond delay is required before the next transfer of data.

High-Speed Wrap-Around

High-speed wrap-around is performed in the same manner as low-speed. It is necessary that the patch panel configuration be recognized.

High-Speed Sense Line Control

The simulate carrier failure sense line can be pulsed to simulate a carrier failure and the simulate interlock failure sense line can be pulsed to simulate an interlock failure. The simulate interlock failure sense line can be pulsed to restore these two lines to their normal status.

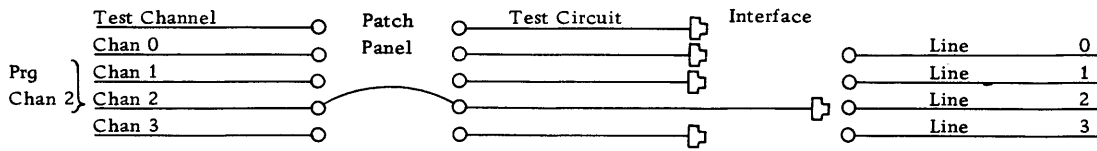
Sense Line Timing

All sense lines will perform properly on a pulse of 20 usec.

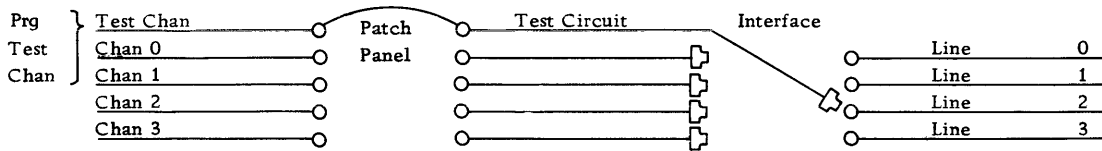
IBM 7750 PROGRAMMED TRANSMISSION CONTROL

COMMON CARRIER

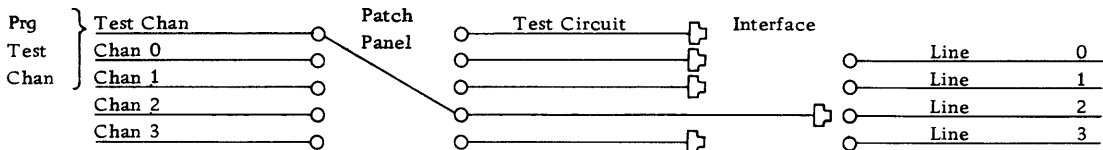
Normal Operation



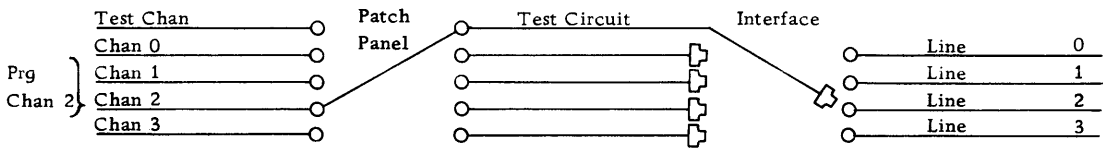
To Differentiate IBM and Common Carrier Faults



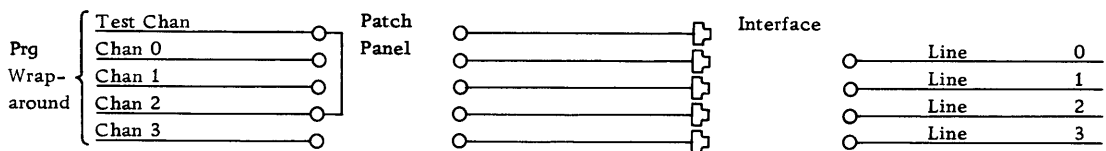
To Localize IBM Faults



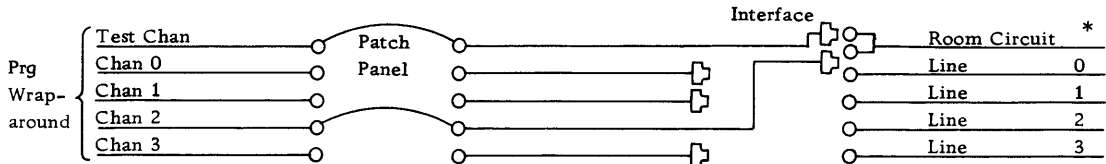
To Localize IBM Faults



Wraparound at Patch Panel



Wraparound at Interface with Room Circuit



*Room circuit is installed by the customer at his option.

Figure 30. Common Carrier Termination

The channel adapter of the 7750 has been designed to provide great flexibility for the system designer in his choice of a communication network. However, certain limitations do exist in the choice of channel adapter configurations, and the purpose of this section is to point these out.

PROGRAMMING CONSIDERATIONS

Processing Capability

Processing capabilities must be carefully considered when designing a system employing the 7750. Under certain circumstances it may be possible to accept more characters from the communications network than the 7750 can process. For example, sixteen high-speed lines receiving six-bit characters at the rate of 1,200 bits per second per line will put into the 7750 about 3,200 characters per second; experience has shown, however, that a typical processing job requires about 15 instructions per character, which would cause process storage to overflow. Moreover, if a relatively complex editing job has to be done by the 7750 on the incoming messages, character handling capability will be reduced. Therefore, it cannot be assumed that the 7750 is capable of processing a given number of characters just because the scanning mechanism is capable of receiving them. The details of the processing task, as well as the peak loading of the communications system and the duration of this peak must be carefully examined. The system designer cannot be sure that the 7750 has enough processing power for a job until these factors are known.

Real-Time Operation

The 7750 is meant to operate in real time with a high degree of reliability. Much thought has been given to the design of the equipment that makes up the 7750, so that efficient real-time operation can be achieved. However, to make full use of the capabilities of the 7750, certain features pertaining

to the communications network must be incorporated into the operational programs for the 7750. These features include:

1. The ability to alter an address relative to the communications channel so that the patch panel and test circuitry may be used on line without interruption of real-time operation. For example, suppose that the 7750 starts to receive erroneous information from one low-speed communications line (say line 13). To test whether this trouble lies in the 7750 or in the communications network, patch this communications line through the test circuitry and test channel to see if proper information is received through this alternate path. To make this test without interfering with the operation of any other communications line, inform the operational program that the information it was formerly receiving from line 13 will now be received on the test channel. The operational program must contain the means to perform this function readily, without interference with normal processing functions and with a minimum of operator intervention. The converse function, that of reassigning addresses for outgoing information must also be included in the operational program.

2. The ability to send a repetitive test message to any designated terminal upon command of the system operator. The sending of this test message must not interfere with the normal operation of the rest of the system. It is also highly desirable that the operating program have the ability to loop this test message through the communications-company patch panel and back into the 7750 for a character-by-character comparison.

The inclusion of the foregoing features in the 7750 operational programs is strongly recommended. The lack of such features will seriously hamper on-line servicing of the 7750 and will result in greatly decreased efficiency in real-time operations.

Channel Capabilities

Certain requirements must be met when using the 7750 channel adapter rack. These requirements are:

1. Packaging requirements.
2. Use of process control scan points.
3. Use of control storage words.

<u>Type of Adapter</u>	<u>Type & Number of Lines</u>	<u>Number of Panels</u>	<u>Permissible Mounting Locations</u>
MCA	0-56 Half Duplex	2	3 and 4
MCA	57-112 Half Duplex	3	1, 3, and 4
FM-STR	1 through 4 Half Duplex or 1 through 4 Full Duplex or Any combination of half and full duplex channels that totals four or less	1	1 or 2 or 3 or 4

Figure 31. Package Configurations of Channel Adapters

<u>Type of Adapter</u>	<u>Number of PCR Scan Points (Required)</u>
MCA	1 or 2 or 3 or 4
FM-STR Full Duplex	2
FM-STR Half Duplex	1

Figure 32. Channel Adapters and Scan Points

<u>Type of Adapter</u>	<u>Number of Channel Words Required</u>	<u>Purpose of Channel Words</u>
MCA	One for each simplex channel connected to each MCA	Send or Receive
	One for each half-duplex channel connected to each MCA	Send or Receive
	Two for each full-duplex channel connected to each MCA	Send or Receive
FM-STR Full Duplex	Four	1. Receive 2. Interlock Error 3. Send 4. Time-Out Tag
FM-STR Half Duplex	Three	1. Send or Receive 2. Interlock Error 3. Time-Out Tag

Figure 33. Control Storage Word Requirements

Packaging Requirements

The 7750 channel adapter contains a maximum of four 10 x 28 SMS card panels. Each variety of channel adapter requires one or more panels. The panels may be mixed in a variety of ways to meet system requirements. Figure 31 shows the packaging configurations of the various channel adapters.

Use of Process Control Scan Points

There are 16 process control scan points that can be utilized by the channel adapters as shown in Figure 32. Note that each MCA may be connected to different numbers of scan points. The proper number to use is determined by the bit speed on the channels connected to the MCA. See "Input Bit Rates."

Use of Control Storage Words

In system design, the space limitations of control storage must be considered. Eight words are required to run programs. The remaining 120 words may be assigned as channel words, with certain restrictions. Figure 33 shows the number of channel words (and their functions) required for each type of adapter.

The locating of these words in control storage must be done in a specified manner. Process control uses addresses 31, 63, 94, 126, 127 (decimal) for process words. MCA's will be assigned blocks of control storage, starting with address 0, 32, 64 and 96 (decimal). Addresses 28, 60, 92, and 124 (decimal) are reserved for test channels. It is recommended that addresses 30 and 62 (decimal) be reserved for "scratch" words by the programmer.

When four MCA's are used, high-speed adapters will be assigned blocks of four addresses, the low-order five bits of which are constant, while the two high-order bits change. Figure 34 shows, as an example, how control storage addresses would be assigned when four MCA's, each scanning 25 channels, and three high-speed adapters are used.

When fewer than four MCA's are used, high-speed adapters are assigned blocks of four addresses, the high-order five bits of which do not change, while the low-order two bits do change. As an example, Figure 35 shows the case in which two MCA's, each scanning 29 channels, and eight half-duplex high-speed adapters are used.

Input Bit Rates

The input bit rates discussed in this section are bit rates from the communications channel to the 7750.

MCA-A	MCA-B	MCA-C	MCA-D
0. 00---00	32. 00---00	64. 10---00	96. 11---00
1. 00---01	33. 01---01	65. 10---01	97. 11---01
2. 00---10	34. 01---10	66. 10---10	98. 11---10
3. 00---11	35. 01---11	67. 10---11	99. 11---11
4. 00---00	36. 01---00	68. 10---00	100. 11---00
5. 00---01	37. 01---01	69. 10---01	101. 11---01
6. 00---10	38. 01---10	70. 10---10	102. 11---10
7. 00---11	39. 01---11	71. 10---11	103. 11---11
8. 00---00	40. 01---00	72. 10---00	104. 11---00
9. 00---01	41. 01---01	73. 10---01	105. 11---01
10. 00---10	42. 01---10	74. 10---10	106. 11---10
11. 00---11	43. 01---11	75. 10---11	107. 11---11
12. 00---00	44. 01---00	76. 10---00	108. 11---00
13. 00---01	45. 01---01	77. 10---01	109. 11---01
14. 00---10	46. 01---10	78. 10---10	110. 11---10
15. 00---11	47. 01---11	79. 10---11	111. 11---11
16. 00---00	48. 01---00	80. 10---00	112. 11---00
17. 00---01	49. 01---01	81. 10---01	113. 11---01
18. 00---10	50. 01---10	82. 10---10	114. 11---10
19. 00---11	51. 01---11	83. 10---11	115. 11---11
20. 00---00	52. 01---00	84. 10---00	116. 11---00
21. 00---01	53. 01---01	85. 10---01	117. 11---01
22. 00---10	54. 01---10	86. 10---10	118. 11---10
23. 00---11	55. 01---11	87. 10---11	119. 11---11
24. 00---00	56. 01---00	88. 10---00	120. 11---00
25. 00---01	57. 01---01	89. 10---01	121. 11---01
26. 00---10	58. 01---10	90. 10---10	122. 11---10 HSA A 3
27. 00---11	59. 01---11	91. 10---11	123. 11---11 HSA A 2
28. 00---00	60. 01---00	92. 10---00	124. 11---00
29. 00---01	61. 01---01	93. 10---01	125. 11---01 HSA A 1
30. S. W.	62. S. W.	94. P. W.	126. P. W.
31. P. W.	63. P. W.	95. P. W.	127. P. W.

S. W. - Scratch Word
P. W. - Process Word

Figure 34. Control Word Assignment--Four MCA's

These rates do not take into consideration whether: (1) the processing capability of the 7750 is adequate to manipulate the total number of bits being received, or (2) information will be lost due to too frequent demands for channel service.

In addition, the bit rates discussed in this section do not include the effects of distortion. In many cases, the bit rates given assume perfect bit shapes. If distortion shortens a bit, the equivalent bit rate is raised. For example, consider a transmission rate of 100 bits per second, subject to 10% distortion, which may shorten the bit. The minimum bit length is nine ms, corresponding to an equivalent bit rate of 111 bits per second. All bit rates given will still apply if the only effect of distortion is to lengthen the bit.

The 7750 is designed so that the process control scanner must scan every communication channel at least once during each bit time on that channel. Additionally, the MCA must take a certain minimum number of scans per bit time on each channel.

MCA	MCA-B
0. 00---00	32. 01---00
1. 00---01	33. 01---01
2. 00---10	34. 01---10
3. 00---11	35. 01---11
4. 00---00	36. 01---00
5. 00---01	37. 01---01
6. 00---10	38. 01---10
7. 00---11	39. 01---11
8. 00---00	40. 01---00
9. 00---01	41. 01---01
10. 00---10	42. 01---10
11. 00---11	43. 01---11
12. 00---00	44. 01---00
13. 00---01	45. 01---01
14. 00---10	46. 01---10
15. 00---11	47. 01---11
16. 00---00	48. 01---00
17. 00---01	49. 01---01
18. 00---10	50. 01---10
19. 00---11	51. 01---11
20. 00---00	52. 01---00
21. 00---01	53. 01---01
22. 00---10	54. 01---10
23. 00---11	55. 01---11
24. 00---00	56. 01---00
25. 00---01	57. 01---01
26. 00---10	58. 01---10
27. 00---11	59. 01---11
28. 00---00	60. 01---00
29. 00---01	61. 01---01
30. S.W.	62. S.W.
31. P.W.	63. P.W.
64. 10---00 HSA	96. 11---00 HSA
65. 10---01	97. 11---01
66. 10---10 B-4	98. 11---10 A-1
67. 10---11	99. 11---11
68. 10---00	100. 11---00 HSA
69. 10---01	101. 11---01
70. 10---10	102. 11---10 A-2
71. 10---11	103. 11---11
72. 10---00	104. 11---00
73. 10---01	105. 11---01 HSA
74. 10---10	106. 11---10 A-3
75. 10---11	107. 11---11
76. 10---00	108. 11---00
77. 10---01	109. 11---01
78. 10---10	110. 11---10 HSA
79. 10---11	111. 11---11 A-4
80. 10---00	112. 11---00
81. 10---01	113. 11---01
82. 10---10	114. 11---10 HSA
83. 10---11	115. 11---11 B-1
84. 10---00	116. 11---00
85. 10---01	117. 11---01
86. 10---10	118. 11---10 HSA
87. 10---11	119. 11---11 B-2
88. 10---00	120. 11---00
89. 10---01	121. 11---01 HSA
90. 10---10	122. 11---10 B-3
91. 10---11	123. 11---11
92. 10---00	124. 11---00
93. 10---01	125. 11---01
94. P.W.	126. P.W.
95. P.W.	127. P.W.

S. W. = Scratch Word
P. W. = Process Word

Figure 35. Control Word Assignment--Fewer Than Four MCA's

These requirements apply to both the high-speed adapters and the MCA. The following terms apply:

H = total number of process control scan points used for all adapters.

L = number of low-speed channels connected to an MCA, including the test channel.

N = number of main frame scan points connected to an MCA.

The multiplexing channel adapter will operate with a variety of bit rates, generally at 200 bits per second or less. Regardless of the operating speed, the following fundamental requirements must be specified:

1. Each MCA must scan an odd number of lines. The quantities H and L must contain no common factors.

2. Each MCA in an I-O frame must scan the same number of lines. This may mean scanning unused points in some MCA's.

3. Up to six different bit rates may be used in one MCA. These speeds are assigned in groups of four channels. Scanning conditions, which insure that the highest bit rate will be properly scanned, insure that all lower bit rates will also be properly scanned.

4. Each MCA may be connected to one, two, three, or four process control scan points. The more process control scan points used, the higher the bit rate that can be scanned in the MCA.

Assuming that these requirements are met, Figures 36 and 37 give the maximum bit rates that can be scanned with various numbers of process control scan points and various numbers of MCA scan points. These figures show the bit rates when an MCA is connected to one, two, three, or four process control scan points.

Number of PCR Scan Points

D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16									
E	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s	b/s									
1	All bit rates in this range are greater than 200 bits per second																								
3																									
5																									
7																									
9																									
11																									
13																	196	182	170						
15																	181	170	-	149					
17																	190	174	160	150	139	140			
19																	187	170	155	143	133	124	116		
21																	169	153	-	130	-	-	105		
23																	193	171	154	140	128	118	110	103	96
25																	177	157	-	129	118	109	101	-	88
27	188	164	-	131	119	-	101	94	-	82															
29	175	153	136	122	111	102	94	87	81	76															

- indicates invalid combination

Figure 36. Multiplexor Scanning Where a Low-Speed Group Is Connected to One PCR Scan Point

		Number of PCR Scan Points								
		1 to 12 b/s	13 b/s	14 b/s	15 b/s	16 b/s				
Number of Low-Speed Group Scan Points	To	<div style="border: 1px solid black; padding: 5px; display: inline-block;"> All bit rates in this range are greater than 200 bps </div>								
	21									
	23						193	193		
	25						---	177		
	27						188	188	---	164
29	175	175	153	153						

---indicates invalid combination

Figure 37. Multiplexor Scanning Capabilities Where a Low Speed Group Is Connected to Two PCR Scan Points

In order to obtain the bit rates shown in Figures 38, 39, and 40, the process control scan points to which the MCA is connected cannot be arbitrarily chosen. In general, certain combinations of scan points must be used. Figures 38, 39, and 40 show the proper combination of scan points for various numbers of MCA scan points and process control scan points. In some cases, more than one combination of scan points will give equivalent results. In all cases, the starting point of the combination has been referred to scan point 1. This represents an arbitrary reference point. For example, the combination 1-5-9 is equivalent to 2-6-10, or 5-9-13.

		Number of PCR Scan Points															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Number of MCA Scan Points	H																
	L																
	1	-	A	A	A	A	A	1,5	1,5	1,6	1,6	1,7	1,7	1,8	1,8	1,9	1,9
	3	-	A	-	A	A	-	1,6	1,5	-	1,6	1,8	-	1,9	1,8	-	1,9
	5	-	A	A	A	-	1,4	1,7	1,5	1,8	-	1,9	1,7	1,10	1,8	-	1,9
	7	-	A	A	A	A	1,4	-	1,5	1,9	1,6	1,10	1,7	1,11	-	1,12	1,9
	9	-	A	-	A	A	-	1,2	1,5	-	1,6	1,11	-	1,12	1,8	-	1,9
	11	-	A	A	A	A	1,4	1,3	1,5	1,2	1,6	-	1,7	1,13	1,8	1,14	1,9
	13	-	A	A	A	A	1,4	1,4	1,5	1,3	1,6	1,2	1,7	-	1,8	1,15	1,9
	15	-	A	-	A	-	-	1,5	1,5	-	-	1,3	-	1,2	1,8	-	1,9
	17	-	A	A	A	A	1,4	1,6	1,5	1,5	1,6	1,4	1,7	1,3	1,8	1,2	1,9
	19	-	A	A	A	A	1,4	1,7	1,5	1,6	1,6	1,5	1,7	1,4	1,8	1,3	1,9
	21	-	A	-	A	A	-	-	1,5	-	1,6	1,6	-	1,5	-	-	1,9
	23	-	A	A	A	A	1,4	1,2	1,5	1,8	1,6	1,7	1,7	1,6	1,8	1,5	1,9
	25	-	A	A	A	-	1,4	1,3	1,5	1,9	-	1,8	1,7	1,7	1,8	-	1,9
	27	-	A	-	A	A	-	1,4	1,5	-	1,6	1,9	-	1,8	1,8	-	1,9
29	-	A	A	A	A	1,4	1,5	1,5	1,2	1,6	1,10	1,7	1,9	1,8	1,8	1,9	

- Indicates invalid combination; A indicates arbitrary connection

Figure 38. Connection Point When an MCA Is Connected to Two Process Control Rack Scan Points

Number of PCR Scan Points

L \ H	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	1			A	A	A	A	1-3-5 1-2-5	1,4,6	1,4,7	1-4-7 1-3-7	1,4,8	1,5,9	1-5-9 1-4-9	1,6,11	1,6,11
3			-	A	A	-	1-2-3 1-3-5	1,2,3	-	1-2-3 1-3-5	1,2,3	-	1-2-3 1-3-5	1,2,3	-	1-2-3 1-3-5
5			A	A	-	A	1-2-5 1-2-3	1,2,3	1,4,7	-	1,3,5	1,5,9	1-2-8 1-2-3	1,4,7	-	1-3-10 1-3-5
7			A	A	A	A	-	1,4,6	1,4,7	1-2-3 1-3-5	1,2,7	1,5,9	1-3-5 1-5-9	-	1,6,11	1-4-7 1-5-11
9			-	A	A	-	1-2-5 1-2-3	1,4,6	-	1-4-7 1-3-7	1,4,7	-	1-4-7 1-2-8	1,4,7	-	1-4-7 1-5-11
11			A	A	A	A	1-2-3 1-3-5	1,2,3	1,4,7	1-4-7 1-3-7	-	1,5,9	1-4-9 1-4-7	1,2,3	1,6,11	1-3-10 1-3-5
13			A	A	A	A	1-3-5 1-2-5	1,2,3	1,4,7	1-2-3 1-3-5	1,4,7	1,5,9	-	1,5,10	1,6,11	1-2-3 1-3-5
15			-	A	-	-	A	1,4,6	-	-	1,2,7	-	1-4-9 1-4-7	1,5,10	-	1-6-11 1-5-11
17			A	A	A	A	1-2-3 1-3-5	1,4,6	1,4,7	1-2-3 1-3-5	1,4,7	1,5,9	1-3-5 1-2-8	1,2,3	1,6,11	1-6-11 1-5-11
19			A	A	A	A	1-2-5 1-2-3	1,2,3	1,4,7	1-4-7 1-3-7	1,2,3	1,5,9	1-3-5 1-5-9	1,4,7	1,6,11	1-2-3 1-3-5
21			-	A	A	-	-	1,2,3	-	1-4-7 1-3-7	1,4,8	-	1-2-8 1-2-3	1,4,7	1,6,11	1-3-10 1-3-5
23			A	A	-	A	1-2-5 1-2-3	1,4,6	1,4,7	1-2-3 1-3-5	1,4,8	1,5,9	1-2-3 1-3-5	1,4,7	1,6,11	1-4-7 1-5-11
25			A	A	-	A	1-2-3 1-3-5	1,4,6	1,4,7	-	1,2,3	1,5,9	1-5-9 1-4-9	1,2,3	-	1-4-7 1-5-11
27			-	A	A	-	1-3-5 1-2-5	1,2,3	-	1-2-3 1-3-5	1,3,5	-	1-5-9 1-4-9	1,5,10	-	1-3-10 1-3-5
29			A	A	A	A	A	1,2,3	1,4,7	1-4-7 1-3-7	1,2,7	1,5,9	1-2-3 1-3-5	1,5,10	1,6,11	1-2-3 1-3-5

- Indicates invalid combination; A indicates arbitrary connection

Figure 39. Connection Points When an MCA Is Connected to Three PCR Scan Points

Number of PCR Scan Points

H L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1				A	A	A	A	1,3,5,7	1-3-5-7 1-2-4-7 1-2-5-7	1,4,7,10 1,3,5,8 1,3,6,8	1,4,7,10	1,4,7,10	1-4-7-10 1-2-6-10 1-3-7-11 1-3-7-10	1-4-8-12 1-5-8-12 1-3-7-11	1,5,9,13	1,5,9,13
3				A	A	-	A	1,3,5,7	-	1,2,3,4 1,2,3,7 1,2,6,7	1,3,5,7	-	1-2-6-10 1-2-3-4 1-2-3-10 1-2-6-7	1-3-5-10 1-3-8-10 1-3-5-7	1,4,7,10	1,5,9,13
5				A	-	A	A	1,3,5,7	1-2-3-4 1-2-5-8 1-2-4-8	-	1,2,5,9	1,4,7,10	1-3-5-7 1-2-7-8 1-2-4-8 1-3-7-10	1-2-3-9 1-2-8-9 1-3-7-9	-	1,5,9,13
7				A	A	A	-	1,3,5,7	1-2-5-6 1-2-4-7 1-2-4-5	1,2,3,4 1,2,3,7 1,2,6,7	1,2,3,4	1,4,7,10	1-3-6-11 1-3-5-7 1-2-4-6 1-3-4-6	-	1,3,5,7	1,5,9,13
9				A	A	-	A	1,3,5,7	-	1,2,5,8 1,3,5,8 1,3,6,8	1,2,6,7	-	1-2-3-4 1-4-7-10 1-2-4-7 1-3-4-6	1-2-3-9 1-2-8-9 1-3-7-9	-	1,5,9,13
11				A	A	A	A	1,3,5,7	1-2-5-6 1-2-5-8 1-2-4-5	1,4,7,10 1,4,7,9 1,4,6,9	-	1,4,7,10	1-2-7-8 1-3-6-11 1-2-7-10 1-2-6-7	1-3-5-10 1-3-8-10 1-3-5-7	1,2,3,4	1,5,9,13
13				A	A	A	A	1,3,5,7	1-2-3-4 1-2-4-7 1-2-4-8	1-2-3-4 1-2-3-7 1-2-6-7	1,2,6,7	1,4,7,10	-	1-4-7-11 1-4-8-11 1-3-7-11	1,2,8,9	1,5,9,13
15				A	-	-	A	1,3,5,7	-	-	1,2,3,4	-	1-2-7-8 1-3-6-11 1-2-6-9 1-2-6-7	1-4-8-12 1-5-8-12 1-3-4-11	-	1,5,9,13
17				A	A	A	A	1,3,5,7	1-3-5-7 1-2-5-8 1-2-5-7	1,2,3,4 1,2,3,7 1,2,6,7	1,2,5,9	1,4,7,10	1-2-3-4 1-4-7-10 1-4-6-7 1-3-4-6	1-3-5-10 1-3-8-10 1-3-5-7	1,2,8,9	1-5-4-13
19				A	A	A	A	1,3,5,7	1-3-5-7 1-2-4-7 1-2-5-7	1,2,5,8 1,3,5,8 1,3,6,8	1,3,5,7	1,4,7,10	1-3-6-11 1-3-5-7 1-3-5-6 1-3-4-6	1-2-3-9 1-2-8-9 1-3-7-9	1,2,3,4	1-5-9-13
21				A	A	-	-	1,3,5,7	-	1,4,7,10 1,4,7,9 1,4,6,9	1,3,6,9	-	1-3-5-7 1-2-7-8 1-3-4-10 1-3-7-10	-	-	1-5-4-13
23				A	A	A	A	1,3,5,7	1-2-3-4 1-2-5-8 1-2-4-8	1,2,3,4 1,2,3,7 1,2,6,7	1,4,7,10	1,4,7,10	1-2-6-10 1-2-3-4 1-2-3-7 1-2-6-7	1-2-3-9 1-2-8-9 1-3-7-9	1,3,5,7	1-5-9-13
25				A	-	A	A	1,3,5,7	1-2-5-6 1-2-4-7 1-2-4-5	-	1,3,5,7	1,4,7,10	1-4-7-10 1-2-6-10 1-3-6-10 1-3-7-10	1-3-5-10 1-3-8-10 1-3-5-7	-	1-5-9-13
27				A	A	-	A	1,3,5,7	-	1,2,3,4 1,2,3,7 1,2,6,7	1,2,5,9	-	1-4-7-10 1-2-6-10 1-3-7-11 1-3-7-10	1-4-7-11 1-4-8-11 1-3-7-11	-	1-5-9-13
29				A	A	A	A	1,3,5,7	1-2-5-6 1-2-5-8 1-2-4-5	1,2,5,8 1,3,5,8 1,3,6,8	1,2,3,4	1,4,7,10	1-2-6-10 1-2-3-4 1-2-3-10 1-2-6-7	1-4-8-12 1-5-8-12 1-3-4-11	1,4,8,12	1-5-9-13

Figure 40. Connection Points When an MCA Is Connected to Four PCR Scan Points

ALPHABETIC LIST OF INSTRUCTIONS, BY NAME

<u>OCTAL</u> <u>OP</u> <u>CODE</u>	<u>MNE</u> <u>MON</u> <u>IC</u>	<u>INSTRUCTION</u>	<u>NO.</u> <u>OF</u> <u>CYCLES</u>	<u>PAGE</u>
1145	AND	AND-	1	29
1165	ANI	AND AND INCREMENT	1	29
1105	ANC	AND COMPLEMENTED-	1	29
1125	ACI	AND COMPLEMENTED AND INCREMENT	1	29
1115	ANC*	AND COMPLEMENTED INDIRECT	2	29
1135	ACI*	AND COMPLEMENTED INDIRECT AND INCREMENT	2	29
1155	AND*	AND INDIRECT	2	29
1175	ANI*	AND INDIRECT AND INCREMENT	2	29
0707	BRA	BRANCH	1	31
0717	BRA*	BRANCH INDIRECT	1	31
0744	BRO	BRANCH ON ONES	1	31
0754	BRO*	BRANCH ON ONES INDIRECT	1	31
0544	BRT	BRANCH ON TEST	1	31
0704	BRZ	BRANCH ON ZERO	1	31
0714	BRZ*	BRANCH ON ZERO INDIRECT	1	31
0003	CAL	COMPARE ADDRESS TO LIMIT	1	31
0023	CAI	COMPARE ADDRESS TO LIMIT AND INCREMENT	1	31
1101	XOR	EXCLUSIVE OR	1	27
1121	XOI	EXCLUSIVE OR AND INCREMENT	1	27
1141	XOC	EXCLUSIVE OR COMPLEMENTED	1	27
1161	XCI	EXCLUSIVE OR COMPLEMENTED AND INCREMENT	1	27
1151	XOC*	EXCLUSIVE OR COMPLEMENTED INDIRECT	2	27
1171	XCI*	EXCLUSIVE OR COMPLEMENTED INDIRECT AND INCREMENT	2	28
1111	XOR*	EXCLUSIVE OR INDIRECT	2	27
1131	XOI*	EXCLUSIVE OR INDIRECT AND INCREMENT	2	27
0702	GTA	GET ADDRESS	1	30
0712	GTA*	GET ADDRESS INDIRECT	2	30
0502	GOA	GET AND OR ADDRESS	1	30
0512	GOA*	GET AND OR ADDRESS INDIRECT	2	30
0102	GOL	GET AND OR LIMIT	1	30
0112	GOL*	GET AND OR LIMIT INDIRECT	2	30
0302	GTL	GET LIMIT	1	30
0312	GTL*	GET LIMIT INDIRECT	2	30
1102	IOR	INCLUSIVE OR	1	28
1122	IOI	INCLUSIVE OR AND INCREMENT	1	28
1142	IOC	INCLUSIVE OR COMPLEMENTED	1	28
1162	ICI	INCLUSIVE OR COMPLEMENTED AND INCREMENT	1	28
1152	IOC*	INCLUSIVE OR COMPLEMENTED INDIRECT	2	28
1172	ICI*	INCLUSIVE OR COMPLEMENTED INDIRECT AND INCREMENT	2	28
1112	IOR*	INCLUSIVE OR INDIRECT	2	28
1132	IOI*	INCLUSIVE OR INDIRECT AND INCREMENT	2	28
1302	LOD	LOAD CHARACTER	1	26
1322	LOI	LOAD CHARACTER AND INCREMENT	1	26
1312	LOD*	LOAD CHARACTER INDIRECT	2	26
1332	LOI*	LOAD CHARACTER INDIRECT AND INCREMENT	2	26

<u>OCTAL</u>	<u>MNE</u>			<u>NO.</u>	
<u>OP</u>	<u>MON</u>		<u>INSTRUCTION</u>	<u>OF</u>	
<u>CODE</u>	<u>IC</u>			<u>CYCLES</u>	<u>PAGE</u>
1342	LDC	LOAD	COMPLEMENTED CHARACTER	1	26
1362	LCI	LOAD	COMPLEMENTED CHARACTER AND INCREMENT	1	26
1352	LDC*	LOAD	COMPLEMENTED CHARACTER INDIRECT	2	26
1372	LCI*	LOAD	COMPLEMENTED CHARACTER INDIRECT AND INCREMENT	2	26
0106	MOC	MOVE	WORD AND OR TO CONTROL STORAGE	2	31
0116	MOC*	MOVE	WORD AND OR TO CONTROL STORAGE INDIRECT	2	31
0306	MWC	MOVE	WORD TO CONTROL STORAGE	2	31
0316	MWC*	MOVE	WORD TO CONTROL STORAGE INDIRECT	2	31
0206	MWP	MOVE	WORD TO PROCESS STORAGE	2	31
0216	MWP*	MOVE	WORD TO PROCESS STORAGE INDIRECT	2	31
1042	OCF	OR	COMPLEMENT TO PROCESS STORAGE	1	29
1052	OCF*	OR	COMPLEMENT TO PROCESS STORAGE INDIRECT	2	29
1072	OCI*	OR	COMPLEMENT TO PROCESS STORAGE INDIRECT AND INCREMENT	2	29
1002	ORP	OR	TO PROCESS STORAGE	1	28
1012	ORP*	OR	TO PROCESS STORAGE INDIRECT	2	28
1032	ORI*	OR	TO PROCESS STORAGE INDIRECT AND INCREMENT	2	28
0602	PTA	PUT	ADDRESS	1	30
0612	PTA*	PUT	ADDRESS INDIRECT	2	30
0202	PTL	PUT	LIMIT	1	30
0212	PTL*	PUT	LIMIT INDIRECT	2	30
0000	SNS	SENSE		1	32
0706	TAC	TRANSMIT	ADDRESS TO CONTROL STORAGE	2	30
0716	TAC*	TRANSMIT	ADDRESS TO CONTROL STORAGE INDIRECT	2	30
0606	TAP	TRANSMIT	ADDRESS TO PROCESS STORAGE	2	30
0616	TAP*	TRANSMIT	ADDRESS TO PROCESS STORAGE INDIRECT	2	30
0506	TOC	TRANSMIT	AND OR ADDRESS TO CONTROL STORAGE	2	30
0516	TOC*	TRANSMIT	AND OR ADDRESS TO CONTROL STORAGE INDIRECT	2	31
1202	UNL	UNLOAD	CHARACTER	1	27
1212	UNL*	UNLOAD	CHARACTER INDIRECT	2	27
1232	ULI*	UNLOAD	CHARACTER INDIRECT AND INCREMENT	2	27
1242	ULC	UNLOAD	COMPLEMENTED CHARACTER	1	27
1252	ULC*	UNLOAD	COMPLEMENTED CHARACTER INDIRECT	2	27
1272	UCI*	UNLOAD	COMPLEMENTED CHARACTER INDIRECT AND INCREMENT	2	27

ALPHABETIC LIST OF INSTRUCTIONS, BY MNEMONICS

<u>OCTAL</u> <u>OP</u> <u>CODE</u>	<u>MNE</u> <u>MON</u> <u>IC</u>	<u>INSTRUCTION</u>	<u>NO.</u> <u>OF</u> <u>CYCLES</u>	<u>PAGE</u>
1125	ACI	AND COMPLEMENTED AND INCREMENT	1	29
1135	ACI*	AND COMPLEMENTED INDIRECT AND INCREMENT	2	29
1105	ANC	AND COMPLEMENTED	1	29
1115	ANC*	AND COMPLEMENTED INDIRECT	2	29
1145	AND	AND	1	29
1155	AND*	AND INDIRECT	2	29
1165	ANI	AND AND INCREMENT	1	29
1175	ANI*	AND INDIRECT AND INCREMENT	2	29
0707	BRA	BRANCH	1	31
0717	BRA*	BRANCH INDIRECT	1	31
0744	BRO	BRANCH ON ONES	1	31
0754	BRO*	BRANCH ON ONES INDIRECT	1	31
0544	BRT	BRANCH ON TEST	1	31
0704	BRZ	BRANCH ON ZERO	1	31
0714	BRZ*	BRANCH ON ZERO INDIRECT	1	31
0023	CAI	COMPARE ADDRESS TO LIMIT AND INCREMENT	1	31
0003	CAL	COMPARE ADDRESS TO LIMIT	1	31
0502	GOA	GET AND OR ADDRESS	1	30
0512	GOA*	GET AND OR ADDRESS INDIRECT	2	30
0102	GOL	GET AND OR LIMIT	1	30
0112	GOL*	GET AND OR LIMIT INDIRECT	2	30
0702	GTA	GET ADDRESS	1	30
0712	GTA*	GET ADDRESS INDIRECT	2	30
0302	GTL	GET LIMIT	1	30
0312	GTL*	GET LIMIT INDIRECT	2	30
1162	ICI	INCLUSIVE OR COMPLEMENTED AND INCREMENT	1	28
1172	ICI*	INCLUSIVE OR COMPLEMENTED INDIRECT AND INCREMENT	2	28
1142	IOC	INCLUSIVE OR COMPLEMENTED	1	28
1152	IOC*	INCLUSIVE OR COMPLEMENTED INDIRECT	2	28
1122	IOI	INCLUSIVE OR AND INCREMENT	1	28
1132	IOI*	INCLUSIVE OR INDIRECT AND INCREMENT	2	28
1102	IOR	INCLUSIVE OR	1	28
1112	IOR*	INCLUSIVE OR INDIRECT	2	28
1362	LCI	LOAD COMPLEMENTED CHARACTER AND INCREMENT	1	26
1372	LCI*	LOAD COMPLEMENTED CHARACTER INDIRECT AND INCREMENT	2	26
1342	LDC	LOAD COMPLEMENTED CHARACTER	1	26
1352	LDC*	LOAD COMPLEMENTED CHARACTER INDIRECT	2	26
1302	LOD	LOAD CHARACTER	1	26
1312	LOD*	LOAD CHARACTER INDIRECT	2	26
1322	LOI	LOAD CHARACTER AND INCREMENT	1	26
1332	LOI*	LOAD CHARACTER INDIRECT AND INCREMENT	2	26
0106	MOC	MOVE WORD AND OR TO CONTROL STORAGE	2	31
0116	MOC*	MOVE WORD AND OR TO CONTROL STORAGE INDIRECT	2	31
0306	MWC	MOVE WORD TO CONTROL STORAGE	2	31
0316	MWC*	MOVE WORD TO CONTROL STORAGE INDIRECT	2	31

OCTAL OP CODE	MNE MON IC	INSTRUCTION	NO. OF CYCLES	PAGE
0206	MWP	MOVE WORD TO PROCESS STORAGE	2	31
0216	MWP*	MOVE WORD TO PROCESS STORAGE INDIRECT	2	31
1072	OCI*	OR COMPLEMENT TO PROCESS STORAGE INDIRECT AND INCREMENT	2	29
1042	OCP	OR COMPLEMENT TO PROCESS STORAGE	1	29
1052	OCP*	OR COMPLEMENT TO PROCESS STORAGE INDIRECT	2	29
1032	ORI*	OR TO PROCESS STORAGE INDIRECT AND INCREMENT	2	28
1002	ORP	OR TO PROCESS STORAGE	1	28
1012	ORP*	OR TO PROCESS STORAGE INDIRECT	2	28
0602	PTA	PUT ADDRESS	1	30
0612	PTA*	PUT ADDRESS INDIRECT	2	30
0202	PTL	PUT LIMIT	1	30
0212	PTL*	PUT LIMIT INDIRECT	2	30
0000	SNS	SENSE	1	32
0706	TAC	TRANSMIT ADDRESS TO CONTROL STORAGE	2	30
0716	TAC*	TRANSMIT ADDRESS TO CONTROL STORAGE INDIRECT	2	30
0606	TAP	TRANSMIT ADDRESS TO PROCESS STORAGE	2	30
0616	TAP*	TRANSMIT ADDRESS TO PROCESS STORAGE INDIRECT	2	30
0506	TOC	TRANSMIT AND OR ADDRESS TO CONTROL STORAGE	2	30
0516	TOC*	TRANSMIT AND OR ADDRESS TO CONTROL STORAGE INDIRECT	2	31
1272	UCI*	UNLOAD COMPLEMENTED CHARACTER INDIRECT AND INCREMENT	2	27
1242	ULC	UNLOAD COMPLEMENTED CHARACTER	1	27
1252	ULC*	UNLOAD COMPLEMENTED CHARACTER INDIRECT	2	27
1232	ULI*	UNLOAD CHARACTER INDIRECT AND INCREMENT	2	27
1202	UNL	UNLOAD CHARACTER	1	27
1212	UNL*	UNLOAD CHARACTER INDIRECT	2	27
1161	XCI	EXCLUSIVE OR COMPLEMENTED AND INCREMENT	1	27
1171	XCI*	EXCLUSIVE OR COMPLEMENTED INDIRECT AND INCREMENT	2	28
1141	XOC	EXCLUSIVE OR COMPLEMENTED	1	27
1151	XOC*	EXCLUSIVE OR COMPLEMENTED INDIRECT	2	27
1121	XOI	EXCLUSIVE OR AND INCREMENT	1	27
1131	XOI*	EXCLUSIVE OR INDIRECT AND INCREMENT	2	27
1101	XOR	EXCLUSIVE OR	1	27
1111	XOR*	EXCLUSIVE OR INDIRECT	2	27

NUMERICAL LIST OF INSTRUCTIONS, BY OP CODE

<u>OCTAL</u> <u>OP</u> <u>CODE</u>	<u>MNE</u> <u>MON</u> <u>IC</u>	<u>INSTRUCTION</u>	<u>NO.</u> <u>OF</u> <u>CYCLES</u>	<u>PAGE</u>
0000	SNS	SENSE	1	32
0003	CAL	COMPARE ADDRESS TO LIMIT	1	31
0023	CAI	COMPARE ADDRESS TO LIMIT AND INCREMENT	1	31
0102	GOL	GET AND OR LIMIT	1	30
0106	MOC	MOVE WORD AND OR TO CONTROL STORAGE	2	31
0112	GOL*	GET AND OR LIMIT INDIRECT	2	30
0116	MOC*	MOVE WORD AND OR TO CONTROL STORAGE INDIRECT	2	31
0202	PTL	PUT LIMIT	1	30
0206	MWP	MOVE WORD TO PROCESS STORAGE	2	31
0212	PTL*	PUT LIMIT INDIRECT	2	30
0216	MWP*	MOVE WORD TO PROCESS STORAGE INDIRECT	2	31
0302	GTL	GET LIMIT	1	30
0306	MWC	MOVE WORD TO CONTROL STORAGE	2	31
0312	GTL*	GET LIMIT INDIRECT	2	30
0316	MWC*	MOVE WORD TO CONTROL STORAGE INDIRECT	2	31
0502	GOA	GET AND OR ADDRESS	1	30
0506	TOC	TRANSMIT AND OR ADDRESS TO CONTROL STORAGE	2	30
0512	GOA*	GET AND OR ADDRESS INDIRECT	2	30
0516	TOC*	TRANSMIT AND OR ADDRESS TO CONTROL STORAGE INDIRECT	2	31
0544	BRT	BRANCH ON TEST	1	31
0602	PTA	PUT ADDRESS	1	30
0606	TAP	TRANSMIT ADDRESS TO PROCESS STORAGE	2	30
0612	PTA*	PUT ADDRESS INDIRECT	2	30
0616	TAP*	TRANSMIT ADDRESS TO PROCESS STORAGE INDIRECT	2	30
0702	GTA	GET ADDRESS	1	30
0704	BRZ	BRANCH ON ZERO	1	31
0706	TAC	TRANSMIT ADDRESS TO CONTROL STORAGE	2	30
0707	BRA	BRANCH	1	31
0712	GTA*	GET ADDRESS INDIRECT	2	30
0714	BRZ*	BRANCH ON ZERO INDIRECT	1	31
0716	TAC*	TRANSMIT ADDRESS TO CONTROL STORAGE INDIRECT	2	30
0717	BRA*	BRANCH INDIRECT	1	31
0744	BRO	BRANCH ON ONES	1	31
0754	BRO*	BRANCH ON ONES INDIRECT	1	31
1002	ORP	OR TO PROCESS STORAGE	1	28
1012	ORP*	OR TO PROCESS STORAGE INDIRECT	2	28
1032	ORI*	OR TO PROCESS STORAGE INDIRECT AND INCREMENT	2	28
1042	OCP	OR COMPLEMENT TO PROCESS STORAGE	1	29
1052	OCP*	OR COMPLEMENT TO PROCESS STORAGE INDIRECT	2	29
1072	OCI*	OR COMPLEMENT TO PROCESS STORAGE INDIRECT AND INCREMENT	2	29
1101	XOR	EXCLUSIVE OR	1	27
1102	IOR	INCLUSIVE OR	1	28
1105	ANC	AND COMPLEMENTED	1	29
1111	XOR*	EXCLUSIVE OR INDIRECT	2	27
1112	IOR*	INCLUSIVE OR INDIRECT	2	28

<u>OCTAL</u> <u>OP</u> <u>CODE</u>	<u>MNE</u> <u>MON</u> <u>IC</u>	<u>INSTRUCTION</u>	<u>NO.</u> <u>OF</u> <u>CYCLES</u>	<u>PAGE</u>
1115	ANC*	AND COMPLEMENTED INDIRECT	2	29
1121	XOI	EXCLUSIVE OR AND INCREMENT	1	27
1122	IOI	INCLUSIVE OR AND INCREMENT	1	28
1125	ACI	AND COMPLEMENTED AND INCREMENT	1	29
1131	XOI*	EXCLUSIVE OR INDIRECT AND INCREMENT	2	27
1132	IOI*	INCLUSIVE OR INDIRECT AND INCREMENT	2	28
1135	ACI*	AND COMPLEMENTED INDIRECT AND INCREMENT	2	29
1141	XOC	EXCLUSIVE OR COMPLEMENTED	1	27
1142	IOC	INCLUSIVE OR COMPLEMENTED	1	28
1145	AND	AND	1	29
1151	XOC*	EXCLUSIVE OR COMPLEMENTED INDIRECT	2	27
1152	IOC*	INCLUSIVE OR COMPLEMENTED INDIRECT	2	28
1155	AND*	AND INDIRECT	2	29
1161	XCI	EXCLUSIVE OR COMPLEMENTED AND INCREMENT	1	27
1162	ICI	INCLUSIVE OR COMPLEMENTED AND INCREMENT	1	28
1165	ANI	AND AND INCREMENT	1	29
1171	XCI*	EXCLUSIVE OR COMPLEMENTED INDIRECT AND INCREMENT	2	28
1172	ICI*	INCLUSIVE OR COMPLEMENTED INDIRECT AND INCREMENT	2	28
1175	ANI*	AND INDIRECT AND INCREMENT	2	29
1202	UNL	UNLOAD CHARACTER	1	27
1212	UNL*	UNLOAD CHARACTER INDIRECT	2	27
1232	ULI*	UNLOAD CHARACTER INDIRECT AND INCREMENT	2	27
1242	ULC	UNLOAD COMPLEMENTED CHARACTER	1	27
1252	ULC*	UNLOAD COMPLEMENTED CHARACTER INDIRECT	2	27
1272	UCI*	UNLOAD COMPLEMENTED CHARACTER INDIRECT AND INCREMENT	2	27
1302	LOD	LOAD CHARACTER	1	26
1312	LOD*	LOAD CHARACTER INDIRECT	2	26
1322	LOI	LOAD CHARACTER AND INCREMENT	1	26
1332	LOI*	LOAD CHARACTER INDIRECT AND INCREMENT	2	26
1342	LDC	LOAD COMPLEMENTED CHARACTER	1	26
1352	LDC*	LOAD COMPLEMENTED CHARACTER INDIRECT	2	26
1362	LCI	LOAD COMPLEMENTED CHARACTER AND INCREMENT	1	26
1372	LCI*	LOAD COMPLEMENTED CHARACTER INDIRECT AND INCREMENT	2	26

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AND INSTRUCTION	29	CLEAR SWITCH	47
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