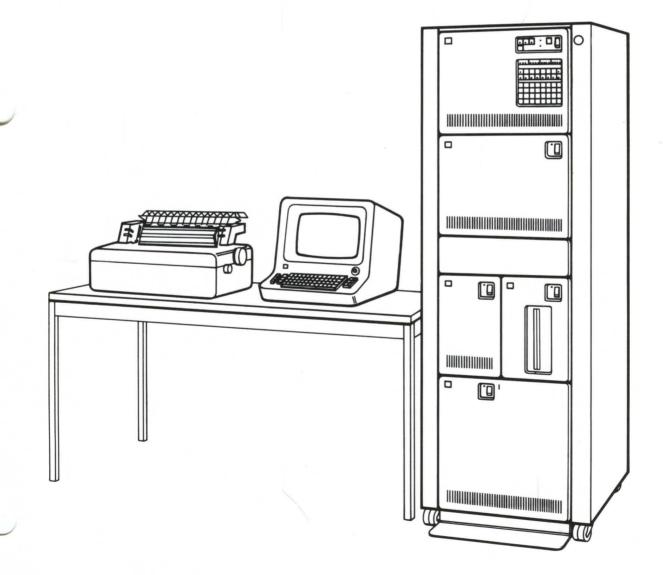


SERIES/1 SYSTEM SUMMARY

GA34-0035-1 File No. S1-00

IBM Series/1 System Summary





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GA34-0035-1 File No. S1-00

IBM Series/1 System Summary

Second Edition (March 1977)

This is a major revision of, and obsoletes GA34-0035-0. Significant changes in this edition include: a new introductory chapter, new processor models, a new line printer, and several new programming products. Numerous changes have been made, and new material added, throughout the manual. Therefore, the manual should be reviewed in its entirety.

Changes are periodically made to the information herein; any such changes will be reported in subsequent revisions or Technical Newsletters. Before using this publication in connection with the operation of IBM systems, have your IBM representative confirm editions that are applicable and current.

A form for readers' comments is provided at the back of this publication. If the form has been removed, send your comments to IBM Corporation, Systems Publications, Department 27T, P.O. Box 1328, Boca Raton, Florida 33432. Comments become the property of IBM.

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This publication is an introduction and reference summary for the IBM Series/1, a family of processors with a varied offering of data processing I/O devices and I/O attachment capabilities. I/O attachment capabilities include: sensor I/O equipment, communications lines, and custom devices. Customer executives, system designers, and programmers, who need a summarized description of what Series/1 is and how it can be used, will find this manual helpful. Others, such as engineers and technicians, will also find this publication useful for initial information when first learning the Series/1.

The subject matter is divided into six major categories:

- Introduction
- Processors and processor features
- User attachment features
- Communications features
- I/O and system support units
- Programming support

This manual is an introduction to the Series/1. A familiarity with data processing concepts and event driven systems is assumed.

Related Publications

The following publications describe in detail various portions of the Series/1. For information regarding current availability of all related Series/1 publications, consult your IBM representative.

Hardware

Processing Units and General Hardware

- IBM Series/1 Model 5 4955 Processor and Processor Features Description, GA34-0021. Describes the functions of the processor including the I/O channel and storage; also includes features directly related to the processor. Provides machine code information for the 4955 instruction set and system-defined I/O operations.
- IBM Series/1 Model 3 4953 Processor and Processor Features Description, GA34-0022. Describes the functions of the processor including the I/O channel and storage; also includes features directly related to the processor. Provides machine code information for the 4953 instruction set and system-defined I/O operations.
- *IBM Series/1 Installation Manual-Physical Planning*, GA34-0029. Describes the physical, electrical, and environmental specifications necessary to *plan* the installation of a Series/1.
- IBM Series/1 Configurator, GA34-0042. Lists all the machine types and features available for Series/1 including maximum quantities and prerequisites. This manual, together with the IBM Series/1 Installation Manual-Physical Planning, is of assistance in planning a Series/1 installation.
- *IBM Series/1 4999 Battery Backup Unit Description*, GA34-0032. Describes the functions and requirements of this unit.

Data Processing I/O Units and Features

Each of the following manuals describes the functions of the I/O unit and its associated attachment feature. Each publication provides the machine code information for the I/O commands, status words, and condition codes.

- IBM Series/1 4962 Disk Storage Unit and 4964 Diskette Unit Description, GA34-0024
- IBM Series/1 4973 Line Printer Description, GA34-0044
- IBM Series/1 4974 Printer Description, GA34-0025
- IBM Series/1 4979 Display Station Description, GA34-0026

Sensor I/O Units and Features

• IBM Series/1, 4982 Sensor Input/Output Unit Description, GA34-0027. Describes the functions of the 4982, its associated attachment feature, and the analog and digital features that are available. Provides the machine code information for the I/O commands, status words, and condition codes.

Communications Features

• *IBM Series/1 Communications Features Description*, GA34-0028. Describes the functions of the asynchronous, binary synchronous, and synchronous data link communications features. Provides the machine code information for the I/O commands, status words, and condition codes.

User Attachment Features

These manuals cover the following features: timers, teletypewriter adapter, customer direct program control, and integrated digital I/O-non-isolated. The channel attachment features are also included.

- *IBM Series/1 Attachment Features Description*, GA34-0031. Describes the functions of each feature. Provides the machine code information for the I/O commands, status words, and condition codes.
- *IBM Series/1 User's Attachment Manual*, GA34-0033. Provides information to assist the user in attaching his equipment to the I/O channel and designated attachment features.

Software

- IBM Series/1 Realtime Programming System: Introduction and Planning Guide, GC34-0102. Introduces the features of the Realtime Programming System and provides information needed to plan a Series/1 software system.
- *IBM Series/1 Program Preparation Subsystem: Introduction*, GC34-0121. Provides a general understanding of the program preparation components and their use in a batch processing environment.
- IBM Series/1 Program Preparation Subsystem: Macro Assembler User's Guide, SC34-0124. Provides the information necessary to code assembler language programs and to assemble them.
- *IBM Series/1 FORTRAN IV: Introduction*, GC34-0132. Summarizes the Series/1 FORTRAN IV language and identifies the resources required to support preparation and execution of FORTRAN IV programs.
- IBM Series/1 FORTRAN IV: Language Reference, GC34-0133. Describes, in detail, the Series/1 FORTRAN IV language elements, and provides descriptions of FORTRAN IV-supplied procedures and the FORTRAN IV Realtime Subroutine Library.
- IBM Series/1 Mathematical and Functional Subroutine Library: Introduction, GC34-0138. Summarizes the Series/1 MFSL subroutines and identifies resources required to support preparation and execution of these subroutines.
- *IBM Series/1 PL/I: Introduction*, GC34-0084. Provides an introduction to the PL/I language support for Series/1 and identifies the resources required to support preparation and execution of PL/I programs.
- IBM Series/1 Base Program Preparation Facilities User's Guide, SC34-0072. Describes how to use the Base Program Preparation Facilities—a text editor, macro assembler, and linkage editor. The book also contains a list of all the messages generated by each program.
- IBM Series/1 Base Program Preparation Facilities Macro Assembler Programmer's Guide, SC34-0074. Provides the information on how to code an assembler language program for the Series/1.
- IBM Series/1 Base Program Preparation Facilities Assembler Language Reference Card, SX34-0076. Provides a quick reference for the Series/1 instruction mnemonics and format.
- *IBM Series/1 Stand-Alone Utilities User's Guide*, GC34-0070. Describes the utilities provided as system control programming with the Series/1 processor, and how to use them.

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Chapter 1. Introduction

This chapter provides an overview of the IBM Series/1. Included are overviews of system design, system components, and programming support. Each topic discussed in this chapter is expanded in later chapters in this manual and in the other manuals that are referenced in the "Preface."

System Design Overview

Series/1 is a family of small general-purpose computers with a varied offering of data processing input/output (I/O) devices and I/O attachment capabilities. The I/O attachment capabilities include: sensor I/O equipment, communications lines, and custom devices. High reliability is projected for the Series/1 through the use of LSI (large scale integration) technology in the processor and MOSFET (metal-oxide semiconductor, field-effect transistor) logic in main storage.

Series/1 is a comprehensive computer system. It is suitable for a variety of applications including conventional data processing as well as sensor-based applications such as energy management and controlled-access security systems.

The Series/1 was designed to meet the needs of installations requiring a single computer or multiple small computing systems. To achieve the flexibility required for various types of installations, the Series/1 is modular in design—most units fit into an EIA* (RS-310B) 19-inch rack. Figure 1-1 shows how the processor and other modular units can be mounted in an IBM rack enclosure. The figure also shows two table-top I/O units, a serial printer, and a display station.

*Electronic Industries Association

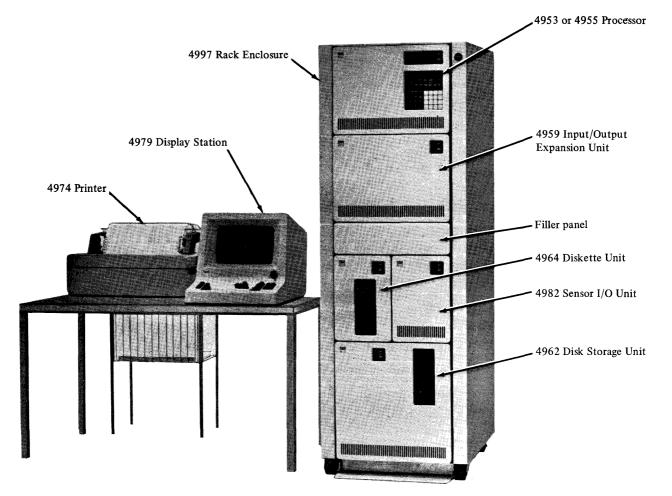


Figure 1-1. Series/1 with modular units mounted in an IBM 4997 Rack Enclosure

For additional flexibility, individual I/O attachment features, processor features, and storage additions are constructed on multi-layer printed-circuit cards. These circuit cards can be selectively plugged into sockets on the backpanel of certain modular units (Figure 1-2). Thus, by selecting the desired modular units and combinations of circuit cards, a system can be customized to meet the needs of the user.

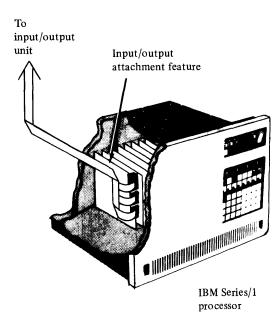


Figure 1-2. Illustration showing how input/output attachment features are plugged into a modular unit

Figure 1-3 shows how Series/1 units and features are grouped. IBM machine-type numbers are assigned to the modular units, enclosures, and DP I/O devices. Features, either I/O attachment cards or other components, are available to expand the capability of the various machine types.

The processor units contain the basic processor card(s), basic storage, basic console, a power supply, and card sockets for plugging processor features, storage additions, and I/O attachment features. When additional I/O capacity is needed, I/O expansion units are available; these units contain a power supply and card sockets for plugging additional I/O feature cards. In some cases, a channel repower feature is required when attaching an I/O expansion unit. This is discussed in Chapter 3.

A battery backup unit is available to switch the processor unit to a user-supplied battery during ac power interruptions. The primary intent of the backup unit is to preserve the contents of processor storage; I/O devices and other units are not powered from the battery backup unit.

IBM rack enclosures include a primary-power receptacle-panel for powering the individual modular units that can be installed in the enclosure. When a system requires space for modular units beyond the capacity of a single rack, multiple racks can be bolted together to form a *multi-bay enclosure*.

I/O attachment feature cards plug into the processor I/O channel sockets. The processor I/O channel directs the flow of information between I/O devices and main storage. There are four categories of I/O attachment feature cards: DP I/O attachment features, communications features, user attachment features, and the sensor I/O unit attachment feature. Sensor I/O feature cards plug into the sensor I/O unit. Each category of features is discussed in subsequent sections of this publication.

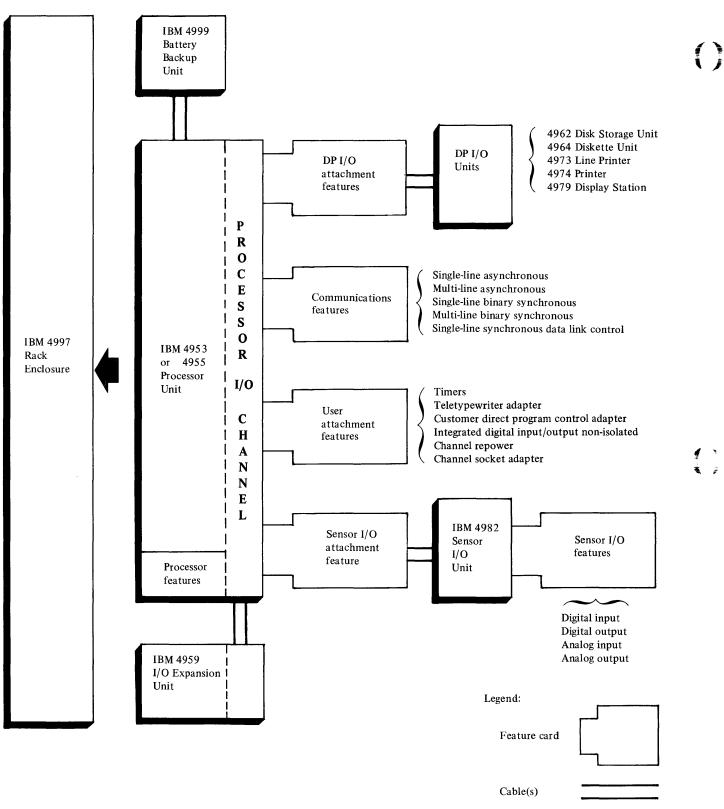


Figure 1-3. Diagram showing how Series/1 units and features are grouped

The following sections provide general descriptions of the Series/1 machine types and each major feature. Additional information about these hardware components can be found in Chapters 2 through 5.

Processor Units

The IBM Series/1 family includes two processors: the Series/1 Model 3 uses a 4953 Processor and the Series/1 Model 5 uses a 4955 Processor. The 4955 Processor has more storage capacity and greater internal speed than the 4953 Processor. The 4955 also offers some special features not available on the 4953. The processor features are discussed in Chapter 2.

IBM 4953 and 4955 Processors

The IBM 4953 Processor and the IBM 4955 Processor are modular units designed to fit in an IBM 4997 Rack Enclosure or an EIA (RS-310B) rack. Each processor unit includes the circuit card(s) that (1) control the interpretation and execution of instructions and (2) generate the I/O channel that links the processor with its external resources.

As previously mentioned, each processor unit also contains a power supply, basic storage, and space for: storage additions, processor features, and I/O attachment features. A basic console is standard with either processor. A programmer console is available as an optional feature.

Both processors have an upward compatible instruction set that is rich in function. This instruction set includes a full complement of bit, byte, 16-bit word, and 32-bit doubleword operations. Also, each processor can operate on four different processing levels. An interrupt mechanism automatically switches levels on a preemptive priority basis. Additional characteristics of the processors are discussed in Chapter 2.

The 4955 Processor differs from the 4953 Processor in four major areas:

- Storage size and address management. The 4955 has a maximum storage capacity of 128K bytes; while the 4953 has a maximum capacity of 64K bytes.
- Speed. The 4955 has approximately three times the internal performance of the 4953 (based on average execution time).
- *Hardware floating-point instructions*. The 4955 has an optional floating-point feature that is not offered on the 4953.
- *Storage protection.* This facility is standard on the 4955, but is not offered on the 4953.

For a comparison of the two processors in tabular form, refer to Chapter 2.

Data Processing I/O Units

This section provides an overview for each data processing I/O unit. Each unit requires an I/O attachment feature card for attachment to the processor I/O channel. The attachment feature can be plugged into either the processor or an I/O expansion unit. For more detailed information about each data processing I/O unit, refer to Chapter 5.

IBM 4962 Disk Storage Unit

The IBM 4962 Disk Storage Unit is a full-width modular unit. It provides substantial direct-access storage for both data records and programs. Data is stored on a fixed magnetic disk. Movable heads are used to read and write data. The total disk capacity is 9,308,160 bytes. Two models of the 4962 are equipped with eight fixed heads to read and write data on the disk. The fixed-head capacity is 122,880 bytes of storage.

The fixed disk and access mechanism are sealed in an enclosure that offers the following advantages:

- Preventive maintenance of the heads, disk, and spindle is eliminated.
- Reliability is improved by dedicated read/write heads; each head reads only the data it has previously written.
- Exposure to external contaminants is virtually eliminated.
- Operator handling is eliminated.

Additional models of the 4962 offer a combination of the disk unit just described and the diskette unit. The diskette unit adds 492,544 bytes (minimum) of storage on a removable diskette. The diskette unit is identical to the IBM 4964 Diskette Unit described in the following section.

IBM 4964 Diskette Unit

The IBM 4964 Diskette Unit is a half-width modular unit designed to fit in an EIA (RS-310B) rack. Data is stored on a removable magnetic media called a diskette. By interchanging diskettes, the Series/1 operator can load new programs or transfer data between systems.

Each side of the diskette has 74 data tracks. Two heads, one on each side of the diskette, are used to read or write data. The total storage capacity of the diskette depends on the data format being used. The following table shows the total storage capacity for the various formats using both sides of the diskette.

Total storage capacity
492,544 bytes
568,320 bytes
606,208 bytes

IBM 4973 Line Printer

The IBM 4973 Line Printer is a free-standing unit. It is an impact-type line printer with 132 print positions per line. This printer provides a medium-to-high speed "hard copy" output for the Series/1 on continuous form paper. The 4973 Printer is available in two print speeds-155 and 414 lines per minute when using a print belt with a character-set length of 48 characters. The print belt is interchangeable; other print belts are available with 64 or 94 EBCDIC character sets. The printer has a programmable vertical forms control; vertical line spacing is either 6 or 8 lines per inch. A pin feed carriage is provided and handles up to six-part forms.

IBM 4974 Printer

The IBM 4974 Printer is a table-top device. It is a serial printer with a wire-matrix print head that produces characters by a pattern of dots. This printer provides a medium-speed "hard copy" output for the Series/1 on either cut or continuous form paper. Printing is performed at a 120 characters per second, bidirectional. The characters are printed 10 per inch with a maximum of 132 characters per line. A forms tractor unit is provided for margin-punched forms of up to six parts.

IBM 4979 Display Station

The IBM 4979 Display Station is a table-top device with a keyboard and cathode ray tube (CRT) display. It serves as a communications link between the operator and the Series/1. The display station provides the ability to (1) enter, modify, or delete data on the display and (2) cause the revised data to be returned to the processor.

The screen is a 12-inch CRT formatted as 24 lines of 80 characters (1920 characters total). Each character is displayed as a pseudo 7 x 7 dot matrix. All information displayed on the screen is refreshed 50/60 times per second, creating an easy-to-read display under normal lighting conditions. Two levels of intensity allow special fields and characters, such as the cursor, to appear brighter than other characters.

The data-entry keyboard design is similar to that of a typewriter. The keyboard has 66 keys allowing input of alphanumeric characters, functions, and interrupt requests. Keys are color coded by function for ease of use. For example, local function keys have white letters on charcoal-grey key tops.

Sensor I/O Units and Features

Sensor input/output units and features permit the Series/1 processor to:

- 1. Receive real-time data (analog or digital from transducers, sensors, and other data sources that monitor a physical process).
- 2. Generate signals to elements that control the physical process.

For example, the processor might receive data from a gauge or flowmeter, compare the data with a predetermined standard, and then produce a signal that operates a relay, valve, or other control mechanism.

This section provides an overview for the sensor I/O Unit and features. For additional information, refer to Chapter 5.

IBM 4982 Sensor Input/Output Unit

The IBM 4982 Sensor Input/Output Unit is a half-width modular unit designed to fit in an EIA (RS-310B) rack. This unit provides a subset of the processor I/O channel for controlling a number of sensor I/O feature cards. The sensor I/O unit contains a power supply, a terminator card, and sockets for eight sensor I/O feature cards. The 4982 attaches to the processor I/O channel by means of the 4982 Sensor Input/Output Unit Attachment Feature card. This card can be plugged into either the processor unit or an I/O expansion unit.

Sensor I/O Features

The following sensor I/O feature cards can be plugged into the 4982 Sensor Input/Output Unit:

Digital Features

- Digital Input/Process Interrupt Non-Isolated (16 points per card)
- Digital Input/Process Interrupt Isolated (16 points per card)
- Digital Output Non-Isolated (16 points per card)

Analog Features

- Analog Input Control (with analog-to-digital converter)
- Amplifier Multirange
- Multiplexer-Reed Relay (8 inputs per card)
- Multiplexer-Solid State (16 inputs per card)
- Analog Output (2 points per card)

Communications Features

The communications features mount in the I/O feature card sockets of the processor or an I/O expansion unit. The following features can be used on switched or non-switched communications lines (except binary synchronous/high speed, which supports nonswitched lines only). Use of switched lines is dependent on line speed and conditioning.

- Asynchronous Communications Single-Line Control (maximum speed 9600 bits per second)
- Binary Synchronous Communications Single-Line Control (maximum speed 9600 bits per second)
- Binary Synchronous Communications Single-Line Control/High Speed (maximum speed 56,000 bits per second)
- Synchronous Data Link Control Single-Line Control (maximum speed 9600 bits per second)
- Asynchronous Communications 8-Line Control (controls for one or two 4-line adapters)
- Asynchronous Communications 4-Line Adapter (maximum speed 2400 bits per second per line)
- Binary Synchronous Communications 8-Line Control (controls for one or two 4-line adapters)
- Binary Synchronous Communications 4-Line Adapter (maximum speed 9600 bits per second)

All data transfers to and from the system are via cycle steal (I/O operations are overlapped with processor operations). The foregoing communication features (except for the binary synchronous/high speed feature) are capable of manual dialing and manual or automatic answering on switched lines. The binary synchronous communications singleline control feature provides the ability to initial program load (IPL) the processor from a remote system. The asynchronous communications single-line control feature and asynchronous communications 4-line adapter feature may be locally attached; that is, no modem required, to appropriate asynchronous terminals using the asynchronous direct connect communications cable feature.

For additional information about the communications features, refer to Chapter 4.

User Attachment Features

A variety of features are provided for the user to attach his own input/output devices and equipment to a Series/1 processor. Both serial and parallel data paths are provided in addition to a multifunction timer. The user attachment features mount in the I/O feature sockets of the processor or an I/O expansion unit. This section describes the following features:

- Timers
- Teletypewriter Adapter
- Customer Direct Program Control
- Integrated Digital Input/Output Non-Isolated

Additional information about the preceding features appears in Chapter 3. Three additional user attachment features are also described in Chapter 3:

- Channel Repower
- Channel Socket Adapter
- Customer Access Panel

Timer Feature

The timer feature card has two separately addressable 16-bit timers. There are four frequency options per timer: 1, 5, 25, and 50 microseconds. If desired, the user can supply his own time base and gating signals through a connector on the card.

Each timer can generate periodic or aperiodic interrupts with, or without, the external gate.

In addition to operating as an interval timer or pulse counter, each timer can operate as a self-contained pulse duration counter with end interrupt.

Teletypewriter Adapter Feature

The teletypewriter adapter feature card provides a way of attaching a serial I/O device. This feature provides a logical subset of the EIA RS232-C interface. The adapter operates in full duplex mode at speeds up to 9600 bits per second. Initial program load is supported by the adapter.

Attachment to a teletypewriter is by a dc current loop (isolated or non-isolated). Two other attachment options are offered: (1) a TTL (transistor-transistor logic) compatible interface and (2) an EIA voltage level interface.

Customer Direct Program Control Adapter Feature

The direct program control adapter feature card supplies a logical subset of the I/O channel architecture. This feature provides a convenient means of attaching I/O devices and subsystems to a 4953 or 4955 Processor. The interface circuits are TTL compatible. The adapter is designed to perform direct program control (DPC) functions only; cycle steal (overlapped) operations cannot be performed. The feature card can be configured to accommodate 4, 8, or 16 I/O device addresses. The adapter allows for interrupt vectoring of 16 interrupt sources.

Integrated Digital Input/Output Non-Isolated Feature

The integrated digital I/O feature card contains:

- Two 16-point groups of non-isolated digital input/process interrupt (DI/PI)
- Two 16-point groups of non-isolated digital output (DO)

Each group of DI/PI and DO have a ready and a sync line for synchronizing their operations with attached devices.

System Support Units

The system support units include the following:

- IBM 4959 Input/Output Expansion Unit
- IBM 4997 Rack Enclosure
- IBM 4999 Battery Backup Unit

The purpose of these units was discussed in the "System Design Overview." Additional information about these units appears in Chapter 5.

Programming Support Overview

The programming support for IBM Series/1 consists of a variety of program products and a set of stand-alone utilities. The stand-alone utilities are furnished as system control programming with each processor; the program products may be purchased separately. This section introduces this support. For a more detailed discussion of each program, refer to Chapter 6, "Programming Support."

Series/1 Realtime Programming System

This program product is the operating system for the Series/1. It controls and manages system resources—storage, processor, and devices. It is a multiprogramming, multitasking, event-driven system that controls environment for both realtime and batch applications. The operating system has four primary components: (1) *supervisor services*, which control such operations as storage allocation and program execution, (2) *data management*, which handles data sets and input/output devices, (3) *utilities*, for installation and maintenance of application programs and data, and (4) *communications*, which directs the transfer of data between programs and remote stations.

Series/1 Program Preparation Subsystem

This program product, which runs under the Realtime Programming System, prepares the application programs that execute under the system. The four components of the Program Preparation Subsystem are:

- The *job stream processor*, which provides a control language for invoking programs and defining program resources
- The *text editor*, used to enter or modify source statements and text data
- The *macro assembler*, which translates assembler source statements into object modules
- The *application builder*, which processes the output of the assembler or a compiler and produces output that is executable under the Realtime Programming System

Series/1 FORTRAN IV

FORTRAN IV consists of two program products: a compiler and object support library, and a Realtime Subroutine Library. The compiler produces code with emphasis on compact storage and performance. The object support library has routines for mathematical calculations, data conversion, error handling, and input/output operations.

The Realtime Subroutine Library offers executive functions, process I/O, system service interface, time-of-day, and date subroutines.

Series/1 Mathematical and Functional Subroutine Library (MFSL)

This program product is a set of subroutines for application programming. It has mathematical, conversion, and error-checking subroutines for use by programs coded in Series/1 FORTRAN IV or assembler language, and service subroutines for assembler language users.

Series/1 PL/I

PL/I consists of two program products: a compiler with a resident library; and a transient library. Series/1 PL/I is aimed at decreasing development time for realtime, scientific or problem-solving, and traditional data processing applications. Its features also make it useful for advanced applications such as transaction processing and data base handling.

Series/1 Base Program Preparation Facilities

This program product comprises three stand-alone programs—a text editor, a macro assembler, and a linkage editor. Each program is loaded individually and executes independently. The text editor is the means of entering source code, the macro assembler converts it to object modules, and the linkage editor combines object modules and converts them to absolute load modules. All input, output, and workspace files reside on disk at locations specified by the programmer.

Series/1 Stand-Alone Utilities

The stand-alone utilities are the system control program for the Series/1. They include such capabilities as diskette and disk initialization, copy, dump, patch, automatic system build, and system verification.

Program Numbers

The following table contains the numbers of the program products and the system control program discussed above.

Program name	Program ordering no.
IBM Series/1 Realtime Programming System	5719-PC1
IBM Series/1 Program Preparation Subsystem	5719-AS1
IBM Series/1 FORTRAN IV	5719-FO1
IBM Series/1 Mathematical and Functional Subroutine Library	5719-LM1
IBM Series/1 PL/I Compiler and Resident Library	5719-PL1
IBM Series/1 PL/I Transient Library	5719-PL3
IBM Series/1 Base Program Preparation Facilities	5719-PA1
IBM Series/1 Stand-Alone Utilities	5719-SC2

Data Security and Integrity

The responsibility for the protection of data and programs from unauthorized or accidental modification, destruction, or disclosure lies with the user. However, the IBM Series/1 has built-in characteristics and optional features to assist the user in achieving a level of protection appropriate to his needs. These characteristics include:

- Parity checking on main storage and data bus of the I/O channel
- Storage protection (4955 Processor only)
- Stand-alone utilities to dump data from disk to diskette for data file backup
- Station address and terminal identification in data communications environments
- Electronic lockout and data protection features for display station
- Block checking on all data transmitted/received on binary synchronous and synchronous data link communications channels
- A battery backup unit to preserve the contents of processor storage during ac power interruptions

Additional guidance and considerations concerning the user's approach to data security may be obtained in several IBM publications such as:

- The Considerations of Data Security in a Computer Environment, G520-2169
- Data Security and Data Privacy Study, G320-1370 through G320-1376

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Chapter 2. Processors and Processor Features

This chapter discusses the characteristics and features of the Series/1 processors. The 4955 and 4953 Processors have the following general characteristics:

- Four priority interrupt levels are offered.
- Basic storage is 16K bytes or 32K bytes (model dependent).
- Processor technology is TTL (transistor-transistor logic), LSI (large scale integration).
- The instruction set includes stacking and linking facilities, multiply and divide, variable field-length operations, and a variety of arithmetic, logical, and branching instructions.
- Supervisor and problem states are implemented using privileged instructions for the supervisor only.
- Basic console is standard, a programmer console is optional.

Each processor is described in the following sections of this chapter. The section on the 4953 will discuss only those features that are different from the 4955. The following table is a comparison of the two processors.

	Comparison of 4953 and 4955 Pro	cessors
Characteristic	4953	4955
Storage size	16-64K bytes	16-128K bytes
Interrupt levels	4	4
Storage cycle time	800 nanoseconds	660 nanoseconds
Instruction execution		
time (weighted)	11.8 microseconds	3.9 microseconds
I/O channel		
Burst mode speed	1.33M bytes/second	1.66M bytes/second
(average)		
Capacity	256 device addresses	256 device addresses
I/O feature locations		
Model A	4*	8
Model B	13*	3
Model C	4*	10
Model D	13*	7
Packaging		
Full rack-width	Models B & D	All models
Half rack-width	Models A & C	(not available)
Basic console	All models	All models
Programmer console	Optional feature	Optional feature
Floating point	(not available)	Optional feature
Storage protection	(not available)	All models

*The number of I/O feature locations available, on any model of the 4953, is reduced by one for each storage increment installed after the basic storage.

4955 Processor Description

The basic 4955 processor unit includes the processor, 16K or 32K bytes of storage, a power supply, and a basic console. Figure 2-1 shows a block diagram of a typical system using the 4955.

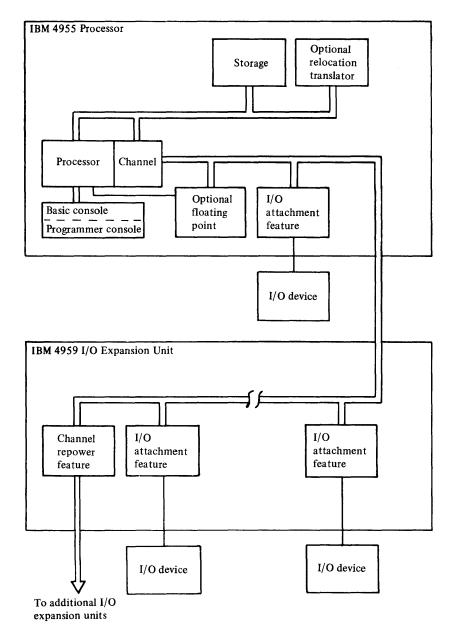


Figure 2-1. Block diagram of an IBM 4955 Processor and an IBM 4959 Input/Output Expansion Unit

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Physical Description

The 4955 is designed to fit in an EIA (RS-310B) rack; it is available in four models (see Figures 2-2 and 2-3). All models are full-width modular units.

- *Model A*. This model has the capacity for 16K through 64K bytes of storage, in 16K-byte increments. There are eight I/O feature locations.
- Model B. This model has the capacity for 16K through 128K bytes of storage, in 16K-byte increments. The storage address relocation translator feature is required when storage capacity exceeds 64K bytes. There are three I/O feature locations.
- *Model C*. This model has the capacity for 32K through 64K bytes of storage, in 32K-byte increments (a maximum of one 16K-byte storage card may be included). There are ten I/O feature locations.
- Model D. This model has the capacity for 32K through 128K bytes of storage, in 32K-byte increments (a maximum of one 16K-byte storage card may be included). The storage address relocation translator feature is required when storage capacity exceeds 64K bytes. There are seven I/O feature locations.

The number of I/O feature locations available, on any model of the 4955, is reduced by one when the floating point feature is installed.

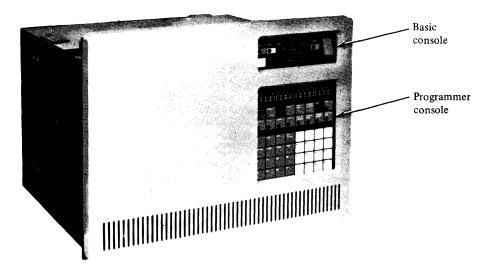
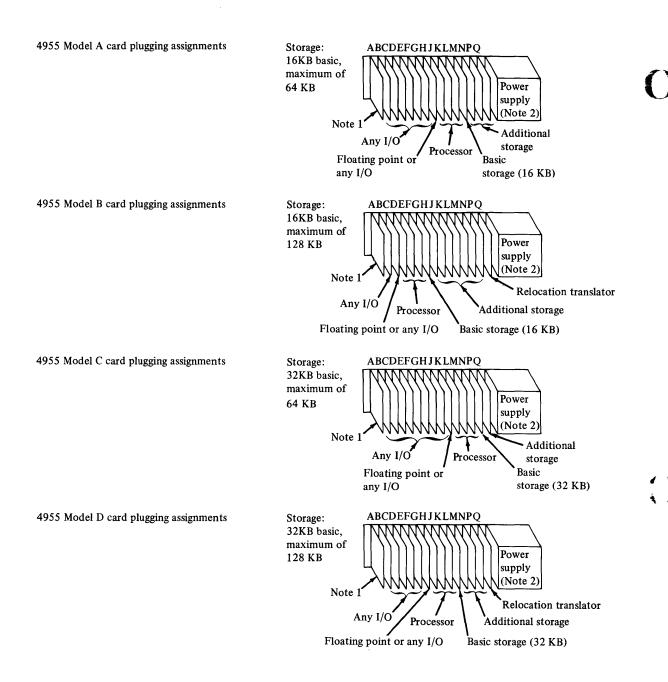


Figure 2-2. IBM 4955 Processor



Note 1. The A position for all models is reserved for the I/O cables or (due to voltage limitations) one of the following I/O feature cards:

- Teletypewriter adapter feature using TTL voltage levels
- Teletypewriter adapter feature using isolated current loop where customer supplies external ±12V power
- Timer feature
- Customer direct program control adapter feature
- 4982 sensor input/output unit attachment feature
- Integrated digital input/output non-isolated feature
- Channel repower feature

Note 2. The communications power feature provides ± 12 volts and is a prerequisite for the following I/O feature cards:

- All communications features
- Teletypewriter adapter feature using the non-isolated current loop
- Teletypewriter adapter feature using the EIA voltage level interface

Figure 2-3. IBM 4955 Processor card plugging assignments

Design Features

Instruction Set and Execution Times

Appendix A contains a list, by instruction type, of the 4955 instruction set and execution times.

The instruction set for the processor is rich in function with a full complement of bit, byte, 16-bit word, and 32-bit double word operations. The architecture is general purpose and is designed to support realtime, interactive applications.

There are over 160 instructions in the *basic* set. These instructions are generally classified as to their method of operation or function performed. Each classification with an example is listed below.

- Shifts
 - Shift Left Circular Double
- Register-to-register
 - Move Word
- Parametric
 - Supervisor Call
- Register immediate
 - Reset Bits Word Immediate
- Branching
 - Jump on Condition
 - Branch on Condition
 - Single bit manipulation
 - Test Bit
- Register to storage (short and long)
 - Add Byte
 - Operate I/O
- Multiple register to storage
 - Store Multiple
- System register to storage (privileged)
 - Set Level Status Block
- Variable field length byte operations
 - Fill Byte Field and Increment
- Storage immediate
 - Subtract Word Immediate
- Storage to storage
 - Move Doubleword
- System register to register (privileged)
 - Copy Current Level

There are seven different addressing modes, including single indirect and double displacement indirect addressing. Any one instruction type may permit up to four address modes.

All storage addressing is defined by byte (eight data bits plus one parity bit) location. Instructions can refer to bits, bytes, words (two bytes), double words (four bytes), or fields as data types.

Storage Size and Speed

Depending upon the model and the amount of storage installed, the 4955 can contain 16K through 128K bytes of storage. The storage cycle time is 660 nanoseconds.

Addressing Scheme

Each byte location in main storage is directly addressable. Byte locations in storage are numbered consecutively, starting with location zero; each number is considered to be the address of the corresponding byte. Storage addresses are 16-bit unsigned binary numbers. This permits a direct addressing range of 65,536 bytes.

When the storage address relocation translator is installed, the 16-bit address is used as a logical address to generate a 24-bit physical address, allowing addressing beyond 65,536 bytes.

Interrupt Structure

The 4955 has four priority interrupt levels with independent registers and status indicators for each level. Level switching can occur in two ways: (1) automatically upon acceptance of an I/O interrupt request from an I/O device or (2) by program control. The interrupt mechanism provides 256 vectored entry points for I/O devices.

The following is a more detailed description of the interrupt structure.

Priority Interrupts. The processor provides four priority interrupt levels. Associated with each level is a bank of hardware registers and status information consisting of eight general registers (16 bits each), an instruction address register, an address key register (for storage protection), and a level status register that includes a set of result indicators.

When switching between levels occurs, the information contained in the interruptedfrom level is automatically preserved by hardware; thus it is not necessary to store the status indicators and general purpose registers in main storage. Automatic vectoring to the service routine for a given device is accomplished by the eight-bit device addresses; thus 256 direct interrupt entry points are provided.

No software polling of devices is required to accept the interrupt or identify the device. Assignment of a given device to an interrupt level is under program control (by masking) and can be dynamically reassigned. Acceptance of priority interrupts by the processor is under program control on the basis of all four levels, one or more individual levels, or one or more individual devices.

Class Interrupts. A special category of interrupts known as *class* interrupts is provided in the processor. This is a means of alerting the system to the occurrence of certain classes of errors or exception conditions. Class interrupts may occur on any of the four priority interrupt levels; the class interrupts preempt operation of the system on any of the priority levels until the *class* interrupt condition has been reset. The seven types of class interrupts are: machine check, program check, power/thermal warning, supervisor call, soft exception trap, trace, and console. Only the power/thermal warning and the console class interrupts can be disabled under program control. Identification and status information about the exception or error is provided. This information may make it possible for the software to recover in a manner that allows normal processing to continue with minimum disruption.

The trace class interrupt provides an instruction trace mechanism to ease software debugging. Instruction tracing may occur on any priority interrupt level. When trace is turned on, a unique class interrupt occurs prior to each instruction. Upon exit from the trace routine, the next instruction is executed and the process repeats until the trace is turned off.

Registers

The registers in the 4955 can be divided into two categories:

- Per-level register (the register is duplicated for each processor priority interrupt level)
- Per-system register (the register is provided only once and is used by all processor priority interrupt levels)

Information that must be saved when a level is preempted is kept in registers supplied for a specific level. Information that is common to all levels or pertains only to the current operating state is kept in registers common to all levels. The registers in each category are listed below.

Registers Supplied on a Per-Level Basis.

- General registers (8 per level)
- Instruction address register
- Level status register
- Address key register (used for storage protection)
- Floating point registers (with the floating point feature)

Registers Supplied on a Per-System Basis.

- Current instruction address register
- Mask register (interrupt levels)
- Processor status word
- Console data buffer (with programmer console feature)
- Segmentation registers (with the storage address relocation translator feature)

Control of I/O

The I/O devices are attached to the processor through the processor I/O channel. The I/O channel (a defined information format and signal sequence common to I/O devices) accommodates a maximum of 256 I/O device addresses. Four priority interrupt levels can be used to facilitate device service.

The processor I/O channel directs the flow of information between I/O devices and main storage. It contains the facilities for control of the I/O operations.

The I/O channel is an asynchronous, multidropped channel that links the processor to its external resources. It consists of address, control, and data lines. Device service through the processor I/O channel can occur as a cycle steal or a direct program control (DPC) operation. Brief descriptions of the cycle steal and DPC operations follow.

Cycle Steal. Each operate I/O instruction can initiate multiple data transfers (maximum of 65,535 bytes per control block). I/O operations are overlapped with processing operations. The device must be able to operate in the cycle steal mode and always interrupts upon normal termination of a cycle steal operation.

Direct Program Control. An immediate data transfer is made to, or from, the device for each Operate I/O instruction. The data can consist of one byte or one word (two bytes). The operation may or may not terminate with an interrupt.

Processor I/O Channel Capability

The maximum burst data rate of the processor I/O channel is 800K words (1.6 megabytes) per second. When multiple cycle stealing devices are interleaved, the aggregate data rate is also 800K words per second.

Storage Protection

A storage protection mechanism is provided as a basic part of the 4955. It protects against (1) access (reading and writing) to defined blocks of storage by the software or by the hardware during an I/O operation and (2) writing in an undesired location within a defined block by the software. This protection is accomplished by comparing a storage key associated with a storage block against an address key associated with the current operation. A read-only bit is associated with each storage key. If the storage address relocation translator is enabled, storage protection is controlled by the relocation feature.

Stacking

The processor provides two special types of stacking facilities. There is no restriction (except storage size) on the number of stacks the programmer can define.

Data Stacking. This facility provides an efficient and simply way to handle last-in/first-out queues of data items and/or parameters in main storage. The data items, or parameters are stack elements. For a given queue, or stack, each element is one, two, or four bytes wide. Instructions for each element size (byte, word, or doubleword) are provided to:

- Push an element into a stack (register to storage)
- Pop an element from a stack (storage to register)

Linkage Stacking. This facility provides an easy method for linking subroutines to a calling program. A stack, one-word wide, is used for saving and restoring the status of general registers and for allocating dynamic work areas. The Store Multiple instruction stores the contents of the registers into the stack and reserves a designated number of bytes in the stack as work area. The Load Multiple and Branch instruction reloads the registers, releases the stack element, and causes a branch back to the calling program.

Basic Console

A basic console is standard in each processor unit (see Figure 2-4). It is intended for dedicated systems that are basically used in an unattended environment. Only minimum controls and indicators are provided. These are: a Load key; switches for Power On/Off, IPL Source, and Mode; and indicators for Load, Wait, Run, and Power On.

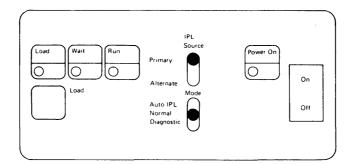


Figure 2-4. Basic console

The 4955 has many optional features. Only those features directly related to the processor are discussed here. The user attachment features are discussed in Chapter 3 and the communications features are discussed in Chapter 4. Refer to Appendix B for a listing of the significant features for Series/1.

Floating Point

The floating point feature is an optional high speed arithmetic unit for the 4955. Four 64-bit floating point registers are provided for each of the four priority interrupt levels. Normalized numbers, contained in these registers, are floating point normalized in sign magnitude form. Signed binary integers can be loaded from main storage into the registers with automatic conversion to floating point, or floating point numbers can be loaded directly. Arithmetic operations can be performed between two registers or between main storage and one register (data in main storage must be in floating point format). The floating point registers can be stored in main storage as floating point numbers or converted to signed binary integers and stored in main storage.

The floating point format is identical with the IBM System 360/370, System/7, and System/3 format (see Figure 2-5). The instructions include addition, subtraction, multiplication, division, compare, load, store, and integer conversion.

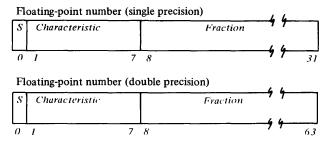


Figure 2-5. Floating point format

Storage Address Relocation Translator

The storage address relocation translator feature is an optional feature for the IBM 4955 Processor Models B and D only. The feature permits addressing of main storage locations beyond 64K bytes. Therefore, the feature is required only when main storage is larger than 64K bytes.

Programmer Console

This feature is intended for operator-oriented systems where programs are being tested or various programs will be entered and executed during the day. This type of environment requires a more versatile console to (1) determine program and machine problems, and (2) to manually alter data and programs in storage. The following indicators and controls are provided: Check and Data Display indicators; Level, Stop, Stop on Address, Instruction Step, Check Restart, and Stop on Error key/indicators; Reset, Store, Data Buffer, Console Interrupt, and Start keys (see Figure 2-6).

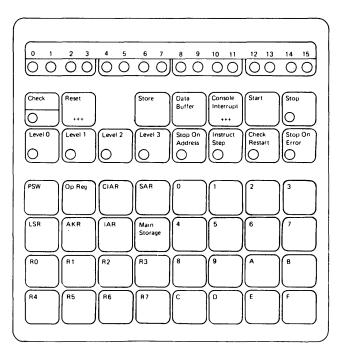


Figure 2-6. Programmer console

4953 Processor Description

The basic 4953 processor unit includes the processor, 16K or 32K bytes of storage, a power supply, and a basic console. Figure 2-7 shows a block diagram of a typical system using the 4953.

The following items are identical for both the basic 4955 and 4953; see the appropriate 4955 sections for these descriptions:

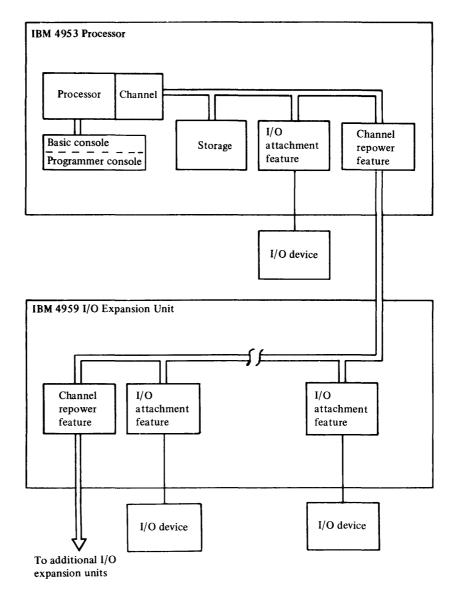
- Addressing scheme
- Interrupt structure
- Registers (except address key register and floating point registers)
- Control of I/O
- Stacking
- Basic console
- Programmer console

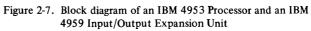
The following items differ between the 4955 and 4953:

- Instruction execution speed
- Storage size and speed
- Processor I/O channel capability

The following items are not available on the 4953:

- Floating point feature
- Storage protection
- Storage address relocation translator feature



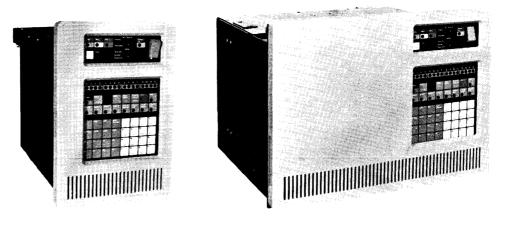


Physical Description

The 4953 is designed to fit in an EIA (RS-310B) rack; it is available in four models (see Figures 2-8 and 2-9). Two models are full-width modular units and two models are half-width modular units. The half-width units are mounted using a rack mounting fixture.

- Model A. This model is a half-width modular unit and has 16K bytes of storage. It has the capacity for 16K through 64K bytes of storage, in 16K byte increments. There are four I/O feature locations, three of which can be used for storage additions.
- Model B. This model is a full-width modular unit and has 16K bytes of storage. It has the capacity for 16K through 64K bytes of storage, in 16K byte increments. There are thirteen I/O feature locations, three of which can be used for storage additions.
- *Model C.* This model is a half-width modular unit and has 32K bytes of storage. It has the capacity for 32K through 64K bytes of storage, in either 16K or 32K byte increments. There are four I/O feature locations, two of which can be used for storage additions.
- Model D. This model is a full-width modular unit and has 32K bytes of storage. It has the capacity for 32K through 64K bytes of storage, in either 16K or 32K byte increments. There are thirteen I/O feature locations, two of which can be used for storage additions.

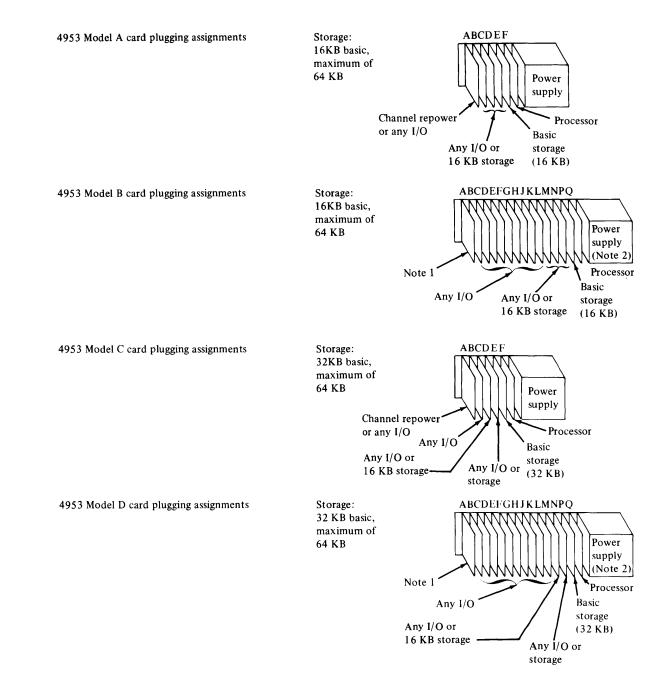
The number of I/O feature locations available, on any model of the 4953, is reduced by one for each storage increment installed after the basic storage. The number of I/O feature locations is also reduced by one when the I/O expansion unit is added because the channel repower feature is a prerequisite for adding the I/O expansion unit to the 4953.



Models A and C

Models B and D

Figure 2-8. IBM 4953 Processor Models A, B, C, and D



Note 1. On Models B and D, only the following feature cards may be plugged into the A position due to voltage limitations:

- Teletypewriter adapter feature using TTL voltage levels
- Teletypewriter adapter feature using isolated current loop where user supplies external ±12V power
- Timer feature
- Customer direct program control adapter feature
- 4982 sensor input/output unit attachment feature
- Integrated digital input/output non-isolated feature
- Channel repower feature

Note 2. On Models B and D, the communications power feature provides ±12 volts and is a prerequisite for the following I/O feature cards:

- All communications features
- Teletypewriter adapter feature using the non-isolated current loop
- Teletypewriter adapter feature using the EIA voltage level interface

On Models A and C ± 12 volts is standard.

Figure 2-9. IBM 4953 Processor card plugging assignments

Design Features

Instruction Set and Execution Times

Appendix A contains a list, by instruction type, of the 4953 instruction set and execution times.

The 4953 instruction set is compatible with the 4955 basic instruction set. However, no instructions are available for storage protection, floating point, or storage address relocation.

Storage Size and Speed

The 4953 can contain 16K through 64K bytes of storage. The storage cycle time is 800 nanoseconds.

Processor I/O Channel Capability

The maximum burst data rate of the processor I/O channel is 666K words (1.33 megabytes if transmitted in pairs) per second. When multiple cycle-stealing devices are interleaved, the aggregate data rate is also 666K words per second.

4953 Processor Features

The 4953 has several optional features. Only those features directly related to the processor are discussed here. The user attachment features are discussed in Chapter 3; the communications features are discussed in Chapter 4. Refer to Appendix B for a listing of the significant features for Series/1.

Programmer Console

The programmer console feature is identical to that on the 4955 except that the address key register is not available on the 4953 and cannot be displayed or altered. The programmer console was described earlier in this publication (see Figure 2-6).

The user attachment features permit the customer to attach his own I/O devices and instruments to an IBM 4953 or 4955 Processor. This chapter describes the following features:

- Timers
- Teletypewriter Adapter
- Customer Direct Program Control Adapter
- Integrated Digital Input/Output Non-Isolated
- Customer Access Panel
- Channel Repower
- Channel Socket Adapter

Timers

The timer feature provides two 16-bit timers. Each timer can be used as an interval timer, pulse counter, or pulse duration counter with end-interrupt. The timers are packaged on one printed circuit card that plugs into either the processor or an I/O expansion unit.

The timer feature can be used with external signals. Each timer has two output lines "run state" and "external gate enable" and two input lines "customer clock" and "external gate". These signal lines are TTL compatible.

The two timers are separately addressable and are started, stopped, read, or set to any value independently under program control. The timers can be read without disturbing their operation; however, to set the timer's value or mode, it must be stopped.

Each timer has a mode register that is used to select one of four internal time bases or an external time base. The timer value is decremented with the selected time base. The internal time bases are 1, 5, 25, and 50 microseconds. The external time base is provided by the user and must be equal to or greater than 20 microseconds when the input is filtered, 1 microsecond when not filtered. An optional filtering capability that can be selected with jumper wires is built into the timer card. An "external gate enable bit" is also contained in the mode register. The time base and external gate enable are program selectable.

The following program selectable running modes are available for each timer:

• Periodic interrupts-internal.

A 16-bit auto-load register is set to any value by program control. This register automatically reloads the timer when the timer underflows, and an interrupt is generated. This provides the capability of generating periodic interrupts on 65,536 possible base values of the timer without program intervention.

- Aperiodic interrupts-internal. The timer is loaded with a value under program control, and an interrupt occurs when the timer underflows. After the first interrupt, the timer is *not* reloaded from the auto-load register and, therefore, counts the full 65,536 counts before the next interrupt occurs unless a new value is loaded under program control.
- Periodic or aperiodic interrupts-external. The timer generates periodic or aperiodic interrupts, but the start and stop of the timer is controlled by the external gate when the timer is in the run state.

Teletypewriter Adapter

The teletypewriter adapter feature provides a way of attaching a serial I/O device to the Series/1. This feature provides a logical subset of the EIA RS232-C interface. The adapter was designed primarily to attach a teletypewriter I/O device such as a Teletype* model ASR 33, ASR 35, or KSR 33. The adapter may also be used to attach other devices that satisfy the interface requirements.

The following is a partial list of different types of devices commercially available that can be attached to this interface.

- Printer-keyboards
- Keyboard-display units
- Keyboard-display-printer units
- Printers
- Tape cassettes
- Tape units
- Card readers
- Badge readers
- Plotters

To attach a serial I/O device to the adapter, the following interface types can be selected:

- Non-isolated current loop
- Isolated current loop
- EIA voltage level interface
- TTL voltage level interface

The "mark" and "space" signal-level convention can also be selected. The teletypewriter adapter uses a four-wire interface for data exchange—two for receive and two for transmit. Operation is full duplex; that is, data can be transmitted and received concurrently.

Data bytes are transmitted across the adapter/device interface serially by bit with the least significant bit being transmitted first. An 11-bit start/stop frame is used for synchronization of each byte. The bit rate is selectable on the feature card with jumper wires. The following bit rates are available:

Bits per second

The teletypewriter adapter feature is code transparent and all 256 binary combinations can be transmitted and received. The data exchange over the interface is not checked for parity or device-dependent control characters. The adapter can be configured to perform initial program load (IPL).

Data transfer between the adapter and the processor is by byte using direct program control (DPC) commands; however, during IPL the transfer is by byte using cycle steal.

^{*}Registered trademark of Teletype Corporation

Diagnostic capability is designed into the teletypewriter adapter feature. A special command places the adapter in diagnostic-wrap state. A subsequent write command sends data to the device and to the receive data register. The adapter then presents an interrupt so that a read command can be issued to verify that the correct data is sent back to processor storage.

The communications power feature furnishes ± 12 volts and *is* a prerequisite for the teletypewriter adapter feature *if* the attached device is connected to either the non-isolated current loop interface or the EIA voltage level interface. An exception to this is when the teletypewriter adapter is plugged into the 4953 Processor Models A or C, where ± 12 volts is standard.

The communications power feature is *not* a prerequisite for the teletypewriter adapter *if* the attached device is connected to either the isolated current loop interface or the TTL voltage level interface. When the attached device is connected to the isolated current loop interface, the user must supply power to drive the transmit and receive loops. When the attached device is connected to the TTL interface, normal logic levels present on the teletypewriter adapter card are used to drive the transmit and receive loops.

Customer Direct Program Control Adapter

The customer direct program control (DPC) adapter feature card provides a convenient means of attaching customer equipment to the processor I/O channel. However, to facilitate attachment of various devices to the adapter interface, additional hardware is required; the DPC adapter provides no functional capability in a stand-alone configuration. The DPC adapter can be used for attachment of: typical digital instruments, another computer, typical data processing I/O equipment (such as low speed readers, punches, or plotters), or typical commercial data acquisition systems.

The customer DPC adapter feature provides the user with a subset of the processor I/O channel. The interface adheres to the processor I/O channel architecture with an additional throughput delay of approximately 2.5 microseconds.

The DPC adapter feature is designed to perform direct program control functions only and can be configured to accommodate four (4), eight (8), or sixteen (16) I/O device addresses. It therefore, allows for interrupt vectoring for up to 16 interrupting sources. All the devices attached to the DPC adapter share a common interrupt level. The adapter has 75 lines including 18 data bus out (2 parity bits), 18 data bus in (2 parity bits), 16 interrupt request in lines (when configured for 16 I/O device addresses), 3 function bits, 4 modifier bits, 4 I/O device address bits, and 12 control and response lines. The data flow is always 16 bits without the parity option or 18 bits (including 2 parity bits) with the parity option.

Diagnostic capability is designed into the DPC adapter feature card. This capability allows the user to send data or control information from the processor and "wrap" the same information back to the processor from either the adapter card or from an external I/O device.

The DPC adapter feature uses TTL non-isolated cable drivers with a current capacity of 175 mA. This allows a wide range of customer termination schemes.

Integrated Digital Input/Output Non-Isolated

The integrated digital input/output non-isolated feature allows the user to add small amounts of digital sensor I/O equipment when the 4982 Sensor Input/Output Unit is not required. The integrated digital I/O feature can also be used for attachment of simple OEM (original equipment manufacturers') devices.

The integrated digital I/O feature contains 32 points (two 16-point groups) of nonisolated digital input/process interrupt (DI/PI) and 32 points (two 16-point groups) of digital output (DO). Each group of 16 points is separately addressable and has a ready and sync line for synchronizing its operation with attached devices. The external sync capability is enabled by program control.

	The DI/PI groups have two 16-position registers, one DI register for reading unlatched data and one PI register for reading latched data. Each position of the DI register follows the state of the corresponding user-input point until the register is read. Each position of the PI register records with a 1-bit, the first 0-bit to 1-bit transition on the corresponding user-input point. When a bit in the PI register becomes active, a process interrupt is generated if PI mode was previously armed by program control. The DI/PI points provide voltage sensing to ± 24 volts dc. Each DO group has a 16-position register. Data is stored in this register under program control. The DO points correspond to the positions of the register. With a user-supplied voltage, each point is rated at a maximum of +52.8 volts dc and 100 milliamps. Without a user-supplied voltage, each point supplies a TTL compatible output voltage. Diagnostic capability is designed into the integrated digital I/O feature. DI/PI groups can be tested with diagnostic commands that disable the user's input lines and force the input data to either 0-bits or 1-bits. Read commands can then be issued to verify that the correct data is sent back to processor storage. DO groups can be tested in a similar manner. A diagnostic command disables the output lines. A special read DO command allows the program to verify data previously sent to the DO group with a write command.	(
Customer Access Panel		
	The customer access panel feature provides an assembly for mounting optional, quick- disconnect type connectors for I/O equipment. The assembly can accommodate one timer connector, one teletypewriter connector, and up to four connectors for either the integrated digital input/output feature, or the customer direct program control feature. The assembly mounts to the standard rack mounting screw holes at the rear of the enclosure frame. The assembly can be mounted behind any blank panel that is at least 133.4 mm (5.25 in.) high. The assembly cannot be mounted behind the 4962 Disk Storage Unit.	1
Channel Repower		(
	The channel repower feature repowers and isolates the I/O channel along a chain of I/O expansion units. The feature is required on all models of the 4953 Processor when a 4959 I/O Expansion Unit is attached. The feature is also required in all 4959 I/O Expansion Units when another 4959 I/O Expansion Unit follows in the chain. The channel repower feature is required in all processor units if a 4999 Battery Backup Unit is installed and there are one or more 4959 I/O Expansion Units attached to the system. In this case, the isolation capability, as well as repowering, is needed. The channel repower feature can also be used for cabling out to a user's attachment or unit. When used for this purpose, the repower feature must be the last series element directly plugged into the I/O channel. (This last series element could be in the processor or an I/O expansion unit depending on the system configuration.)	
Channel Socket Adapter		
•	The channel socket adapter feature consists of an IBM printed circuit card that plugs into the backpanel of the IBM 4953 or 4955 Processor or 4959 I/O Expansion Unit. On the top edge of the IBM printed circuit card is an industry standard connector that accepts the user-provided I/O adapter card. To power the user's circuits, +5 volts dc at 3 amperes is available at the connector.	
	Note. The channel socket adapter feature is described in the <i>IBM Series/1 User's Attach-</i> ment Manual, GA34-0033. The adapter translates the 1 mm (0.040 in.) IBM backpanel socket to a 1.5 mm (0.060 in.) commercially available connector for printed circuit cards that have tabs on 4 mm (0.156 in.) centers. The channel socket adapter is oriented primarily to the end-user who has design and build capability.	(

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Chapter 4. Communications Features

This chapter discusses the communications features available on the Series/1. These features provide a variety of communications options. There are several single-line and multiple-line telecommunications capabilities. In addition, there are various combinations of line speeds, line configurations, clocking sources, and data codes to choose from. All of the communications features transfer data to and from the processor in cycle-steal mode.

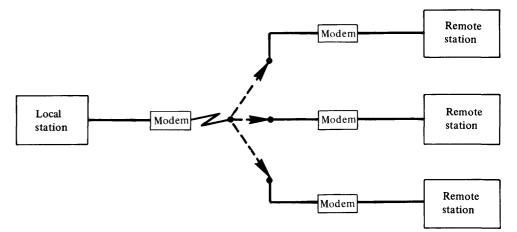
Communications lines can operate in one of three different types of data links:

- Point-to-point non-switched
- Point-to-point switched
- Multipoint

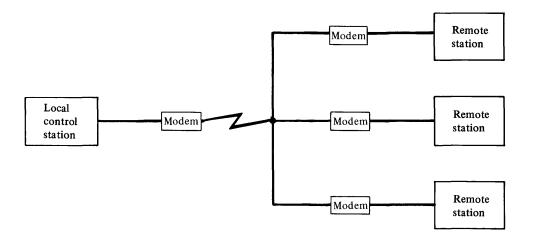
A communications link connecting a single local station and a single remote station, in a non-switchable connection, is a point-to-point non-switched data link.



A communications link that has one local station that can be switched to any one of several remote stations is a point-to-point switched data link.



The control (local) station in a multi-point data link is physically connected to all remote stations. The control station can communicate via a poll routine using a unique remote station address. Only the addressed station can respond to the poll at one time.



The communications features are discussed by category:

- Synchronous features
- Binary synchronous features
- Asynchronous features
- Communications support features

Synchronous Features

Synchronous Data Link Control (SDLC) Single-Line Control

The SDLC single-line control feature is a medium-speed option that allows the Series/1 to communicate with remote terminals and host systems via a modem and a communications line facility.

This feature provides the control circuitry for a single half-duplex communication line at data rates up to 9,600 BPS (bits per second), on a switched or non-switched basis.

Data transmission is serial-by-bit, using the synchronous data link method of character and bit transmission. Communications can be established with devices using any ASCII, EBCDIC, or compatible 8-bit code.

The following communication attributes are applicable:

- Point-to-point non-switched
- Point-to-point switched
- Multipoint
- Primary station
- Secondary station
- Manual call/answer
- IPL (not applicable)
- Business machine clocking
- Modem clocking
- Error recovery facilities

Binary Synchronous Features

Binary Synchronous Communications (BSC) Single-Line Control (Medium Speed)

The BSC single-line control feature is a medium speed option that allows the Series/1 to communicate with remote terminals and host systems via a modem and a communications line facility.

This feature provides the control circuitry for a single half-duplex communication line at data rates up to 9,600 BPS on a switched or non-switched basis.

Data transmission is serial-by-bit, using the binary synchronous communication method of character and bit transmission. ASCII and EBCDIC transmission codes can be used. Transparency is available when using EBCDIC code.

The following communication attributes are applicable:

- Point-to-point non-switched
- Point-to-point switched
- Multipoint
- Primary station
- Secondary station
- Manual call/answer
- IPL (host initiated)
- Business machine clocking
- Modem clocking
- Error recovery facilities

Binary Synchronous Communications (BSC) Single-Line Control/High Speed

The BSC single-line control/high speed feature is an option that allows the Series/1 to communicate with remote terminals and host systems via a modem and a communication line facility.

This feature provides the control circuitry for a single half-duplex communications line at data rates up to 56,000 BPS on a non-switched basis only.

Data transmission is serial-by-bit, using the binary synchronous communications method of character and bit transmission.

The following communication attributes are applicable:

- Point-to-point non-switched
- Primary station
- Secondary station
- IPL (host initiated)
- Modem clocking
- Error recovery facilities

Binary Synchronous Communications 4-Line Adapter

This feature provides the circuitry necessary to accommodate up to four half-duplex communication lines. Data rates are dependent on the number of lines and various line speeds used.

This device requires the BSC 8-line control feature to provide control circuitry. (When eight lines are required, two BSC 4-line adapters are required.) The BSC 8-line control feature is described in the next section of this chapter.

The multiple-line data rates are as follows: up to 9,600 BPS on lines 1 and 2; and up to 2,400 BPS on lines 3 through 8 when two 4-line adapters are used. When a single 4-line adapter is used, the data rates for each line can be up to 4,800 BPS.

Binary Synchronous Communications 8-Line Control

This feature provides the control circuitry for up to two BSC 4-line adapters. Data rates are 9,600 BPS for lines 1 and 2 and up to 2,400 BPS on lines 3 through 8 when two BSC 4-line adapters are used. When a single 4-line adapter is used, the data rates for each line can be up to 4,800 BPS. Data transfer to and from the processor is via cycle-steal mode.

The communication attributes of the BSC 8-line control feature are the same as discussed in the previous section, "BSC Single-Line Control," except that IPL cannot be performed.

Asynchronous Features

Asynchronous Communications Single-Line Control (ACC)

The ACC single-line control feature is a medium-speed option that allows the Series/1 to communicate with remote terminals and host systems via a modem and a communications line facility.

This feature provides the control circuitry for a single half-duplex communications line at data rates up to 9,600 BPS on a switched or non-switched basis.

Data transmission is serial-by-bit, using the asynchronous communications start/stop method of character and bit transmission. Applicable transmission codes include: PTTC/ EBCD, PTTC/Correspondence, and Eight Bit Data Interchange.

The following communication attributes are applicable:

- Point-to-point non-switched
- Point-to-point switched
- Multipoint*
- Primary station
- Secondary station*
- IPL (not applicable)
- Business machine clocking
- No modem clocking
- Error recovery facilities

*This feature does not provide for recognition of station addresses. If the feature is to be used as a secondary station in a multi-point network, station address recognition must be provided by programming.

Asynchronous Communications 4-Line Adapter Feature

This feature provides the circuitry necessary to accommodate up to four half-duplex communications lines. Each of these lines can operate at data rates up to 2,400 BPS.

This device requires the ACC 8-line control feature to provide control circuitry. (When eight lines are used, two ACC 4-line adapters are required.)

The ACC 8-line control feature is described in the next section of this chapter.

Asynchronous Communications 8-Line Control Feature

This feature provides the control circuitry for up to two asynchronous communications 4-line adapter features.

The communication attributes of the ACC 8-line control feature are the same as discussed in the previous section, "ACC Single-Line Control."

The communications indicator panel is available as an option to the communications features. This panel provides visual display of the various states and conditions of a single selectable communication line, as well as providing a means of manually controlling certain modem functions.

This panel attaches to any single or multi-line control by a connector on that feature. Line selection and information to be displayed are selected by manipulation of the eight panel switches. The eight lights on the panel can display coded status information and modem control line settings such as: data set ready, clear to send, transmit, and receive data.

This unit mounts under the front cover of the 4953 Processor, the 4955 Processor, or the 4959 I/O Expansion Unit. (The panel cannot be mounted on Models A or C of the 4953 Processor.)

Communications Power

This feature provides the additional ± 12 -volt regulated power required for attachment of one or more communications feature cards. The communications power feature is not required on 4953 Models A and C (± 12 volts is standard on these models).

The communications power feature is required for some applications of the teletypewriter adapter feature. See "Teletypewriter Adapter" in Chapter 3.

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Chapter 5. I/O and System Support Units

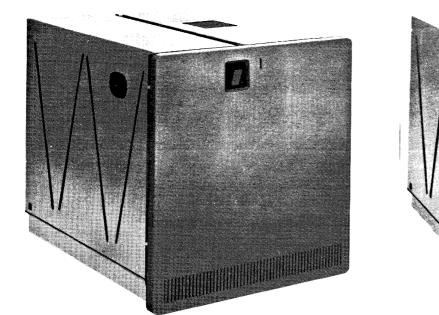
This chapter describes, in more detail, the Series/1 I/O units and system support units. The following units are discussed:

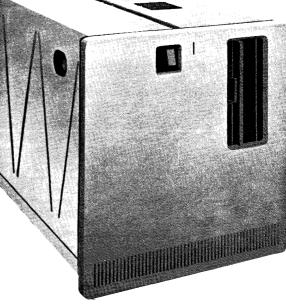
- IBM 4962 Disk Storage Unit
- IBM 4964 Diskette Unit
- IBM 4973 Printer
- IBM 4974 Printer
- IBM 4979 Display Station
- IBM 4982 Sensor Input/Output Unit
- IBM 4959 Input/Output Expansion Unit
- IBM 4997 Rack Enclosure
- IBM 4999 Battery Backup Unit

IBM 4962 Disk Storage Unit

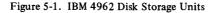
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The IBM 4962 Disk Storage Unit is a direct access storage device. This unit is available in four models (Figure 5-1). Models 1, 1F, 2, and 2F have a fixed disk with 9,308,160 bytes of storage accessed by two movable heads. Models 1F and 2F have an additional 122,880 bytes on the same disk, but accessed by eight fixed heads. Combination disk/diskette models have fixed-disk storage as previously described plus 606,208 bytes (maximum) on a removable diskette.





4962 Models 1,1F



4962 Models 2, 2F-

O

Models

The four different models of the 4962 Disk Storage Unit are summarized in the following table.

Storage Capacity of 4962 Models (in bytes)			
4962 model	Fixed disk storage movable heads	Fixed heads	Diskette storage (maximum)
1	9,308,160		
1F	9,308,160	122,880	
2	9,308,160		606,208
2F	9,308,160	122,880	606,208

All models of the 4962 require the 4962 Disk Attachment Feature for attachment to the Series/1. The 4962 Models 2 and 2F include a diskette drive identical in function to the 4964 Diskette Unit. Therefore; 4962 Models 2 and 2F require two attachment features: (1) the 4962 Disk Attachment Feature and (2) the 4964 Diskette Attachment Feature.

Design Features

The 4962 Disk Storage Unit is a completely self-contained modular unit. It is designed to mount in the full width of an EIA (RS-310B) rack.

Fixed Disk

As shown in Figure 5-2, two read/write data heads are used to record or retrieve information from concentric data bands on the single, fixed disk. A servo head, used for data clocking and seek controls, is mounted with the read/write heads on the actuator assembly that moves the heads to a specified track location. The data tracks accessed by heads 0 and 1 are located on one surface of the disk; the servo tracks are located on the opposite surface. On Models 1F and 2F, the servo track surface of the disk also contains eight data tracks that are accessed by fixed read/write heads. Data, or programs, requiring fast access should be placed in this area.

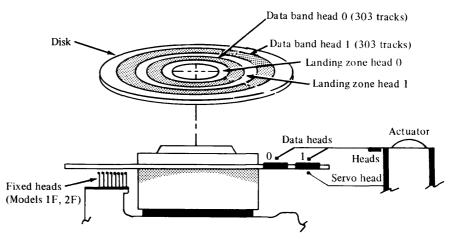


Figure 5-2. Disk and access mechanism

Diskette

Except for the external physical characteristics, the diskette unit in the 4962 Models 2 and 2F is identical to the 4964 Diskette Unit. This unit is described in a subsequent part of this chapter.

Operating Characteristics

Fixed Disk Specifications

The 4962 Disk Storage Unit provides a Series/1 processor with substantial data storage capacity on its fixed disk. The specifications of the fixed disk drive (all models) are as follows:

Factor	Magnitude	Unit
Rotational speed	2964	RPM (nominal)
Rotation time	20.2	milliseconds
Average rotational delay or latency	10.1	milliseconds
Capacity (movable heads)		(nominal)
Bytes/sector	256	bytes
Sectors/track	60	sectors
Tracks/cylinder		
Models 1, 1F, 2, 2F	2	tracks
Cylinders/disk (Note 1)	303	cylinders
Total disk capacity		
Models 1, 1F, 2, & 2F	9,308,160	bytes
Data rate		
To or from disk (Note 2)	889,000	bytes/second
		(nominal)
To or from channel (Note 3)	380,000	bytes/second
Access time (movable heads)		
Cylinder to cylinder	10	milliseconds (max)
Average seek (101 cylinders)	40	milliseconds (max)
Capacity (fixed heads-Models 1F and 2F only)		
Fixed heads	8	heads
Bytes/sector	256	bytes
Sectors/track	60	sectors
Total capacity	122,880	bytes
Average rotational delay or latency	10.1	milliseconds
		(nominal)

Notes.

- 1. The tracks (one under each head) that can be accessed without repositioning the heads are called a cylinder.
- 2. The data rate to or from the disk is 1.13 microseconds per byte or 141 nanoseconds per bit.
- 3. The data rate to or from the channel is the average time for multiple-sector data transfers over two rotations of the disk.

Diskette Specifications

The diskette specifications for the 4962 Models 2 and 2F are identical to those for the 4964 Diskette Unit described in a subsequent part of this chapter.

Operator Controls and Indicators

A Power On/Off switch and a Power On indicator are mounted on the front panel of each model of the 4962. When the Power switch is placed in the On position, ac and dc power are applied to the modular unit. The Power On indicator is lit when the Power switch is placed in the On position and voltages reach normal operating levels.

IBM 4964 Diskette Unit

The 4964 Diskette Unit is a data-exchange storage device designed for use with a Series/1 processor. This compact, direct-access storage device has a single, removable, magnetic diskette that serves as a data exchange medium. The diskette combines the small batch data storage properties of punched cards with many of the features of magnetic tape. The diskette has the added advantage of providing direct access to a specified group of records filed sequentially or randomly on it. The diskette unit is used for temporary or permanent storage of programs or data; the processor can refer to this storage to complete a specific task or application. The 4964 attaches to the Series/1 by means of the 4964 Diskette Attachment Feature, which can be plugged into either the processor unit or an I/O expansion unit. See Figure 5-3 for an illustration of the 4964 Diskette unit.

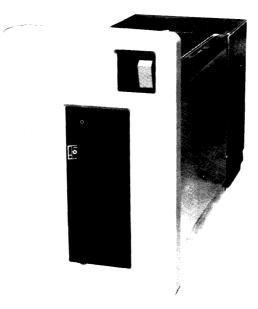


Figure 5-3. IBM 4964 Diskette Unit

Design Features

The 4964 Diskette Unit is a compact modular unit that fits in half the width of an EIA (RS-310B) rack. A rack-mounting fixture is required for mounting the unit.

As shown in Figure 5-4, two read/write heads are used to record or retrieve information from the 74 data tracks on each side of the removable diskette. The read/write heads are mounted on a carriage that moves the heads to the track location specified by the I/O command. The data tracks are divided into physical locations on the diskette called sectors. Each sector is initialized with a unique ID field; this permits random access to any sector on a data track. The diskette can be initialized with sector lengths of 128, 256, or 512 bytes.

An IBM 4964 Diskette Unit can exchange diskette data with other IBM devices using a one-sided diskette recorded in basic data exchange format (128-byte sector format).

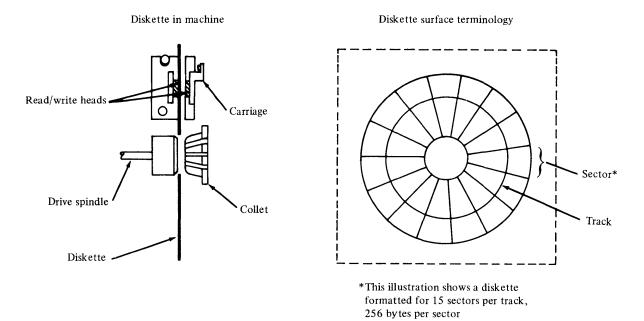
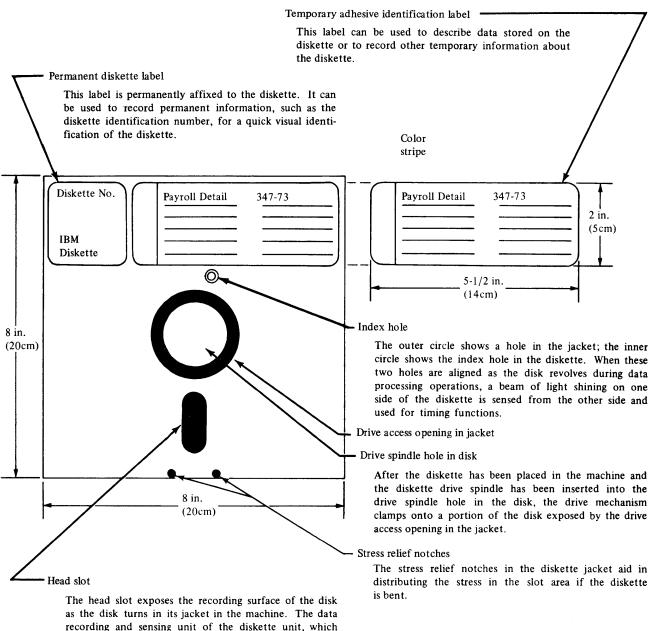


Figure 5-4. Diskette access mechanism and terminology

Figure 5-5 shows the diskette including its permanent jacket, which protects the surfaces from contamination. The figure also provides additional design information.



as the disk turns in its jacket in the machine. The data recording and sensing unit of the diskette unit, which is called a *read/write head* and is similar to the record/ playback head in a tape recorder, moves to specified positions along the length of the slot. Moving to a specified position is called *accessing a track*.

Figure 5-5. Diskette storage medium

Operating Characteristics

The data storage capacity of the 4964 depends on the sector length selected. This information and other specifications for the diskette unit are provided in the following table:

Factor	Magnitude	Unit
Maximum data storage capacity for a two-sided diskette (formatted 512 byte sectors)	606,208	bytes
Data transfer rate	31,250	bytes/second
Track to track access time derived from: T = (number of track crossings x 5 ms) + (35 ms	40 s settling time)	milliseconds
Tracks/inch	48	tracks
Total tracks/diskette surface	77	tracks
Data tracks/diskette surface	74	tracks
Capacity by sector size (formatted)		
128 bytes/sector	492,544	bytes
256 bytes/sector	568,320	bytes
512 bytes/sector	606,208	bytes
Rotational speed	360	RPM
Latency	83.8	milliseconds

Operator Controls and Indicators

A Power On/Off switch and Power On indicator are located on the 4964 front panel. When this switch is in the On position, ac and dc power are applied to the 4964. Power goes off, without regard to sequence, when the Power On/Off switch is placed in the Off position. The Power On indicator is lit when the Power On/Off switch is in the On position and voltages are at normal operating levels. The IBM 4973 Line Printer provides medium-to-high speed "hard copy" output for the Series/1 on continuous-form paper. Print speed is dependent on (1) the printer model and (2) the length of the character set. Two models of the 4973 are available. Model 1 prints 155 lines per minute and Model 2 prints 414 lines per minute when a character-set length of 48 characters is used.

The 4973 attaches to the Series/1 by means of the 4973 Line Printer Attachment Feature. This feature can be plugged into either the processor unit or an I/O expansion unit. See Figure 5-6 for an illustration of the 4973.

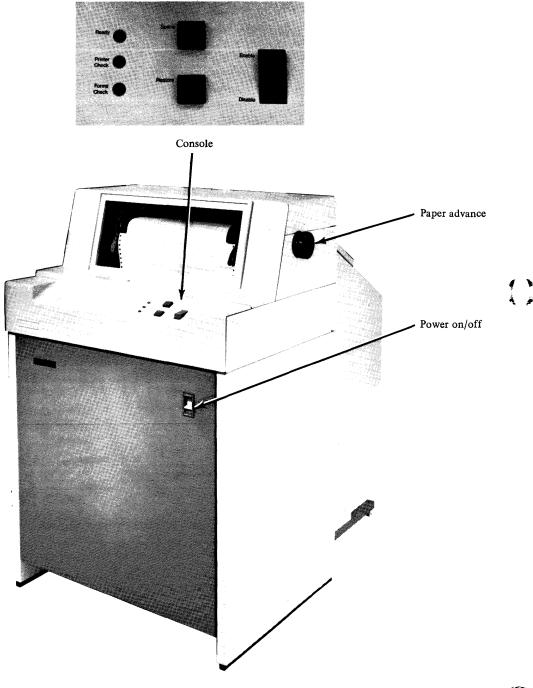


Figure 5-6. IBM 4973 Line Printer

Design Features

The 4973 Line Printer is a free-standing unit. It consists of three basic components: printing unit, carriage, and console. The printing unit consists of a platen, print belt, ink ribbon, and print hammers (66 print hammers for the Model 1 and 132 print hammers for the Model 2). Printing is accomplished by the print hammers, which selectively force the paper against the inked ribbon and the engraved characters on the print belt. The print hammers are selected through a belt translator and fired when the desired character on the belt is in the correct print position. If desired, the belt translator can be loaded, under program control, with the print-belt position to be printed for each of the possible 256 hexadecimal codes. The print belt is interchangeable and is available with 48, 64, or 94 EBCDIC character sets.

Both models of the 4973 have a pin-feed carriage that handles up to six-part forms. The carriage moves the forms at either 6 or 8 lines per inch under program control. Forms can also be skipped under program control at the rate of 12 inches per second.

The printer console contains the indicators and switches necessary for manual control of the printer (see "Operator Controls and Indicators").

Operating Characteristics

The approximate printing rates attainable for each model of the 4973 are as follows:

Length of	Lines per minute	
character set	4973 Model 1	4973 Model 2
48	155	414
64	120	300
94	80	235

Other specifications for either model:

Factor	Magnitude	Unit
Print-line length	132	Characters per line
Horizontal character spacing	10	Characters per inch
Vertical line spacing	6 or 8	Lines per inch
Forms skipping rate	12	Inches per second

The 4973 Printer will handle up to six-part forms with a maximum width of 381 mm (15 in.) and a maximum thickness of 76.2 mm (0.018 in).

Operator Controls and Indicators

Figure 5-6 shows the printer console and other controls for the 4973. The Power switch is located on the printer stand and turns the mainline power to the printer on or off. The Paper Advance knobs are located on either side of the printer cover; these knobs allow the operator to adjust the forms manually. The remaining indicators and switches are located on the printer console. The indicators are: Ready, Printer Check, and Forms Check. The switches are: Enable/Disable (system control), Carriage Restore, and Carriage Space.

The 4974 is a serial printer that provides medium-speed "hard copy" output for the Series/1 on either cut or continuous forms. The 4974 attaches to the Series/1 by means of the 4974 Printer Attachment Feature, which can be plugged into either the processor unit or an I/O expansion unit. See Figure 5-7 for an illustration of the 4974.

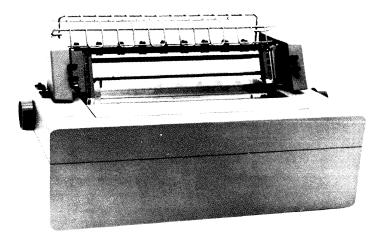


Figure 5-7. IBM 4974 Printer

Design Features

The 4974 Printer is a table-top unit. It consists of two basic components—a printing unit and a forms tractor. The printing unit consists of a platen, print head, and ribbon unit. A print head carrier transports the print head and ribbon unit horizontally along the print line; printing occurs in either direction.

The print head has eight vertical wires that are individually controlled by magnets. Characters are formed by printing a pattern of dots in a vertical arrangement that corresponds to a matrix stored in a *wire-image buffer*. The character-pattern matrix is 8-high by 7-wide. When a character is to be printed, the print head moves horizontally across the paper, along the print line, while selectively forcing the print wires against the ribbon to make the dots on the paper.

The wire-image buffer can be initialized, under program control, to a standard 64 EBCDIC character set. When the buffer is initialized, certain alternate characters can be specified to overlay their EBCDIC equivalents in the standard character set. If desired, the user can transfer his own complete wire-image table from main storage. Any eight-bit character code can be defined and selected (and altered) by the user to print a character set of up to 96 characters.

Forms are moved vertically using either a pressure feed for cut forms or a forms tractor for margin-punched continuous forms. Movement of the forms is under program control. During an I/O operation, parameters can be specified for: forms length, overflow line, and either the skip line on the next form or the number of lines to be spaced (84 lines maximum).

Operating Characteristics

The approximate printing rates attainable are as follows:

Characters per line	Lines per minute
34	150
45	122
70	86
90	69
132	49

Other specifications for the 4974:

Factor	Magnitude	Unit
Print speed	120	Characters per second
Print-line length (maximum)	132	Characters per line
Horizontal character spacing	10	Characters per inch
Vertical line spacing	6	Lines per inch

The 4974 Printer will accept up to six-part forms with a maximum thickness of 76.2 mm (0.018 in.). Five and six-part forms should be tried for satisfactory feeding, registration, and print quality. Card stock continuous forms are not recommended. For optimum handling of continuous forms, the special feature form stand (#4450) is recommended.

Operator Controls

The 4974 Printer has a number of controls. These controls are used primarily for moving and adjusting the paper or forms. The following table lists each control and briefly describes its purpose.

Control	Purpose	
• Power Switch	Used primarily to turn the power off when	
	the printer is being serviced.	
• Mode Switch	Provides three control positions: Print,	
	Wait, and Top of Forms.	
 Paper Advance Knobs 	Moves the forms for vertical positioning.	
• Paper Release Lever	Aids in forms removal or insertion of paper.	
• Horizontal Fine Adjustment Knob	Provides fine adjustment of the print line to vertical lines on the form.	
Copy Control Dial	Allows adjustment of the distance from the print head to the platen for various form thicknesses.	
• Ribbon Feed-Roll Release Knob	Provides clearance for removing and install- ing the printer ribbon.	
• End of Forms Switch	Signals that the end of the form is 1 to 3 inches from the line being printed.	

The IBM 4979 Display Station (Figure 5-8) is a data entry/operator station for the Series/1. It serves as a communication link between the user and the system. It provides image display of data transmitted to or from the processor. The display station enables the user to (1) retrieve data from the processor, (2) enter, modify, or delete data on the display, and (3) cause the revised data to be returned to the processor. The 4979 attaches to the Series/1 by means of the 4979 Display Station Attachment Feature, which can be plugged into either the processor unit or an I/O expansion unit.

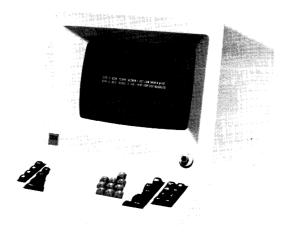


Figure 5-8. IBM 4979 Display Station

Design Features

or components-

The IBM 4979 Display Station is a table-top unit. It consists of two major components— a display screen and a keyboard.

Display Screen

The display screen is a 12-inch (diagonal) cathode ray tube (CRT). It has the capacity for 1920 characters arranged in a format of 24 lines of 80 characters each. Each character displayed consists of data generated in a pseudo 7 x 7 dot matrix on the CRT screen. The display on this unit is refreshed 50/60 times per second, creating an easy-to-read display under normal lighting conditions. The display station displays characters as: numeric, uppercase alphabetic, and special symbols. A special symbol (that resembles an underscore), called a *cursor*, is displayed beneath a character or character position on the display screen to indicate where the next character entered from the keyboard will be stored.

All data moved to and from the screen/keyboard is held in a buffer. The buffer capacity is 1920 characters. System data is transmitted to and from the buffer under program control.

The screen displays both data entered by the operator and data from the system. Under operator control, characters are displayed on the screen as they are entered and can be altered before they are transmitted to main storage. In order to transmit information entered from the keyboard, an interrupt request key must be pressed. This causes an interrupt to the processor. A subsequent processor issued command transfers the data.

Areas on the screen that always contain the same type of information are called *fields*. When a screen is divided into fields, it is called a formatted screen.

There are two types of fields on the display. A *protected data field* is primarily used by the application program and data cannot be entered into these fields from the keyboard. All operator entries are made in *input fields*. These fields are unprotected and data can be entered, modified, or erased by keyboard action. The user's program designates which data characters (fields) are protected and which are not. Protected characters have a lower light intensity than unprotected characters.

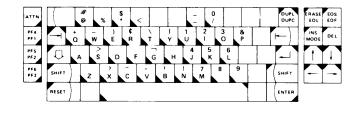
Unformatted screens can be used also. When the screen is unformatted, the operator uses the screen in a free-form manner.

Console Keyboard

The display station keyboard is a data-entry style keyboard similar to that of a typewriter. The alphanumeric and special character keys are located in the center area of the keyboard with special control keys on each side. (See Figure 5-9.)

The keyboard is arranged in four different key groups:

- Shift/Lock keys
- Graphic Alphanumeric
- Local Function
- Interrupt Request



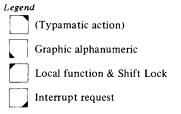


Figure 5-9. IBM 4979 keyboard layout

Certain keys within the graphic alphanumeric and local function categories have typamatic action. This means that they have the ability to repeat their character or operation automatically when held down. The other keys have momentary action; only one character or operation is entered when the key is pressed.

The Shift and Lock keys operate the same as on a standard typewriter keyboard.

The graphic alphanumeric keys represent the printable alphanumeric, space, and graphic symbols contained within the EBCDIC character set.

The local function keys cause movement of the data characters or the cursor within the attachment, but do not cause an interrupt request.

The Interrupt Request keys cause an attention interrupt request to the processor. The keyboard can be locked under program control to protect against unauthorized use. This feature is called *electronic lockout*.

Operator Controls

The display station has three external (off-keyboard) operator controls. These controls are located on a single knob that is situated on the front of the display station above the keyboard.

- On-Off
- Brightness
- Contrast

These controls allow for powering the unit and adjustment of the brightness and contrast of the display for a comfortable viewing level.

Operating Chatacteristics

The characteristics for the 4979 are shown in the following table:

Factor	Magnitude	Unit
Screen size (diagonal)	12	inches
Display format		
Characters per line	80	characters
Number of lines	24	lines
Total capacity	1920	characters
Display buffer capacity	1920	characters
Number of keys on keyboard	66	keys

IBM 4982 Sensor Input/Output Unit

The IBM 4982 Sensor Input/Output Unit (Figure 5-10) provides a flexible, modular approach for attaching the user's process I/O applications to the Series/1. The 4982 attaches to the Series/1 by means of the 4982 Sensor Input/Output Unit Attachment Feature, which can be plugged into either the processor unit or an I/O expansion unit. The sensor I/O unit has the capacity for eight sensor I/O feature cards. The various feature cards available are shown in Figure 5-11. These feature cards can be used in any combination except that only one analog input control card and one multirange amplifier cards installed in the 4982. Each 4982 Sensor I/O Unit, although not restricted to a single sensor I/O type, can contain the following maximum sensor points of each type:

- 128 Digital Input/Process Interrupt (DI/PI) points, either isolated or non-isolated
- 128 Digital Output (DO) points
- 112 Solid State Multiplexer Analog Input (AI) channels (sometimes referred to as points)-no Amplifier Multirange card used
- 96 Solid State Multiplexer AI channels (Amplifier Multirange card used)
- 56 Reed Relay Multiplexer AI channels (no Amplifier Multirange card used)
- 48 Reed Relay Multiplexer AI channels (Amplifier Multirange card used)
- 16 Analog Output (AO) points

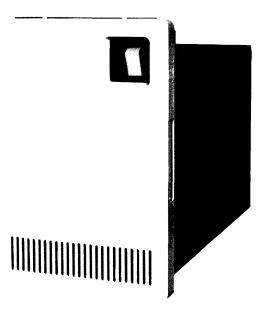


Figure 5-10. IBM 4982 Sensor Input/Output Unit

Design Features

The IBM 4982 Sensor Input/Output Unit is a compact modular unit that fits in half the width of an EIA (RS-310B) rack. A rack mounting fixture is required for mounting the unit. The 4982 is equipped as follows:

- A circuit board with nine card sockets (eight sensor I/O feature sockets and one termination socket)
- A 3.1 m (10 ft) attachment feature cable
- Cable termination and control functions (termination card)
- A power supply

The eight feature sockets and the termination card are accessible from the rear of the unit. The termination card, which connects the 4982 to the attachment feature cable, contains termination and control logic for the unit. Located in the front section of the unit, the 4982 power supply receives input power from the individual primary power distribution panel in the 4997 Rack Enclosure.

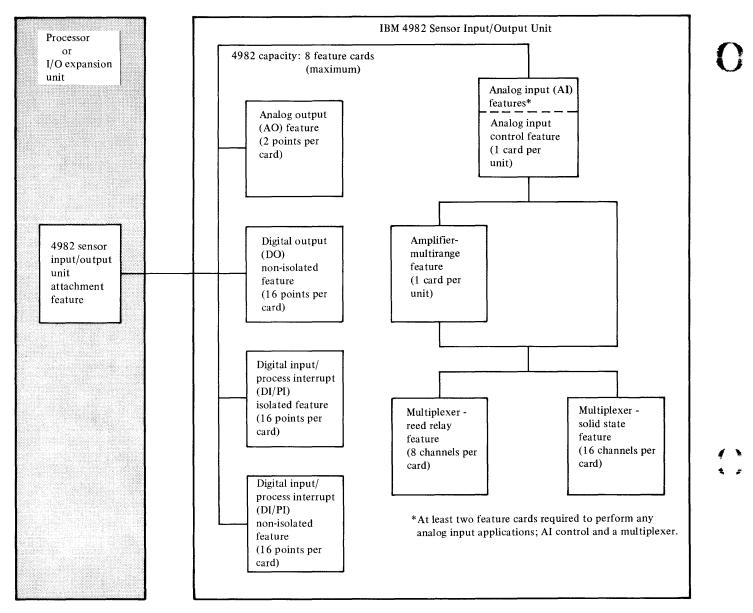


Figure 5-11. IBM 4982 Sensor Input/Output Unit configurator

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Card locations (slots) for the 4982 termination card and sensor I/O features are shown in Figure 5-12. Sensor I/O features are installed in any location and in any order, with the exception of analog input. The analog input control feature (if used) occupies card location 0, and the multirange amplifier feature (if used) occupies card location 1. A multiplexer feature occupies the location adjacent to the analog input control feature or to the multirange amplifier feature. Additional multiplexer features occupy successively adjacent locations.

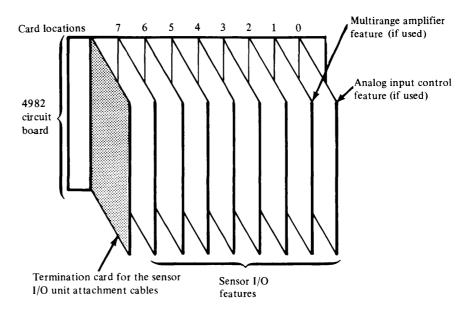


Figure 5-12. IBM 4982 Sensor I/O Unit card locations (rear view)

The suggested user cable connector is a commercially available 56-pin connector with a protective hood. This connector requires no special tools and provides an orderly method of terminating the large number of connections required for attaching a typical user process. For additional information, refer to the *Series/1 Installation Manual–Physical Planning Manual*, GA34-0029.

Direct program control commands are used for data transfers between the processor I/O channel and the sensor I/O features. The features are individually addressed from the processor using assigned feature addresses.

Operator Controls and Indicators

A Power On/Off switch and a Power On indicator are mounted on the front panel of the sensor I/O unit. When the Power switch is placed in the On position, power is applied to the unit. The Power On indicator is lit when the Power switch is placed in the On position and voltages are at normal operating levels.

Digital Input/Process Interrupt Isolated

The isolated DI/PI feature is a digital input logic card with signal conditioning at the user inputs. The card provides 16 points of optically isolated digital inputs for sensing high and low level logic voltage levels. There are four basic modes of operation:

- Digital Input. This mode allows 16 bits of unlatched user input data to be transferred to the processor. No interrupts are generated.
- Process Interrupt. In this mode, an interrupt is generated when a positive transition occurs at the user inputs; 16 bits of latched user data can be transferred to the processor. This mode is enabled by program control.
- External Sync. This mode allows the user to move 16 bits of input data into registers and then generate an interrupt. A non-isolated "external sync" input and a "sync ready" output are available for the user to synchronize parallel data transfers by using the DI/PI feature. External sync mode is enabled by program control.
- Diagnostic. In this mode. input data can be forced to 0-bits or 1-bits, overriding any user input states. Therefore, proper data flow and feature card operation can be checked by software. In addition, a status word is available to determine or verify the state or mode of the DI/PI card. Diagnostic mode is enabled by program control.

Digital Input/Process Interrupt Non-Isolated

The non-isolated DI/PI feature is a digital input logic card with signal conditioning at the user inputs. The card provides 16 points of digital input for sensing contact closures or logic voltage levels.

The non-isolated DI/PI feature is similar to the isolated DI/PI feature except for the following:

- A process interrupt input is sensed as a negative transition.
- Each of the 16 input points, with high or low level capabilities, can detect either user contact closure (contact sense) or user voltage levels (voltage sense).

A voltage of +48 volts dc is supplied by the 4982 to sense the opening and closing of the user contacts in the contact sense application. The user contacts are connected directly to the input terminals.

The state (high or low) of a user voltage is sensed in the voltage sense application.

Digital Output Non-Isolated

The non-isolated digital output (DO) feature card provides 16 points of solid state nonisolated DO. Each card has a 16-position register. Data is stored in this register under program control. The DO points correspond to the positions of the register. With a usersupplied voltage, each point is rated at a maximum of +52.8 volts dc and 250 milliamps. Without a user-supplied voltage, each point supplies a TTL compatible output voltage.

Analog Input Subsystem

The simplest AI subsystem configuration consists of the analog input control card and a single multiplexer card. The analog input control card is used in every configuration because it contains the analog-to-digital converter and the control logic for the rest of the subsystem. There are two kinds of multiplexer cards to choose from: multiplexer-solid state and multiplexer-reed relay. When additional inputs are required, up to seven multiplexer cards of either type, in any mix, can be used with the analog input control card. For measuring low level signals, the multirange amplifier is added to the subsystem. The 4982 can accommodate six multiplexer cards when the multirange amplifier is installed.

The AI subsystem configuration using multiplexer-solid state provides the fastest scanning and sampling rates. This configuration provides a differential input when the multirange amplifier is installed. The input is single-ended when the multirange amplifier is not installed. The conversion sequence lasts 72-172 microseconds depending on the input-voltage range selected and whether zero correction is to be done.

The AI subsystem configuration using multiplexer-reed relay cards provides the best performance in noisy environments because of its high common-mode voltage rejection. This configuration has a true differential input regardless of whether an amplifier card is installed. The conversion sequence lasts 5 milliseconds when the 5 volt input range is used and 8.2 milliseconds for the other input voltage ranges. All conversions automatically incorporate zero correction.

The AI subsystem achieves a very good temperature coefficient and stability specification with the zero correction logic on the analog input control card. The zero correction feature measures the offset voltage error, caused by temperature and aging in the multirange amplifier and the analog input control card, and digitally subtracts the error to obtain corrected measurements.

Analog Input Control Card

The analog input control card contains an 11 bit plus sign bit analog-to-digital converter for measuring signals in the -5 volt to +5 volt range. The card also contains the logic for controlling the sequencing of the other AI subsystem cards. Only two adjustments are required on the card: one for zero calibration and the other for full-scale calibration. Two diagnostic commands are used for this purpose; they also help diagnose the analog input control card and the amplifier card.

Amplifier Multirange Card

This card is a true differential input instrumentation amplifier with seven programmable input voltage ranges. It is required for measuring low level signals. The amplifier uses switched frequency compensation for wide bandwidth and fast settling. It uses the latest FET input operational amplifiers for high input impedance, very low input bias current, low noise, and good common-mode rejection ratio. There are two adjustments on the card: one for the offset voltage adjustment of the input stage and the other for the offset voltage.

Multiplexer-Solid State Card

The multiplexer-solid state card is a solid state multiplexer using MOS field effect transistors for switching. There are 16 two-wire inputs on the card. Solder tabs are provided so the user can solder capacitors to the card. This forms a low pass input filter for attenuating high-frequency normal-mode noise. The user can adjust the filter bandwidth by adjusting the capacitance value. The sampling rate with an input filter is restricted to 100 samples per second. If external noise is not a problem, much faster sampling rates can be obtained by operating without the capacitor. The maximum voltage which can be applied to either input line under normal operating conditions is 10 volts. Up to 15 volts can be applied as overload to all inputs simultaneously without damage. The input signal can have an equivalent source resistance of 1 kilohm with a 250 ohm source unbalance.

Multiplexer-Reed Relay Card

The multiplexer-reed relay is a reed relay multiplexer using the "flying capacitor" method of isolation. This technique gives the card a 200 volt common-mode voltage limit and a common-mode rejection ratio of 120 dB. There are 8 two-wire inputs per card with a 0.64 hertz, low pass input filter on each input to attenuate normal-mode noise. Because of the polarized capacitor in the input filter, the normal-mode signal on the 5 volt range is limited to -0.5 volts to +5 volts and the normal-mode overvoltage limit is -1 volt to +6 volts. The input signal can have an equivalent source resistance of 1 kilohm with a 1 kilohm source unbalance.

Analog Output

The analog output feature generates two points of analog output with a resolution of 9 bits plus sign or 10 bits. Each output point can be programmed to generate an output voltage up to ± 5 , ± 10 , or 0-+10 volts full scale, with a long term stability of $\pm 1/2$ the least significant bit (LSB) per 10,000 hours. The maximum output impedance is 1 ohm; the maximum current out is 5 milliamps at ± 10 volts, short circuit protected.

IBM 4959 Input/Output Expansion Unit

The IBM 4959 I/O Expansion Unit provides the Series/1 Processor with additional I/O feature locations. (See Figure 5-13.) A channel repower feature is required in the attached to unit if the 4959 is attached to:

- 1. A 4955 Processor with battery backup
- 2. Any 4953 Processor
- 3. Another 4959 I/O Expansion Unit

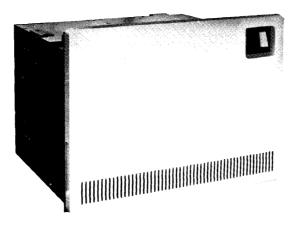
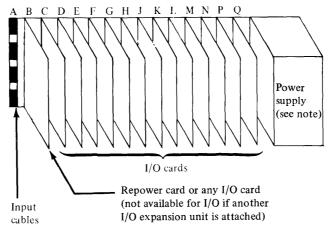


Figure 5-13. IBM 4959 Input/Output Expansion Unit

Design Features

A maximum of 14 I/O feature locations are contained in this full-width modular unit. (See Figure 5-14.) I/O features that can be plugged into the 4959 include: data processing I/O attachment features, communications features, user attachment features, and the sensor I/O unit attachment feature.



Note. The communications power feature provides ± 12 volts and is a prerequisite for the following I/O feature cards:

- All communications features
- Teletypewriter adapter feature using the non-isolated current loop
- Teletypewriter adapter feature using the EIA voltage level interface

Figure 5-14. IBM 4959 I/O Expansion Unit card plugging assignments

The 4959 I/O Expansion Unit contains a 300 watt power supply that distributes power to the various I/O feature cards. An optional feature for the power supply provides ± 12 -volt power for communications features. Cooling fans are contained in the upper section of this unit.

Operator Controls and Indicators

A Power On/Off switch and a Power On indicator are mounted on the front panel of the I/O expansion unit. When the Power switch is placed in the On position, power is applied to the unit. The Power On indicator is lit when the Power switch is placed in the On position and voltages are at normal operating levels.

IBM 4997 Rack Enclosure

The IBM 4997 Rack Enclosure provides mounting space for IBM Series/1 modular units. It has EIA (RS-310B) rack-mounting dimensions for housing standard 482.6 mm (19-inch) rack units. It is available in two sizes, under four model designations (see Figure 5-15).





Model 2A, 2B

Figure 5-15. IBM 4997 Rack Enclosures

Models 1A and 1B have the capacity for mounting two full-width modular units or comparable combinations of full and half-width modular units (limited to one 4962 Disk Storage Unit). The enclosure is 1 m (39.4 in.) high, 0.61 m (24 in.) wide, and 0.75 m (29.5 in.) deep.

Models 2A and 2B have the capacity for mounting four full-width modular units or a comparable combination of full and half-width modular units (limited to two 4962 Disk Storage Units). The enclosure is 1.8 m (70 in.) high, 0.61 m (24 in.) wide, and 0.75 m (29.5 in.) deep.

Plain front filler panels are provided with Models 1A and 2A. Decorative front filler panels are provided with Models 1B and 2B making them more suitable for areas of public display.

A rack mounting fixture is available for mounting half-width modular units. This optional feature has the capacity for two half-width units.

Design Features

All models of the 4997 Rack Enclosure provide an ac distribution system. The distribution system contains a 20-ampere circuit breaker and either four outlets (Models 1A, 1B) or eight outlets (Models 2A, 2B) mounted vertically at the rear of the enclosure. On the front frame of all enclosures is an instant power-off button (Emergency Pull). This is a manual control that turns off all power by tripping the main circuit breaker. The circuit breaker must be reset manually.

Each enclosure includes directional front wheels and swivel-type rear casters, removable side covers, and a rear door. A multi-bay arrangement may be obtained by removing the side covers and fastening the units together.

IBM 4999 Battery Backup Unit

The IBM 4999 Battery Backup Unit provides the IBM 4953 or 4955 Processor with emergency ac power when utility power is inadequate or temporarily lost. (See Figure 5-16.) The 4999 is available in two models based on the operating voltage of the processor:

- Model 1. For 100-123.5 volts ac, 50/60 Hz power
- Model 2. For 200–230 volts ac, 50/60 Hz power

Both of the models are half-width modular units that mount in an EIA (RS-310B) rack by means of the rack mounting fixture.



Figure 5-16. IBM 4999 Battery Backup Unit

Design Features

Utility power is supplied to the Series/1 Processor through connections on the 4999 Battery Backup Unit. This power is monitored by the unit, and in the event of a power failure, the input power to the Battery Backup Unit is automatically replaced by 12-volt battery power. The battery and charger unit are supplied by the user. The battery power is inverted from dc to ac and supplied to the processor as square-wave ac power at the required voltage level.

An ac power failure produces a class interrupt in the processor and turns on a status bit that remains on as long as power is supplied by the battery.

The backup unit can support only the processor. (A 100 ampere/hour battery could power the processor for 20 to 60 minutes.)

Operator Controls and Indicators

The 4999 Battery Backup Unit has controls and indicator lights that allow manual control of power and automatic monitoring of the unit. These controls and indicators include:

- Utility Power On/Off switch
- Battery Circuit Breaker
- Reset pushbutton
- Utility Power indicator
- Standby indicator
- On-Battery indicator
- Low Battery indicator
- Offline indicator

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Chapter 6. Programming Support

This chapter describes the program products offered in support of the IBM Series/1, and the Stand-Alone Utilities furnished as system control programming.

Realtime Programming System

The Realtime Programming System is the basic control program upon which applications are built. It is flexible and is suitable for a wide variety of applications. The operating system controls and manages system resources such as processor storage and devices. It is a multiprogramming, multitasking, event-driven, disk-based system that controls the environment for both realtime and batch applications.

The Realtime Programming System has four components-supervisor services, data management, utilities, and communications. The interface to these components is through macros, operator commands, job control statements, FORTRAN IV, and PL/I.

Supervisor Services

Supervisor services control the allocation and distribution of system resources. The supervisor manages:

- Storage
- Partitions
- Task sets
- Tasks
- Programs
- Events
- Queues
- Timers
- Serially reusable resources
- Interrupts
- Errors

Storage

Storage management controls the allocation of available protected or unprotected processor storage. It allocates that storage as a result of a request from a system or user program.

Partitions

The supervisor manages storage for program execution in partitions. A partition is a contiguous storage area of fixed size established at system generation. A partition begins and ends on a 2KB boundary, and there can be from 2 to 13 partitions defined. Partition 0 is always the system partition, and partitions 1-12 are for applications.

Task Sets

A task set is a named collection of programs, data, and control blocks that perform a related set of work. Only one task set can execute in a partition at a time, and each partition has a queue of task sets waiting to execute in that partition. There are three types of task sets:

- System task set—contains the programs, data, and control blocks that make up the supervisor. It executes in partition 0, resides in protected storage (if the processor is equipped with it), and executes in supervisor state.
- User task set—contains the programs, data, and control blocks that perform a related set of operations for an application.
- Shared task set—a special type of user task set that contains tasks, programs, event definitions, serially reusable resources, and queues to be shared across user task sets.

During task set installation, a task set can be bound to its execution environment so that execution is initiated more rapidly. Binding does such things as predefining tasks and queues and pre-opening data sets prior to task set execution.

Another feature of task set management is rollout/rollin. *Rollout* discontinues execution of a task set and copies its execution environment to a disk data set so that a higher priority task set can execute. *Rollin* copies the disk data set back into storage and resumes executing the task set.

Tasks

A task is a unit of work—a single thread of execution through one or more programs within a task set. In the simplest case, it consists of one program. In more complex situations, a task can be several programs with overlays.

Each task set has a *primary task*—the first task activated when a task set begins execution. A task set can optionally contain one or more *secondary tasks*. Secondary tasks are tasks initiated by a program executing under either the primary or another secondary task. Tasks can be activated by:

- Process interrupts
- Program interrupts
- Timer services
- Other tasks

Programs

Program management controls both problem programs and supervisor programs. *Problem programs* can be either (1) storage-resident programs, which remain in storage until task set termination, or (2) disk overlays, which reside on disk until loaded into an overlay area within the partition. A *supervisor program* can be either storage-resident or a disk-resident transient.

Events

Task execution can be synchronized by identifying events, specifying the points where execution must be suspended until the event occurs, and signalling the waiting task when the event occurs. For example, a programmer can define events to indicate that:

- An I/O operation is complete
- A task has reached a certain point in its processing
- An element has been added to a queue
- An occurrence has happened a specified number of times

Queues

The supervisor manages two types of data queues-storage and disk. *Storage queues* reside completely in processor storage. *Disk queues* can vary-their definitions reside in processor storage; their control information and data elements reside either in processor storage or in a direct-access data set.

Timers

The services of timer management control logical timers, and supply the time-of-day (maintained in the system), and the date (also maintained in the system). These services are used for time and date dependent operations.

Serially Reusable Resources

The supervisor provides facilities to designate a resource, such as a program, event, queue, or data set, as one that tasks must use serially. The supervisor serializes access to serially reusable resources that can be requested asynchronously from different tasks.

When a task requests access to a serially reusable resource, the resource is then *busy* and subsequent requests from other tasks are not granted until the resource is released by the task that requested it.

Interrupts

Interrupt management processes both I/O interrupts and class interrupts. The supervisor handles priority interrupts from data-processing I/O devices and sensor I/O devices. When an I/O interrupt occurs, it starts a previously defined interrupt service task.

Class interrupt handlers process interrupts from error or exception conditions. They handle these types of interrupts:

- Machine check
- Program check
- Power/thermal warning
- Programmer console
- Trace
- Soft exception
- Supervisor call

Errors

Error management services assist in the determination and correction of errors detected by hardware and software. Error management functions are:

- Error logging and reporting
- Abnormal termination of a task
- Copying primary storage to a data set for later retrieval
- Establishing task error exits
- Displaying/patching storage
- Attended/unattended status indicator
- System reload and restart
- System termination

Data Management

Data management moves information between processor storage and external devices, maintains the data on those devices, and controls those devices. Data management is divided into two categories—data set management and device management.

Data set management handles data sets, which are named collections of data residing on a device. It has:

- Three levels of access-basic (EXIO), physical (READ/WRITE) and logical (GET/PUT)
- Two access methods—sequential and direct
- Three data set organizations-consecutive, random, and partitioned

Device management handles physical devices, and the errors and interrupts from them. The data-processing I/O portion of device management controls the:

- Operator station (teletypewriter or equivalent)
- Display station
- Matrix printer
- Line printer
- Diskette unit
- Fixed-disk storage unit

The sensor-based I/O portion of device management controls:

- Digital input and output
- Analog input and output

Data management also has facilities for accessing timers.

Utilities

The Realtime Programming System utilities are divided into two categories—*stand-alone utilities* and *system utilities*. The stand-alone utilities are loaded into processor storage from diskette, whereas the system utilities require a disk as the system-resident volume. Once a stand-alone utility is loaded, no other program can execute concurrently with it. The stand-alone utilities are:

- Processor-storage-to-diskette dump
- Disk initialization
- System build (builds a disk in preparation for executing system utilities or for system generation)

The system utilities run under the operating system, and they require a disk as the system-resident volume. The system utilities are:

- Compress-consolidates free space within a data set or volume
- Copy-copies an image from one location to another
- Define-creates, deletes, or renames a data set, member, or volume; also builds or deletes a data set definition
- Initialize-formats a diskette
- IPLmaint-prepares a diskette for a storage-to-diskette dump, or changes the name of the system to be loaded by the next IPL sequence
- Merge-combines two partitioned data sets or volumes into a third partitioned data set or volume
- Patch-modifies information stored on a disk or diskette
- Report-generates reports (directories, data dumps, or storage-image dumps)

Communications

The communications component directs the transfer of data between programs and remote stations. A *remote station* is either a terminal or another computer. Communications handles point-to-point connections between stations that use start-stop (asynchronous) and binary synchronous line control. The communications component:

- Establishes, terminates, and controls access between programs and remote stations
- Transfers data between programs and remote stations on point-to-point lines
- Permits online testing of start/stop communications terminals

Hardware Configuration Requirements

The minimum hardware required by the operating system is:

processor	IBM 4953 Processor (48KB minimum)
	or
	IBM 4955 Processor (48KB minimum)
IPL devices	One IBM 4962 Model 2 or Model 2F Disk Storage Unit (combination disk/diskette unit)
	or
	One IBM 4962 Model 1 or Model 1F Disk Storage Unit <i>and</i> one IBM 4964 Diskette Unit

operator	One IBM 4979 Display Station
station	or A teletypewriter or other ASCII device that is compatible with the
	Teletypewriter Adapter #7850. If this type of operator station is chosen, the processor must be equipped with the Teletypewriter Adapter.
hard-copy	One IBM 4973 Line Printer
device	or
	One IBM 4974 Printer
	or
	A teletypewriter or other ASCII device that is compatible with the
	Teletypewriter Adapter #7850. If this type of hard-copy device is chosen, the processor must be equipped with the Teletypewriter
	Adapter.

The operating system permits more than one of all the devices in the preceding list, with the exception of the processor.

The optional hardware that is available for use with the operating system is:

- The IBM 4982 Sensor Input/Output Unit, which supports:
 - Analog input
 - Analog output
 - Digital input
 - Digital output
- Integrated Digital Input/Output Non-Isolated (#1560)
- Timers (#7840)
- Communications adapters for asynchronous (start-stop) and binary synchronous communications:
 - Asynchronous Communications Single-Line Control (#1610)
 - Binary Synchronous Communications Single-Line Control-low/medium speed (#2074)
 - Binary Synchronous Communications Single-Line Control-high speed (#2075)
 - Asynchronous Communications 8-Line Control (#2091)
 - Asynchronous Communications 4-Line Adapter (#2092)
 - Binary Synchronous Communications 8-Line Control (#2093)
 - Binary Synchronous Communications 4-Line Adapter (#2094)
 - Communications Indicator Panel (#2000)

Note. Operating system communications supports two types of terminals-the IBM 2740 Communications Terminal (Model 1), and the Teletype Model ASR 33/35.

- Floating-point (#3920)
- Programmer console (#5650)
- IBM 4999 Battery Backup Unit

Program Preparation Subsystem

The Program Preparation Subsystem provides program preparation capability in a batch processing environment. The subsystem consists of four components:

- A job stream processor
- A text editor
- A macro assembler
- An application builder

Job control statements are provided to invoke a task set and describe the data sets and devices it uses. The job stream processor reads, analyzes, and processes the job control statements, and provides transition from one batch program to the next.

The text editor is used to create and modify text data sets, such as data sets containing source code or job control statements. Source code data sets created with the text editor can be assembled by the Program Preparation Subsystem's macro assembler, or compiled by the Series/1 FORTRAN IV or Series/1 PL/I compilers.

The object modules that result from assembly or compilation are processed by the application builder before execution. This three-phase program produces the task sets that execute under the Realtime Programming System.

The Program Preparation Subsystem requires the same minimum hardware configuration as the Realtime Programming System. The subsystem's components run in a 16KB or larger partition, called the batch partition, under control of the operating system. The storage size of the minimum configuration, 48KB, allows at least a 16KB partition for the Program Preparation Subsystem. The batch partition is not reserved for the subsystem; realtime applications can use it either when the subsystem is inactive or by preempting the partition during a batch processing session.

Job Stream Processor

The job stream processor controls batch processing activity. It reads and analyzes the stream of job control statements that specify the task sets to be executed and the data sets and devices that the task sets use. Control statements and data that apply to the execution of a task set are grouped into steps; related steps, such as an assembly and application build, are grouped into jobs. The job stream processor provides transition from step to step and from job to job.

Control statements can come from a variety of sources; they can be entered through an interactive device, including the operator station, or the job stream processor can read them from a disk or diskette data set. During a batch processing session, the source of control statements can be changed from one device or data set to another.

The ability to specify the data sets and devices that a task set will use by coding job control statements gives considerable flexibility. A task set can be device independent, because the data sets and devices it uses can be changed by simply changing job control statements. For example, input data for a program can come from a disk in one job, an interactive device in another, and a diskette in a third.

Control statements that specify data sets and devices can be grouped into lists and stored on the system. A job can use them by referencing the list instead of repeating all of the control statements, and each job can tailor the list to its specific needs.

Job control statements provide capabilities to do the following:

- Identify a task set to be executed.
- Define data sets and devices. The user can create or delete permanent data sets, and can create temporary data sets.
- Pass parameters to a task set.
- Change the source of job control statements during a batch processing session.
- Assemble or compile a program, build a task set, and execute the task set by coding job control statements.
- Include data with control statements.
- Delimit jobs and steps.
- Cancel steps in order to correct control statement errors.
- Include comments on and between control statements.

Text Editor

The text editor is used to create, modify, list, and save text data sets. These data sets can be used as input to the subsystem's macro assembler or to a compiler.

The text editor executes in the batch partition. Once invoked, the text editor can be used conversationally by entering commands and text from an interactive device, or it may be used in a non-conversational mode if commands and text come from a data set. The editor's input can come from the IBM 4979 Display Station. If the display station is also used as the interface to the operating system, the text editor operates in shared (splitscreen) mode; the user can define part of the screen, usually the lower portion, for system use, while the upper screen area is set aside for the editor.

The text editor's commands provide the capability to do the following:

- Copy or move one or more lines from one location to another
- Change or replace text within a field for one or more lines
- Delete some or all lines
- List or display all or part of a single line or of multiple lines
- Search for text and print each line containing the text
- Insert lines
- Save text in and retrieve text from a disk or diskette data set
- Set tabs
- Clear the editor workspace
- Display the current settings for session variables; that is, line length, last line number, tab character, tab columns, portion of line to be displayed, and number of records in the workspace
- Suspend an editing session and resume it without respecifying session variables and with the same workspace conditions that existed in the prior session

Macro Assembler

The macro assembler translates symbolic source statements into an object module, which consists of object code and information that the application builder uses for its processing. The macro assembler executes as a batch job, either alone or as part of a multi-step job that can assemble, build and execute a task set.

The assembler processes three types of source statements—machine instructions, assembler instructions, and macro instructions. Each machine instruction is the mnemonic representation of a single processor instruction (Appendix A contains the instruction set). Assembler instructions direct the assembler to perform certain operations, such as defining data constants or reserving storage areas. Macro instructions generate a predefined sequence of machine and assembler instructions.

Assembler Instructions

Assembler instructions perform these functions:

- Define and structure control sections, dummy control sections, common control sections, and global control sections
- Control base register usage
- Adjust the location counter
- Define data or reserve storage for data
- Maintain a control section stack
- Define entry points
- Identify external symbols and weak external symbols
- Assign values to symbols and reference registers symbolically
- Copy source statements from a library
- Communicate between subroutines via parameters
- Control listing format and content
- Change the start, end, and continuation columns for source statements
- Check sequence of source statements

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Macro Instructions

The macro instructions perform these functions in a macro definition:

- Branch conditionally and unconditionally, which allows conditional assembly.
- Define and initialize global variables, that is, variables used to communicate between macro definitions.
- Define and initialize local variables, that is, variables used within a macro definition.
- Assign values to global and local variables. Variables can contain arithmetic, binary, or character data.
- Generate error messages and comments.

Assembler Options

Assembler options are specified on a job control statement. Options are available to do the following:

- Request or suppress listings
- Control the content and format of listings
- Request or suppress macro phase processing
- Dump the assembler's internal work data sets
- Request or suppress object module output

Application Builder

The application builder creates a task set from object modules produced by the macro assembler or a compiler, and from information specified on application builder control statements. The task set contains programs, data, and control blocks, including a control module and an optional prebind module. A control module is a set of tables and control blocks that contain control and parameter information pertaining to the task set. This information is used by the operating system to execute requested functions. The prebind module contains specifications used during task set installation, a process that enables a task set to start execution more rapidly.

The application builder is a three-phase program. All phases can run as a single job or step, or the phases can be executed in multiple jobs. Phase 1 primarily combines object modules into composite modules, which are further processed by phase 3. Composite modules can be simple or overlay structured. A simple structure contains a resident segment (a segment is one or more object modules) that remains in primary storage for the duration of task set execution. Overlay structures contain overlay segments in addition to the resident segment.

Phase 2 creates the control module and the optional prebind module according to information supplied on phase 2 control statements.

Phase 3 creates task sets by accomplishing the following:

- Combining composite modules, with addresses resolved relative to a partition origin
- Resolving external references
- Combining global sections into a task set global area
- Combining overlay segments into an overlay module
- Combining resident segments, their associated common and overlay areas, and the control module with addresses assigned and references resolved

At the user's request, the application builder produces maps of the composite module and the task set.

This section describes the Series/1 FORTRAN IV program products, a compiler and object support library, and a Realtime Subroutine Library.

FORTRAN IV Language

The language meets the ISA S61.1-1976 draft standard, and together with MFSL meets most of American National Standard (ANS) FORTRAN, X3.10-1966. The language has also been enhanced with IBM extensions to support multi-tasking and programming communications. Source programs written in the FORTRAN IV language can be used for plant and laboratory automation, process control, report generation, problem solving, and sensor-based data acquisition. FORTRAN IV is particularly useful in writing programs for applications that involve mathematical computations and other manipulation of numerical data.

FORTRAN IV Compiler and Object Support Library

FORTRAN IV Compiler

The FORTRAN IV compiler is a serially reusable, single task set that can execute as a batch job under the Program Preparation Subsystem in a Realtime Programming System environment. The compiler translates a source program into an object module acceptable to the application builder. Source statements are analyzed by the FORTRAN IV compiler for correct syntax, and appropriate diagnostic error messages are produced when errors are detected. In addition to the object module, the compiler optionally produces the following maps and listings:

- Source statements listing
- Statement label map with relative addresses
- Map of storage locations for variables and arrays
- Hexadecimal listing of the object code with statement offsets identified
- Cross-reference index for symbols and labels

The FORTRAN IV compiler can execute on a Series/1 configuration that does not have floating-point support. Similarly, FORTRAN IV programs that do not use REAL numbers do not require floating-point support. The FORTRAN IV compiler executes in a batch environment under control of the Realtime Programming System. It operates in the same minimum hardware configuration as the operating system except that at least a 16KB batch partition is required.

FORTRAN IV Object Support Library

The object support library is a group of subroutines designed to be combined, as needed, with the object modules produced by the compiler to form a task set executable on a Series/1 computer under control of the Realtime Programming System supervisor. The library subroutines perform:

- Input/output processing
- Error handling
- Explicit and implicit service operations
- Bit manipulation functions

The compiler generates a call to the necessary library routine at the appropriate point in the object code. During application builder processing, copies of these library routines are made part of the task set. Then, at execution time, the library routines perform their various functions.

FORTRAN IV Realtime Subroutine Library

The Realtime Subroutine Library provides operating system support. The procedures in this library are available to programs via the CALL statement. Figure 6-1 summarizes the functions provided.

Subroutine category	Functions
Execute function subroutines	Start and stop programs, and delay execution for a period or until a specified time.
Process I/O subroutines	Analogread input groups in sequence or in a user-specified sequence, and write output registers. Digitalread input registers, and set and reset digital output points or groups.
System service interface subroutines	Define and delete events and queues. Wait for and post event completion. Add and remove an element from a queue. Define, delete, request, and release a resource. Connect to or disconnect from an interrupt. Attach and detach (terminate) a task. Queue a task set for execution and terminate it. Modify System Scheduler table and System Task Set table. Set task error exit. Read and write time-of-day. Set ROLLIN/ROLLOUT status.
Time and date subroutines	Determine the current time-of-day and calendar date.

Figure 6-1. Functions that the FORTRAN IV Realtime Subroutine Library performs

Mathematical and Functional Subroutine Library

The Mathematical and Functional Subroutine Library (MFSL) is a set of subroutines provided as a program product for Series/1 application programming. MFSL supports the Series/1 FORTRAN IV program product and the macro assembler language that is part of the Series/1 Program Preparation Subsystem program product.

The operating environment for MFSL normally includes the Series/1 Realtime Programming System and the Program Preparation Subsystem. However, a user-written operating system that provides the required interfaces can also use the MFSL subroutines. MFSL is compatible with any Series/1 hardware configuration that includes the primary and secondary storage required for the MFSL subroutines used. The configuration requires floating-point support only if the user application requires REAL (floatingpoint) arithmetic. MFSL functions that operate on integer (fixed-point) variables have no internal requirements for floating-point support. If the processor does not have floatingpoint capability and it is needed, then the floating-point emulator option of the Realtime Programming System should be included. There are four kinds of MFSL subroutines:

- Mathematical subroutines
- Conversion subroutines
- Error-checking subroutines
- Service subroutines (assembler applications only)

The following sections describe each kind of MFSL subroutine.

Mathematical Subroutines

The mathematical subroutines in MFSL provide a basic computational facility for logarithmic and trigonometric functions, the hyperbolic tangent function, and miscellaneous functions that are useful in application programming. A complete list of the mathematical subroutine functions follows:

- Arc tangent, one or two arguments
- Cosine
- Divide doubleword integers
- Exponential function
- Exponentiation
- Hyperbolic tangent
- Logarithms, common or natural
- Maximum value
- Minimum value
- Modular arithmetic
- Multiply doubleword integers
- Positive difference
- Sine
- Square root
- Transfer of sign

Conversion Subroutines

MFSL includes subroutines that convert numeric data between the external EBCDIC format, used by many key entry devices and printers, and the internal integer (fixed-point) or real (floating-point) format that the computer requires to do arithmetic operations on the data. These subroutines are invoked by the CALL statement in FORTRAN IV and the CALL macro instruction in assembler language. The available conversions are listed in Figure 6-2.

From	То
EBCDIC, with or	Floating-point single precision (REAL*4)
without exponent	Floating-point double precision (REAL*8)
EBCDIC, no exponent	Fullword integer (INTEGER*2)
-	Doubleword integer (INTEGER*4)
Floating-point single	EBCDIC, with exponent
precision	EBCDIC, no exponent
Floating-point double	EBCDIC, with exponent
precision	EBCDIC, no exponent
Fullword integer	EBCDIC, no exponent
Doubleword integer	EBCDIC, no exponent

Figure 6-2. Conversion provided by MFSL Conversion Subroutines

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Error-checking Subroutines

The MFSL subroutines do not produce error messages, but communicate with the user through flags in the MFSL library work area. The user must either check function arguments before invoking a subroutine or use the error-checking subroutines to validate the results. The error-checking subroutines check for the following errors:

- Logarithmic, trigonometric, exponential, square root, or conversion subroutine errors
- Floating-point divide by zero, overflow, or underflow

Service Subroutines (Assembler Only)

The MFSL subroutines require an operating environment that includes the MFSL library work area and an interruption handling facility. This environment is established by the compiler for FORTRAN IV programs or for a set of programs whose main program is in FORTRAN IV. Assembler language programs that do not execute in a FORTRAN IV environment must perform these service subroutine calls. The library service subroutines provide these functions:

- Initialize and delete the library work area
- Specify the abnormal termination routine

PL/I

Series/1 PL/I is a subset of the American National Standard (ANS) Programming Language PL/I (ANSI X3.53-1976), plus extensions. It requires two additional program products for its operation: IBM Series/1 Program Preparation Subsystem and IBM Series/1 Real-time Programming System. PL/I consists of two products: (1) a compiler with a resident library and (2) a transient library. The resident library is made part of a program prior to execution of the application builder. The transient library is installed into the shared task set of the execution system to support the application object program.

The PL/I compiler executes in a batch environment requiring a 28KB partition under control of the Realtime Programming System. It operates in the same minimum hardware configuration as the operating system, except that the processor must have 64KB of storage.

The Series/1 PL/I language is extensive in function and allows development of application programs that can be extended or changed. Highlights of the PL/I offering include:

- Language extensions
- Input/Output (I/O) capability
- Multiple data types and organizations
- Data manipulation features
- Productivity features
- Additional features

Language Extensions

Series/1 PL/I extends the PL/I language to allow easy development of realtime applications, while simultaneously retaining the basic structure and philosophy of the PL/I language. To achieve this, extensions are provided in the following areas:

- Ability to schedule, execute, and control external procedures as independent parallel tasks
- Ability to schedule and execute task sets
- Support for synchronization and control of program data and flow by using EVENT variables, LOCK variables, and deadlock avoidance
- Extension of event concepts to recognize time-of-day events, events triggered by external causes (that is, process interrupts), repetitive events, and resetting events
- Extension of PL/I record I/O to handle digital and analog I/O

I/O Capability

Series/1 PL/I supports both stream and record I/O. Stream I/O statements read and write data with a minimum of programming effort, because automatic formatting and conversion are provided. The following specific options are available:

- List directed I/O.
- Allows the user to read or write data with automatic formatting and conversion.
- Edit-directed I/O.

A range of format items, including picture qualifications and control, allows generation of complex reports with a minimum of programming effort.

Record I/O statements allow more control over I/O. The following options are available:

• Consecutive synchronous I/O.

This facility is available through the use of the READ, WRITE, and REWRITE statements. The EVENT options for asynchronous I/O improves execution-time performance.

• Direct I/O.

This facility is available through the use of the READ, WRITE, DELETE and REWRITE statements with the KEY option. Asynchronous direct I/O is also permitted.

• Sensor I/O.

The facility for handling both sequential and random sampling of analog and digital I/O is available through the use of the READ and REWRITE statements.

• Transient files.

This form of file organization allows communication of data between operating system queues using PL/I READ and WRITE statements. The PL/I program can detect and handle the empty queue situation by coding an ON-unit for the PENDING ON-condition.

Data Types and Organizations

Series/1 PL/I supports arithmetic data, string data, and program control data. Arithmetic data can be represented in either binary or decimal radix and can be either fixed or floating point. Fixed point binary word and doubleword precisions are supported. Decimal fixed point data can have up to 15 digit positions, with up to 15 fractional positions. String data can be either bit or character, with fixed or varying length attributes. Program control data can be label, event, activation, lock, or pointer. Entry and file parameters are also supported.

PL/I data may be organized into arrays of up to 15 dimensions or in structures (hierarchical collections of data, not necessarily of the same type). A structure can also be dimensioned.

Data Manipulation Features

Series/1 PL/I supports all major PL/I operators, data types, and statements. Of particular interest are:

- String operations, including substrings, concatenation, and general boolean operations
- Language built-in functions, including mathematical functions, string functions, and array functions
- Structure assignment
- Automatic data conversions in expressions
- Generalized subscripting
- Full support for internal and external procedures
- Control structures including IF-THEN, IF-THEN-ELSE, DO, and DO-WHILE

Productivity Features

Included in this category are:

- Compile-time diagnostic messages
- Compile-time listing aids
- Execution-time diagnostic messages
- User programming and control of error conditions with the PL/I ON-handling language

Additional Features

These features make Series/1 PL/I uniquely suitable as a general application development tool. Of particular interest are:

- Storage efficiency gained by the generation of reenterable code and support for automatic storage allocation
- Program modularity and interface checking provided by the PL/I block structure and scope rules and the ENTRY attribute
- The ability to build and manipulate chained data lists and rings using the PL/I list processing support; that is, the pointer data type and based storage

In summary, Series/1 PL/I is aimed at decreasing application development time in areas such as realtime, scientific or problem solving, as well as traditional data processing. These features also make it useful when implementing advanced applications such as transaction processing and data base handling.

Base Program Preparation Facilities

This program product consists of a text editor, a macro assembler, and a linkage editor. These components are the basic tools for preparing executable load modules for the IBM Series/1. The following topics describe these components.

Text Editor

The text editor is used to create and modify source statements and files that can be used as input to the macro assembler.

The operator station is the interface with the editor. It is used to invoke the editor, to define workspace on the disk, and to enter conversational commands and text. These commands can create new text, retrieve text from a diskette, and change, add, delete, or list text. The editor uses the operator station to write messages and prompt for commands or text.

Here is a summary of the functions of the text editor commands:

- Copy one or more lines from one area in the editor workspace to another
- Change a field or character string
- Delete lines
- End the editing session
- Search for text and print each line containing the text
- Get text data from a diskette
- Insert lines
- List at the operator station or printer one or more text lines
- Copy all text lines to a diskette
- Set tabs

The module being edited can contain up to 65,535 lines of text (with a maximum of 128 characters per line). The editor sends its output to diskette and can print a listing at either the operator station or the printer.

Macro Assembler

The macro assembler translates symbolic source statements into a relocatable object module. There are three types of instructions—machine instructions, which are mnemonic representations of single processor instructions; assembler instructions, which request the assembler to perform certain operations during assembly; and macro instructions, which define sequences of machine and assembler instructions for use in the current assembly or in all assemblies.

Assembler instructions can be used to perform these functions:

- Define and structure control sections and dummy control sections
- Control base register usage
- Define data or reserve storage for data
- Define entry points
- Identify external symbols
- Assign values to symbols and reference registers symbolically
- Control listing format and content

The macro instructions can be used to perform these functions in a macro definition:

- Branch conditionally and unconditionally, which provides a conditional assembly capability.
- Define and initialize global variables, that is, variables used to communicate between macro definitions.
- Define and initialize local variables, that is, variables used with a macro definition.
- Assign values to global and local variables. Variables can contain arithmetic, binary, or character data.
- Generate error message and comments.

The macro assembler prompts the operator for the locations of assembler files and for assembler options. Source input comes from the diskette except for user-defined macro definitions, which may reside on disk. Three disk workspaces are required, and the output object module is written to disk.

Assembler options are available to do the following:

- Request or suppress listings
- Control the content of listings
- Pass a parameter used during macro processing

Assembler listings are written to the printer.

Linkage Editor

The linkage editor combines and links relocatable object modules into a single, non-relocatable load module with all cross references resolved, and places the load module on disk. All executable programs must be in load module format.

The linkage editor does the following:

- Processes macro assembler object modules
- Combines and links object modules
- Assigns storage addresses
- Resolves external references
- Relocates address-dependent locations relative to a specific load point
- Prepares diagnostic and storage map listings

Before input processing begins, the user must allocate three disk workspaces, define input data files, and define the location of the output load module. This information is entered through the operator station in response to linkage editor prompts.

Hardware Configuration Requirements

The Series/1 can be configured using different combinations of processors and devices. The minimum hardware configuration required to support the Base Program Preparation Facilities is:

processor	IBM 4953 Processor (32 KB minimum) or IBM 4955 Processor (32 KB minimum)
disk/diskette	One IBM 4962 Model 2 or Model 2F Disk Storage Unit (combination disk/diskette unit) or One IBM 4962 Model 1 or Model 1F Disk Storage Unit and one IBM 4964 Diskette Unit
	To improve performance, macro assembler work files can optionally be assigned to a second or third disk, if available.
printer	One IBM 4974 Printer
operator station	A teletypewriter or other ASCII device that is compatible with the Teletypewriter Adapter #7850, which must be installed on the processor

In addition to the minimum hardware configuration, multiple diskettes and disks are supported.

Stand-Alone Utilities

The Stand-Alone Utilities are furnished as system control programming for the IBM Series/1. These utilities enable the user to IPL, initialize diskette and disks, copy, dump, patch, perform automatic system build, and verify the system. Figure 6-3 shows the utilities and their functions.

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Purpose	Utility	Function
Initial program load	Diskette IPL Bootstrap	Loads a program from a fixed diskette location.
	Disk IPL Bootstrap/Loader	Loads a program from a user-specified disk location.
Direct access initialization	Diskette Initialization	Formats tracks into sectors. Analyzes track for defects; assigns alternate cylinders. Writes identification records.
	Disk Initialization	Verifies sector identification records. Analyzes sectors for defects; assigns alternate sectors.
Modify diskette header records	Create Diskette HDR1 Delete Diskette HDR1	Writes a basic exchange HDR1 record Rewrites a HDR1 as unused.
Copy data	Diskette to Disk Copy Disk to Diskette Copy	Copies data from one direct-access storage medium to another.
Dump data	Diskette to Printer Dump Disk to Printer Dump Storage to Printer Dump	Prints a specified direct-access file or processor storage area. The listing is in hexadecimal with EBCDIC translation.
	Storage to Diskette Dump	Writes the contents of processor storage to a diskette.
Change direct- access data	Diskette Patch Disk Patch	Modifies specified bytes on diskette or disk.
System build	Automatic System Build	Copies the Stand-Alone Utilities from the IBM-supplied diskette to predefined disk areas.
	System Verification	Ensures that the system disk was built properly.

Figure 6-3. Stand-Alone Utilities

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Appendix A. Instruction Set and Estimated Execution Times

This appendix contains a list, by instruction type, of the Series/1 instruction set. Each entry contains the assembler instruction name, assembler mnemonic, and estimated execution time by processor. The instruction names for extended mnemonics are indented under the basic machine instruction. If a given instruction is not available on one of the processors, NA appears in the appropriate execution-time column. An asterisk (*) indicates that there is an indirect version of the machine mnemonic.

The following assumptions were used in calculating these execution times:

- For most instructions, a typical execution time is given. Register to Storage, Register to Storage (Long), Multiple Register to Storage, System Register to Storage, Floating Point Register to Storage, Storage Immediate, and Storage to Storage instructions use address modification fields. When address modification is used, two words are appended to the instruction and contain a displacement to be added to a base register. Register to Storage instruction times assume that the destination is a register.
- For some of those instructions which have data or mode-dependent ranges, a minimum time is given, indicated by an (M) with the instruction times. The minimum time for arithmetic instructions does not include exception conditions such as divide or multiply by zero.
- No indirect addressing.
- No Storage Address Relocation Translator Feature installed.
- Additional qualifying remarks on the conditions used for calculating typical times appear as a note with each group of instructions as necessary.

Note. These times are to be used for planning purposes only. When the above assumptions are not applicable, refer to the appropriate processor manual for the formulas to calculate each instruction execution time.

Meaning of symbols

Immediate Count

Count in Register

- * indicates that there is an indirect version of machine mnemonic
- M indicates minimum time

		Execution Time In Nanoseconds	
Instruction Name SHIFTS	Mnemonic	4953	4955
<i>Note.</i> Shift instruction times use cour and SLTD instruction times assume a	0	· •	ctively. SLT
Shift Left Circular	SLC		
Immediate Count		6600	3080
Count in Register		6600	3080
Shift Left Logical	SLL		
Immediate Count		9600	3300
Count in Register		9600	3300
Shift Right Logical	SRL		
Immediate Count		7800	3080
Count in Register		7800	3080
Shift Right Arithmetic	SRA		
Immediate Count		8400	3080
Count in Register		8400	3080
Shift Left Circular Double	SLCD		
Immediate Count		15600	4620
Count in Register		15600	4620
Shift Left Logical Double	SLLD		

12000

12000

4840

4840

		Execution Time In Nanoseconds	
Instruction Name	Mnemonic	4953	4955
Shift Right Logical Double	SRLD		
Immediate Count		10200	4620
Count in Register		10200	4620
Shift Right Arithmetic Double	SRAD		
Immediate Count		10800	4620
Count in Register		10800	4620
Shift Left and Test	SLT	15000	7700
Shift Left and Test Double	SLTD	20400	7920
REGISTER TO REGISTER			
Reset Bits Word	RBTW	4200	1100
OR Word	OW	4200	1100
Subtract Carry Indicator	SCY	4800	1540
Exclusive OR Word	XW	4200	1100
Move Word	MVW	4200	1100
Compare Word	CW	4200	1100
Complement Register	CMR	4800	1320
Interchange Registers	IR	4800	1320
Add Word	AW	4200	1100
Add Word with Carry	AWCY	4800	1540
Subtract Word	SW	4200	1100
Subtract Word with Carry	SWCY	4800	1540
Add Carry Register	ACY	4800	1540
Invert Registers	VR	4800	1320
Copy Level Status Registers	CPSLR	6000	1100
Set Indicators	SEIND	6000	2420

PARAMETRIC INSTRUCTIONS

Note. The EN and DIS instruction times assume manipulation of the summary mask only. For the 4953, the LEX instruction time assumes execution on level 0, with level 1 pending.

Supervisor Call	SVC	24200	13420
Level Exit	LEX	15000	2860
Enable	EN	4800	2200
Disable	DIS	4600	2200
Stop	STOP	3600	1540
Diagnose	DIAG	7800 (M)	1980 (M)
Interchange Operand Keys	ЮРК	NA	1760

REGISTER IMMEDIATE

Note. The TWI instruction time assumes more than one bit is tested, at least one bit tested is a one, and not all bits are one.

Add Byte Immediate	ABI	4200	1100
Move Byte Immediate	MVBI	3600	880
Compare Byte Immediate	CBI	3600	1100
Add Word Immediate	AWI	5400	1540
Subtract Word Immediate	SWI	5400	1540
OR Word Immediate	OWI	5400	1540
Reset Bits Word Immediate	RBTWI	5400	1540
Exclusive OR Word Immediate	XŴI	5400	1540
Compare Word Immediate	CWI	5400	1540
Test Word Under Mask Immediate	TWI	5400	2200
AND Word Immediate	NWI	5400	1540
BRANCHING			
Jump on Condition	JC		
Jump on Equal	JE	6000	1320
Jump if Off	JOFF	6000	1320
Jump on Zero	JZ	6000	1320
Jump if Mixed	JMIX	6000	1320
Jump on Positive	JP	6000	1320
Jump if On	JON	6000	1320
Jump on Negative	JN	6000	1320
Jump on Even	JEV	6000	1320

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			n Time In seconds
Instruction Name	Mnemonic	4953	4955
Jump on Arithmetically			
Less Than	JLT	6000	1320
Jump on Arithmetically			
Less Than or Equal	JLE	6000	1320
Jump on Logically Less		(000	1220
Than or Equal	JLLE	6000	1320
Jump on Carry	JCY	6000	1320
Jump on Logically Less Than	JLLT	6000	1320
Jump on Not Condition	JNC	1200	1100
Jump on Not Equal	JNE	4200	1100
Jump if Not Off	JNOFF	4200 4200	1100 1100
Jump on Not Zero Jump on Not Mixed	JNZ JNMIX	4200	1100
Jump on Not Mixed	JNMIX	4200	1100
Jump if Not On	JNON	4200	1100
Jump on Not Negative	JNN	4200	1100
Jump on Not Even	JNEV	4200	1100
Jump on Arithmetically		.200	
Greater Than or Equal	JGE	4200	1100
Jump on Arithmetically	102		
Greater Than	JGT	4200	1100
Jump on Logically			
Greater Than	JLGT	4200	1100
Jump on Logically			
Greater Than or Equal	JLGE	4200	1100
Jump on No Carry	JNCY	4200	1100
Branch Indexed Short	BXS	4200	1320
Jump Unconditional	J	4200	880
No Operation	NOP	4200	880
Jump and Link	JAL	5400	1320
Branch and Link Short	BALS	5400	1980
Jump on Count	JCT	6600	1760
Branch on Condition	BC*	(000	15/0
Branch on Equal	BE	6000	1760
Branch if Off	BOFF	6000	1760
Branch on Zero	BZ	6000	1760
Branch on Positive	BP	6000	1760
Branch if Mixed	BMIX	6000	1760
Branch on Negative	BN	6000	1760
Branch if On Branch an Frank	BON	6000	1760 1760
Branch on Even	BEV	6000	1700
Branch on Arithmetically Less Than	BLT	6000	1760
Branch on Arithmetically	BLI	0000	1700
Less Than or Equal	BLE	6000	1760
Branch on Logically Less	DEL	0000	1700
Than or Equal	BLLE	6000	1760
Branch on Carry	BCY	6000	1760
Branch on Logically Less Than	BLLT	6000	1760
Branch on Not Condition	BNC*		
Branch on Not Equal	BNE	4200	1540
Branch on Not Zero	BNZ	4200	1540
Branch if Not Off	BNOFF	4200	1540
Branch on Not Positive	BNP	4200	1540
Branch on Not Mixed	BNMIX	4200	1540
Branch on Not Negative	BNN	4200	1540
Branch if Not On	BNON	4200	1540
Branch on Not Even	BNEV	4200	1540
Branch on Arithmetically			
Greater Than or Equal	BGE	4200	1540
Branch on Arithmetically	- 97	1000	
Greater Than	BGT	4200	1540

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		Execution Time In Nanoseconds	
Instruction Name	Mnemonic	4953	4955
Branch on Logically			
Greater Than	BLGT	4200	1540
Branch on Logically			
Greater Than or Equal	BLGE	4200	1540
Branch on No Carry	BNCY	4200	1540
Branch Unconditional Branch External	B*	4800	1760
Branch and Link	BX BAL*	4800 6600	1760 1980
Branch and Link External	BALX	6600	1980
Branch on Condition Code	BCC*	6000	1760
Branch on Not Error	BNER	6000	1760
Branch on Not Condition Code	BNCC*	4200	1540
Branch on Error	BER	4200	1540
Branch on Overflow Branch on Not Overflow	BOV* BNOV*	5400 3600	1760 1540
	DINOV	3000	1340
REGISTER TO STORAGE SHORT			
Move Word Short	MVWS*	5400	2420
SINGLE BIT MANIPULATION			
Note. Single Bit Manipulation instruction times a	ssume that the tested bin	t is bit number 2	or 3.
Test Bit	ТВТ	8400	4840
Test Bit and Set On	TBTS	9600	6500
Test Bit and Reset	TBTR	9600	6720
Test Bit and Invert	TBTV	9600	6500
REGISTER TO STORAGE			
Move Byte	MVB	11400	2860
OR Byte	OB	12000	2640
Reset Bits Byte	RBTB	12000	2640
Exclusive OR Byte	XB	12000	2644
Compare Byte	CB	11400	2640
Move Byte and Zero	MVBZ	12000	3740
Add Byte Subtract Byte	AB SB	13800 13800	2640 2640
Move Word	MVW	8400	2640
OR Word	OW	8400	2640
Reset Bits Word	RBTW	9000	2640
Exclusive OR Word	XW	8400	2640
Compare Word	CW	9000	2640
Move Word and Zero	MVWZ	9400	3520
Add Word Subtract Word	AW SW	8400 9000	2640 2640
Move Double Word	MVD	10800	3520
OR Double Word	OD	10800	4400
Reset Bits Double Word	RBTD	11200	4400
Exclusive OR Double Word	XD	11400	4400
Compare Double Word	CD .	11400	3520
Move Double Word and Zero	MVDZ	12800	4840
Add Double Word Subtract Double Word	AD SD	11400 12000	4400 4400
Move Word Immediate	MVWI	8400	3300
Move Address	MVA	8400	3300
Push Byte	PSB	13800	6160
Pop Byte	PB	14400	6380
Multiply Byte	MB	15000 (M)	11660 (M)
Divide Byte Push Word	DB PSW	16200 (M)	18260 (M)
Push Word Pop Word	PSW PW	13000 12400	6160 6380
Multiply Word	MW	13200 (M)	10780 (M)
Divide Word	DW	15600 (M)	17160 (M)
Push Double Word	PSD	14200	6600
Pop Double Word	PD	13600	6820

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Instruction Name		Execution Time In Nanoseconds	
	Mnemonic	<i>4953</i>	4955
Multiply Double Word	MD	13200 (M)	38260 (M)
Divide Double Word	DD	22200 (M)	41580 (M)
REGISTER TO STORAGE (LONG)			
Move Word	MVW*	7200	2420
OR Word	OW*	7200	2420
Reset Bits Word	RBTW*	7200	2420
Exclusive OR Word	XW*	7200	2420
Operate I/O	IO*	8800 (M)	4400 (M)
Add Word	AW*	7200	2420
Subtract Word	SW*	7800	2640

MULTIPLE REGISTER TO STORAGE

Note. Multiple Register to Storage instruction times assume 5 General Purpose Registers are loaded and stored.

Load Multiple and Branch	LMB	32400	11440
Store Multiple	STM	36500	14080

SYSTEM REGISTER TO STORAGE (PRIVILEGED)

Note. The SELB Instruction time assumes the In-process Flag and Trace are off, and Summary Mask is on. The SELB and CPLB times assume the selected level is equal to the current level. For 4953, SELB time assumes execution on level zero, with level 1 pending.

Set Address Key Register	SEAKR	NA	3080
Set Instruction Space Key	SEISK	NA	3080
Set Operand 1 Key	SEOOK	NA	3080
Set Operand 2 Key	SEOTK	NA	3080
Set Interrupt Mask Register	SEIMR	10200	3300
Set Segmentation Register	SESR	NA	3740
Set Storage Key	SESK	NA	5720
Set Level Status Block	SELB	37000	12540
Copy Address Key Register	CPAKR	NA	4180
Copy Instruction Space Key	CPISK	NA	4180
Copy Operand 1 Key	CPOOK	NA	4180
Copy Operand 2 Key	CPOTK	NA	4180
Copy In-Process Flags	CPIPF	12600	3520
Copy Processor Status and Reset	CPPSR	9000	3520
Copy Interrupt Mask Register	CPIMR	9200	3300
Copy Segmentation Register	CPSR	NA	3960
Copy Storage Key	CPSK	NA	4620
Copy Level Block	CPLB	25200	11880
FLOATING POINT			
Floating Move	FMV	NA	7760
Floating Move Double	FMVD	NA	8140
Floating Move and Convert	FMVC	NA	9900 (M)
Floating Move and Convert Double	FMVCD	NA	12980 (M)
Floating Add	FA	NA	11220 (M)
Floating Add Double	FAD	NA	12100 (M)
Floating Subtract	FS	NA	11220 (M)
Floating Subtract Double	FSD	NA	12100 (M)
Floating Multiply	FM	NA	22220 (M)
Floating Multiply Double	FMD	NA	30140 (M)
Floating Divide	FD	NA	29480 (M)
Floating Divide Double	FDD	NA	54780 (M)
Floating Compare	FC	NA	6820 (M)
Floating Compare Double	FCD	NA	7040 (M)
Set Floating Level Block	SEFLB	NA	16060 (M)
Copy Floating Level Block	CPFLB	NA	19580 (M)
			S/

Instruction Name		Execution Time In Nanoseconds	
	Mnemonic	4953	4955
VFL BYTE OPERATIONS			
<i>Note.</i> CT is the count of the last byte me each value in this group of instructions. F group of instructions.	-		
Fill Byte Field and Decrement	FFD	3600CT	1980CT
Fill Byte Field and Increment	FFN	3600CT	1980CT
Move Byte Field and Decrement	MVFD	5400CT	2420CT
Move Byte Field and Increment	MVFN	5400CT	2420CT
Compare Byte Field Not Equal			
and Decrement	CFNED	7800CT	3300CT
Compare Byte Field Not Equal			
and Increment	CFNEN	7800CT	3300CT
Scan Byte Field Not Equal			
and Decrement	SFNED	5400CT	2680CT
Scan Byte Field Not Equal			
and Increment	SFNEN	5400CT	2680CT
Compare Byte Field Equal			
and Decrement	CFED	7800CT	3300CT
Compare Byte Field Equal			
and Increment	CFEN	7800CT	3300CT
Scan Byte Field Equal and			
Decrement	SFED	5400CT	2680CT
Scan Byte Field Equal and			
Increment	SFEN	5400CT	2680CT

STORAGE IMMEDIATE

Note. The TWI instruction time assumes more than one bit is tested, at least one bit tested is one, and not all bits tested are one.

and not an ons tested are one.				
OR Word Immediate	OWI	6600	4620	
Reset Bits Word Immediate	RBTWI	6600	4620	
Compare Word Immediate	CWI	5800	4180	
Move Word Immediate	MVWI	5400	4180	
Move Address	MVA	5400	4180	
Add Word Immediate	AWI	6600	4840	
Subtract Word Immediate	SWI	6600	4620	
Test Word Under Mask Immediate	TWI	7000	4400	
STORAGE TO STORAGE				
Move Byte	MVB	12600	5060	
OR Byte	OB	15000	5280	
Reset Bits Byte	RBTB	15200	5280	
Compare Byte	CB	14400	4400	
Move Word	MVW	12000	5060	
OR Word	OW	13200	5280	
Reset Bits Word	RBTW	13800	5280	
Compare Word	CW	13000	4400	
Move Double Word	MVD	15600	6380	
OR Double Word	OD	17000	7260	
Reset Bits Double Word	RBTD	17000	7260	
Compare Double Word	CD	17000	6160	
Add Word	AW	14000	5060	
Subtract Word	SW	14000	5060	
Add Double Word	AD	18400	8140	
Subtract Double Word	SD	18400	8140	
SYSTEM REGISTER TO REGISTER (PR	NVILEGED)			
Copy Address Key Register	CPAKR	NA	2200	
Copy Instruction Space Key	CPISK	NA	2200	
Copy Operand 1 Key	CPOOK	NA	2200	
Copy Operand 2 Key	CPOTK	NA	2200	

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Instruction Name		Execution Time In Nanoseconds	
	Mnemonic	<i>4953</i>	4955
Set Address Key Register	SEAKR	NA	1760
Set Instruction Space Key	SEISK	NA	1760
Set Operand 1 Key	SEOOK	NA	1760
Set Operand 2 Key	SEOTK	NA	1760
Copy Current Level	CPCL	5400	1540
Set Console Data Lights	SECON	5400	1540
Copy Console Data Buffer	CPCON	4800	1540

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Note. Conditional Jump and Branch instructions having true and complement forms for testing of a condition have times listed for both cases of a Jump (or Branch) being taken or not taken. One time appears with true condition testing form of the instruction; the other with the complement form. The JCT instruction time assumes the count is greater than one.

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Appendix B. Series/1 Hardware

The symbol # precedes all feature numbers. All other numbers are IBM machine types.

Number Name

PROCESSORS

- 4953-A Processor Unit, 16K Bytes (64K max), 4 I/O feature locations
- 4953-B Processor Unit, 16K Bytes (64K max), 13 I/O feature locations
- 4953-C Processor Unit, 32K Bytes (64K max), 4 I/O feature locations 4953-D Processor Unit, 32K Bytes (64K max), 13 I/O feature locations
- 4955-A Processor Unit, 16K Bytes (64K max), 8 I/O feature locations
- 4955-В Processor Unit, 16K Bytes (128K max), 3 I/O feature locations 4955-C
- Processor Unit, 32K Bytes (64K max), 10 I/O feature locations
- 4955-D Processor Unit, 32K Bytes (128K max), 7 I/O feature locations

PROCESSOR FEATURES

- #5650 **Programmer** Console
- Storage Address Relocation Translator (4955 only) #6335
- #3920 Floating Point (4955 only)

STORAGE ADDITIONS

- #6315 Storage Addition, 16K Bytes (4953 only)
- #6316 Storage Addition, 32K Bytes (4953 only)
- #6325 Storage Addition, 16K Bytes (4955 only)
- #6326 Storage Addition, 32K Bytes (4955 only)

USER ATTACHMENT FEATURES

- #7840 Timers (2 per card)
- #7850 Teletypewriter Adapter
- #5430 Customer Direct Program Control Adapter
- #1560 Integrated Digital Input/Output Non-Isolated (32 DI/32 DO points)
- #1565 Channel Repower
- #1595 Channel Socket Adapter
- **Customer Access Panel** #1590

DATA PROCESSING I/O

- 4962-1 Disk Storage Unit, 9.3M bytes (without fixed heads)
- 4962-1F Disk Storage Unit, 9.3M bytes (with fixed heads)
- 4962-2 Disk Storage Unit, 9.3M bytes (without fixed heads with diskette drive)
- 4962-2F Disk Storage Unit, 9.3M bytes (with fixed heads with diskette drive)
- #3580 4962 Disk Storage Unit Attachment
- 4964-1 Diskette Unit
- 4964 Diskette Unit Attachment #3581
- 4973-1 Line Printer Unit (150 lines/minute)
- 4973-2 Line Printer Unit (400 lines/minute)
- 4973 Line Printer Attachment #5630
- 4974-1 Printer Unit (120 characters/second)
- #5620 4974 Printer Attachment
- 4979-1 **Display Station**
- #3585 4979 Display Station Attachment

Number Name

SENSOR I/O

- 4982-1 Sensor I/O Unit (capacity for up to 8 sensor I/O cards)
- #6305 4982 Sensor I/O Unit Attachment
- #3525 Digital Input/Process Interrupt Non-Isolated (16 points)
- #3530 Digital Input/Process Interrupt Isolated (16 points)
- #3535 Digital Output Non-Isolated (16 points)
- #1060 Analog Input Control
- #1070 Amplifier Multirange
- #4940 Multiplexer-Reed Relay (8 channels)
- #4950 Multiplexer-Solid State (16 channels)
- #1065 Analog Output (2 points)

COMMUNICATIONS

- #1610 Asynchronous Communications Single Line Control (9,600 BPS)
- #2074 Binary Synchronous Communications Single Line Control (9,600 BPS)
- #2075 Binary Synchronous Communications Single Line Control/High Speed (56,000 BPS)
- #2090 Synchronous Data Link Communications Single Line Control (9,600 BPS)
- #2091 Asynchronous Communications 8-Line Control
- #2092 Asynchronous Communications 4-Line Adapter
- #2093 Binary Synchronous Communications 8-Line Control
- #2094 Binary Synchronous Communications 4-Line Adapter
- #2000 Communications Indicator Panel
- #2010 Communications Power

SYSTEM SUPPORT

- 4959-A I/O Expansion Unit
- 4999-1 Battery Backup Unit (for 100–123.5 volt ac systems)
- 4999-2 Battery Backup Unit (for 200–235 volt ac systems)
- 4997-1A Rack Enclosure Unit 1 metre high (plain filler panels)
- 4997-1B Rack Enclosure Unit 1 metre high (decorative filler panels)
- 4997-2A Rack Enclosure Unit 1.8 metre high (plain filler panels)
- 4997-2B Rack Enclosure Unit 1.8 metre high (decorative filler panels)
- #4540 Rack mounting fix ture

This is only a partial list; additional features, such as cables, are listed in the Series/1 Configurator and in the Series/1 Installation Manual-Physical Planning. The order numbers for these manuals are listed in the "Preface".

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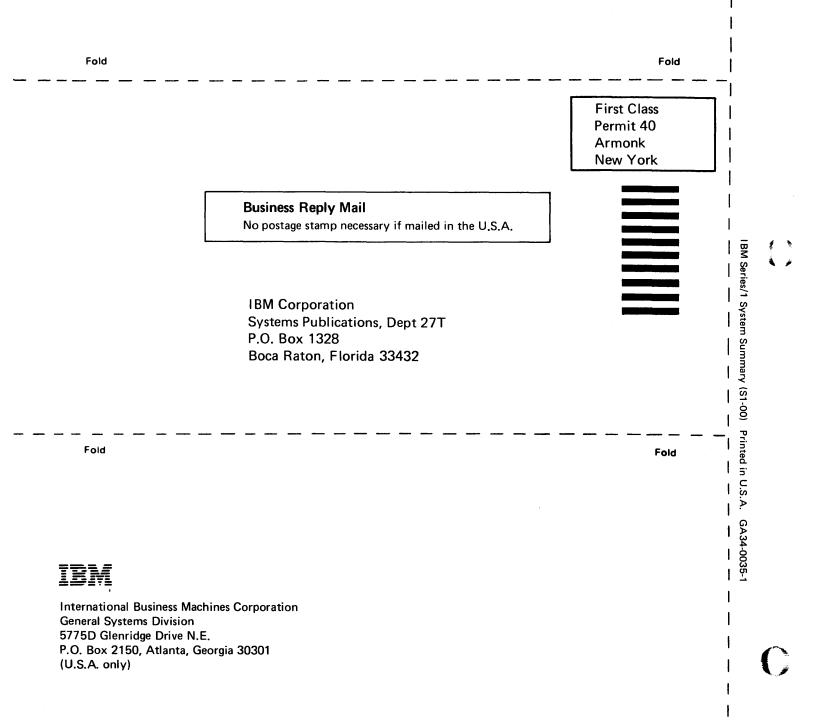
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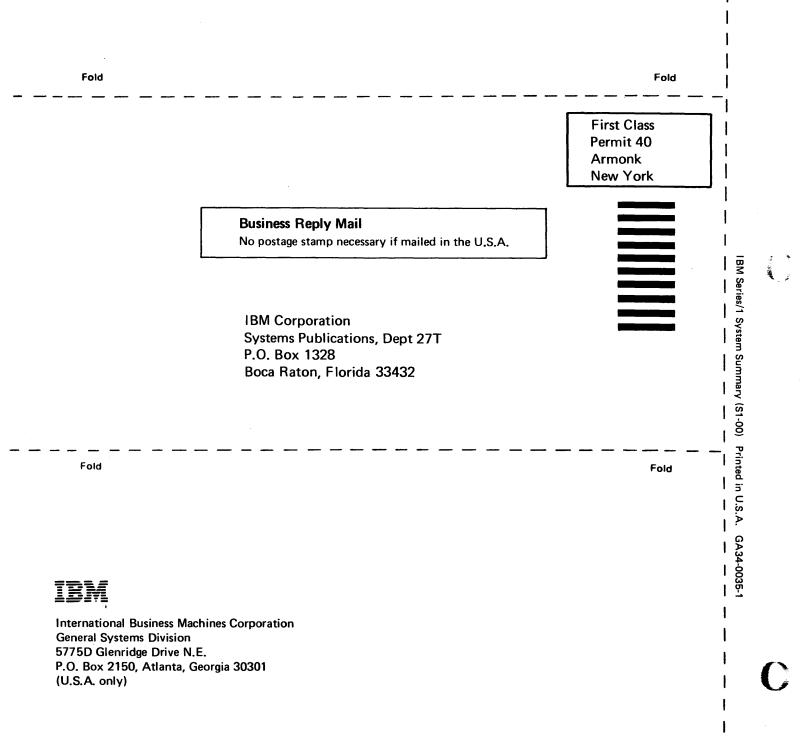
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