IBM

Series/1

GA34-0227-1

File No. S1-16

IBM Series/1
4967 Disk Unit Subsystem and Attachment Feature Description

IBM

Series/1

GA34-0227-1

File No. S1-16

IBM Series/1
4967 Disk Unit Subsystem and Attachment Feature Description

Second Edition (June 1986)

This is a major revision of, and obsoletes, GA34-0227-0. Due to the many changes and additons, this manual should be read in its entirety.

Use this publication only for the purpose stated in the Preface.

Changes are periodically made to the information herein; any such changes will be reported in subsequent revisions or Technical Newsletters.

It is possible that this material may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Publications are not stocked at the address given below. Requests for copies of IBM publications should be made to your IBM representative or the IBM branch office serving your locality.

This publication could contain technical inaccuracies or typographical errors. A form for readers' comments is provided at the back of this publication. If the form has been removed, address your comments to IBM Corporation, Information Development, Department 28E, Internal Zip 1803, P.O. Box 1328, Boca Raton, Florida 33429-1328. IBM may use or distribute any of the information you supply in any way it believes appropriate without incurring any obligation whatsoever. You may, of course, continue to use the information you supply.

Preface

This publication describes the Series/1 4967 High-Performance Disk Subsystem and Attachment Feature. The information in this publication is intended for assembler language programmers who need to create or modify programs written for the 4967 High-Performance Disk Subsystem. The reader should understand data processing terminology and stored-program concepts.

The subject matter is presented in two chapters:

- Chapter 1, "Introduction," describes the 4967 High-Performance Disk Subsystem and Attachment Feature.
- Chapter 2, "Operations," describes the Series/1 machine-level language the processor uses to transfer data to and from the attachment card. Chapter 2 also gives information about status, error recovery, and initial program load.

Prerequisite Publications

- *IBM Series/1 Principles Of Operation*, GA34-0152
- For processor information, refer to the applicable processor and processor features description manual.

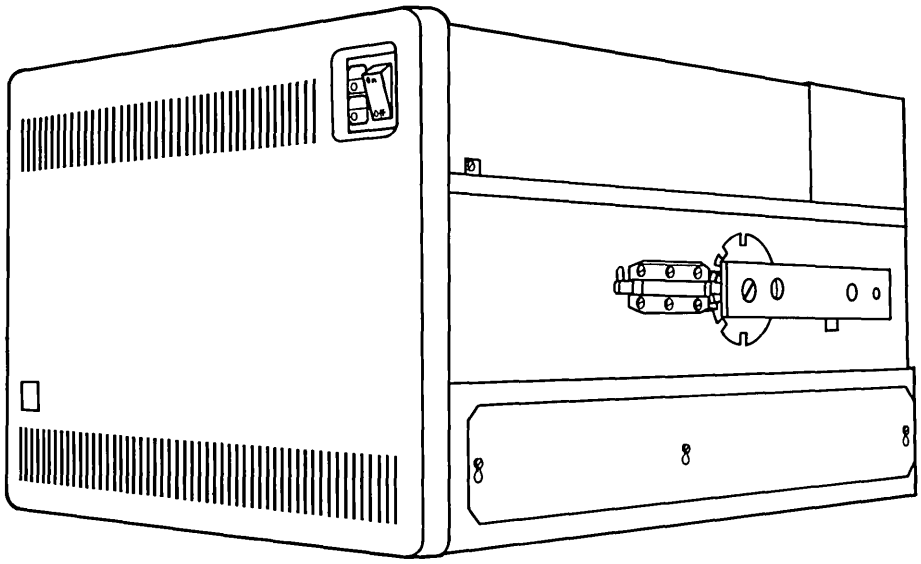
Related Publications

- *IBM Series/1 Installation Manual — Physical Planning*, GA34-0029
- *IBM Series/1 Operator's Guide*, GA34-0039
- *IBM Series/1 Customer Site Preparation Manual*, GA34-0050

Contents

Chapter 1. Introduction

The IBM Series/1 4967 High-Performance Disk Subsystem and Attachment Feature consists of one to four disk units and one attachment feature card.



Models

There are four models of the 4967 disk unit: Models 2CA, 2CB, 3CA, and 3CB. The 2CA and 3CA models are the primary disk units. The 2CB and 3CB are expansion units. The following tables list the model numbers, differences, and associated specifications:

Disk storage units

Model	*Capacity*
2CA	200 megabytes with controller
2CB	200 megabytes
3CA	358.9 megabytes with controller
3CB	358.9 megabytes

Disk specifications

Access times	
Latency	10.1 milliseconds
Average access time	25 milliseconds
Track to track access time	9.0 milliseconds
Data transfer rate	1.5 megabytes/second (instantaneous)
Transferred from disk to storage (Note 1)	600 kilobytes/second (worst case)
Disk rotation speed	2964 revolutions per minute
Bytes per record	256
Records per sector	2
Sectors per track	49 (usable) 1 (spare)
Data bytes per track	25,088 (user data)
Total data tracks accessible per head (cylinders)	572 (2CA and 2CB) 1024 (3CA and 3CB)
Tracks per cylinder (heads)	14

Note: The effective data rate is the average time needed to read or write 1372 records within a cylinder. This rate depends upon the processor model and cache storage performance. The rates listed in the specification table use a Series/1 4955 model F processor. Cache storage performance depends upon the user application. (See "Cache Storage").

Attachment Card

The attachment card is a cycle-steal device that controls up to four disk storage units.

The attachment has the following features:

- Interprets the Operate I/O instruction's immediate device control block (IDCB)
- Processes the IDCB command
- Reads the device control block (DCB) specified by the cycle-steal IDCB, in cycle-steal mode
- Starts and stops cycle-steal data transfers
- Monitors and checks accuracy of all data transfers
- Furnishes status information, reports condition codes, and presents interrupt requests to the processor
- Performs automatic error-recovery procedures
- Provides for alternate sector processing automatically
- Provides for variable-length IPL records, up to 65,536 bytes
- Provides attachment circuit testing with or without disconnecting the attachment-to-disk-unit control cables
- Optimizes data transfers when instructions are issued to more than one disk unit
- Optimizes disk throughput by allowing seek overlaps with read or write operations
- Provides an attachment maintained error log
- Provides cache storage of 384K-bytes.

Common Adapter

The common adapter consists of two cards mounted in the primary disk unit. It provides the interface between the disk unit(s) and the attachment card.

Cache Storage

Cache storage consists of a microprocessor and 384K-bytes of storage that reduces access time for applications with heavy, non-random disk use. Cache storage is organized in 2K-byte pages.

The cache storage algorithm selects data sectors that are probable candidates for system read requests and pre-fetches these sectors into cache storage. During write operations, data is placed into cache storage after it is written to the disk. As a result, many disk requests are satisfied with data contained in cache storage, eliminating mechanical access delays. Applications that are primarily write-oriented or random in disk usage may experience little or no improvement. Cache storage functions are transparent to the programmer.

Factors increasing cache storage effectiveness include:

1. High read/write ratio.

2. Sequential or proximity read operations.

3. Frequent reference type usage of data within a relatively limited area (indexes, for example).

Cache storage updates its contents as requests from different areas of the disk are needed.

Chapter 2. Operations

This chapter describes the commands, operations, condition codes, cycle-steal status words, and recommended error recovery procedures.

Device Addressing

Restrictions are placed on the 4967 Disk Unit addresses used for various disk unit configurations. If one or two disk units are attached, the first disk unit low-order address bit must be 0. The second disk unit address is sequential to the first.

When three or four disk units are attached, the first disk unit low order two bits must be 0. The remaining units addresses are sequential to the first.

Direct Program Control (DPC)

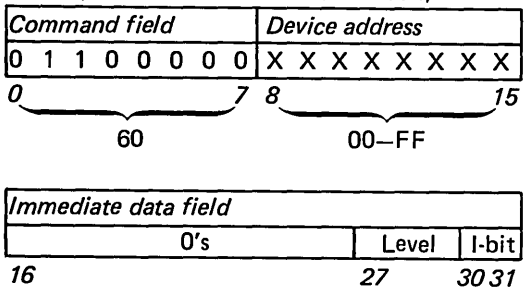
The DPC commands and hexadecimal codes follow:

- Prepare (60)
- Device Reset (6F)
- Read Device ID (20)
- Attachment Storage Diagnostic (4E)
- Attachment General Diagnostic (41)
- Attachment Cache Diagnostic (42)
- Load Seek Required Address Direct (52)
- Load Seek Control Direct (53)
- Sense Disk Unit Direct (54)
- Diagnostic Reset Common Adapter (4F)
- Write Cache Control (45)
- Enable Data Collection Mode (4C)
- Clear Error Log (43)
- Load Diagnostic Word 1 (48)
- Load Diagnostic Word 2 (49).

Prepare

The immediate device control block (IDCB) format for the Prepare command follows:

IDCB (immediate device control block)

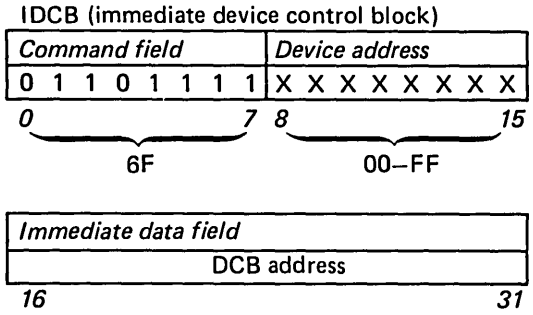


Before using any command that generates an interrupt, issue the Prepare command to the attachment card. The Prepare command loads the interrupt level and I-bit into the specified disk unit. The I-bit (31) determines if the disk unit can report interrupt requests. If the I-bit is set to 1, the disk unit presents interrupt requests on the level defined by the level bit field (27–30). If the I-bit is set to 0, the disk unit cannot present interrupt requests. All disk units attached to the attachment card are assigned to the same interrupt level. However, a separate interrupt I-bit is provided for each disk unit so that each unit's I-bit may be prepared. All disk units interrupt on the same level assigned to the disk unit that last received a Prepare command.

The attachment card is interrupt pending for the particular disk unit until the I-bit is set to 1 and the processor services the interrupt, or until a Device Reset, Halt I/O, System reset, or Power-on reset occurs.

Device Reset

The format of the IDCB for a Device Reset command follows:

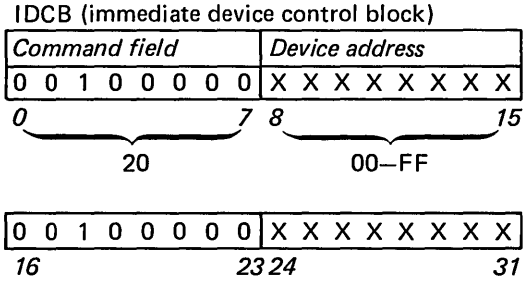


The Device Reset command resets all pending interrupts and all previously established control and status conditions for the specified device address. This command does not reset the 4967 disk unit ID, device address, and prepare registers. The attachment card is always able to accept and carry out this command even if it is busy or an interrupt is pending from a previous command.

Read Device ID

The format of the IDCB for the Read Device ID command follows:

IDCB (immediate device control block)



The Read Device ID command transfers the identification (ID) word from the attachment card to the immediate data field of the IDCB. After command processing, the immediate data field contains the following:

Bits 16-19 Define a class code of 3, which represents a multi-device attachment with a controller and a configurable domain size.

Bit 20 Not used; must be 0.

Bits 21-23 Base address divisibility code where:

21	22	23	Means
0	0	1	BA divisibility of 2
0	1	0	BA divisibility of 4

Bits 24-29 4967 assigned code (000101)

Bit 30 A cycle-stealing device (binary 1).

Bit 31 An IBM device (binary 0).

An even address assignment is used for the attachment card. The jumper pin configuration on the attachment card prevents an odd address assignment for the base address.

The attachment ID is jumpered on the attachment card during installation to reflect the existing configuration. Consider the following example on how to determine if three disk units are installed. Assume that the first device address is 8. A Read Device ID command to device address 8 yields 3216, which indicates a base address divisibility code of four (bits 21–23) and a 4967 is attached (bits 24–29). A second Read Device ID command must then be issued to base address plus 3 or, in this case, to base address 11. Because the fourth disk unit in this example is not attached, a condition code of 0 is presented. If a fourth disk unit is attached, the condition code is not 0.

As another example, assume that two disk units are attached and a Read Device ID command issued to the base device address 6 contains 3116 in the immediate data field. This indicates a base address divisibility code of 2 and that a 4967 is attached. A second Read Device ID is now issued to base address plus 1, or, in this case, 7. Since a second disk unit is attached, the condition code is not 0.

Note: In the case of base address divisibility 4, the base address increment is 3. For base address divisibility 2, the base address increment is 1.

Attachment Storage Diagnostic

The IDCB for the Attachment Storage Diagnostic command follows:

IDCB (immediate device control block)

Command field	*Device address*
0 1 0 0 1 1 1 0	X X X X X X X X
0 *7*	*8* *15*
4E	00–FF

Immediate data field
Immediate data
16 *31*

This command instructs the attachment card to run an attachment storage diagnostic test. Any detected failure in the attachment storage is reported as an exception interrupt with status available. The attachment equipment check bit (bit 10) in cycle-steal status word 4 is set to 1 if an error occurs. The immediate data word of the Write Immediate command is not used, but is checked for parity. A normal device end interrupt indicates a successful attachment storage check.

Attachment General Diagnostic

The IDCB for the Attachment General Diagnostic command follows:

IDCB (immediate device control block)

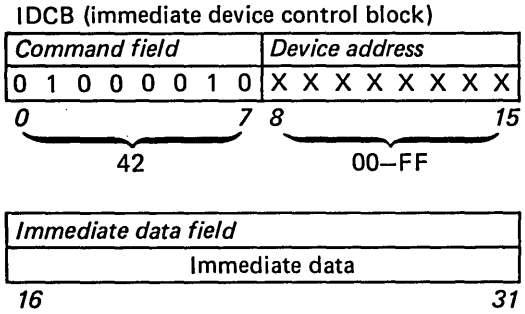
Command field	*Device address*
0 1 0 0 0 0 0 1	X X X X X X X X
0 *7*	*8* *15*
41	00–FF

Immediate data field
Immediate data
16 *31*

This command causes the attachment card to test its data registers and control latches. Any failure causes an exception interrupt with the attachment equipment check bit (10) set to 1 in cycle-steal status word 4. The IDCB immediate data word is not used and should be 0's.

Attachment Cache Diagnostic command

The IDCB for the Attachment Cache Diagnostic follows:



This command causes the attachment card to test and initialize the cache storage. The IDCB immediate data word is not used and should be 0's.

A defective cache storage location disables the associated 2K-byte page. The number of pages disabled is found in cycle-steal status word 13, bits 3–7. If this test detects more than 20 disabled cache pages, the equipment check bit is set to 1 and interrupt condition code 2 (CC2) is returned.

The cache status is saved in cycle-steal status word 6, bits 5-7:

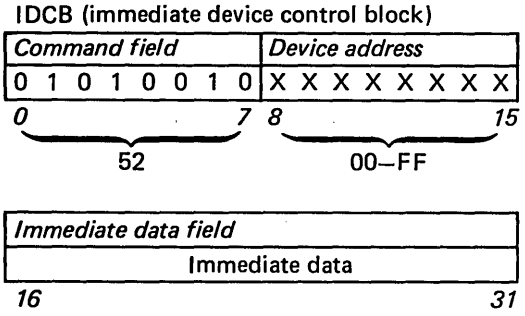
Bit 5 - Module 1 or 2 has one or more disabled pages
Bit 6 - Module 3 or 4 has one or more disabled pages
Bit 7 - Module 5 or 6 has one or more disabled pages

Note: There may be cases where the equipment check bit is set to 1 and no cache pages have been disabled. This condition may indicate defective cache storage support hardware and this hardware can also incorrectly flag a cache page.

The attachment card can disable up to 20 cache pages while the system is running, during power-on diagnostics, or by this test without degrading cache storage performance.

Load Seek Required Address Direct

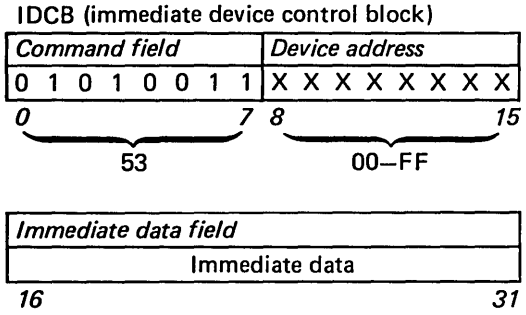
The IDCB for the Load Seek Address Direct command follows:



This command is used with the Load Seek Control Direct command to perform special diagnostic wrap functions. For a description of this command, see the Load Seek Control Direct command.

Load Seek Control Direct

The IDCB for the Load Seek Control Direct command follows:



This command performs special diagnostic wrap functions for the disk unit and must be issued following a Load Seek Required Address Direct command. This sequence of commands transfers the file control block (FCB) word 5 (access control word) from the common adapter to the disk unit controls. The FCB for the selected disk unit must be loaded before issuing these commands (see Load FCB Diagnostic). The definition of bits used in FCB word 5 follows:

FCB Word 5	If bit is 0:	If bit is 1:
0	0	Recal.
1	Reserved	Hd Off In
2	Hd Sel 8	Hd Off Out
3	Hd Sel 4	Reserved
4	Hd Sel 2	Reserved
5	Hd Sel 1	Diag Cmd
6	Cyl 512	DC Rst
7	Cyl 256	Not used
8	Cyl 128	Not used
9	Cyl 64	Not used
10	Cyl 32	Not used
11	Cyl 16	Not used
12	Cyl 8	Not used
13	Cyl 4	Not used
14	Cyl 2	Not used
15	Cyl 1	

We recommend the following procedure for issuing the commands and responses:

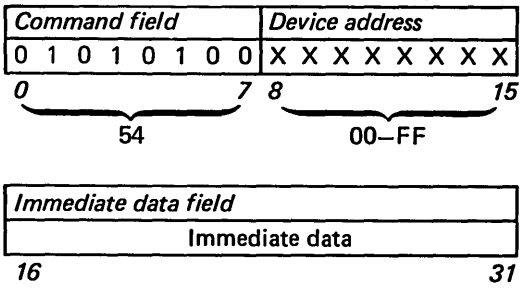
1. Issue the Load Seek Required Address Direct command. Processing this command loads the right-hand byte (cylinder address bits 1 to 128) directly to the selected disk unit. It provides a means of directly loading the required address register for diagnostic use. An interrupt is presented when this command completes.

2. Issue the Load Seek Control Direct command. This command transmits the high-order bit of the cylinder number and the head select byte to the selected disk unit. If data bit 0 is set to 0, a seek and head selection cycle begins. If data bit 0 is set to 1, the disk unit performs diagnostic functions. An interrupt is presented when this operation completes.

Sense Disk Unit Direct

The IDCB for this command follows:

IDCB (immediate device control block)

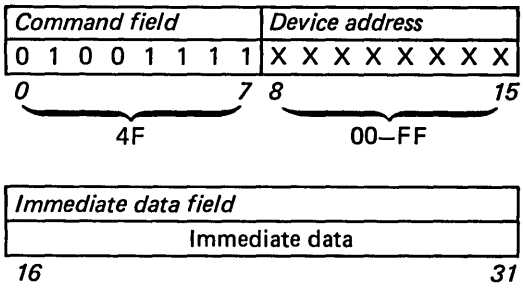


This command fetches the sense byte from the selected disk unit. An interrupt is presented when this command completes. The sense data is placed in the low order byte of the disk status word of the FCB. To read the word into main storage, issue a Start Cycle-Steal Status command. The IDCB immediate data word is not used and should be 0's. Word 5, bits 8–15 contain the sense byte.

Diagnostic Reset Common Adapter

The IDCB for the Diagnostic Reset Common Adapter follows:

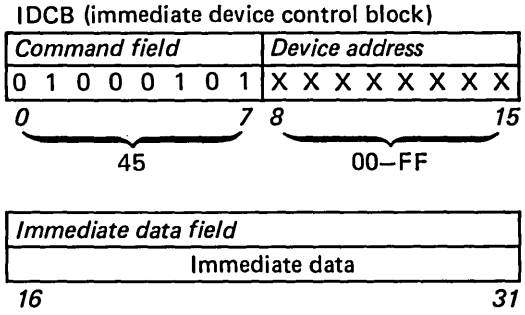
IDCB (immediate device control block)



This diagnostic command resets the disk unit controls. All disk unit operations in progress end. However, they may end with unpredictable results. Therefore, use this command for diagnostic purposes only. The IDCB immediate data word is not used and should be 0's.

Write Cache Control

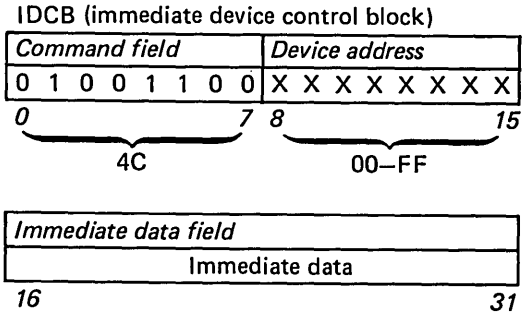
The IDCB for the Write Cache Control command follows:



This command causes the attachment card to check the immediate data portion of the IDCB and then take the correct action. When the immediate data word is 0, the attachment card sets an indicator that makes the cache storage not available. If the immediate data word contains something other than 0, the indicator is set to make the cache storage available. A System Reset, Halt I/O, or power-on reset enables cache storage.

Enable Data Collection Mode

The IDCB for the Enable Data Collection Mode command follows:



Use this command to enable the statistical data collection into cache storage. However, cache storage must be disabled before issuing this command or a delayed command reject results. When data collection mode is enabled, information concerning each subsequent read or write operation to a disk unit is stored in the cache storage. The IDCB immediate data word is not used and should be 0's.

All commands sent to the disk unit, such as Read and Write, during data collection mode stores the following 22 bytes into cache storage at the next sequential cache storage address:

Bytes	Description
3	Time stamp #1 (time operation issued to disk)
2	Address of DCB
2	DCB command word (word 0)
3	DCB RBA (right adjusted)
2	DCB record count (word 3, bits 4-15)
2	DCB byte count (word 6)
2	DCB data address (word 7)
1	Interrupt information byte/interrupt status byte
1	Interrupt condition code (right adjusted)
1	Disk # (two bits, right adjusted)
3	Time stamp #2 (time of interrupt to system)

Notes:

1. The time stamp is a three-byte binary count used only as an approximate indication of the time taken between and during operations.

2. The attachment card continuously increases the count until it wraps back to 0. The time required to wrap the count is approximately two hours.

3. To find the approximate duration of that operation, including seek, rotational latency, and data transfer time, subtract time stamp #1 from time stamp #2.

4. Each time stamp count represents about 400 microseconds.

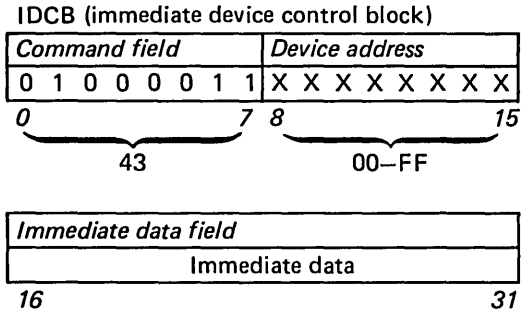
5. If many operations are being performed at the same time, the time stamp may be very inaccurate.

When cache storage is full, data collection stops. To read the collected data back into the system for analysis, use the Read Cache Diagnostic command. Since cache storage is disabled for disk data use during this operation, all read and write operations proceed without the cache storage. Disk unit performance is reduced. System Reset, power-on reset, Halt I/O, and the Write Cache Control command, which enables cache, end data collection mode.

To find out how much data was collected, use the Read Attachment Definition command.

Clear Error Log

The IDCB for the Clear Error Log command follows:

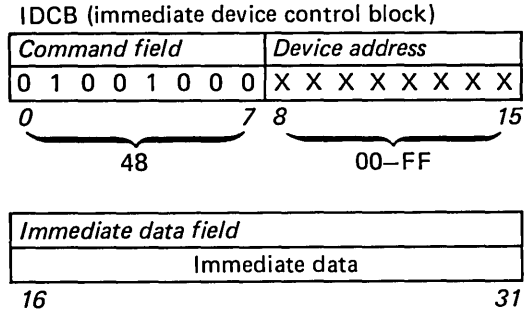


Use this command to clear the attachment error log after a series of diagnostic commands that left false errors in the log or after the log has been dumped. The IDCB immediate data word is not used and should be 0's.

> **Note:** For information about reading the error log, see the Read Attachment Storage command.

Load Diagnostic Word 1

The IDCB for the Load Diagnostic Word 1 command follows:



This command loads the immediate data word into the data buffer register in the common adapter (located in the base disk unit).

Load Diagnostic Word 2

The IDCB for the Load Diagnostic Word 2 command follows:

IDCB (immediate device control block)

Command field	*Device address*
0 1 0 0 1 0 0 1	X X X X X X X X
0 *7*	*8* *15*
49	00—FF

Immediate data field
Immediate data
16 *31*

This command allows operation of the disk unit controls and the disk unit interface in a single-cycle mode for diagnostic purposes. The diagnostic register is loaded with the immediate data word of the DPC command.

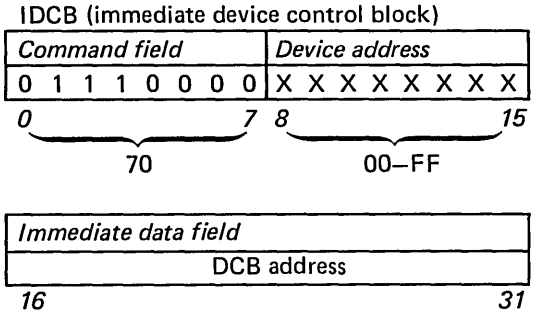
Cycle-Steal Commands

Command processing in cycle-steal mode permits overlapping a disk operation with processor operations and other I/O operations.

Begin all cycle-steal operations with an Operate I/O instruction. This instruction points to an eight-word device control block (DCB) that contains the information needed to perform the cycle-steal operation.

Start Command

The IDCB for the Start command follows:



The Operate I/O instruction references an IDCB containing the Start command and an address pointing to the device control block (DCB). The DCB contains the information needed to perform a cycle-steal operation. On a Start command, the attachment card fetches the DCB, checks for parity, and forces a cycle-steal address key of hex 000.

Start Command Operations

The following table summarizes the possible disk unit operations using Start Cycle-Steal commands. These commands must have the IDCB command field encoded with the binary value hex 70.

Start command operations

Operation type	Function IDCB CMD FLD=01110000 DCB cntrl word bit 2 (I/F)		DCB device dependent field 8 9 10 11 12 13 14 15
Control	Recalibrate	0	0 0 0 0 0 0 0 1
Read	Read data	1	D 0 0 1 0 0 0 0
	Read verify	0	D 0 0 1 0 0 0 1
	Read data repeat	1	0 0 0 1 0 0 1 0
	Read ID	1	0 0 0 1 0 1 0 0
	Read disk unit direct	1	D 0 0 1 1 0 0 0
	Read data recovery record 1	1	D 0 0 1 1 1 1 0
	Read data recovery record 2	1	D 0 0 1 1 1 1 1
Write	Write data	0	D 0 1 0 0 0 0 0
	Write data with read verify	0	D 0 1 0 0 0 0 1
	Write data repeat	0	0 0 1 0 0 0 1 0
	Write format	0	D 0 1 0 0 1 0 0
	Write ID	0	0 0 1 0 0 1 0 1
Scan	Scan data equal	1	F 0 1 1 0 0 0 0
	Scan data not equal	1	F 0 1 1 0 0 0 1
	Scan data low/equal	1	F 0 1 1 0 0 1 0
	Scan data low	1	F 0 1 1 0 0 1 1
	Scan data high/equal	1	F 0 1 1 0 1 0 0
	Scan data high	1	F 0 1 1 0 1 0 1
	Scan read single ID	1	0 0 1 1 0 1 1 0
	Scan alternate ID's	1	0 0 1 1 0 1 1 1

Bit 8 specifies if the (D) invert ECC option or (F) the scan options is invoked.

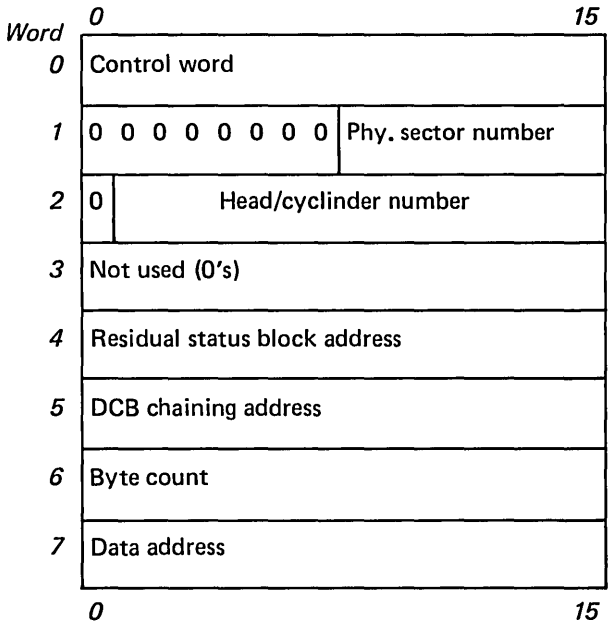
(D) Invert ECC - If this bit set to 1, the disk unit inverts the generated ECC code before comparing it with the ECC bytes coming off the disk unit. Or, it inverts the generated ECC code before writing the data record. If this bit is set to 0, then no invert is done.

(F) Scan Option - If this bit is set to 1, the scan operation returns the portion of the data record following the hit location. If set to 0, the entire data record containing the hit location returns along with a hit location pointer (scan hit count) in the cycle-steal status word 7, bits 8–15.

Physical Operations

The DCB's format for operations using physical locations on the disk follows:

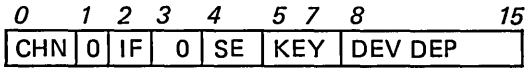
DCB (device control block)



DCB Word 0 - Control Word

This 16-bit word represents the cycle-steal operation. Specified DCB control word operations not carried out by the disk unit subsystem result in a specification check. The format of the control word follows:

Control word



Bit 0 Chaining Flag - indicates a DCB chaining operation. After successfully completing the current DCB, the attachment card does not interrupt but instead fetches the next DCB in the chain. Errors that produce interrupts stop further chaining. This flag may be used on all disk unit operations.

Bit 1 Set this bit to 0. Otherwise, a DCB specification check occurs.

Bit 2 Input Flag - specifies if the cycle-steal is a read or write operation. Set this bit to 1 for a scan or a read operation and 0 for a write operation. To specify the type of read or write function to be done, see the following information on the device dependent field. If incorrectly specified, a DCB specification check bit is set in the interrupt status byte (ISB).

Bit 3 Set this bit to 0. If not, a DCB specification check occurs.

Bit 4 Suppress Exception (SE) - when set to 1, the disk unit status is stored at the address specified by the residual status block (RSB) address field of DCB word 4. If it is a retryable operation, it is retried the number of times specified. If SE is set 0, no status is stored at the RSB address, and no retry of operations is done.

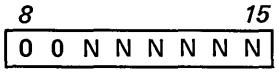
Bit 5-7 Cycle-Steal Address Key - a three-bit key presented by the disk unit during data transfers to verify that the program has authorization to access processor storage. Use this key on all disk unit operations that cycle-steal data to or from main storage.

Bits 8-15 Modifier Bits - describe the specific cycle-steal operation requested with this DCB. Refer to the DCB control word device dependent field table for specific operation requests. An incorrect value in these bits ends this operation without data being transferred. A DCB specification check is presented in the ISB with the interrupt. This field is ignored during a Start Cycle-Steal Status command.

DCB Word 1 - Physical Sector Number

This byte contains the physical sector number to be processed. It must be right-justified within the byte.

Use physical sector numbers for the read ID, write ID, write format, and read-data recovery operations.



Data and scan operations specifying multiple records operate first on the RBA specified record. Data records that follow this operation are processed in the record number sequence.

DCB Word 2 - Head/Cylinder

This word contains the head and cylinder number for physical operations and is organized as follows:

Word 2 head and cylinder

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Use	0	0	H	H	H	H	C	C	C	C	C	C	C	C	C	C

The following configuration gives the specific head and cylinder number:

Bits	2			5	6											15
	H	H	H	H	C	C	C	C	C	C	C	C	C	C	C	C
	8	4	2	1	512	256	128	64	32	16	8	4	2	1		

The maximum values for the head number and cylinder number are 13 (hex D) and 571 (hex 23B) for 2CA or 2CB or 1023 (hex 3FF) for 3CA or 3CB, respectively. If values larger than these are encoded, a DCB specification check results. Code bits 0 and 1 as 0's, or a DCB specification check occurs.

DCB Word 3 - Record Count

Not used.

DCB Word 4 - Residual Status Block (RSB) Address

The address contained in this word points to five words that are the beginning of a processor storage area where the RSB is stored. The RSB is stored only when the SE bit is set to 1, and a hard error did not occur. Soft error recovery procedures (ERP) are also begun.

DCB Word 5 - DCB Chain Address

This address is used to fetch the next DCB in the chain when the current DCB operation completes without a hard error and the chaining bit (control word 0, bit 0) is set to 1.

DCB Word 6 - Byte Count

This count represents the number of bytes transferred for the current DCB operation. The byte counts in the following table are required, or an exception interrupt is presented and a DCB specification check occurs.

Operation		Byte count (Hexadecimal)	(Decimal)
Read ID	(Note 5)	XXXX*	XXXX
Write ID	(Note 5)	XXXX	XXXX
Write Data Repeat		0100	0256
Write Format		0206	0518
Read Data Repeat		0100	0256
Read Data Recovery	Record 1 and 2	0100	0256
Read Disk Direct	(Note 3)	XXXX	XXXX
Read Verify	(Note 3)	XXXX	XXXX
Read Data	(Note 3)	XXXX	XXXX
Write Data	(Note 3)	XXXX	XXXX
Scan	(Note 4)	XXXX	XXXX
Scan Alternate IDs		0054	0084
Scan ID		0006	0006

*XXXX equals byte count specified

Notes:

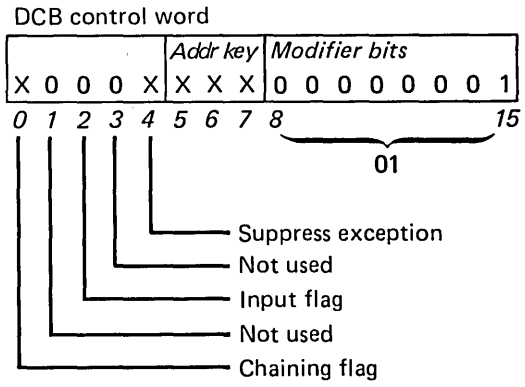
1. A byte count of 0 results in a no-operation instruction with condition code=3 returned to the system.
2. The byte count must be even or a DCB specification check occurs.
3. Bit 15 must be 0's.
4. Bits 7 and 15 must be 0.
5. The byte count must be a multiple of six bytes, not to exceed hex 0300 or decimal 0768.
6. Scan operations use the byte count field for specifying two lengths. Bits 0-7 specify the data length, and bits 8-15 specify the key length.

DCB Word 7 - Data Address

The data address is the starting storage address for the data associated with the operation to be performed. If the data address is odd, the operation ends and no data transfers. An exception interrupt occurs and the DCB specification bit is set to 1.

Recalibrate

This operation causes the disk unit to move the access mechanism to cylinder 0 and select head 0. When the seek completes, ready and home conditions are set in the cycle-steal status block. DCB words 1, 2, 3, 6, and 7 are not used; however, they are fetched and must have correct parity. Word 0 of the DCB is organized as follows:



Read Data Recovery Record 1

This operation recovers the first data record associated with a defective sector ID.

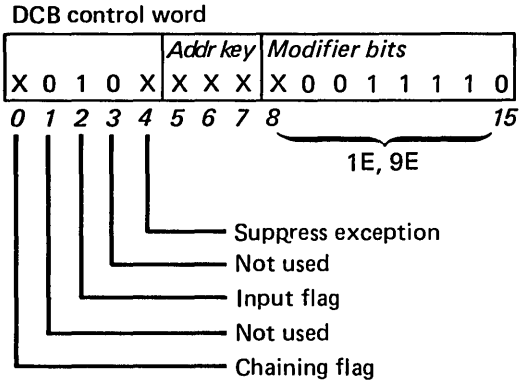
The starting ID on the track is determined from the physical sector number in word 1 of the DCB. A 00 denotes the first sector ID following index. A 01 denotes the second, and so forth.

The byte count in the DCB must be 256 and the sector number must be the physical sector containing the record to be recovered.

DCB Word 2 contains the head and cylinder numbers. DCB Word 3, bits 6–15, must contain the byte skip displacement (BSD). The head, cylinder, and BSD are obtained using a Scan Read Single ID command.

> **Note:** If a hard ECC error in the data field is detected, the data record transfers to the system before the attachment card presents the end operation interrupt.

DCB word 0 is organized as follows:

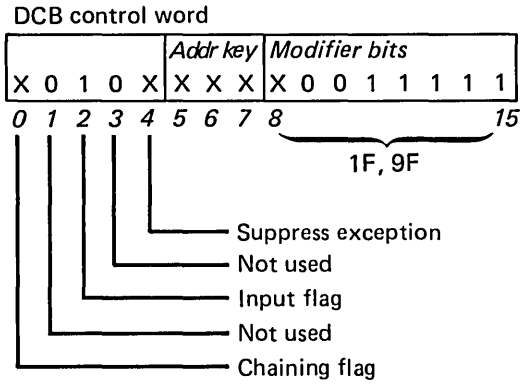


> **Note:** For an explanation of the modifier bits, see "Start Command Operations."

Read Data Recovery Record 2

This operation resembles the Read Data Recovery Record 1. However, it is used to recover the second data record associated with a defective sector ID.

DCB word 0 is organized as follows:



Note: For an explanation of the modifier bits, see "Start Command Operations."

Read ID

This operation transfers the ID field of a sector into main storage at the data address specified in the DCB. The byte count field of the DCB determines the number of sector IDs read into main storage. The byte count must be a multiple of 6 bytes up to a maximum of 128 IDs (6 bytes ID length) x 128 = 768 bytes maximum.

Flag byte						Logical sector number								Head number						Cylinder number							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F	F	F	F	F	F	S	S	S	S	S	S	S	S	S	S	0	0	H	H	H	H	C	C	C	C	C	C	C	C	C	C

Physical sector						Byte skip displacement									
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
S	S	S	S	S	S	D	D	D	D	D	D	D	D	D	D

DCB Word 2 - Head/Cylinder Number

This word specifies the head and cylinder containing the ID to be read.

The starting ID on the track is determined from the physical sector number in word 1 of the DCB. A 00 denotes the first sector ID following index. A count of 01 denotes the second, and so forth.

The ERP for this operation depends upon the control word bit 4 (SE bit). When the SE bit is set to 1, the hardware performs retries before the error is considered a hard error. When the operation ends, the status is stored at the location the RSB address points to in the DCB unless an exception occurs. Status is then available to a Start Cycle-Steal Status command.

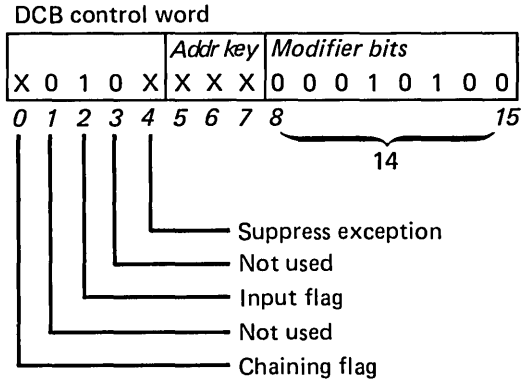
If the SE bit is set to 0, no retries are attempted, and a CRC error results in the insertion of hex FF (all 6 bytes) into main storage for the attempted ID. The read ID operation is then resumed with status available to a Start Cycle-Steal Status command.

The bit meanings of the flag byte follow:

Bit 0 - Defective ID field (factory)
Bit 1 - Not used; must be 0
Bit 2 - Not used; must be 0
Bit 3 - User defect
Bit 4 - Defective data field (factory)
Bit 5 - Unused alternate sector

Note: All flag bits are used in ID field comparison.

DCB word 0 is organized as follows:

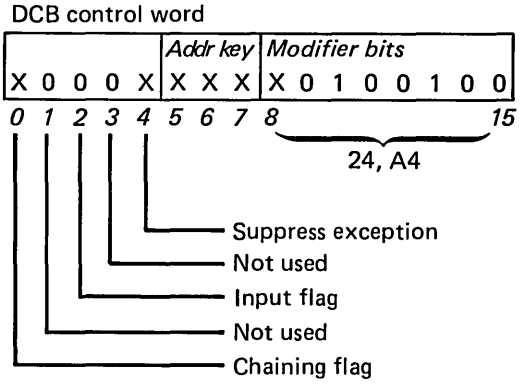


Write Format

This operation writes the sector ID and both data records associated with the ID. The physical sector number specified in the DCB is the location to which the data is written. The byte count field must be equal to decimal 518 (hex 0206), which represents 6 bytes for the ID and 512 bytes for the two records. The ERP for this operation operates as specified in the control word.

Use the Write Cache Control command to disable the cache storage before the Write Format command, or a delayed command reject is issued.

Note: Reenable cache storage when all ID operations are complete.



Write ID

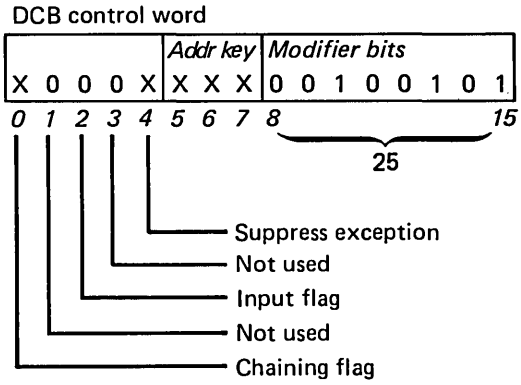
This operation writes 6 bytes of sector ID information onto a specified sector. The data pointed to by the data address field in the DCB is written into the sector ID field specified by the physical sector number byte in the DCB.

The sector ID field follows:

Flag byte						Logical sector number								Head number						Cylinder number							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F	F	F	F	F	F	S	S	S	S	S	S	S	S	S	S	0	0	H	H	H	H	C	C	C	C	C	C	C	C	C	C

Physical sector						Byte skip displacement									
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
S	S	S	S	S	S	D	D	D	D	D	D	D	D	D	D

DCB word 0 is organized as follows:



DCB Word 2 - Head/Cylinder Number: The physical sector number byte in the DCB is used as the starting location to write on the disk. A 0 in this byte specifies the first sector after index. A count of 1 specifies the second sector after index, and so on to the end of the track (0 to 49 is valid).

The byte count is specified as a multiple of 6 bytes up to a maximum of 128 sectors (768 bytes).

> **Note:** Data records associated with the ID must be written following a write ID operation. Use the Write Data command for this or use the Write Format command to write both the ID and the data fields. Old data fields associated with a rewritten ID may not be readable following the Write ID operation. Use read data recovery commands to recover data before writing the ID.

During initialize programs, a Read ID command must be carried out before a Write ID command. Writing a previously flagged defective sector as good may result in the loss of user data.

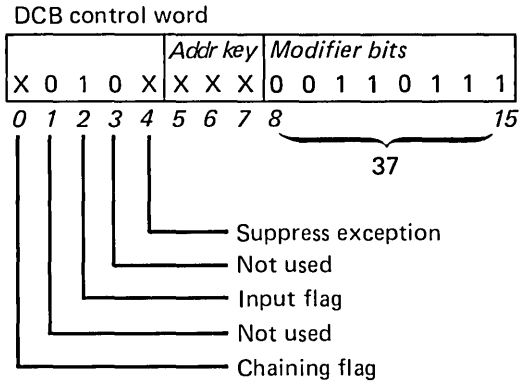
Disable the cache storage by using the Write Cache Control command before issuing a Write ID command, or a delayed command reject is issued.

> **Note:** Reenable cache storage when all ID operations are complete.

Scan Alternate IDs

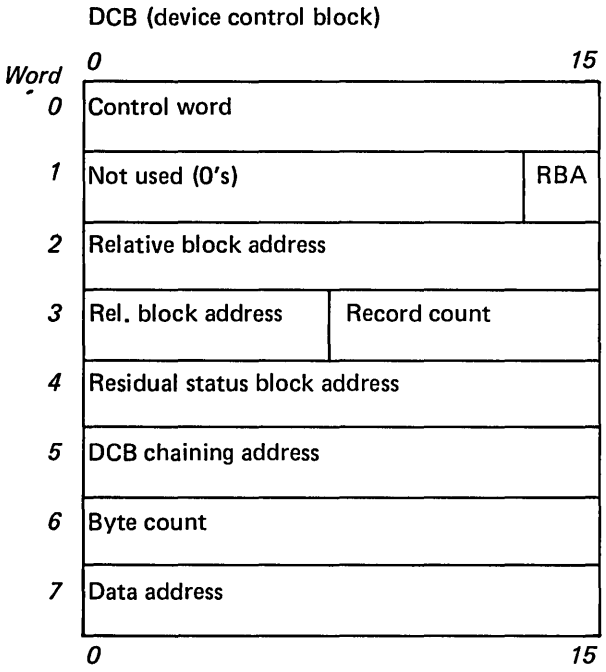
This operation uses the cylinder number in word 2 of the DCB to start a search for the alternate sectors located on the cylinder. The byte count must be hex 54 for a maximum of 14 sector IDs. The IDs returned are logical sectors, from 686 to 699. When alternates are assigned, the data returned is hex FF, which indicates those sectors are not available for reassignment.

DCB word 0 format follows:



Logical Operations

The format of the DCB Block for operations using the logical record number specified by an RBA follows:

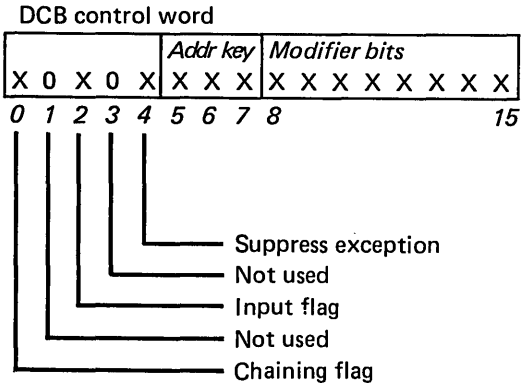


Note: If the RBA is greater than 784,783 for models 2CA or 2CB or 1,404,927 for models 3CA or 3CB for read, write, and scan commands, the attachment card presents an error interrupt, and sets the DCB specification bit to 1. The beginning RBA for the CE cylinder (570) for models 2CA and 2CB is 782,040. The beginning RBA for the CE cylinder(1022) for models 3CA and 3CB is 1,402,184.

Data and scan operations that specify multiple records process first on the record specified by the RBA. The data records that follow process in record number sequence.

DCB Word 0 - Control Word

This word is organized as follows:



DCB Word 1 - Not Used

Do not use this word; set to 0's.

DCB Word 2 - Relative Block Address (RBA)

This word contains the RBA on the disk unit where the operation begins.

> **Note:** If the RBA is greater than 784,783 for models 2CA or 2CB, or 1,404,927 or models 3CA or 3CB for read, write, or scan commands, the attachment card presents an error interrupt, and set the DCB specification bit to 1. The beginning RBA for the CE cylinder (570) in models 2CA and 2CB is 782,040. The beginning RBA for the CE cylinder (1022) in models 3CA and 3CB ia 1,402,184.

DCB Word 3 - Record Count

This byte contains the count for the total number of records involved with a Scan or Read/Write Repeat operation. When Scan, Read Repeat, or Write Repeat operations are carried out, the total record count must be N-1 (N is the number of records to be processed). The maximum count of 4095 allows approximately three cylinders of records to be processed. The scan count field has the value:

Bit	Record count
4	2048
5	1024
6	512
7	256
8	128
9	64
10	32
11	16
12	8
13	4
14	2
15	1

Use bits 0—3 for the high-order bits of the RBA field.

DCB Word 4 - Residual Status Block (RSB) Address

This word contains the address in main storage where the RSB is stored.

DCB Word 5 - Chaining Address

This word contains the address of the next DCB in a chaining operation.

DCB Word 6 - Byte Count

This word contains the number of data bytes to be transferred for the current DCB.

DCB Word 7 - Data Address

This word contains the address in main storage where the data transfer starts.

Read Data

This operation causes the attachment card to cycle-steal data from the disk unit (cache disabled) or cache storage (cache enabled) into main storage. If cache storage is enabled and no data is present in it during the operation, the data is fetched from the disk unit and placed into cache storage before being transferred to the system.

The common adapter searches for the proper record on the disk and transfers it to processor storage as indicated by the data address field of the DCB. The byte count specifies the number of bytes to be transferred. The byte count must be an even number to reflect word boundaries.

The ERP for this operation depends upon the SE bit. When the SE bit is set to 1, the controller performs retries before the error is considered to be a hard error. When the operation finishes, the status is stored at the location indicated by the RSB address in the DCB, unless an exception occurs. Status is then available to a Start Cycle-Steal Status command.

If cache storage is enabled and a read miss occurs, additional data is transferred from the disk unit into cache storage. Transferring more data is part of the cache function that anticipates future data requirements by pre-fetching more records than required. This operation results in system time saving because this pre-fetched data resides in cache storage.

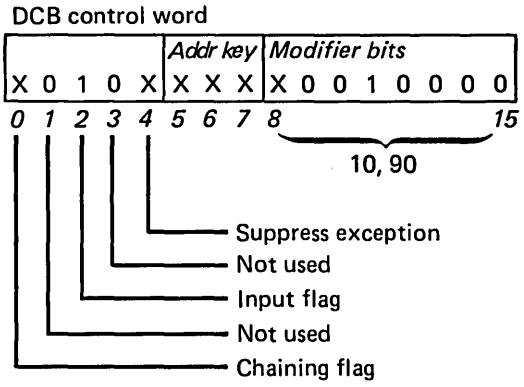
If a hard error occurs on a pre-fetched data record, the attachment card ends the operation with an exception interrupt and no data is transferred to the system. An exception interrupt occurs whether or not the data in error was requested.

Cycle-steal status words 9 and 10 identify the data record in error. Read the requested record using the Read Disk Direct command, if the record in error has not been reassigned.

> **Note:** If cache storage is disabled and a hard ECC error in the data field occurs, the data record read on the last retry transfers to the system before the end operation interrupt is presented. If cache storage is enabled, no error data transfers.

If the SE bit is set to 0, retries are not attempted, and errors result in the end of the operation with status available to a Start Cycle-Steal Status command.

If a record hit does not occur after one revolution, a no record found error is presented along with any other errors.



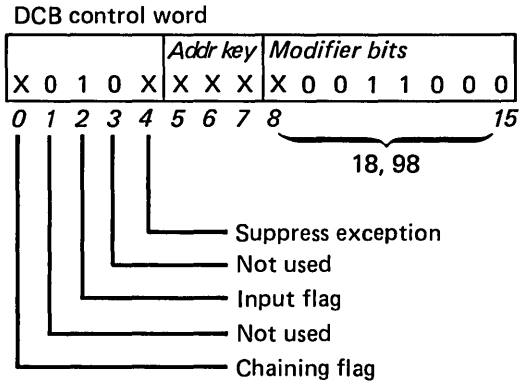
Note: For an explanation of the modifier bits, see Start command operations.

Programming Consideration

If DCB word 0, bit 8, is set to 1, the attachment card inverts the error correction code (ECC) characters before making a comparison between the ECC characters generated by the attachment card and the ECC characters read from the disk. If bit 8 is set to 0, the attachment card does not invert the ECC characters.

Read Disk Unit Direct

This operation resembles the read data operation except that the data read back to the system is transferred from the disk unit, even if the data were present in the cache storage. Use this operation for a bit for bit check on the recorded data on the disk. DCB word 0 is organized as follows:



Note: For an explanation of the modifier bits, see "Start Command Operations."

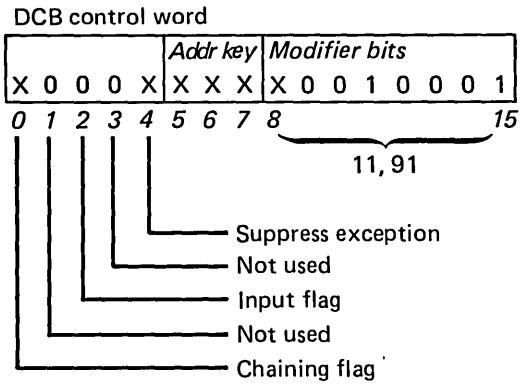
Read Verify

Use this operation to validate data written on the disk. It operates like the Read Data operation, except that no data is transferred to storage during processing. This operation could be used following a Write; however, it is far more efficient to use the Write with the Read Verify operation instead. The ERP for Write with Read Verify allows the data to be rewritten and included in the ERP. Separate Write and Read Verify operations do not allow data to be rewritten and included in the ERP. The DCB contains the byte count, the RSB address, and the RBA. The controller converts the RBA to a search argument (head number and cylinder number).

The ERP for this operation depends upon the SE bit. When the SE bit is set to 1, the hardware performs retries before determining a hard error. When the operation finishes, the status is stored at the location pointed to by the RSB address in the DCB unless an exception occurs. In this case, status is available to a Start Cycle-Steal Status command.

If the SE bit is set to 0, no retries are attempted, and any errors result in the end of the operation with status available to a Start Cycle-Steal Status command.

Read verify does not use cache storage. DCB word 0 is organized as follows:



Note: For an explanation of the modifier bits, see "Start Command Operations."

Read Data Repeat

This operation is similar to a read data operation except data is transferred to storage for only the last record processed. All records up to the last record are not transferred but are verified for proper ECC. Only full records may be specified. The byte count in the DCB must be 256 or an exception interrupt occurs with DCB specification bit set to 1. The number of records to be processed is contained in DCB word 3, and in the form N-1, where N is the number of full records involved in the operation (maximum is 4095 records).

Up to 1,048,576 bytes (4096 full records) may be involved in this operation without regard to track or cylinder boundaries and without intermediate interrupts. Only the last 256 bytes of data are transferred to storage. This operation does not involve cache storage.

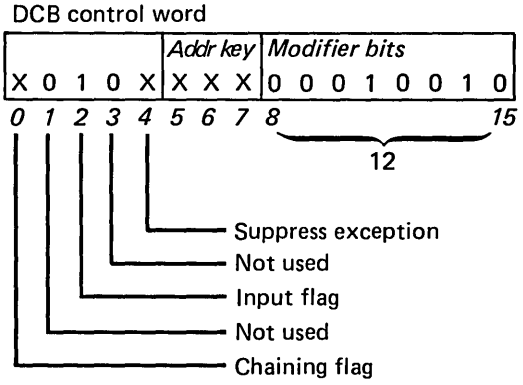
The ERP for this operation depends upon the control word bit 4 (SE bit). When the SE bit is set to 1, the hardware performs retries before the error is considered a hard error.

> **Note:** The number of retries depends upon the operation and is found in cycle-steal status words 2 and 3.

When the operation finishes, the status stores at the location the RSB address points to in the DCB unless an exception occurs. Then, status is available to a Start Cycle-Steal Status command.

If the SE bit is set to 0, no retries are attempted, and any errors result in the end of the operation with status available to a Start Cycle-Steal Status command.

DCB word 0 is organized as follows:



Write Data with Read Verify

The Write Data and Write Data with Read Verify commands transfer data to the disk from the DCB data address, starting at the search argument location specified in the DCB.

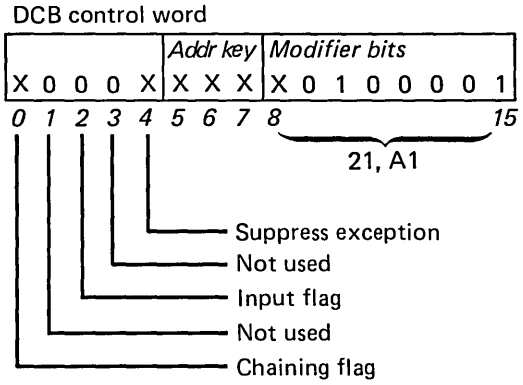
Up to 65,534 bytes can be written without regard to track or cylinder boundaries and without intermediate interrupts. If the byte count goes to 0 before the end of a complete 256- byte record, the attachment card fills the remainder of that record with all 0 data.

This operation has two forms. The first form writes data without read verify. The second form writes data with read verify. The written data is then automatically read back and ECC checked before the operation completes. Use the write data with verify option instead of separate write and verify operations so that automatic ERP can retry both the write and verify if the verify fails.

If cache storage is enabled, all data residing in it to be updated by the Write Data operation is written first. That cache data, plus the data from main storage not residing in cache storage, are written to the disk unit. Hit data is updated both in cache storage and on the disk so that future read operations to this data come from the cache storage and do not reference the disk. Therefore, if you want to do a read back check on recently written data, use the Read Disk Unit Direct operation to ensure that the data is read from the disk.

The ERP depends upon the control word bit 4 (SE). When the SE bit is set to 1, the hardware performs retries before the error is considered a hard error. When the operation finishes, the status is stored at the location the RSB address in the DCB points to, unless an exception occurs. Status is then available to a Start Cycle-Steal Status command.

If the SE bit is set to 0, no retries are attempted, and errors end the operation with status available to a Start Cycle-Steal Status command. DCB word 0 is organized as follows:

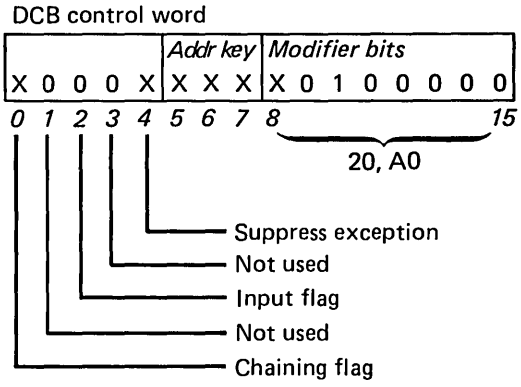


Note: For an explanation of the modifier bits, see Start command operations.

Write Data

For an explanation, see "Write Data Repeat."

The DCB word 0 (control word) format follows:



Note: For an explanation of the modifier bits, see Start command operations.

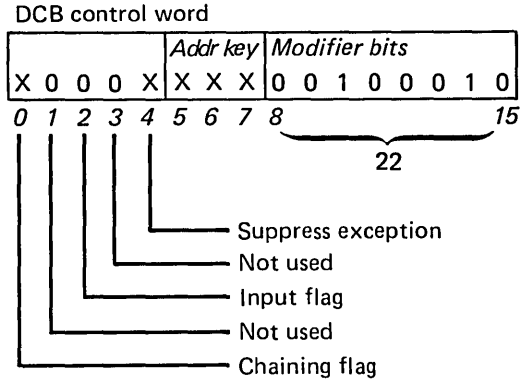
Write Data Repeat

This operation resembles a write data operation, except that only one data record transfers from storage and is written to the disk multiple times, depending upon the record count word of the DCB. The byte count in the DCB must be 256, or an exception interrupt occurs with DCB specification bit set to 1 in the ISB. The number of records to be processed is contained DCB word 3. The record count is in the form N-1, where N is the number of full records in the operation (maximum is 4096 records and maximum record count in word 3 is 4095).

Up to 1,048,576 bytes (4096 full records) can be used in this operation without regard to track or cylinder boundaries and without intermediate interrupts.

The ERP for this operation depends upon the control word bit 4 (SE). When the SE bit is set to 1, the hardware performs retries before the error is considered a hard error. When the operation finishes, the status is stored at the location pointed to by the RSB address in the DCB, unless an exception occurs. The status is then available to a Start Cycle Steal Status command.

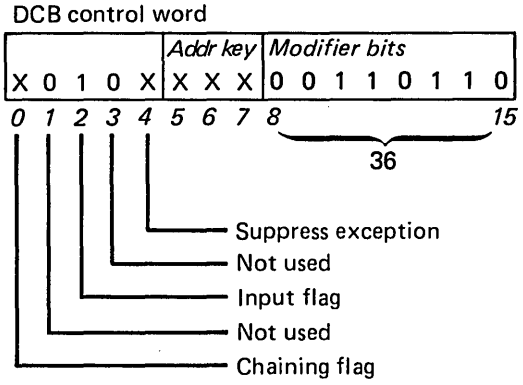
If the SE bit is set to 0, no retries are attempted, and any errors end the operation with status available to a Start Cycle-Steal Status command. Write Data Repeat does not involve the cache storage. DCB word 0 is organized as follows:



Scan Read Single ID

Use this operation to find the physical location of a sector given its RBA. Using the specified RBA, this operation seeks to the cylinder where an ID search starts. The search uses a cylinder number and a logical sector number derived from the RBA as the scan argument and scans for an equal condition. When a hit occurs, the entire ID of the final sector returns to the data address specified in the DCB. The byte count must be equal to six, or a DCB specification check occurs.

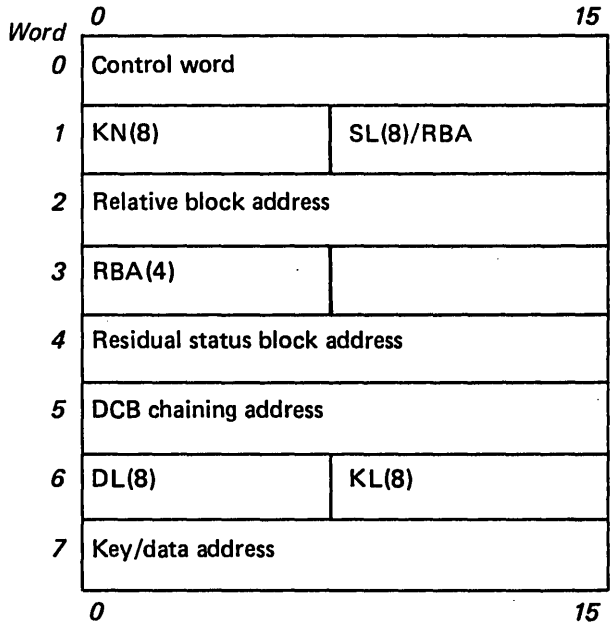
If the search ends with no hit condition met, then a no record found condition returns. For chained operations, the status returns in the RSB block associated with the DCB. DCB word 0 format follows:



Scan Operations

The DCB format for scan operations follow:

DCB (device control block)



KN - Number of keys scanned in each record (256-byte disk record). (bits 0–7). Valid values are 1–64.

SL - Skip length bits 8–15; displacement from the beginning of the record to the first key to be scanned. (Specified in bytes; must be even.) Valid values are 0–254.

RBA - Relative block address bit 15 is the highest bit of the RBA for models 3CA and 3CB.

DL - Data length bits 0–7, specified in bytes; must be even. Valid values are 2–254.

KL - (Bits 8–15) Key length specified in bytes; must be even. Valid values are 2–254.

If the previous parameters are not within the valid limits, a DCB specification check occurs.

Note: For a valid scan operation, the following relationships between the various scan parameters must be maintained:

SL + (KN) (KL + DL) <= 256

Scan Option - If this bit (bit 8 of DCB word 0) is set to 1, the scan operation returns only the portion of the data record that follows the hit location. If this bit is set to 0, the entire data record containing the hit location returns along with a hit location pointer (scan hit count) in cycle-steal status word 7, bits 8-15.

This operation causes a data comparison search between a key argument and the data record(s) contained on a given disk unit. A single key argument transfers from main storage to the attachment card. The starting address of the key argument is specified by the DCB word 7, data address. The DCB relative block address specifies the starting point on the disk unit for the search. The DCB record count field defines the number of data records to be searched. If an equality condition is found, data transfers to main storage; otherwise, no transfer of data to main storage occurs. The interrupt information byte (IIB) and the RSB both contain status bits indicating whether or not an equality condition was found. The RSB contains the scan hit byte count when a hit occurs.

The key argument record may contain a maximum of 254 bytes. If a scan hit occurs, the data comparison ends and all or part of the disk data record returns to the system at the data address specified. The data length specified in the DCB or the control bit (bit 8) in the control word determines the data length returned.

If the equality test fails, the search continues until a hit occurs or the DCB record count has been depleted.

The input flag must be set to 1 for the scan operation.

The ERP for this operation depends on the control word bit 4 (SE). When the SE bit is set to 1, the hardware performs the retries before the error is considered a hard error. When the operation finishes, status is stored at the location the RSB address in the DCB points to, unless an exception occurs. Status is then available to a Start Cycle-Steal Status command.

If the SE bit is set to 0, no retries are attempted, and errors end the operation with status available to a Start Cycle-Steal Status command.

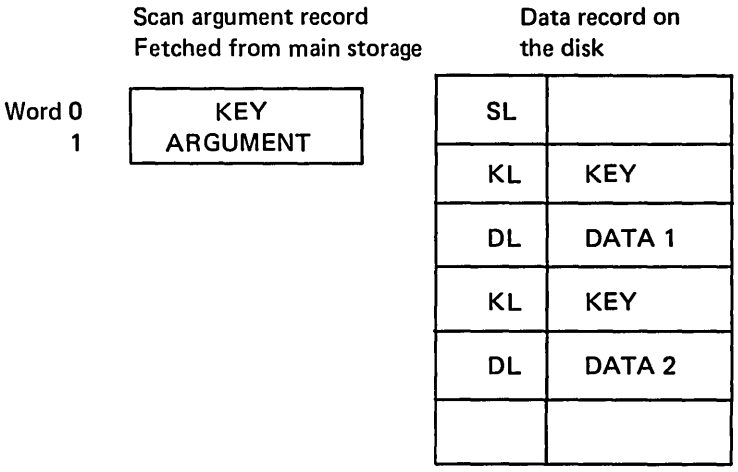
The scan operation stops with the first scan hit, a hard error, or a depletion of the record count.

Scanning starts with the data record the RBA in the DCB points to. The record count in the DCB determines the number of records scanned. A count of 0 causes one record to be scanned, a count of 1 for two records, and so forth, up to 4095 for 4096 records, maximum.

Note: If a control unit error occurs preventing it from fetching disk data (for example, no record found), the residual address points to the last byte of the DCB, and the residual count is unchanged from the number specified. This indicates that the key argument record was read from storage into the disk unit controls, and the DCB did not write any words back to storage.

The same residual address and residual byte count are returned if a scan-not-hit condition occurs. Consider the following example:

Scan data record diagram

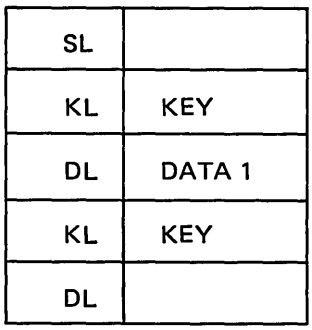


SL = The displacement into the record to be skipped before the first comparison is started (skip length = SL). (0-254, must be even.)

KL = The length of data used as a key for the comparison(s) (key length = KL). (2-254, must be even.)

DL = The length of the data which follows each key field (data length = DL). (2-254, must be even.)

The scan data record transferred to main storage can be in two forms. With the scan option bit set to 0, the data returned is the entire data record. A pointer to the location of the scan hit is available in cycle-steal status word 7, bits 8–15, and in the RSB block, word 5.



F=0, Scan hit on first key

F=1, Scan hit on first key

With the scan option bit set to 1, only the portion of the data record that follows the key hit for the specified data length returns.

Following is a list of the scan operations and DCB word 0, bits 8–15 (device dependent field) representation:

Scan data not equal	(F011 0001)
Scan data low or equal	(F011 0010)
Scan data low	(F011 0011)
Scan data high or equal	(F011 0100)
Scan data high	(F011 0101)

These operations work in the same sequence as the scan equal, except for the data compare.

The following table summarizes the compare operations:

Scan data equal	Key argument	= Disk unit data
Scan data not equal	Key argument	$\neq$ Disk unit data
Scan data low or equal	Key argument	$\geq$ Disk unit data
Scan data low	Key argument	$>$ Disk unit data
Scan data high or equal	Key argument	$\leq$ Disk unit data
Scan data high	Key argument	$<$ Disk unit data

Use scan not hit, scan equal hit, high compare, and low compare bits together to define the status of the scan operations. These status indicators are presented in both the RSB and the cycle-steal status block.

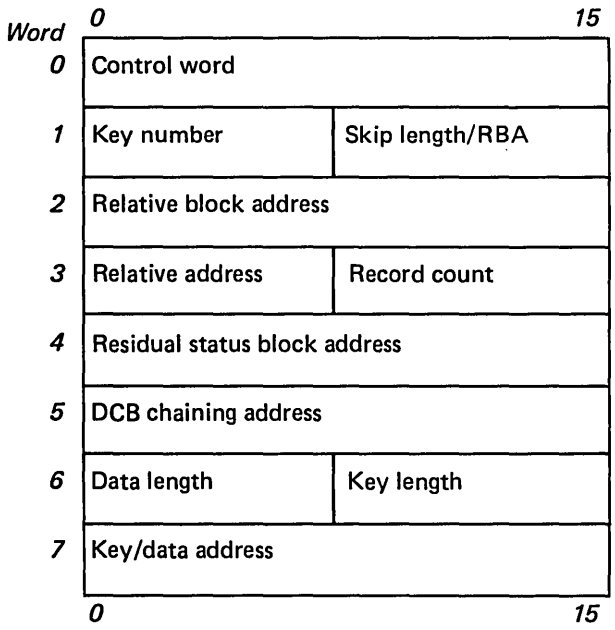
Command	Data compare	Scan not hit	Scan equal hit	High compare	Low compare
Scan Equal	Equal	0	1	0	0
	Not equal	1	0	X	X
Scan Not Equal	Equal	1	0	0	0
	Not equal	0	0	X	X
Scan Low or Equal	Equal	0	1	0	0
	Low	0	0	0	1
	High	1	0	1	0
Scan Low	Equal	1	0	0	0
	Low	0	0	0	1
	High	1	0	1	0
Scan High or Equal	Equal	0	1	0	0
	Low	1	0	0	1
	High	0	0	1	0
Scan High	Equal	1	0	0	0
	Low	1	0	0	1
	High	0	0	1	0

1 = Bit is on (1)
X = Either high compare or low compare is on (1)

Scan Data Equal

The DCB for the Scan Data Equal command follows:

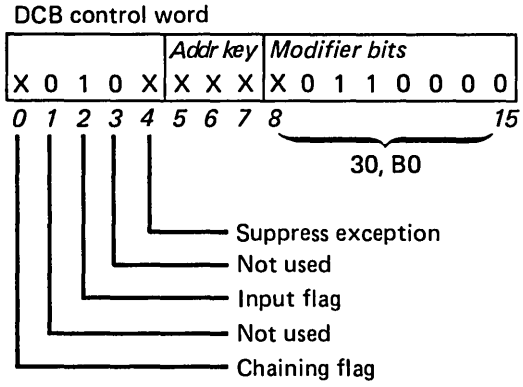
DCB (device control block)



Word 0 - Control Word

This word is organized as follows:

DCB control word

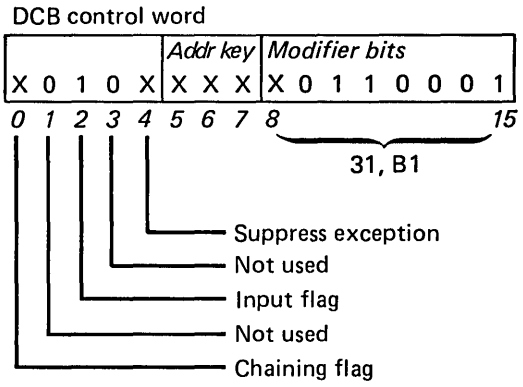


Note:

Scan Option If this bit is set to 1, the scan operation returns only the portion of the data record following the hit location. If this bit is set to 0, the entire data record containing the hit location returns along with a hit location pointer (scan hit count) in the cycle-steal status word 7, bits 8-15. This note is applicable to the remaining scan operations.

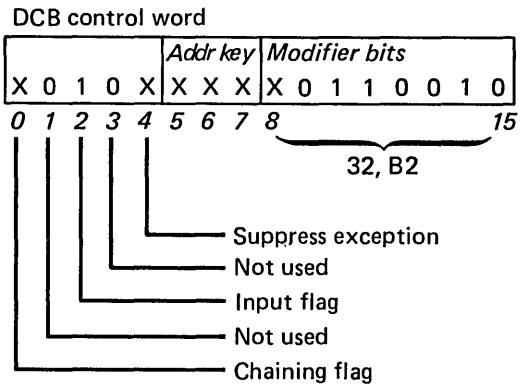
Scan Data Not Equal

The scan data not equal control word follows:

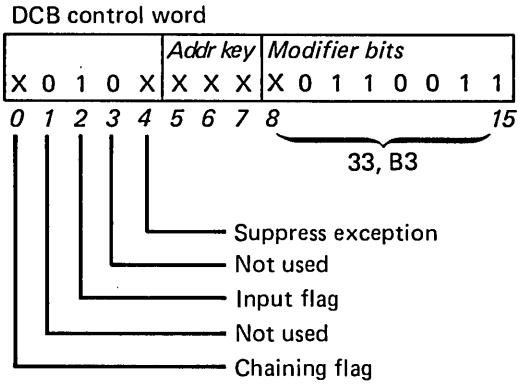


Scan Data Low or Equal

The control word (word 0) of the DCB follows:

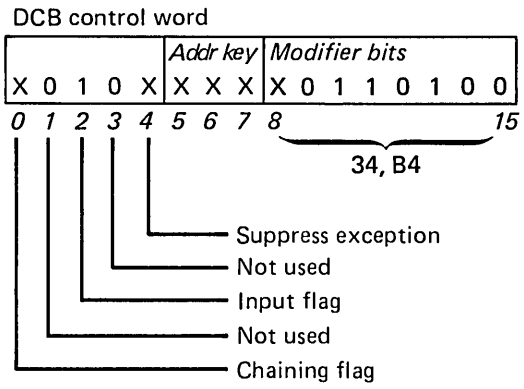


Scan Data Low



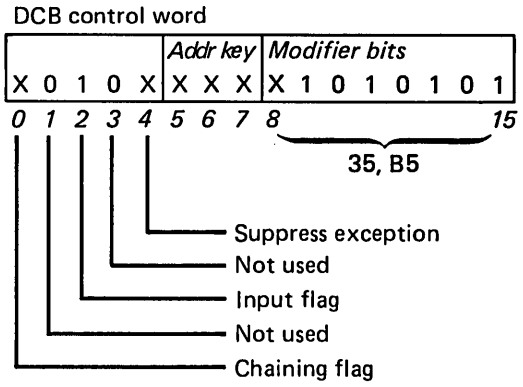
Scan Data High or Equal

The control word of the DCB follows:



Scan Data High

The control word format for the DCB follows:



Start Control Command

The Start Control command starts attachment-directed operations. These control operations are identified in bits 8–15 of the DCB control word (word 0). The IDCB for the Start Control command follows:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 1 1 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
7C	00–FF

Immediate data field
DCB address
16 ... *31*

The DCB for the Start Control command follows:

DCB (device control block)

Word	*0* ... *15*
0	Control word
1	Attachment storage address
2	Device selector
3	Not used (0's)
4	Not used (0's)
5	Chaining address
6	Byte count
7	Data address
	0 ... *15*

DCB Word 0—Control Word

The control word format follows:

- Bit 0—Chaining Flag
- Bit 1—Not Used
- Bit 2—Input Flag
- Bit 3—Not Used
- Bit 4—Suppress Exception
- Bits 5–7—Cycle-Steal Address Key
- Bits 8–15—Operation Modifier.

The operation modifiers follow:

- Write Attachment Storage
- Read Attachment Storage
- Read Attachment Definition
- Attachment Initialize.

Start Control Operations

The following table summarizes the start control operations.

> **Note:** If any other disk units have an operation in progress, the controller returns a delayed command reject. The SE bit must be 0 for all controller operations or a DCB specification check occurs.

Start control operations

Command type	Function IDCB CMD FIELD=0111 1100 DCB control word bit 2	(I/F)	DCB (8-15) device dependent field
Write	Write attachment storage	0	1110 1000
	Attachment initialize	0	1110 0010
Read	Read attachment storage	1	1110 0100
	Read attachment definition	1	1111 1101

Write Attachment Storage

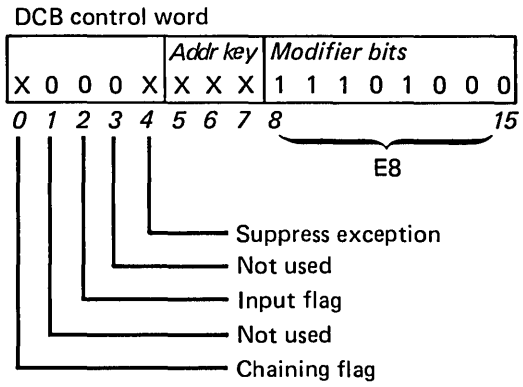
This operation loads the attachment's random access storage with microcode patches.

DCB (device control block)

Word	0 — 15
0	Control word
1	Attachment storage address
2	Device selector
3	Not used (0's)
4	Not used (0's)
5	Chaining address
6	Byte count
7	Data address

DCB Word 0 - Control Word

DCB word 0 format follows:



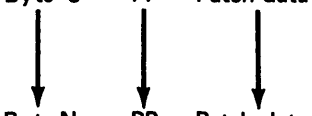
DCB Word 1 - Attachment Storage Address

The attachment card loads within a defined range of controller storage. The combination of DCB word 1 (controller start address) and DCB word 6 (byte count) should not exceed this range. The defined address range for the 4967 attachment card is hex E000 to hex EFFF.

If the patch is for the common adapter, do not use word 1. The attachment card does not check this range. If the defined range is exceeded, a DCB specification check occurs. A device end interrupt is presented at the end of a successful write controller storage command.

The data format follows:

```
Byte 0 = NN   Patch segment number (0,1,. . .N,'FF')
Byte 1 = LL   Storage patch level (X'01' to X'FF)
Byte 2 = CC   Read-only storage compatibility number byte 0
Byte 3 = CC   Read-only storage compatibility number byte 1
Byte 4 = SS   Patch checksum byte 0
Byte 5 = SS   Patch checksum byte 1
Byte 6 = PP   Patch data
```



```
Byte N = PP   Patch data
```

The module 64K sum of bytes 4 through N must be hex 0000 for a correct checksum. The read only storage compatibility number, patch checksum and patch segment number must be correct for the attachment card to enter the initialized state. Otherwise, a CC2 interrupt occurs with cycle-steal status word 3, bit 13 set to 1.

> **Note:** The first six bytes of data sent with a write attachment storage operation are not loaded into storage. They are used to determine read only storage compatibility. If the random access storage patch must be loaded in several parts, each part must be preceded with these six bytes. After each part loads, the read only storage compatibility and random access storage checksum are tested. The patch segment number is tested to insure it is in sequence. The first segment must be 0, and each subsequent segment greater until the last segment, which must be hex FF. If read only storage compatibility and patch checksum are correct, the attachment card sets the initialized state flag to 1 after each part is loaded. If an error is detected while loading a part, the patch branch table clears, and an error is presented. Load the entire patch branch table last.

DCB Word 2 - Device Selector

The format for this word follows:

Bit 0 First segment flag (set to 1 for the first segment of multi-segment patch)

Bit 1 Last segment flag (set to 1 for the last segment of multi-segment patch)

Bits 2-14 Not used; set to 0's

Bit 15 Device selector number (0 = attachment card, 1 = common adapter)

Note: For a single segment patch, bits 0 and 1 are set to 1's, and byte 0 of the patch is hex FF.

When word 2, bit 15 indicates the patch is for the common adapter, do not use word 1. Patch data is sent to the common adapter in order, and all addresses are implied.

DCB Words 3-4

Not used; set to 0s.

DCB Word 5 - Chaining Address

This word contains the address of the next DCB for data chaining operations.

DCB Word 6 - Byte Count

This word contains the transfer byte count and is used with DCB word 1 (attachment starting address). Refer to the description of DCB word 1 for information on the range of valid addressing.

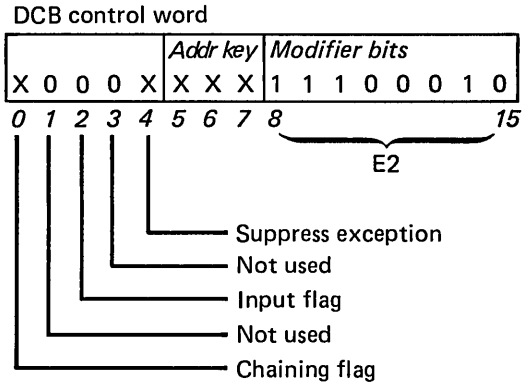
DCB Word 7 - Data Address

This word contains the starting storage address for the data address associated with the operation to be performed.

Attachment Initialize

Use of this command results in a no-operation.

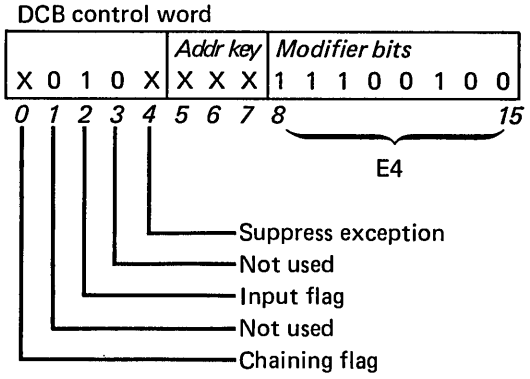
DCB word 0 format follows:



Read Attachment Storage

When this command is processed, the attachment card cycle steals the number of bytes indicated in DCB word 6 from attachment storage to main storage, starting at the address indicated in DCB word 1. The starting address of main storage is specified in the DCB word 7.

The defined attachment card address range for this operation is hex E000 to EFFF. A DCB specification check results if this range is exceeded. This operation does not use DCB word 2 (device selector). DCB word 0 format follows:



The Read Attachment Storage command can be used to read the attachment error log by issuing the command with DCB word 1 set to hex E2A0 and DCB word 6 set to hex 0030.

The format of the error log data follows.

Words 0-7

These words contain the DCB of the last logged error (CC2).

Words 8-21

These words contain the cycle-steal status of the last logged error.

Word 22

Bits 0-7 IDCB command byte of the last logged error

Bits 8-15 ISB byte of last logged error

Word 23

Bit 0 Not used; 0.

Bits 1-3 Condition code of last logged error

Bits 4-7 Drive number of last logged error

- **Bit 4** Drive 0 (base unit)
- **Bit 5** Drive 1 (expansion unit)
- **Bit 6** Drive 2 (expansion unit)
- **Bit 7** Drive 3 (expansion unit)

Bits 8-15 Diagnostic checkpoint (hex FE or hex FF)

Read Attachment Definition

This operation returns up to six words of data to processor main storage.

Word 0

The arithmetic sum (module 64K) of the three read-only storage checksums (used for random access storage patch compatibility determination). If DCB word 2, bit 15 is set to 1, this word contains the common adapter read only storage compatibility number.

Word 1

Byte 0 Always 00.

Byte 1 Random access storage patch level (00 if attachment card/common adapter is not initialized; 01–FF, if attachment card/common adapter is initialized).

Word 2

Bit 0 A 0 if attachment card/common adapter is not initialized; a 1 if attachment card/common adapter is initialized.

Bit 1 Patch checksum error.

Bit 2 Not used.

Bit 3 Read-only storage/patch compatibility error.

Bits 4-14 Not used.

Bit 15 Patch sequence number error.

Word 3

Bit 0 Data collection mode active.

Bits 1-7 Not used.

Bits 8-15 Last cache page referenced in data collection mode (valid only if bit 0 is set to 1).

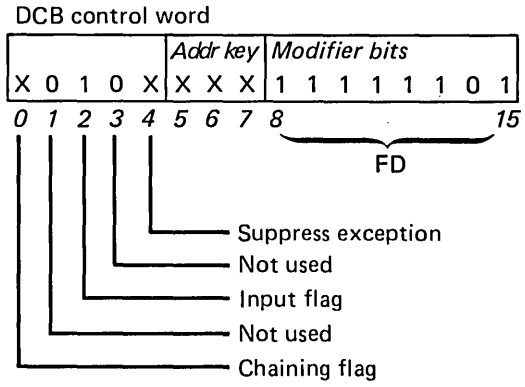
Words 4 and 5

These words are not used.

> **Note:** The DCB byte count must be even and decimal 12 or less. DCB word 2, bit 15 (device selector number) indicates attachment card (0) or common adapter (1) for this operation.

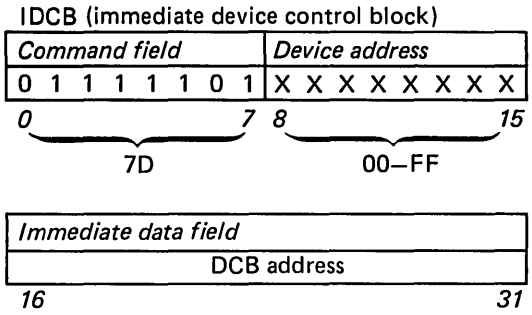
DCB Word 0

DCB word 0 format follows:

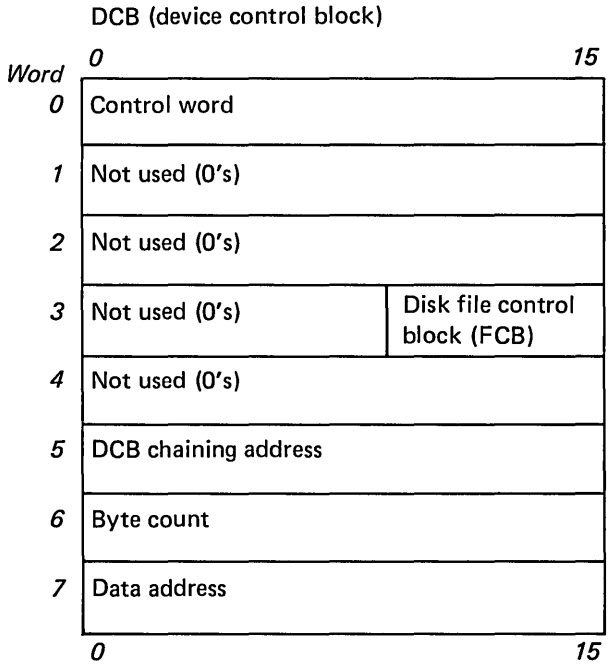


Start Cycle-Steal Diagnostic Command

The IDCB for the Start Cycle-Steal Diagnostic command follows:



The DCB for the Start Cycle-Steal Diagnostic command follows:



DCB Word 0 - Control Word

The control word is organized as follows:

Bits 0-1: These bits are not used; set to 0's.

Bit 2 - Input Flag: This bit controls direction of data flow and must be set to 1 for a read operation and to 0 for a write operation.

Bits 3-4: These bits are not used; set to 0's.

Bits 5-7 - Cycle-Steal Address Key: This is a 3—bit key that the disk unit presents during data transfers to verify that the program has authorization to access processor storage.

Bits 8-15 - Operation Modifier: The operation modifiers follow:

- Attachment Diagnostic Write Test
- Common Adapter Write FCB Diagnostic
- Write Common Adapter Patch Diagnostic
- Write Common Adapter Data Buffer Diagnostic
- Write Cache Diagnostic
- Attachment Read Only Storage Diagnostic
- Read Common Adapter Data Buffer Diagnostic
- Attachment Diagnostic Read Test
- Read Diagnostic Word 1
- Read Diagnostic Word 2
- Read Cache Diagnostic
- Common Adapter Read FCB Diagnostic.

DCB Words 1-2

These words are not used; set to 0's.

DCB Word 3 - Disk File Control Block/Buffer Number

Bits 0–7 of this word are not used; set to 0's. Bits 8–15 of this word represent the disk file control block.

DCB Word 4

This word is not used; set to 0's.

DCB Word 5 - Chaining Address

This word contains the address of the next DCB in a chaining operation.

DCB Word 6 - Byte Count

This word contains the transfer byte count for the current operation.

DCB Word 7 - Data Address

This word contains the main storage address for the start of the data transfer during the current operation.

Start Cycle-Steal Diagnostic Operations

The Start Cycle-Steal Diagnostic Operations are summarized in the following table.

Start cycle steal diagnostic operations

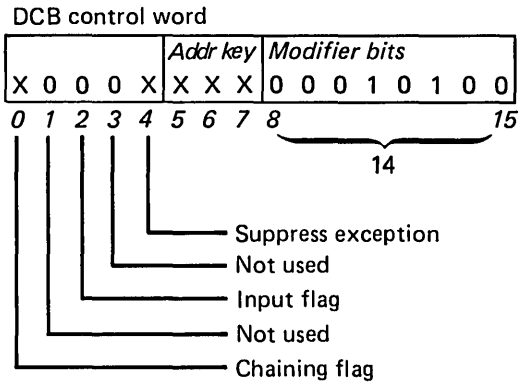
Command type	Function IDCB CMD FIELD=0111 1101 DCB control word bit 2	(I/F)	DCB device dependent field
Write	Attachment diagnostic write test	0	0001 0100
	Common adapter write FCB diag	0	0010 0000
	Common adapter diag/patch	0	0010 0110
	Common adapter data buff diag	0	0010 0111
	Write cache diag	0	0010 0011
Read	Attachment ROS diagnostic	1	0001 0010
	Common adapter data buff diag	1	0001 0011
	Attachment diagnostic read test	1	0001 0111
	Diagnostic word 1	1	1000 1000
	Diagnostic word 2	1	1000 1001
	Read cache diag	1	0010 0001
	Common adapter read FCB diag	1	0010 0010

Note: A delayed command reject returns for these diagnostic operations if any other disk units have an operation in progress. The SE and chain bit options are not used for these diagnostic operations. Therefore, the SE and chain bits are ignored.

Attachment Diagnostic Write Test

This diagnostic test exercises the attachment high speed data bus in the write direction. When this operation is processed, the attachment card is isolated electrically from the disk unit controls. The attachment card cycle-steals words from main storage beginning at the DCB data address and continues until the byte count is 0. Use even byte counts.

The data is checked only for parity errors. If a parity error occurs for any of the words transferred, the attachment card presents an exception interrupt. The error appears as an equipment check in word 4 of the cycle-steal status block. A cycle-steal error on the data channel is reported in bits 4–7 of the ISB. The byte count must be an even number. If the byte count is odd, a DCB specification check is not generated. However, another error can occur. DCB word 0 format follows:



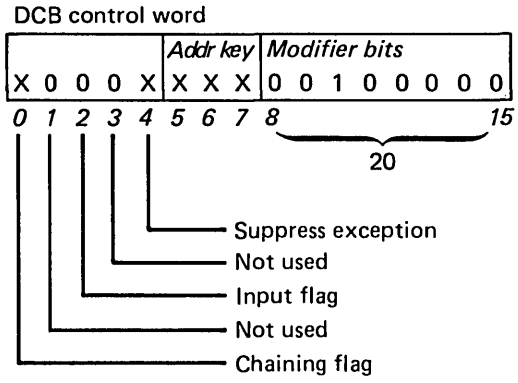
Common Adapter Write FCB Diagnostic

This diagnostic operation writes the file control block (FCB) for the selected disk unit into the common adapter FCB buffer area. Up to 16 FCB words can be written, depending upon the byte count in the DCB. The byte count can be any number between 2 and 32, inclusive. The FCB is written in ascending order, starting with FCB word 0. Bits 14 and 15 of DCB word 3 determine which disk unit FCB is written.

- 00 = disk unit 0
- 01 = disk unit 1
- 10 = disk unit 2
- 11 = disk unit 3.

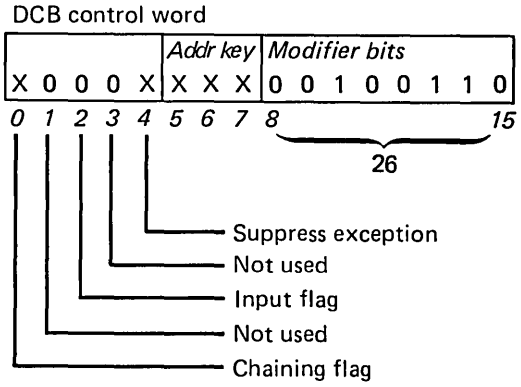
Note: If a byte count is larger than 32, the selected FCB wraps continuously until the byte count is 0. With the exception of requiring an even number, the byte count is not checked.

DCB word 0 format follows:



Write Common Adapter Diagnostic/Patch

This diagnostic command transmits predefined data to the common adapter for use as read only storage patch data or diagnostic program data. DCB word 0 format follows:



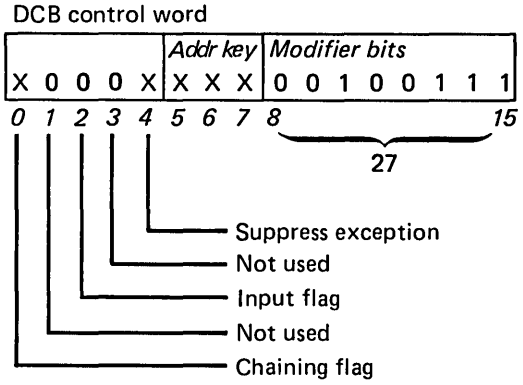
Write Common Adapter Data Buffer Diagnostic

This operation selectively cycle steals one 256-byte record to the selected common adapter data buffer from main storage. The DCB contains the data address, buffer number, and byte count needed for the operation. Byte count must be hex 100.

DCB word 3, bits 14 and 15, specifies the buffer number. DCB word 6 specifies the byte count.

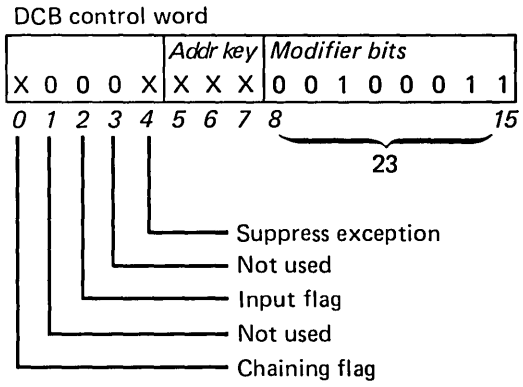
Valid buffer number	Byte count	Buffer being read
Word 3 (14-15)	Word 6	
00 (Read Only)	0100	FCB buffer area
01	0100	Data buffer area 1
10	0100	Data buffer area 2
11	0100	Data buffer area 3

DCB word 0 format follows:



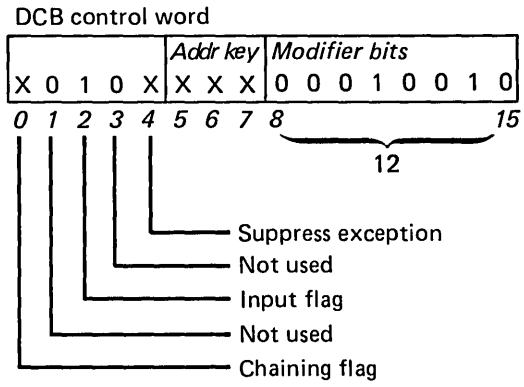
Write Cache Diagnostic

This command cycle steals data into the specified cache page. The DCB data address word contains the main storage starting address. The DCB byte count must be hex 0800. If it is not, a DCB specification check is not generated, but other errors can occur. The DCB record count field specifies the cache page number and should be in the range 0 to hex BF. Disable cache storage using the Write Cache Control command or the operation ends with a delayed command reject. DCB word 0 format follows:



Attachment Read Only Storage Diagnostic

This operation causes the attachment card to generate a checksum for each read only storage module and to cycle-steal six words (two for each module) into main storage. The first word is the reference checksum for read only storage module 1, and the second word is the calculated value for module 1. The next two words are for read only storage module 2, and the last two words are for read only storage module 3. Each set represents the referenced and calculated checksums for the respective read only storage module. Compare each set of words to see if any read only storage module is defective. An equal compare means the corresponding read only storage module is good. Set this byte count to decimal 12. An incorrect byte count generates a DCB specification check. DCB word 0 format follows:



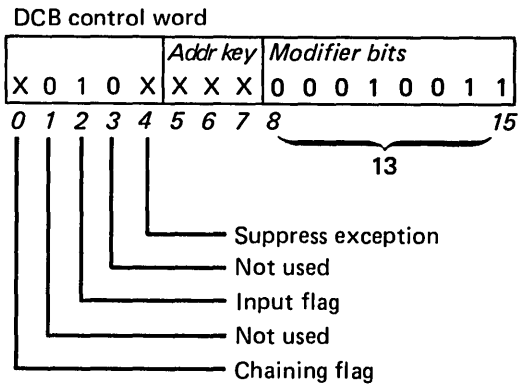
Read Common Adapter Data Buffer Diagnostic

This operation causes the attachment card to selectively cycle steal one 256-byte record from the selected common adapter data buffer to main storage. The DCB contains the data address, buffer number, and byte count needed for the operation. This byte count must be hex 100.

DCB word 3, bits 14 and 15 specify the buffer number. DCB word 6 specifies the byte count.

Valid buffer number	Byte count	Buffer being read
Word 3 (14-15)	Word 6	
00 (Read Only)	0100	FCB buffer area
01	0100	Data buffer area 1
10	0100	Data buffer area 2
11	0100	Data buffer area 3

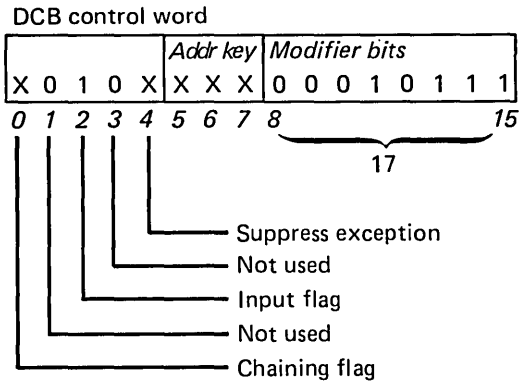
Organize DCB word 0 as follows:



Attachment Diagnostic Read Test

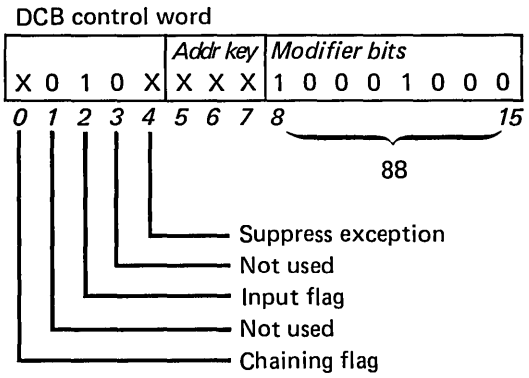
This diagnostic test exercises the attachment card high speed data bus in the read direction. The DCB byte count specifies the number of bytes stored in main storage, beginning at the data address location in the DCB. The byte count must be even or the attachment card returns a DCB specification check to the processor. A minimum byte count of 256 is recommended.

When the operation completes, the first word in main storage at the data address location contains hex 0000, the second word hex 0101, the third word hex 0202, and so on. Each byte in each word increases by one (modulo 256). The attachment card is electrically isolated from the disk unit common adapter during this operation. Organize the DCB word 0 as follows:



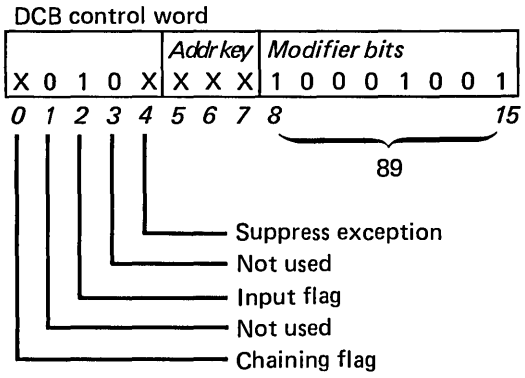
Read Diagnostic Word 1

This command cycle steals a word from the disk unit control data buffer register to the location indicated by the DCB data address. The byte count must be hex 2. If it is not, a DCB specification check is not generated, but other errors can occur. The DCB word 0 format follows:



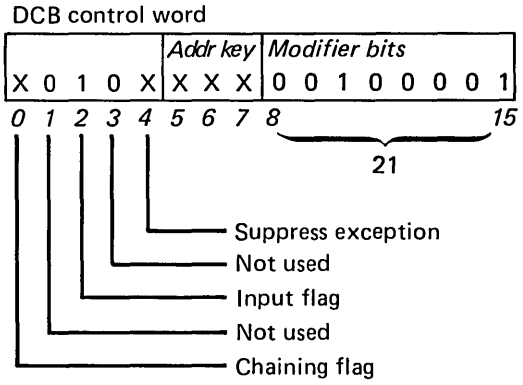
Read Diagnostic Word 2

This command cycle steals a word from disk unit control data buffer register to the location indicated by the DCB data address. The byte count must be hex 2. If it is not, a DCB specification check is not generated, but other errors can occur. The DCB word 0 format follows:



Read Cache Diagnostic

This command cycle steals data from the specified cache page into main storage, starting at the location contained in the DCB data address. The DCB byte count must be hex 0800. If it is not, a DCB specification check is not generated, but other errors can occur. The DCB record count field contains the cache page number, in the range 0 to hex BF. The DCB word 0 format follows:



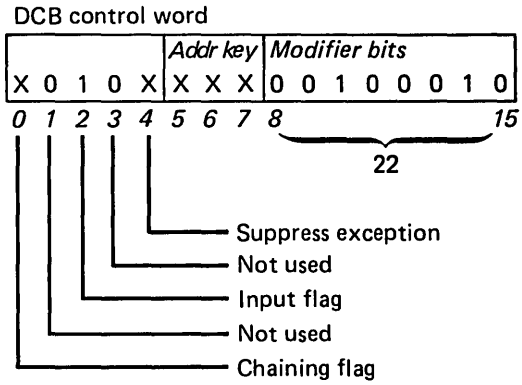
Common Adapter Read FCB Diagnostic

Use this diagnostic operation to read the selected disk unit FCB. Up to 16 FCB words can be read, depending upon the DCB byte count. The byte count can be any number between 2 and 32, inclusive. The FCB is read in ascending order, starting with FCB word 0. Bits 14 and 15 of DCB word 3 select the disk unit FCB to be read.

- 00 = disk unit 0
- 01 = disk unit 1
- 10 = disk unit 2
- 11 = disk unit 3.

Note: If the byte count is larger than 32, the selected FCB wraps continuously until the byte count is 0. The byte count must be an even number. If it is not, a DCB specification check is not generated, but other errors can occur.

DCB word 0 format follows:



Start Cycle-Steal Status

The Start Cycle-Steal Status command causes 14 words of status information to be transferred, in cycle-steal mode, from the 4967 to processor storage. The information is used to determine the status of an operation that did not process correctly.

All DCB words are transferred. However, only the control word, byte count, and data address are used. The SE bit and chain bit are ignored, since these options are not applicable to a Start Cycle-Steal Status command.

For this operation, the IDCB structure follows:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 1 1 1 1	X X X X X X X X
0 *7*	*8* *15*
7F	00–FF

Immediate data field
DCB address
16 *31*

The DCB format follows:

DCB (device control block)

Word	*0* *15*
0	Control word
1	Not used (0's)
2	Not used (0's)
3	Not used (0's)
4	Not used (0's)
5	DCB chaining address
6	Byte count
7	Data address
	0 *15*

DCB Word 0—Control Word

The control word (word 0) bits are:

- Bit 0—Chaining flag
- Bit 1— Not used; set to 0
- Bit 2—Input flag
- Bit 3— Not used; set to 0
- Bit 4—Suppress exception
- Bits 5–7—Cycle-steal address key
- Bits 8–15— Not used

DCB Word 1

Not used

DCB Word 2

Not used

DCB Word 3

Not used

DCB Word 4

Not used

DCB Word 5—Chaining Address

This word contains the next DCB address for chaining operations.

DCB Word 6—Byte Count

This word contains the transfer byte count. If DCB word 6 is not hex 001C, a DCB specification check occurs.

DCB Word 7—Data Address

This word contains the storage address for the start of the data to be transferred.

Cycle-Steal Status Words

The 14 cycle-steal status words the Start Cycle-Steal Status command transfers are organized as follows:

Cycle-steal status words

Word	0 — 15
0	Residual address
1	Residual count
2	Error status
3	Error status
4	Error status
5	Error status
6	Cache information word
7	Scan information word
8	Last DCB address
9	Last RBA
10	Last RBA
11	Disk unit diag sense bytes 1 and 2
12	Disk unit sense byte 3 and wrap
13	Attachment diagnostic word
	0 — 15

A description follows of the words transferred to main storage, starting with word 0. In case of a disk unit interface parity check error, the status words returned pertaining to the disk and common adapter may not be valid.

Cycle-Steal Status Word 0 - Residual Address

This word contains the residual address that is the highest main storage address of the last cycle-steal transfer successfully completed or attempted during the last cycle-stealing operation. This address is not updated during a Start Cycle-Steal Status command.

The residual address may be a data address, a DCB address, or an RSB address. The meaning of the residual address depends upon the type of operation invoked.

For a read operation, the residual address points to the last byte stored in main storage. This word could be data or a word of the RSB.

For a write operation, the residual address contains the address of the last byte fetched from main storage. Cycle-steal status words 9 and 10 determine the last sector written on the disk. If a hard error occurs before the attachment card issues an operation to the disk unit, the residual address points to the low order byte of the error word of the DCB for all commands. An example of this would be a DCB specification check. The residual address does not necessarily represent the highest storage address accessed if the SE bit is set to 1, because previous ERP retries could have failed at a higher storage address.

Cycle-Steal Status Word 1 - Residual Count

This word contains the residual byte count of data requested for the last DCB operation. This count reflects the number of bytes of data not transferred by the last operation that can be retried, or the last individual operation if none can be retried.

Cycle-Steal Status Word 2 - Error Status

This word contains soft error retry counts. The bit field assignments follow:

Bits 0-3 CRC/ECC check

Bits 4-7 Write gate return check

Bits 8-11 Sector sync/format

Bit 12 Data unsafe

Bit 13 Disk not ready

Bit 14 ECC invoked

Bit 15 Any soft error retry

Cycle-Steal Status Word 3 - Error Status

This word is an extension of the soft error retry counts and contains some hard error bits. The bit field assignments follow:

Bits 0-3 No record found (soft error retries)

Bit 4 Storage data check (soft error retry)

Bit 5 Invalid storage address (soft error retry)

Bit 6 Protect check

Bit 7 Interface data check (soft error retry)

Bit 8 Attachment interface parity check (soft error retry)

Bit 9 Common adapter clock out of synchronization

Bit 10 Common adapter read only storage parity check

Bit 11 Sector synchronization parity check

Bit 12 Common adapter storage parity check

Bit 13 Storage patch rejected

Bits 14-15 Write error (soft error retries)

Cycle-Steal Status Word 4 - Error Status

The format of this word follows:

Bit 0 Hard Error

This bit is set to 1 when a hard error occurs. The hard error causes the operation to end, and an exception interrupt is presented. If the SE bit is set to 0, any error causes this bit to be set to 1.

Bit 1 Attachment Detected Interface Parity Check

This bit is set to 1 when the attachment card detects a parity error on either the data bus or the tag bus interface between the disk unit common adapter and the attachment card.

Bit 2 Attachment Global Time Out

This bit is set to 1 when an operation takes too long (approximately 15-30 seconds). An exception interrupt is presented.

Bit 3 Attachment Interface Cable Continuity Check

This bit is set to 1 when the attachment card interface cables are detached or broken.

Bit 4 Attachment Detected Premature End

This bit is set to 1 when the disk unit controller ends an operation prematurely. The controller can present another error in the status to define this condition. Premature end is a redundant error check to ensure that defective cache data is not sent to the system.

Bit 5 Disk Unit Not Attached

Bit 6 Attachment Equipment Check

This bit is set to 1 when the attachment card detects a hardware error.

Bit 7 Write Error

This bit is set to 1 if a hard ECC error occurs on a write with read verify operation. If the suppress exception (SE) bit is set to 1, the write operation is retried up to three times before this write error is presented.

Bit 8 SERDES or Storage Parity Error

Bit 9 Data Buffer/Internal Card-Parity Error

Bit 10 Channel Error Check

Bit 11 ECC Inverted

Bit 12 Cycle-Steal Status Error

This bit set to 1 indicates that an error occurred while processing a Start Cycle-Steal Status command.

> **Note:** Attachment status is valid; disk status cannot be guaranteed.

Bit 13 End of Disk

This bit is set to 1 when a disk unit operation causes automatic cylinder switching into the CE cylinder (cylinder number 570).

Bit 14 Attachment Local Time Out

This bit is set to 1 when the attachment card senses that an interface handshake sequence takes too long (approximately 2–5 seconds) or fails to complete. This time-out condition can be considered a form of equipment check.

Bit 15 Disk Interface Error

This bit is set to 1 for any of four conditions:

- Cable open
- Missing control sample
- Daisy bus parity check in the disk unit is detected
- Interrupt not reset after a sense.

Further information about bit 15 can be obtained from cycle-steal status word 12, bits 8-11:

Bit 8 Disk cable continuity

Bit 9 Disk unit-no control sample received

Bit 10 Disk unit-daisy bus parity check (inbound)

Bit 11 Disk unit-interrupt not reset after a sense

Cycle Steal Status Word 5 - Error Status

The format of this word follows:

Bit 0 CRC/ECC Check

This bit is set to 1 if a command finds a sector ID or record that causes a hard CRC check during a read function. If the SE bit is set to 1, the error is retried eight times before being presented as a hard error. A CRC check occurring on an ID field during an ID search is presented as a no record found.

Bit 1 Tag Out Parity Check

This bit is set to 1 if a data channel tag bus parity check in the disk unit controls is detected.

Bit 2 Channel Data Parity Error

This bit is set to 1 when the disk unit control detects a parity error on the data channel bus on the interface between the disk unit controls and the attachment card.

This check cannot be retried by the disk unit controls.

Bit 3 Write Gate Return Check

This bit is set to 1 when 'write gate' is active in the disk unit control, but is not active in the disk unit. The error is retryable if the SE bit is set to 1 and is retried four times before being presented as a hard error.

Bit 4 No Record Found

This bit is set to 1 if the addressed sector being searched for cannot be found within one revolution, and either the retry count has been exhausted or the SE bit is set to 0. This error is retried eight times if the SE bit is set to 1.

Bit 5 Invalid Command Parameter

This bit is set to 1 when the disk unit controls detect an invalid command parameter. The conditions that set this bit to 1 follow:

- Invalid command byte
- Byte count greater than 0300 hex or 768 decimal for Read ID, Write ID, Read Diagnostic commands
- Record number greater than 4095 for Read/Write/Scan commands (DCB word 1)
- Sector number greater than 49 for Read ID/Write ID/Read Diagnostics commands. (DCB word 1)

Bit 6 Sector or Format Check

This bit is set to 1 if missing or extraneous sector pulses occur between normal sector pulse intervals. The format check logic is active whenever a sector pulse occurs during a read or write operation. If the SE bit is set to 1, an error is retried eight times before being presented as a hard error.

Bit 7 Disk Unit Time-Out or Hardware Check

This bit is set to 1 when either a time-out period has elapsed and an operation is not complete or an abnormal hardware condition is detected. When this bit is set to 1, an exception interrupt occurs. This bit condition is generated by the disk unit controls and is independent of the attachment card time-out, bit 2, status word 4.

Further specific information can be obtained from word 12, bits 12–15.

Bit 12 Disk unit interrupt not received

Bit 13 Common adapter did not receive an expected interrupt from the R/W hardware

Bit 14 Code carried out by the controller in an unused read-only storage location or inconsistent hardware were detected

Bit 15 Buffer port address check

Bit 8 Disk Unit Not Attached

This bit is set to 1 when a command is issued to an unattached disk unit.

Bit 9 Brake Applied

This bit is set to 1 when an error occurs that causes the disk brake to be applied while the drive motor power is present.

Bit 10 Head/Track Unavailable

This bit is set to 1 when an access request specifies a non-existent cylinder (between cylinder 573 and 1023) or a non-existent head number (14 or 15).

Bit 11 Disk Unit Command Error

This bit is set to 1 if the disk unit encounters an illegal tag code or a parity error on either the control bus or the tag lines.

Bit 12 Data Unsafe

This bit set to 1 indicates that certain failures have occurred that may cause loss of customer data.

The error is retried only once.

Bit 13 Seek Incomplete

This bit set to 1 reflects access motion in progress.

Bit 14 Home

This bit is set to 1 after a successful power-up sequence or recalibrate operation to the disk unit. The heads are at cylinder 0, head 0.

Bit 15 Not Ready

This bit set to 1 indicates the disk unit is not in the ready condition.

Cycle-Steal Status Word 6 - Cache Information Word

Bit 0 Operation end interrupt received

Bit 1 Data operation ready interrupt received

Bit 2 Cache write through

Bit 3 Cache prefetch invoked

Bit 4 Cache enabled

Bits 5-7 Cache status/failing cache module

These bits have a dual definition. Under error-free conditions, these bits have the following meanings:

Bit 5 Cache used for this operation

Bit 6 Total read hit

Bit 7 Cache installed (always = 1)

However, immediately following the processing of the cache diagnostic test operation, these bits have meanings described in "Direct Program Control."

Bits 8-15 Read Hit Ratio Percentage (BCD Coded)

For example, 75 percent is coded as bits 8-15 = 0111 0101, and 100 percent is 1010 0000.

If defective cache storage causes an equipment check, the byte contains hex BC.

Cycle-Steal Status Word 7 - Scan Information Word

Bits 0 Reserved

Bits 1-3 1 2 3

0 0 0 (2CA or 2CB)
0 0 1 (3CA or 3CB)
0 1 0 Reserved
1 0 0 Reserved
1 0 1 Reserved
1 1 0 Reserved
1 1 1 Reserved

Bit 4 Scan not hit

Bit 5 Scan equal hit

Bit 6 Scan high compare

Bit 7 Scan low compare

Bits 8-15 Scan hit count

This count indicates the displacement length (in bytes) following the key argument hit, from the beginning of the record to the beginning of the data.

Cycle-Steal Status Word 8 - Last DCB Address

This word contains the starting address of the last DCB used by the attachment card.

Cycle-Steal Status Words 9-10 - Logical Record Number

These two words contain the RBA of the last record processed unless ECC invoked or head offset invoked.

Condition	Value
ECC invoked	Last ECC records RBA
Head offset invoked	Last head offset records RBA
Both	Last ECC records RBA
Neither	RBA of last record accessed

Word 9, bits 11-15 are the high order 5 bits of RBA

Word 10, bits 0-15 are the low order 16 bits of RBA

Cycle-Steal Status Word 11 - Disk Unit Diag Sense Bytes 1 and 2

Sense diagnostic byte 1 is contained in the high order byte and sense diagnostic byte 2 is contained in the low-order byte. The following is a tabulation of the sense bits contained in diagnostic sense bytes 1 and 2.

Note:

- A sense bit cannot be used individually.
- Each sense bit relates only to other sense bits.
- Diagnostic sense information can be processed only through the maintenance analysis procedures.

Diagnostic Sense Byte 1

BITS
0 1 2

1 1 1 Power not good
1 0 1 Disk speed/VCO check
1 1 0 PLO out of sync
1 0 0 Seek time-out error
0 1 1 Unexpected guard band
0 1 0 Servo off-track error
0 0 1 Guard band 2
0 0 0 System service request (not an error)

Bit 3 On track
Bit 4 Guard band

BITS
5 6

1 0 Crossing tracks inward
0 1 Crossing tracks outward
0 0 Captured on track or retracted
1 1 Not used

Bit 7 Interrupt

Diagnostic Sense Byte 2

Bit 0 - Odd track
1 - Access reset
2 - Depress profile
3 - Accelerate
4 - Not used
5 - Not used
6 - Not used
7 - Retract

Cycle-Steal Status Word 12 - Disk Unit Diagnostic Sense Byte 3 and Wrap Byte

Diagnostic sense byte 3 is contained in the high order byte and diagnostic wrap byte is contained in the low order byte.

Diagnostic sense byte 3, bits 0, 1, and 2

0 1 2

0 0 0 Write and not ready
0 0 1 Write and servo not on track
0 1 0 Write and sector overrun
0 1 1 Write and read or write and head off servo
1 0 0 Access electronics (AE) unsafe w/o AE selected
1 0 1 Write and AE select error
1 1 0 Not write and AE unsafe w/AE selected
1 1 1 Write and AE unsafe

Bits 3-4 Used to identify data unsafe when bits 0, 1, and 2 are 0's

Bit 5 Not used

Bit 6 Sector counter error

Bit 7 Card/cable unseated

Bits 8-15 The disk unit diagnostic wrap byte is placed into this location when transferred from the disk.

If cycle-steal status word 5, bit 7 is set to 1, bits 12–15 have the following meaning:

Bit 12: Disk unit interrupt not received
Bit 13: Read or write hardware time out
Bit 14: Hardware check
Bit 15: Buffer port address check

If cycle-steal status word 4, bit 15 is set to 1, bits 8–11 have the following meaning:

Bit 8: Disk unit cable continuity check
Bit 9: No control sample received from disk unit
Bit 10: Disk unit daisy bus parity error
Bit 11: Disk unit interrupt not reset after sense

Cycle-Steal Status Word 13 - Attachment Diagnostic Word

This word contains diagnostic information used in the intermittent failure strategy (see "Intermittent Strategy" in the *IBM Series 1 4967 High-Performance Disk Subsystem Maintenance Information Manual*, SY34-0249).

Bits 0-2 Failure path

Bits 3-7 Number of disabled cache pages

Bits 8-15 Error modifier

Attachment Status Reporting

The types of status information the attachment card presents to inform the processor of the results of an I/O operation follow:

- Condition codes (Operate I/O and priority interrupt)
- Interrupt status information
- Start Cycle-Steal Status (defined previously)
- Start Cycle-Steal Diagnostic (defined previously)

Condition Codes

Operate I/O Condition Codes

The attachment card or the data channel reports the condition code after completion of the Operate I/O instruction. Condition codes are recorded in the even, carry, and overflow indicators of the level status register (LSR).

Operate I/O condition codes presented after an I/O instruction follow:

Mode	Command	Condition code value 0	1	2	3	4	5	6	7
DPC	Prepare	X	N	N	N	N	X	N	X
DPC	Device Reset	X	N	N	N	N	N	N	X
DPC	Read Device ID	X	N	N	N	N	X	N	X
CS	Start	X	X	X	N	N	X	X	X
CS	Start Cycle Steal Status	X	X	X	N	N	X	X	X
CS	Start Cycle Steal Diagnostic	X	X	X	N	N	X	X	X
CS	Start Cycle Steal Controller	X	X	X	N	N	X	X	X

An "X" in the appropriate position means the condition code may be reported in response to an Operate I/O instruction. The "N" means that the condition code value is not reported and has the binary value 0. The condition code is mutually exclusive and has a priority sequence. That is, CC0 has the highest priority and is reported first. CC1 has the second highest priority and is reported second, and so on, sequentially, through all the condition codes.

The meaning of the condition codes presented while processing the Operate I/O instruction follow:

I/O Instruction condition codes

Condition code (CC) value	LSR position			Reported by	Meaning
	Even	Carry	Over-flow		
0	0	0	0	Channel	Device not attached
1	0	0	1	Att	Busy
2	0	1	0	Att	Busy after reset
3	0	1	1	Att	Command reject
4	1	0	0		Not used
5	1	0	1	Chan/Att	Interface data check
6	1	1	0	Att	Controller busy
7	1	1	1	Att	Satisfactory

CC0- Device not attached

Reported by the data channel when the addressed disk unit is not attached.

CC1- Busy

Reported by the disk unit when it is unable to process a command because it is in the busy state. The disk unit enters the busy state upon acceptance of a command that requires an interrupt for termination. The disk unit exits the busy state when the attachment card accepts the interrupt. When CC1 is reported, a subsequent priority interrupt from the disk unit always occurs.

CC2- Busy after reset

Reported by the disk unit when it is unable to process a command because of a reset pending. There is no interrupt to indicate end of this condition.

CC3- Command reject

Reported when the IDCB contains an incorrect parameter, such as an odd-byte DCB address, or an incorrect function/modifier combination. When the disk unit reports a command reject, it does not fetch the DCB.

> **Note:** When a user issues a DPC Read command, the attachment card loads its ID word into the immediate data field of the IDCB associated with the command.

CC4

Not used.

CC5- Interface data check

Reported by the attachment card or data channel when a parity error is detected on the data channel during a data transfer.

CC6- Controller busy

Reported when the controller is processing the IDCB of the last Operate I/O instruction. Another Operate I/O instruction is sent to a different disk unit address also processed by this controller. The system continues to loop on the affected Operate I/O instruction until CC6 is no longer reported.

> **Note:** The duration of a controller busy condition is short and the system may never experience a CC6 under normal operating conditions.

CC7- Satisfactory

Reported when the attachment card accepts the command.

Interrupt Condition Codes

The following condition codes are reported to the processor upon presentation of a priority interrupt request:

Interrupt condition codes

Condition code (CC) value	LSR position			Reported by	Meaning
	Even	Carry	Over-flow		
0	0	0	0		Not used
1	0	0	1		Not used
2	0	1	0	Attachment	Exception
3	0	1	1	Attachment	Device end
4	1	0	0	Attachment	Attention
5	1	0	1		Not used
6	1	1	0	Attachment	Attention and exception
7	1	1	1	Attachment	Attention and device end

CC1 — Not used.

CC2- Exception — Reported when an error or exception condition is associated with the interrupt. The error or exception condition is described in the interrupt status byte or in the device-dependent status words.

CC3- Device end — Reported when no exception or attention condition occurs during an I/O operation.

CC4- Attention — Reported when the disk unit is ready and a previous command ended with not ready (cycle-steal status word 5, bit 15). The attachment card also reports this condition code after a successful IPL (initial program load) and is followed with a Prepare command with no intermediate resets.

CC5 — Not used.

CC6- Attention and exception — Reported when attention and exception are both present.

CC7- Attention and device end — Reported when attention and device end are both present.

IIB Indicators

The 4967 attachment card provides the IIB on attention or device end interrupts. The IIB contains all 0's on an attention interrupt (CC4). On a device end interrupt (CC3) or (CC7), the following IIB information may be presented.

Bit 0 - Permissive Device End: When this bit is set to 1, it indicates that soft error information is available in an RSB. For DCB chaining, this bit indicates that at least one of the RSBs stored has soft error information. This bit is set to 1 if at least one DCB in the chain used the SE bit option. The resulting RSB indicates a soft error retry.

Bit 1 - Scan Not Hit: This bit set to 1 indicates the scan condition requested was not met.

Bit 2 - Scan Equal Hit: This bit set to 1 indicates the scan condition requested resulted in an equal hit.

Bit 3 - Scan High Compare: This bit set to 1 indicates the scan condition requested resulted in the disk unit data being greater than the key argument.

Bit 4 - Scan Low Compare: This bit set to 1 indicates the scan condition requested resulted in the disk unit data being less than the key argument.

> **Note:** The above four bits (IIB 1 through 4) pertain only to the last DCB carried out. If a scan operation is located within a chain of DCBs, the results of that operation are available in an RSB. Ensure the associated DCBs for the scan operation has its SE bit to 1.

Bits 5-7: Not used. Bits are 0 at interrupt time.

ISB Error Indications

The 4967 attachment card sends the ISB on an exception interrupt (CC 2) or attention and exception interrupt (CC 6) presentation. Multiple ISB bits can be set to 1 at the same time.

Bit 0 - Device Dependent Status Available: This bit indicates that further attachment card status information is available in the cycle-steal status block. To obtain this information, issue a Start Cycle-Steal Status command.

Bit 1 - Delayed Command Reject: This bit indicates that an incorrect parameter is in the IDCB, such as an odd-byte DCB address or an incorrect function or modifier field. This bit is also set to 1 if a DPC command is issued outside of the 4967 command set. A diagnostic operation issued to a disk unit other than disk unit 0, or other busy disk units, is also rejected with this bit set to 1. This bit is set to 1 in the ISB only when these error conditions cannot be recorded by CC3 (command reject) during the Operate I/O envelope. This bit is also set to 1 when a write ID is attempted and cache storage has not been disabled.

Bit 2 - Incorrect Length Record: Not used; must be 0.

Bit 3 - DCB Specification Check: This bit indicates that an invalid parameter was found in the DCB, preventing processing of this command. This bit could reside in any of the eight DCB words. The residual address in the cycle-steal status block points to the last byte of the word where the first error was found.

Bit 4 - Storage Data Check: Storage data check is set to 1 for cycle-steal output operations only. It indicates that the storage location accessed during the current output cycle contained a parity error. The parity in main storage is not corrected. No machine check condition occurs. See Note.

Bit 5 - Invalid Storage Address: This bit is set to 1 as a result of a cycle-steal operation or a DCB when accessing beyond the system's main storage. The operation is then immediately ended. See Note.

Bit 6 - Protect Check: The attachment card attempted to access a main storage location without the correct key. See Note.

Bit 7 - Interface Data Check: A parity error was detected on the I/O interface during a cycle-steal data transfer. Either the attachment card or the data channel can detect this condition.

> **Note:** The attachment card retries the specified operation one time for these four error states if SE bit is set to 1. If the operation fails a second time, a hard error condition is presented (CC2 or CC6), and the appropriate ISB bit is set to 1. If the retry procedure is successful, a permissive device end is presented in the IIB. The previous error is indicated in the RSB returned to main storage at the end of the operation. The retry procedure is not performed when the SE bit is set to 0.

Residual Status Block (RSB)

When the SE bit is set to 1, a RSB of information returns to the user. When the SE bit in the DCB control word is set to 1, the RSB is stored at the address specified in the DCB word 4 when the operation completes. The attachment card forces a cycle-steal address key of hex 000 when it stores the RSB. It does not store RSB information when it detects a hard error condition, even if the SE bit is set to 1.

The attachment card stores an RSB for each DCB whenever the SE bit is set to 1, whether or not the DCB is chained. If an exception interrupt occurs, no RSB is stored for that DCB. Any status from that exception is available in the either the ISB or the cycle-steal status block, or both. If the RSB logs soft error retries, and an exception interrupt occurs, the program can obtain the soft error counters and hard error information for the last DCB from the cycle-steal status block.

If a DCB or chain of DCBs ends with no exception interrupt, IIB bit 0 indicates the presence of soft error retry information in any RSB of that chain. IIB bit 0 is an accumulative bit for all RSB soft error information in the DCB chain. For an exception end, no IIB is available. Therefore, previous RSBs of the chained operations that caused the hard error must be searched for soft error information. Word 1, bit 1, of each RSB or cycle-steal status block indicates whether or not soft error information is available for the associated DCB.

The format of the RSB follows:

Residual status block (RSB)

Word	0 — 15
0	Residual count
1	RSS flags
2	Retry counts word 1
3	Retry counts word 2
4	Cache information word
5	Scan information word

The meanings of RSB words follow.

Residual Status Block Word 0 - Logical Record Number: This word contains the low order 16 bits of the RBA of the last record processed unless ECC invoked or head offset invoked. Word 5 contains the high order bits.

Residual Status Block Word 1 - RSB Flags: This word presents status bits consistent with I/O architecture. Specifically:

Bit 0 End of chain

Bit 1 Retry

Bits 2-14 Not used

Bit 15 No exception

Residual Status Block Word 2 - Retry Counts Word 1: This word contains the soft error retry counts. The error conditions each have four-bit fields to contain the counts. The bit field assignments follows:

Bits 0-7 CRC check

Bits 4-7 Write gate return check

Bits 8-11 Sector/format check

Bit 12 Data unsafe

Bit 13 Not ready

Bit 14 ECC invoked

Bit 15 Soft error retry

Residual Status Block Word 3 - Retry Counts Word 2: This word is an extension of the soft error retry counts. The bit field assignments follow:

Bits 0-3 No record found

Bit 4 Storage data check

Bit 5 Invalid storage address

Bit 6 Protect check

Bit 7 Interface data check

Bit 8 Disk unit interface parity check

Bits 9-11 Not used

Bit 12 Highest bit of the RBA

Bit 13 Head offset invoked

Bits 14-15 Write error

Residual Status Block Word 4 - Cache Information Word

Bit 0 Operation end interrupt received

Bit 1 Data operation ready interrupt received

Bit 2 Write through

Bit 3 Pre-fetch invoked

Bit 4 Cache storage enabled

Bit 5 Cache storage used for this operation

Bit 6 Total read hit

Bit 7 Cache storage installed (always 1)

Bits 8-15 Read hit ratio percent (BCD)

Residual Status Block Word 5 - Scan Information Word

Bits 0-3 High order four bits of the last logical record number

Bit 4 Scan Not Hit

This bit set to 1 indicates that the conditions of the requested operation were not met. See "Scan Operations."

Bit 5 Scan Equal Hit

This bit set to 1 indicates an equal condition between a scan argument and a key. See "Scan Operations."

Bit 6 Scan High Compare

This bit set to 1 indicates the disk data key is higher in value than the scan argument. See "Scan Operations."

Bit 7 Scan Low Compare

This bit set to 1 indicates that the disk data key is lower in value than the scan argument. See "Scan Operations."

Bits 8-15 Scan Hit Byte Count

These bits contain the byte displacement within the record where the scan hit occurred.

Initial Program Load (IPL)

The attachment card supports primary or alternate IPL from the first or second disk unit. Upon receiving the IPL signal, the attachment card issues a Recalibrate command to the selected disk unit. This positions the disk unit to RBA zero. If the given disk unit is not ready, the attachment card waits until the disk unit becomes ready before issuing the command.

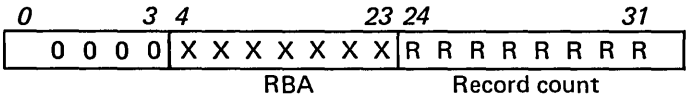
After recalibration, the attachment card issues a Read Disk Direct command for RBA 0, a byte count of 256, and a storage starting address of 0. If an error occurs during this read, the attachment card retries twenty times for both the recalibrate and the Read Disk Direct command. If all retries fail, the system hangs with the load light on.

> **Note:** The attachment card disables cache storage during the IPL procedure, and reenables the cache storage after IPL completes. This allows the user to IPL the system, even if the cache storage fails the power-on diagnostics. After IPL completes, the user has the option to disable the defective cache storage. We recommend enabling the cache storage at this time. A defective cache storage then appears on the next operation as an attachment equipment check (word 4, bit 6) with error modifier hex BC in word 6, bits 8-15. (See "Error Recovery Procedures" for more information). If this error occurs, to continue this operation, disable the cache storage. However, disk performance is degraded with the cache storage disabled.

Jumpers on the attachment card allow one of the following IPL configurations:

- Disk unit 0 is primary and disk unit 1 is alternate
- Disk unit 0 is alternate and disk unit 1 is primary
- Disk unit 0 is primary (alternate not supported)
- Disk unit 0 is alternate (primary not supported)
- Disk unit 1 is primary (alternate not supported)
- Disk unit 1 is alternate (primary not supported)
- IPL not supported

The attachment card transfers a maximum of 65,536 bytes of data (256 data records) into main storage. After the first data record of 256 bytes is transferred from RBA 0, the remaining data records can be fetched from the same or different RBA. After successfully transferring the 256-byte record into storage, the last two words transferred indicate if further records are required and where they are located. The format of the last two words follows:



- The RBA field specifies the starting record for reading the additional data records.

- The record count field specifies the number of additional data records to be read.

A zero record count indicates that no additional records will be read into main storage. With a record count of 255, a total of 65,536 bytes of data are read into main storage. The additional records are read beginning with the record specified by the RBA.

If a read error occurs after reading the first record, the total IPL is retried up to twenty times. Assigned alternates recover automatically. Heads and cylinders switch automatically as heads cross boundaries.

After an unsuccessful IPL, the system hangs with the load light on. If the IPL is successful, the Prepare command results in an attention interrupt, unless a Device Reset occurs prior to the Prepare.

Alternate Sector Assignment

After a consistent no record found or an ECC error, the sector ID or data field is considered defective. The two records associated with the defective sector must be recovered and assigned to an alternate sector. The original sector is flagged as defective, and all future references to the data are directed to the assigned alternate sector on the same cylinder.

> **Note:** Before assigning a sector to an alternate, try to restore the sector to an error-free condition by rewriting the data. If the data is read error-free after rewriting, the sector has been restored. If you cannot restore the sector, assign an alternate, and attempt to recover the data.

If the original sector developed its fault in the ID field, data recovery is accomplished using Read Data Recovery Record 1 and Read Data Recovery Record 2 commands. Faults developed in the data records themselves require reconstruction by backup or other means. The next available alternate is then located and rewritten with the ID (logical record only) and data of the original sector. The original ID error is then written as defective. Second, and future, errors are assigned in the same manner. There are 14 (maximum) alternate sectors per cylinder.

If the write ID operation fails due to the original defect, then the ID must be written into the data areas (record 1 and 2) for the full length of the data record (use write format).

The previous procedure must be contained in a system utility and it is also provided in the diagnostic utility program package.

User written programs designed for this function must implement the same type support to preserve the accuracy of the disk unit data.

> **Note:** If the original data fields cannot be recovered without an error, an inverted ECC must be written in the alternate sector. The inverted ECC serves as a flag to the user when he attempts to read the data in the alternate. The inverted ECC tells the user that the data is not correct and must be checked. Rewriting the data in the normal manner removes the inverted ECC.

Error Recovery

1. Inspect the Operate I/O condition code.

   a. If the Operate I/O condition code is 7 (satisfactory), go to step 2.

   b. If the Operate I/O condition code is 0, 1, 2, 3, 5, or 6, use the following charts.

Command	Operate I/O CC	Recommended action
Prepare	0	Exit the error-recovery procedure (device not attached).
	1,2,6	Exit the error-recovery procedure (equipment error).
	3	Examine the IDCB function modifier; exit the error-recovery procedure if the IDCB is correct.
	5	Retry three times; exit error-recovery procedure if problem persists.
Device Reset	0	Exit the error-recovery procedure (device not attached).
	1,2,6	Exit the error-recovery procedure (equipment error).
	3	Examine IDCB function modifier; exit the error-recovery procedure if the IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.
Halt I/O	0,1,3,5,6	Exit the error-recovery procedure (equipment error).
Read Device ID	0	Exit the error-recovery procedure (device not attached).
	1,2,6	Exit the error-recovery procedure (equipment error).
	3	Examine the IDCB function modifier; exit the error-recovery procedure if IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.
Attachment General Diagnostic, Attachment Cache Storage Diagnostic, Attachment Cache Storage Control, Load Diagnostic Word 1, Load Diagnostic Word 2	0	Exit the error-recovery procedure (device not attached).
	1,2,6	Exit the error-recovery procedure (equipment error).
	3	Examine the IDCB function modifier; exit the error-recovery procedure if IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.

Command	Operate I/O CC	Recommended action
Attachment Read Only Storage Diagnostic, Diagnostic Reset Common Adapter, Load Seek Address Direct	0	Exit the error-recovery procedure (device not attached).
	1,2,6	Exit the error-recovery procedure (equipment error).
	3	Examine the IDCB function modifier; exit the error-recovery procedure if IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.
Load Seek Control Direct, Sense Disk Unit Direct, Enable Data Collection Mode	0	Exit the error-recovery procedure (device not attached).
	1,2,6	Exit the error-recovery procedure (equipment error).
	3	Examine the IDCB function modifier; exit the error-recovery procedure if IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.

Command	Operate I/O CC	Recommended action
Start, Start Control	0	Exit the error-recovery procedure (device not attached).
	1	Issue a Device Reset; retry the failing operation. (The attachment may be busy when the retry occurs following a Device Reset command. Exit the error recovery procedure if the problem persists.
	2	Retry the operation three times. The attachment may be busy as a result of a Device Reset command. Exit the error-recovery procedure if the problem persists (equipment error).
	3	Examine the IDCB function modifiers; exit the error-recovery procedure if the IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.
	6	Retry until the command is accepted.
Start Diagnostic, Start Cycle Steal Status	0	Exit the error-recovery procedure (device not attached).
	1	Issue a Device Reset; retry the failing operation. (The attachment may be busy when the retry occurs following a Device Reset command. Exit the error recovery procedure if the problem persists.
	2	Retry the operation three times. The attachment may be busy as a result of a Device Reset command. Exit the error-recovery procedure if the problem persists (equipment error).
	3	Examine the IDCB function modifiers; exit the error-recovery procedure if the IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.
	6	Retry until the command is accepted.

2. Inspect the interrupt condition code.

   - If the interrupt condition code is 3 or 4, exit the error-recovery procedure.
   - If the interrupt condition code is 2 or 6, use the following charts.

Interrupt status byte (hex)	Recommended action
80	Issue a Start Cycle Steal Status command and go to step 3.
40	Retry the original operation. If still unsuccessful, perform an operator message and exit the error recovery procedure.
20	Not used.
10	Retry the original operation. If still unsuccessful, perform an operator message and exit the error recovery procedure.
08	Retry the original operation. If still unsuccessful, perform an operator message and exit the error recovery procedure.
04	Retry the original operation. If still unsuccessful, perform an operator message and exit the error recovery procedure.
02	Retry the original operation. If still unsuccessful, perform an operator message and exit the error recovery procedure.
01	Retry the original operation. If still unsuccessful, perform an operator message and exit the error recovery procedure.

3. Inspect the cycle-steal status word bits shown in the following chart. The chart lists the errors, the priorities in which they should be tested for, and the bit(s) to be tested. It also identifies the appropriate action to perform when an error is detected.

Bit(s) tested in cycle steal status word	Bit condition tested for	Priority	Recommended first action*	Error
Word 5, bit 12	1	1	1	Data unsafe
Word 5, bit 15	1	2	2	Not ready
All bits except Word 4, bit 13	1	3	3	All other hard errors except end of disk
Word 4, bit 13	1	4	4	End of disk

*Described in the following chart

Error conditions should be tested in order of priority (priority 1 is the highest). Begin the recovery sequence with the recommended action associated with the highest priority error detected.

Action	Description
1	Use procedures 1, 2, and 3 below
2	Use procedure 4 below
3	Use procedures 1, 2, and 3 below
4	Use procedure 5 below

1. Issue a Device Reset.

2. Issue a Recalibrate.

3. Retry the original operation. If still unsuccessful, perform an operator message, and exit the ERPs.

4. Make sure that the device is powered on and the Prepare command has been issued and wait for an attention interrupt. You may use an operator message here. Exit ERPs.

   Note: If the not ready condition occurred during an operation, status on the operation is available from other cycle-steal status words.

5. The ERP can take at least two different forms. The form used depends upon the reading of multiple records and how disk data is organized. If multiple sector reads or writes are sequentially organized and accessed between different drives, then the ERP calculates the next disk address, the starting record search argument, and the proper byte count. If this condition is not expected, then an error could exist in either the user program or the hardware. Therefore, perform step 1.

Notes:

1. The actions specify the ERP to be repeated once before issuing a hard error. A hard error requires intervention by a customer service representative.

2. Electrical conditions exist with duration greater than the ERP. The ERP retry ensures a hard error rather than a transient electrical condition.

3. When cache storage is enabled and the requested data is not found in cache storage, it can fetch more data than requested. If the prefetched data is defective, the operation ends and no data transfers to the system (see Read Data description). The defective disk sector should be rewritten or reassigned immediately. The operation can be retried using the the Read Disk Unit Direct command. This command disables cache storage and data is not prefetched. However, system performance is reduced. If the error sector is part of the prefetched data, then the retry will be successful.

   This extended ERP reduces disk performance if the defective sector is in the prefetch data since the attachment card performs retries and the system also performs retries. If the error sector is part of the requested data, then the Read Disk Unit Direct command also fails, and the sector must be assigned to an alternate.

4. During power-on diagnostics, the attachment card checks cache storage for defective pages. Background checking is also done. If 20 or fewer pages are defective, those pages are disabled for the duration of the power-on. The performance degradation caused by up to 20 defective cache pages is minimal. If the attachment card detects more than 20 defective cache pages, a flag is set, and any future operations (except Start Cycle-Steal Status) end with attachment equipment check bit set to 1 and bits 8-15, word 6, contain hex BC.

   Replace the defective attachment card. However, when degraded performance can be tolerated, the system can continue running without cache storage. The Write Cache Control command is used to disable the cache storage. Software must notify the system operator that this failure has occurred so that the attachment card can be replaced as soon as possible. A repeating message is suggested. Cache storage remains disabled until it is either re-enabled or a power-on, system reset, or Halt I/O occurs.

Off Line Maintenance

Each disk unit has its own power supply and power on/off switch, and can be powered off independently. If a disk unit without the controller is powered off, it responds not ready to attempted operations at the system level. If the disk unit containing the common adapter is powered off, disk units attached to that controller report not ready when the system attempts a disk unit operation.

Note: If the disk unit is switched on, and its associated interrupt prepare register is enabled, an attention interrupt may not be presented to the system. An attention interrupt is returned if not ready was given on a previous command, or if the attachment card was powered off and on.

For off line maintenance on any disk units, the entire sub system should be taken out of service.

The highest address disk unit terminates the daisy-chain cable with +5 volts.

Appendix A. Reference Summary

DPC Commands

Command	Hex
Prepare	20
Device Reset	6F
Read ID	20
Attachment Storage Diagnostic	4E
Attachment General Diagnostic	41
Attachment Cache Diagnostic	42
Load Seek Required Address Direct	52
Load Seek Control Direct	53
Sense Disk Unit Direct	54
Diagnostic Reset Common Adapter	4F
Write Cache Control	45
Enable Data Collection Mode	4C
Clear Error Log	43
Load Diagnostic Word 1	48
Load Diagnostic Word 2	49

Cycle-Steal Commands

Command	Hex
Start	70
Start Control	7C
Start Cycle-Steal Diagnostic	7D

Condition Codes

Operate I/O

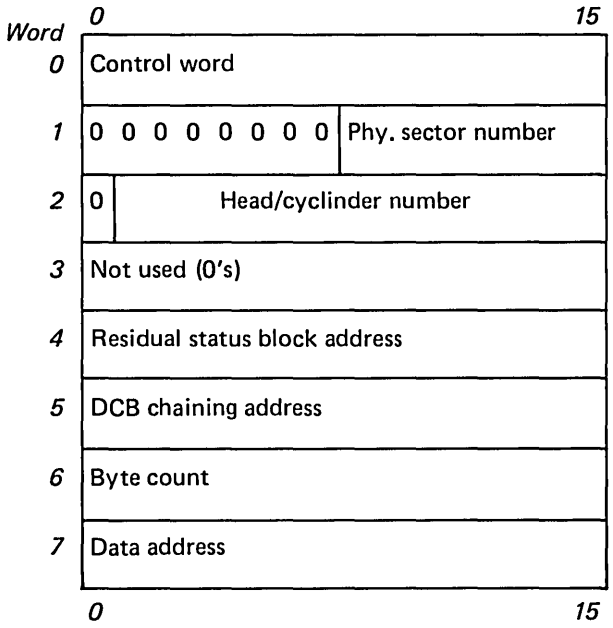
CC	Meaning
0	Device not attached
1	Busy
2	Busy after reset
3	Command reject
4	Not used
5	Interface data check
6	Controller busy
7	Satisfactory

Interrupt

CC	Meaning
0	Not used
1	Not used
2	Exception
3	Device end
4	Attention
5	Not used
6	Attention and exception
7	Attention and device end

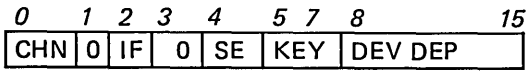
DCB Format (Physical Operations)

DCB (device control block)



Word 0 - Control Word

Control word



Bit 0 Chaining flag

Bit 1 Not used; must be 0

Bit 2 Input flag

Bit 3 Not used; must be 0

Bit 4 Suppress exception

Bits 5-7 Cycle-steal address key

Bits 8-15 Modifier bits

Recalibrate	00000001
Read Data Recovery Record 1	X0011110
Read Data Recovery Record 2	X0011111
Read ID	00010100
Write Format	X0100100
Write ID	00100101
Scan Alternate ID's	00110111

Word 1

Not used; set to 0's.

Word 2 - RBA

Contains the RBA on the disk where the operation begins.

Word 3 - Record Count

Contains the count for the total number of records involved with a scan or read/write operation.

Word 4 - RSB Address

Contains the address in main storage where the RSB is stored.

Word 5 - Chaining Address

Contains the address of the next DCB in a chaining operation.

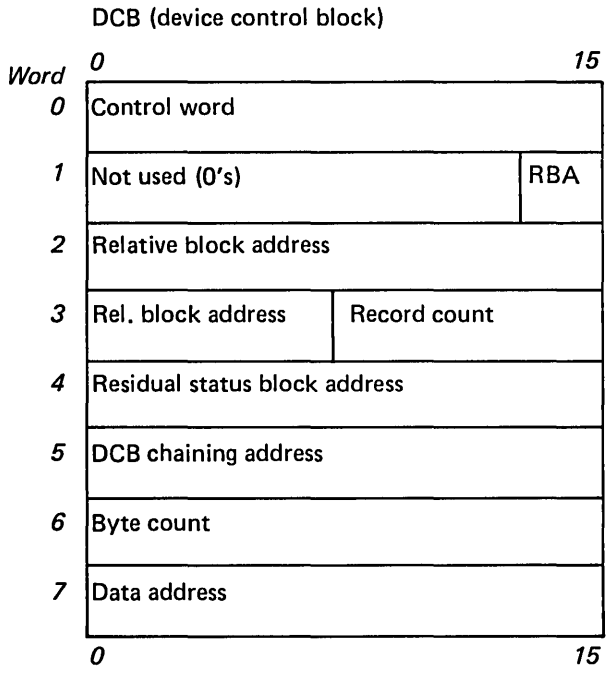
Word 6 - Byte Count

Contains the number of data bytes to be transferred for the current operation.

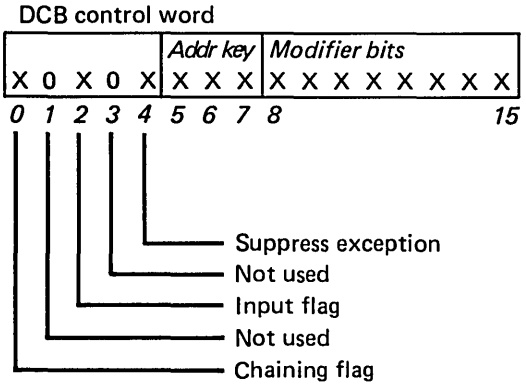
Word 7 - Data Address

Contains the address in main storage where the data transfer starts.

DCB Format (Logical Operations)



Word 0 - Control Word



Bit 0 Chaining flag

Bit 1 Not used; set to 0

Bit 2 Input flag

Bit 3 Not used; set to 0

Bit 4 Suppress exception

Bits 5-7 Cycle-steal address key

Bits 8-15 Modifier bits

Read Data	X0010000
Read Disk Unit Direct	X0011000
Read Verify	X0010001
Read Data Repeat	00010010
Write Data with Read Verify	X0100001
Write Data	X0100000
Write Data Repeat	00100010
Scan Read Single ID	00110110

Word 1

Bits 0–14 not used; set to 0's. Bit 15 is the highest RBA bit for models 3CA and 3CB.

Word 2 - RBA

Contains the RBA on the disk where the operation begins.

Word 3 - Record Count

Contains the count for the total number of records involved with a scan or read/write operation.

Word 4 - RSB Address

Contains the address in main storage where the RSB is stored.

Word 5 - Chaining Address

Contains the address of the next DCB in a chaining operation.

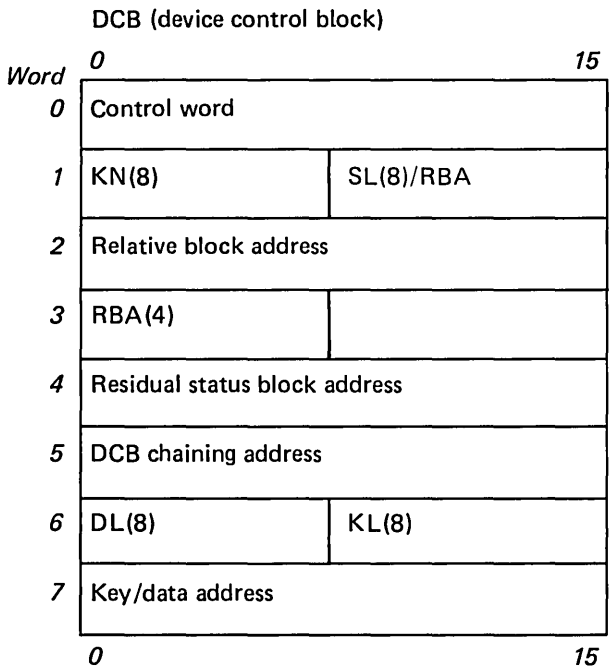
Word 6 - Byte Count

Contains the number of data bytes to be transferred for the current operation.

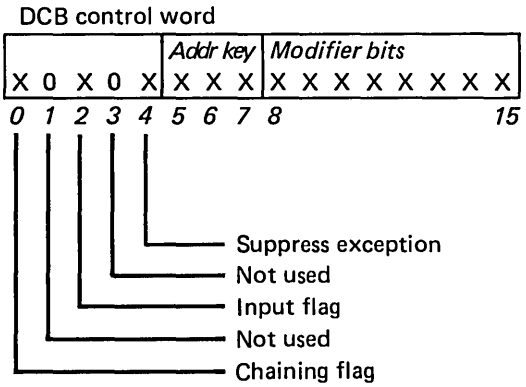
Word 7 - Data Address

Contains the address in main storage where the data transfer starts.

DCB Format (Scan Operations)



Word 0 - Control Word



Bit 0 Chaining flag

Bit 1 Not used; set to 0

Bit 2 Input flag

Bit 3 Not used; set to 0

Bit 4 Suppress exception

Bits 5-7 Cycle-steal address key

Bits 8-15 Modifier bits

Scan Data Equal	X0110000
Scan Data Not Equal	X0110001
Scan Data Low or Equal	X0110010
Scan Data Low	X0110011
Scan Data High or Equal	X0110100
Scan Data High	X0110101

Word 1

KN (bits 0-7)- Number of keys scanned in each record (256-byte record). Valid values are 0–127.

SL (bits 8-15)- Displacement from the beginning of the record to the first key to be scanned, specified in bytes, and must be even. Valid values are 0-254.

Bit 15 is highest RBA bit for models 3CA and 3CB.

Word 2 - RBA

Contains the low-order 16 bits of the RBA on the disk where the operation begins.

Word 3 - RBA

Bits 0–3 contain the high-order RBA bits. Bits 4–15 are not used and should be 0.

Word 4 - RSB Address

Contains the address in main storage where the RSB is stored.

Word 5 - Chaining Address

Contains the address of the next DCB in a chaining operation.

Word 6 - Data and Key Length

Bits 0–7 specify the data length (in even bytes) and bits 8–15 specify the key length (in even bytes). Valid values for the data length and key length are 2-254.

Word 7 - Key/Data Address

Contains the starting address of the key argument.

Cycle-Steal Status Words

Word 0 - Residual Address

Contains a data, DCB, or RSB address that is the highest main storage address of the last cycle-steal transfer.

Word 1 - Residual Count

Contains the residual byte count of requested data for the DCB operation.

Word 2 - Error Status

Contains soft error retry counts.

Bits 0-3	CRC/ECC check
Bits 4-7	Write gate return check
Bits 8-11	Sector sync/format
Bit 12	Data unsafe
Bit 13	Disk not ready
Bit 14	ECC invoked
Bit 15	Any soft error retry

Word 3 - Error Status

Contains an extension of the soft error retry counts and contains some hard error bits.

Bits 0-3	No record found (soft error retries)
Bit 4	Storage data check (soft error retry)
Bit 5	Invalid storage address (soft error retry)
Bit 6	Protect check
Bit 7	Interface data check (soft error retry)
Bit 8	Attachment interface parity check (soft error retry)
Bit 9	Common adapter clock out of synchronization
Bit 10	Common adapter read only storage parity check
Bit 11	Sector synchronization parity check
Bit 12	Common adapter storage parity check
Bit 13	Storage patch rejected
Bits 14-15	Write error (soft error retries)

Word 4 - Error Status

Bit 0	Hard error
Bit 1	Attachment detected interface parity check
Bit 2	Attachment global time out
Bit 3	Attachment interface cable continuity check
Bit 4	Attachment detected premature end
Bit 5	Disk unit not attached
Bit 6	Attachment equipment check
Bit 7	Write error
Bit 8	SERDES or storage parity error
Bit 9	Data buffer/internal card-parity error
Bit 10	Channel error check
Bit 11	ECC inverted
Bit 12	Cycle-steal status error
Bit 13	End of disk
Bit 14	Attachment local time out
Bit 15	Disk interface error

Word 5 - Error Status

Bit 0	CRC/ECC check
Bit 1	Tag out parity check
Bit 2	Channel data parity error
Bit 3	Write gate return check
Bit 4	No record found
Bit 5	Invalid command parameter
Bit 6	Sector or format check
Bit 7	Disk unit time-out or hardware check
Bit 8	Head offset invoked
Bit 9	Brake applied
Bit 10	Head/track unavailable
Bit 11	Disk unit command error
Bit 12	Data unsafe
Bit 13	Seek incomplete
Bit 14	Home
Bit 15	Not ready

Word 6 - Cache Information

Bit 0 Operation end interrupt received

Bit 1 Data operation ready interrupt received

Bit 2 Cache write through

Bit 3 Cache prefetch invoked

Bit 4 Cache enabled

Bits 5-7 Cache status/failing cache module

These bits have a dual definition. Under error-free conditions, these bits have the following meanings:

Bit 5 Cache used for this operation

Bit 6 Total read hit

Bit 7 Cache installed (always = 1)

However, immediately following the processing of the cache diagnostic test operation, these bits have meanings described in "Direct Program Control."

Bits 8-15 Read hit ratio percentage (BCD coded)

Word 7- Scan Information

Bit 0 Reserved

Bits	
1 2 3	
0 0 0	(2CA or 2CB)
0 0 1	(3CA or 3CB)
0 1 0	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

Bit 4 Scan not hit

Bit 5 Scan equal hit

Bit 6 Scan high compare

Bit 7 Scan low compare

Bits 8-15 Scan hit count

Word 8 - Last DCB Address

Words 9 and 10 - Logical Record Number

Contains the RBA of the last record processed unless ECC invoked or head offset invoked.

Word 11 - Disk Unit Diagnostic Sense Bytes 1 and 2

Diagnostic Sense Byte 1

Bits 0 1 2	
1 1 1	Power not good
1 0 1	Disk speed/VCO check
1 1 0	PLO out of sync
1 0 0	Seek time-out error
0 1 1	Unexpected guard band
0 1 0	Servo off-track error
0 0 1	Guard band 2
0 0 0	System service request (not an error)

Bit 3 On track

Bit 4 Guard band

Bits 5 6	
1 0	Crossing tracks inward
0 1	Crossing tracks outward
0 0	Captured on track or retracted
1 1	Not used

Bit 7 Interrupt

Diagnostic Sense Byte 2

Bit 0 - Odd track
1 - Access reset
2 - Depress profile
3 - Accelerate
4 - Not used
5 - Not used
6 - Not used
7 - Retract

Word 12 - Disk Unit Diagnostic Sense Byte 3

Diagnostic sense byte 3, bits 0, 1, and 2

Bits
0 1 2

0 0 0 Write and not ready
0 0 1 Write and servo not on track
0 1 0 Write and sector overrun
0 1 1 Write and read or write and head off servo
1 0 0 Access electronics (AE) unsafe w/o AE selected
1 0 1 Write and AE select error
1 1 0 Not write and AE unsafe w/AE selected
1 1 1 Write and AE unsafe

Bits 3-4 Used to identify data unsafe when bits 0, 1, and 2 are 0's

Bit 5 Not used

Bit 6 Sector counter error

Bit 7 Card/cable unseated

Bits 8-15 Diagnostic wrap byte

If cycle-steal status word 5, bit 7 is set to 1, bits 12–15 have the following meaning:

Bit 12: Disk unit interrupt not received
Bit 13: Read or write hardware time out
Bit 14: Hardware check
Bit 15: Buffer port address check

If cycle-steal status word 4, bit 15 is set to 1, bits 8–11 have the following meaning:

Bit 8: Disk unit cable continuity check
Bit 9: No control sample received from disk unit
Bit 10: Disk unit daisy bus parity error
Bit 11: Disk unit interrupt not reset after sense

Word 13- Attachment Diagnostic

Bits 0-2 Failure path

Bits 3-7 Number of disabled cache pages

Bits 8-15 Error modifier

Index

P

R

S

W

IBM Series/1 4967 High-Performance Disk Subsystem
and Attachment Feature
Order No. GA34-0227-1

READER'S COMMENT FORM

This manual is part of a library that serves as a reference source for systems analysts, programmers, and operators of IBM systems. You may use this form to communicate your comments about this publication, its organization, or subject matter, with the understanding that IBM may use or distribute whatever information you supply in any way it believes appropriate without incurring any obligation to you. Your comments will be sent to the author's department for whatever review and action, if any, are deemed appropriate.

Note: *Copies of IBM publications are not stocked at the location to which this form is addressed. Please direct any requests for copies of publications, or for assistance in using your IBM system, to your IBM representative or to the IBM branch office serving your locality.*

Note: Staples can cause problems with automated mail sorting equipment.
Please use pressure sensitive or other gummed tape to seal this form.

Thank you for your cooperation. No postage stamp necessary if mailed in the U.S.A. (Elsewhere, an IBM office or representative will be happy to forward your comments or you may mail directly to the address in the Edition Notice on the back of the title page.)

GA34-0227-1
Printed in U.S.A.

Reader's Comment Form

Cut or Fold Along Line

Fold and tape | Please Do Not Staple | Fold and tape

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 40 ARMONK, N.Y.

POSTAGE WILL BE PAID BY ADDRESSEE:

International Business Machines Corporation
Information Development, Department 28E
1803 (Internal Zip)
P.O. Box 1328
Boca Raton, Florida 33429-9960

Fold and tape | Please Do Not Staple | Fold and tape

IBM®

IBM

International Business Machines Corporation

GA34-0227-1

GA34-0227-1
Printed in U.S.A.