IBM

Series/1

GA34-0241-0

File No. S1-09

IBM Series/1
Synchronous Communication Single-Line Control Attachment Feature
Description

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First Edition (May 1983)

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Preface

This book describes the Series 1/Synchronous Communications Single-Line Control (SCSLC) attachment feature. The information in this publication is intended for assembler language programmers who need to create or modify programs written for the SCSLC. The reader should understand data processing terminology and stored-program concepts.

The subject matter is presented in eight chapters:

- Chapter 1, "Introduction," describes the SCSLC.
- Chapter 2, "Synchronous Communication Single Line Control," describes the attachment feature card data flow, device addressing, and jumper options.
- Chapter 3, "Device Commands," describes the set of attachment commands.
- Chapter 4, "Status," presents the status information available to the user.
- Chapter 5, "Synchronous Data Link Control (SDLC/HDLC)," presents the commands and formats used in SDLC/HDLC operation.
- Chapter 6, "Binary Synchronous Communication (BSC)," presents the commands, format, and modes used in BSC operation.
- Chapter 7, "Communications Indicator Panel," describes the communications indicator panel and associated lights and switches.
- Chapter 8, "Error Recovery," describes the error conditions and recommended recovery technique.

Prerequisite Publications

- *IBM Series/1 Principles of Operation*, GA34-0152
- For processor information, refer to the applicable processor and processor feature description manual.

Related Publications

- *IBM Series/1 Installation Manual—Physical Planning*, GA34-0029
- *IBM Series/1 Operator's Guide*, GA34-0039
- *IBM Series/1 Customer Site Preparation Manual*, GA34-0050
- *IBM Synchronous Data Link Control, General Information*, GA27-3093
- *General Information–Binary Synchronous Communications*, GA27-3004
- *IBM Implementation of X.21 Interface, General Information Manual*, GA27-3287

Contents

Chapter 1. Introduction

The synchronous communication single line control (SCSLC) feature provides bisynchronous communications (BSC) or synchronous data link control/high level data link control (SDLC/HDLC) protocols. It supports bit rates up to 56000 bits-per-second (V.35) and 48000 bits-per-second (X.21). Operation may be point-to-point or multipoint. IPL capability is supported for switched or leased lines.

The SCSLC communication feature provides several line speeds, line configurations, clocking sources, line protocols, and data transmission codes to choose from.

Interfaces

The SCSLC feature provides a CCITT[1] X.21 (switched and leased) or V.35 (leased) interface. It also has local attachment capabilities through an EIA[2] RS-422A interface using customer supplied cabling.

1 The International Telegraph and Telephone Consultative Committee
2 Electronic Industries Association

Data Links

The SCSLC attachment can operate with any one of the following types of data links:

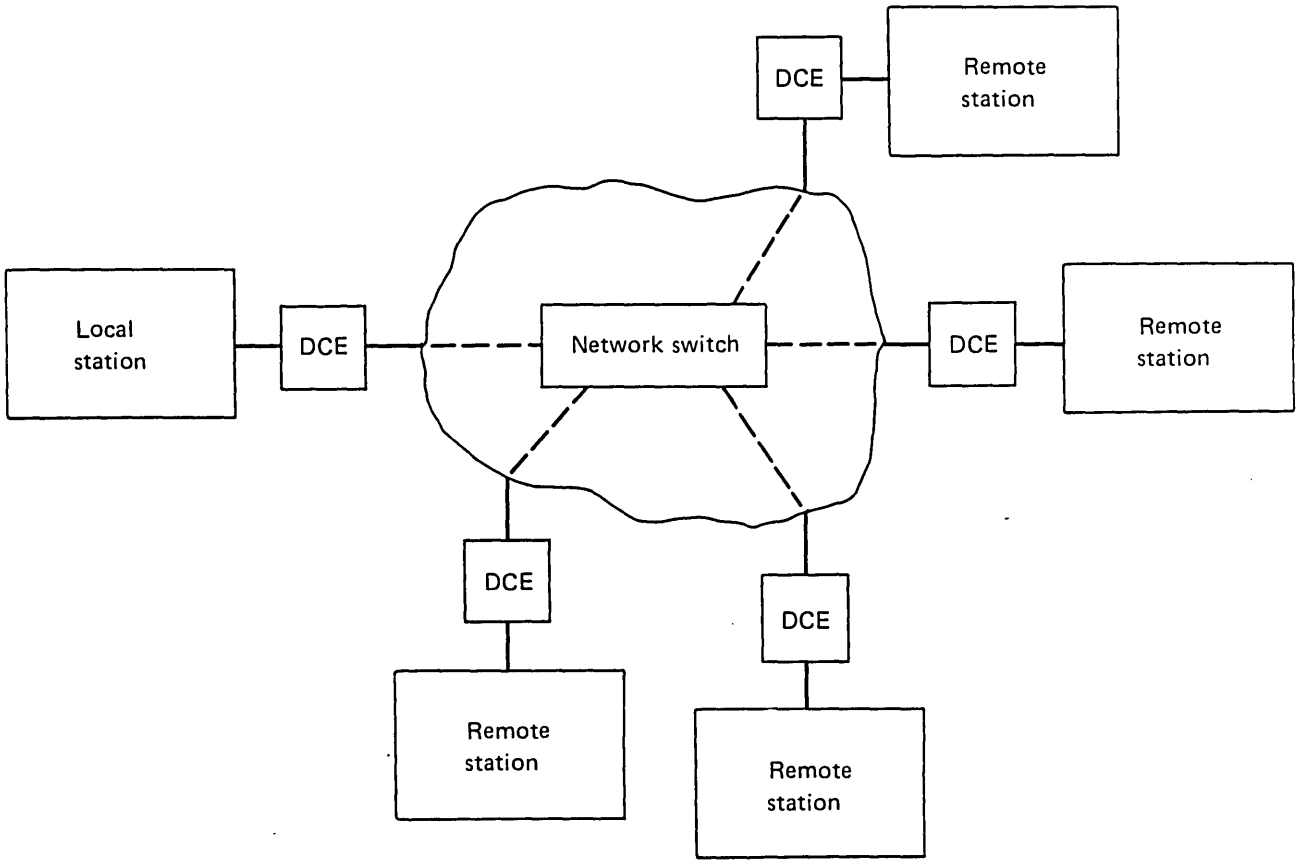
- Point-to-point nonswitched
- Point-to-point switched
- Multipoint nonswitched
- Local attach (direct connect)

Point–to–Point Nonswitched (Leased)

A *point–to–point nonswitched* data link consists of a local station connected to a single remote station using a CCITT V.35 or CCITT X.21 interface. The line is called *nonswitched* because of the permanent connection between the local station and the remote station through their data circuit-terminating equipment (DCEs).

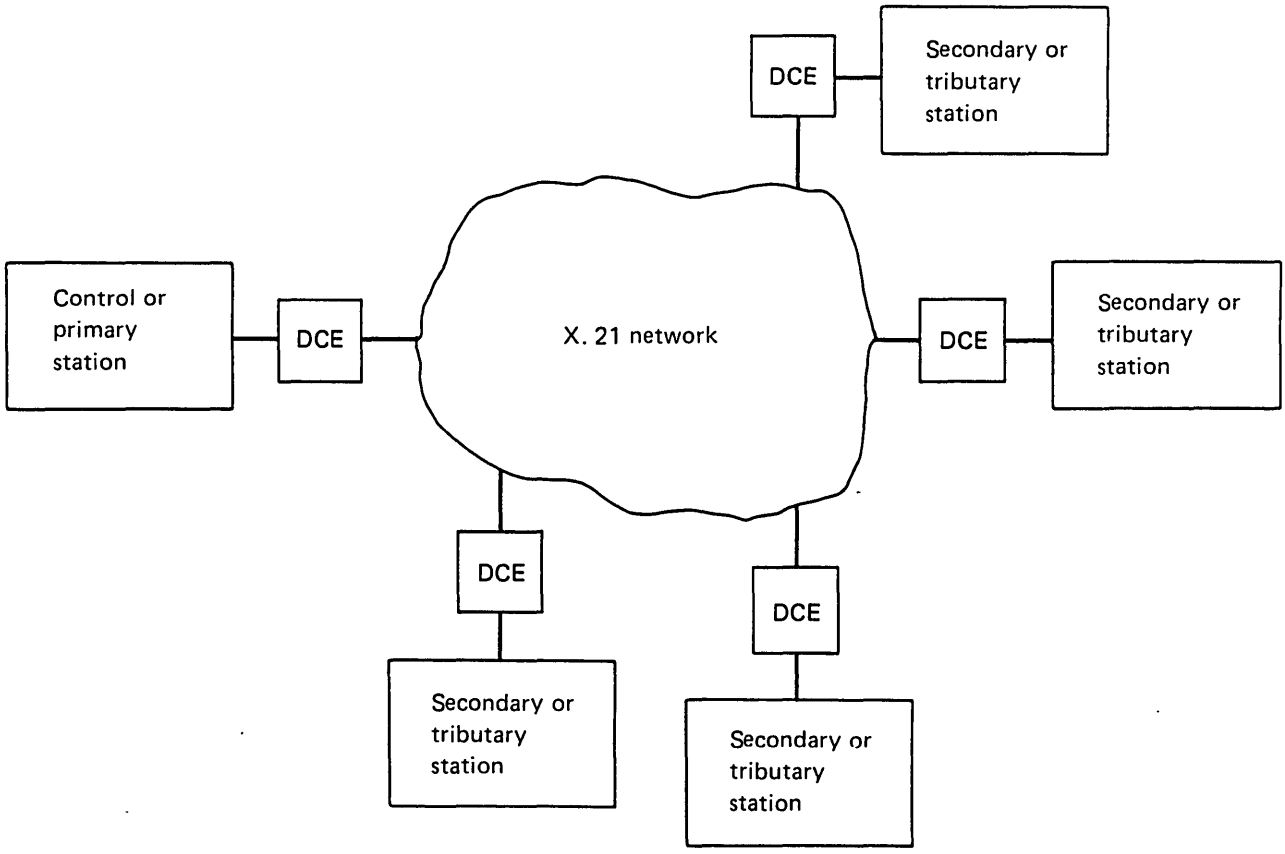
Point–to–Point Switched

A *point–to–point switched* data link consists of a local station connected to one of several remote stations (using CCITT X.21 interface) after establishing a link between the local station and the remote station. The connection remains only for the duration of the communication.



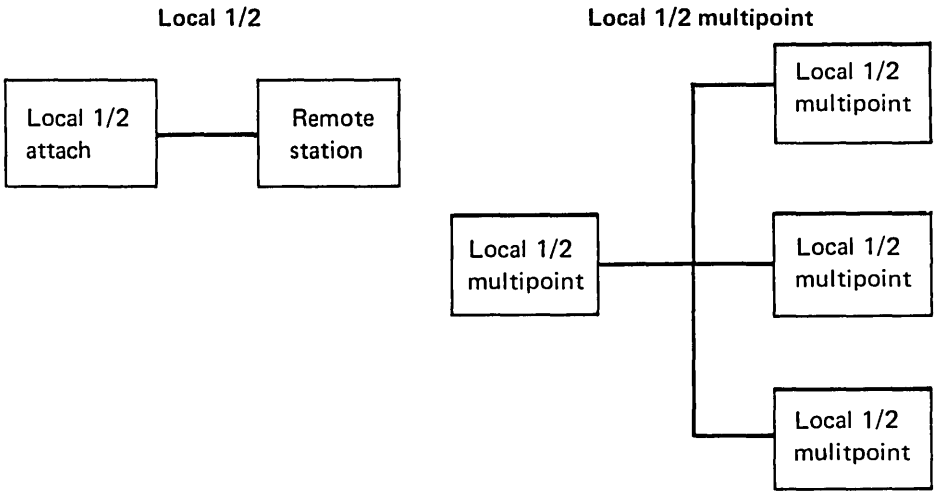
Multipoint Nonswitched

A *multipoint nonswitched data link* consists of a primary/control station connected to several secondary/tributary stations through their DCEs. The primary/control station polls the secondary or tributary stations using unique station addresses. Only the addressed station can respond to the poll.



Local Attach (SCSLC)

Local attach (direct connect) capabilities are available in several modes using the EIA RS-422A interface.



Data Link Controls (DLC)

The SCSLC communication feature provides the following data link controls:

- BSC
- SDLC/HDLC

Transmission Codes

BSC

The BSC feature uses:

- American Standard Code for Information Interchange (ASCII)—nontransparent only
- Extended binary-coded decimal interchange code (EBCDIC)—transparency is available

SDLC/HDLC

The SDLC/HDLC feature allows any 8-bit code, including:

- ASCII
- EBCDIC

Transparency is standard in all SDLC/HDLC procedures.

Chapter 2. Synchronous Communication Single-Line Control

Introduction

The synchronous communication single–line control (SCSLC) attachment provides one International Telegraph and Telephone Consultative Committee (CCITT) X.21 interface that allows the interchange of data between the Series/1 processor and a remote terminal that uses the synchronous mode of data transmission. The terminal must comply with the electrical and functional requirements of CCITT recommendation X.21. Interconnection between the Series/1 and the remote terminal may be made by using public or private leased data networks, as well as switched lines. In addition, terminals can be locally connected at distances up to 1220 meters (4000 feet).

The attachment supports synchronous data link control/high level data link control (SDLC/HDLC) or binary synchronous communication (BSC) protocol. When operating with SDLC/HDLC protocol, it can be operated in duplex mode. Duplex mode allows data to be concurrently transmitted and received between the Series/1 and the terminal. The communicating bit rate is normally controlled by clocking signals supplied by the data circuit-terminating equipment (DCE), except when using the local attach option, which provides clocking by the attachment. The attachment provides clocking for data rates of 9,600 or 48,000 bits per second (bps) when the local attach option is used.

For further information about the X.21 interface, refer to *IBM Implementation of X.21 Interface - General Information Manual*, GA27-3287. In case of a conflict with the CCITT X.21 recommendation, use the IBM documentation.

> **Note:** The local attach option allows the connection of remote terminals without DCEs by using the EIA RS-422A interface for distances up to 1220 meters (4000 feet).

The attachment also provides one CCITT V.35 interface and supports both the SDLC/HDLC and BSC protocols with a maximum rate of 56,000 bps.

> **Note:** Sustained throughput at 48,000 and 56,000 bps when using BSC protocol is considerably less than the clocking rate. Refer to the chapter on BSC protocol.

Two basic connection methods exist for the local attach options:

- **Local Attach 1:** Internal clocking occurs at a data rate of 9,600 bps with the remote device capable of deriving the clocking information from the data stream. This mode of operation allows connecting the remote terminal up to a distance of 1220 meters (4000 feet), using an EIA RS-422A interface. This clocking method supports only the SDLC/HDLC half-duplex operation. When operating in local 1 mode, the attachment transmits and receives in NRZI mode (bits 9 and 12 of the control word are ignored on transmit and bit 9 is ignored on receive). The attachment automatically transmits leading pads at the beginning of each frame sequence.
- **Local Attach 2:** The attachment provides a 48,000 bps clocking signal to an EIA RS-422A interface. This allows the remote device to use the clock as if a data circuit-terminating equipment (DCE) were present. If using this method of operation, the remote terminal must be connected at a distance up to 305 meters (1000 feet). Both the SDLC/HDLC (half-duplex and duplex) and bisynchronous (BSC) half-duplex protocols are supported in this mode.

  Note: Multidrop configuration is allowed when using local attach 1 or 2.

Control of up to 10 remote stations may be achieved by attaching them in a multi-drop configuration (stub length not exceeding 15 meters (45 feet)).

Note: For cable information, refer to the maintenance logic diagrams and the *Customer Site Preparation Manual,* GA34-0050.

Refer to the flowchart (Figure 2-1) for a graphic representation of installation considerations and available options.

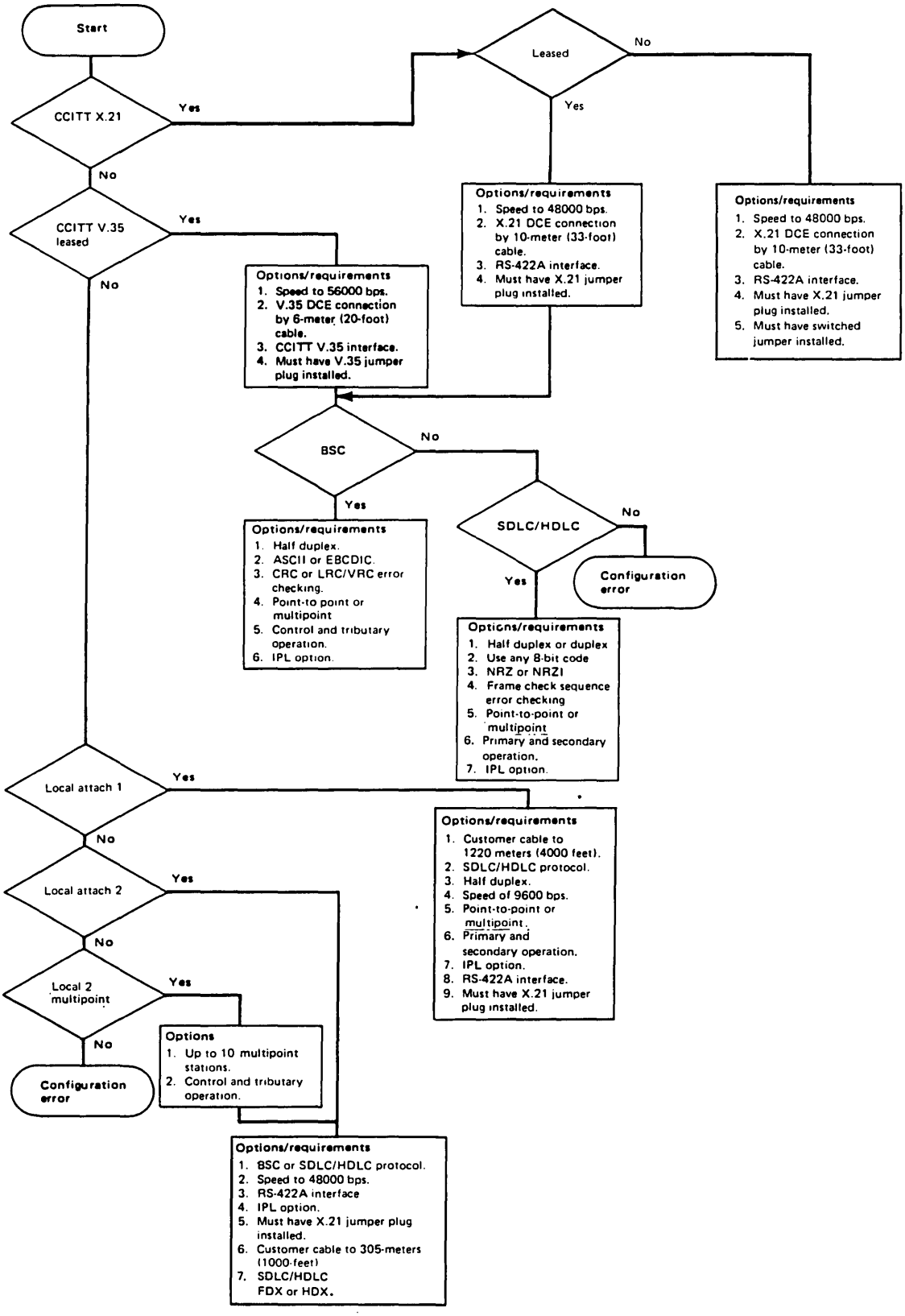


Figure 2-1. Installation considerations and options

Data Flow

Data transmission and reception protocol may be either SDLC/HDLC or BSC. Two characters at a time are fetched from processor storage during transmission. Bits 0–7 hold the first character transmitted and bits 8–15 hold the next. However, if the first character is located at an odd data address or the last character is located at an even data address, only one data character is fetched and transmitted.

On receive, the first bit received is placed in the least-significant bit, the second bit placed in the next higher bit position, and so on, until a character is assembled. The first character received is placed in bits 0–7 and the second character is placed into bits 8–15. Again, however, if the first character has an odd data address or the last character has an even data address, only one character is assembled and placed into processor storage.

See Figure 2-2 for an example of data flow for both transmit and receive operations.

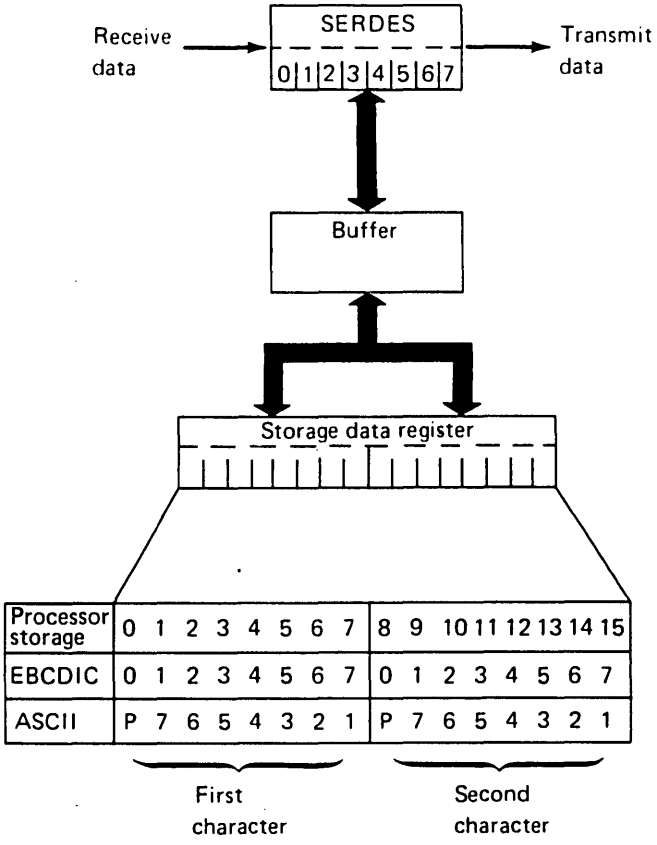


Figure 2-2. Data flow

Device Addressing

The attachment can respond to Operate I/O commands for two unique device addresses. The addresses are contiguous, beginning with an even address. The attachment card jumper positions are for the assignment of the base device address which is always even.

Note: This attachment always uses two device addresses.

When in half-duplex mode, device 0 is the even address. The following table shows the device commands, addresses, and mode of operation.

	Half Duplex		Duplex	
Command	**Dev 0**	**Dev 1**	**Dev 0**	**Dev 1**
Start	X		X	
Enable*	X		X	
Disable*	X		X	
Transmit*	X		X	
Receive*	X			X
Timer*	X		X	X
Start Control**	X		X	
Start Cycle Steal Status	X	X	X	X
Start Diag 1	X	X	X	X
Start Diag 2**	X		X	
Read ID	X	X	X	X
Halt I/O	X	X	X	X
Device Reset	X	X	X	X
Prepare	X	X	X	X
Start Modification**	X		X	

Note: Any command directed to device 0 or device 1, other than the ones indicated above, will cause an exception interrupt.

*DCB specification check reported
**Delayed command reject reported

Jumperable Options

The following attachment options can be enabled by installation of a card jumper:

Allow IPL: This jumper causes the attachment to monitor for a BSC or SDLC/HDLC IPL sequence.

Bi-Sync Mode: This jumper sets the attachment to BSC mode. Absence of this jumper indicates SDLC/HDLC mode to the attachment.

Local Attach 1: This jumper is installed in the local attach 1 cable. The attachment provides clocking in the SDLC/HDLC mode at a speed of 9,600 bps.

Note: The X.21 jumper plug must be installed.

Local Attach 2: This jumper is installed in the local attach 2 cable. The attachment provides clocking at a speed of 48,000 bps.

Note: The X.21 jumper plug must be installed.

Secondary Station Address/Multipoint Address: These jumpers are used to assign the secondary station address in SDLC/HDLC mode, or to assign the multipoint address in BSC mode.

Note: In BSC mode the attachment is a multipoint tributary if the multipoint address is not 0. Therefore, 0 is not a valid multipoint address.

Signal to Protective Ground: If this jumper is installed, signal ground is connected to protective ground. Installation of this jumper is to meet local code requirements when attaching to X.21 data circuit terminating equipment (DCE).

X.21 Jumper: If this jumper plug is installed, the attachment operates with the X.21 interface.

V.35 Jumper: If this jumper plug is installed, the attachment operates with the V.35 interface.

Note: Refer to the maintenance logic diagrams for jumper locations and cable information.

Chapter 3. Device Commands

The attachment has several device commands:

- Prepare
- Start Diagnostic 1
- Start Diagnostic 2
- Read ID
- Halt I/O
- Device Reset
- Start Control
- Start Modification
- Start
- Start Cycle-Steal Status

Prepare

The Prepare command controls the interrupt parameters of the addressed device. The immediate data field (bits 16–31) contains the level and I-bit. The attachment accepts and executes a Prepare command, even if it is busy or has an interrupt request pending from a previous command. The IDCB for the Prepare command has the following format:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 0 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
60	00–FF •

Immediate data field		
0's	Level	I
16 ... *26*	*27* ... *30*	*31*

Level - bits 27–30: This 4-bit field specifies the priority interrupt level assigned to the device. The binary value of bits 27–30 indicates priority levels of 0-3.

Bits 27-30	Level
0000	0
0001	1
0010	2
0011	3

I-Bit - bit 31: This bit determines if the device can present interrupt requests. An I-bit set to 1 means that the device can request an interrupt; a 0 means that the device cannot interrupt.

Each time the attachment presents an interrupt request, it stores the level data and presents it to the processor. Either a system reset or a power-on reset resets the prepare information (level and I-bit).

The Prepare command causes an interrupt request only when the attachment is not prepared (I-bit set to 0) and has an interrupt pending upon receipt of a Prepare command with the I-bit set to 1.

A successful Prepare command always causes the attachment to respond with a condition code 7 (satisfactory).

Start Diagnostic 1

The IDCB for the Start Diagnostic 1 command is:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 1 1 0 1	X X X X X X X X
0 ... *7*	*8* ... *15*
7D	00–FF

Immediate data field
DCB address
16 ... *31*

This command causes two types of tests to occur in the attachment. The results of the tests are placed in processor storage, beginning at the address specified in word 7 (data address) of the DCB. The byte count for this operation must be equal to 11, and the data address must be even. Otherwise, an exception interrupt occurs with bit 3 (DCB specification check) set in the interrupt status byte.

A DCB specification check occurs if the DCB control word has any bit set to 1 other than bit 2, 5, 6, or 7.

The DCB format is as follows:

Word	*0 1 2 3 4 5 6 7 8* ... *15*
0	0 0 1 0 0 | K E Y | 0's
1	Not used (0's)
2	Not used (0's)
3	Not used (0's)
4	Not used (0's)
5	Not used (0's)
6	Byte count (must be hex B)
7	Data address (even)

The first diagnostic test is an attachment storage test that consists of writing/reading 1's and 0's through all the attachment storage locations. If the test is successful, a hex FF is written into data word 5, high-order byte. If the test fails, a hex 00 is written into data word 5, bits 0–7.

Note: During initial power-on sequencing, the attachment storage patch (PATCH) area is tested. The diagnostic command does not test the PATCH area.

The next test computes a checksum for the two read only storage (ROS) modules used by the attachment. The result, along with a checksum that was written into the ROS modules at the time the modules were fabricated, are placed in data words 1, 2, 3, and 4 in the following manner:

Data word 1	Stored checksum ROS 1
Data word 2	Computed checksum ROS 1 (complemented)
Data word 3	Stored checksum ROS 2
Data word 4	Computed checksum ROS 2 (complemented)
Data word 5	Bits 0-7 (FF good storage test)
	Bits 0-7 (00 storage test failure)
	Bits 8-15 (Secondary station or MP tributary address)
Data word 6	Bits 0-7 Bit 0 Not used Bit 1 BSC jumper Bit 2 X.21 switched jumper Bit 3 Local attach 2 jumper Bit 4 Local attach 1 jumper Bit 5 Allow IPL jumper Bit 6 V.35 jumper Bit 7 Not used
	Bits 8-15 refer to text

The attachment reports the secondary station/multipoint tributary address jumpers in data word 5, bits 8–15. The attachment also reports the configuration jumpers in data word 6, bits 0–7. Bits 8–15 of the data storage register are set to a hex AA to test the byte mode of data transfer to storage. If byte mode fails, a hex AA appears in data word 6, bits 8–15, otherwise, the value stored in data word 6, bits 8–15, is dependent upon the processor storage initialization.

Start Diagnostic 2

Following is the IDCB for the Start Diagnostic 2 command:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 1 1 1 0	X X X X X X X X
0 — *7*	*8* — *15*
7E	00–FF

Immediate data field
DCB address
16 — *31*

This command causes a wrap test to occur in the attachment. The results are placed in processor storage, beginning at the address specified in word 7 (data address) of the DCB. The byte count for this operation must be equal to 2 and the data address must be even. Otherwise, an exception interrupt occurs with bit 3 (DCB specification check) set in the interrupt status byte (ISB).

A DCB specification check occurs if the DCB control word has any bit set to one other than bit 2, 5, 6, 7, or 15. The DCB for the Start Diagnostic 2 command is:

Word	*0 1 2 3 4 5 6 7 8*		*15*
0	0 0 0 0 0	K E Y 0's	X
1	Not used (0's)		
2	Not used (0's)		
3	Not used (0's)		
4	Not used (0's)		
5	Not used (0's)		
6	Byte count (must be 2)		
7	Data address (must be even)		

DCB word 0, bit 15, indicates the following:

- Bit 15 = 1, signal timing provided
- Bit 15 = 0, signal timing not provided

Note: Signal timing provided indicates that data circuit terminating equipment (X.21 or V.35) is attached and is supplying the signal timing during the wrap test.

With the X.21 jumper plug installed, the attachment is tested in the X.21 mode in the following sequence:

1. Test 1 checks the control, indicate, receive, and transmit lines. If the test is successful, the attachment sets bits 0–3 in data word 1 to 1's.
2. Test 2 causes the attachment to monitor the signal timing lines for transitions if bit 15 of DCB word 0 is set to a one. If transitions are detected, the associated bit in data word 1 is set to 1. The byte timing indicator is set to a zero when bit 15 of DCB word 0 is set to 1. If bit 15 of DCB word 0 is set to zero, the attachment drives the signal timing line with a 48,000 bps clocking signal. When the card wrap connector is installed, these transitions are monitored on the byte timing line and if detected, the associated bits for signal timing and byte timing in data word 1 are set to 1.
3. Test 3 causes the attachment to perform a BSC wrap test. If the test is successful, the attachment sets bit 6 in data word 1 to a 1.

   Note: This test is not performed in local attach 1 mode.
4. Test 4 causes the attachment to perform an SDLC wrap test. If the test is successful, the attachment sets bit 7 in data word 1 to a 1.
5. Test 5 causes the attachment to read the switches on the indicator panel and report the hexadecimal value in bits 8–15 of data word 1. If the indicator panel is not attached, the attachment reports a hex 00 in bits 8–15 of data word 1.

Bit 15 of the DCB control word must be set to 0. There are no changes to tests one through five.

Note: Data word 1 has the following bit definitions for X.21:

Bit	Definition
0	Transmit
1	Receive
2	Indicate
3	Control
4	Signal timing
5	Byte timing
6	BSC wrap
7	SDLC wrap
8-15	Indicator panel switch setting

Local Attach 1

The attachment card must have the following jumpers installed:

J1-A16 to J1-B16
J1-A17 to J1-B17
J1-A18 to J1-B18
J1-A19 to J1-B19

Bit 15 of the DCB control word must be set to 0. In test 2, the 'byte timing' line is not examined (Bit 5 of data word 1 is 0). Test 3 is not performed. Bit 6 of data word one is set to 0.

Local Attach 2

The attachment card must have a jumper from J1-A20 to J1-B20 installed. Bit 15 of the DCB control word must be set to a 0. There are no changes to tests one through five.

Local Attach 2 Multipoint

The attachment card must have the following jumpers installed:

J1-A19 to J1-B19
J1-A20 to J1-B20

With the V.35 jumper plug installed, the attachment is tested in the V.35 mode.

Note: All tests, with the exception of Tests 1 and 2, function in the same manner as the preceding X.21 tests. Test 2 is not performed in V.35 mode.

Test 1 causes transitions on the 'request-to-send' (RTS) line while monitoring the 'clear-to-send' (CTS) line. If the test is successful, the attachment sets the associated bit in data word 1 to a 1. The attachment also checks for an active level on the 'data-set-ready' line.

Data word 1 has the following bit definitions for V.35:

Bit	Definition
0	Data-set-ready (DSR)
1	Clear-to-send (CTS)
2	Request-to-send (RTS)
3	Not used (0's)
4	Not used (0's)
5	Not used (0's)
6	BSC wrap
7	SDLC wrap
8-15	Indicator panel switch setting

Note: The diagnostic 2 results for word 1, bits 0–7 are:

Configuration	*Result*
X.21 DCE wrap	FB
X.21 cable wrap	FB
X.21 card wrap	FF
Local 1	F9
Local 2	FF
V.35	E3

Read ID

The Read ID command transfers the attachment's identification word from the device to the data word position of the IDCB.

The attachment's ID is 5042. The IDCB for the Read ID command is:

IDCB (immediate device control block)

Command field	*Device address*
0 0 1 0 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
20	00–FF

Immediate data field	
0 1 0 1 0 0 0 0	0 1 0 0 0 0 1 0
16	*31*

Halt I/O

This command halts all I/O activity on the I/O interface and sets 'DTE ready'. It resets the residual byte count to 0 and clears pending interrupts. It does not reset the I-bit, prepared level or residual address.

IDCB (immediate device control block)

Command field	*Device address*
1 1 1 1 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
F0	00–FF

Immediate data field
0's
16 ... *31*

Device Reset

The Device Reset command resets the addressed device. Pending interrupt requests (except controller end) are cleared. This command does not reset the prepare level, I-bit, residual address, and interface state. The Device Reset command has the following format:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 0 1 1 1 1	X X X X X X X X
0 *7*	*8* *15*
6F	00–FF

Immediate data field
0's
16 *31*

A Device Reset command issued to the attachment causes the attachment to become busy after reset while carrying out the reset functions. The length of time that the attachment remains in busy after reset is a function of the microcode program in the attachment. The attachment may present a busy after reset (CC2) to an Operate I/O immediately following a Device Reset.

Start Control (Leased Lines)

To setup operating conditions, use the Start Control command. The IDCB for the Start Control command is:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 0 0 0 1	X X X X X X X X
0 ... *7*	*8* ... *15*
71	00–FF

Immediate data field
DCB address
16 ... *31*

Following is the format for the Start Control (set mode) DCB:

DCB (device control block)

Word	*0 1 2 3 4 5 6 7 8* ... *15*
0	X 0 0 0 0 K E Y 0 0 0 0 0 0 0 0
1	0 0 0 0 0 0 0 0 0 0 0 X X X 0 0
2	Not used (0's)
3	Not used (0's)
4	Not used (0's)
5	Chaining address
6	Not used (0's)
7	Not used (0's)

Word 0: Word 0 has the following format:

Bit 0 - Chaining: This bit, when set to 1, indicates chaining is in effect.

Bits 1–4: These bits are not used and must be set to 0.

Bits 5–7 - Key: These bits represent a 3-bit key. The attachment presents this key to the processor during data transfers to verify that the program has authorization to access processor storage. An invalid address key causes an exception-interrupt request (condition code 2), with bit 6 set to 1 (protect check) in the ISB.

Bits 8–15: These bits are not used and must be set to 0.

Word 1: Word 1 has the following format:

Bits 0–10: These bits are not used and must be 0's.

Bit 11 - Enable PCI: If this bit is a 1, the attachment supports a program controlled interrupt (PCI).

Bit 12 - Mode: If this bit is a 1, the attachment is in duplex mode of operation. If this bit is a 0, the attachment is in half-duplex mode of operation.

Note: When this bit is a 1, the attachment supports only SDLC/HDLC mode.

Bit 13 - Installation Test: If this bit is a 1, the attachment performs internal tests (used for installation measurements).

Bit 14: This bit is not used and must be 0.

Bit 15: This bit is not used and must be 0.

Words 2–4: These words are not used and must be set to 0.

Word 5 - Chaining Address: This word contains the address of the next DCB in a chaining operation.

Note: Chaining should not be used on the Start Control (leased) command because the only function that can be performed is set mode.

Words 6–7: These words are not used and must be set to 0.

Start Control (X.21 Switched)

To operate in the X.21 switched environment, software must use the Start Control command. This command along with associated DCBs allows the attachment to make a transition through defined X.21 CCITT states that are necessary to establish a switched connection on an X.21 network. This command may also be issued during leased operation (X.21 or V.35) local connect mode, or after the connection is established on a switched network to set the operational mode (Set Mode operation). For example; to setup PCI or duplex modes.

Use this command to perform the following Start Control operations:

1. Set mode
2. Network provided information
3. Auto-answer
4. Clear

The IDCB for the X.21 switched mode of operation is the same as for the Start Control command for leased lines and is as follows:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 0 0 0 1	X X X X X X X X
0 *7*	*8* *15*
71	00–FF

Immediate data field
DCB address
16 *31*

Set Mode

The set mode DCB format is as follows:

DCB (device control block)

Word	0	5	7	8	15
0	X 0 0 0 0	K E Y		0 0 0 0 0 0 0 0	
1	0 0 0 0 0 0 0 0 0 0 X X X X X X				
2	Not used (0's)				
3	Not used (0's)				
4	Not used (0's)				
5	Chaining address				
6	Byte count				
7	Data address				

Word 0

Bit 0 - Chaining: Set this bit to 1 when specifying a chaining operation.

Bits 1–4: These bits are not used and must be 0's.

Bits 5–7 - Key: These bits represent a 3-bit key. The attachment presents this key to the processor during data transfers to verify that the program has authorization to access processor storage. An invalid address key causes an exception-interrupt request (condition code 2), with bit 6 set to 1 (protect check) in the interrupt status byte (ISB).

Bits 8–15: These bits are not used and must be set to 0's.

Word 1

Bits 0–9: These bits are not used and must be set to 0's.

Bit 10 - Auto Answer: Set this bit to 1 when the remote station is configured for auto-answer. When this bit is a 1, the attachment uses 2 seconds as a time-out (T3). When this bit is a 0, the attachment uses 60 seconds as a time-out.

Bit 11 - Enable Program Controlled Interrupt (PCI): If this bit is a 1, the attachment supports PCI.

Bit 12 - Mode: If this bit is a 1, the attachment is in duplex mode. If this bit is a 0, the attachment is in half duplex mode.

Note: Duplex mode is only used in SDLC/HDLC mode of operation.

Bit 13 - Test: This bit is used for installation tests.

Bit 14 - Direct Call: If this bit is a 1, a direct call is in effect, and no selection or facility registration/cancellation parameters will be transmitted.

Bit 15 - Registration/Cancellation Selection: If this bit is a 1, software provides a selection or facility registration/cancellation code for transmission.

Words 2–4: These words are not used and must be set to 0's.

Word 5 - Chaining Address: This word contains the address of the next DCB in a chaining operation.

Word 6 - Byte Count: This 16-bit byte count word contains the number of bytes included in the selection sequence or facility registration/cancellation code.

Note: The attachment supports a maximum byte count of 255 bytes. If the byte count specified is greater than 255, an exception interrupt (CC2) is reported with bit 3 (DCB specification check) set in the ISB.

Word 7 - Data Address: This word contains the address, in processor storage, of the selection sequence required to establish a connection on the switched X.21 network or facility registration/Cancellation code.

Notes:

1. The Data Address and Byte Count of data word 1 are meaningful only when bit 15 is a 1.
2. The selection sequence and facility registration/cancellation codes must be coded exactly as required by the network. These are not checked by the attachment prior to transmission to the network DCE.
3. If either of the following conditions exist, the attachment reports an exception interrupt with bit 3 (DCB specification check) set to 1 in the ISB.
   - The BSC jumper is installed and the Set Mode DCB specifies duplex mode.
   - Both bits 14 and 15 are set to 1 in word 1 of the Set Mode DCB.
4. The format of the Start Cycle-Steal Status words (CCSW) reported after an interrupt to a Start Control command depends on the BSC jumper. If the jumper is installed, BSC status is reported. If it is not installed, SDLC status is reported.
5. The Set Mode DCB specifying either direct call or selection causes the attachment to take the following actions:
   a. The attachment checks for CCITT state 1 and, if not active, presents an exception interrupt (CC2) with bit 0 (device dependent status available) set in the ISB, and BSC bit 2 (DCE interface error) set in cycle-steal status word 1, or SDLC bit 7 (DCE interface error) set in cycle-steal status word 2. If CCITT state 1 is active, the attachment enters CCITT state 2.
   b. If the data circuit terminating equipment (DCE) does not provide CCITT state 3 within 3 seconds (T1), the attachment reports an exception interrupt (CC2) with bit 0 (device dependent status available) set in the interrupt status byte (ISB), BSC bit 15 (T1 time-out) set in cycle-steal status word 4 or in the case of SDLC mode, bit 15 (T1 time-out) is set in cycle-steal status word 5.
   c. After detecting CCITT state 3, the attachment enters CCITT state 4 and transmits the selection or facility registration/cancellation (SFRC) parameters pointed to by the Set Mode DCB. The attachment transmits 2 synchronization (SYN) characters preceding the SFRC parameters.

d. After transmitting the SFRC parameters, the attachment enters CCITT state 5 and reports a device end interrupt (CC3) or initiates a chaining operation if so specified in the control word. If Direct Call is specified, no SFRC is transmitted and the attachment interrupts or initiates a chaining operation after making the transition from CCITT state 3 to CCITT state 5. If a DCE clear occurs during selection, an attention interrupt (CC4) is presented and no NPI DCB is fetched.

Network Provided Information (NPI)

The NPI DCB is an integral part of the connection process and must be issued when an outgoing call is attempted. The format of the NPI DCB is as follows:

DCB (device control block)

Word	0 1 2 3 4 5 7 8 15
0	0 0 1 0 1 | K E Y | 0 0 0 0 0 0 0 1
1	Not used (0's)
2	Not used (0's)
3	Not used (0's)
4	Status address
5	Not used (0's)
6	Byte count
7	Data address

Word 0 - Control Word:

Bits 0–1: These bits are not used and must be set to 0's.

Bit 2 - Input Flag: When this bit is set to a 1 it allows cycle-steal of data into main storage. This bit is set to 1 along with bit 4 to prevent an exception interrupt (CC2) being reported.

Bit 3: This bit is not used and must be set to 0.

Bit 4 - Suppress Exception: When this bit is set to a 1 it allows residual status reporting. This bit along with bit 2 is set to 1 or an exception interrupt (CC2) is reported, with bit 3 (DCB specification check) set in the ISB.

Bits 5–7 - Key: These bits represent a 3-bit key. The attachment presents this key to the processor during data transfers to verify that the program has authorization to access processor storage. An invalid address key causes an exception-interrupt request (CC2), with bit 6 set to 1 (protect check) in the interrupt status byte (ISB).

Bits 8–14: These bits are not used and must be set to 0's.

Bit 15 - Network Provided Information (NPI): This bit is set to 1 to establish that this is an NPI DCB when issued under a Start Control command.

Words 1–3: These words are not used and all bits must be set to 0's.

Word 4 - Status Address: This 16-bit word contains the processor storage address of the residual status block (RSB). The RSB contains two words, the first of which is the residual byte count. The second (word 1) contains the system architecture bits as follows:

Bit 0 - End Of Chain (EOC): This bit is set to 1 to indicate no chaining since chaining from the NPI DCB is not permitted.

Bits 1–14: These bits are not used and must be set to 0's.

Bit 15 - No Exception (NE): This bit is set to 1 to indicate the NPI was received without error. A T2 or T3 timeout or an ILR to an NPI causes the NE bit to be set to 0 because these conditions are reported by an exception interrupt.

> **Note:** Use of the set suppress exception (SE) bit and the residual status block (RSB) allows software to determine the number of bytes received in the NPI without issuing a Start Cycle-Steal Status command.

Word 5: This word is not used and all bits must be set to 0's.

Word 6 - Byte Count: This word contains the total byte count allocated for the NPI.

The attachment supports a maximum byte count of 255 bytes. If the byte count specified is greater than 255, an exception interrupt (CC2) is reported, with bit 3 (DCB specification check) set in the ISB.

All network provided information (call progress signals (CPS) and DCE provided information (DPI) are passed into processor storage beginning with CPS (when present). This information is passed to processor storage as coded by the network. The attachment deletes any inserted synchronization (SYN) characters. The input flag (I/F) and suppress exception (SE) bits of the DCB control word must be set to 1; if not, the attachment presents an exception interrupt (CC2) with bit 3 (DCB specification check) set to 1 in the ISB. The selection or facility registration/cancellation sequence or a direct call must have been previously specified by a Set Mode DCB. If the NPI DCB is issued before the Set Mode DCB or on a leased network, the attachment presents an exception interrupt (CC2) with bit 3 (DCB specification check) set in the ISB.

The attachment may be in one of several states when the NPI DCB is fetched. The execution of the Set Mode DCB specifying selection, facility registration/cancellation; or direct call allows the attachment to move to CCITT state 5. The attachment may cause a transition to CCITT state 6, 7, 10, 11, 12, or 19 before fetching the NPI DCB. The CPS and DPI information (up to 255 bytes maximum) are stored on the attachment when not directed by the NPI DCB. The NPI DCB must be issued after an outgoing call by the Set Mode DCB. Chaining from the Set Mode DCB is recommended.

The NPI DCB causes the attachment to take the following actions:

1. CCITT state 7, 12, or 19 must be detected within 20 seconds (T2) after entering CCITT state 5. If it is not, the attachment reports an exception interrupt (CC2) with bit 0 (device dependent status available) set in the ISB, BSC bit 14 (T2 time-out) set in cycle-steal status word 4, or SDLC bit 14 (T2 time-out) set in cycle-steal status word 5.
2. If the attachment detects CCITT state 12, or 19, it stores the CPS and DPI information into processor storage as directed by the NPI DCB. Once the attachment receives the CPS and DPI signals, it waits (T3) for 2 or 60 seconds for CCITT state 12 or 19 to come active.
3. If CCITT state 12 or 19 is not reached, the attachment reports an exception interrupt (CC2) with bit 0 (device dependent status available) set in the interrupt status byte (ISB), BSC bits 14, 15 (T3 time-out) set in cycle-steal status word 4, or SDLC bits 14, 15 (T3 time-out) set in cycle-steal status word 5.
4. Once CCITT state 12 or 19 is presented by the DCE, the attachment presents an interrupt (see following note). CCITT State 12 is a transition made by the DCE and therefore receive data may appear at the interface as soon as

CCITT state 12 is established. CCITT State 13 may be entered if the DCE provides receive data to the attachment. The attachment must be directed by a receive DCB conforming to either SDLC/HDLC or BSC format in order to accept the data. If the DCE presents CCITT state 19, the attachment starts a 2-second timer (T6) and then goes through a clearing sequence (CCITT states 19, 20, 21, and 1). If CCITT state 1 is reached, the attachment presents an attention interrupt (CC4) with bit 0 (clear successful) set in the IIB. If CCITT state 1 is not reached, the attachment reports an attention interrupt with bit 7 (clear failure - T6 time-out) set in the IIB.

Note: If the byte count specified in the DCB is equal to or greater than the number of bytes received in the NPI, the attachment presents a device end interrupt (CC3) when state 12 (ready for data) is reached. If the byte count is insufficient to allow for cycle-stealing all of the NPI information into processor storage, the attachment reports an exception interrupt (CC2) with bit 2 (incorrect length record - long record) set in the ISB. If state 19 (DCE clear) is reached, the attachment presents an attention interrupt (CC4) with IIB bit 0 (clear successful) set or with bit 7 (clear failure) set. The attachment remains busy to the NPI or Auto-Answer DCB when terminated with an attention interrupt. Therefore, the software must issue a Device Reset command.

The format for the Auto-Answer DCB is as follows:

DCB (device control block)

Word	0 1 2 3 4 5 7	8 15
0	0 0 1 0 1 K E Y	0 0 0 0 0 0 1 0
1	Timer 1	Not used (0's)
2	Not used (0's)	
3	Not used (0's)	
4	Status address	
5	Not used (0's)	
6	Byte count	
7	Data address	

Word 0 - Control

Bits 0–1: These bits are not used and must be set to 0's.

Bit 2 - Input Flag: This bit and bit 4 must be set to 1 or an exception interrupt (CC2) is reported, with bit 3 (DCB specification check) set in the ISB.

Bit 3: This bit is not used and must be set to 0.

Bit 4 - Suppress Exception: This bit when set to 1 allows residual status reporting. This bit along with bit 2 must be set to 1 or an exception interrupt (CC2) is reported, with bit 3 (DCB specification check) set in the ISB.

Bits 5–7 - Key: These bits represent a 3-bit key. The attachment presents this key to the processor during data transfers to verify that the program can access processor storage. An invalid address key causes an exception-interrupt request (CC2), with bit 6 set to 1 (protect check) in the ISB.

Bits 8–13: These bits are not used and must be set to 0's.

Bit 14 - Auto-Answer: This bit is set to 1 to identify the DCB as an Auto-Answer DCB.

Bit 15: This bit is not used and must be set to 0.

Word 1

Bits 0–7 - Timer 1: Use these bits to limit the time the attachment waits for an incoming call. The time is specified in increments of 106 milliseconds. If a value of 0 is coded, the attachment waits indefinitely.

Bits 8–15: These bits are not used and must be set to 0's.

Words 2–3: These words are not used and all bits must be set to 0's.

Word 4 - Status Address

Bit 0 - End Of Chain (EOC): Set this bit to 1 to indicate no chaining; the attachment does not permit chaining from the Auto-Answer DCB.

Bits 1–14: These bits are not used and must be set to 0's.

Bit 15 - No Exception (NE): This bit is set to a 1 to indicate the DPI was received without error. A T4 time-out or an ILR to an Auto-Answer causes the NE bit to be set to 0 since these conditions are reported in an exception interrupt.

Word 5: This word is not used and all bits must be set to 0's.

Word 6 - Byte Count: This word indicates the total number of bytes allocated for the DCE provided information (DPI). The attachment supports a maximum byte count of 255 bytes. If the byte count specified is greater than 255, an exception interrupt (CC2) is reported, with bit 3 (DCB specification check) set in the ISB.

Word 7 - Data Address: This word contains the address in processor storage of the starting location for the DPI.

Notes:

1. Use of the SE bit and the RSB allows software to determine the number of bytes received in the DPI without issuing a Start Cycle-Steal Status command.
2. The Auto-Answer DCB can be issued before an incoming call is detected or in response to an attention interrupt. If issued before an incoming call, the attachment, on detection of an incoming call:
   - Establishes the connection
   - Cycle-steals the DPI into processor storage
   - Deletes any SYN characters in the DPI
   - Presents an interrupt (see the note following this list)

   The time that the attachment waits for an incoming call can be limited by specifying a time-out period in word 1 of this DCB. If the timer expires before an incoming call, the attachment presents an exception interrupt (CC2), with bit 0 (device dependent status available) set in the ISB, and BSC bit 1 (time-out) set in cycle-steal status word 1 or SDLC bit 4 (time-out) set in cycle-steal status word 2. A timer value (DCB word 1) of 0 results on no time-out.
3. The Auto-Answer command is valid for switched line opertion only. If issued while in leased line mode, the attachment presents an exception interrupt (CC2) with bit 3 (DCB specification check) set in the ISB.

Handling An Incoming Call

The attachment takes the following actions to handle an incoming call:

1. If not in Auto-Answer mode, the attachment recognizes CCITT state 8 and presents an attention interrupt (CC4) with the interrupt information byte equal to 0.
2. The attachment must next be directed by the Auto-Answer DCB.
3. The attachment must enter CCITT state 9 within 500 milliseconds or the DCE may cancel the call and proceed to the DCE ready state.
4. The attachment, once directed by the Auto-Answer DCB, enters CCITT state 9 and starts a 2-second timer (T4).

5. When in CCITT state 10, the DCE provides the DPI (if present) to the attachment.
6. After recognizing CCITT state 12 or 19, the attachment cycle-steals the DPI into processor storage.
7. When CCITT state 12 or 19 is active, the attachment presents an interrupt (see the note following this list)
8. CCITT state 13 can be entered if the DCE provides receive data to the attachment. The attachment must be directed by a receive DCB in order to accept the data.
9. If the attachment does not reach CCITT state 12 or 19, a 2-second time-out (T4) occurs. The attachment then presents an exception interrupt (CC2) with bit 0 (device dependent status available) set in the ISB, BSC bit 13 (T4 time-out) set in cycle-steal status word 4 or SDLC bit 13 (T4 time-out) set in cycle-steal status word 5.
10. CCITT state 8 may be an incoming call from the network indicating information is available (charge information previously requested through selection). In this situation, the DCE ends the call (after the DPI is provided) by entering CCITT state 19.
11. The attachment then starts a 2-second timer (T6) and procedes to clear the line.
12. An attention interrupt (CC4) is then presented (see the note following this list) for the Auto-Answer DCB with bit 0 (clear successful) set in the IIB.
13. If the clearing operation is not successful (CCITT state 1 is not reached), the attachment reports an attention interrupt (CC4) with bit 7 (clear failure T6 time-out) set in the IIB.
14. If CCITT state 19 is not entered within 2-seconds, the same condition exists that is present for a normal call when CCITT state 12 is not reached; a T4 time-out occurs.

Note: If the byte count specified in the DCB is equal to or greater than the number of bytes received in the NPI, the attachment presents a device end interrupt (CC3) when state 12 (ready for data) is reached. If the byte count is insufficient to allow for cycle-stealing all of the NPI information into processor storage, the attachment reports an exception interrupt (CC2) with bit 2 (incorrect length record - long record) set in the ISB. If state 19 (DCE clear) is reached, the attachment presents an attention interrupt (CC4) with IIB bit 0 (clear successful) set or with bit 7 (clear failure) set. The attachment remains busy to the NPI or Auto-Answer DCB when ended with an attention interrupt, therefore the software must issue a Device Reset command.

Clear

The Clear operation is valid for switched line operation only. If this operation is issued while in leased line mode, the attachment presents an exception interrupt (CC2) with bit 3 (DCB specification check) set in the ISB.

The format of the Clear DCB is as follows:

DCB (device control block)

Word	0 4	5 7	8 15
0	0 0 0 0 0	K E Y	0 0 0 0 0 1 0 0
1	Not used (0's)		
2	Not used (0's)		
3	Not used (0's)		
4	Not used (0's)		
5	Not used (0's)		
6	Not used (0's)		
7	Not used (0's)		

The attachment executes the line clearing procedure on an X.21 switched network and returns to ready (CCITT state 1). A device end interrupt (CC3) occurs at the completion of the clearing procedure. If an error occurs during the clearing procedure, the attachment presents an exception interrupt (CC2) with bit 0 (device dependent status available) set in the ISB.

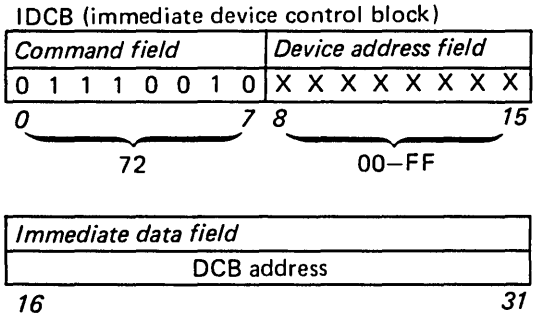
When the attachment receives a clear operation, it does the following:

- The attachment enters CCITT state 16 and starts a 2-second (T5) timer.
- When the attachment makes the transition to CCITT state 1, a device end interrupt (CC3) occurs.
- If CCITT state 1 is not reached within 2-seconds, an exception interrupt (CC2) is reported with bit 0 (device dependent status available) set in the ISB, BSC bits 13 and 15 (T5 time-out) set in cycle-steal status word 4 or SDLC bits 13 and 15 (T5 time-out) set in cycle-steal status word 5.
- CCITT state 16 may be entered from any state except state 1.
- If a Clear DCB is issued to the attachment while in CCITT state 1, a device end interrupt (CC3) occurs.

Start Modification

This command is used to modify the attachment microcode. This command initiates a cycle-steal operation for device 0. If issued to device 1, a delayed command reject is reported (information status byte, bit 1 is set on). The IDCB for this command is as follows:

IDCB (immediate device control block)



A description of the DCB for the Start Modification command is:

1. Word 0 is used to support KEY (bits 5–7).
2. Words 2–5 of the DCB are not used.
3. Word 1 of the DCB contains the address of the attachment storage location where the microcode patch begins.
4. Word 6 of the DCB contains the byte count of the number of bytes to be allocated in the attachment for the microcode patch.
5. Word 7 of the DCB contains the processor storage address where the microcode patch begins.

Note: The attachment does not support chaining for the Start Modification command.

Start

Information on the Start command is presented in Chapters 5 and 6 of this document.

Start Cycle-Steal Status

Information on the Start Cycle-Steal Status command is presented in Chapters 5 and 6 of this document.

Chapter 4. Status

Interrupt Information Byte (IIB)

When the attachment presents an interrupt request to the processor, the IIB is used to record information that cannot be indicated to the program by the condition codes (CCs). The IIB is meaningful only with condition codes 1, 3, or 4.

If the IIB bit 0 is a 1 when condition code 3 is reported, the suppress-exception (SE) bit was equal to 1 for a previous receive operation and a suppressible error occurred.

If condition code 1 (PCI) is reported, the IIB high byte contains the DCB identifier.

An attention interrupt (CC4) and IIB bit 0 set to 1 indicates a successful data circuit terminating equipment (DCE) initiated clear. An attention interrupt (CC4) and IIB bit 7 set to 1 indicates an unsuccessful DCE initiated clear. When interrupt condition code 2 is reported, the IIB has a fixed format called the interrupt status byte (ISB).

Interrupt Status Byte (ISB)

When the attachment presents an interrupt request to the processor, the ISB is used to record status that cannot be indicated to the program by condition codes. The ISB is meaningful only when interrupt condition code 2 is reported. The processor detects the ISB in bits 0–7 of the interrupt ID word.

Definitions of the ISB bits are as follows:

Bit 0 - Device-Dependent Status Available: If this bit is a 1, additional status is available by using the Start Cycle-Steal Status command. This bit may be a 1 in conjunction with bit 2 (incorrect-length record).

Bit 1 - Delayed Command Reject: This bit is a 1 for the following conditions:

- The command field of the IDCB contains an invalid function or modifier bit combination.
- The IDCB contains an odd DCB address.
- A Start command other than Start Control is issued in response to an attention interrupt caused by an incoming call.
- A Start Modification command is issued to device one.
- A command was issued to the wrong device.

Bit 2 - Incorrect-Length Record: This error can occur during both transmit and receive operations. It is caused by any of the following conditions:

- The byte count decremented to 0 because the attachment did not detect a change-of-direction (COD) character, and the chaining flag is off.
- The attachment detected a COD character, and the byte count has not been decremented to 0.

  In this case, interrupt status byte bit 0 is also a 1. A Start Cycle-Steal Status command can be used to determine the location of the COD in storage (residual address).

- In X.21 switched mode, if the byte count specified in the DCB is equal to or greater than the number of bytes received in the NPI, the attachment presents a device end interrupt (CC3) when state 12 (ready for data) is reached. If the byte count is not sufficient to allow for cycle-stealing all of the NPI signals into storage, the attachment reports an exception interrupt (CC2) with bit 2 (Incorrect-Length Record) set in the ISB.

Bit 3 - DCB Specification Check: This bit is set to a 1 if any of the following conditions exist when the DCB is examined:

- An odd byte chaining address with the chain bit set to a 1 in the control word.
- An odd byte SDLC status address with the SE bit set on in the control word.
- An odd byte data address for a Start Cycle-Steal Status command.
- The SDLC byte count does not equal 8 or 12 for a Start Cycle-Steal Status command.
- There is an odd byte data address for a Start Diagnostic command.
- The byte count is not hexadecimal 11 for a Start Diagnostic 1 command.
- The byte count is not 2 for a Start Diagnostic 2 command.
- The byte count is 0 for a receive operation.
- The byte count is 0 for a transmit operation.
- The input flag (I/F) bit of the control word was not set to 1 for a Start Diagnostic or a Start Cycle-Steal Status command.
- More than one of the following operations was specified in the control word at the same time: receive, transmit, disable terminal, and enable terminal.
- Bit 3 of the SDLC control word is set to one for a Start command.
- Bit 1 of the SDLC control word is set to one for a Start command without a previous set mode DCB specifying PCI.
- The I/F bit of the control word for a NPI Set Control DCB or Auto-Answer DCB is not set to one.
- A Start command was issued to the wrong device.
- The BSC byte count does not equal 6 or 10 for a Start Cycle-Steal Status command.
- An SDLC receive operation with the SE bit set to 0.
- An Auto-Answer or NPI DCB which specifies a byte count greater than 255.
- A Set Control DCB issued to a leased line with a Clear, NPI, Selection or Direct Call, or Auto-Answer command specified.
- A Set Mode, DCB with direct call and selection or facility registration/cancellation specified.
- A DCB other than a transmit or receive with the program-controlled-interrupt (PCI) bit set to one in the control word was issued.
- A set mode DCB specifying duplex when the BSC jumper is on was issued.
- A set mode DCB specifying installation test (bit 13 set to one in word 1 of the DCB) was set to one while any other bit in word 1 of the DCB is set to one.
- A Set Mode DCB specifying selection (Bit 15 or in word 1 of the DCB) and the byte count (DCB word 6) specified as zero.
- A Start Diagnostic 1 command occurred with any bit set to one in the control word other than bit 2 or bits 5–7. A Start Diagnostic 2 command occurred with any bit set to one in the control word other than 2, 5, 6, 7, or 15.

- In BSC mode, an exit transparent command was issued with the byte count not equal to 2.
- A Start Control command with a DCB specifying Auto-Answer, Clear, or NPI with the chaining bit set to one.
- A Start Control command with a DCB specifying Auto-Answer, or NPI without the set exception (SE) bit set to one.
- A Start Control command with a DCB specifying Auto-Answer or NPI with an odd status address.
- A Start Control command issued specifying Auto-Answer, NPI, or a set mode with selection, or a direct call set to one when the attachment is already connected on a switched line.

Bit 4 - Storage Data Check: This bit is set to 1 during cycle-steal output operations only to indicate that the processor storage location accessed during the current cycle contains incorrect parity. The attachment ends the operation with an exception interrupt request.

Bit 5 - Invalid Storage Address: This bit is set to 1 if the address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment ends the operation with an exception interrupt request.

Bit 6 - Protect Check: This bit is set to 1 if the attachment attempts to access a storage location without the correct cycle-steal key.

Bit 7 - Interface Data Check: This bit is set to 1 if a parity error was detected on an interface cycle-steal data transfer. The condition may be detected by the channel or the attachment. In either case, the attachment ends the operation with an exception interrupt request.

Status After Resets

Power-On Reset

Resets the attachment, performs an attachment storage and attachment read-only storage test, and resets the X.21 interface to DTE ready. The control parameters are reset to no PCI and half-duplex.

System Reset

Acts the same as power-on-reset except that no attachment storage test is performed.

Halt I/O and Device Reset

Functions the same as the power-on-reset, with the exception that the prepare level and I-bit, residual address and control parameters are not reset. Device reset does not reset the X.21 state.

The following table shows the function for each of the resets:

Reset function	Reset used			
Reset prepare level	Power on reset	System reset		
Reset I bit	Power on reset	System reset		
Reset X21 interface (DTE ready)	Power on reset	System reset		Halt I/O
Reset all DCB information displayed by communication indicator panel	Power on reset			
Reset residual address	Power on reset			
Reset residual byte count	Power on reset	System reset	Device reset	Halt I/O

Condition Codes

The attachment or channel reports condition codes to the processor during the execution of every Operate I/O instruction and upon acceptance of every interrupt. Condition codes are recorded in the even, carry, and overflow indicators.

Condition codes reported during an Operate I/O instruction are as follows:

CC value	Even	Carry	Overflow	Reported by	Meaning
0	0	0	0	Channel	Device not attached
1	0	0	1	Device	Busy
2	0	1	0	Device	Busy after reset
3	0	1	1	Device	Command reject
4	1	0	0	Device	Intervention req'd*
5	1	0	1	Chan/Dev	Interface data check
6	1	1	0	Device	Controller busy
7	1	1	1	Device	Satisfactory

*Not reported by the attachment.

Condition codes reported during interrupt acceptance are as follows:

CC value	Even	Carry	Overflow	Meaning
0	0	0	0	Controller end
1	0	0	1	PCI
2	0	1	0	Exception
3	0	1	1	Device end
4	1	0	0	Attention*
5	1	0	1	Attention and PCI*
6	1	1	0	Attention and exception*
7	1	1	1	Attention and device end*

*Not reported by the attachment.

Notes:

1. The attachment presents attention interrupts with the base device address.
2. The attachment presents an attention interrupt when it detects an incoming call (state 8) and is not already in auto-answer mode.
3. If the attachment detects a DCE clear indication (state 19), the attachment starts a 2-second timer (T6), completes the line clearing process, and presents an attention interrupt (CC4) with bit 0 (clear successful) set in the IIB. If the clearing process is unsuccessful, an attention interrupt is presented with bit 7 (clear failure T6 time-out) set in the IIB.
4. If an Operate I/O command is being processed when a clear indication is detected, the attachment reports an attention interrupt as indicated above. The software must issue a device reset to the busy lines to clear the busy condition in the attachment.

Chapter 5. Synchronous Data Link Control (SDLC/HDLC)

The synchronous data link control/high level data link control (SDLC/HDLC) capability allows transfer of serial data to and from a remote terminal or host system by a DCE and communications line facility. The SDLC/HDLC function can be used for connecting a Series/1 processor to telecommunication equipment or to other processors having compatible adapters.

Note: The attachment processes both the SDLC and HDLC protocols in the same manner.

- Data transmission uses SDLC/HDLC control procedures.
- Any 8-bit data code may be used.
- Bit rates can be up to 56,000 bps using V.35 interface.
- The attachment may serve as either a primary or secondary station.
- Internal clocking is available for local attach 1 mode operation.
- Non-return-to-zero inverted (NRZI) coding is used with internal clocking (local attach 1).
- Non-return-to-zero (NRZ) coding or NRZI coding may be used with clocking supplied by the DCE or local attach 2.

Data transmission is serial-by-bit, using the synchronous data link control (SDLC) method of character and bit transmission. For a general discussion of the SDLC/HDLC procedures see *IBM Synchronous Data Link Control — General Information*, GA27-3093.

The attachment can communicate with host systems using Extended Binary-Coded Decimal Interchange Code (EBCDIC) or any other 8-bit data code. The SDLC/HDLC uses a specific set of line control characters, but because of an inherent transparency in SDLC/HDLC, the data characters can be any 8-bit code that is mutually acceptable to the sending and receiving stations.

The SDLC/HDLC communication can operate on a leased line at rates up to 56,000 bps using V.35 interface.

When using internal (business machine) clocking (local attach 1), the characters are transmitted and received using NRZI coding. When clocking is provided by the DCE, software may select either NRZ or NRZI coding. Internal clocking provides the strobe pulses used to strobe bits between the DCE and the attachment. In receive mode, internal clocking also establishes and maintains bit synchronization through an advance or retard of the data strobe. A transmission rate of 9,600 bps is available through the internal clocking feature.

Operating Modes

Monitor Mode

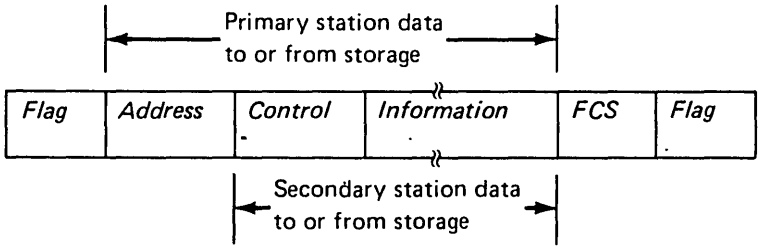
A receive operation places the attachment in monitor mode. While in this mode, the attachment is constantly monitoring the line, looking for a flag character. If the attachment is operating as a secondary station, it checks the address following the flag. If the address is its own (or the broadcast address), the attachment goes into receive mode. If the address is not the address of the attachment, the attachment remains in monitor mode.

IPL Mode

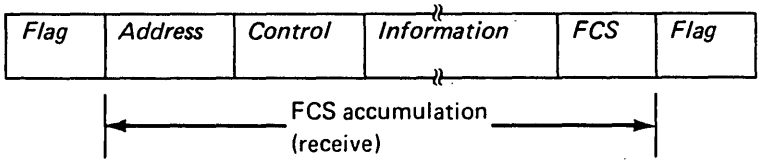
The attachment is placed in IPL mode by the attachment IPL jumper. While in this mode and not busy, the attachment monitors for an IPL sequence. If it receives an IPL sequence, the attachment processes it and presents a device end interrupt. If an error occurs during the IPL sequence, the attachment holds the IPL line to the processor active and again monitors for the IPL sequence.

Receive Mode

If the attachment is operating as a primary station, data is transferred to main storage beginning with the A-field (address field). When the attachment is operating as a secondary station in receive mode, data is transferred to processor storage beginning with the C-field (control field). It also automatically checks the received address to determine if the frame is intended for this station. If the frame is intended for this station, the attachment transfers the data to storage (beginning with the C-field).

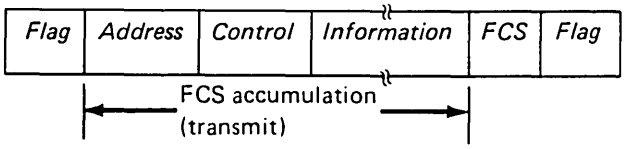


The accumulation of frame-check sequences starts with the address and includes the received frame-check sequence (FCS).



Transmit Mode

This mode is established when the program issues a transmit operation. Frame-check sequence accumulation begins with the first character to be transmitted after the beginning flag character and continues until the byte count (DCB word 6) decrements to 0.



The attachment then automatically transmits the frame-check sequence (FCS) followed by a flag character. If the attachment is operating as a primary station, the address of the receiver comes from processor storage. If the attachment is operating as a secondary station, the hardware provides the A-field of the frame.

SDLC/HDLC IPL

When the attachment is not busy processing a software command, it monitors the 'receive data' line for an IPL sequence. The IPL sequence proceeds as follows:

1. The system doing the IPL sends a Set Initialization Mode (SIM) command that causes the Series/1 processor to begin an IPL sequence. The bit configuration of the control byte for the SIM command is hex 17. All of the commands and responses in this sequence are common to both SDLC and HDLC protocols.
2. If the allow IPL jumper is installed, the attachment responds with an unumbered acknowledgement (UA, hex 73). The attachment sets the IPL line to the Series/1 and prepares the system to receive the IPL data. If the attachment is not jumpered for allow IPL, a disconnected mode (DM, hex 53) response is issued by the attachment.
3. The system doing the IPL transmits one data frame of up to 64000 bytes. The first byte of data in the information field (I-field) is placed in the Series/1 processor storage at location 0.
4. If the received frame check sequence (FCS) is valid, the Series/1 transmits a receive not ready (RNR, hex 35) with an Nr count equal to 1 to acknowledge receipt of the information frame (IPL load). The attachment then presents an interrupt to the processor on level 0 with the attachment device address in register 7 (the attachment is automatically prepared to level 0 with the I-bit set on). Program execution then starts at location 0.
5. Should a data error be detected, the attachment holds the IPL line to the processor active, does not respond, and monitors for a retry (new set initialization mode (SIM) command). The system doing the IPL must start the sequence anew and not simply retransmit the I-frame.

   Notes:

   a. The attachment monitors for the IPL sequence only when not busy; therefore, if a receive operation is pending and a SIM command is received, it is passed to the software the same as a normal frame.

   b. While the I-frame containing the IPL load may be up to 64K-bytes long, it is not recommended that an IPL load of this length be used. The 16-bit frame check sequence (FCS) loses some of its inherent checking capability when the frame length is greater than 4000 bytes. Also, the possibility of receiving a line hit and bad data, even though it is determined to be invalid by the FCS, is also a function of the length of the I-frame.

   c. If a secondary station address is jumpered, the attachment monitors for the IPL command frame as a secondary station. If no station address is jumpered, the attachment monitors for the IPL command as a primary station.

Switched Line IPL

On a switched line, the attachment IPLs as follows:

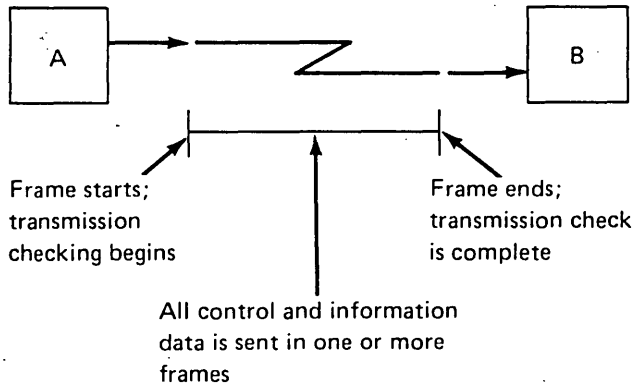
1. When detecting an incoming call, the attachment determines if it has been prepared.
2. If the attachment has been prepared, it presents an attention interrupt and allows the software to issue an Auto-Answer DCB as in normal operation.
3. If no Auto-Answer is issued within 300 milliseconds, and the allow IPL jumper is installed, the attachment disregards the call progress signals (CPS) and the DCE network provided information (DPI) signals passed from the DCE during call establishment.
4. The attachment then monitors for the IPL sequence as discussed in the preceding section, SDLC/HDLC IPL.

Transmission Codes

The SDLC/HDLC function allows data communication using any 8-bit data code, including EBCDIC.

Control Characters

Two levels of information grouping are used in SDLC/HDLC procedures. The basic level, called a frame, is checked by the attachment for transmission errors. The frame is the vehicle for all commands, responses, and information transmitted using SDLC/HDLC procedures.

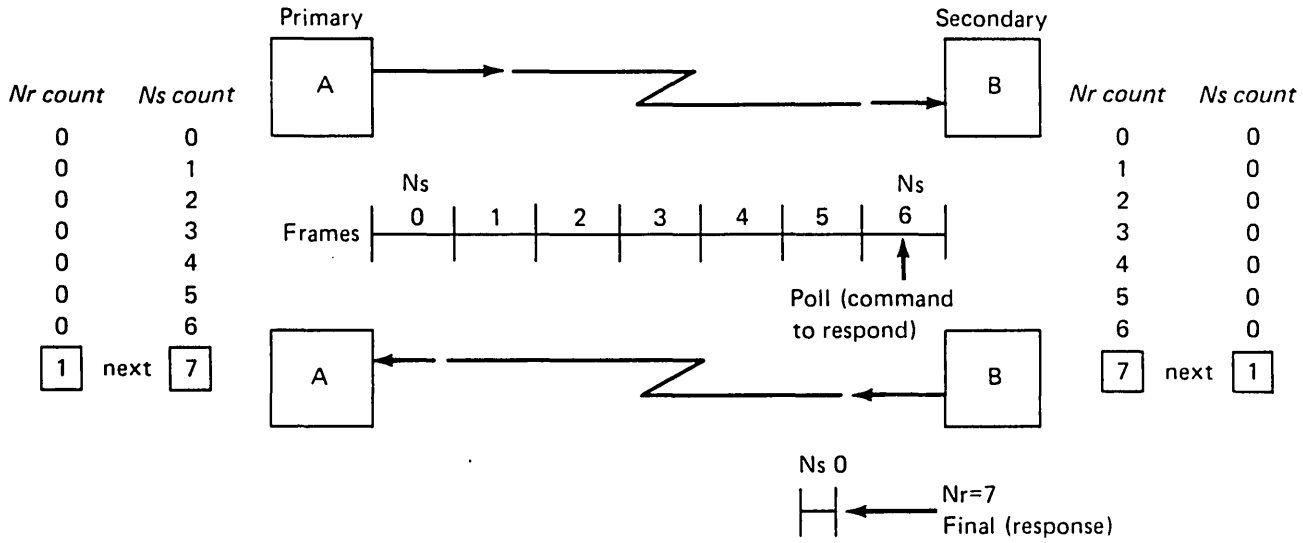


In the higher level of grouping, a frame sequence is checked by the program for missing or duplicated frames. At a station that transmits sequenced frames, the program counts and numbers each sequenced frame; this count is called Ns. At a station receiving sequenced frames, the program counts each error free sequenced frame that it receives; this count is called Nr.

The program advances the Nr count when it checks a frame and finds it to be error free. Nr then becomes the count of the next expected frame and should agree with the next incoming Ns count. If the incoming Ns does not agree with Nr, the frame is out of sequence, and the Nr count does not advance. Out-of-sequence frames are rejected or saved, at the option of the program. The receiving station accepts the incoming Nr count (confirmation) if the out-of-sequence frame is otherwise error free.

The counting capacity for Nr or Ns is 8, using the digits 0 through 7. These counts can wrap around; (7 is followed by 0). Up to seven frames may be sent before the receiver reports its Nr count to the transmitter because some or all of the frames may need repeating. The reported Nr count is the sequence number of the next frame that the receiving station expects to receive, therefore, if the count is not the same at a checkpoint as the transmitter's next sequence number, some of the frames already sent must be repeated.

The Nr and Ns counts of both stations are initialized to 0 at the discretion of the primary station. At all other times, the counts advance as sequenced frames are sent and received.



If B responds with Nr =:	*Then A may send, on request, Ns frames:*
7 (as above, all frames check OK)	7, 0, 1, 2, 3, 4, 5 (continue)
6 (frame 6 discarded because of error)	6, 7, 0, 1, 2, 3, 4 (retransmit and continue)
5 (error on frame 5; 5 and 6 discarded)	5, 6, 7, 0, 1, 2, 3 (retransmit and continue)
4 (error on frame 4; 4–6 discarded)	4, 5, 6, 7, 0, 1, 2 (retransmit and continue)
3 (error on frame 3; 3–6 discarded)	3, 4, 5, 6, 7, 0, 1 (retransmit and continue)
2 (error on frame 2; 2–6 discarded)	2, 3, 4, 5, 6, 7, 0 (retransmit and continue)
1 (error on frame 1; 1–6 discarded)	1, 2, 3, 4, 5, 6, 7 (retransmit and continue)
0 (error on frame 0; no frames accepted)	0, 1, 2, 3, 4, 5, 6 (retransmit)

Note: Shaded frames are retransmitted.

Frame Format

All active communication regulated by SDLC/HDLC procedures have a format called a frame, with each frame enclosed in flags.

Starting from the beginning flag as a reference point, eight consecutive binary bits are dedicated to the secondary station address (A). The next eight consecutive bits comprise the control (C) information, which can be a command or response. At least 16 more bits are transmitted after the C-field before the ending flag is sent. These 16 bits, called the frame-check sequence (FCS) contain the transmission checking information; therefore, the internal structure of any valid frame must consist of at least 32 consecutive binary bits. Any information (I) field is sent following the C-field and preceding the FCS field. The I-field is not restricted in format or content. In a frame with an I-field, the maximum length is not restricted.

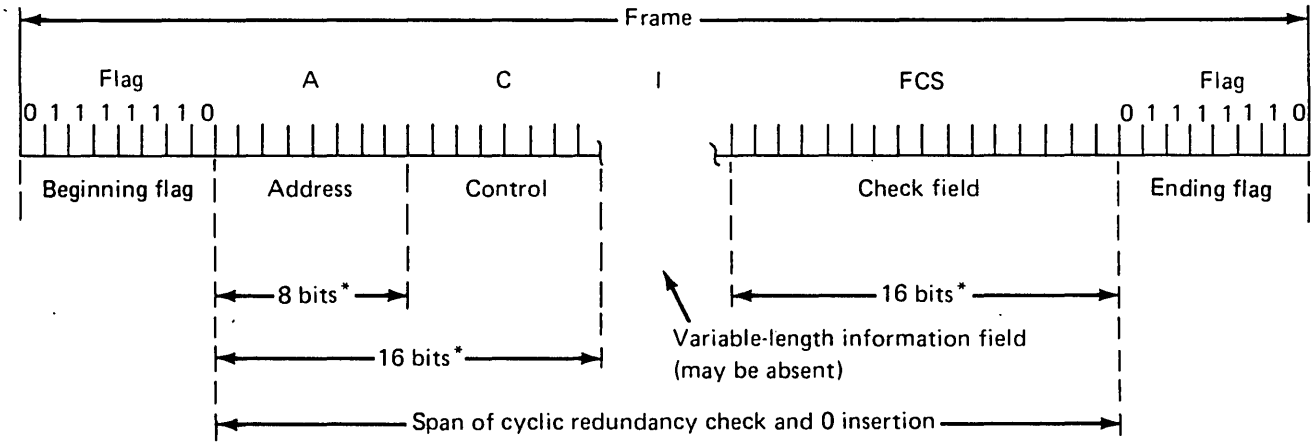
The transmission check at the receiver is complete when the ending flag is recognized. The receiving attachment separates the I-field from the FCS information when the ending flag is received, and does not put the FCS into storage.

Flag

Two flags, the beginning flag and the ending flag, enclose the SDLC/HDLC frame. The beginning flag serves as a reference for the positions of the A and C-fields, and initiates transmission error checking; the ending flag ends the check for transmission errors. Both beginning and ending flags have the binary configuration 01111110. The bit orientation of SDLC/HDLC allows the flag to be recognized at any time.

Notes:

1. A flag can be followed by a frame or by another flag.
2. For a receive operation, the flags are detected but not passed to the processor.
3. For a transmit operation, flags are transmitted at the beginning and ending of a frame, as well as between frames for chaining operations. Line speed, channel availability, and software efficiency affects the insertion of flags between frames.
4. To eliminate the possibility of the transmission line going idle or the receiving station losing synchronization during idle transmission periods, use the hold line active (HLA) bit in the DCB.



*Excluding inserted 0's.

Frame Format

Primary/Secondary Station Addressing

During a receive operation, when the attachment is jumpered for operation as a secondary station, the attachment compares the address to its own individual address and to the common station address (broadcast address - all 1's) to determine if it should accept the frame associated with the address just received.

Note: The address does not pass on to the processor.

During a receive operation, when the attachment is jumpered for operation as a primary station, the address is not examined but is passed to the processor.

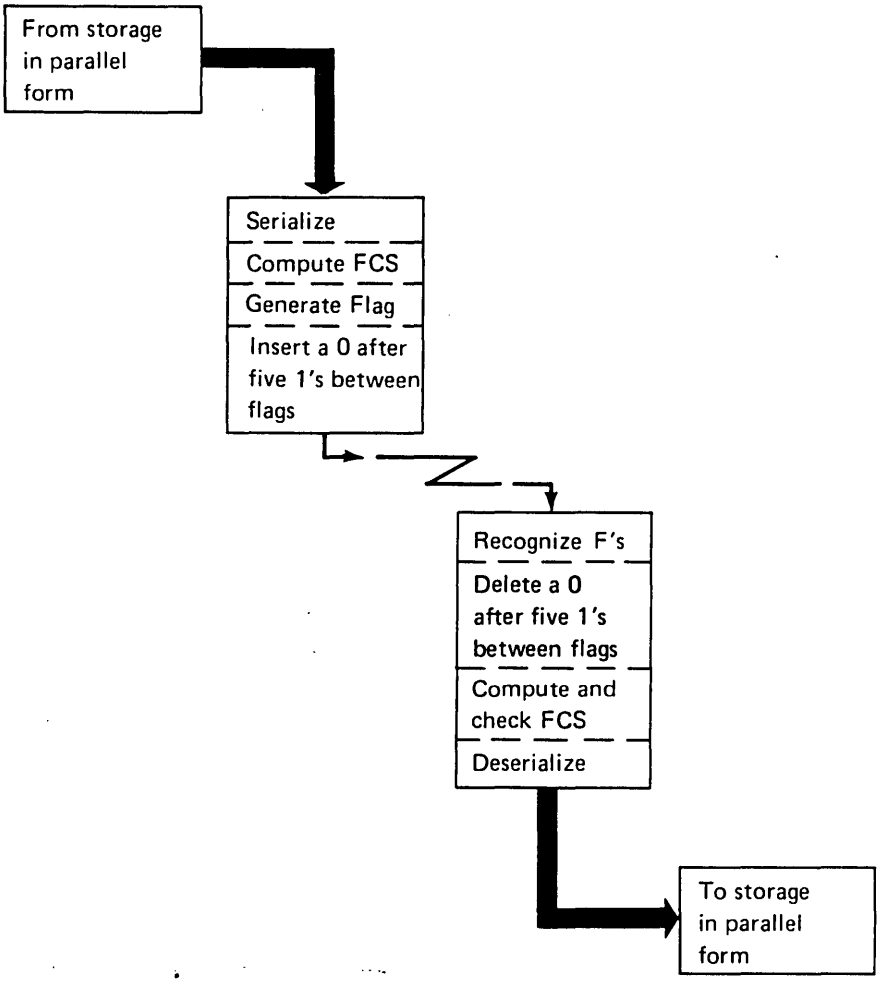
During a transmit operation, when the attachment is jumpered for operation as a secondary station, the attachment reads its address from the address jumpers and transmits it after the initial flag. This procedure is accomplished without interaction with the processor.

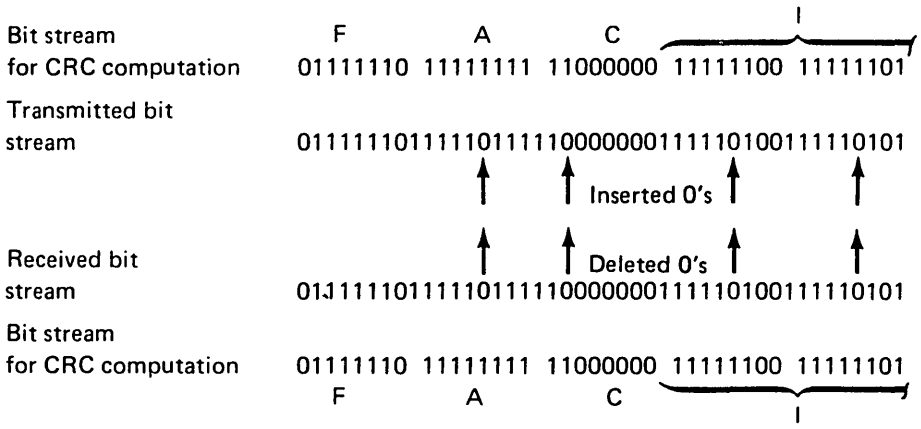
During a transmit operation, when the attachment is jumpered for operation as a primary station, the software must provide the secondary station address of the remote station as the first byte to be transmitted.

0-Insertion

A frame is identified because it begins with a flag and contains only non-flag bit patterns (the frame ends at the next flag). This characteristic does not restrict the contents of a frame, since SDLC/HDLC procedures require that the transmitting station inserts a binary 0 after any succession of five contiguous 1's within the frame. No pattern of 01111110 (flag) is ever transmitted by chance. After testing for flag recognition, the receiver removes a 0 that follows a received succession of five contiguous 1's. The attachment automatically provides 0-insertion and deletion. Inserted and removed 0's are not included in the transmission error check. (A 1 that follows five 1's is not removed.)

Note: When using NRZI transmission recording, 0-insertion eliminates the remaining possibility of prolonged non-transition periods in the active state. NRZI transmission allows the transmit data line to change states when a logical 0 is transmitted.





Data Link Control Functions and Zero Insertion/Deletion

Active Stations

A series of contiguous flags can be transmitted by a station to maintain bit synchronization and to maintain the data link in an active state. In duplex mode, a series of flags may also be used to hold the authority to transmit and to avoid time-outs at the linked station(s). In half-duplex mode, if no poll/final (P/F) bit was sent on the preceding frame, a series of flags may also be used to hold the authority to transmit and to avoid time-outs at the linked station(s).

Note: The use of NRZI transmission recording and 0-insertion is restricted to the active state of the data link.

Address Field

The primary station manages a data link by issuing commands to the secondary stations that recognize their addresses in the A-field of a received frame.

A primary station can address all secondaries by sending an all 1's address (hex FF). A secondary station may receive a common address or its individual address; however, when a secondary station sends any response, only its individual address is used.

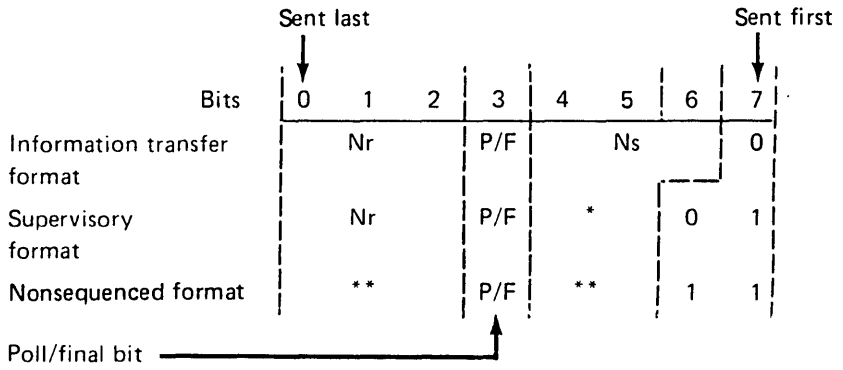
Balanced Operation

When duplex mode us used to support CCITT recommendation X.25 for link access procedure (LAP) and link access procedure, balanced mode (LAPB), the address field used as follows:

	Frame address (hexadecimal)	
	DTE to DCE	DCE to DTE
Command frame	01	03
Response frame	03	01

Control Field and Poll/Final (P/F) Bit

The control field (C-field) contains, within its eight binary digits, the capability to encode the commands and responses required to control a data link. The C-field has the following three formats:



*Codes for supervisory commands/responses
**Codes for nonsequenced commands/responses

Note: The commands and responses are controlled by software to correspond to the link level protocol used.

Each C-field contains the format identifier and poll/final (P/F) bits. The codes for the C-field commands and responses are as follows:

Format (See Note)	Sent last ↓ Binary configuration		Sent first ↓	Acronym	Command	Reponse	I-field prodibited	Resets Nr and Ns	Confirms frames through Nr-1	Defining characteristics
NS	000	P/F	0011	U1	X	X				Command or response that requires unnumbered information
	000	F	0111	RIM		X	X			Initialization needed; expect SIM
	000	P	0111	SIM	X		X	X		Set initialization mode: the using system prescribes the procedures
	100	P	0011	SNRM	X		X	X		Set normal response mode: transmit on command
	000	F	1111	DM		X	X			This station is offline
	010	P	0011	DISC	X		X			Do not transmit or receive information
	011	F	0011	NSA		X	X			Acknowledge NS commands
	100	F	0111	FRMR		X				Invalid frame received; must receive SNRM, DISC, or SIM
	101	P/F	1111	XID	X	X				System identification in I-field
	001	P/F	0011	NSP	X		X			Response optional if no P-bit
	111	P/F	0011	TEST	X	X				Check pattern in I-field
S	Nr	P/F	0001	RR	X	X	X		X	Ready to receive
	Nr	P/F	0101	RNR	X	X	X		X	Not ready to receive
	Nr	P/F	1001	REJ	X	X	X		X	Transmit or retransmit, starting with frame Nr
I	Nr	P/F	Ns 0	I	X	X			X	Sequenced I-frame

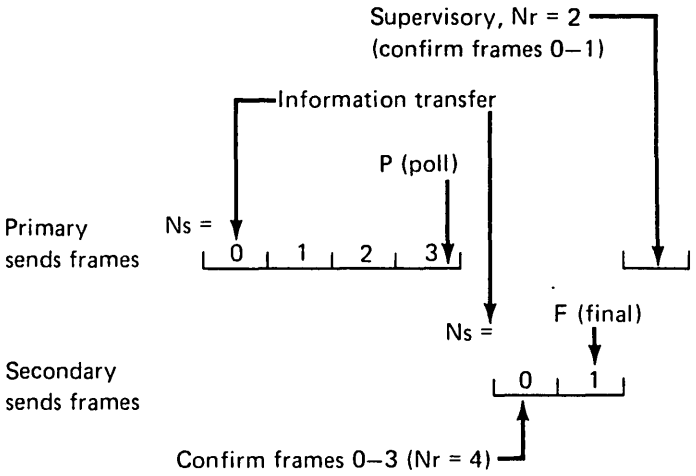
Note: NS = nonsequenced, S = supervisory, I = information.

The P/F bit is the send-receive control. A poll bit is sent to the secondary station to authorize transmission; the secondary station returns a final bit in response to the poll bit. **Do not confuse the final bit with the F-frame (flag) delimiter pattern.** Normally, only one poll bit is outstanding (unanswered by a final bit) on a data link.

Information Transfer Format

A C-field in the information transfer format is a part of each sequenced frame transmitted over a data link. The C-field contains the poll-final (P/F) bit and the Nr and Ns counts.

Stations transmitting information-transfer frames request configuration by sending the Ns count; they confirm by sending the Nr count.



Supervisory Format

The supervisory format is used with the information transfer format. Frames containing a supervisory format C-field convey ready or busy conditions and can be used to report sequence errors (thus requesting retransmission). Such frames may be interspersed with frames having a C-field of the information transfer format. Whether or not a primary station has information data to transmit, it may use a frame having a C-field of the supervisory format to poll a secondary station. A secondary station may use the supervisory format to respond to a request for confirmation. Frames with a supervisory format C-field are not counted in the Nr or Ns counts.

Nonsequenced Format

Command and response frames having a C-field in nonsequenced format are used for data link management. Data link management includes activating and initializing secondary stations, controlling the response mode of a secondary station, and reporting of procedural errors (not recoverable by retransmission). Information data may also be transmitted, using a frame with a C-field of the nonsequenced format. Frames with a nonsequenced format C-field are not counted in the Nr or Ns counts.

Information Field (I-Field)

An I-field is normally included with every frame having a C-field in the information-transfer format. These information-transfer frames are the only ones that are sequenced.

SDLC/HDLC procedure is designated as a vehicle for data contained in the I-field. The I-field contains data that is moved, by using the data link, from place to place in the system. The I-field is unrestricted in format and content and its contents are not apparent to the components of data link control.

There are provisions for an I-field in frames with a nonsequenced format C-field, but these are unprotected by sequence checking.

Frame Check Sequence Field

The FCS field, also called the block check character (BCC), contains 16 binary digits. It follows the I-field (if there is one; the C-field if not) and immediately precedes the ending flag. These 16 digits result from a mathematical computation on the digital value of all binary bits within the frame (excluding inserted 0's). The purpose is to validate transmission accuracy.

The transmitting SDLC/HDLC attachment performs the computation and sends the resulting FCS value. The receiving SDLC/HDLC attachment performs a similar computation and checks its results; it discards a frame that is found to be incorrect and does not advance its Nr count.

Synchronization

The basic SDLC/HDLC attachment receives timing pulses from the DCE. This establishes and maintains bit synchronization. When the attachment starts to transmit, it automatically transmits a flag character to establish frame and byte synchronization.

Some DCE (to operate properly) may require NRZI-recorded data and/or pad characters. DCB control word bits 9 and 12 may be used to satisfy particular DCE requirements.

If internal clocking (local 1 attach mode) is used, the attachment operates in NRZI mode. It automatically sends two pad characters (hex 00) before sending the beginning flag, which causes 16-bit transitions to precede the flag character.

SDLC/HDLC Timers

The attachment has two programmable timers. Each timer can count up to 27 seconds, in 106-millisecond increments. Bits 0 through 7 of DCB word 1 control timer 1, and bits 8 through 15 control timer 2.

Timer 1

Timer 1 can be used in a variety of ways:

- *Idle detect timer.* If a receive operation is specified, the attachment runs timer 1 for the duration specified by bits 0 through 7 of DCB word 1. When this time runs out, the attachment begins checking the line for an idle condition. If it detects an idle condition, the attachment presents an exception-interrupt request.

  If the attachment detects a flag character while timer 1 is running, it immediately begins checking for an idle condition and stops timer 1. If it detects an idle condition from the time that timer 1 stops until the receive operation ends, the attachment presents an exception-interrupt request.

  If the program assigns a value of 0 to timer 1, the attachment does not check for an idle condition.

  Note: An idle condition is 15 contiguous 1's on the line.
- *DCE ready time-out.* This time-out occurs if DCE ready is not returned by the DCE within the specified time during an enable terminal operation. In V.35 mode, the attachment waits for 'data set ready' (DSR) to come ready. If the time-out period is specified as 0, no time-out occurs.
- *Disable data terminal ready time-out.* During a disable terminal operation, a time-out occurs if DCE ready is not deactivated within the specified time. A timer value of 0 causes the attachment to wait indefinately for the DCE to go ready. Failure to receive DCE ready within the specified time results in an exception interrupt with bit 0 (device dependent status available) set in the ISB and bit 4 (time-out) set in cycle-steal status word 2. DCE ready must be active before the transition to DTE controlled not ready can be made (state 14). If the time-out period is specified as 0, no time-out occurs.

  Note: Disable must not be issued when device one is busy.
- *Auto-Answer time-out.* Along with the Auto-Answer command, timer 1 is used to limit the time the attachment waits for an incoming call. If the time-out period is specified as 0, no time-out occurs.
- *Clear to send time-out.* During a transmit operation, a DCE interface error occurs if 'clear to send' (CTS) is not returned by the DCE within the specified time. If the time-out period is specified as 0, no time-out occurs.

  Note: This CTS time-out is valid only in V.35 mode of operation.
- *Program delay.* When the operation is not an enable terminal, disable terminal, receive, or transmit operation, the program can use timer 1 for timing purposes. A value of 0 results in an immediate device end interrupt (CC3).

Timer 2

Timer 2 is used in the following ways:

- *Nonproductive receive time-out.* This time-out is used only during receive operations. Its purpose is to limit the total nonproductive receiving time for a total receive operation. A total receive operation can be a single receive operation or a chain of receive operations initiated by a single Operate I/O instruction.

When chaining receive operations, the value for timer 2 is taken from each DCB in the chain. The timer runs anytime the attachment is not receiving flags or frames. When timer 2 times out, the attachment presents an exception interrupt request. When the timer is set to 0's, no time-out occurs.

- *Hold-line-active timer.* When timer 2 is used in conjunction with a transmit operation, with bit 15 on in the DCB control word, the attachment transmits flag characters for the duration of the time specified by bits 8 through 15 of DCB word 1, or until another transmit operation begins.

Note: A value of 0 set into timer 2 causes the attachment to hold the line active for either 0-time or an indefinite time.

SDLC/HDLC Commands

There are two SDLC/HDLC commands:

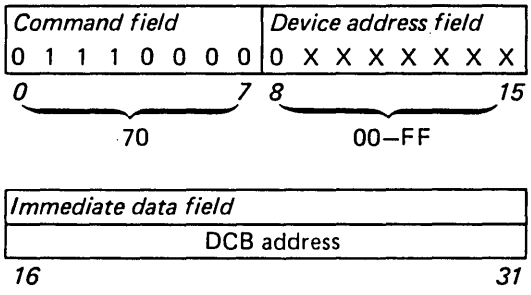
- Start
- Start Cycle-Steal Status

The programmer must ensure that the program always tests the Operate I/O condition codes following an Operate I/O Instruction.

Start

The Start command transfers the address of a DCB to the attachment. When the attachment accepts the Start command, it fetches the DCB from the processor storage address specified in the IDCB immediate data field and begins executing the operation.

IDCB (immediate device control block)



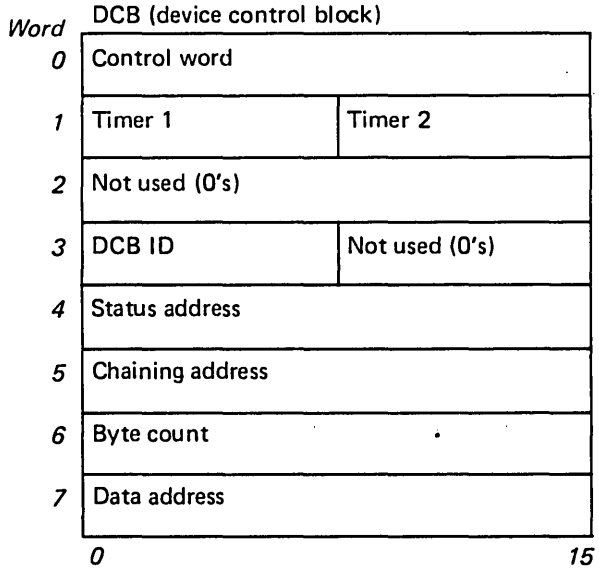
SDLC/HDLC Device Control Block (DCB)

The DCB is an 8-word area in processor storage that describes the specific parameters of the cycle-stealing operation. The program assigns its location in storage. The data is loaded and changed by the program. The attachment fetches the DCB using a cycle-steal address key of 000 after successful execution of a Start command.

The DCB address transferred to the attachment by the IDCB points to word 0. The table is in ascending storage address order, with the lowest storage address at the top of the table.

Note: The address of the DCB in processor storage must be even. If the address is odd, the attachment presents an exception interrupt (CC2), with bit 1 (delayed command reject) set in the ISB, and ends the cycle-steal operation.

The SDLC/HDLC DCB format is as follows:



Word 0 - Control Word

Bit 0 - Chaining Flag (CHN): If this bit is set to 1, the attachment fetches the next DCB in the chain after the successful completion of the current DCB operation. If this bit is set to 0 and the operation is successfully completed, the attachment presents a device end interrupt. If an error occurs on a transmit operation, the appropriate status is set in the attachment and an exception interrupt (CC2) is presented with the chaining action broken. In a receive operation, the suppress exception (SE) bit must be set to 0. This allows suppression of certain error conditions (refer to bit 2 for information on error interrupts).

Note: The attachment supports only command chaining.

Bit 1 - Program-Controlled Interrupt (PCI): This bit causes the device to present a PCI at the completion of the DCB fetch. The data transfer, associated with the DCB, may commence even though the PCI may be pending in the attachment. When this bit is set to 1, bits 0–7 of DCB word 3 are placed in the interrupt information byte (IIB) upon interrupt presentation.

The attachment recognizes this bit only during a transmit or receive operation. A DCB specification check (bit 3 of the interrupt status byte) is presented if attempted on any other command.

To use the PCI, a Start Control command DCB must have been previously issued with bit 11 set to one in word 1 (Set Mode operation). If a Set Mode operation was not issued with this bit set to 1, the attachment reports an exception interrupt (CC2) with bit 3 (DCB specification check) set in the ISB.

Bit 2 - Input Flag (IF): When the input flag bit is set to 1, the attachment can cycle-steal data into processor storage once it establishes byte synchronization. A receive operation is specified when this bit is set to 1.

For a receive operation, a device end interrupt occurs if chaining is not specified and no errors occur. A device end interrupt occurs if the no-exception (NE) bit (residual status block (RSB) word 1, bit 15) is set in all residual status blocks associated with the current frame sequence. A permissive device end interrupt (interrupt condition code 3 and IIB bit 0 set) occurs if a RSB has had the NE bit set to 0 for any frame received in the current frame sequence. If bit 12 of the control word is set to 0 on a receive operation and the poll/final (P/F) bit is detected as set, chaining ends and the chained-to-DCB is not fetched. Therefore, avoid the use of chaining from a receive operation to any operation other than a receive.

Since IPL is supported, use receive DCB chaining to handle frame sequences. The IPL function requires the attachment to search for the SIM command. If a frame is received other than SIM, it is discarded. Therefore, the attachment cannot anticipate another receive command when chaining is not used.

An error interrupt is present when:

- The X.21 DTE/DCE interface is not ready for data transfers (bit 0, device-dependent status available, of the ISB is set).
- The V.35 DSR interface line is off (bit 0, device-dependent status available, of the ISB is set).
- The byte count in the DCB is specified as 0 (bit 3, DCB specification check, of the interrupt status byte (ISB) is set).

Bits 0–7 of word 1 of the DCB can be used with the input flag bit to specify the idle detect time-out period.

DCB word 1, bits 8–15 can be used with the input flag bit to specify the nonproductive receive time-out period.

> **Note:** The input flag bit must be set to 1 whenever data is to be cycle-stolen into processor storage. Therefore, it must also be set to 1 when either a Start Diagnostic or a Start Cycle-Steal Status command is initiated to prevent a DCB specification check error interrupt from occurring.

Two types of general errors exist: suppressible and nonsuppressible. Nonsuppressible errors always cause an exception interrupt request (CC2). The following errors are suppressible:

- Overrun
- Aborted frame
- Incorrect-length record
- Frame check sequence (FCS)

The action taken when a suppressible error occurs depends on the setting of the suppress exception (SE) bit (which must be a 1 for receive mode). If the SE bit is a 1, the attachment posts the error in the residual status block and either presents a device end interrupt request (CC3) with interrupt information byte bit 0 set to 1 or chains to the next DCB.

Bit 3: This bit is not used and must be a 0.

Bit 4 - Suppress Exception (SE): Set this bit to 1 when a specifying a Receive command. If this is not done, the attachment presents an exception interrupt (CC2) with bit 3 (DCB specification check) set in the ISB. The SE bit allows the attachment to suppress errors that could cause it to miss the next frame. The attachment stores the RSB, beginning at the status address specified in the DCB, when a suppressible error occurs (including short frame) or when the byte count equals 0 upon detecting the ending flag. For a frame whose length in bytes is equal to the byte count specified in the DCB, or for a short frame, the NE bit (RSB word 1, bit 15) is set to one. In this case, the residual byte count in word 0 must be examined to determine the number of bytes received.

> **Note:** This attachment does not support SDLC/HDLC receive operations with the SE bit set to 0.

The attachment handles the SE bit as shown in the following table:

Conditions	Results							
	Chn bit	SE bit	P/F bit	Int CC	IIB bit 0 *	Chain	Post resid. status	EOC bit **
No errors	0	1	0	3	0	no	yes	1
	0	1	1	3	0	no	yes	1
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	0	no	yes	1
	1	1	1	***	n/a	yes	yes	0
Suppressible errors	0	1	0	3	1	no	yes	1
	0	1	1	3	1	no	yes	1
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	1	no	yes	1
	1	1	1	***	n/a	yes	yes	0

* When condition code 2 is reported, the IIB is called the ISB and bit 0 has a different meaning. Refer to "Interrupt Status Byte" in this chapter for a description of the ISB bits.

** Refer to status address (DCB word 4) for a description of this bit.

*** If the Pad/Control bit (bit 12 of the control word) is on during a receive operation, no interrupt (CC3) occurs, instead, chaining takes place.

For example, if a block check error occurs and the error can not be suppressed, an exception interrupt must be given with the block check character (BCC) error reported by the cycle-steal status operation. This could cause the attachment to miss the next frame if only one flag is between frames. By using the SE bit, the attachment cycle-steals the residual status block into storage (which indicates that a BCC error occurred for that frame) while continuing to check the received data.

Note: The attachment recognizes the SE bit only in conjunction with a receive operation; it is otherwise disregarded.

Bits 5–7 - Cycle-Steal Address Key (KEY): This is a 3-bit key presented to the processor by the attachment during data transfers so that the processor can ascertain whether the attachment can access certain processor storage blocks.

Bit 8: This bit is not used and must be set to 0.

Bit 9 - NRZI Coding (NRZI): This bit causes the transmission of data according to NRZI encoding. When using the internal clocking feature (local attach 1), NRZI encoding is automatic and this bit is disregarded.

Bit 10 - Enable Terminal (ENB): Use this bit to set the X.21 interface to DTE ready. When operating as X.21 leased, a device end interrupt or chain occurs immediately after DTE ready is set. When operating as X.21 switched, an interrupt or chain operation (if so specified by bit 0 of the control word) occurs after the the attachment detects state 1. This bit may be used with bits 0–7 of word 1 of the DCB to limit the time that the attachment waits for DCE ready to become active (27 seconds maximum).

Failure to get DCE ready in the specified time results in an exception interrupt with bit 0 (device dependent status available) set in the ISB, and bit 4 (time-out) set in cycle-steal status word 2. If timer 1 of the DCB is specified as 0, the attachment does not interrupt until DCE ready is returned.

If the V.35 jumper plug is installed, the attachment checks for 'data set ready' (DSR).

Note: Do not issue enable when device 1 is busy.

Bit 11 - Disable Terminal (DSB): This bit (in X.21 leased mode) causes the DTE to assume the DTE ready (state 1). An interrupt or chaining operation (if so specified by bit 0 of the control word) begins immediately after the DTE ready state is set.

This bit (in X.21 switched mode) causes the DTE to assume the DTE controlled not ready (state 14). An interrupt or chaining operation (if so specified by bit 0 of the control word) begins immediately after the controlled not ready state is set.

This bit, if set to one, causes an immediate device end interrupt if the V.35 jumper plug is installed.

This bit may be used in conjunction with bits 0 through 7 of word 1 of the DCB to limit the time the attachment waits for DCE ready to become active.

Failure to obtain DCE ready within the specified time results in an exception interrupt with bit 0 (device dependent status available) set in the ISB and bit 4 (time-out) set in cycle-steal status word 2. If timer 1 of the DCB is specified as 0, no time-out occurs. DCE ready must be active before the transition to DTE controlled not ready can be made (state 14).

Bit 12 - Pad/Control: If bit 14 of the control word is set to 1 (transmit mode), bit 12 causes the transmission of two pad characters (hex 55 or hex 00 if in NRZI mode) to precede the first flag of a frame sequence. If bit 2 of the control word is set to 1 (receive mode), bit 12 prevents the attachment from breaking a chaining operation (no interrupt) when the poll/final (P/F) bit is set to 1.

Bit 13 - Secondary/Primary (S/P): This bit determines if the attachment operates as a secondary or a primary station. Set this bit to 1 for a primary station and to 0 for a secondary station. However, during a receive operation, the attachment examines the address portion of a received frame only if the attachment is being used as a secondary station. On a transmit operation, the attachment generates its own address only when it is operating as a secondary station.

Bit 14 - Transmit Operation (XMIT):

X.21 Leased

This operation causes the attachment to verify that the DCE is ready (CCITT state 1). If the equipment (DCE) returns 'ready', the attachment activates the control lead for at least 24 bit times before establishing synchronization and cycle-steals data from processor storage. Data associated with the current DCB is transmitted as one frame.

If the DCB is not ready, an exception interrupt occurs immediately, with bit 0 (device-dependent status available) set in the interrupt status byte and bit 7 (DCE interface error) set in the cycle-steal status word 2.

If a 0 byte count is specified in the DCB, an exception interrupt is presented with bit 3 (DCB specification check) set in the ISB.

A device end interrupt is presented when the byte count goes to 0 and the chaining flag is off. The C-line is deactivated for half-duplex, but remains active for duplex operation.

X.21 Switched

This operation causes the attachment to verify that DCE is ready for data (CCITT state 12) before attempting to transmit data. If ready for data is presented to the attachment, the data associated with the current DCB is transmitted as one frame. If ready for data (CCITT state 12) is not present, an exception interrupt (CC2) occurs immediately.

If the DCE interface is not ready for data (CCITT state 12), an exception interrupt (CC2) occurs with bit 0 (device dependent status available) set in the ISB, and bit 7 (DCE interface error) set in cycle steal status word 2.

A device end interrupt (CC3) is presented when the byte count goes to 0 and the chaining flag is a 0.

If a byte count of 0 is specified in the DCB, an exception interrupt (CC2) is presented with bit 3 (DCB specification check) set in the ISB.

V.35 Leased

This operation starts a timer (refer to bits 0–7 of word 1 of the DCB) and sends a 'request-to-send' (RTS) to the DCE. As soon as 'clear-to-send' (CTS) returns from the DCE, the attachment establishes synchronization and cycle-steals data from processor storage.

An exception interrupt occurs immediately, with bit 0 (device-dependent status available) set in the ISB and bit 7 (DCE interface error) set in cycle-steal status word 2 if the 'data-set-ready' (DSR) line from the DCE is off. Failure to receive 'clear-to-send' (CTS) from the DCE within the time-out period results in an exception interrupt with bit 0 (device-dependent status available) set in the ISB and bit 7 (DCE interface error) set in cycle-steal status word 2.

Transmit mode is reset and 'request-to-send' (RTS) drops after the ending flag is transmitted. This process occurs only if the chaining flag is off and hold line active (bit 15 set) is not specified.

A device end interrupt is presented when the byte count goes to 0 and the chaining flag is off.

If a byte count of 0 is specified in the DCB, an exception interrupt is presented with bit 3 (DCB specification check) set in the ISB.

Bit 15 - Hold Line Active (HLA): Use this bit in conjunction with bit 14 (transmit operation). If bit 15 is a 1 when the byte count goes to 0, the attachment stays in transmit mode and transmits flag characters until another operation begins or until the time specified in timer 2 elapses.

> **Note:** A value of 0 set into timer 2 causes the attachment to hold the line active for either 0-time or an indefinite time. The controlling parameter, for example, if the attachment is operating in duplex mode; an indefinite 'hold line active' (HLA) occurs.

Word 1 - Timers: Use this 16-bit word to specify time-out periods. The amount of time is specified in increments of 106 milliseconds, with a maximum time-out period of 27 seconds.

Bits 0–7 Timer 1: In conjunction with receive (bit 2 of the control word set to 1), use these bits to specify the idle detect time-out period. If chaining of receive DCB's takes place, specify the time-out period in each DCB so that the attachment can detect an idle condition after it receives the first frame. If the time-out period is selected as zero, the idle detect timer does not run, and is therefore not checked.

> **Note:** The idle detect time-out period is a specified period of time. After this period of time, the receive line is checked for an idle condition (15 contiguous 1-bits).

In conjunction with enable terminal, use these bits to specify the DCE ready time-out period. A timer value of zero causes the attachment to wait indefinately for the DCE to become ready. In V.35 mode, the attachment waits as above for 'data set ready' (DSR) to come active.

When the enable terminal, disable terminal, input flag, and transmit bits of the DCB control word are set to 0, software can use timer 1 as a timer. If the timeout period is selected as 0, or when the timeout period expires, a device end interrupt is presented, or a chaining operation continues (if specified).

In V.35 mode, use timer 1 in conjunction with transmit to specify the clear-to-send time-out period.

> **Note:** The 'clear-to-send' (CTS) time-out period is the period of time that the attachment allows for the return of 'clear-to-send' (CTS) on a transmit operation, using the V.35 interface (DCE interface error, cycle-steal status word 2, bit 7, is set to 1).

Use timer 1 in conjunction with disable terminal to specify the time the attachment allows for the DCE to become ready. Then set the interface to DCE controlled not ready.

Bits 8–15 - Timer 2: Use timer 2 in conjunction with receive (bit 2 of the control word set to 1) to specify the non-productive receive time-out period. If chaining of receive DCBs is to take place, specify the time-out period in all of the DCBs in the chain. If the time-out period is specified as 0, the non-productive receive timer does not run, and is therefore not checked.

> **Note:** The non-productive receive time-out period is the period of time after which the current receive operation is terminated if the signal on the line is unintelligible (no frames or flags).

In conjunction with hold line active (HLA), use timer 2 to specify the amount of time that the line is active. In half-duplex mode of operation, when the time-out period is 0, the line is not active. In duplex mode of operation, when the time-out period is 0, the line is indefinately active.

Word 2: This word is not used.

Word 3 - DCB ID: If specifying PCI, bits 0–7 must contain the DCB identifier.

Word 4 - Status Address: Use the status address word in conjunction with bit 4, SE, of the control word. Use bit 4 of the control word and the status address only for receive operations. The address this word contains is the processor storage address of the RSB. If bit 4 of the control word is a 1 and the attachment detects any of the conditions that set residual status flags, an exception-interrupt request does not occur. Instead, the attachment automatically stores two words of information into the RSB and monitors the line, looking for an ending flag character. When it detects the ending flag, the attachment presents a normal device-end interrupt request or begins a chaining operation. The first word stored in the RSB is the residual byte count; the second word contains the residual status flags.

Residual Status Flags: The second word of the RSB contains the residual status flags. These bits have the following meanings:

Bit 0 - End-Of-Chain (EOC): This bit is associated with the permissive device end interrupt; that is, EOC is set to one when a frame having the P/F bit set to one is received and bit 12 of the control word is set to 0. EOC is also set to one if chaining is not specified in the current DCB.

Bits 1–7: These bits are not used and must be 0's.

Bit 8 - Overrun: This condition occurs during a receive operation.

Bit 9 - Abort: This condition occurs during a receive operation.

Bit 10 - Long Frame: This bit indicates that the byte count has been reduced to 0, and the current frame has not ended. The attachment continues to monitor the receive line until the end of the frame. However, any data received after the byte count reaches 0 is lost.

Bit 11 - Frame Check Sequence (FCS) Error: The FCS received is incorrect.

Bits 12–14: These bits are not used and must be 0's.

Bit 15 - No Exception (NE): This bit indicates one of two conditions. The first is that the frame is the correct length and error free. The second condition is that the attachment received an error free but short frame. To determine which condition caused this bit to be set, examine the residual byte count. If the residual byte count is not 0, a short frame was received.

Word 5 - Chaining Address: The chaining address word contains the storage address of the next DCB, and is used when chaining is indicated (bit 0 of the control word is a 1). The chain address must be even. If the address is odd, the attachment sets the ISB bit 3 to a 1 and ends the operation.

Word 6 - Byte Count: This 16-bit byte-count word contains the number of bytes to be transferred during the operation specified in the current DCB control word.

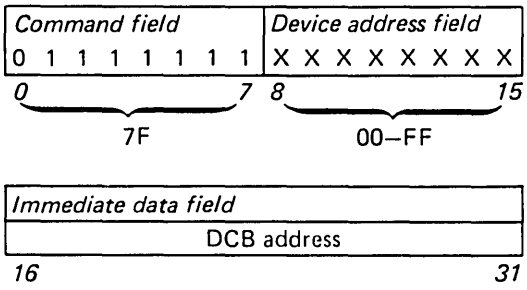
Word 7 - Data Address: This is the address in processor storage where data transfer starts.

Start Cycle-Steal Status

This command initiates a cycle-steal operation to the addressed device to collect status information relative to the previous cycle-steal operation (not start cycle-steal status).

The Start Cycle-Steal Status command causes the attachment to transfer status information (about the previous cycle-steal operation) to the processor.

IDCB (immediate device control block)



The word transferred from the data word position of the IDCB is the 16-bit logical storage address of the DCB.

When a cycle-steal data transfer is ended by an exception condition (interrupt condition code 2), bit 0 of the ISB may be set to one. If bit 0 is a one, further device information regarding the cause of the exception condition may be found by executing a start cycle-steal status (SCSS) command. This command may also be issued at any time to obtain information regarding logic card jumpers and DCE line status. The byte count for this operation must be 8 or 12 for SDLC/HDLC, and the data address must be even.

The format of the start cycle-steal status DCB is as follows:

Word	0 1 2 3 4	5 6 7	8 ... 15
0	0 0 1 0 0	K E Y	0's
1	Not used (0's)		
2	Not used (0's)		
3	Not used (0's)		
4	Not used (0's)		
5	Not used (0's)		
6	Byte count (see note)		
7	Data address (even)		

Note: The attachment supports a byte count of 8 for SDLC half-duplex on leased lines, and a byte count of 12 for switched X.21 operation. This is compatible with the current IBM software.

The data address (word 7) must be on a word boundary (bit 15 set to 0). If it is not, an exception interrupt request (CC2) occurs with DCB specification check bit (bit 3) set to 1 in the ISB.

See "Cycle-Steal Status Words" later in this chapter for a description of the status information.

Cycle-Steal Status Words

Word 0: Word 0 contains the processor storage address of the last attempted cycle-steal transfer. This residual address may be a data address, DCB address, or RSB address. The following table shows the type of address that the residual address can be for various error conditions. Where there is more than one possibility, the program must decide which type of address cycle-steal status word 0 contains.

Error condition	Residual address		
	DCB address	Status address	Data address
Delayed command reject	N/A	N/A	N/A
DCB specification check	X		
Storage data check	X		X
Invalid storage address	X	X	X
Protect check	X	X	X
Interface data check	X	X	X
Overrun		X	X
Time-out	X		X
Modem interface error	X		X
Block check error	X		X
Abort		X	X
Idle or inactivity detected	X		X
Nonproductive receive	X		X

Note: If an error should occur during a start cycle-steal status operation, the residual address is not altered.

Word 1: Word 1 contains the residual byte count for the previous data transfer.

Word 2: If you receive an exception interrupt request (CC2) and an ISB of hex 80, issue a Start Cycle-Steal Status (SCSS) command to further define the error.

Bit 0 - Overrun: During a receive operation, overrun occurs if the receive buffer (attachment hardware) is not read within 16-bit times since its last reading excluding 0-bit deletion).

During a transmit operation, overrun occurs if the transmit buffer was not reloaded within 16-bit times since it was last filled (excluding 0-bit insertion).

Bit 1 - Abort: While receiving a frame, seven consecutive 1-bits (no 0-bit insertion) were received after at least one byte of data had already been cycle-stolen into storage. If no bytes of data have been stored, the abort condition is ignored and the attachment continues to monitor the receive line for a flag or an idle condition.

Bit 2 - Long Frame: This bit indicates that the byte count has been decremented to 0, and the current frame being received has not ended.

Bit 3 - Block Check Error (BCC or FCS): The frame check sequence (BCC 16-bits) computed from the received data does not equal hex F0B8.

Bit 4 - Time-Out: This bit is set to one to indicate that one of the time-outs has occurred. Only one time-out may occur for any operation.

See word 5 for an indication of the DTE and DCE lines that were active when the time-out occurred.

In V.35 mode, the DCE did not return DSR after an enable operation.

Bit 5 - Idle Detect: This condition occurs during a receive operation after the idle detect time-out period has ended and 15 consecutive 1-bits (no 0-bit insertion) have been detected.

> **Note:** The attachment does not look for an idle condition if the idle detect time-out period is specified as 0.

Bit 6 - Nonproductive Receive: This bit is set to one if the attachment has been receiving bits that do not result in flags or frames for a period longer than that specified in bits 8–15 (timer 2) of word 1 of the DCB.

> **Note:** The attachment does not look for a nonproductive receive condition if the nonproductive receive time-out period was specified as 0.

Bit 7 - DCE Interface Error: In X.21 leased-line mode, the DCE went to DCE not ready during a transmit or receive operation.

In V.35 mode 'clear-to-send' (CTS) was not returned from DCE after setting 'request to send' (RTS).

In X.21 switched mode, the DCE interface is not ready for data.

Bits 8–12: These bits are not used and must be 0's.

Bit 13 - Local Attach 1: This bit indicates that the local attach 1 jumper is installed in the cable.

> **Note:** In local attach 1, the attachment provides clocking at 9,600 bps in SDLC/HDLC mode only. The clocking signal is not provided to the remote terminal.

Bits 14–15: These bits are not used and must be 0's.

Word 3

Bit 0 - Data Terminal Ready (DTR): This bit is set to 1 if DTR is active.

Bit 1 - Data Set Ready (DSR): This bit is set to 1 if DSR is active.

Bit 2 - Request-To-Send (RTS): This bit is set to 1 if RTS is active.

Bit 3 - Clear-To-Send (CTS): This bit is set to 1 if CTS is active.

Note: Bits 0–3 have no meaning on an X.21 network. However, for software compatibility, these bits have the following meaning:

Bit		0	1	2	3
SCSS following	Enable normal	on	on	off	off
	Enable error	on	off	off	off
	Disable normal	off	off	off	off
	Disable error	off	off	off	off
	Transmit normal	on	on	on	on
	Transmit error	on	on	on	off
	Receive normal	on	on	off	off
	Receive error	on	off	off	off

Bits 4–5: These bits are not used and must be 0's.

Bit 6 - Transmit Mode: This bit, when set to 1, indicates the attachment is in transmit mode.

Bit 7: This bit is not used and must be a 0.

Bits 8–15 - Secondary Station Address: These bits represent the secondary station address.

Word 4

Bits 0–8: These bits are not used and must be 0's.

Bit 9 - X.21 Switched: When this bit is set to 1, the attachment is jumpered for operation on an X.21 switched network.

Bit 10 - V.35: When this bit is set to 1, the attachment is jumpered for V.35 operation.

Bit 11: This bit is not used and must be 0.

Bit 12 - Local Attach 2: When this bit is set to 1, the attachment is jumpered for local attach 2.

Notes:

1. The attachment provides clocking at 48,000 bps in either SDLC/HDLC or BSC mode.
2. The clocking information is available to the remote terminal through a customer supplied cable.
3. Local attach 1 and local attach 2, when both jumpered, indicates the attachment is operating as a local 2 multipoint master.

4. If a station address is also jumpered on the attachment, the attachment is operating as a local 2 multipoint slave.

Bit 13: This bit is not used and must be a 0.

Bit 14 - IPL: When this bit is set to 1, the allow IPL jumper is installed.

Bit 15 - BSC: When this bit is set to 1, the bisynchronous mode jumper is installed.

Word 5

Bits 0–7 - X.21: These bits represent a BCD coded value equal to the CCITT state representing the X.21 interface conditions. For example: CCITT state 12 (decimal) is encoded as an 8-bit BCD value of 12. If the CCITT state cannot be determined, a hexadecimal 00 is reported. The state indicates the condition resulting from the last command issued.

Note: Bits 8–11 indicate the real time value of the interface lines.

Bit 8 - Transmit: This bit represents the state of the X.21 interface 'transmit' line.

Bit 9 - Receive: This bit represents the state of the X.21 interface 'receive' line.

Bit 10 - Indicate: This bit represents the state of the X.21 interface 'indicate' line.

Bit 11 - Control: This bit represents the state of the X.21 interface 'control' line.

Bits 12–15: These bits represent the binary coded decimal (BCD) value of the DTE timeouts that apply to an X.21 switched connection.

Chapter 6. Binary Synchronous Communication (BSC)

The attachment supports BSC protocol to assist in future migration of the user to SDLC/HDLC protocol.

The BSC capability allows transfer of serial data to and from a remote terminal or host system through a DCE and leased or switched communication line facility. The BSC function can be used for connecting a Series/1 processor to telecommunication equipment or to other processors having compatible adapters. The BSC capability supports the following:

- Data transmission rates up to 56,000 bps.

  Note: Due to post and pre-processing delays in the attachment, the sustained data throughput when running at data transmission speeds of 48,000 and 56,000 bps is considerably less than the clocking rate. Depending on message size, the maximum throughput at 48,000 and 56,000 bps transmission speeds is 15,000 bps.
- Supports EBCDIC or ASCII code.
- May be used as multipoint primary or multipoint secondary station.
- Line error checking is provided for both EBCDIC and ASCII modes of transmission.

BSC can use either Extended Binary-Coded Decimal Interchange Code (EBCDIC) or American Standard Code for Information Interchange (ASCII) transmission codes. The program controls the selection of codes. If the program does not specify ASCII code, the attachment automatically selects EBCDIC code.

For further information on the BSC mode of operation, refer to *General Information - Binary Synchronous Operation*, GA27-3004.

Operating Modes

The attachment has several operating modes that are selected by control characters:

- Text
- Transparent text
- Control
- Selected
- Passive
- IPL
- Transmit
- Receive

Text Mode

Text mode is selected when the first start-of-heading (SOH) or start-of-text (STX) control character is decoded. Subsequent SOH and STX characters are treated as data characters. During text mode, the attachment processes header or text characters and accumulates a block check character (BCC). Synchronization (SYN) characters and the first SOH or STX characters decoded are not included in the BCC accumulation. Text mode is terminated after the attachment decodes an end-of-text (ETX) or end-of-transmission-block (ETB) character.

Transparent Text Mode

Transparent text mode is selected when a data-link-escape (DLE) STX sequence is decoded during a transmit or receive operation. While in this mode, any kind of binary data can be transmitted or received. The following changes from text mode occur:

- The attachment recognizes individual control characters or control sequences, such as end-of-transmission-block (ETB), start-of-text (STX), and enquiry (ENQ), only as data, with no other associated function.
- All inserted synchronization (SYN) characters are preceded automatically by a data-link-escape (DLE) character (DLE-SYN).
- A second DLE is automatically attached to every data DLE to distinguish it as a DLE control character, rather than data. This second DLE and the inserted DLE-SYNs are deleted automatically upon reception and do not enter processor storage.

To exit transparent text mode, use one of the following ending sequences:

- DLE-ETX
- DLE-ETB
- DLE-ITB
- DLE-ENQ

These sequences must be transmitted by using the exit transparent operation. In transparent text mode, the transmitting attachment automatically inserts a second data-link-escape (DLE) between the first DLE and the end-of-text (ETX), end-of-transmission-block (ETB), enquiry (ENQ), or intermediate-transmission-block (ITB). The receiving station discards the first DLE. The inserted DLE and the ETX, ETB, ENQ, or ITB are considered as two data characters and placed in storage. The exit transparent operation prevents the attachment from inserting a second data-link-escape (DLE). The receiving station recognizes the ending sequences as ending sequences, not data. Because the DLEs

in these ending sequences are true DLEs and are not placed in storage at the receiver, they should not be included in the byte count for the receiving station.

Only DLE-ITB leaves the attachment in text mode; all others cause a change of direction (COD).

During transparent text mode, a block-check-character (BCC) is accumulated as in normal text mode. The only DLE characters included in the BCC are the data DLEs.

Control Mode

In a multipoint configuration, when the attachment receives a valid end-of-transmission (EOT) sequence, it enters control mode. While in control mode, the attachment monitors for its station address. If the attachment does not enter selected mode and detects an address sequence other than its own, it resets character synchronization.

Selected Mode

The attachment enters selected mode when it decodes its own station address twice (contiguously) after establishing byte synchronization. If a receive operation has been initiated, the message sequence, starting with the second station address character, transfers to storage.

Notes:

1. The attachment's station-address (used in multipoint configuration only) is determined by discrete jumpers on the feature card.
2. BSC control characters may not be used as an address.
3. EBCDIC bit 2 or the ASCII bit 6 of the station address is not used.
4. The program may use these bits to differentiate between a polling and a selecting sequence.
5. Multipoint address bit 0 must not be jumpered on when using ASCII.

Passive Mode

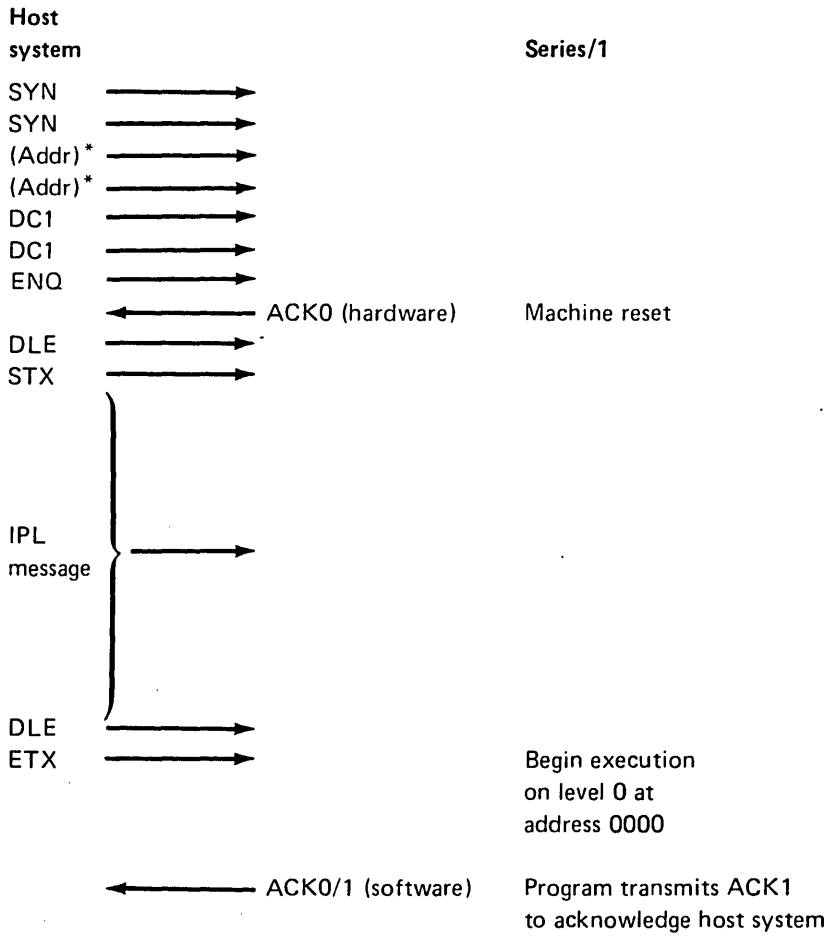
The attachment in a multipoint network is in passive mode when it is not in selected or in control mode. Passive mode is entered when the attachment is powered on. The attachment enters other modes, depending upon the characters received on the line as previously described.

Initial Program Load (IPL) Mode

IPL by a host system may be accomplished through the attachment using EBCDIC characters only. A jumper must be installed on the feature card to allow the attachment to IPL the processor.

If the attachment receives an IPL sequence (DC1-DC1-ENQ), it responds with an EBCDIC even acknowledgment (ACK0) after a 50-millisecond delay.

If the attachment is a multipoint tributary station, its address must be included in the IPL sequence, as shown in the following example. (It must also have been placed in control mode as described earlier.)



*Used only if the attachment is a multipoint tributary.

The host must then transmit DLE-STX (to enter transparent text mode), which is followed by the IPL program. The attachment does not check this sequence (DLE-STX) for validity and does not place it into storage. Instead, the attachment enters transparent text mode and places all succeeding data into storage beginning at location 0000.

Upon receiving a DLE-ETX followed by a valid block-check-character (BCC), the attachment presents a device-end interrupt request, on level 0, with the device address in register 7. The IPL'd program must handle this interrupt request. The program must also transmit a positive acknowlegement back to the host system.

If the IPL operation is unsuccessful, the attachment holds the processor in IPL mode (the Load light is on) and monitors the line for a retry of the IPL operation.

Note: The maximum number of bytes that the host IPL program using the BSC mode can load is 65,535; however, the quality of the transmission line must be considered when transmitting 65,535 bytes.

BSC IPL

When using BSC protocol, an IPL is detected and processed as follows:

1. The attachment monitors for the IPL sequence only if the allow IPL jumper is installed.
2. When the attachment detects an IPL sequence, it responds with an EBCDIC acknowledgement (ACK0).
3. If the attachment is a multipoint tributary station, it must be in selected mode.
4. The originator (host) must first transmit a data-link escape (DLE), then a start of text (STX) sequence, followed by the IPL program.

   Note: The DLE STX sequence is stripped from the loaded IPL program.
5. The received IPL program is placed in processor storage starting at location 0000.
6. At the end of the program, the originator (host) sends a data-link escape (DLE) end of text (ETX) sequence.
7. The IPL is successful if the block check character (BCC) following the DLE ETX sequence is valid.
8. If the attachment detects a block check character (BCC) error, the processor stays in IPL mode while the attachment continues to monitor for an IPL to allow for retries.
9. Following a successful IPL operation, the processor is reset and program execution begins at processor storage location 0000.
10. At this point, the attachment presents a device end interrupt on interrupt level 0.

Switched Line IPL

After detecting an incoming call, the attachment determines if it has been prepared. If prepared, the attachment presents an attention interrupt (CC4) and allows the software to issue an Auto-Answer DCB as in normal operation. If no Auto-Answer is issued within 300 milliseconds, the attachment disregards the call progress signals (CPS) and DCE provided information (DPI) signals passed from the DCE during call establishment. The attachment then monitors for the IPL sequence as explained in the preceding section entitled "Leased Line IPL."

Transmit Mode

The attachment fetches transmission data from storage two characters at a time (except as previously noted). The high-order byte holds the first character to be sent and the low-order byte holds the next character. After a character has been transferred into the serializer/deserializer (SERDES), it is transmitted over the line, low-order bit first.

ASCII characters in storage are eight bits long - seven data bits plus one parity bit. This parity bit should not be confused with the parity bit in storage. The ASCII parity bit is bit 0 in a byte of storage.

The attachment does not check the ASCII parity during transmit operations; therefore, the program must maintain odd parity in storage when transmitting the data.

Programming Consideration

The BSC protocol as implemented has the restriction that the data block size on transmit and receive operations must not exceed 2,000 bytes when the data rate is over 19,200 bps.

Note: Link data transmission speeds over 19,200 bps result in a through-put of approximately 15,000 bps.

Receive Mode

The first bit received is transferred into the low-order bit position of a byte. The second bit received is transferred into the next higher bit position, and so on until a character is assembled. When two characters are to be transferred to storage, the first character received is loaded into the high-order byte of the storage data register and the next character is loaded into the low-order byte before the data is transferred to storage. Data is written into storage without any code translation.

Transmission Codes

The BSC mode allows data communication using EBCDIC or ASCII line codes. The program can specify ASCII after the IPL. The attachment establishes EBCDIC if:

- The program does not specify a code
- A power-on reset occurs
- A system reset occurs

Control Characters

Note: For detailed information about BSC line control, refer to *General Information-Binary Synchronous Communications*, GA27-3004.

Name	Abbr	EBCDIC	ASCII
Start of heading	SOH	SOH	SOH
Start of text	STX	STX	STX
End of transmission block (Note 1)	ETB	ETB	ETB
End of text (Note 1)	ETX	ETX	ETX
End of transmission (Note 1)	EOT	EOT	EOT
Enquiry (Note 1)	ENQ	ENQ	ENQ
Negative acknowledge (Note 1)	NAK	NAK	NAK
Synchronous idle	SYN	SYN	SYN
Data link escape	DLE	DLE	DLE
Intermediate block character	ITB	IUS	US
Initial program load (Notes 2 and 3)	IPL	DC1 DC1 ENQ	
Even acknowledge (Note 1)	ACK0	DLE(70)	DLE 0
Odd acknolwedge	ACK1	DLE/	DLE 1
Wait before transmit-positive acknolwedge (Note 1)	WACK	DLE ,	DLE ;
Mandatory disconnect Note 1)	DISC	DLE EOT	DLE EOT
Reverse interrupt (Note 1)	RVI	DLE @	DLE <
Temporary text delay	TTD	STX ENQ	STX ENQ
Transparent start of text (Note 4)	XSTX	DLE STX	
Transparent intermediate block block (Note 4)	XITB	DLE IUS	
Transparent end of text (Note 4)	XETX	DLE ETX	
Transparent end of transmission block (Note 4)	XETB	DLE ETB	
Transparent synchronous idle (Note 4)	XSYN	DLE SYN	
Transparent block cancel (Note 4)	XENQ	DLE ENQ	
Transparent TTD (Note 4)	XTTD	DLE STX DLE ENQ	
Data DLE in transparent mode (Note 4)	SDLE	DLE DLE	

Notes:

1. These control characters and sequences cause a change-of-direction (COD) interrupt request after the required action has been completed.
2. Not applicable in ASCII format.
3. In general use as IPL sequence.
4. Transparent mode is not available in ASCII.

The functions of the control characters are as follows:

Mnemonic	Function
ACK0	Indicates affirmative acknowlegement of even blocks.
ACK1	Indicates affirmative acknowlegement of odd blocks.
DISC	Used only on switched communication facilities to initiate a disconnect.
DLE	Alert the attachment to test the next character for a defined control sequence in transparent text mode. In text mode, DLE is treated as data.
ENQ	Resets text mode without BCC transmission and comparison.
EOT	End of transmission.
ETB or ETX	Resets text mode with BCC comparison.
IPL	Control characters to initiate an IPL sequence.
ITB	Included in the BCC; it causes the BCC to be sent.
NAK	Negative response to a request for a reply, or to a block of heading or a block of text in error.
RVI	Reverses direction of data transfer.
SOH or STX	Resets control mode and sets the attachment to text mode. BCC accumulation starts with the first character after the first SOH or STX character is transmitted/received.
SYN	Transmitted automatically by the attachment to establish and maintain synchronization.
TTD	Alerts the receiving station of a temporary text delay.
WACK	Indicates a temporary not-ready-to-continue (or not-ready-to-receive) condition.
XDLE	In transparent text mode, the transmitter adds a second DLE after each data DLE. At the receiver, the first DLE is removed and does not enter storage or the BCC.
XENQ	Switches off transparent text mode and cancels the current block of data.
XETX/XETB	Same as ETB or ETX, but turns off transparent text mode.
XITB	Same as ITB, but turns off transparent text mode.
XSTX	Switches off control mode and sets the attachment to transparent text mode.
XSYN	Transmitted automatically by the attachment to establish and maintain synchronization in transparent text mode.
XTTD	Alerts the receiving station to a temporary text delay in transparent text mode.

Note: An X is defined as DLE.

Line Error Checking

Two different types of checking are used, depending on the code selected. Cyclic redundancy check (CRC) is used with EBCDIC and longitudinal redundancy and vertical redundancy checking (LRC/VRC) is used with ASCII.

To correct an error, retransmit the data block in error.

Synchronization And Timing

The attachment receives strobe pulses from the DCE. These pulses establish and maintain bit synchronization. A specific series of characters precedes each transmission to establish character synchronization.

Transmit Synchronization

The attachment automatically begins transmission with a leading pad character (hex 55), followed by the initial synchronizing pattern of two synchronizing (SYN) characters. If using internal clocking, the attachment transmits two leading pad characters.

SYN Insertion

To maintain synchronization, the attachment inserts a synchronization pattern of SYN-SYN at approximately one-second intervals. In transparent text mode, this synchronization pattern is DLE-SYN. These characters are also inserted as time-fill characters when the attachment is not transmitting such as when it is fetching a new DCB during a chaining operation.

SYN Deletion

SYN characters or transparent SYN characters are deleted and not placed in storage.

Trailing Pad Characters

The attachment automatically transmits a trailing pad character (hex FF) after every change-of-direction (COD) character or after the block-check-character (BCC), if the change of direction calls for BCC. This ensures that the last character sent (COD or BCC) goes online in its entirety. A pad of hexadecimal FF also provides the second character of the negative acknowlege (NAK) and end-of-transmission (EOT) control character sequences. The attachment does not begin an interrupt request or chaining operation until the entire pad character is transmitted.

Receive Synchronization

Character phase synchronization is established when two consecutive synchronization (SYN) characters followed by any non-SYN character are received and decoded. Character phase is maintained because the transmit station periodically inserts a synchronization pattern into the data stream.

Time-Outs

The following is a list of the possible time-outs while in the BSC mode of operation:

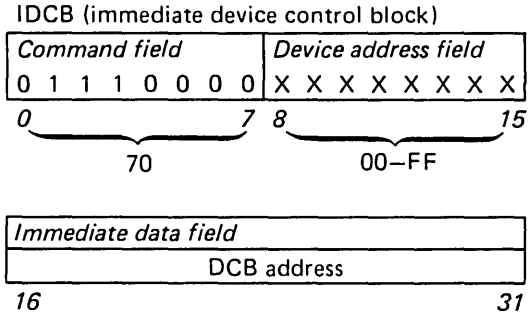
- *Character synchronization time-out.* The period of time the attachment waits for character phase to be established after initiating a receive operation.
- *Continuous synchronization time-out.* A continuous synchronization pattern or transparent synchronization idle (in transparent mode) is received while in character phase.
- *Synchronization loss time-out.* While receiving data, no synchronization pattern or transparent synchronization idle is received.
- *DCE not ready time-out.* Bit 12 of the control word is used to limit the time (maximum of 3 seconds) the attachment waits for DCE ready to become active.
- *Programmable time-out.* Used by the software for timing purposes when the operation specified in the DCB is not transmit, receive, enable, or disable terminal. A 2-second time-out is active.
- *Clear-To-Send (CTS) time-out.* The period of time the attachment allows for the return of 'clear-to-send' (CTS) on a transmit operation. Using the V.35 interface, DCE interface error, cycle-steal status word 1, bit 2, is set to one.

- Start
- Start Cycle-Steal Status

The programmer must ensure that the program always tests the Operate I/O condition codes following an Operate I/O instruction.

Start

The Start command initiates a cycle-steal operation for the addressed device. The format of the IDCB for the Start command is:

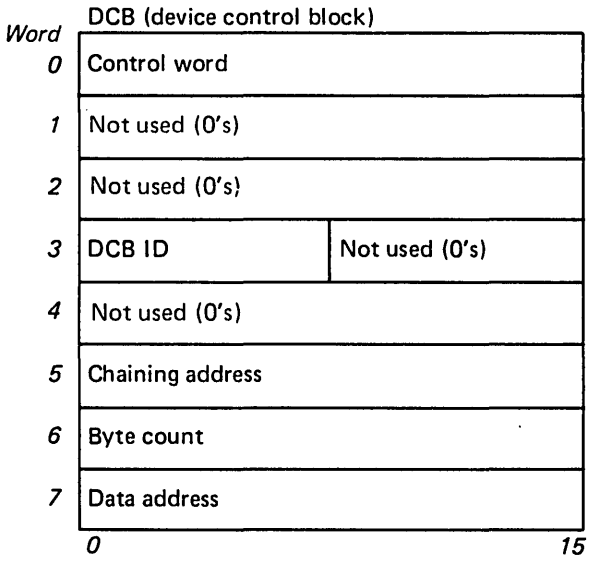


The DCB is an 8-word area in processor storage describing the specific parameters of the cycle-stealing operation. The program assigns its location in storage, and it loads and changes the data. The attachment fetches the data by using a cycle-steal address key of 000 after it completes a successful execution of a Start command.

The DCB address is transferred to the attachment through the IDCB, which points to word 0 of the DCB. The table is in an ascending storage address order with the lowest storage address at the top of the table.

> **Note:** The address of the DCB in processor storage must be even. If the address is odd, the attachment presents an exception interrupt (CC2), with bit 1 (delayed command reject) set in the interrupt status byte and ends the cycle-steal operation.

The format of the BSC DCB is as follows:



Word 0 - Control Word: Control word 0 defines the cycle-stealing operation to be performed. The format of the control word is as follows:

Bit 0 - Chaining Flag: If this bit is set to 1, the next DCB in the chain is fetched after the successful completion of the current DCB operation. If this bit is set to 0 and the operation is successfully completed, the attachment presents a device end interrupt.

> **Note:** In transmit mode at data rates over 19,200 bps, multiple synchronization (SYN) characters are present between data blocks.

Bit 1 - Program Controlled Interrupt (PCI): This bit causes the attachment to present a PCI at the completion of the DCB fetch. The data transfer associated with the DCB may begin even though the PCI may be pending in the attachment. When this bit is set to a 1, bits 0–7 of DCB word 3 are placed in the IIB upon interrupt presentation.

This bit is recognized only during a transmit or receive operation. A DCB specification check (bit 3 of the ISB) is presented if this bit is set on any other command.

To use PCI, a Start Control set mode DCB must have previously been issued with bit 11 set on in word 1. If the set mode was not issued, the attachment does not examine this bit.

Bit 2 - Input Flag: If this bit is set to 1, the attachment can cycle-steal data into processor storage once byte synchronization is established. A device end interrupt is presented when it receives a change of direction (COD).

If the byte count in the DCB is 0, an exception interrupt is presented with bit 3 (DCB specification check) set in the ISB.

In X.21 modes, if the DTE/DCE interface is not ready for a data transfer, an exception interrupt (CC2) occurs with bit 0 (device dependent status available) set in the ISB, and bit 2 (DCE interface error) set in cycle-steal status word 1.

Use this bit with bit 12 to limit the time that the attachment allows to establish character phasing. Failure to establish character phase within 3 seconds results in an exception interrupt with bit 0 (device dependent status available) set in the ISB, and bit 1 (time-out) set in cycle-steal status word 1.

If the attachment is jumpered to operate with the V.35 interface, an exception interrupt occurs with bit 0 (device-dependent status available) set in the ISB, and bit 2 (DCE interface error) set in cycle-steal status word 1, if the 'data set ready' line from the DCE is off.

Bit 3: This bit is not used and must be set to 0.

Bit 4: This bit is not used and must be set to 0.

Bits 5–7 - Cycle-Steal Address Key: These bits represent a 3-bit storage access key the attachment presents during data transfers.

Bit 8: This bit is not used and must be set to 0.

Bit 9 - Set ASCII Mode: This bit sets up the attachment to allow communications using ASCII code. If this bit is set to 0, it causes the attachment to recognize EBCDIC code.

Bit 10 - Enable Terminal: This bit sets the X.21 interface to DTE ready. An interrupt or chaining operation (if so specified by bit 0 of the control word) occurs after DCE ready (CCITT state 1) is detected. Use bit 12 of the control word (start timer) to limit (to 3 seconds) the time that the attachment waits for DCE ready to become active. Failure to receive DCE ready within this time results in an exception interrupt with bit 0 (device dependent status available) set in the ISB and bit 1 (time-out) set in cycle-steal status word 1. If the start timer bit is off, an enable with no time-out occurs.

If the V.35 jumper plug is installed, the attachment checks for 'data set ready' (DSR). Subsequent action taken is as described above for X.21 modes.

Bit 11 - Disable Terminal: This bit (in X.21 leased mode) when set to one causes the DTE to assume the DTE ready (state 1). An interrupt or chaining operation (if so specified by bit 0 of the control word) begins immediately after the DTE ready state is set.

This bit (in X.21 switched mode) when set to one causes the DTE to assume the DTE controlled not ready (state 14). An interrupt or chaining operation (if so specified by bit 0 of the control word) begins immediately after the controlled not ready state is set.

If the V.35 jumper plug is installed, the attachment causes an immediate device end interrupt.

This bit may be used with bits 0–7 of word 1 of the DCB to limit the time the attachment waits for DCE ready to become active. Failure to receive DCE ready within this time results in an exception interrupt being presented with bit 0 (device dependent status available) set in the ISB and bit 4 (time-out) set in cycle-steal status word 2. If timer 1 of the DCB is specified as zero, no time-out occurs. DCE ready must be active before the transition to DTE controlled not ready can be made (state 14).

Note: Disable must not be issued when device 1 is busy.

Bit 12 - Start Timer: Use this bit with bits 2, 10, or 11 to provide a 3-second time-out. In the absence of bits 2, 10, and 11 of the control word, this bit provides a timer for software and a 2-second time-out occurs. The attachment presents a device end interrupt at the completion of this period.

Bit 13 - Transmit:

X.21 Leased

This operation causes the attachment to ensure that the DCE does not indicate DCE not ready. If DCE not ready is *not* active, the attachment activates the control lead for at least 24 bit times before establishing synchronization and cycle-steals data from processor storage.

If DCE not ready is active, an exception interrupt occurs immediately, with bit 0 (device-dependent status available) set in the ISB and bit 2 (DCE interface error) set in cycle-steal status word 1.

When the byte count goes to 0, and a COD character is detected, a device end interrupt is presented.

If the byte count goes to 0, the chaining bit is set to 0, and no COD is sent, an exception interrupt is presented with bit 2 incorrect-length-record (ILR) set in the ISB.

If a COD character is detected before the byte count going to 0, an exception interrupt is presented with bits 0 and 2 (short record) set in the ISB.

If a byte count of 0 is specified in the DCB, an exception interrupt is presented with bit 3 (DCB specification check) set in the ISB.

Note: At data rates over 19,200 bps, an intermediate-block-character (ITB) is not supported unless it occurs on a DCB boundary. For example, the ITB character must be the last byte in the data buffer associated with a transmit DCB.

X.21 Switched

This bit causes the attachment to ensure that the DCE is ready for data (CCITT state 12 - call establishment complete) before attempting to transmit data. If ready for data is present on the interface, the attachment transmits the data associated with the current DCB. If ready for data is not present (CCITT state 12), an exception interrupt (CC2) occurs with bit 0 (device dependent status available) set in the ISB and bit 2 (DCE interface error) set in cycle-steal status word 1.

A device end interrupt (CC3) is presented when the byte count goes to 0, and the attachment transmits a change of direction (COD) character.

An exception interrupt (CC2) is presented if the attachment detects a COD character before the byte count goes to 0. In addition to the exception interrupt (CC2) being presented, bits 0 and 2 (short record) are set in the ISB.

If specifying a byte count of 0 in the DCB, an exception interrupt (CC2) is presented with bit 3 (DCB specification check) set in the ISB.

V.35 Leased

This operation starts a 3-second timer and turns on 'request-to-send' to the DCE. As soon as 'clear-to-send' returns from the DCE, the attachment establishes synchronization and cycle-steals data from processor storage.

An exception interrupt occurs immediately, with bit 0 (device-dependent status available) set on in the ISB and bit 2 (DCE interface error) set in cycle-steal status word 1, if the data set ready line from the DCE is off.

Failure to receive 'clear to send' from the DCE within the 3-second time-out period results in an exception interrupt with bit 0 (device-dependent status available) set in the ISB and bit 2 (DCE interface error) set in cycle-steal status word 1.

Transmit mode is reset and 'request to send' to the DCE is dropped after the pad character is sent following a COD control character or a BCC, if required.

Bit 14 - Exit Transparent: This bit allows transmission of control sequences while in transparent text mode. It should be set to one in the final DCB used for a transmit transparent text operation. The attachment does not transmit a delimiting data-link-escape (DLE), nor does it accumulate the single DLE in the block-check-character (BCC). Bit 14 should only be used in a DCB following a block of transparent text.

When this bit is specified, the byte count must be equal to 2 or a DCB specification check (interrupt status byte, bit 3) is reported.

Bit 15: This bit is not used and must be 0.

Word 1: This word is not used and must be set to 0's.

Word 2: This word is not used and must be set to 0's.

Word 3 - DCB ID: When program-controlled-interrupt (PCI) is specified, bits 0–7 of this word contain the DCB identifier.

Word 4: This word is not used and must be set to 0's.

Word 5 - Chaining Address: The chaining address word contains the storage address of the next DCB used when chaining is specified.

The chaining address must be even. If it is odd, the attachment sets interrupt status byte bit 3 to a 1 and ends the operation.

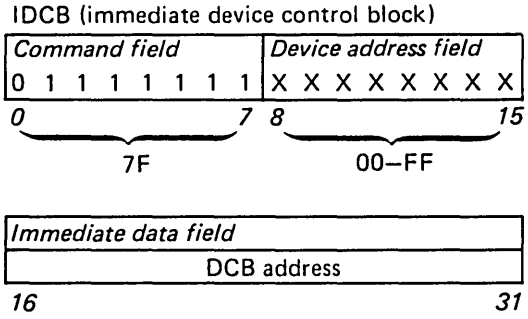
Word 6 - Byte Count: The byte count word contains the number of bytes to be transferred to or from storage.

> **Note:** The BSC protocol as implemented has the restriction that the data block size on transmit and receive operations must not exceed 2,000 bytes when the data rate is over 19,200 bps.

Word 7 - Data Address: The data address is the address in processor storage where data transfer starts.

Start Cycle-Steal Status (SCSS)

The Start Cycle-Steal Status command causes the device to initiate a cycle-steal operation to collect status information about the previous cycle-steal operation. The format of the IDCB for this command is as follows:



The byte count in the DCB (word 6) must be equal to 6 or 10, and the data address (word 7) must be on a word boundary (bit 15 set to 1) or an exception interrupt request (CC2) occurs with DCB specification check (bit 3) set to 1 in the ISB.

Cycle-Steal Status Words

Five words of status information are available by using the Start Cycle-Steal Status (SCSS) command.

Word 0: Word 0 contains the processor storage address of the last attempted cycle-steal data transfer. This residual address may be either a data or DCB address. When reporting a DCB address, the attachment reports the address of the low-order byte of the last DCB word that the attachment attempted to fetch.

Word 1: Word 1 has the following format:

Bit 0 - Overrun: During a receive operation, overrun occurs if the attachment does not read the receive buffer (attachment hardware) within 16-bit times since it was last read.

During a transmit operation, overrun occurs if the transmit buffer is not reloaded within 16-bit times since it was last filled.

Bit 1 - Time-Out: This bit is set to 1 if any of the following conditions exist:

- In X.21 mode, DCE ready is not received from the DCE within 3 seconds after an enable terminal operation begins (if bit 12 of DCB word 0 is set to 1).
- In V.35 mode, 'data-set-ready' (DSR) is not active from the DCE within 3 seconds after an enable terminal operation begins (if bit 12 of DCB word 0 is a 1).
- Character phase is not established within 3 seconds of acceptance of a receive operation (if bit 12 of DCB word 0 is a 1).
- A continuous synchronization pattern is received for 3 seconds.
- While receiving data, no synchronization pattern is received for a period of 3 seconds.

Bit 2 - DCE Interface Error: This bit is set to 1 if any of the following conditions exist:

- The DCE went to DCE not ready during a transmit or receive operation.
- In V.35 mode, 'clear-to-send' (CTS) was not returned from the DCE after setting 'request-to-send' (RTS).

Bit 3 - Block Check Error: This bit is set to 1 if the block check character (BCC) received over the data link does not compare with the BCC accumulated. In ASCII mode, a longitudinal redundancy check (LRC) or vertical redundancy check (VRC) error is indicated.

Data transfer to processor storage ceases upon detection of an ASCII VRC (even parity) error, or in EBCDIC, following a block-check-character (BCC) error after an intermediate-transmission-block (ITB) character.

> **Note:** A 1-second delay occurs before presentation of the error interrupt to reduce the probability of the transmit station passing data if the receive station replys with an immediate negative acknowlegement.

Bit 4 - Multipoint Transmit Error: This bit is set to 1 if a transmit operation was attempted before being selected when the attachment is a tributary on a multipoint network.

Bit 5: This bit is not used and must be set to 0.

Bit 6 - Multipoint Tributary: This bit is set to 1 if the attachment is a multipoint tributary terminal.

Bit 7 - Improper Configuration: When this bit is set to 1, the attachment is configured improperly.

Bits 8–15 - Multipoint Address: These bits contain the address the attachment is jumpered to. The BSC station address (used in multipoint configuration only) is determined by discrete jumpers on the attachment card. Control characters may not be used as an address. The EBCDIC 2-bit or the ASCII 6-bit of the station address is not used by the hardware. The program, however, may use these bits to differentiate between a polling and a selection sequence.

> **Note:** The attachment uses the multipoint address jumpers to indicate multipoint tributary. For example, any jumper set on in the multipoint address field causes the attachment to react as a multipoint tributary. Therefore, hex 00 is an invalid multipoint address.

Word 2

Bit 0 - Data Terminal Ready (DTR): This bit is set to 1 if DTR is active.

Bit 1 - Data Set Ready (DSR): This bit is set to 1 if DSR is active.

Bit 2 - Request To Send (RTS): This bit is a 1 if RTS is active.

Bit 3 - Clear To Send (CTS): This bit is set to 1 if CTS is active.

Note: Bits 0–3 have no meaning on an X.21 network. Therefore, for software compatability, these bits have the following meaning:

Bit		0	1	2	3
SCSS following	Enable normal	on	on	off	off
	Enable error	on	off	off	off
	Disable normal	off	off	off	off
	Disable error	off	off	off	off
	Transmit normal	on	on	on	on
	Transmit error	on	on	on	off
	Receive normal	on	on	off	off
	Receive error	on	off	off	off

Bits 4–5: These bits are not used and must be 0's.

Bit 6 - Transmit Mode: When this bit is set to 1, the attachment is in transmit mode.

Bit 7: This bit is not used and must be 0.

Bits 8–15: These bits indicate the current setting of the communications indicator panel DISPLAY/FUNCTION SELECT switches (if installed); the bits are 0's if the communications indicator panel is not installed.

Word 3

Bits 0–8: These bits are not used and must be 0's.

Bit 9 - X.21 Switched: If this bit is set to 1, it indicates the attachment is jumpered for X.21 operation and is operating in switched mode.

Bit 10 - V.35: If this bit is set to 1, it indicates the attachment is jumpered for V.35 operation.

Bit 11: This bit is not used and must be 0.

Bit 12 - Local Attach 2: If this bit is set to 1, it indicates the attachment is jumpered for local attach 2. The attachment provides clocking at 48,000 bps in either SDLC/HDLC or BSC mode. The clocking information is available to the remote terminal by a customer supplied cable.

Bit 13: This bit is not used and must be 0.

Bit 14 - IPL: If this bit is set to 1, it indicates the allow IPL jumper is installed.

Bit 15 - BSC: If this bit is set to 1, it indicates the bisynchronous mode jumper is installed.

Word 4

Bits 0–7: These bits represent a BCD coded value equal to the CCITT state representing the X.21 interface conditions. For example: CCITT state 12 (decimal) is encoded as an 8 bit BCD value of 12. If the CCITT state can not be determined, a hexadecimal 00 is reported. The reported state indicates the condition resulting from the last command issued.

Note: Bits 8–11 indicate the real time value of the interface lines.

Bit 8 - Transmit: This bit reflects the state of the X.21 interface 'transmit' line.

Bit 9 - Receive: This bit reflects the state of the X.21 interface 'receive' line.

Bit 10 - Indicate: This bit reflects the state of the X.21 interface 'indicate' line.

Bit 11 - Control: This bit reflects the state of the X.21 interface 'control' line.

Bits 12–15: These bits represent the binary coded decimal (BCD) value of the DTE time-outs applicable to an X.21 switched connection.

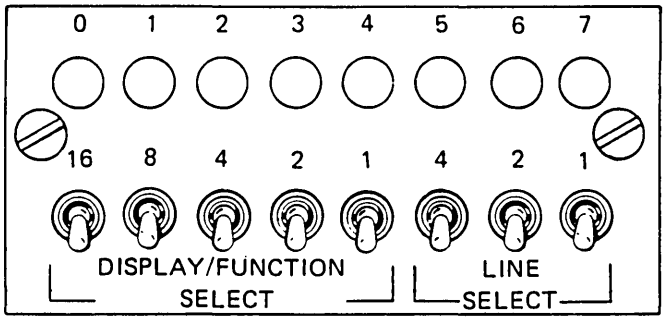
BSC Timer Usage

The following conditions govern the timer use when using BSC protocol:

1. The timers are used with receive (bit 2 of the control word set to 1) and bit 12 of the control word to limit the time the attachment allows to establish character synchronization. The attachment waits 3 seconds for this time-out.
2. The timers are used with enable terminal to specify the DCE ready time-out period. The attachment waits 3 seconds for this time-out.

   Note: In V.35 mode, the attachment waits 3 seconds for 'data set ready' to come active.
3. In the absence of bit 2 and other bits in the device dependent field of the control word, a timer is provided for software. The attachment waits 2 seconds for this time-out.
4. The timers are used with receive to specify the time the attachment allows for a continuous synchronization pattern or transparent sync idle (in transparent mode). The attachment waits 3 seconds for this time-out.
5. Timer 1 is used with the Auto-Answer command to limit the time the attachment waits for an incoming call. If the timeout period is specified as 0, an indefinite time-out is in effect.
6. In transmit mode (V.35 only), the attachment waits 3 seconds for 'clear-to-send' (CTS) to come active after setting 'request-to-send' (RTS).
7. In conjunction with disable terminal, timer 1 is used to specify the time the attachment allows for the DCE to become ready. The time-out period is 3 seconds. If a time time-out occurs, bit 1 (time-out) is set to 1 in cycle-steal status word 1.

Chapter 7. Communications Indicator Panel



LINE SELECT Switches

Line select switches 2 and 4 must be set to 0 (down) for valid indications. Line select switch 1 is used to select either device 0 or device 1.

> **Note:** During X.21 switched operation at 48,000 bps, the panel does not display while an auto-answer DCB is active. During a transmit or receive operation using BSC protocol, the panel does not display.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION SELECT switches determine what information is displayed on the panel. The following is a list of switch settings and the information that is displayed on the panel:

Switch setting						
16	8	4	2	1	Indicator	Display
0	0	0	0	0	0-7	Bits 0-7 of control word
0	0	0	0	1	0-7	Bits 8-15 of control word
0	0	0	1	0	0-7	Timer 1
0	0	0	1	1	0-7	Timer 2
0	0	1	0	0	0-7	Bits 0-7 of PCI ID
0	0	1	0	1	0-7	Bits 0-7 of status address
0	0	1	1	0	0-7	Bits 8-15 of status address
0	0	1	1	1	0-7	Bits 0-7 of chain address
0	1	0	0	0	0-7	Bits 8-15 of chain address
0	1	0	0	1	0-7	Bits 0-7 of byte count
0	1	0	1	0	0-7	Bits 8-15 of byte count
0	1	0	1	1	0-7	Bits 0-7 of data address
0	1	1	0	0	0-7	Bits 8-15 of data address
0	1	1	0	1	0-7	Bits 0-7 of CSSW-0
0	1	1	1	0	0-7	Bits 8-15 of CSSW-0
0	1	1	1	1	0-7	Bits 0-7 of CSSW-1
1	0	0	0	0	0-7	Bits 8-15 of CSSW-1
1	0	0	0	1	0-7	Bits 0-7 of CSSW-2
1	0	0	1	0	0-7	Bits 8-15 of CSSW-2
1	0	0	1	1	0-7	Bits 0-7 of CSSW-3
1	0	1	0	0	0-7	Bits 8-15 of CSSW-3
1	0	1	0	1	0-7	Bits 0-7 of CSSW-4
1	0	1	1	0	0-7	Bits 8-15 of CSSW-4
1	0	1	1	1	0-7	Bits 0-7 of CSSW-5 (SDLC)
1	1	0	0	0	0-7	Bits 8-15 of CSSW-5 (SDLC)
1	1	0	0	1	0-7	Bits 0-7 X.21 interface state
1	1	0	1	0	0-1	Device 0/device 1 busy flags
					2-4	Not used
					5-7	Interrupt condition code
1	1	0	1	1	0-7	Secondary or MP address
1	1	1	0	0	0-7	Lamp test
1	1	1	0	1	0-7	Interrupt status byte
1	1	1	1	0	0-3	X.21 interface status (TRIC)
					4-7	V.35 interface status (DTR/DSR/RTS/CTS)
					5-7	Interrupt condition code
1	1	1	1	1	0-2	Not used
					3-7	Set mode DCB word 1 bits 11-15

Chapter 8. Error Recovery

Error recovery for the Synchronous Communications Single Line Control is as follows:

1. Inspect the Operate I/O condition code and use the following chart:

Command	Operate I/O CC	Recommended action
Read ID, Prepare	0	Terminate (device not attached).
	1,2,4,6	Terminate (hardware error).
	3	Examine the IDCB function modifier; terminate if IDCB is correct.
	5	Retry three times; terminate if the problem persists.
	7	Satisfactory
Halt I/O	0,1,2,3,4,5,6	Terminate (equipment error).
	7	Satisfactory
Device Reset	0	Terminate (device not attached).
	1,2,4,5,6	Terminate (equipment error).
	3	Examine IDCB function modifier; terminate if the IDCB is correct.
	7	Satisfactory
Start, Start Cycle-Steal Status, Start Diag 1, Start Diag 2, Start Mod, and Start Control	0	Terminate (device not attached).
	1	Retry after device end if the device is busy or device reset, retry; if trouble persists, terminate.
	2	Terminate
	3	Examine the IDCB function modifiers; terminate if the IDCB is correct.
	4	Terminate
	5	Retry three times; terminate if the problem persists.
	6	Retry after controller and interrupt.
	7	Satisfactory

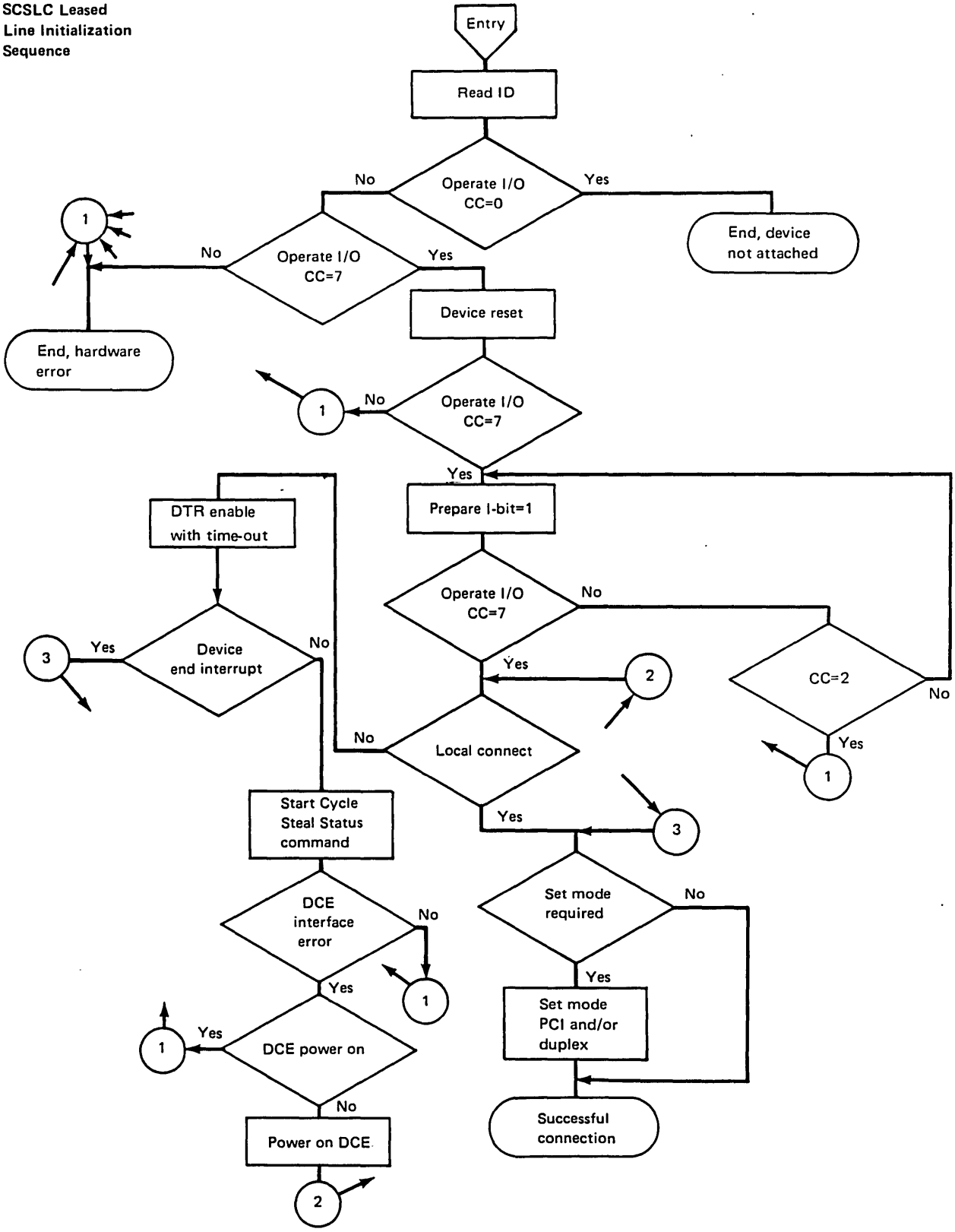
2. Inspect the interrupt condition code.

- If the interrupt condition code is 3, terminate.
- If the interrupt condition code is 2 or 4, use the following chart.

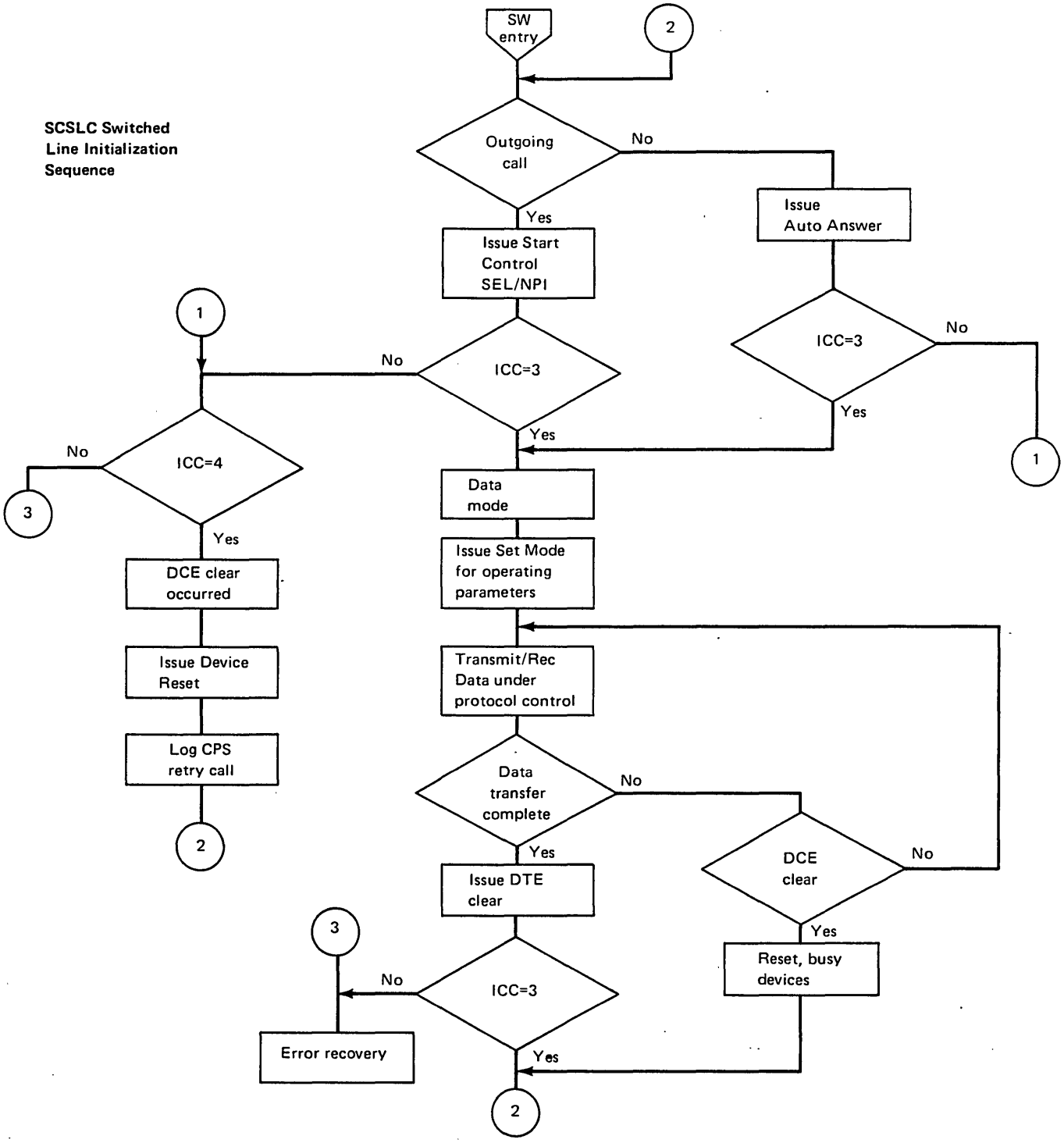
CC	Interrupt status byte (hex)	Recommended action
2	A0	Normal ending operation to the receive DCB if a COD was detected prior to decrementing the byte count to 0. Perform a Start Cycle Steal Status command to obtain residual address and ensure that status word 1 is 0. Not reported in SDLC/HDLC data transfer mode.
2	80	Issue a Start Cycle Steal Status command; examine bits for determination of further action.
2	40	Examine IDCB for valid function modifier or odd DCB address; correct error condition and retry.
2	20	Occurs during a receive operation and indicates that the byte count decremented to 0 and no COD character was detected. Increases the receive data buffer size and byte count and retry. Not reported in SDLC/HDLC data transfer mode.
2	10	Indicates the attachment has detected an invalid situation in the DCB.
2	08	Storage data check; retry operation; if error persists, terminate.
2	04	Invalid storage address; correct program and retry.
2	02	Protect check; varify the protect key and retry. This error can occur only on processors with storage protect feature.
2	01	Interface data check; retry the operation three times; terminate if error persists.
4	80	Indicates the attachment has detected a DCE clear state on the interface and the clear operation terminated in a successful completion.
4	01	Indicates the attachment has detected a DCE clear state on the interface and the clear operation terminated unsuccessfully.
4	00	Indicates the attachment has detected an incoming call on a X.21 switched network.

Appendix A. Attachment Initialization

SCSLC Leased Line Initialization Sequence



SCSLC Switched Line Initialization Sequence



Appendix B. Communications Operator's Self-Test Procedure

The communication adapters operator self-test program needs a minimum system configuration of a Series/1 processor with 16K storage, a diskette drive feature 4964 or 4962 model 2, a programmer console feature 5650, and one communication adapter feature 2080.

1. Remove power, disconnect the DCE cable at the DCE and connect the wrap connector at the DCE end of the cable, as follows:

DCE cable part number	Wrap connector part number
1632206	1633812*
6844126	6844140*

   * If DCE wrap is available, place switch in wrap position.

2. Insert the basic diskette (diskette must be configured to match the self-test configuration).
3. Press the load button on the programmer console.
4. If the system has only a programmer console go to step 11.
5. Wait for the input/output device (as configured in the diagnostic diskette) to print the following message:

   RDY

   ENTER

6. Begin the operator self-test program by entering B3CEF on the input/output device.
7. The output device then prints:

   ENTER DEVICE ADDRESS AND LOOP COUNT

   ENTER

8. Enter FDAXX (where DA=device address and XX=loop count in hexadecimal).

   Example

   F1801 (DA=18, loop count=01).

9. Wait for one of the following messages to appear; then take the appropriate operator action:

Message:

DEVICE ADDRESS ERROR

REENTER DEVICE ADDRESS AND LOOP COUNT

ENTER

Operator Action:

Verify that the device address is correct and call the service organization or return to step 8.

Message:

TEST WAS SUCCESSFUL

Operator Action:

None, self explanatory

Message:

THE TEST FAILED, CALL THE SERVICE ORGANIZATION

Operator Action:

Verify that the cable and wrap connector have the correct part numbers and call the service organization or return to step 8.

After the loop count has been exhausted, the program returns to step 8. At this time, you may run the test again or end the program by returning the system to the operating state.

(Steps 10 through 16 of this procedure are only for systems with a programmer console.)

Note: The running time for the 2080 feature for each pass is 2 seconds.

10. Wait for a hexadecimal 3800 to appear in the lights of the programmer console.
11. Press the Data Buffer key and enter 000B; then press the Console Interrupt key. Press the Data Buffer key again and enter 3CEF. Next press the Console Interrupt key twice.
12. Wait for 3CE1 to appear in the lights of the programmer console.
13. Press Data Buffer key and enter 001F; then press the Console Interrupt key.
14. Press the Data Buffer key and enter DAXX (where DA=device address and XX=loop count). Press the Console Interrupt key twice.
15. Wait for one of the following values to appear in the lights of the programmer console:

Value in lights	Operator action
3CE2	Verify the address is correct and call the service organization or go to step 11.
3CE3	Self-explanatory (test successful)
3CE4	Verify that the cable and wrap connector has the correct part numbers and call the service organization or return to step 11.

16. Press the Data Buffer key, enter 0006 and press the Console Interrupt key twice. Wait for the lights to indicate 3CE1. Proceed to step 13 to run the test again, or return the system to the operating state.

Appendix C. CCITT State Conditions

The following table illustrates the CCITT state conditions that the attachment responds to. It also shows the condition of the X.21 lines for each of the states.

State Nr.	Name	T	C	R	I
1	Ready	1	Off	1	Off
2	Call request	0	On	1	Off
3	Proceed to select	0	On	+	Off
4	Selection signal	IA5	On	+	Off
5	DTE waiting	1	On	+	Off
6	DCE waiting	1	On	SYN	Off
7	Call progress signal	1	On	IA5	Off
8	Incoming call	1	Off	BEL	Off
9	Call accepted	1	On	BEL	Off
10*	DCE provided information	1	On	IA5	Off
11*	Connection in progress	1	On	1	Off
12	Ready for data	1	On	1	On
13	Data transfer	D	On	D	On
14	DTE controlled not ready DCE ready	0/1	Off	1	Off
15	Call collison	0	On	BEL	Off
16**	DTE clear request	0	Off	X	X
17*	DCE clear confirmation	0	Off	0	Off
18	DTE ready DCE not ready	1	Off	0	Off
19**	DCE clear indication	X	X	0	Off
20	DTE clear confirmation	0	Off	0	Off
21	DCE ready	0	Off	1	Off
22***	DTE uncontrolled not ready DCE not ready	0	Off	0	Off
23	DTE controlled not ready DCE not ready	0/1	Off	0	Off
24***	DTE uncontrolled not ready DCE ready	0	Off	1	Off

X.21 Interface Lines
- T = Transmit
- C = Control
- R = Receive
- I = Indicate

*State 10 is not displayed during outgoing calls since the attachment does not examine the network provided information (NPI). No distinction can be made between state 7 and 10. The attachment does not monitor or report state 11 or 17.

**DCE clear indication or DTE clear request may be entered from any state except ready (CCITT state 1).

***State 22 and 24 are not displayed by the communications indicator panel since DTE uncontrolled not ready is not supported by the attachment.

Glossary

The following is a list of terms that appear in the body of this document and their respective meanings.

ACK0: Even acknowledge

ACK1: Odd acknowledge

ASCII: American Standard Code for Information Interchange

BCC: Block Check Character

bps: Bits-per-second

BSC: Bisynchronous Communications

C-Field: Control field

CC: Condition Codes

CCITT: Consultative Comittee for International Telephone and Telegraph

CCITT State #: State condition as defined in the CCITT X.21 specification and in Chapter 2 "CCITT State Conditions."

CHN: Chaining flag

COD: Change of direction

CPS: Call progress signals

CRC: Cyclic redundancy check

CTS: Clear-to-send

DCB: Device control block

DCE: Data circuit terminating equipment

DLE: Data-link-escape

DPI: DCE provided information

DSR: Data set ready

DTE: Data terminal equipment

DTR: Data terminal ready

Duplex: Full duplex bi-directional communication with transmit and receive data occurring simultaneously.

EBCDIC: Extended Binary-Coded Decimal Interchange Code

EIA: Electronic Industries Association

ENQ: Enquiry

EOC: End of chaining operation

EOT: End of transmission

ETB: End of transmission block

ETX: End-of-text

FCS: Frame check sequence

Half-duplex: Bi-directional communication with transmit and receive data occurring alternately.

HDLC: High-Level Data Link Control

hex: Hexadecimal (base 16)

HLA: Hold-line-active

I-bit: Interrupt bit, used to ascertain interrupt can be requested

IA5: International alphabet #5 (similar to USASCII)

IDCB: Immediate device control block

I-field: Information field

IF: Input flag

I/F: Input flag

IIB: Interrupt information byte

ILR: Incorrect length record

I/O: Input/Output

IPL: Initial program load

ITB: Intermediate transmission block

ISB: Interrupt status byte

KEY: A 3-bit key that the attachment presents to the processor during data transfers to verify that the program has authorization to access processor storage

LAP: Link access procedure

LAPB: Link access procedure, balanced mode

Leased lines: Dedicated lines that are used to interface 2 or more DCEs

LRC: Longitudinal redundancy check

NAK: Negative acknowledgement

NE: No exception

NPI: Network provided information

Nr: Count of received frames

NRZ: Non-return-to-zero

NRZI: Non-return-to-zero-inverted

Ns: Count of transmitted frames

PCI: Program controlled interrupt

P/F: Poll final bit

RNR: Receive-not-ready

ROS: Read-only-storage

RS–422A: EIA interface specification

RSB: Residual status block

RTS: Request-to-send

SCSLC: Synchronous Communication Single-Line Control attachment

SCSS: Start Cycle-Steal Status command

SDLC: Synchronous Data Link Control

SE: Suppress exception

SERDES: Serializer/deserializer, attachment logic that converts data from serial to parallel and vice-versa

SIM: Set initialization mode

SOH: Start of header

STX: Start-of-text

Switched lines: Lines terminating in local and/or distant telephone switching exchange. Used to interface DCTs with DCE and switched X.21 network

SYN: Synchronization character

T#: CCITT timeout period (refer to CCITT X.21 specification)

V.35: CCITT interfacing specification

VRC: Vertical redundancy check

X.21: CCITT network specification

X.25: CCITT packet switching recommendation

Index

T

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IBM Series/1 Synchronous Communication Single-Line
Control Attachment Feature Description
Order No. GA34-0241-0

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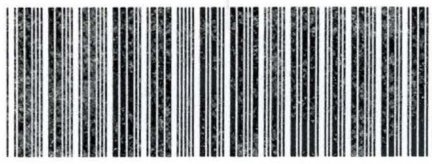

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