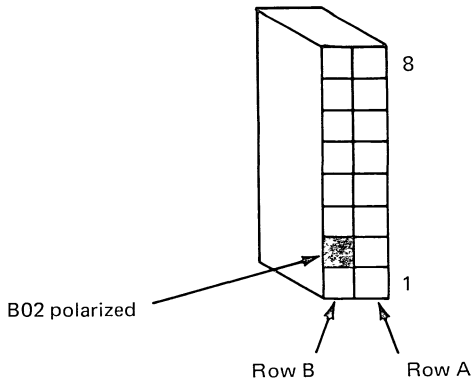
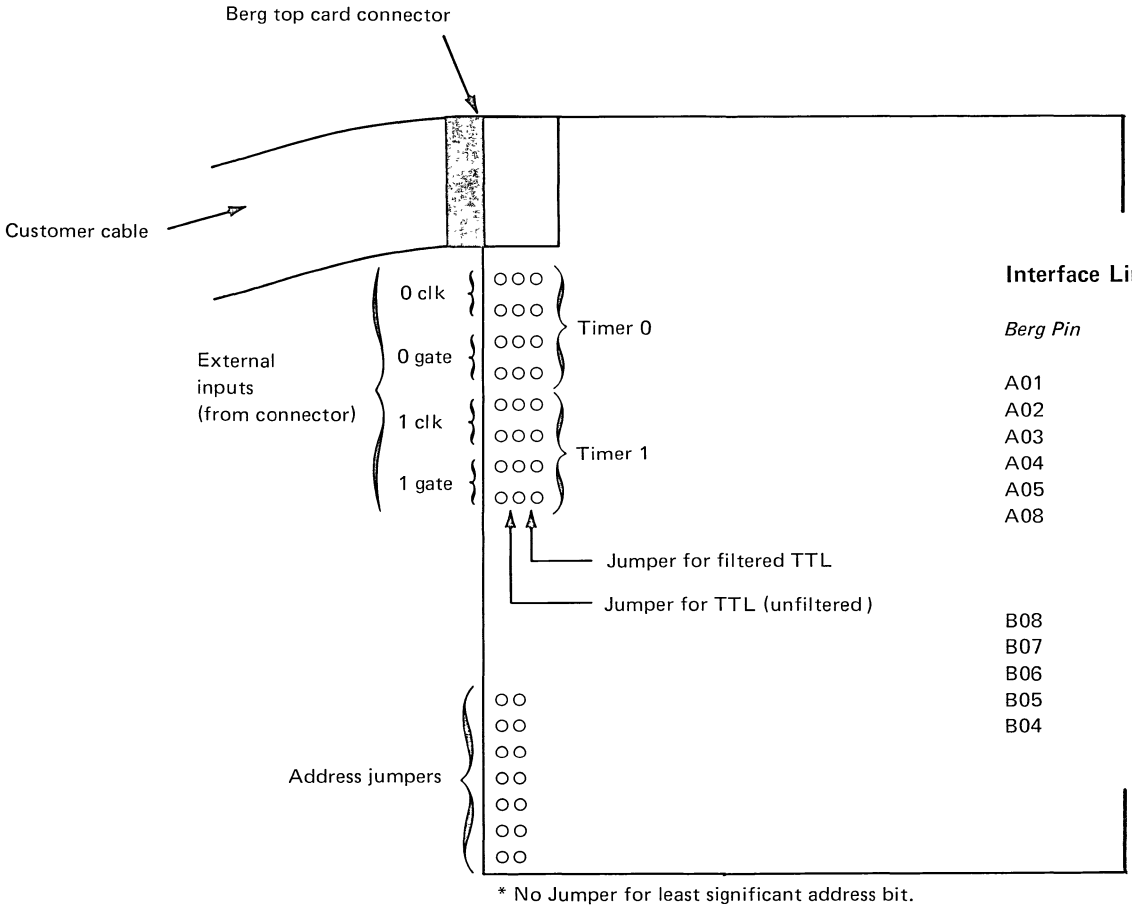
STATUS AFTER RESETS

Condition	*Reset*					
	Timer	*Auto-load reg*	*Prepare reg*	*Mode reg*	*Pending interrupts*	*Timer run state*
Power on reset	X (to all 1's)	X (to all 1's)	X	X	X	X
System reset			X	X	X	X
Halt I/O				X	X	X
Device reset				Y	Y	Y

X = reset in both timers
Y = reset in address timer only



Wiring view
berg connector



* No Jumper for least significant address bit.

Interface Lines on Customer Cable

Berg Pin	*Timer 0*	
A01	Customer clock	To timers
A02	External gate	To timers
A03	Run state	From timers
A04	External gate enabled	From timers
A05	Signal ground	
A08	Frame ground strap	To frame
	Timer 1	
B08	Customer clock	To timers
B07	External gate	To timers
B06	Run state	From timers
B05	External gate enabled	From timers
B04	Signal ground	

One device address for both timers (device address must be even).
Bit 15 of address bus selects one of the two timers.

Sequence		Part	EC 374831				
1050AA	1 of 2	6826706	7-1-78				

Sequence		Part	EC 374831				
1050AA	2 of 2	6826706	7-1-78				

TIMERS CARD DATA FLOW