

4963 DISK ATTACHMENT CARD

STANDARD CHANNEL

4963 TOP CARD CONNECTORS

ADDRESS BUS BIT--00-----B02  
 ADDRESS BUS BIT--01-----B03  
 ADDRESS BUS BIT--02-----B04  
 ADDRESS BUS BIT--03-----B05  
 ADDRESS BUS BIT--04-----B07  
 ADDRESS BUS BIT--05-----B08  
 ADDRESS BUS BIT--06-----B09  
 ADDRESS BUS BIT--07-----B10  
 ADDRESS BUS BIT--08-----B12  
 ADDRESS BUS BIT--09-----D02  
 ADDRESS BUS BIT--10-----D04  
 ADDRESS BUS BIT--11-----D05  
 ADDRESS BUS BIT--12-----D06  
 ADDRESS BUS BIT--13-----D07  
 ADDRESS BUS BIT--14-----D09  
 ADDRESS BUS BIT--15-----D10  
 ADDRESS BUS BIT--16-----D11  
 ADDRESS GATE-----M08  
 ADDRESS GATE RETURN-----M09  
 # BURST RETURN----- (P04)  
 CONDITION CODE IN BIT-00-D12  
 CONDITION CODE IN BIT-01-D13  
 CONDITION CODE IN BIT-02-B13  
 # CYCLE BYTE INDICATOR----- (P10)  
 CYCLE INPUT INDICATOR-----P09  
 CYCLE STEAL REQUEST IN-----M02  
 DATA BUS BIT-----00-----G02  
 DATA BUS BIT-----01-----G03  
 DATA BUS BIT-----02-----G04  
 DATA BUS BIT-----03-----G05  
 DATA BUS BIT-----04-----G07  
 DATA BUS BIT-----05-----G08  
 DATA BUS BIT-----06-----G09  
 DATA BUS BIT-----07-----G10  
 DATA BUS BIT-----P0-----G12  
 DATA BUS BIT-----08-----J02  
 DATA BUS BIT-----09-----J04  
 DATA BUS BIT-----10-----J05  
 DATA BUS BIT-----11-----J06  
 DATA BUS BIT-----12-----J07  
 DATA BUS BIT-----13-----J09  
 DATA BUS BIT-----14-----J10  
 DATA BUS BIT-----15-----J11  
 DATA BUS BIT-----P1-----J12  
 DATA STROBE-----M10  
 HALT OR MCK-----M07  
 INITIATE IPL-----P07  
 IPL-----S04  
 POLL-----M12  
 POLL IDENTIFIER BIT--00--P11  
 POLL IDENTIFIER BIT--01--S02  
 POLL IDENTIFIER BIT--02--S03  
 POLL IDENTIFIER BIT--03--P12  
 POLL IDENTIFIER BIT--04--P13  
 POLL PRIME-----M13  
 POLL PROPAGATE-----M11  
 POLL RETURN-----M04  
 POWER ON RESET-----S05  
 REQUEST IN BUS BIT--00--S07  
 REQUEST IN BUS BIT--01--S08  
 REQUEST IN BUS BIT--02--S09  
 REQUEST IN BUS BIT--03--S10  
 REQUEST IN BUS BIT--04--S12  
 REQUEST IN BUS BIT--05--S13  
 REQUEST IN BUS BIT--06--U02  
 REQUEST IN BUS BIT--07--U04  
 REQUEST IN BUS BIT--08--U05  
 REQUEST IN BUS BIT--09--U06  
 REQUEST IN BUS BIT--10--U07  
 REQUEST IN BUS BIT--11--U09  
 REQUEST IN BUS BIT--12--U10  
 REQUEST IN BUS BIT--13--U11  
 REQUEST IN BUS BIT--14--U12  
 REQUEST IN BUS BIT--15--U13  
 SERVICE GATE-----P05  
 SERVICE GATE RETURN-----P06  
 STATUS BUS BIT-----00--J13  
 STATUS BUS BIT-----01--G13  
 STATUS BUS BIT-----02--M03  
 STATUS BUS BIT-----03--P02  
 SYSTEM RESET-----M05

W22-- -FILE DATA BUS BIT 00  
 W23-- -FILE DATA BUS BIT 01  
 W24-- -FILE DATA BUS BIT 02  
 W25-- -FILE DATA BUS BIT 03  
 W26-- -FILE DATA BUS BIT 04  
 W28-- -FILE DATA BUS BIT 05  
 W29-- -FILE DATA BUS BIT 06  
 W30-- -FILE DATA BUS BIT 07  
 W31-- -FILE DATA BUS BIT P0  
 W03-- -FILE DATA BUS BIT 08  
 W04-- -FILE DATA BUS BIT 09  
 W05-- -FILE DATA BUS BIT 10  
 W06-- -FILE DATA BUS BIT 11  
 W07-- -FILE DATA BUS BIT 12  
 W09-- -FILE DATA BUS BIT 13  
 W10-- -FILE DATA BUS BIT 14  
 W11-- -FILE DATA BUS BIT 15  
 W12-- -FILE DATA BUS BIT P1  
 X31-- -INTRFC PAR CHECK  
 X03-- -FILE TAG 0  
 X04-- -FILE TAG 1  
 X05-- -FILE TAG 2  
 X06-- -FILE TAG 3  
 X12-- -FILE TAG P  
 X25-- -AKN REQ OUT  
 X28-- -STROBE IN  
 X29-- -REQUEST IN  
 X13-- -PARAKEET POR  
 X23-- -SYSTEM RESET  
 X24-- -REQUEST OUT  
 X26-- -STROBE OUT  
 X30-- -AKN REQ IN PWRD  
 X32-- -SYSTEM PWR ON RST  
 X07-- -FILE TAG 4  
 X09-- -FILE TAG 5  
 X10-- -FILE TAG 6  
 X11-- -FILE TAG 7  
 W02-- GND  
 W08-- GND  
 W27-- GND  
 W33-- GND  
 X02-- GND  
 X08-- GND  
 X27-- GND  
 X33-- GND  
 W32-- NOT USED  
 # W13-- -IPL  
 # X22-- -BURST MODE

TOP CARD CONNECTORS

22	W	02
33		13
22	X	02
33		13

CABLE LOCATIONS

VOLTAGE PIN ASSIGNMENTS  
 +5V---D03---J03---P03---U03  
 GND---D08---J08---P08---U08  
 -5V---G06  
 +8.5V---G11

# LINES ARE NOT USED BY THIS ATTACHMENT.

SEE 4963 THEORY DIAGRAMS  
 MANUAL FOR DATA FLOW

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4963 ATTACHMENT CARD  
 E.C. HISTORY MACH.  
 08-17-78 374947  
 SERIES 1  
 IBM CORP. GSD  
 DATE LAST E.C.  
 01-15-79 375147 P.N. 6837768

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0

0 0 0

4963 DISK ATTACHMENT CABLE

ATTACHMENT CABLES  
PIN ASSIGNMENTS

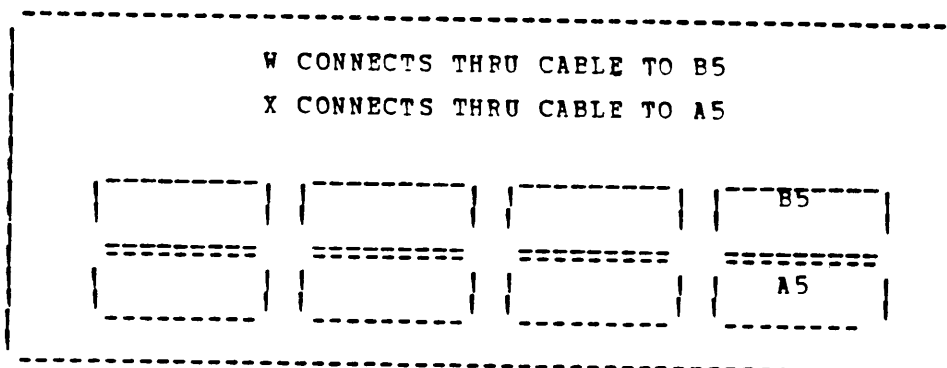
DUC BOARD (A2)  
PIN ASSIGNMENTS

W22--	-FILE DATA BUS BIT 00	--	B5B02
W23--	-FILE DATA BUS BIT 01	--	B5B03
W24--	-FILE DATA BUS BIT 02	--	B5B04
W25--	-FILE DATA BUS BIT 03	--	B5B05
W26--	-FILE DATA BUS BIT 04	--	B5B06
W28--	-FILE DATA BUS BIT 05	--	B5B08
W29--	-FILE DATA BUS BIT 06	--	B5B09
W30--	-FILE DATA BUS BIT 07	--	B5B10
W31--	-FILE DATA BUS BIT 08	--	B5B11
W03--	-FILE DATA BUS BIT 08	--	B5D03
W04--	-FILE DATA BUS BIT 09	--	B5D04
W05--	-FILE DATA BUS BIT 10	--	B5D05
W06--	-FILE DATA BUS BIT 11	--	B5D06
W07--	-FILE DATA BUS BIT 12	--	B5D07
W09--	-FILE DATA BUS BIT 13	--	B5D09
W10--	-FILE DATA BUS BIT 14	--	B5D10
W11--	-FILE DATA BUS BIT 15	--	B5D11
W12--	-FILE DATA BUS BIT P1	--	B5D12
X31--	-INTRFC PARITY CHECK	--	A5B11
X03--	-FILE TAG 0	--	A5D03
X04--	-FILE TAG 1	--	A5D04
X05--	-FILE TAG 2	--	A5D05
X06--	-FILE TAG 3	--	A5D06
X12--	-FILE TAG P	--	A5D12
X25--	-AKN REQ OUT	--	A5B05
X28--	-STROBE IN	--	A5B08
X29--	-REQUEST IN	--	A5B09
X13--	-PAPAKEET POP	--	A5D13
X23--	-SYSTEM RESET	--	A5B03
X24--	-REQUEST OUT	--	A5B04
X26--	-STROBE OUT	--	A5B06
X30--	-AKN REQ IN PWRD	--	A5B10
X32--	-SYSTEM PWR ON RST	--	A5B12
X07--	-FILE TAG 4	--	A5D07
X09--	-FILE TAG 5	--	A5D09
X10--	-FILE TAG 6	--	A5D10
X11--	-FILE TAG 7	--	A5D11
W02--	GND	--	B5D02
W08--	GND	--	B5D08
W27--	GND	--	B5B07
W33--	GND	--	B5B13
X02--	GND	--	A5D02
X08--	GND	--	A5D08
X27--	GND	--	A5B07
X33--	GND	--	A5B13
W32--	NOT USED	--	A5B12
* W13--	-IPL	--	B5D13
* X22--	-BURST MODE	--	A5B02

PROCESSOR ATTACHMENT  
TOP CARD CONNECTORS

22	W	02
33		13
22	X	02
33		13

CABLE LOCATIONS



DUC BOARD (A2) (CARD SIDE VIEW)

\* LINES ARE NOT USED

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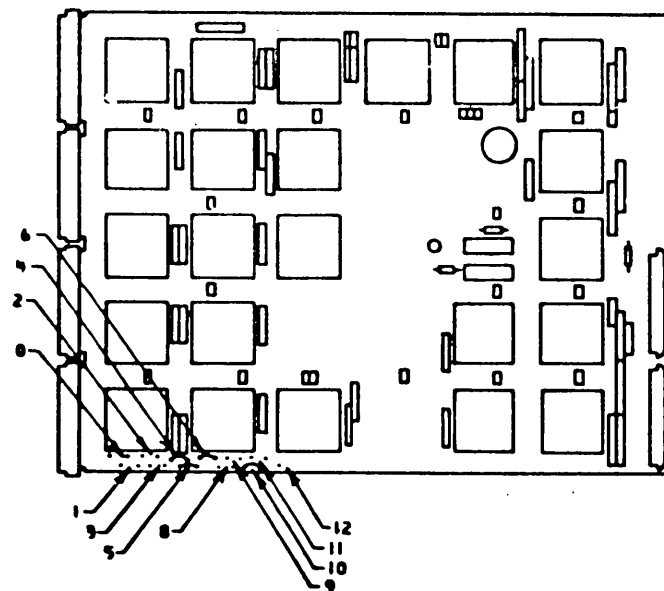
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SHSCT

0 0 0

SF502



**CHART A**

DEVICES COUNT				
	1 DEVICE CONNECTOR	2 DEVICE CONNECTOR	3 DEVICE CONNECTOR	4 DEVICE CONNECTOR
JUMPER 11	X	X	X	
JUMPER 12	X	X		

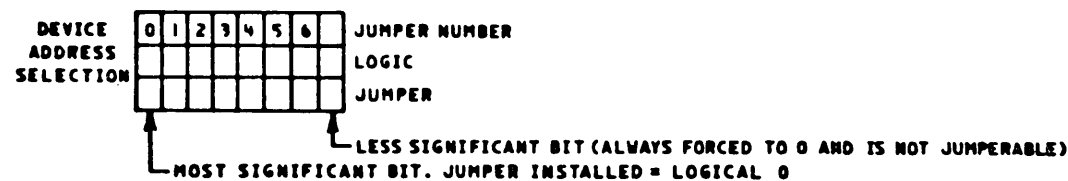
\* MEANS JUMPER INSTALLED DEVICE I.D. WILL BE SET  
AUTOMATICALLY DEPENDING ON THE NUMBER OF FILES  
CONNECTED:  
UP TO 2 FILES - DEVICE I.D. = 3106  
3 OR 4 FILES - DEVICE I.D. = 3206

**CHART D**

IPL SELECTION			
	JUMPER 8	JUMPER 9	JUMPER 10
IPL NOT SUPPORTED			
FILE 0 PRIMARY			X
FILE 1 PRIMARY	X		X
FILE 0 SECONDARY	X	X	
FILE 1 SECONDARY		X	X
FILE 0 PRIMARY AND FILE 1 SECONDARY	X	X	X
FILE 1 PRIMARY AND FILE 0 SECONDARY	X	X	X

\* MEANS JUMPER INSTALLED

JUMPER P/N 4410751, QTY MAX 12



**NOTES:**

- 1 THE BASE ADDRESS IS ALWAYS DIVISIBLE BY 2. IF MORE THAN 2 FILES ARE CONNECTED THE BASE ADDRESS MUST BE DIVISIBLE BY 4
- 2
- 3 CARD JUMPERS AS SHOWN  
 BASE ADDRESS = F0 = 1111 0000  
 IPL = FILE 0 PRIMARY  
 DEVICE ID = 3206 = 0011 0010 0000 0110  
 CONFIGURATION ENTRIES FOR OPTIONS AS SHOWN  
 -F07A 0000 0000 0000 0000 0000 3206  
 -F17A 0000 0000 0000 0000 0000 3206  
 -F27A 0000 0000 0000 0000 0000 3206  
 -F37A 0000 0000 0000 0000 0000 3206

NOTES

EC HISTORY		DRAWING TITLE	
31 AUG 78	374947	CARD JUMPERS	
2 FEB 79	375351	MACH 4963 ATTACHMENT	
		PART NO 6897770	
<b>C</b>	CLASSIFICATION		<b>IBM</b> CORP

NOTES

4963 DEDICATED CABLES (TO FILE 0 & FILE 1)

DUC BOARD (A2)  
PIN ASSIGNMENTS

B3B03-- -CNTRL SAMPLE FILE 0  
 B3B04-- -DU INTRPT FILE 0  
 B3B05-- -SECTOR 0  
 B3B08-- +NRZ DATA 0  
 B3B09-- -MISSING SECTOR 0  
 B3B10-- -WRITE DATA 0  
 B3B12-- +INTRFC DEGATE FILE 0  
 B3D03-- +WRITE GATE RTN 0  
 B3D04-- -DATA SELECT 0  
 B3D05-- -FAST SYNC 0  
 B3D06-- -RESET ERROR FILE 0  
 B3D07-- -INDEX 0  
 B3D09-- -READ 0  
 B3D10-- +READ CLOCK 0  
 B3D11-- -WRITE 0  
 B3D12-- +WRITE CLOCK 0  
 B3B02-- -CABLE CONTINUITY OUT  
 B3D13-- -CABLE CONTINUITY IN  
 B3B07-- GND  
 B3B13-- GND  
 B3D02-- GND  
 B3D08-- GND

FILE 0 BOARD (A1)  
PIN ASSIGNMENTS

-- A5B03  
 -- A5B04  
 -- A5B05  
 -- A5B08  
 -- A5B09  
 -- A5B10  
 -- A5B12  
 -- A5D03  
 -- A5D04  
 -- A5D05  
 -- A5D06  
 -- A5D07  
 -- A5D09  
 -- A5D10  
 -- A5D11  
 -- A5D12  
 -- A5B02  
 -- A5D13  
 -- A5B07  
 -- A5B13  
 -- A5D02  
 -- A5D08

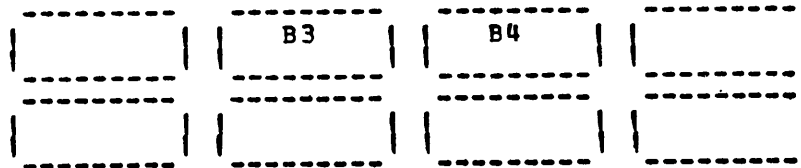
DUC BOARD (A2)  
PIN ASSIGNMENTS

B4B03-- -CNTRL SAMPLE FILE 1  
 B4B04-- -DU INTRPT FILE 1  
 B4B05-- -SECTOR 1  
 B4B08-- +NRZ DATA 1  
 B4B09-- -MISSING SECTOR 1  
 B4B10-- -WRITE DATA 1  
 B4B12-- +INTRFC DEGATE FILE 1  
 B4D03-- +WRITE GATE RTN 1  
 B4D04-- -DATA SELECT 1  
 B4D05-- -FAST SYNC 1  
 B4D06-- -RESET ERROR FILE 1  
 B4D07-- -INDEX 1  
 B4D09-- -READ 1  
 B4D10-- +READ CLOCK 1  
 B4D11-- -WRITE 1  
 B4D12-- +WRITE CLOCK 1  
 B4B02-- -CABLE CONTINUITY OUT  
 B4D13-- -CABLE CONTINUITY IN  
 B4B07-- GND  
 B4B13-- GND  
 B4D02-- GND  
 B4D08-- GND

FILE 1 BOARD (A1)  
PIN ASSIGNMENTS

-- A5B03  
 -- A5B04  
 -- A5B05  
 -- A5B08  
 -- A5B09  
 -- A5B10  
 -- A5B12  
 -- A5D03  
 -- A5D04  
 -- A5D05  
 -- A5D06  
 -- A5D07  
 -- A5D09  
 -- A5D10  
 -- A5D11  
 -- A5D12  
 -- A5B02  
 -- A5D13  
 -- A5B07  
 -- A5B13  
 -- A5D02  
 -- A5D08

B3 CONNECTS THRU CABLE TO A5 DU BOARD FILE 0  
 B4 CONNECTS THRU CABLE TO A5 DU BOARD FILE 1  
 (IF EXISTING)



DUC BOARD (A2)

A5B02 TIED TO A5D13 ON BOARD



DU BOARD (A1)

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4963 DEDICATED CABLES (TO FILE 2 & FILE 3)

DUC BOARD (A2)  
PIN ASSIGNMENTS

A4B03-- -CNTRL SAMPLE FILE 2  
 A4B04-- -DU INTRPT FILE 2  
 A4B05-- -SECTOR 2  
 A4B08-- +NRZ DATA 2  
 A4B09-- -MISSING SECTOR 2  
 A4B10-- -WRITE DATA 2  
 A4B12-- +INTRFC DEGATE FILE 2  
 A4D03-- +WRITE GATE RTN 2  
 A4D04-- -DATA SELECT 2  
 A4D05-- -FAST SYNC 2  
 A4D06-- -RESET ERROR FILE 2  
 A4D07-- -INDEX 2  
 A4D09-- -READ 2  
 A4D10-- +READ CLOCK 2  
 A4D11-- -WRITE 2  
 A4D12-- +WRITE CLOCK 2  
 A4B02-- -CABLE CONTINUITY IN  
 A4D13-- -CABLE CONTINUITY OUT  
 A4B07-- GND  
 A4B13-- GND  
 A4D02-- GND  
 A4D08-- GND

FILE 2 BOARD (A1)  
PIN ASSIGNMENTS

-- A5B03  
 -- A5B04  
 -- A5B05  
 -- A5B08  
 -- A5B09  
 -- A5B10  
 -- A5B12  
 -- A5D03  
 -- A5D04  
 -- A5D05  
 -- A5D06  
 -- A5D07  
 -- A5D09  
 -- A5D10  
 -- A5D11  
 -- A5D12  
 -- A5B02  
 -- A5D13  
 -- A5B07  
 -- A5B13  
 -- A5D02  
 -- A5D08

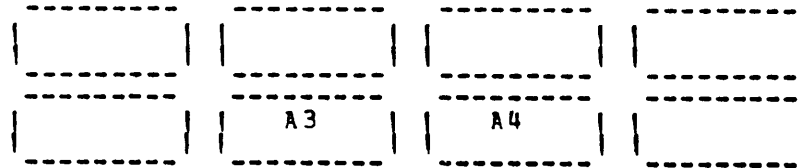
DUC BOARD (A2)  
PIN ASSIGNMENTS

A3B03-- -CNTRL SAMPLE FILE 3  
 A3B04-- -DU INTRPT FILE 3  
 A3B05-- -SECTOR 3  
 A3B08-- +NRZ DATA 3  
 A3B09-- -MISSING SECTOR 3  
 A3B10-- -WRITE DATA 3  
 A3B12-- +INTRFC DEGATE FILE 3  
 A3D03-- +WRITE GATE RTN 3  
 A3D04-- -DATA SELECT 3  
 A3D05-- -FAST SYNC 3  
 A3D06-- -RESET ERROR FILE 3  
 A3D07-- -INDEX 3  
 A3D09-- -READ 3  
 A3D10-- +READ CLOCK 3  
 A3D11-- -WRITE 3  
 A3D12-- +WRITE CLOCK 3  
 A3B02-- -CABLE CONTINUITY IN  
 A3D13-- -CABLE CONTINUITY OUT  
 A3B07-- GND  
 A3B13-- GND  
 A3D02-- GND  
 A3D08-- GND

FILE 3 BOARD (A1)  
PIN ASSIGNMENTS

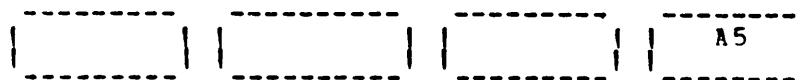
-- A5B03  
 -- A5B04  
 -- A5B05  
 -- A5B08  
 -- A5B09  
 -- A5B10  
 -- A5B12  
 -- A5D03  
 -- A5D04  
 -- A5D05  
 -- A5D06  
 -- A5D07  
 -- A5D09  
 -- A5D10  
 -- A5D11  
 -- A5D12  
 -- A5B02  
 -- A5D13  
 -- A5B07  
 -- A5B13  
 -- A5D02  
 -- A5D08

A4 CONNECTS THRU CABLE TO A5 DU BOARD FILE 2  
 (IF EXISTING)  
 A3 CONNECTS THRU CABLE TO A5 DU BOARD FILE 3  
 (IF EXISTING)



DUC BOARD (A2)

A5B02 TIED TO A5D13 ON BOARD



DU BOARD (A1)

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S.F. 4963

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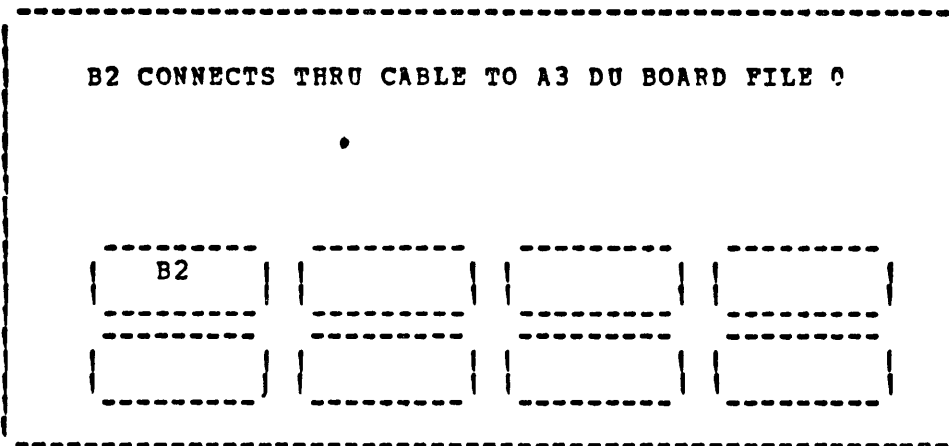
4963 CHAIN CABLE

DUC BOARD (A2)  
PIN ASSIGNMENTS

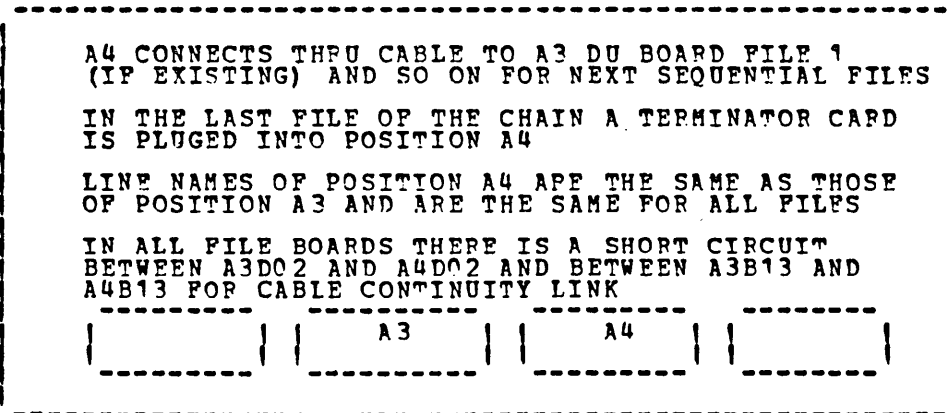
B2B02-- -DU TAG BUS BIT 0  
 B2B03-- -DU TAG BUS BIT 1  
 B2B04-- -DU TAG BUS BIT 2  
 B2B05-- -DU TAG BUS BIT P  
 B2B06-- NOT USED  
 B2B07-- +5 VOLTS FOR TERM CD  
 B2B08-- +5 VOLTS FOR TERM CD  
 B2B09-- +5 VOLTS FOR TERM CD  
 B2B10-- NOT USED  
 B2B11-- NOT USED  
 B2B12-- -CONTROL SAMPLE PCVD  
 B2B13-- -CABLE CONTINUITY IN  
 B2D02-- -CABLE CONTINUITY OUT  
 B2D03-- NOT USED  
 B2D04-- -MC DATA BUS BIT 0  
 B2D05-- -MC DATA BUS BIT 1  
 B2D06-- -MC DATA BUS BIT 2  
 B2D07-- -MC DATA BUS BIT 3  
 B2D08-- GND  
 B2D09-- -MC DATA BUS BIT 4  
 B2D10-- -MC DATA BUS BIT 5  
 B2D11-- -MC DATA BUS BIT 6  
 B2D12-- -MC DATA BUS BIT 7  
 B2D13-- -MC DATA BUS BIT P

FILE 0 BOARD (A1)  
PIN ASSIGNMENTS

-- A3B02  
 -- A3B03  
 -- A3B04  
 -- A3B05  
 -- A3B06  
 -- A3B07  
 -- A3B08  
 -- A3B09  
 -- A3B10  
 -- A3B11  
 -- A3B12  
 -- A3B13  
 -- A3D02  
 -- A3D03  
 -- A3D04  
 -- A3D05  
 -- A3D06  
 -- A3D07  
 -- A3D08  
 -- A3D09  
 -- A3D10  
 -- A3D11  
 -- A3D12  
 -- A3D13



DUC BOARD (A2)



DU BOARD A1 (FILE 0)

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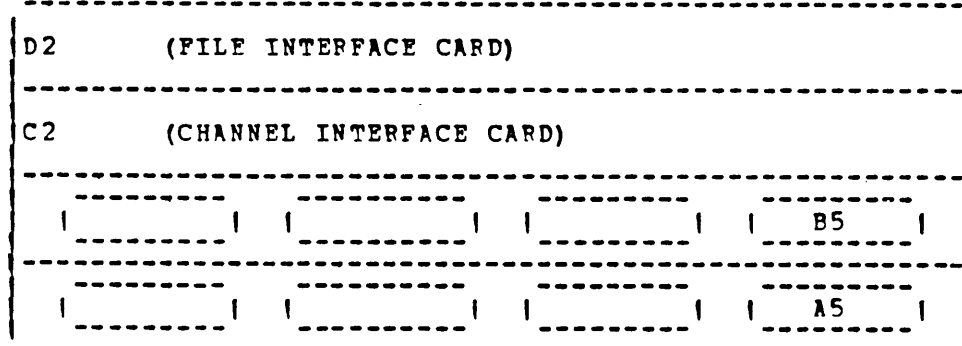
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 E.C. HISTORY MACH.  
 08-17-78 374947 4963  
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0 0 0

4963 DUC BOARD (A2) CABLE POSITIONS A5, B5 TO CARD A2C2

DUC BOARD (A2) CABLE POSITIONS A5, B5 PIN ASSIGNMENTS	DUC CARD A2C2 PIN ASSIGNMENTS	
B5B02--	-FILE DATA BUS BIT 00	-- C2M08-
B5B03--	-FILE DATA BUS BIT 01	-- C2M09-
B5B04--	-FILE DATA BUS BIT 02	-- C2M10-
B5B05--	-FILE DATA BUS BIT 03	-- C2M11-
B5B06--	-FILE DATA BUS BIT 04	-- C2M12-
B5B08--	-FILE DATA BUS BIT 05	-- C2M13-
B5B09--	-FILE DATA BUS BIT 06	-- C2S02-
B5B10--	-FILE DATA BUS BIT 07	-- C2S03-
B5B11--	-FILE DATA BUS BIT 08	-- C2S12-
B5D03--	-FILE DATA BUS BIT 08	-- C2S04-
B5D04--	-FILE DATA BUS BIT 09	-- C2S05-
B5D05--	-FILE DATA BUS BIT 10	-- C2S06-
B5D06--	-FILE DATA BUS BIT 11	-- C2S07-
B5D07--	-FILE DATA BUS BIT 12	-- C2S08-
B5D09--	-FILE DATA BUS BIT 13	-- C2S09-
B5D10--	-FILE DATA BUS BIT 14	-- C2S10-
B5D11--	-FILE DATA BUS BIT 15	-- C2S11-
B5D12--	-FILE DATA BUS BIT P1	-- C2S13-
A5B11--	-INTERC PARITY CHECK	-- C2P11-
A5D03--	-FILE TAG C	-- C2U04-
A5D04--	-FILE TAG 1	-- C2U05-
A5D05--	-FILE TAG 2	-- C2U06-
A5D06--	-FILE TAG 3	-- C2U07-
A5D12--	-FILE TAG P	-- C2U13-
A5B05--	-AKN REQ OUT	-- C2J06-
A5B08--	-STROBE IN	-- C2J10-
A5B09--	-REQUEST IN	-- C2J11-
A5D13--	-PARAKEET POR	-- C2M02-
A5B03--	-SYSTEM RESET	-- C2M03-
A5B04--	-REQUEST OUT	-- C2J13-
A5B06--	-STROBE OUT	-- C2J12-
A5B10--	-AKN REQ IN POWERED	-- C2J05-
A5B12--	-SYSTEM PWR ON RST	-- C2M06, C2D13-
A5D07--	-FILE TAG 4	-- C2U09-
A5D09--	-FILE TAG 5	-- C2U10-
A5D10--	-FILE TAG 6	-- C2U11-
A5D11--	-FILE TAG 7	-- C2U12-
B5D02--	GND	
B5D08--	GND	
B5B07--	GND	
B5B13--	GND	
A5D02--	GND	
A5D08--	GND	
A5B07--	GND	
A5B13--	GND	
B5D13--	-IPL (NOT USED)	-- C2D12-
A5B02--	BURST MODE (NOT USED)	-- C2U02-



DUC (A2) BOARD (CARD SIDE VIEW)

SPE 4963 THEORY DIAGRAMS  
MANUAL FOR DATA FLOW

COPYRIGHT IBM CORP 1976

4963 DUC BOARD PINS  
E.C. HISTORY MACH.  
08-17-78 374947 4963  
DATE LAST E.C. P.N. 6837774  
02-01-79 375351

S  
5  
0  
6

0 0 0

4963 DUC BOARD (A2) CABLE POSITIONS B2,B3,B4,A3,A4 TO CARD C2

DUC BOARD (A2) B2,B3,B4,A3,A4	CABLE POSITIONS PIN ASSIGNMENTS	DUC CARD A2C2 PIN ASSIGNMENTS
B2B02	-- -DU TAG BUS BIT 0	-- C2B10-
B2B03	-- -DU TAG BUS BIT 1	-- C2B09-
B2B04	-- -DU TAG BUS BIT 2	-- C2B12-
B2B05	-- -DU TAG BUS BIT P	-- C2B13-
B2B12	-- -CNTRL SAMPLE RCVD	-- C2P04-
B2D04	-- -HC DATA BUS BIT 0	-- C2J07-
B2D05	-- -HC DATA BUS BIT 1	-- C2G07-
B2D06	-- -MC DATA BUS BIT 2	-- C2G08-
B2D07	-- -MC DATA BUS BIT 3	-- C2G09-
B2D09	-- -MC DATA BUS BIT 4	-- C2G10-
B2D10	-- -MC DATA BUS BIT 5	-- C2J09-
B2D11	-- -MC DATA BUS BIT 6	-- C2G12-
B2D12	-- -MC DATA BUS BIT 7	-- C2G13-
B2D13	-- -MC DATA BUS BIT P	-- C2G05-
B3B03	-- -CNTRL SAMPLE FILE 0	-- C2J02-
B3B04	-- -DU INTRPT FILE 0	-- C2P02-
B3B12	-- +INTRFC DEGATE FILE 0	-- C2G03-
B3D06	-- -RESET ERROR FILE 0	-- C2P12-
B4B03	-- -CNTRL SAMPLE FILE 1	-- C2G02-
B4B04	-- -DU INTRPT FILE 1	-- C2D11-
B4B12	-- +INTRFC DEGATE FILE 1	-- C2B07-
B4D06	-- -RESET ERROR FILE 1	-- C2P13-
A4B03	-- -CNTRL SAMPLE FILE 2	-- C2J04-
A4B04	-- -DU INTRPT FILE 2	-- C2P05-
A4B12	-- +INTRFC DEGATE FILE 2	-- C2P07-
A4D06	-- -RESET ERROR FILE 2	-- C2M05-
A3B03	-- -CNTRL SAMPLE FILE 3	-- C2G04-
A3B04	-- -DU INTRPT FILE 3	-- C2P06-
A3B12	-- +INTRFC DEGATE FILE 3	-- C2P09-
A3D06	-- -RESET ERROR FILE 3	-- C2M04-
D4B07	-- +PLA CLOCK	-- C2B08-

GROUND FOR CARD ON BOARD  
C2B08

CABLE CONTINUITY LINK  
DUC BOARD (A2)  
PIN ASSIGNMENTS

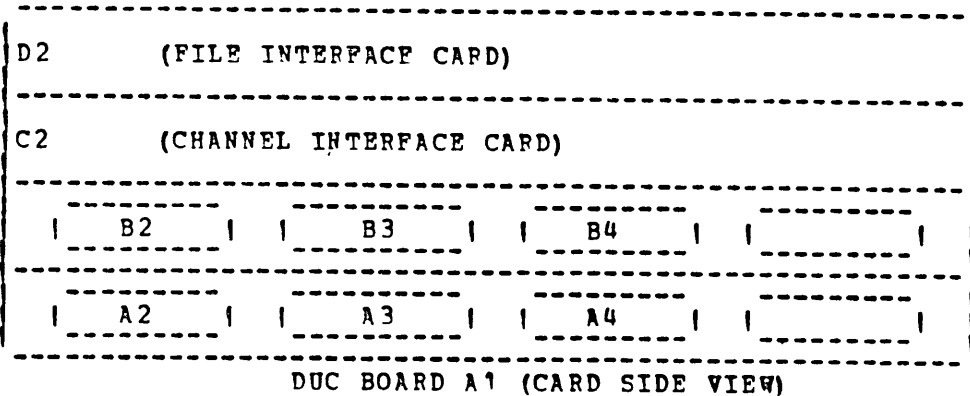
DUC BOARD (A2)  
PIN ASSIGNMENTS

B2D02	-- GND	
B2B13	-- CHAIN CABLE CONT.	-- B3B02-
B3B02	-- DEDIC. CABLE FILE 0 CONT.	
B3D13	-- DEDIC. CABLE FILE 0 CONT.	-- B4B02,A2D02-
B4B02	-- DEDIC. CABLE FILE 1 CONT.	
B4D13	-- DEDIC. CABLE FILE 1 CONT.	-- A4D13,A2D03-
A4D13	-- DEDIC. CABLE FILE 2 CONT.	
A4B02	-- DEDIC. CABLE FILE 2 CONT.	-- A3D13,A2D04-
A3D13	-- DEDIC. CABLE FILE 3 CONT.	
A3B02	-- DEDIC. CABLE FILE 3 CONT.	-- C2M07,A2B02,A2B03, A2B04-

DUC BOARD (A2) CABLE CONTINUITY JUMPERS

DEPENDING ON THE NUMBER OF FILES CONNECTED A JUMPER  
MUST BE INSTALLED ON THE DUC BOARD (A2) PER THE  
FOLLOWING TABLE

	A2B02-A2D02	A2B03-A2D03	A2B04-A2D04
1 FILE CONNECTED	YES	NO	NO
2 FILES CONNECTED	NO	YES	NO
3 FILES CONNECTED	NO	NO	YES
4 FILES CONNECTED	NO	NO	NO



SEE 4963 THEORY DIAGRAMS  
MANUAL FOR DATA FLOW

4963 DUC BOARD PINS

E.C. HISTORY MACH.  
08-17-78 374947

4963

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DATE 02-01-79 LAST E.C. 375351  
IBM CORP. GSD P.N. 6837775

0 0 0

SANCY



4963 DUC BOARD (A2) CABLE POSITIONS B3,B4,A3,A4, TO CARD D2

DUC BOARD (A2) CABLE POSITIONS  
B3,B4,A3,A4 PIN ASSIGNMENTS

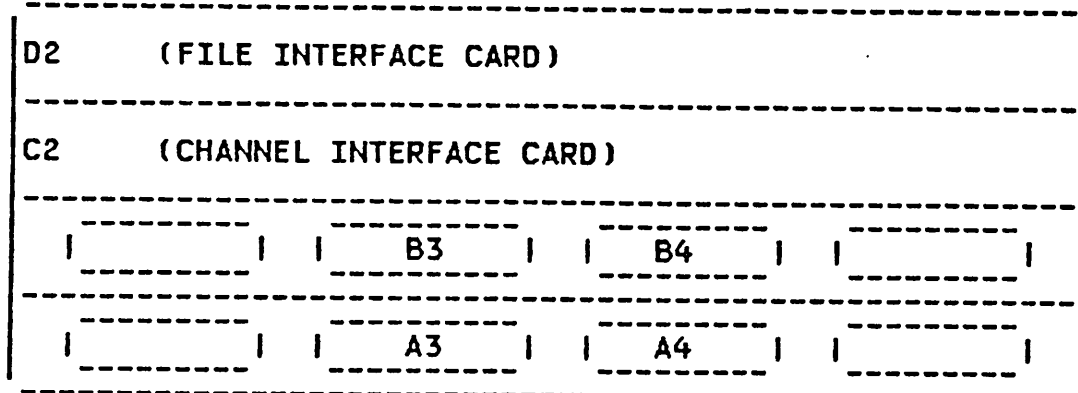
DUC CARD A2D2  
PIN ASSIGNMENTS

B3B05--	--SECTOR 0	-- D2J07-
B3B08--	+NRZ DATA 0	-- D2P05-
B3B09--	-MISSING SECTOR 0	-- D2D12-
B3B10--	-WRITE DATA 0	-- D2P02-
B3D03--	+WRITE GATE RTN 0	-- D2J02-
B3D04--	-DATA SELECT 0	-- D2D07-
B3D05--	-FAST SYNC 0	-- D2D05-
B3D07--	-INDEX 0	-- D2J05-
B3D09--	-READ 0	-- D2D02-
B3D10--	+READ CLOCK 0	-- D2J12-
B3D11--	-WRITE 0	-- D2D10-
B3D12--	+WRITE CLOCK 0	-- D2J10-
B4B05--	--SECTOR 1	-- D2J09-
B4B08--	+NRZ DATA 1	-- D2P06-
B4B09--	-MISSING SECTOR 1	-- D2D13-
B4B10--	-WRITE DATA 1	-- D2S02-
B4D03--	+WRITE GATE RTN 1	-- D2J04-
B4D04--	-DATA SELECT 1	-- D2D09-
B4D05--	-FAST SYNC 1	-- D2D06-
B4D07--	-INDEX 1	-- D2J06-
B4D09--	-READ 1	-- D2D04-
B4D10--	+READ CLOCK 1	-- D2J13-
B4D11--	-WRITE 1	-- D2D11-
B4D12--	+WRITE CLOCK 1	-- D2J11-
A4B05--	--SECTOR 2	-- D2G07-
A4B08--	+NRZ DATA 2	-- D2M04-
A4B09--	-MISSING SECTOR 2	-- D2B12-
A4B10--	-WRITE DATA 2	-- D2M02-
A4D03--	+WRITE GATE RTN 2	-- D2G02-
A4D04--	-DATA SELECT 2	-- D2B07-
A4D05--	-FAST SYNC 2	-- D2B04-
A4D07--	-INDEX 2	-- D2G04-
A4D09--	-READ 2	-- D2B02-
A4D10--	+READ CLOCK 2	-- D2G12-
A4D11--	-WRITE 2	-- D2B09-
A4D12--	+WRITE CLOCK 2	-- D2G09-
A3B05--	--SECTOR 3	-- D2G08-
A3B08--	+NRZ DATA 3	-- D2M05-
A3B09--	-MISSING SECTOR 3	-- D2B13-
A3D10--	-WRITE DATA 3	-- D2M03-
A3D03--	+WRITE GATE RTN 3	-- D2G03-
A3D04--	-DATA SELECT 3	-- D2B08-
A3D05--	-FAST SYNC 3	-- D2B05-
A3D07--	-INDEX 3	-- D2G05-
A3D09--	-READ 3	-- D2S12-
A3D10--	+READ CLOCK 3	-- D2G13-
A3D11--	-WRITE 3	-- D2B10-
A3D12--	+WRITE CLOCK 3	-- D2G10-
A5D13--	-PARAKEET POR	-- D2S03,S13

CARD PINS TIED TOGETHER ON BOARD FOR TEST POINTS

D2S09--	+CLOCK 2 TP	-- D2S11---
D2S05--	+T6 CLOCK TP	-- D2S05,S06,S07-
D2M08--	+WRITE SELECT TP	-- D2S08---
D2S10--	+BIT RING 8 TP	-- D2U10---

PINS ON CARD TIED TO GROUND AT BOARD  
D2M11,M12,P04,P10,P11,P12,U04,U05



DUC BOARD A2 (CARD SIDE VIEW)

SEE 4963 THEORY DIAGRAMS  
MANUAL FOR DATA FLOW

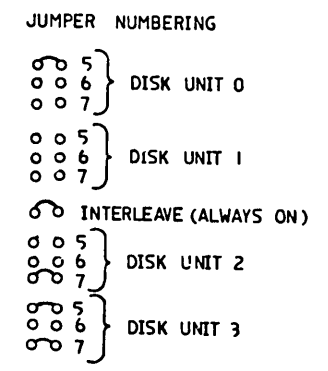
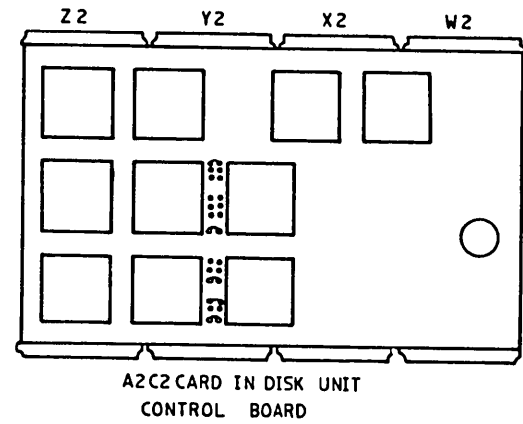
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4963 DUC BOARD PINS

E.C. HISTORY	MACH.
17AUG78 374947	
01FEB79 375351	4963

DATE	LAST E.C.	IBM CORP. GSD
10AUG81	323396	P.N. 6837776

80500  
0 0 0



IN THE ABOVE EXAMPLE  
 DISK UNIT 0 IS A MODEL 64A  
 DISK UNIT 1 IS A MODEL 59B  
 DISK UNIT 2 IS A MODEL 23B  
 DISK UNIT 3 IS A MODEL 29B

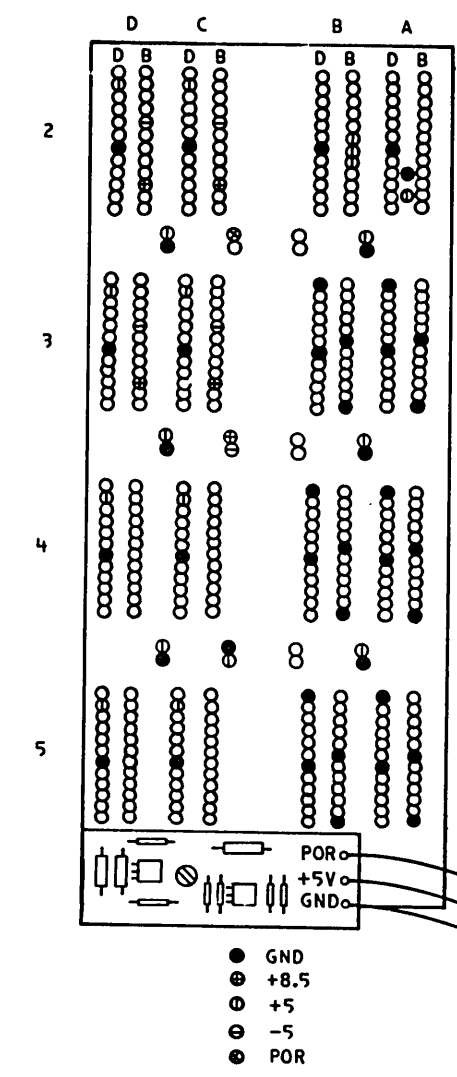


MODEL DESIGNATION

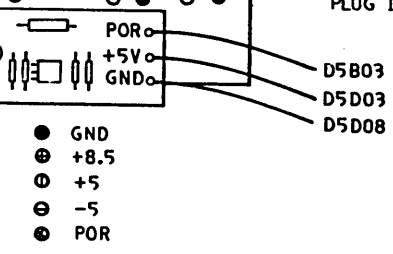
JUMPER NUMBER	5	6	7
DISK UNIT NOT INSTALLED		X	X
MODELS 23A OR 23B			X
MODELS 29A OR 29B	X		X
MODELS 58A OR 58B			
MODELS 64A OR 64B	X		

AN 'X' IN THE TABLE SIGNIFIES THAT A JUMPER IS INSTALLED. JUMPER P/N 1675209

DISK UNIT CONTROL BOARD  
 PIN PATTERN (PIN SIDE VIEW)



- CARDS
- CHANNEL CARD  
PLUGS IN C2
  - FILE CARD  
PLUGS IN D2
- # OF FILES ATTACHED
- 1 FILE JUMPER  
A2B02 TO A2D02
  - 2 FILES JUMPER  
A2B03 TO A2D03
  - 3 FILES JUMPER  
A2B04 TO A2D04
  - 4 FILES NO JUMPERS
- ATTACHMENT CABLES
- W2 PLUGS TO B5
  - X2 PLUGS TO A5
- CHAIN CABLE
- A3 OF FILE 0 TO B2
- DEDICATED CABLES
- A5 OF FILE 0 TO B3
  - A5 OF FILE 1 TO B4
  - A5 OF FILE 2 TO A4
  - A5 OF FILE 3 TO A3
- DECOUPLING CAP  
 PLUG IN A2

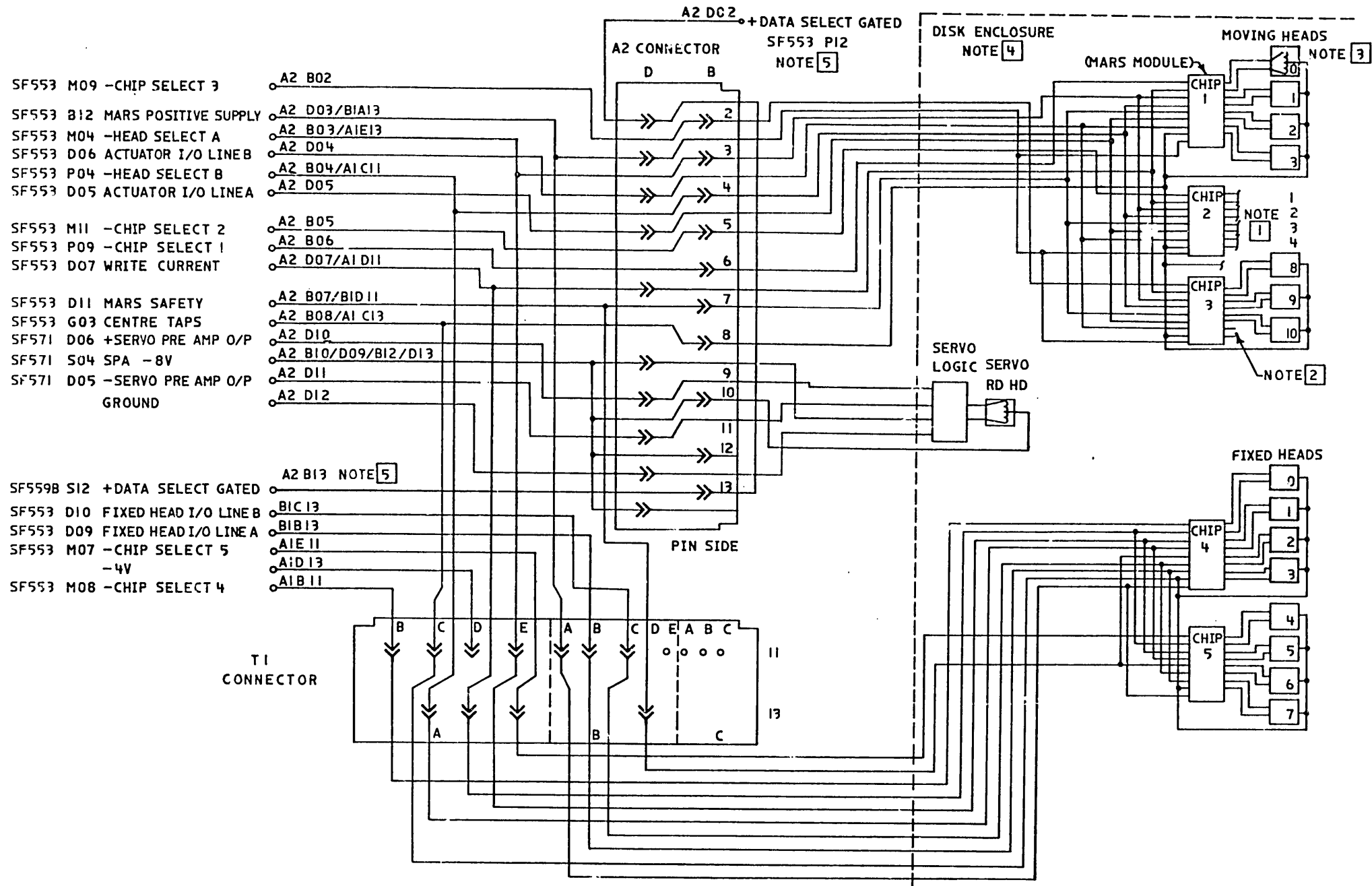


D5B03  
 D5D03  
 D5D08

EC HISTORY		DRAWING TITLE
20 FEB 79	375351	DUC JUMPERING
11 MAR 80	375662	MACH 4963
10 AUG 81	323396	PART NO 6839630
C	CLASSIFICATION	
	IBM CORP	

905710

905710



- SF553 M09 -CHIP SELECT 3
- SF553 B12 MARS POSITIVE SUPPLY
- SF553 M04 -HEAD SELECT A
- SF553 D06 ACTUATOR I/O LINE B
- SF553 P04 -HEAD SELECT B
- SF553 D05 ACTUATOR I/O LINE A
- SF553 M11 -CHIP SELECT 2
- SF553 P09 -CHIP SELECT 1
- SF553 D07 WRITE CURRENT
- SF553 D11 MARS SAFETY
- SF553 G03 CENTRE TAPS
- SF571 D06 +SERVO PRE AMP O/P
- SF571 S04 SPA -8V
- SF571 D05 -SERVO PRE AMP O/P
- GROUND
- SF559B S12 +DATA SELECT GATED
- SF553 D10 FIXED HEAD I/O LINE B
- SF553 D09 FIXED HEAD I/O LINE A
- SF553 M07 -CHIP SELECT 5
- 4V
- SF553 M08 -CHIP SELECT 4

TI CONNECTOR

PIN SIDE

SERVO LOGIC SERVO RD HD

FIXED HEADS

MOVING HEADS

DISK ENCLOSURE

MARS MODULE

A2 DC2 + DATA SELECT GATED  
SF553 P12  
NOTE 5

A2 CONNECTOR

NOTES:

- 1 CHIP 2 IS WIRED IN A SIMILAR MANNER TO CHIP 1
- 2 HEAD 11 IS NOT FITTED IF AN UNSAFE CONDITION IS DETECTED LOGIC CIRCUITS FORCE SELECTION OF HEAD 11 TO AVOID OVERWRITING DATA TRACKS
- 3 HEAD 0 NOT FITTED IF FIXED HEADS ARE INCLUDED IN DE.
- 4 COMPONENTS WITHIN THE DE ARE SEALED AND CANNOT BE SERVICED IN THE FIELD
- 5 DATA SELECT GATED IS LOOPED THROUGH THE A2 CONNECTOR TO TEST IF CONNECTOR IS CORRECTLY INSTALLED.

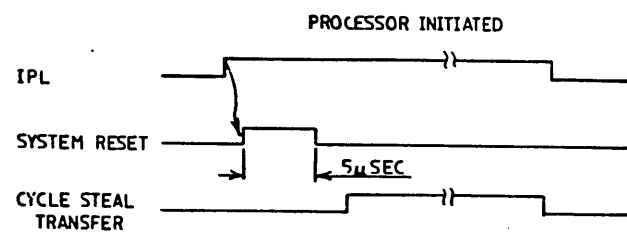
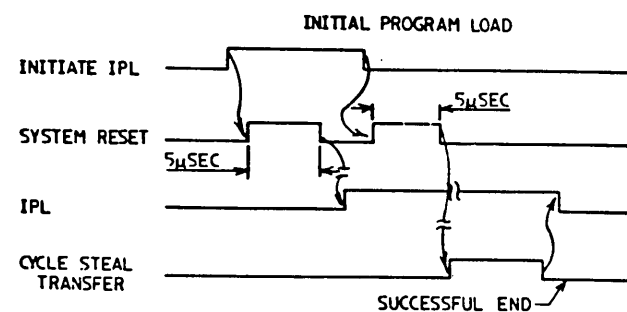
HEAD SELECTION DECODE (DOWN LEVEL=1)								
SYSTEM HEAD SELECT CODE	HEAD SELECTED	OUTPUT LINES SELECTED						
		CHIP SELECTS						
		1	2	3	4	5	A	B
00000	0	1	0	0	0	0	0	0
00001	1	1	0	0	0	0	1	0
00010	2	1	0	0	0	0	0	1
00011	3	1	0	0	0	0	1	1
00100	4	0	1	0	0	0	0	0
00101	5	0	1	0	0	0	1	0
00110	6	0	1	0	0	0	0	1
00111	7	0	1	0	0	0	1	1
01000	8	0	0	1	0	0	0	0
01001	9	0	0	1	0	0	1	0
01010	10 NOTE 3	0	0	1	0	0	0	1
01011	11 NOTE 2	0	0	1	0	0	1	1
01100	INVALID CODES	0	0	0	0	0	0	0
01101		0	0	0	0	0	1	0
01110		0	0	0	0	0	0	1
01111		0	0	0	0	0	1	1
10000	FH0	0	0	0	1	0	0	0
10001	FH1	0	0	0	1	0	1	0
10010	FH2	0	0	0	1	0	0	1
10011	FH3	0	0	0	1	0	1	1
10100	FH4	0	0	0	0	1	0	0
10101	FH5	0	0	0	0	1	1	0
10110	FH6	0	0	0	0	1	0	1
10111	FH7	0	0	0	0	1	1	1
11000	INVALID CODES	0	0	0	0	0	0	0
11001		0	0	0	0	0	1	0
11010		0	0	0	0	0	0	1
11011		0	0	0	0	0	1	1
11100		0	0	0	0	0	0	0
11101		0	0	0	0	0	1	0
11110		0	0	0	0	0	0	1
11111	0	0	0	0	0	1	1	

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	HEAD SELECTION DU CABLE	
11 MAR 80	375662	MACI' 4963	
		PART NO 6839719	
		CLASSIFICATION	
D		IBM CORP	

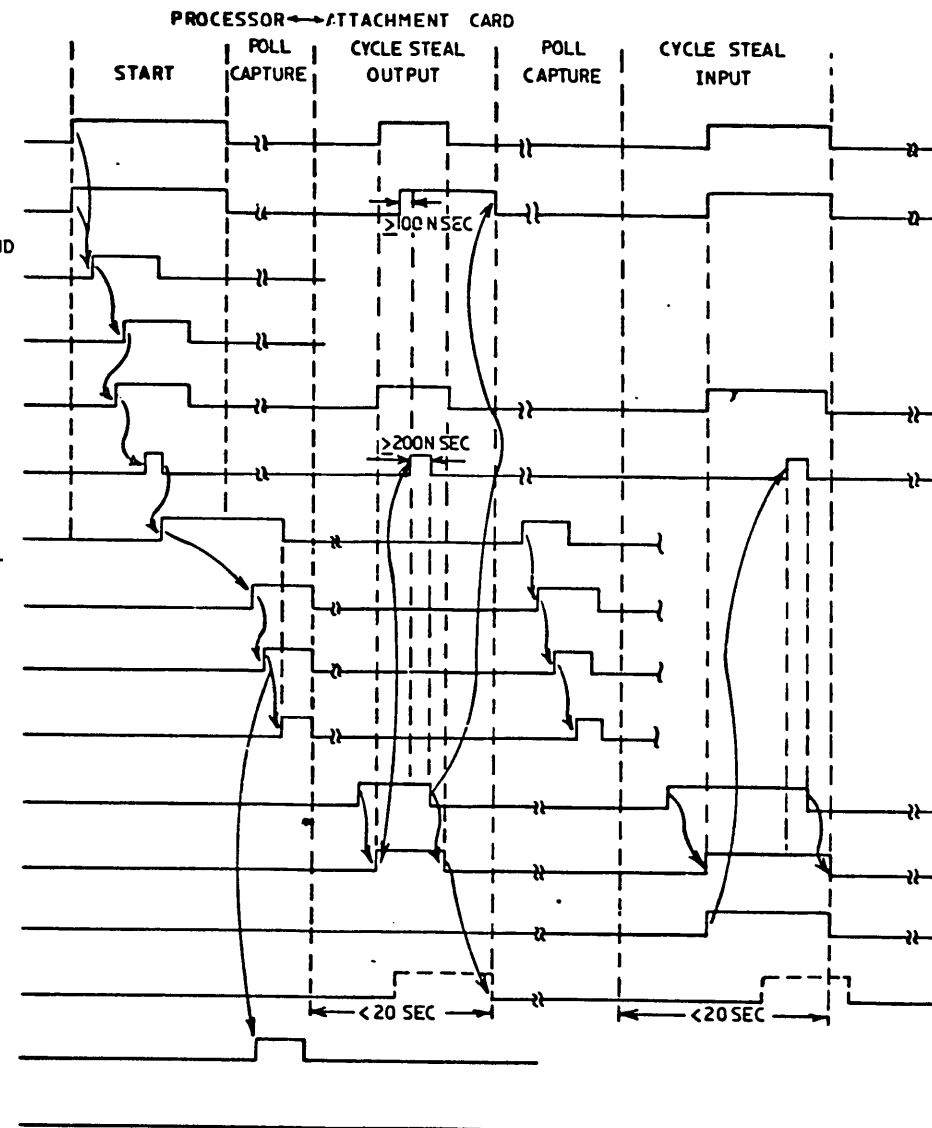
SUN7

SUN7

THE FOLLOWING SEQUENCE CHARTS ARE FOR REFERENCE ONLY AND TIMINGS ARE APPROXIMATE



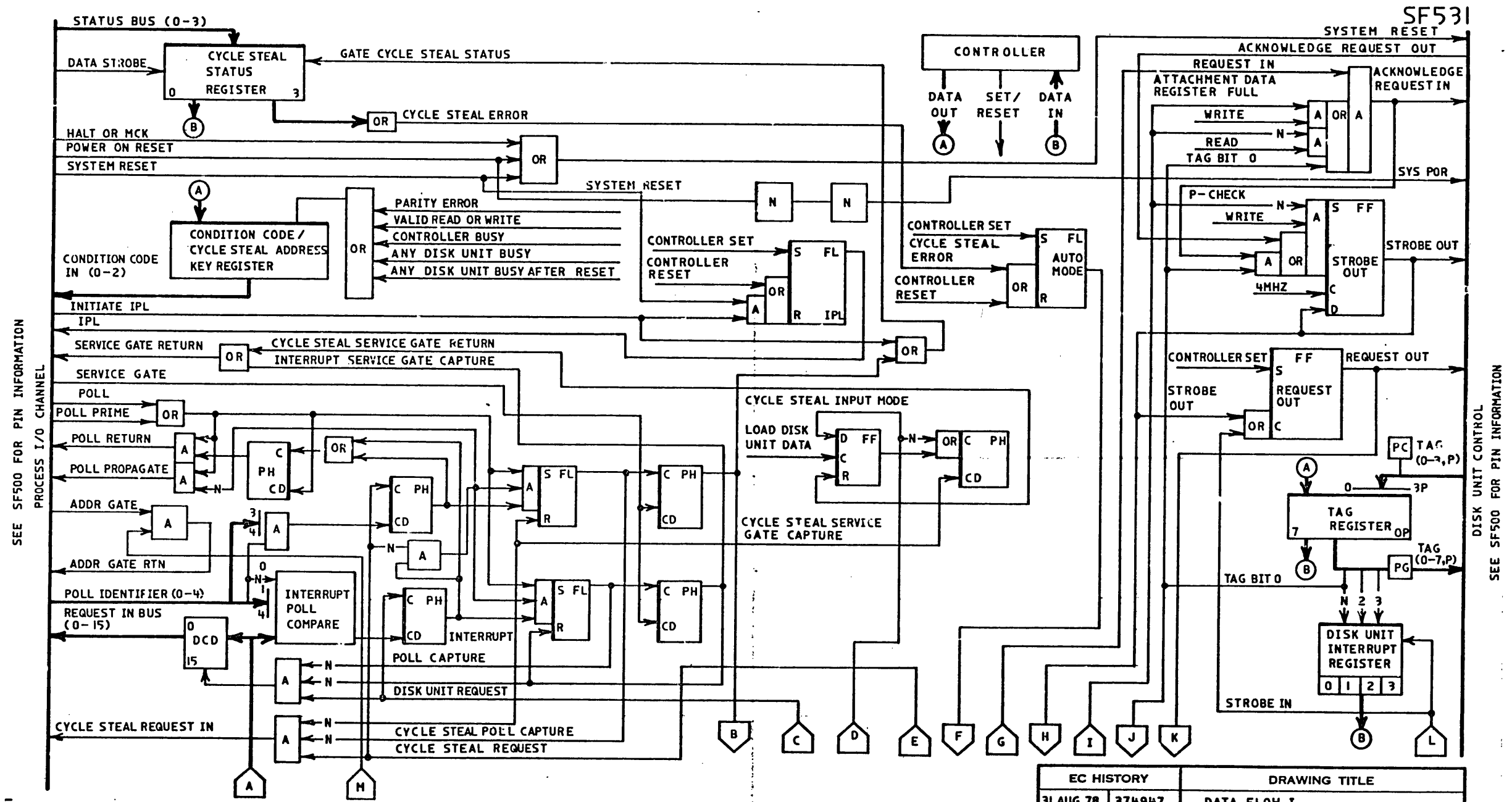
- ◁ ADDRESS BUS (17)  
BIT 16 OFF INDICATES CYCLE STEAL TO OR FROM STORAGE TO THE I/O DEVICE
- ◁ DATA BUS  
DATA BUS CONTAINS THE DEVICE CONTROL BLOCK (DCB) ADDRESS DURING A START COMMAND
- ▷ ADDRESS GATE
- ◁ ADDRESS GATE RETURN
- ◁ CONDITION CODE IN SIGNALS THE KEY DURING CYCLE ST TRANSFER
- ▷ DATA STROBE  
USED BY DEVICE TO REGISTER THE DATA ON OUTBOUND TRANSFER
- ◁ CYCLE STEAL REQUEST  
USED BY I/O DEVICE TO REQUEST AN INTERVAL OR ACCESS TO STORAGE RESOURCES
- ▷ POLL IDENTIFIER  
IDENTIFY NATURE OF POLL
- ▷ POLL  
IS CAPTURED BY FIRST DEVICE TO SEE IT WITH REQUEST IN RAISED
- ◁ POLL RETURN  
SENT BY I/O DEVICE TO SIGNAL A POLL CAPTURE HAS BEEN TAKEN
- ▷ SERVICE GATE  
INDICATES BEGIN TRANSFER TO THE DEVICE
- ◁ SERVICE GATE RETURN  
SIGNALS RECOGNITION OF SERVICE GATE
- ◁ OUTPUT/INPUT INDICATOR  
OFF OUTPUT FROM STORAGE ON INPUT TO STORAGE
- ▷ C.S. STATUS BUS  
SIGNALS THE DEVICE OF ANY ERRORS THE CHANNEL HAS DETECTED
- ▷ POLL PROPAGATE  
IF REQUEST IS NOT ON
- ◁ REQUEST IN BUS  
ONE OF 16 LINES ON FOR INTERRUPT REQUEST



EC HISTORY		DRAWING TITLE	
20FEB79	375351	DPC AND CYCLE STEAL SEQ	
		MACH	4963
		PART NO 6839631	
C		CLASSIFICATION	IBM CORP

SUNW

SUNW



SF531

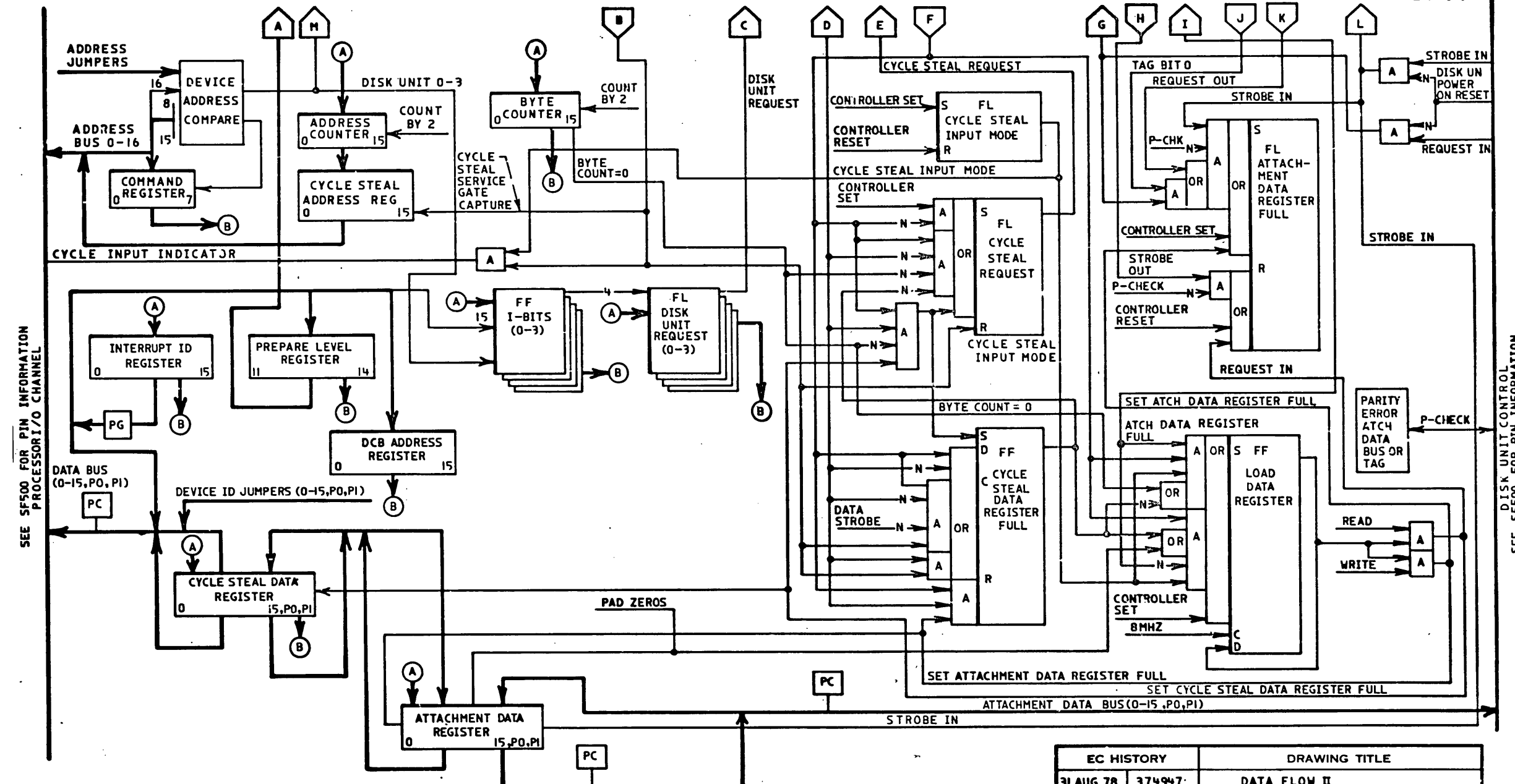
EC HISTORY		DRAWING TITLE
31 AUG 78	374947	DATA FLOW I
2 FEB 79	375351	MACH 4963
11 MAR 80	375662	PART NO 6837777

C	CLASSIFICATION	<b>IBM</b> COPP

11/10/77

SLSM

SF532



SEE SF500 FOR PIN INFORMATION PROCESSOR I/O CHANNEL

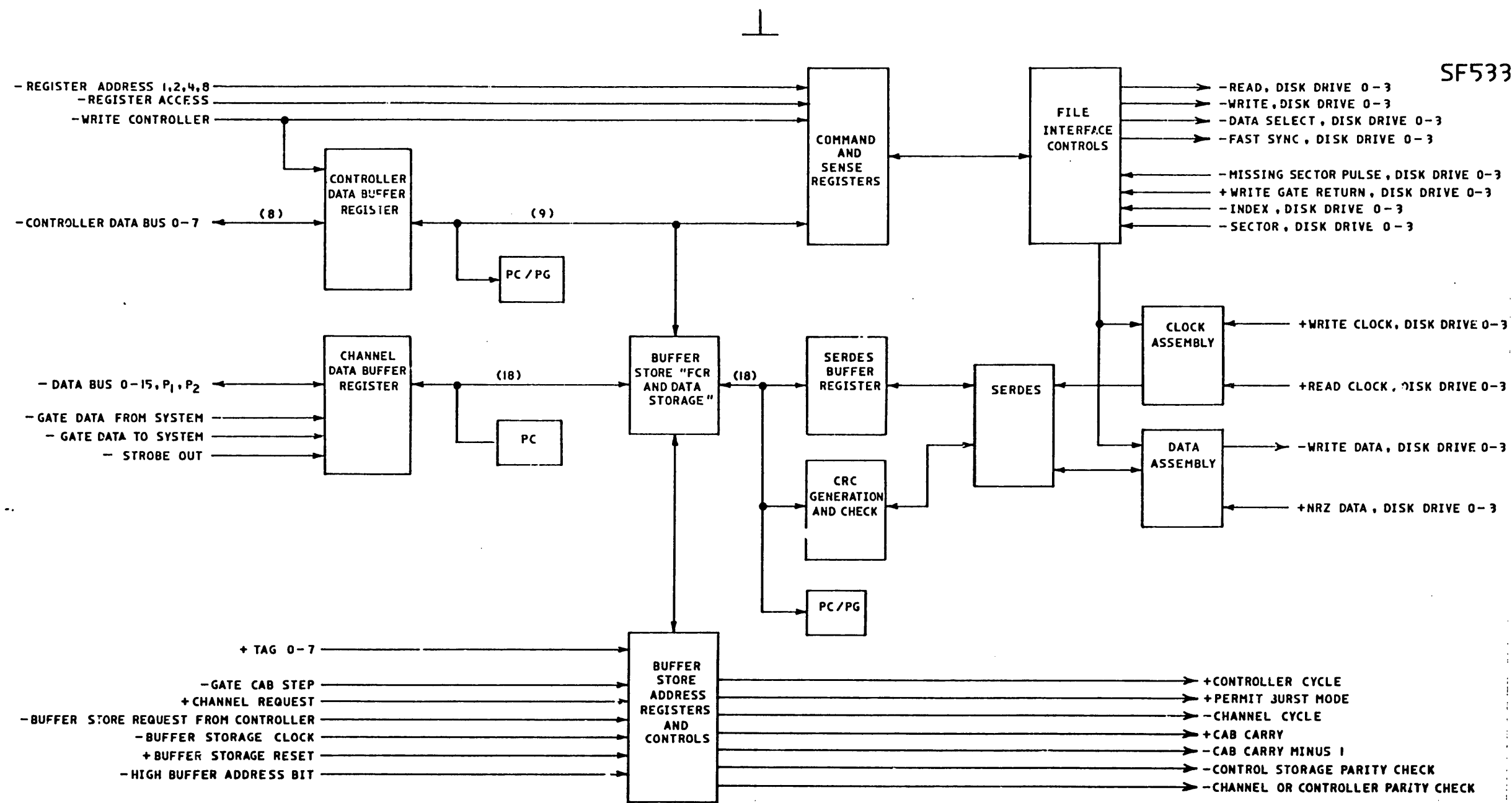
SEE SF500 FOR PIN INFORMATION DISK UNIT CONTROL

N2WJTTU

N2WJTTU

EC HISTORY		DRAWING TITLE	
31 AUG 78	374947	DATA FLOW II	
2 FEB 79	375351	MACH 4963	
		PART NO 6837778	
		CLASSIFICATION	<b>IBM</b> CORP

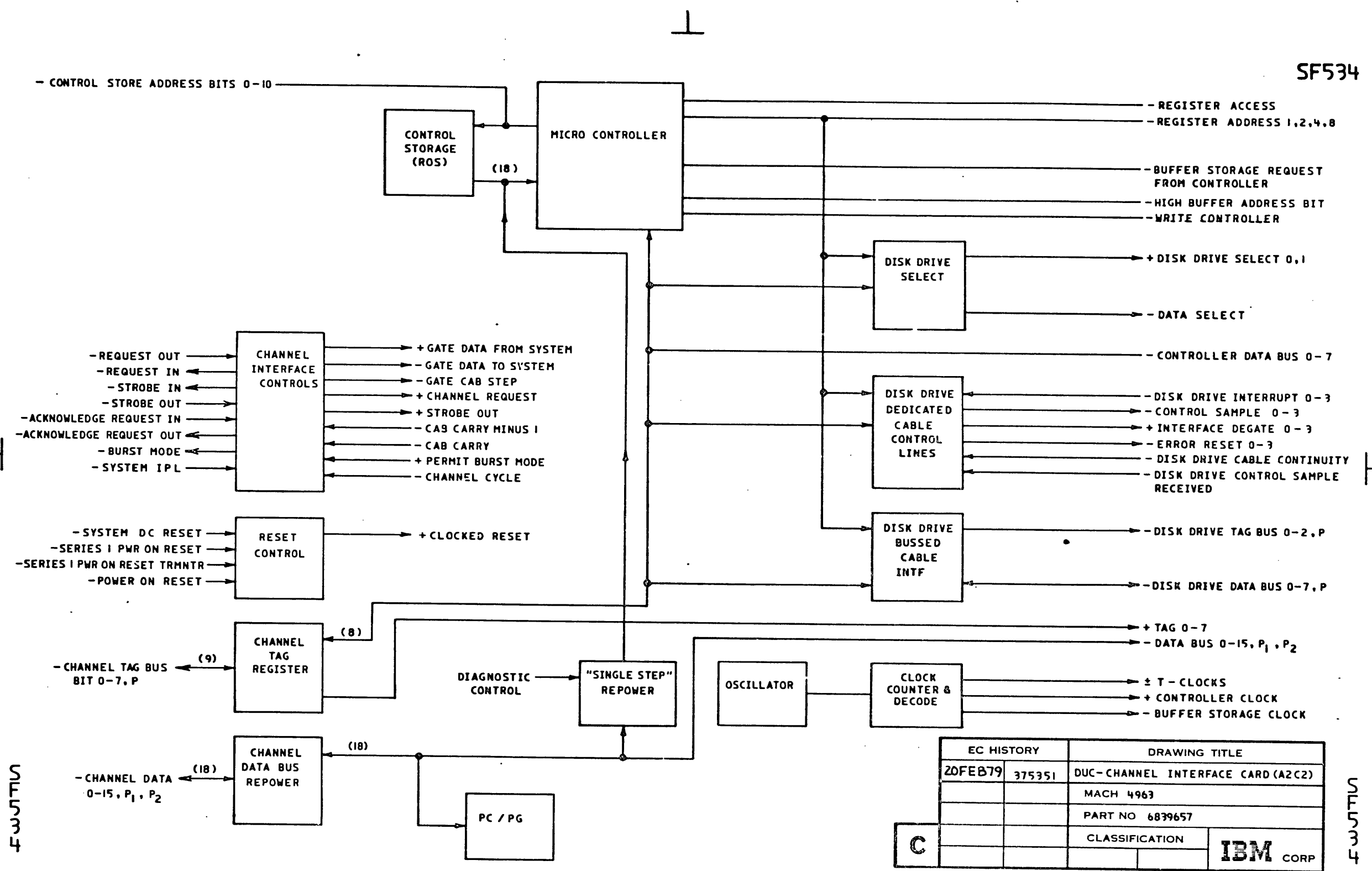
SF533



EC HISTORY		DRAWING TITLE	
20FEB79	375351	DUC- FILE INTERFACE CARD (A2D2)	
		MACH	4963
		PART NO	6839656
		CLASSIFICATION	
<b>C</b>		<b>IBM</b> CORP	

W33333

W33333



EC HISTORY		DRAWING TITLE	
Z0FEB79	375351	DUC-CHANNEL INTERFACE CARD (A2C2)	
		MACH 4963	
		PART NO 6839657	
C		CLASSIFICATION	IBM CORP

F33371U

F33371U



SF535

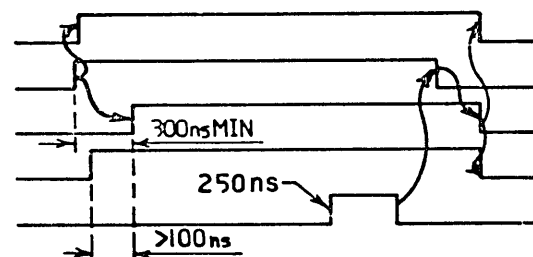
LINE NAME	PIN
+ TAG 0	A2-D2 X24
1	X25
2	X26
3	X28
4	X29
5	X30
6	X32
7	X33
- CONTROLLER DATA BUS BIT 0	Y23
1	Y24
2	Y25
3	Y26
4	Y28
5	Y29
6	Y30
7	Y32
- DATA BUS BIT 0	Z05
1	Z06
2	Z07
3	Z09
4	Z10
5	Z11
6	Z12
7	Z13
8	Z22
9	Z23
10	Z24
11	Z25
12	Z26
13	Z28
14	Z29
15	Z30
P1 (0-7)	Z02
P2 (8-15)	Z03
+ DISK DRIVE SELECT BIT 0	W06
1	W07
- DATA SELECT	W09
- REGISTER ADDRESS 1	X05
2	X06
4	X22
8	X23
- REGISTER ACCESS	X11
- WRITE CONTROLLER	Y22

LINE NAME	PIN
+ GATE DATA FROM SYSTEM	A2-D2 Y05
- GATE DATA TO SYSTEM	Y07
+ STROBE OUT	Y09
- GATE CAB STEP	W29
+ CHANNEL REQUEST	X03
- BUFFER STORE REQUEST FROM CONTROLLER	X13
- BUFFER STORAGE CLOCK	Y33
+ BUFFER STORAGE RESST	Y06
+ PERMIT BURST MODE	W13
- CHANNEL CYCLE	W10
+ CAB CARRY	X09
- CAB CARRY MINUS 1	X10
+ CONTROLLER CYCLE	W11
+ T0	W12
+ T0	Y13
+ T1	X02
+ T2	W33
+ T4	W32
- T5	W28
+ T7	Y11
+ T9	W30
+ OSCILLATOR INPUT	W03
+ OSCILLATOR OUTPUT	W23
- CONTROLLER WRAP	W05
- CONTROLLER WRAP	W22
+ EXTERNAL RESET	W26
- CONTROL STORAGE PARITY CHECK	W02
- HIGH BUFFER ADDRESS BIT	X12
- CHANNEL OR CONTROLLER PARITY CHECK	Y03
+ DIAGNOSTIC DATA	Z32
+ DIAGNOSTIC LATCH 1	Y12
2	Z33
3	Y02
+ SCAN DATA	X07
- LEFTMOST BYTE	Y10

EC HISTORY		DRAWING TITLE	
20FEB79	375351	CAP - CHANNEL FILE INTF TOP CARD	
		MACH 4963	CONNECTORS
		PART NO 6839658	
C		CLASSIFICATION	IBM CORP

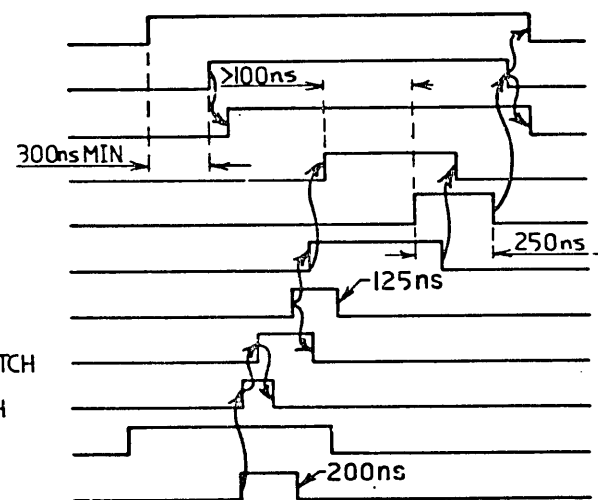
COMMAND MODE - WRITE

- \* + TAG BUS OUT
- \* + REQUEST OUT
- \* + AKN REQUEST OUT
- \* + ATTACH I/O DATA BUS OUT
- \* + STROBE OUT



HIGH SPEED DATA MODE - WRITE

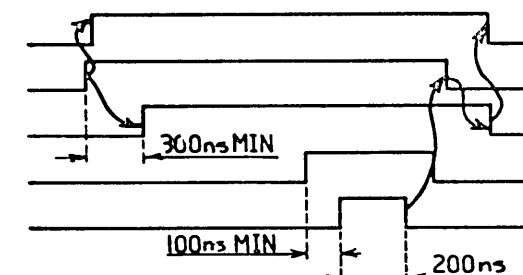
- \* + TAG BUS IN
- \* + REQUEST IN
- \* + ATTACH I/O DATA BUS OUT
- \* + AKN REQUEST IN
- \* + STROBE OUT
- + I/O DATA REG FULL LATCH
- + LOAD ATTACH DATA REG
- + RESET CS DATA REG FULL LATCH
- + CS DATA REG FULL LATCH
- + CS SEQUENCE
- + S/I DATA STROBE



\* ATTACHMENT INTERFACE LINE

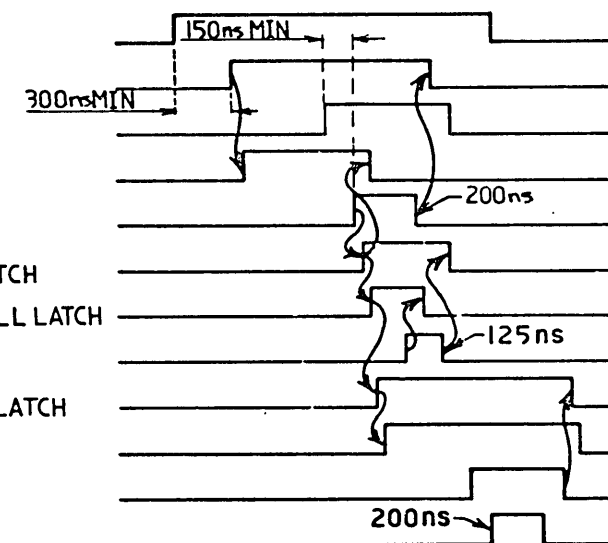
COMMAND MODE READ

- \* + TAG BUS OUT
- \* + REQUEST OUT
- \* + AKN REQUEST OUT
- \* + ATTACH I/O DATA BUS IN
- \* + STROBE IN



HIGH SPEED DATA MODE - READ

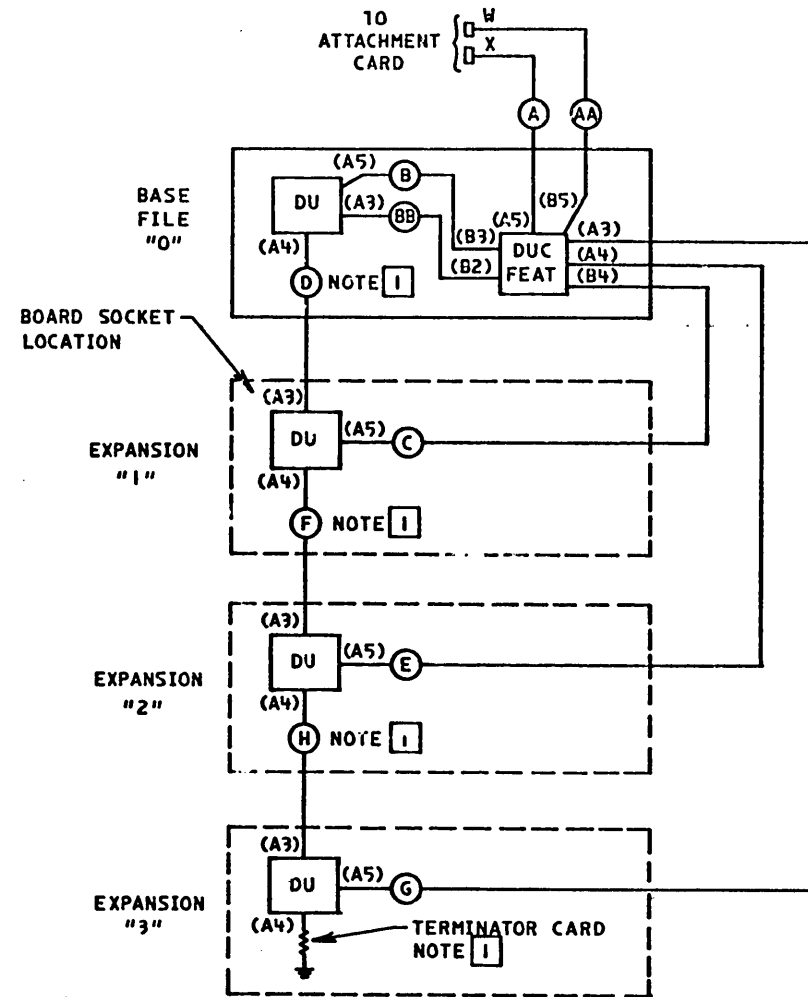
- \* + TAG BUS IN
- \* + REQUEST IN
- \* + ATTACH DATA BUS IN
- \* + AKN REQUEST IN
- \* + STROBE IN
- + I/O DATA REG FULL LATCH
- + SET CS DATA REG FULL LATCH
- + LOAD CS DATA REG
- + CS DATA REG FULL LATCH
- + CS SEQUENCE
- + SERVICE GATE RTN
- + S/I DATA STROBE



EC HISTORY		DRAWING TITLE	
20FEB79	375351	ATTACHMENT TO CAP TIMINGS	
		MACH 4963	
		PART NO 6839654	
C		CLASSIFICATION	IBM CORP

SUN 3

SUN 3



NOTE:  
 I TERMINATOR CARD PN 5861353 PLUGS INTO POSITION A4 OF DU BOARD (A1) OF LAST FILE

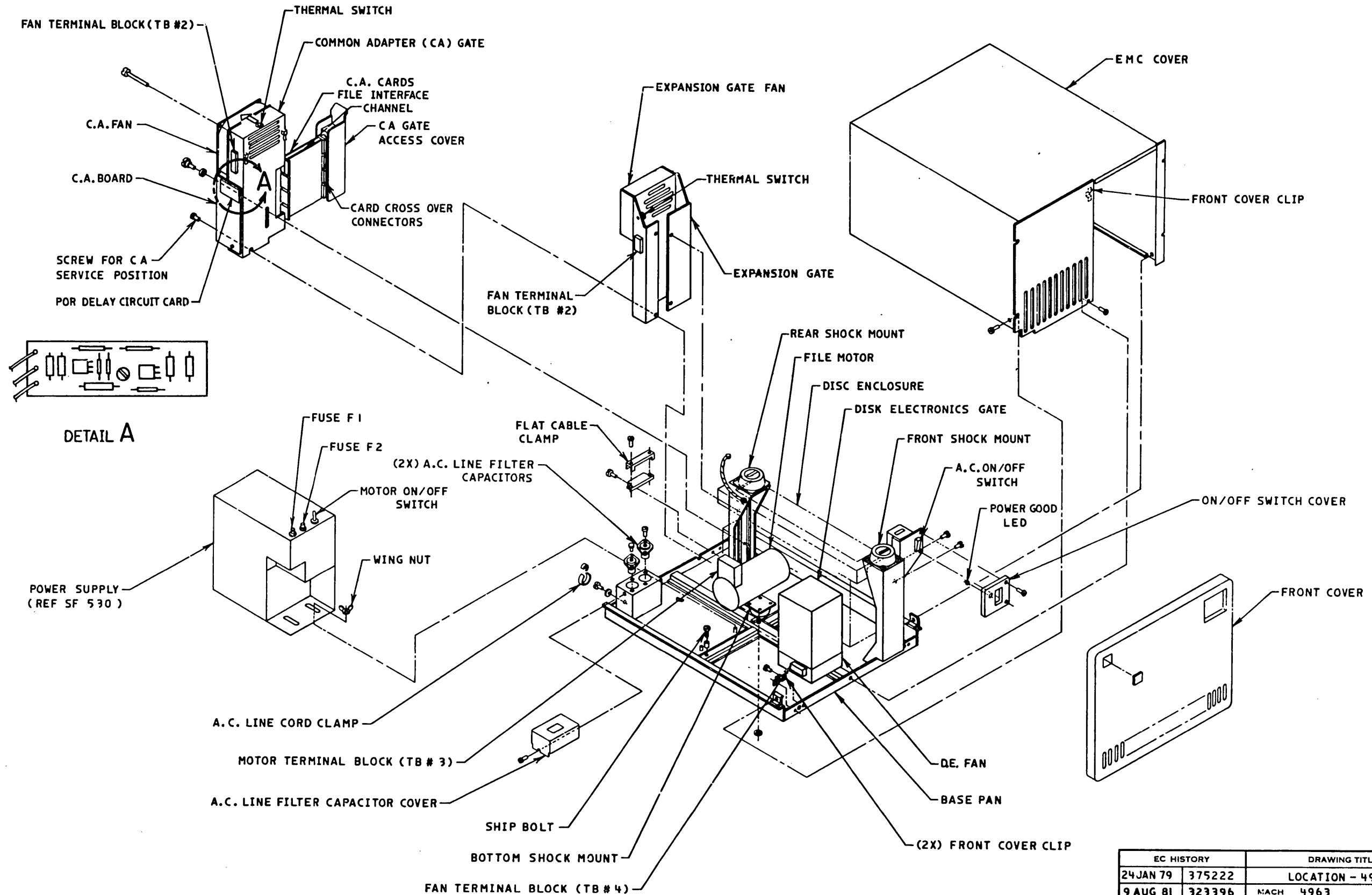
NO.	FLAT CABLE P/N	CABLE TYPE (REF)	USED ON
(A)	4411709 SEQ 001	5802425	4411397
(AA)	4411709 SEQ 002	5802425	4411397
(B)	4411710 SEQ 001	5802425	4411397
(BB)	4411710 SEQ 002	5802225	4411397
(C)	4411711	5802425	4411399
(D)	4411714	5802225	4411399
(E)	4411712	5802425	4411400
(F)	4411715	5802225	4411400
(G)	4411713	5802425	4411401
(H)	4411716	5802225	4411401

5802425-20 SIG (4 GND-D8, D2, B7, B13)  
 5802225-20 SIG (1 GND-D8)

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	CABLING OF DU'S	
		MACH 4963	
		PART NO 5839655	
C		CLASSIFICATION	IBM CORP

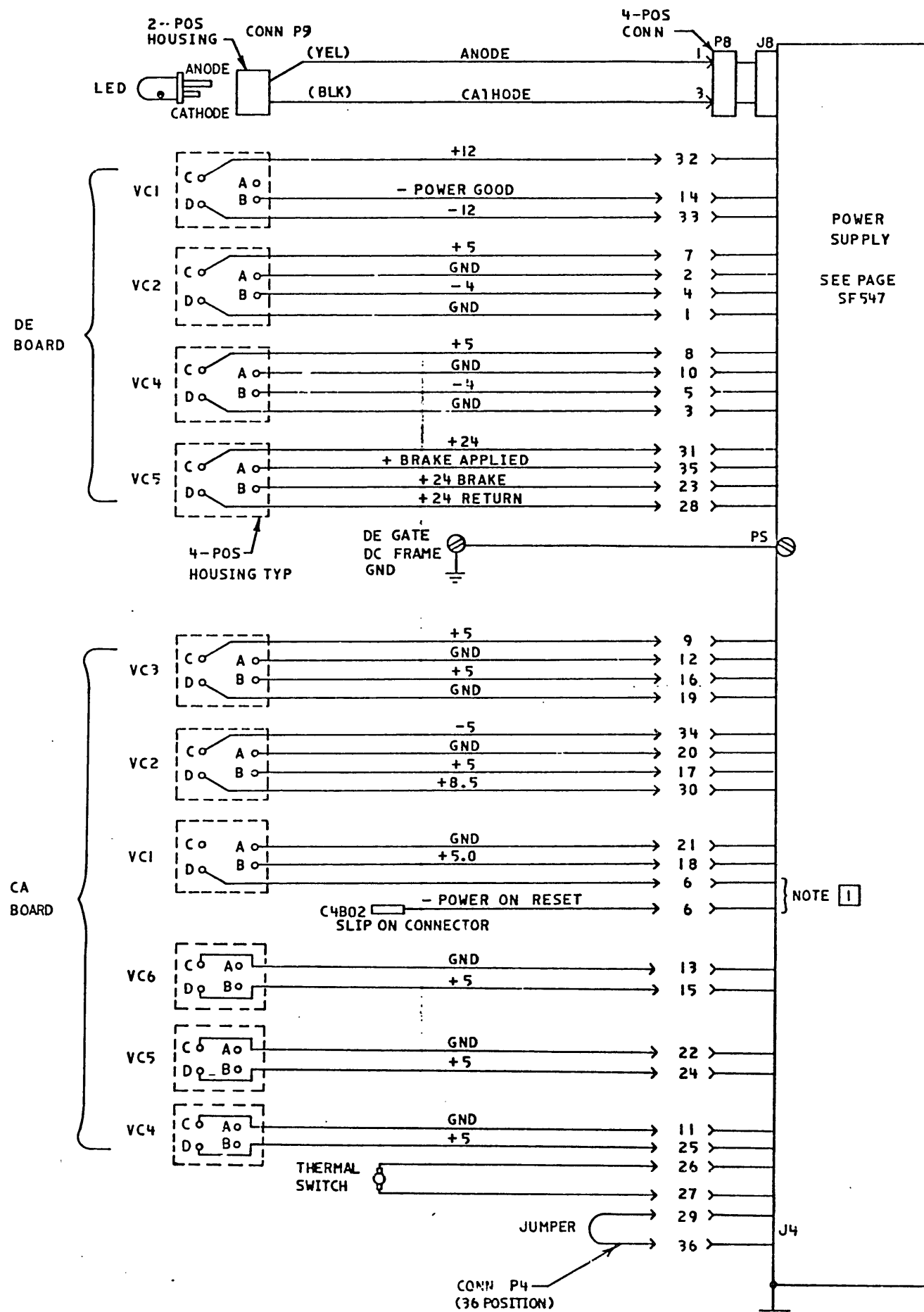
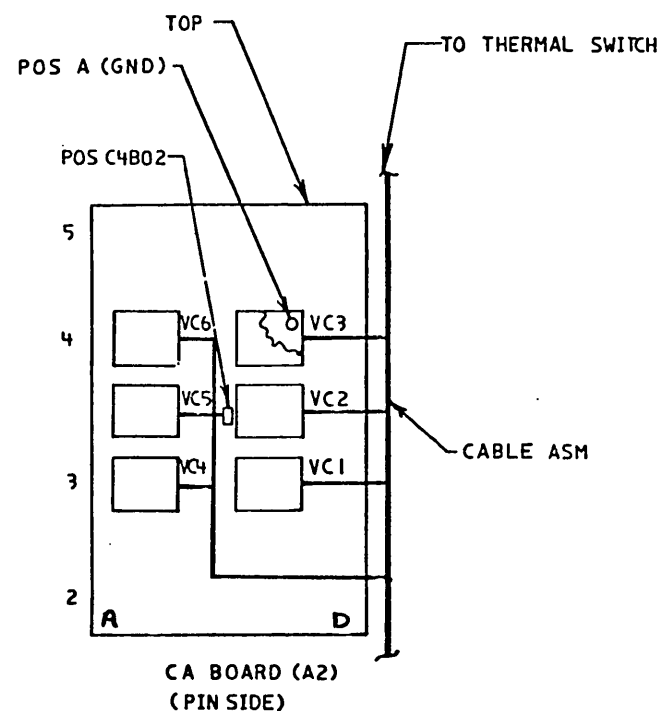
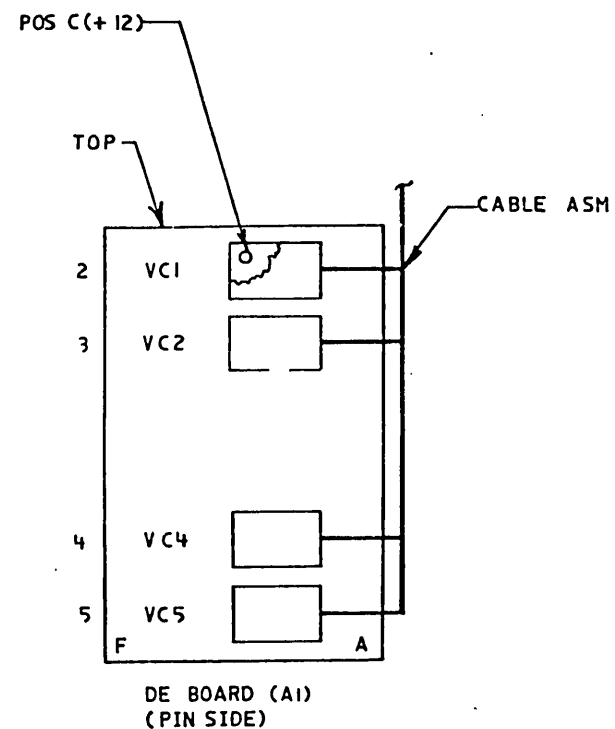
51573

51573



EC HISTORY		DRAWING TITLE	
24 JAN 79	375222	LOCATION - 4963	
9 AUG 81	323396	MACH	4963
		PART NO 4412888	
		CLASSIFICATION	
<b>D</b>		<b>IBM</b> CORP	

S  
F  
5  
4  
4



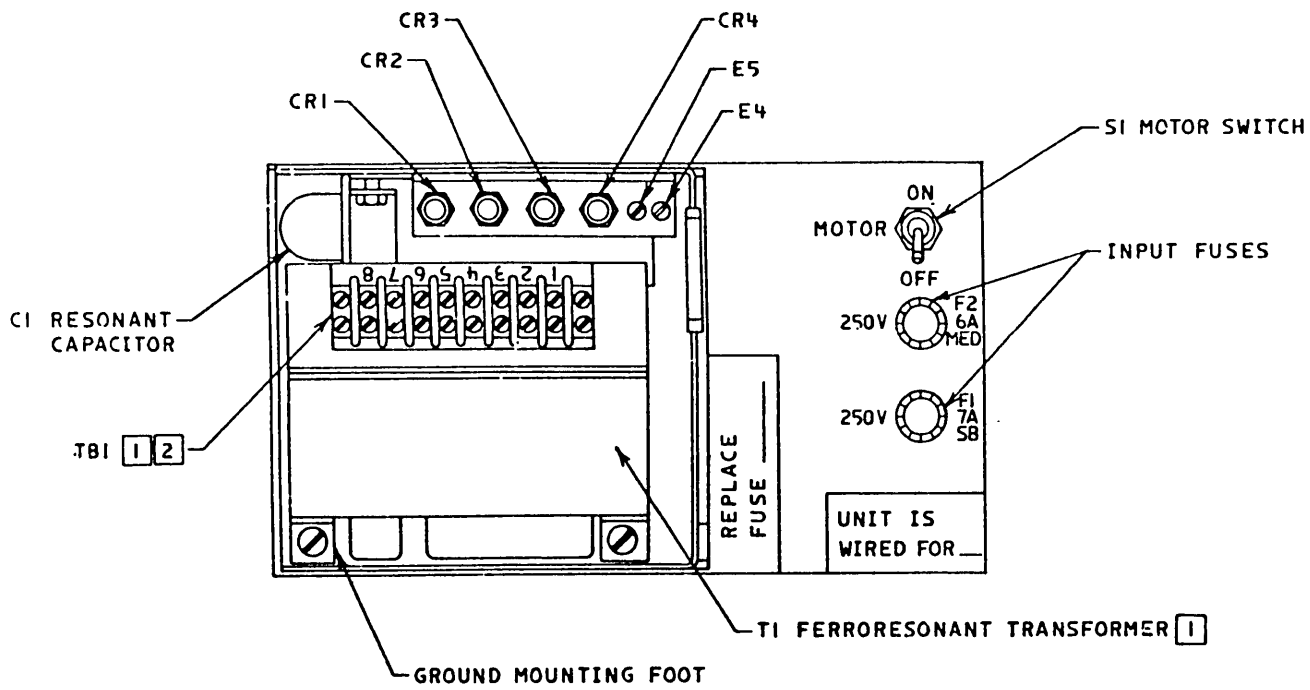
NOTE:

1 DEPENDS ON 4963 EC LEVEL, POWER ON RESET (6) CAN BE WIRED TO VC1-D OR SLIP ON CONNECTOR THAT PLUGS TO C4B02 ON BOARD

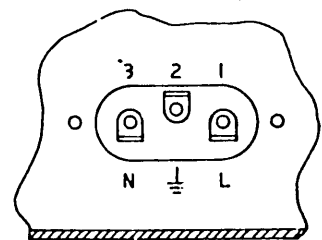
SF 545

SF 545

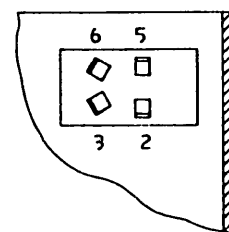
EC HISTORY		DRAWING TITLE
31 AUG 78	374947	SCHEMATIC - BDS DC
2 FEB 79	375351	MACH 4963
11 MAR 80	375662	PART NO 6837362
D		CLASSIFICATION
		IBM CORP



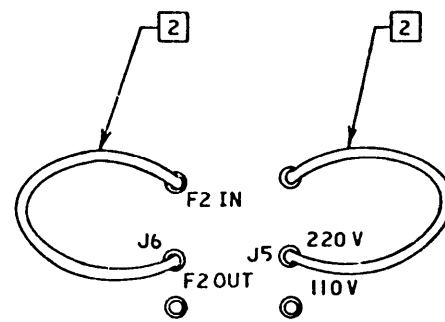
TOP VIEW



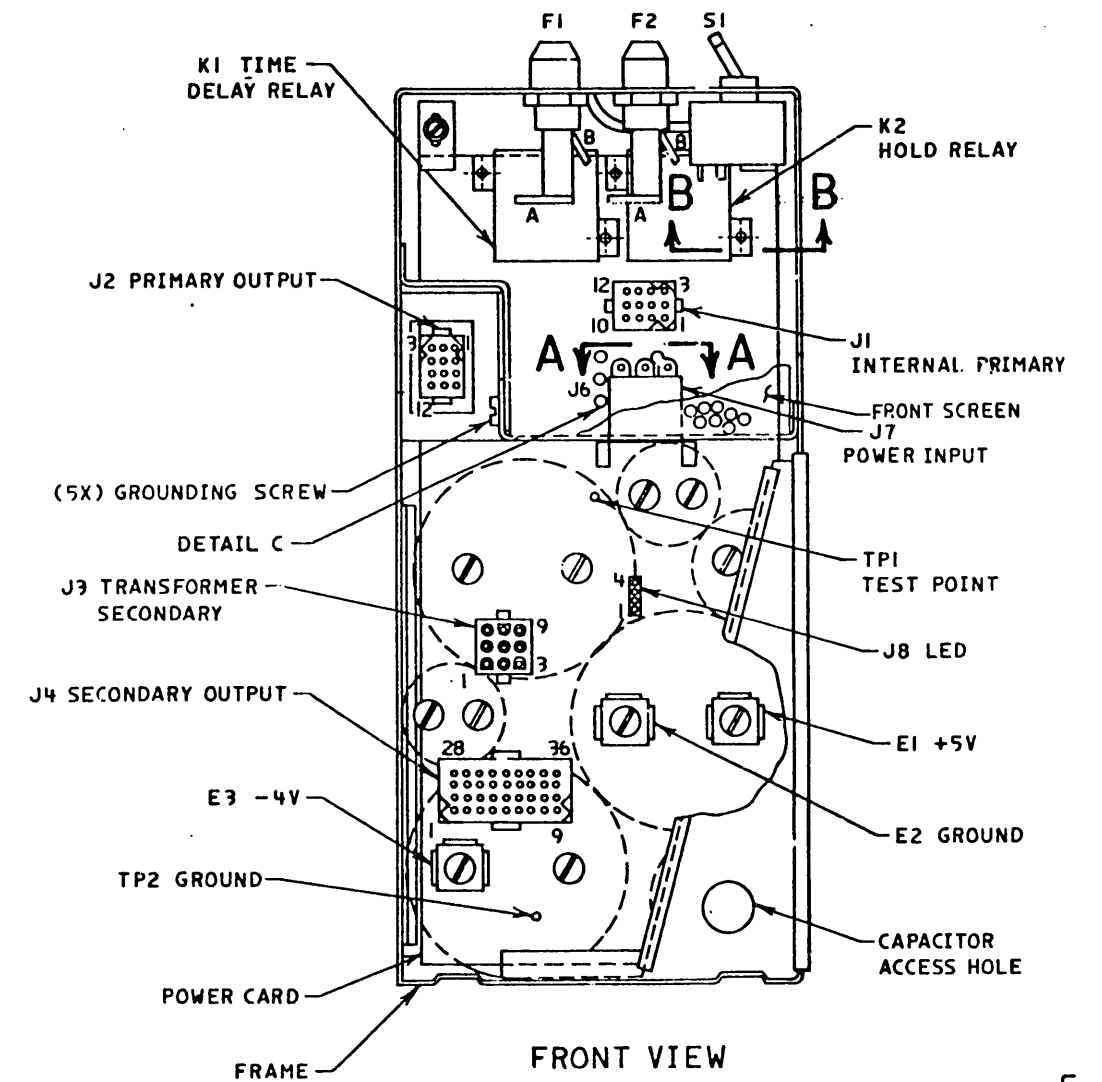
PARTIAL VIEW A-A  
WIRING SIDE OF J7 CONN



PARTIAL VIEW B-B  
WIRING SIDE OF SI MOTOR SWITCH



DETAIL C  
J5 AND J6 JUMPERS



FRONT VIEW

NOTES:

- 1 TI AND TBI ARE SHOWN WITH SHIELD REMOVED
- 2 SEE TABLE 1, PAGE SF 547, FOR WIRING INSTRUCTIONS

EC HISTORY		DRAWING TITLE	
31 AUG 78	374947	POWER SUPPLY VIEWS	
2 FEB 79	275351	MACH 4963	
11 MAR 80	375662	PART NO 4411341	
D		CLASSIFICATION	IBM CORP

J7 VAC INPUT (PLUG VIEW)

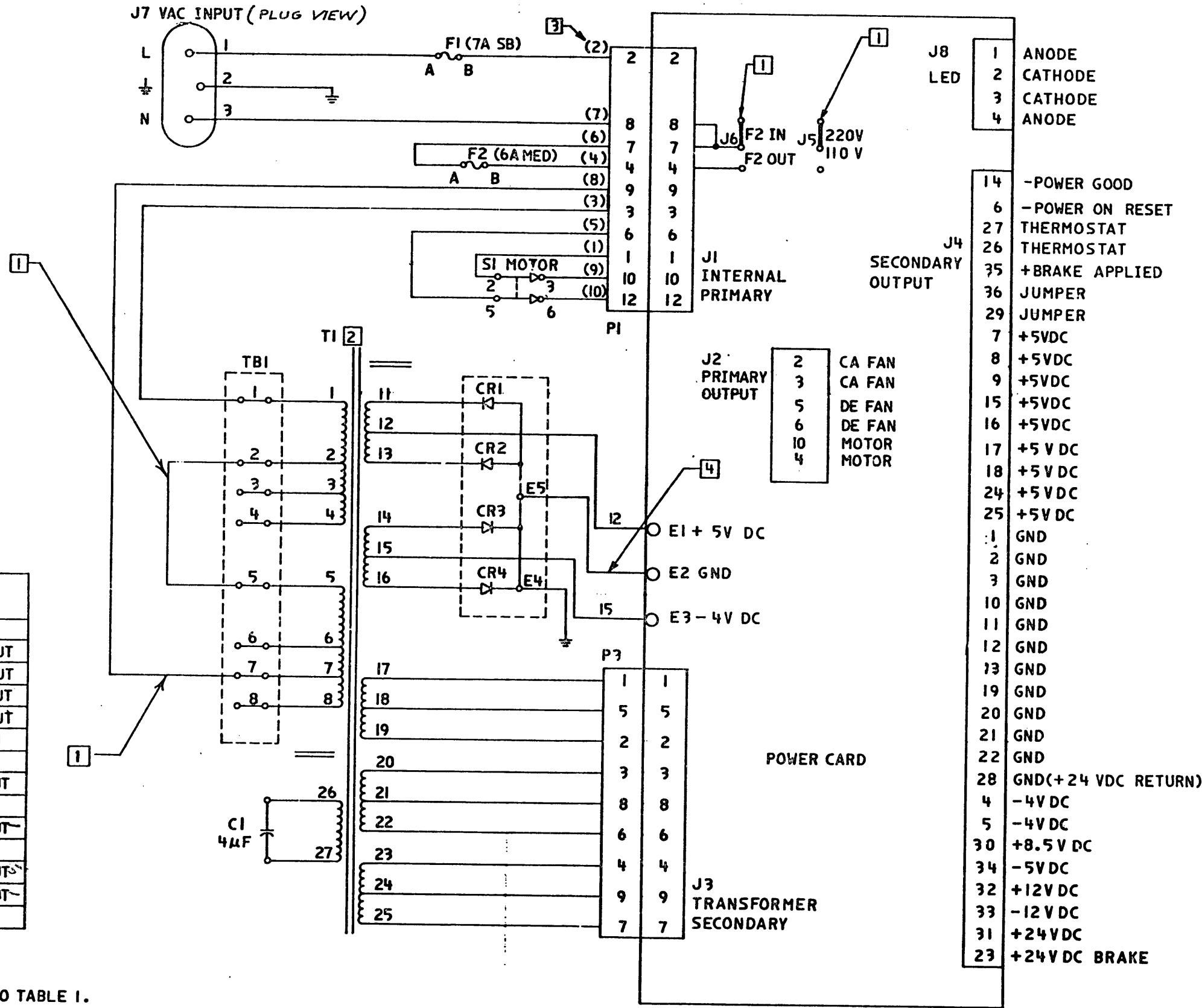


TABLE I  
ALTERNATE VOLTAGES

VOLTS	FREQ	TBI		J5	J6
		INPUT	JUMPER		
AC	Hz				
100	50,60	1-2	1-5,2-6	110V	F2 OUT
110	50,60	1-3	1-5,3-7	110V	F2 OUT
115	60	1-4	1-5,4-8	110V	F2 OUT
120	60	1-4	1-5,4-8	110V	F2 OUT
200	50,60	1-6	2-5	220V	F2 IN
208	60	1-7	2-5	220V	F2 IN
220	50	1-7	3-5	220V	F2 OUT
220	60	1-7	3-5	220V	F2 IN
<del>230</del>	<del>50</del>	<del>1-8</del>	<del>3-5</del>	<del>220V</del>	<del>F2 OUT</del>
<del>230</del>	<del>60</del>	<del>1-8</del>	<del>4-5</del>	<del>220V</del>	<del>F2 IN</del>
<del>235</del>	<del>50</del>	<del>1-8</del>	<del>4-5</del>	<del>220V</del>	<del>F2 OUT</del>
<del>240</del>	<del>50</del>	<del>1-8</del>	<del>4-5</del>	<del>220V</del>	<del>F2 OUT</del>
240	60	1-8	4-5	220V	F2 IN

1 WIRING SHOWN IS FOR 208V AC.  
FOR ALTERNATE VOLTAGES, REFER TO TABLE I.

2 TI (60Hz): P/N 4411333 REF OR P/N 6825363 REF  
TI (50Hz): P/N 4411334 REF OR P/N 6825364 REF

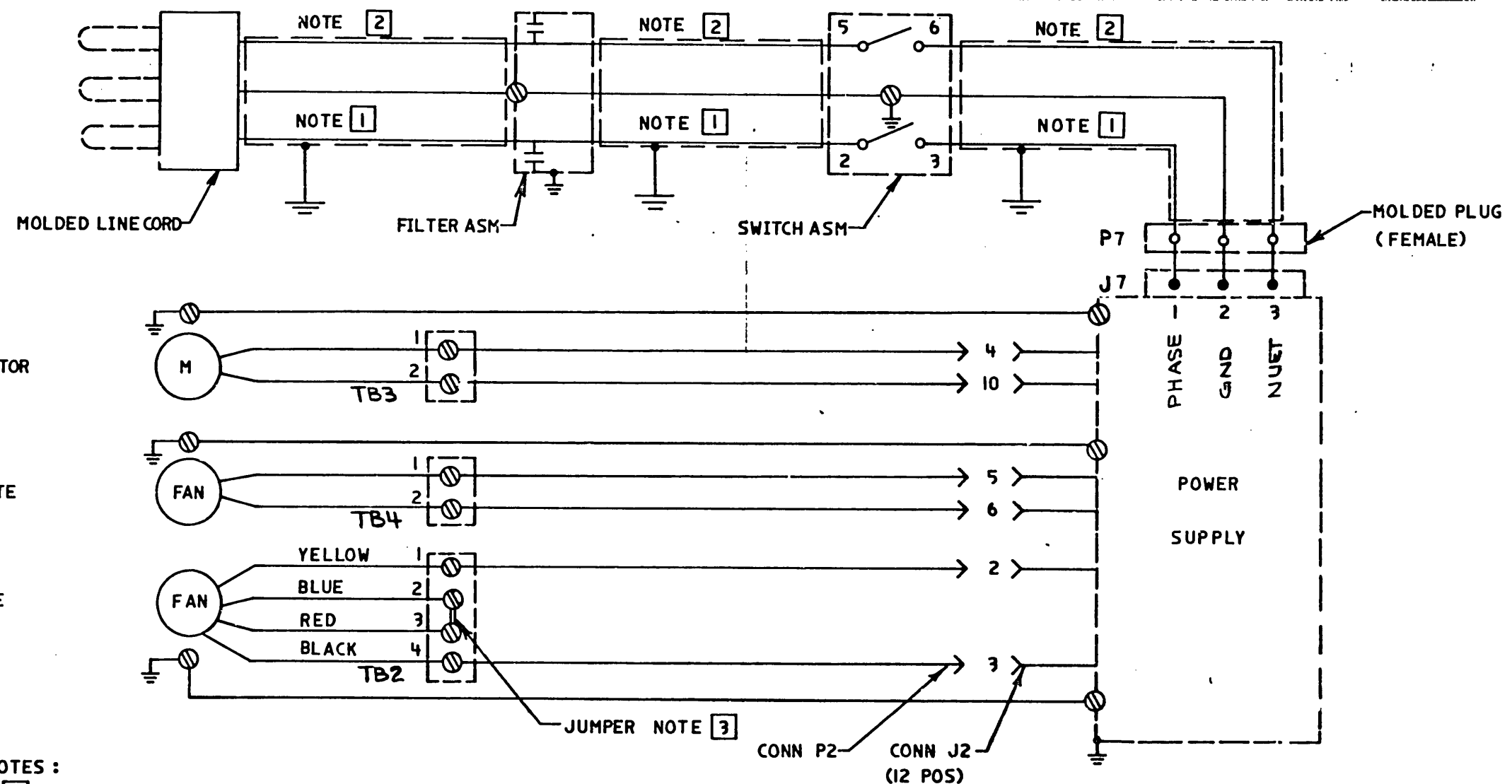
3 INTERNAL PRIMARY CABLE ASM WIRE NUMBERS

4 LARGE WIRE WITHOUT A WIRE NUMBER

EC HISTORY		DRAWING TITLE	
SEE EC	HISTORY	PWR SPLY INTERNAL WIRING	
2 FEB 79	375351	MACH 4963	
11 MAR 80	375662	PART NO 4411329	
D		CLASSIFICATION	IBM CORP

SF547

SF547



NOTES :

- 1 COLOR OF LEAD IS BLACK OR BROWN
- 2 COLOR OF LEAD IS WHITE OR LIGHT BLUE
- 3 JUMPER SHOWN FOR 220V CONNECTION. FOR 110V INSTALL JUMPERS BETWEEN POS 1 TO 2 AND 3 TO 4

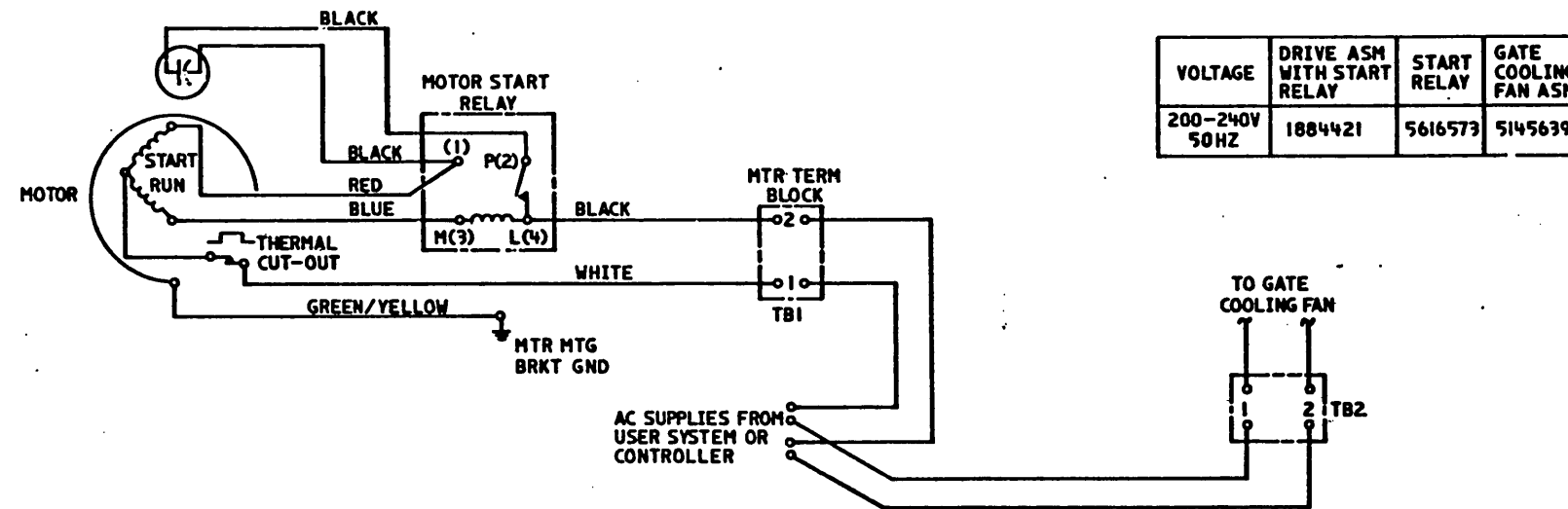
EC HISTORY		DRAWING TITLE	
31AUG78	374947	SCHEMATIC - PWR AC	
2 FEB79	375351	MACH 4963	
		PART NO 6837363	
C	CLASSIFICATION		IBM CORP

00FJ78

00FJ78

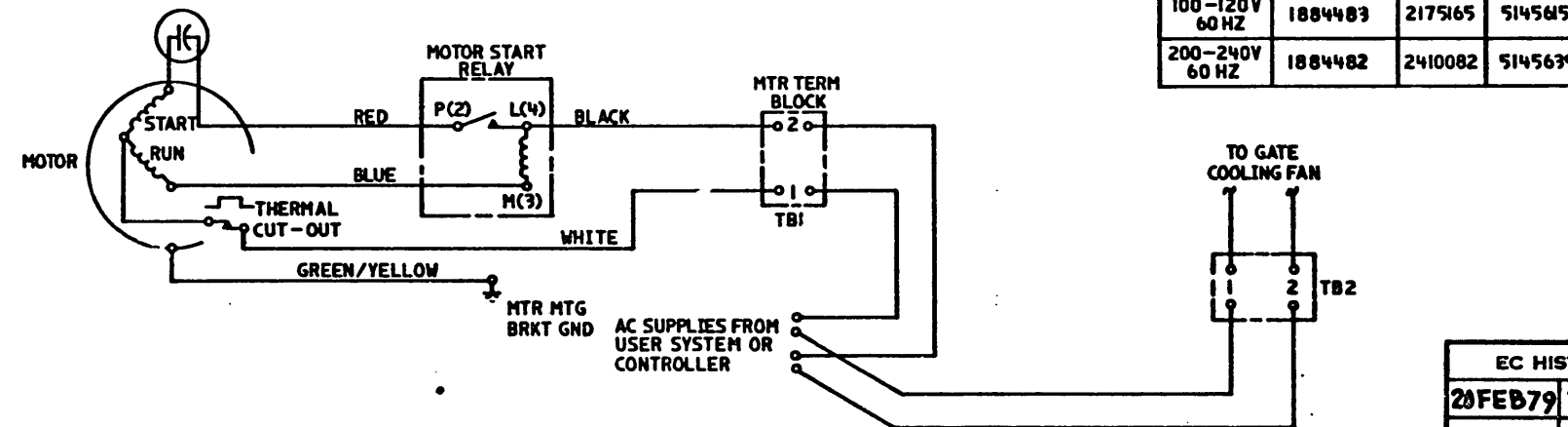


200-240V 50HZ



VOLTAGE	DRIVE ASM WITH START RELAY	START RELAY	GATE COOLING FAN ASM
200-240V 50 HZ	1884421	5616573	5145639

100-120V 60HZ  
200-240V 60HZ

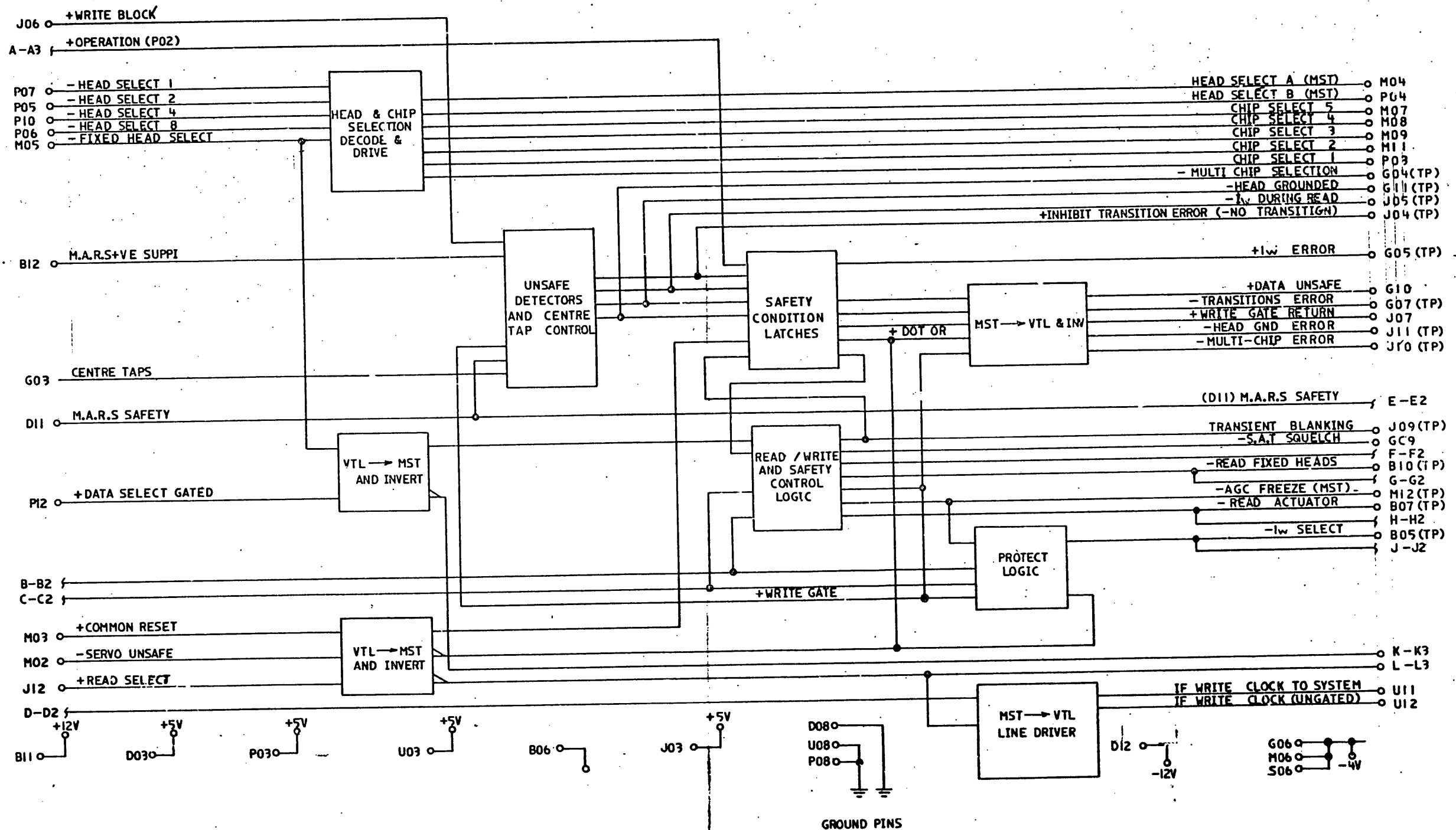


VOLTAGE	DRIVE ASM WITH START RELAY	START RELAY	GATE COOLING FAN ASM
100-120V 60 HZ	1884483	2175165	5145645
200-240V 60 HZ	1884482	2410082	5145639

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AC POWER TO DU	
		MACH 4963	
		PART NO 6839629	
		CLASSIFICATION	IBM CORP
C			

SHEET 6

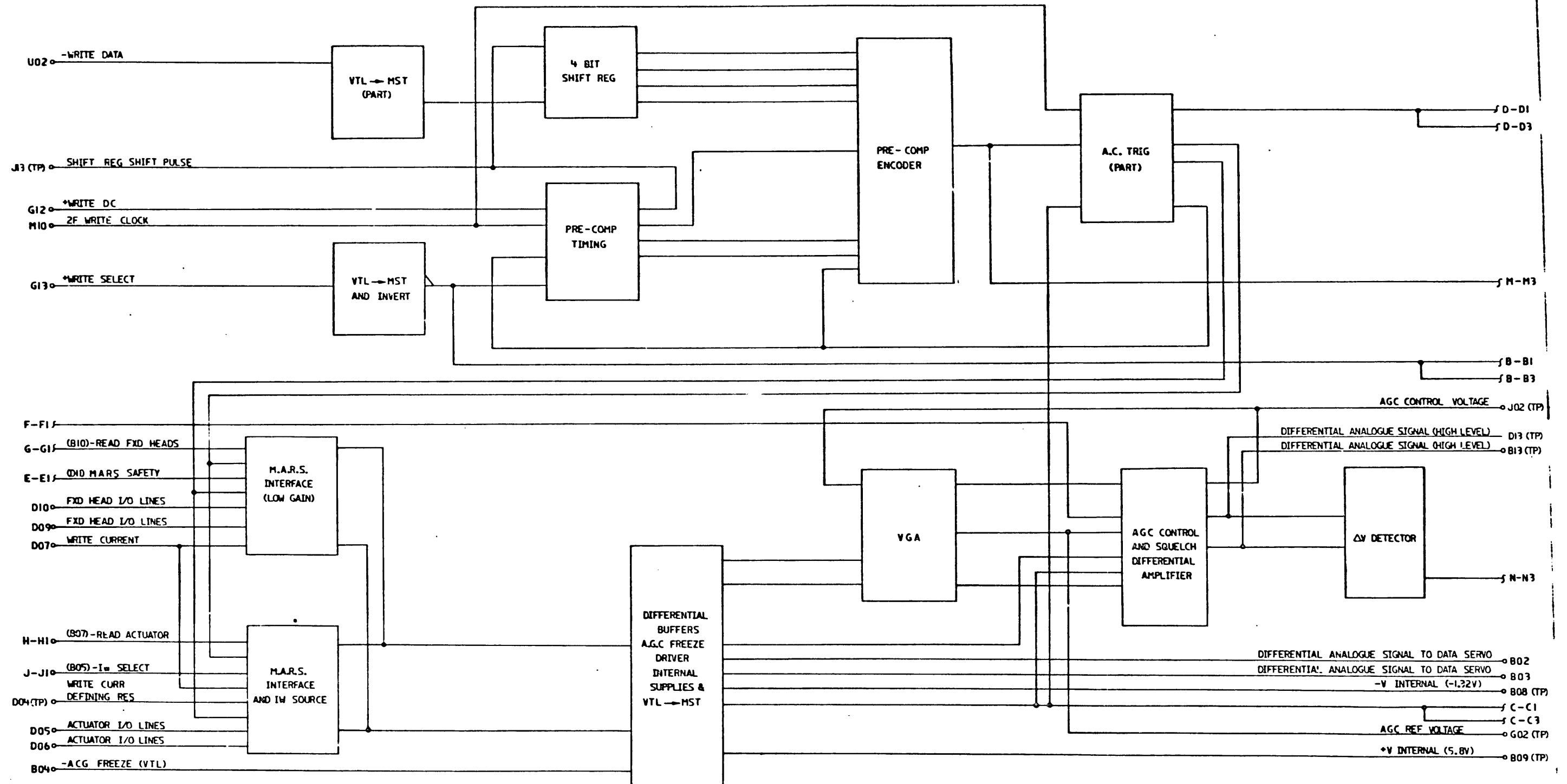
SHEET 6



EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIB2 DATA CHANNEL CARD	
		MACH 4963	
		PART NO 6839601	
		CLASSIFICATION	IBM CORP

D

312520

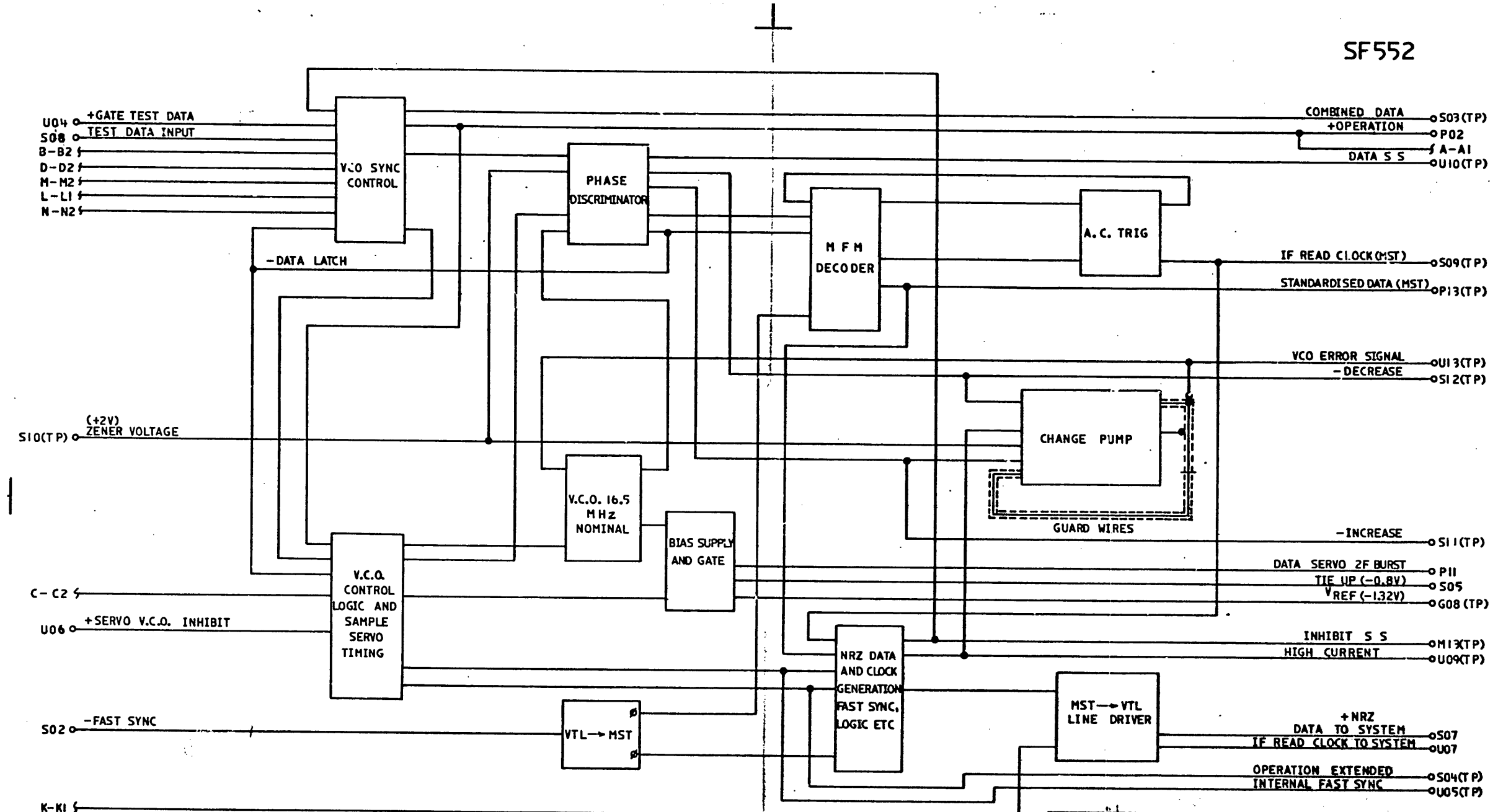


EC HISTORY		DRAWING TITLE	
20FEB79	375351	A1 B2 DATA CHANNEL CARD	
		MACH 4963	
		PART NO 6839602	
		CLASSIFICATION	IBM CORP

D

55551

SF552



N5J7T15

N5J7T15

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIB2 DATA CHANNEL CARD	
		MACH 4963	
		PART NO 6839603	
C		CLASSIFICATION	IBM CORP

AIB2 - DATA CHANNEL - INPUT

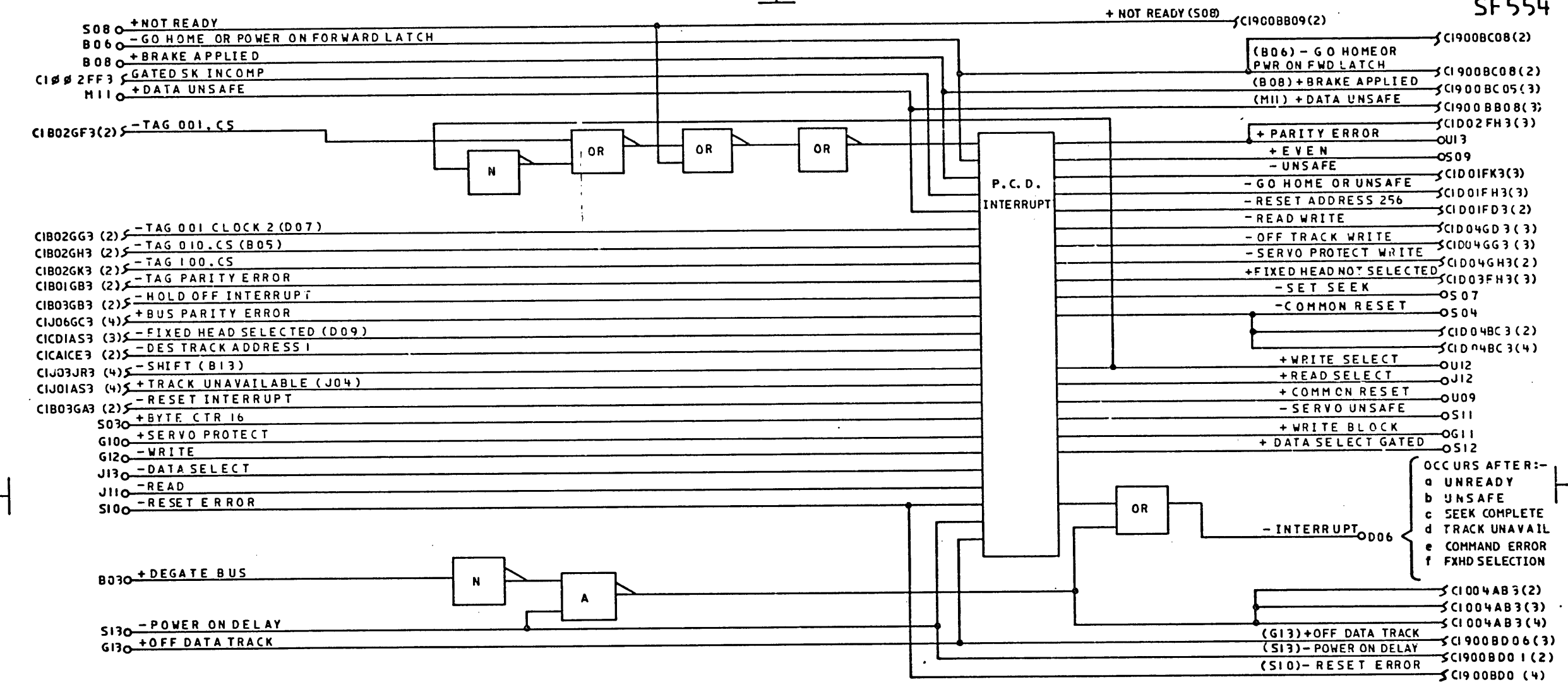
AIB2 - DATA CHANNEL - OUTPUT

PIN	LINE NAME	SOURCE	PAGE	PIN	LINE NAME	SYNC	PAGE
SF550	J06 + WRITE BLOCK	C2G11	SF554	SF550	M04 HEAD SEL A(MST)	A2B03 A1E13	SF527
	PU7 - HEAD SEL 1	C2P12	SF556		P04 HEAD SEL B(MST)	A2B04 A1C11	SF527
	P05 - HEAD SEL 2	C2P10	SF556		M07 CHIP SELECT 5	A1E11	SF527
	P10 - HEAD SEL 4	C2J06	SF556		M08 CHIP SELECT 4	A1B11	SF527
	P06 - HEAD SEL 8	C2G02	SF556		M09 CHIP SELECT 3	A2B02	SF527
	M05 - FIXED HEAD SEL	C2D09 (D1D13) (D2J04)	SF556		M11 CHIP SELECT 2	A2B05	SF527
	B12 M.A.R.S.	A2D03 (B1A13)	SF527		P09 CHIP SELECT 1	A2B06	SF527
	G03 CENTER TAPS	A2B08 (A1C13)	SF527		G09 -S.A.T. SQUELCH	F1B13	SF527
	D11 MARS SAFETY	A2B07 (B1D11)	SF527		U11 IF WRITE CLOCK	A5D12	SF503
	P12 + DATA SEL GATED	A2D02	SF527		U12 IF WRITE CLOCK	D2J05	SF564
	M03 + COMMON RESET	C2U09	SF554	SF551	B02 DIFF ANALOG SIG	E2B03	SF567
	M02 - SERVO UNSAFE	C2S11	SF554		B03 DIFF ANALOG SIG	E2D02	SF567
	J12 + READ SELECT	C2J12	SF554	SF552	P02 + OPERATION		TP
SF551	U02 - WRITE DATA	A5B10	SF503		P11 DATA SERVO 2F	E2G08	SF568
	G12 + WRITE D.C.	D1D11			S05 TIE UP		TP
	M10 2F WRITE CLOCK	E2G12	SF568		S07 + NRZ DATA	A5B08	TP
	G13 + WRITE SELECT	C2U12-E1C13	SF554		U07 IF READ CLOCK	A5D10	TP
	D10 FXD HDS I/O LINES	B1B13-E1R13	SF527	SF550	G10 + DATA UNSAFE	C2M11	SF554
	D09 FXD HDS I/O LINES	B1C13-E1B11	SF527		J07 + WRITE GATE RTN		TP
	D07 WRITE CURRENT	A2D07-A1D11	SF527		J05 + IN DURING READ		TP
	D05 ACTUATOR I/O LINES	A2D05-D1B13	SF527	SF552	S09 IF READ CLOCK		TP
	D06 ACTUATOR I/O LINES	A2D04-D1B11	SF527		P13 STANDARDIZED DATA		TP
	B04 - AGC FREEZE	C2G02-D2G08	SF556		S03 COMBINED DATA		TP
SF552	U04 + GATE TEST DATA		TP		U10 DATA SS		TP
	S08 TEST DATA INPUT		TP				
	U06 + SERVO VCO INHIBIT	E2G03	SF568				
	S02 - FAST SYNC	A5D05	SF503				

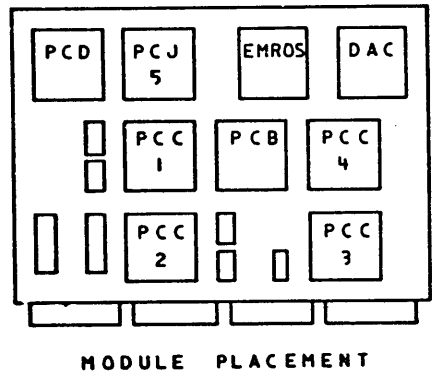
EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIB2 DATA CHANNEL	
11 MAR 80	375662	MACH 4963	
		PART NO 6839604	
C		CLASSIFICATION	IBM CORP

3 5 5 3

3 5 5 3



POWER SUPPLIES  
 +5V PINS D03, J03, P03, U03  
 GND PINS D08, J08, P08, U08  
 +12V PIN B11  
 -12V PIN D12

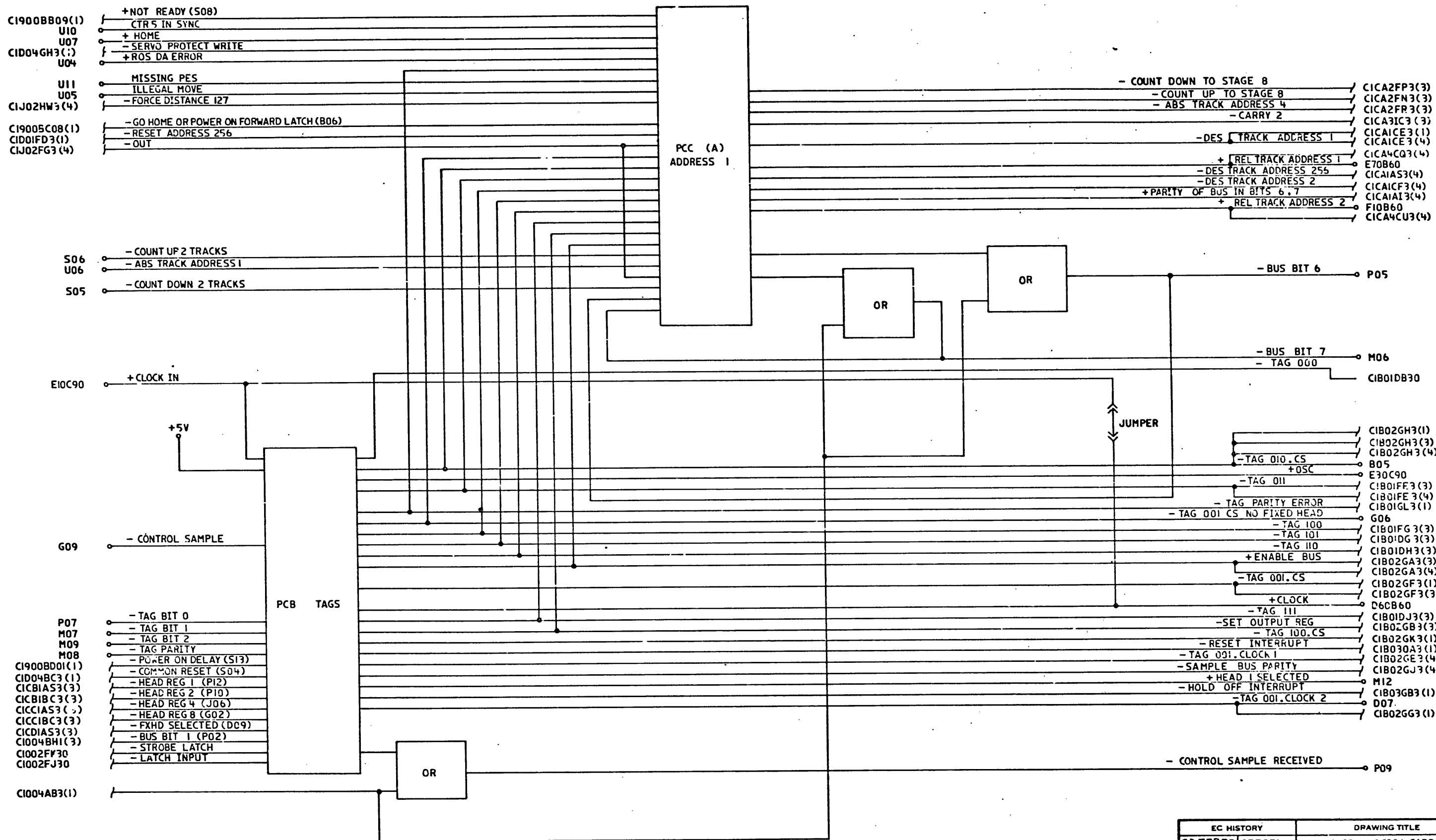


\* NOTE: SEE LOGIC PAGE SF585A FOR TAG DECODE INFORMATION

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIC2 LOGIC 1.	
		MACH 4963	
		PART NO 6839605	
C		CLASSIFICATION	IBM CORP

FJSTUS

SF554



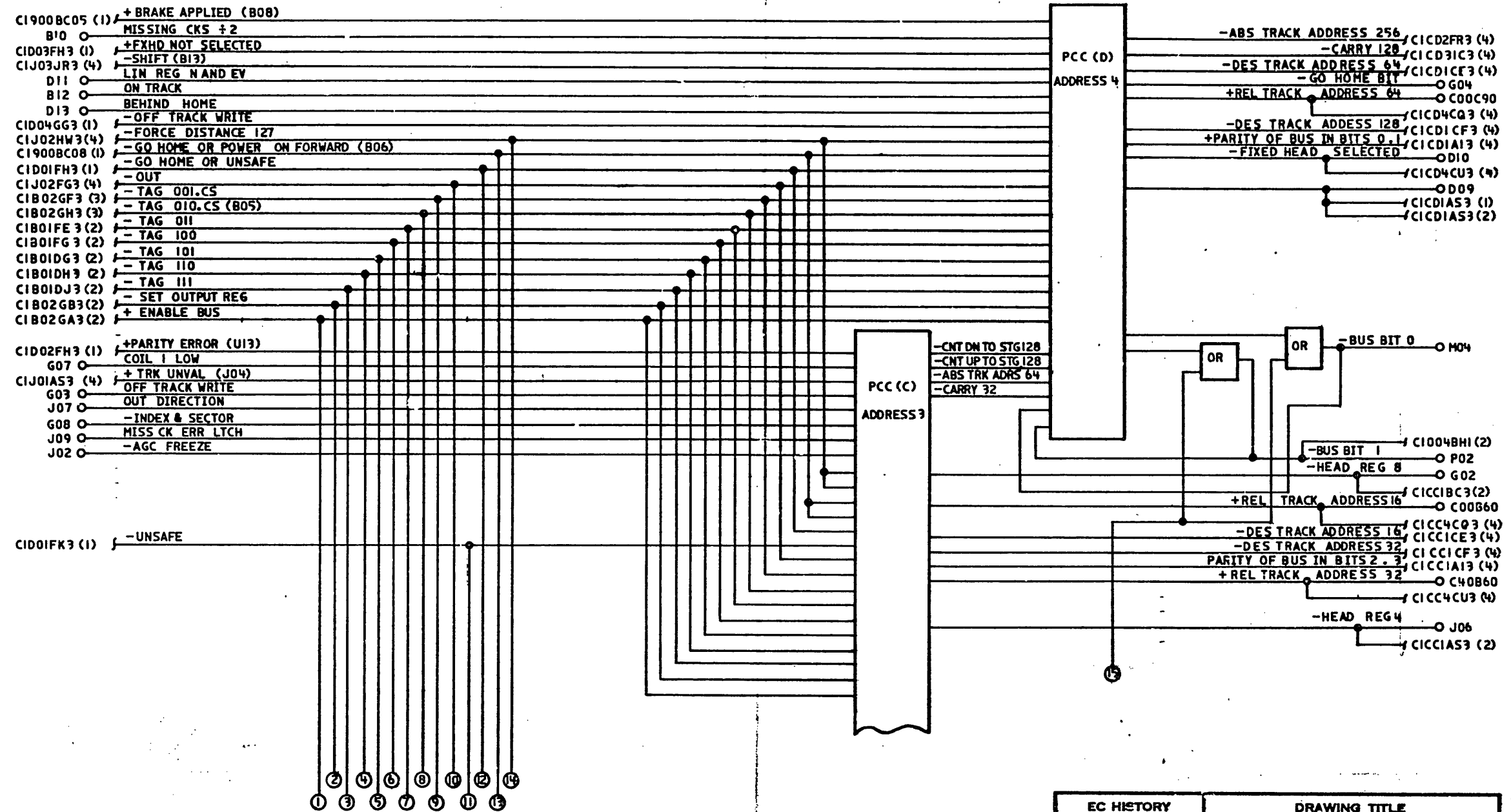
EC HISTORY		DRAWING TITLE	
20 FEB 79	375 351	AIC2 LOGIC 1 CARD	
		MACH 4963	
		PART NO 68 39606	
		CLASSIFICATION	IBM CORP

D

SUS

SUS

SF556A



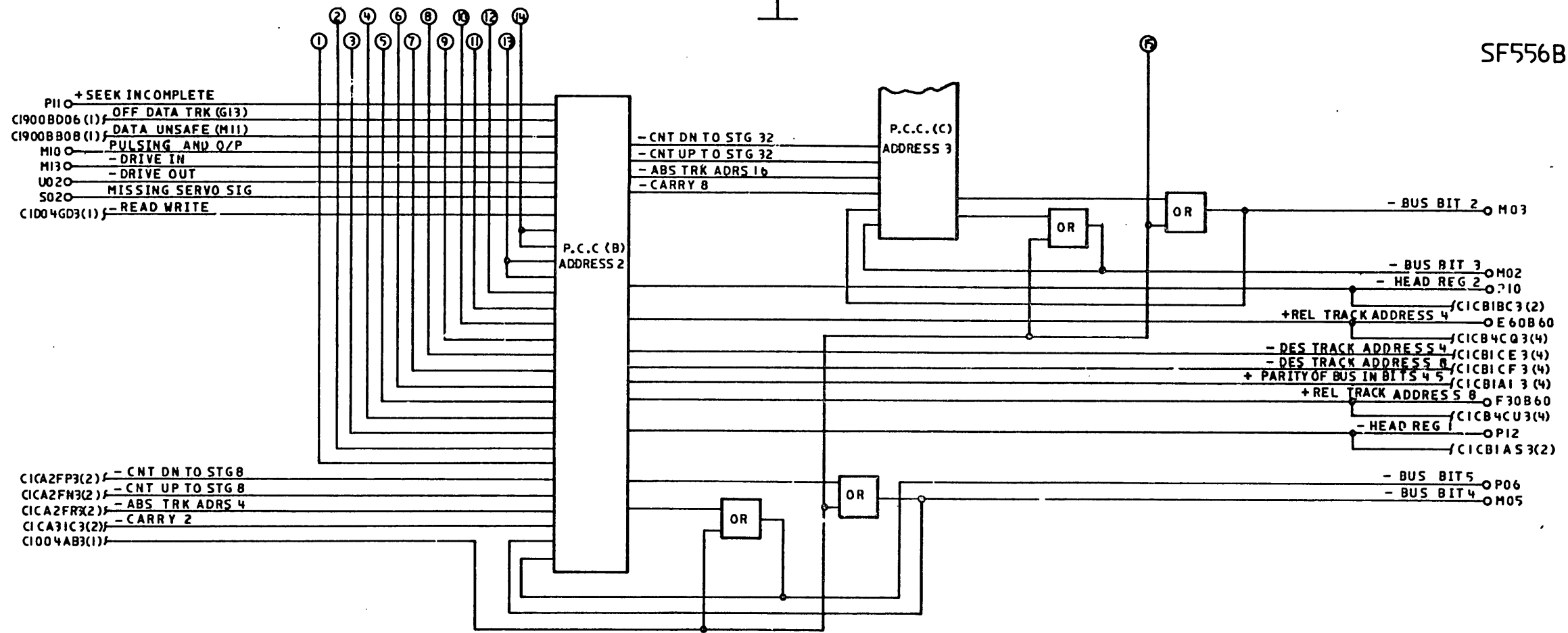
SF556A

SF556A

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIC2 LOGIC I	
		MACH 4963	
		PART NO 6839607	
C		CLASSIFICATION	IBM CORP



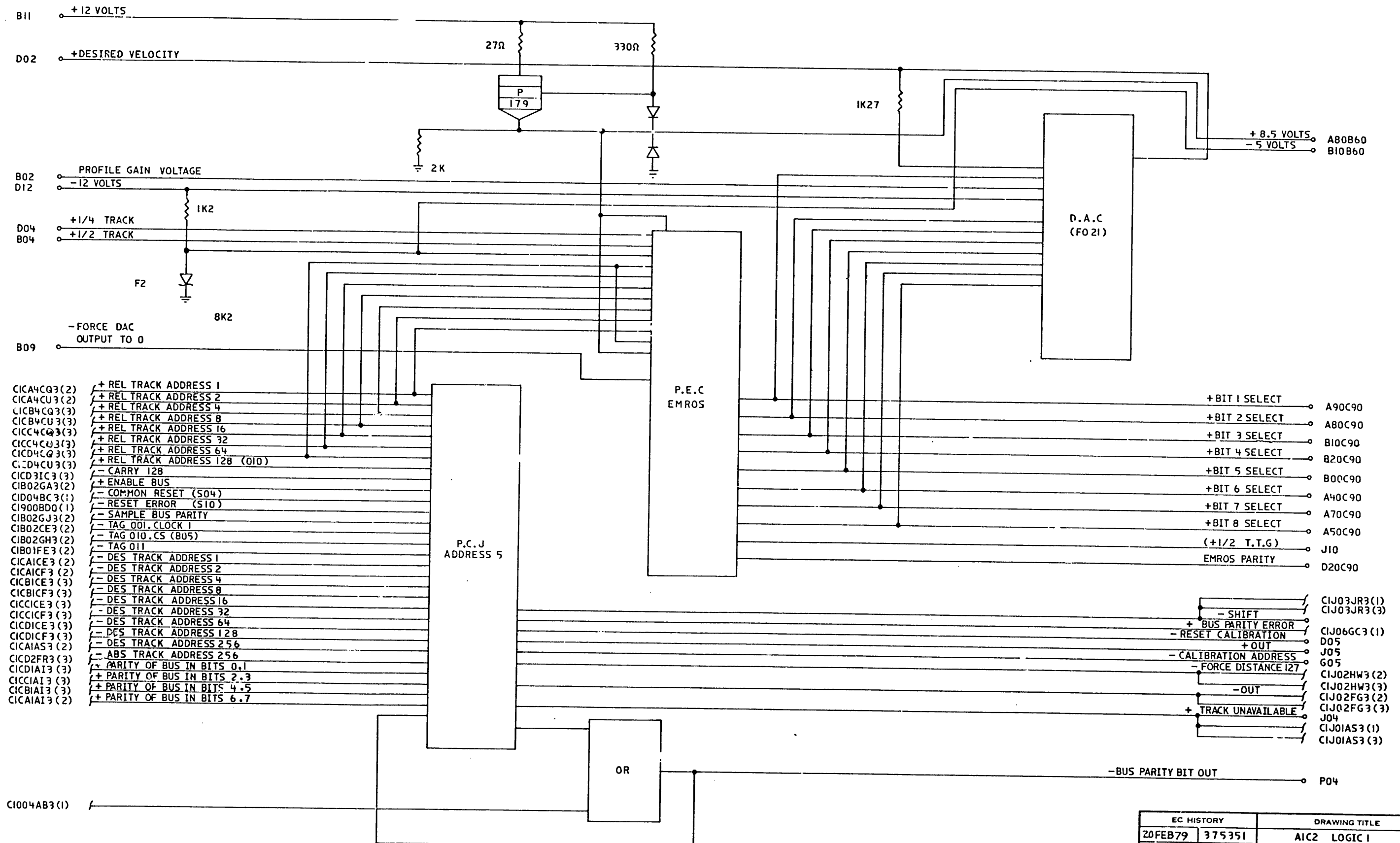
SF556B



B6-JJTUS

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIC2 LOGIC I	
		MACH 4963	
		PART NO 6839608	
C		CLASSIFICATION	IBM CORP

B6-JJTUS

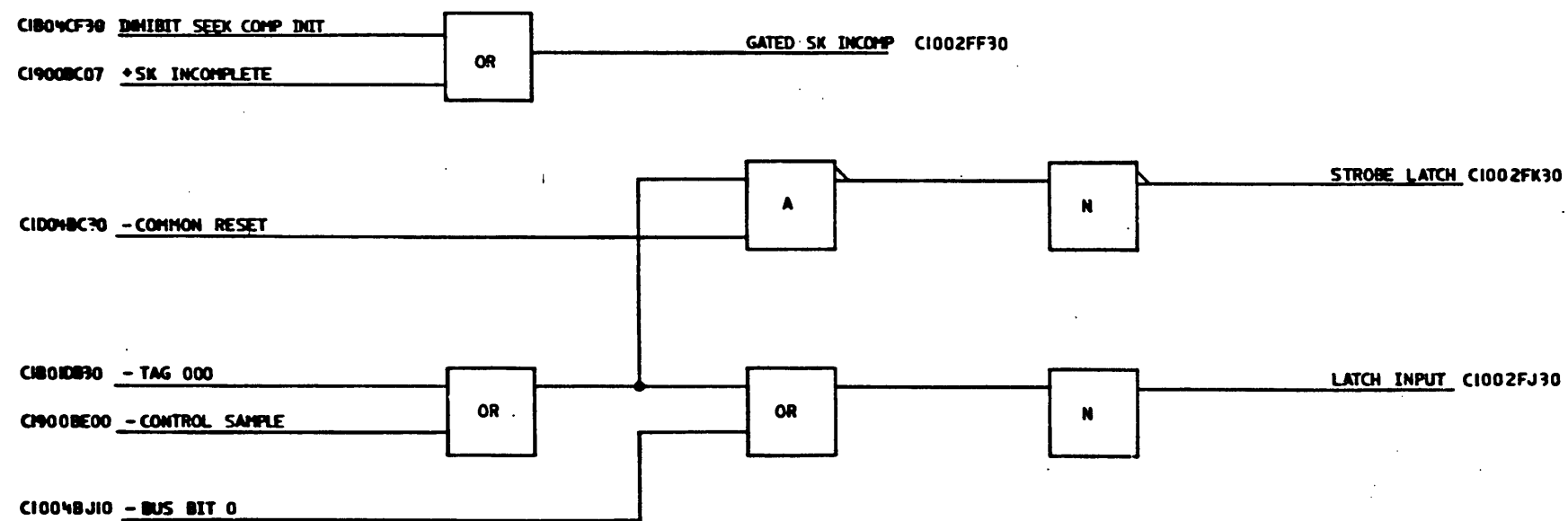


EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIC2 LOGIC 1	
11 MAR 80	375662	MACH 4963	
		PART NO 6839609	
		CLASSIFICATION	
		IBM CORP	

SF 557

D

SF558



EC HISTORY		DRAWING TITLE	
20FEB79	375351	A1C2 LOGIC 1	
		MACH 4963	
		PART NO 6839610	
<b>C</b>		CLASSIFICATION	<b>IBM</b> CORP

8 5 5 7 1 5

8 5 5 7 1 5

SF559A

AIC2 - LOGIC 1 - INPUT

AIC2 - LOGIC 1 - INPUT

PIN	LINE NAME	SOURCE	PAGE	PIN	LINE NAME	SOURCE	PAGE
SF554 S08	+NOT READY	D2M07	SF562	SF556 D11	LINE REG N + EV	D2B03	SF560
B06	-GO HOME	D2U10	SF562	B12	ON TRACK	F2G12 (E2G13)	SF570 (SF568)
B08	+BRAKE APPLIED	F2M02 (D2P07)	SF570 (SF563)	D13	BEHIND HOME	D2U11	SF565
M11	+DATA UNSAFE	B2G10	SF550	G07	COIL LOW	F2G03	SF570
S03	+BYTE CTR 16	D2S08	SF565	G03	OFF TRACK WRITE	E2D09	SF567
G10	+SERVO PROTECT	D2U06	SF563	J07	OUT DIRECTION	F2S13 (D2D06)	SF570 (SF562)
G12	-WRITE	A5D11	SF503	G08	-INDEX AND SECTOR	D2P05	SF563
J13	-DATA SELECT	A5D04	SF503	J09	MISS CK ERR LCH	D2M03	SF563
J11	-READ	A5D09	SF503	J02	-AGC FREEZE	D2G09 (B2B04)	SF565 (SF551)
S10	-RESET ERROR	A5D06 (D2P13)	SF503 (SF563)	P11	+SEEK INCOMPLETE	F2S07 (D2J13)	SF570 (SF563)
B03	+DEGATE BUS	A5D12	SF503	M10	PULSING AND O/P	D2M04	SF563
S13	-POWER ON DELAY	F2P02 (D2U09)	SF570 (SF563)	M13	-DRIVE IN	F2P11 (D2S07)	SF570 (SF565)
G13	+OFF DATA TRACK	E2J13 (E1A11)	SF568 (SF510)	U02	-DRIVE OUT	F2S13 (D2U07)	SF570 (SF565)
				S02	MISSING SERVO SIG	D2M02	SF563
SF555 U10	CRT 5 IN SYNC	D2G07	SF562				
U07	+HOME	D2P10	SF562	SF557 D02	+DESIRED VELOCITY	D2B02	SF561
U04	+ROS ERROR	D2D09	SF565	B02	PROFILE GAIN VOLTAGE	D2B08	SF562
U11	MISSING PES	F2J04	SF570				
U05	ILLEGAL MOVE	D2P04	SF563	D04	+1/4 TRACK	D2B10	SF560
S06	-COUNT UP 2 TRACKS	D2D05	SF560	B04	+1/2 TRACK	D2D10	SF560
U06	-ABS TRK ADDRESS 1	D2B05	SF560				
S05	-COUNT DN 2 TRACKS	D2D07	SF560				
G09	-CONTROL SAMPLE	A5B03	SF503				
P07	-TAG BIT 0	A4B02 (A3B02)	SF505				
M07	-TAG BIT 1	A4B03 (A3B03)	SF505				
M09	-TAG BIT 2	A4B04 (A3B04)	SF505				
M08	-TAG PARITY	A4B05 (A3B05)	SF505				

SF559A

SF559A

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIC2 LOGIC 1	
		MACH 4963	
		PART NO 6839611	
C		CLASSIFICATION	IBM CORP

AIC2 - LOGIC I - OUTPUT

PIN	LINE NAME	SYNC	PAGE
SF554	UI3 + PARITY ERROR	-	TP
	S09 +EVEN	- F2B03 (E2J06)	SF570 (SF568)
	S07 -SET SEEK	- D2M12	SF562
	S04 - COMMON RESET	-	TP
	UI2 + WRITE SELECT	-B2G13 (E1C13)	SF 551
	J12 +READ SELECT	-B2J12 (F1C11)	SF 550
	U09 +COMMON RESET	-B2M03	SF 550
	S11 - SERVO UNSAFE	-B2M02	SF 550
	G11 + WRITE BLOCK	-B2J06	SF 550
	S12 + DATA SFL GATED	-A2B13	SF527
	D06 - INTERRUPT	-A5B04	SF503
SF555	P05 -BUS BIT 6	-A4D11 (A3D11)	SF (SF505)
	M06 -BUS BIT 7	-A4D12 (A3D12)	SF (SF505)
	B05 -TAG 010 CS	-	TP
	G06 - TAG NO FIXED HEAD	-	TP
	M12 + HEAD I SELECTED	- D2P09	SF 562
	D07 - TAG CLOCK 2	- D2509	SF 565
	P09 - CONT SAMPLE REC'D	- A3B12	SF505

AIC2 LOGIC I - OUTPUT

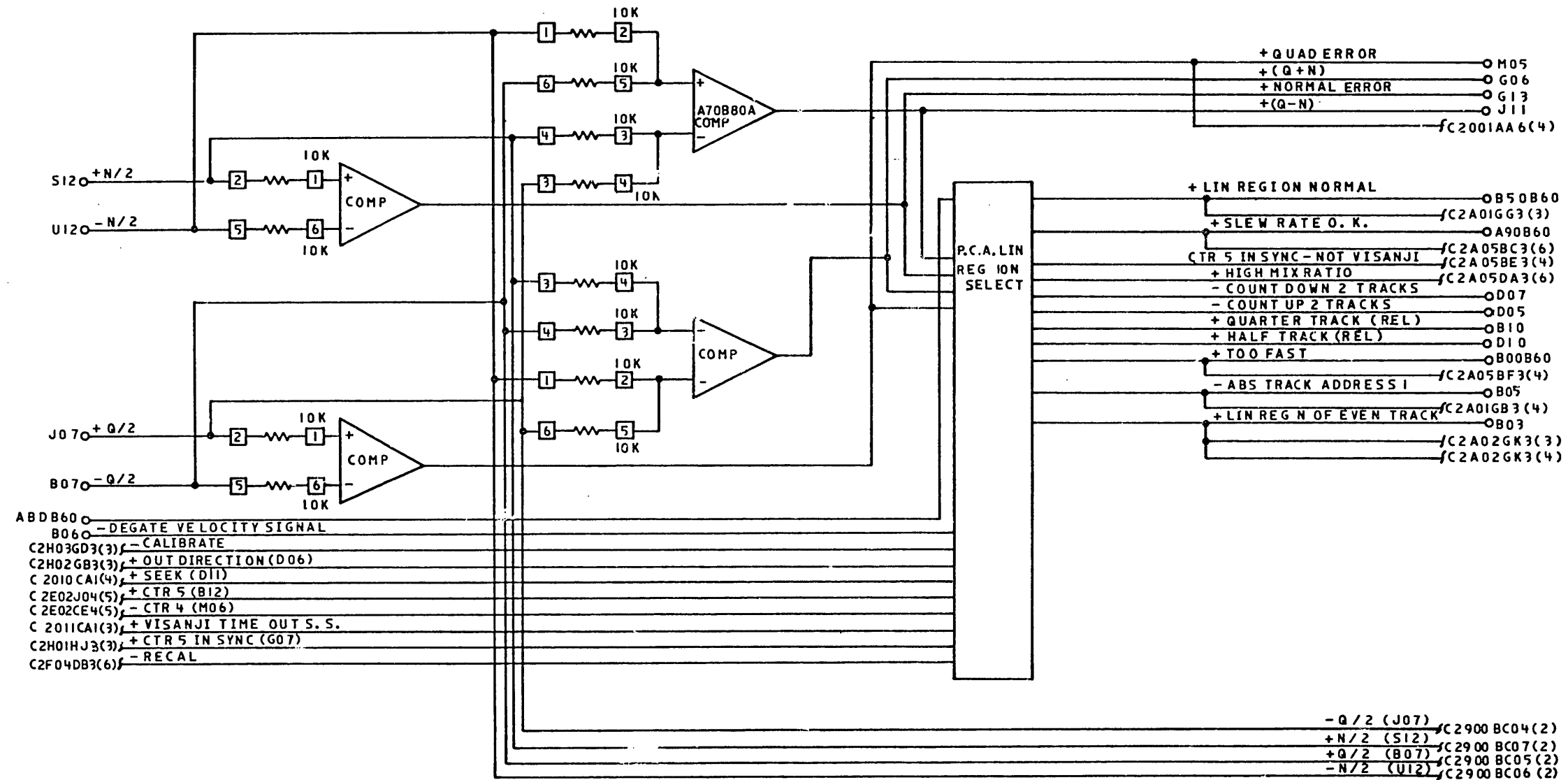
PIN	LINE NAME	SYNC	PAGE
SF556	G04 - GO HOME BIT	- D2 P12	SF562
	D10 + REL TRK ADDRESS	-	TP
	D09 - FIXED HEAD SEL	-D2J04 (B2M05)	SF565 (SF550)
	M04 -BUS BIT 0	-A4D04 (A3D04)	SF505
	P02 -BUS BIT 1	-A4D05 (A3D05)	SF505
	G02 -HEAD REG 8	-B2F06	SF 550
	J06 -HEAD REG 4	-B2P10	SF 550
	M03 -BUS BIT 2	-A4D06 (A3D06)	SF505
	M02 -BUS BIT 3	-A4D07 (A3D07)	SF505
	P10 -HEAD REG 2	-B2P05	SF 550
	P12 -HEAD REG 1	-B2P07	SF 550
	P06 -BUS BIT 5	-A4D10 (AD10)	SF505
	M05 -BUS BIT 4	-A4D09 (A3D09)	SF505
SF557	J10 + 1/2 TTG		
	B13 - SHIFT	-D2504	SF565
	D05 - RESET CAL	-D2P11	SF 562
	J05 +OUT	-D2U02	SF 562
	G05 - CAL ADDRESS	-D2M08	SF 562
	J04 +TRACK UNAVAILABLE	-	TP (SF557)
	P04 - BUS PARITY BIT OUT	-A4D13 (A3D13)	SF505

B 9 J J T T S

B 9 J J T T S

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIC2 LOGIC I	
11 MAR 80	375662	MACH 4963	
		PART NO 6839612	
C		CLASSIFICATION	IBM CORP

SF560



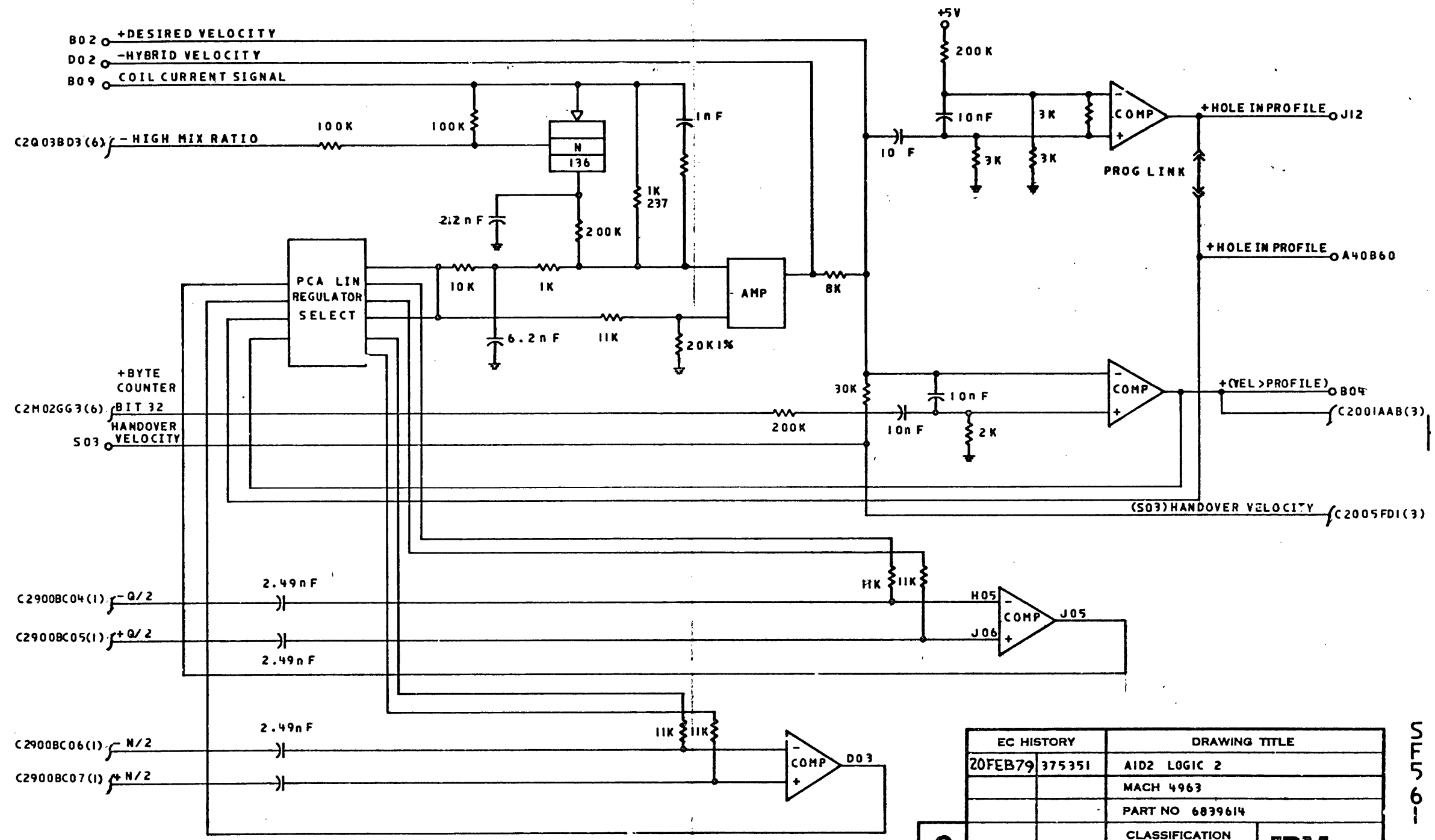
- ABDB60 - DEGATE VELOCITY SIGNAL
- B06 - CALIBRATE
- C2H03GD3(3) - CALIBRATE
- C2H02GB3(3) - OUT DIRECTION (D06)
- C 2010 CA1(4) - SEEK (D11)
- C 2E02J04(5) - CTR 5 (B12)
- C 2E02CE4(5) - CTR 4 (M06)
- C 2011CA1(3) - VISANJI TIME OUT S. S.
- C2H01HJ3(3) - CTR 5 IN SYNC (G07)
- C2F04DB3(6) - RECAL

POWER SUPPLIES  
 +5V D03, J03, P03, U03  
 GND D08, J08, P08, U08  
 -12V D12  
 +12V B11  
 +24V J02

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AID2 LOGIC 2	
11 MAR 80	375662	MACH 4963	
		PART NO 6839613	
C	CLASSIFICATION		IBM CORP

06575

06575

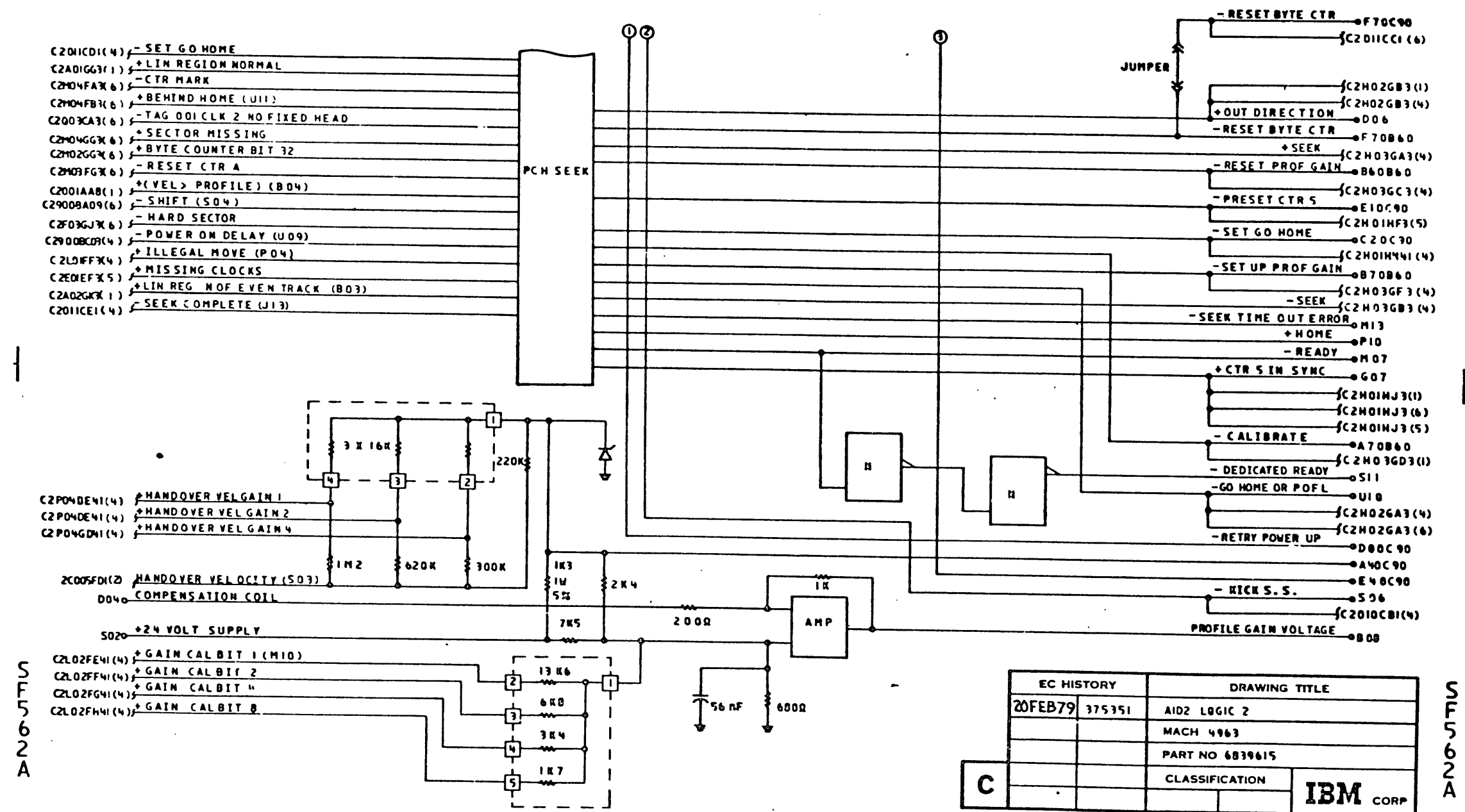


EC HISTORY		DRAWING TITLE	
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		MACH 4963	
		PART NO 6839614	
		CLASSIFICATION	
<b>C</b>			<b>IBM</b> CORP

SHEET 6

SHEET 6

SF562A

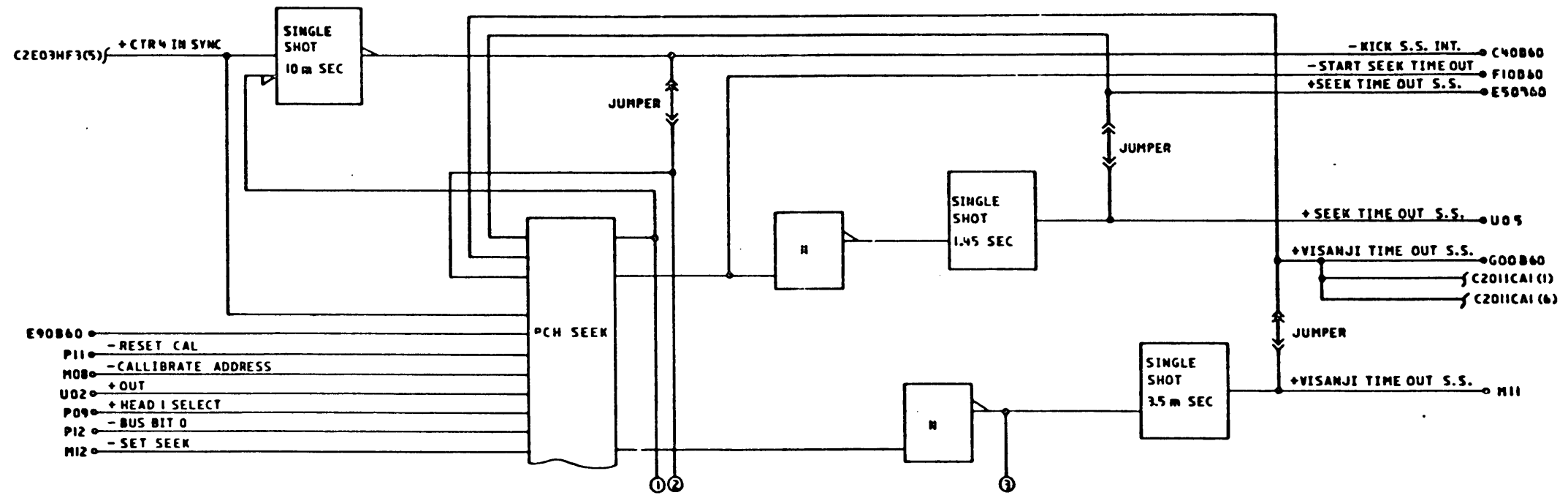


EC HISTORY		DRAWING TITLE	
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		MACH 4863	
		PART NO 6839615	
		CLASSIFICATION	
		<b>IBM</b> CORP	

SF562A

SF562A

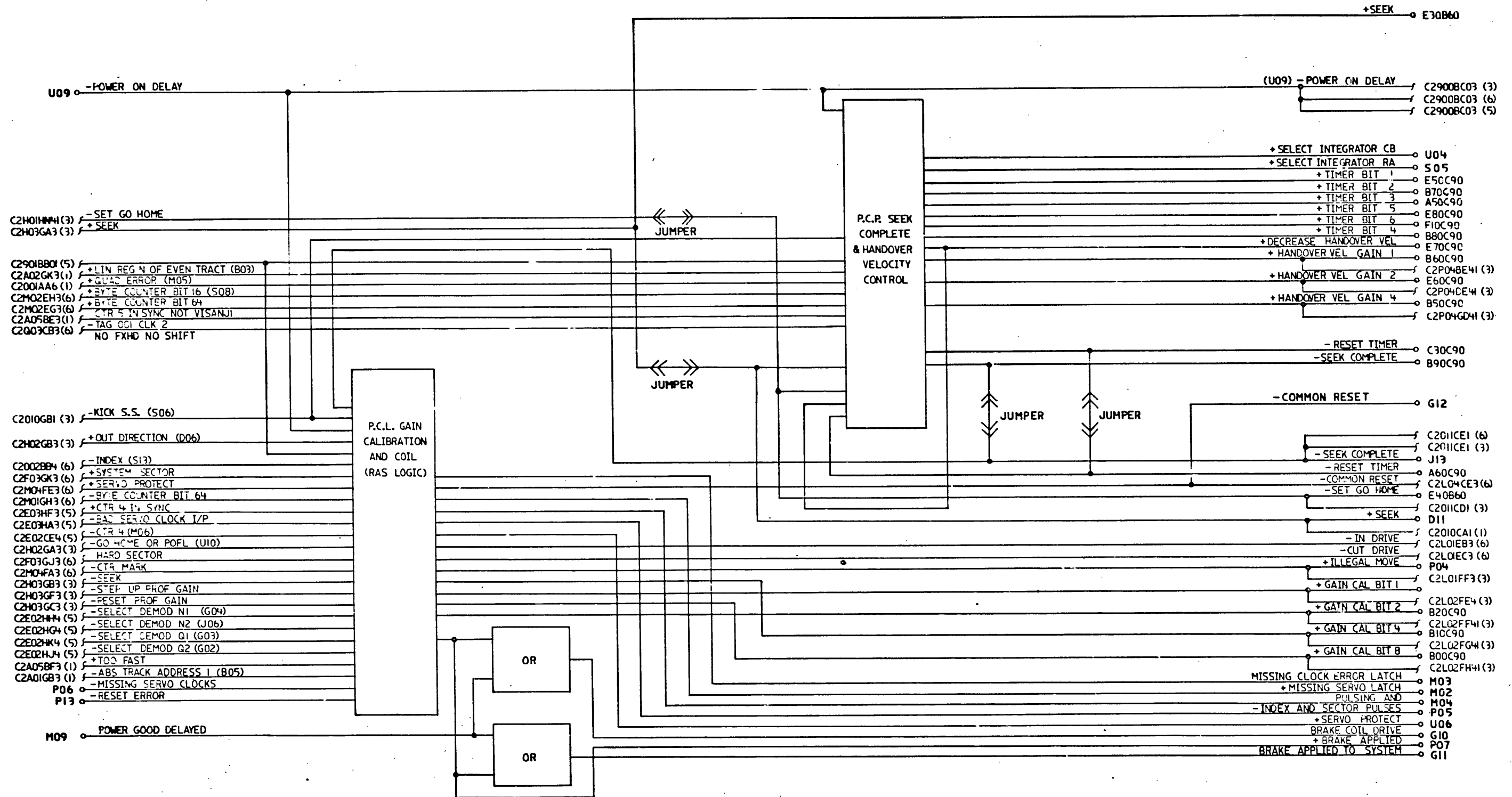




BNSJTS

SFTS2B

EC HISTORY		DRAWING TITLE	
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		MACH 4963	
		PART NO 6839616	
C		CLASSIFICATION	IBM CORP

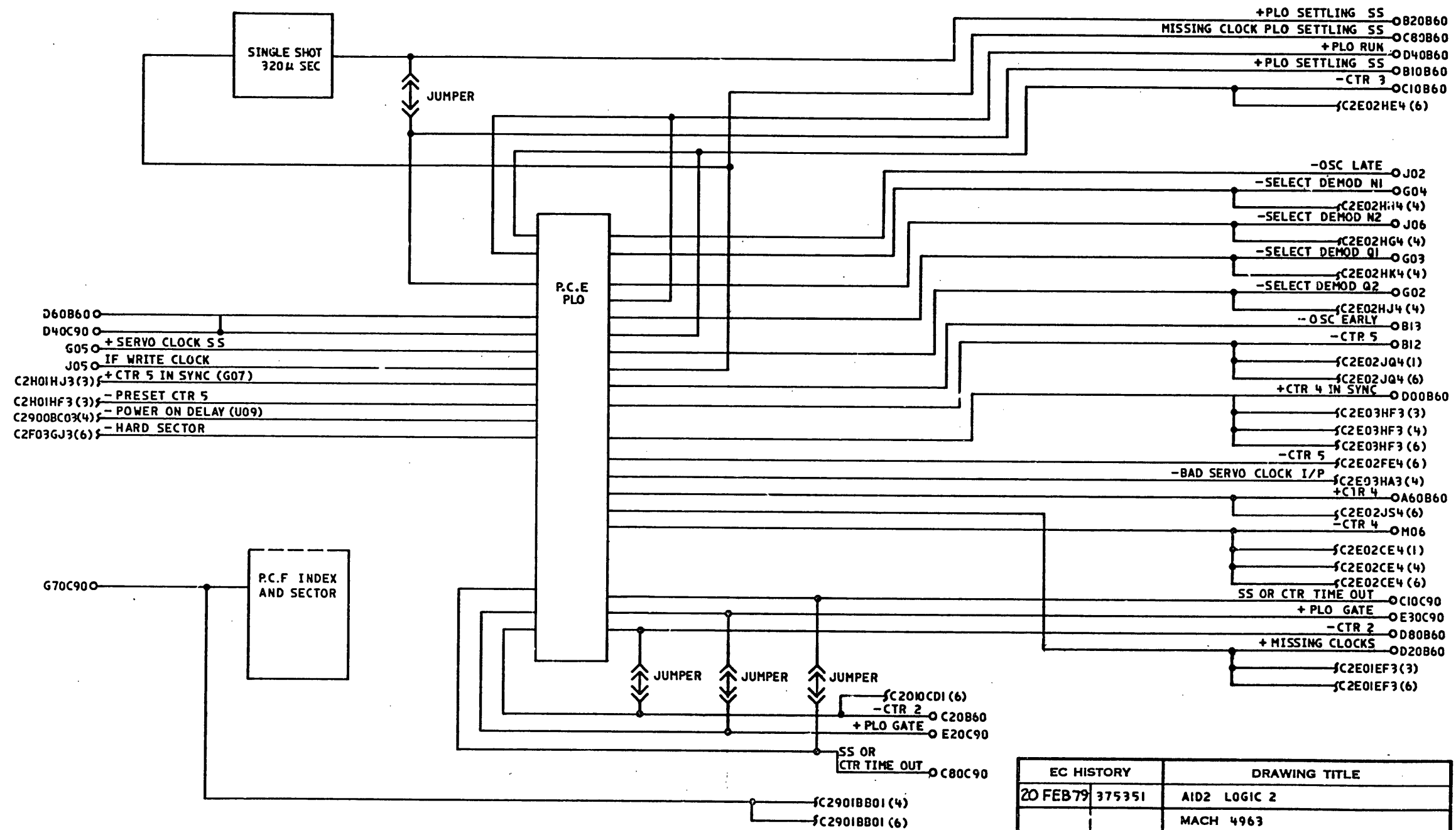


EC HISTORY		DRAWING TITLE	
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		MACH 4963	
		PART NO 6839617	
		CLASSIFICATION	IBM CORP
D			

30575

30575

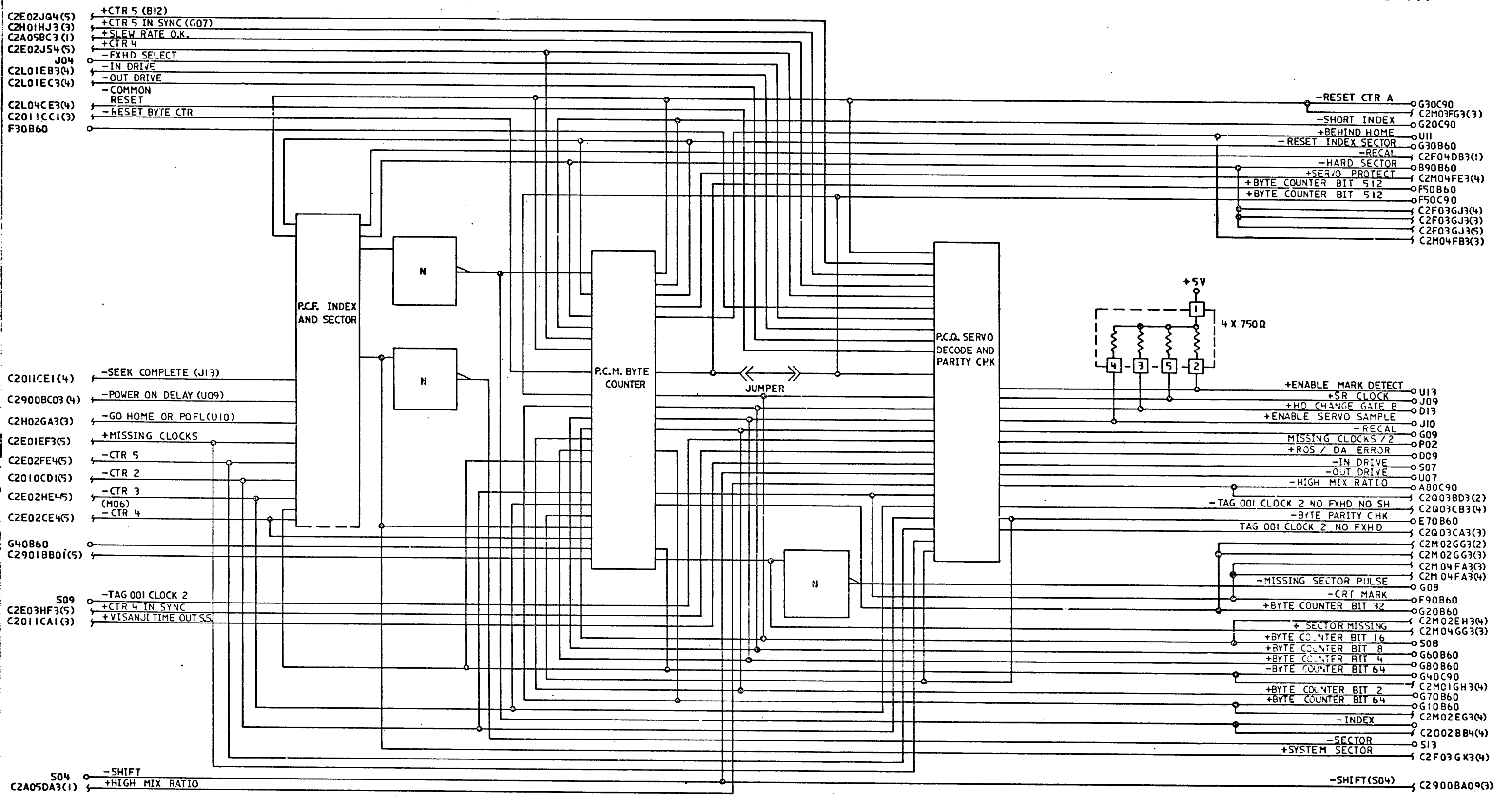
SF564



F05TUS

F05TUS

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	A1D2 LOGIC 2	
		MACH 4963	
		PART NO 6839618	
C		CLASSIFICATION	IBM CORP



EC HISTORY		DRAWING TITLE	
20FEB79	375351	A1 D2 LOGIC 2	
		MACH 4963	
		PART NO 6839619	
		CLASSIFICATION	IBM CORP

56515

56515

AID2-LOGIC 2-INPUT

	PIN	LINE NAME	SOURCE	PAGE
SF560	S12	+ N/2	- F2D13	SF570
	U12	- N/2	- F2M08	SF570
	J07	+ Q/2	- F2S02	SF570
	B07	- Q/2	- F2D11	SF570
	B06	-DEGATE VELOCITY SIG	-	TP
SF561	B02	+DESIRED VELOCITY	-C2D02	SF557
	D02	-HYBRID VELOCITY	-	TP
	B09	COIL CURRENT	-F2S10	SF570
	S03	HANDOVER VELOCITY	-	TP
SF562	P11	-RESET CALIBRATION	-C2D05	SF557
	M08	-CALIBRATE ADDRESS	-C2G05	SF557
	U02	+OUT	-C2J05	SF557
	P09	+HD SEC 1	-C2M12	SF555
	P12	-BUS BIT 0	-C2G04	SF556
	M12	-SET SEEK	-C2S07	SF554
	D04	COMPENSATION COIL	-E4A14	
	S02	+24 VOLTS	-F2G02 (B5E14)(E5A14)	SF570
SF563	U09	-POWER ON DELAY	-F2P02(C2S13)	SF570(SF554)
	P06	-MISSING SERVO CLOCKS	-F2G13	SF570
	P13	-RESET ERROR	-A5D06(C2S10)	SF 503(SF554)
	M09	POWER GOOD DELAYED	-F2P09	SF 570
SF564	G05	+SERVO CLOCK S.S.	-F2B04	SF 570
	J05	IF WRITE CLOCK	-B2U12	SF550
SF565	J04	-FIXED HEAD SELECT	-C2D09 (B2M05)(D1D13)	SF556 (SF550)
	S09	-TAG CLOCK 2	-C2D07	SF 555
	S04	-SHIFT	-C2B13	SF557

AID2-LOGIC 2-OUTPUT

	PIN	LINE NAME	SYNC	PAGE
SF560	M05	+ QUAD ERROR		TP
	G06	+(Q+N)		TP
	G13	+NORMAL ERROR	-F2B12	SF570
	J11	+(Q-N)		TP
	D07	-COUNTDN 2 TKS	-C2S05	SF555
	D05	-COUNTUP 2 TKS	-C2S06	SF555
	B10	+ QUARTER TK	-C2D04	SF557
	D10	+ HALF TRACK	-C2B04	SF557
	B05	- ABS TK ADDRESS !	-C2U06	SF555
	B03	+ LINREG N EVEN TK	-C2D11	SF556
SF561	J12	+ HOLE IN PROFILE		TP
	B04	+(VEL> PROFILE)		TP
SF562	V05	+ SEEK TIME OUT S.S.		
	M11	TIME OUT S.S.		
	D06	+OUT DIRECTION	-C2J07(F2513)	SF556(SF570)
	M13	-SEEK TIME OUT ERROR		TP
	P10	+HOME	-C2U07	SF555
	M07	-READY	-C2S08	SF555
	G07	+CTR 5 IN SYNC	-C2U10	SF555
	S11	-DEDICATED READY		TP
	U10	-GO HOME OR PRO	-C2B06	SF554
	S06	-KICK S.S.		TP
B08	PROFILE GAIN VOLTAGE	-C2B02	SF557	

SF566A

SF566A

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AID2 LOGIC 2	
11MAR80	375662	MACH 4963	
		PART NO 6839620	
C		CLASSIFICATION	IBM CORP

SF566B

AID2 - LOGIC 2 - OUTPUT

AID2 - LOGIC 2 - OUTPUT

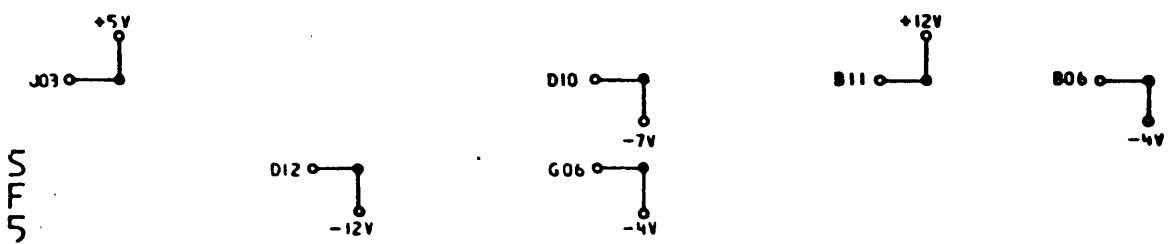
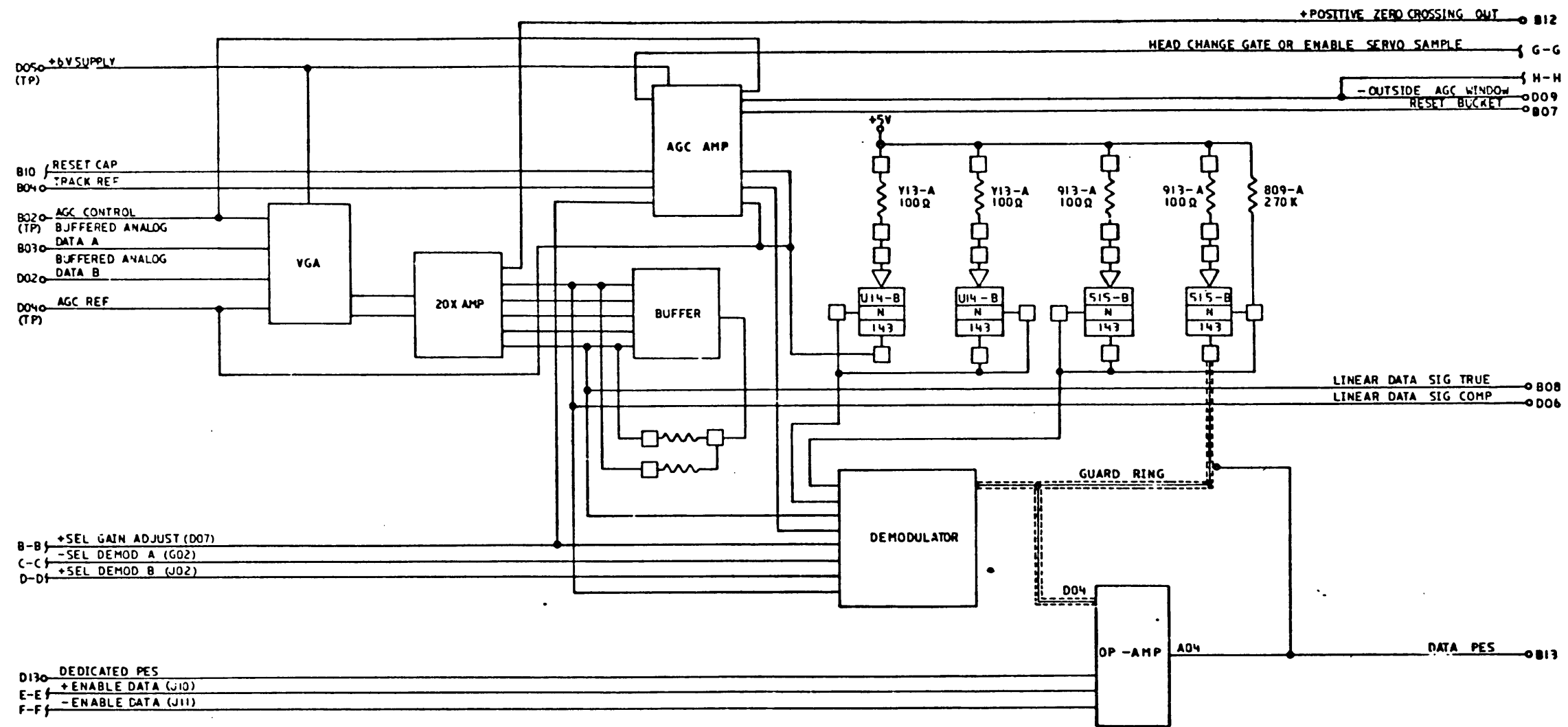
PIN	LINE NAME	SYNC	PAGE	PIN	LINE NAME	SYNC	PAGE
SF563 U04	+SEL INTEG CB	F2P07	SF570	SF565 U11	+BEHIND HOME	C2D13	SF556
S05	+SEL INTEG RA	F2P05	SF570	U13	DETECT	E2G04	SF568
G12	-COMMON RESET		TP	J09	SR CLOCK	E2G10	SF568
J13	-SEEK COMPLETE	C2P11 (F2507)	SF556 (SF570)	D13	+HD CHANGE GATE	E2D11	SF568
D11	+SEEK	F2508	SF570	J10	+ENABLE SERVO SPL	E2J04	SF568
P04	+ILLEGAL MOVE	C2U05	SF555	G09	-RECAL	C2J02 (B2R04)	SF567 (SF551)
M10	+GAIN CAL BIT 1		TP	P02	MISSING CLOCKS/2	C2B10	SF556
M03	-MISSING CLK ERROR LATCH	C2J09	SF556	D09	+ROS/DA ERROR	C2U04	SF555
M02	+MISS SERVO LATCH	C2S02	SF556	S07	-IN DRIVE	F2P11 (C2M13)	SF570 (SF556)
M04	PULSING AND	C2M10	SF556	U07	-OUT DRIVE	F2M13 (C2U02)	SF570 (SF556)
P05	-INDEX AND SECTOR	C2G08	SF556	G08	-MISSING SECTOR PULSE	A5B09	SF503
U06	+SERVO PROTECT	C2G10	SF554	S08	+BYTE COUNTER BIT 16	C2U03	SF559A
G10	+BRAKE COIL DRIVE	B3A14	SF	S13	-INDEX	A5D07 (F1A11)	SF503
P07	+BRAKE APPLIED	F2M02 (C2B08)	SF570 (SF554)	S10	-SECTOR	A5B05	SF503
G11	+BRAKE APPLIED TO SYS	B5A14	SF545				
SF564 J02	-OSC LATE	E2J07	TP				
G04	-SEL DEMOD N1	F2D09	SF570				
J06	-SEL DEMOD N2	F2B10	SF570				
G03	-SEL DEMOD Q1	F2B08	SF570				
G02	-SEL DEMOD Q2	F2B09	SF570				
B13	-OSC EARLY	E2G07	SF568				
B12	+CTR 5		TP				
M06	-CTR 4		TP				

S1159621

S1159621

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AID2 LOGIC 2	
11 MAR 80	375662	MACH 4963	
		PART NO 6839621	
C		CLASSIFICATION	IBM CORP

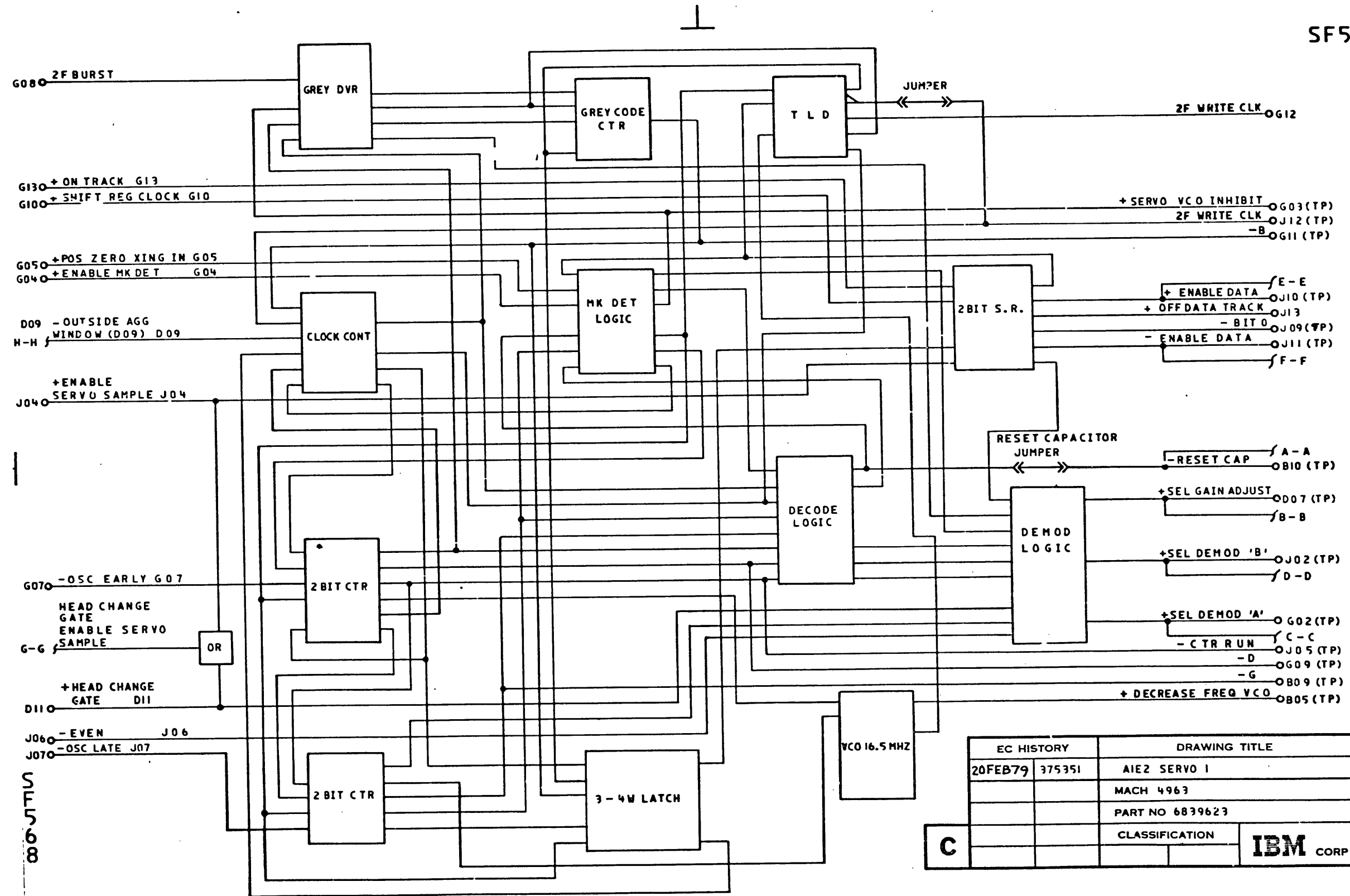
SF567



76507

76507

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIE2 SERVO 1	
		MACH 4963	
		PART NO 6839622	
C		CLASSIFICATION	IBM CORP



EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIE2 SERVO 1	
		MACH 4963	
		PART NO 6839623	
C		CLASSIFICATION	IBM CORP

80655

80655



AIE2 - SERVO 1 - INPUT

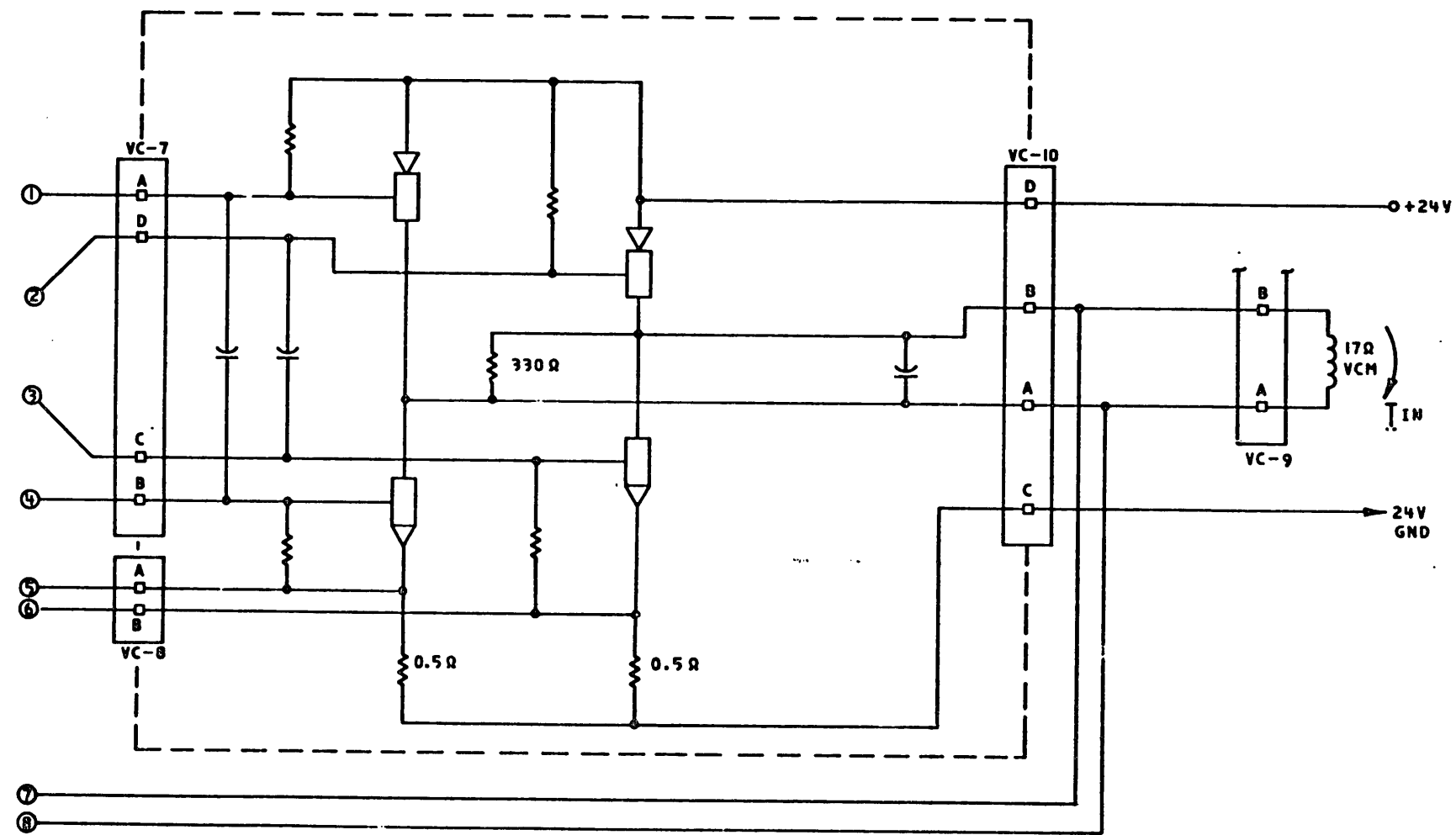
AIE2 - SERVO 1 - OUTPUT

PIN	LINE NAME	SOURCE	PAGE	PIN	LINE NAME	SYNC	PAGE
SF567 B10	RESET CAP			SF567 B12	+POS ZERO XING	E2G05	SF568
B04	TRACK REF	F2B07	SF570	D09	-OUT AGC WINDOW	C2G03	SF556
B03	BUFFERED DATA A	B2B02	SF551	B07	RESET BUCKET		TP
D02	BUFFERED DATA B	B2B03	SF551	B08	LINEAR DATA TRUE		TP
D07	+SEL GAIN ADJUST		TP	D06	LINEAR DATA COMP		TP
G02	+SEL DEMODE A		TP	B13	DATA PES	F2P06	SF570
J02	+SEL DEMODE B		TP				
D13	DEDICATED PES	F2D02	SF570	SF568 G12	2F WRITE CLOCK	B2M10	SF551
J10	+ENABLE DATA		TP	G03	+SERVO INHIBIT	B2U06	SF552
J11	-ENABLE DATA		TP	J13	+OFF DATA TRACK	C2G13	SF554
SF568 G08	2F BURST	B2P11	SF552				
G13	+ON TRACK	C2B12 (F2G12)	SF556 (SF570)				
G10	+SHIFT REG CLOCK	D2J09	SF556				
G05	+POS ZERO XING	E2B12	SF567				
G04	+ENABLE MARK DETECT	D2U13	SF565				
D09	-OUT AGC WINDOW	C2G03	SF556				
J04	+ENABLE SERVO SPL	D2J10	SF565				
G07	-OSC EARLY	D2B13	SF564				
D11	+HEAD CHANGE GATE	D2D13	SF565				
J06	-EVEN	F2B03 (C2S09)	SF570 (SF554)				
J07	-OSC LATE	D2J02	SF564				

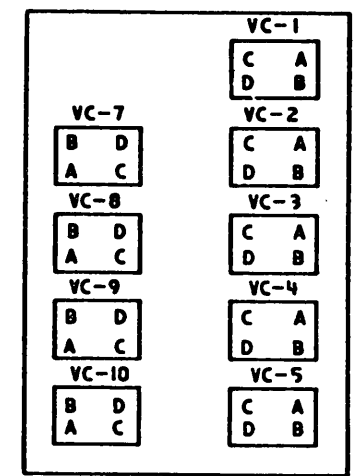
EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIE2 SERVO 1	
		MACH 4963	
		PART NO 5839624	
C		CLASSIFICATION	IBM CORP

96 JTUS

96 JTUS



ACTIVATOR DRIVER CARD

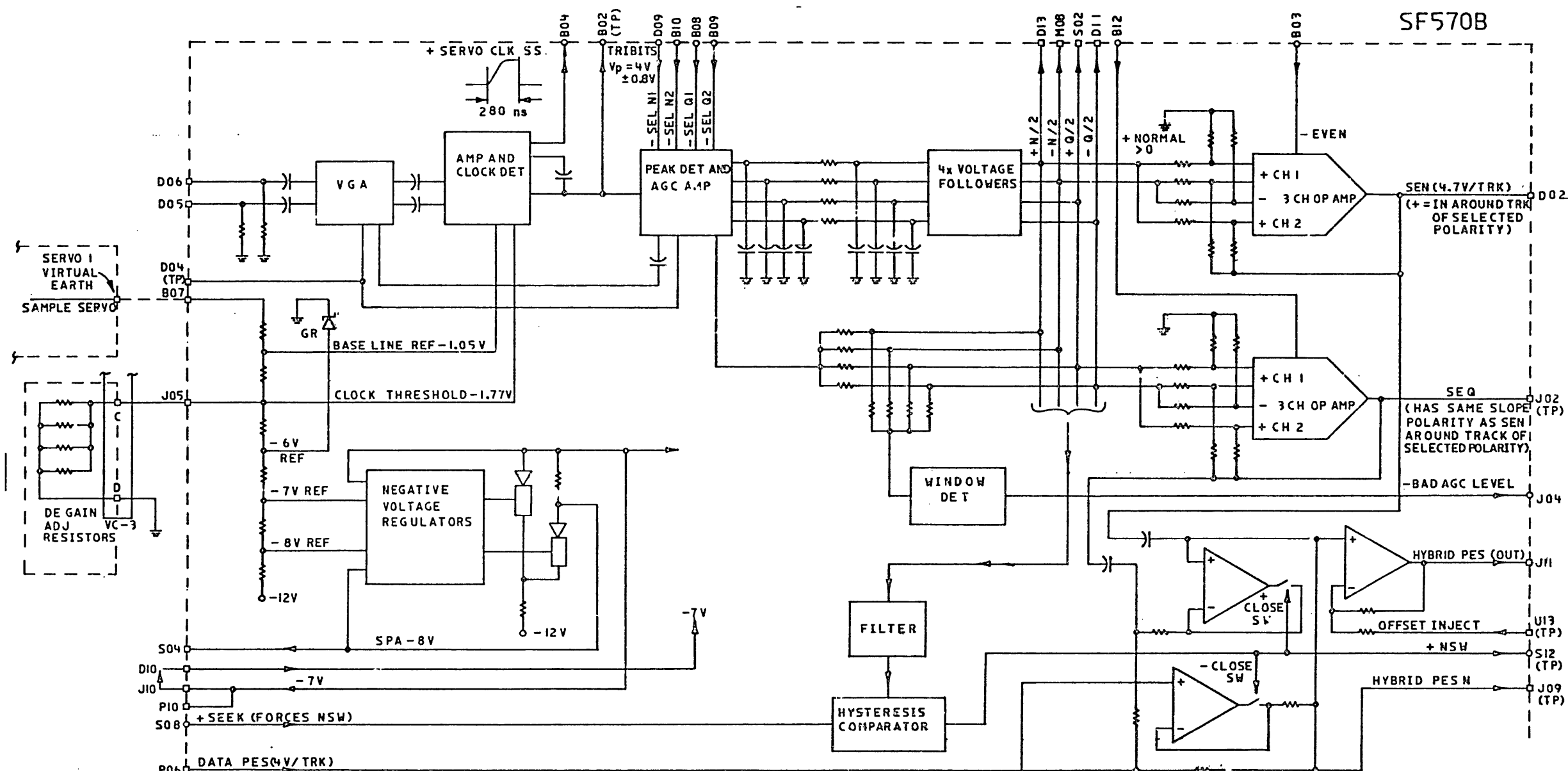


BOARD SHOWING VOLTAGE CROSSOVERS

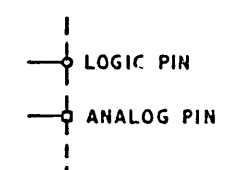
SF570A

SF570A

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	ACTIVATOR DRIVER CARD	
11 MAR 80	375662	MACH 4963	
		PART NO 6839625	
C		CLASSIFICATION	IBM CORP



B0575

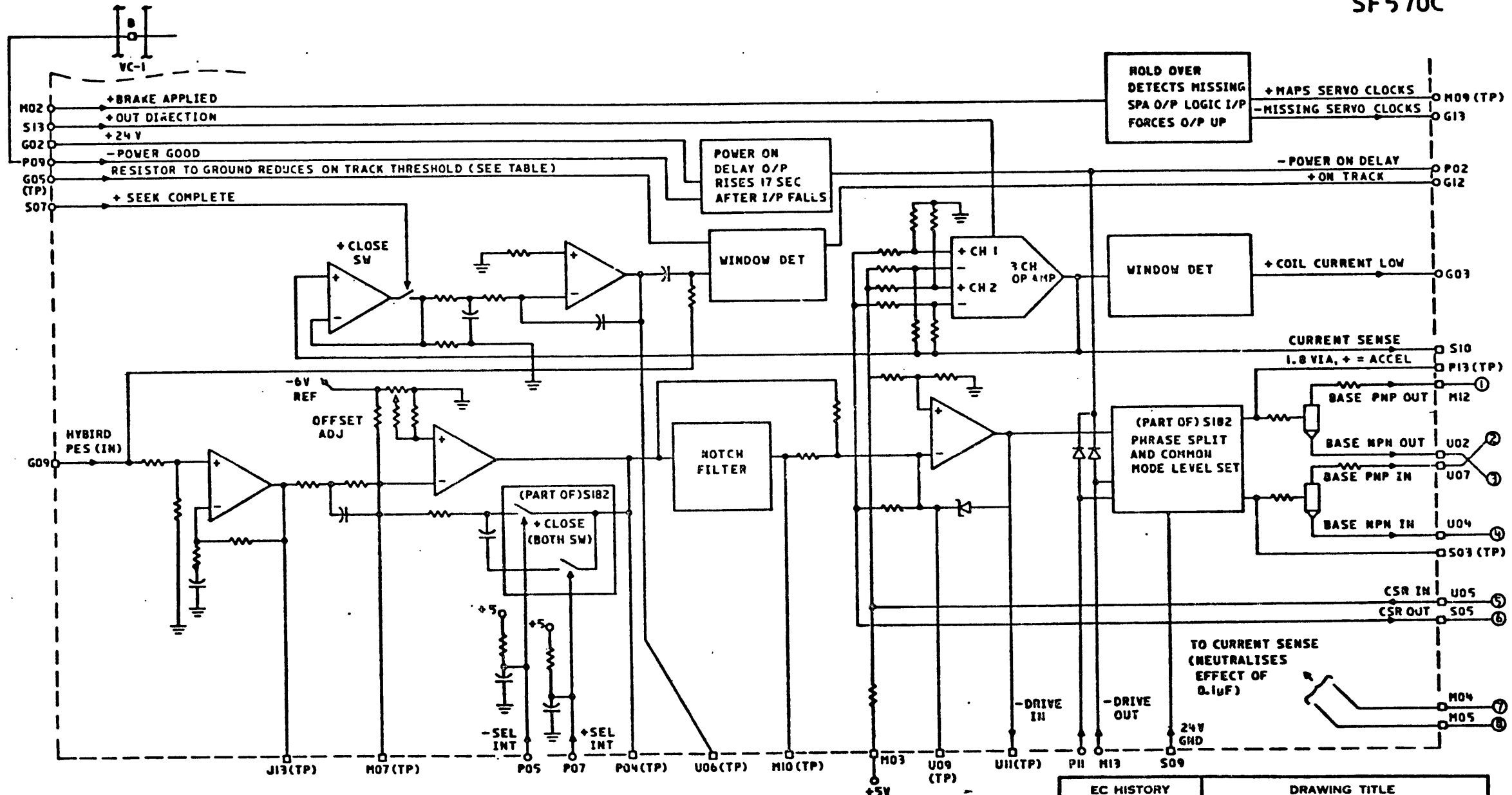


VOLTAGES			
V	PIN	V	PIN
+24	G02	-4	B06, G06, M06, S06
+12	B11, M11, S11, B05	-7	D10, J10, P10, U10
+5	D03, J03, P03, U03	-12	D12, M12
GND	D08, J08, P08, U08		

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	A1F2	SERVO 2
11 MAR 80	375662	MACH	4963
		PART NO 6839626	
C		CLASSIFICATION	IBM CORP

S57570B

SF570C



ON TRK THRESHOLD	
G05 R	% TRK DC
∞	12%
25.5 K	10%
10.2 K	8%
5.1 K	6%

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIF2 SERVO 2	
		MACH 4963	
		PART NO 6839627	
C		CLASSIFICATION	IBM CORP

NOV 79

NOV 79

SF571

AIF2 - SERVO 2 - INPUT

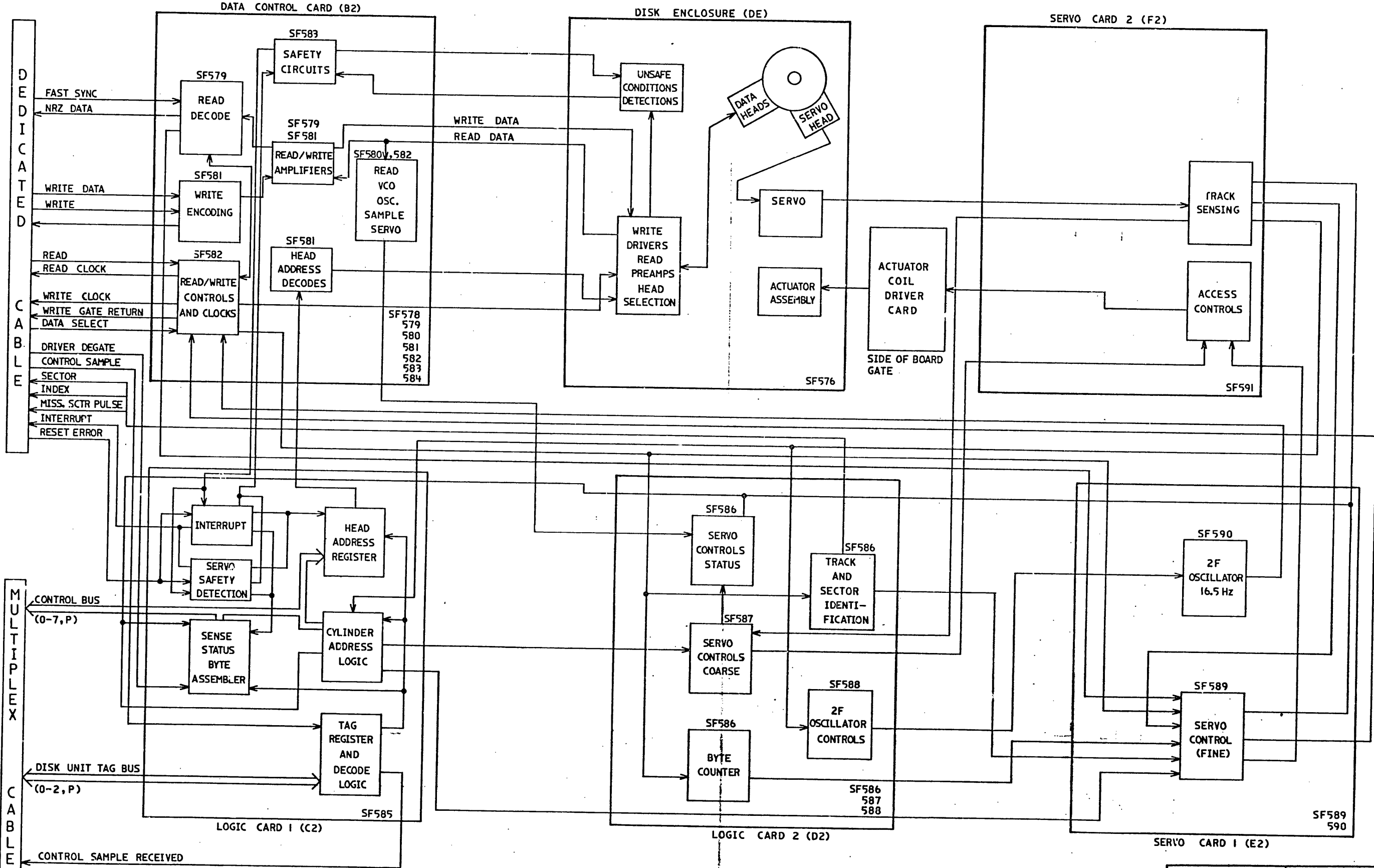
AIF2 - SERVO 2 - OUTPUT

PIN	LINE NAME	SOURCE	PAGE	PIN	LINE NAME	SYNC	PAGE
SF570 B03	- EVEN	E2J06 (C2509)	SF568 (SF554)	SF570 D02	SENSE	E2D13	SF567
B12	+ NORMAL	D2G13	SF560	J04	-BAD AGC	C2U11	SF555
B09	- SEL Q2	D2G02	SF564	J11	HYBRID PES	F2G09 (D1E13)	SF570 (SF510)
B08	- SEL Q1	D2G03	SF564	G13	-MISS SERVO CLKS	D2P06	SF562
B10	- SEL N2	D2J06	SF564	P02	- POWER ON DELAY	D2U09 (C2513)	SF563 (SF565)
D09	- SEL N1	D2G04	SF564	G03	+COIL CURRENT LOW	C2G07	SF556
D06	SERVO OUTPUT	A2D10	SF527	S10	CURRENT SENSOR	D2B09	SF561
D05	SERVO OUTPUT	A2D11	SF527	B04	+SERVO CLK S.S.	D2G05	SF564
B07	SAMPLE SERVO	E2B04	SF567	D13	+N/2	D2512	SF560
J05	DE GAIN	B3E14 (D1C13)	SF510	M08	-N/2	D2U12	SF560
D10	-7 VOLTS	F2U10 (F2J10)(F2D10)(E2D10)	SF570 (SF545)	S02	+Q/2	D2J07	SF560
S08	+SEEK	D2D11	SF563	D11	-Q/2	D2B07	SF560
P06	DATA PES	E2B13	SF567	S04	SPA	A2D09(A2D13)A2B10(A2B12)	SF527
M02	+ BRAKE APPLIED	D2P07 (C2B08)	SF563 (SF554)	G12	+ON TRACK	C2B12, E2G13, T2D06	
S13	+OUT DIRECTION	D2D06 (C2J07)	SF562 (SF556)	U04	BASE NPN IN	ACT DR CARD	
G02	+12 VOLTS	E5A14 (D2S02) (B5E14)	SF545 (SF562)				
P09	-POWER GOOD	D2M09	SF563				
S07	+SEEK COMPLETE	C2P11 (D2J13)	SF556 (SF563)				
G09	HYBRID PES	F2J11 (D1E13)	SF570				
P05	-SEL INT	D2S05	SF563				
P07	+SEL INT	D2U04	SF563				
P11	- DRIVE IN	D2S07 (C2M13)	SF565 (SF556)				
M13	- DRIVE OUT	D2U07 (C2U02)	SF565 (SF556)				
S09	+24 VOLT GND	B6E01 (E6A01)	SF545				
G10	-POWER GOOD	VC-1-B	SF545				

SF571

SF571

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIF2 SERVO 2	
11 MAR 80	375662	MACH 4963	
		PART NO 6839628	
C		CLASSIFICATION	IBM CORP



SF57

EC HISTORY		DRAWING TITLE	
20FEB79	375351	DISK CARDS	
		MACH 4963	
		PART NO 6839632	
		CLASSIFICATION	IBM CORP

DISK ENCLOSURE CONTROLS

THE FOLLOWING CIRCUITS ARE CONTAINED IN THE DE: READ/ WRITE SELECTION CIRCUITS FOR WRITE DRIVERS AND READ PRE-AMPLIFIERS, HEAD SELECTION LOGIC, AND DETECTION FOR UNSAFE LOGIC.

READ/WRITE SELECTION

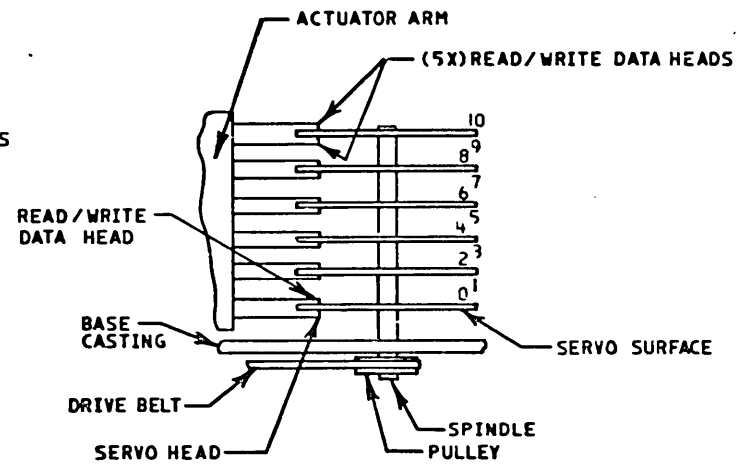
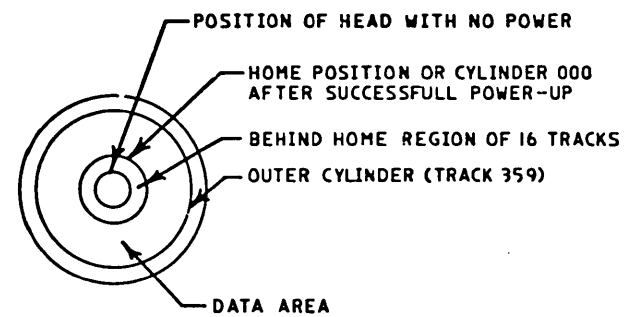
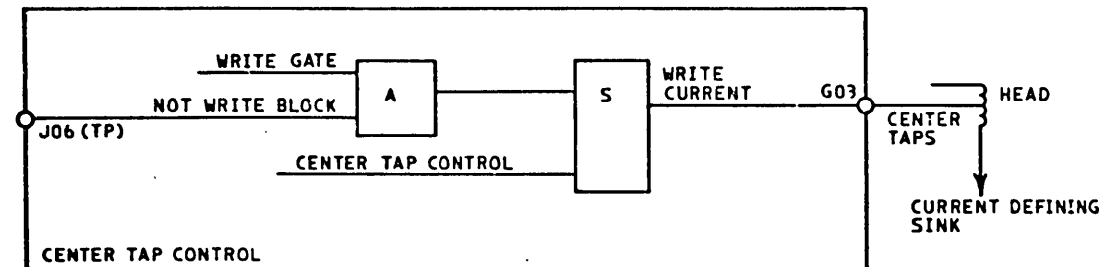
READ AND WRITE MODE SELECTION IS CONTROLLED BY THE 'CENTER TAP' LINE; THIS LINE IS CONNECTED TO THE WRITE DRIVERS AND THE READ PRE-AMPLIFIERS.

IN THE WRITE MODE, THE 'CENTER TAP' LINE IS RAISED TO A POSITIVE-VOLTAGE LEVEL, AND, WHEN 'WRITE GATE' AND 'NOT WRITE BLOCK' ARE APPLIED, WRITE CURRENT IS FED THROUGH THE HEAD.

IN THE READ MODE, THE 'CENTER TAP' LINE IS GROUNDED; THIS SELECTS THE READ CIRCUITS IN THE DE.

PART OF THE CENTER TAP CIRCUIT ACTS AS A CURRENT LIMITER THAT LIMITS THE CENTER-TAP CURRENT TO A SAFE LEVEL.

WRITE MODE



HEAD SELECTION LOGIC

HEADS ARE SELECTED BY A 5-BIT SELECTION CODE PROVIDED BY THE SYSTEM. THIS CODE, HELD IN A REGISTER IN THE DSD, IS CONVERTED INTO CONTROL SIGNALS THAT SELECT CORRESPONDING COMBINATIONS OF MOVING AND FIXED HEADS.

THE MAXIMUM NUMBER OF HEADS FOR WHICH SELECTION IS PROVIDED IN DES WITH FIXED HEADS, IS TEN MOVING HEADS WITH EIGHT FIXED HEADS.

IN DES WITH MOVING HEADS ONLY, THE MAXIMUM FOR WHICH SELECTION IS PROVIDED IS 11 MOVING HEADS.

HEAD SELECTION DECODE

THE SYSTEM CODES FOR SELECTION OF THE APPROPRIATE HEADS ARE GIVEN IN THE TABLE.

HEAD SELECT CODE (FROM SYSTEM)	HEAD SELECTED	OUTPUT LINES SELECTED						
		CHIP SELECTS					HEAD SELECTS	
		1	2	3	4	5	A	B
<b>MOVING HEADS:</b>								
00000	0	1	0	0	0	0	0	0
00001	1	1	0	0	0	0	1	0
00010	2	1	0	0	0	0	0	1
00011	3	1	0	0	0	0	1	1
00100	4	0	1	0	0	0	0	0
G0101	5	0	1	0	0	0	1	0
00110	6	0	1	0	0	0	0	1
00111	7	0	1	0	0	0	1	1
01000	8	0	0	1	0	0	0	0
01001	9	0	0	1	0	0	1	0
01010	10	0	0	1	0	0	0	1
01011	11*	0	0	1	0	0	1	1
<b>FIXED HEADS:</b>								
10000	0	0	0	0	1	0	0	0
10001	1	0	0	0	1	0	1	0
10010	2	0	0	0	1	0	0	1
10011	3	0	0	0	1	0	1	1
10100	4	0	0	0	0	1	0	0
10101	5	0	0	0	0	1	1	0
10110	6	0	0	0	0	1	0	1
10111	7	0	0	0	0	1	1	1

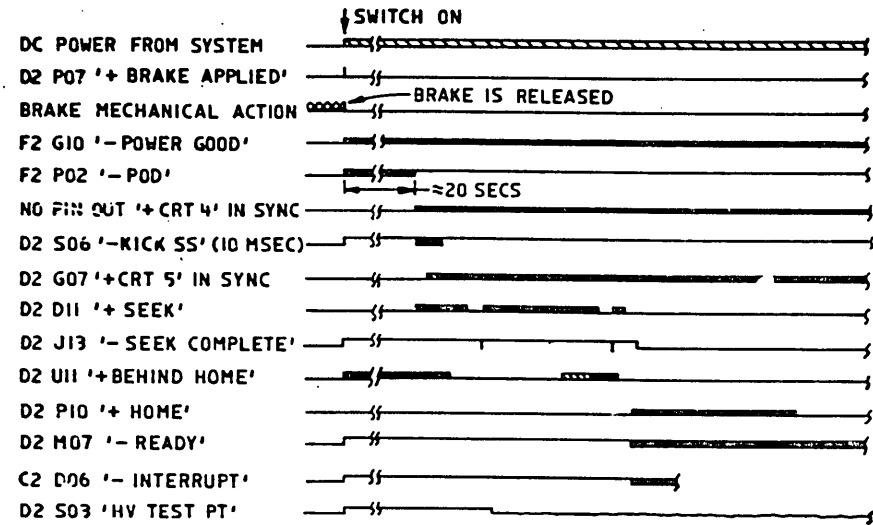
\*NO PHYSICAL HEAD 11 EXISTS BUT A HEAD POSITION 11 IS A SPARE INPUT ON THE DSD ACTUATOR. THE CODE FOR HEAD 11 IS FORCED WHEN AN 'UNSAFE' CONDITION IS DETECTED.

SLS76

SLS76

EC HISTORY		DRAWING TITLE	
20FEB79	375351	DISK ENCLOSURE	
		MACH 4963	
		PART NO 6839633	
C		CLASSIFICATION	IBM CORP

POWER ON LOGIC SEQUENCE TIMING

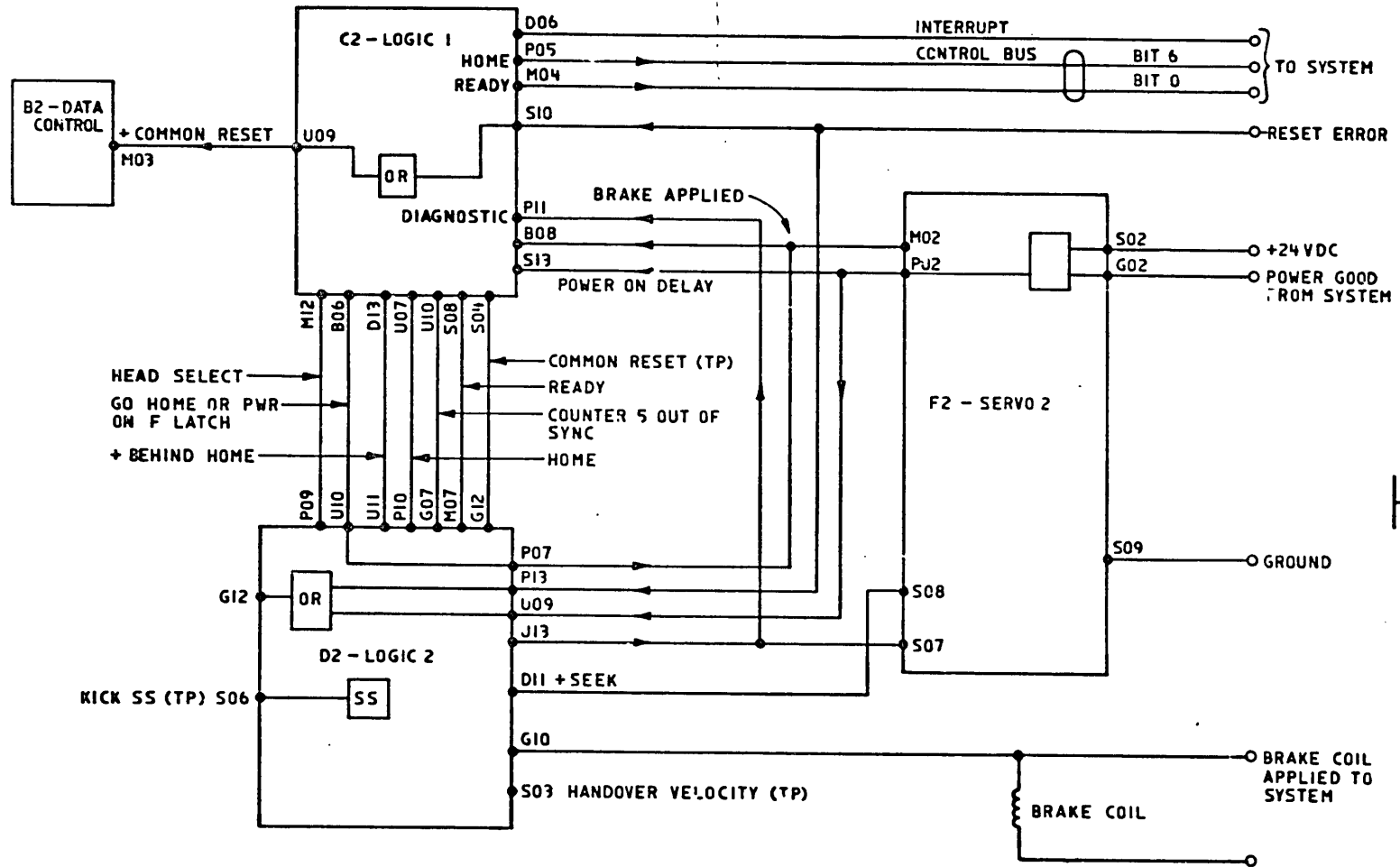


NOTE: THIS CHART INDICATES THE CORRECT SEQUENCE OF EVENTS. ACTUAL TIMES AND WAVE FORMS WILL VARY FROM SYSTEM TO SYSTEM.

POWER ON LOGIC SEQUENCE

1. AC AND DC POWER ARE APPLIED TO THE DSD.
2. 'BRAKE APPLIED' REMAINS ESSENTIALLY NEGATIVE TO PROVIDE RETURN PATH FOR BRAKE CURRENT WHICH RETRACTS THE BRAKE AND ALLOWS THE SPINDLE TO ACCELERATE.
3. '-PWR GOOD' IS RAISED BY THE USING SYSTEM WHEN DC VOLTAGES ARE WITHIN TOLERANCE.
4. '-POD' BECOMES ACTIVE FOR APPROXIMATELY 20 SECONDS TO ALLOW THE DISK SPEED TO STABILIZE AT 3125 RPM.
5. 'CTR 4' COMES INTO SYNCHRONIZATION AFTER '-POD' TIMES OUT AND FIRES THE 'KICK SS'. IF 'CTR 4' FAILS TO COME INTO SYNC BEFORE '-POD' AND 'PLO HOLDOVER SS' TIMES OUT, THEN BRAKE APPLIED WILL BE RAISED, THE BRAKE WILL ACTIVATE AND 'BRAKE APPLIED' TO SYSTEM WILL BE RAISED. AC AND DC POWER WILL THEN BE SWITCHED OFF WITHIN 5 SECONDS.
6. '-KICK SS' APPLIES MAXIMUM ACCELERATION TO THE ACTUATOR ARM FOR 10 MILLISECONDS TO MOVE THE ACTUATOR ARM INTO THE DATA AREA.
7. DURING THE INITIAL ACCESS MOVEMENT 'CTR 5' COMES INTO SYNCHRONIZATION.
8. '+ SEEK' IS RAISED WITH THE 'KICK SS' CYCLE AND IS LOWERED WHEN THE ACTUATOR COMES TO REST.
9. '-SEEK COMPLETE' INITIATES A 'RECALIBRATE' CYCLE.
10. AT THE COMPLETION OF THE RECALIBRATE CYCLE 'HOME' AND 'READY' BECOME ACTIVE AND AN INTERRUPT IS RAISED.
11. DURING THIS RECALIBRATE CYCLE, 'HANDOVER VELOCITY (HV)' IS CALIBRATED. THIS IS AN ANALOG VOLTAGE THAT SHOULD BE SET TO A SIMILAR LEVEL EACH TIME THE DSD IS POWERED UP. THIS LEVEL WILL HOWEVER VARY FROM DSD TO DSD.

577



EC HISTORY		DRAWING TITLE	
20FEB79	375351	POWER ON SEQ	
		MACH 4963	
		PART NO 6829634	
C		CLASSIFICATION	IBM CORP

577



**DATA CONTROL (B2 CARD)**

**INTRODUCTION**

THE DATA CONTROL OPERATIONS OF THE DU ARE CONTROLLED BY LOGIC CONTAINED ON ONE CARD. THIS LOGIC CONTROLS THE WRITING OF DATA ONTO THE DISKS AND THE READING OF THAT DATA WHEN READ COMMANDS ARE ISSUED BY THE SYSTEM.

THE DATA CONTROL CARD INTERFACES WITH THE SYSTEM DIRECTLY, FOR THE TRANSFER OF DATA AND TO EFFECT SOME CONTROL SIGNALS. THE REMAINING CONTROL SIGNALS ARE HANDLED ON OTHER CARDS. THE DATA CONTROL CARD ALSO PRODUCES SIGNALS USED IN THE SERVO CONTROL CIRCUITS.

THE DATA CONTROL INCLUDES THE FOLLOWING ANALOG AND DIGITAL CIRCUITS:

- MODE CONTROL LOGIC
- READ DATA (PAGE SF579)
- READ DATA SEPARATION (PAGE SF584)
- DATA CONTROL SAMPLE SERVO CONTROL (PAGE SF580)
- WRITE DATA (PAGE SF581)
- WRITE SAFETY DETECTION (PAGE SF583)
- DISK ENCLOSURE CONTROLS (PAGE SF576)
- VOLTAGE CONTROLLED OSCILLATOR CONTROL (PAGE SF582)

**MODE CONTROL LOGIC**

THREE SIGNALS, ONE GENERATED IN THE DU AND THE OTHER TWO PROVIDED BY THE SYSTEM, CONTROL THE MODE OF OPERATION:

- \* DATA SELECT 'GATED' (GENERATED ON LOGIC 1, C2 CARD)
- \* WRITE SELECT
- \* READ SELECT

**+ DATA SELECT GATED**

THIS SIGNAL GATES THE FOLLOWING SIGNALS TO THE SYSTEM WHEN IT IS APPLIED TO THE LINE DRIVER CIRCUITS:

- '1F WRITE CLOCK' (CARD PIN B2U11)
- '1F READ CLOCK' (CARD PIN B2U07)
- 'NRZ DATA' (CARD PIN B2S07)

A FURTHER DRIVER (IN THE WRITE LINE DRIVER), USED ONLY AS AN MST TO VTL LEVEL CONVERTER, PROVIDES UNGATED '1F WRITE CLOCK' SIGNALS TO OTHER CARDS IN THE DSD (DATA STORE).

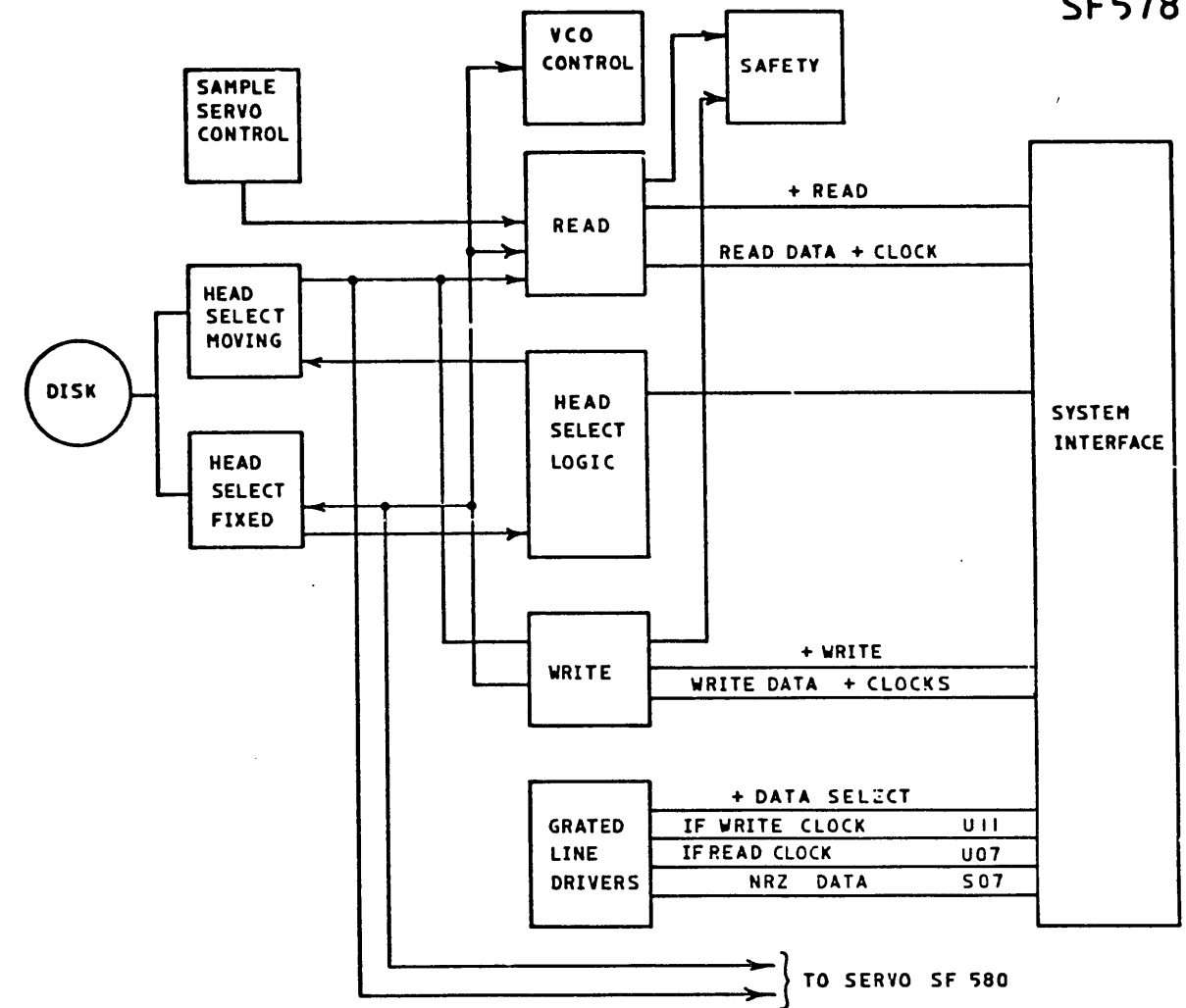
**+READ SELECT**

OPERATIONS EFFECTED WHEN '+ READ SELECT' IS ACTIVATED ARE DESCRIBED IN "READ DATA", ON PAGE SF582

**+ WRITE SELECT**

OPERATIONS EFFECTED WHEN '+ WRITE SELECT' IS ACTIVATED ARE DESCRIBED IN "WRITE DATA", ON PAGE SF581.

51578



SF578

EC HISTORY		DRAWING TITLE	
20FEB79	375351	A1B2 DATA CONTROL	
		MACH 4963	
		PART NO 6839635	
C		CLASSIFICATION	IBM CORP

51578

DATA CONTROL (B2 CARD) (CONTINUED)

READ DATA

CIRCUIT DESCRIPTION

DATA READ FROM THE DISKS CAUSE EACH SELECTED HEAD TO GIVE ANALOG OUTPUT SIGNALS OF LESS THAN 1 MILLIVOLT. THESE SIGNALS ARE AMPLIFIED AND DIFFERENTIATED SO THAT CORRESPONDING DIGITAL DATA CAN BE PRODUCED TO BE USED BY THE SYSTEM.

THE DATA SIGNALS FROM THE MOVING AND FIXED HEADS ARE AMPLIFIED AND ROUTED THROUGH A LOW-PASS FILTER TO A VARIABLE-GAIN AMPLIFIER (VGA) AND TO THE SERVO CONTROL CIRCUIT. TWO AC-COUPLED INPUTS ARE APPLIED TO THE VGA; BOTH PRODUCE DIFFERENTIAL AC CURRENTS IN THE VGA. ONE OF THESE INPUTS IS SET WITH RESPECT TO A REFERENCE VOLTAGE AND THE OTHER HAS A GAIN CONTROL VOLTAGE APPLIED TO IT. THE SIGNAL CURRENTS PRODUCED ARE IN A RATIO THAT DEPENDS ON THE DIFFERENTIAL VOLTAGE BETWEEN THE TWO INPUTS. THESE SIGNAL CURRENTS ARE CONVERTED IN THE VGA TO SIGNAL VOLTAGES.

TO ENSURE THAT THE OUTPUT DC POTENTIAL DOES NOT VARY WITH GAIN, COMPENSATING GATES, CONTROLLED BY THE SAME REFERENCE AND GAIN CONTROL VOLTAGE AS THE INPUT CIRCUIT, ARE CONNECTED INTO THE OUTPUT CIRCUIT.

THE SIGNAL VOLTAGES AT THE OUTPUT OF THE VGA ARE APPLIED TO A LINEAR GAIN AMPLIFIER THAT HAS A GAIN OF APPROXIMATELY TEN. THE OUTPUT OF THE LINEAR GAIN AMPLIFIER IS APPLIED TO A DATA DETECTOR, AND TO AN AMPLITUDE DETECTOR AND HOLD CIRCUIT THAT PRODUCES THE GAIN CONTROL VOLTAGE.

NOTE: DURING WRITE OPERATIONS (SEE "WRITE DATA"), VGA FORMS A 'SQUELCH' CIRCUIT THAT ELIMINATES LARGE TRANSIENTS IN THE INPUT OF THE DATA CHANNEL, PARTICULARLY DURING TURN-ON AND TURN-OFF TIMES.

THE DATA DETECTOR CIRCUIT EXTRACTS FROM THE ANALOG SIGNAL TIMING INFORMATION CONTAINED IN THE SIGNAL PEAKS. THIS TIMING INFORMATION IS PROCESSED IN THE VOLTAGE-CONTROLLED OSCILLATOR (VCO) SYNC CONTROL, PHASE DISCRIMINATOR AND MFM DECODES CIRCUITS, DESCRIBED LATER.

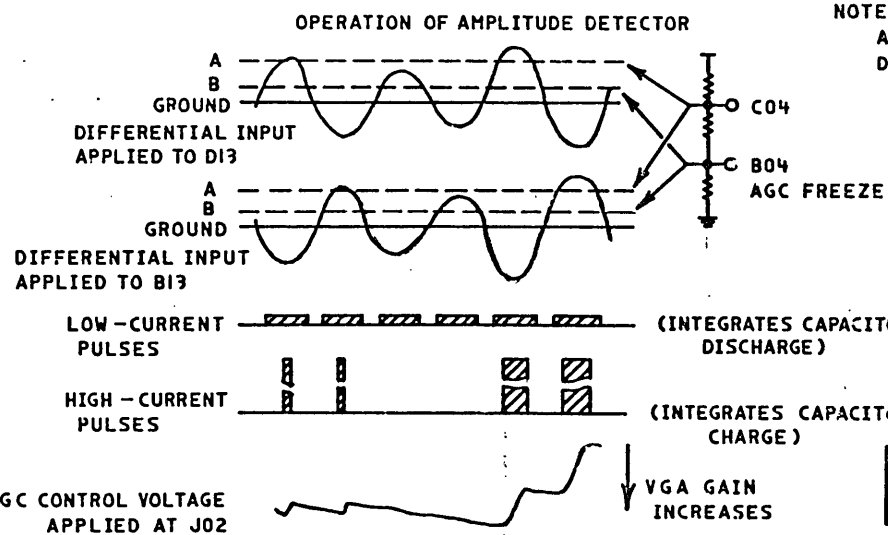
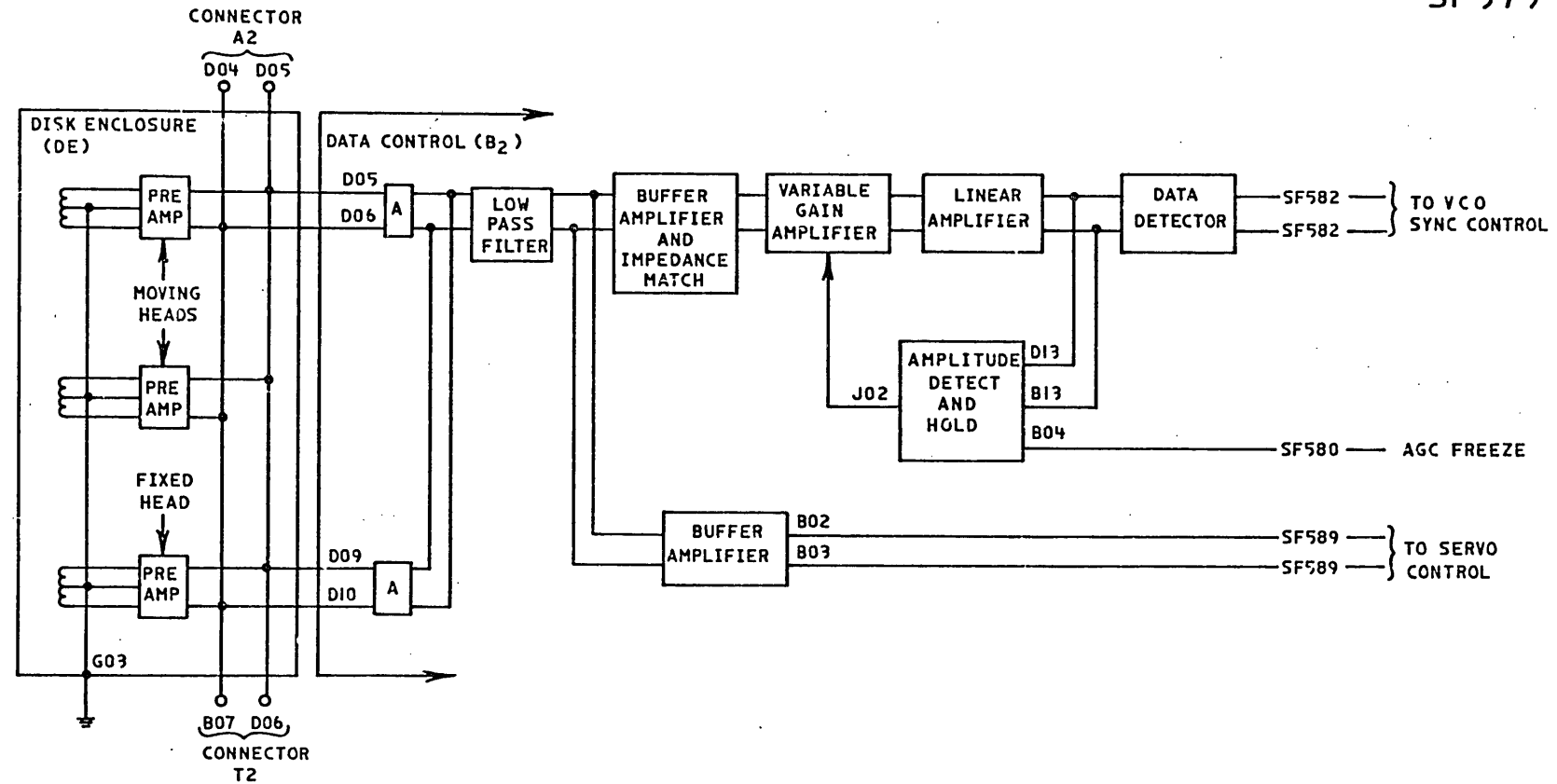
AMPLITUDE DETECTOR AND HOLD CIRCUIT

TWO REFERENCE LEVELS (A AND B) ARE SET IN THE AMPLITUDE DETECTOR AND HOLD CIRCUIT AS FOLLOWS.

WHEN SIGNALS APPLIED AT EITHER OF THE DIFFERENTIAL INPUTS TO THE VGA ARE OF GREATER AMPLITUDE THAN THE FIRST OF THE REFERENCE LEVELS (A) AN INTEGRATOR CAPACITOR IN THE AMPLITUDE DETECTOR AND HOLD CIRCUIT IS CHARGED POSITIVELY. LOW-CURRENT SIGNAL PULSES DISCHARGE THE CAPACITOR. WHEN THE CIRCUIT IS BALANCED, HIGH CURRENT PULSES OCCUR ONLY AT THE PEAKS OF INPUT WAVEFORMS.

THE SECOND REFERENCE LEVEL (B) IS A REFERENCE POTENTIAL THAT DETERMINES THE DISCHARGE CHARACTERISTICS OF THE INTEGRATOR CAPACITOR.

DURING THE TIMES THAT SAMPLE SERVO INFORMATION IS READ, THE TWO REFERENCE LEVELS ARE RAISED ABOVE THE NORMAL DATA-READ LEVELS, AND THE CHARGING AND DISCHARGING OF THE INTEGRATOR CAPACITOR ARE INHIBITED. THIS PREVENTS TRANSIENT DISTURBANCES IN THE READ CHANNEL.



EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIB2 READ DATA	
		MACH 4963	
		PART NO 6839636	
		CLASSIFICATION	IBM CORP

579

579

DATA CONTROL (CONTINUED)

DATA CONTROL SAMPLE SERVO CONTROL

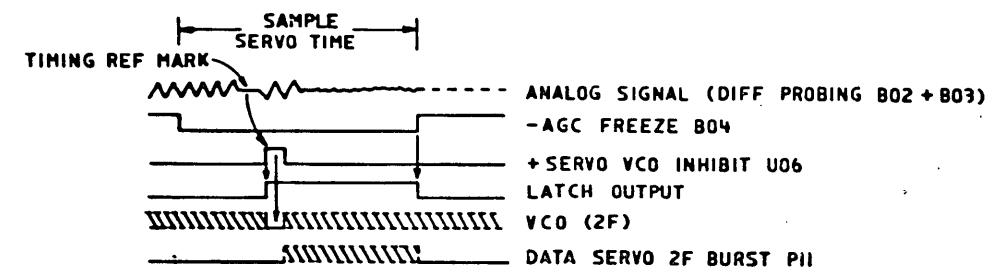
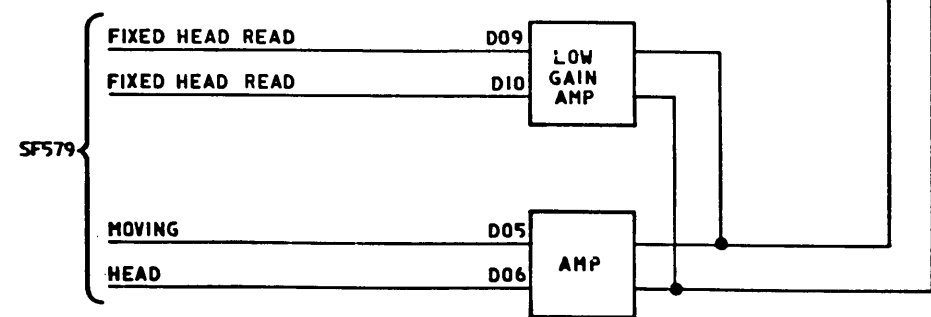
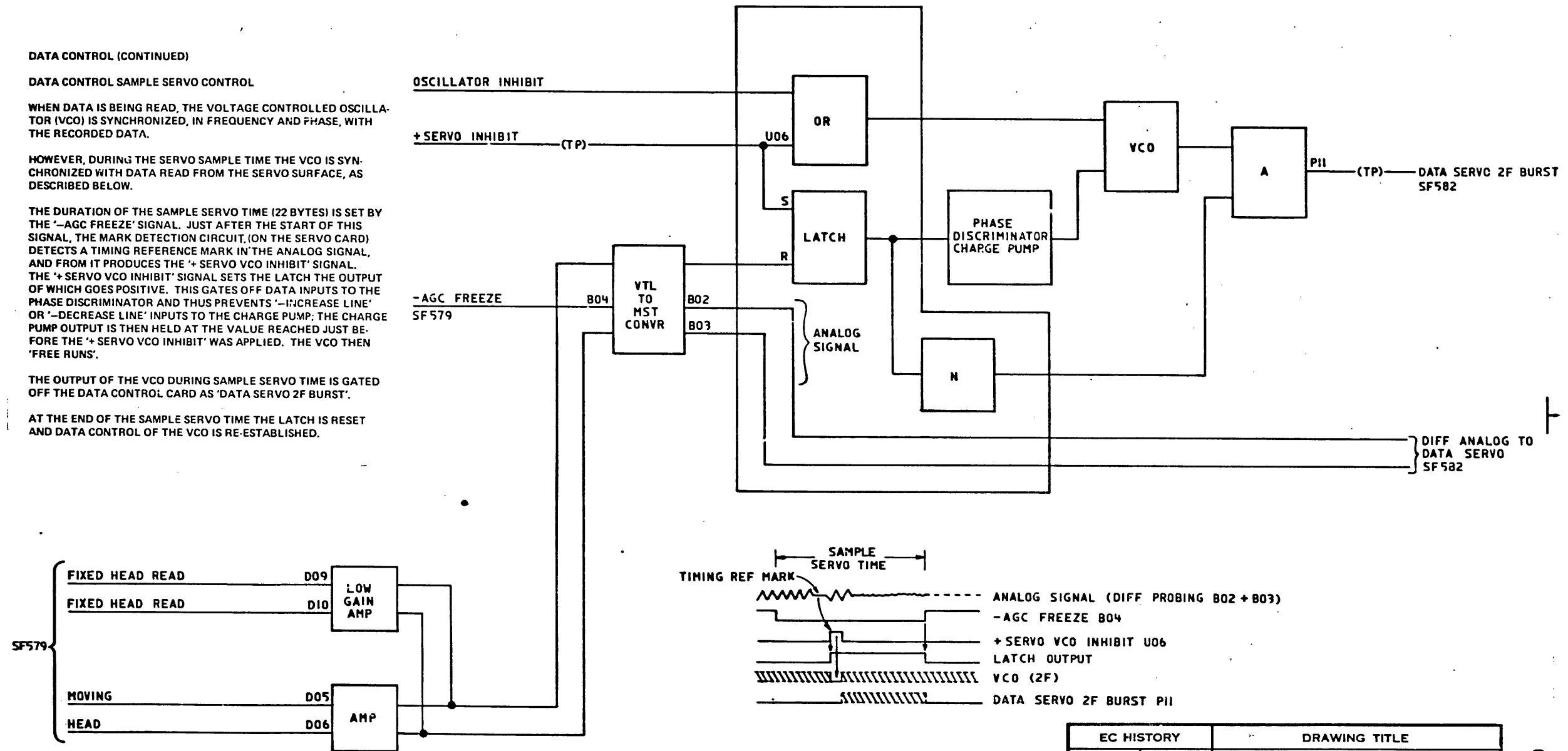
WHEN DATA IS BEING READ, THE VOLTAGE CONTROLLED OSCILLATOR (VCO) IS SYNCHRONIZED, IN FREQUENCY AND PHASE, WITH THE RECORDED DATA.

HOWEVER, DURING THE SERVO SAMPLE TIME THE VCO IS SYNCHRONIZED WITH DATA READ FROM THE SERVO SURFACE, AS DESCRIBED BELOW.

THE DURATION OF THE SAMPLE SERVO TIME (22 BYTES) IS SET BY THE '-AGC FREEZE' SIGNAL. JUST AFTER THE START OF THIS SIGNAL, THE MARK DETECTION CIRCUIT, (ON THE SERVO CARD) DETECTS A TIMING REFERENCE MARK IN THE ANALOG SIGNAL, AND FROM IT PRODUCES THE '+SERVO VCO INHIBIT' SIGNAL. THE '+SERVO VCO INHIBIT' SIGNAL SETS THE LATCH THE OUTPUT OF WHICH GOES POSITIVE. THIS GATES OFF DATA INPUTS TO THE PHASE DISCRIMINATOR AND THUS PREVENTS '-INCREASE LINE' OR '-DECREASE LINE' INPUTS TO THE CHARGE PUMP; THE CHARGE PUMP OUTPUT IS THEN HELD AT THE VALUE REACHED JUST BEFORE THE '+SERVO VCO INHIBIT' WAS APPLIED. THE VCO THEN 'FREE RUNS'.

THE OUTPUT OF THE VCO DURING SAMPLE SERVO TIME IS GATED OFF THE DATA CONTROL CARD AS 'DATA SERVO 2F BURST'.

AT THE END OF THE SAMPLE SERVO TIME THE LATCH IS RESET AND DATA CONTROL OF THE VCO IS RE-ESTABLISHED.



EC HISTORY		DRAWING TITLE	
20FEB79	375351	A1B2	DATA CHANNEL SERVO
			MACH 4963
			PART NO 6839637
C		CLASSIFICATION	IBM CORP

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**WRITE DATA**

**NOTE:** 'PRE-COMPENSATION', MENTIONED IN THE FOLLOWING TEXT, IS A DISTORTION OF MFM (MODIFIED FREQUENCY MODULATION) ENCODED DATA TO COMPENSATE FOR TIMING ERRORS.

DATA TO BE WRITTEN ON THE DISK IS SERIAL 'NRZ' DATA APPLIED TO THE '-WRITE DATA' INPUT U02. THE '-WRITE DATA' SIGNAL IS CONVERTED TO MST LEVELS AND APPLIED TO THE 4-BIT SHIFT REGISTER AS DESCRIBED BELOW.

'WRITE SELECT' IS APPLIED TO THE PRE-COMPENSATION TIMING VIA THE VTL TO MST CONVERTER AND INVERTER. '2F WRITE CLOCK' IS DIVIDED BY 2 IN THE -2 AC TRIGGER AND APPLIED TO THE PRE-COMPENSATION TIMING CIRCUIT AS '1F'. WHEN 'WRITE SELECT' IS ACTIVE, '1F' IS GATED INTO THE PRE-COMPENSATION CIRCUIT WHICH THEN PRODUCES '2F EARLY', '2F ON TIME', AND '2F LATE' OUTPUTS. THE OUTPUTS ARE CLOCK PULSES OF DIFFERENT PHASES WITH RESPECT TO EACH OTHER. '2F EARLY' AND '2F LATE' ARE DISPLACED RESPECTIVELY + AND -9 NANOSECONDS FROM '2F ON TIME'.

THE '1F' SIGNAL IS ALSO APPLIED TO THE MFM ENCODER IN WHICH IT IS ANDED WITH THE '2F EARLY' OUTPUT OF THE PRE-COMPENSATION TIMING CIRCUIT. THIS PRODUCES NARROW PULSES AT BIT-CELL RATE. THE NARROW PULSES CLOCK 'WRITE DATA' INTO THE 4-BIT SHIFT REGISTER.

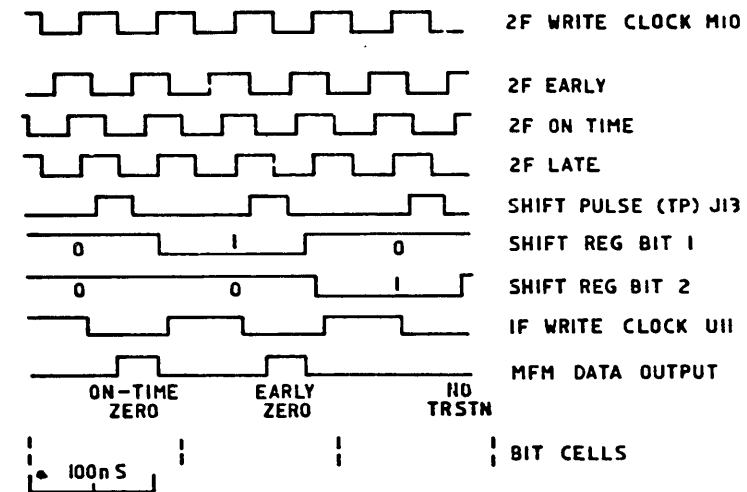
THE SHIFT REGISTER CHANGES THE SERIAL INPUT DATA INTO A 4-BIT PARALLEL SIGNAL THAT IS APPLIED TO THE MFM ENCODER. THE MFM ENCODER PRODUCES MFM-CODED DATA (A TRAIN OF PULSES EACH OF APPROXIMATELY 30 NANOSECONDS DURATION) THAT IS CONVERTED TO 'BI-PHASE' SIGNALS BY AN AC TRIGGER. THE BI-PHASE SIGNAL IS APPLIED TO THE HEADS VIA THE WRITE LINE DRIVERS.

THE PRE-COMPENSATION CIRCUIT USES THE '2F EARLY' TO ADD PRE-COMPENSATION TO THE ENCODED DATA.

THE MFM ENCODER OUTPUT IS ALSO APPLIED TO THE DATA SEPARATOR CIRCUIT WHICH READS BACK THE WRITTEN DATA DURING A WRITE OPERATION.

THE '+ WRITE DC' CONTROL LINE IS USED ONLY DURING MANUFACTURING TESTS.

**WRITE ENCODING TIMING EXAMPLE**

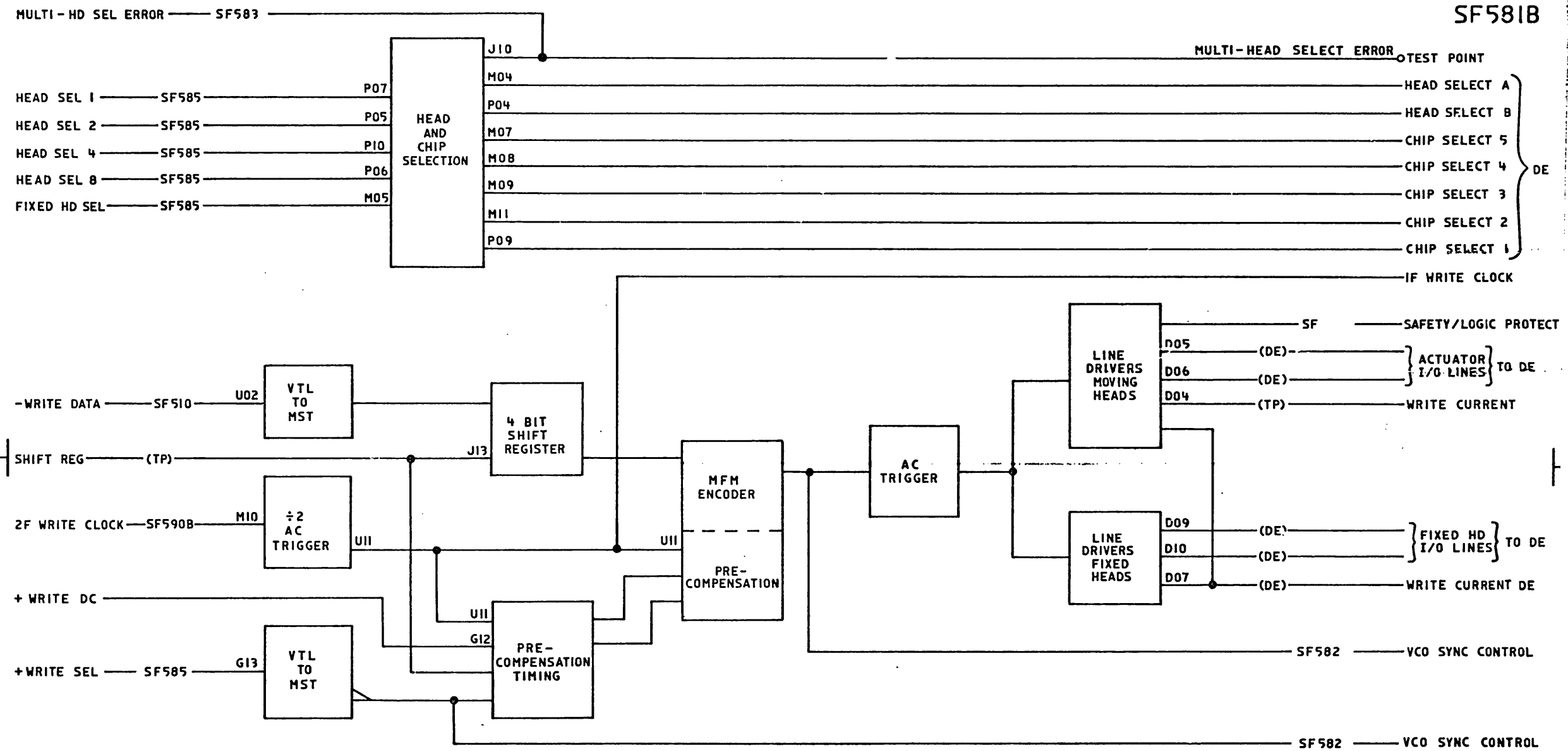


SF581A

EC HISTCRY		DRAWING TITLE	
20 FEB 79	375351	A1B2 WRITE DATA	
		MACH 4963	
		PART NO 6839638	
C	CLASSIFICATION		IBM CORP

SF581A

SF581B



SF581B

SF581B

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIB2 WRITE DATA	
11 MAR 80	375662	MACH 4963	
		PART NO 6839639	
C		CLASSIFICATION	IBM CORP

SF582

VOLTAGE CONTROLLED OSCILLATOR (VCO) CONTROL

THE VCO AND ASSOCIATED CONTROL CIRCUIT FORM A PHASE-LOCKED LOOP THAT TRACKS THE FREQUENCY AND AVERAGE PHASE OF THE READ INPUT DATA SIGNAL, AND CORRECTS FOR ANY DRIFT IN THESE SIGNAL COMPONENTS.

CIRCUIT OPERATION

THE 2F READ CLOCK APPLIED TO THE 'DATA LATCH' IS COMPARED WITH THE 'DATA SS (SINGLE SHOT)' FOR COINCIDENCE. IF THE 'DATA SS' PULSE IS COMPLETED BEFORE THE END OF THE CORRESPONDING 'DATA LATCH' PULSE, AN '-INCREASE LINE' IS ACTIVATED. IF THE 'DATA SS' PULSE IS COMPLETED AFTER THE END OF THE CORRESPONDING 'DATA LATCH' PULSE, A '-DECREASE LINE' IS ACTIVATED. THE COMBINED OUTPUT (AN ANALOG CONTROL VOLTAGE) IS APPLIED TO THE VCO TO RESTORE THE CORRECT COINCIDENCE OF THE 'DATA LATCH' PULSES WITH THE 'DATA SS' PULSE.

RELATIVELY LARGE DISCONTINUITIES OF THE DATA SIGNAL CAN CAUSE LOSS OF SYNCHRONIZATION OF THE 'DATA LATCH' AND 'DATA SS' SIGNALS. THEREFORE, WHEN THE SOURCE OF THE DATA SIGNAL CHANGES, FOR EXAMPLE WHEN CHANGING FROM WRITING TO READING, THE VCO CONTROL CIRCUIT IS SWITCHED MOMENTARILY TO THE 'FAST SYNCHRONIZATION' STATE.

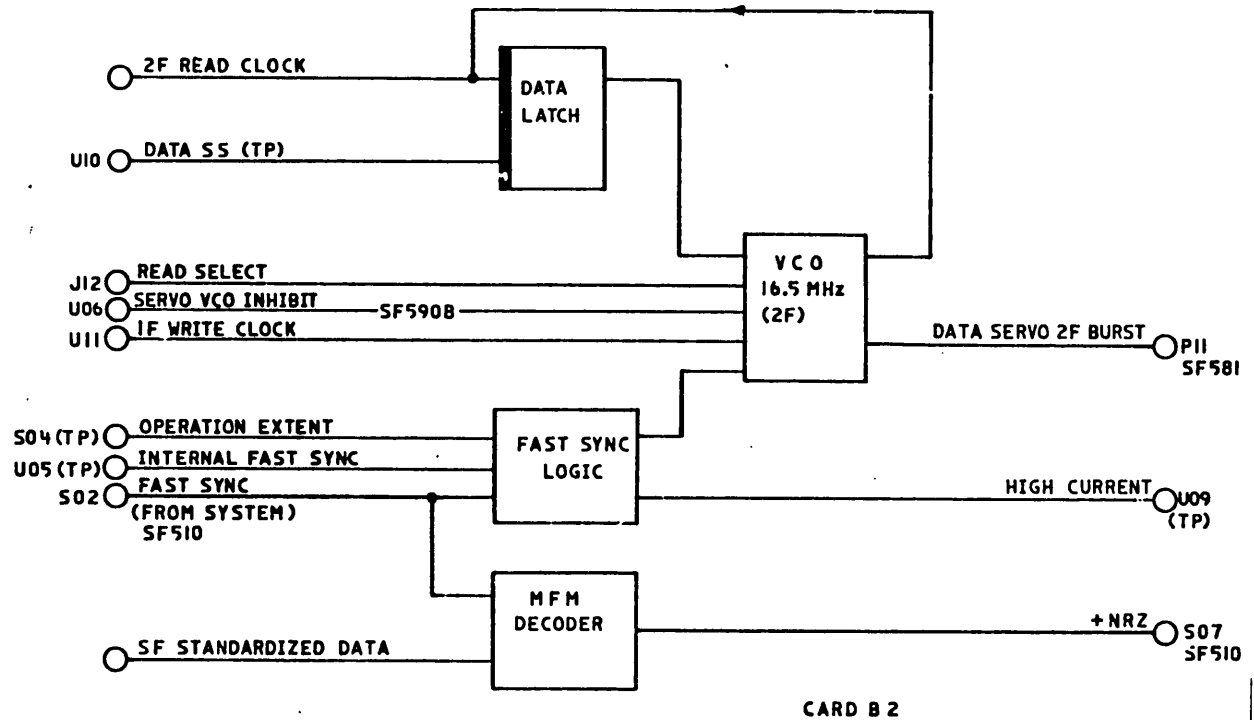
DURING FAST SYNCHRONIZATION THE VCO OPERATES SIMILARLY TO THE MANNER DESCRIBED FORMERLY, EXCEPT THAT THE SIGNALS INVOLVED ARE MUCH GREATER.

THE 'FAST SYNC' SIGNAL APPLIED TO THE FAST SYNC LOGIC CAN BE IN ONE OF TWO PHASES DEPENDING ON THE MODE (READ OR WRITE) IN WHICH THE DSD IS OPERATING. THE FAST SYNC LOGIC SELECTS THE APPROPRIATE FAST SYNC INPUT, THAT IS, 'FAST SYNC' FROM USING SYSTEM OR 'INTERNAL FAST SYNC'.

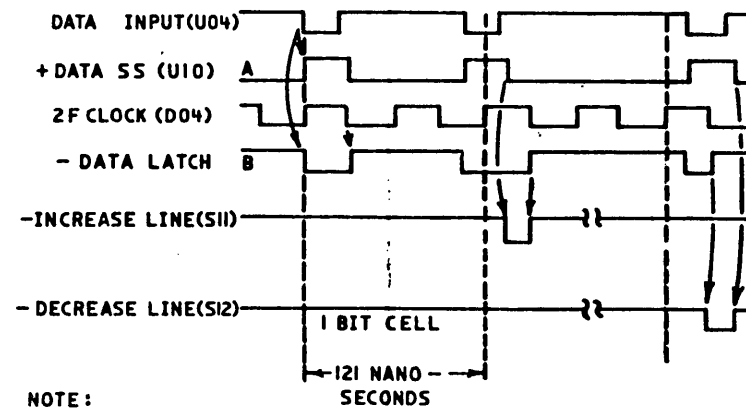
THE 'INHIBIT SS' PULSE SETS A VCO CONTROL LATCH, THE OUTPUT OF WHICH CUTS OFF THE DATA APPLIED TO THE PHASE DISCRIMINATOR AND DATA DECODER PART OF THE VCO. THE VCO IS STOPPED DURING THIS TIME BY A 2F CLOCK PULSE.

THE CIRCUIT IS RESET BY THE END OF THE 'INHIBIT SS' PULSE AND THE DATA PULSES, THE VCO IS THEN RESTARTED SO THAT THE DATA PULSES AND THE VCO OUTPUT ARE SYNCHRONIZED.

WHEN THE DSD IS NOT UNDER THE CONTROL OF THE USING SYSTEM, THE VCO IS SYNCHRONIZED WITH THE WRITE CLOCK.



VCO CONTROL DIAGRAM



NOTE: THIS IS A SIMPLIFIED TIMING DIAGRAM. OSCILLATOR LATE AND EARLY PULSES DO NOT OCCUR ON CONSECUTIVE SERVO CLOCK PULSES.

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	A1B2 VCO CONTROL	
11 MAR 80	375662	MACH 4963	
		PART NO 6839640	
C	CLASSIFICATION		IBM CORP

NCSJ T11

NCSJ T11

**WRITE SAFETY DETECTION**

**GENERAL**

WRITE SAFETY DETECTION CIRCUITS ON THE DATA CHANNEL CARD CHECK OPERATIONS OF THE DSD THAT COULD AFFECT DATA WRITEN ON THE DISKS OR DATA BEING WRITTEN.

THESE CIRCUITS CHECK FOR THE FOLLOWING UNSAFE CONDITIONS:

- NO TRANSITIONS - THAT IS, FAILURE OF WRITE DRIVERS TO SWITCH CURRENT IN A HEAD IN WRITE MODE.
- HEAD GROUNDED - THIS CAUSES EXCESSIVE CURRENT IN THE CENTER-TAP LINE.
- MULTI-CHIP SELECTION - THIS CAUSES EXCESSIVE CURRENT IN THE POSITIVE POWER SUPPLY TO THE DE CIRCUITS.
- SERVO UNSAFE - LOGICAL OR ANALOG UNSAFE CONDITIONS EXTERNAL TO THE DATA CHANNEL.
- WRITE CURRENT WHEN NOT WRITING.

EACH OF THE FIRST FOUR UNSAFE CONDITIONS LISTED ABOVE CAUSES A LATCH TO BE SET IN THE SAFETY CONDITION LATCHES.

THE LATCH OUTPUTS ARE ORED AND THE OUTPUT OF THE OR IS DOT ORED WITH '+ SERVO UNSAFE' TO PRODUCE THE LINE '+ DATA UNSAFE'.

**NO TRANSITIONS**

NORMALLY, WHEN THE CURRENT IN A HEAD IS REVERSED DURING A WRITE OPERATION, VOLTAGE SPIKES ARE PRODUCED IN THE HEAD WINDING. IF THESE SPIKES ARE MISSING, (THAT IS, NO TRANSITIONS OCCUR) EITHER THE HEAD, OR THE WRITE DRIVER HAS FAILED.

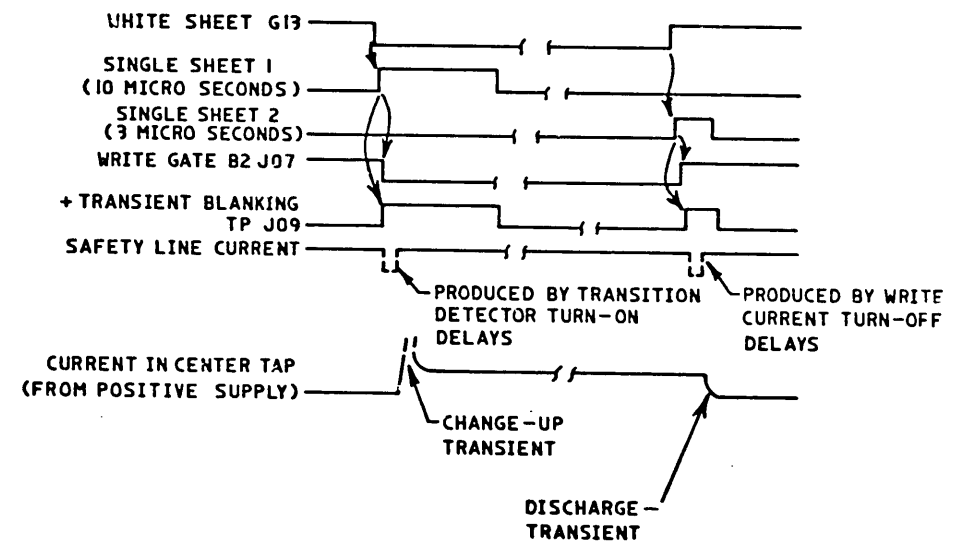
THE VOLTAGE DUE TO THIS FAILURE AND WITH '- WRITE GATE' PRODUCES THE '- NO TRANSITIONS DURING WRITING' SIGNAL. THIS SIGNAL SETS THE APPROPRIATE SAFETY CONDITION LATCH.

**HEAD GROUNDED**

A HEAD-TO-GROUND SHORT CIRCUIT CAN CAUSE CURRENT IN THE CENTER-TAP LINE TO EXCEED THE THRESHOLD SET IN THE ASSOCIATED CURRENT THRESHOLD SENSE CIRCUIT; THEN A 'HEAD GROUNDED' ERROR SIGNAL IS PRODUCED.

**MULTI-CHIP SELECTION**

IF CURRENT IN THE POSITIVE SUPPLY TO THE DE EXCEEDS THE THRESHOLD SET IN THE ASSOCIATED CURRENT THRESHOLD SENSE CIRCUIT, A 'MULTI-CHIP SELECTION' ERROR SIGNAL IS PRODUCED.

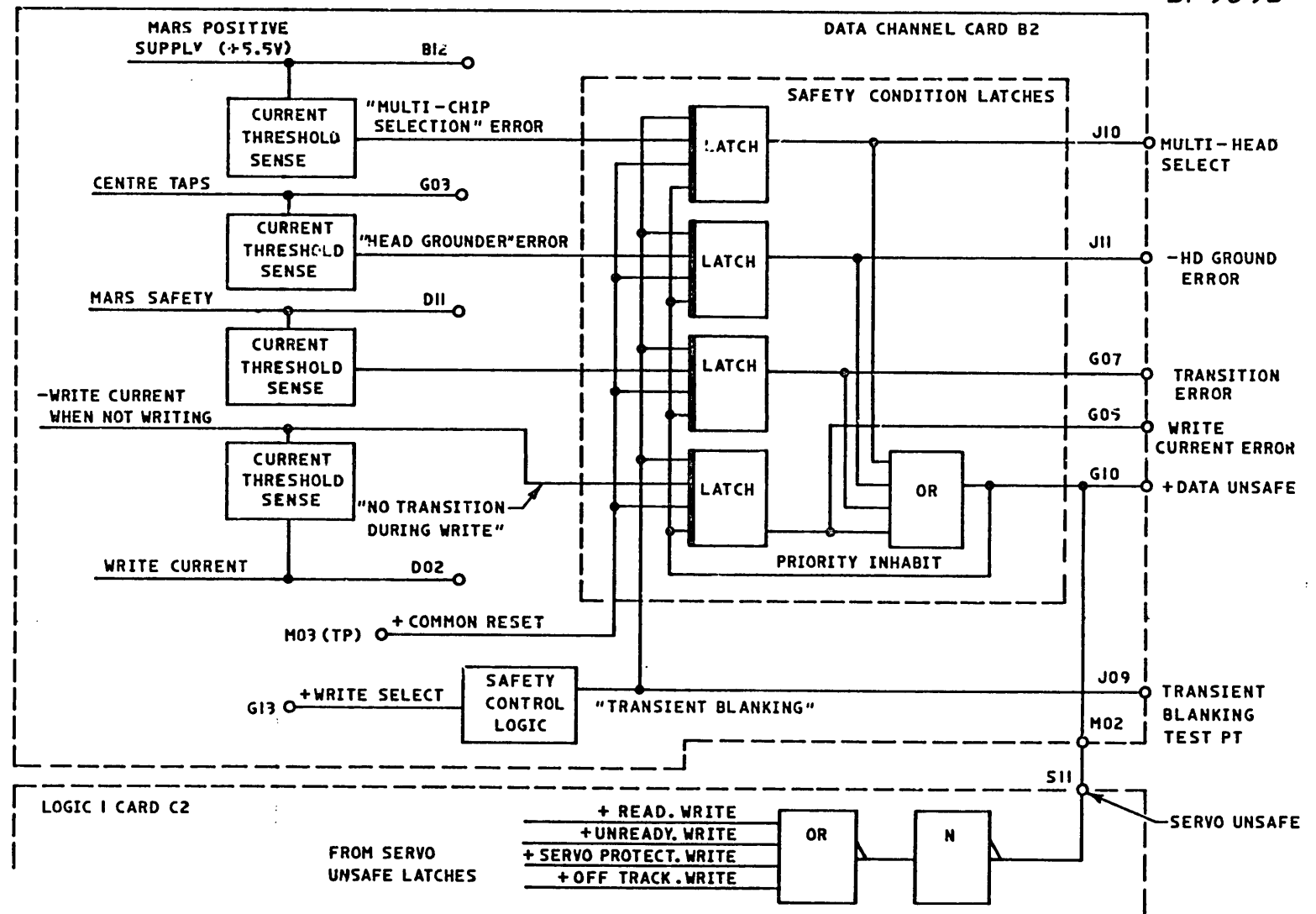


EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	A2B2 WRITE SAFETY	
		MACH 4963	
		PART NO 6839641	
C		CLASSIFICATION	IBM CORP

SF583A

SF583A

SF583B



EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIB2	WRITE SAFETY
11 MAR 80	375662	MACH	4963
		PART NO 6839642	
C		CLASSIFICATION	
		IBM CORP	

SULLIVAN

SULLIVAN



READ DATA SEPARATION

DATA FROM THE DATA DETECTOR CONSISTS OF A TRAIN OF PULSES THAT CONTAIN TIMING INFORMATION RELATED TO PEAKS IN THE ORIGINAL ANALOG SIGNAL. THE DATA SEPARATION LOGIC IDENTIFIES THE TIMING INFORMATION AS '1' OR '0' PULSES, ELIMINATES THE '0' PULSES, AND RE-TIMES THE '1' PULSES WITH THE INTERNAL CLOCK.

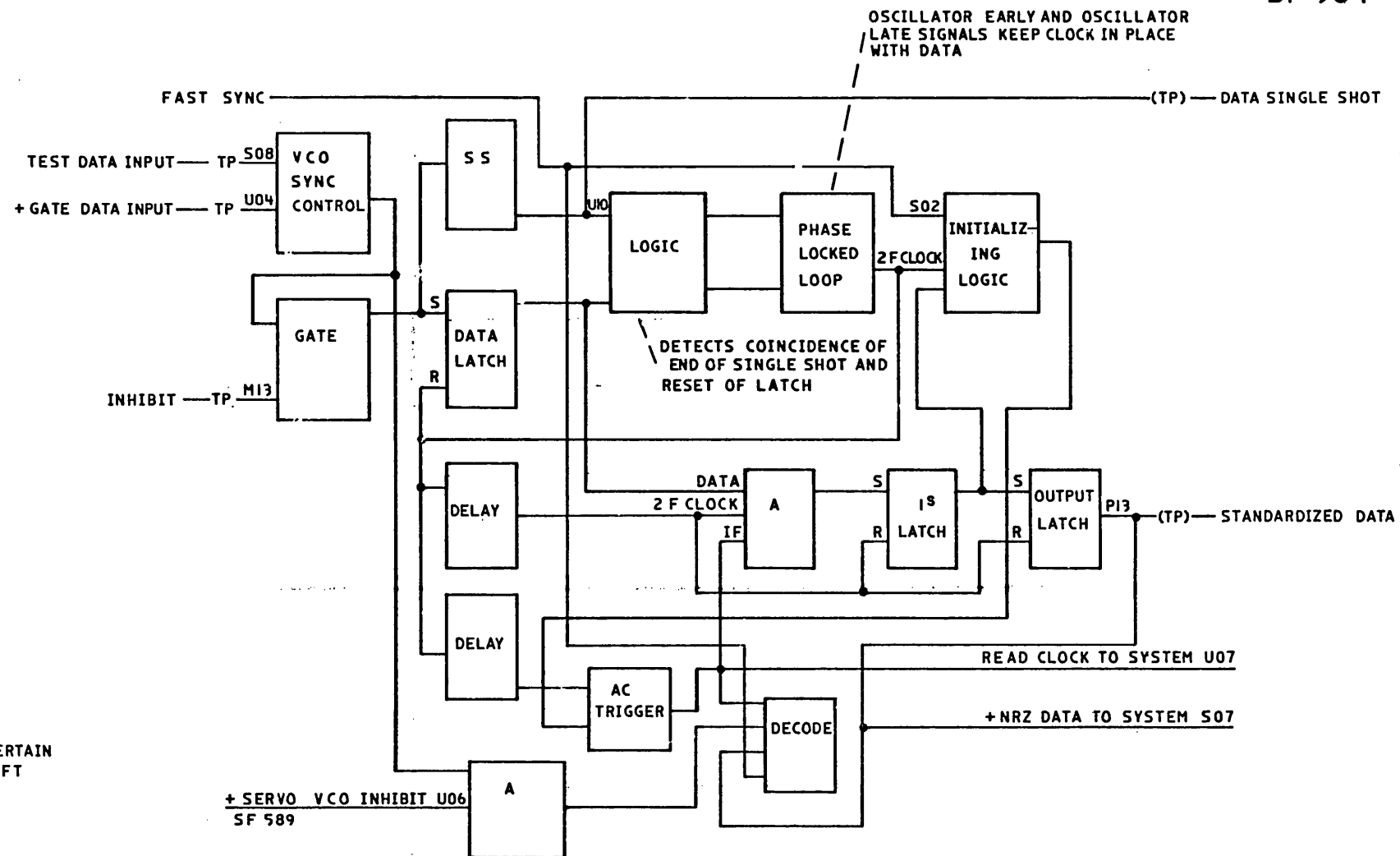
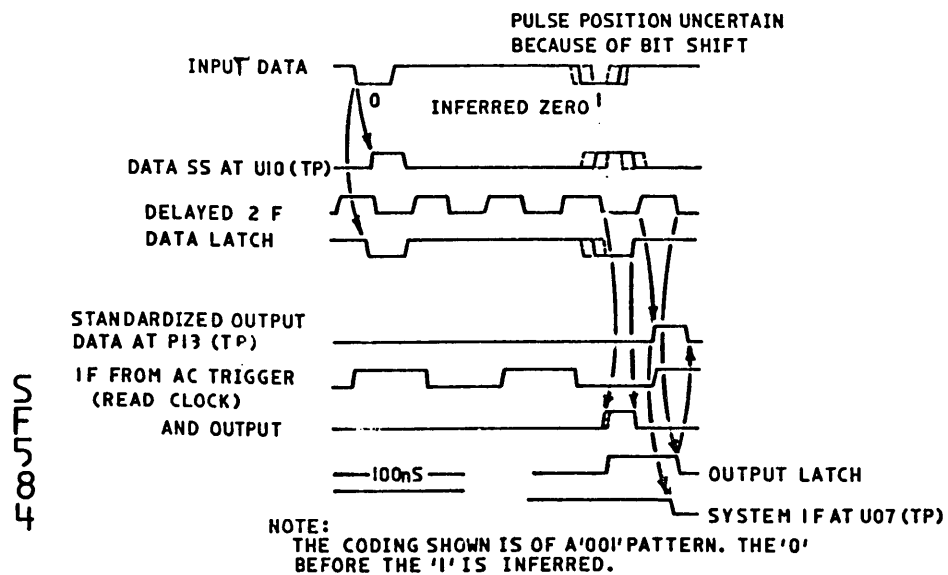
(DEFINITION OF '1S' AND '0S': A '1' BIT IS TRANSMITTED DURING THE SECOND HALF OF A 1F CLOCK CYCLE. A '0' BIT IS TRANSMITTED DURING THE FIRST HALF OF A 1F CLOCK CYCLE, EXCEPT WHEN A '0' IMMEDIATELY FOLLOWS A '1' BIT. IN THIS CASE, NO '1' BIT IS TRANSMITTED DURING THE 1F CLOCK CYCLE.)

NOTE: IN THE FOLLOWING DESCRIPTION IT ASSUMED THAT THE PHASE LOCKED LOOP IS 'LOCKED' TO THE AVERAGE PHASE AND FREQUENCY OF THE INPUT DATA SIGNAL.

THE INPUT DATA IS ROUTED THROUGH THE VCO SYNC CONTROL, WHICH, IN THE READ MODE, INVERTS THE DATA SIGNAL AND APPLIES IT THROUGH THE GATE (IN THIS MODE THE 'INHIBIT' SIGNAL ON THE GATE IS INEFFECTIVE) TO THE DATA LATCH AND THE SINGLE SHOT CIRCUIT. THE SINGLE SHOT CIRCUIT FORMS PART OF THE DISCRIMINATOR THAT CONTROLS THE PHASE OF THE PHASE-LOCKED LOOP.

IF THE DATA LATCH IS SET, THE DATA IS APPLIED TO AN AND GATE (THAT FORMS PART OF A MFM DECODER CIRCUIT) WITH A DELAYED '2F CLOCK' SIGNAL, AND A '1F' SIGNAL FROM THE AC TRIGGER. WHEN THESE THREE INPUTS ARE SATISFIED, THE OUTPUT OF THE AND CIRCUIT SETS THE '1S' LATCH; THIS LATCH PROVIDES AN OUTPUT WHEN A '1' IS DETECTED. THE OUTPUT OF THE '1S' LATCH IS APPLIED TO THE OUTPUT LATCH WHICH, IN TURN, GIVES AN OUTPUT SIGNAL IN THE FORM OF 30-NANOSECOND PULSES.

THE INITIALIZING LOGIC FORCES THE PHASE OF THE AC TRIGGER SO THAT THE 1F THAT THE TRIGGER PRODUCES CORRESPONDS TO THE TIMING OF BIT CELLS DURING FAST SYNCHRONIZATION.



EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIB2 READ DATA	
11 MAR 80	375662	MACH 4963	
		PART NO 6839643	
C	CLASSIFICATION		IBM CORP

LOGIC 1 CARD (C2)

INTERRUPT SENSE CYCLE

SENSE COMMAND CYCLE AFTER A POWER-UP

NOTE: THE NUMBERS QUOTED IN THE CIRCLES REFER TO THEIR CORRESPONDING NUMBERS SHOWN IN THE TIMING DIAGRAM.

THE FOLLOWING USER SYSTEM-TO-DSD SENSE STATUS SEQUENCE OCCURS AFTER AN INTERRUPT ① :

1. TAG CODE 100 (TAG 4) ② IS SET BY THE SYSTEM.
2. AFTER A DELAY OF 100 NANoseconds, 'CONTROL SAMPLE' ③ IS SET.
3. THE DSD READS THE TAG CODE ④ AND SETS THE SENSE DATA ON THE CONTROL BUS ⑤ ; 'CONTROL SAMPLE RECEIVED' ⑥ IS ALSO SET.
4. CONTROL BUS READ INFORMATION ⑦ IS READ BY THE SYSTEM, THEN 'CONTROL SAMPLE' IS RESET.
5. THE DSD RECEIVES 'CONTROL SAMPLE' AND RESETS 'INTERRUPT', 'CONTROL SAMPLE RECEIVED', AND ('SLIGHTLY DELAYED) THE CONTROL BUS.
6. DSD INTERNAL TIMING GATES OFF THE 'HOLD OFF INTERRUPT' WHICH RESETS 'INTERRUPT'.

TAG	SEEK CONTROL	DES'D ADDRESS	WRAP BACK	SENSE	DIAG SENSE 1	DIAG SENSE 2	DIAG SENSE 3	
001		010	011	100	101	110	111	
BUS	0	1	2	3	4	5	6	7
	RECAL	128		FIXED HD NOT SEL	ON TRACK	BEHIND HOME	NOT SHIFT	
	FIX HD SEL	64		BRAKE APPLIED	LIN REG N & EV	MISSING CKS ÷ 2	NOT OFF TRK WRITE	
	HEAD SEL 8	32		TRACK UNAVAIL	MISG IND & SECT	NOT MISG CK ERR LTH	INSIDE AGC WINDOW	
	HEAD SEL 4	16		COMMAND ERROR	OUT DIRECTION	COIL 1 LOW	-AGC FREEZE	
	HEAD SEL 2	8		UNSAFE	NOT DRIVE OUT	MISS SERVO SIG	DEMOSDS PULSING	
	HEAD SEL 1	4		SEEK INCPLT	NOT DRIVE IN	OFF DATA TRACK	NOT READ WRITE	
		2		HOME	TAG ERROR	NOT MISSING PES	NOT SERVO PROT WR	
	CYLINDER SEL	1		NOT READY	VEL PROFILE ERR	CTR 5 IN SYNC	ILLEGAL MOVE	

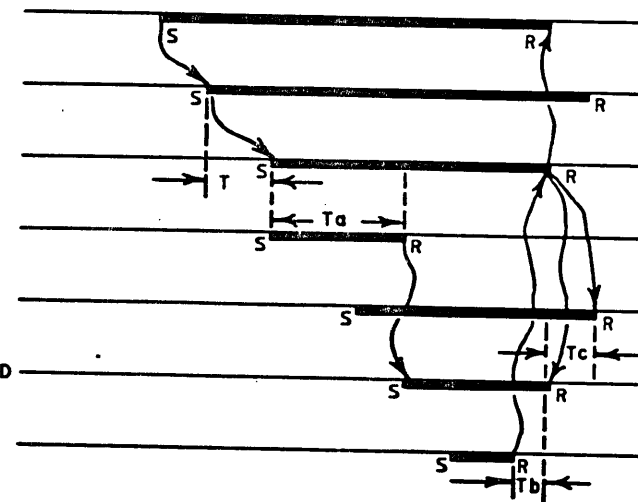
TIMING DIAGRAM

SEQUENCE AFTER DSD INTERRUPT

NOTE: THE TIMINGS SHOWN ARE AT THE DSD PIN LOCATIONS

- T = 100 nS MINIMUM
- Ta = 1 μS MINIMUM
- Tb = 500 nS MINIMUM
- Tc = 0 nS MINIMUM
- 30 nS MAXIMUM

1. INTERRUPT
2. TAG BUS VALID
3. CONTROL SAMPLE
4. TAG LINES READ
5. CONTROL BUS
6. CONTROL SAMPLE RECEIVED
7. CONTROL BUS READ



DSD INTERRUPT TO USING MACHINE

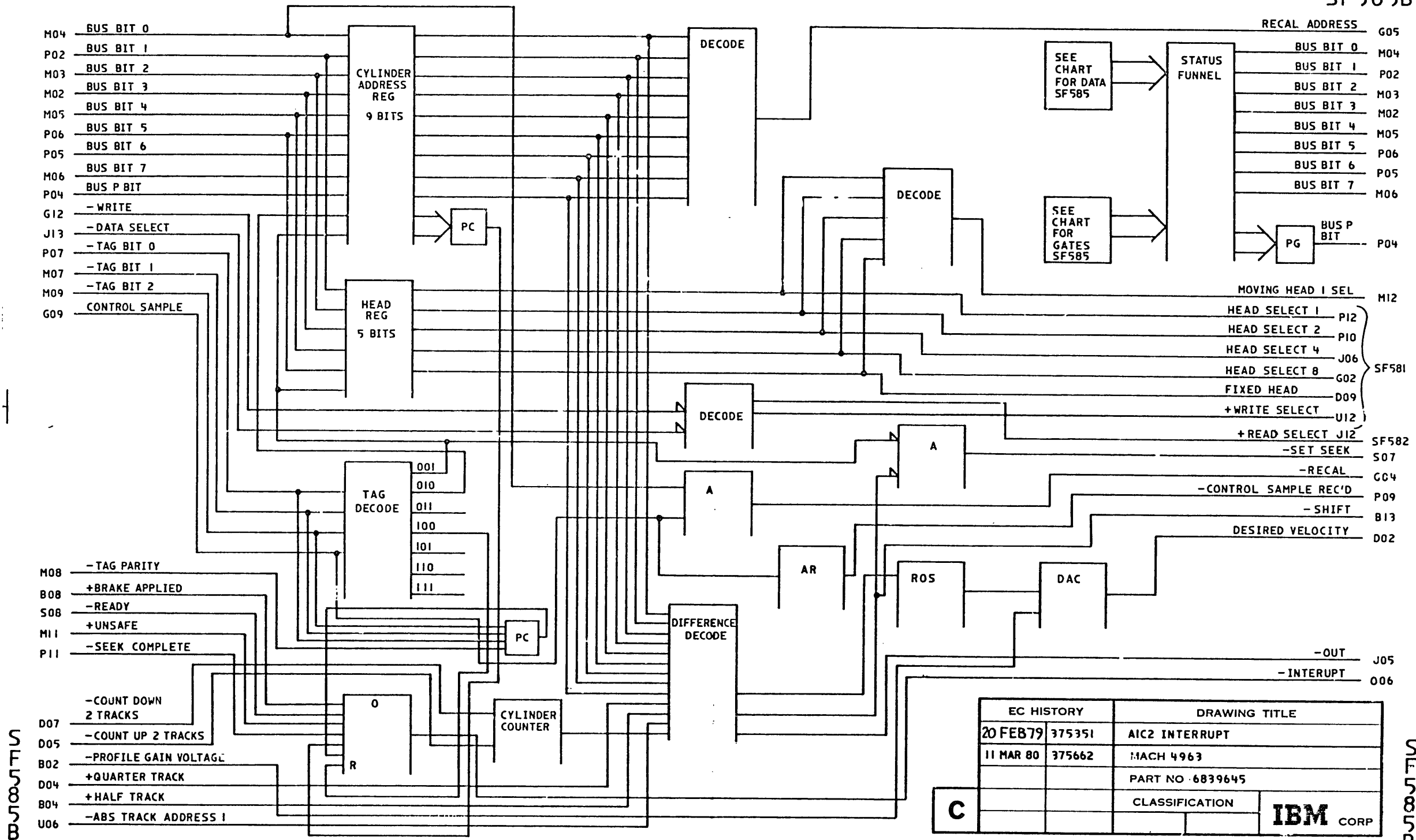
TAG DECODE TAG 100 (TAG 4)  
SENSE CYCLE TAG 100 (TAG 4)  
CONTROL BUS

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIC2 INTERRUPT	
		MACH 4963	
		PART NO 6839644	
C		CLASSIFICATION	IBM CORP

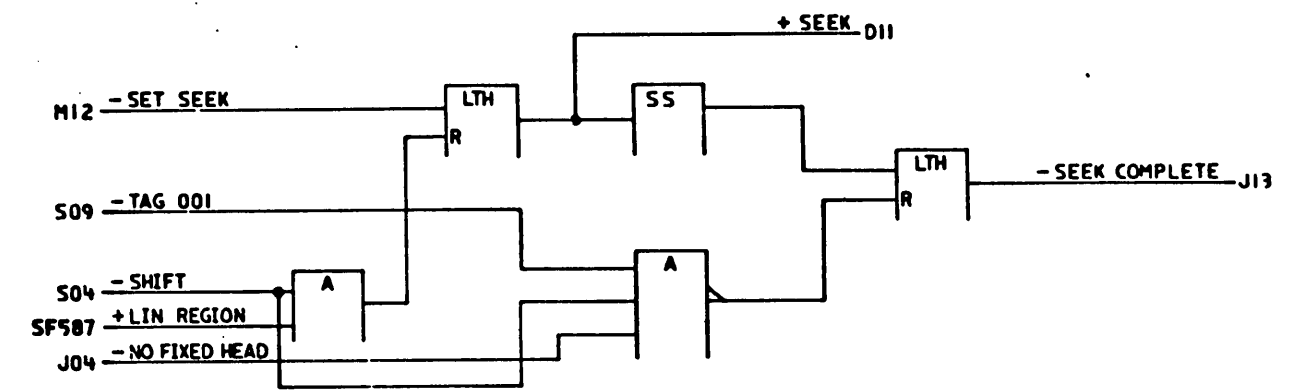
SF585A

SF585A

SF585B



EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIC2 INTERRUPT	
11 MAR 80	375662	MACH 4963	
		PART NO 6839645	
C		CLASSIFICATION	IBM CORP



LOGIC 2

WRITE CLOCK IS DIVIDED BY 16 BY COUNTERS. COUNTER 4 OUTPUT IS THE SAME FREQUENCY AS THE SERVO CLOCK SS. COUNTER 5 IS USED TO DISTINGUISH BETWEEN NORMAL AND QUADRATURE CELLS CORRESPONDING TO ALTERNATE SERVO CLOCK PULSES.

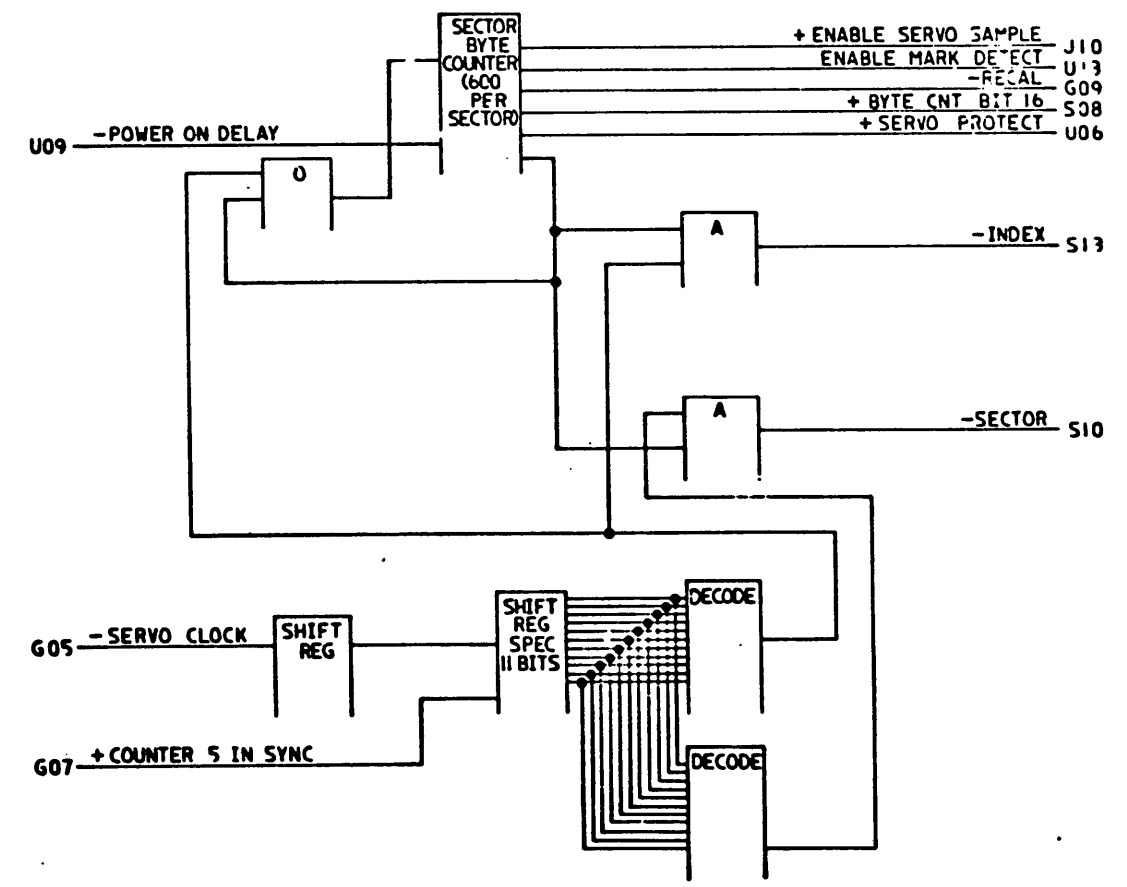
COUNTER 4 AND 5 OUTPUTS ARE DECODED INTO 4 OUTPUTS CORRESPONDING TO THE N1, N2 AND Q1, Q2. ANY OUT OF SYNC CONDITION WILL BE SIGNALED TO THE OSCILLATOR BY THE OSCILLATOR EARLY OR LATE LINES TO FORCE A FREQUENCY SHIFT TO BRING THE WRITE CLOCK BACK INTO SYNCHRONISM.

THE SYNC DETECTOR PROVIDES PROTECTION FOR ANY GROSS TIMING ERRORS.

MISSING CLOCK PULSES ARE FED TO A 1 BIT SHIFT REG AND DECODE TO LOOK FOR INDEX AND SECTOR PULSES.

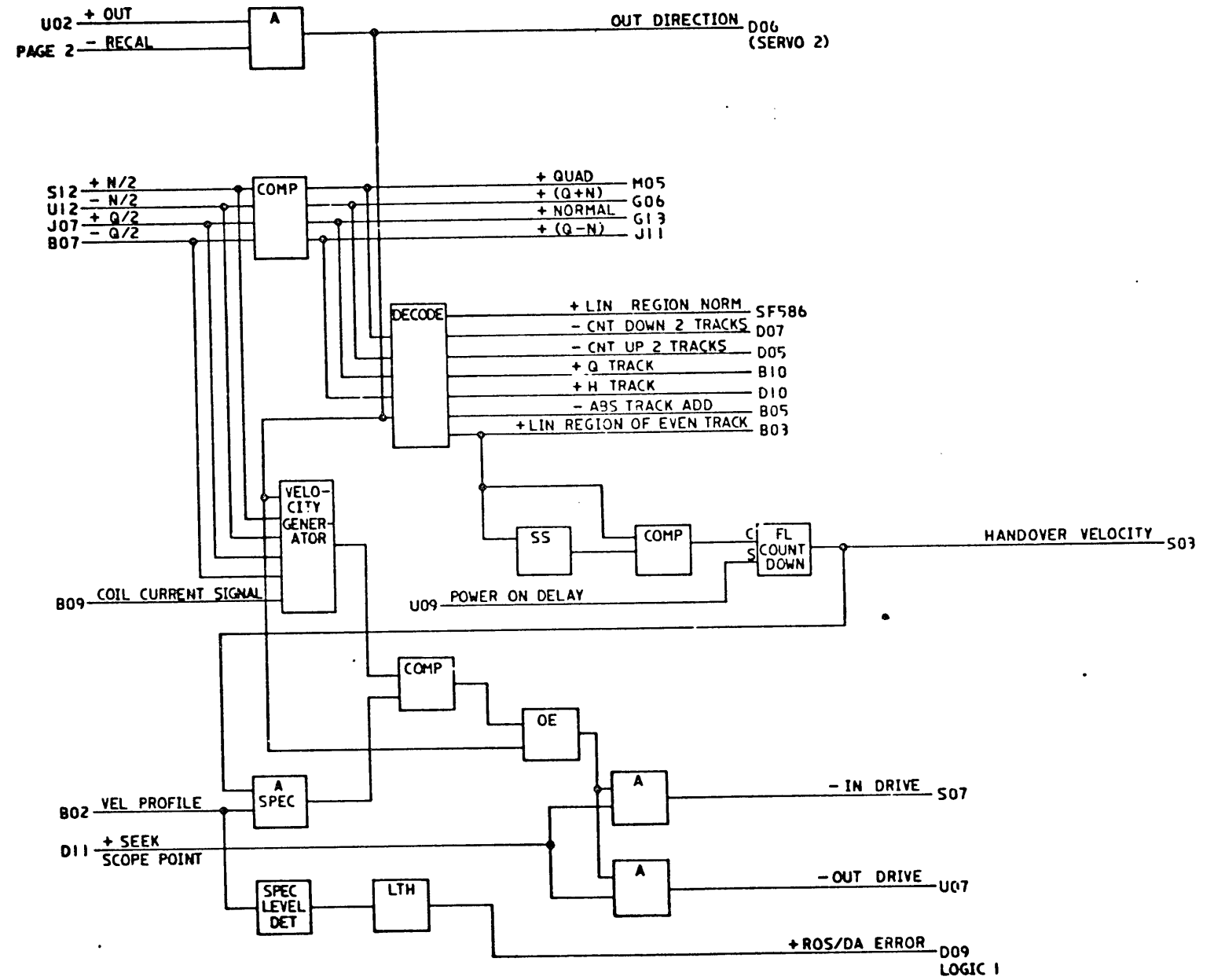
HANDOVER VELOCITY CALIBRATION IS USED AFTER POWER UP TO PROVIDE AN OFFSET VOLTAGE TO THE "DESIRED VELOCITY" VOLTAGE. THE REQUIRED OFFSET IS GENERATED BY PRESETTING THE COUNTER AT THE START OF HVC TO 7 AND CHECKING VELOCITY OVER 2 TRACKS. IF VELOCITY IS 1.9mm PER TRACK THE COUNTER IS DECREMENTED BY 1 AND THE CYCLE REPEATED UNTIL THE TIME IS 1.9mm/TRACK OR UNTIL THE COUNTER HAS REACHED 0 WHEN ALLOW HVC IS RESET.

PROFILE GAIN VOLTAGE IS RECALIBRATED IN A SIMILAR METHOD EXCEPT THAT THE COUNTER IS RESET TO ZERO AND INCREMENTS UP UNTIL +VEL PROF DROPS OR THE COUNTER IS FULL. "COUNTER FULL" PREVENTS THE COUNTER RESETTING TO ZERO IF ITS MAXIMUM COUNT IS EXCEEDED. RECALIBRATION ONLY TAKES PLACE ON COMMAND FROM THE SYSTEM.



68375

EC HISTORY		DRAWING TITLE	
20FEB79	375351	AID2 SECTOR AND INDEX	
		MACH 4963	
		PART NO 6839646	
		CLASSIFICATION	IBM CORP
D			



EC HISTORY		DRAWING TITLE	
20FEB79	375351	A1D2 HANDOVER VELOCITY	
		MACH 4963	
		PART NO 6839647	
		CLASSIFICATION	IBM CORP

D

515587

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PHASE LOCKED OSCILLATOR (PLO) LOOP

THE PLO IS SYNCHRONIZED IN PHASE AND FREQUENCY BY THE SERVO SIGNAL CLOCK PULSES AS FOLLOWS:

THE VOLTAGE CONTROLLED OSCILLATOR (VCO) RUNS AT APPROXIMATELY 16.5 MHz. THE OUTPUT 2F IS DIVIDED BY 2 TO GIVE '1F WRITE CLOCK'.

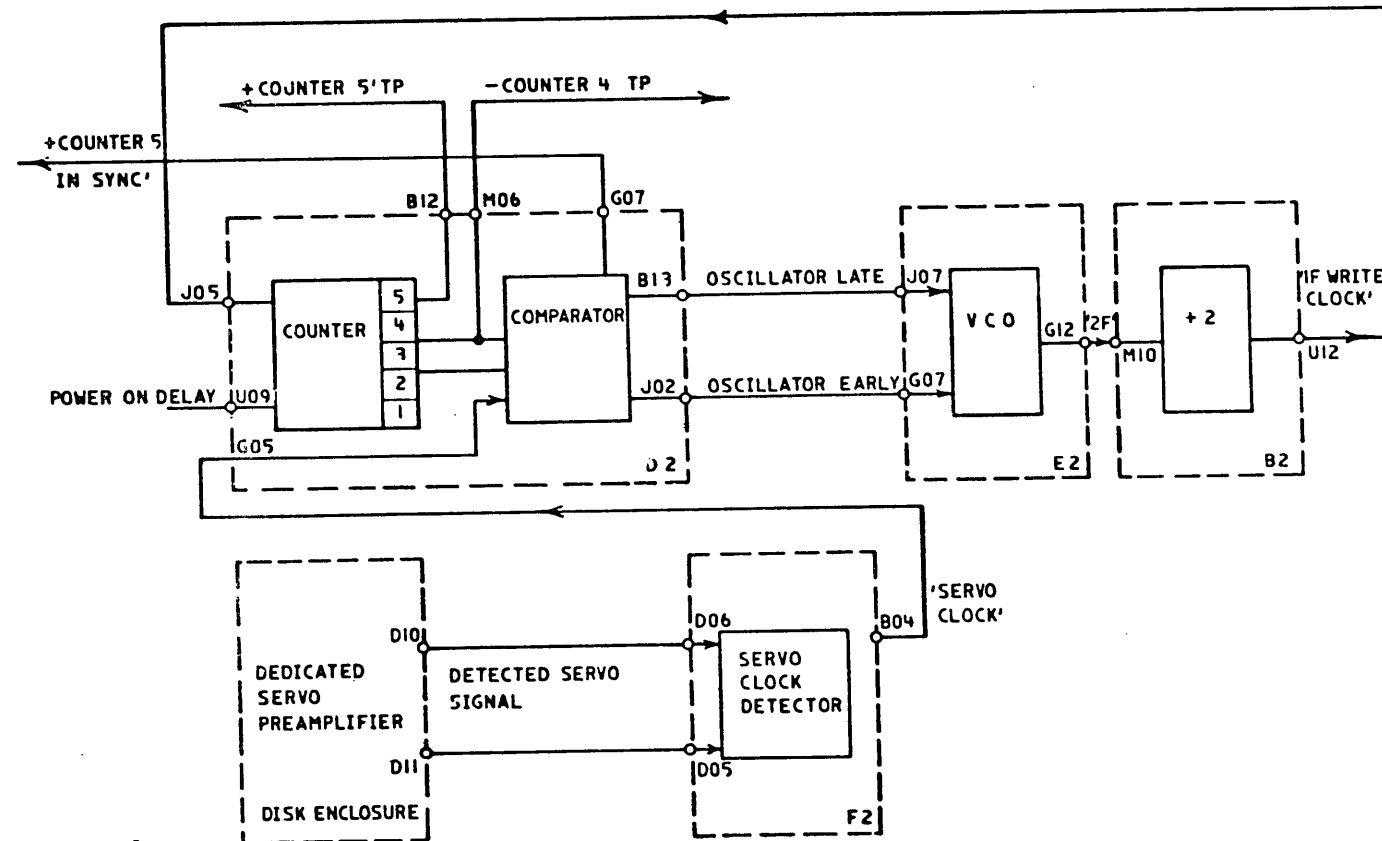
'1F WRITE CLOCK' DRIVES A 5 BIT COUNTER; 'COUNTER 4' OUTPUT IS 1/16TH OF THE PLO FREQUENCY. THE 'SERVO CLOCK' PULSES TRIGGER A SINGLE SHOT (+ SERVO CLOCK SS - 280 nS).

FOR THE PLO TO BE IN SYNCHRONIZATION THE TRAILING EDGE OF THE SERVO CLOCK SS MUST COINCIDE WITH THE MID POINT OF THE NEGATIVE LEVEL OF THE 'COUNTER 4' SIGNAL.

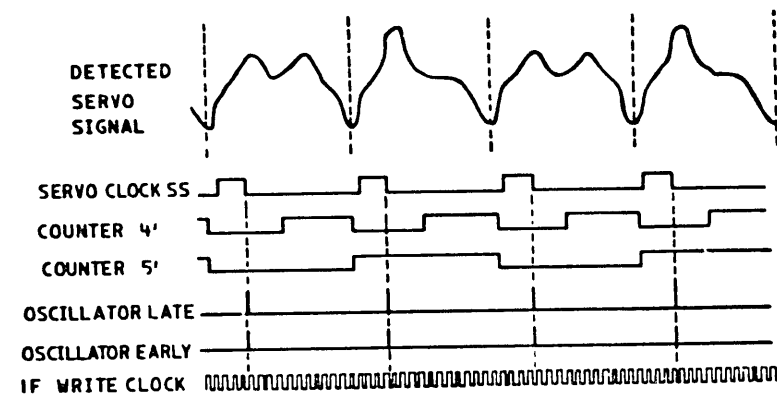
A COMPARATIVE CIRCUIT ON THE LOGIC 2 (D2) CARD LOOKS FOR THIS COINCIDENCE AND PROVIDES AN OUTPUT OF OSCILLATOR EARLY OR LATE TO THE VCO TO CORRECT ANY MISALIGNMENT.

DURING NORMAL SYNCHRONOUS OPERATION, NARROW OSCILLATOR LATE AND OSCILLATOR EARLY SIGNALS ARE PRODUCED CONTINUOUSLY AS SHOWN IN THE TIMING DIAGRAM.

THE PLO IS USED BY THE USING SYSTEM TO SERIALIZE WRITE DATA.



PLO DIAGRAM



PLO TIMING DIAGRAM

EC HISTORY		DRAWING TITLE	
20 FEB 77	375 351	AID2 PLO	
		MACH 4963	
		PART NO 6839648	
C		CLASSIFICATION	IBM CORP

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**SERVO CONTROL E2 SERVO 1**

**SERVO MARKER FIELD**

THE SERVO MARKER FIELD CONTAINS A PATTERN SEQUENCE OF POSITIVE ZERO CROSSINGS (9) (POSITIVE GOING PULSES THAT PASS THROUGH 0 (ZERO) VOLTS) THAT SYNCHRONIZE THE DEMODULATOR WAVEFORMS 'SELECT DEMOD A', AND 'SELECT DEMOD B'.

**SERVO GAIN FIELD**

THE SERVO GAIN FIELD IS JUST OVER TWO BYTES OF EACH 22-BYTE SERVO SAMPLE FIELD. IN THE SERVO GAIN FIELD, A FIXED-AMPLITUDE SIGNAL CALLED 'DATA SURFACE LINEAR' (1) CONTROLS THE AUTOMATIC GAIN CONTROL (AGC) LOOP SO THAT THE LOOP COMPENSATES FOR CHANGES DUE TO:

- HEAD-TO-DISK SURFACE VARIATIONS.
- SURFACE CHANGES.
- TRACK LOCATION VARIATIONS THAT OCCUR BECAUSE OF DIFFERENCES IN LINEAR SPEED BETWEEN INNER TRACKS AND OUTER TRACKS, AND, THUS, COUPLING BETWEEN HEAD AND DISK SURFACE.

THE AGC LOOP COMPRISES THE VARIABLE GAIN AMPLIFIER (VGA) AND THE AGC AMPLIFIER.

THE 'SELECT GAIN ADJUST' SIGNAL (2) IS ACTIVE THROUGHOUT THE SERVO GAIN FIELD. THIS CAUSES THE DEMODULATOR TO GIVE AN OUTPUT THAT IS ASYNCHRONOUSLY RECTIFIED AND THEN APPLIED TO THE AGC LOOP. THE AGC LOOP INVERTS THE DEMODULATOR OUTPUT AND SUBTRACTS IT FROM THE 'TRACK REFERENCE SIGNAL' (3). THE DIFFERENCE VOLTAGE CHARGES THE GAIN STORE CAPACITOR C2.

THE RESULTING GAIN VOLTAGE ACROSS THE GAIN STORE CAPACITOR C2 IS FILTERED AND BUFFERED IN THE AGC AMPLIFIER. THE AMPLIFIER THEN PRODUCES A SIGNAL TO THE NEW LEVEL REQUIRED FOR THE PARTICULAR SECTOR IF EITHER 'ENABLE SERVO SAMPLE' (4) IS ACTIVE, OR IF 'ENABLE SERVO SAMPLE' (4) AND 'HEAD CHANGE GATE' (5) ARE ACTIVE 'ENABLE SERVO SAMPLE' (4), WHICH IS ACTIVE FOR THE WHOLE OF THE SAMPLE SERVO FIELD, REDUCES THE GAIN OF THE AGC AMPLIFIER (TO WITHIN THE LIMITS (6) SHOWN ON THE TIMING DIAGRAM) IN OPERATIONS OUTSIDE THE SAMPLE SERVO FIELD. THE 'HEAD CHANGE GATE' (5) COMPENSATES FOR HEAD RESPONSE DURING A HEAD-CHANGE OPERATION.

IF THE AGC VOLTAGE IS EITHER TOO SMALL, OR ABSENT COMPLETELY, AN AGC DETECTOR CAUSES THE AMPLIFIER TO GIVE AN 'OUTSIDE AGC WINDOW' OUTPUT SIGNAL (6), WHICH IS INDICATED A 'TAG 111' (THAT IS, TAG 7) DIAGNOSTIC DATA.

THE GAIN STORE CAPACITOR C2 IS RESET AFTER THE END OF THE SERVO GAIN FIELD, WHEN THE 'RESET CAPACITOR' SIGNAL (7) IS ACTIVATED.

**SERVO ERROR FIELD**

THE SERVO ERROR FIELD IS 4.5 BYTES OF THE 22-BYTE SERVO SAMPLE FIELD. DURING THE SERVO ERROR FIELD, THE SERVO ERROR CIRCUIT MEASURES THE AMOUNT AND DIRECTION (EITHER IN OR OUT) THAT THE HEAD IS OFF TRACK, AND PRODUCES A 'DATA POSITION ERROR' SIGNAL THAT CORRESPONDS TO THE ERROR. THIS SIGNAL RETURNS THE HEAD ON TRACK TO READ OR WRITE DATA IN THE PARTICULAR SECTOR.

BEFORE THE SERVO ERROR FIELD OF A PARTICULAR SECTOR IS ENTERED, THE ERROR CAPACITOR C1 IS RESET BY 'RESET CAPACITOR' APPLIED TO IT THROUGH THE CIRCUIT. THEREFORE, NO VOLTAGE IS ACROSS C1. THUS THE 'DATA POSITION ERROR' SIGNAL FOR THE PREVIOUS SECTOR IS REMOVED.

IF A HEAD IS OFF-TRACK WHEN THE SERVO ERROR FIELD IS ENTERED, THE RESULTING ERROR SIGNAL CAUSES THE DEMODULATOR TO PRODUCE AN 'ERROR SAMPLE' SIGNAL. THE 'ERROR SAMPLE' IS SYNCHRONOUSLY RECTIFIED BY 'SELECT DEMOD A' AND 'SELECT DEMOD B' SYNCHRONIZED TO THE LINEAR SIGNAL ZERO CROSSINGS. THE RECTIFIED SAMPLE SIGNAL IS APPLIED TO THE ERROR CAPACITOR C1, CHARGING C1, OVER THE PERIOD OF THE SERVO ERROR FIELD, TO A LEVEL THAT CORRESPONDS TO THE AMOUNT OF ERROR. THE '+SELECT DEMOD A' AND '+SELECT DEMOD B' PULSES ARE SWITCHED ALTERNATELY ON AND OFF WITH RESPECT TO EACH OTHER, AT TIMES DETERMINED BY THE DECODING AND GATING OUTPUT OF COUNTER 2. THE POLARITIES OF THESE DEMODULATOR SIGNALS DEPEND ON WHETHER THE TRACK IS ODD OR EVEN NUMBERED.

THE ERROR VOLTAGE ON C1 IS APPLIED TO THE OPERATIONAL AMPLIFIER, SWITCHED AS A VOLTAGE FOLLOWER BY THE '+ENABLE DATA' AND '-ENABLE DATA' INPUTS, AND THE OPERATIONAL AMPLIFIER PROVIDES THE 'DATA POSITION ERROR' SIGNAL AT ITS OUTPUT.

THE 'DATA POSITION ERROR' SIGNAL IS APPLIED TO THE HEAD ACTUATOR COIL VIA A COMPENSATOR CIRCUIT (NOT SHOWN). THIS MOVES THE HEAD TO THE ON-TRACK POSITION SO THAT THE DATA FIELD THAT FOLLOWS THE SERVO ERROR FIELD, WITHIN THE SAME SECTOR, CAN BE READ OR WRITTEN.

**TIMING REFERENCE**

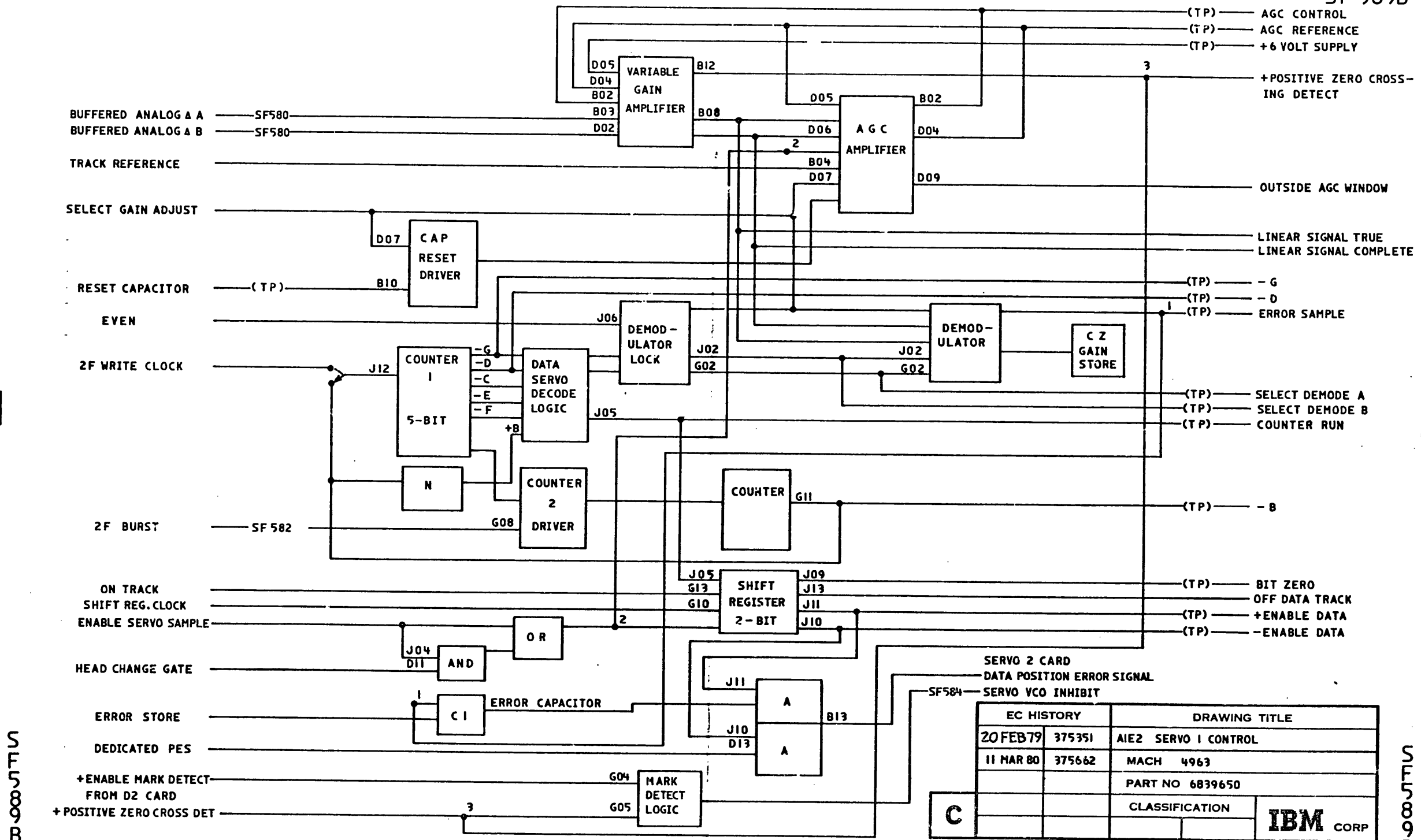
TIMING IN THE SAMPLE SERVO FIELD, BETWEEN THE BEGINNING OF THE ID MARKER FIELD AND THE END OF THE SERVO ERROR FIELD, IS BASED ON A REFERENCE FREQUENCY PROVIDED BY THE DEDICATED SERVO HEAD. PHASE CORRECTION OF THIS FREQUENCY IS PROVIDED BY THE MARK DETECT LOGIC CIRCUIT.

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EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIE2 SERVO 1 CONTROL	
		MACH 4963	
		PART NO 6839649	
C		CLASSIFICATION	IBM CORP

SF 589B



EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIE2 SERVO 1 CONTROL	
11 MAR 80	375662	MACH 4963	
		PART NO 6839650	
		CLASSIFICATION	IBM CORP

B 00000

B 00000



SF590A

**SERVO 1 (E2)**

**SAMPLE SERVO MARKER FIELD**

**MARKER FIELD**

THE ALTERNATING PEAKS IN THE 'OFF TRACK' SIGNAL MEASURE OFF-TRACK ERROR. THE PEAKS ARE SYNCHRONOUSLY RECTIFIED IN RELATION TO A SQUARE WAVE SIGNAL (G02, J02) SYNCHRONIZED TO THE LINEAR SIGNAL ZERO CROSSINGS. THIS PRODUCES A SIGNAL PROPORTIONAL TO THE OFF-TRACK ERROR, THAT IS USED TO POSITION THE HEADS CORRECTLY OVER THE PARTICULAR TRACK.

THE OUTPUT OF THE MARK DETECTOR RELEASES THE VOLTAGE CONTROLLED OSCILLATOR (VCO) FROM THE CONTROL OF THE DEDICATED SERVO SURFACE, TO WHICH IT WAS PHASE LOCKED. THE VCO FREE RUNS AT THE RELEASE FREQUENCY FOR THE 10 MICRO-SECOND PERIOD OF THE SERVO GAIN AND ERROR FIELDS. DURING THAT PERIOD, THE VCO OUTPUT GENERATES THE CONTROL AND GATING SIGNALS.

**NOTE:** ANY SMALL VELOCITY ERROR DURING THIS PERIOD CAN BE IGNORED.

THE SIGNALS '+ SELECT GAIN ADJUST', '- RESET CAPACITOR', '+ SELECT DEMOD A' AND '+ SELECT DEMOD B' ARE DERIVED BY DECODING THE OUTPUTS OF COUNTER 1 AND COUNTER 2 (FIVE-BIT COUNTERS). THESE COUNTERS ARE CONTROLLED BY THE 'COUNTER RUN' LINE THAT IS ACTIVATED AT A POINT ON THE SAMPLE SERVO SIGNAL (MARKER).

**THE COUNTER:**

- CONTROLS A LOGIC SWITCH IN THE CLOCK CONTROL. THE SWITCH CONNECTS EITHER '2F WRITE CLOCK', OR THE OUTPUT OF COUNTER 2 INTO THE CLOCK INPUT OF COUNTER 1.
- INHIBITS THE ANALOG CONTROL SIGNALS (WHEN THE COUNTER IS DEACTIVATED).

WHEN 'COUNTER RUN' IS DEACTIVATED, COUNTER 1 RUNS FROM THE START OF 'ENABLE MARK DETECT', AND RESETS AT EVERY CHANGE OF '+ POSITIVE ZERO CROSSING'. IF THE COUNTER 1 REACHES A COUNT OF '-F', THE NEXT ZERO CROSSING SETS '+ SERVO VCO INHIBIT', AND RESETS THE COUNTER 1.

IF THE NEXT ZERO CROSSING OCCURS WHEN '-F' IS NOT ACTIVE, THE SERVO MARKER IS RECOGNIZED, '+ SERVO VCO INHIBIT' IS RESET, AND 'COUNTER RUN' IS ACTIVATED.

'SERVO VCO INHIBIT' RELEASES CONTROL OF THE VCO, FROM THE DEDICATED SERVO SURFACE; THE VCO THEN PRODUCES THE '2F BURST'. 'COUNTER RUN' SWITCHES THE COUNTER 1 'CLOCK' TO THE OUTPUT OF COUNTER 2. COUNTER 1, WHICH DIVIDES BY SIX, IS DRIVEN BY '2F BURST', VIA A SINGLE BIT COUNT IN COUNTER 2, AND ADVANCES ON BOTH POLARITIES OF THE INPUT SIGNAL.

WHEN 'COUNTER RUN' IS ACTIVE, IT ALSO INHIBITS THE RESET OF COUNTER 1, AND ALLOWS ANALOG CONTROL DECODE TO OPERATE. THIS PRODUCES GAIN, DEMODULATOR AND RESET CAPACITOR SIGNALS.

THE 'SELECT GAIN ADJUST' LINE IS CONTROLLED BY 'DEFAULT GATE' OR 'HEAD CHANGE GATE'. A TWO-BIT SHIFT REGISTER CONTROLS THE 'ENABLE DATA' LINES.

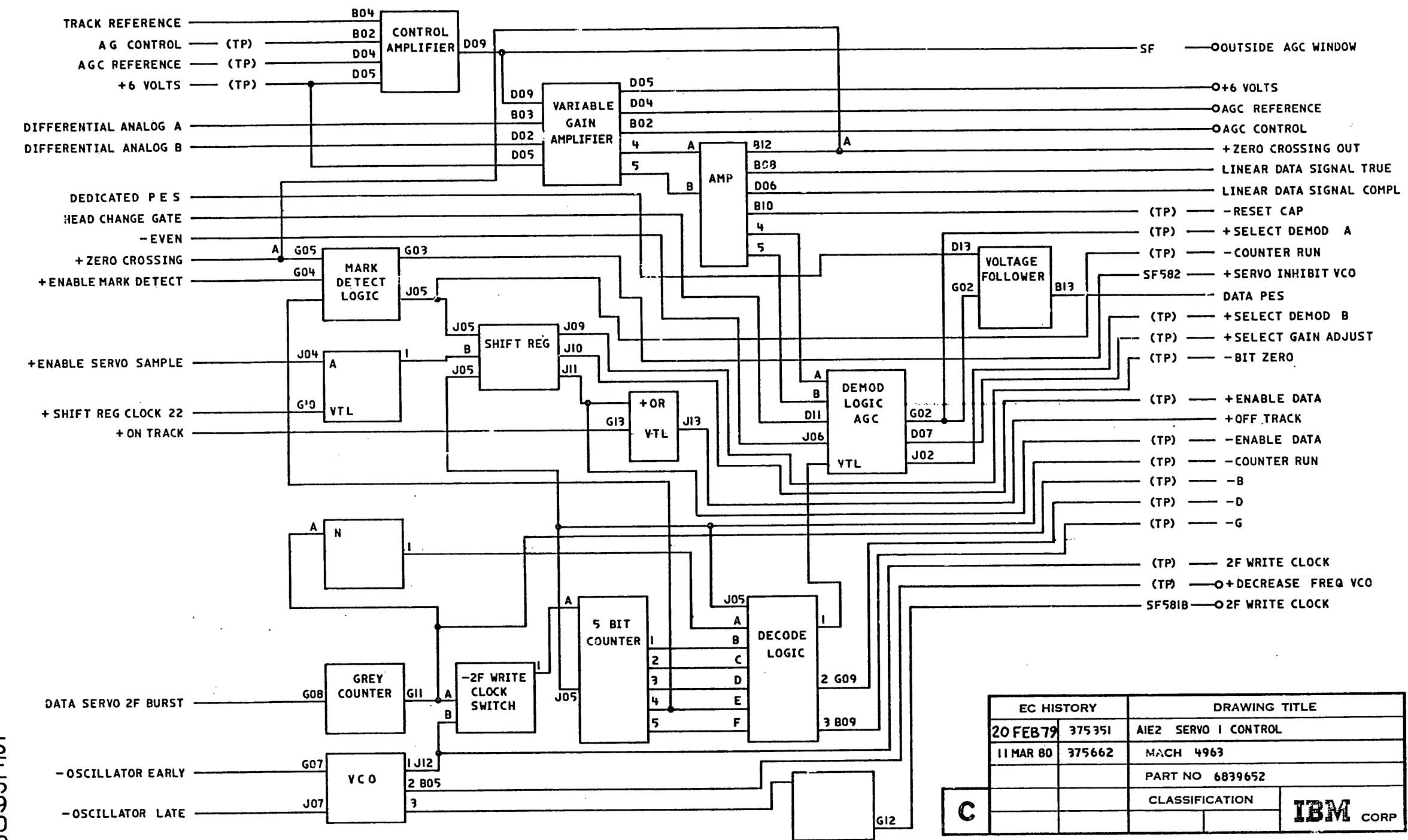
'COUNTER RUN' APPLIED TO THE SHIFT REGISTER INDICATES THAT A SAMPLE HAS BEEN FOUND THAT IS CLOCKED BY '+ SHIFT REGISTER CLOCK', A SIGNAL DERIVED FROM THE DEDICATED SERVO SURFACE. THE GATING CAUSES 'ENABLE DATA' TO BE ACTIVATED ON THE SECOND SAMPLE FOUND AND DEACTIVATED ON THE THIRD SAMPLE FOUND.

SF590A

SF590A

EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	A1E2 SERVO 1 CONTROL	
		MACH 4963	
		PART NO 6839651	
C		CLASSIFICATION	IBM CORP

SF5908



EC HISTORY		DRAWING TITLE	
20 FEB 79	375351	AIE2 SERVO I CONTROL	
11 MAR 80	375662	MACH 4963	
		PART NO 6839652	
C		CLASSIFICATION	IBM CORP

SERVO 2 LOCATION F2

THIS CARD CONSISTS OF FIXED AND VARIABLE GAIN AMPLIFIERS TO AMPLIFY THE DIFFERENTIAL OUTPUT FROM THE DEDICATED SERVO READ HEADS TO A CONSTANT OUTPUT LEVEL. INCLUDED IS CIRCUITRY TO DETECT SERVO CLOCK PULSES WHICH FIRE A 280  $\mu$ SEC SINGLE SHOT.

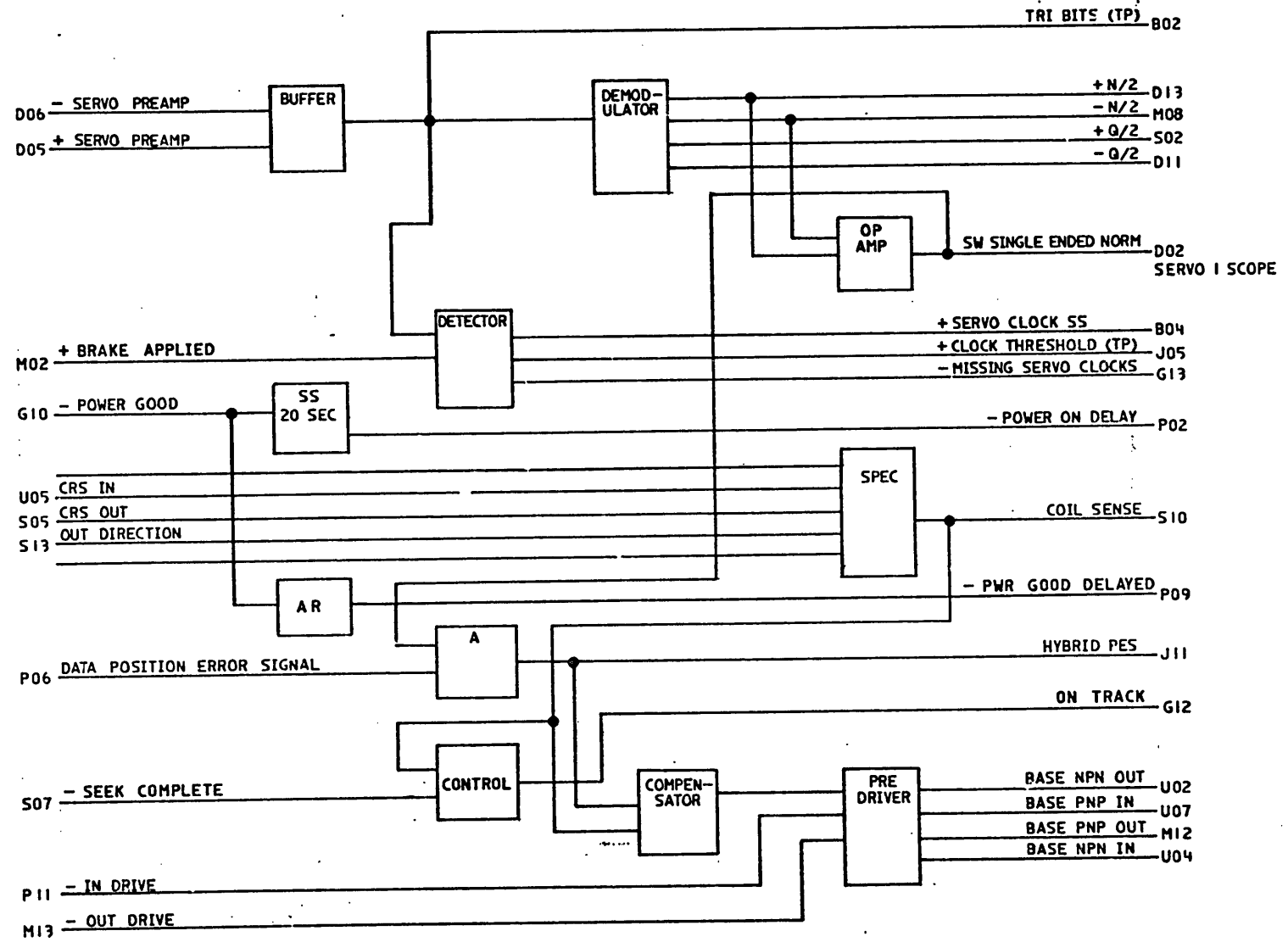
PEAKS ON THE AMPLIFIED OUTPUT ARE DETECTED AND SELECTED BY THE SEL N1, N2, Q1 AND Q2 LINES INTO THEIR RESPECTIVE  $\pm N/2$  AND  $\pm Q/2$  OUTPUTS, CORRESPONDING TO THE NORMAL AND QUADRATURE FIELDS RECORDED ON THE SERVO SURFACE.

THE N SIGNALS AND THE Q SIGNALS ARE FED TO BUFFERS. THE INPUT IS HOWEVER INVERTED TO ONE BUFFER. SERVO SIGNALS ON THE DEDICATED SURFACES ARE INVERTED IN PHASE ON ALTERNATE TRACKS WHICH ALLOW SELECTION OF THE CORRECT POLARITY OF THE OUTPUT SIGNAL. "DATA PES" FROM SERVO 1 IS COMBINED TO FORM A "HYBRID PES O/P".

THE "DELAY" IN "POWER GOOD DELAYED" IS OF THE ORDER OF  $\mu$ SECS AND ENTIRELY DUE TO CIRCUIT DELAYS IN THE FILTERS.

THE VOLTAGES DEVELOPED ACROSS CURRENT SENSE RESISTORS (CSR) ON THE D.E. DRIVE BOARD TO DETECT LOW VOICE COIL MOTOR CURRENT. "+OUT DIRECTION" CONTROLS THE INPUT POLARITY TO ENSURE CORRECT OUTPUT FOR BOTH DIRECTIONS OF ACCESS ARM TRAVEL. VCM START AND FINISH ARE DIRECT CONNECTION TO THE VOICE COIL WINDINGS AND PROVIDE COMPENSATION TO THE AMPLIFIER. "VOICE COIL CURRENT SIGNAL" IS A VOLTAGE LEVEL WHICH IS PROPORTIONAL TO THE VOICE COIL CURRENT. THE VOICE COIL CURRENT SIGNAL IS AMPLIFIED WHEN "SEEK COMPLETE" IS ACTIVE AND ENSURES THAT THERE IS MINIMAL VOICE COIL CURRENT. "+ ON TRACK" DROPS IF SUFFICIENT VOICE COIL CURRENT IS DETECTED TO MOVE THE ACCESS ARM OFF TRACK.

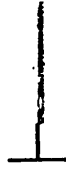
"HYBRID PES." "SEL INT" PROVIDES CONTROL OF A CAPACITOR WHICH HOLDS THE "HYBRID PES" LEVEL CONSTANT DURING ACCESSING TO REDUCE TRANSIENTS AT ACCESS COMPLETION. THE SIGNAL DRIVES THE VOICE COIL MOTOR TRANSISTOR MATRIX. "IN DRIVE" AND "OUT DRIVE" OVERRIDE THE INPUT SIGNAL AND FORCE THE ACCESS DRIVE INTO FULL IN OR OUT MOTION.



EC HISTORY		DRAWING TITLE	
20FEB79	375351	AIF2 SERVO 2 CARD	
		MACH 4963	
		PART NO 6839653	
C		CLASSIFICATION	IBM CORP

1-9156

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SF599

NOTE: SCOPE PICTURES GO WITH MAP 7A74

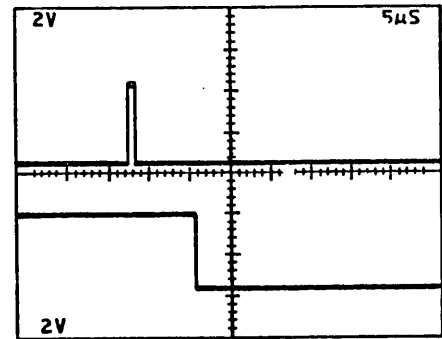


FIGURE 1

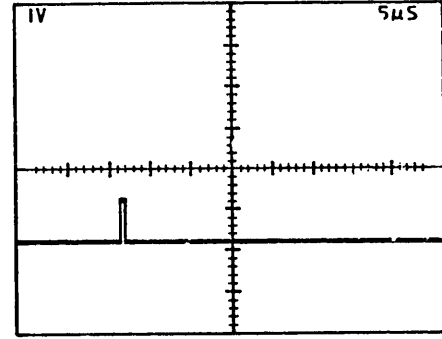


FIGURE 2

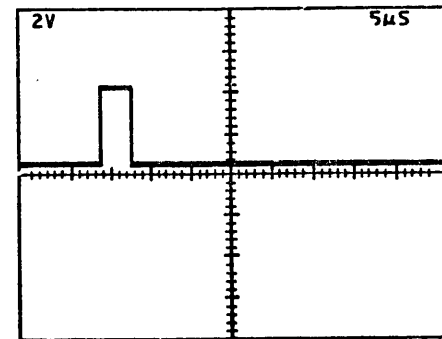


FIGURE 3

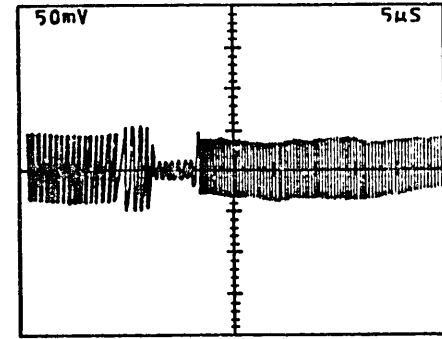


FIGURE 4

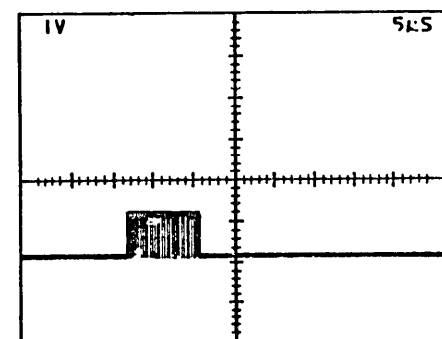


FIGURE 5

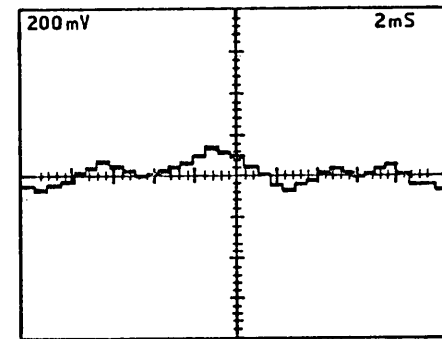


FIGURE 6

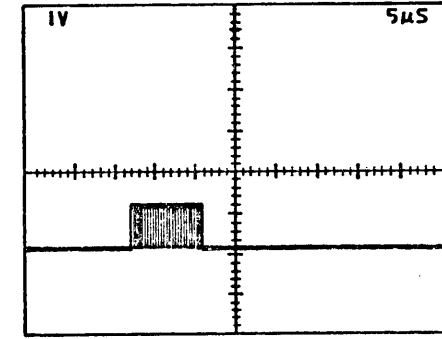


FIGURE 7

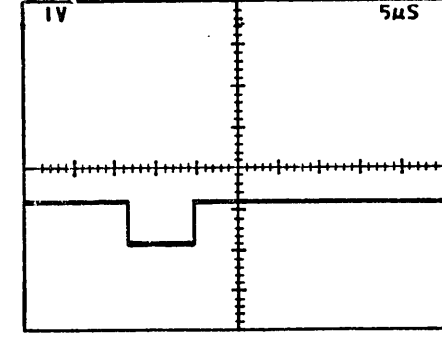


FIGURE 8

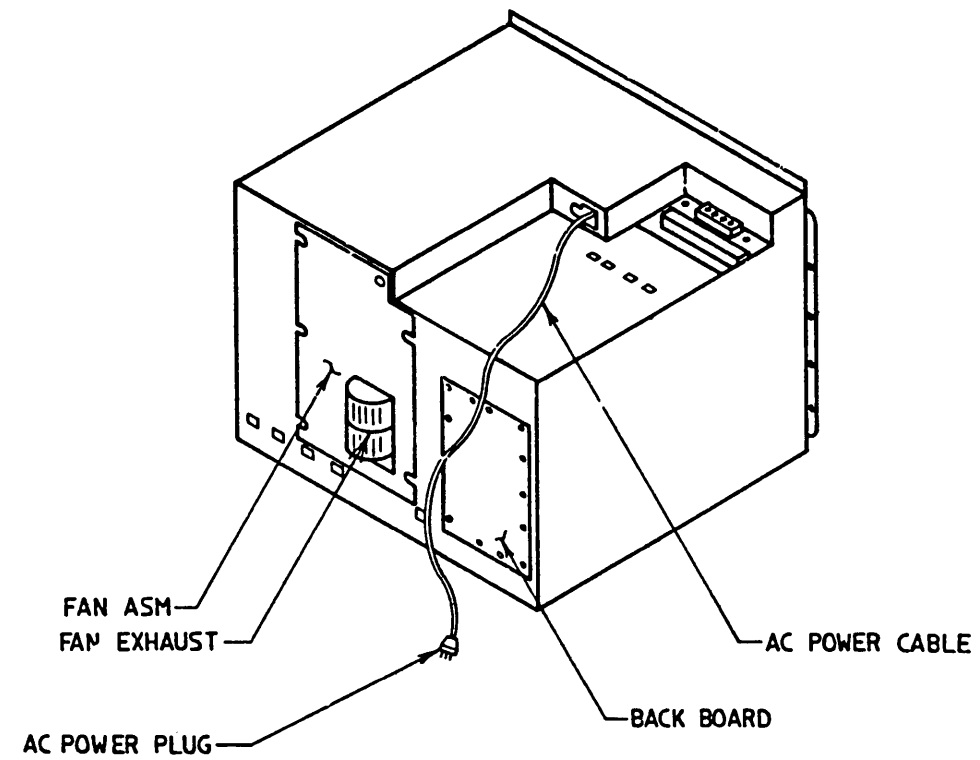
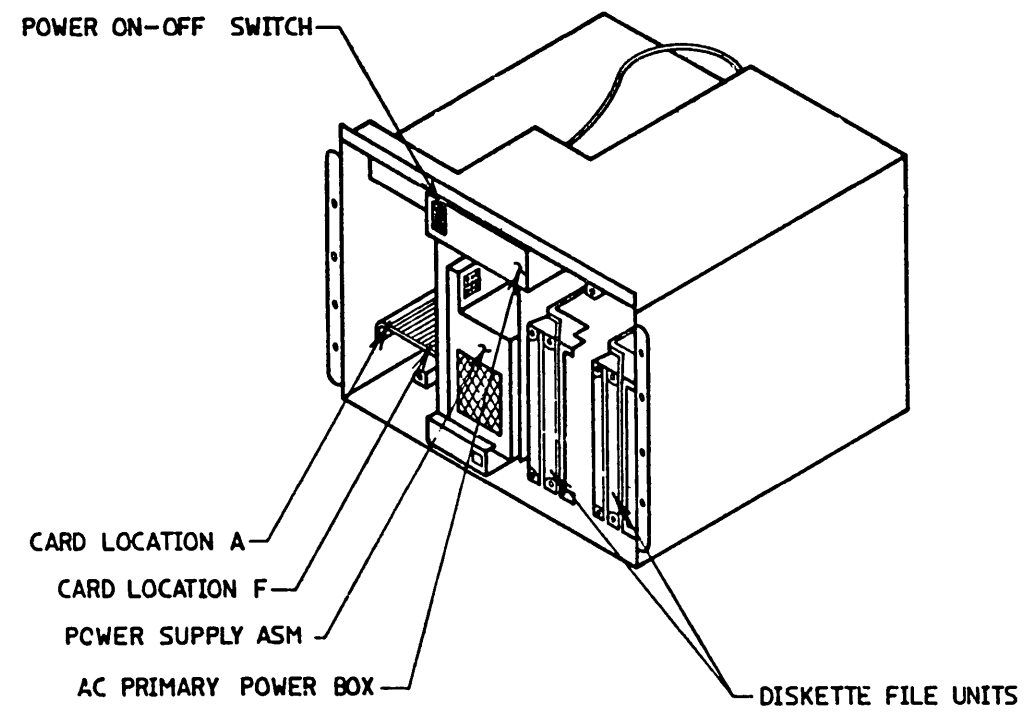
995715

EC HISTORY		DRAWING TITLE	
9APR80	375662	MAP 7A74 SCOPE PICTURES	
		MACH 4963	
		PART NO 6846296	
C	CLASSIFICATION		IBM CORP

995715



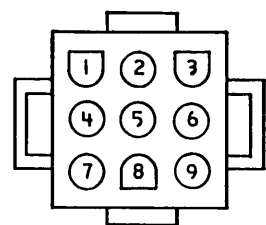
YB250



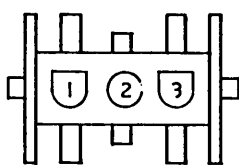
Y  
B  
2  
5  
0

EC HISTORY		DRAWING TITLE	
15 JAN 81	987627	CARD FILE COMPONENT LOC 230W	
11 MAR 81	987996	MACH	
		PART NO 6844506	
<b>C</b>		CLASSIFICATION	<b>IBM</b> CORP

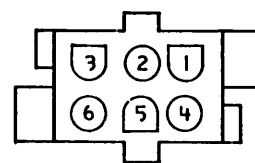
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PI (MATING VIEW)



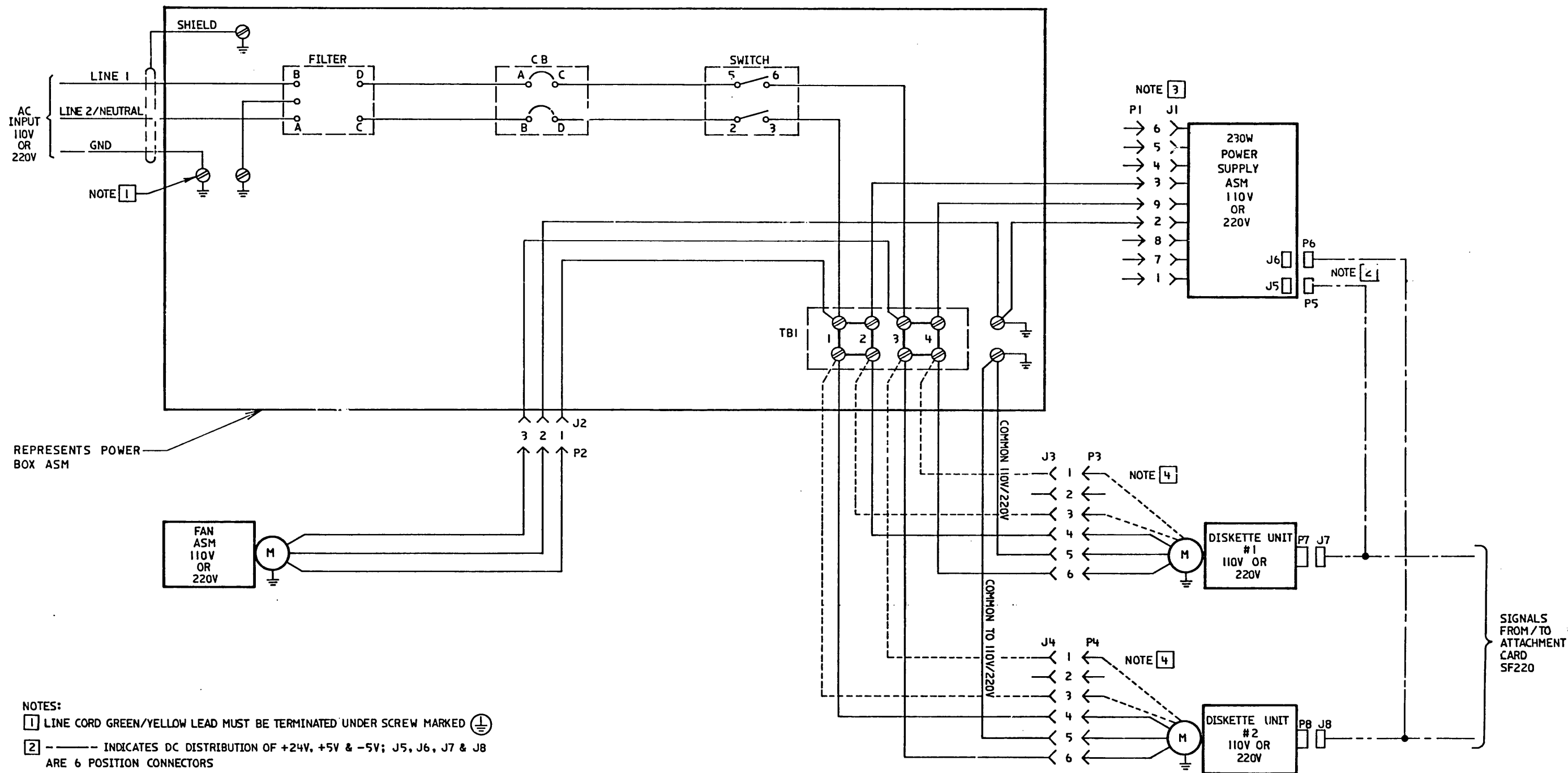
J2 (MATING VIEW)



J3 OR J4 (MATING VIEW)

CHART A

JUMPERING	
110V	220V
POS 3 - POS 7	
POS 9 - POS 8	POS 7 - POS 8
POS 8 - POS 1	POS 8 - POS 1



REPRESENTS POWER BOX ASM

NOTES:

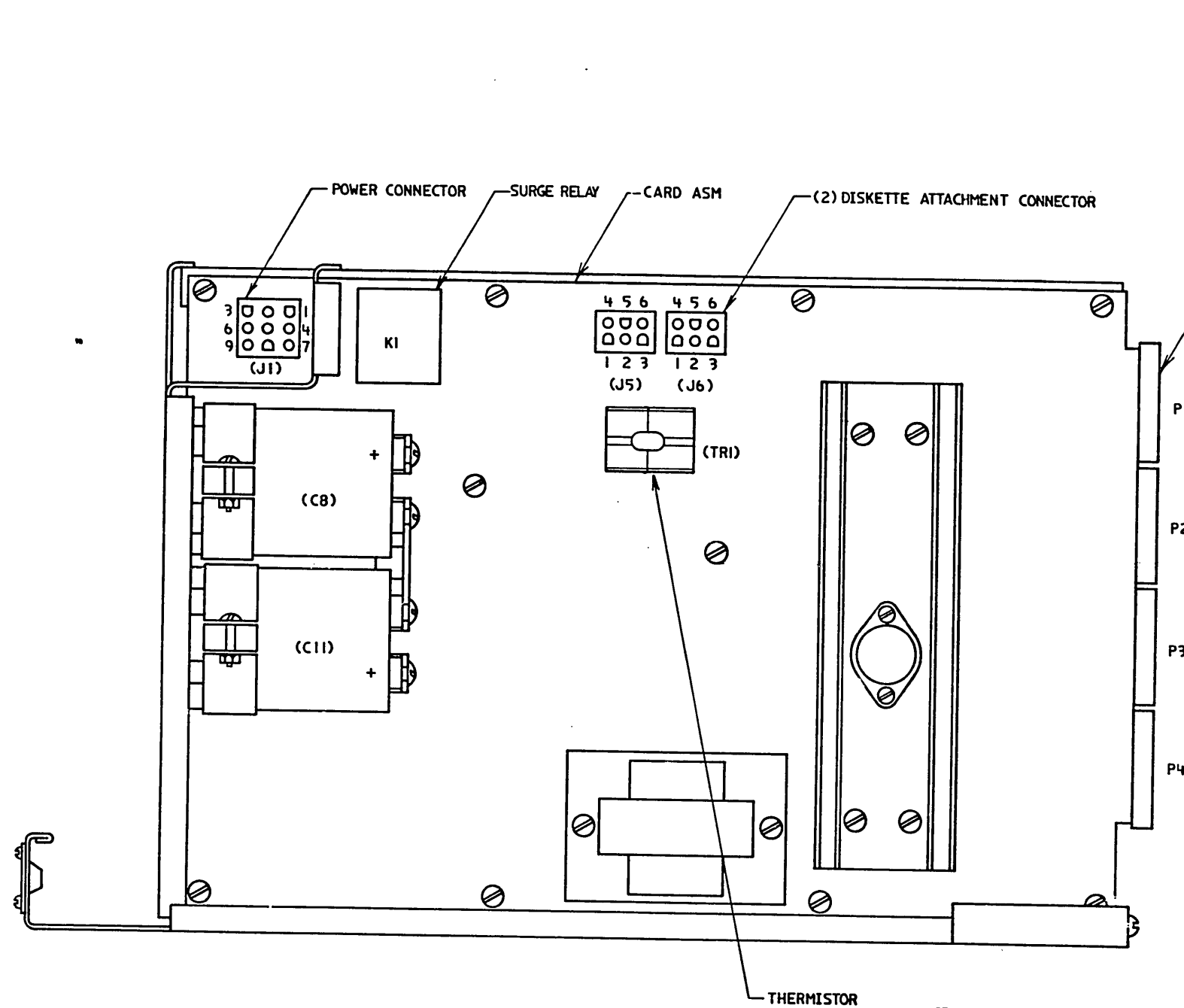
- [1] LINE CORD GREEN/YELLOW LEAD MUST BE TERMINATED UNDER SCREW MARKED
- [2] - - - - - INDICATES DC DISTRIBUTION OF +24V, +5V & -5V; J5, J6, J7 & J8 ARE 6 POSITION CONNECTORS
- [3] JUMPERS ARE PART OF CONNECTOR P1 ON CABLE ASM. SEE CHART A 110V & 220V JUMPERING
- [4] ——— INDICATES 110V AC DISTRIBUTION TO DISKETTE UNITS  
 - - - - - INDICATES 220V AC DISTRIBUTION TO DISKETTE UNITS
- 5 THIS IS A WIRING DIAGRAM ONLY. SEE MM FOR PHYSICAL LOCATION OF COMPONENTS

EC HISTORY		DRAWING TITLE	
15 JAN 81		AC & DC POWER DISTR FOR	
11 MAR 81	987996	230 W PWR SUPPLY	
11 MAY 81	994241	PART NO 6844504	
11 NOV 81	466946	CLASSIFICATION	

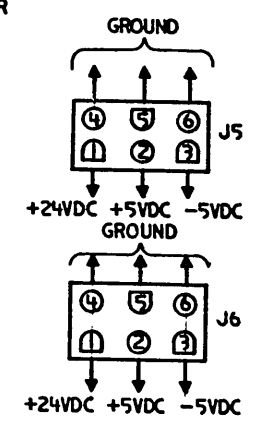
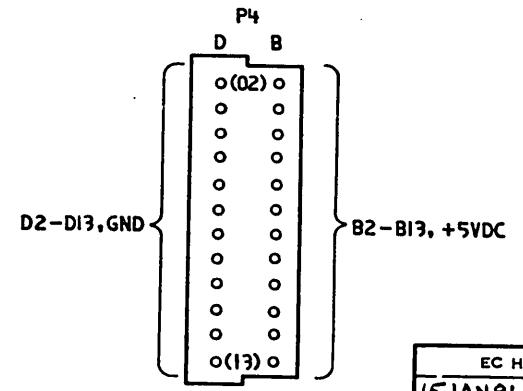
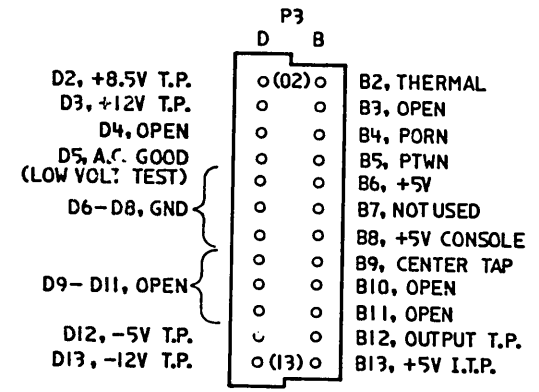
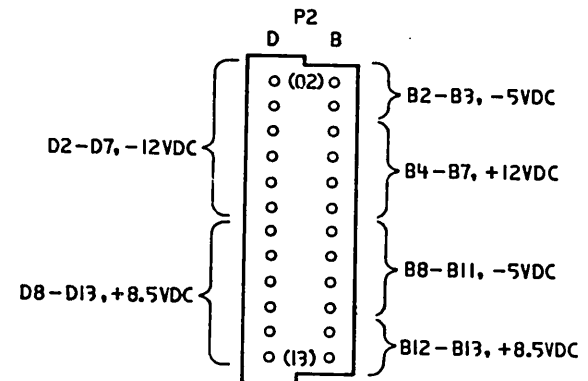
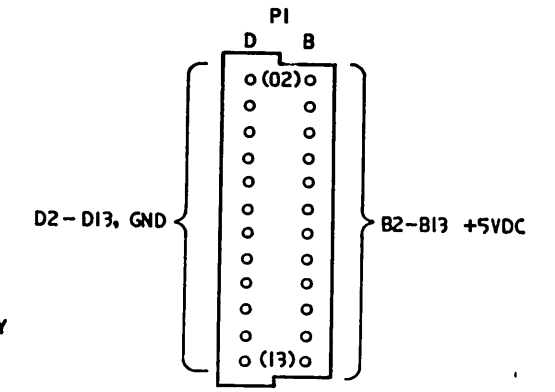
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IBM CORP

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CARD ASSEMBLY PLUGS INTO COLUMN H OF BACK BOARD

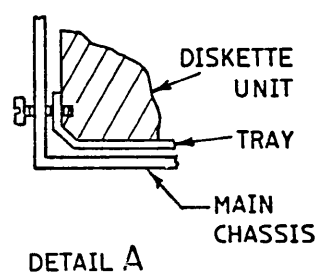
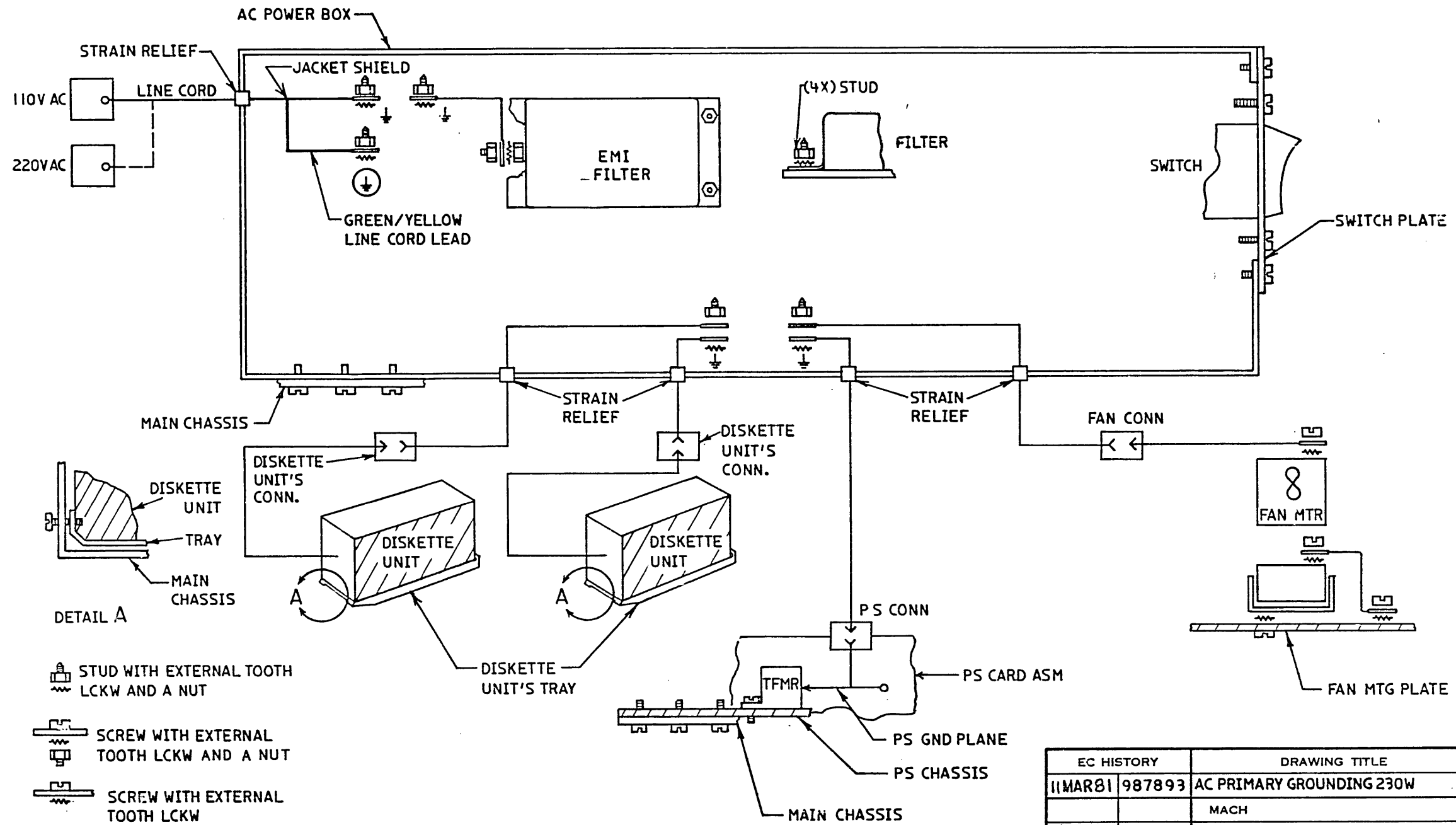


COMPONENTS	
SYM	DESCRIPTION
C8, C11	CAPACITORS, 1100μF, 200VDC

EC HISTORY		DRAWING TITLE	
15JAN81	487627	POWER SUPPLY ASM, 230W	
26AUG81	466762	MACH	
		PART NO 6844507	
		CLASSIFICATION	
		IBM CORP	

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Y B 2 6 0



- STUD WITH EXTERNAL TOOTH LCKW AND A NUT
- SCREW WITH EXTERNAL TOOTH LCKW AND A NUT
- SCREW WITH EXTERNAL TOOTH LCKW
- METAL TO METAL CONTACT

AC GROUND SYMBOLS

EC HISTORY		DRAWING TITLE	
11MAR81	987893	AC PRIMARY GROUNDING 230W	PS
		MACH	
		PART NO 6030961	
<b>C</b>		CLASSIFICATION	<b>IBM</b> CORP

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