IBM

Field Engineering

Theory-Maintenance

SUPPLEMENTED BY SN 34-0059

System/3
5444 Disk Storage Drive Attachment

SY34-0021-1

IBM Field Engineering
Theory-Maintenance

System/3
5444 Disk Storage Drive Attachment

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Second Edition (November 1970)

This is a major revision of, and obsoletes, SY34-0021-0. This edition incorporates use of the disk attachment in the IBM 5406 in addition to its previous use in the IBM 5410. Chapter 2 is completely new and now contains second-level diagrams of each card in the disk attachment. Chapter 3 has been extensively revised by adding more detailed information on disk attachment operations.

Changes are periodically made to the information herein; any such changes will be reported in subsequent revisions or Technical Newsletters.

Some illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

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Preface

This is a combined theory-diagram manual on the disk attachment for the IBM System/3 Model 10 and System/3 Model 6. There are no other manuals for the disk attachment.

This manual is organized into three chapters: introduction, functional units, and operations. Information on how to use each chapter is found on the first page of the chapter.

The page numbering system of this manual is as follows:

8 XXX

1
2
3

1 Section number: applies to the Model 6 FETM. This manual is Section 8.

2 Chapter number: a "1" means chapter 1, a "2" means chapter 2, a "3" means chapter 3.

3 Page number of chapter: numbered 01 through 99.

The diagrams and flowcharts in this manual are at engineering level 571538. Other manuals needed to understand and service the file attachment are:

- Field Engineering Theory of Operations Manual, *IBM 5410 Central Processing Unit*, Order No. SY31-0207
- Field Engineering Maintenance Diagrams Manual, *IBM 5410 Central Processing Unit*, Order SY31-0202
- Field Engineering Maintenance Manual, *IBM 5410 Central Processing Unit*, Order No. SY31-0244
- Field Engineering Theory-Maintenance Manual, *System/3 Model 6 5406 Processing Unit and Attachments*, Order No. SY34-0022
- Field Engineering Theory of Operations Manual, *IBM 5406 Central Processing Unit*, Order No. SY34-0023
- Field Engineering Theory-Maintenance Manual, *IBM 5444 Disk Storage Unit*, Order No. SY33-0026
- Field Engineering Theory-Maintenance Manual, *IBM 5444 Disk Storage Drive (Machines with serial numbers up to 30100)*, Order No. SY33-0026
- IBM Maintenance Library, *5444 Disk Storage Drive, Theory-Maintenance (Machines with serial numbers above 30100)*, Order No. SY33-0029

Abbreviations

ACK	Acknowledged
ALD	Automated Logic Diagram
ALU	Arithmetic and Logic Unit
AM	Address Mark
BCA	Bit Count Appendage
C	Byte containing the binary number that corresponds to the number of the track
CC	Cyclic Check
CCR	Cycle Control Ring
CPU	Central Processing Unit
CSR	Cycle Steal Request
DBI	Data Bus In
DBO	Data Bus Out
DCF	Disk Control Field
DFCR	Disk File Control Register
DFDR	Disk File Data Register
F	Flag Byte
FCU	File Control Unit
G	Gap
HSA	High Speed Access
ID	Identifier Area
I/O	Input/Output
IPL	Initial Program Load
LIO	Load I/O Instruction
LSR	Local Storage Register
N	Byte in the disk control field
0E	Sync Byte Character
PC	Parity Check
PG	Parity Generator
S	Sector Byte
SAR	Storage Address Register
SERDES	Serializer-Deserializer
SIO	Start I/O Instruction
SLD	Solid Logic Dense
SNS	Sense I/O Instruction
TIO	Test I/O Instruction

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This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

Title page, ii	8-227, 8-228
iii, iv	8-231, 8-232
8-101 through 8-104	8-237 through 8-242
8-107 through 8-112	8-249, 8-250
8-201 through 8-208	8-305, 8-306
8-211, 8-212	8-313, 8-314
8-213, 8-214	X-1, X-2
8-215, 8-216	

A change to the text or to an illustration is indicated by a vertical line to the left of the change.

Summary of Amendments

1. Incorporate information for high speed access
2. Technical corrections

Note. Please file this cover letter at the back of the manual to provide a record of changes.

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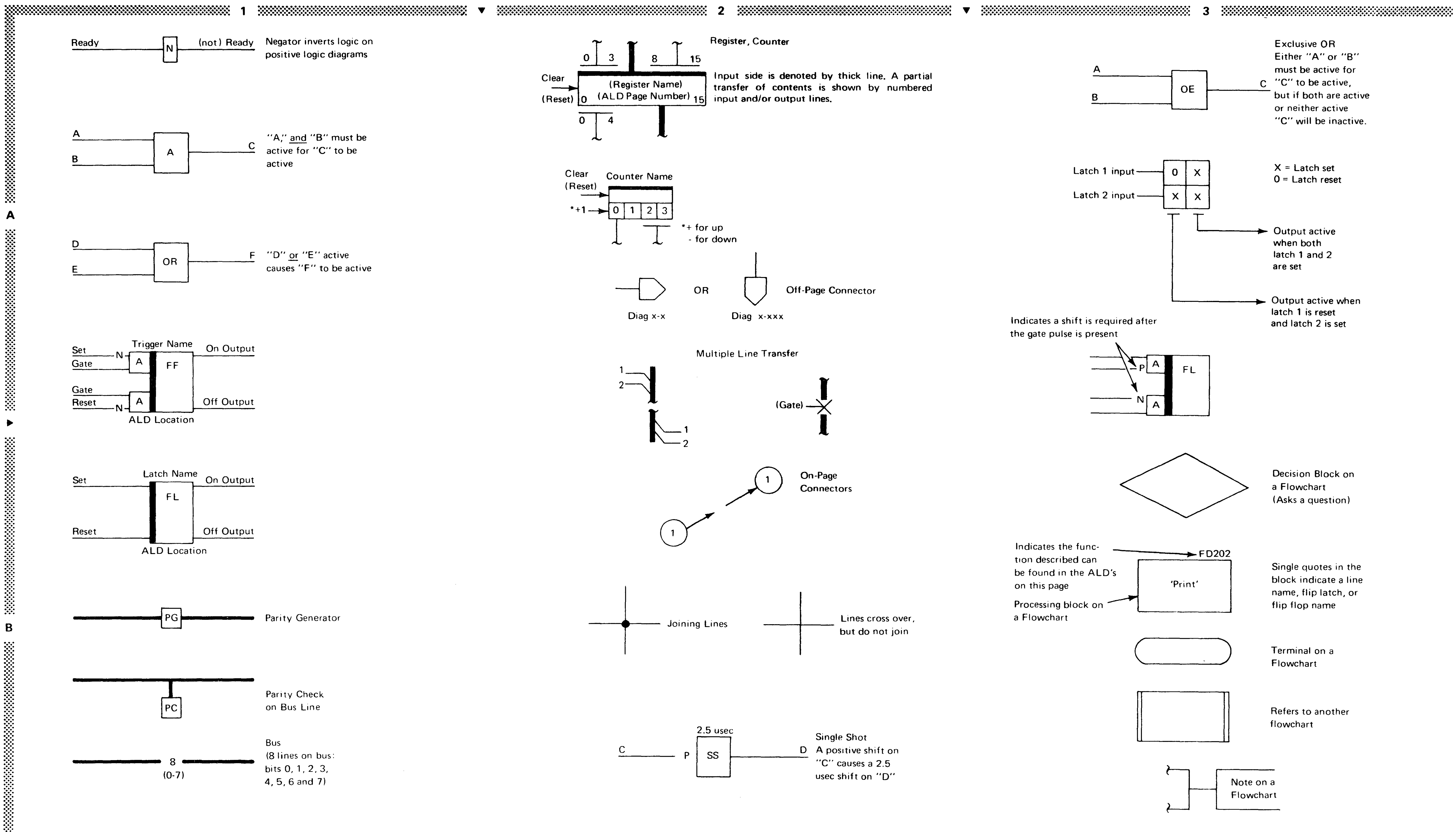
Chapter 1. Introduction

Chapter 2. Functional Units

Chapter 3. Operations


1
2
3
A
B
Ready
N
(not) Ready
Negator inverts logic on positive logic diagrams
A
B
A
C
"A," and "B" must be active for "C" to be active
D
E
OR
F
"D" or "E" active causes "F" to be active
Set
Gate
Gate
Reset
Trigger Name
FF
On Output
Off Output
ALD Location
Set
Reset
Latch Name
FL
On Output
Off Output
ALD Location
PG
Parity Generator
PC
Parity Check on Bus Line
8
(0-7)
Bus (8 lines on bus: bits 0, 1, 2, 3, 4, 5, 6 and 7)
Register, Counter
Clear
(Reset)
(Register Name)
(ALD Page Number)
0 3 8 15 0 4
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input and/or output lines.
Clear (Reset)
Counter Name
*+1
0 1 2 3
*+ for up
- for down
OR
Off-Page Connector
Diag x-x
Diag x-xxx
Multiple Line Transfer
(Gate)
On-Page Connectors
Joining Lines
Lines cross over, but do not join
2.5 usec
C
P
SS
D
Single Shot
A positive shift on "C" causes a 2.5 usec shift on "D"
Exclusive OR
Either "A" or "B" must be active for "C" to be active, but if both are active or neither active "C" will be inactive.
OE
Latch 1 input
Latch 2 input
X = Latch set
0 = Latch reset
Output active when both latch 1 and 2 are set
Output active when latch 1 is reset and latch 2 is set
Indicates a shift is required after the gate pulse is present
P
N
FL
Decision Block on a Flowchart (Asks a question)
Indicates the function described can be found in the ALD's on this page
FD202
'Print'
Processing block on a Flowchart
Single quotes in the block indicate a line name, flip latch, or flip flop name
Terminal on a Flowchart
Refers to another flowchart
Note on a Flowchart

A

IBM 5444 DISK STORAGE DRIVE ATTACHMENT

The IBM 5444 Disk Storage Drive Attachment, also called the disk attachment or file control unit (FCU), can attach either one or two 5444 Disk Storage Drives to the IBM System/3 Model 10 or the IBM System/3 Model 6.

The file control unit is the interface between the disk storage drive and the central processing unit (CPU). The file control unit (FCU) provides a way for the disk storage drive to use the facilities of the CPU to communicate with core storage. Communication between the CPU and file control unit (FCU) is via the data bus out (DBO) lines and data bus in (DBI) lines, with additional lines for control signal interchange.

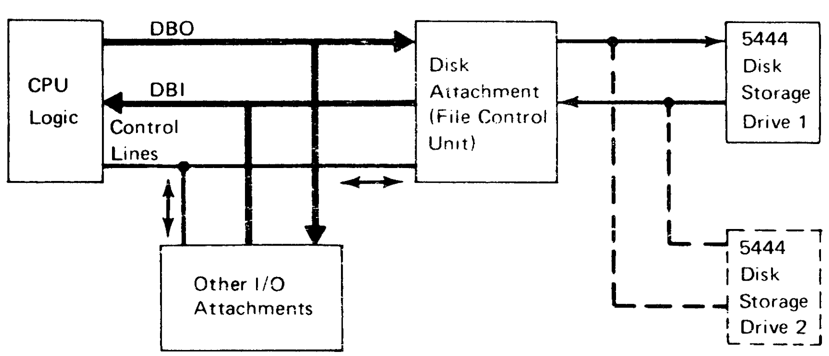
The disk attachment is located in the main gate of the CPU. In the Model 10 it is located in gate 01A-A2; in the Model 6 it is located in gate 01A-A1.

A disk attachment may be either *standard* or *high speed*, depending on the model of 5444 Disk Storage Drive attached to the CPU. The difference between a standard and high speed attachment is determined by the type of logic card plugged into positions G2 and F2 of the attachment board.

The standard disk attachment is used in either the Model 6 or Model 10 CPU to attach 5444 Disk Storage Drives with friction drive or stepper motor access mechanisms.

The high speed disk attachment is used only with the Model 10 CPU to attach 5444 Disk Storage Drives with the high-speed access feature installed.

B



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The file control unit contains logic circuits to:

1. Decode program instructions into signals to control a disk operation.
2. Generate timing signals for data transfer to and from the disk.
3. Address the local storage registers assigned to disk operation.
4. Detect error conditions.
5. Generate the cyclic code (CC) and bit count appendage (BCA) check characters.
6. Provide status information about the file control unit and drive(s).
7. Generate cycle steal requests.
8. Serialize data (change from parallel-by-byte to serial-by-bit) and deserialize data (change from serial-by-bit to parallel-by-byte).
9. Control the high-speed access interface line for drives that have the high-speed access feature installed. (Model 10 CPU only.)

Program Instructions

Four program instructions are used for disk operation:

1. Load I/O (LIO)
2. Test I/O (TIO) / Advance Program Level (APL)
3. Sense I/O (SNS)
4. Start I/O (SIO)

Load I/O (LIO)

Load I/O transfers two bytes of data from core storage into either of the local storage registers assigned to disk, disk file data register (DFDR) or disk file control register (DFCR). For diagnostic purposes, a CE load I/O (LIO) instruction transfers two bytes from core storage to the file control unit. This information controls logic lines in a manner that duplicates disk drive functions to facilitate diagnostic programs.

Test I/O (TIO)

Test I/O / Advance Program Level tests for operating conditions of the drive and attachment. This instruction is used to branch the program into subroutines depending on the results found in the test (condition met or not met). If the system has the dual program feature, the program may branch into another program depending on the conditions found in the test. Without the dual program feature, the program loops on the advance program level (APL) instruction until the condition specified in the test is no longer present.

Sense I/O (SNS)

Sense I/O transfers (1) the two bytes in either local storage register (LSR) or (2) two bytes of file control unit status information into core storage. The four status bytes indicate operating conditions about the file control unit and drive(s). Each bit within each byte carries a significance, providing up to 32 indications of the condition of the units.

Start I/O (SIO)

Start I/O selects the drive an operation is directed to, selects the disk (either fixed or removable), and specifies the command (operation) to be performed. These commands are:

Seek—positions the read heads in the 5444 to a desired location (cylinder) and selects a read head to be used in the next start I/O instruction operation (read, write, or scan). Head selection determines the upper or lower surface of the disk to be addressed.

Write—records data on the disk from the data field in core storage.

Read—reads data recorded on the disk and transfers the data to the data field in core storage.

Scan—compares data on disk with a data field in core storage. An equal, low or equal, or high or equal indication can be obtained.

Timing

File control unit circuits are controlled by timing (clock) signals. These signals are generated by (1) a crystal oscillator (write clock) or (2) signals produced from the clock signals when data is read from the disk (read clock). Clock signals drive other time-generating logic needed to control the transfer of data through the file control unit and to and from the disk.

Local Storage Register Addressing

The local storage registers disk file data register and disk file control register are addressed by the file control unit to:

1. Locate the data field in core storage.
2. Locate the disk control field in core storage.
3. Increment or decrement the address in a register.
4. Load the local storage register with an address.

Error Detection

Errors in the file control unit may be of two types:

1. Error in data (parity).
2. Failure of the file control unit to follow the functional objectives of a program instruction.

1

Parity Errors

The parity of the data is checked as it enters the file control unit. After the data byte is under control of the file control unit, the parity bit is separated from the data byte, but retained and transferred in step with the data through the file control unit. At each transfer point the parity is compared with the separated parity bit. As the data byte leaves the file control unit to be recorded on disk, the odd-even status of the data bits is checked against the separated parity bit to insure that the data was transferred out of the file control unit with the same parity as when it entered the file control unit.

In place of recording parity bits on the disk, the file control unit generates check characters (cyclic code and bit count appendage) from the serialized data bits and records the characters at the end of the identifier area (ID) and data fields on the disk. With a known input (the data byte parity), the parity of the check character can be predicted. The check character generated is therefore compared with the separated parity bit for error in generation.

When data is read from the disk, the check characters are regenerated and compared to the check characters recorded on disk to insure that the data was read correctly. Before the data byte is returned to the CPU, a parity bit generator reinserts the parity bit that was removed from it before the byte was serialized.

Functional Objective Errors

Functional objectives of each program instruction are checked and if the objectives are not met, an error is indicated by setting an error latch. If an error is indicated, the operation in progress is ended, and a status (error) latch is set to indicate the type of error.

Cycle Steal Requests (CSR)

A cycle steal request operation permits the file control unit to share processing time with the CPU and other I/O devices. Cycle steal requests for disk data transfer are highest in priority of the cycle steal devices.

The file control unit requests a cycle steal when there is data or control information to transfer to or from the file control unit or when the address of a LSR is to be modified. A LSR is usually addressed during a cycle steal to locate the data field or the disk control field in core storage.

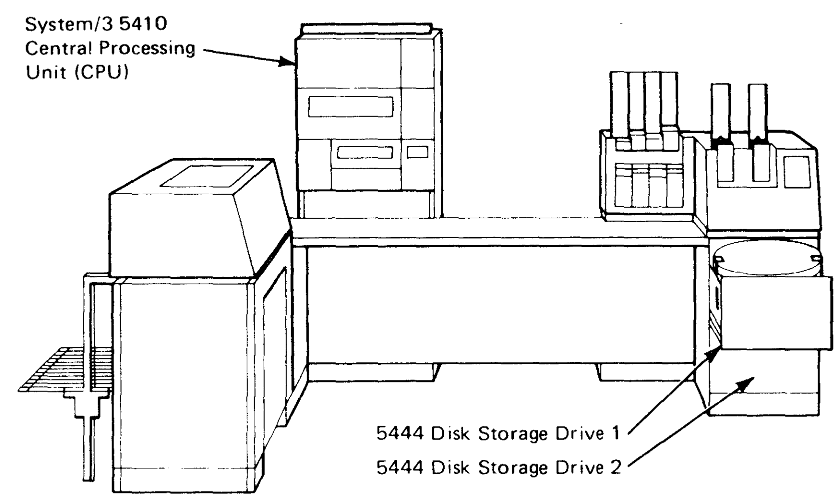
One data byte is buffered (stored) in the file control unit. As a result the file control unit requests a cycle steal one cycle before the data is needed at the file control unit, or one cycle after the data byte is ready to send to the CPU.

Serializer-Deserializer (Serdes)

Data is transferred to the file control unit parallel-by-byte but is recorded on the disk serial-by-bit. Data is read from the disk serial-by-bit and transferred to the CPU parallel-by-byte.

Two registers in the file control unit operate in a multifunction manner to change the byte into bits or the bits back into a byte. One register acts as a buffer while the other shifts or vice-versa. These registers are called a serdes (serializer-deserializer).

2



Note: Drive 1 and drive 2 are also called spindle 0 and spindle 1, respectively.
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High-Speed Access Control

During seek operations on disk drives with the high-speed access feature installed, the disk attachment must monitor the carriage position relative to the desired track. Depending on the length of the seek, the disk attachment deactivates the high-speed access interface line at various numbers of tracks before the end of the seek. This is to allow the carriage to slow to normal speed and stop at the desired track without overtravel.

IBM 5444 DISK STORAGE DRIVE

The IBM 5444 Disk Storage Drive is a direct access storage device for the IBM System/3 Model 10 or System/3 Model 6.

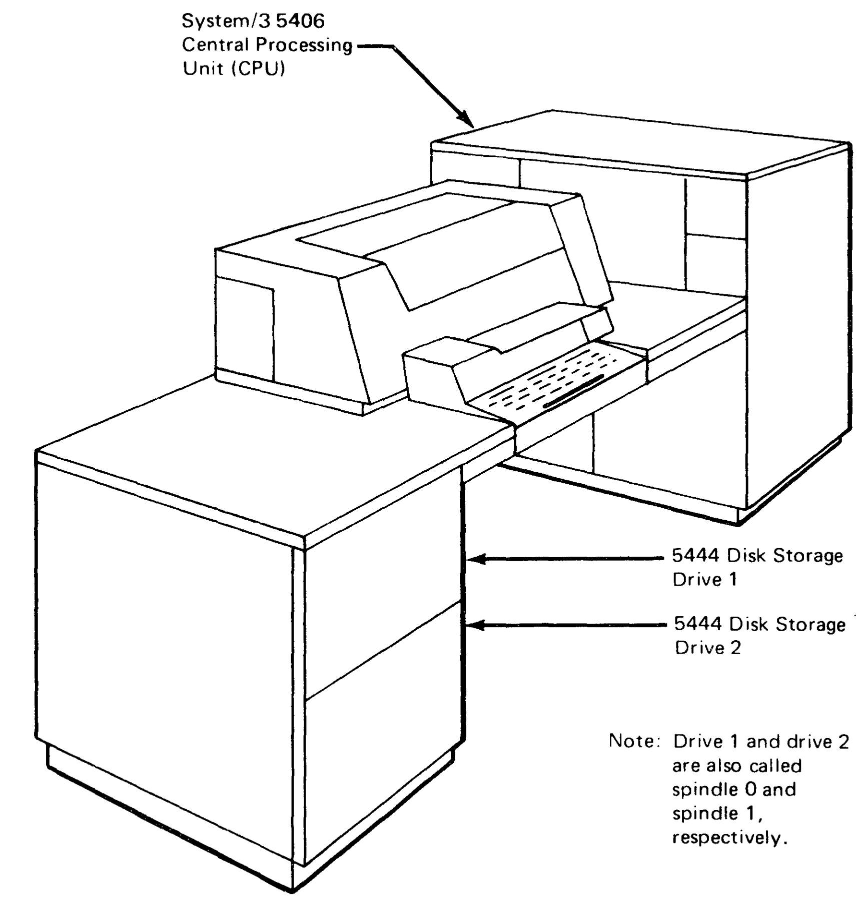
A 5444 drive contains two disks mounted on a common spindle. One disk is permanently mounted in an enclosure at the base of the drive spindle. The other disk, which is removable, is housed in a cartridge at the top of the spindle above the fixed disk. When removed from the drive, the cartridge is placed into a base to form a fully sealed enclosure for protected, off-line storage.

5444 Disk Storage Drives use either of two types of access drive mechanism, friction drive or stepper motor. Early drives below serial number 30100 use friction drive, later drives above serial number 30100 use the stepper motor.

A high speed access feature is available for drives above serial number 30100 and is available for use on the Model 10 only. High speed access and normal speed drives can not be installed (mixed) on the same system.

A system can contain one or two drives. The drives are mounted within the system on sliding drawers.

3



Note: Drive 1 and drive 2 are also called spindle 0 and spindle 1, respectively.

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Six models of the 5444 can be used to obtain four different drive configurations as shown in the following tables. The first table lists and describes the available models. The second table shows the drive configurations.

Available Models

Model	Description
1	Single drive. Accesses 104 cylinders on removable cartridge and 104 cylinders on fixed nonremovable disk.
2	Single drive. Accesses 204 cylinders on removable cartridge and 204 cylinders on fixed nonremovable disk.
3	Single drive. Accesses 204 cylinders on removable cartridge only.
A1, A2, A3	Model A1, A2, and A3, are equivalent to models 1, 2, and 3 except that high speed access is installed. These models are available on the Model 10 only.

Drive Configurations

No. of Drives	Normal Speed Model(s)	High Speed Model(s)	Storage Capacity (million bytes)	*Cylinders Accessed* Removable Cartridge	Fixed Disk
1	1	A1	2.46	104	104
1	2	A2	4.92	204	204
2	2&3	A2&A3	7.37	204	204
2	2	A2	9.83	204	204

Model 1 is located in the upper drawer; model 3 or a second model 2 is located in a lower drawer.

The disk drive uses solid logic dense (SLD)-100 circuits and SLD-100 line levels between the drive and disk attachment.

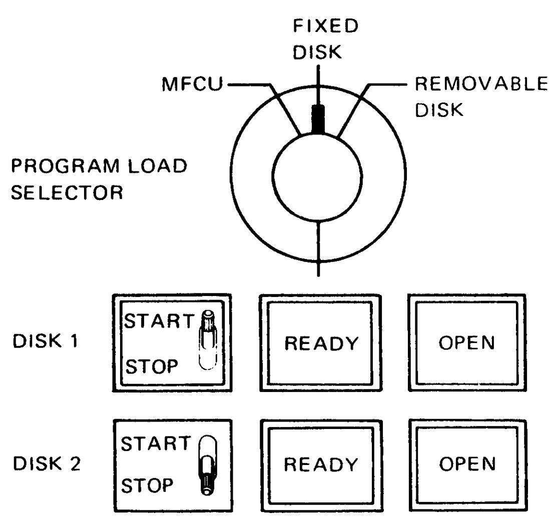
For further information about the 5444 disk storage drives, refer to:

FE Theory-Maintenance Manual, *IBM 5444 Disk Storage Drive, (Machines with serial numbers up to 30100)*, Order No. SY33-0026

IBM Maintenance Library, *5444 Disk Storage Drive, Theory-Maintenance, (Machines with serial numbers above 30100)*, Order No. SY33-0029

Operator Console (Model 10)

Operator controls for the disk drives are located on the system console.



Program Load Selector

This three-position switch determines what I/O device will be selected for the program load operation:

MFCU position selects the multi-function card unit.

Fixed Disk and Removable Disk select disk drive one and either the fixed (lower) or removable (upper) disk, depending on the switch position.

The START-STOP switch and indicators READY and OPEN provide individual control and status for the drives:

Start-Stop switches apply AC power to the respective drive.

Ready indicator on means that the respective drive is ready for operation.

Open indicator on means that the drive drawer may be opened to attend to the drive or to change the removable disk.

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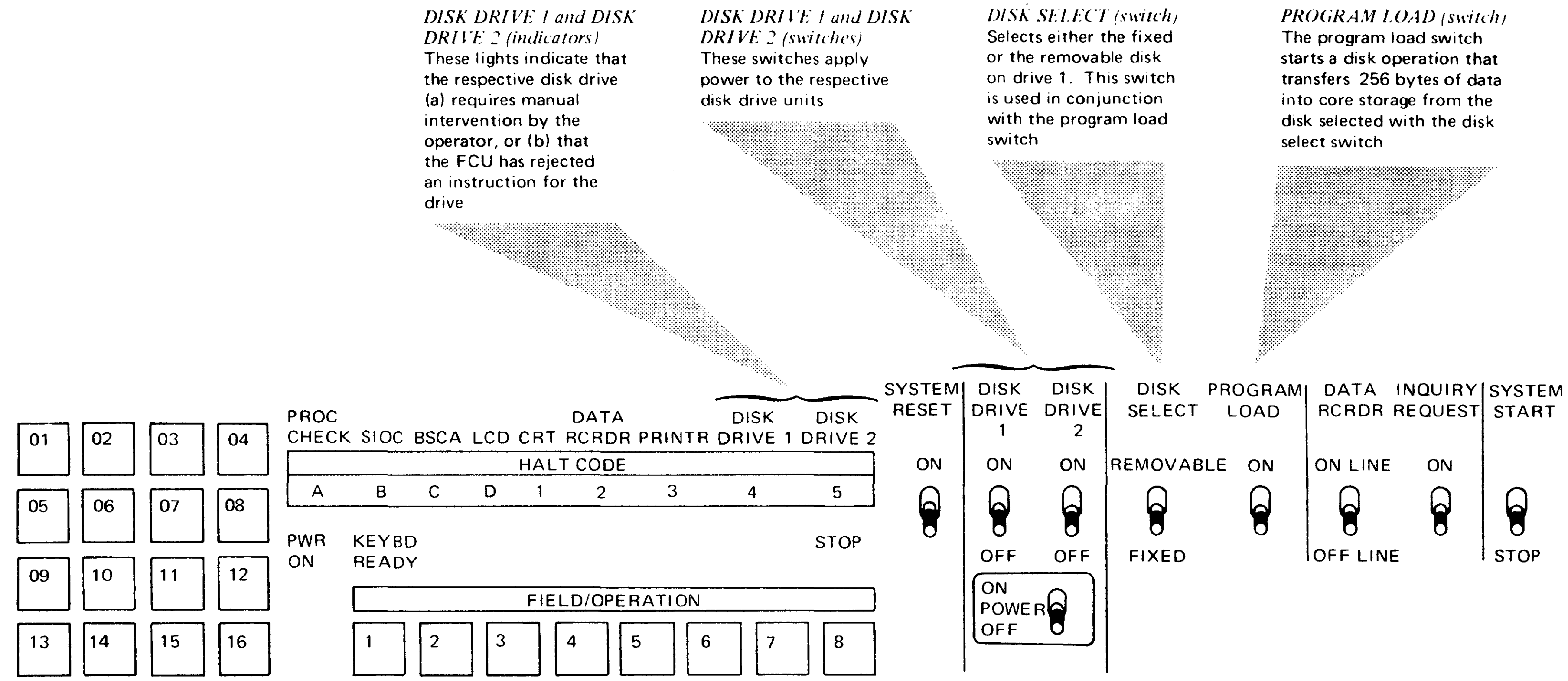
Operator Console (Model 6)

Operator controls for the disk drives are located on the system console.



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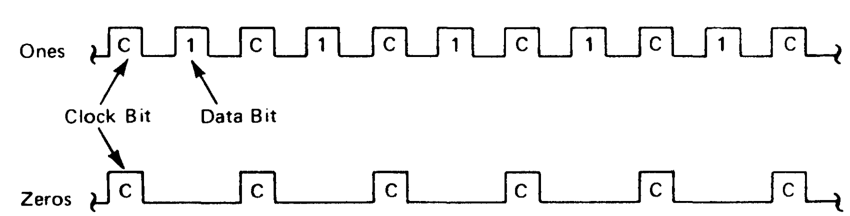
Data Storage

Data is recorded (written) on the disk serially by byte and serially by bit. In addition to data, clock bits are recorded on the disk. Data bits are recorded between the clock bits in a continuous pattern without separation or extra bits as markers. The clock bits provide timing signals when the data is recovered (read) from the disk. This method of recording data is referred to as double-frequency recording. A data byte of hexadecimal FF, for example, is written as all ones—twice the frequency of zeros that are recorded as clock bits only.



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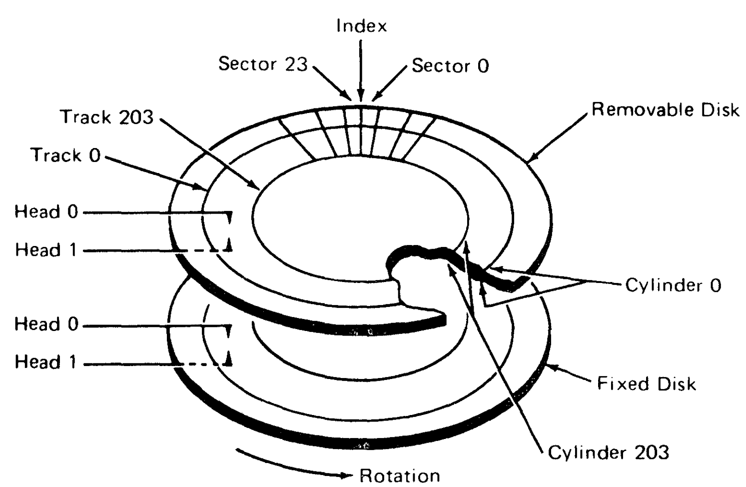
Data recorded on the disk does not contain a parity bit; it is removed from the data byte before it is recorded on the disk. Instead of a parity bit, check characters are generated from the data bits and recorded at the end of the data field. When data is recovered (read) from the disk, the check characters are regenerated and compared with the check characters recorded on the disk to verify the data.

Data is recovered serially by bit and reassembled into an 8-bit byte. A parity-bit generator reinserts the parity bit removed in the recording process, before the data byte is returned to the system for processing.

Track Format

The track is the smallest addressable unit to which the drive access mechanism can position its heads. Each track is divided into 24 sectors, each with its own address. A sector may be read or written selectively through programming. A fixed point on the disk, index, is the starting point for all tracks. Each disk surface contains either 104 or 204 tracks. The tracks that are related to each other in the vertical plane on a single disk form a cylinder. On drives with two disks, the corresponding cylinders on both disks have the same cylinder numbers. Depending on the disk drive model, 100 or 200 cylinders are used for data storage. Cylinders 001, 002, and 003 are for alternate tracks and cylinder 103 or 203 is for customer engineer use.



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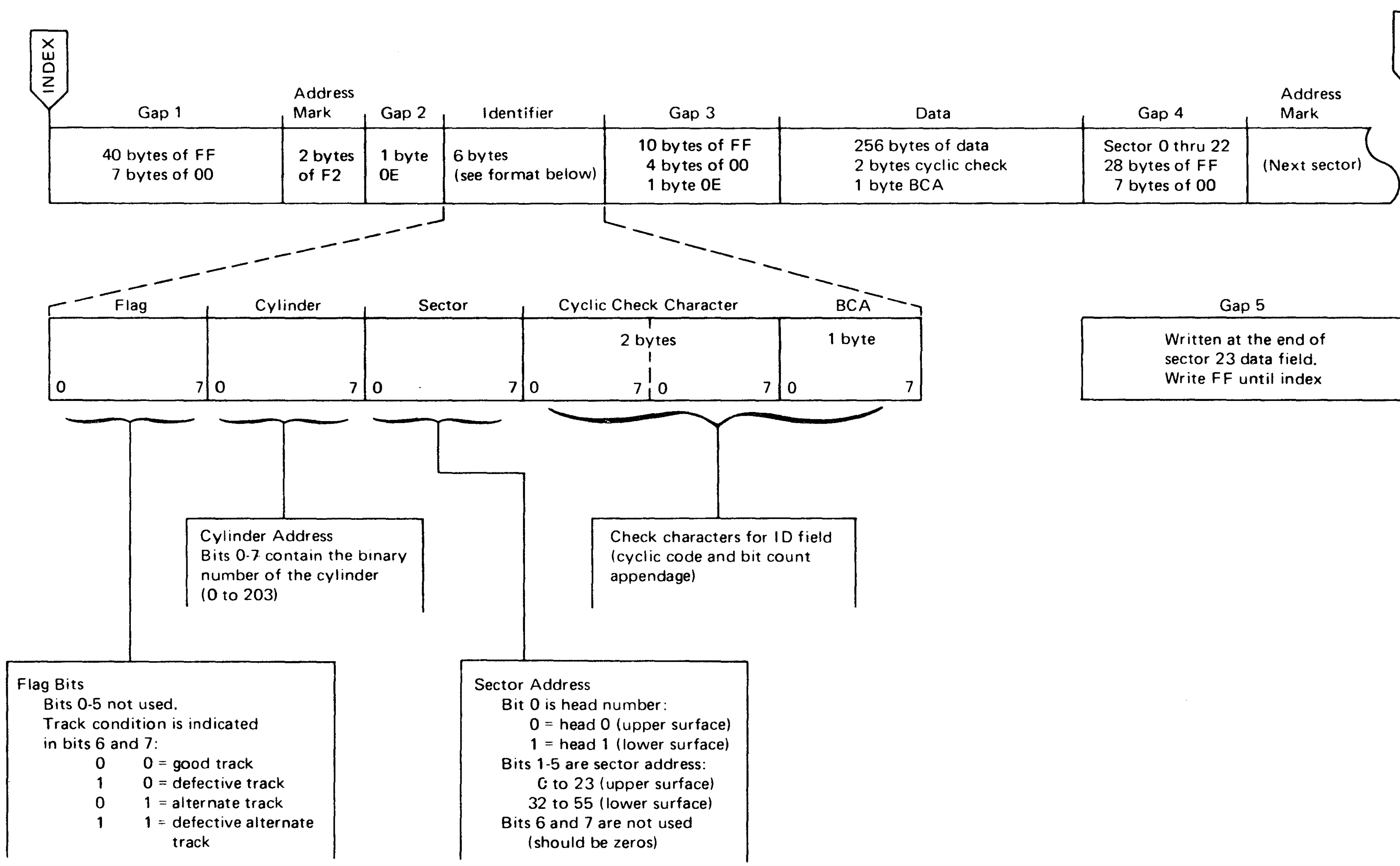
Index — A mark which is fixed for each disk and provides orientation information to the disk attachment. It is the starting point for every track.

G1 — A gap area between index and the first address mark. G1 contains 40 bytes of FF followed by seven bytes of zeros.

AM — Address mark (AM) is a specially written group of bits that indicate the start of a new sector. AM contains two bytes. (See "Data Separator" for additional information on address marks.)

G2 — A gap area between an address mark and the identifier of a sector. G2 contains a one-byte sync character (hexadecimal 0E).

ID — The identifier area (ID) of a sector contains six bytes, one flag byte, two address bytes, and three bytes of check characters.



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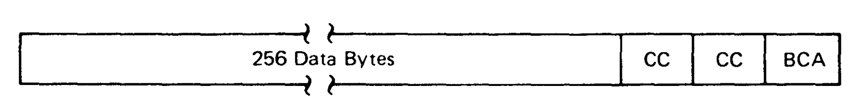
G3 — A gap area between the identifier and the data area of a sector. G3 contains 15 bytes: ten bytes of FF, followed by four bytes of zeros, followed by one sync character (hexadecimal 0E).

Data — The data area contains 256 bytes of data and three bytes of check characters.



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G4 — A gap area between the data field and the address mark of the next sector. G4 contains 28 bytes of FF and seven bytes of zeros.

G5 — A gap area between the end of the last sector and index. G5 is filled with FF (number of ones varies with disk rotational speed).

The track format for address marks, gaps, identifier fields, and data field is established by the disk attachment while executing a write identifier command. (This command is principally used to prepare a new disk for operation.) Data recorded on the disk during subsequent write data operations is written between gaps three and four. These gaps may vary slightly in length due to disk rotational speed.

Local Storage Registers (LSR)

Two local storage registers, located in the CPU, are assigned to disk operation. They are the disk file data register and disk file control register.

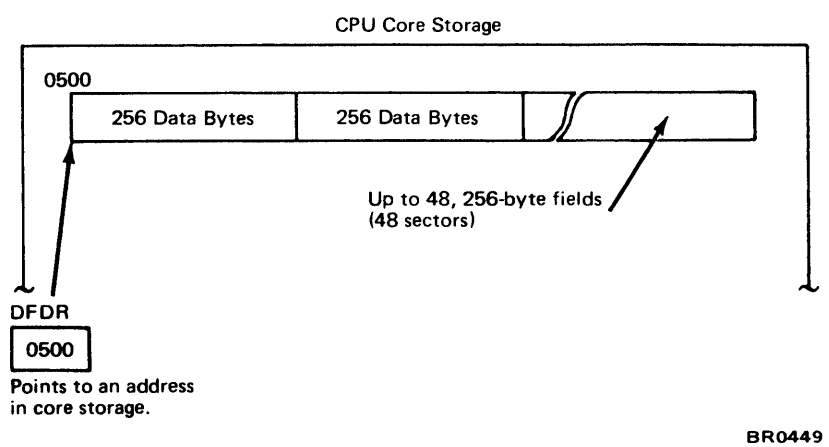
Disk File Data Register (DFDR)

This register addresses the disk data field in core storage. The data field contains data to be written on the disk or data received from the disk.

At the start of an operation, the disk file data register contains the two-byte address of the first byte in the data field. The disk file data register is updated by one as each byte is read from or written on the disk. At the end of an operation, the address in the disk file data register is one greater than the last address used during the operation. (For read data diagnostic, scan, and write identifier commands, the disk file control register address is equal to the original address.) If there is no data transferred, the contents of the disk file data register remain unchanged.

Note: In any of the described operations, the contents of the disk file data register are not predictable if an equipment check occurs.

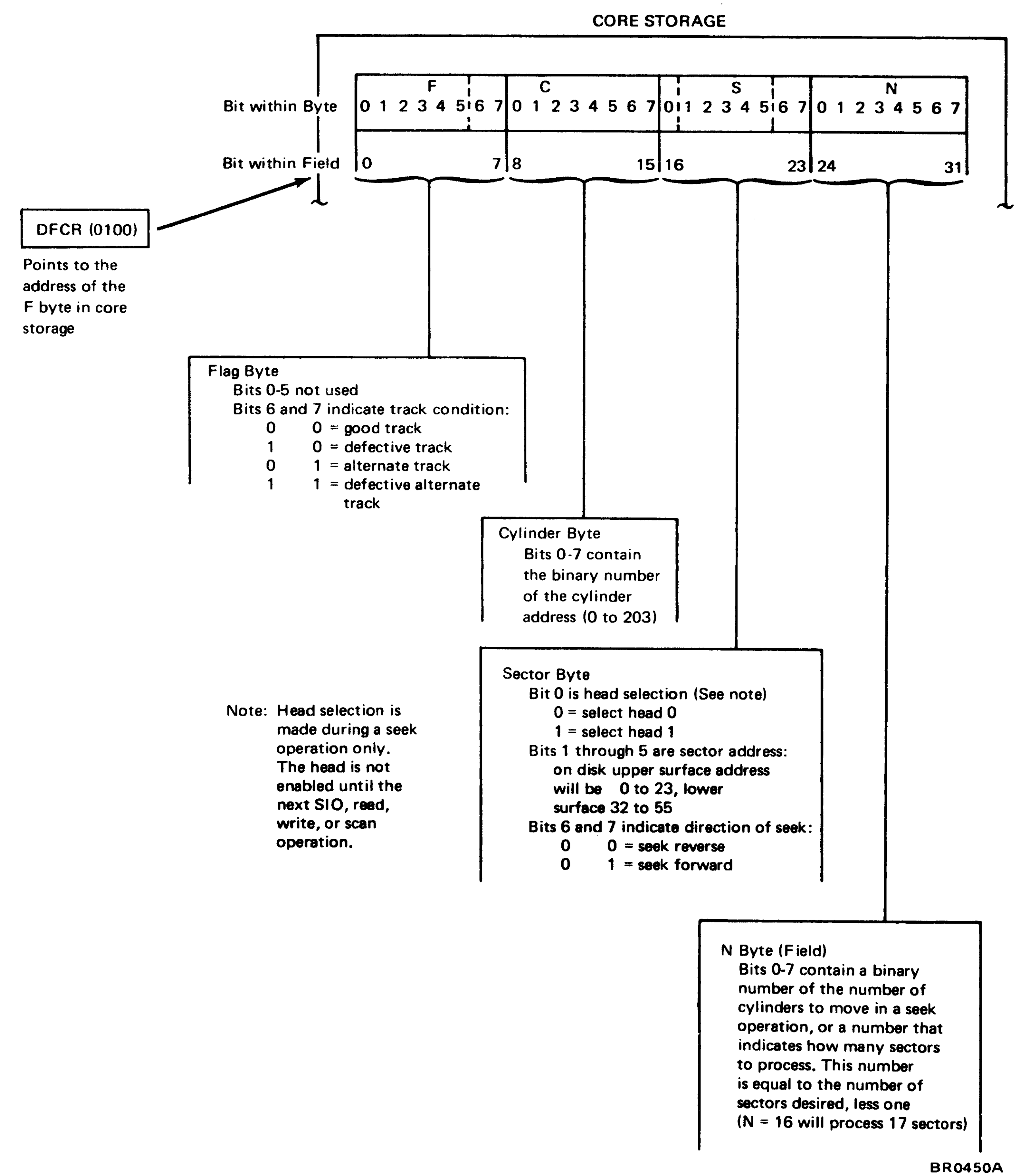
The data field format is:



Disk File Control Register (DFCR)

The disk file control register contains the address of a four-byte disk control field (DCF) in core storage. The disk control field contains information regarding (1) track condition, (2) cylinder address, (3) sector address, (4) head selection, (5) number of sectors to process during an operation, (6) number of cylinders to move the access mechanism during a seek instruction, and (7) the direction in which the access mechanism should move for the seek operation.

The disk control field format is:



1 2 3

A

B

File Instructions

Before a disk operation begins, a load I/O instruction is issued to load the local storage registers, disk file data register and disk file control register, with the address in core storage of the data field and disk control field, respectively.

Next, the availability and operating status of the device should be checked with the test I/O and sense I/O instructions. If the results of the test I/O and sense I/O indicate that the device is ready to accept an instruction, a start I/O instruction is issued.

All devices on the data bus out receive the start I/O instruction; however, only the device that decodes its address from the device address in the Q-byte may accept the instruction. The device that decodes its address must return a signal to the CPU (I/O condition A–I/O condition B) to indicate if the device accepts or rejects the instruction.

After the start I/O instruction cycles (I-op, I-Q, I-R) are complete, the instruction is set up in the disk attachment. The disk attachment will complete the specific operation with only cycle steal requests from the CPU.

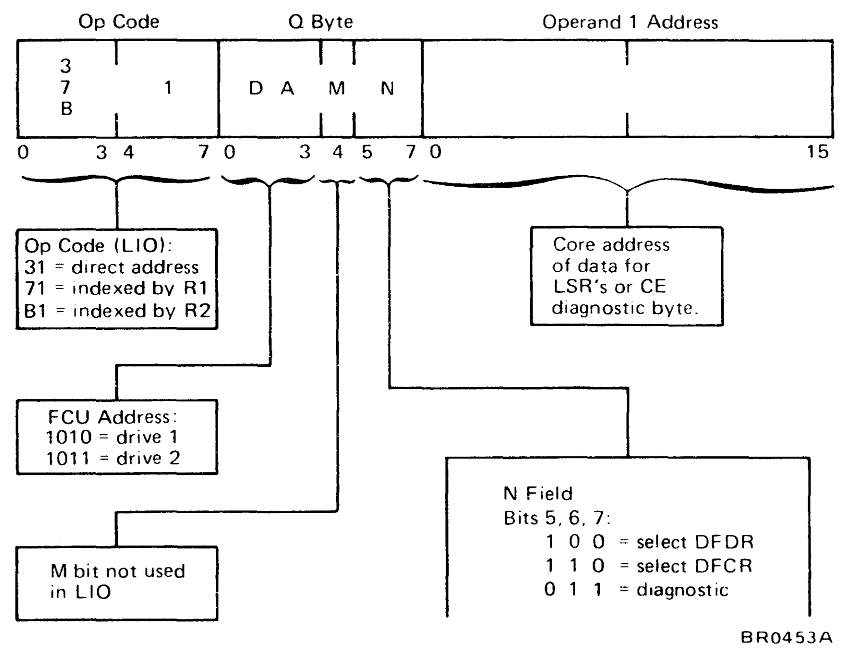
If a start I/O instruction read, write, or scan instruction is issued to a drive that is currently in a seek operation, the instruction will be provisionally accepted (held) by the disk attachment for execution at the end of the seek. If a seek check (error) occurred during the seek operation, the provisionally held start I/O instruction will be reset and a status bit set to indicate the result.

The disk instructions and the functional objectives of each are given in the following headings: Load I/O, Test I/O, Sense I/O, and Start I/O.

Load I/O (LIO)

- This instruction loads the local storage registers (disk file data register or disk file control register) with an address used by the file control unit during start I/O instructions.
- Load I/O can be used to set diagnostic CE mode, allowing CE control of a disk operation.

The format of the Load I/O instruction is:



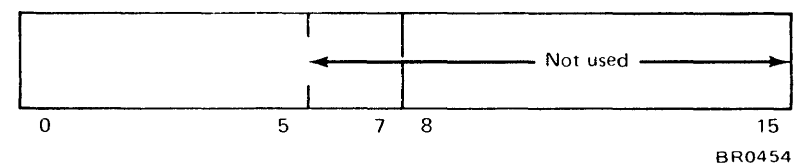
DFDR and DFCR (N Field = 100 or 110)

Two bytes located in storage at the address specified by the operand address are loaded into the register designated by the N bits as shown. If any combination of N bits other than shown is used, a processor check stop will occur.

Diagnostic (N Field = 011)

This combination of N bits is for diagnostic use. The file control unit logic is operated at a reduced rate of speed with no data transfer to and from the disk. The rate of speed is controlled by the diagnostic program. One clock pulse is issued with each diagnostic load I/O instruction. By stopping the CPU after a diagnostic load I/O instruction, the disk operation can be stopped to probe signal levels with a light indicator or a sense I/O instruction command may be issued to sense the status of attachment conditions.

In diagnostic mode, two bytes, located at the operand 1 address, control the disk operation. The format and description of these two bytes follow.



Bit 0–Index. Presence of this bit generates an index pulse in the file control unit. Index stays on until the next load I/O instruction is issued without bit 0 on, or until a CPU system reset occurs.

Bit 1–Write Oscillator. A write oscillator pulse is generated each time a load I/O instruction is issued with bit 1 on.

Bit 2–Separated Clock. A separated clock pulse is generated each time a load I/O instruction is issued with bit 2 on.

Bit 3–AM Indicate. An address mark indicate pulse is generated each time a load I/O instruction is issued with bit 3 on. (This pulse normally is produced when the data separator reads an address mark.)

Bit 4–Separated Data. One separated data pulse is generated when bit 4 is on. When a data bit is desired, it should be used after a separated clock bit is issued. Bits 1-4 operate file control unit lines of the same name and allow program control of these lines.

Bit 5–Inhibit CPU Request. This bit will cause CPU requests made by the attachment, to be inhibited until the next LIO instruction without this bit on or there is a system reset.

If a high speed FCU is installed, this bit also simulates a track crossing pulse from both drives. The track crossing pulse will stay on until the next LIO instruction without this bit or a system reset.

Bits 6-15. These bits are not used.

A diagnostic load I/O instruction sets the file control unit into a diagnostic mode. In diagnostic mode, the file control unit is not busy to another load I/O instruction or start I/O instruction. Load I/O instructions can be issued during a sense I/O instruction when they would normally not be accepted.

Programming Note: An example of proper instruction sequence after the disk file control register and disk file data register are loaded is:

LIO	(Diagnostic; to set the file control unit into diagnostic mode)	
SIO	(Write ID)	
LIO	(Diagnostic)	Operate file control unit interface lines by the appropriate bit or bits present in the diagnostic control byte.
LIO	(Diagnostic)	
LIO	(Diagnostic)	
LIO	(Diagnostic)	

Diagnostic mode is reset at the end of the start I/O instruction or by a system reset.

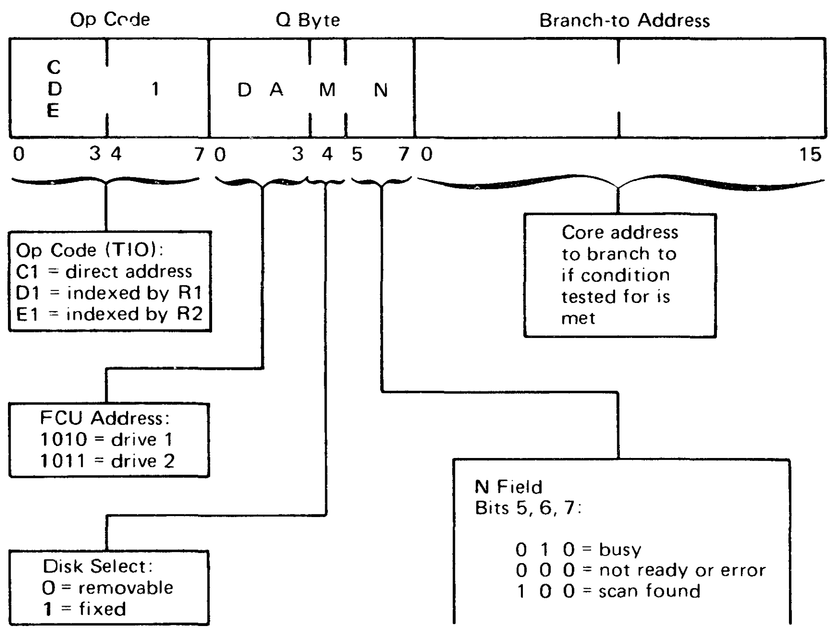
Load I/O General Notes

1. If the file control unit is busy, the load I/O instruction becomes equivalent to an advance-program-level-on-busy operation.
2. Load I/O does not set any disk status conditions. The M-bit is not used by the file control unit.
3. Load I/O is executed if the drive is executing a seek or recalibrate instruction, and a read, write, or scan has not been provisionally accepted.
4. If the drive is not ready, a load I/O instruction is executed.

Test I/O / Advance Program Level (TIO/APL)

- This instruction is used to test for scan-found, error, drive-not-ready, and file control unit busy.

The format of the test I/O instruction is:



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Busy (N Field = 010)

A control-unit-busy condition may be indicated by a test I/O and branch/advance program level instruction or by the rejection of a load I/O or start I/O. The busy condition is indicated to all file I/O instructions except sense I/O while:

1. The file is executing any read, write, or scan on any drive.
2. The file has provisionally accepted any operation for automatic execution at the conclusion of a seek currently in progress.

Not Ready or Error (N Field = 000)

The ready state of the disk drive is indicated to the file control unit by the conditioning of the file ready line. Failures that result in a not-ready state of the disk drive include:

- Failures of drive interlock switches
- Failure of the disk to maintain the rotational speed
- Failures that interrupt the normal head loading sequence or which cause the heads to unload
- A failure of ac power
- The occurrence of an unsafe condition

Unsafe conditions turn on latches located in the file circuitry.

1. Write unsafe latch
   a. Write selected and no write transitions detected.
   b. Write selected and multiple heads selected.
   c. Write not selected and write current source on.
2. Erase unsafe latch
   a. Write selected and erase current source not on.
   b. Write not selected and erase current source on.
3. Read/write selection unsafe latch
   a. Read selected and write selected.
   b. Read selected and erase selected.
   c. File accessing and write selected.
   d. File accessing and erase selected.

A test I/O instruction error is indicated when either drive is addressed if the following device status is present:

Data check
Track condition check
Missing address mark
End of cylinder
No record found
Equipment check (if not caused by unsafe)
No-op
Overrun

Note: See "Device Status" for description of the individual device status conditions. An error is indicated if there is a *seek check* or *unsafe* for the drive addressed. A seek check or unsafe condition for the unselected drive does not cause an error to be indicated. The drive to which the device status applies may be determined by the device status, status address (byte 1, bits 6-7).

Scan Found (N Field = 100)

The result of a start I/O scan instruction is determined by a test I/O scan found. The result is indicated if either drive 1 or drive 2 is addressed. The drive that the scan found condition occurred on is determined by a sense I/O instruction in status byte 1, bit 7.

Test I/O General Notes

1. If any N field other than the three previously shown (010,000, or 100) is used, the operation causes a processor-check stop. The test I/O instruction does not receive a busy indication if a seek is in progress on either or both drives 1 and 2 and no other operation has been provisionally accepted. If another operation (read, write, or scan) has been provisionally accepted or is in progress, busy is indicated when either drive is addressed.
2. File control unit busy rejects (equivalent to advance program level) a start I/O seek when the addressed drive is executing a previous seek instruction. This busy condition is not indicated by test I/O and branch/advance program level but may be checked by sense I/O. A busy condition occurs only when two consecutive seeks are issued to the same drive and the second seek is issued before the first is completed.
3. If a read, write, or scan is issued to a drive that is currently seeking, the new instruction is provisionally accepted for execution at the end of the seek. The provisionally accepted instruction causes a busy indication to a test I/O instruction. If there is a seek check at the end of the seek, the provisionally accepted read, write, or scan is not executed and no-op is set.
4. The scan-found indication is reset by the next start I/O.

Advance Program Level (APL)

An advance program level instruction tests for the same conditions as the test I/O instruction and uses the same N field codes. The OP code, however, is different (F1).

The format of the advance program level instruction is:

Op Code	Q Byte			
F1	DA	M	N	Not Used

BR0463

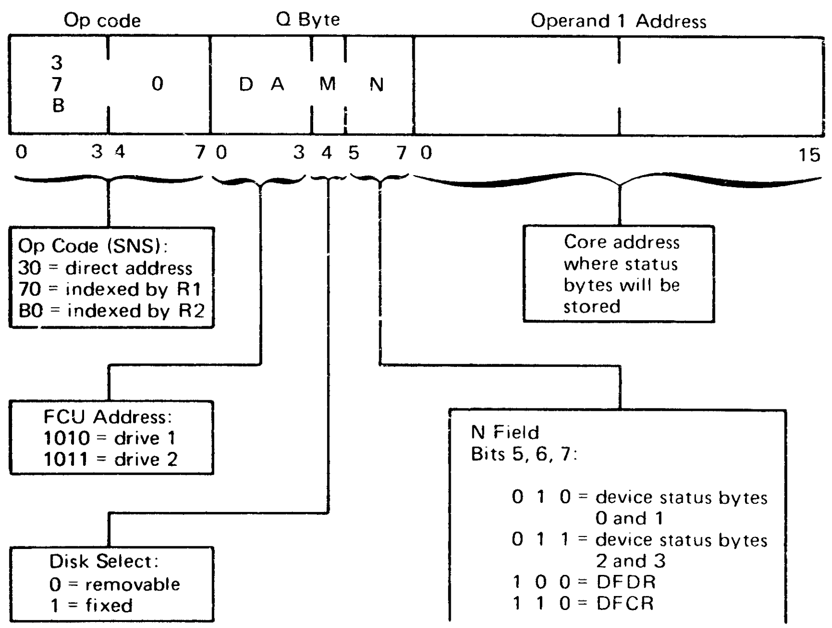
The manner in which the CPU executes the advance program level instruction depends on whether the advance program level feature is installed on the CPU.

Operation: This instruction tests for the conditions specified in the Q byte. If the condition tested for is present, a system with the dual programming feature installed activates the inactive program level; a system without the dual programming feature loops on the advance program level instruction until the condition no longer exists. If the condition is not present, systems with and without the dual programming feature take the next sequential instruction in the active program level.

Sense I/O (SNS)

- This instruction causes the contents (two bytes) of the specified local store register or device status to be stored into core storage at the address specified in the first operand address.

The format of the sense I/O instruction is:



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Device Status (N Field = 010 or 011)

- Device status is four bytes of information assembled by the control unit which provide information about the control unit and the file.
- Device status is made available by use of a sense I/O instruction.

The device status bits are:

	Byte 0	Byte 1	Byte 2	Byte 3
Bit 0	No-op	Scan Equal Hit	Unsafe	CE sense Bit
Bit 1	Intervention Required	Cylinder Zero	TAP Line A	CE sense Bit
Bit 2	Missing Address Marker	End of Cylinder	TAP Line B	CE sense Bit
Bit 3	Equipment Check	Seek Busy	TAP Line C	Not Bit Ring Inhibit
Bit 4	Data Check	100 Cylinder	Index	Standard Write Trigger
Bit 5	No Record Found	Overrun	Head Settling	Condition Priority Request
Bit 6	Track Condition Check	Status Address A	CE sense Bit	Bit Ring 0
Bit 7	Seek Check	Status Address B	Model 6	Not CC-Register Position 17

BR0457A

B

Byte 0, Bit 0—No Op. This bit indicates that the last issued command was not executed. It is caused by the selected file being unsafe or by a seek check occurring during a seek on the drive that read, write, or scan is provisionally accepted for. The no-op status bit is reset only by (1) a sense I/O command, (2) a CPU check reset, or (3) a general reset.

Byte 0, Bit 1—Intervention Required. This bit indicates that the addressed drive is not ready. The condition may be corrected by making the file ready. An uninstalled second drive causes an intervention required indication in response to a start I/O. A two-drive system with an uninstalled fixed disk on the second drive also causes an intervention required when the fixed disk is addressed.

A seek in reverse of too many cylinders may cause the high speed model files to become not ready if the carriage mechanism approaches cylinder zero at a speed greater than the normal speed files. This can occur from cylinder 4 or greater if a reverse seek beyond cylinder zero is attempted. Recalibration will never cause ready to drop as it is executed in low speed mode. To reinstate ready, the file power must be turned off and back on again.

Byte 0, Bit 2—Missing Address Mark. This bit is set on any multisector operation after identifier area orientation is established when any two following sequential sectors read from the file have identical bits in bit position 5 of the head/sector byte of the identifier. If this condition is detected before ID orientation or on a single sector operation, it is indicated after the control unit has determined that the record cannot be found on the track. This bit is also set if no address mark is found and index has passed twice while looking for address mark. This bit is not set if a data check is detected in one of the two identifier fields.

Byte 0, Bit 3—Equipment Check. This bit indicates that the control unit has detected a hardware failure, such as a CC register check, an equipment check write gate, a check counter error, a parallel parity check, or a serdes check. This status bit will also indicate that the selected drive has detected an unsafe drive condition.

Byte 0, Bit 4—Data Check. This status bit indicates that a cyclic check or bit-count appendage check was detected while reading the identifier area or data fields from the file.

Byte 0, Bit 5—No Record Found. This bit indicates that the first identifier called for on a read, write, or scan could not be found on the track; or, after the first hit of a multisector operation, there is a subsequent identifier noncompare. This bit is set with track condition check. The identifier compare takes place on all bits of the identifier.

Byte 0, Bit 6—Track Condition Check. This status bit is an indication that a data operation was attempted, but the track condition bits in the flag byte in main storage did not agree with the track condition bits written on the file.

Byte 0, Bit 7—Seek Check. This status bit indicates that the control unit has detected a seek error caused by one of the following conditions:

1. Access overrun on selected drive while go forward is active
2. Go forward or go reverse active and drive not ready
3. Go reverse active, cylinder zero active and not in a recalibrate operation
4. Go forward or go reverse active for longer than 1 to 2 seconds
5. Track crossing pulse from drive sensed at the end of head settling time

Byte 1, Bit 0—Scan Equal Hit. This status bit indicates that the equal condition was satisfied whenever a scan equal/low, an equal/high, or equal command is issued.

Byte 1, Bit 1—Cylinder Zero. An indication that the selected drive's access mechanism is positioned at cylinder zero.

Byte 1, Bit 2—End of Cylinder. This status indicates that on a multiple sector data or scan operation one of the following occurred:

a. An attempt was made to operate beyond the end of the cylinder. (Head 1 of the selected disk).
b. Head 1 ID's were written on Head 0 (Bit 0=1 of S byte) and an attempt was made to operate beyond the end of the track. This can happen on alternate tracks.

In both cases, all sectors up to and including the last one on the track were successfully handled.

Byte 1, Bit 3—Seek Busy. This bit indicates that the drive addressed by the sense I/O is seeking (includes head settling time).

Byte 1, Bit 4—100 Cylinder. This status bit indicates that the first drive (drive 0) attached to the system has 100 cylinders available to the customer. This indication is generated by the attachment hardware.

Byte 1, Bit 5—Overrun. This bit is set when a data cycle request is not honored within the time required to maintain data transfer with the file. This condition occurs due to a process-check stop which stops the CPU clock.

Byte 1, Bits 6 and 7—Status Address A and Status Address B. Status A and Status B indicate the address of the drive that was specified in the last read, write, or scan instruction. They provide the drive number that pertains to the attachment-dependent status bits.

Bit 6 Status Address A	Bit 7 Status Address B	Drive
0	0	1
0	1	2

This address is updated when a start I/O is accepted or provisionally accepted on either drive.

Byte 2, Bit 0–Unsafe. This bit indicates that one of the following errors has been detected by the disk drive:

1. Write unsafe
   a. Write selected and no write transitions detected.
   b. Write selected and multiple heads selected.
   c. Write not selected and write current source on.
2. Erase unsafe
   a. Write selected and erase current source not on.
   b. Write not selected and erase current on.
3. Read/write selection unsafe
   a. Read selected and either write or erase selected.
   b. Carriage accessing and either write or erase selected.

Byte 2, Bit 1–Tap Line A. Used by the timing analysis program (TAP). These lines can be jumpered at the drive to sense signals that normally are not checked. See note 5.

Byte 2, Bit 2–Tap Line B. Same as byte 2, bit 1.

Byte 2, Bit 3–Tap Line C. Same as byte 2, bit 1.

Byte 2, Bit 4–Index. This line is active for about 43 micro seconds starting with each index pulse from the selected drive.

Byte 2, Bit 5–Head Settling. This line turns on at the end of a seek operation to time out head settling. It is on for 24.67 (+3.2, –3.74) milliseconds for the high speed files and about 28 milliseconds for the standard speed drives.

Byte 2, Bit 6–Wireable CE Sense Bit. This sense bit allows the customer engineer to provide the CPU with MST signals which normally are not available for sensing (used for diagnostic programs).

Byte 2, Bit 7–Model 6. This bit indicates that the CPU is a 5406.

Byte 3, Bit 0, Bits 1 and 2–Wireable CE Sense Bit. Same as byte 2, bit 6.

Byte 3, Bit 3–Not Bit Ring Inhibit. For CE use in diagnostic programs.

Byte 3, Bit 4–Standard Write Trigger. For CE use in diagnostic programs.

Byte 3, Bit 5–Condition Priority Request. This bit indicates the status of the condition-priority-request latch.

Byte 3, Bit 6–Bit Ring 0. This bit is active at bit ring 0 time.

Byte 3, Bit 7–(Not) Cyclic Check-Register Position 17. This bit indicates the status of position 17 of the cyclic check-register.

DFDR/DFCR (N Field = 100 or 110)

The local storage register designated in the N field coding is sensed and the address in the local storage register is transferred into core storage at the address specified in the operand one address.

Sense I/O General Notes

1. If any combination of N bits other than the four designated is used, the operation causes a processor-check stop.
2. The file attachment is not busy to a sense I/O.
3. Sense I/O does not set any file status conditions.
4. The sense bytes are placed in core so that the highest numbered byte is placed at the highest address.
5. TAP lines A, B, and C are normally jumpered to the three unsafe latches in the file drive. If these lines (jumpers) are moved to sense other signals as required in diagnostic programs, be sure to reinstall the jumpers to the unsafe latches. (See 5444 ALD FN260 for drives below serial 30100, 5444 ALD FS260 for drives above serial 30100, for normal jumpering of these lines.)
6. Device status bits equipment check (due to unsafe condition) cylinder zero, seek check, seek busy, intervention required, unsafe, head settling, and index may vary depending on the drive selected by the sense I/O instruction. These bits are presented only when the drive to which they apply is selected. They are reset when the drive to which they apply is selected if the error condition is no longer present. All remaining bits may be presented when either drive is selected by sense I/O. All remaining bits except no-op are reset when a start I/O is executed on either drive. No-op is reset by the sense I/O instruction that transfers no-op to core storage (N code 010).

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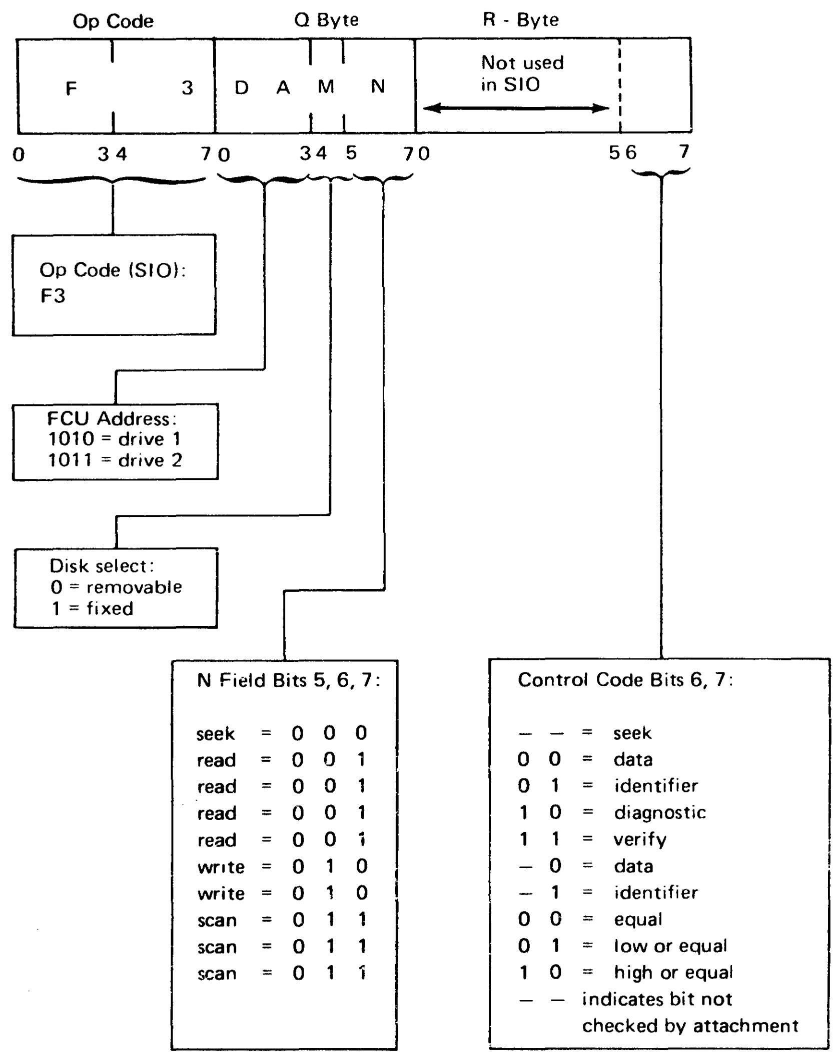
Start I/O (SIO)

- This instruction selects an I/O device and provides the additional information to specify the detailed operation.

The format of the start I/O instruction is:



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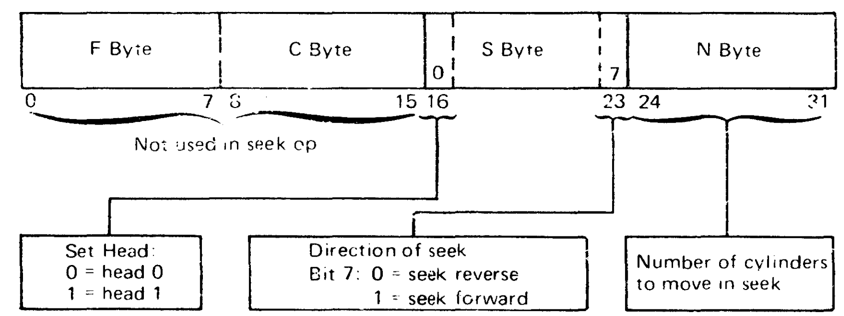
B

There are four basic disk operations: write, read, scan, and seek. These are further defined into twelve specific operations.

Operation	*Definer*
Write	Data
	Identifier
Read	Data
	Identifier
	Diagnostic
	Verify
Scan	Equal
	Low or Equal
	High or Equal
Seek	Forward
	Reverse
	Recalibrate

Seek

The head access of the selected drive is moved a specified number of cylinders, and the specified head number is set for future read, write, or scan operations. Seek uses only two bytes of information from the disk control field: the S and N bytes. The disk file control register address must contain the address of the F byte.



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The N byte specifies the number of cylinders the access mechanism will move on the seek. Bit 23 of the S byte specifies the direction of movement. Forward (bit 23 = 1) is from cylinder 0 to 202.

Recalibration is executed by specifying a seek in the reverse direction and a number of cylinders to be moved that is equal to or greater than 223. Head 0 is selected automatically for a recalibration operation.

Seek Forward: Moves the head-access mechanism forward. (Forward direction is from the outer edge of the disk to the inner tracks.)

Seek Reverse: Moves the head-access mechanism from the inner to the outer edge of the disk.

Seek Recalibrate: Moves the head-access mechanism to cylinder zero. This positions the mechanism to a specific location (cylinder zero) when needed in error recovery routines. On high speed drives, recalibrate operation is always in low (normal) speed.

Write Operations

Write Data: Records data on disk from the data field in core storage.

Write Identifier: Records addresses from the disk control field for sectors and cylinders in the identifier area field on disk. Address marks and gaps generated by the file control unit are written by this command. Twenty-four sectors are always written.

Read Operations

Read Data: Recovers data recorded on disk and transfers this information to the data field in core storage.

Read Identifier: Transfers only the identifier area field information on disk into the disk control field.

Read Diagnostic: The file control unit is operated with reduced requirements for detection of address marks. Otherwise, this operation is very similar to read data.

Read Verify: Does not transfer any information. Regenerates the cyclic check and bit count appendage check characters and compares them with the check characters recorded on the disk. This command usually follows a write operation and verifies that the data-check characters were written correctly.

Scan Equal: Compares data on disk with data in core. The result is indicated by a status bit and is available to a sense I/O instruction or test I/O instruction.

Scan Low or Equal and Scan High or Equal: These commands differ from scan equal only in the indication returned about the compare.

Initial Program Load (IPL)

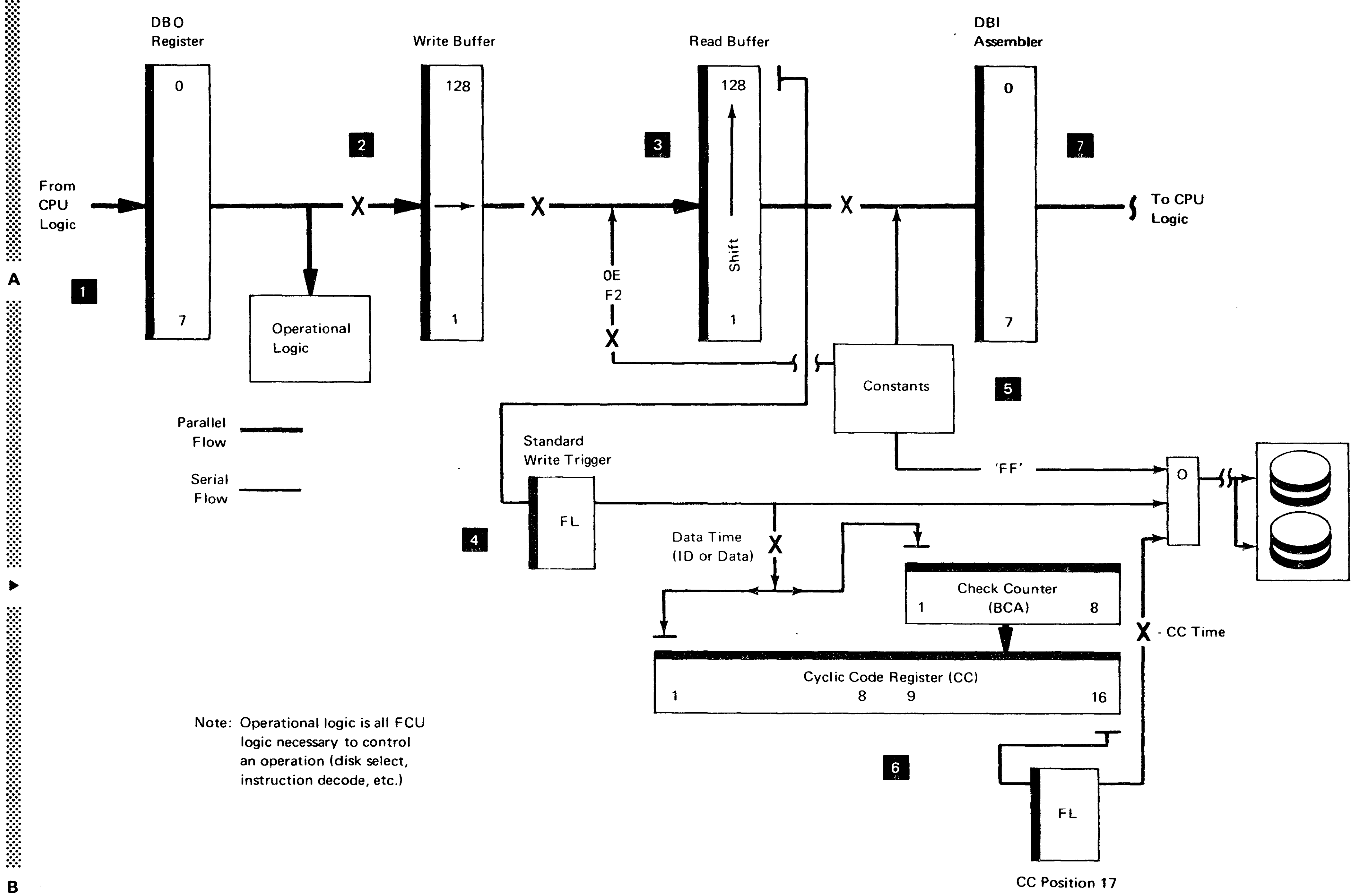
The initial program load operation is not under program control. It is started with the program load switch on the operator console.

An initial program load operation reads a 256-byte data field from sector 0, head 0, from either the fixed or removable disk as determined by the program load selector switch on the operator console. Drive 1 is selected by the file control unit. Initial program load cannot be performed from drive 2.

At the start of an initial program load operation, the disk file data register address is set to 0000 and a seek recalibrate is performed to position the read heads to cylinder 0. Data is read from the first sector past index (sector 0). At the end of the data field, the file control unit signals the central processing unit to start processing at core address 0000.

No compare is made on the identifier of the first record; the first record found after the index mark is read and any error conditions are made available for program testing. If no record is found or the wrong record is read, the program will not start correctly. An unsuccessful initial program load operation requires an operator retry.

A test I/O and branch instruction should be performed to test for errors or busy before attempting the first start I/O instruction.



Write Operation

1 Start I/O instructions and data enter the file control unit via the data bus out. The Q and R bytes are decoded for the file control unit address and the specific operation to be performed. The operation is stored in the operation register within the operational logic.

2 After the start I/O operation I-Q and I-R cycles are complete, the file control unit requests a cycle steal, selects a local storage register for an address of a control or data field, and receives the data (in parallel) into the write buffer from the data bus out. One data byte is buffered (stored) in the write buffer until it is needed at the read buffer.

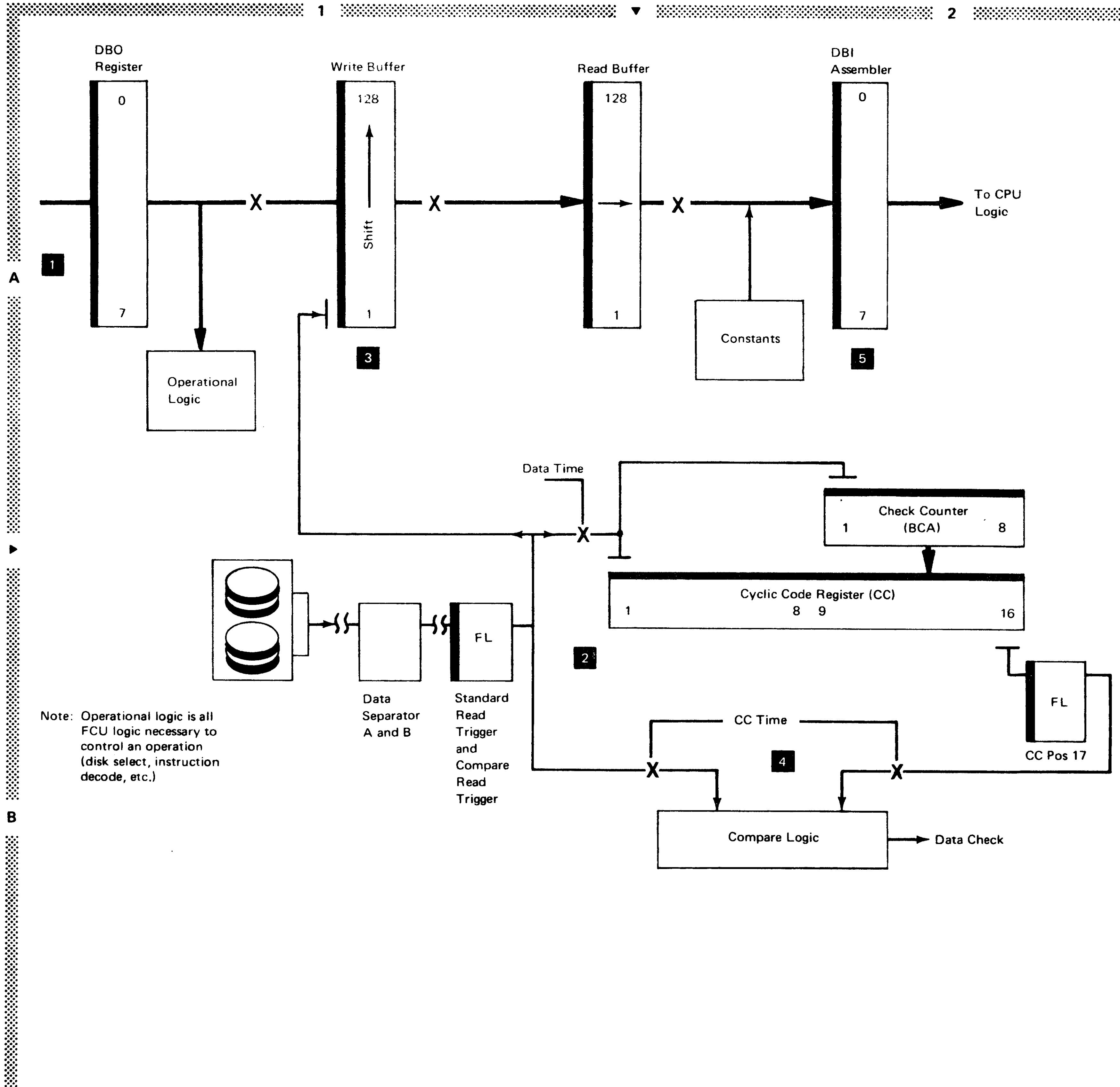
3 Control circuits transfer the write buffer to the read buffer, start a shift operation to serialize the byte, and at the same time generate another cycle steal request to refill the write buffer.

4 The shifted bits are transferred out of the read buffer into the standard write trigger. The standard write trigger output is combined with clock signals and sent to the drive to be recorded.

5 Constants for address marks (F2) and sync bytes (0E) are generated by the constants generator and gated into the read buffer to be serialized. One constant FF is combined directly with clock bits to write all ones on the disk. Other constants are gated onto the data bus in to modify the local storage register addresses.

6 The serialized data bits enter the check counter and cyclic code register to generate the cyclic check and bit count appendage check characters. At the end of the identifier area or data field, the cyclic check register shifts (serializes) the register contents into cyclic check register position 17. This register position functions in the same manner as the standard write trigger. Its output is combined with clock timing and sent to the drive to be recorded on disk.

7 The data bus in assembler gates the constants onto the data bus in lines for use at the CPU.



Note: Operational logic is all FCU logic necessary to control an operation (disk select, instruction decode, etc.)

Read Data Operation

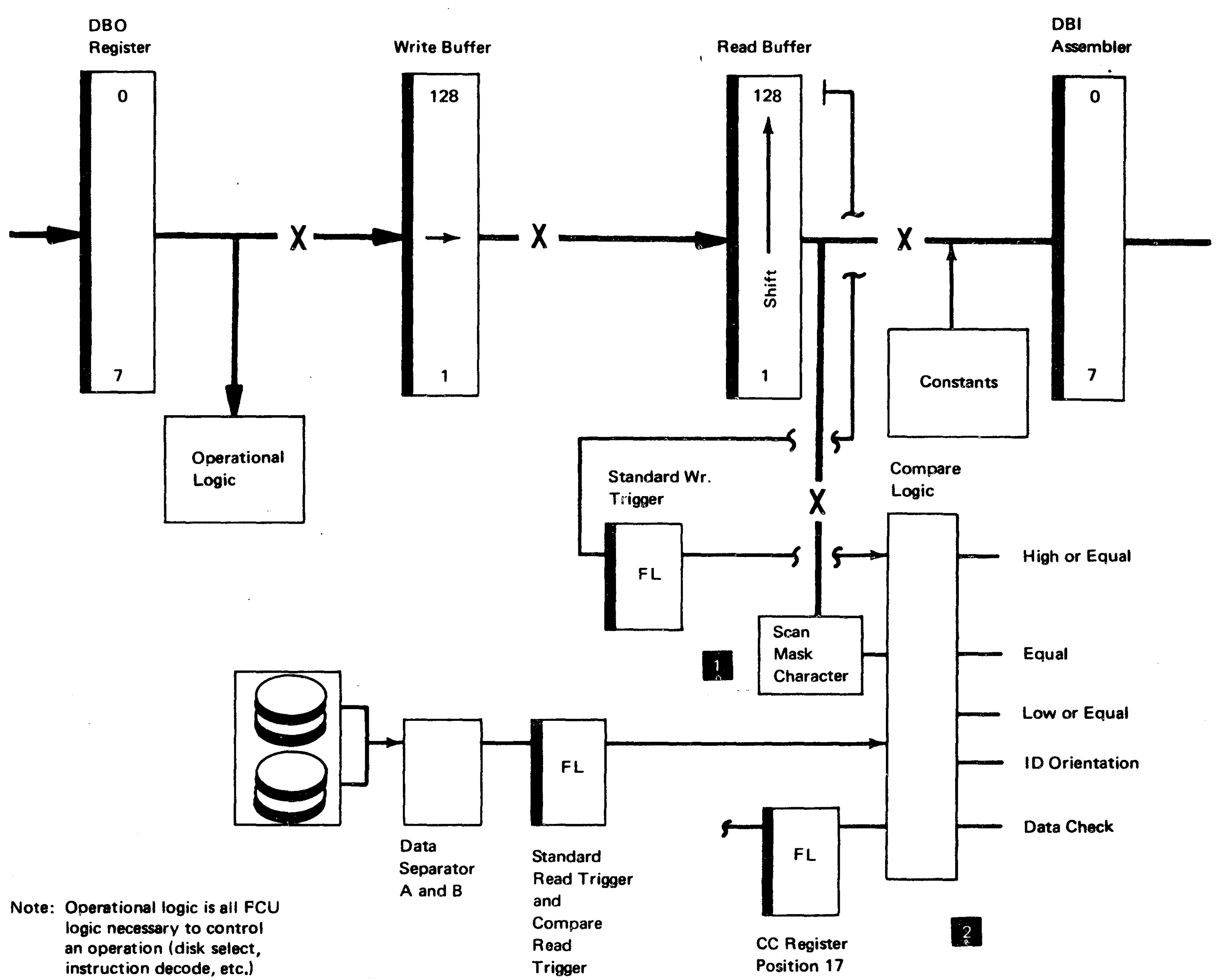
1 Start I/O instructions enter the file control unit via the data bus out register. The Q and R bytes are decoded for the file control unit address and the specific operation to be performed. The operation is stored in the operation register within the operation logic.

2 The drive is conditioned to read data from the disk. Raw data from the drive enters the file control unit through the data separator, standard read, and compare read triggers. The data bits enter the check counter and cyclic code register to regenerate the bit count appendage and cyclic check characters, and enter the write buffer to be deserialized.

3 The serial bits enter the write buffer until it is full (8 bits). Then the write buffer register contents are transferred to the read buffer until a cycle steal operation can gate the read buffer onto the data bus in and transfer the byte to the CPU.

4 At the end of the identifier area or data field, the regenerated cyclic check and bit count appendage characters are compared to the check characters recorded on disk with the compare logic. The characters should compare correctly; if not, a data check is indicated.

5 Constants are gated onto the data bus in when needed to modify local storage register addresses.



Note: Operational logic is all FCU logic necessary to control an operation (disk select, instruction decode, etc.)

Compare/Scan Operation

The file control unit compare function looks at data from two sources and indicates the result of the compare. Examples of compare are:

1. The file control unit searching for a specific address on the disk. Data in the disk control field is compared to the identifier area field read from disk. When a correct compare (match) is found, identifier area orientation is active.
2. A data field in core storage may be compared to a data field on disk and the result indicated as file control unit status. An equal, low or equal, or high or equal indication may result.
3. Cyclic code and bit count appendage check characters are regenerated when data is read. The regenerated characters are compared to the check characters recorded on the disk at the end of identifier area and data fields, to check that the data was recovered properly. The compare function resembles a combination disk read and disk write operation. Disk control field data from the CPU is serialized in the same manner as in a write operation but is not gated out to the disk. Identifier area field data read from the disk is received into the file control unit in the same manner as in a read operation, and gated to the compare logic to compare against the data from the CPU.

1 A scan operation (sense I/O instruction) is different only because a scan mask character (hex 'FF') can prevent a compare (block) until the scan mask is no longer present.

2 To compare check characters, the cyclic check register position 17 is gated to the compare logic along with the data read from disk. A data check results if a noncompare is found.

1 ▼ 2 ▼ 3

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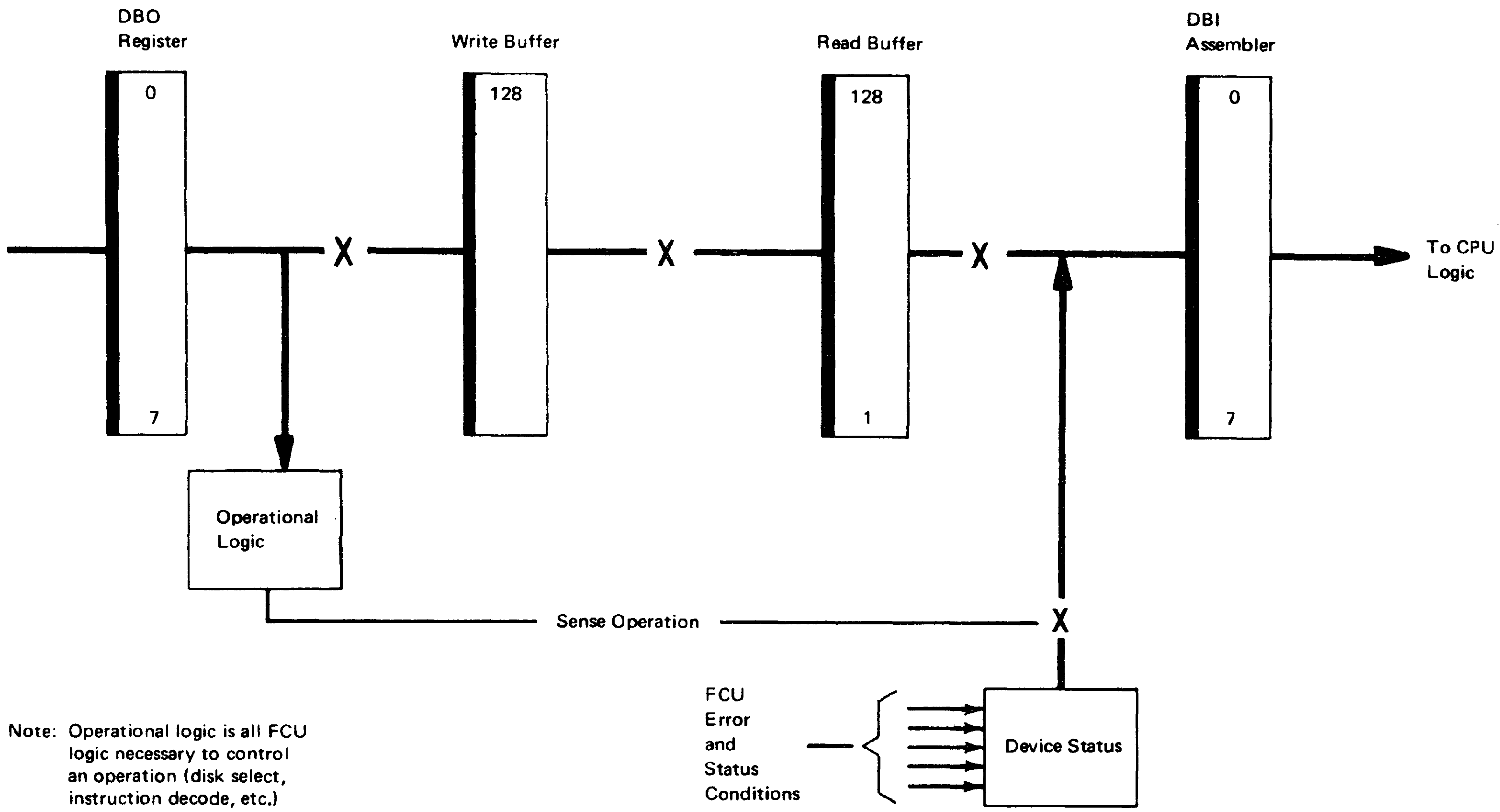


Note: Operational logic is all FCU logic necessary to control an operation (disk select, instruction decode, etc.)

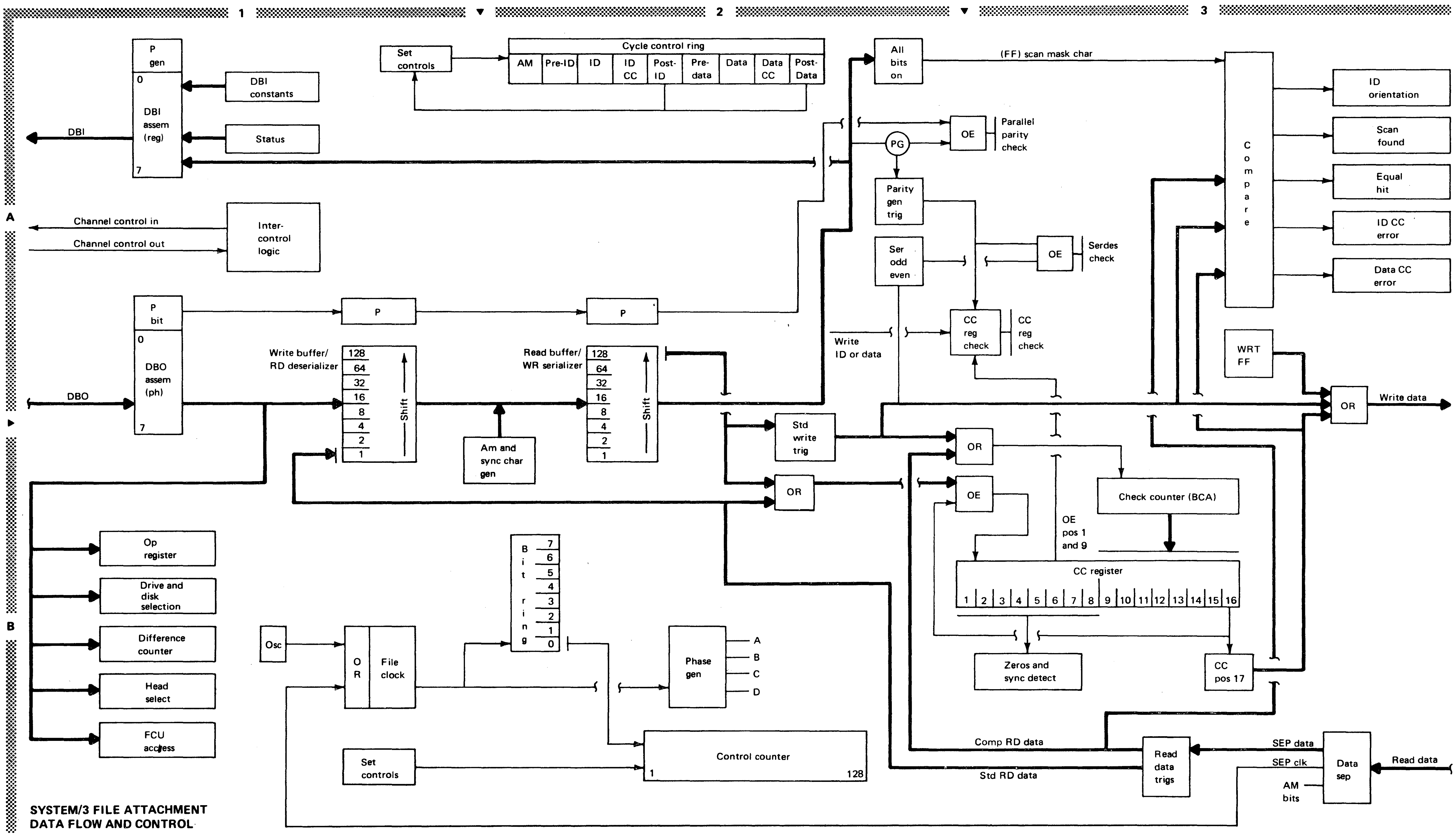
B

Sense Operation

A sense operation does not require any data transfer from the CPU or drive. The instruction is decoded in the file control unit and gates the file control unit status onto the data bus in for use at the CPU.

Load I/O and Test I/O Operations

These instructions do not transfer data through the file control unit. A load I/O instruction selects a local storage register in the CPU. The test I/O instruction causes the file control unit to return an I/O condition A or I/O condition B in response to a specific test command.



SYSTEM/3 FILE ATTACHMENT DATA FLOW AND CONTROL

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B

INTRODUCTION TO FUNCTIONAL UNITS

This chapter describes the functional units of the disk attachment and contains second-level diagrams. Chapter 2 is divided as follows:

1. A functional unit index for the second-level diagrams and a cross reference chart for card locations vs ALDs.
2. A layout of the disk attachment board and the major logic functions within each card.
3. An overall data flow of the disk attachment.
4. A CPU-to-disk attachment and disk-attachment-to-disk-drive interface diagram.
5. Second-level diagrams combined with descriptions of the functional units.

Each card location has its own group of second-level diagrams. For most card locations, there is a description of the functional units contained on the card in front of the second-level diagrams.

The 8-XXX references on the second-level diagrams are page numbers to the card second-level diagram that originates the incoming signal line. An asterisk refers to an interface line and is shown on the interface diagram, page 8-205. There are no second-level diagrams for drive 1 seek controls, card F2, because the logic on card F2 is identical to the logic on card G2. Where a drive 1 seek control line is referenced on the second-level diagrams, the reference is to a card G2 diagram. The reference is in parentheses to indicate that it actually originates on card F2:

Example

8-213 refers to drive 0, card G2
(8-213) refers to drive 1, card F2

The GDXXX references below latches and logic blocks within the diagrams refer to disk attachment ALDs. The GDXXX numbers in the lower left corner of each diagram refer to the span of disk attachment ALD pages for that card position.

File control units to attach standard speed access drives, use version 000 ALDs. File control units to attach high speed access drives use version 001 ALDs. Version numbers are printed below the ALD page number.

1 2 3

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Functional Unit Index

Functional unit	Card location	Description	Diagram
Address mark detect	L2	8-224	8-225
Bit ring	L2	8-224	8-225
CE controls	P2	8-236	8-237
Check counter (BCA)	P2	8-236	8-237
Clock	R2	8-244	8-247
Clock gate	J2	8-216	8-217
Compare	N2	8-232	8-234
Compare read data trigger	L2	8-226	8-227
Constants	Q2	——	8-243
Control counter	K2	8-222	8-223
Cycle control ring	K2	8-220	8-221
Cyclic code register	L2	8-226	8-227
Data separator	D4-E4	8-208	8-209
Data bus in (DBI)	R2	8-244	8-245
Data bus out (DBO)	S2	8-248	8-251
Difference counter	G2	8-212	8-213
Erase gate	J2	8-216	8-219
Error conditions	M2 - N2	8-228	8-230 thru 8-235
Go slow counter	G2	8-214	8-214
Index	J2	8-216	8-218
Initial selection	T2	8-252	8-253, 8-254
Initial program load (IPL)	P2	8-236	8-239
LSR selection	P2	8-236	8-239
Operation register	S2	8-248	8-249
Priority request 3 (data)	Q2	8-240	8-241
Priority request 7 (seek)	E2	8-210	8-211
Read buffer	S2	8-248	8-251
Read gate	J2	8-216	8-217
Resets	M2	8-228	8-230, 8-231
Seek (common controls)	E2	8-210	8-211
Seek (individual drive controls)	G2	8-212	8-213, 8-215
Serdes	S2	8-248	8-251
Serdes control	Q2	8-240	8-241
Standard read data trigger	L2	8-226	8-227
Standard write trigger	S2	8-248	8-251
Write buffer	S2	8-248	8-251
Write gate	J2	8-216	8-219

CARD ALD cross reference chart			
By card location		By ALD location	
C2	GD–811	GD–101-104	R2
C3	801	111-117	L2
C4	901-902	121-125	K2
D2	911	201-204	T2
D3	501	211-216	S2
D4	511-512	301-304	E2
E2	301-304	311-317	G2
E4	521	321-327	F2
F2	321-327	501	D3
G2	311-317	511-512	D4
H2	not used	521	E4
J2	621-626	601-606	P2
K2	121-125	611-615	Q2
L2	111-117	621-626	J2
M2	711-713	701-706	N2
N2	701-706	711-713	M2
P2	601-606	801	C3
Q2	611-615	811	C2
R2	101-104	901-902	C4
S2	211-216	911	D2
T2	201-204		
U2	not used		

1 ▼ 2 ▼ 3

Note 1

Location	Functions	ALD page(s)	Card type
A2			
B2			
C2	TAPs line receivers	ALD page GD811	7043
C3	File meter	ALD page GD801	6456
C4	File line drivers; Spindle 0 and 1 ready; Drawer release; Drawer release light	ALD pages GD901 thru GD902	3362
D2	File line drivers	ALD page GD911	3363
D3	FCU osc; Write drivers	ALD page GD501	0997
D4	Data separator	ALD pages GD511 thru GD512	0998
E2	Common seek controls; Seek cycle; Priority request 7; Seek times 1, 2, 3, 4; Seek time out counter; Head settle counter; Disk select	ALD pages GD301 thru GD304	3353
E4	Data separator	ALD page GD521	7874
F2	Spindle 1 seek control; Difference counter; Seek time out counter; Initial seek time; Forward-reverse; Go; Reset go; Recalibrate op; Pre end; End seek; Seek check; Head trigger	ALD pages GD321 thru GD327	Note 2
G2	Spindle 0 seek control; Difference counter; Seek time out counter; Initial seek time; Forward-reverse; Go; Reset go; Recalibrate op; Pre end; End seek; Seek check; Head trigger	ALD pages GD311 thru GD317	Note 2
H2	(not used)		
J2	Read gate; Write gate; Erase gate; Clock gate; Write data; Execute; Write FF; N carry; Index	ALD pages GD621 thru GD626	3358
K2	Cycle control ring and controls; Control counter and controls; Count zero gate	ALD pages GD121 thru GD125	3350
L2	Bit ring; Cyclic check register; Sync detect; Zeros detect; Address mark detect; Standard read data trigger; Compare read data trigger	ALD pages GD111 thru GD117	3349
M2	Resets; Select file; Start op; FCU error 1; No record found; Set end of cylinder; Intervention required; Overrun	ALD pages GD711 thru GD713	3361
N2	Compare Scan; ID orientation; CC register check; Parallel parity check; Serdes check; FCU error 1, 2 and 3; Track condition check; Data check	ALD pages GD701 thru GD706	3360
P2	LSR select; IPL; CE controls; Check counter (BCA); Check counter error; Sense byte selection	ALD pages GD601 thru GD606	3355
Q2	Priority request 3; Input data time; Data area; ID area; Serdes controls; Constants; CPU controls	ALD pages GD611 thru GD615	3357
R2	DBI assembler; FCU clock; Phase oscillator	ALD pages GD101 thru GD104	3348
S2	Op register; Spindle select; Serdes; Bus out; Parity check; Standard write trigger	ALD pages GD211 thru GD216	3352
T2	Initial selection; CE mode; I/O condition A and B; I/O attention	ALD pages GD201 thru GD204	3359
U2	(not used)		
V2	Cable; Cable; Cable; Cable		

For FCU with high speed access only; Go slow counter Aux counter

A

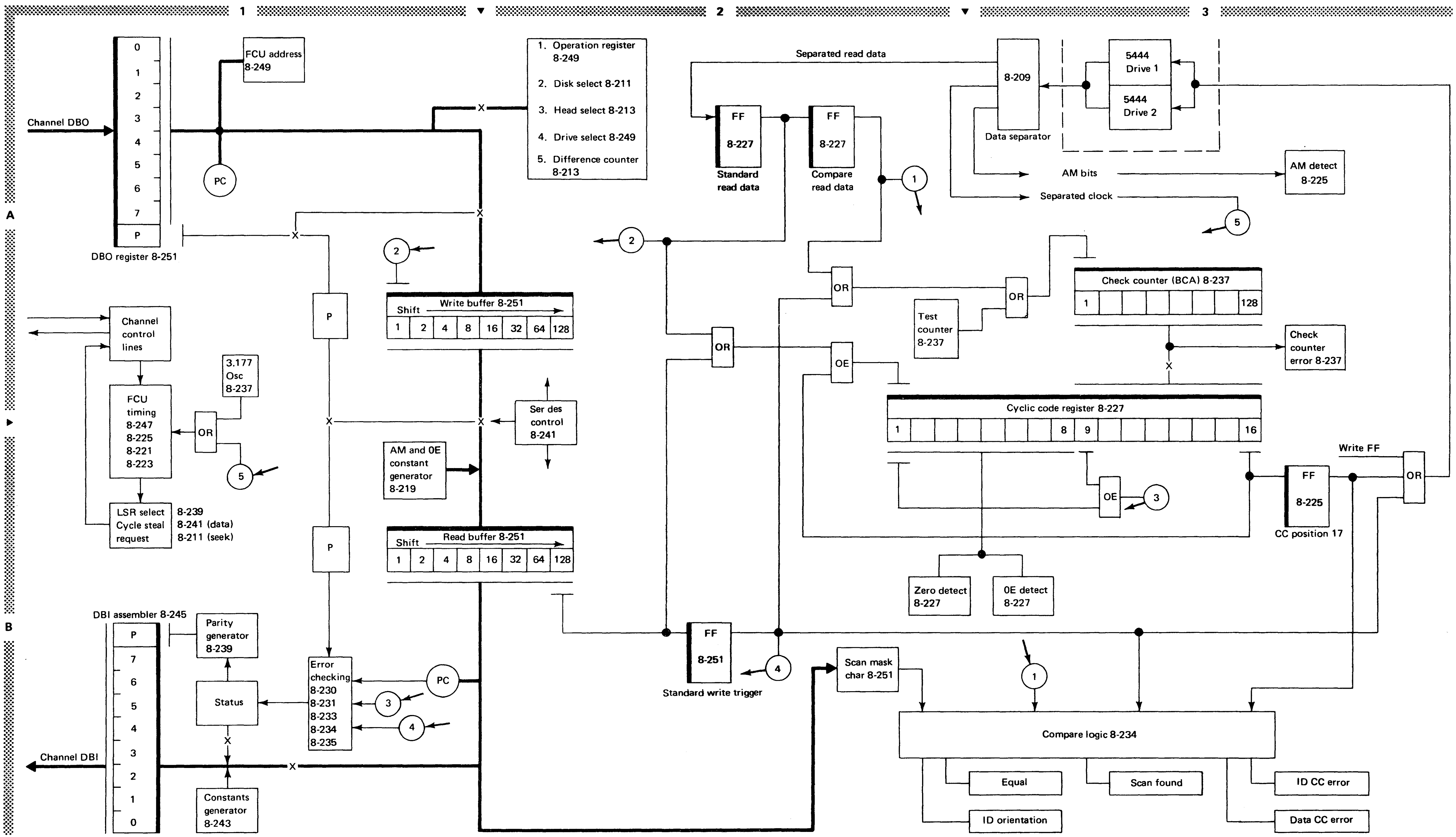
B

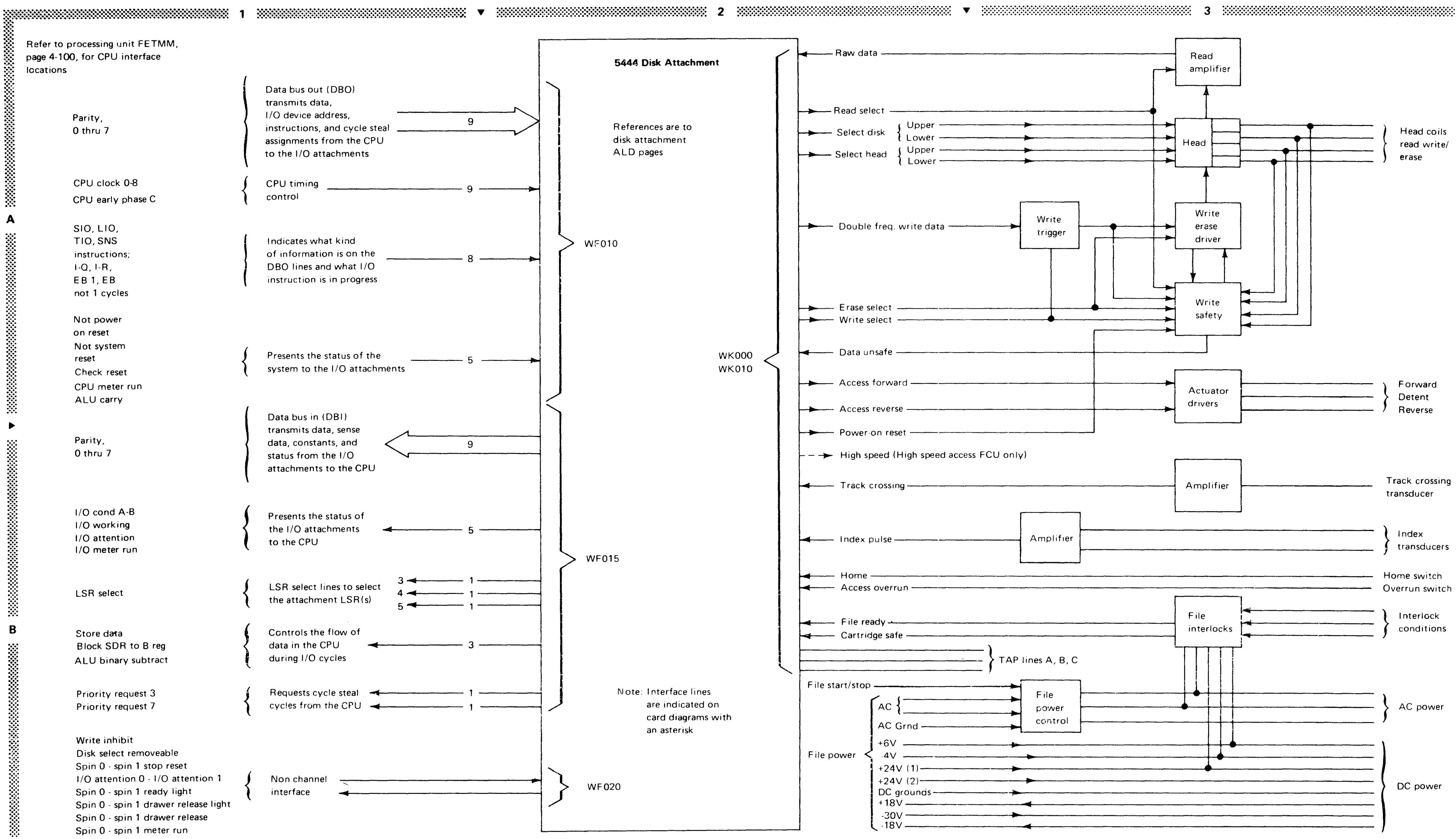
Note 1. Card F2 logic is identical to card G2 except for drive reference. Card F2 is not shown in the second level diagrams, refer to card G2 for drive 1 logic representation

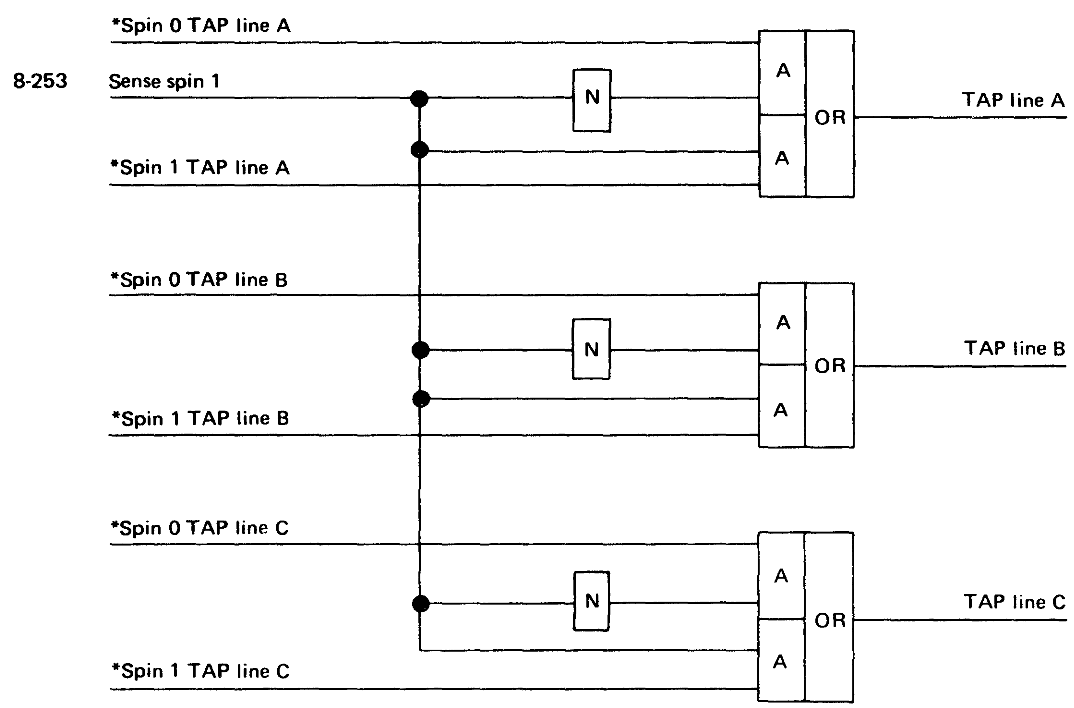
Note 2. Card type for FCU without high speed access is 3354, with high speed access card type is 6884

(card side)

5410 Disk attachment board location is 01A-A2
5406 Disk attachment board location is 01A-A1

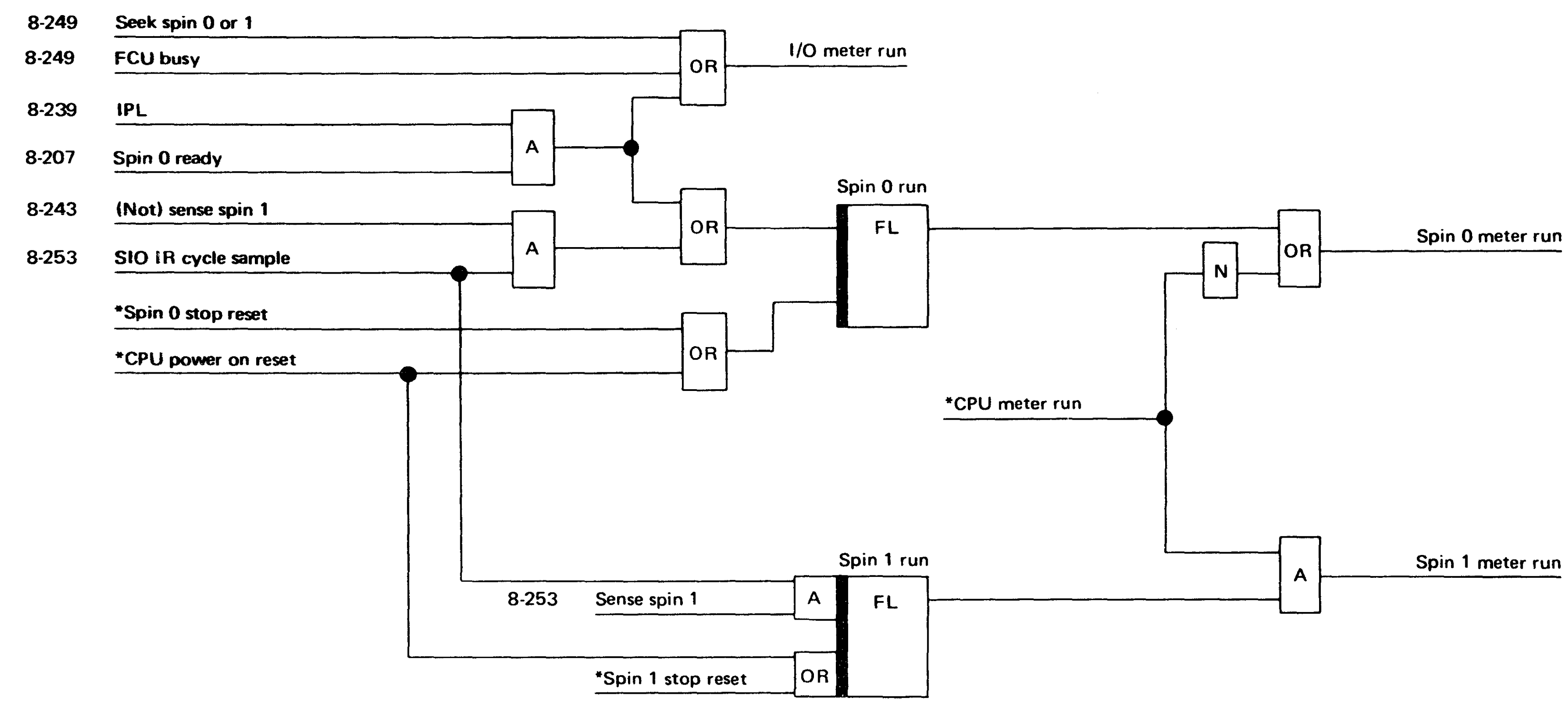

Channel DBO
DBO register 8-251
FCU address 8-249
PC
1. Operation register 8-249
2. Disk select 8-211
3. Head select 8-213
4. Drive select 8-249
5. Difference counter 8-213
Separated read data
8-209
Data separator
5444 Drive 1
5444 Drive 2
FF 8-227
Standard read data
FF 8-227
Compare read data
AM bits
AM detect 8-225
Separated clock
Channel control lines
FCU timing 8-247 8-225 8-221 8-223
3.177 Osc 8-237
OR
LSR select Cycle steal request
8-239
8-241 (data)
8-211 (seek)
Write buffer 8-251
Shift
1 2 4 8 16 32 64 128
P
Ser des control 8-241
AM and OE constant generator 8-219
Read buffer 8-251
Test counter 8-237
Check counter (BCA) 8-237
Check counter error 8-237
OE
Cyclic code register 8-227
Write FF
FF 8-225
CC position 17
Zero detect 8-227
OE detect 8-227
DBI assembler 8-245
Parity generator 8-239
Status
Error checking 8-230 8-231 8-233 8-234 8-235
Constants generator 8-243
Channel DBI
FF 8-251
Standard write trigger
Scan mask char 8-251
Compare logic 8-234
Equal
Scan found
ID CC error
ID orientation
Data CC error


1
2
3
A
B
Refer to processing unit FETMM, page 4-100, for CPU interface locations
Parity, 0 thru 7
Data bus out (DBO) transmits data, I/O device address, instructions, and cycle steal assignments from the CPU to the I/O attachments
9
CPU clock 0-8
CPU early phase C
CPU timing control
9
SIO, LIO, TIO, SNS instructions; I-Q, I-R, EB 1, EB not 1 cycles
Indicates what kind of information is on the DBO lines and what I/O instruction is in progress
8
Not power on reset
Not system reset
Check reset
CPU meter run
ALU carry
Presents the status of the system to the I/O attachments
5
Parity, 0 thru 7
Data bus in (DBI) transmits data, sense data, constants, and status from the I/O attachments to the CPU
9
I/O cond A-B
I/O working
I/O attention
I/O meter run
Presents the status of the I/O attachments to the CPU
5
LSR select
LSR select lines to select the attachment LSR(s)
3
4
5
1
1
1
Store data
Block SDR to B reg
ALU binary subtract
Controls the flow of data in the CPU during I/O cycles
3
Priority request 3
Priority request 7
Requests cycle steal cycles from the CPU
1
1
Write inhibit
Disk select removeable
Spin 0 - spin 1 stop reset
I/O attention 0 - I/O attention 1
Spin 0 - spin 1 ready light
Spin 0 - spin 1 drawer release light
Spin 0 - spin 1 drawer release
Spin 0 - spin 1 meter run
Non channel interface
5444 Disk Attachment
References are to disk attachment ALD pages
WF010
WF015
WF020
WK000
WK010
Note: Interface lines are indicated on card diagrams with an asterisk
Raw data
Read amplifier
Read select
Select disk
Upper
Lower
Select head
Upper
Lower
Head
Head coils read write/ erase
Double freq. write data
Write trigger
Write erase driver
Erase select
Write select
Write safety
Data unsafe
Access forward
Access reverse
Actuator drivers
Forward
Detent
Reverse
Power on reset
High speed (High speed access FCU only)
Track crossing
Amplifier
Track crossing transducer
Index pulse
Amplifier
Index transducers
Home
Home switch
Access overrun
Overrun switch
File ready
Cartridge safe
File interlocks
Interlock conditions
TAP lines A, B, C
File start/stop
File power control
AC
AC Grnd
AC power
File power
+6V
-4V
+24V (1)
+24V (2)
DC grounds
+18V
-30V
-18V
DC power



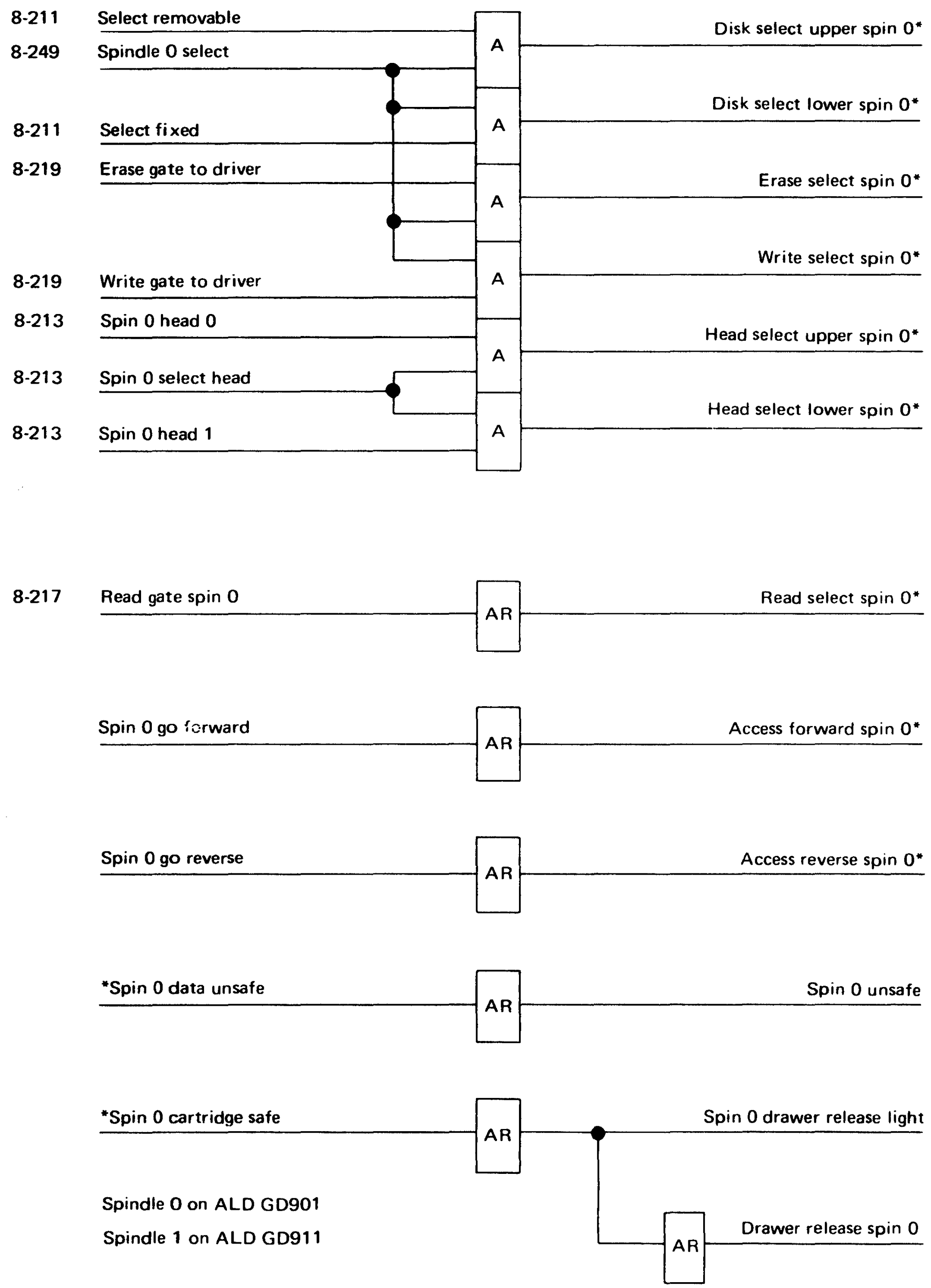
Card C2
GD801 thru GD811

*Interface Line Page 8-205



Card C3
GD801 thru GD811

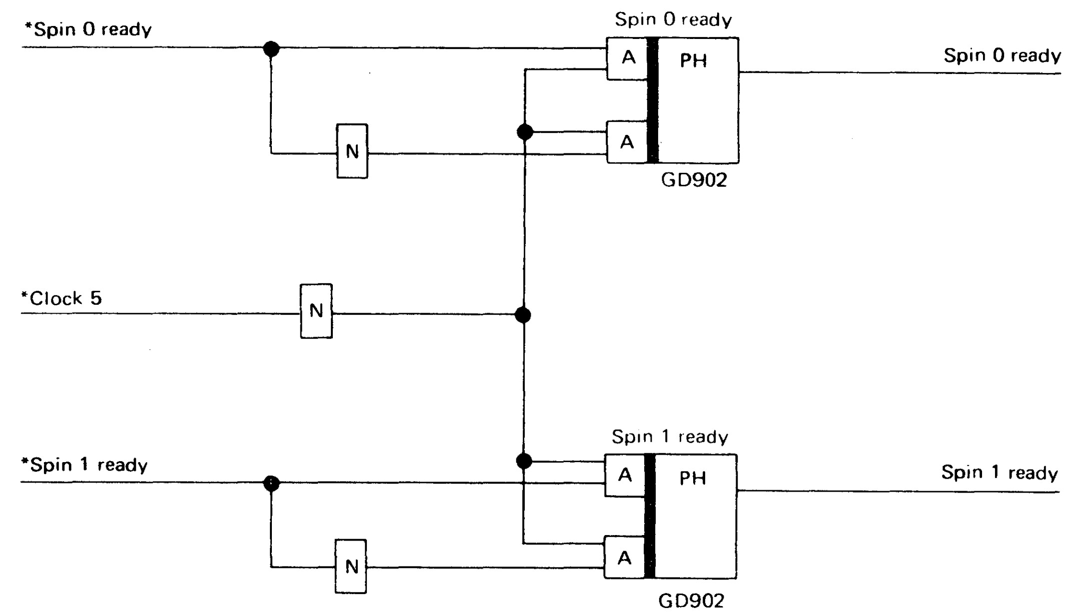
*Interface line page 8-205



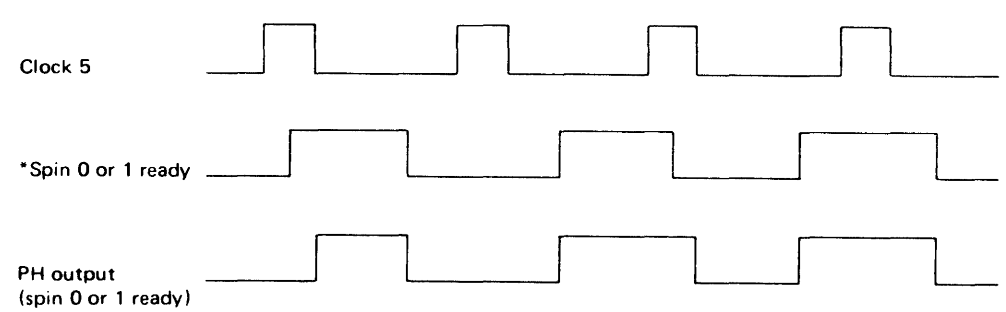
Note: Only spindle 0 lines are shown. Spindle 1 lines are identical except for spindle reference

*Interface line page 8-205

GD901 thru GD911



Note: Spin 0 or spin 1 ready may set or reset only at (not) clock 5 time



*Interface line page 8-205

GD901 thru GD911

CARDS D3, D4, AND E4

Cards D3, D4, and E4 are shown on one diagram and contain the following logic:

1. File control unit oscillator (card D3)
2. Data separator (cards D4 and E4)

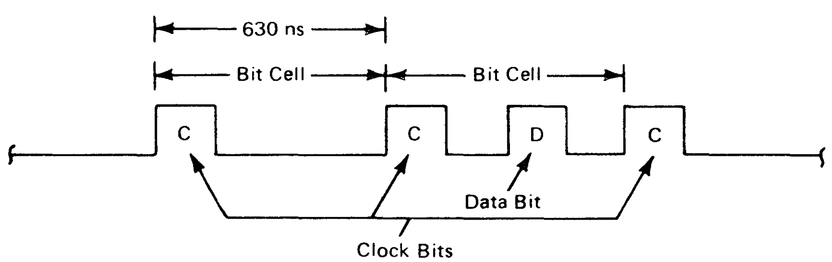
The file control unit oscillator produces a 3.177 MHz square-wave signal which is gated into the file control unit clock with 'clock gate'.

Raw data received from the drive consists of clock bits, data bits, and address marks. The function of the data separator is to separate the three signals into different outputs: separated clock, separated data, and address mark bits.

The data separator must be stabilized before it can function properly. This is accomplished by reading at least 10 bytes of FF followed by at least 7 bytes of 00, which explains the purpose of the sector gaps before each address mark in the track format.

After the data separator is stabilized on clock bits by reading zeros, it directs each clock bit detected to the separated clock output. The separated clock output drives the file control unit clock during a read operation.

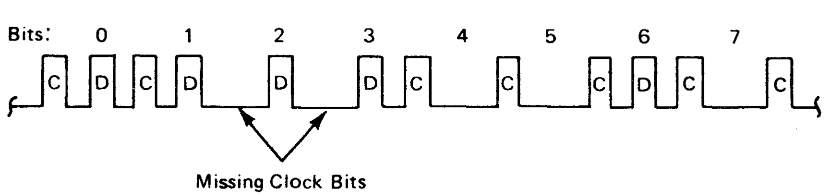
The space between two clock pulses is called a bit cell. Data bits are recorded after a clock bit. Therefore a bit detected after a clock bit is recognized as a data bit and is directed to the separated data output.



BR0464A

Separated data pulses are processed by the file control unit standard-read and compare-read triggers. As a result, the compare-read data signal is one bit cell in length and one bit cell later in relation to when the data bit was read.

Each sector begins with an address mark (AM), a unique pattern encoded on the disk which cannot be found in a data pattern. Within the limitations of double frequency recording, the only possibility is the omission of clock bits. Two bytes of F2, with clock bits missing, are written for address marks.



BR0465

The data separator can detect the missing clock bits and direct this indication to a separate output, address mark bits. Address mark bits are processed by the address mark detect logic on card L2-1, to check if the address mark bits are in proper relation to the rest of the file control unit timing circuits.
These checks are:

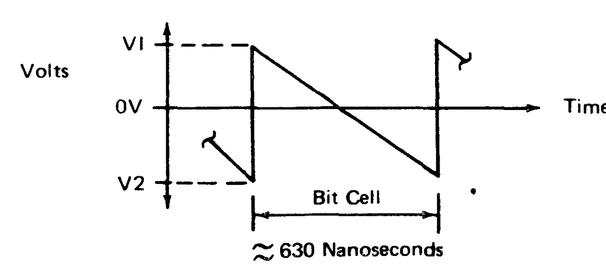
1. That there was compare data during bit ring 0, 1, and 6 time. If not, there may have been missing bits in the address mark.
2. That address mark indicate was not active during bit ring 0, 1, 4, 5, 6, or 7 time. If address mark indicate is detected during this time, a false address mark detect or an address mark was detected at the incorrect time.
3. That compare read was not up at bit ring 2, 3, 4, 5, or 7 time. This indicates that bits were read when they should not have been.
4. That address mark indicate was active at bit ring 2 and 3 time.

All operations, except read data diagnostic, check for all four of the above requirements for address mark detection. Read data diagnostic reduces the requirements by eliminating check conditions 1, 2, and 3. If any of the check conditions are detected during an operation (check 4 for read data diagnostic), start address mark search FL is reset to prevent generation of the address mark detect signal.

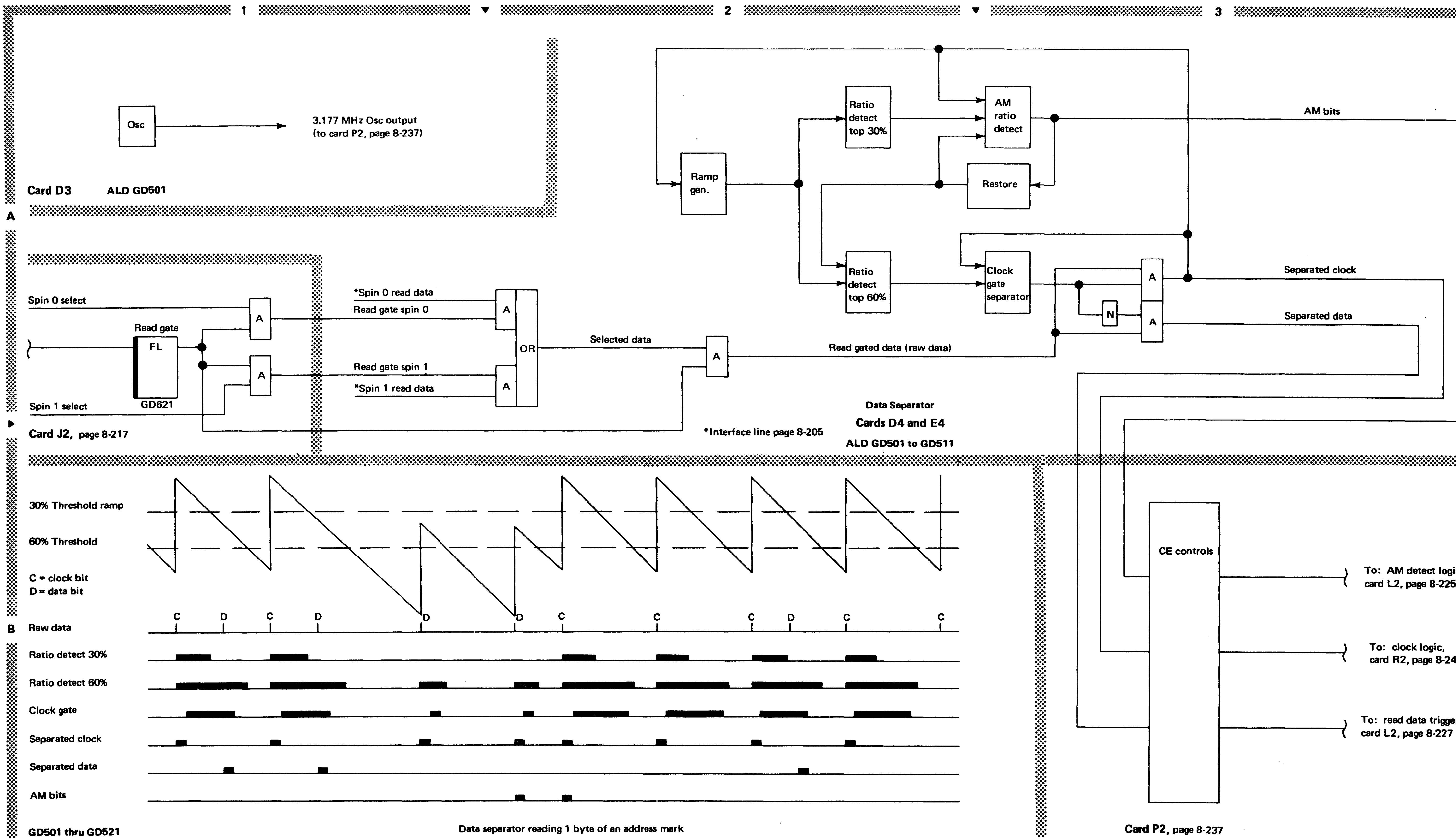
Data Separator Adjustment:

Note. Board locations differ with CPUs. XX refers to board A-A2 in the 5410, to A-A1 in the 5406.

1. Remove card in location A-XXJ2 to select 'read gate spin 0' and 'read gate' for data separator A card.
2. Disable '+spin 0 read data' and '+spin 1 read data' inputs to data separator A, with jumpers to –4 volts (D4G13 to D4B06) and (D4J13 to D4G06).
3. Disable 'ratio circuit 2' output on data separator A with jumper to logic ground (D4B07 to D4D08).
4. Jumper '3.177 MHz osc output' signal on oscillator card (D3D07) into data separator A card (D4G03).
5. Observe 'ramp' waveform on data separator B output (E4G02).
6. Adjust potentiometer on data separator B card (A-XXE4) until 'ramp' waveform is swinging equally about logic ground with a ±100 millivolt tolerance. V1 should equal V2 within ±100 mV.



BR0471


Osc
3.177 MHz Osc output
(to card P2, page 8-237)
Card D3 ALD GD501
Spin 0 select
Read gate
FL
GD621
Spin 1 select
Card J2, page 8-217
*Spin 0 read data
Read gate spin 0
Read gate spin 1
*Spin 1 read data
OR
Selected data
Read gated data (raw data)
Ramp gen.
Ratio detect top 30%
Ratio detect top 60%
AM ratio detect
Restore
Clock gate separator
N
AM bits
Separated clock
Separated data
Data Separator
Cards D4 and E4
ALD GD501 to GD511
*Interface line page 8-205
30% Threshold ramp
60% Threshold
C = clock bit
D = data bit
Raw data
Ratio detect 30%
Ratio detect 60%
Clock gate
Separated clock
Separated data
AM bits
GD501 thru GD521
Data separator reading 1 byte of an address mark
CE controls
To: AM detect logic, card L2, page 8-225
To: clock logic, card R2, page 8-247
To: read data trigger, card L2, page 8-227
Card P2, page 8-237

CARD E2

Card E2 is shown on one diagram and contains seek controls that are common to the individual drive seek controls shown on card G2. The following logic is shown:

1. Head settle common counter
2. Seek-time-out common counter
3. Priority request 7
   (seek cycle-steal request)
4. Fixed-removable disk selection
5. Sense signals for device status

The head settle common counter is advanced by clock 0 from the CPU and steps continuously. The counter's output is gated to the selected drive difference counter during head settle time, to develop a 27.6 to 28.3 ms time delay. This time delay prevents another start I/O instruction operation from starting until the access mechanism motion has stopped, following a seek operation.

The seek time-out common counter is advanced by raw index pulses from spindle 0 if spindle 1 is not ready, or from spindle 1 if spindle 1 is ready. This counter's output is gated to the selected drive's seek-time-out counter when 'go' for the selected drive is active. The purpose of this counter is to develop a 1 to 2 second time base which is used to set a seek check if a seek operation has not ended within this time.

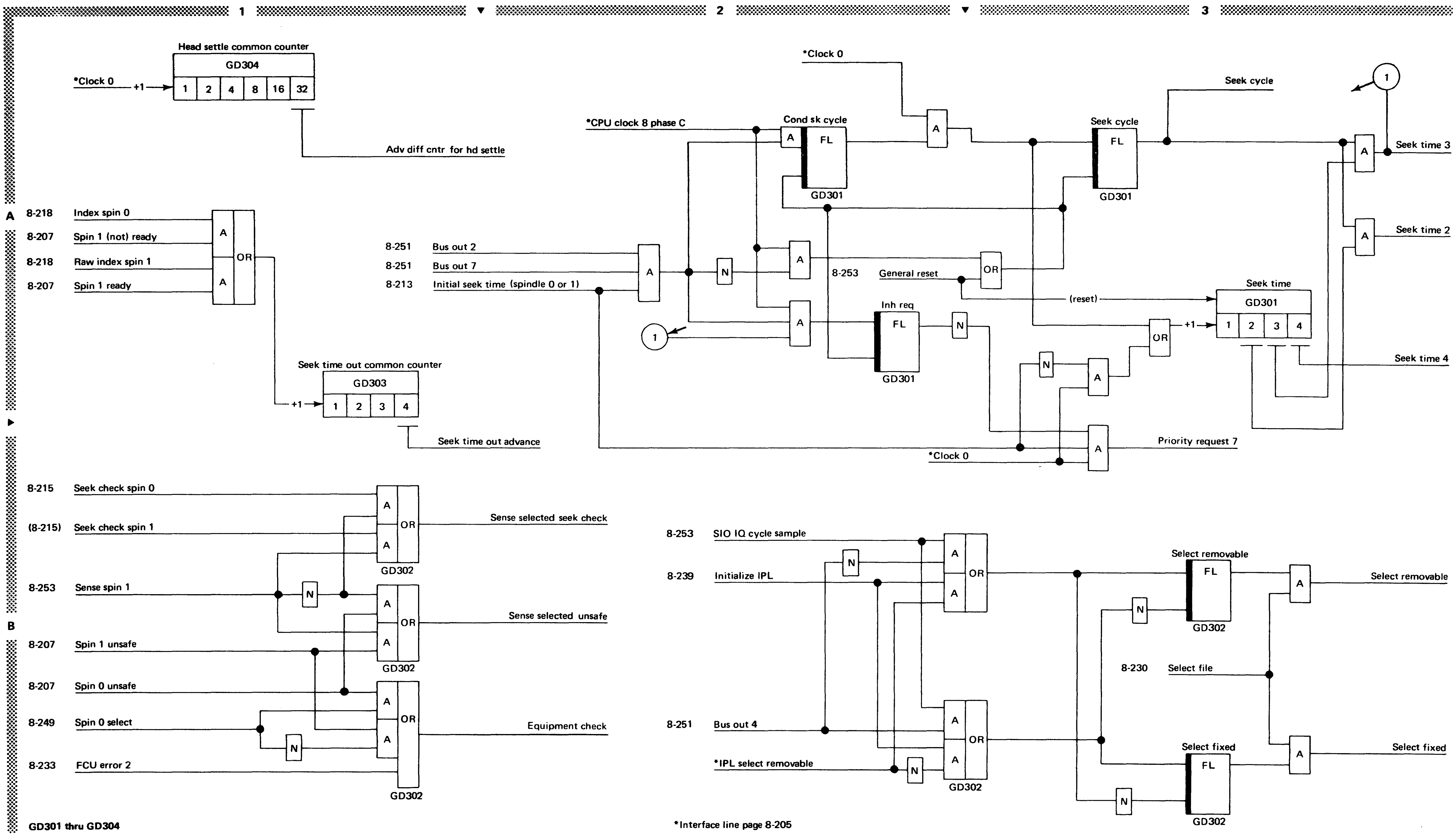
Priority request 7 is the seek instruction cycle steal request (CSR). Four CSRs are made during a seek operation to bring control information in the disk control field to the file control unit. Each cycle steal request modifies the disk file control register address plus one (see logic on Q2-2) to address each successive byte in the disk control field. Only information in the S and N bytes is used in seek control.

A cycle steal request is made by the file control unit until it is honored by the CPU. The CPU indicates that it is honoring the request by returning bus out lines 2 and 7 active at clock 8 time. This sets the condition seek cycle latch in the file control unit and prepares the logic in the file control unit to accept the information on the data bus out in the next cycle. Each cycle steal request honored advances the seek time counter plus one and keeps track of which cycle steal request the file control unit has made. The seek time counter gates the file control unit logic to direct the S and N byte information into the head trigger and difference counter logic.

The inhibit request latch is set after the fourth seek cycle steal request is made to halt any further cycle steal requests.

Fixed-removable disk selection gates the control logic in the 5444 drive to select either the upper or lower disk. For a start I/O instruction, the selection is indicated with a bus out 4 condition during an initial program load. The program load selector switch on the operator console determines the selection.

Sense signals for device status seek check (byte 0, bit 7), unsafe (byte 2, bit 0), and equipment check (byte 3, bit 0) are generated on this card. These signals are gated to the data bus in during a sense instruction.



GD301 thru GD304

*Interface line page 8-205

1 2 3

A

CARD G2

Card G2 is shown on 4 pages and contains seek control and 5444 drive head selection logic for disk drive 0. Drive 1 seek controls on card F2 are not shown, but card F2 has logic identical to that of card G2 except that the drive references are to drive 1. For some cards shown on other pages, references are made to drive 1 seek controls. These references are shown in parentheses and refer to card G2. (8-213) refers to drive 1.

Card G2 (and F2) can be one of two types, depending if the FCU is to attach standard or high speed drives.

Cards G2 (and F2) in FCUs to attach the high speed drives contain a go slow counter. The basic logic and operation, however, remain the same as the standard speed FCU. Because the logic was repackaged for high speed access, the second level diagrams reference two locations in the ALDs where the various logic can be found. References to high speed access (HSA) ALDs will have a (HSA) suffix.

The following logic is shown on card G2:

1. Difference counter
2. Seek time-out counter
3. Initial seek time
4. Head trigger
5. Forward-reverse
6. Recalibrate operation
7. Seek check
8. Go
9. Head settling latch
10. For FCUs with high speed access, the go slow counter.

The difference counter indicates the number of cylinders to move in a seek operation. This counter is used in conjunction with the head settle counter to develop the head settle time delay. During a seek operation, at seek time 4 when the N byte information is on the data bus out, the binary complement is set with the counter by (not) data bus out conditions. For example, N=7 would set the difference counter to a value of 248. Track crossing pulses from the drive advance the counter until it carries, which indicates that the desired count was reached. (The counter receives one advance pulse at the start of its operation so that the count is correct.) During head settle time, the counter is advanced with the head settle counter. (See card E2.)

B

The seek time-out counter is a two-position counter to aid in the 1 to 2 second time base for a seek check condition. (See card E2 and error conditions on card M2 for seek check conditions.)

Initial seek time indicates the start of a seek operation at start I/O instruction I-R cycle time and is reset at the end of seek 4 time, the last of the file control unit seek cycle steal requests.

The head trigger is set with bus out 0 during a seek operation when the seek counter is at 3. The S-byte information is on the data bus out at this time. In a recalibrate operation, the head trigger is set to 0. If the allow-head-switch latch is set, the head-enable latch prevents a head selection until index 2 time.

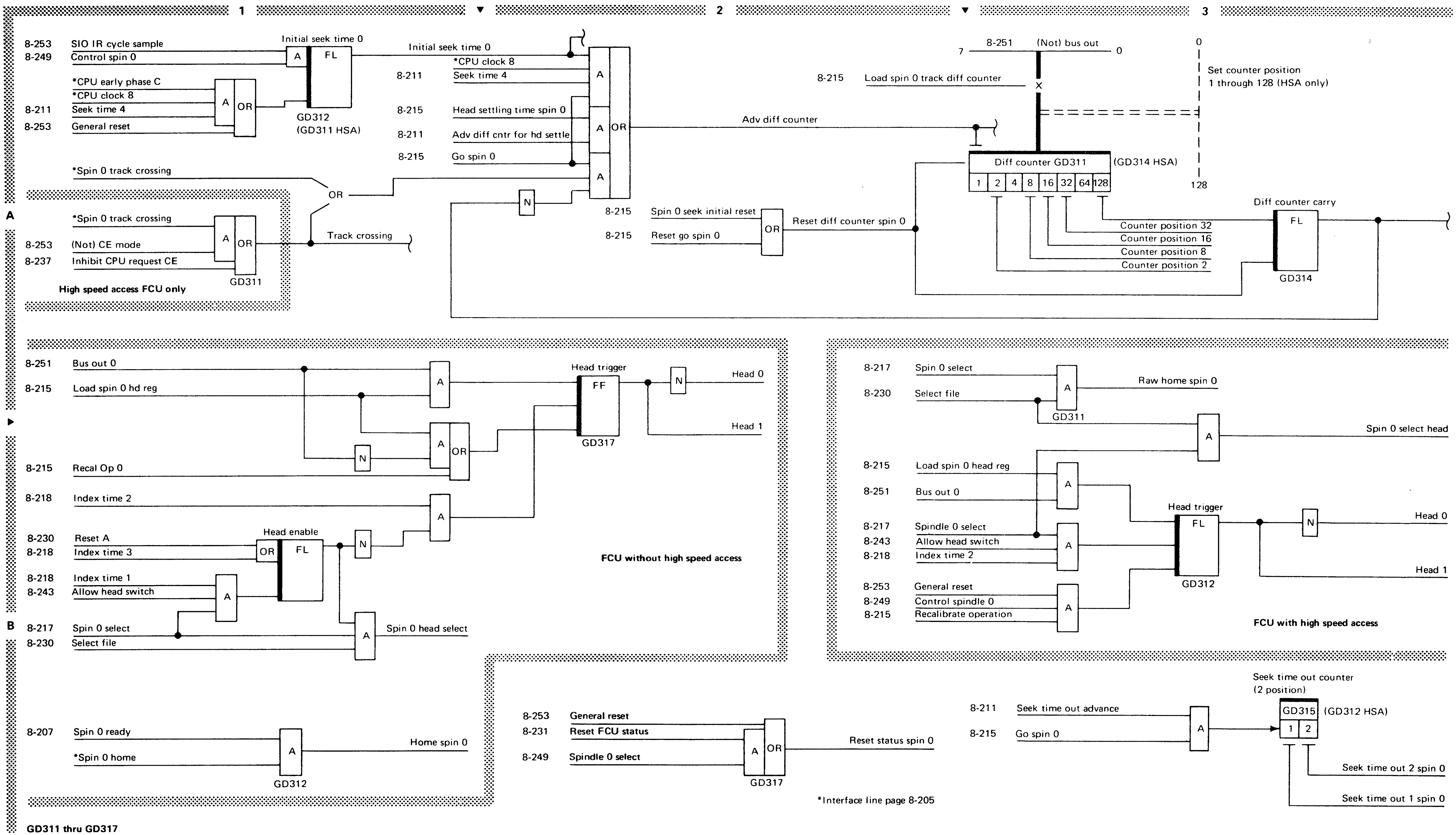
The forward-reverse latch determines in which direction the drive access mechanism will travel in a seek operation. The latch is set with a bus out 7 condition when the S-byte information is on the data bus out.

When the file control unit is to perform a seek-recalibrate operation, the recalibrate operation latch is set. A reverse seek instruction and a bus out with a value greater than 223 at seek 4 time (N byte) indicate that the latch is to be set.

Seek check is set when one of five error conditions is sensed during a seek operation. (See error conditions on card M2 for these error descriptions.)

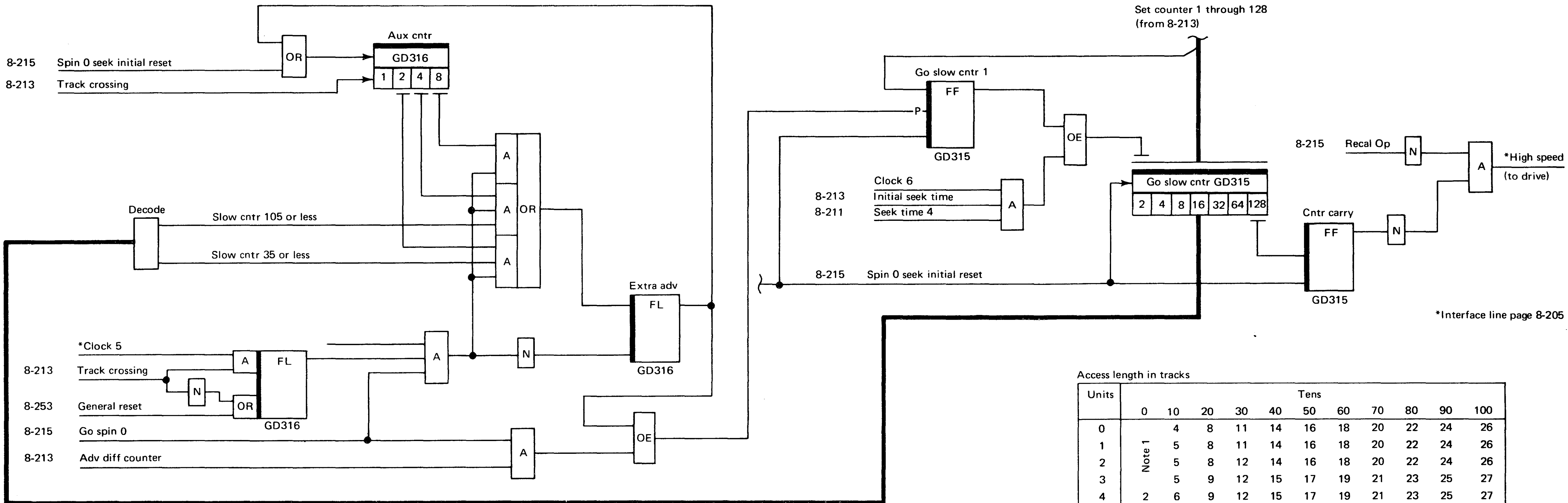
Go is the signal to start the mechanical motion in the drive for the seek operation. A signal to the drive to stop the access motion results when this latch is reset.

Setting the head settling latch starts the head settling time out, and gates the file control unit logic to generate the 27.6 to 28.3 ms time base for the delay.



*Interface line page 8-205

GD311 thru GD317



This logic is for FCU with high speed access only.

High Speed Access

The 5444 drive access operates at high speed under control of the high speed interface line. When the interface line is active, the drive will access at high speed, deactivating the line causes the drive to access at slow (normal) speed.

A go slow counter, located in the FCU, monitors the drive carriage relative to the desired track. Depending on the length of the seek, the FCU will deactivate the high speed interface line at various number of tracks before the end of the seek operation as shown in the chart.

The diagram on this page shows the high speed interface line control logic, and is the only additional circuitry added to the normal speed FCU.

Go Slow Counter

The go slow counter controls the high speed interface line. Note that the high speed interface line is active at the start of a seek operation and remains active until the go slow counter carries. The high speed interface line is not active during a seek recalibrate operation.

At the start of a seek operation, the go slow counter is set to the same value as the difference counter. Then before the access mechanism starts to move, the go slow counter is advanced by a count of three. (Two counts by direct input to the 2-bit trigger and one count by the 'adv. diff counter' signal as described on page 8-212.)

After the initial advance of three counts, the go slow counter is advanced by 'adv diff counter' signals and extra advance pulses as gated by the auxiliary counter.

Auxiliary Counter

This counter, and a decode network, develop the extra advance pulses to the go slow counter to achieve the deactivation of the high speed interface line as shown in the chart. The auxiliary counter is advanced by track crossing pulses received from the drive, and its count is reset with each extra advance pulse to the go slow counter.

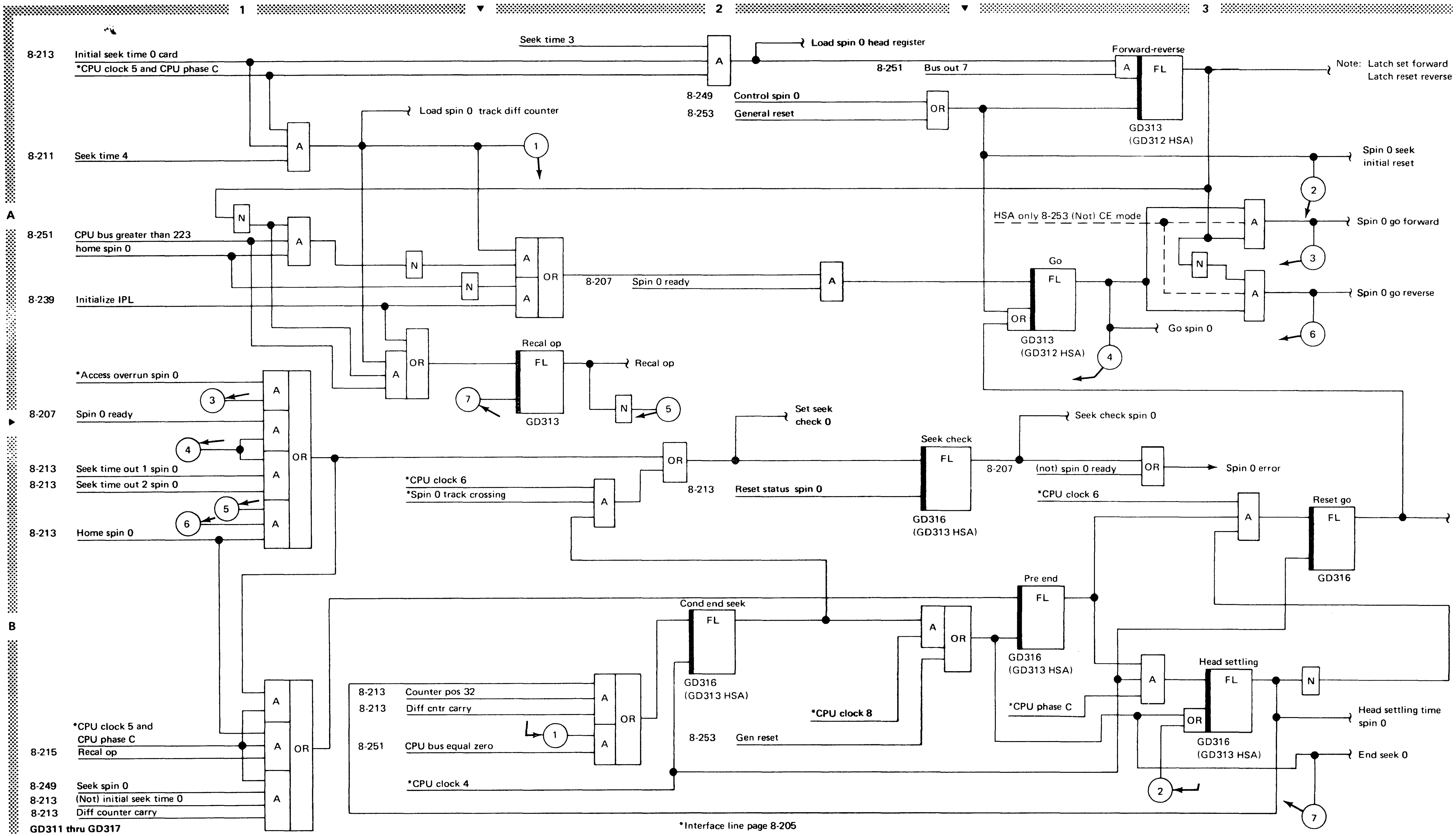
Access length in tracks

Units	Tens 0	10	20	30	40	50	60	70	80	90	100
0	Note 1	4	8	11	14	16	18	20	22	24	26
1	Note 1	5	8	11	14	16	18	20	22	24	26
2	Note 1	5	8	12	14	16	18	20	22	24	26
3	Note 1	5	9	12	15	17	19	21	23	25	27
4	2	6	9	12	15	17	19	21	23	25	27
5	3	6	9	13	15	17	19	21	23	25	27
6	3	6	10	13	15	17	19	21	23	25	27
7	3	7	10	13	15	17	19	21	23	25	27
8	4	7	10	14	16	18	20	22	24	26	28
9	4	7	11	14	16	18	20	22	24	26	28

Units	Tens 110	120	130	140	150	160	170	180	190	200
0	28	29	30	31	32	33	34	36	37	38
1	28	29	30	31	32	33	35	36	37	38
2	28	29	30	31	32	34	35	36	37	38
3	28	29	30	31	33	34	35	36	37	38
4	28	29	30	32	33	34	35	36	37	38
5	28	29	31	32	33	34	35	36	37	
6	28	30	31	32	33	34	35	36	37	
7	29	30	31	32	33	34	35	36	37	
8	29	30	31	32	33	34	35	36	38	
9	29	30	31	32	33	34	35	37	38	

Number of tracks, before the desired track, that the high speed interface line is deactivated.

Note 1. High speed is not active for seek lengths of 3 tracks or less.


1
2
3
A
B
8-213 Initial seek time 0 card
*CPU clock 5 and CPU phase C
Seek time 3
Load spin 0 head register
Forward-reverse
8-251 Bus out 7
Note: Latch set forward
Latch reset reverse
8-249 Control spin 0
8-253 General reset
GD313
(GD312 HSA)
Load spin 0 track diff counter
8-211 Seek time 4
Spin 0 seek
initial reset
HSA only 8-253 (Not) CE mode
Spin 0 go forward
8-251 CPU bus greater than 223
home spin 0
Go
8-207 Spin 0 ready
Spin 0 go reverse
8-239 Initialize IPL
Go spin 0
GD313
(GD312 HSA)
Recal op
Recal op
*Access overrun spin 0
GD313
8-207 Spin 0 ready
Set seek
check 0
Seek check spin 0
Seek check
8-207 (not) spin 0 ready
Spin 0 error
8-213 Seek time out 1 spin 0
8-213 Seek time out 2 spin 0
*CPU clock 6
*Spin 0 track crossing
8-213 Reset status spin 0
*CPU clock 6
Reset go
GD316
(GD313 HSA)
8-213 Home spin 0
GD316
Pre end
Cond end seek
Head settling
GD316
(GD313 HSA)
GD316
(GD313 HSA)
8-213 Counter pos 32
8-213 Diff cntr carry
*CPU clock 8
*CPU phase C
Head settling time
spin 0
*CPU clock 5 and
CPU phase C
8-215 Recal op
8-251 CPU bus equal zero
8-253 Gen reset
GD316
(GD313 HSA)
End seek 0
*CPU clock 4
8-249 Seek spin 0
8-213 (Not) initial seek time 0
8-213 Diff counter carry
GD311 thru GD317
*Interface line page 8-205

CARD J2

Card J2 is shown on three pages and contains the following logic:

1. Read gate
2. Clock gate
3. Index
   a. Index reset
   b. Index passed
4. Execute
5. End write identifier area operation
6. N carry latch
7. Write gate
8. Erase gate
9. Write gate equipment check
10. Write data to spindles 0 and 1
11. Set fixed-write data

Read gate conditions the read heads in the drive and the logic in the file control unit to read data from the disk.

Clock gate selects either the 3.177 MHz oscillator or the separated clock signals from the data separator to drive the file control unit clock.

Index logic processes the raw index pulse from the drives and synchronizes it with the file control unit clock and bit ring signals. Index reset and index passed indicate when an index has passed twice in an operation. They are used to set error status under some conditions; for example, no record found.

Execute is set as a result of a 'start op' pulse whenever index is not active. Execute is an indication to the file control unit to start an operation.

Activating an end write identifier area operation terminates a write identifier area operation.

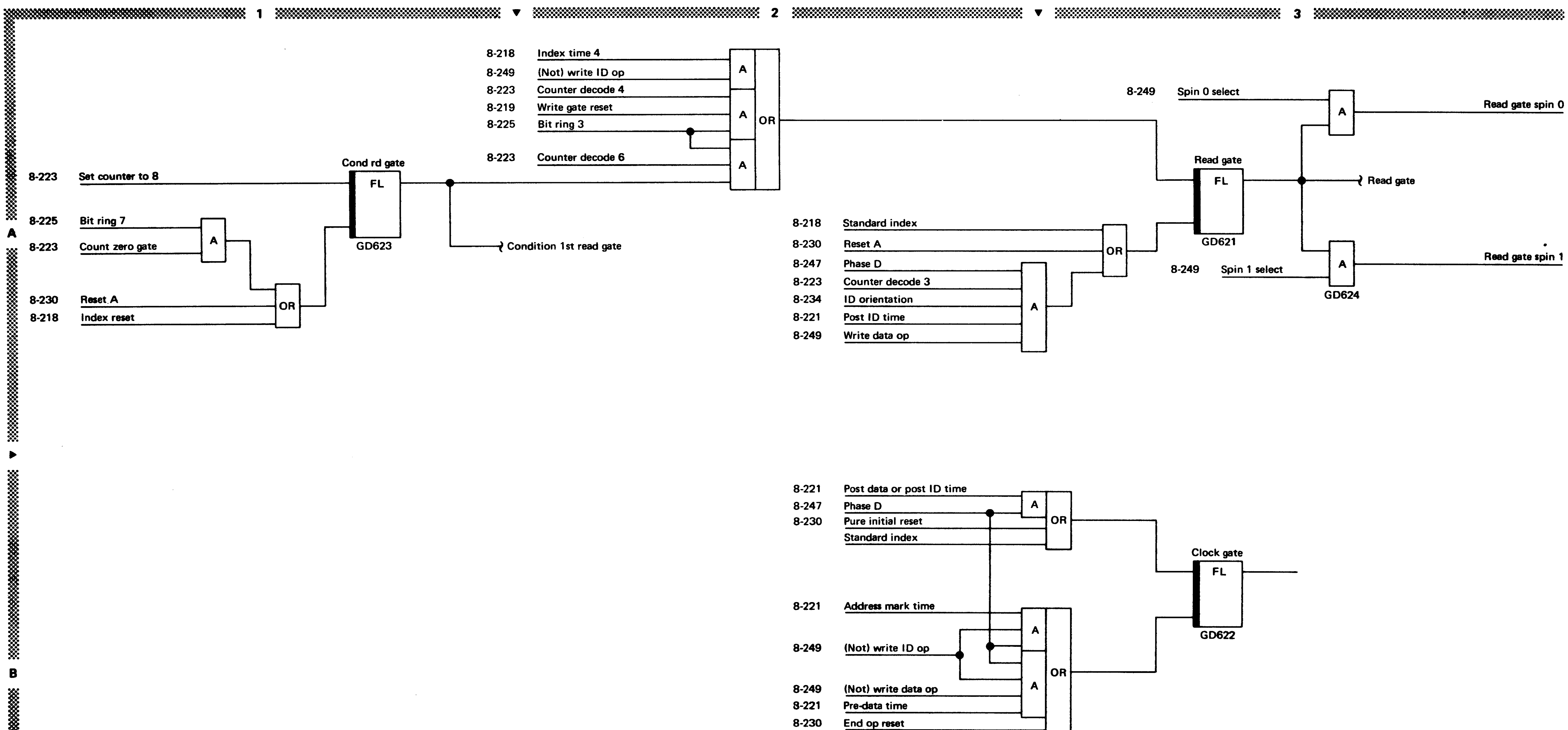
The N carry latch is set when the N field in the disk control field (in core storage) has decremented the number of sectors as specified at the start of an operation. This latch gates the reset logic on card M2-1 to end an operation in progress.

Write gate and erase gate condition the read-write heads in the drive to write information on the disk.

Write gate equipment check is an error indication and is active when write gate is active, index is sensed, and the file control unit is not in a write identifier area operation.

Write data to spindles 0 and 1 is the file control unit "outlet" for data to the drives. This is where data and the write clock signals are combined. Write FF conditions this logic to write all ones on the disk for sector gaps. Block clock is active only during a write identifier area operation and is responsible for the missing clock pulses in the address mark.

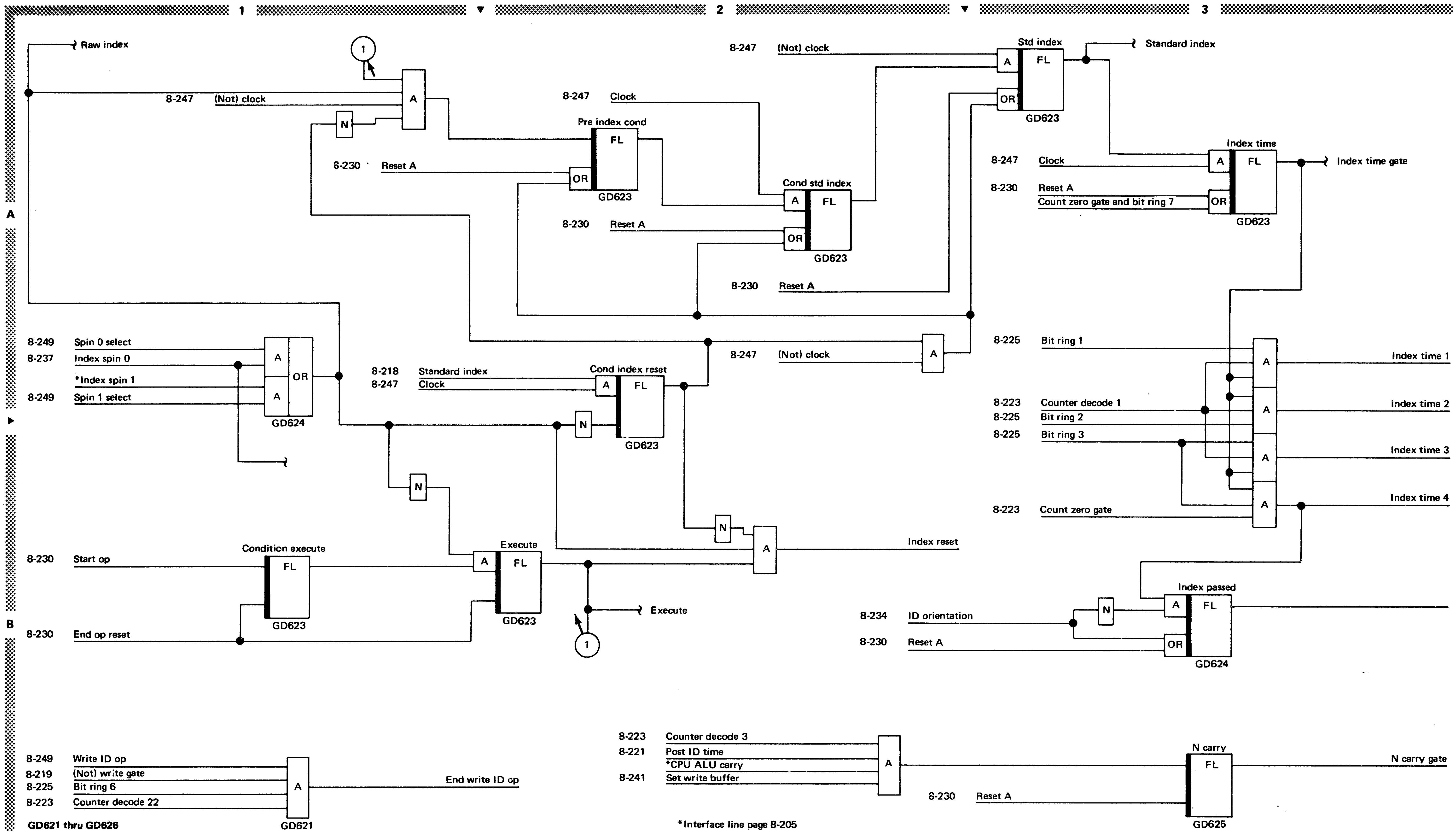
Set fixed-write data generates constants F2 and 0E, the address mark and sync byte characters. During a write operation, these characters are gated into the read buffer to be serialized and written on disk.



Note: The clock gate latch determines if the separated clock or the write oscillator drives the file control unit clock. If the clock gate latch is set, the clock is driven from the write oscillator, if reset, the clock drive is from seperated clock pulses

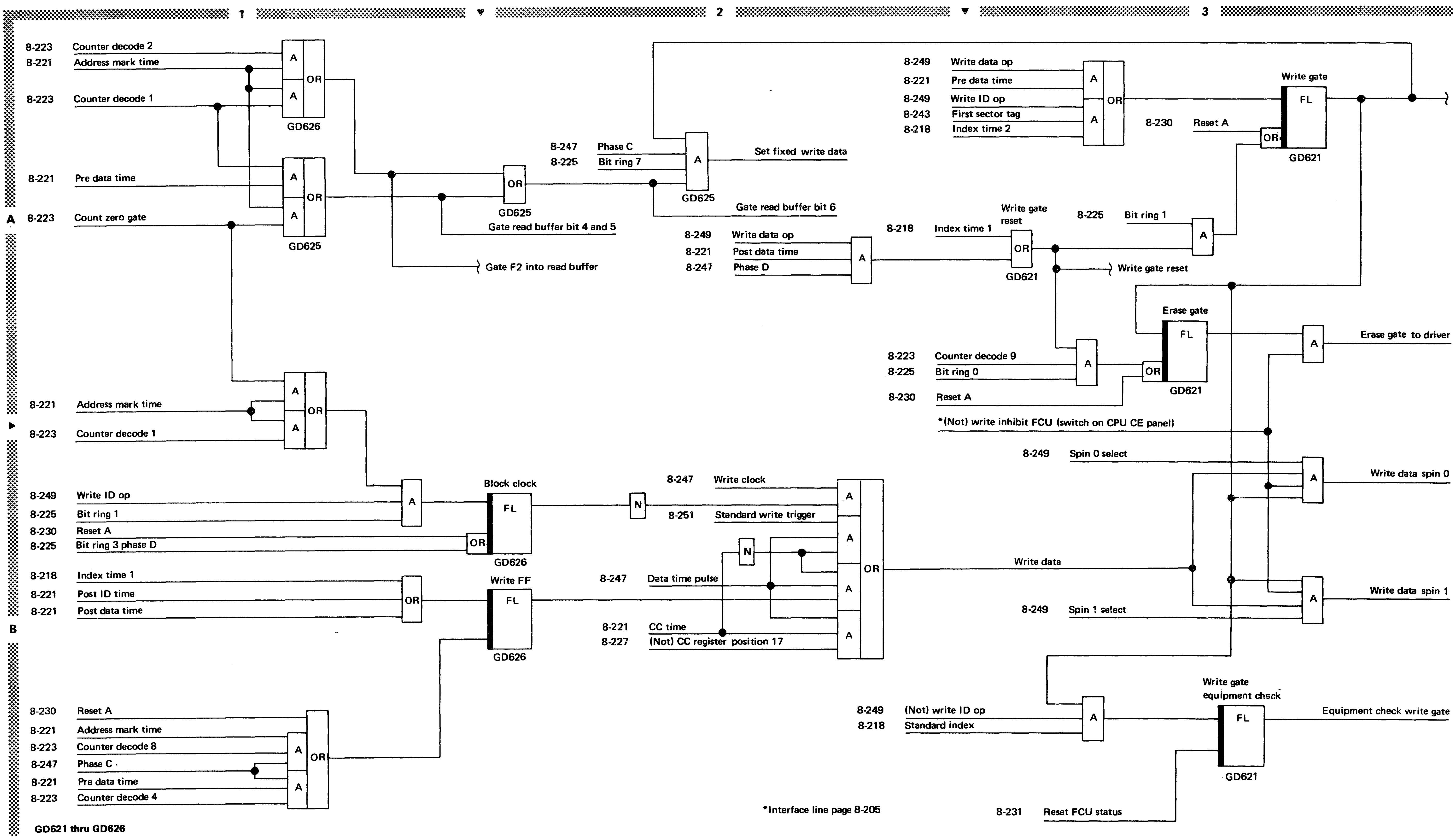
*Interface line page 8-205

GD621 thru GD626



GD621 thru GD626

*Interface line page 8-205



1
2
3
A
B
8-223 Counter decode 2
8-221 Address mark time
8-223 Counter decode 1
GD626
8-221 Pre data time
8-223 Count zero gate
GD625
8-247 Phase C
8-225 Bit ring 7
GD625
Set fixed write data
Gate read buffer bit 6
Gate read buffer bit 4 and 5
Gate F2 into read buffer
8-249 Write data op
8-221 Pre data time
8-249 Write ID op
8-243 First sector tag
8-218 Index time 2
Write gate
8-230 Reset A
GD621
8-249 Write data op
8-221 Post data time
8-247 Phase D
8-218 Index time 1
Write gate reset
8-225 Bit ring 1
GD621
Write gate reset
Erase gate
8-223 Counter decode 9
8-225 Bit ring 0
8-230 Reset A
GD621
Erase gate to driver
*(Not) write inhibit FCU (switch on CPU CE panel)
8-221 Address mark time
8-223 Counter decode 1
8-249 Spin 0 select
Write data spin 0
8-249 Write ID op
8-225 Bit ring 1
8-230 Reset A
8-225 Bit ring 3 phase D
Block clock
GD626
8-247 Write clock
8-251 Standard write trigger
8-218 Index time 1
8-221 Post ID time
8-221 Post data time
Write FF
GD626
8-247 Data time pulse
8-221 CC time
8-227 (Not) CC register position 17
Write data
Write data spin 1
8-249 Spin 1 select
8-230 Reset A
8-221 Address mark time
8-223 Counter decode 8
8-247 Phase C
8-221 Pre data time
8-223 Counter decode 4
8-249 (Not) write ID op
8-218 Standard index
Write gate equipment check
GD621
Equipment check write gate
*Interface line page 8-205
8-231 Reset FCU status
GD621 thru GD626

1

CARD K2

Card K2 is shown on two pages and contains the following logic:

1. Cycle control ring, page 8-221
2. Control counter, page 8-223

Cycle Control Ring (CCR)

The cycle control ring provides gating signals that correspond to the sector fields on disk. There are nine conditions or times in the cycle control ring cycle:

1. Address mark (AM)
2. Preidentifier–gap 2 (pre ID)
3. Identifier (ID)
4. Identifier cyclic code and bit count appendage characters (ID CC)
5. Postidentifier–part of gap 3 (post ID)
6. Predata–part of gap 3
7. Data
8. Data cyclic code and bit count appendage characters (data CC)
9. Postdata–gap 4

The cycle control ring starts in address mark time and will cycle through conditions 1 through 5 in the order listed above. The cycle control ring may continue with conditions 6 through 9 or return to address mark time after condition 5, depending on the file control unit operation.

2

Each sector starts with an address mark. If the cycle control ring is started (synchronized) when an address mark is detected (or is to be written), and advanced at the end of each field, the cycle control ring can signal what field is presently in operation and determine what will be the next field.

When searching for a specific address in a cylinder, the cycle control ring cycles address mark through post ID time. During this time the file control unit will compare the sector address on disk with the address in the disk control field (in core storage). If a correct compare was made (ID orientation), the cycle control ring may end the operation or continue on with predata through postdata time. If a correct compare was not made, the cycle control ring returns to address mark time and compares the next sector address with the disk control field. The functional objective of the file control unit operation (op-code) determines how the cycle control ring cycles. The end of sector fields is indicated by:

1. 'Address mark' or 'sync byte detect' ANDed with 'clock'.
2. 'CCR advance gate' ANDed with 'clock'.

'CCR advance gate' is set when' preadvance gate', 'bit ring 7 time', 'phase D', and 'count zero gate' are active. 'Preadvance gate' is set at the beginning of an operation when the control counter decode is 3 and at bit ring 1 time. The 'preadvance' latch remains set until the end of an operation.

3

Gate logic determines if the cycle control ring is to continue into predata time after post ID time or return to address mark time after postdata, and to set address mark time at the start of an operation. These gates are:

1. 'Post ID time', '(not) write ID operation', '(not) IPL operation', and '(not) ID orientation'
2. 'Post data time' and '(not) N carry gate'
3. 'Condition first AM'

The chart on this page shows the cycle control ring cycles and brief descriptions of the operations performed in each for read data or scan, write data, and write identifier instructions.

The control counter is described briefly on page 8-222.

A

B

	AM Time		Pre ID		ID		ID CC		Post ID		Pre Data		Data		Data CC		Post Data
Read or scan Ops	FCU searches for zeros detect and then two bytes of 'F2' with clock bits missing (address marks).	2	Request a cycle steal for the 'F' byte from the disk control field (DCF).	1	Continue to cycle steal C and S information out of the disk control field (DCF). Compare DCF FCS with FCS read from disk ID field. Regenerate CC and BCA characters.	3	Compare regenerated CC and BCA characters with those written on disk.	3	Activate ID orientation if ID field and CC and BCA characters compare correctly. Subtract 3 from DFCR address. Set 'N carry latch' if N field (in DCF) equal 'FF'.	3	FCU sets up to read 256 bytes of data.	1	Read 256 data bytes. Cycle steal to transfer data bytes to CPU. Regenerate CC and BCA characters.	3	Compare regenerated data, CC and BCA characters with those recorded on disk.	3	If multi-sector operation, prepare to return to AM time. If last sector, end operation after post data time.
Write Data Op	Same as read data operation.	2	Same as read data operation.	1	Same as read data operation.	3	Same as read data operation.	3	Same as read data operation.	3	Write gate active. Write 4 bytes of ones, 4 bytes of zeros, and 1 sync byte 0E. Cycle steal first data byte from data field.	3	Write 256 data bytes. Cycle steal each character from the data field. Generate CC and BCA characters.	3	Write data, CC, and BCA characters on disk.	3	If multi-sector operation, prepare to go back into AM time. If last sector of operation, end cycle after post data.
Write ID Op	Write 13 bytes of ones, 7 bytes of zeros and 2 bytes of 'F2' with missing clock bits (address marks).	3	Write sync byte '0E' cycle steal 'F' byte from DCF. (gap 2)	3	Cycle steal C and S information from disk control field and write the bytes on disk. Generate CC and BCA characters.	3	Write CC and BCA characters on disk that were generated from ID data.	3	Start writing 10 bytes of ones. (gap 3)	3	Finish writing the 10 bytes of ones. Write 4 bytes of zeros and one sync byte 0E. Cycle steal first data byte from data field (gap 3).	3	Write the same data character 256 times. Generate CC and BCA characters cycle steal each data byte from the data field.	3	Write CC and BCA characters on disk generated from data bytes.	3	Write 15 bytes of ones. If last sector, write ones until index (gap 4 and gap 5 respectively).

Note: The number in this column indicates the condition that advances the CCR into the next time. These conditions are:

1. 'Sync byte (0E) detect' ANDed with 'clock'.
2. 'Address mark detect' ANDed with 'clock'.
3. 'Counter advance gate' ANDed with 'clock'.

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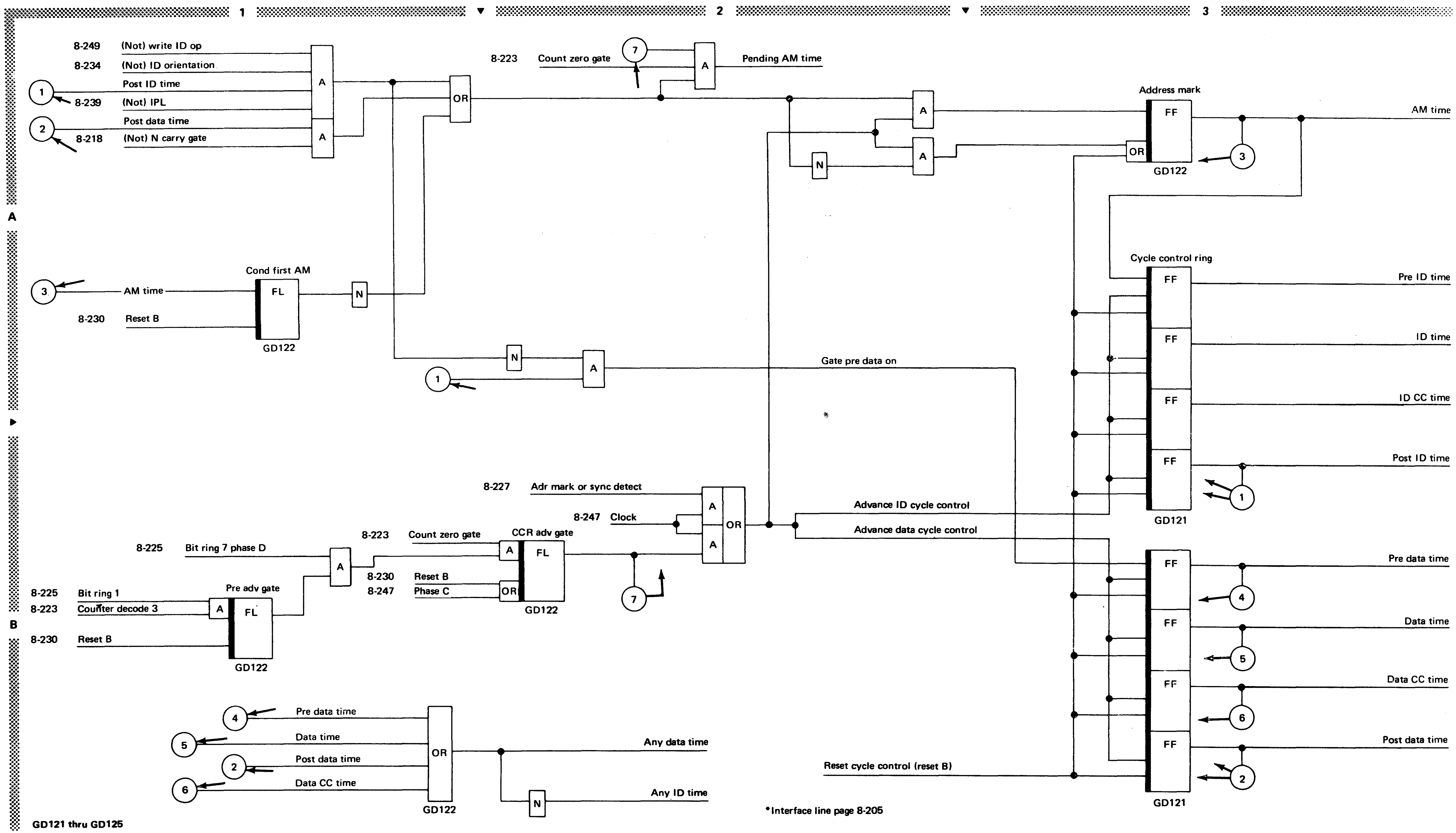

1
2
3
A
B
8-249 (Not) write ID op
8-234 (Not) ID orientation
Post ID time
8-239 (Not) IPL
Post data time
8-218 (Not) N carry gate
A
A
OR
8-223 Count zero gate
7
A
Pending AM time
Address mark
FF
OR
GD122
AM time
N
AM time
Cond first AM
FL
8-230 Reset B
GD122
Cycle control ring
FF
Pre ID time
FF
ID time
Gate pre data on
FF
ID CC time
FF
Post ID time
GD121
8-227 Adr mark or sync detect
8-247 Clock
Advance ID cycle control
Advance data cycle control
8-225 Bit ring 7 phase D
8-223 Count zero gate
CCR adv gate
FL
8-230 Reset B
8-247 Phase C
GD122
8-225 Bit ring 1
8-223 Counter decode 3
Pre adv gate
FL
8-230 Reset B
GD122
FF
Pre data time
FF
Data time
FF
Data CC time
FF
Post data time
GD121
Pre data time
Data time
Post data time
Data CC time
OR
GD122
Any data time
Any ID time
Reset cycle control (reset B)
*Interface line page 8-205
GD121 thru GD125

Control Counter

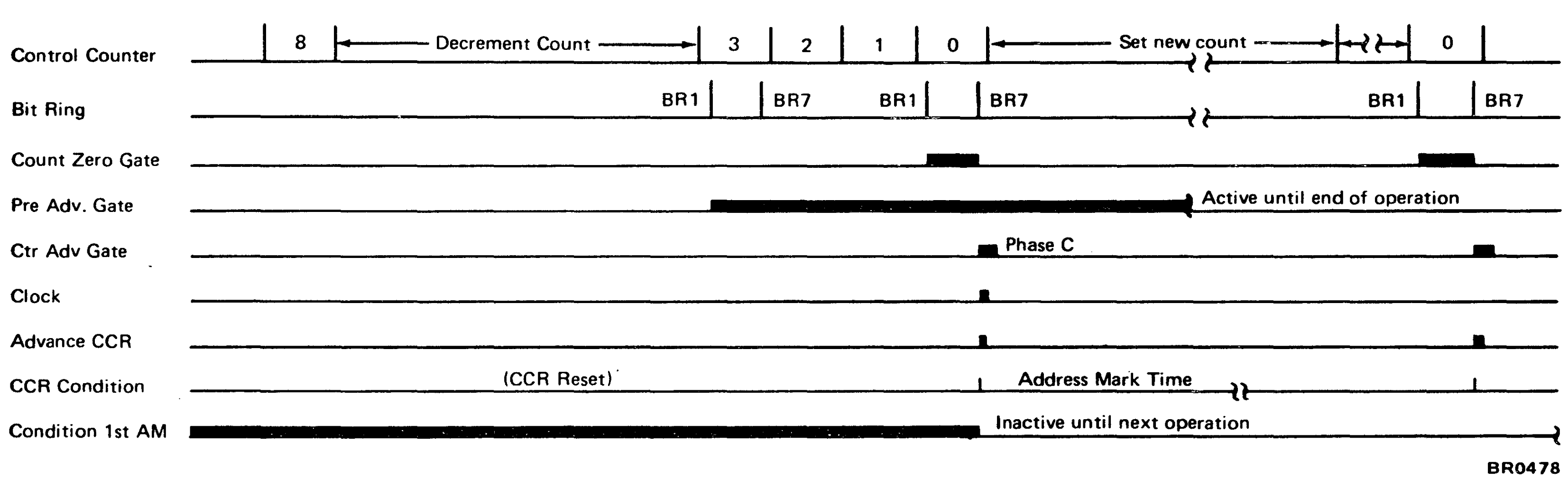
Individual field operations within the file control unit are definite in length. For example, the identifier area field is always six bytes in length. The control counter controls file control unit circuits within a field and signals the ends of fields. This counter can be set to predetermined values, then changed by one as each byte is processed. When the counter reaches zero an indication is given to the file control unit.

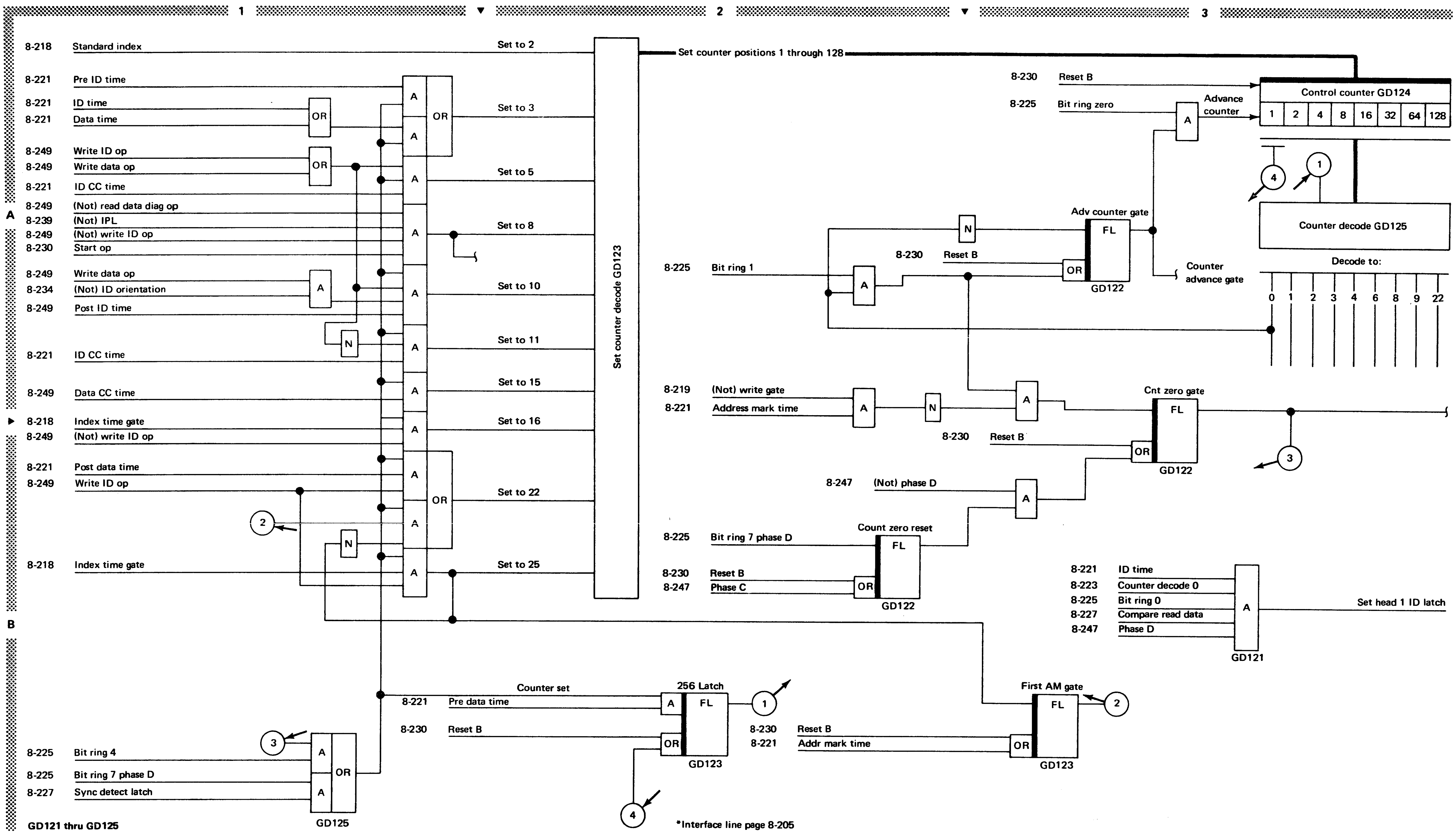
The control counter is an eight-position binary counter which increases in value with each advance pulse. Its maximum value (all positions on) is 255; 256 is considered zero (all positions off). A count of ten requires the counter to be preset to 246.

Predetermined values are set into the counter with decode logic which considers op-code commands, the field within the sector format that is to be operated on (zone), index pulse, and counter set. Zone lines and/or op-code lines select the circuit block that corresponds to the desired counter value. The 'counter-set' line activates the gate logic and decodes the selected block to turn on the necessary counter positions to produce the desired count. Bit ring 0 is ANDed with the advance-counter gate to provide the counter advance.

Resetting the bit ring leaves bit ring position 7 active. When 'bit ring inhibit' goes inactive, the next clock pulse steps the bit ring to 0. This action produces a redundant control-counter advance. The value preset into the counter is one more than the actual count needed to allow for this redundant advance.

Counter position outputs are fed into a decode network which interprets the counter condition into decimal values. File control unit logic uses these indications to prepare for the next sequential operation or to signal the end of an operation.





DISK ATTACHMENT–Functional Units
Card K2 (Part 4 of 4)

CARD L2

Card L2 is shown on two pages and contains the following logic:

1. Address mark detect
2. Bit ring
3. Cyclic code register
4. Standard read data and compare read data triggers.

Address Mark Detection

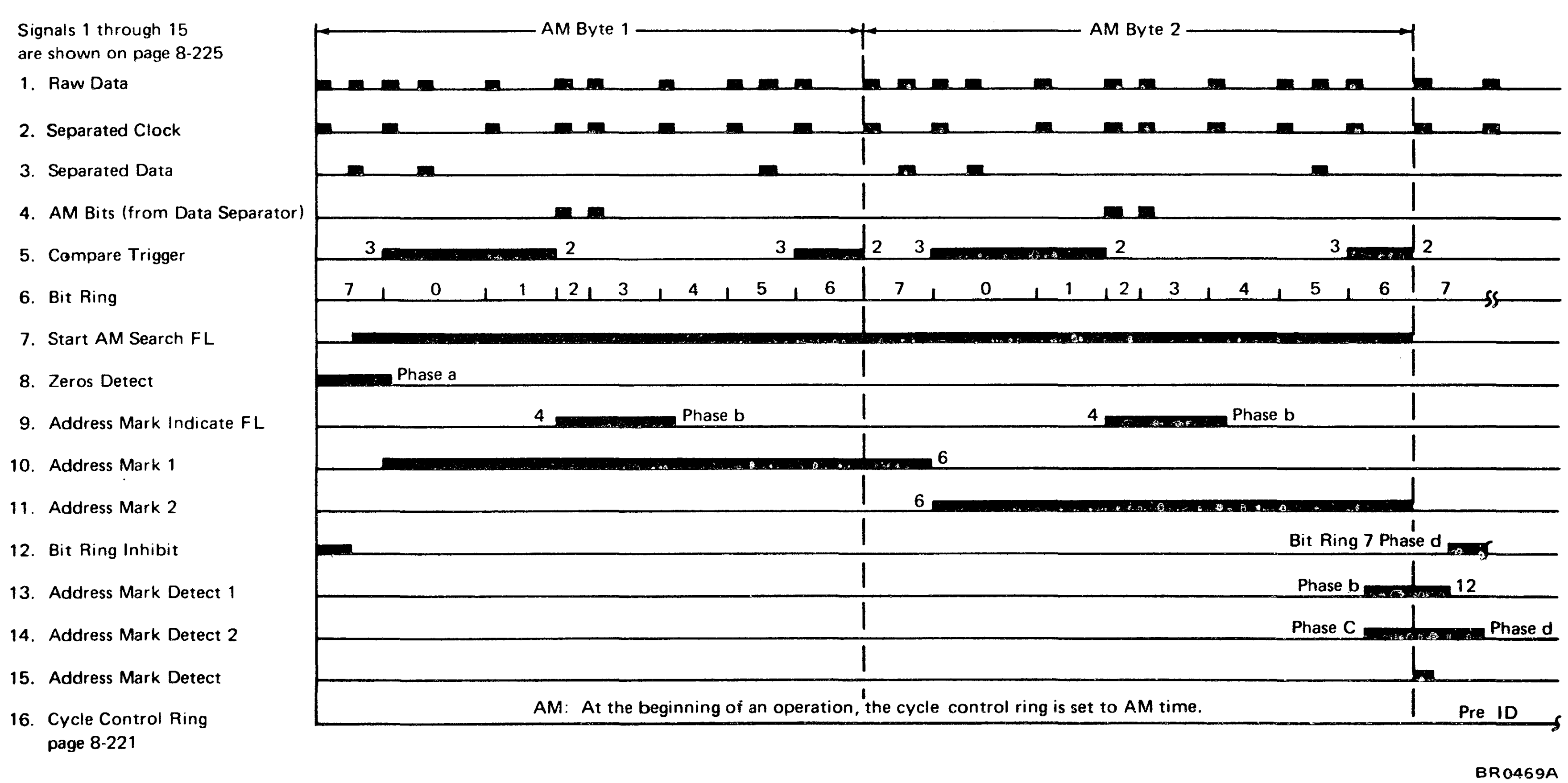
The address mark detect logic (page 8-225) processes the address mark bits from the data separator and checks for the following conditions:

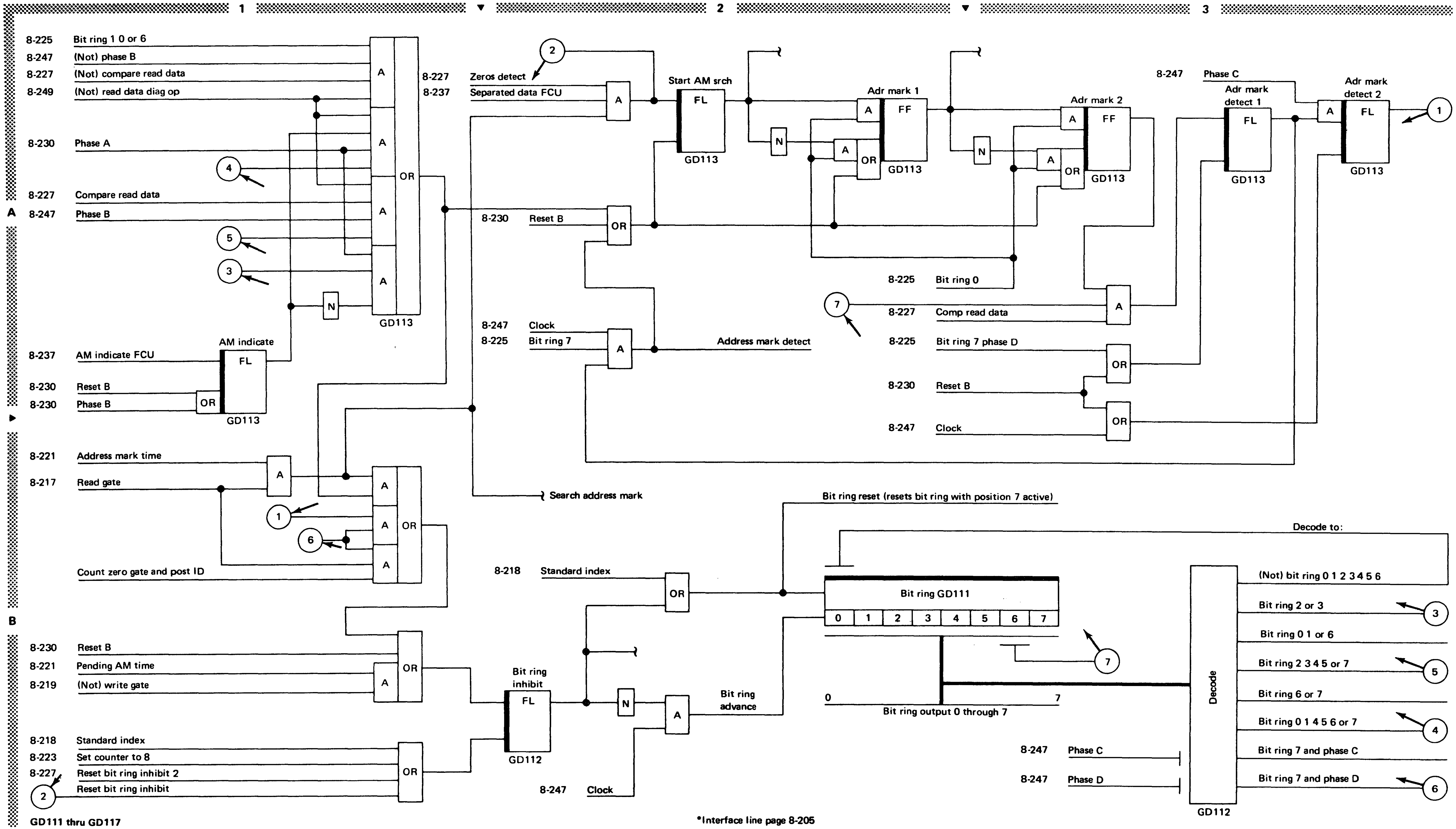
1. That there was compare data during bit ring 0, 1, and 6 time. If not, there may have been missing bits in the address mark.
2. That address mark indicate was not active during bit ring 0, 1, 4, 5, 6, or 7 time. If address mark indicate is detected during this time, a false address mark detect or an address mark was detected at the incorrect time.
3. That compare read was not up at bit ring 2, 3, 4, 5, or 7 time. This indicates that bits were read when they should not have been.
4. That address mark indicate was active at bit ring 2 and 3 time.

All operations, except read data diagnostic, check for all four of the above requirements for address mark detection. Read data diagnostic reduces the requirements by eliminating check conditions 1, 2, and 3. If any of the check conditions are detected during an operation (check 4 for read data diagnostic), start address mark search FL is reset to prevent generation of the address mark detect signal. The address mark detect signal advances the cycle control ring from address mark time into pre ID time.

Bit Ring

The bit ring (page 8-225) provides the file control unit with timing for the sub byte level. Each of its eight outputs is active for the length of time of one bit cell and is named for the bits within a byte, zero through seven. The bit ring is advanced with clock pulses which are gated with the 'bit ring inhibit' line. 'Bit ring inhibit' is active when the bit ring must be held from stepping to synchronize with a data byte or at the start of an operation. Bit ring outputs are used throughout the file control unit to gate logic at the sub byte level; for example, to locate the flag bits 6 and 7 within the F byte. When reset, the 'bit ring 7' output is active and remains in this state until the 'bit ring inhibit' line is inactive.





1
2
3
A
B
8-225 Bit ring 1 0 or 6
8-247 (Not) phase B
8-227 (Not) compare read data
8-249 (Not) read data diag op
8-230 Phase A
8-227 Compare read data
8-247 Phase B
GD113
8-227
8-237
AM indicate
8-237 AM indicate FCU
8-230 Reset B
8-230 Phase B
GD113
8-221 Address mark time
8-217 Read gate
Count zero gate and post ID
8-230 Reset B
8-221 Pending AM time
8-219 (Not) write gate
8-218 Standard index
8-223 Set counter to 8
8-227 Reset bit ring inhibit 2
Reset bit ring inhibit
GD111 thru GD117
Zeros detect
Separated data FCU
Start AM srch
GD113
8-230 Reset B
8-247 Clock
8-225 Bit ring 7
Address mark detect
Search address mark
Adr mark 1
GD113
Adr mark 2
GD113
8-225 Bit ring 0
8-227 Comp read data
8-225 Bit ring 7 phase D
8-230 Reset B
8-247 Clock
8-247 Phase C
Adr mark detect 1
GD113
Adr mark detect 2
GD113
Bit ring reset (resets bit ring with position 7 active)
Decode to:
8-218 Standard index
Bit ring GD111
0 1 2 3 4 5 6 7
Bit ring inhibit
GD112
Bit ring advance
8-247 Clock
Bit ring output 0 through 7
8-247 Phase C
8-247 Phase D
Decode
GD112
(Not) bit ring 0 1 2 3 4 5 6
Bit ring 2 or 3
Bit ring 0 1 or 6
Bit ring 2 3 4 5 or 7
Bit ring 6 or 7
Bit ring 0 1 4 5 6 or 7
Bit ring 7 and phase C
Bit ring 7 and phase D
*Interface line page 8-205

Cyclic Code Register (CC Register)

The cyclic code register shown on page 8-227:

1. Generates the cyclic code characters
2. Deserializes the cyclic code character and the bit count appendage byte to be written on disk
3. Detects the sync byte 0E recorded in the field gaps ('sync byte' detect, used for controlling the cycle control ring)
4. Detects zeros recorded in the sector field gaps ('zeros detect', used in address mark detection)

Signals from the op-code register and cycle control ring determine which function the cyclic code register will perform. Input to the cyclic code register can be from:

1. Position 128 of the read buffer on a write operation
2. The 'standard read' trigger on a read operation
3. The bit count appendage register. The eight bits of the bit count appendage register transfer in parallel into positions 9 through 16 of the cyclic code register

Cyclic code characters are generated from data bits during read data, write data, write identifier area, or verify commands. Data bits enter position one of the cyclic code register and are shifted toward position sixteen at the rise of phase A time. The first two data bytes enter the cyclic code register unchanged. The first bit of the third byte and each successive bit is exclusive ORed (OE) with the output from position sixteen before entering position one. Position one will assume the result of the OE. Cyclic code generation ends with the last data bit for the data field processed.

At cyclic check time, the contents of the cyclic code register are shifted out bit by bit into position seventeen. The output of position seventeen is combined with clock pulses, gated to the selected drive, and recorded on the disk. Active output of position seventeen is the (not) condition (a one bit is written on disk as a zero).

After writing the cyclic code characters, positions 9 through 16 of the cyclic code register are reset and the contents of the bit count appendage register are transferred into these positions. The cyclic code register then continues its shift operation to write the bit count appendage character in the same manner as the cyclic code characters are written.

Cyclic Code Register Check

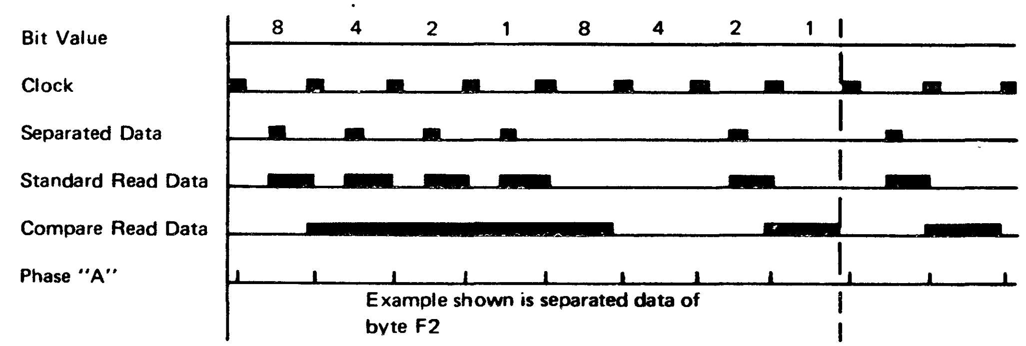
The parity of the generated check character in the cyclic code register is checked against two other flip-flops which indicate the parity of the byte transferred into the read buffer. The following table shows the correct (no error) conditions of the three flip-flops. If other than these conditions occur, a cyclic code check is indicated.

'FF' Name	O = Odd E = Even			
CC Odd-Even	E	E	O	O
Odd Count P Xfer	E	O	E	O
Odd Byte Xfer	E	O	O	E

BR0481

Standard Read Data Trigger and Compare Read Data Trigger

Separated data pulses are processed by the file control unit standard read and compare read triggers (page 8-227). As a result, the compare read data signal is one bit cell in length and one bit cell later in relation to when the data bit was read.



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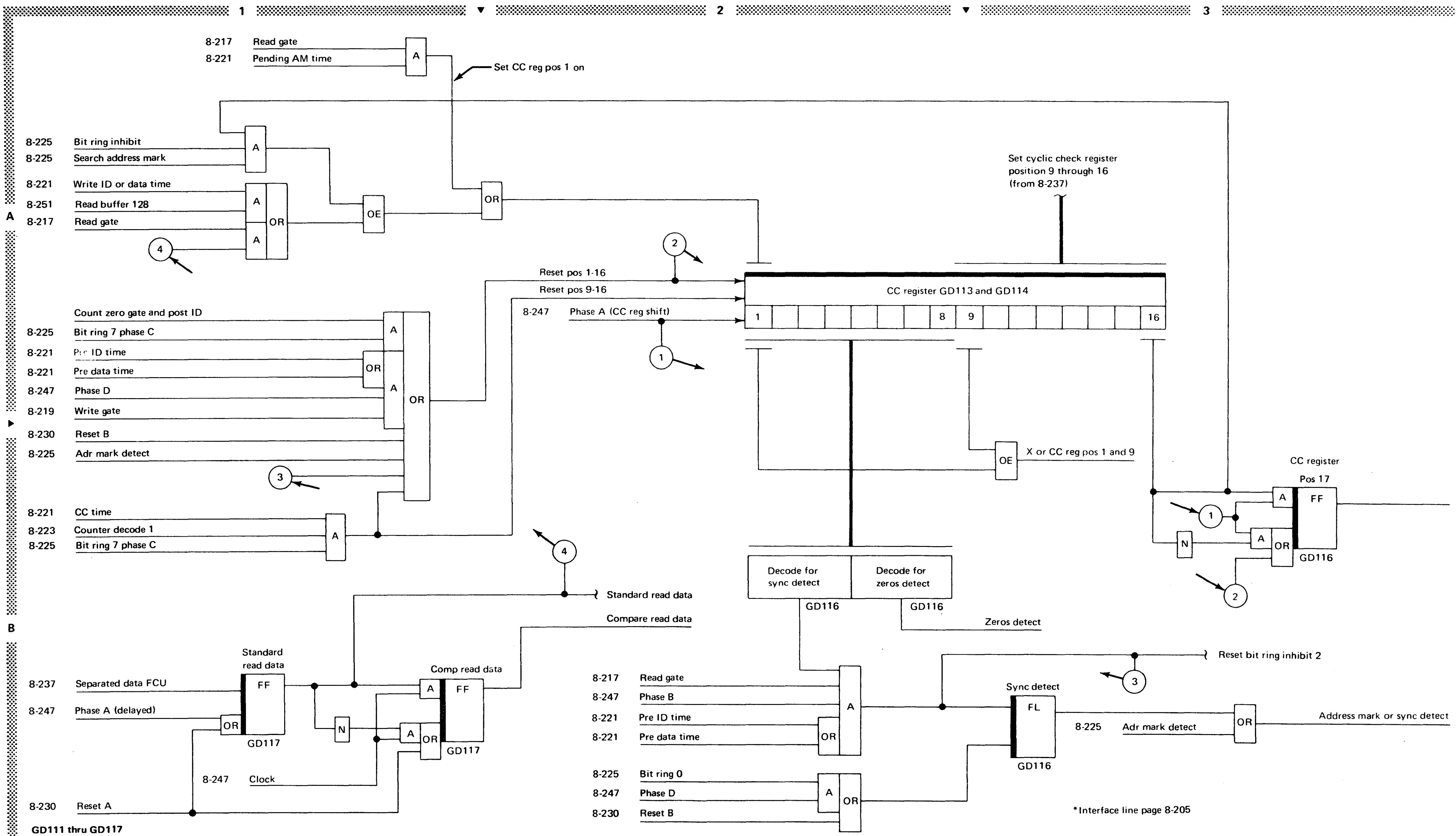

1
2
3
A
B
8-217 Read gate
8-221 Pending AM time
Set CC reg pos 1 on
8-225 Bit ring inhibit
8-225 Search address mark
8-221 Write ID or data time
8-251 Read buffer 128
8-217 Read gate
Set cyclic check register position 9 through 16 (from 8-237)
Reset pos 1-16
Reset pos 9-16
8-247 Phase A (CC reg shift)
CC register GD113 and GD114
Count zero gate and post ID
8-225 Bit ring 7 phase C
8-221 Pre ID time
8-221 Pre data time
8-247 Phase D
8-219 Write gate
8-230 Reset B
8-225 Adr mark detect
X or CC reg pos 1 and 9
CC register
Pos 17
GD116
8-221 CC time
8-223 Counter decode 1
8-225 Bit ring 7 phase C
Decode for sync detect
Decode for zeros detect
GD116
GD116
Standard read data
Compare read data
Zeros detect
Standard read data
8-237 Separated data FCU
8-247 Phase A (delayed)
GD117
Comp read data
GD117
8-247 Clock
8-230 Reset A
GD111 thru GD117
8-217 Read gate
8-247 Phase B
8-221 Pre ID time
8-221 Pre data time
8-225 Bit ring 0
8-247 Phase D
8-230 Reset B
Reset bit ring inhibit 2
Sync detect
GD116
8-225 Adr mark detect
Address mark or sync detect
*Interface line page 8-205

1 2 3

CARD M2

Card M2 is shown on pages 8-230 and 8-231 and contains the following logic:

1. Resets
2. Error conditions
3. Signals for status information

Resets

The reset logic is shown on page 8-230.

Resets are performed to set the file control unit into the condition needed to start an operation or to stop an operation in progress. In the case of some error conditions, a reset is performed to halt the operation.

'Reset A', 'reset B', and 'pure initial reset' are active at the beginning of an operation at clock 0 time. The drive selected by the logic on page 8-249 is also enabled at this time. The 'start op' pulse at clock 4 time starts the operation set up in the operation resister.

The other inputs into the large OR circuit are the normal ending signals for an operation and the error reset conditions.

Error Conditions

The simplified reset logic figure, page 8-229, shows the error inputs into the reset logic. The conditions that cause the error signals are described below.

Seek Check

Seek checks indicate an abnormal condition during a seek operation. Conditions that set seek check are:

1. No seek ends 1 to 2 seconds after 'go' is active.
2. 'Go Forward' is active and access overrun is indicated. 'Access overrun' occurs when the access mechanism is at its inner stop.
3. 'Go Reverse' is active, 'cylinder zero' is indicated, and file control unit is not in a recalibrate operation.
4. A track crossing pulse is sensed after head settling time.
5. 'Go' is active and drive becomes (not) ready during a seek operation.

Virgin Track

This error indicates that an 'index' pulse passed twice while looking for an address mark and none was found.

First Record Not Found

This error indicates that 'ID orientation' was not established after an address mark was located. 'Index' passed twice after locating the address mark.

Set End of Cylinder

Indicates one of two conditions:

1. That 'index' was sensed while reading from head 1
2. That 'index' was sensed while reading an alternate track from head 0 which was originally located on the lower surface of the disk (head 1)

Overrun

Indicates that a data cycle steal request from the file control unit was not honored by the CPU before the next file control unit 'set write buffer' time or 'gate data to DBI' time.

No Record Found

Indicates a 'first record not found' or virgin track error, or that a successive identifier area field did not compare successfully after 'ID orientation' was established.

Equipment Check Write Gate

Indicates that 'write gate' was active at 'standard index' time and that the file control unit was not in a 'write ID' operation.

Check Counter Error

Indicates that 'check counter' register positions 8 through 128 were not reset at 'index 2' time, or that the check counter register did not advance to a count of 192 from index 4 time until the control counter decoded to 1. Both of these conditions are checked only during a write operation.

Cyclic Check Register Check

Indicates that a cyclic code check character was not generated with parity as predicted by the 'odd count parity transferred' and 'odd byte transferred' latches.

Parallel Parity Check

Indicates that the parity of the byte entering the read buffer was not the same as when that byte entered the write buffer from the bus-out latches.

Serdes Check

Indicates that the parity of the serialized byte shifted out of the read buffer was not the same as that byte entering the read buffer.

Missing Address Mark

Indicates that a virgin track error was found, or that the units position of the sector count was not odd-or-even different from the last sector read in a multisector read or write operation. This condition can also mean that the units position of the sector address was not even after a head switch during index time.

Track Condition Check

This error indicates that bits 6 and 7 of the flag byte in the disk control field were not the same as bits 6 and 7 of the flag byte read from disk.

Data Check

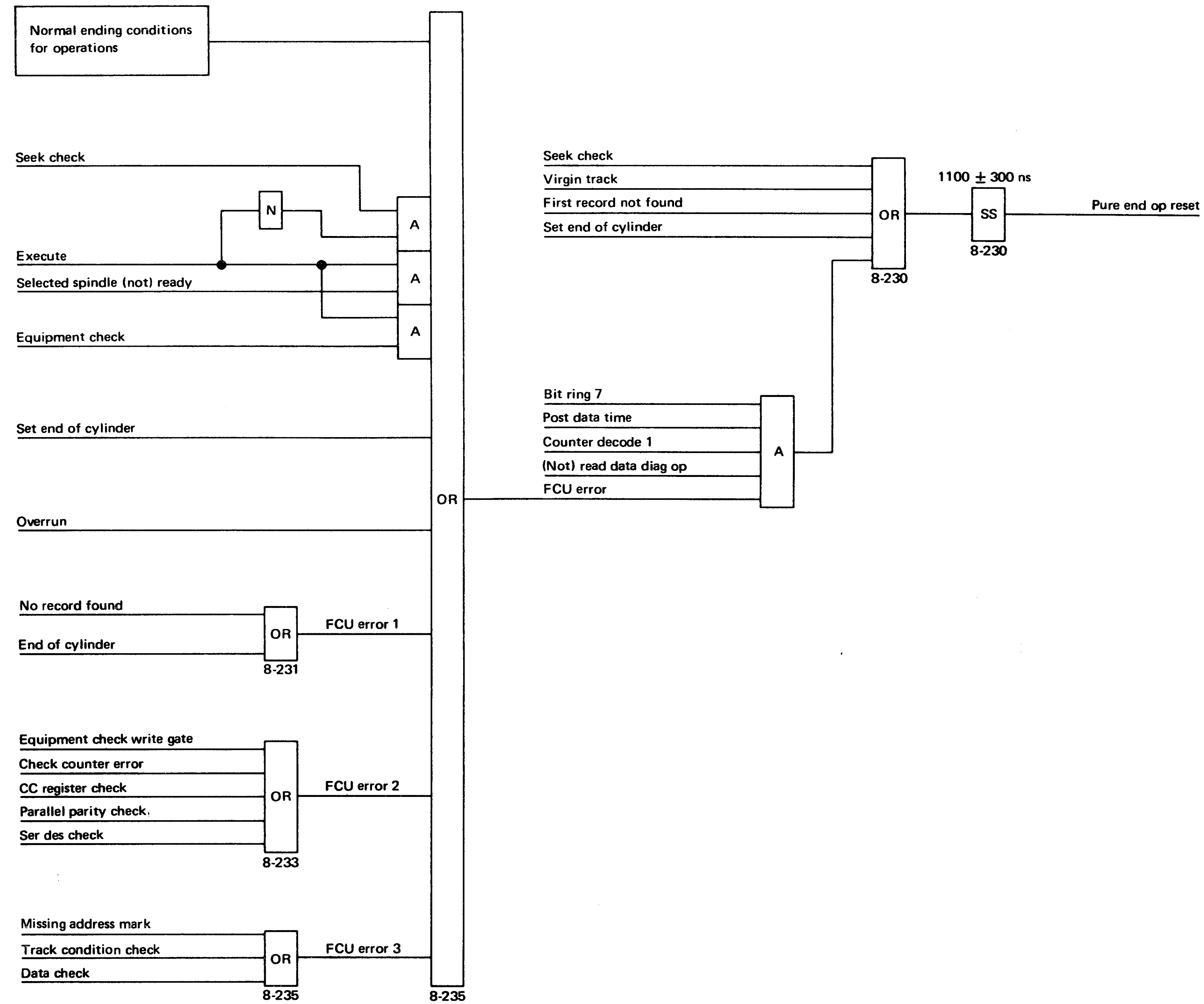
This error indicates that the cyclic code or bit count appendage check characters read from disk during an identifier area compare or read data operation were not the same as the cyclic check and bit count appendage regenerated during the read operation.

Equipment Check

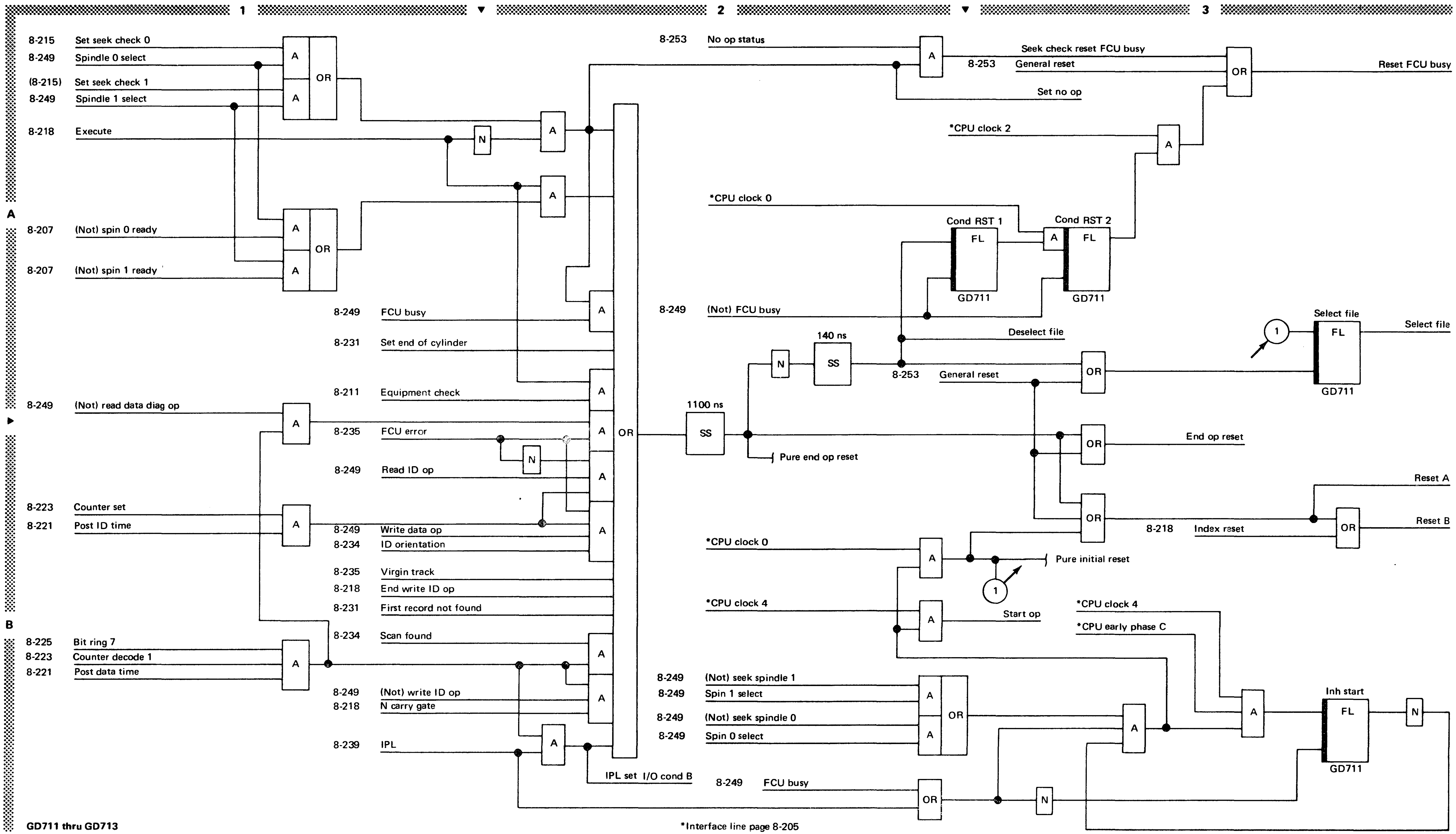
This error indicates any of the file control unit error 2 conditions plus spindle unsafe conditions.

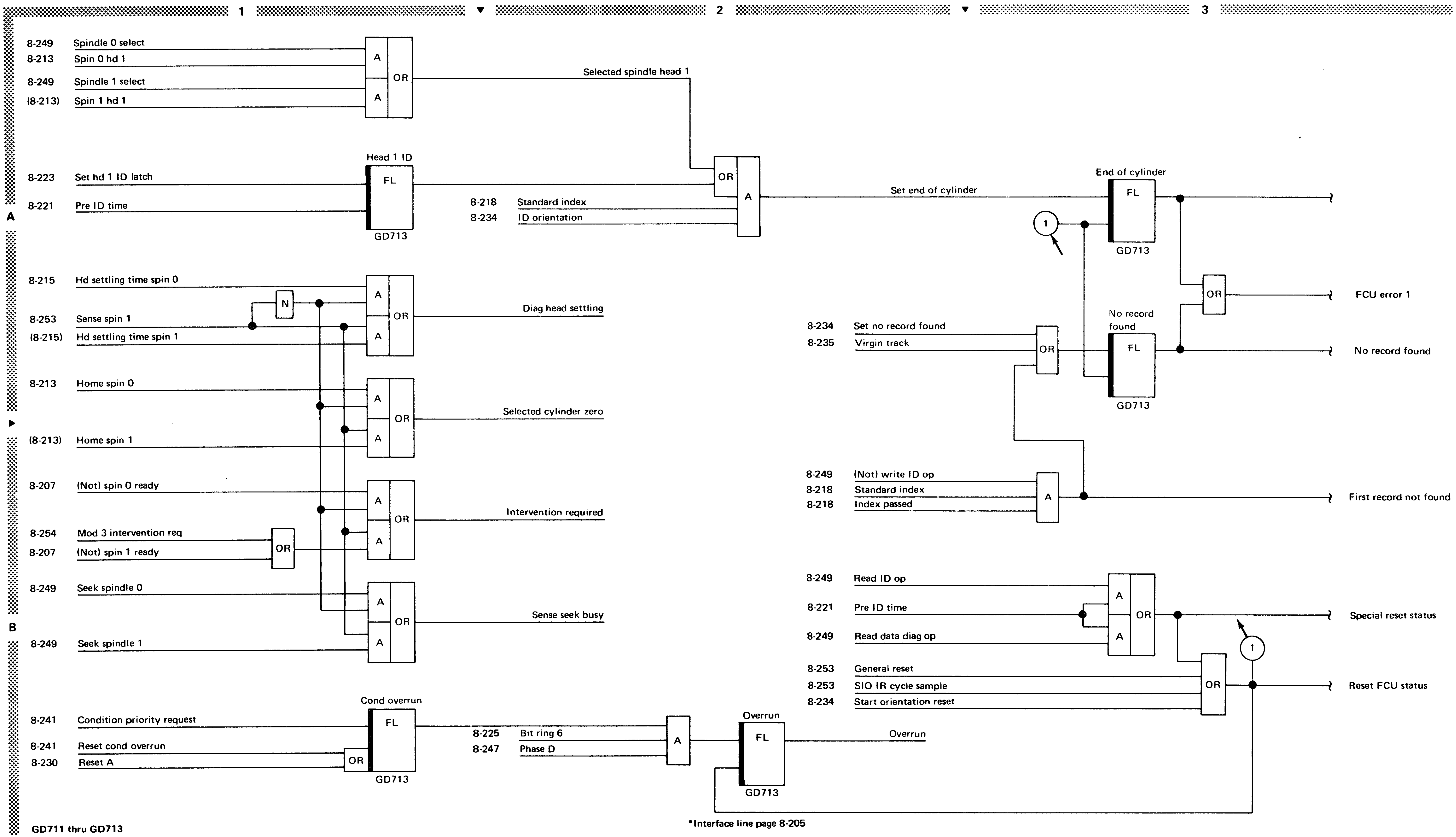
Status Signals

The signals, 'diagnostic head settling', 'selected cylinder zero', 'intervention required', and 'sense seek busy', are input signals for file control unit sense information.



Simplified Reset Logic


8-215 Set seek check 0
8-249 Spindle 0 select
(8-215) Set seek check 1
8-249 Spindle 1 select
8-218 Execute
8-207 (Not) spin 0 ready
8-207 (Not) spin 1 ready
8-249 FCU busy
8-231 Set end of cylinder
8-211 Equipment check
8-249 (Not) read data diag op
8-235 FCU error
8-249 Read ID op
8-223 Counter set
8-221 Post ID time
8-249 Write data op
8-234 ID orientation
8-235 Virgin track
8-218 End write ID op
8-231 First record not found
8-234 Scan found
8-225 Bit ring 7
8-223 Counter decode 1
8-221 Post data time
8-249 (Not) write ID op
8-218 N carry gate
8-239 IPL
IPL set I/O cond B
8-253 No op status
Seek check reset FCU busy
8-253 General reset
Set no op
Reset FCU busy
*CPU clock 2
*CPU clock 0
Cond RST 1
Cond RST 2
GD711
8-249 (Not) FCU busy
140 ns
Deselect file
Select file
8-253 General reset
1100 ns
Pure end op reset
End op reset
Reset A
Reset B
8-218 Index reset
*CPU clock 0
Pure initial reset
*CPU clock 4
Start op
*CPU clock 4
*CPU early phase C
8-249 (Not) seek spindle 1
8-249 Spin 1 select
8-249 (Not) seek spindle 0
8-249 Spin 0 select
Inh start
8-249 FCU busy
GD711 thru GD713
*Interface line page 8-205


1
2
3
A
B
8-249 Spindle 0 select
8-213 Spin 0 hd 1
8-249 Spindle 1 select
(8-213) Spin 1 hd 1
A
A
OR
Selected spindle head 1
Head 1 ID
8-223 Set hd 1 ID latch
8-221 Pre ID time
FL
GD713
OR
A
8-218 Standard index
8-234 ID orientation
Set end of cylinder
End of cylinder
FL
GD713
1
8-215 Hd settling time spin 0
N
8-253 Sense spin 1
(8-215) Hd settling time spin 1
Diag head settling
8-213 Home spin 0
(8-213) Home spin 1
Selected cylinder zero
8-207 (Not) spin 0 ready
8-254 Mod 3 intervention req
8-207 (Not) spin 1 ready
Intervention required
8-249 Seek spindle 0
8-249 Seek spindle 1
Sense seek busy
OR
FCU error 1
No record found
8-234 Set no record found
8-235 Virgin track
FL
GD713
No record found
8-249 (Not) write ID op
8-218 Standard index
8-218 Index passed
First record not found
8-249 Read ID op
8-221 Pre ID time
8-249 Read data diag op
Special reset status
8-253 General reset
8-253 SIO IR cycle sample
8-234 Start orientation reset
Reset FCU status
Cond overrun
8-241 Condition priority request
8-241 Reset cond overrun
8-230 Reset A
FL
GD713
8-225 Bit ring 6
8-247 Phase D
Overrun
FL
GD713
Overrun
GD711 thru GD713
*Interface line page 8-205

1 2 3

A

B

CARD N2

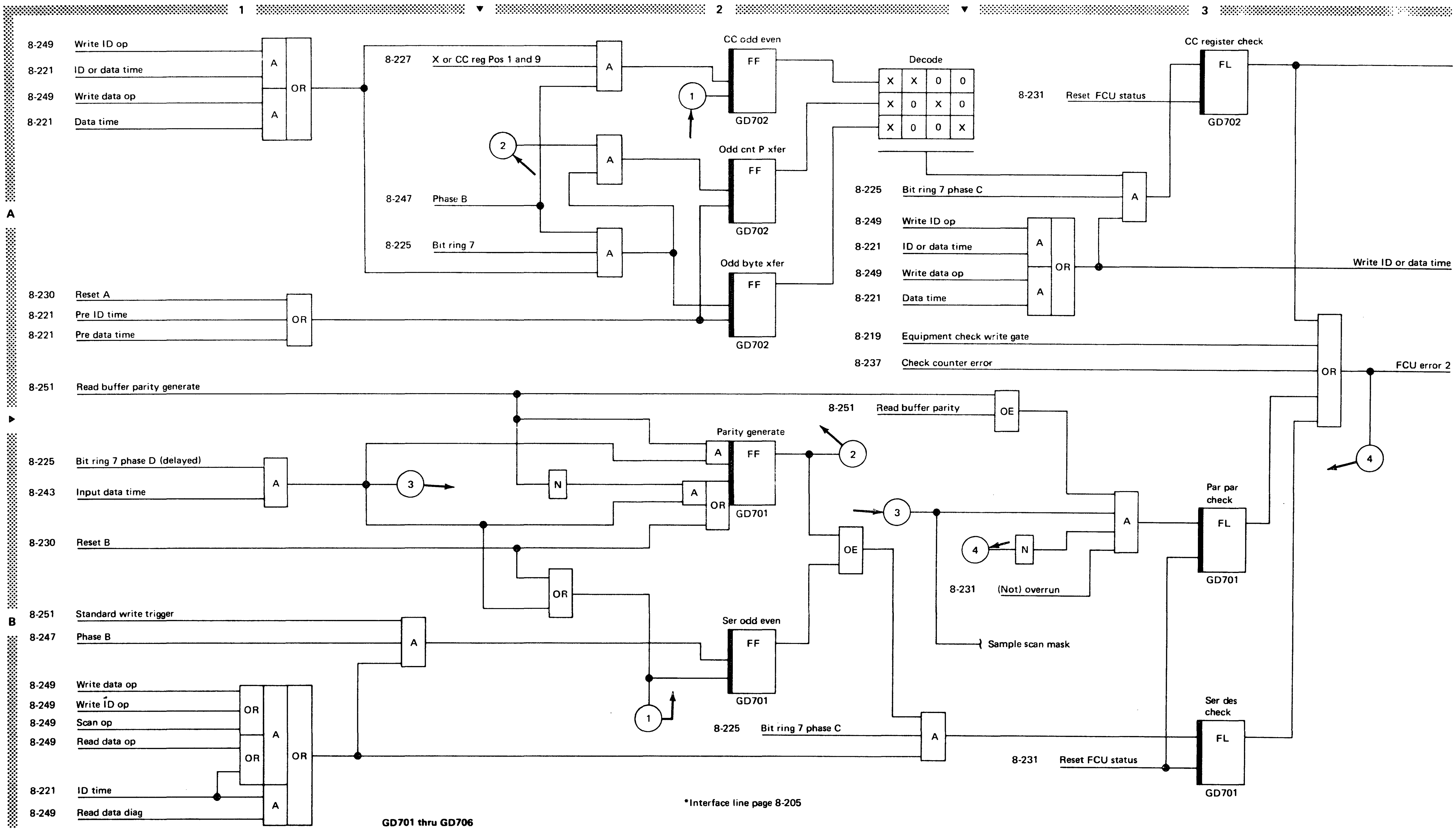
Card N2 is shown on three pages and contains the following logic:

1. Error conditions
   a. Cyclic code register check
   b. Parallel parity check
   c. Serdes check
   d. Missing address mark
   e. Track condition check
   f. Virgin track
   g. Data check
   h. ID CC error
2. Compare

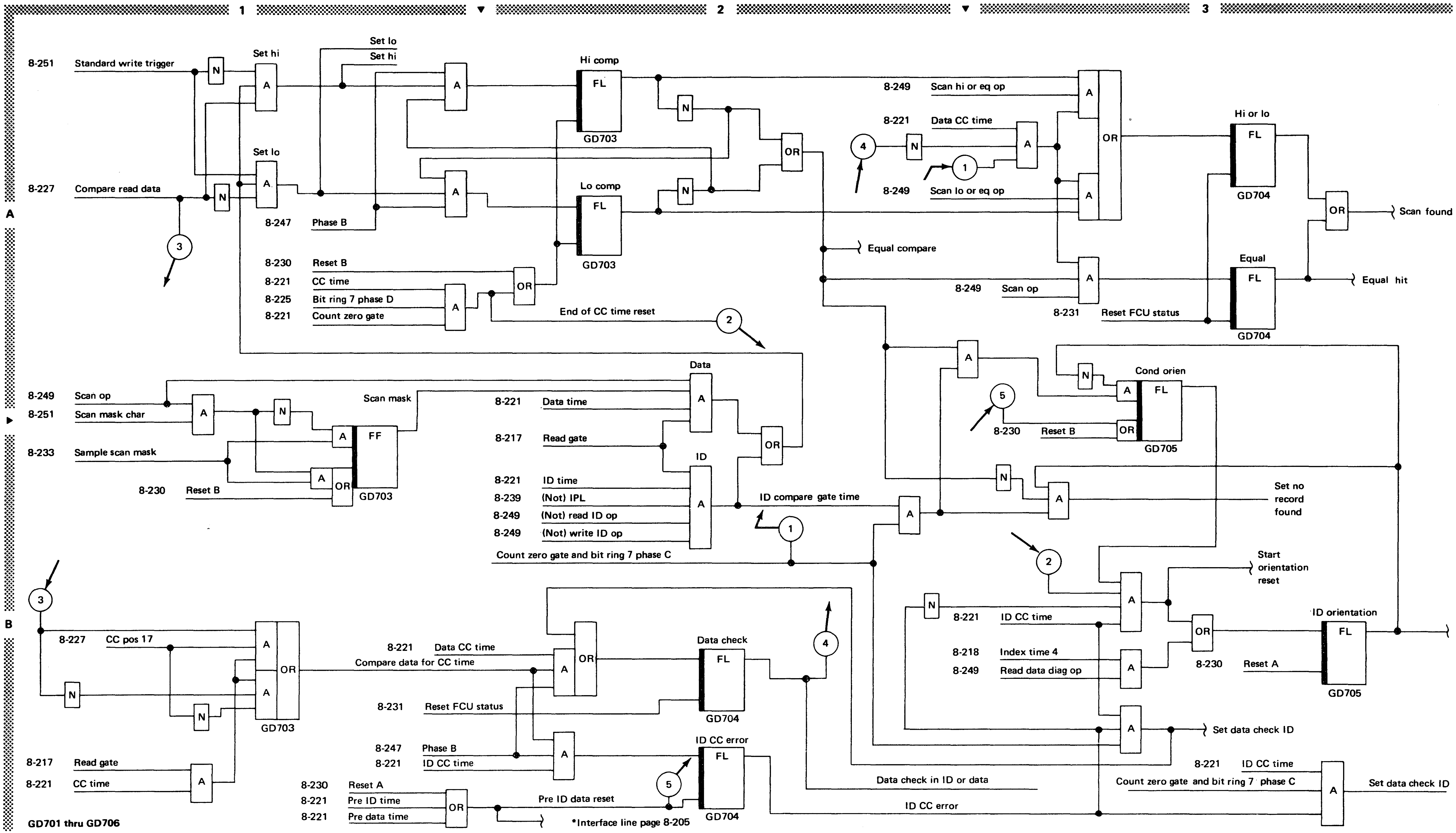
The error condition objectives are described on page 8-228.

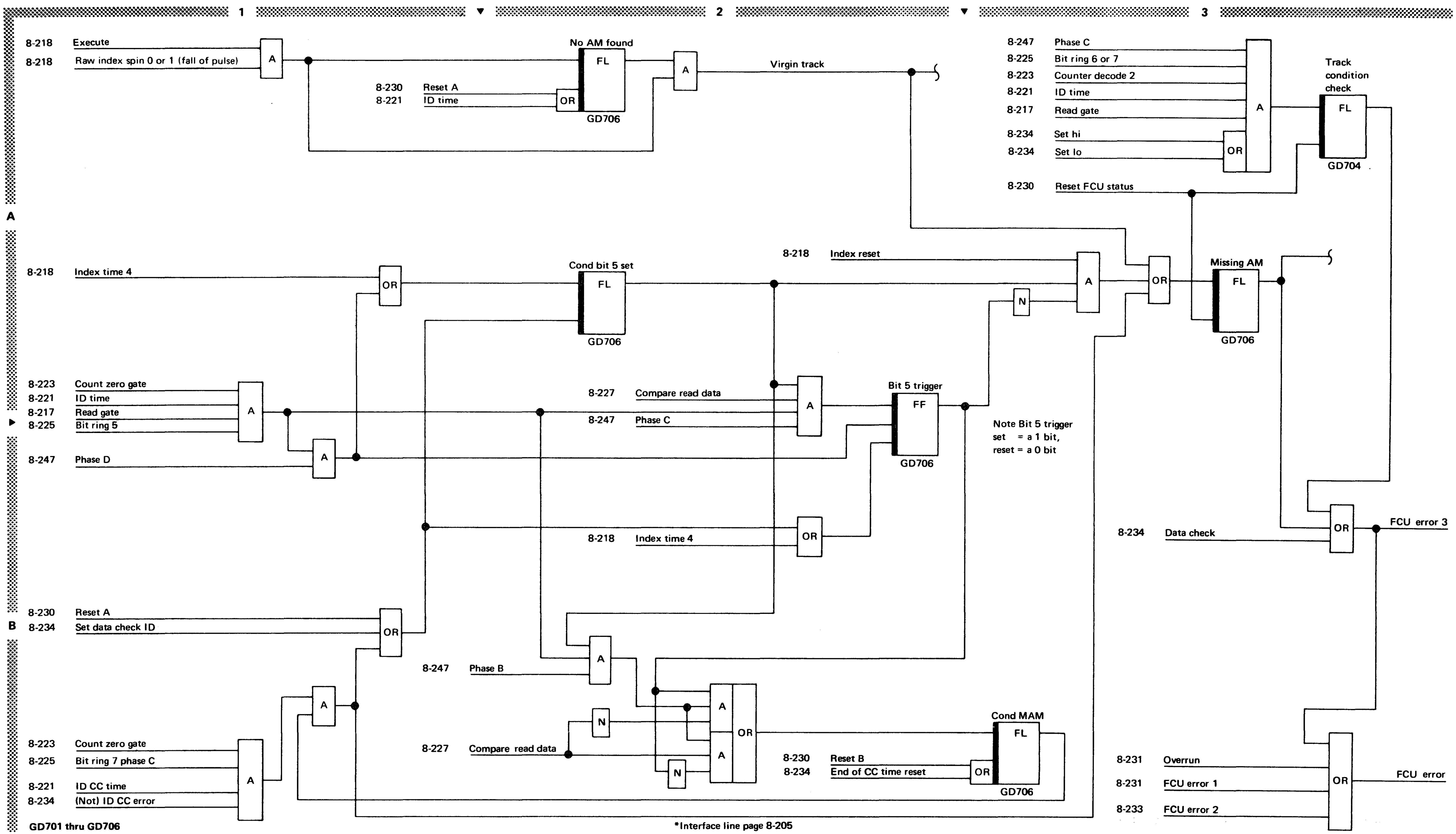
The compare logic receives its input from two sources, the standard write trigger and the compare read data trigger. The compare logic can indicate 'hi' if the compare read data trigger source is greater than the standard write trigger, 'lo' if the standard write trigger source is greater than the compare read data trigger source, or 'equal' if the two sources match correctly.

The hi, lo, or equal conditions are gated by the operation being performed by the file control unit to indicate 'ID orientation', 'scan found', or 'data check'.



1
2
3
A
B
8-249 Write ID op
8-221 ID or data time
8-249 Write data op
8-221 Data time
OR
8-227 X or CC reg Pos 1 and 9
CC odd even
FF
GD702
Decode
X X 0 0
X 0 X 0
X 0 0 X
CC register check
FL
GD702
8-231 Reset FCU status
8-247 Phase B
8-225 Bit ring 7
Odd cnt P xfer
Odd byte xfer
8-225 Bit ring 7 phase C
8-249 Write ID op
8-221 ID or data time
8-249 Write data op
8-221 Data time
Write ID or data time
8-230 Reset A
8-221 Pre ID time
8-221 Pre data time
8-219 Equipment check write gate
8-237 Check counter error
FCU error 2
8-251 Read buffer parity generate
8-251 Read buffer parity
OE
Parity generate
GD701
8-225 Bit ring 7 phase D (delayed)
8-243 Input data time
N
Par par check
8-230 Reset B
8-231 (Not) overrun
8-251 Standard write trigger
8-247 Phase B
Ser odd even
Sample scan mask
8-249 Write data op
8-249 Write ID op
8-249 Scan op
8-249 Read data op
8-221 ID time
8-249 Read data diag
8-225 Bit ring 7 phase C
Ser des check
8-231 Reset FCU status
*Interface line page 8-205
GD701 thru GD706


1
2
3
A
B
8-251 Standard write trigger
Set hi
Set lo
Set hi
Set lo
Hi comp
FL
GD703
8-227 Compare read data
Lo comp
FL
GD703
8-247 Phase B
8-230 Reset B
8-221 CC time
8-225 Bit ring 7 phase D
8-221 Count zero gate
End of CC time reset
Equal compare
8-249 Scan hi or eq op
8-221 Data CC time
8-249 Scan lo or eq op
8-249 Scan op
8-231 Reset FCU status
Hi or lo
FL
GD704
Equal
FL
GD704
Scan found
Equal hit
8-249 Scan op
8-251 Scan mask char
8-233 Sample scan mask
8-230 Reset B
Scan mask
FF
GD703
Data
8-221 Data time
8-217 Read gate
ID
8-221 ID time
8-239 (Not) IPL
8-249 (Not) read ID op
8-249 (Not) write ID op
Count zero gate and bit ring 7 phase C
ID compare gate time
Cond orien
FL
8-230 Reset B
GD705
Set no record found
Start orientation reset
8-227 CC pos 17
GD703
8-217 Read gate
8-221 CC time
8-221 Data CC time
Compare data for CC time
8-231 Reset FCU status
8-247 Phase B
8-221 ID CC time
8-230 Reset A
8-221 Pre ID time
8-221 Pre data time
Pre ID data reset
*Interface line page 8-205
Data check
FL
GD704
ID CC error
FL
GD704
8-221 ID CC time
8-218 Index time 4
8-249 Read data diag op
8-230 Reset A
ID orientation
FL
GD705
Set data check ID
8-221 ID CC time
Count zero gate and bit ring 7 phase C
Set data check ID
Data check in ID or data
ID CC error
GD701 thru GD706


1
2
3
A
B
8-218 Execute
8-218 Raw index spin 0 or 1 (fall of pulse)
No AM found
FL
GD706
8-230 Reset A
8-221 ID time
Virgin track
8-247 Phase C
8-225 Bit ring 6 or 7
8-223 Counter decode 2
8-221 ID time
8-217 Read gate
8-234 Set hi
8-234 Set lo
Track condition check
GD704
8-230 Reset FCU status
8-218 Index reset
8-218 Index time 4
Cond bit 5 set
Missing AM
8-223 Count zero gate
8-221 ID time
8-217 Read gate
8-225 Bit ring 5
8-247 Phase D
8-227 Compare read data
8-247 Phase C
Bit 5 trigger
FF
Note Bit 5 trigger
set = a 1 bit,
reset = a 0 bit
8-234 Data check
FCU error 3
8-218 Index time 4
8-230 Reset A
8-234 Set data check ID
8-247 Phase B
8-227 Compare read data
Cond MAM
8-230 Reset B
8-234 End of CC time reset
8-223 Count zero gate
8-225 Bit ring 7 phase C
8-221 ID CC time
8-234 (Not) ID CC error
8-231 Overrun
8-231 FCU error 1
8-233 FCU error 2
FCU error
GD701 thru GD706
*Interface line page 8-205

CARD P2

Card P2 is shown on two pages and contains the following logic:

1. CE controls
2. Check counter (bit count appendage)
3. Local storage register selection
4. Initial program load latches

CE Controls

This logic is active for a load I/O instruction diagnostic operation.

Normal input to index, oscillator, separated clock, separated data, and address mark indicator lines is blocked and controlled instead by bits present in the load I/O instruction diagnostic byte. (See the description of the load I/O instruction diagnostic byte, load I/O instruction in chapter 1.) The file control unit cycle steal requests may also be blocked in addition to the other input mentioned.

Check Counter (BCA)

The bit count appendage check character is generated in the check counter. The counter will accumulate 255 data bits, reset to zero by overflowing, and continue to count toward 255 bits again. When data input stops, the result is left in the check counter to be written after the cyclic code characters on disk. The manner in which the bit count appendage bits are written is explained under "Cyclic Code Register."

A test is made on the check counter before it is used in a start I/O instruction write operation by allowing the counter to step at each phase B time, in the area following index. The output is compared to a predicted value at the proper time and a check counter error is indicated if the results do not compare. Two checks are made on the check counter: (1) that positions 8 through 128 are reset off at index 2 time, and (2) that the counter stepped to a value of at least 192 from index 4 time until the control counter is decremented to 1 (the control counter was set to 25 at index 4 time). There are 8 inputs per byte (phase B), for 24 bytes of the 25 byte countdown for a total of 192 advance pulses.

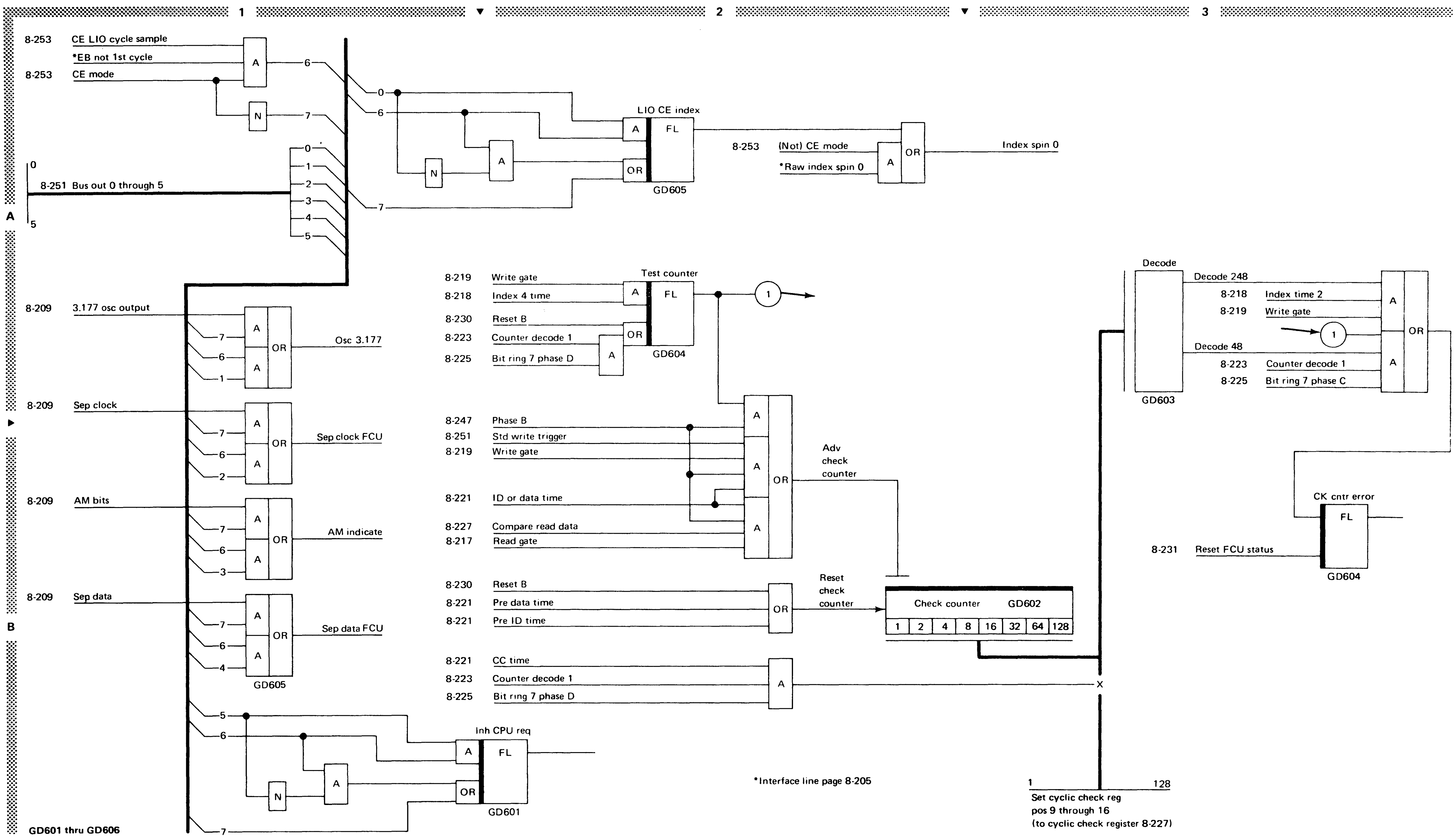
Local Storage Register Selection

The file control unit addresses the local storage registers during load I/O instructions, sense I/O instructions, and during cycle steal cycles (I/O cycle). Local storage registers are addressed at CPU clock 8 and clock 4 times.

Status byte latches 0-1, 2-3, disk file control register and disk file data register, are set during the I-Q cycle of an instruction with the N-field bits. These latches gate the file control unit logic to select the desired sense byte or local storage register.

Initial Program Load Latches

The initial program load latches are set at the start of an initial program load command. The output of the latch controls the file control unit logic which performs the initial program load operation.



*Interface line page 8-205

1 2 3

A

B

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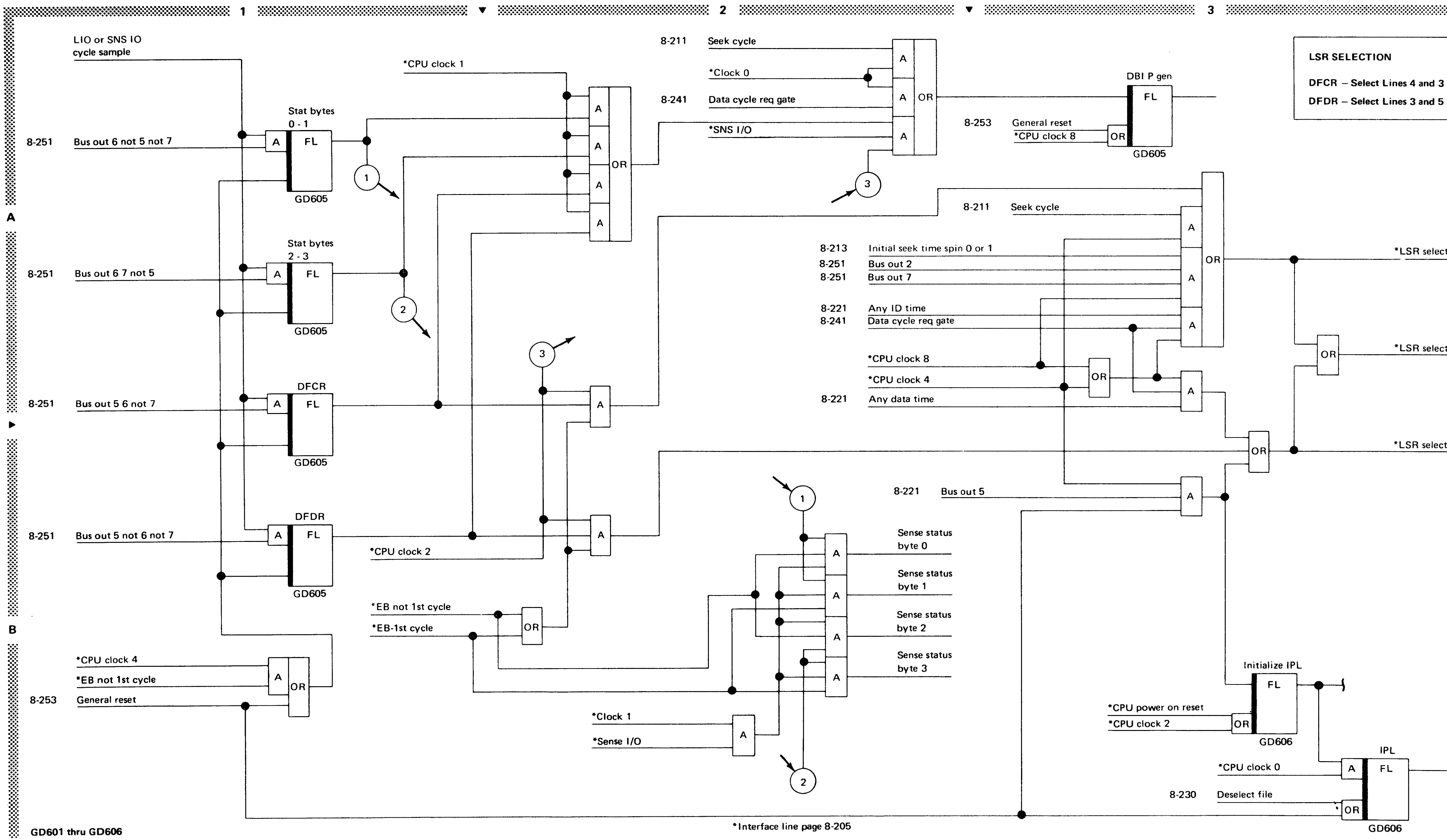


LIO or SNS IO cycle sample
8-251 Bus out 6 not 5 not 7
Stat bytes 0 - 1
GD605
*CPU clock 1
8-251 Bus out 6 7 not 5
Stat bytes 2 - 3
8-251 Bus out 5 6 not 7
DFCR
8-251 Bus out 5 not 6 not 7
DFDR
*CPU clock 2
*EB not 1st cycle
*EB-1st cycle
*CPU clock 4
*EB not 1st cycle
8-253 General reset
GD601 thru GD606
8-211 Seek cycle
*Clock 0
8-241 Data cycle req gate
*SNS I/O
DBI P gen
8-253 General reset
*CPU clock 8
LSR SELECTION
DFCR – Select Lines 4 and 3
DFDR – Select Lines 3 and 5
8-211 Seek cycle
8-213 Initial seek time spin 0 or 1
8-251 Bus out 2
8-251 Bus out 7
8-221 Any ID time
8-241 Data cycle req gate
*CPU clock 8
*CPU clock 4
8-221 Any data time
*LSR select 4
*LSR select 3
*LSR select 5
8-221 Bus out 5
Sense status byte 0
Sense status byte 1
Sense status byte 2
Sense status byte 3
*Clock 1
*Sense I/O
Initialize IPL
*CPU power on reset
*CPU clock 2
GD606
IPL
*CPU clock 0
8-230 Deselect file
*Interface line page 8-205

CARD Q2

Card Q2 is shown on two pages and contains the following logic:

1. Priority request 3 (data cycle steal request)
2. Serdes control

Priority request 3 is highest in priority of the cycle steal I/O attachments. The file control unit requests a cycle steal (I/O cycle) whenever it needs the CPU facilities to address core storage or to modify the address in a local storage register. Constants which modify core storage or the local storage register address are generated by the file control unit during an I/O cycle and may be added or subtracted to the value in the local storage register or core. The constant may also be entered into these locations without change. A cycle steal request is started when one of the inputs to the 'condition prior request' latch is active, and gated by a final condition, 'bit ring 7 and phase C'. The remainder of the cycle steal request is as follows:

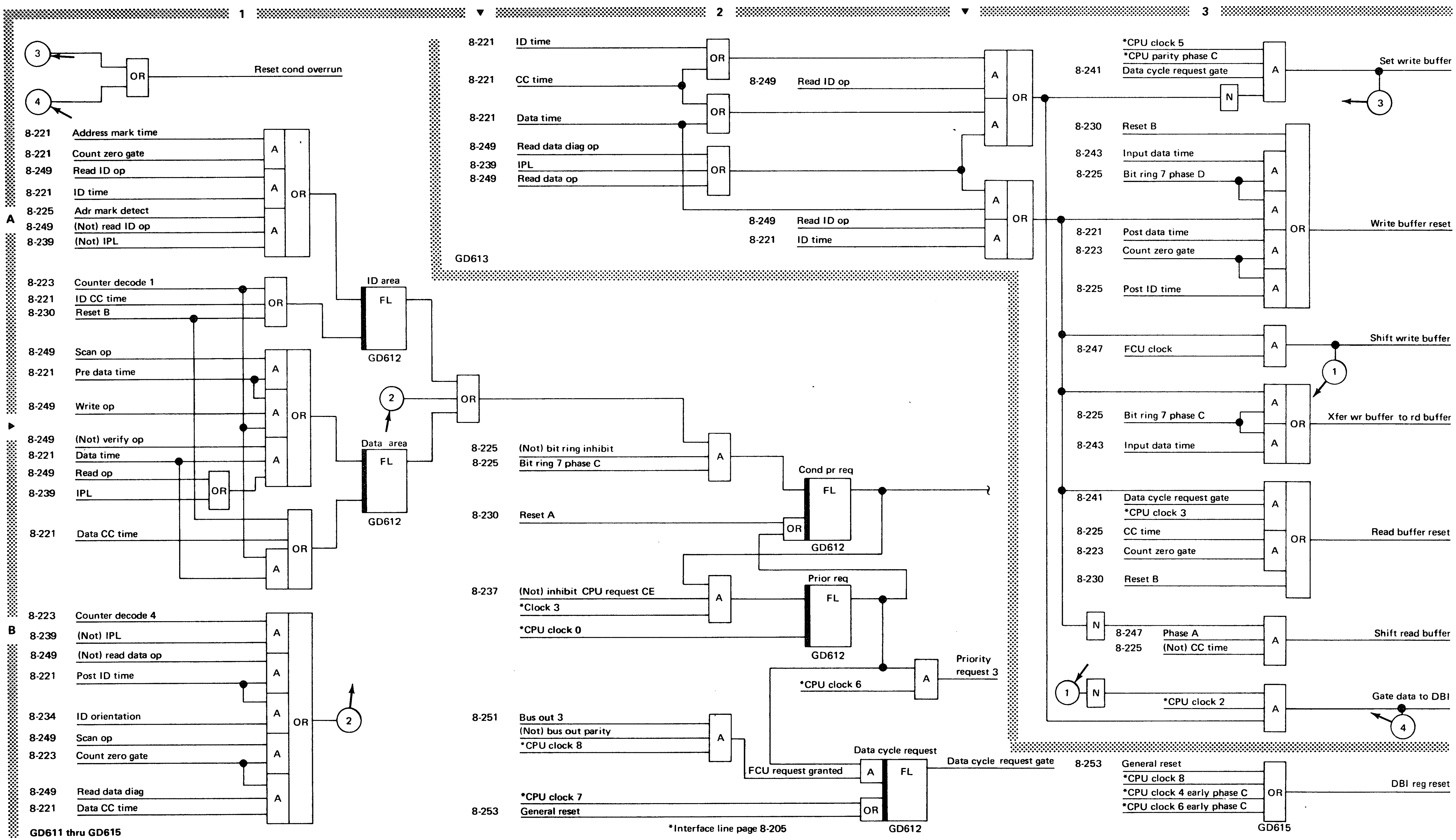
Clock 3–The 'prior request' latch is set.
Clock 6–The request for an I/O cycle is active on the interface lines.
Clock 8–The CPU responds to the cycle steal request by 'bus out 3' active. The 'data cycle request' latch is set to indicate that the next I/O cycle is for the file control unit.

The I/O cycle is a result of a priority request. The following actions occur during the I/O cycle:

Clock 0–Reset 'condition prior request' latch
Clock 2–Data in the file control unit or a constant generated in the file control unit is gated onto the data bus in lines.
Clock 4–A constant which modifies a local storage register address can be gated onto the data bus in.
Clock 5–Information in the CPU is available to the file control unit on the data bus out lines.

The latches arithmetic and logic unit binary subtract, store data, and block SDR to B register are located in the file control unit and control how the CPU processes the constants and data. If the arithmetic and logic unit binary subtract latch is set, the constant is subtracted from the value at the specified location; if the latch is not set, the constant is added to the value. If the store data latch is set, the sum or difference is restored to core storage or the local storage register. If the block SDR to B register latch is set, data from core storage is prevented from reaching the B register in the CPU. As a result, information entered into the B register from the data bus in is not modified.

The serdes registers are controlled by the serdes control logic. The gates generate, reset, shift, and transfer data within and through the registers. The signal names are self-explanatory as to their functions.


1
2
3
A
B
Reset cond overrun
8-221 Address mark time
8-221 Count zero gate
8-249 Read ID op
8-221 ID time
8-225 Adr mark detect
8-249 (Not) read ID op
8-239 (Not) IPL
8-223 Counter decode 1
8-221 ID CC time
8-230 Reset B
ID area
GD612
8-249 Scan op
8-221 Pre data time
8-249 Write op
8-249 (Not) verify op
8-221 Data time
8-249 Read op
8-239 IPL
8-221 Data CC time
Data area
GD612
8-223 Counter decode 4
8-239 (Not) IPL
8-249 (Not) read data op
8-221 Post ID time
8-234 ID orientation
8-249 Scan op
8-223 Count zero gate
8-249 Read data diag
8-221 Data CC time
GD611 thru GD615
8-221 ID time
8-221 CC time
8-221 Data time
8-249 Read data diag op
8-239 IPL
8-249 Read data op
8-249 Read ID op
8-249 Read ID op
8-221 ID time
GD613
8-225 (Not) bit ring inhibit
8-225 Bit ring 7 phase C
Cond pr req
8-230 Reset A
GD612
Prior req
8-237 (Not) inhibit CPU request CE
*Clock 3
*CPU clock 0
GD612
Priority request 3
*CPU clock 6
8-251 Bus out 3
(Not) bus out parity
*CPU clock 8
FCU request granted
Data cycle request
Data cycle request gate
*CPU clock 7
8-253 General reset
*Interface line page 8-205
GD612
*CPU clock 5
*CPU parity phase C
8-241 Data cycle request gate
Set write buffer
8-230 Reset B
8-243 Input data time
8-225 Bit ring 7 phase D
8-221 Post data time
8-223 Count zero gate
8-225 Post ID time
Write buffer reset
8-247 FCU clock
Shift write buffer
8-225 Bit ring 7 phase C
8-243 Input data time
Xfer wr buffer to rd buffer
8-241 Data cycle request gate
*CPU clock 3
8-225 CC time
8-223 Count zero gate
8-230 Reset B
Read buffer reset
8-247 Phase A
8-225 (Not) CC time
Shift read buffer
*CPU clock 2
Gate data to DBI
8-253 General reset
*CPU clock 8
*CPU clock 4 early phase C
*CPU clock 6 early phase C
DBI reg reset
GD615

1 2 3

A

B

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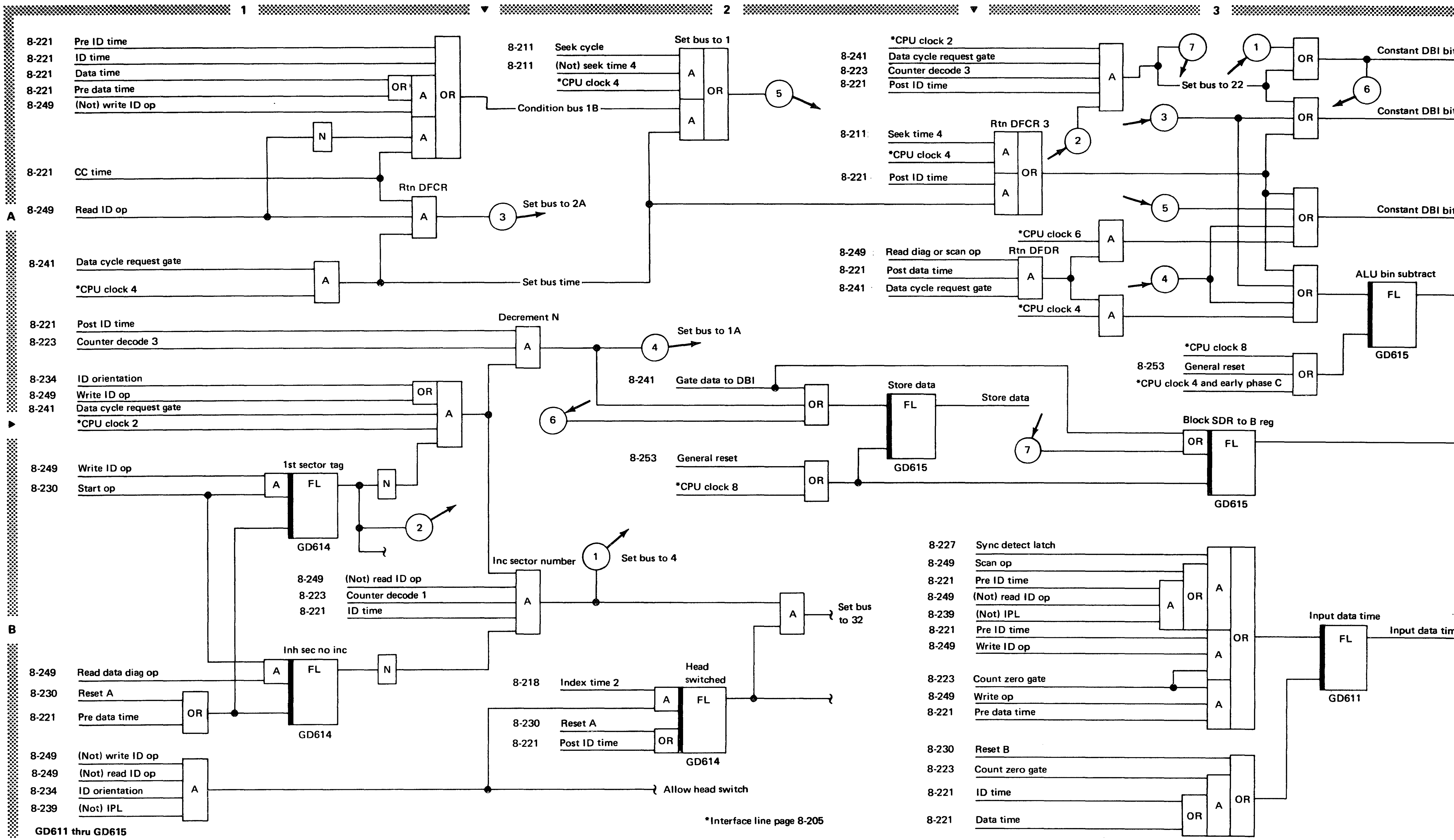


1
2
3
A
B
8-221 Pre ID time
8-221 ID time
8-221 Data time
8-221 Pre data time
8-249 (Not) write ID op
Condition bus 1B
8-221 CC time
8-249 Read ID op
Rtn DFCR
Set bus to 2A
8-241 Data cycle request gate
*CPU clock 4
Set bus time
8-211 Seek cycle
8-211 (Not) seek time 4
*CPU clock 4
Set bus to 1
8-221 Post ID time
8-223 Counter decode 3
Decrement N
Set bus to 1A
8-234 ID orientation
8-249 Write ID op
8-241 Data cycle request gate
*CPU clock 2
8-249 Write ID op
8-230 Start op
1st sector tag
GD614
Inc sector number
Set bus to 4
8-249 (Not) read ID op
8-223 Counter decode 1
8-221 ID time
Set bus to 32
8-249 Read data diag op
8-230 Reset A
8-221 Pre data time
Inh sec no inc
GD614
8-249 (Not) write ID op
8-249 (Not) read ID op
8-234 ID orientation
8-239 (Not) IPL
GD611 thru GD615
8-218 Index time 2
8-230 Reset A
8-221 Post ID time
Head switched
GD614
Allow head switch
*Interface line page 8-205
8-241 Gate data to DBI
Store data
Store data
GD615
8-253 General reset
*CPU clock 8
*CPU clock 2
8-241 Data cycle request gate
8-223 Counter decode 3
8-221 Post ID time
Set bus to 22
Rtn DFCR 3
8-211 Seek time 4
*CPU clock 4
8-221 Post ID time
*CPU clock 6
8-249 Read diag or scan op
Rtn DFDR
8-221 Post data time
8-241 Data cycle request gate
*CPU clock 4
Constant DBI bit 5
Constant DBI bit 6
Constant DBI bit 7
ALU bin subtract
GD615
*CPU clock 8
8-253 General reset
*CPU clock 4 and early phase C
Block SDR to B reg
GD615
8-227 Sync detect latch
8-249 Scan op
8-221 Pre ID time
8-249 (Not) read ID op
8-239 (Not) IPL
8-221 Pre ID time
8-249 Write ID op
8-223 Count zero gate
8-249 Write op
8-221 Pre data time
8-230 Reset B
8-223 Count zero gate
8-221 ID time
8-221 Data time
Input data time
Input data time
GD611

CARD R2

Card R2 is shown on two pages and contains:

1. Data bus in assembler
2. File control unit clock and phase generator

The data bus in assembler is the file control unit "outlet" for information to the CPU. Data, constants, and status information are grouped and gated onto the data bus in through this register. The data bus in parity bit is generated on card P2-2.

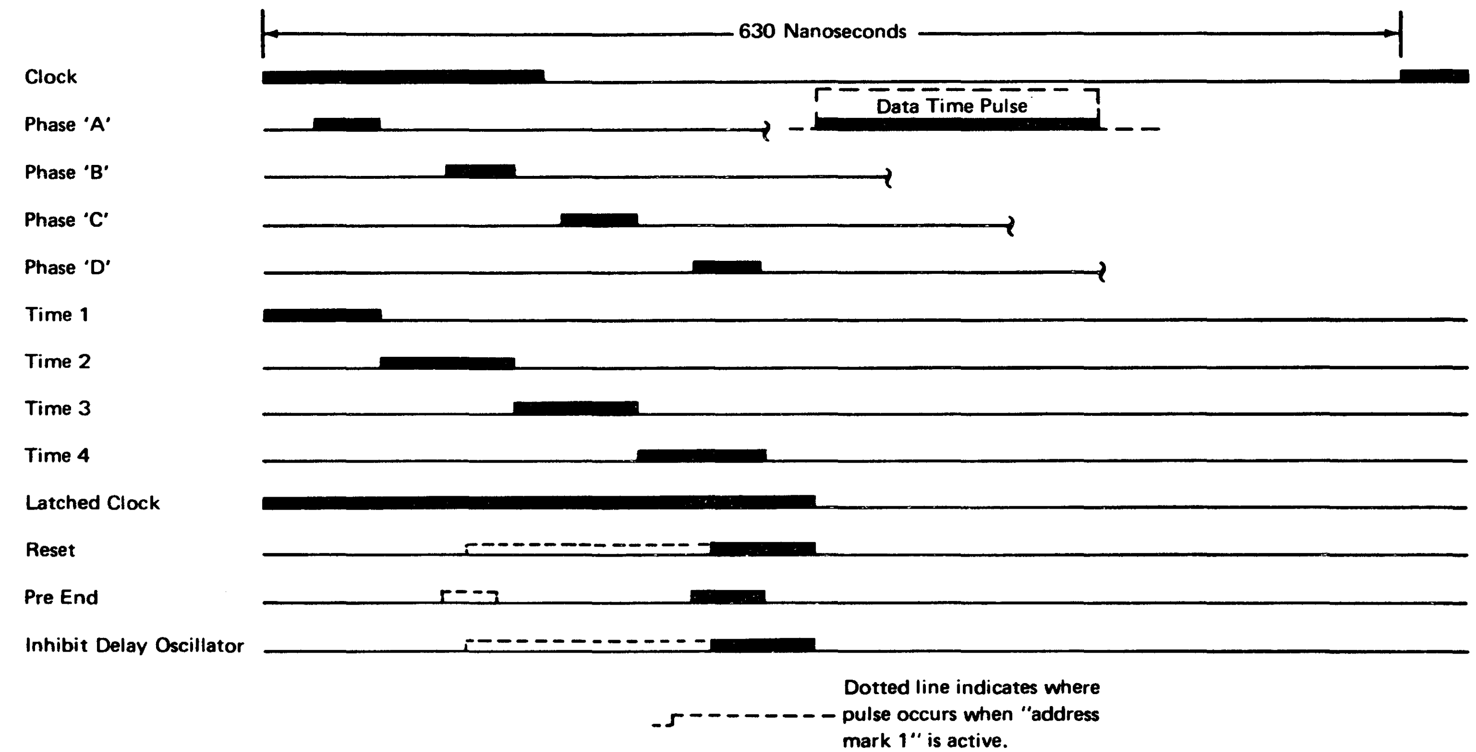
The file control unit clock provides basic timing for file control unit operation. The clock may be driven by a 3.177 oscillator (write clock) or separated clock pulses from the data separator (read clock). The clock is started when 'execute' is active. These signals are produced at the beginning of an operation, after the I-Q and I-R cycles are complete.

During a write operation, or during any operation for which the clock bits from the disk are not usable, the clock is driven with the 3.177 oscillator. When data is being read from the disk, the clock is driven with the separated clock pulses from the data separator. A gating signal, 'clock gate', determines which signal (oscillator or separated clock) has control. If 'clock gate' is active, the oscillator drives the clock.

When the clock drive is changed from oscillator drive to separated clock pulses or vice versa, a sliver (partial) pulse can be produced. 'Start read clock' triggers 1 and 2 prevent the sliver by sequencing the changeover.

Clock pulses are alternately gated to produce clock and data time pulses. Timing within each bit cell is accomplished with phase pulses 'A', 'B', 'C', 'D'. These pulses are generated with each clock pulse by a delay line (delay oscillator) and a four-ring FF circuit. Each phase pulse is 40 nanoseconds in duration and 40 nanoseconds apart.

During a search for an address mark on disk, phase pulses 'C' and 'D' are not produced. The phase generator is turned off after phase B with a gate line, 'address mark one', which stops the generation of phases 'C' and 'D'. When the clock is driven with separated clock pulses, noise spikes read from the disk could be mistaken for a clock pulse. The 'noise reject' flip latch prevents a clock pulse from being recognized before phases 'A' through 'D' are complete.



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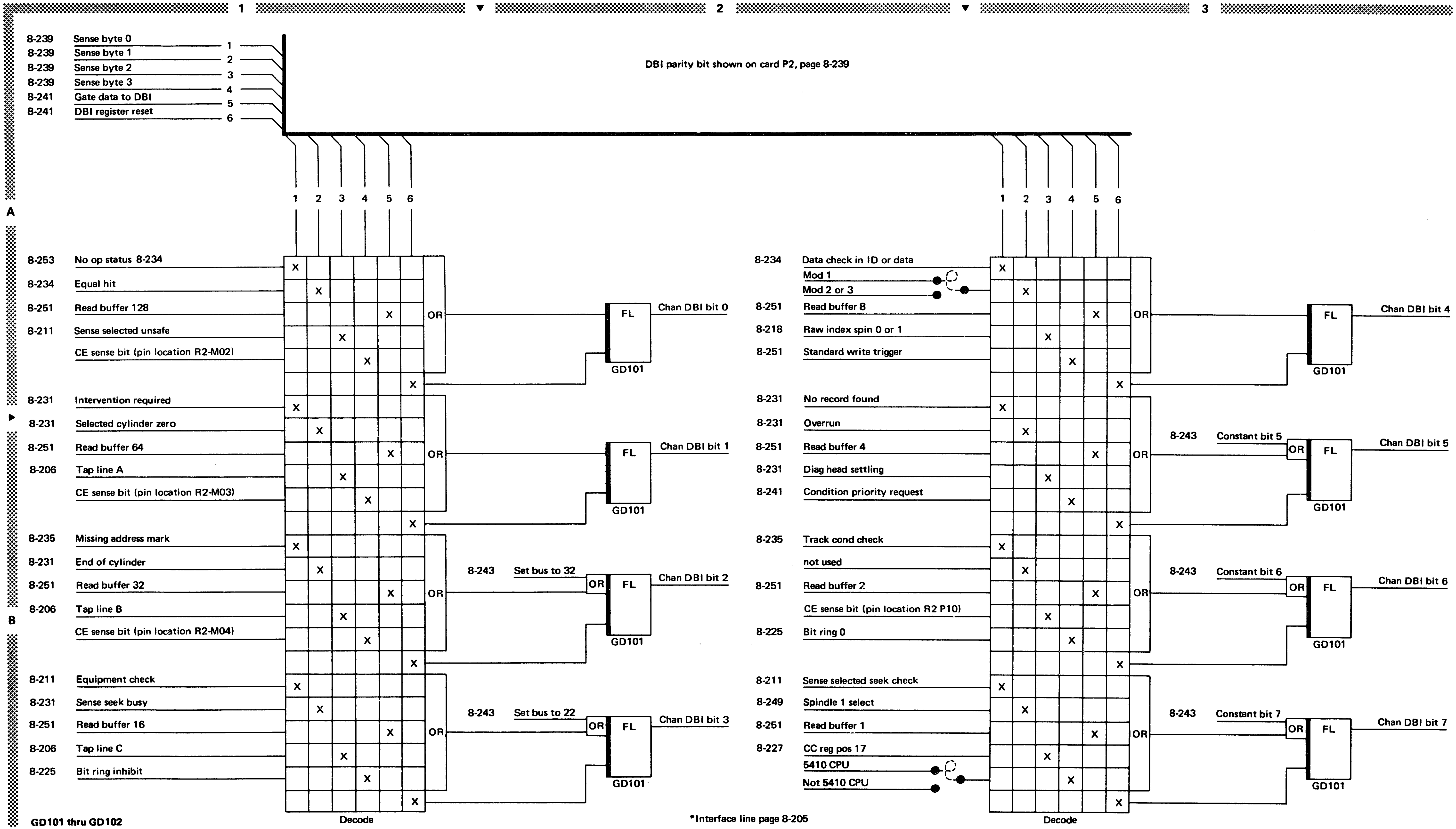
1
2
3
A
B
8-239 Sense byte 0
8-239 Sense byte 1
8-239 Sense byte 2
8-239 Sense byte 3
8-241 Gate data to DBI
8-241 DBI register reset
DBI parity bit shown on card P2, page 8-239
8-253 No op status 8-234
8-234 Equal hit
8-251 Read buffer 128
8-211 Sense selected unsafe
CE sense bit (pin location R2-M02)
Chan DBI bit 0
8-231 Intervention required
8-231 Selected cylinder zero
8-251 Read buffer 64
8-206 Tap line A
CE sense bit (pin location R2-M03)
Chan DBI bit 1
8-235 Missing address mark
8-231 End of cylinder
8-251 Read buffer 32
8-206 Tap line B
CE sense bit (pin location R2-M04)
8-243 Set bus to 32
Chan DBI bit 2
8-211 Equipment check
8-231 Sense seek busy
8-251 Read buffer 16
8-206 Tap line C
8-225 Bit ring inhibit
8-243 Set bus to 22
Chan DBI bit 3
GD101 thru GD102
Decode
8-234 Data check in ID or data
Mod 1
Mod 2 or 3
8-251 Read buffer 8
8-218 Raw index spin 0 or 1
8-251 Standard write trigger
Chan DBI bit 4
8-231 No record found
8-231 Overrun
8-251 Read buffer 4
8-231 Diag head settling
8-241 Condition priority request
8-243 Constant bit 5
Chan DBI bit 5
8-235 Track cond check
not used
8-251 Read buffer 2
CE sense bit (pin location R2 P10)
8-225 Bit ring 0
8-243 Constant bit 6
Chan DBI bit 6
8-211 Sense selected seek check
8-249 Spindle 1 select
8-251 Read buffer 1
8-227 CC reg pos 17
5410 CPU
Not 5410 CPU
8-243 Constant bit 7
Chan DBI bit 7
OR
FL
GD101
*Interface line page 8-205
Decode

1 2 3

A

B

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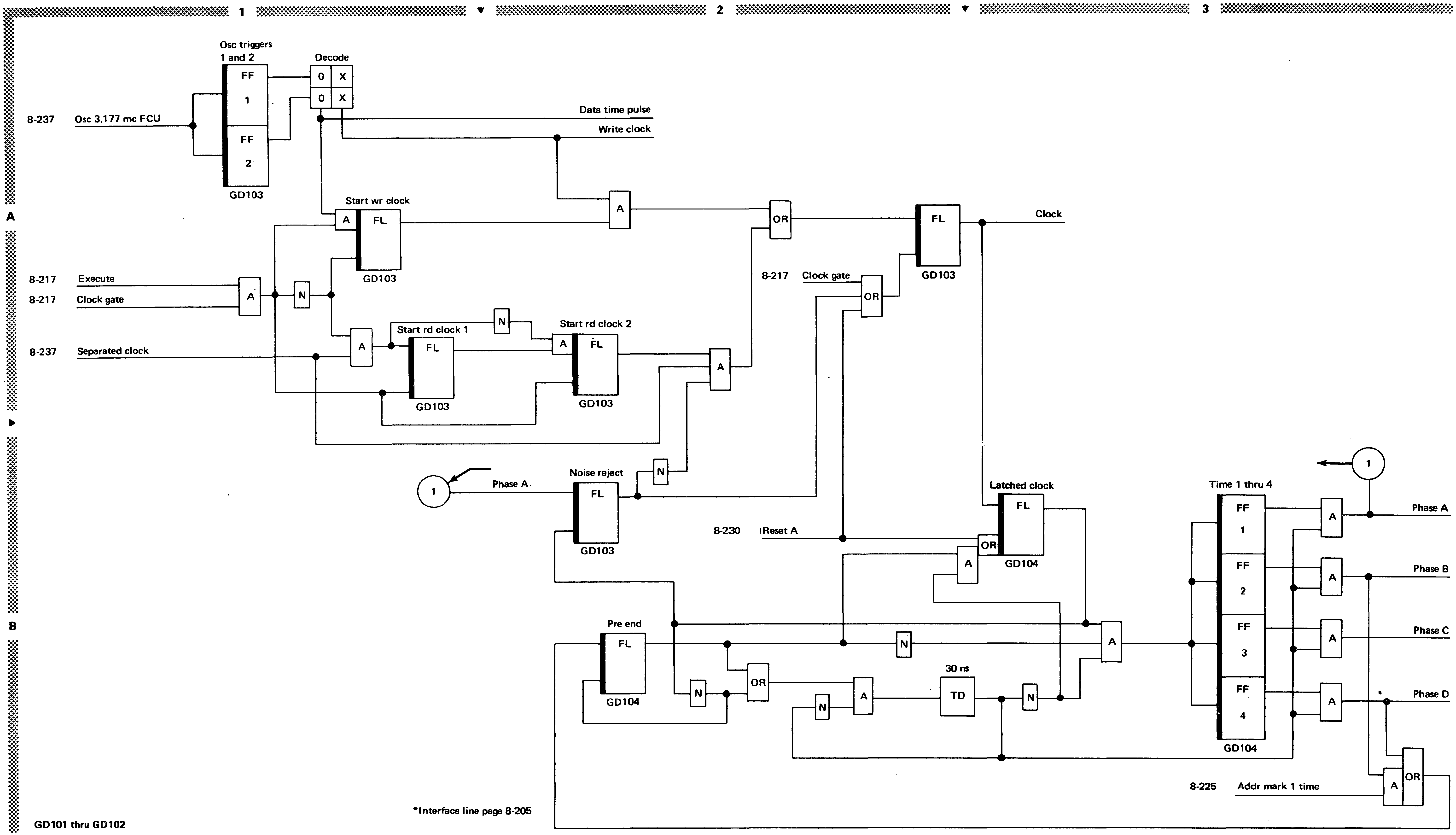


DISK ATTACHMENT–Functional Units
Card R2 (Part 3 of 3)

CARD S2

Card S2 is shown on two pages and contains the following logic:

1. Operation register
2. Bus out register
3. Read buffer/write serializer and write buffer/read deserializer (Serdes)

Operation Register

The operation register is set by bus out lines which sense the N-field and control field of the start I/O instruction during the start I/O instruction I-Q and I-R cycles. This instruction is retained by the file control unit until the operation is complete or certain errors occur.

Bus Out Register

All CPU information sent to the file control unit via the data bus out enters the file control unit through the bus out register. Three decode networks check the bus out register output for errors in parity and seek control, CPU bus greater than 223, and CPU bus equal to zero. The parity bit is detached from the data byte at this point and is transferred through the file control unit separately.

Read Buffer/Write Serializer and Write Buffer/Read Deseiralizer (Serdes)

- Two registers, referred to as serdes, handle data in the file control unit.
- Each register can shift data bits or function as a buffer for the other register.
- Parity bit from the data bus out is not used in the registers.

Two eight-position, dual-purpose registers handle data in the file control unit. Both registers may shift bits toward the high-order end or pass the data byte in parallel without change. These registers, read buffer/write serializer and write buffer/read deserializer (serdes), provide serialization of data during a write operation and deserialization of data during a read. In both operations, the write buffer is the input register, the read buffer is the output.

Write Operation

Data is gated into the write buffer register from the data bus out on a cycle steal operation. The data byte is temporarily held there until it is needed in the read buffer. Another operation transfers the data byte from the write buffer into the read buffer and requests another byte from the CPU to fill the write buffer.

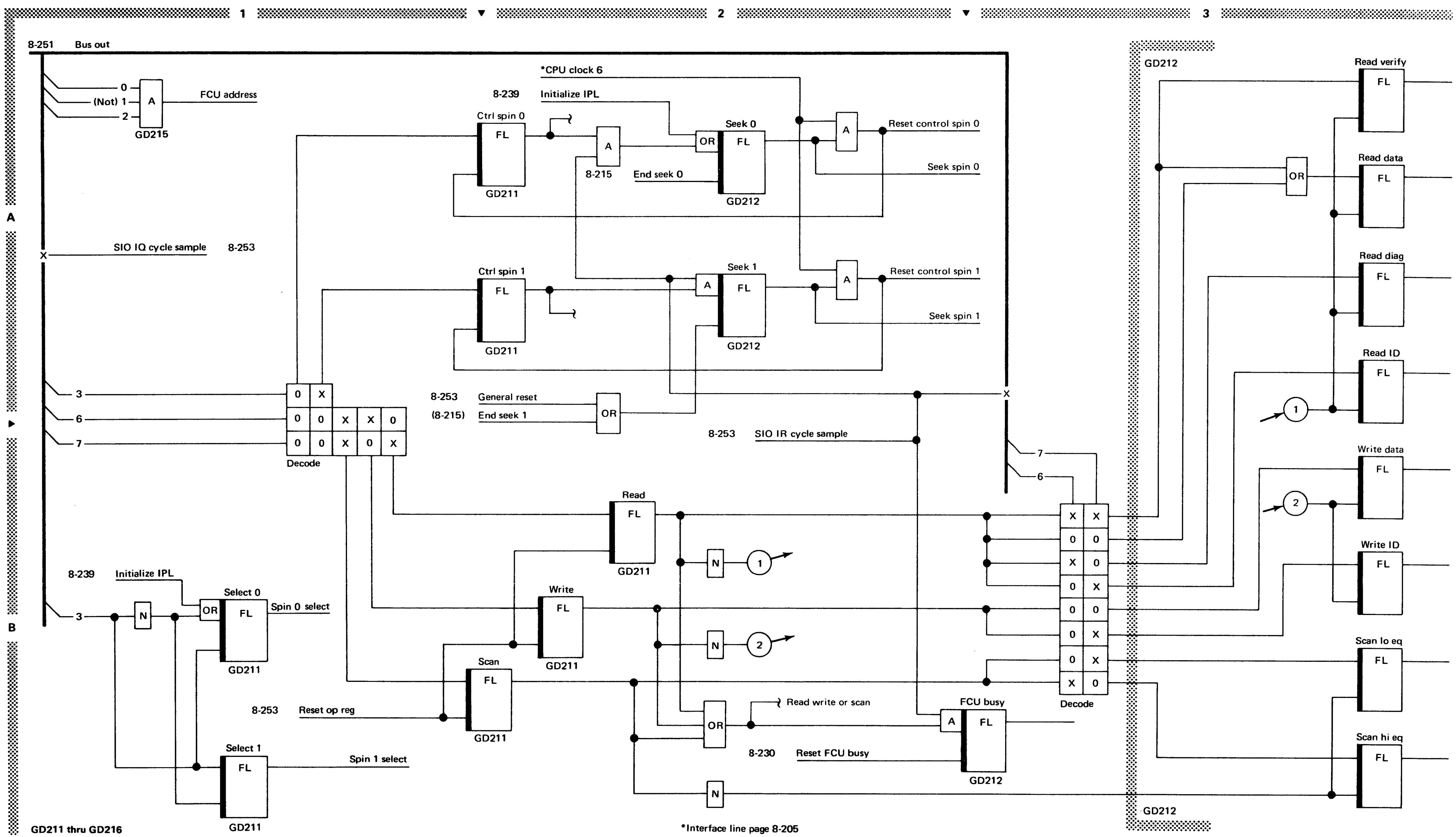
Shift operation of the read buffer can now begin, shifting the bits toward the high-order end and into the 'standard write' trigger where the bit is combined with clock timing and sent on to the disk to be recorded.

As the last bit is shifted out of the read buffer, the write buffer is gated into the read buffer and a cycle steal request is generated to reload the write buffer. This operation continues until the end of the command.

Special bytes that are written on the disk (F2 for address marks) are gated into the read buffer for deserialization. Cyclic code and bit count appendage bytes are not gated into the read buffer for deserialization.

Read Operation

Separated data from the data separator enters the write buffer on the low-order end. The bits are shifted upward to the high-order end as each bit arrives until eight bits are read. The byte is then transferred to the read buffer where it is temporarily held before it can be transferred to the data bus in assembler for entry into the CPU. A parity bit is generated at the data bit in assembler before the read buffer information is gated onto the data bus out.


8-251 Bus out
0
(Not) 1
2
A
FCU address
GD215
*CPU clock 6
8-239 Initialize IPL
Ctrl spin 0
FL
GD211
A
8-215
End seek 0
Seek 0
OR
FL
GD212
A
Reset control spin 0
Seek spin 0
SIO IQ cycle sample 8-253
Ctrl spin 1
FL
GD211
Seek 1
A
FL
GD212
A
Reset control spin 1
Seek spin 1
3
6
7
Decode
8-253 General reset
(8-215) End seek 1
OR
8-253 SIO IR cycle sample
Read
FL
GD211
N
1
Write
FL
GD211
N
2
Scan
FL
GD211
8-253 Reset op reg
OR
Read write or scan
FCU busy
A
FL
GD212
8-230 Reset FCU busy
N
8-239 Initialize IPL
3
N
Select 0
OR
FL
GD211
Spin 0 select
Select 1
FL
GD211
Spin 1 select
GD211 thru GD216
*Interface line page 8-205
7
6
Decode
GD212
Read verify
FL
Read data
OR
FL
Read diag
FL
Read ID
FL
1
Write data
FL
2
Write ID
FL
Scan lo eq
FL
Scan hi eq
FL
GD212
1
2
3
A
B

1 2 3

A

B

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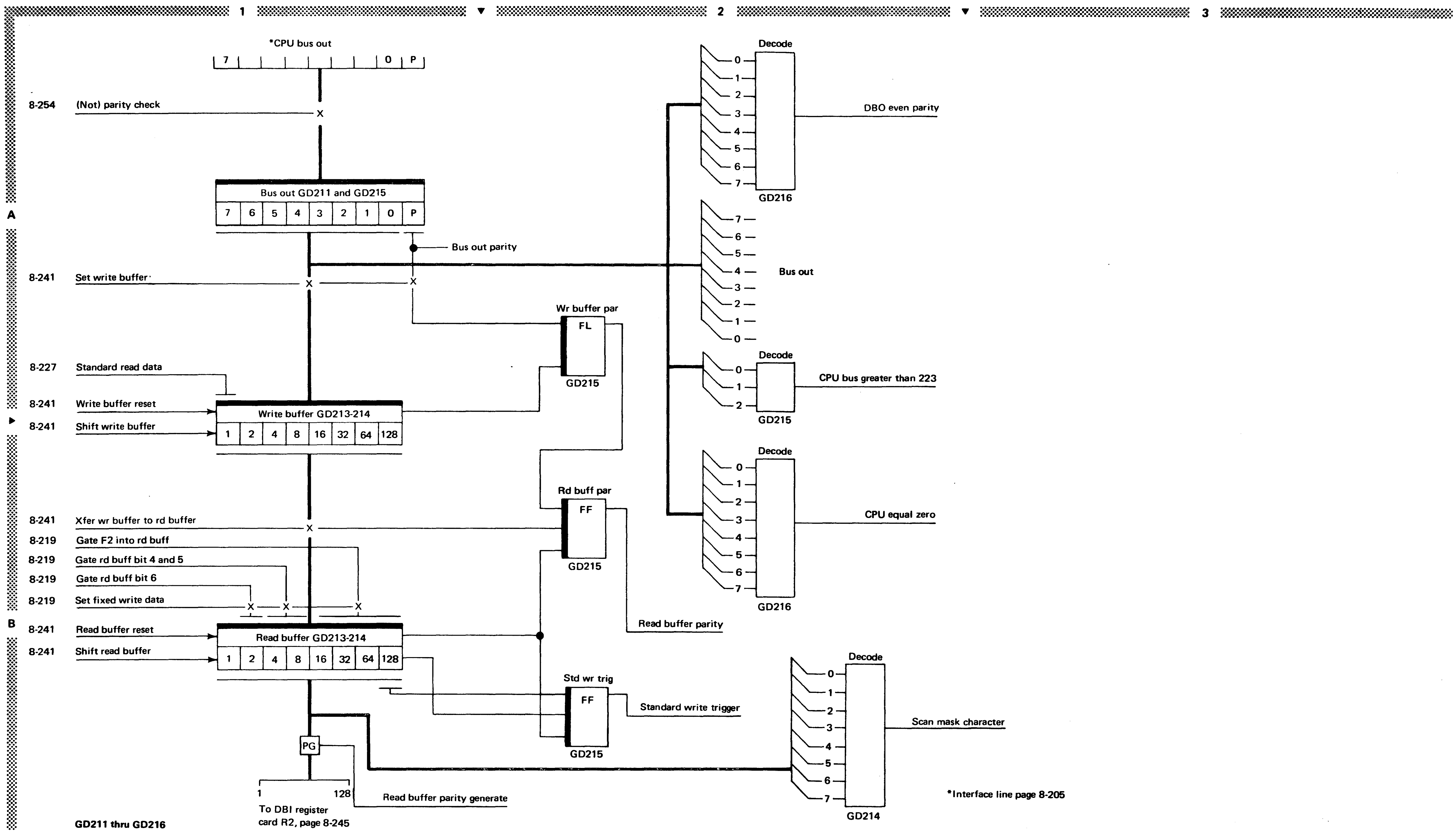
*CPU bus out
8-254 (Not) parity check
Bus out GD211 and GD215
Bus out parity
8-241 Set write buffer
Wr buffer par
FL
GD215
8-227 Standard read data
8-241 Write buffer reset
8-241 Shift write buffer
Write buffer GD213-214
Rd buff par
FF
GD215
8-241 Xfer wr buffer to rd buffer
8-219 Gate F2 into rd buff
8-219 Gate rd buff bit 4 and 5
8-219 Gate rd buff bit 6
8-219 Set fixed write data
8-241 Read buffer reset
8-241 Shift read buffer
Read buffer GD213-214
Read buffer parity
Std wr trig
FF
GD215
Standard write trigger
PG
To DBI register
card R2, page 8-245
Read buffer parity generate
GD211 thru GD216
Decode
GD216
DBO even parity
Bus out
Decode
GD215
CPU bus greater than 223
Decode
GD216
CPU equal zero
Decode
GD214
Scan mask character
*Interface line page 8-205

CARD T2

Card T2 is shown on two pages and contains the following logic:

1. Initial selection
2. Signals for device status
3. I/O conditions A and B
4. I/O attention

Initial Selection

Initial selection prepares the file control unit to start an operation. It contains logic to sample the data bus out (either for normal operation or for diagnostic operation), reject an instruction, return I/O condition A and/or I/O condition B signals, and indicate if the drive requires attention with the I/O attention signal line.

Signals for Device Status

The no-op status latch is set for either of two conditions: 1) when the file control unit cannot execute an instruction due to the file control unit being unsafe, or 2) after a seek operation, there is a seek check and the operation register is holding an instruction to be executed after the seek.

Sense spindle 1 latch is set with a bus out 3 condition which gates the file control unit to sense the drive sensitive status conditions.

I/O Condition A and I/O Condition B

I/O conditions A and B signals indicate the status of the file control unit to the CPU. The CPU interprets the returned I/O conditions A and B combination and can determine if the file control unit can accept or will reject an instruction issued to it.

	I/O Attachment Condition				I/O Condition A	I/O Condition B	CPU Reaction
I–O Cycle of any I/O Instruction	Incorrect DBO Parity				1	1	Processor Check Stop
	Correct DBO Parity	Q Byte not correct			0	0	Processor Check Stop with Q Byte Invalid Check
		Correct Q Byte	SNS Instruction		0	1	Proceed to next sequential instruction
			SIO or LIO Instruction	Reject Instruction	1	0	Retry I/O instruction
				Accept Instruction	0	1	Proceed to next sequential instruction
			TIO or APL Instruction	Condition not met	0	1	Proceed to next sequential instruction
				Condition met	1	0	Branch to effective address
SIO I-R, LIO E-B, & I/O Cycles	Incorrect DBO Parity				1	1	Processor Check Stop
	Correct DBO Parity				0	0	Continue as normal

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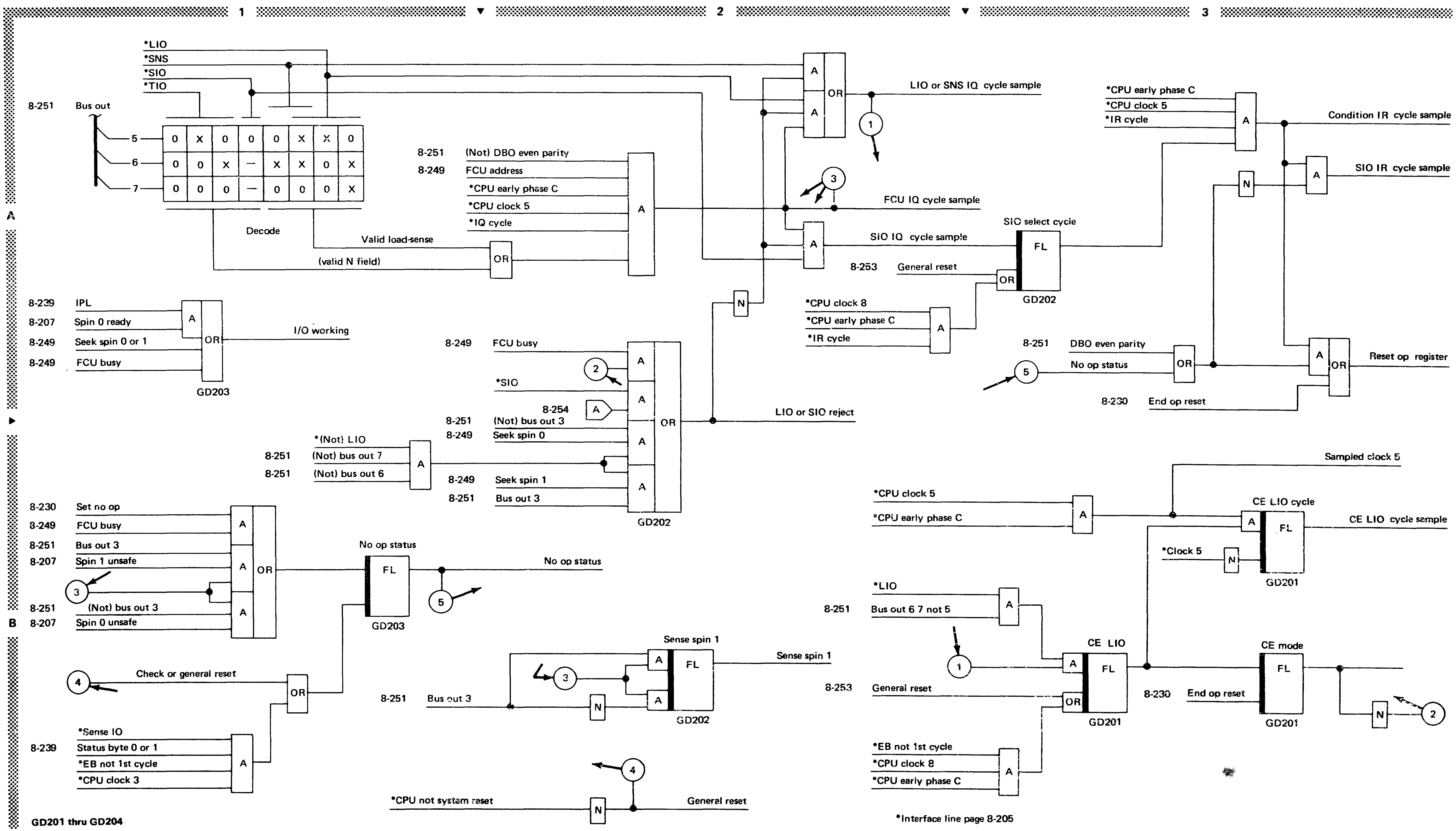
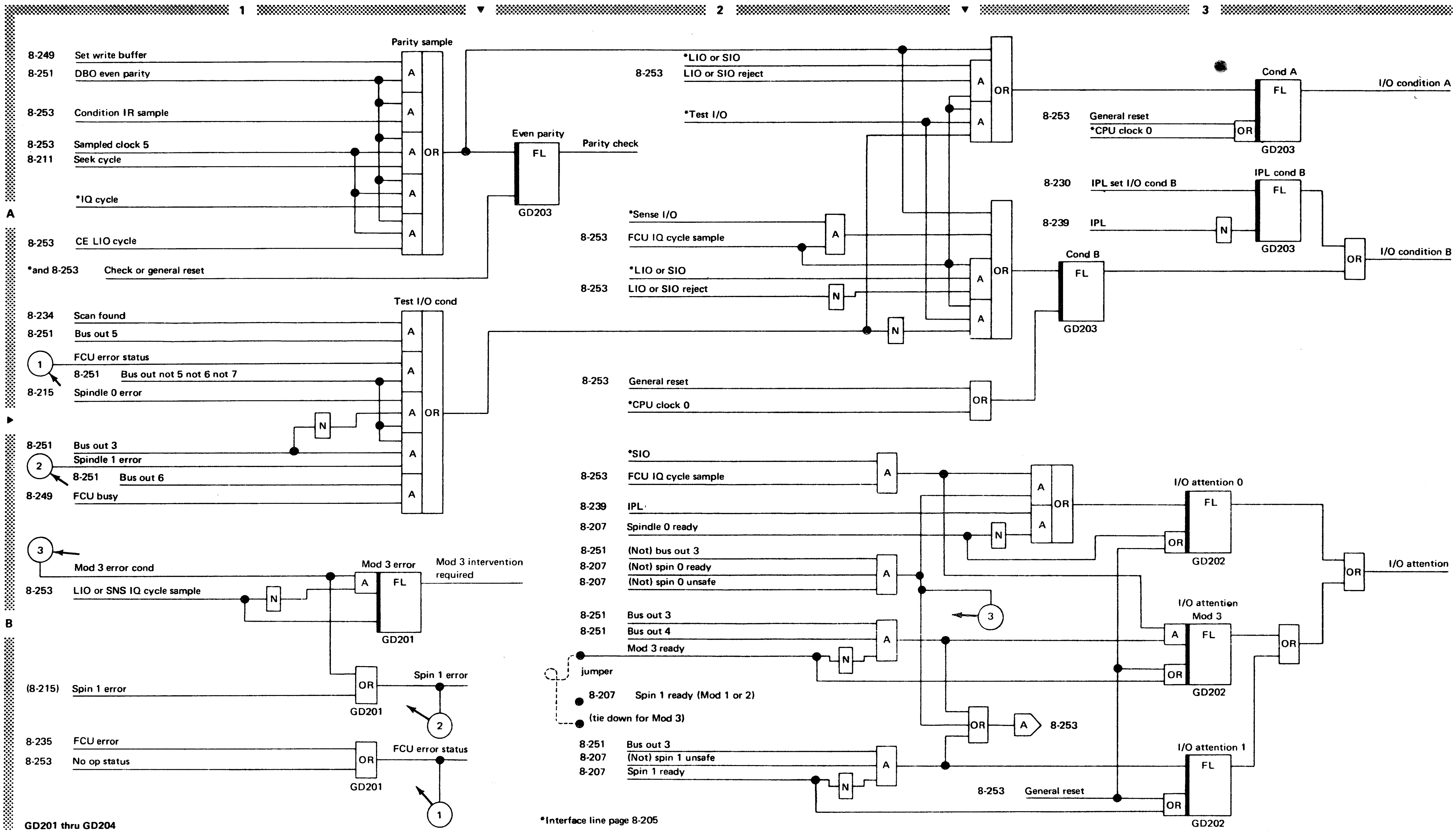
I/O Attention

I/O attention illuminates the disk drive 'I/O attention' indicators on the operator console for the Model 6 or turns off the 'ready' indicator for the Model 10, when the disk drive is not ready or requires attention from the operator.


1
2
3
A
B
*LIO
*SNS
*SIO
*TIO
8-251
Bus out
5
6
7
Decode
Valid load-sense
(valid N field)
8-251
(Not) DBO even parity
8-249
FCU address
*CPU early phase C
*CPU clock 5
*IQ cycle
LIO or SNS IQ cycle sample
FCU IQ cycle sample
SIO IQ cycle sample
SIO select cycle
8-253
General reset
GD202
*CPU clock 8
*CPU early phase C
*IR cycle
*CPU early phase C
*CPU clock 5
*IR cycle
Condition IR cycle sample
SIO IR cycle sample
8-251
DBO even parity
No op status
Reset op register
8-230
End op reset
8-239
IPL
8-207
Spin 0 ready
8-249
Seek spin 0 or 1
8-249
FCU busy
I/O working
GD203
8-249
FCU busy
*SIO
8-254
8-251
(Not) bus out 3
8-249
Seek spin 0
LIO or SIO reject
*(Not) LIO
8-251
(Not) bus out 7
8-251
(Not) bus out 6
8-249
Seek spin 1
8-251
Bus out 3
GD202
8-230
Set no op
8-249
FCU busy
8-251
Bus out 3
8-207
Spin 1 unsafe
8-251
(Not) bus out 3
8-207
Spin 0 unsafe
No op status
No op status
GD203
Check or general reset
*Sense IO
8-239
Status byte 0 or 1
*EB not 1st cycle
*CPU clock 3
Sense spin 1
Sense spin 1
8-251
Bus out 3
GD202
*CPU not system reset
General reset
Sampled clock 5
*CPU clock 5
*CPU early phase C
CE LIO cycle
CE LIO cycle sample
*Clock 5
GD201
*LIO
8-251
Bus out 6 7 not 5
CE LIO
8-253
General reset
GD201
CE mode
8-230
End op reset
GD201
*EB not 1st cycle
*CPU clock 8
*CPU early phase C
*Interface line page 8-205
GD201 thru GD204


1
2
3
A
B
8-249 Set write buffer
8-251 DBO even parity
8-253 Condition IR sample
8-253 Sampled clock 5
8-211 Seek cycle
*IQ cycle
8-253 CE LIO cycle
*and 8-253 Check or general reset
Parity sample
Even parity
FL
GD203
Parity check
8-234 Scan found
8-251 Bus out 5
FCU error status
8-251 Bus out not 5 not 6 not 7
8-215 Spindle 0 error
8-251 Bus out 3
Spindle 1 error
8-251 Bus out 6
8-249 FCU busy
Test I/O cond
Mod 3 error cond
8-253 LIO or SNS IQ cycle sample
Mod 3 error
GD201
Mod 3 intervention required
(8-215) Spin 1 error
Spin 1 error
8-235 FCU error
8-253 No op status
FCU error status
GD201 thru GD204
*LIO or SIO
8-253 LIO or SIO reject
*Test I/O
*Sense I/O
8-253 FCU IQ cycle sample
*LIO or SIO
8-253 LIO or SIO reject
Cond A
8-253 General reset
*CPU clock 0
I/O condition A
8-230 IPL set I/O cond B
IPL cond B
8-239 IPL
I/O condition B
Cond B
8-253 General reset
*CPU clock 0
*SIO
8-253 FCU IQ cycle sample
8-239 IPL
8-207 Spindle 0 ready
8-251 (Not) bus out 3
8-207 (Not) spin 0 ready
8-207 (Not) spin 0 unsafe
8-251 Bus out 3
8-251 Bus out 4
Mod 3 ready
jumper
8-207 Spin 1 ready (Mod 1 or 2)
(tie down for Mod 3)
8-251 Bus out 3
8-207 (Not) spin 1 unsafe
8-207 Spin 1 ready
8-253
I/O attention 0
GD202
I/O attention
I/O attention Mod 3
I/O attention 1
8-253 General reset
*Interface line page 8-205

A

▶

B

INTRODUCTION TO OPERATIONS

This chapter contains detailed flowcharts and timing charts of the operations performed by the disk attachment.

Flowcharts

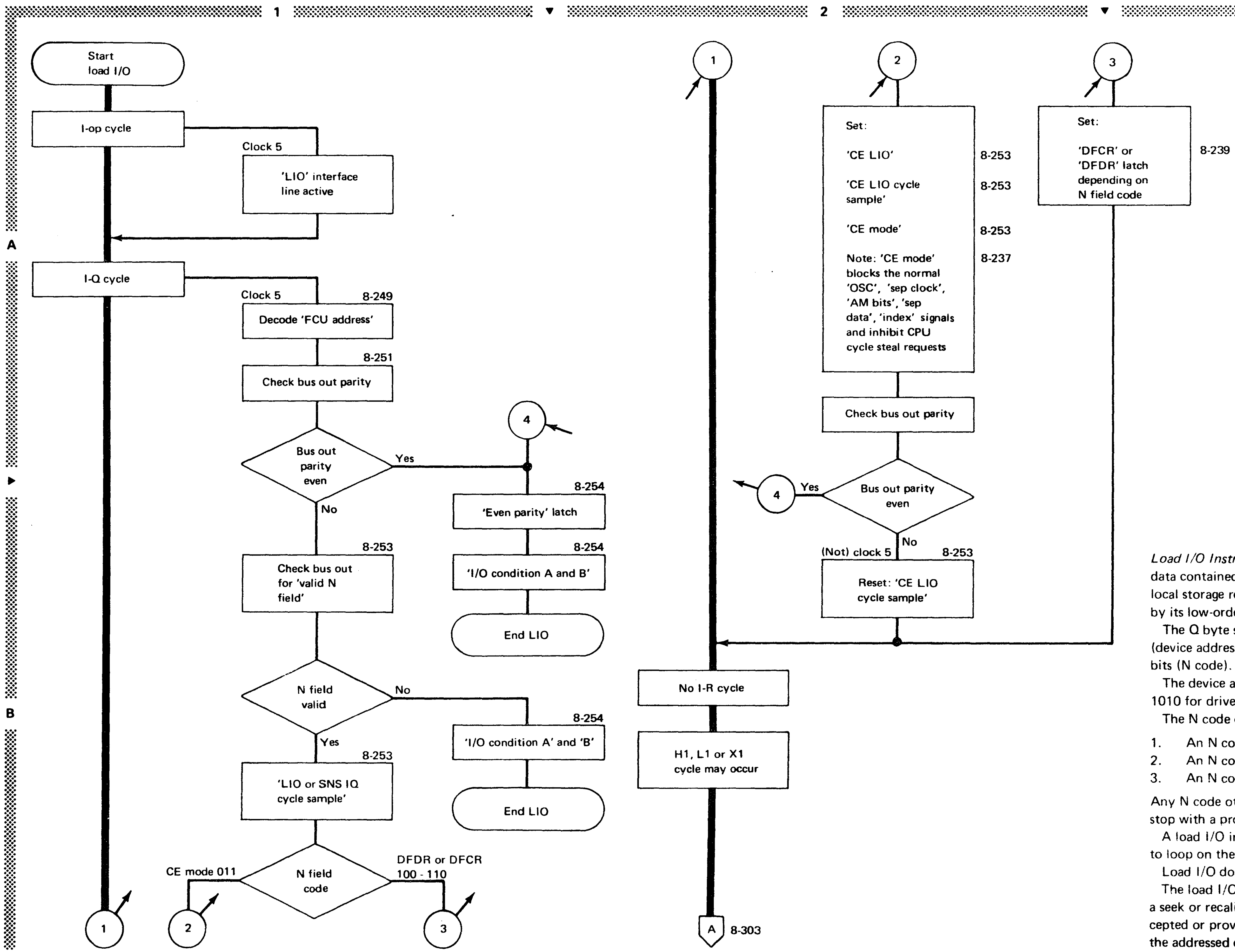
The flowcharts contain three levels of information. By reading down the heavy dark lines, the reader can learn the major objectives of the operation. The second level of information is obtained by reading the information in the boxes that branch off the heavy dark line. The information that is contained in each block in a heavy dark line is explained in the blocks that branch off from it. The third level of information is contained in the note blocks (open ended blocks) that branch off the second level blocks. Information in these blocks is intended to explain why an action has been performed.

The page references next to the blocks refer to the second level diagrams in chapter 2. A clock time to the side of a block, indicates the CPU time that causes the action described in the block.

Timing Charts

The timing charts in this chapter are to be used to supplement the information found in the flowcharts and the second level diagrams in chapter 2.

The numbers at the start or ending of a signal line in the timing chart refer to the number at the left hand side of the timing chart. This reference indicates the signal, or signals, that caused the desired line name to become active or inactive. Line references are for individual timing charts (signal line numbers are not the same from chart to chart).



Load I/O Instruction Operation: This instruction loads the two bytes of data contained in the operand addressed by the operand address into a local storage register specified by the Q byte. The operand is addressed by its low-order byte.

The Q byte specifies the drive that is to operate in the first four bits (device address) and the local storage register to be loaded in the last three bits (N code). The M bit is not used.

The device address portion of the Q byte can take either of two values: 1010 for drive 1, or 1011 for drive 2.

The N code can specify only three values:

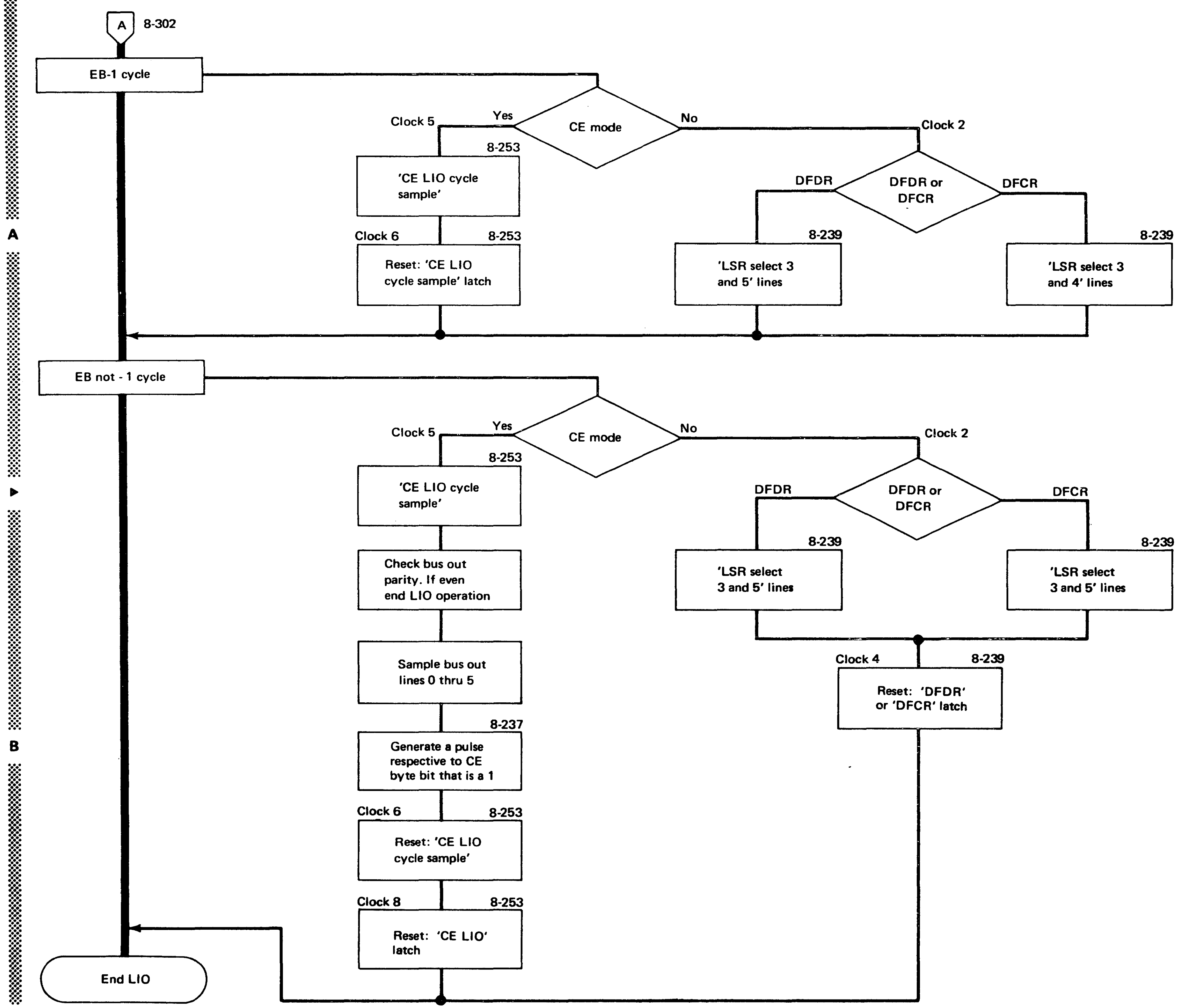
1. An N code of 011 is for customer engineer use.
2. An N code of 100 specifies the disk file data address register.
3. An N code of 110 specifies the disk file control address register.

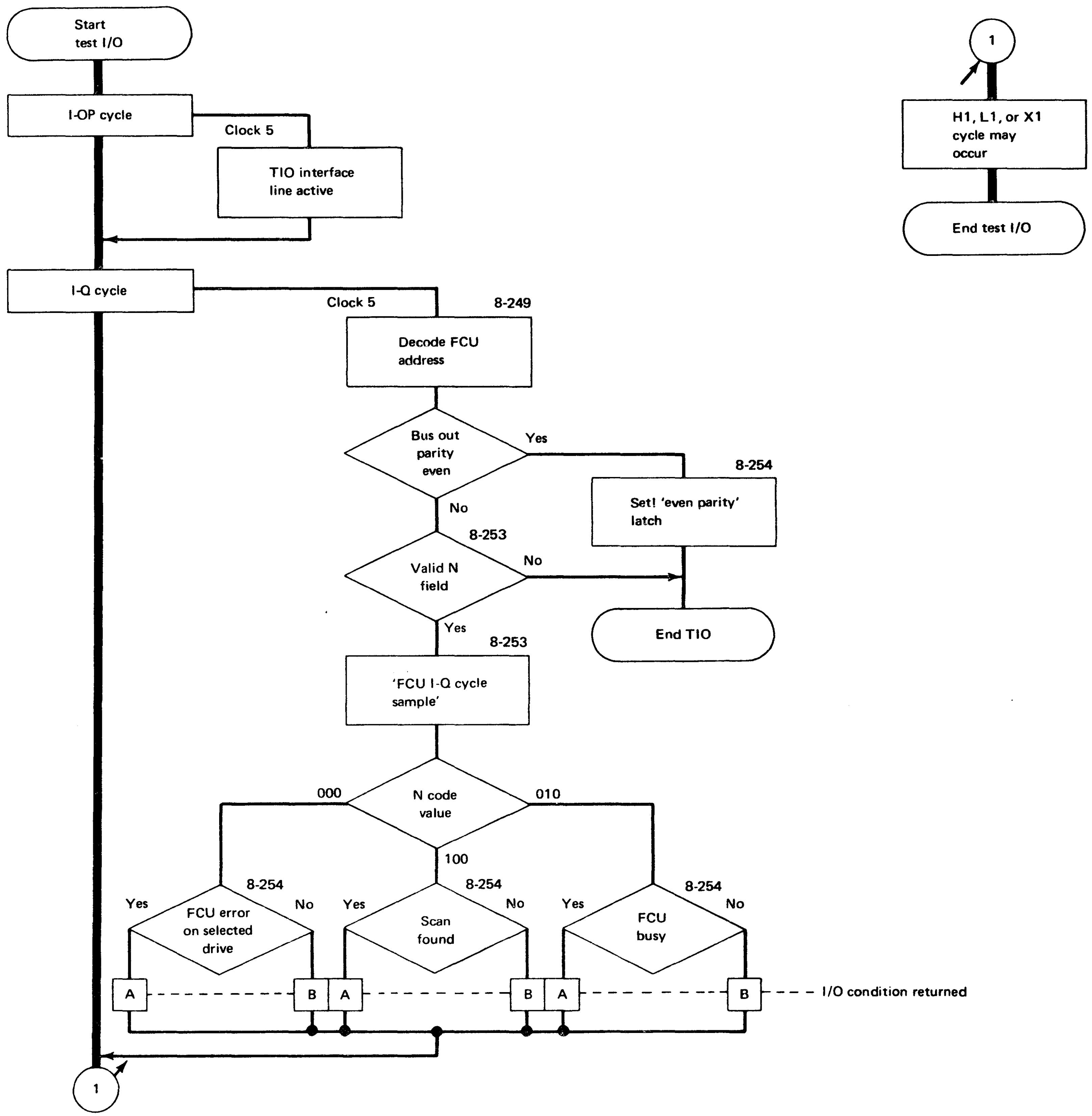
Any N code other than the ones specified causes the processing unit to stop with a processor check and an invalid-Q-byte indication.

A load I/O instruction issued to a busy control unit causes the program to loop on the load I/O instruction until the control unit is no longer busy.

Load I/O does not set any file status conditions.

The load I/O instruction is executed if the addressed drive is executing a seek or recalibrate operation and a read, write, or scan has not been accepted or provisionally accepted. The load I/O instruction is executed if the addressed drive is not ready.


A 8-302
EB-1 cycle
CE mode
Yes
No
Clock 5
8-253
'CE LIO cycle sample'
Clock 6
8-253
Reset: 'CE LIO cycle sample' latch
Clock 2
DFDR or DFCR
DFDR
DFCR
8-239
'LSR select 3 and 5' lines
8-239
'LSR select 3 and 4' lines
EB not - 1 cycle
CE mode
Yes
No
Clock 5
8-253
'CE LIO cycle sample'
Check bus out parity. If even end LIO operation
Sample bus out lines 0 thru 5
8-237
Generate a pulse respective to CE byte bit that is a 1
Clock 6
8-253
Reset: 'CE LIO cycle sample'
Clock 8
8-253
Reset: 'CE LIO' latch
Clock 2
DFDR or DFCR
DFDR
DFCR
8-239
'LSR select 3 and 5' lines
8-239
'LSR select 3 and 5' lines
Clock 4
8-239
Reset: 'DFDR' or 'DFCR' latch
End LIO



Test I/O Instruction Operation: This instruction tests for the conditions specified in the Q byte. If the condition tested for is present, the next instruction is taken from the storage address specified by the operand address and the address of the next sequential instruction is placed in the address recall register. If the condition is not present, the next sequential instruction is executed and the address contained in the operand address is stored in the address recall register. The information stored in the address recall register remains there until the next decimal, insert-and-test-characters, or branch instruction is executed.

The Q byte specifies the drive to be tested and the conditions to be tested for. The device address portion of the Q byte specifies the drive to be tested and can take on two values: hexadecimal A indicating drive 1 and hexadecimal B indicating drive 2.

The N code of the Q byte can specify testing for any of three conditions:

1. N code 000–(not ready/check) indicates that the drive is not in condition to operate or that a check condition has been detected. A check condition is indicated when either drive is addressed if the following device status is present.

   Data check
   Track condition check
   Missing address marker
   End of cylinder
   No record found
   Equipment check not caused by unsafe
   No-op
   Overrun

   A check condition is also indicated if a seek check or unsafe exists for the addressed drive. A seek check or an unsafe for the drive not addressed will not be indicated. The drive that has the check condition can be determined from the status byte.
2. N code 010–(busy) control unit either is executing a read, write, or scan operation or has provisionally accepted one of these operations for execution at the end of the seek operation in progress.
3. N code 100–(scan found) indicated when either drive is addressed. The sense byte indicates which drive contains the scan found condition. The scan found indication is reset by the next start I/O instruction.

Any N code other than those listed causes the processing unit to come to processor check stop with an invalid-Q-byte indication.

The M bit is not used except when addressing the second drive because it is possible that the fixed disk is not installed. Addressing an uninstalled fixed disk results in a not ready indication.

Sense I/O Instruction Operation: This instruction causes the two bytes contained in the specified local storage register or the specified two bytes of status information to be transferred to the two-byte field in storage addressed by the operand address. The operand is addressed by the low-order byte.

The Q byte specifies the drive to be sensed and the register or status bytes to be transferred. The device address portion of the Q byte specifies the drive to be sensed. The device address can be either of two hexadecimal values: A specifies drive 1, and B specifies drive 2. The N code specifies what is to be transferred to storage as follows:

1. N code 010–status bytes 0 and 1
2. N code 011–status bytes 2 and 3
3. N code 100–disk file data address register
4. N code 110–disk file control address register

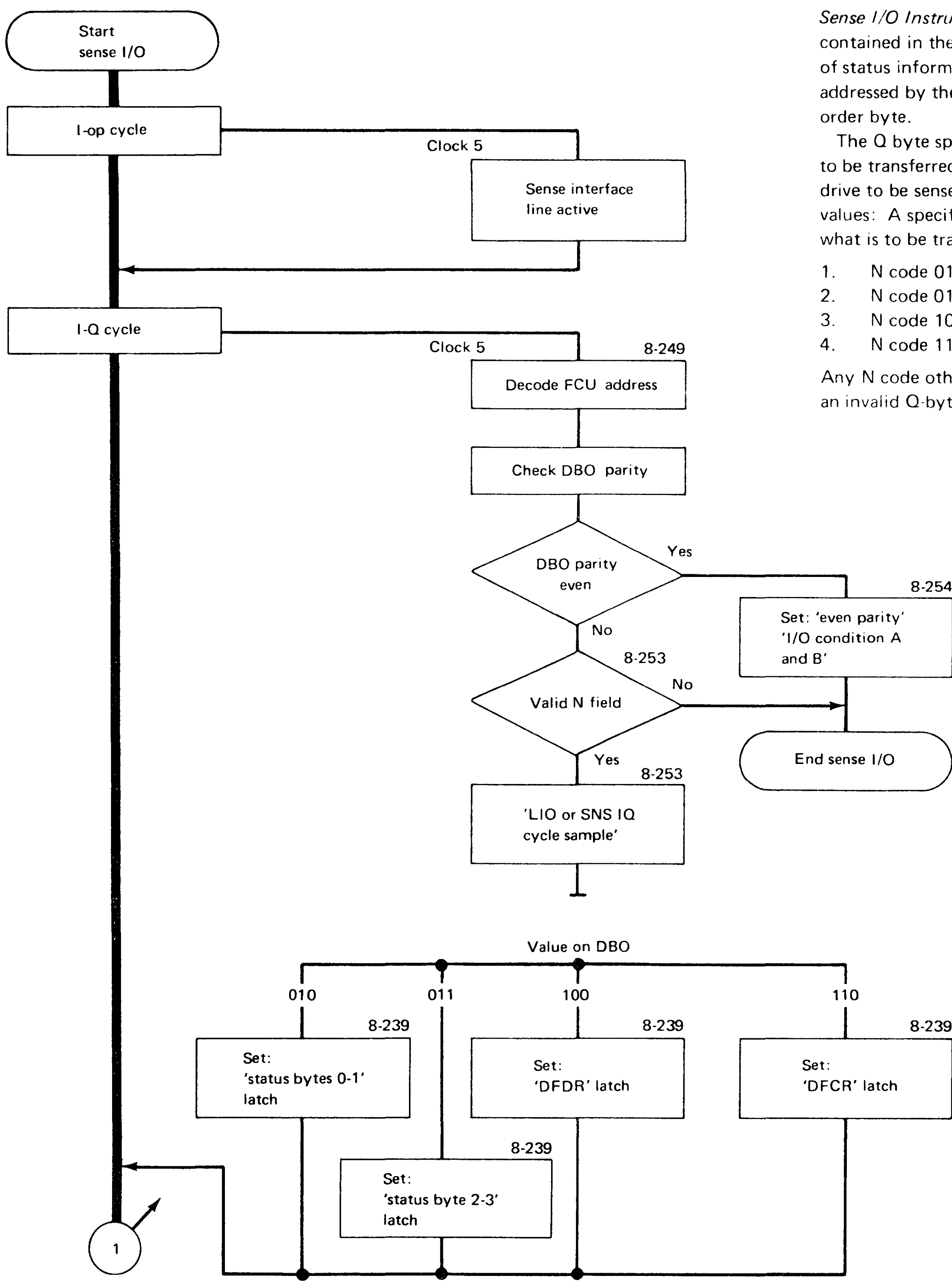
Any N code other than those specified causes a processor check stop with an invalid Q-byte indication.

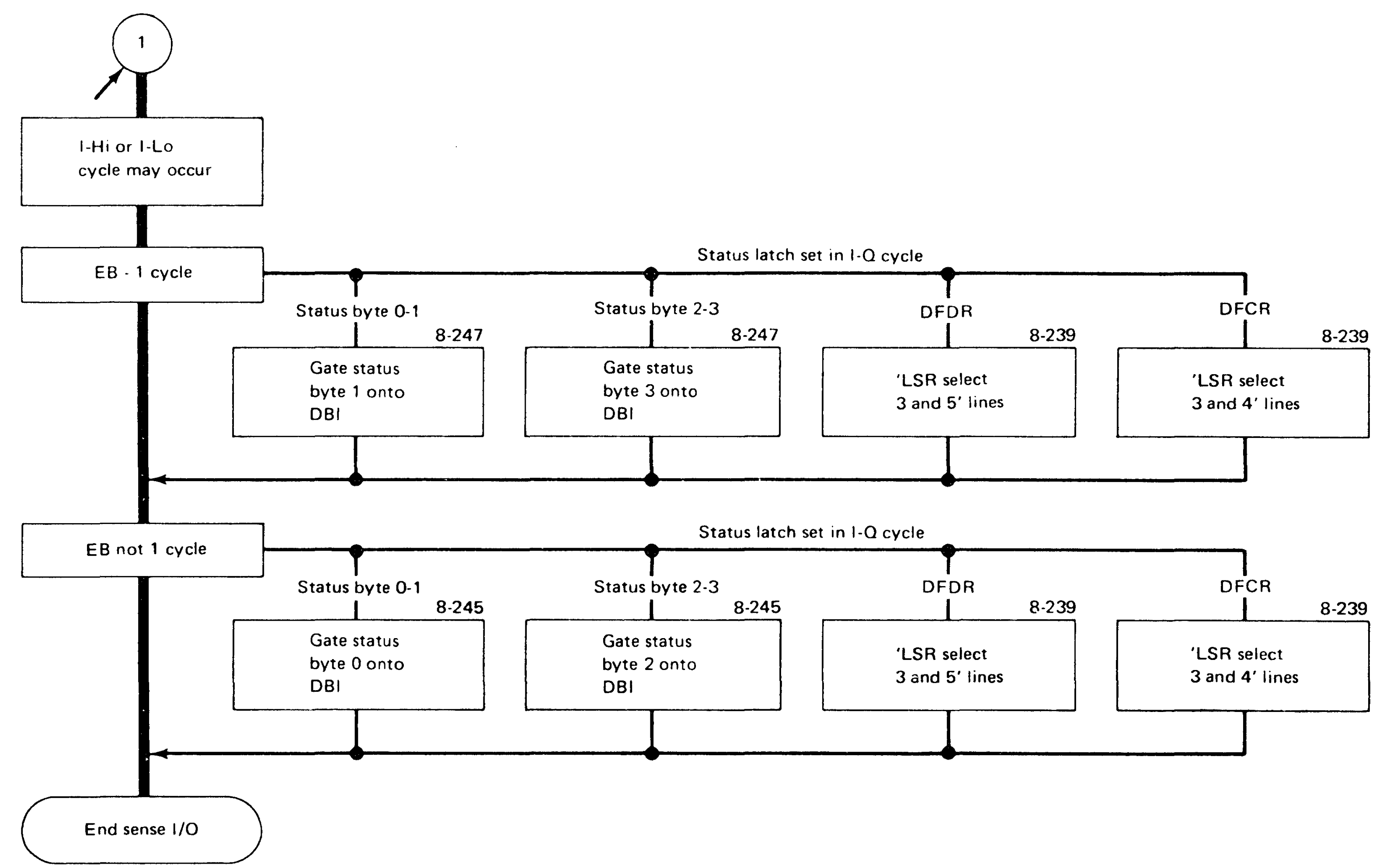
The M bit is used in this instruction to determine if the intervention required status bit will be set if the second drive is addressed and the fixed disk is not installed.

The sense I/O instruction will be accepted by the file control unit no matter what other operations are in progress at the time.

Some bits of the status bytes are drive sensitive to the sense I/O instruction. Equipment check caused by unsafe, cylinder 0, seek check, seek busy, intervention required, unsafe, head settling, and index are set in the status bytes only when they apply to the drive addressed by the sense I/O instruction. These bits, if they can be reset, are reset by the same sense I/O instruction that transfers them to storage.

All remaining status bits are presented with the status bytes to a sense I/O for either drive. All status bits except no-op are reset by the next start I/O instruction issued to either drive. No-op is reset by the sense I/O instruction to either drive that transfers it to storage.





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INITIAL PROGRAM LOAD

The initial program load is a disk read operation, started by the program load switch. A second switch, disk select, determines which disk in drive 1 data is to be read from. Sector zero data field on the selected disk is read and transferred into core storage starting at address 0000. When the 256 byte data field is read, the central processing unit starts processing at core location 0000.

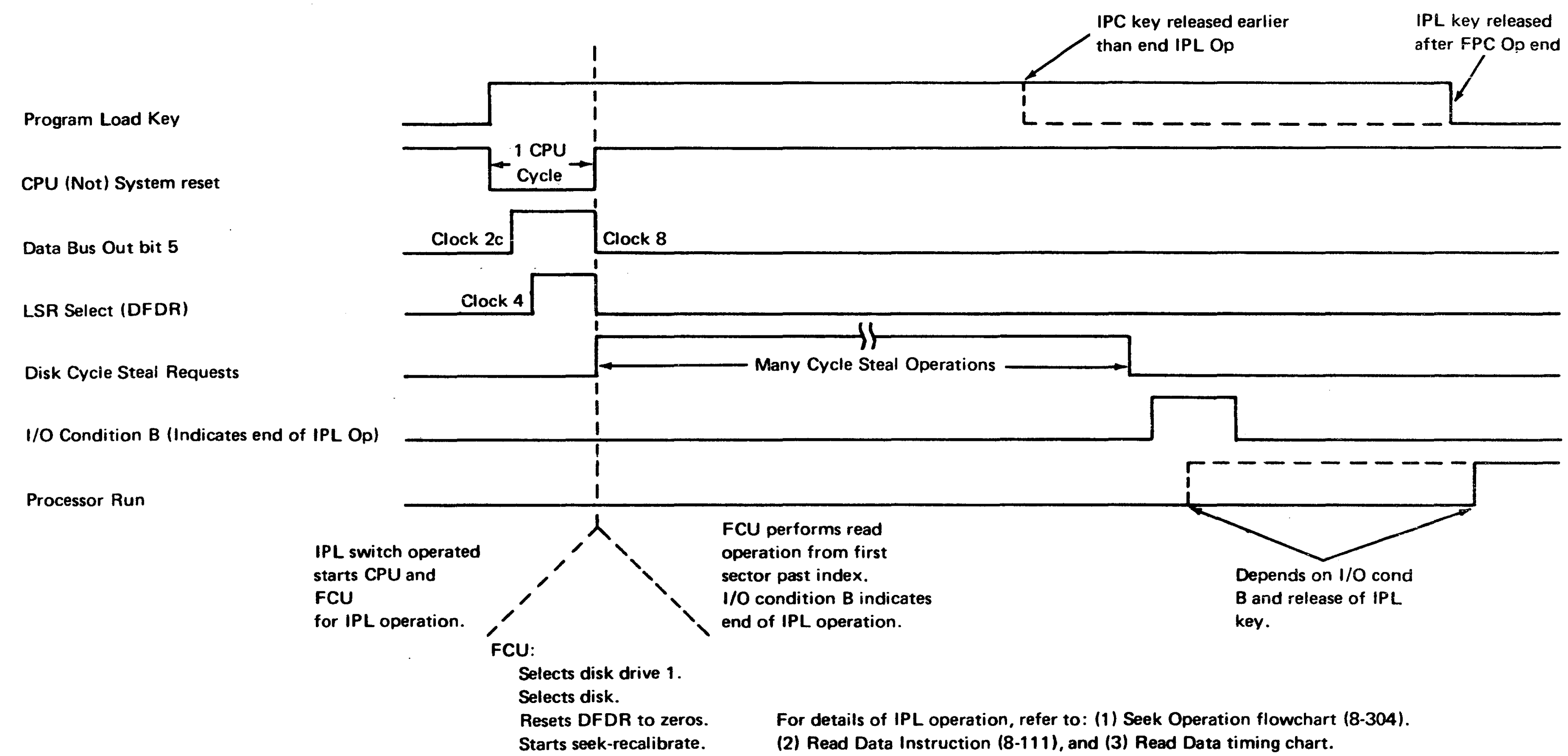
An initial program load is accomplished as follows:

1. The program load selector is set either to the fixed disk or removable disk position to select the disk to IPL from.
2. Operate the program load switch to start the IPL operation.

The program load switch starts a CPU system reset and activates DBO 5. One CPU machine cycle is started to reset the IAR to 0000. DBO 5 and system reset is sent to the file control unit and is a signal to start an IPL operation. An IPL operation:

1. Selects disk drive 1 (spindle 0).
2. Selects the disk determined by the program load selector and head 0.
3. Selects the DFDR and resets it to 0000.
4. Starts a seek recalibrate operation to position the read heads to cylinder zero.

When the seek operation is complete and the head settle time has ended, the file control unit starts a read operation on the first sector after index. This read operation is exactly like a start I/O instruction read data operation except that the sector ID field is not compared to the disk control field in core. Two hundred fifty-six data bytes are read, each byte is transferred to the CPU with a cycle steal request (I/O cycle). At the end of the data field, the file control unit activates I/O condition B to signal the CPU to start processing at core location 0000. If I/O condition B is activated before the program load switch is released, the CPU waits until the switch is released before starting to process.



For details of IPL operation, refer to: (1) Seek Operation flowchart (8-304). (2) Read Data Instruction (8-111), and (3) Read Data timing chart.

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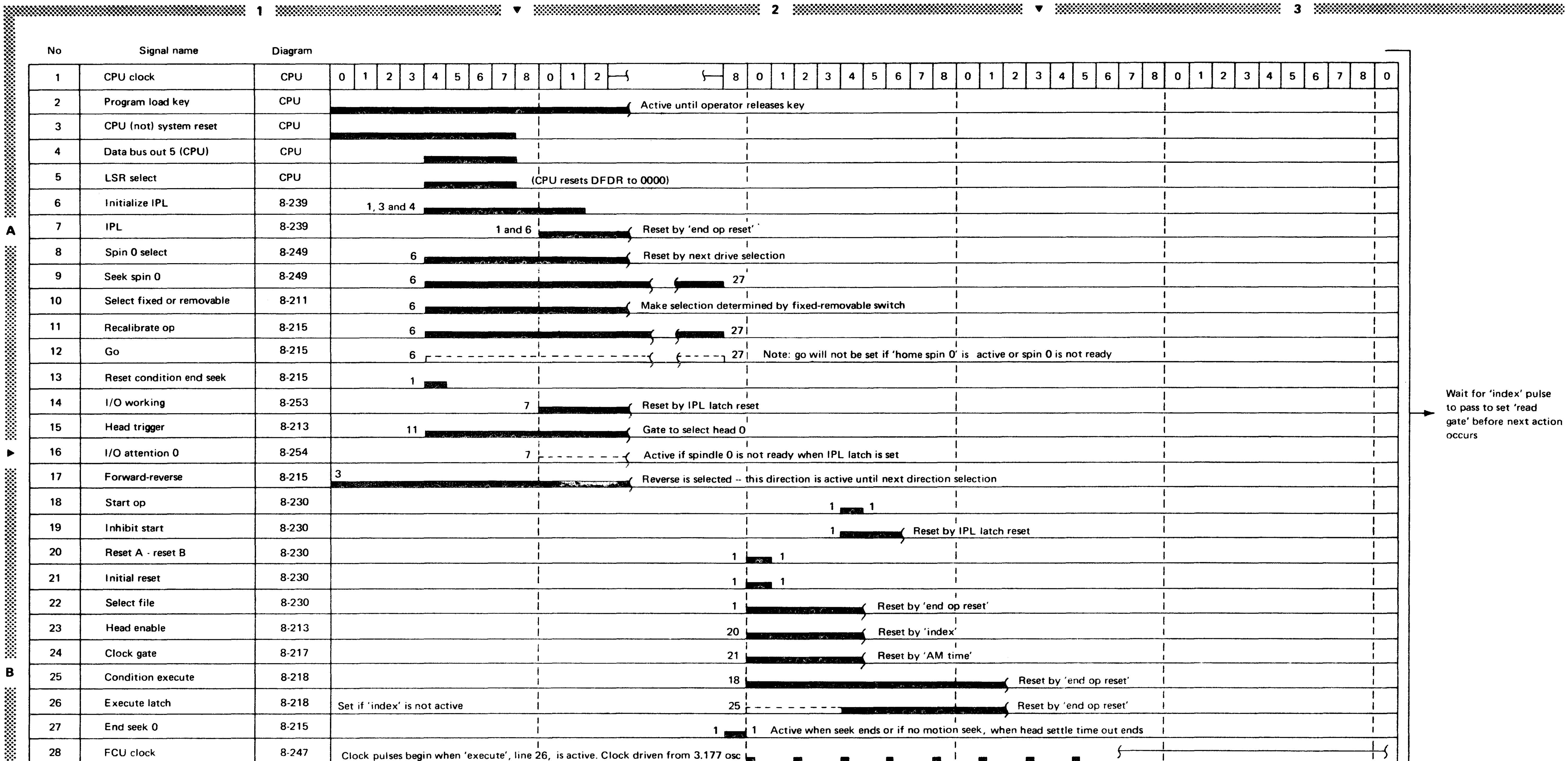
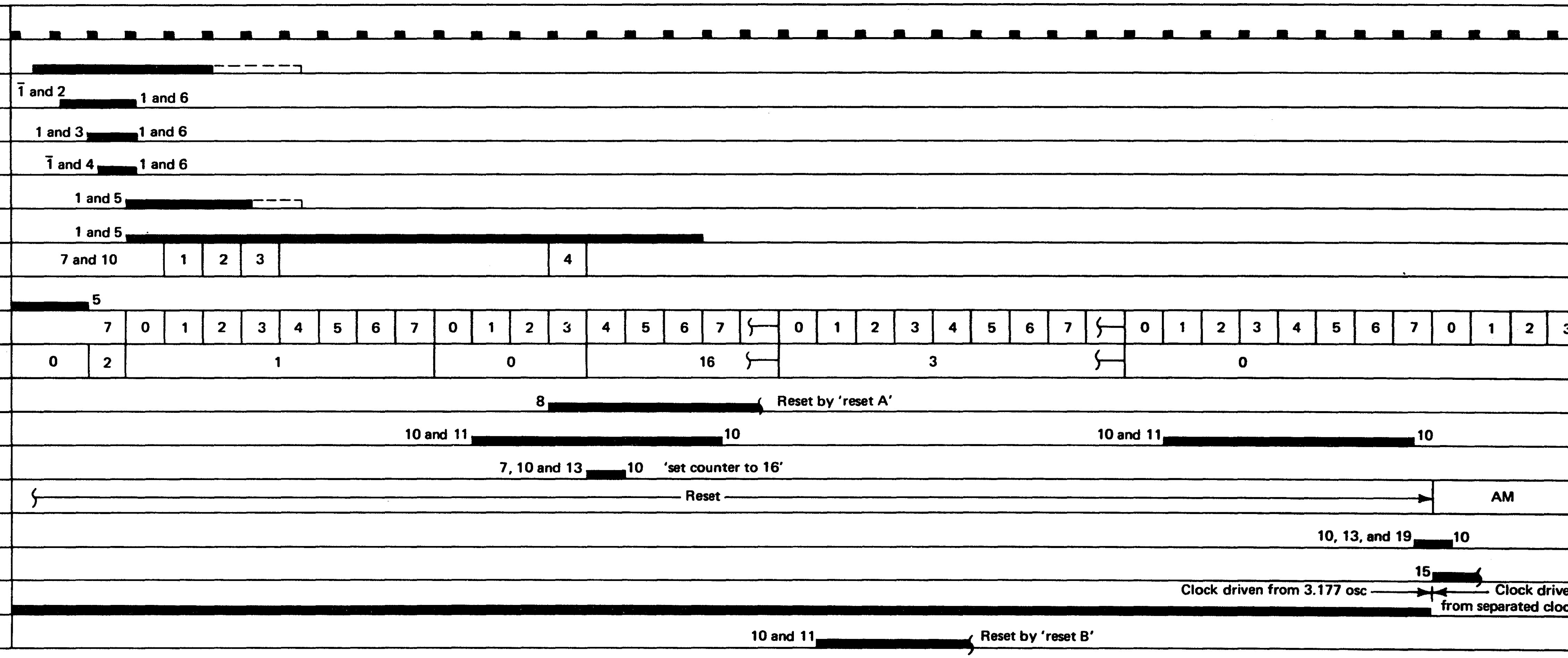


Program load key is operated, FCU sets up for IPL operation, then waits for index to continue

1 ▼ 2 ▼ 3

A

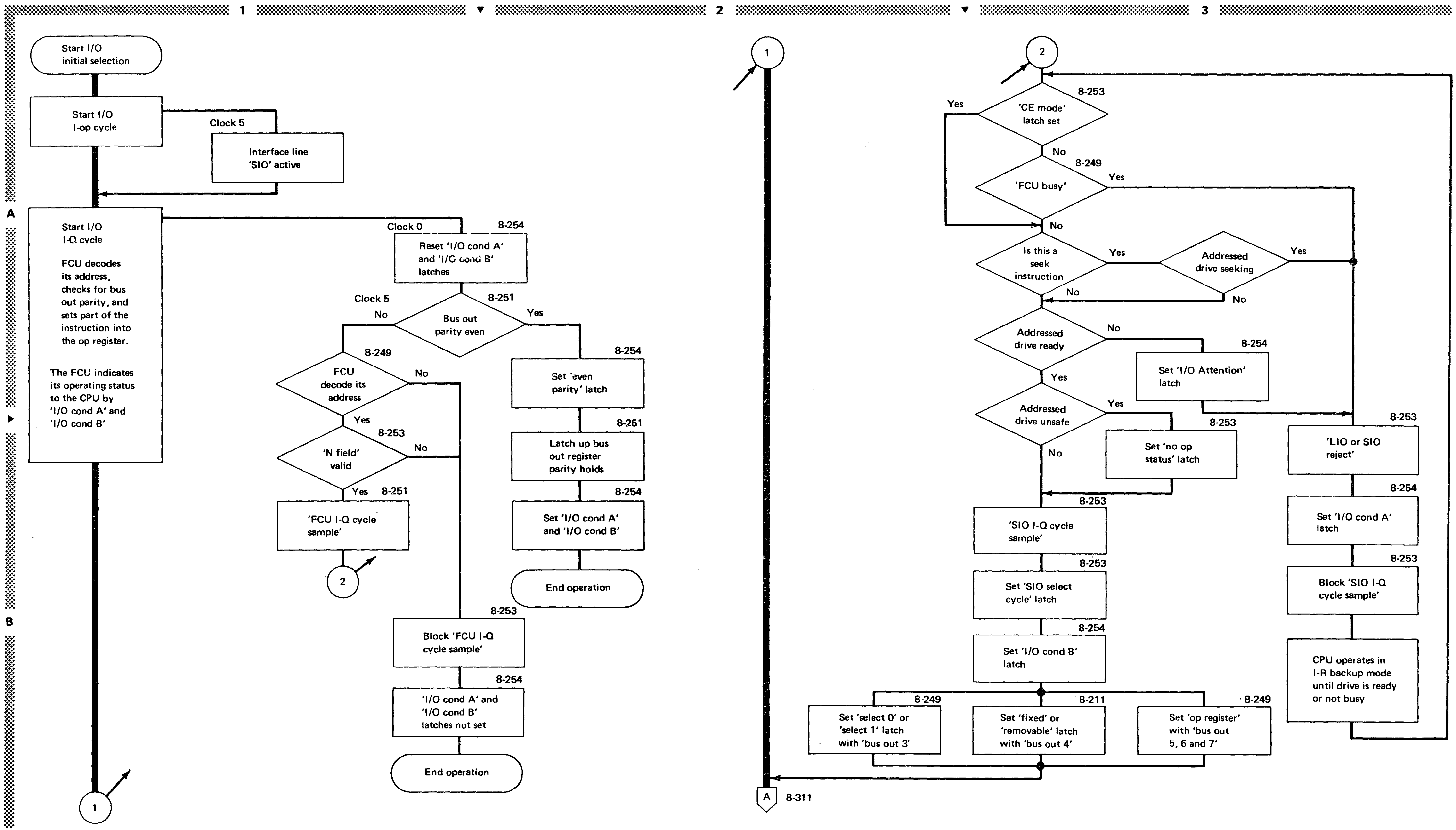
No	Signal name	Diagram
1	FCU clock	8-247
2	Raw index	8-218
3	Pre index condition	8-218
4	Condition standard index	8-218
5	Standard index	8-218
6	Condition index reset	8-218
7	Index time	8-218
8	Index times 1 through 4	8-218
9	Bit ring inhibit	8-227
10	Bit ring (starts at 7)	8-227
11	Control counter	8-223
12	Read gate	8-217
13	Count zero gate	8-223
14	Counter set	8-223
15	Cycle control ring	8-221
16	CCR advance gate	8-221
17	Condition first AM	8-221
18	Clock gate	8-218
19	Pre advance gate	8-221

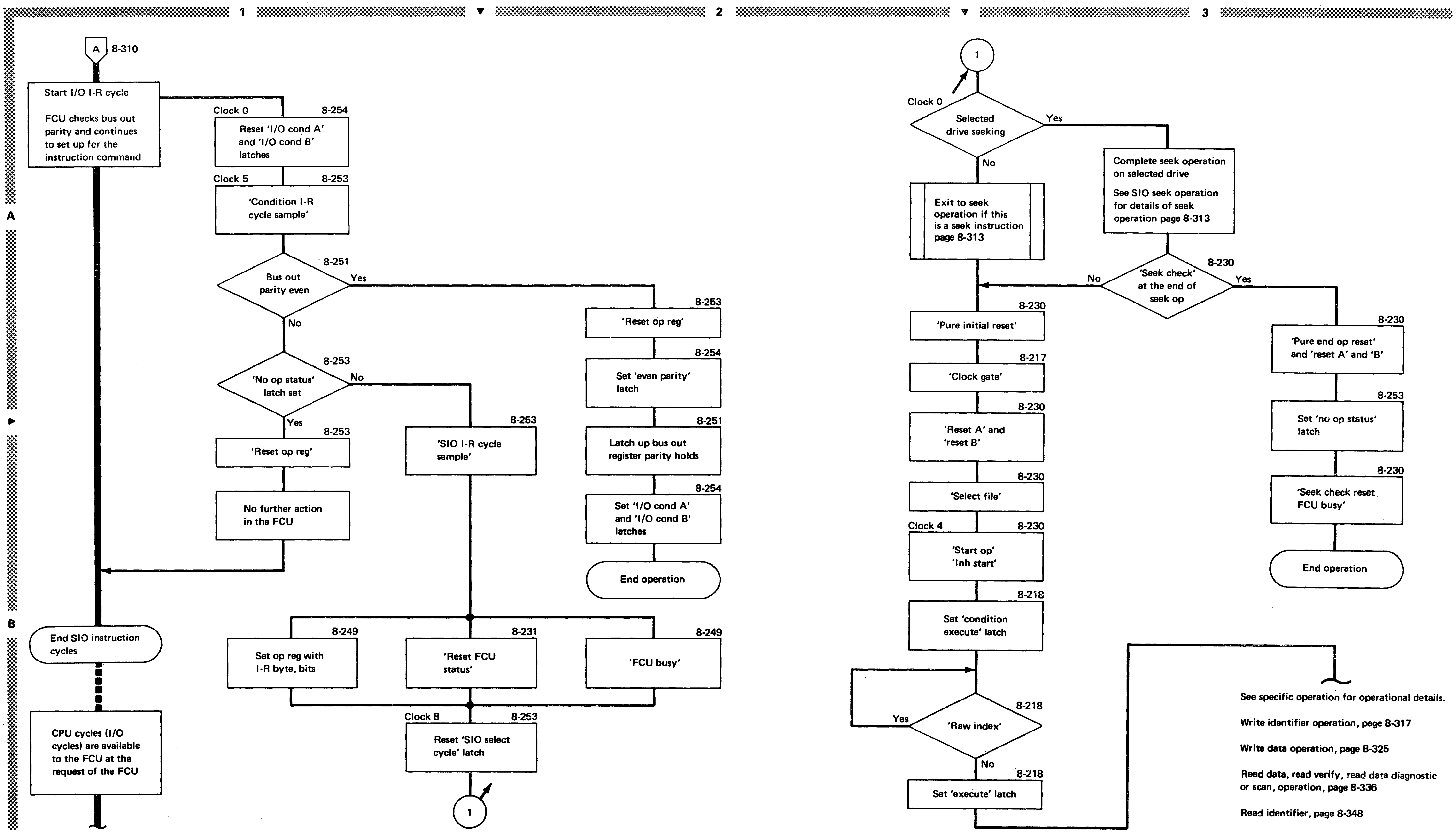


Sense 'index', set 'read gate', then wait for zeros and address mark detect to continue

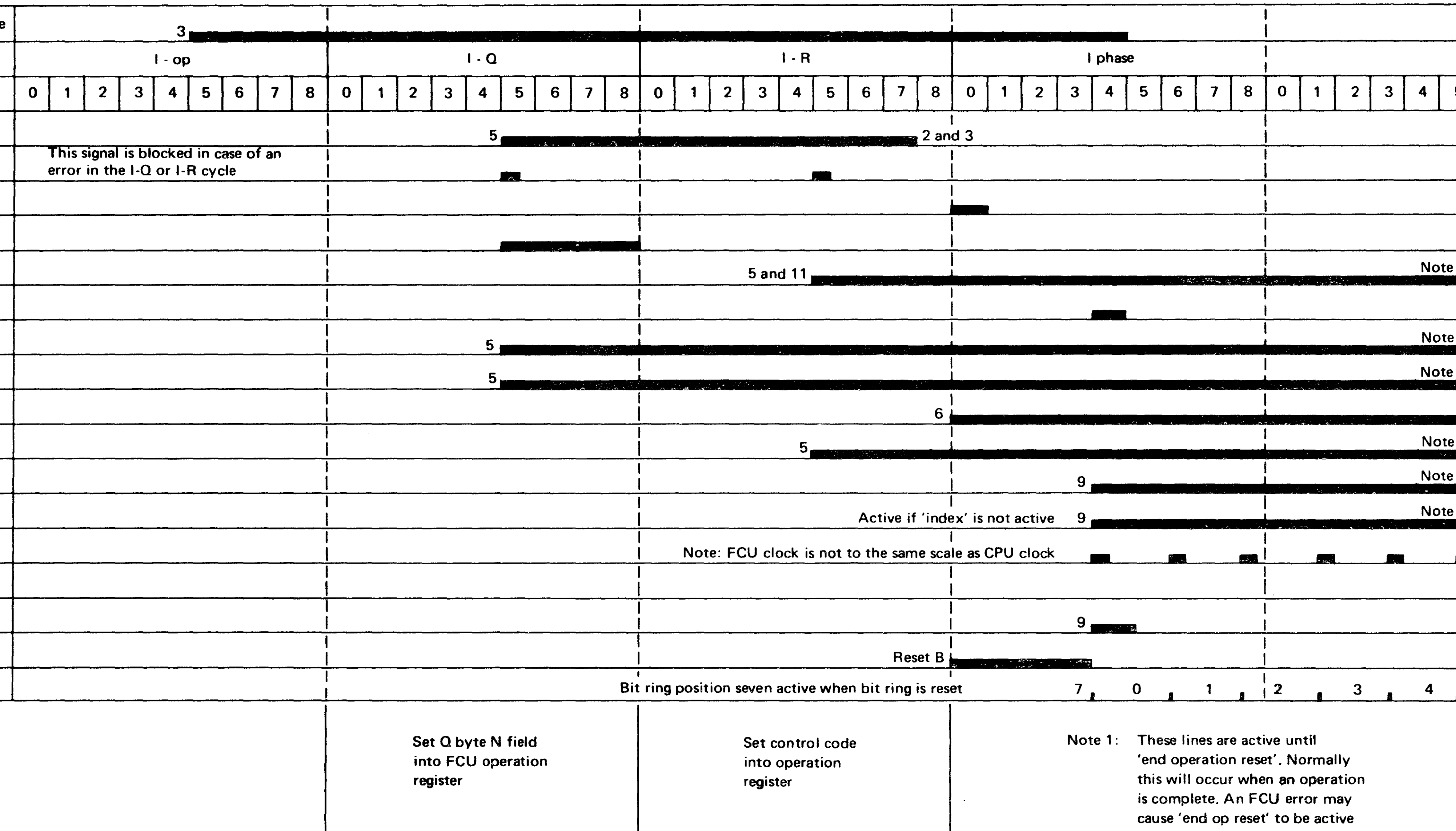
B

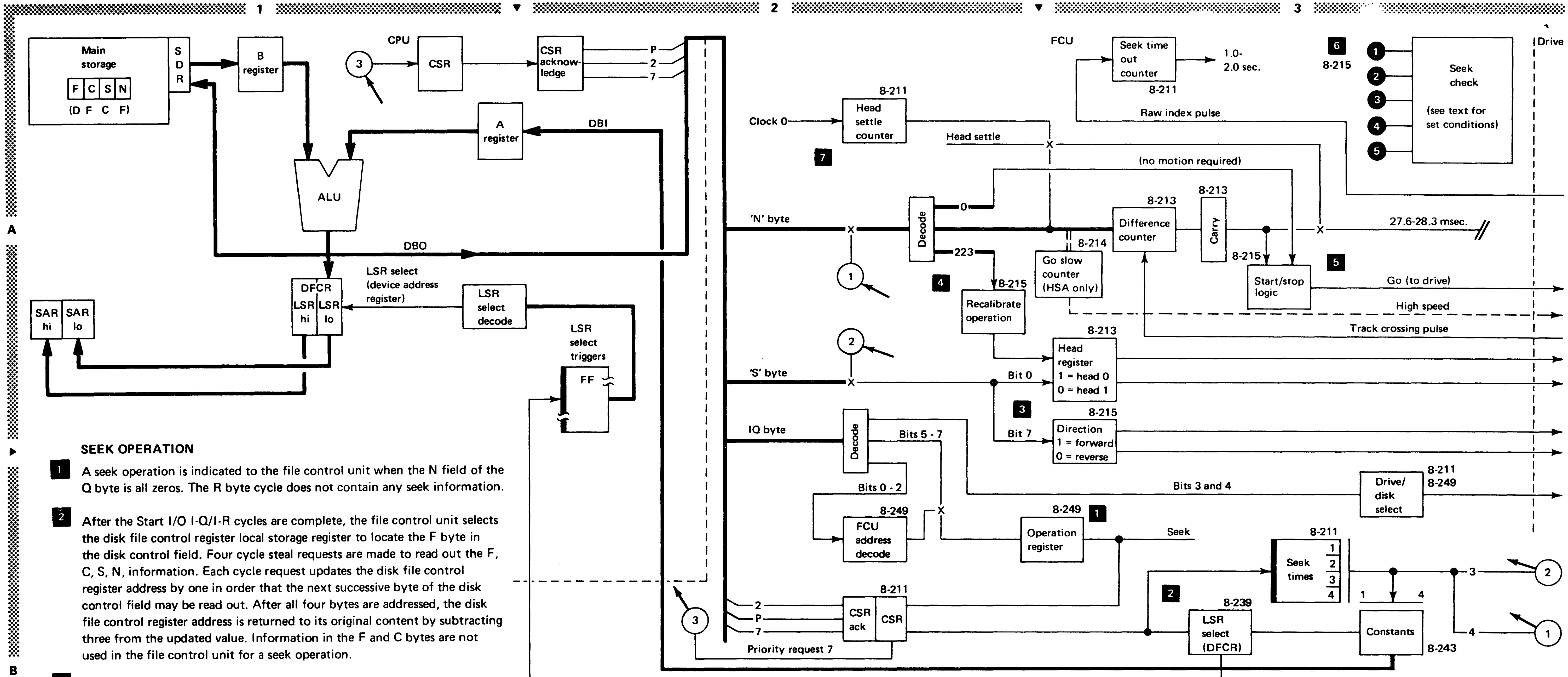
Wait for 'zeros detect' and address mark detect. When an address mark is detected the FCU continues to read the ID field, however no ID compare with the disk control field is made	The FCU cycles through the ID field. When the cycle control ring reaches data time, the FCU starts to read data and sends it to the CPU to be stored at the DFDR address. Note: see read data operation for details of read data field	At post data time, counter decode 1 and bit ring 7 time, (this condition occurs at the end of post data time) 'pure end op reset' is active to deselect the drive and reset the 'IPL' latch	'IPL set I/O condition B' is active and indicates the end of the IPL operation to the CPU. The CPU starts processing at core location 0000


1
2
3
A
B
Start I/O
initial selection
Start I/O
I-op cycle
Clock 5
Interface line
'SIO' active
Start I/O
I-Q cycle
FCU decodes
its address,
checks for bus
out parity, and
sets part of the
instruction into
the op register.
The FCU indicates
its operating status
to the CPU by
'I/O cond A' and
'I/O cond B'
Clock 0
8-254
Reset 'I/O cond A'
and 'I/O cond B'
latches
Clock 5
8-251
No
Bus out
parity even
Yes
8-249
FCU
decode its
address
No
Yes
8-253
'N field'
valid
No
Yes
8-251
'FCU I-Q cycle
sample'
2
8-254
Set 'even
parity' latch
8-251
Latch up bus
out register
parity holds
8-254
Set 'I/O cond A'
and 'I/O cond B'
End operation
8-253
Block 'FCU I-Q
cycle sample'
8-254
'I/O cond A' and
'I/O cond B'
latches not set
End operation
1
1
2
8-253
Yes
'CE mode'
latch set
No
8-249
Yes
'FCU busy'
No
Is this a
seek
instruction
Yes
Addressed
drive seeking
Yes
No
No
Addressed
drive ready
No
8-254
Set 'I/O Attention'
latch
Yes
Addressed
drive unsafe
Yes
8-253
Set 'no op
status' latch
No
8-253
'LIO or SIO
reject'
8-254
Set 'I/O cond A'
latch
8-253
Block 'SIO I-Q
cycle sample'
CPU operates in
I-R backup mode
until drive is ready
or not busy
8-253
'SIO I-Q cycle
sample'
8-253
Set 'SIO select
cycle' latch
8-254
Set 'I/O cond B'
latch
8-249
Set 'select 0' or
'select 1' latch
with 'bus out 3'
8-211
Set 'fixed' or
'removable' latch
with 'bus out 4'
8-249
Set 'op register'
with 'bus out
5, 6 and 7'
A
8-311


1
2
3
A
B
A 8-310
Start I/O I-R cycle
FCU checks bus out parity and continues to set up for the instruction command
Clock 0 8-254
Reset 'I/O cond A' and 'I/O cond B' latches
Clock 5 8-253
'Condition I-R cycle sample'
8-251
Bus out parity even
Yes
No
8-253
'Reset op reg'
8-254
Set 'even parity' latch
8-251
Latch up bus out register parity holds
8-254
Set 'I/O cond A' and 'I/O cond B' latches
End operation
8-253
'No op status' latch set
No
Yes
8-253
'Reset op reg'
No further action in the FCU
8-253
'SIO I-R cycle sample'
End SIO instruction cycles
CPU cycles (I/O cycles) are available to the FCU at the request of the FCU
8-249
Set op reg with I-R byte, bits
8-231
'Reset FCU status'
8-249
'FCU busy'
Clock 8 8-253
Reset 'SIO select cycle' latch
1
1
Clock 0
Selected drive seeking
Yes
No
Exit to seek operation if this is a seek instruction page 8-313
Complete seek operation on selected drive
See SIO seek operation for details of seek operation page 8-313
8-230
'Seek check' at the end of seek op
No
Yes
8-230
'Pure initial reset'
8-217
'Clock gate'
8-230
'Reset A' and 'reset B'
8-230
'Select file'
Clock 4 8-230
'Start op' 'Inh start'
8-218
Set 'condition execute' latch
8-218
'Raw index'
Yes
No
8-218
Set 'execute' latch
8-230
'Pure end op reset' and 'reset A' and 'B'
8-253
Set 'no op status' latch
8-230
'Seek check reset FCU busy'
End operation
See specific operation for operational details.
Write identifier operation, page 8-317
Write data operation, page 8-325
Read data, read verify, read data diagnostic or scan, operation, page 8-336
Read identifier, page 8-348

No	Signal name	Diagram
1	Start I - O	Interface line
2	CPU cycle	
3	CPU clock times	CPU
4	SIO select cycle	8-253
5	Cycle sample - (I-Q or I-R)	8-253
6	Initial reset	8-230
7	I - O condition B	8-254
8	FCU busy	8-249
9	Start op	8-230
10	Drive select	8-249
11	Write read or scan operation	8-249
12	Clock gate	8-217
13	Write ID, read ID, read data, or scan (specific operation)	8-249
14	Condition execute	8-218
15	Execute	8-218
16	FCU clock	8-247
17	Raw index	8-218
18	Set counter to 8	8-223
19	Bit ring inhibit	8-225
20	Bit ring	8-225





SEEK OPERATION

1 A seek operation is indicated to the file control unit when the N field of the Q byte is all zeros. The R byte cycle does not contain any seek information.

2 After the Start I/O I-Q/I-R cycles are complete, the file control unit selects the disk file control register local storage register to locate the F byte in the disk control field. Four cycle steal requests are made to read out the F, C, S, N, information. Each cycle request updates the disk file control register address by one in order that the next successive byte of the disk control field may be read out. After all four bytes are addressed, the disk file control register address is returned to its original content by subtracting three from the updated value. Information in the F and C bytes are not used in the file control unit for a seek operation.

3 Bit zero of the S byte selects the head to be enabled in a read, write or scan operation. Bit seven of the S byte determines the direction the access mechanism will move.

4 The N byte is set into the difference counter and indicates the number of cylinders the head access mechanism should move. If the N byte is equal to zero, no access motion is required and the seek time is only as long as it takes the four cycle steal operations to complete. If N is equal to or greater than 223, and reverse direction is specified, a recalibrate operation is indicated. A recalibrate operation selects head zero and ignores the condition of the zero bit in the S byte. The file control unit is set up with all seek control information when the fourth cycle steal is complete; mechanical motion (if required) is started at this time.

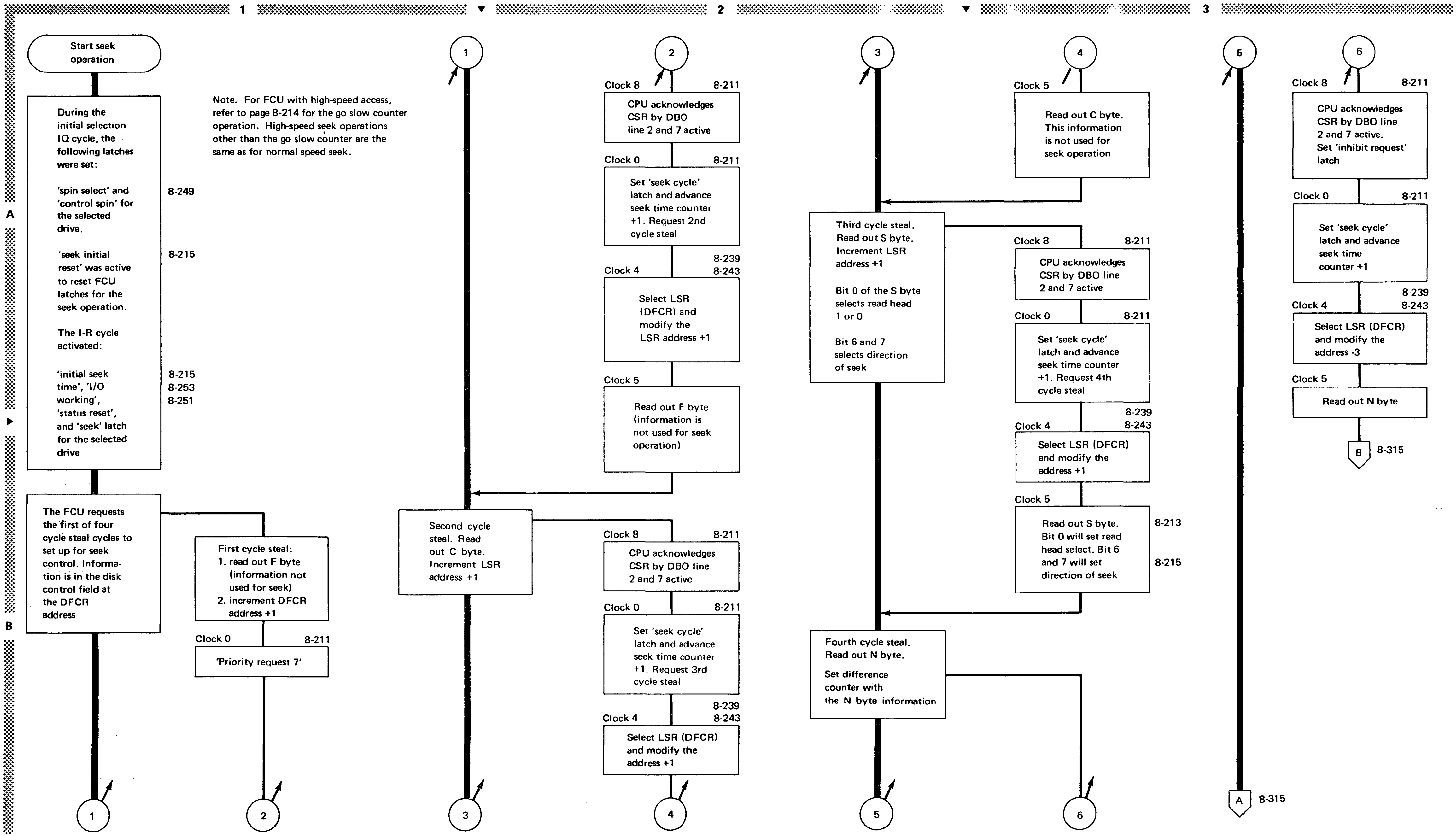
5 Track crossing pulses increment the difference counter as each cylinder is crossed. When the difference counter carries (FF) the 'go' line is deactivated and access motion stops. An interlock time of −24.67 (+3.2, −3.74) milliseconds for the high speed drives, or approximately 28 milliseconds for the standard speed drives, and prevents another disk start I/O operation from starting until head settle motion is ended (see 7).

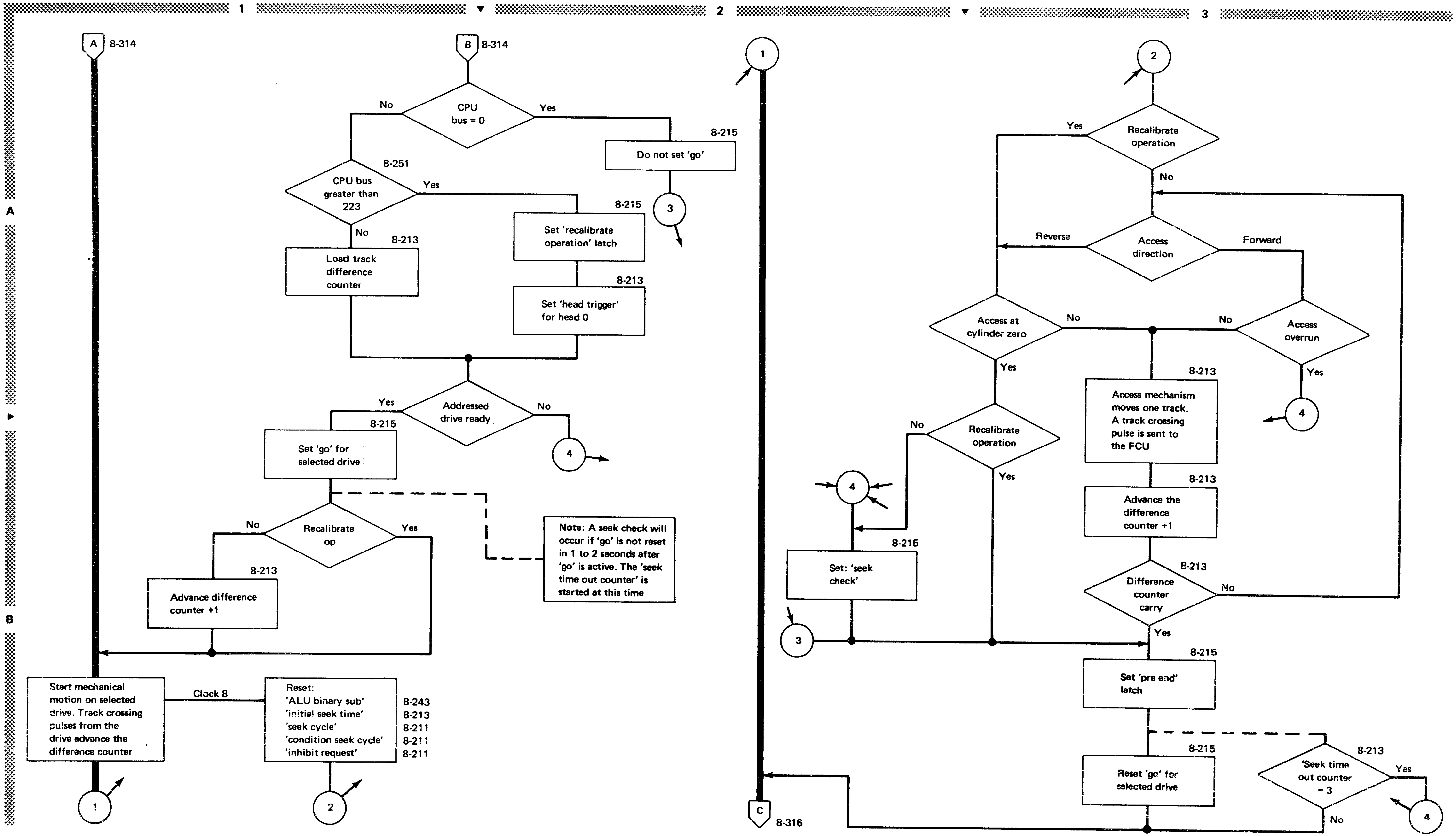
6 Seek checks indicate an abnormal condition during a seek operation. Conditions that set seek check are:

1. No seek end 1 to 2 seconds after 'go' is active.
2. 'Go forward' active and access overrun indicated. 'Access overrun' occurs when the access mechanism is at its inner stop.
3. 'Go reverse' active, 'cylinder zero' indicated, and not in a recalibrate operation.
4. A track crossing pulse was sensed during head settling time.
5. 'Go' active and drive goes not ready during a seek operation.

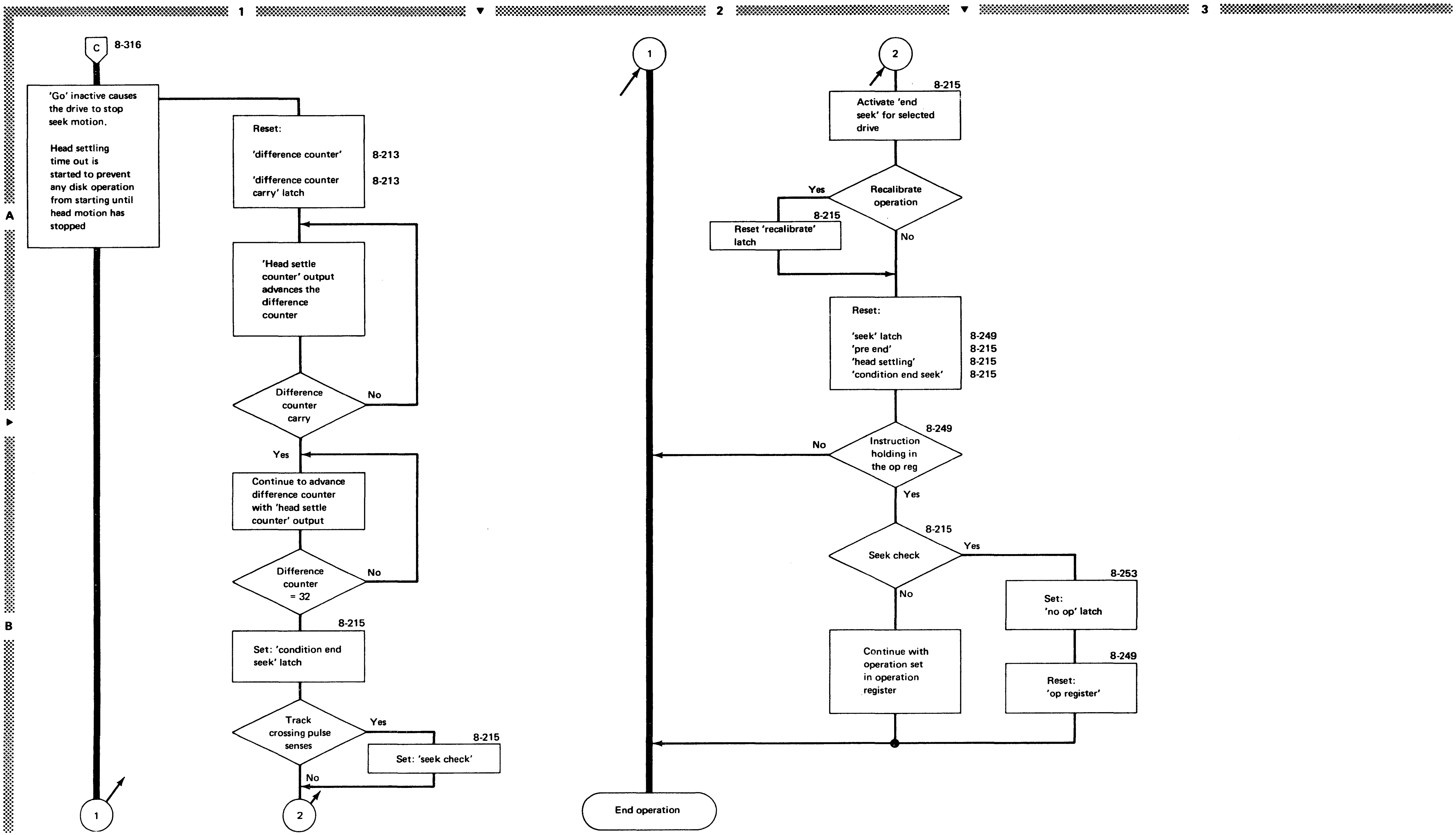
7 Two counters generate time for head settle −24.67 (+3.2, −3.74) milliseconds for the high speed drives, or approximately 28 milliseconds for the standard speed drives, and seek time out (1 - 2 sec). The head settle counter is advanced with clock zero and uses the difference counter for full counting. The difference counter is reset when 'go' drops so it can be used in the head settle time out. The seek time out counter is advanced with raw index pulses from the selected drive.

Note. For FCU with high-speed access, refer to page 8-214 for the go slow counter operation. High-speed seek operations other than the go slow counter are the same as for normal speed seek.





1
2
3
A
B
A 8-314
B 8-314
CPU bus = 0
No
Yes
8-215
Do not set 'go'
3
8-251
CPU bus greater than 223
Yes
No
8-215
Set 'recalibrate operation' latch
8-213
Load track difference counter
8-213
Set 'head trigger' for head 0
Addressed drive ready
Yes
No
8-215
Set 'go' for selected drive
4
Note: A seek check will occur if 'go' is not reset in 1 to 2 seconds after 'go' is active. The 'seek time out counter' is started at this time
Recalibrate op
No
Yes
8-213
Advance difference counter +1
Start mechanical motion on selected drive. Track crossing pulses from the drive advance the difference counter
Clock 8
Reset:
'ALU binary sub' 8-243
'initial seek time' 8-213
'seek cycle' 8-211
'condition seek cycle' 8-211
'inhibit request' 8-211
1
2
2
Recalibrate operation
Yes
No
Access direction
Reverse
Forward
Access at cylinder zero
No
Yes
Access overrun
No
Yes
8-213
Access mechanism moves one track. A track crossing pulse is sent to the FCU
4
Recalibrate operation
No
Yes
4
8-215
Set: 'seek check'
8-213
Advance the difference counter +1
8-213
Difference counter carry
No
Yes
3
8-215
Set 'pre end' latch
8-215
Reset 'go' for selected drive
8-213
'Seek time out counter = 3
Yes
No
4
C 8-316


1
2
3
A
B
C 8-316
'Go' inactive causes the drive to stop seek motion.
Head settling time out is started to prevent any disk operation from starting until head motion has stopped
Reset:
'difference counter' 8-213
'difference counter carry' latch 8-213
'Head settle counter' output advances the difference counter
Difference counter carry
No
Yes
Continue to advance difference counter with 'head settle counter' output
Difference counter = 32
No
8-215
Set: 'condition end seek' latch
Track crossing pulse senses
Yes
8-215
Set: 'seek check'
No
1
2
1
End operation
2
8-215
Activate 'end seek' for selected drive
Recalibrate operation
Yes
8-215
Reset 'recalibrate' latch
No
Reset:
'seek' latch 8-249
'pre end' 8-215
'head settling' 8-215
'condition end seek' 8-215
8-249
Instruction holding in the op reg
No
Yes
8-215
Seek check
Yes
No
8-253
Set: 'no op' latch
8-249
Reset: 'op register'
Continue with operation set in operation register

1 ▼ 2 ▼ 3

A

▶

B

WRITE IDENTIFIER OPERATION

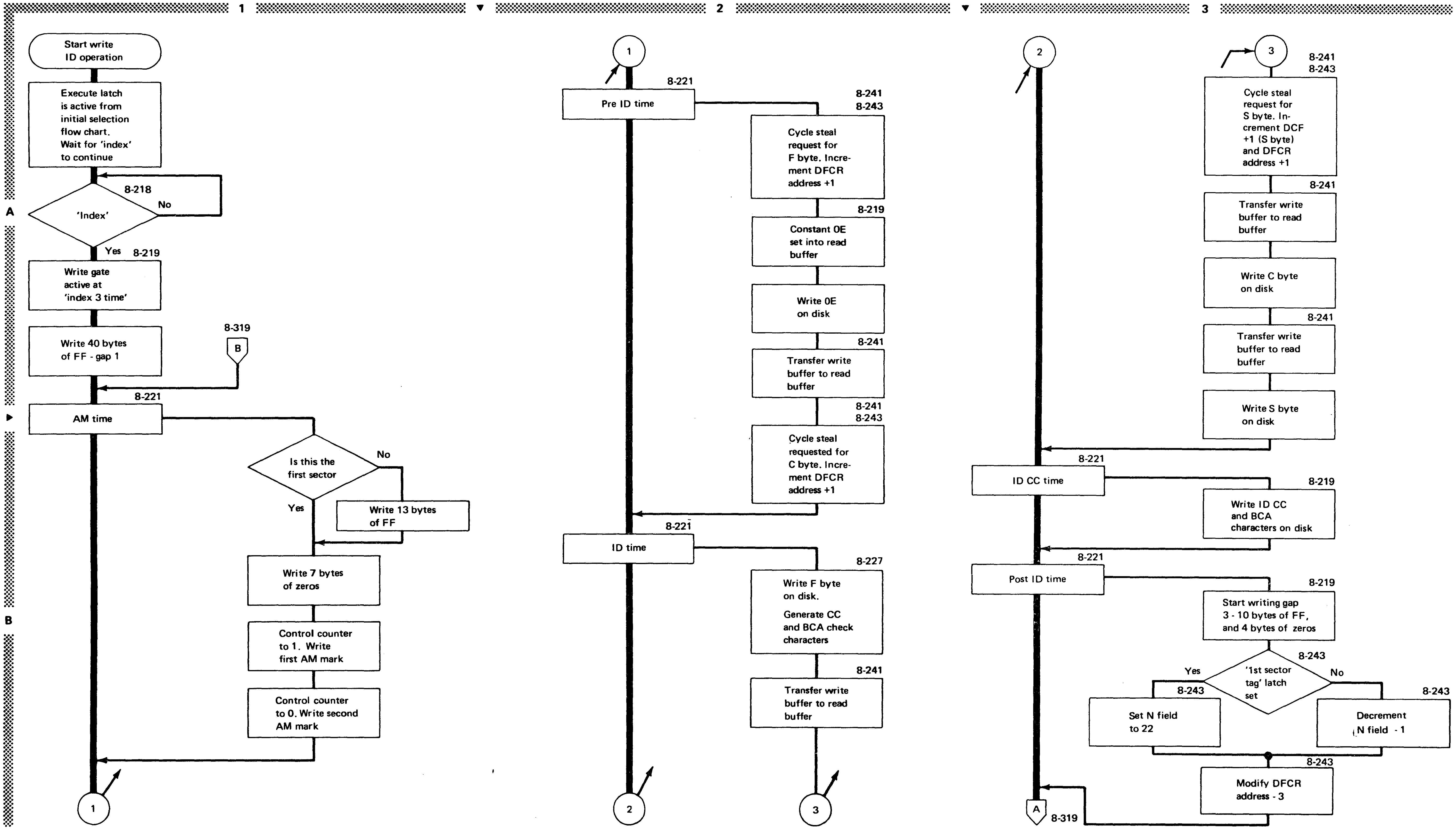
This instruction initiates the writing of a 24-sector format on the selected disk. The operation always starts at the index marker on the disk and writes 24-sector formats. There is no identifier-field compare on a write-identifier instruction before writing.

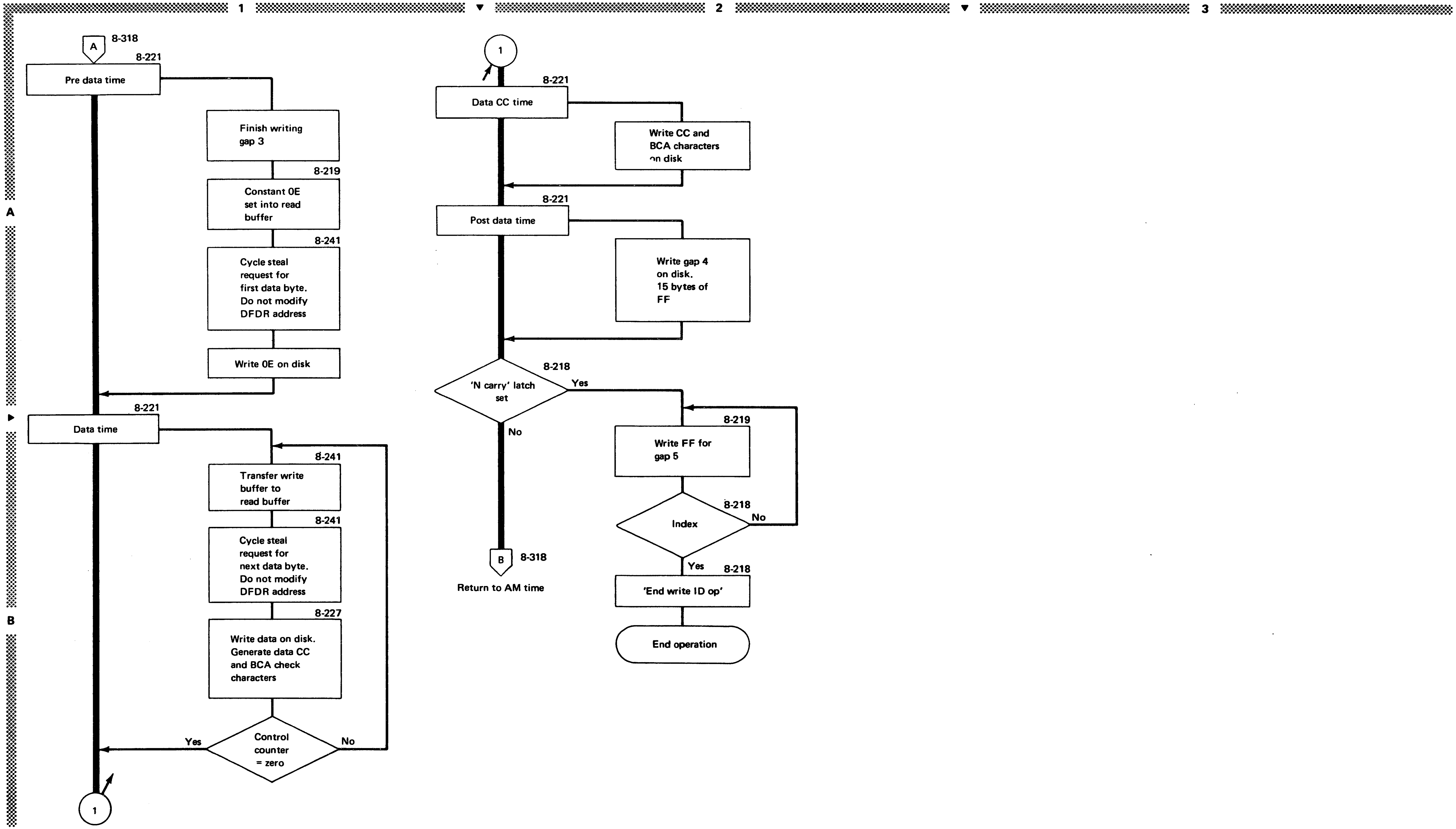
- This operation always writes 24 sectors per track.
- Operation starts at index.
- The N byte in the disk control field is automatically set to 22 by the file control unit (24 sectors are written).
- Sector number is incremented by one. N byte is decremented by one for each sector written. Both of these bytes are in the disk control field in core.
- The DFDR local storage register is not updated for each byte written in the data field. The same character is written repeatedly for the 256 byte data field.
- Cyclic code and bit count appendage characters are generated for the ID and data field. These characters are written at the end of their respective fields within each sector format.
- Two bytes of 'F2' with 2 clock bits missing are written for address marks.

The contents of the sector-identifier field is the first three bytes of the disk-control field (F, C, S) as addressed by the DFCR. The N byte is set by the control unit to ensure writing exactly 24 sectors per track. As each identifier is written on the file the sector number of the disk-control field (S byte) is incremented by one and the N field is decremented by one.

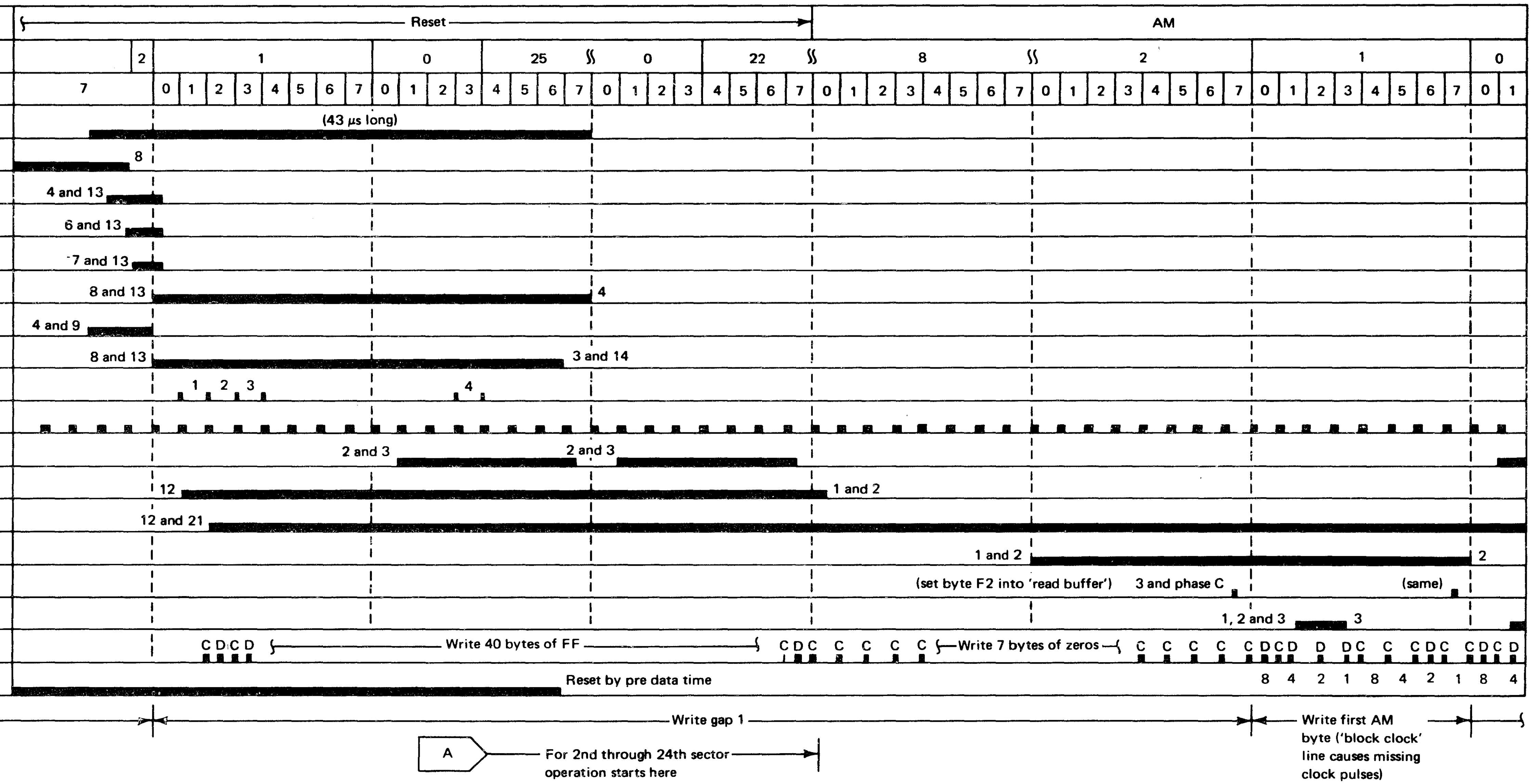
The data field for each sector is written with data from core addressed by the DFDR. This register is not incremented so the entire 256-byte field is written with the same character. If all records have been written, the N byte contains hexadecimal EF.

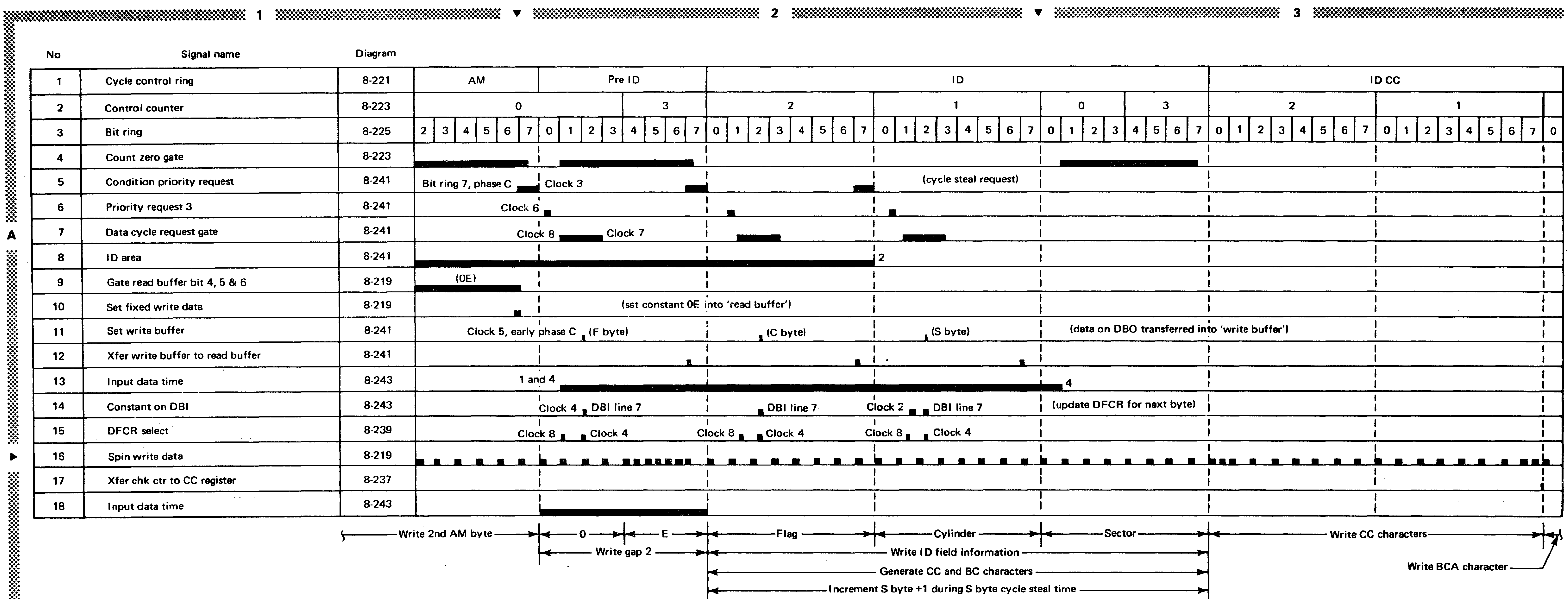
The file control unit is busy to all new operations during a write-identifier operation except sense I/O. The read verify command must be used to check for write errors after a write identifier command, in order to meet file performance specifications.


1
2
3
A
B
Start write ID operation
Execute latch is active from initial selection flow chart. Wait for 'index' to continue
8-218
'Index'
No
Yes
8-219
Write gate active at 'index 3 time'
Write 40 bytes of FF - gap 1
8-319
B
8-221
AM time
Is this the first sector
No
Yes
Write 13 bytes of FF
Write 7 bytes of zeros
Control counter to 1. Write first AM mark
Control counter to 0. Write second AM mark
1
1
8-221
Pre ID time
8-241
8-243
Cycle steal request for F byte. Increment DFCR address +1
8-219
Constant 0E set into read buffer
Write 0E on disk
8-241
Transfer write buffer to read buffer
8-241
8-243
Cycle steal requested for C byte. Increment DFCR address +1
8-221
ID time
8-227
Write F byte on disk.
Generate CC and BCA check characters
8-241
Transfer write buffer to read buffer
2
3
2
3
8-241
8-243
Cycle steal request for S byte. Increment DCF +1 (S byte) and DFCR address +1
8-241
Transfer write buffer to read buffer
Write C byte on disk
8-241
Transfer write buffer to read buffer
Write S byte on disk
8-221
ID CC time
8-219
Write ID CC and BCA characters on disk
8-221
Post ID time
8-219
Start writing gap 3 - 10 bytes of FF, and 4 bytes of zeros
8-243
'1st sector tag' latch set
Yes
No
8-243
Set N field to 22
8-243
Decrement N field - 1
8-243
Modify DFCR address - 3
A
8-319

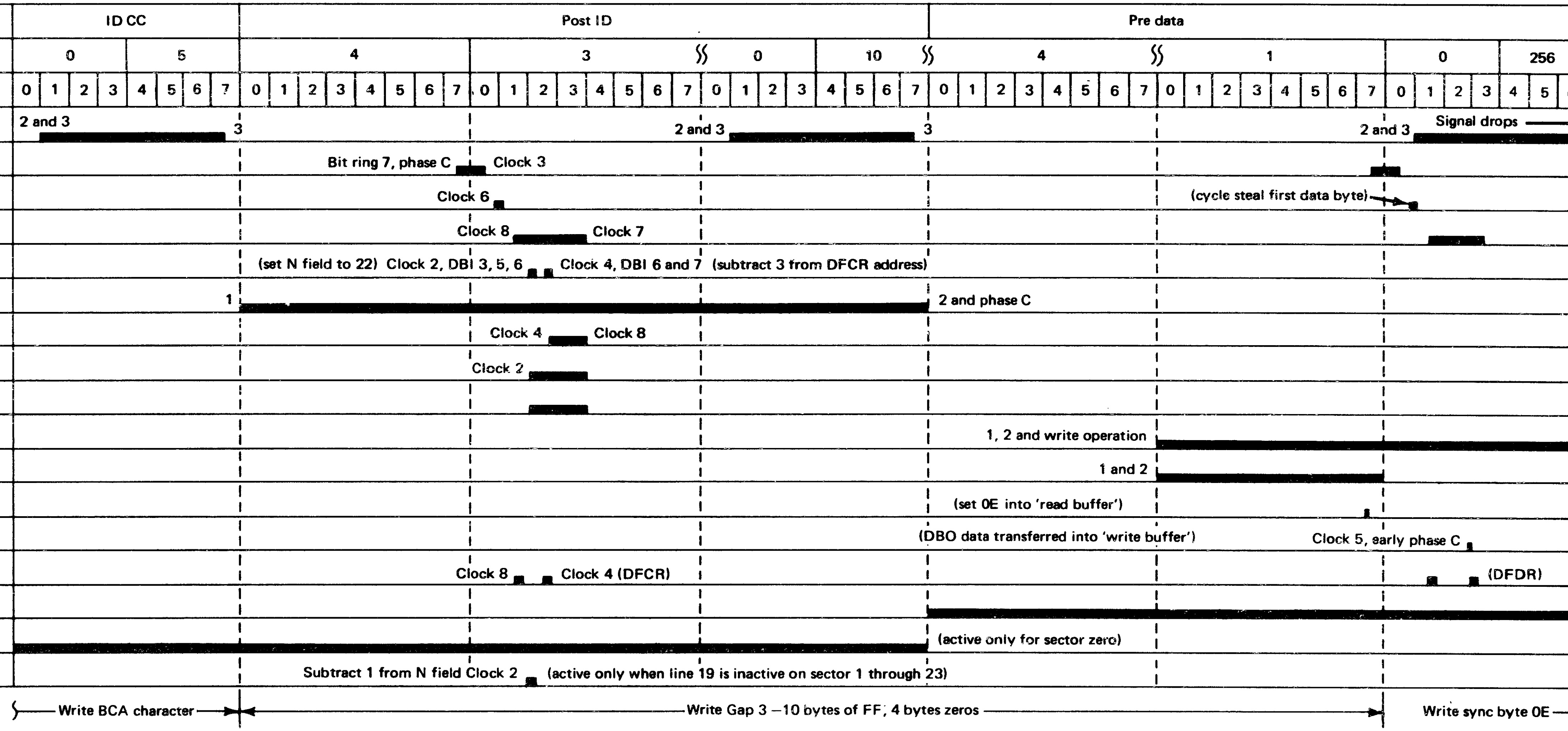

1
2
3
A
B
A
8-318
8-221
Pre data time
Finish writing gap 3
8-219
Constant 0E set into read buffer
8-241
Cycle steal request for first data byte. Do not modify DFDR address
Write 0E on disk
8-221
Data time
8-241
Transfer write buffer to read buffer
8-241
Cycle steal request for next data byte. Do not modify DFDR address
8-227
Write data on disk. Generate data CC and BCA check characters
Control counter = zero
Yes
No
1
1
8-221
Data CC time
Write CC and BCA characters on disk
8-221
Post data time
Write gap 4 on disk. 15 bytes of FF
8-218
'N carry' latch set
Yes
No
B
8-318
Return to AM time
8-219
Write FF for gap 5
8-218
Index
No
Yes
8-218
'End write ID op'
End operation

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Raw index	8-218
5	Bit ring inhibit	8-225
6	Pre index condition	8-218
7	Condition standard index	8-218
8	Standard index	8-218
9	Condition index reset	8-218
10	Index reset	8-218
11	Index time	8-218
12	Index time 1, 2, 3, 4	8-218
13	Clock	8-247
14	Count zero gate	8-223
15	Write FF	8-219
16	Write gate	8-219
17	Gate F2 into read buffer	8-219
18	Set fixed write data	8-219
19	Block clock	8-219
20	Spin write data	8-219
21	1st sector tag	8-243

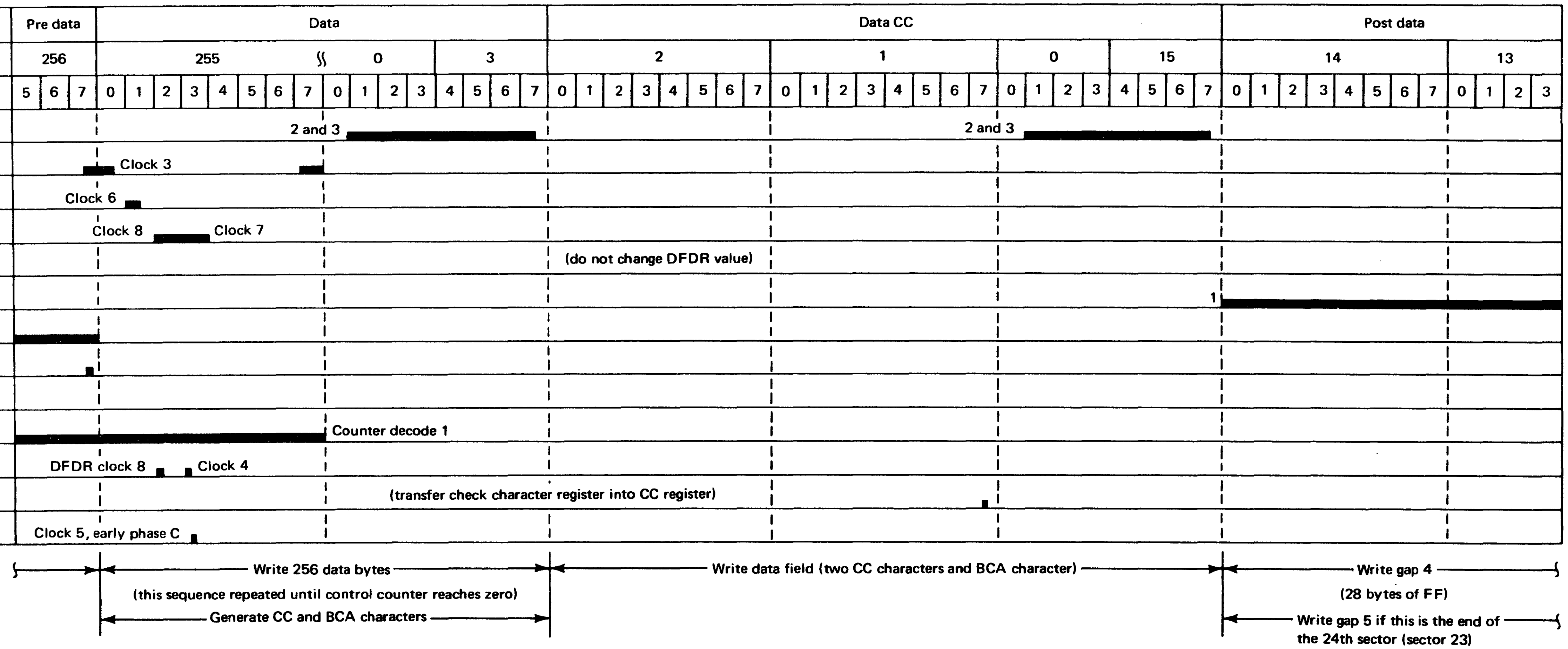



1
2
3
A
B
No
Signal name
Diagram
1 Cycle control ring 8-221
2 Control counter 8-223
3 Bit ring 8-225
4 Count zero gate 8-223
5 Condition priority request 8-241
6 Priority request 3 8-241
7 Data cycle request gate 8-241
8 ID area 8-241
9 Gate read buffer bit 4, 5 & 6 8-219
10 Set fixed write data 8-219
11 Set write buffer 8-241
12 Xfer write buffer to read buffer 8-241
13 Input data time 8-243
14 Constant on DBI 8-243
15 DFCR select 8-239
16 Spin write data 8-219
17 Xfer chk ctr to CC register 8-237
18 Input data time 8-243
AM
Pre ID
ID
ID CC
Bit ring 7, phase C
Clock 3
(cycle steal request)
Clock 6
Clock 8
Clock 7
(0E)
(set constant 0E into 'read buffer')
Clock 5, early phase C
(F byte)
(C byte)
(S byte)
(data on DBO transferred into 'write buffer')
1 and 4
Clock 4
DBI line 7
Clock 2
(update DFCR for next byte)
Clock 8
Clock 4
Write 2nd AM byte
0
E
Flag
Cylinder
Sector
Write CC characters
Write gap 2
Write ID field information
Generate CC and BC characters
Increment S byte +1 during S byte cycle steal time
Write BCA character

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Count zero gate	8-223
5	Condition prior request	8-241
6	Prior request 3	8-241
7	Data cycle request gate	8-241
8	Constant on DBi	8-243
9	Write FF	8-219
10	ALU binary subtract	8-243
11	Store data	8-243
12	Block SDR-B register	8-243
13	Data area	8-241
14	Gate bits 4, 5, & 6 to read buffer (0E)	8-219
15	Set fixed write data	8-219
16	Set write buffer	8-241
17	LSR selected	8-239
18	Input data time	8-243
19	1st sector tag	8-243
20	Decrement N	8-243



No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Count zero gate	8-223
5	Condition prior request	8-241
6	Priority request 3	8-241
7	Data cycle request gate	8-241
8	Constant on DBI	8-243
9	Write FF	8-219
10	Input data time	8-243
11	Xfer write buffer to read buffer	8-241
12	Block SDR-B register	8-243
13	Data area	8-241
14	LSR select	8-239
15	BCA to CC register gate	8-237
16	Set write buffer	8-241

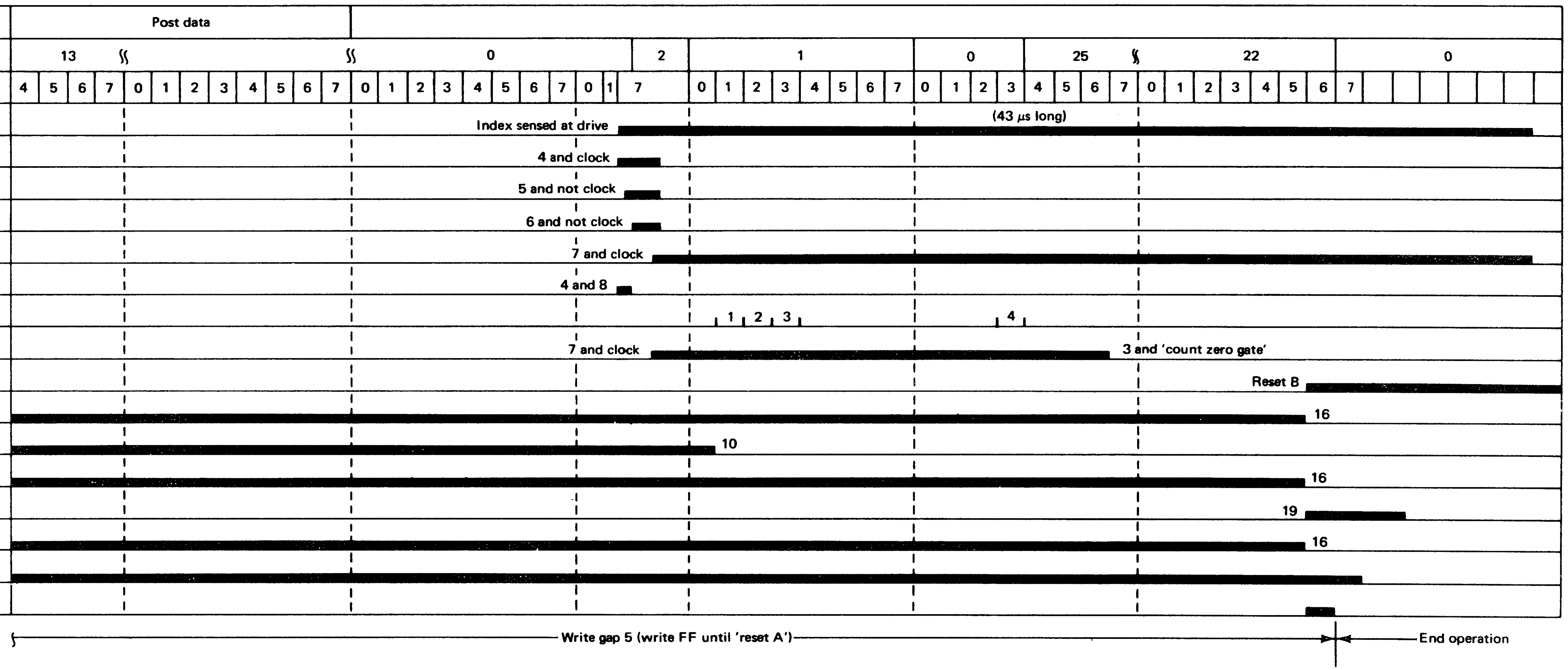


No	Signal name	Diagram	Timing
1	Cycle control ring	8-221	Post data / AM
2	Control counter	8-223	13 ⟆ 0 / 22 / 21 ⟆ 9 / 8 / 7 / 6 / 5
3	Bit ring	8-225	4 5 6 7 0 1 2 3 4 5 6 7 / 0 1 2 3 4 5 6 7 / 0 1 2 3 4 5 6 7 / 0 1 2 3 4 5 6 7 / 0 1 2 3 4 5 6 7 / 0 1 2 3 4 5 6 7 / 0 1 2
4	Write FF	8-219	Phase C
5	Count zero gate	8-223	2 and 3

Write FF (gap 4 or 5)

Return to A on page 8-320 for sector 1 through 24.
For ending sequence after the 24th sector, see next page

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-221
4	Raw index	8-218
5	Pre index condition	8-218
6	Condition index	8-218
7	Standard index	8-218
8	Condition index reset	8-218
9	Index reset	8-218
10	Index times 1, 2, 3 & 4	8-218
11	Index time	8-218
12	Bit ring inhibit	8-225
13	Write FF	8-219
14	Write gate	8-219
15	Erase gate	8-219
16	Reset A	8-230
17	Execute	8-218
18	FCU busy	8-249
19	End write ID	8-218



A

B

1 2 3

A

WRITE DATA OPERATION

This instruction initiates the transfer of data from core storage to the selected track on the disk. Data is transferred in multiples of 256 bytes. The entire data contents of a cylinder may be written (maximum of 48 sectors) if started with sector 0, head 0. Only consecutive sectors are written when multiple-sector operation is indicated.

- Data in core storage to be written on disk is transferred when the ID information in the disk control field correctly compares with an ID area read from disk.
- 256 data bytes per sector are written in the data field. Up to 48 sectors may be written during one start I/O instruction. The file control unit switches head selection and updates the sector number in the disk control field to 32 when required in a multi-sector operation.
- The DFDR is addressed to obtain the location of the data byte to be written. The DFDR is updated one for each cycle steal within the data field.
- Cyclic code and BCA characters are generated and written after the data field. Only the data field CC and BCA are re-written. The ID area remains unchanged.
- Operation ends when the N byte in the disk control field carries. File control unit logic brings up 'end op reset' at post data time when the N byte carry is indicated.

Writing of data begins with the sector specified by the file identifier in the disk-control field located in the core storage. A comparison is made between disk control field identifier and sector identifiers read from the selected disk track. Comparing begins with the first ID to pass under the read head. An equal compare of the 3-byte identifier enables the transfer of the 256-byte sector data. The data is fetched from core using the DFDR for addressing. When multiple sectors are indicated, the attachment logic updates the disk control field sector number by plus one and decrements the N field by one. This updated identifier is compared with the next identifier read from the disk. In the multiple-sector write that requires head switching, the attachment updates the last disk address in the control field by adding nine to it. An equal comparison must be made on all succeeding addresses before their corresponding data fields are written on the disk. The data field of a sector is not written if an error is indicatred before writing of data begins.

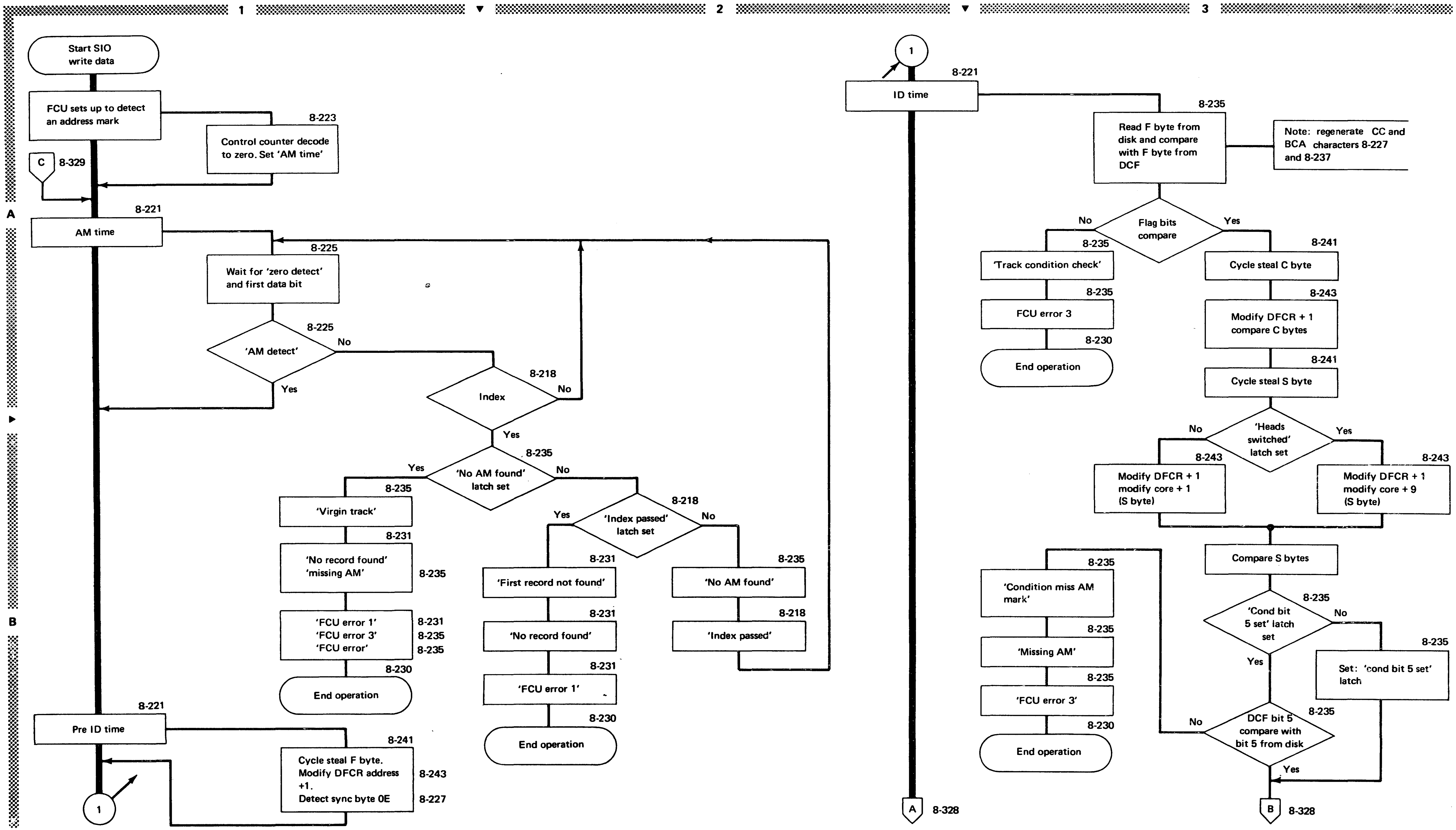
B

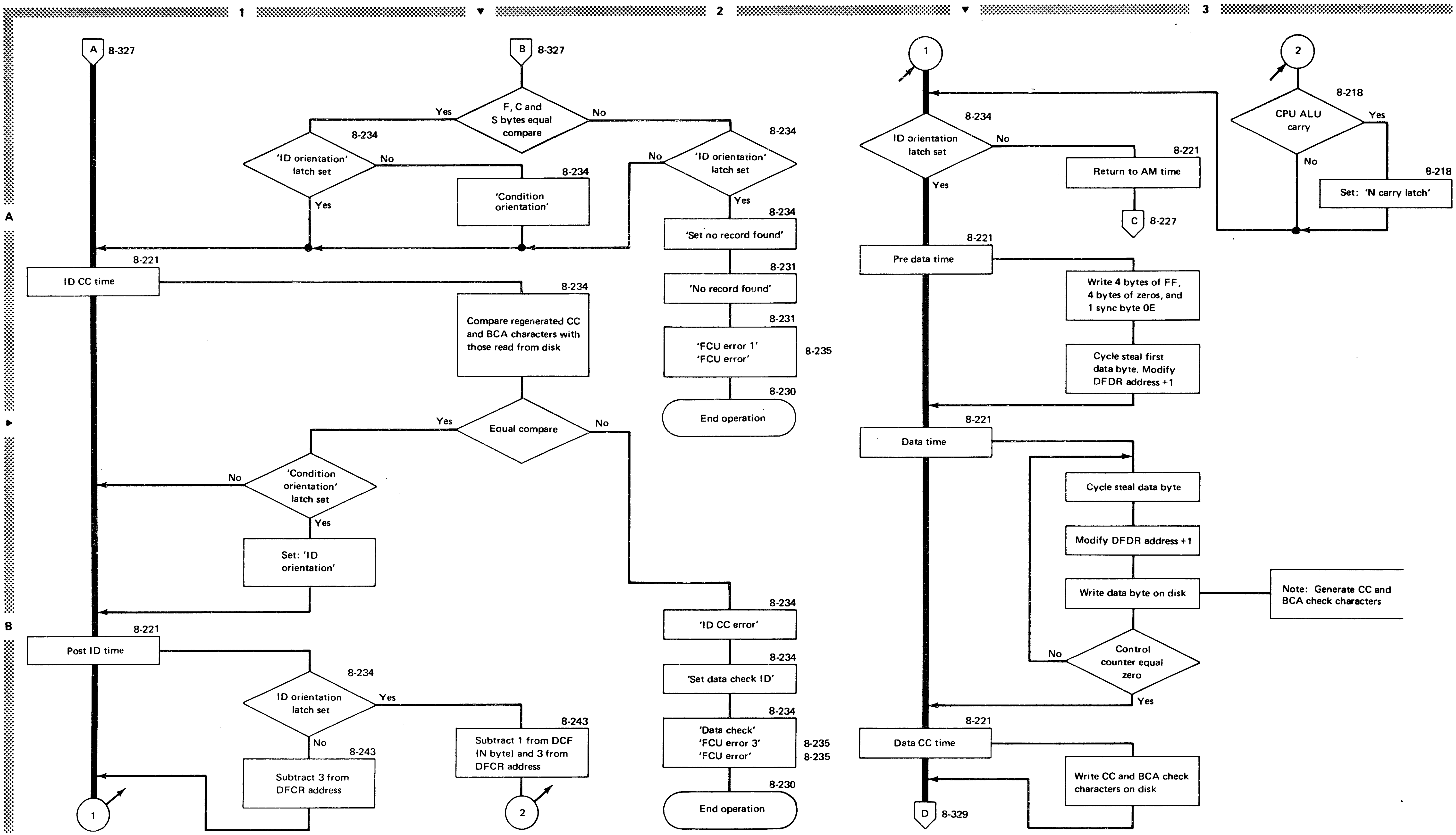
The write-data operation is ended by completing the N+1 sectors called for in the N byte of the disk-control field or by the detection of an error condition. An equipment check ends the operation immediately. The presence of the error can be determined by a test I/O and branch instruction.

The control unit is busy to any new operation except sense I/O while it is performing a write data operation. During writing, the control unit generates two cyclic-check characters and a one bit-count-appendage byte for each data field. The characters are recorded at the end of the data field. The verify command must be used to check for write errors to meet file performance specifications.

During the writing of each identifier and data field, the attachment hardware generates two cyclic-check bytes and one bit-count-appendage byte which are automatically written at the end of each field.

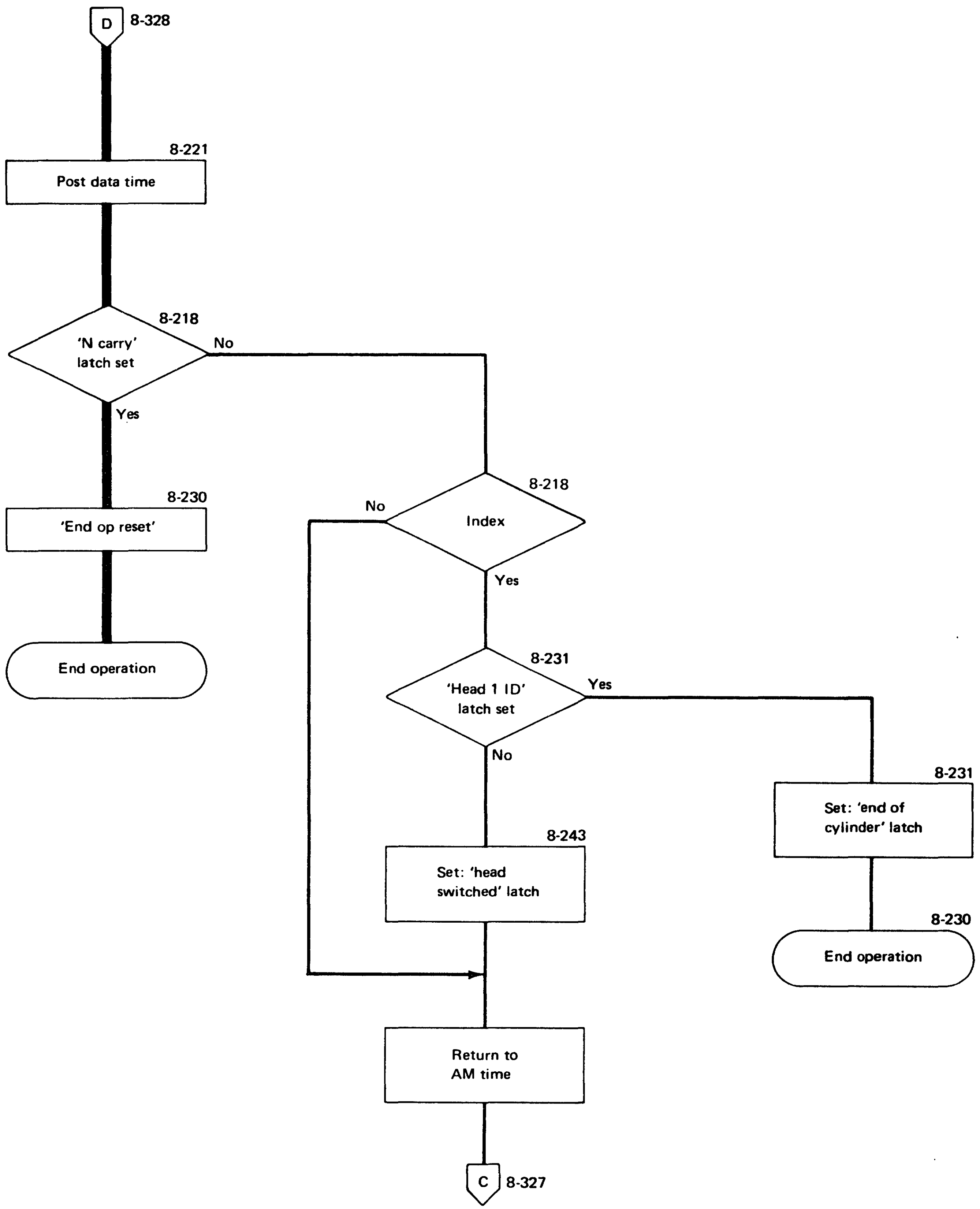
At the end of the operation the disk-control field contains information about the progress of the operation. The identifier portion of the disk-control field indicates the last sector written or attempted to be written. The number of records written (or attempted to be written in case of an error condition) can be determined by subtracting the contents of the N byte of the disk-control field from its original value unless all records have been processed.


1
2
3
A
B
Start SIO write data
FCU sets up to detect an address mark
8-223
Control counter decode to zero. Set 'AM time'
C
8-329
8-221
AM time
8-225
Wait for 'zero detect' and first data bit
8-225
'AM detect'
No
Yes
8-218
Index
No
Yes
8-235
'No AM found' latch set
Yes
No
8-235
'Virgin track'
8-231
'No record found' 'missing AM'
8-235
'FCU error 1' 'FCU error 3' 'FCU error'
8-231
8-235
8-235
8-230
End operation
8-218
'Index passed' latch set
Yes
No
8-231
'First record not found'
8-231
'No record found'
8-231
'FCU error 1'
8-230
End operation
8-235
'No AM found'
8-218
'Index passed'
8-221
Pre ID time
8-241
Cycle steal F byte. Modify DFCR address +1. Detect sync byte 0E
8-243
8-227
1
1
8-221
ID time
8-235
Read F byte from disk and compare with F byte from DCF
Note: regenerate CC and BCA characters 8-227 and 8-237
Flag bits compare
No
Yes
8-235
'Track condition check'
8-235
FCU error 3
8-230
End operation
8-241
Cycle steal C byte
8-243
Modify DFCR + 1 compare C bytes
8-241
Cycle steal S byte
'Heads switched' latch set
No
Yes
8-243
Modify DFCR + 1 modify core + 1 (S byte)
8-243
Modify DFCR + 1 modify core + 9 (S byte)
Compare S bytes
8-235
'Cond bit 5 set' latch set
No
Yes
8-235
Set: 'cond bit 5 set' latch
8-235
DCF bit 5 compare with bit 5 from disk
No
Yes
8-235
'Condition miss AM mark'
8-235
'Missing AM'
8-235
'FCU error 3'
8-230
End operation
A
8-328
B
8-328

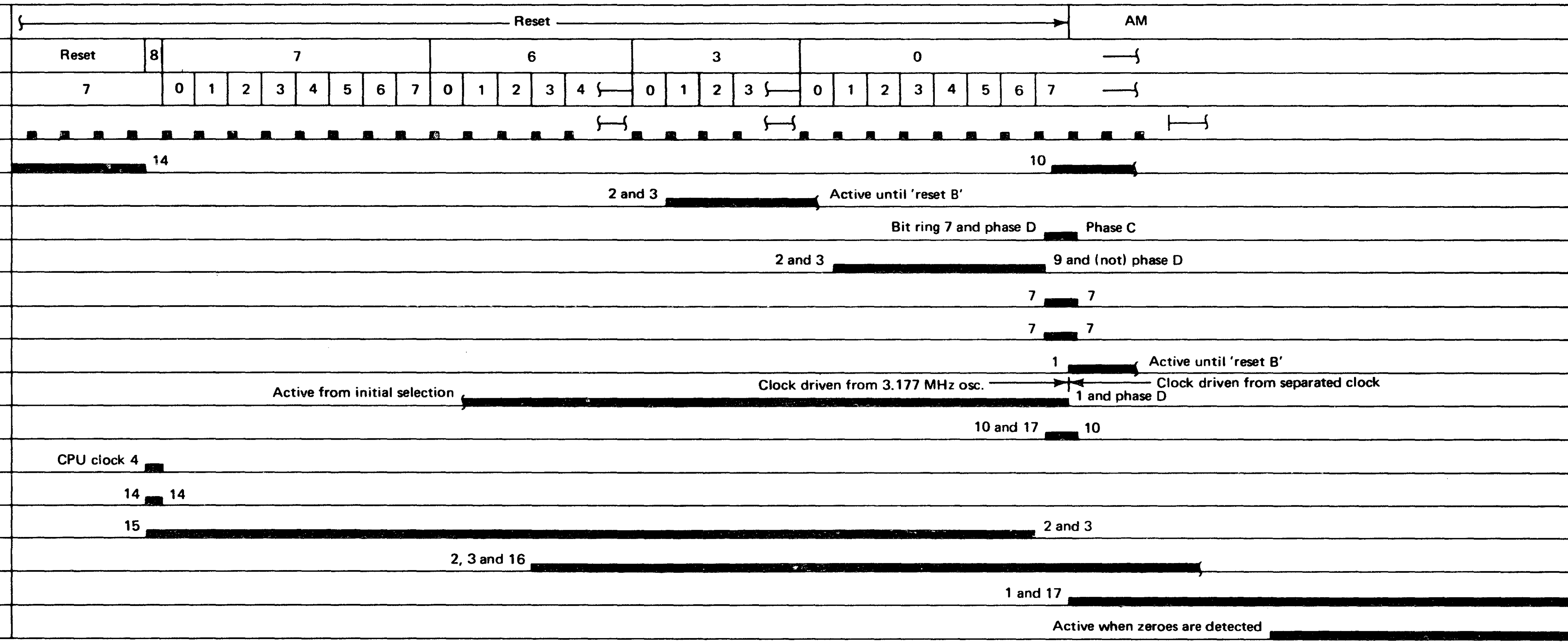

A 8-327
B 8-327
F, C and S bytes equal compare
Yes
No
'ID orientation' latch set
8-234
'Condition orientation'
'ID orientation' latch set
'Set no record found'
'No record found'
8-231
'FCU error 1'
'FCU error'
8-235
End operation
8-230
ID CC time
8-221
Compare regenerated CC and BCA characters with those read from disk
Equal compare
'Condition orientation' latch set
Set: 'ID orientation'
'ID CC error'
'Set data check ID'
'Data check'
'FCU error 3'
'FCU error'
Post ID time
ID orientation latch set
Subtract 1 from DCF (N byte) and 3 from DFCR address
8-243
Subtract 3 from DFCR address
1
2
ID orientation latch set
Return to AM time
C 8-227
CPU ALU carry
8-218
Set: 'N carry latch'
Pre data time
Write 4 bytes of FF, 4 bytes of zeros, and 1 sync byte 0E
Cycle steal first data byte. Modify DFDR address +1
Data time
Cycle steal data byte
Modify DFDR address +1
Write data byte on disk
Note: Generate CC and BCA check characters
Control counter equal zero
Data CC time
Write CC and BCA check characters on disk
D 8-329

A

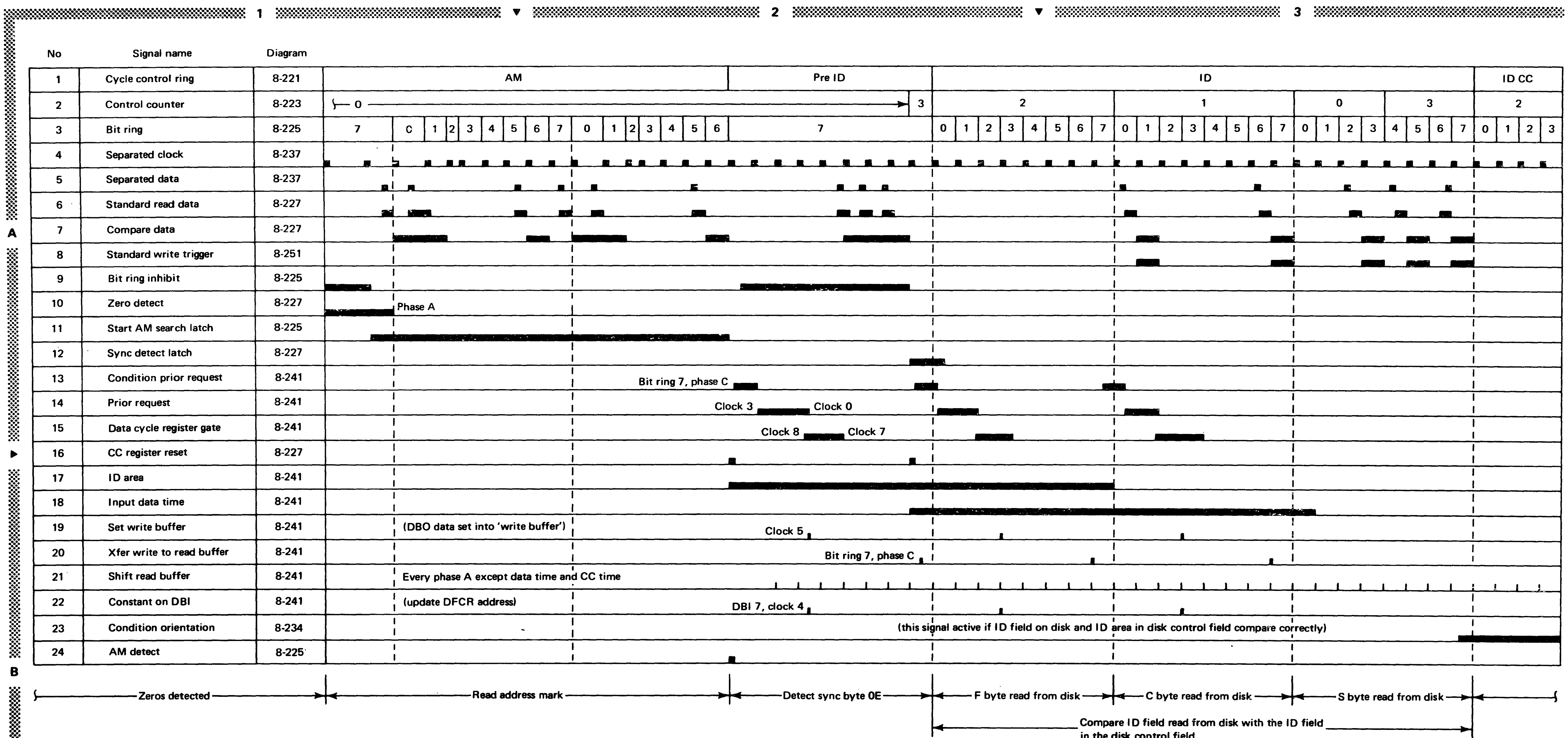
B


D 8-328
8-221
Post data time
8-218
'N carry' latch set
No
Yes
8-230
'End op reset'
End operation
8-218
Index
No
Yes
8-231
'Head 1 ID' latch set
Yes
No
8-231
Set: 'end of cylinder' latch
8-243
Set: 'head switched' latch
8-230
End operation
Return to AM time
C 8-327

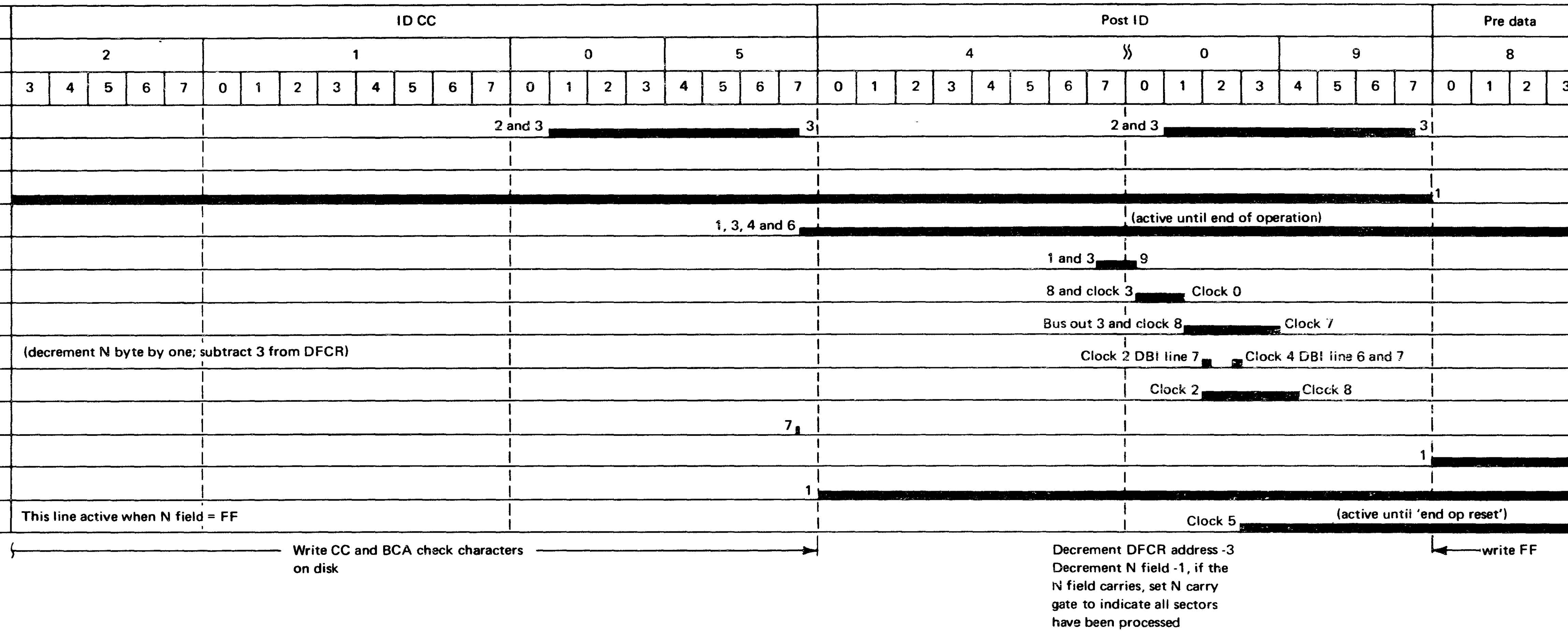
No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Clock	8-247
5	Bit ring inhibit	8-225
6	CCR pre advance gate	8-223
7	CCR advance gate	8-223
8	Count zero gate	8-223
9	Count zero reset	8-223
10	Pending AM time	8-221
11	Conditions 1st AM	8-221
12	Clock gate	8-217
13	Set CC register pos 1 on	8-227
14	Start op	8-230
15	Set counter to 8	8-223
16	Condition read gate	8-218
17	Read gate	8-218
18	Search address mark	8-225
19	Zero detect	8-227



In the initial selection flow chart, the file control unit was set up for a write data operation. The next objective is to locate an address mark. Address mark detection is started when zeros in the sector gaps are detected to indicate to the file control unit that an address mark is approaching the read heads in the drive. The next data bit read, after zeros detect, starts the FCU looking for the address mark.

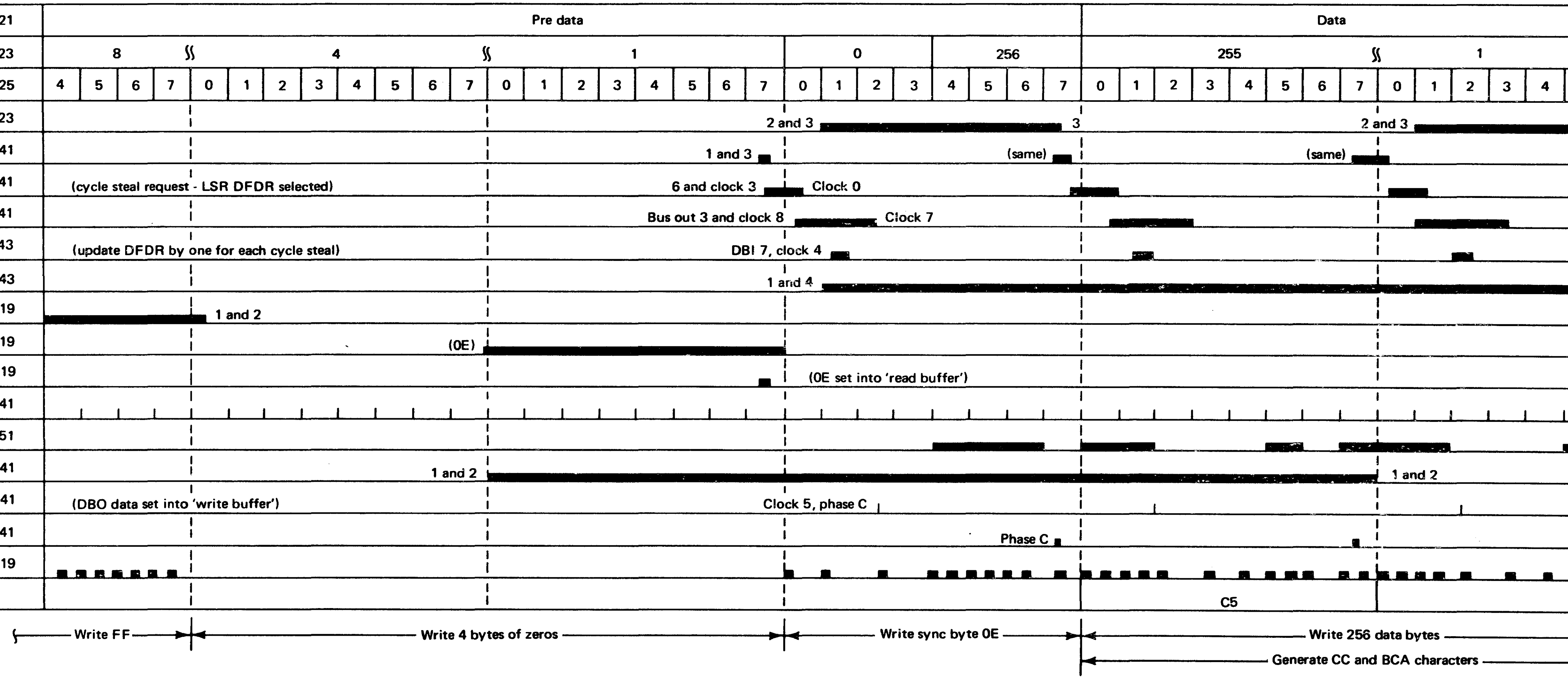

1
2
3
A
B
No
Signal name
Diagram
1 Cycle control ring 8-221
2 Control counter 8-223
3 Bit ring 8-225
4 Separated clock 8-237
5 Separated data 8-237
6 Standard read data 8-227
7 Compare data 8-227
8 Standard write trigger 8-251
9 Bit ring inhibit 8-225
10 Zero detect 8-227
11 Start AM search latch 8-225
12 Sync detect latch 8-227
13 Condition prior request 8-241
14 Prior request 8-241
15 Data cycle register gate 8-241
16 CC register reset 8-227
17 ID area 8-241
18 Input data time 8-241
19 Set write buffer 8-241
20 Xfer write to read buffer 8-241
21 Shift read buffer 8-241
22 Constant on DBI 8-241
23 Condition orientation 8-234
24 AM detect 8-225
AM
Pre ID
ID
ID CC
Phase A
Bit ring 7, phase C
Clock 3
Clock 0
Clock 8
Clock 7
(DBO data set into 'write buffer')
Clock 5
Bit ring 7, phase C
Every phase A except data time and CC time
(update DFCR address)
DBI 7, clock 4
(this signal active if ID field on disk and ID area in disk control field compare correctly)
Zeros detected
Read address mark
Detect sync byte 0E
F byte read from disk
C byte read from disk
S byte read from disk
Compare ID field read from disk with the ID field in the disk control field

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Count zero gate	8-223
5	Bit ring inhibit	8-225
6	Condition orientation	8-234
7	ID orientation	8-234
8	Condition prior request	8-241
9	Prior request latch	8-241
10	Data cycle request gate	8-241
11	Constant on DBI	8-243
12	ALU binary subtract	8-243
13	Start orientation reset	8-234
14	Write gate	8-219
15	Write FF	8-219
16	N carry gate	8-218



1 ▼ 2 ▼ 3

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Count zero gate	8-223
5	Condition prior request	8-241
6	Prior request latch	8-241
7	Data cycle request gate	8-241
8	Constant on DBI	8-243
9	Input data time	8-243
10	Write FF	8-219
11	Gate read buffer 4, 5, & 6	8-219
12	Set fixed write data	8-219
13	Shift read buffer (phase A)	8-241
14	Standard write trigger	8-251
15	Data area	8-241
16	Set write buffer	8-241
17	Xfer write buffer to read buffer	8-241
18	Write data to drive	8-219
19	Hex character written	

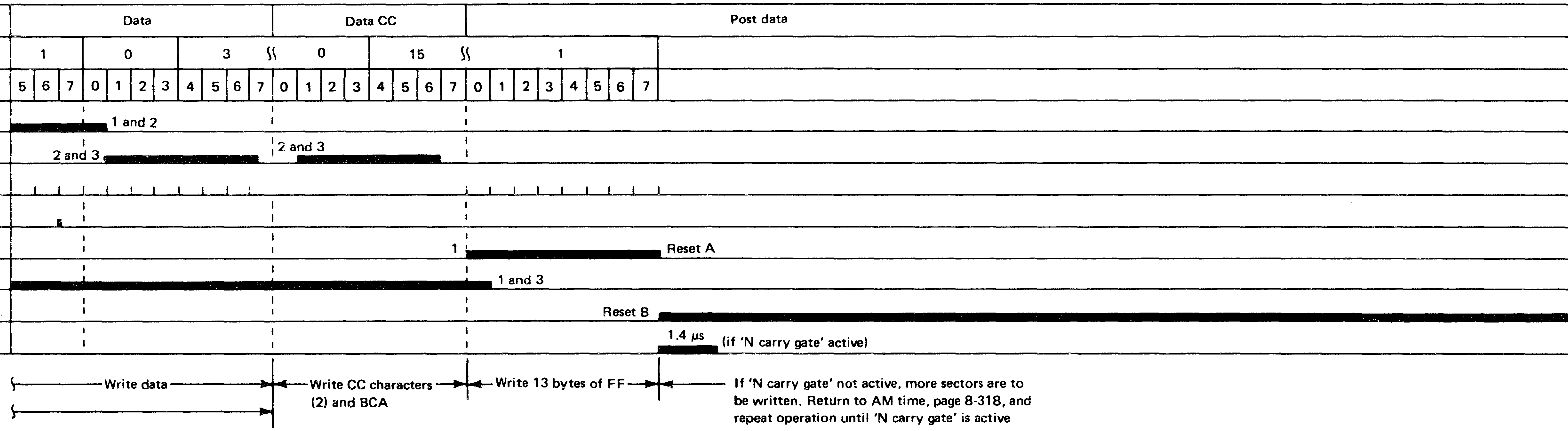


A

B

1 2 3

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Input data time	8-243
5	Count zero gate	8-223
6	Shift read buffer	8-241
7	Xfer write buffer to read buffer	8-241
8	Write FF	8-219
9	Write gate	8-219
10	Bit ring inhibit	8-225
11	End op reset	8-230



A

B

READ OPERATIONS

Read Data Operation

This instruction initiates the transfer of data from the selected disk to core storage. Data is transferred in multiples of 256 bytes (contents of an individual file sector). The entire contents of a cylinder may be read (48 sectors) if started with sector 0 head 0. Only consecutive sectors are read when multiple-sector reads are indicated.

- Reading of data begins when the ID information in the disk control field correctly compares with an ID field read from disk.
- All of the sector data field is read (256 bytes). Up to 48 sectors may be read in one operation. The file control unit switches heads and updates the sector address in the disk control field to 32, if required in a multiple sector read operation.
- The DFDR is addressed to obtain the location of the first byte in core where data is to be transferred. The DFDR is updated with each cycle steal request during the 256 byte data field.
- Cyclic code and BCA characters are generated and compared with the check characters recorded on disk. A non-compare will be indicated with a data check.

Reading of data begins with the sector specified by the disk-control field located in core. A comparison is made between this core identifier and sector identifier read from the selected disk track. Comparing begins with the first ID field to come under the head. An equal compare of the 3-byte identifier (flag, cylinder and sector) enables the reading and transfer of the 256-byte sector data. This data is read into core using the DFDR for memory addressing. If multiple sectors are indicated, the attachment logic updates the sector address by one and decrements the N field by one; both are found in the disk-control field. If the multiple-sector read requires head switching, the attachment updates the last sector address by adding nine to it. This updated identifier is compared with the next identifier read from the file. Any error found in this identifier causes the operation to end after the transfer of the data portion of the sector to core.

During a read operation, the attachment generates two cyclic check bytes and a bit-count-appendage byte from the data that has been read and compares these to the CC bytes and bit-count-appendage byte read back with the data, thus providing a check for read errors. During multiple-sector reads, the operation terminates at the end of any sector in which an error is detected, except an equipment check causes an immediate end.

At the end of an operation, the four bytes of the disk-control field contains information about the progress of the operation. The number of sectors processed is equal to the original value of N minus the present value unless all sectors requested have been processed. If all sectors have been processed, the value of N is hexadecimal FF. The residual value of N is located in the N byte of the disk-control field at the end of the operation. The head/sector byte of the identifier portion of the disk-control field is the last identifier processed unless (1) there is a missing address marker or (2) no identifier has been processed. If no identifier has been processed, the identifier in the disk-control field is the identifier of the first sector desired. If there is a missing address marker and a sector has been processed on a multi-sector operation, then the identifier in the disk-control field is the identifier of the sector that has the missing address marker. The last data field in core is the data portion of the sector following the sector with the missing address marker.

The file control unit is busy to all other operations except sense I/O during a read-data operation.

Read Verify Operation

This instruction is used for write checking and should be used after every write instruction. (Instruction sequence should be write, test I/O, then read verify.) The instruction operates exactly like a read-data instruction, except that the data field is not transferred to core, and no cycle-steal requests are made to transfer data field characters or to update DFDR. (DFDR address is not changed.) The function of write checking is done by regenerating and comparing the cyclic check characters as in a normal read-data command.

At the end of the operation, the disk-control field contains information about the progress of the operation. The identifier portion of the disk-control field indicates the last sector verified or attempted to be verified. The number of records verified or attempted to be verified can be determined by subtracting the contents of the N byte of the disk-control field from its original vlaue unless all records have been verified.

The file control unit is busy to all other instructions except a sense I/O during a read verify command.

The differences of the read verify operation from the read data operation are as follows:

1. 'Verify op' blocks data cycle steal requests on diagram 8-241.
2. DFDR address +1 modification is blocked because 'data cycle request gate' is not active at data time, diagram 8-243.

Otherwise this operation is the same as the read data operation.

Read Data Diagnostic Operation

This command operates similarly to a read-data command. The command always begins at index and reads up to a maximum of 48 sectors. However, the operation should not be used for more than 24 sectors. Exceeding the 24-sector limit increases the chances of reading the wrong data field into core, and therefore must not be done. The data portion of the record is read and placed in core beginning at the address specified in DFDR. The sector number in the disk control field is incremented by one and the N byte is decremented by one as the operation is repeated on following sectors. The data address is returned to its original value at the beginning of each sector so that the following data field overlays the first data field in core. The operation continues until (1) the end of the sector in which the N byte is reduced to FF, (2) the end of cylinder is reached, or (3) an equipment check is detected. No other error conditions will end the operation. At this time the contents of the last sector read are available in core.

This command operates with reduced requirements for detection of address markers to improve the opportunity for recovering data that is not readable with a read-data due to a missing address marker. The reduced requirements are described in chapter 2 address mark detection.

The original identifier in core should be the identifier of the first record on the track so that at the end of the operation the identifier area in core contains the identifier of the last record read, unless there is a no-record found without a data check or a track-condition check. If there is a no-record found without data check or track-condition check, this is an indication that there was a missing address marker earlier on the track.

See diagram 8-225 for address mark detection logic and functional unit description on page 8-224.

The DFDR address is returned to the original address at the end of each sector by the constant 'return DFCR' on diagram 8-243.

1 2 3

A

B

(Intentionally blank)

1 ▼ 2 ▼ 3

A ▶ B

Scan Operations

The scan operation searches the data fields on the disk to find one that meets certain specified conditions when compared to a sector-sized data field in storage. Up to one cylinder of data (48 sectors) can be scanned in one operation. The scan operation can specify one of the following conditions to satisfy the scan:

1. Equal
2. Low or equal
3. High or equal

The data in the sectors on the disk is compared with the 256 characters in the disk data field in storage. The disk data field is addressed by the disk field data register. The comparison of individual characters within the sector can be masked off by placing a mask character consisting of all bits (hexadecimal FF) in each non-compare byte in the disk data field in storage. If only 10 bytes are to be compared the field must contain 246 mask characters in the byte positions of the characters that are not to be scanned.

Scanning of the data begins with the sector specified by the identifier portion of the disk control field. Comparing of sector addresses begins with the first sector identifier to come under the head. After the beginning sector is scanned, the S byte is updated to the identifier of the next sector and the N byte is decreased by 1 for each sector scanned.

The operation ends under the following conditions:

1. When the data on the disk satisfies whichever condition is specified by the start I/O instruction—
   a. Equal to the storage data field
   b. Equal to or lower than the storage data field
   c. Equal to or higher than the storage data field
2. At the end of the sector in which the sector count in the N byte of the disk control field goes to FF.
3. When the end of the cylinder is reached.
4. At the end of any sector in which an error occurs after the first identifier specified by the disk control field has been found.

The control unit is busy to any new operations except sense I/O while performing a scan operation.

A scan found condition is indicated to a test I/O and branch or advance program level instruction. The appropriate bit in the status byte is also set by a scan equal condition.

At the end of the operation the disk control field contains information about the progress of the operation. The identifier portion contains the sector identifier of the last sector scanned unless there is a missing address marker. If there is a missing address marker, the identifier portion indicates the sector with the missing address marker. If no sector has been scanned, the identifier portion indicates the first sector designated. The number of sectors scanned can be determined by subtracting the contents of the N byte from the original vlaue of the N byte unless all sectors have been processed. If all sectors have been processed, the N byte is hexadecimal FF.

The disk file data address register contains the original address at the end of the operation unless equipment check occurs. The register contains the address of the last character processed in the event of an equipment check.

The read data operational flowchart and timing charts may be used for scan operations with the following exceptions.

1. Scan is set into the operation register, diagram 8-249.
2. The DFDR address is returned to the original starting address by the signal 'return DFCR' on diagram 8-243.
3. Comparing of the 'standard write trigger' and the 'compare read data trigger' is on diagram 8-234.
4. The scan mask is detected on diagram 8-251 and blocks the compare logic on diagram 8-234.

Scan Low or Equal

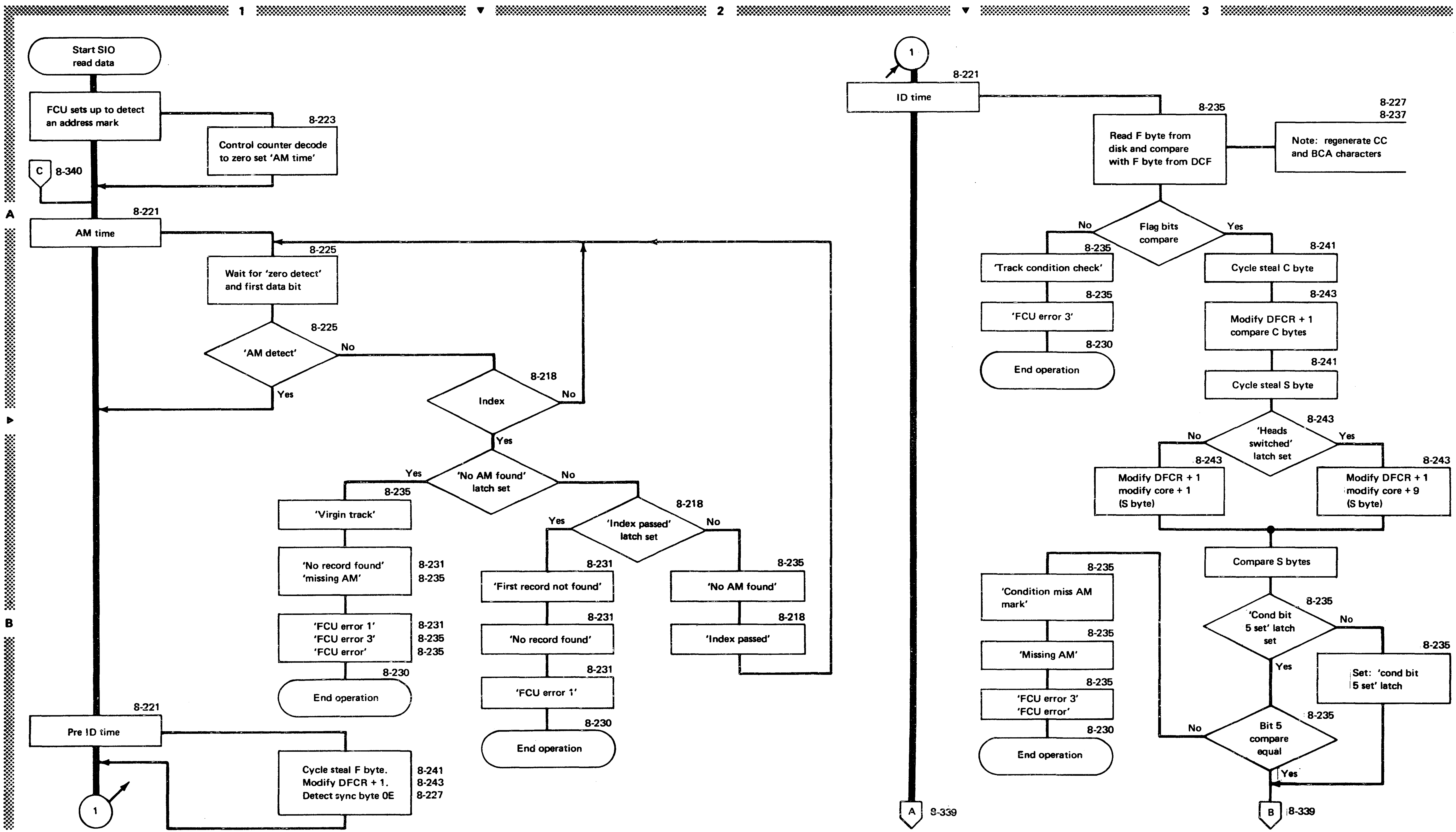
This instruction starts a scan operation similar to the scan-equal command except that this operation ends when the first disk data field is found that is lower than or equal to the masked data field in core.

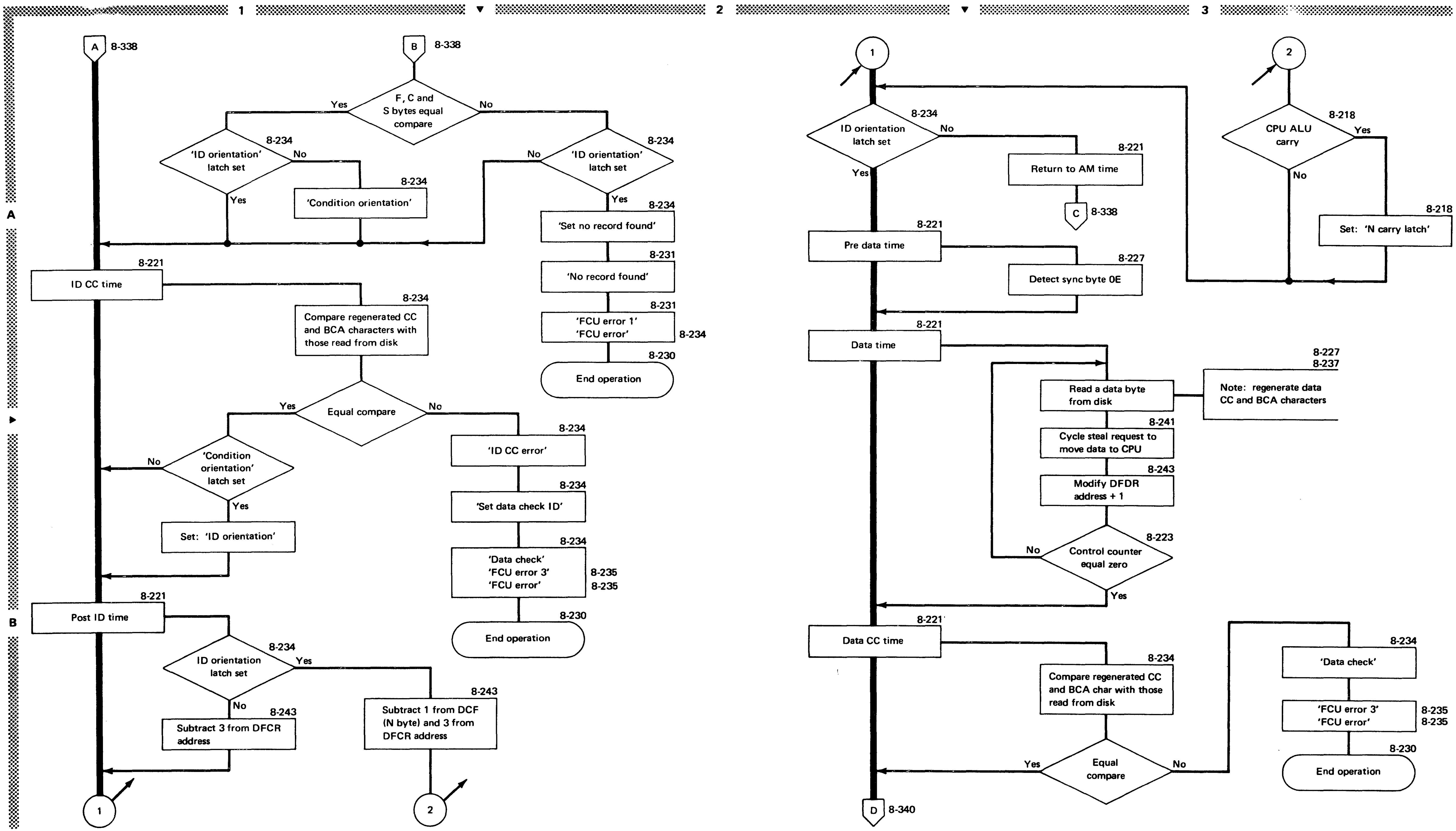
A scan-found condition is indicated to test I/O and branch or advance-program-level instruction after the end of the scan if a data field is found on the disk that is equal to or lower than the field in core. The scan equal bit of the device status is set if the two fields are equal. All other conditions are the same as in the scan-equal operation.

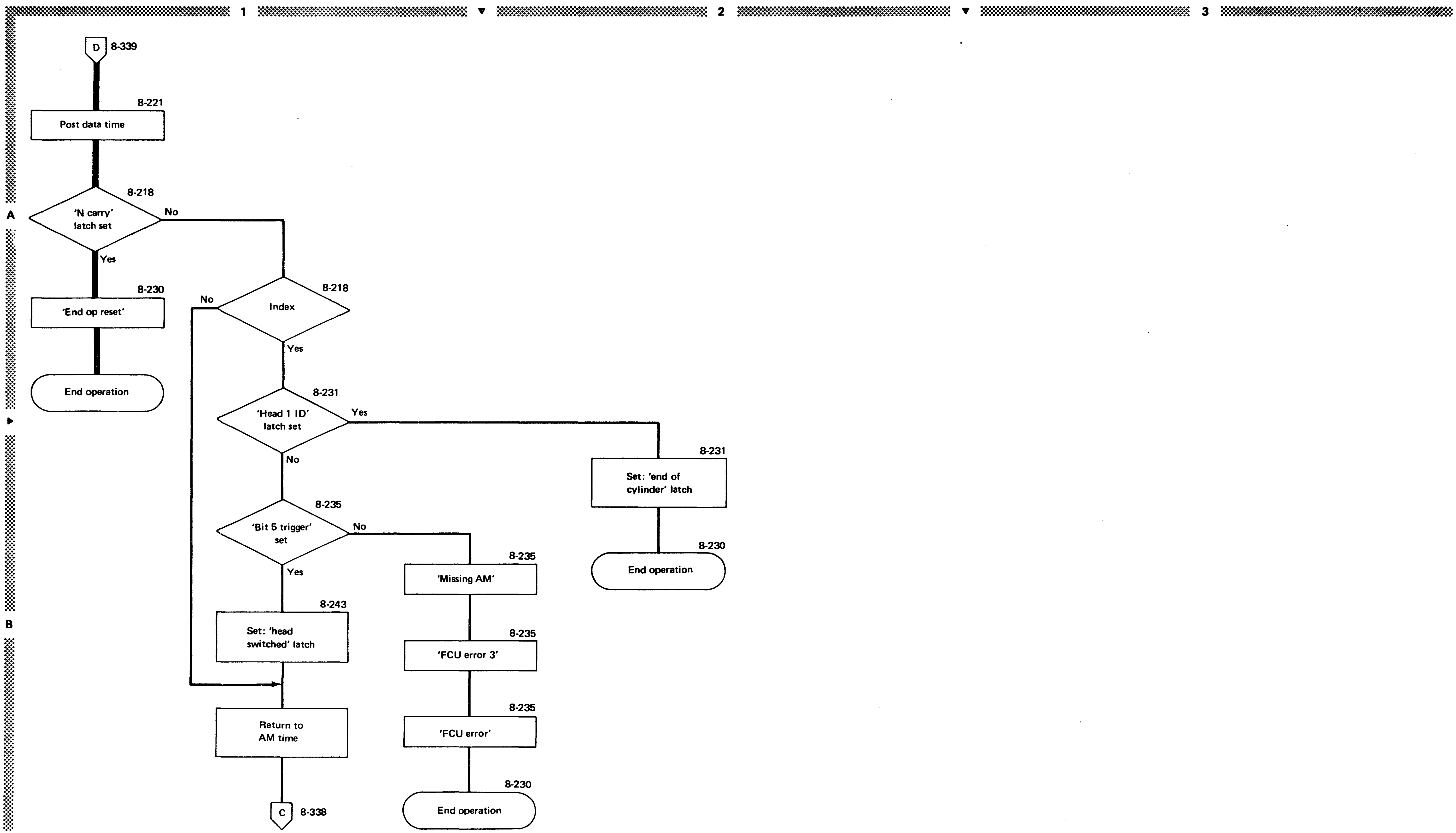
Scan High or Equal

This instruction starts a scan operation similar to the scan-equal command except that this operation ends when the first disk data field is found that is higher than or equal to the masked data field in core.

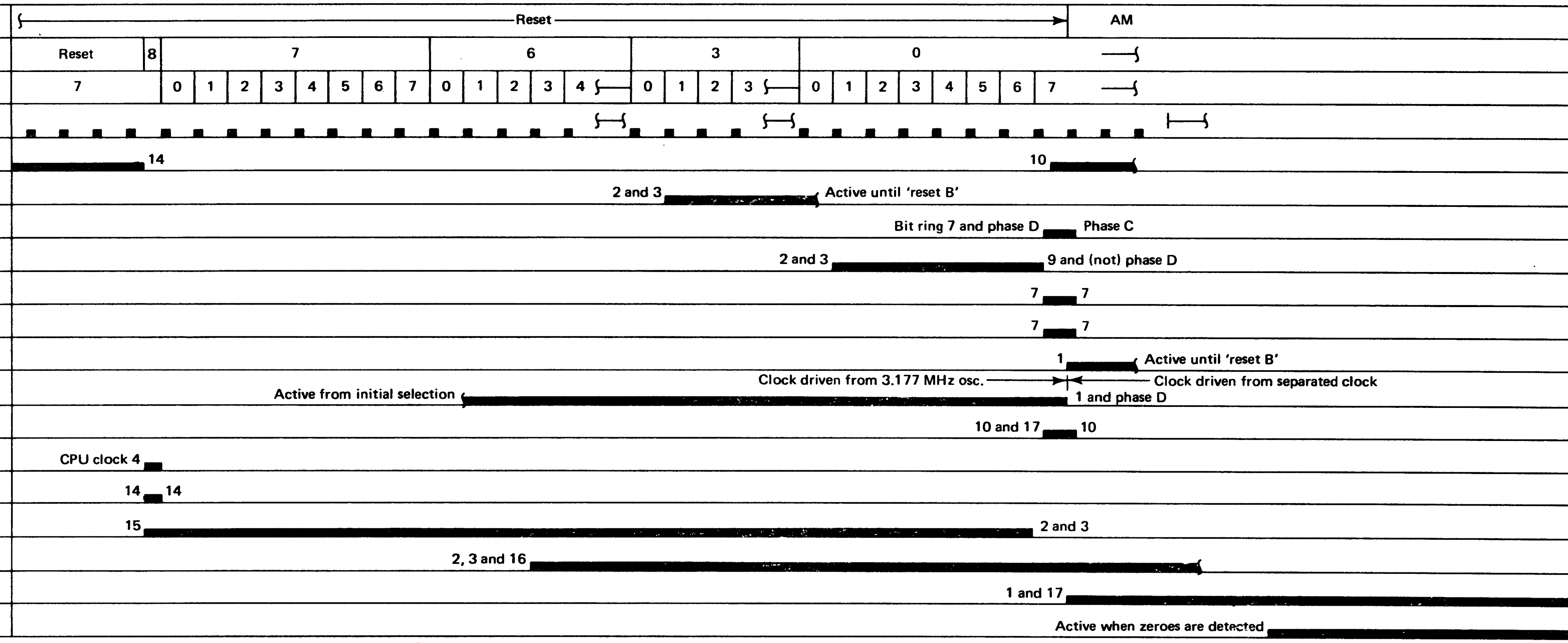
A scan-found condition is indicated to a test I/O and branch or advance-program-level instruction after termination of the scan if a data field is found on the disk that is equal to or higher than the data field in core. The scan equal bit of the device status is set if the two fields are equal. All other conditions are the same as in the scan-equal operation.


1
2
3
A
B
Start SIO read data
FCU sets up to detect an address mark
8-223
Control counter decode to zero set 'AM time'
C 8-340
8-221
AM time
8-225
Wait for 'zero detect' and first data bit
8-225
'AM detect'
No
Yes
8-218
Index
No
Yes
'No AM found' latch set
Yes
No
8-235
'Virgin track'
'No record found' 'missing AM'
8-231
8-235
'FCU error 1' 'FCU error 3' 'FCU error'
8-231
8-235
8-235
8-230
End operation
8-218
'Index passed' latch set
Yes
No
8-231
'First record not found'
8-231
'No record found'
8-231
'FCU error 1'
8-230
End operation
8-235
'No AM found'
8-218
'Index passed'
8-221
Pre ID time
Cycle steal F byte. Modify DFCR + 1. Detect sync byte 0E
8-241
8-243
8-227
1
1
8-221
ID time
8-235
Read F byte from disk and compare with F byte from DCF
8-227
8-237
Note: regenerate CC and BCA characters
Flag bits compare
No
Yes
8-235
'Track condition check'
8-235
'FCU error 3'
8-230
End operation
8-241
Cycle steal C byte
8-243
Modify DFCR + 1 compare C bytes
8-241
Cycle steal S byte
8-243
'Heads switched' latch set
No
Yes
8-243
Modify DFCR + 1 modify core + 1 (S byte)
8-243
Modify DFCR + 1 modify core + 9 (S byte)
Compare S bytes
8-235
'Condition miss AM mark'
8-235
'Missing AM'
8-235
'FCU error 3' 'FCU error'
8-230
End operation
8-235
'Cond bit 5 set' latch set
No
Yes
8-235
Set: 'cond bit 5 set' latch
8-235
Bit 5 compare equal
No
Yes
A 8-339
B 8-339


1
2
3
A
B
A 8-338
B 8-338
F, C and S bytes equal compare
Yes
No
'ID orientation' latch set
'Condition orientation'
'Set no record found'
'No record found'
'FCU error 1' 'FCU error'
End operation
ID CC time
Compare regenerated CC and BCA characters with those read from disk
Equal compare
'Condition orientation' latch set
Set: 'ID orientation'
'ID CC error'
'Set data check ID'
'Data check' 'FCU error 3' 'FCU error'
Post ID time
ID orientation latch set
Subtract 3 from DFCR address
Subtract 1 from DCF (N byte) and 3 from DFCR address
ID orientation latch set
Return to AM time
C 8-338
Pre data time
Detect sync byte 0E
Data time
Read a data byte from disk
Note: regenerate data CC and BCA characters
Cycle steal request to move data to CPU
Modify DFDR address + 1
Control counter equal zero
CPU ALU carry
Set: 'N carry latch'
Data CC time
Compare regenerated CC and BCA char with those read from disk
'Data check'
'FCU error 3' 'FCU error'
D 8-340
8-221
8-227
8-230
8-231
8-234
8-235
8-218
8-223
8-237
8-241
8-243


1
2
3
A
B
D 8-339
8-221
Post data time
8-218
'N carry' latch set
No
Yes
8-230
'End op reset'
End operation
8-218
Index
No
Yes
8-231
'Head 1 ID' latch set
Yes
No
8-231
Set: 'end of cylinder' latch
8-230
End operation
8-235
'Bit 5 trigger' set
No
Yes
8-235
'Missing AM'
8-235
'FCU error 3'
8-235
'FCU error'
8-230
End operation
8-243
Set: 'head switched' latch
Return to AM time
C 8-338

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Clock	8-247
5	Bit ring inhibit	8-225
6	CCR pre advance gate	8-223
7	CCR advance gate	8-223
8	Count zero gate	8-223
9	Count zero reset	8-223
10	Pending AM time	8-221
11	Condition 1st AM	8-221
12	Clock gate	8-217
13	Set CC register pos 1 on	8-227
14	Start op	8-230
15	Set counter to 8	8-223
16	Condition read gate	8-218
17	Read gate	8-218
18	Search address mark	8-225
19	Zero detect	8-227



In the initial selection flow chart, the file control unit was set up for a read data read verify, read data diagnostic or scan operation. The next objective is to locate an address mark. Address mark detection is started when zeros in the sector gaps are detected to indicate to the file control unit that an address mark is approaching the read heads in the drive. The next data bit read, after zeros detect, starts the FCU looking for the address mark.

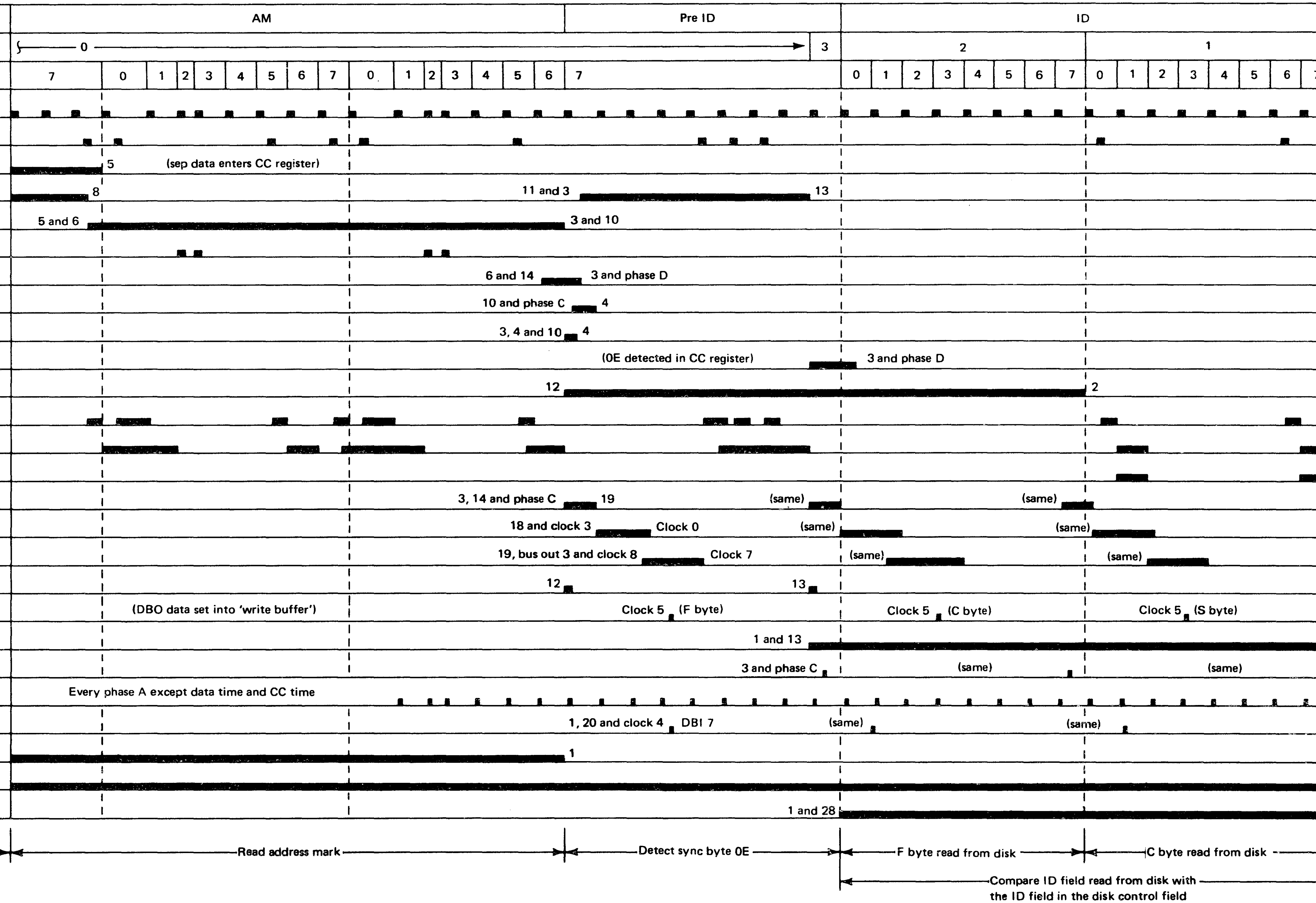
The timing charts that follow show this sequence: (1) locate an address mark, (2) successfully detect the address mark, (3) compare the ID field on disk with the disk control field in core storage (a non compare results), (4) locate another address mark, (5) compare disk ID field and disk control field (a successful compare results), (6) read the data field from disk, (7) and end the operation.

1 ▼ 2 ▼ 3

A

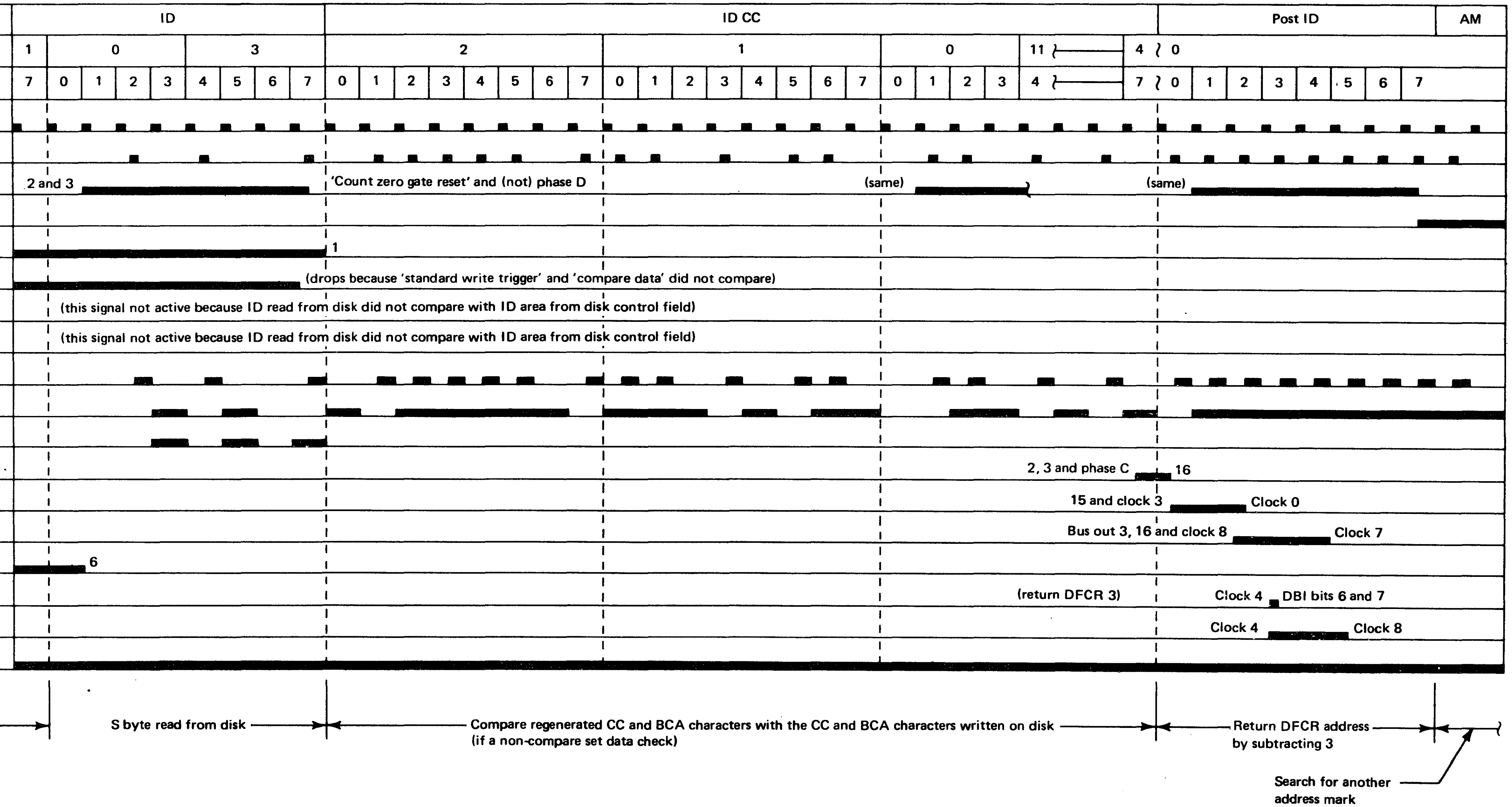
B

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Separated clock	8-237
5	Separated data	8-237
6	Zero detect	8-227
7	Bit ring inhibit	8-225
8	Start AM search	8-225
9	AM indicate	8-225
10	AM detect 1	8-225
11	AM detect 2	8-225
12	AM detect	8-225
13	Sync detect latch	8-227
14	ID area	8-241
15	Standard read data	8-227
16	Compare data	8-227
17	Standard write trigger	8-251
18	Cond prior request	8-241
19	Prior request latch	8-241
20	Data cycle request	8-241
21	CC register reset	8-227
22	Set write buffer	8-241
23	Input data time	8-243
24	Xfer write buffer to read buffer	8-241
25	Shift read buffer	8-241
26	Constant on DBI	8-243
27	Search address mark	8-225
28	Read gate	8-218
29	ID compare gate time	8-234



1 2 3

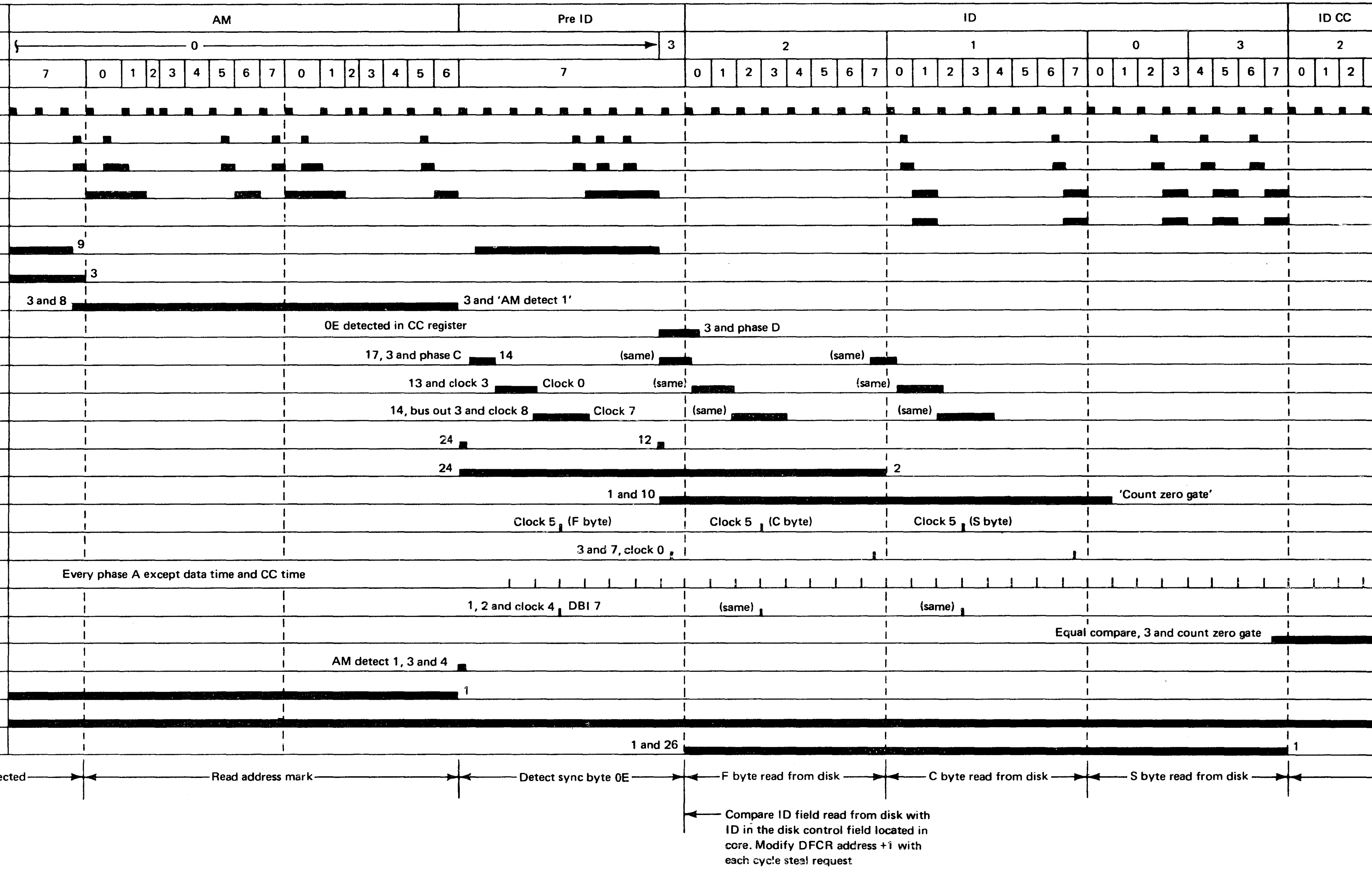
No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Separated clock	8-237
5	Separated data	8-237
6	Count zero gate	8-223
7	Bit ring inhibit	8-225
8	ID compare gate time	8-234
9	Equal compare	8-234
10	Condition orientation	8-234
11	ID orientation	8-234
12	Standard read data	8-227
13	Compare data	8-227
14	Standard write trigger	8-251
15	Condition prior request	8-241
16	Prior request latch	8-241
17	Data cycle request gate	8-241
18	Input data time	8-243
19	Constant on DBI	8-243
20	ALU binary subtract	8-243
21	Read gate	8-218



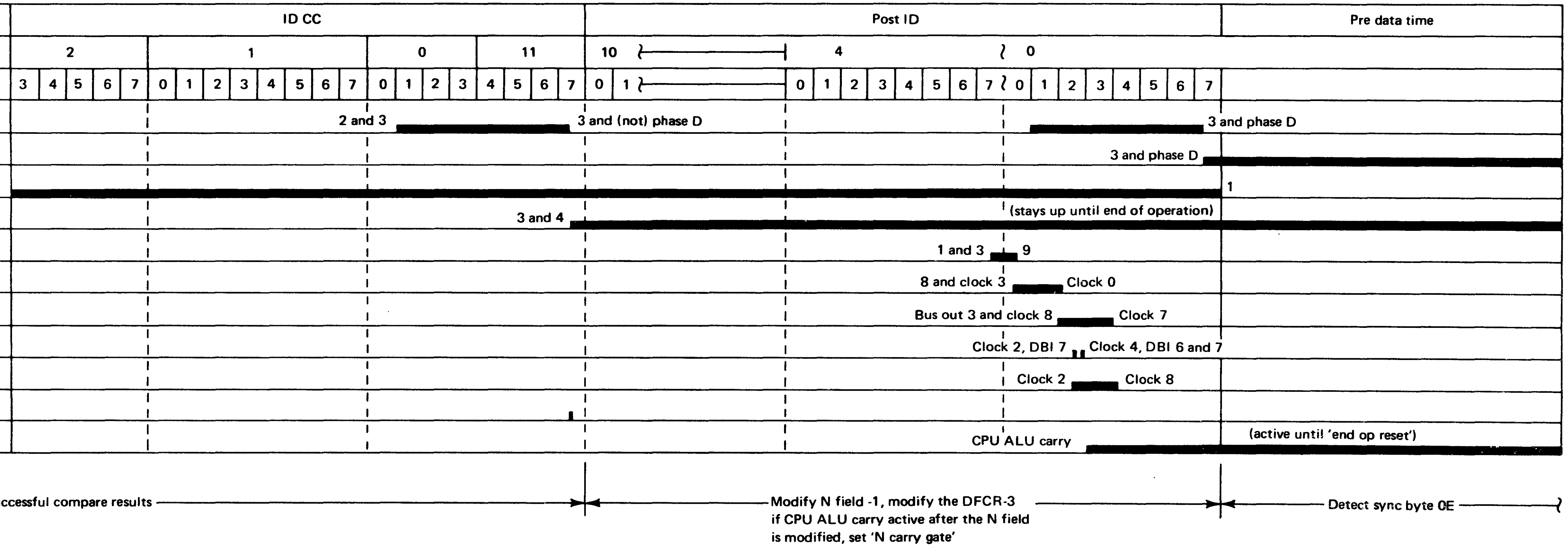
A

B

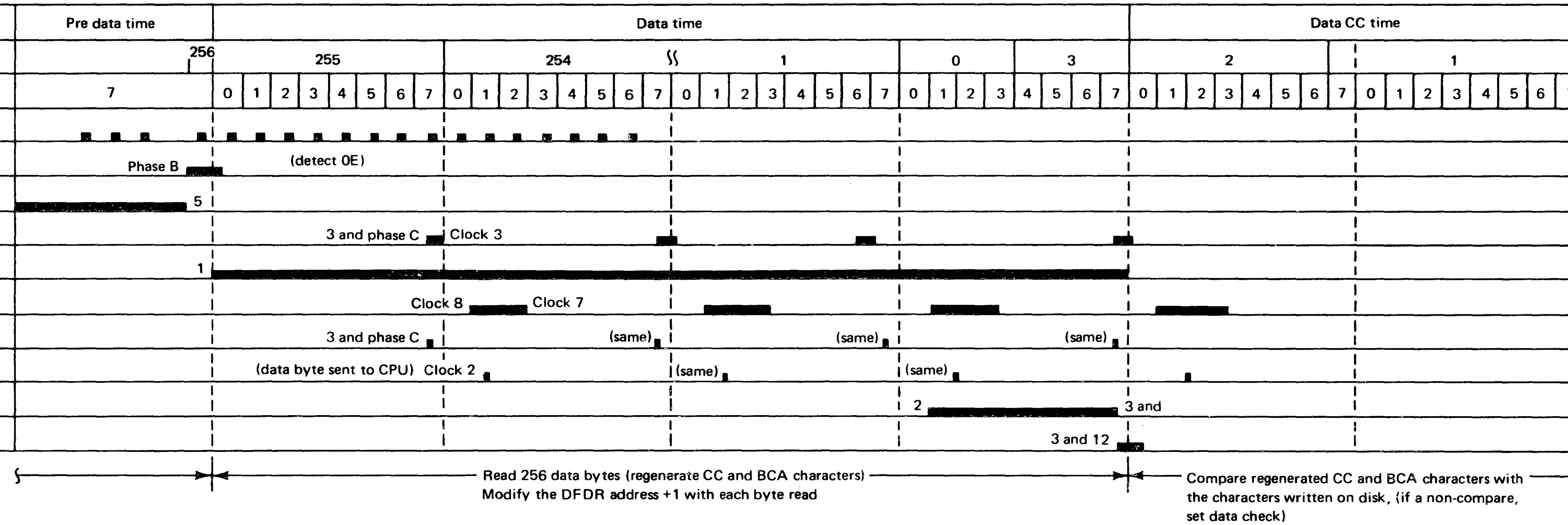
No	Signal name	Diagram
1	Cycle control ring	8-223
2	Control counter	8-223
3	Bit ring	8-225
4	Separated clock	8-237
5	Separated data	8-237
6	Standard read data	8-227
7	Compare data	8-227
8	Standard write trigger	8-251
9	Bit ring inhibit	8-225
10	Zero detect	8-227
11	Start AM search	8-225
12	Sync detect latch	8-227
13	Condition prior request	8-241
14	Prior request latch	8-241
15	Data cycle request gate	8-241
16	CC register reset	8-227
17	ID area	8-241
18	Input data time	8-243
19	Set write buffer	8-241
20	Xfer writer to read buffer	8-241
21	Shift read buffer	8-241
22	Constant on DBI	8-243
23	Condition orientation	8-234
24	AM detect	8-225
25	Search address mark	8-225
26	Read gate	8-218
27	ID compare gate time	8-234



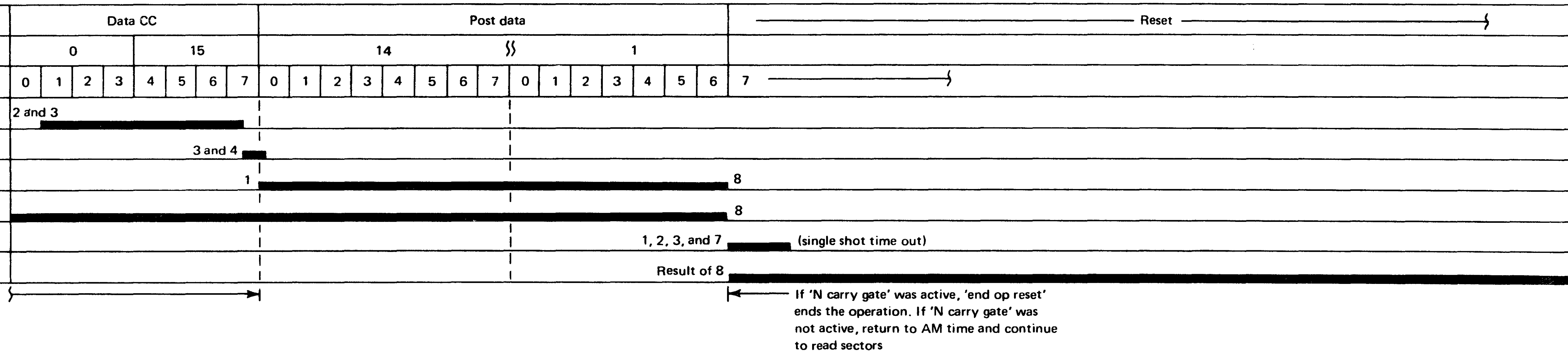
No	Signal name	Diagram
1	Cycle control ring	8-223
2	Control counter	8-223
3	Bit ring	8-225
4	Count zero gate	8-223
5	Bit ring inhibit	8-225
6	Condition orientation	8-234
7	ID orientation	8-234
8	Condition prior request	8-241
9	Prior request latch	8-241
10	Data cycle request gate	8-241
11	Constant on DBI	8-243
12	ALU binary subtract	8-243
13	Start orientation reset	8-234
14	N carry gate	8-218



No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-221
4	Separated data	8-237
5	Sync detect latch	8-227
6	Bit ring inhibit	8-225
7	Condition prior request	8-241
8	Data area	8-241
9	Data cycle request gate	8-241
10	Xfer write buffer to read buffer	8-241
11	Gate data to DBI	8-241
12	Count zero gate	8-241
13	CCR adv gate	8-241



No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Count zero gate	8-223
5	CCR advance gate	8-221
6	Clock gate	8-217
7	N carry gate	8-218
8	End op reset	8-230
9	Bit ring inhibit	8-225



1 2 3

A

READ IDENTIFIER OPERATION

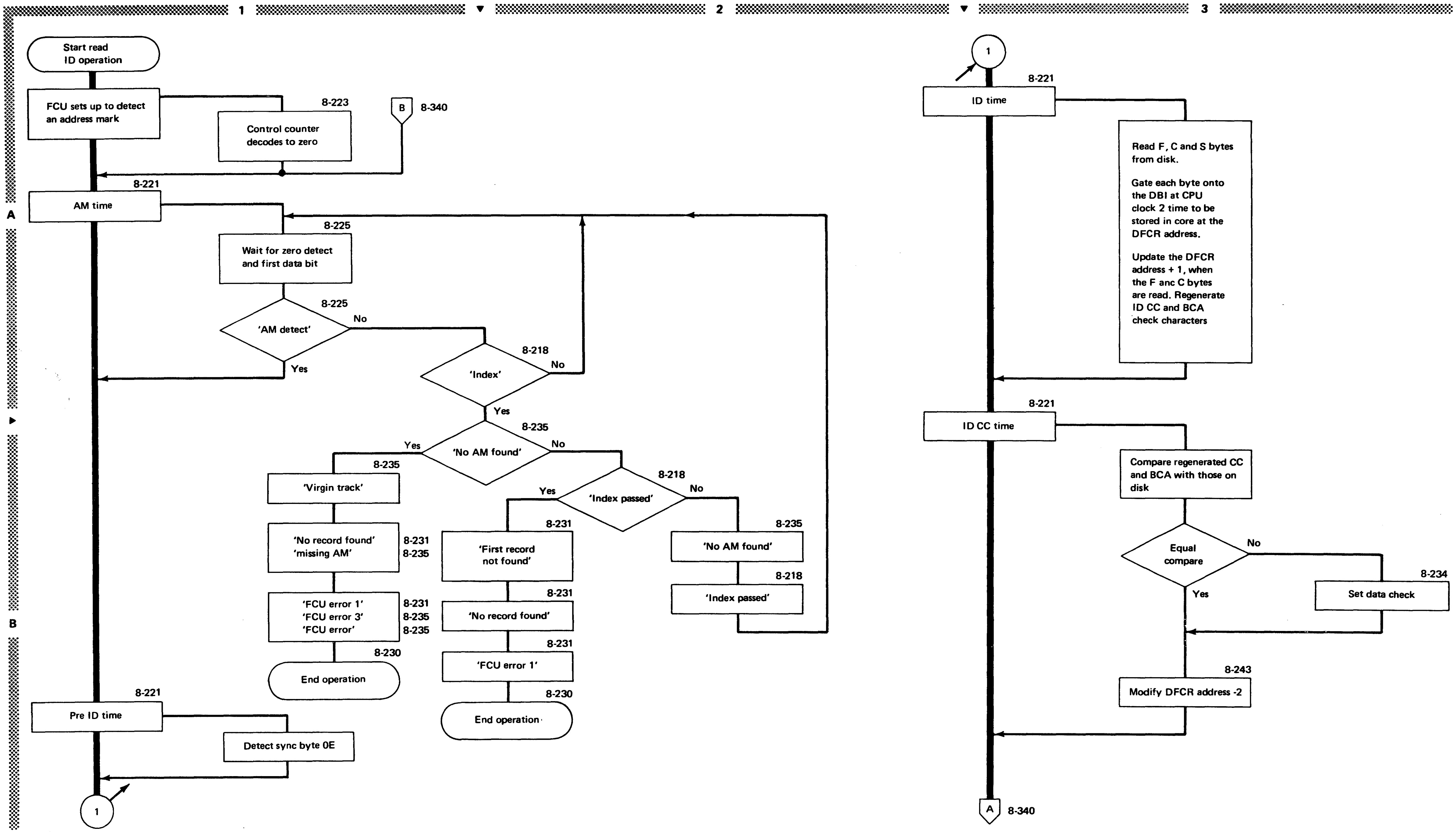
- Transfers the first identifier field (3 bytes) of a sector to pass under the read heads into core storage at an address specified by the DFCR.
- If an error is detected in the first ID field, the DFCR address is returned to its original address and the next ID field is read.
- Operation ends when an ID field is read without an error, a no record found is detected, or an equipment check occurs.
- The control unit is busy to any new operation.
- When the operation ends, the disk control field in core contains the FCS information of the ID field read from disk. The DFCR contains the original address after an equipment check.

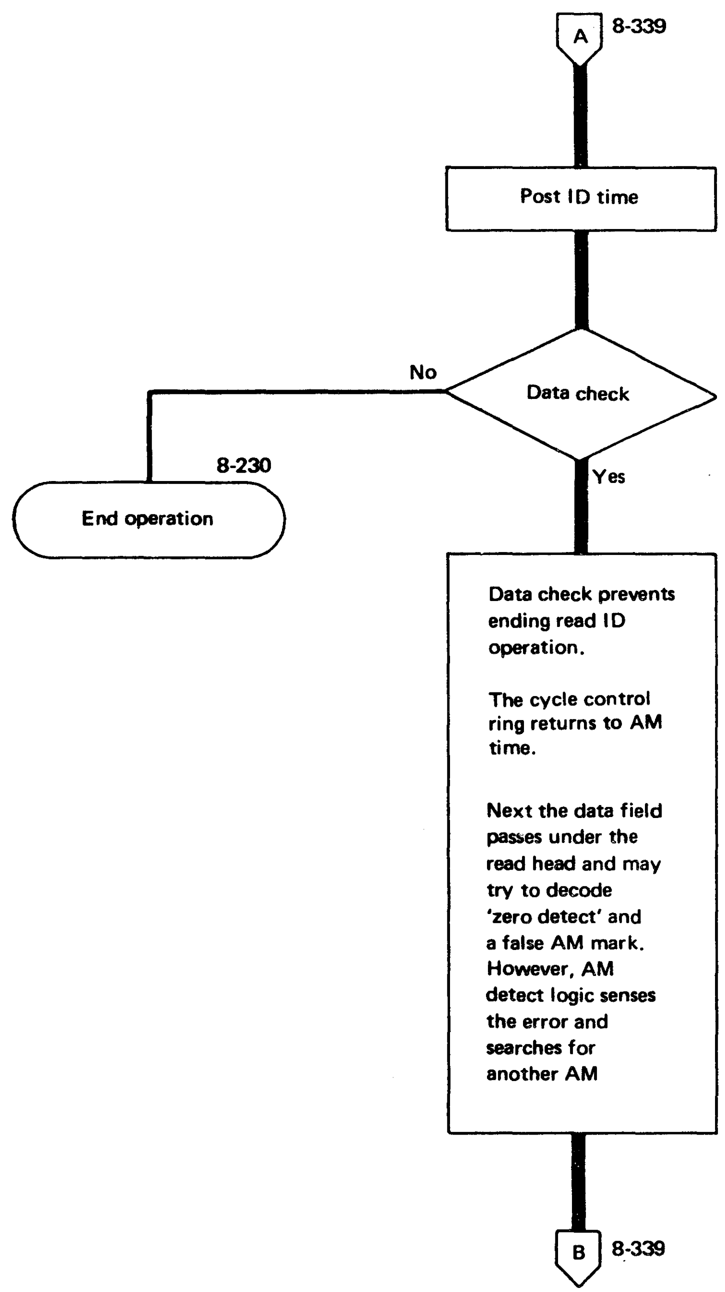
This instruction initiates the transfer of a sector identifier (3 bytes–F, C, and S) from the selected disk to core storage. The operation starts with the next identifier to come under the head. It transfers the first sector identifier it find to the address designated by DFCR. If an error is found in this identifier, the next sector identifier is read and transferred to core starting at the original address contained in DFCR. The operation is terminated by the transfer of the first sector identifier without data check. A no-record status found during a read ID instruction indicates that an error-free ID was not found on the selected track.

The control unit is busy to any new operation except sense I/O while performing a read-identifier operation. The control unit does not use the information contained in the disk-control field during this period. At the end of this operation, the first three bytes (F, C, S) of the disk-control field contain the last sector identifier read from the file. The last byte (N field) of the disk-control field is not changed.

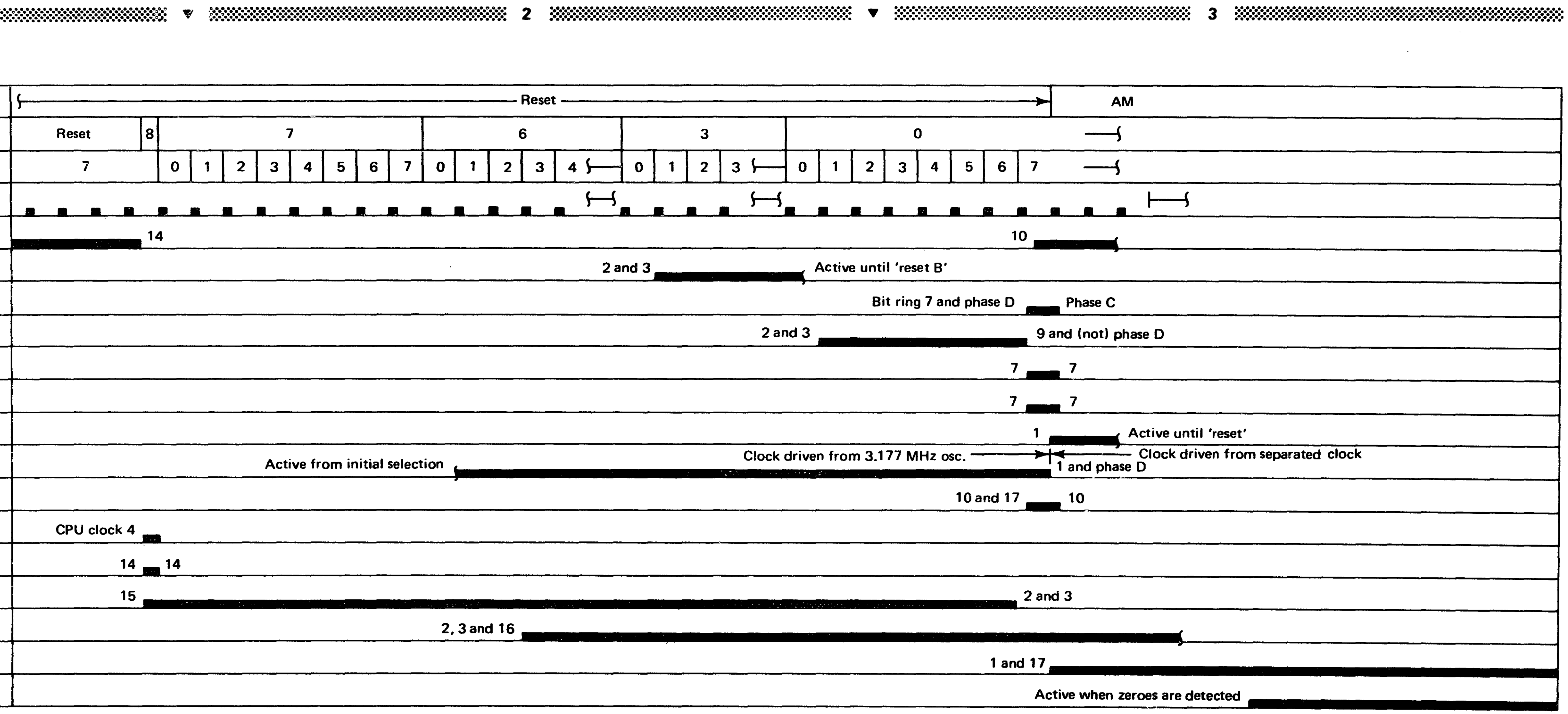
This operation does not switch heads. At the end of the operation, DFCR contains the original address unless there is an equipment check.

B


1
2
3
A
B
Start read ID operation
FCU sets up to detect an address mark
8-223
Control counter decodes to zero
B 8-340
8-221
AM time
8-225
Wait for zero detect and first data bit
8-225
'AM detect'
No
Yes
8-218
'Index'
No
Yes
8-235
'No AM found'
Yes
No
8-235
'Virgin track'
'No record found' 'missing AM' 8-231 8-235
'FCU error 1' 'FCU error 3' 'FCU error' 8-231 8-235 8-235
8-230
End operation
8-218
'Index passed'
Yes
No
8-231
'First record not found'
8-231
'No record found'
8-231
'FCU error 1'
8-230
End operation
8-235
'No AM found'
8-218
'Index passed'
8-221
Pre ID time
Detect sync byte 0E
1
1
8-221
ID time
Read F, C and S bytes from disk.
Gate each byte onto the DBI at CPU clock 2 time to be stored in core at the DFCR address.
Update the DFCR address + 1, when the F anc C bytes are read. Regenerate ID CC and BCA check characters
8-221
ID CC time
Compare regenerated CC and BCA with those on disk
Equal compare
No
Yes
8-234
Set data check
8-243
Modify DFCR address -2
A 8-340

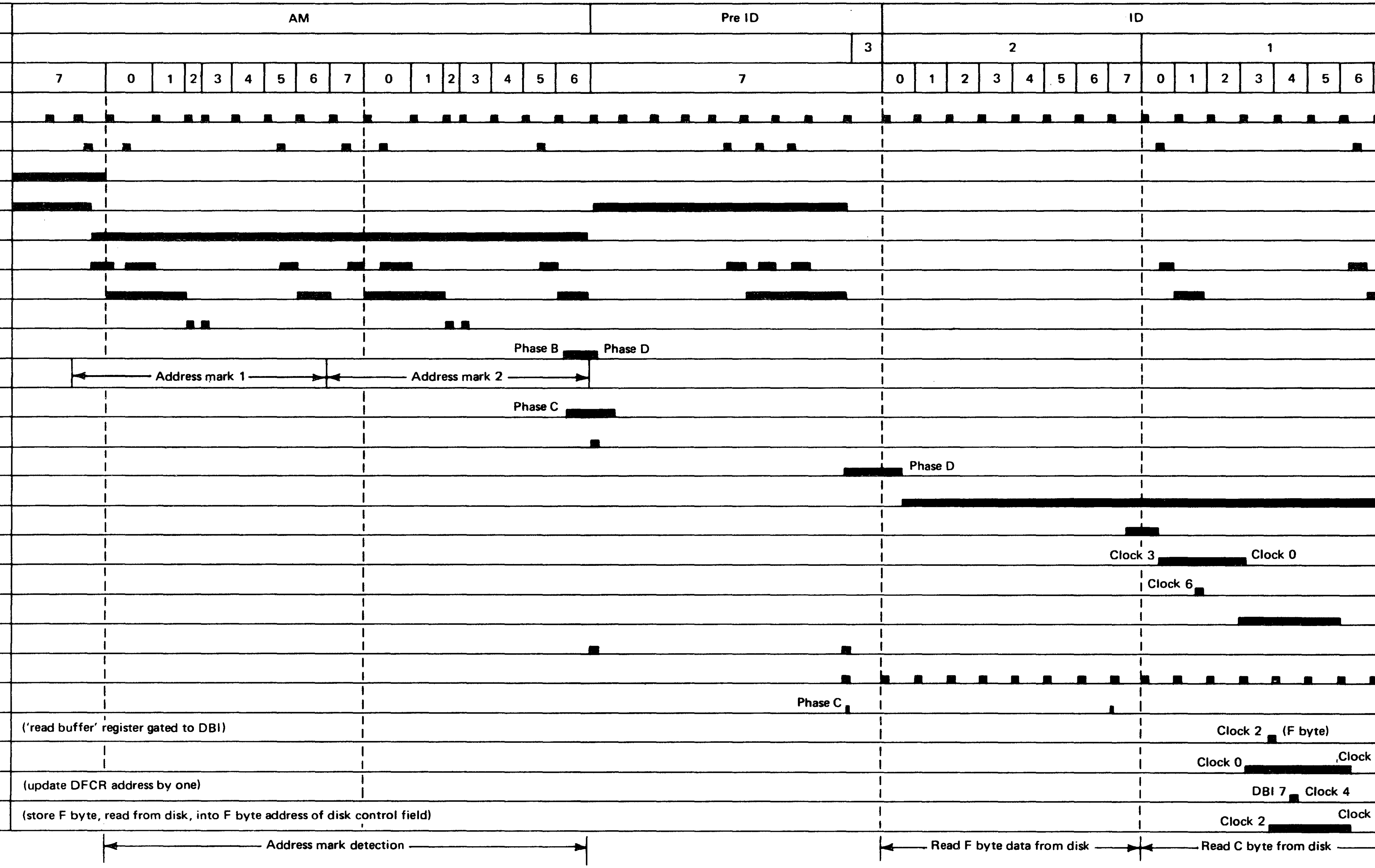

A 8-339
Post ID time
Data check
No
Yes
8-230
End operation
Data check prevents ending read ID operation.
The cycle control ring returns to AM time.
Next the data field passes under the read head and may try to decode 'zero detect' and a false AM mark. However, AM detect logic senses the error and searches for another AM
B 8-339

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Clock	8-247
5	Bit ring inhibit	8-225
6	CCR pre advance gate	8-223
7	CCR advance gate	8-223
8	Count zero gate	8-223
9	Count zero reset	8-223
10	Pending AM time	8-221
11	Condition 1st AM	8-221
12	Clock gate	8-217
13	Set CC register pos 1 on	8-227
14	Start op	8-230
15	Set counter to 8	8-223
16	Condition read gate	8-218
17	Read gate	8-218
18	Search address mark	8-225
19	Zero detect	8-227



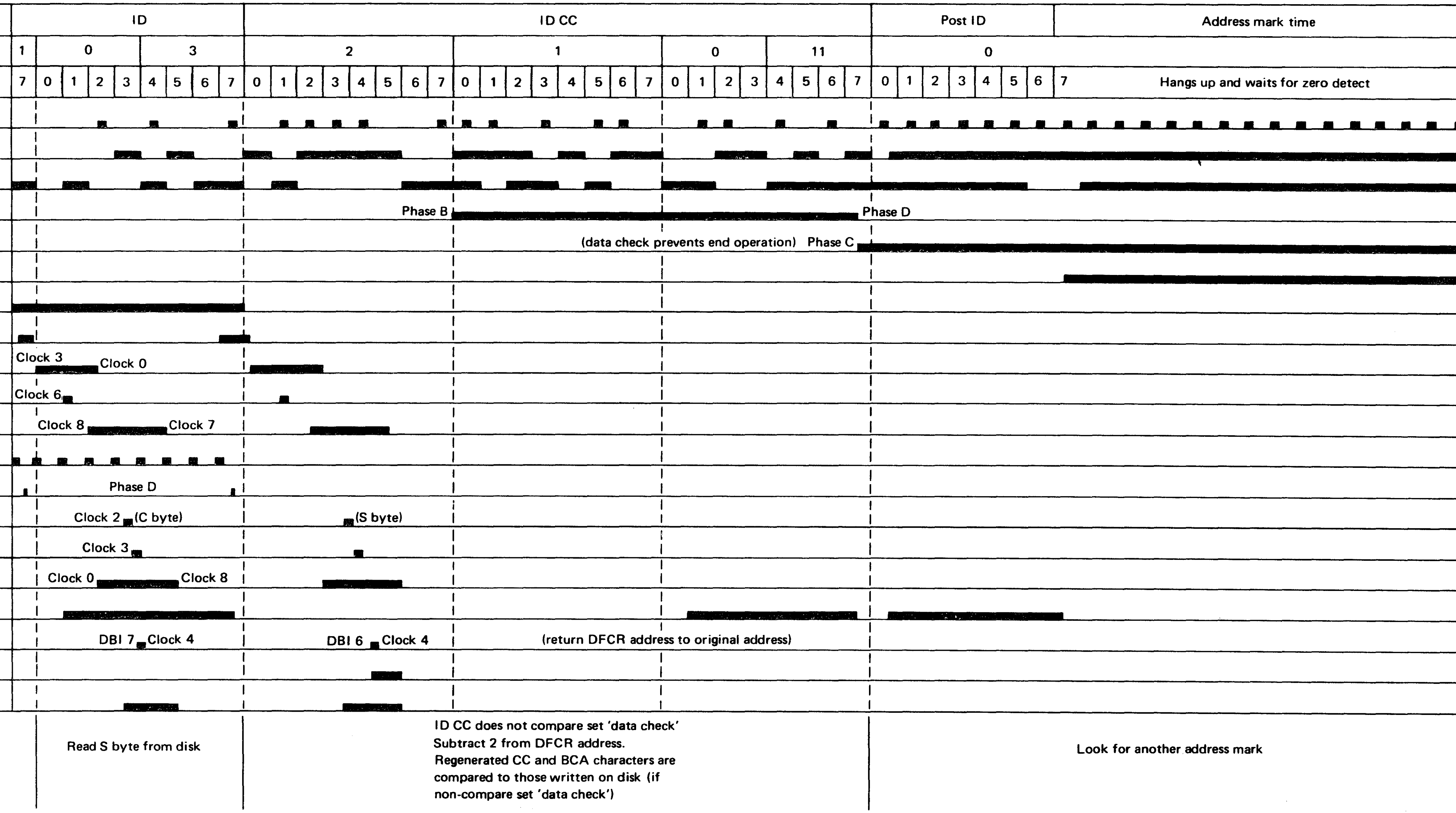
In the initial selection flow chart, the file control unit was set up for a read identifier operation. The next objective is to locate an address mark. Address mark detection is started when zeros in the sector gaps are detected to indicate to the file control unit that an address mark is approaching the read heads in the drive. The next data bit read, after zeros detect, starts the FCU looking for the address mark.

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Separated clock	8-237
5	Separated data	8-237
6	Zero detect	8-227
7	Bit ring inhibit	8-225
8	Start AM search	8-225
9	Standard read data	8-227
10	Compare data	8-227
11	Address mark indicate	8-225
12	Address mark detect 1	8-225
13	Address mark triggers	8-225
14	Address mark detect 2	8-225
15	Address mark detect	8-225
16	Sync detect latch	8-227
17	ID area	8-241
18	Condition prior request	8-241
19	Prior request latch	8-241
20	Prior request 3	8-241
21	Data cycle request gate	8-241
22	CC register reset	8-227
23	Shift write buffer	8-241
24	Xfer write buffer to read buffer	8-241
25	Gate data to DBI	8-241
26	DBI parity generate	8-239
27	Constant on DBI	8-243
28	Store data and block SDR - B register	8-243



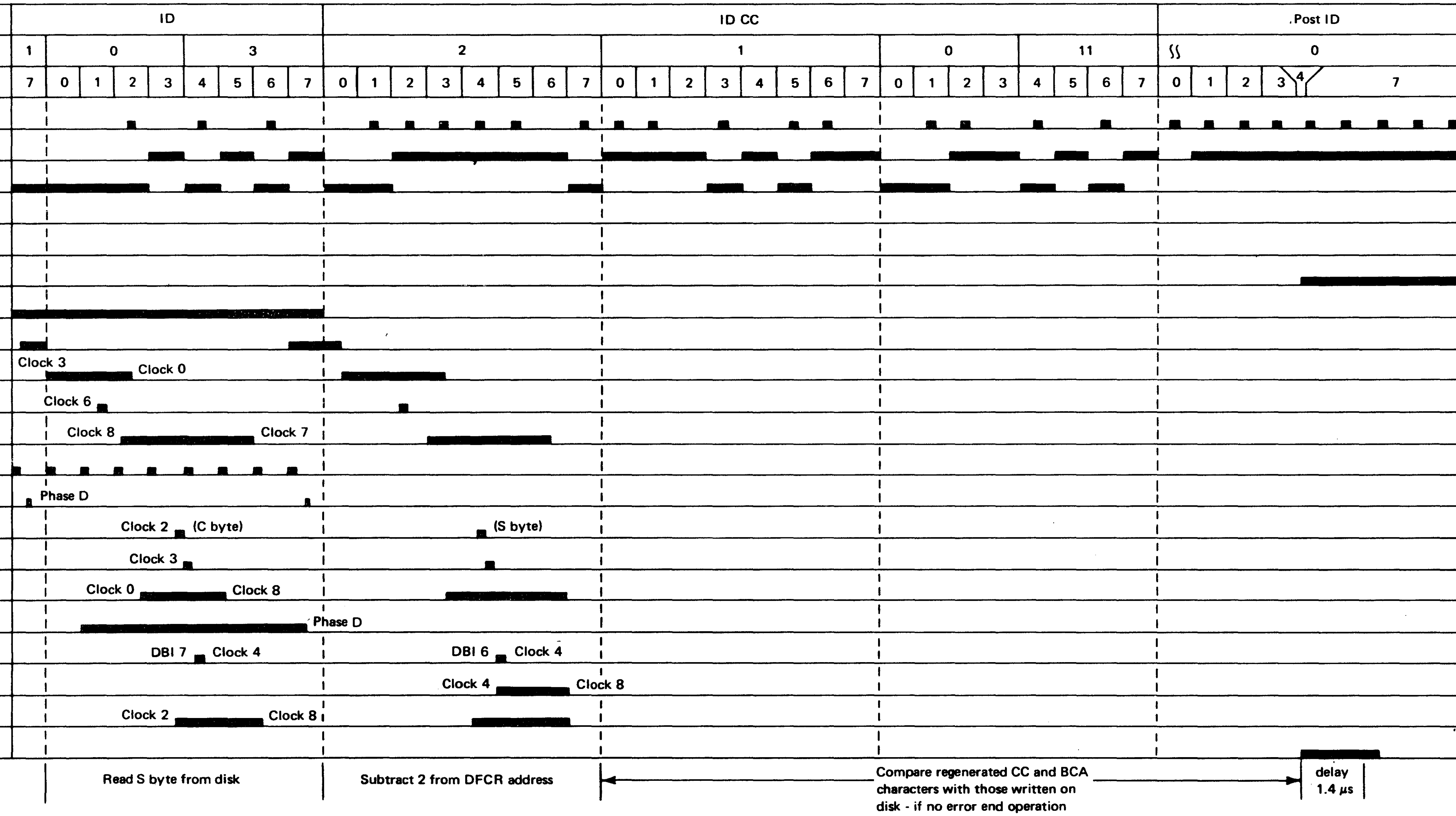
A

No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Separated data	8-239
5	Compare data	8-227
6	CC register position 17	8-227
7	ID CC error	8-234
8	Data check	8-234
9	Bit ring inhibit	8-225
10	ID area	8-241
11	Condition prior request	8-241
12	Prior request latch	8-241
13	Prior request 3	8-241
14	Data cycle request gate	8-241
15	Shift write buffer	8-241
16	Reset write buffer	8-241
17	Gate data to DBI	8-241
18	Reset read buffer	8-241
19	DBI parity generate	8-239
20	Count zero gate	8-223
21	Constant on DBI	8-243
22	ALU binary subtract	8-243
23	Store data and block SDR B register	8-243

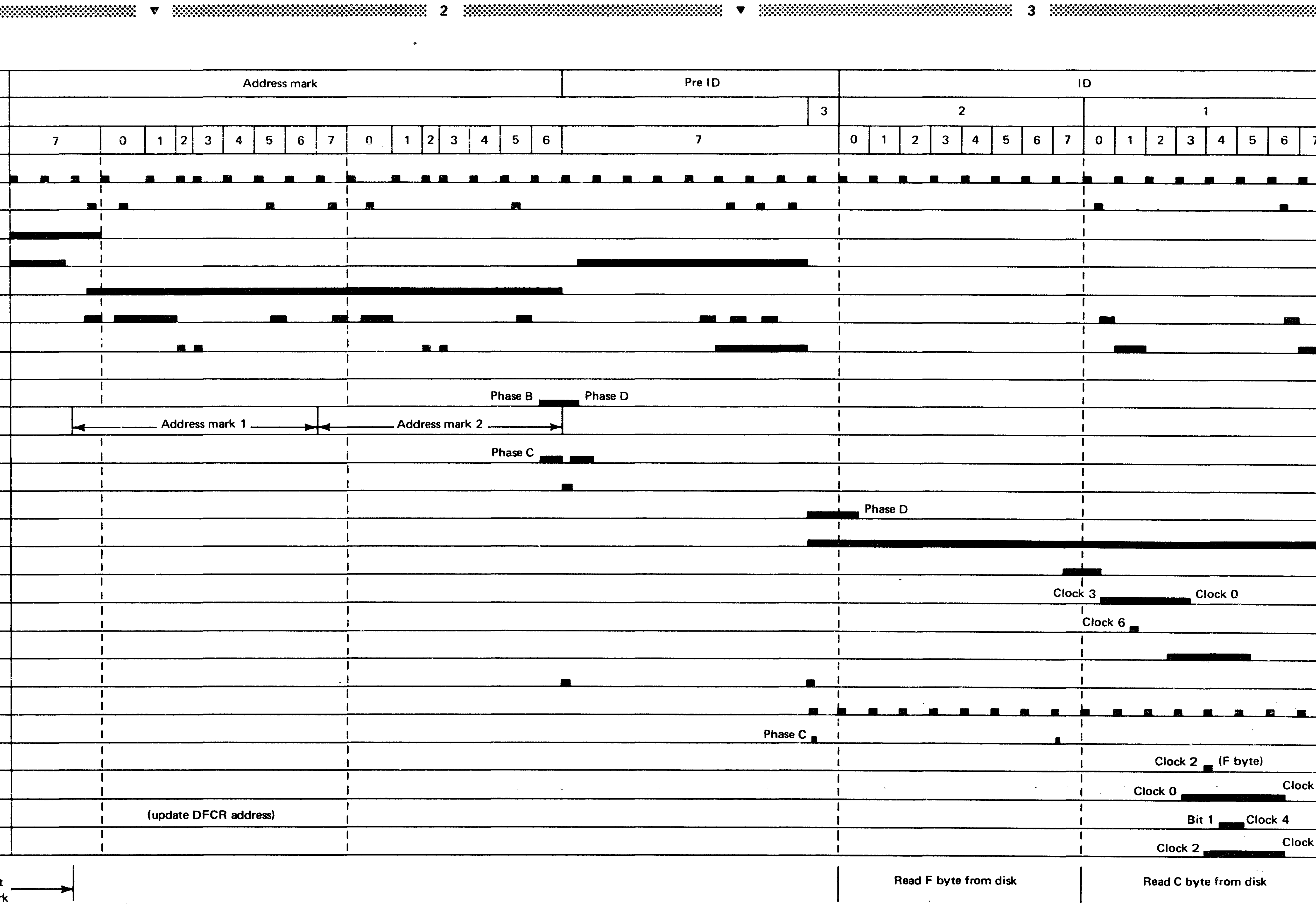


B

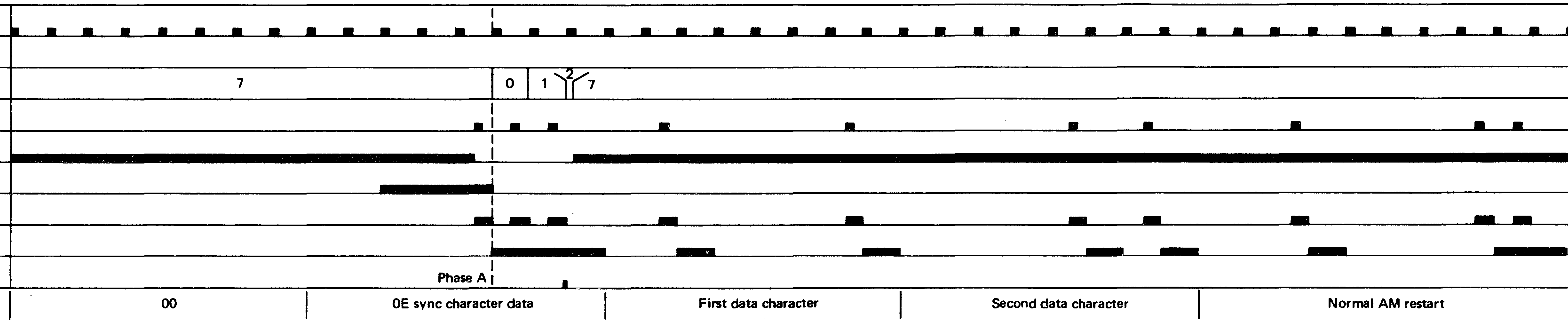
No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Separated data	8-237
5	Compare data	8-227
6	CC register position 17	8-227
7	ID CC error	8-234
8	Data check	8-234
9	Bit ring inhibit	8-225
10	ID area	8-241
11	Cond prior req	8-241
12	Prior request latch	8-241
13	Prior request 3	8-241
14	Data cycle request gate	8-241
15	Shift write buffer	8-241
16	Reset write buffer	8-241
17	Gate data to DBI	8-241
18	Reset read buffer	8-241
19	DBI parity generate	8-239
20	Count zero gate	8-223
21	Constant on DBI	8-243
22	ALU binary subtract	8-243
23	Store data and block SDR - B register	8-243
24	Pure end op reset	8-230



No	Signal name	Diagram
1	Cycle control ring	8-221
2	Control counter	8-223
3	Bit ring	8-225
4	Separated clock	8-237
5	Separated data	8-237
6	Zero detect	8-227
7	Bit ring inhibit	8-225
8	Start AM search	8-225
9	Standard read data	8-227
10	Compare data	8-227
11	Address mark indicate	8-225
12	Address mark detect 1	8-225
13	Address mark trigger's	8-225
14	Address mark detect 2	8-225
15	Address mark detect	8-225
16	Sync detect latch	8-227
17	ID area	8-241
18	Condition prior request	8-241
19	Prior request latch	8-241
20	Prior request 3	8-241
21	Data cycle request gate	8-241
22	CC register reset	8-227
23	Shift write buffer	8-241
24	Xfer write buffer to read buffer	8-241
25	Gate data to DBI	8-241
26	DBI parity generate	8-239
27	Constant on DBI	8-243
28	Store data and block SDR - B register	8-243



No	Signal name	Diagram
1	Clock	8-247
2	Control counter	8-223
3	Bit ring	8-225
4	Separated data	8-239
5	Bit ring inhibit	8-225
6	Zero detect	8-227
7	Standard read data	8-227
8	Compare read data	8-227
9	Reset start AM search	8-225



Note: While looking for the next address mark, the data field will pass under the read head. Zeros in the gap preceding the data field will set 'zero detect'. Normally the next bit will be the first bit of the address mark, however in this example it is the sync character 0E. The address mark detect circuits sense the error and cause 'AM restart'

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