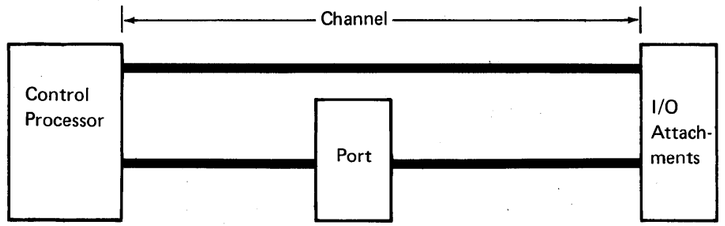
Contents

Channel

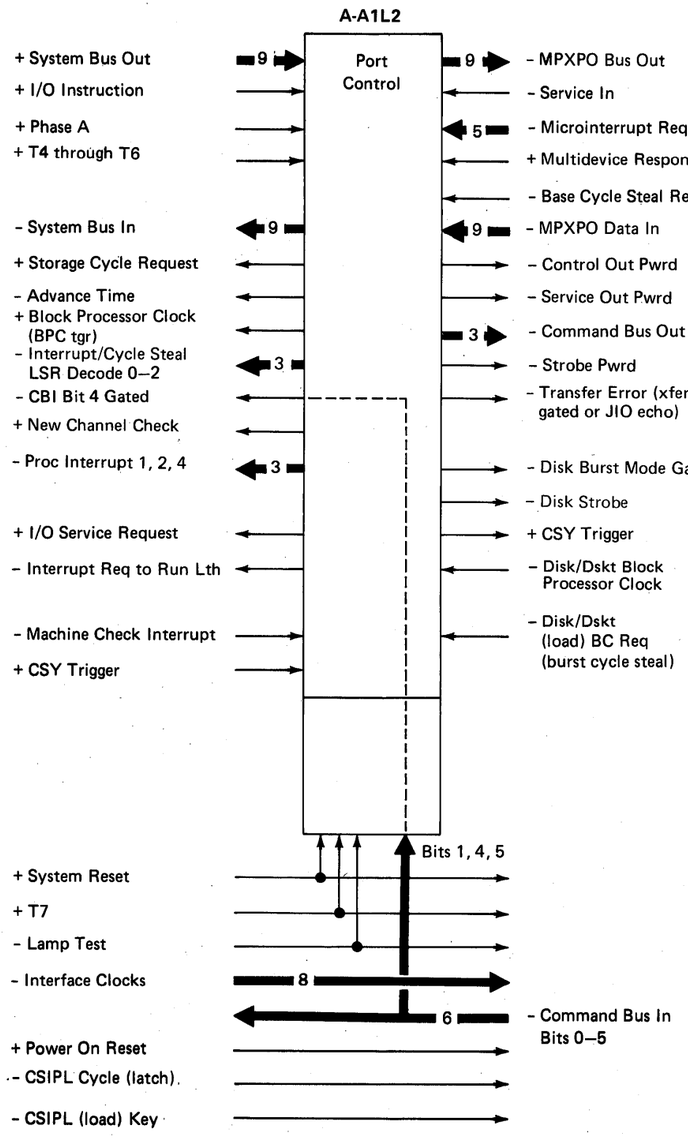
INTRODUCTION

The channel contains data buses and synchronizing controls that move the data and commands between the control processor, main storage or control storage, and the I/O attachments.

The channel has lines that go directly from the control processor to the I/O attachments and lines that go to a port and then to the I/O attachments.



The channel, as used in System/34, is the internal link between the control processor and the logic for control of I/O functions. The channel contains a port through which part of this control passes.



DATA FLOW

The channel is a common data and timing link for the following functions:

- Movement of data by the control processor directly between control storage or main storage and the I/O attachments (I/O storage instructions).
- Burst cycle steal or base cycle steal between control storage or main storage and the I/O attachments (cycle steal mode).
- Movement of data between the control processor local storage registers and the I/O attachments (I/O immediate instruction).
- Direct control of the channel or the I/O functions by the control processor that may or may not include data movement (I/O control load and I/O control sense instructions).
- Information to the control processor from tested I/O conditions (jump on I/O condition instruction).

The channel supplies the necessary controls to support the following:

- I/O instructions (immediate, storage, and jump)
- Interrupts (five levels)
- Burst cycle steal (disk or diskette)
- Base cycle steal (work stations)
- Initial program load
- Error detection

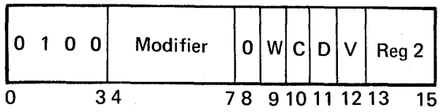
I/O Instructions

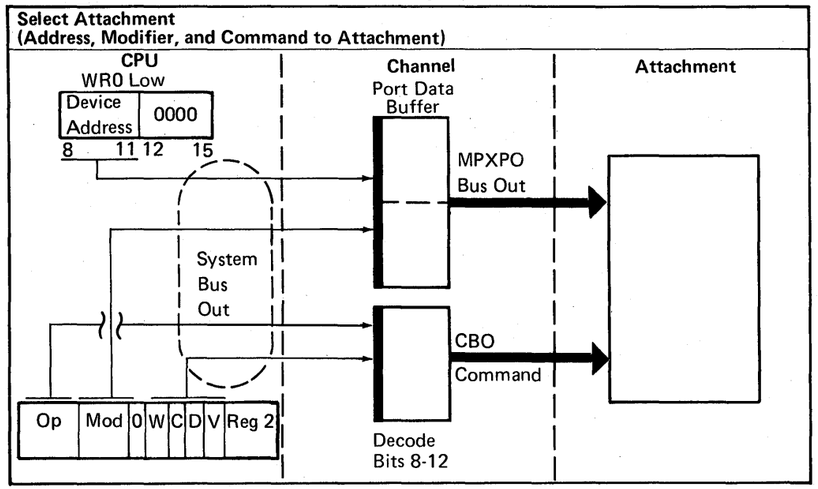
Processing Unit Storage Link to I/O Attachments

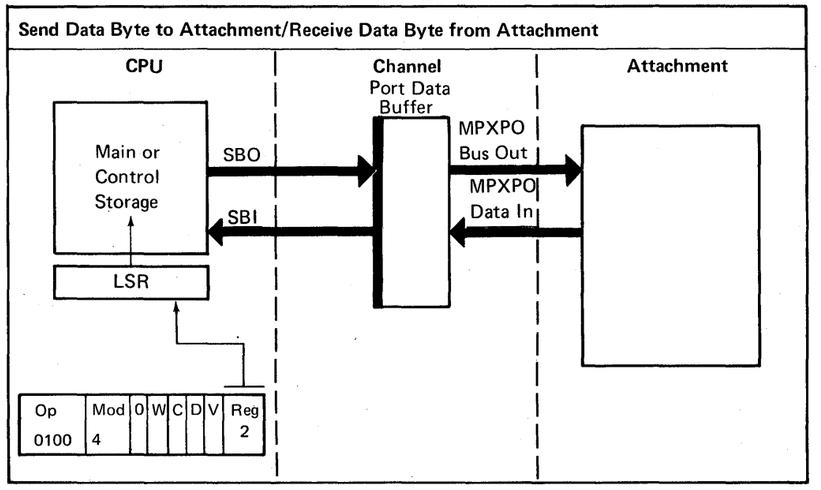
I/O Storage (WTCL, WTCH, RDCL, RDCH, WTM, RDM)

The channel gates all data moved by the control processor from control storage or main storage to the I/O attachments. Data can either be read from storage and moved to the I/O attachments or read from the I/O attachments and written into storage.

All storage addressing, storage write control, and address updates are controlled by the control processor. The I/O storage instructions are described in detail under *I/O Storage* later in this section.



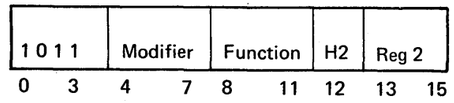




Control Processor Local Storage Register Link to I/O Attachments

I/O Immediate (IOL, IOCL, IOS, IOCS, SILSB)

The control processor interfaces directly with the channel when moving data into or out of the control processor local storage registers. The control processor handles all control processor local storage register selection and the write controls directly from the I/O instruction fields. The channel gates data to or from the control processor local storage register, the port, and the I/O attachments. The I/O immediate instruction that performs this function includes several commands that are described here.



The I/O immediate instruction has four main functions:

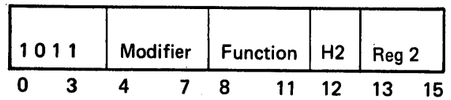
1. Moves a single byte of data from the control processor local storage register to the I/O attachment or from the I/O attachment to the control processor local storage register.
2. Directs control of the channel and the I/O functions that may or may not include data movement.
3. Directs control of the control processor functions.
4. Directs control of the main storage processor functions.

The different commands that are a function of the I/O immediate command are:

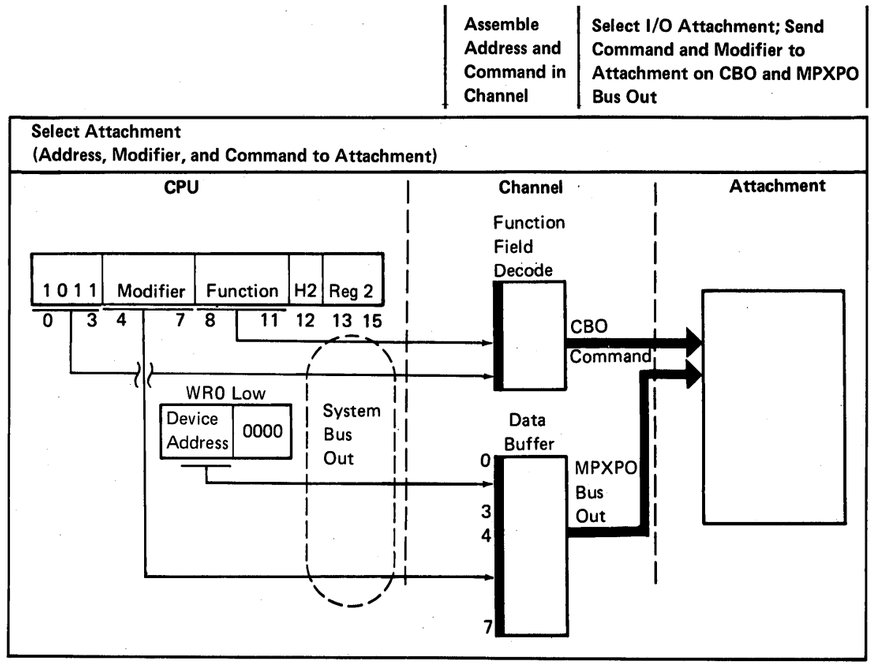
- I/O Load–Moves the data from the local storage register to the I/O attachment.
- I/O Sense–Moves the data from the I/O attachment to the local storage register.
- I/O Control Load–Moves the contents of the local storage register to the I/O attachment.
- I/O Control Sense–Moves the information from the I/O attachment to the local storage register.
- Sense Interrupt Level Status Byte–Determines which device is requesting service on a given interrupt level.
- Control Processor Load Function–Sets/resets, enables/disables conditions and indicators in the control processor. (This instruction does not go to the channel.)
- Control Processor Sense–Moves information to the control processor concerning the status of the CE panel, address switches, I/O clocks, errors, and the processor condition register. (This instruction does not go to the channel.)

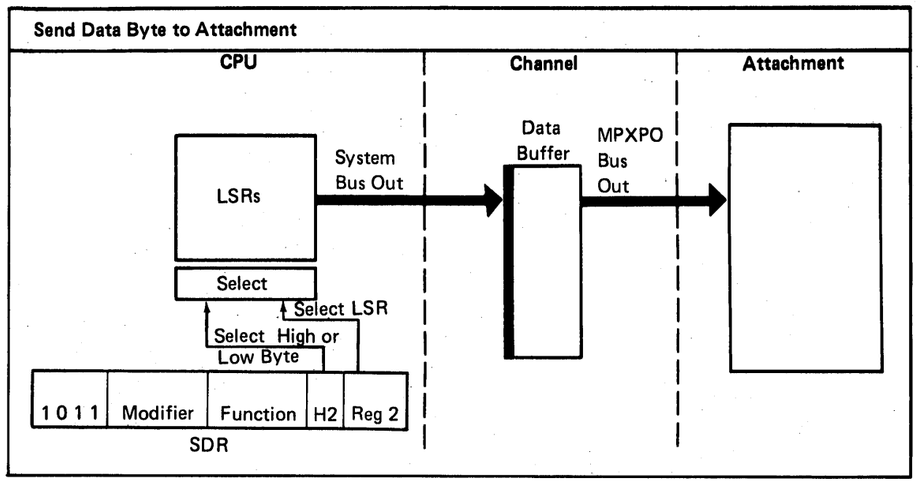
The basic functions of the I/O load, I/O sense, and sense interrupt level status byte commands are described here. More complete descriptions may be found later in this section under the heading *Commands*.

I/O Load or I/O Control Load (IOL, IOCL)

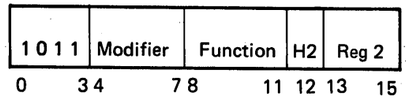


This function of the I/O immediate instruction moves 1 byte of data or control information from a local storage register to an I/O attachment.

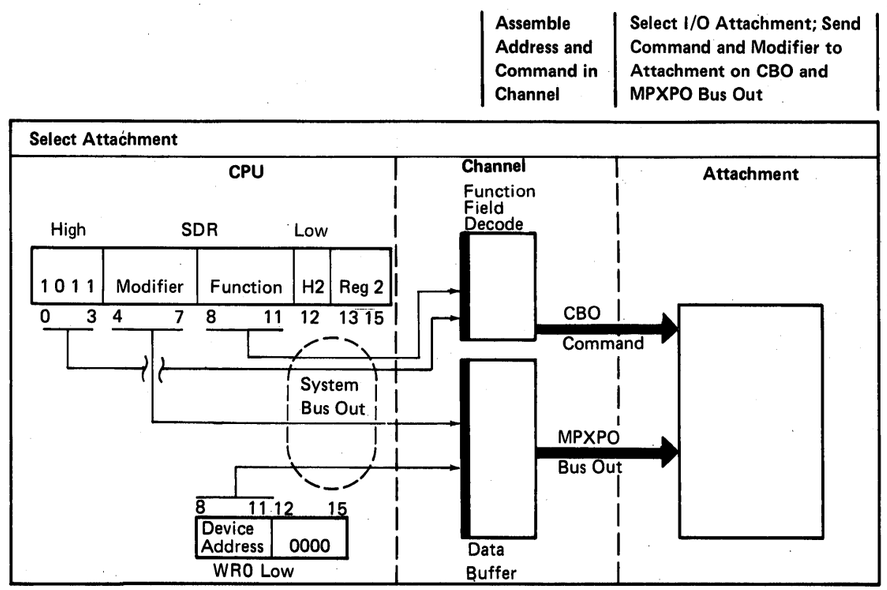


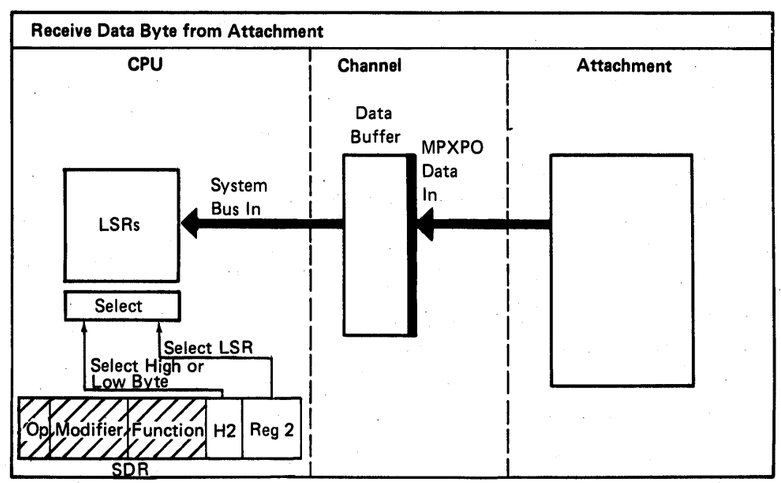


I/O Sense or I/O Control Sense (IOS, IOCS)



This function of the I/O immediate instruction moves 1 byte of data or status type information from an I/O attachment to a local storage register.



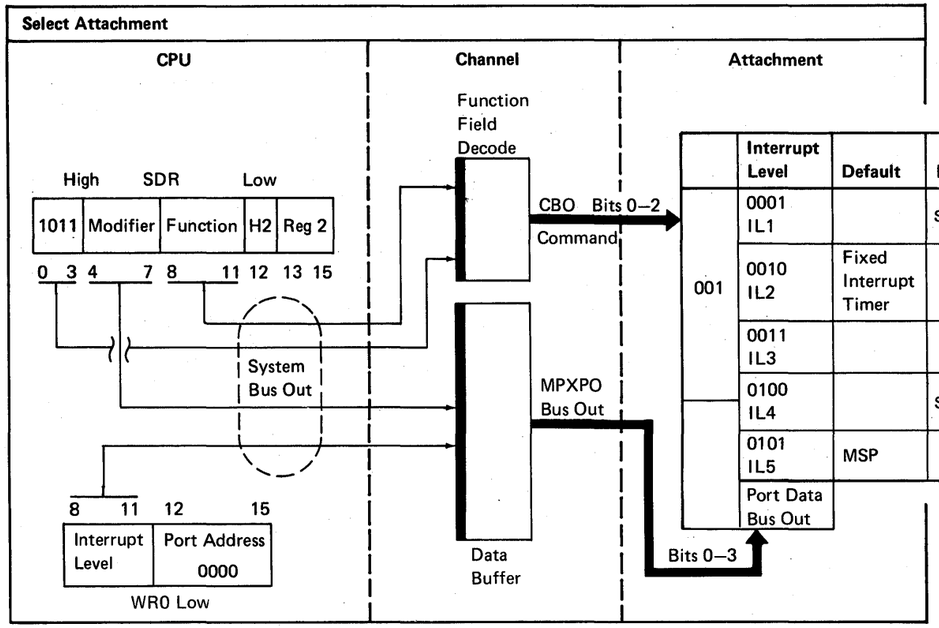


5

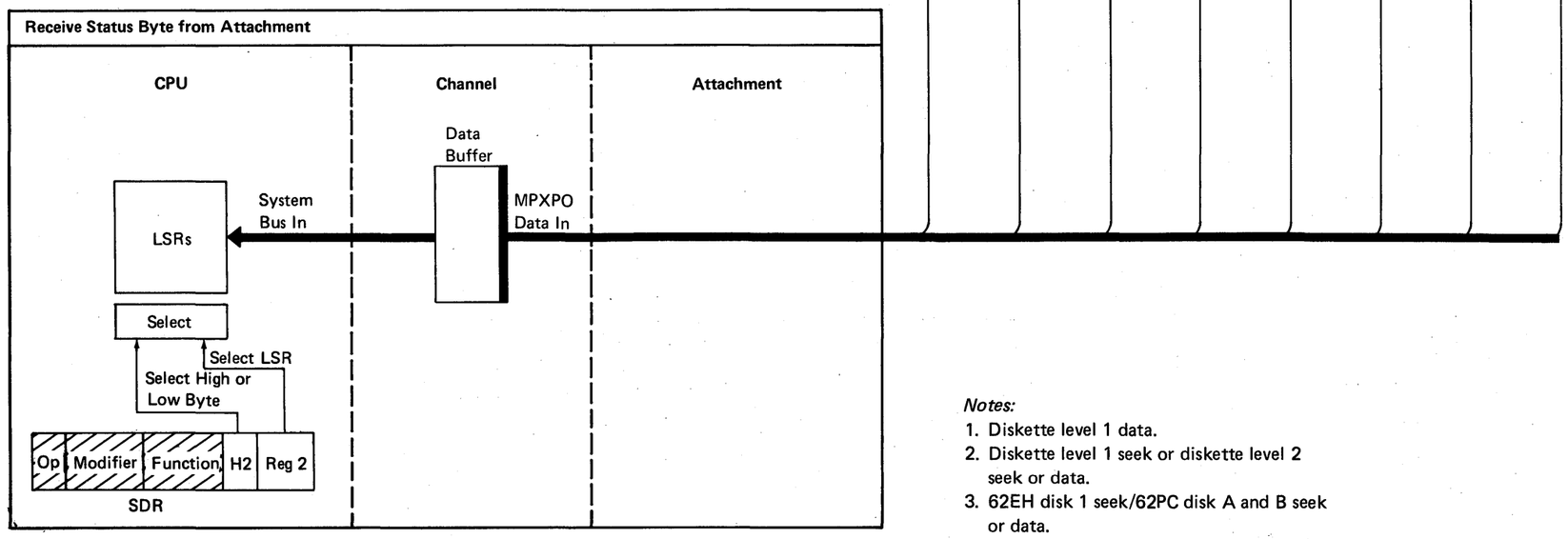
Sense Interrupt Level Status Byte (SILSB)

1011	Modifier	Function	H2	Reg 2
0	3 4	7 8	11 12	13 15

This function of the I/O immediate instruction moves 1 byte of status information from the I/O attachment to the selected local storage register. This status byte determines which devices are requesting service on a given interrupt level.



	Interrupt Level	Default	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
001	0001 IL1		See Note 1						62EH Disk 2 Data	62EH Disk 1 Data
	0010 IL2	Fixed Interrupt Timer			Data Comm					
	0011 IL3									
	0100 IL4		See Note 2	Unit Record	Work Station 1	Printer 1			62EH Disk 2 Seek	See Note 3
	0101 IL5	MSP								
	Port Data Bus Out									



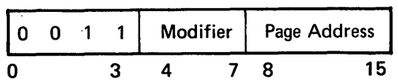
Notes:

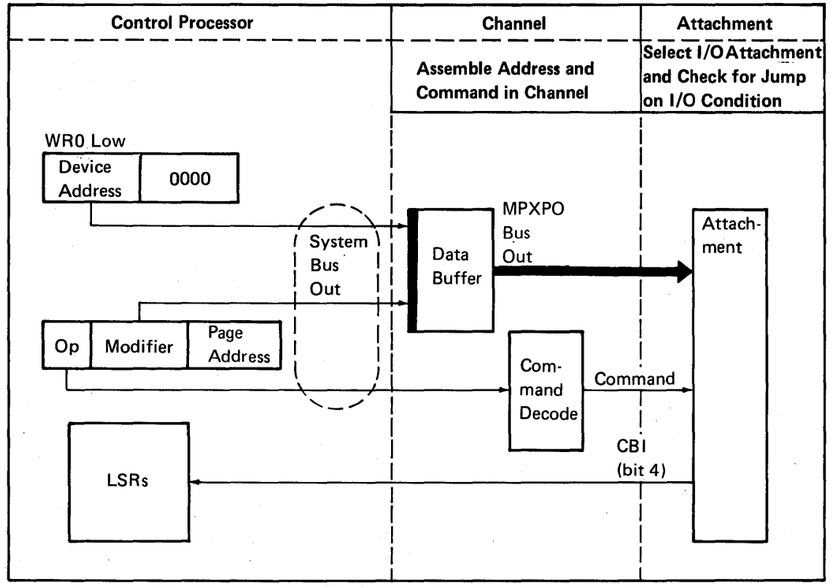
1. Diskette level 1 data.
2. Diskette level 1 seek or diskette level 2 seek or data.
3. 62EH disk 1 seek/62PC disk A and B seek or data.

Control Processor Jump on I/O Condition Link to I/O Attachments

Jump on I/O Condition (JIO)

The sequence of the control processor instructions can be changed inside a page boundary (256-word limit) by the jump-on-I/O-condition instruction. This instruction tests I/O conditions and if the condition tested is active, a jump to the page address specified in the instruction is taken. The 'CBI bit 4' port line indicates if the I/O condition tested is active. The control processor then replaces the 8 low-order bits of the microaddress register with the contents of the page address field. When the I/O condition tested is not active, the control processor takes the next instruction in sequence.





PORT CARD

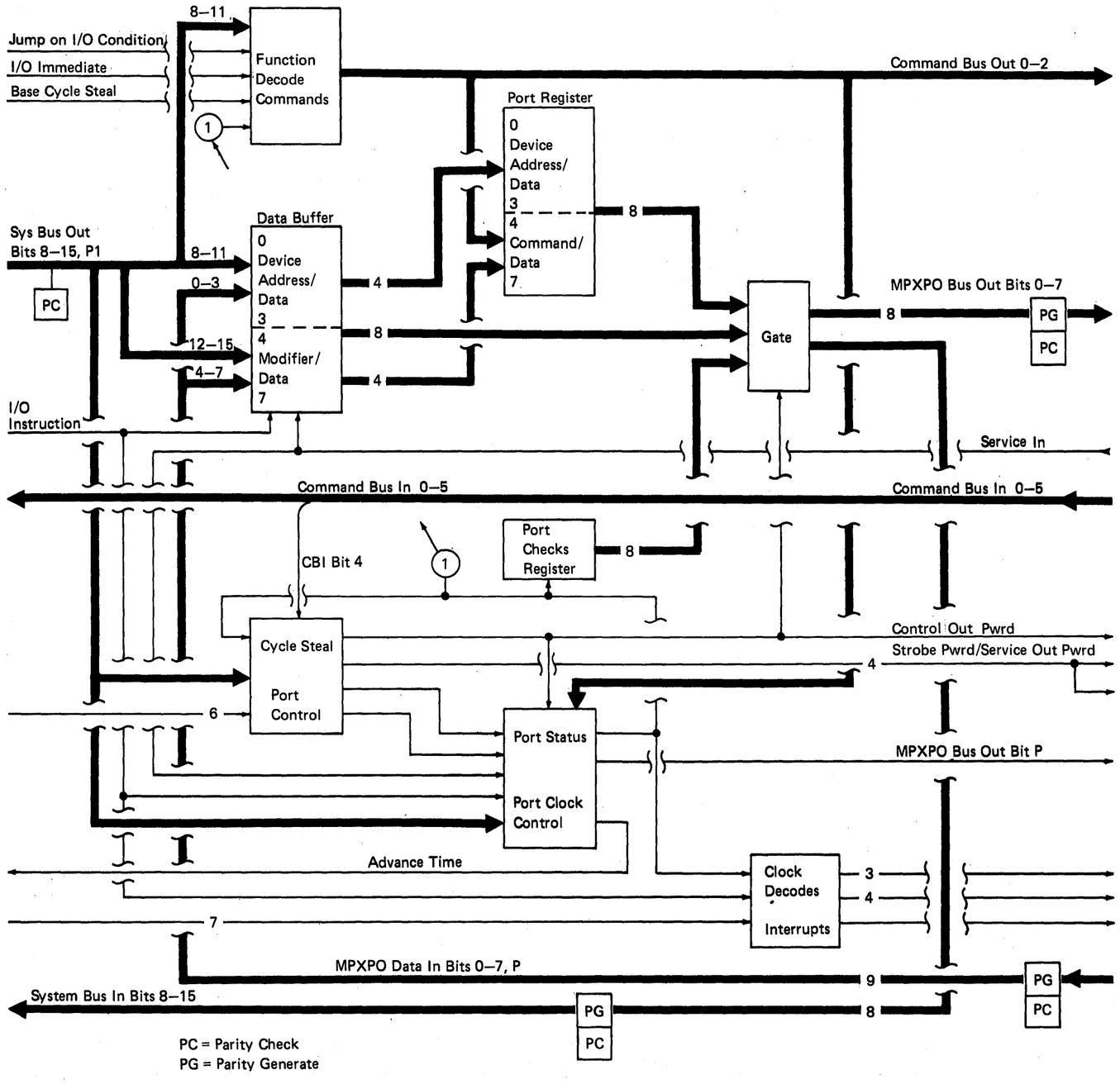
The majority of the port lines are generated/terminated in the port card, although some port lines originate in the control processor and disk attachments.

All data buses in the channel/port/devices are 1 byte wide with each bus containing odd parity. Thus, a 1-byte bus contains 8 data bits and 1 parity bit.

Port Parity

The port normally operates in odd parity mode. For diagnostic purposes, the port (through an I/O control load) can be set to operate in even parity mode. In this case, data received from or sent to the control processor or I/O device is expected to have even parity. Because the control processor operates with odd parity, the port causes a control processor check when sending data to the control processor in the even parity mode of operation. Even parity mode is used only when running diagnostics to cause control processor checks for diagnostic analysis. System reset sets the port to odd parity.

Port 0



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Port Clock

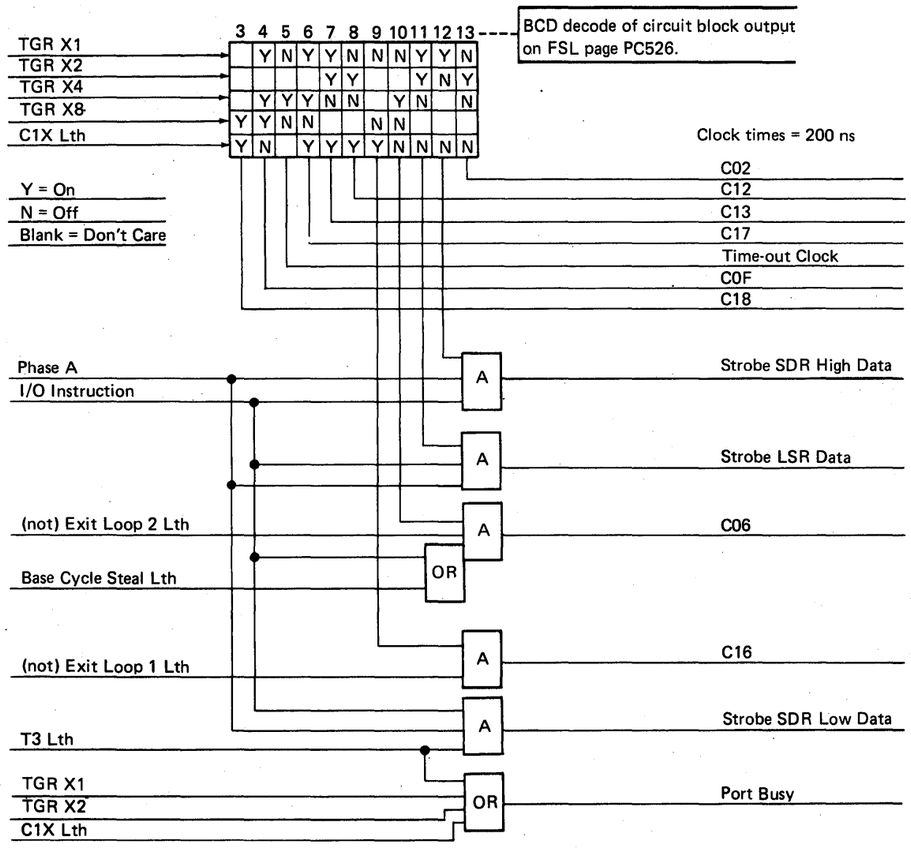
The port clock generates the interface timings between the control processor and the I/O attachments. The port clock runs only for I/O instructions and base cycle steal operations. During other operations, the port clock is reset. When the control processor decodes an I/O instruction, it activates the 'I/O instruction' line during time T3 (Z); this line remains active through the end of time T6. An 'I/O instruction' line causes the control processor clock to extend times T3 and T6 and, at the same time, gates the port clock triggers, which are controlled by the shift of the 'phase A' line. Port clock output times are decoded from the inputs of triggers X1, X2, X4, and X8, and the C1X latch.

The port clock will loop in one of two conditions while waiting for a response from the I/O attachment:

- 'Control out pwrd' line (C) sequence loop:
  - The port clock loops (C07, C0F, C0E, C06, and so on) while waiting for the I/O attachment to respond with an active 'service in' (F) or 'multidevice response' line (P).
  - The 'strobe pwrd' line (U) continues to pulse while waiting for a response.
  - The 'exit loop 1' latch (N) is set (anded condition of service in, phase A, and C06) and stops the port clock from looping.
  - The 'C1X' latch (R) is set by the active 'exit loop 1 lth' line and permits the port clock to go into the second loop condition (the C1X latch adds one to the tens position of the port clock for the second loop clock timings).

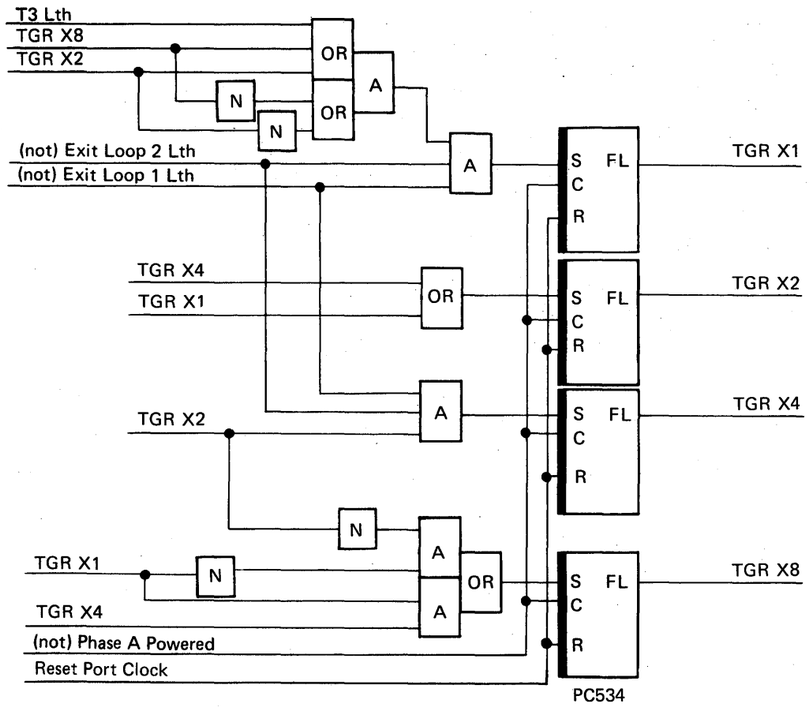
- 'Service out pwrd' line (G) sequence loop:
  - The port clock loops (C17, C1F, C1E, C16, and so on) while waiting for the I/O attachment to respond with inactive 'service in' and inactive 'multidevice response' lines (J) (X).
  - The 'strobe pwrd' line (V) continues to pulse while waiting for a response.
  - The 'exit loop 2' latch (Q) is set (anded condition of not service in, not multidevice response, phase A, and C16 clock time) and stops the port clock from looping.
  - The 'C1X' latch (Y) is reset by the active 'exit loop 2 lth' line, and the port clock stops looping and continues on through C02 and C00 times to a wait state (C00).

Generation of Port Clock Times



PC526

Generation of Port Triggers



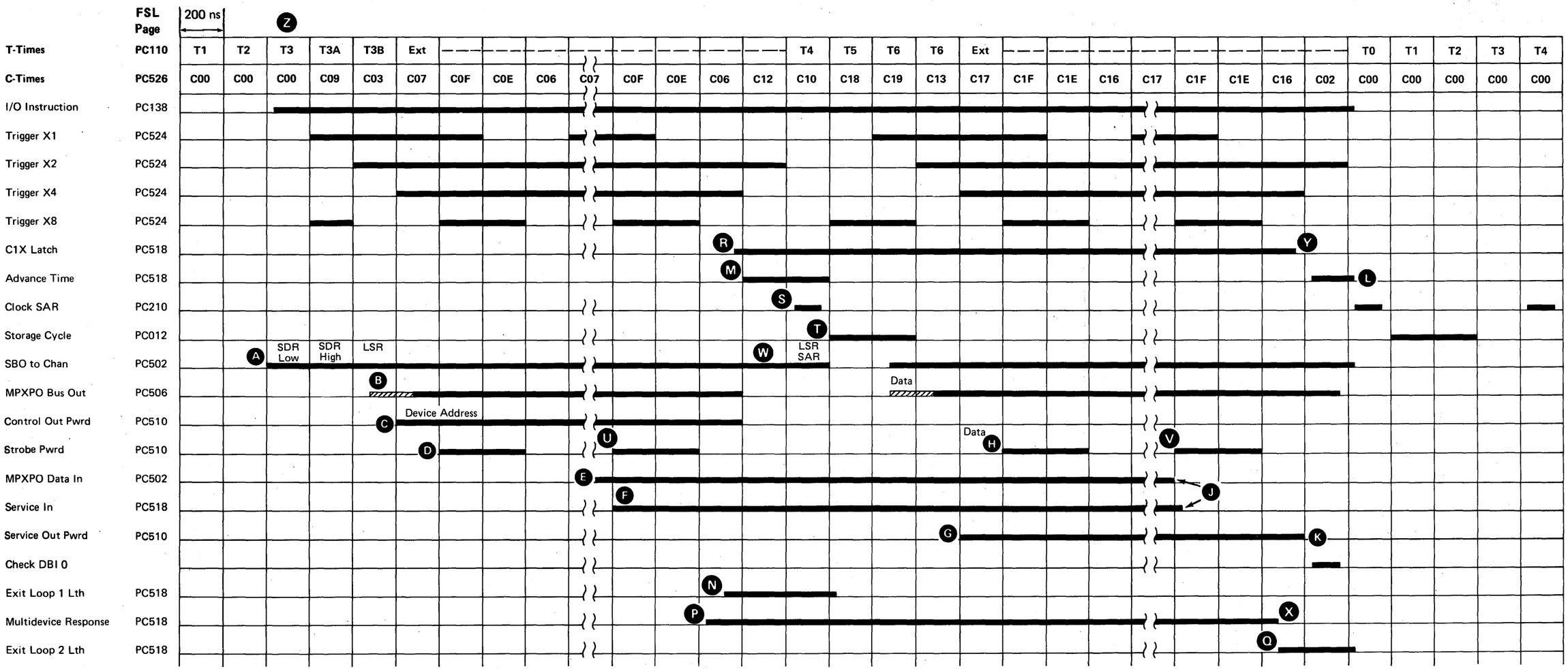
PC534

During the first three 200-nanosecond extended T3 times, storage data register low, storage data register high, and local storage register 0 (low) (of the correct interrupt level) are gated to the port card (A). During the T3 times that follow, the port gates the device address and modifier on the 'MPXPO bus out' lines (B), activates the 'control out pwrd' line (C), and sends a 'strobe pwrd' line (D) out to the device attachment. When the 'control out pwrd' line is activated, the port clock loops (C07, C0F, C0E, C06, C07, and so on), sending out 'strobe pwrd' pulses while waiting for the I/O device to respond (or until a time-out occurs).

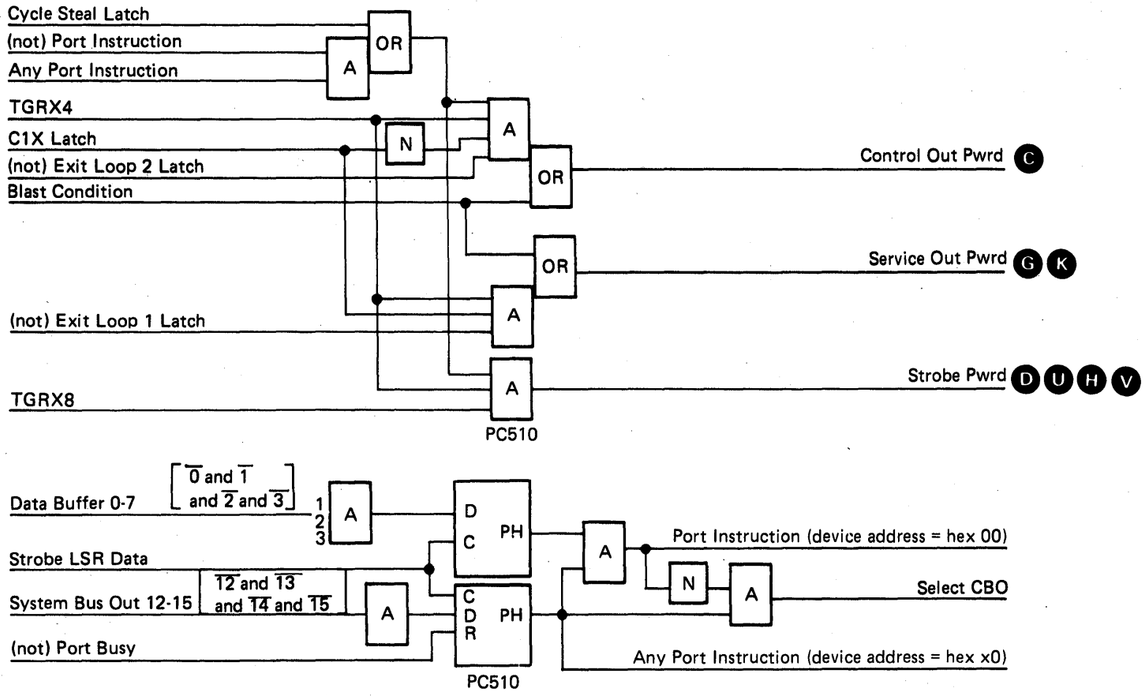
When the device responds, it places data on the 'MPXPO data in' lines (E) (indicates when data is moved from the I/O attachment to the control processor) and activates the 'service in' line (F). The rise of the 'service in' line (or a time-out) advances the port clock, and the port activates the 'advance time' line (M) to signal the control processor clock to advance to time T4 (select and gate LSR to channel (S) (W)). The system clock continues to advance normally to time T6.

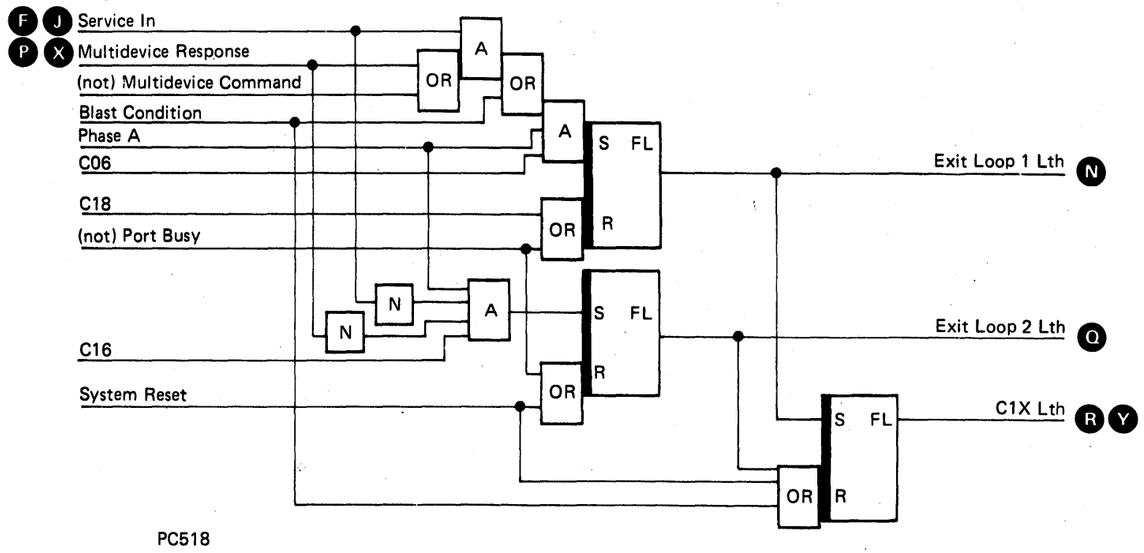
During time T6, the port sends the 'service out pwrd' line (G), which indicates that data is ready to be sent or that data was received.

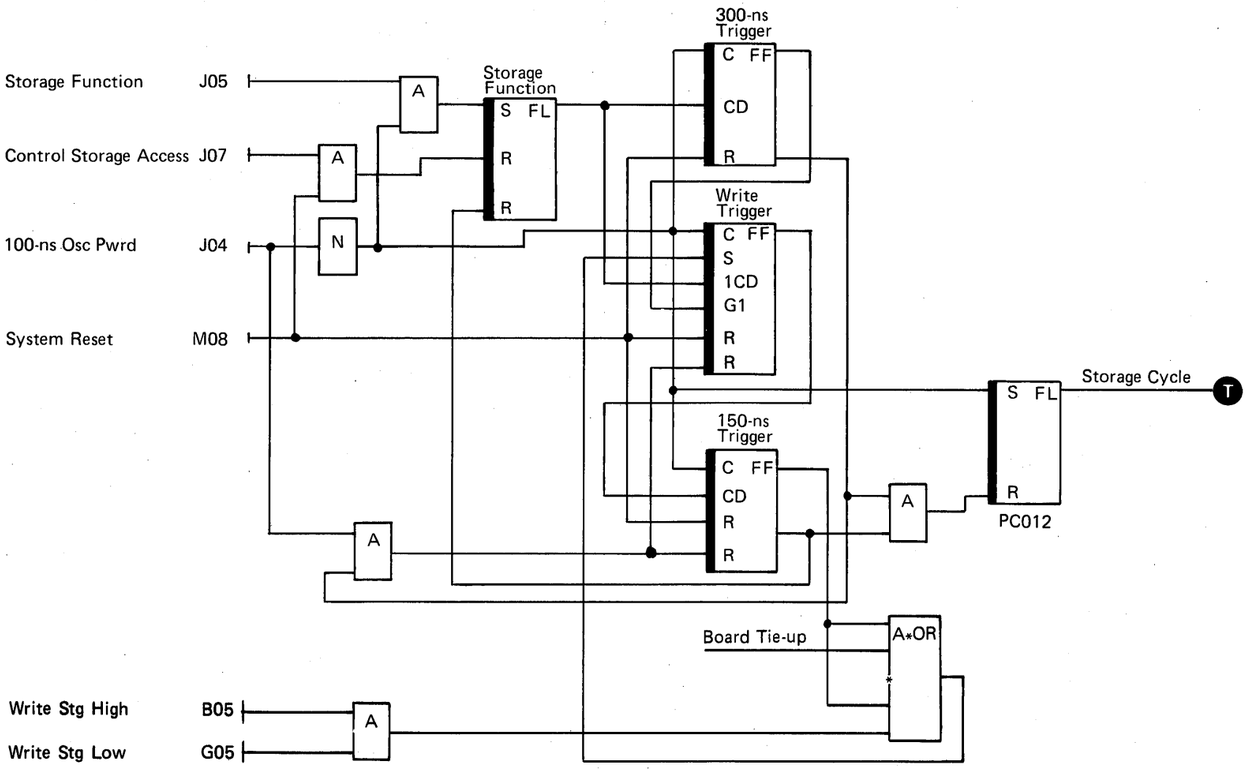
The 'strobe pwrd' line (H) is again sent for the I/O device to use. The port clock loops with the 'service out pwrd' line active, and the 'strobe pwrd' pulses continue to be generated while the port waits for the I/O device to respond (or a time-out to occur). The I/O device responds by taking the data off the 'MPXPO bus out' line (or if data was sent to the control processor, by turning off the 'MPXPO data in' lines) and by turning off the 'service in' line (J). The port responds by advancing the port clock to turn off the 'service out pwrd' line (K) and then activates the 'advance time' line (L), causing the control processor clock to run again to time T0.

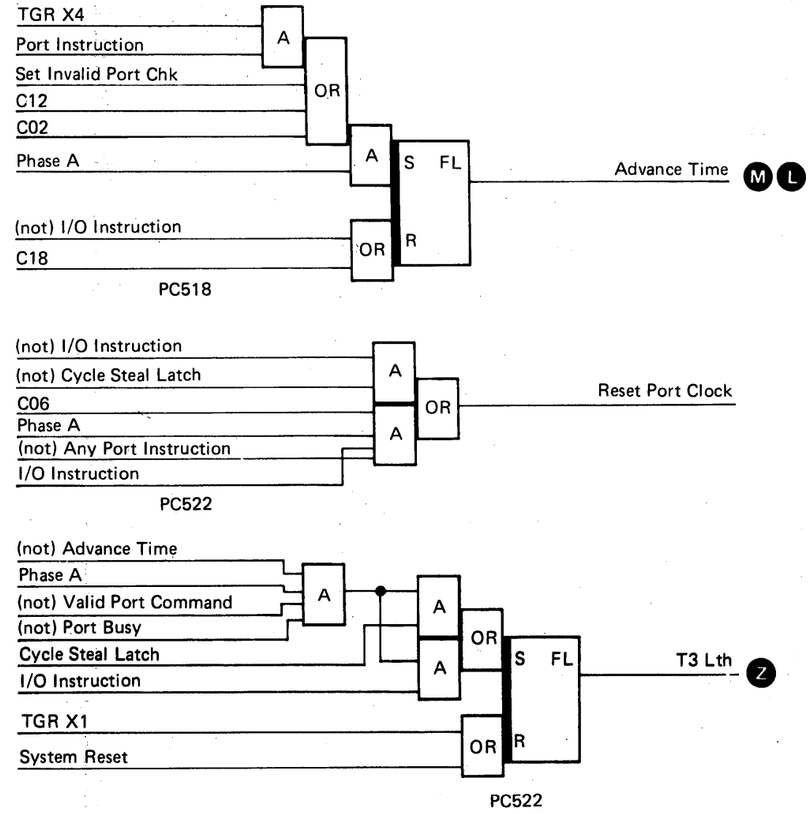

FSL Page
200 ns
T-Times PC110 T1 T2 T3 T3A T3B Ext T4 T5 T6 T6 Ext T0 T1 T2 T3 T4
C-Times PC526 C00 C00 C00 C09 C03 C07 C0F C0E C06 C07 C0F C0E C06 C12 C10 C18 C19 C13 C17 C1F C1E C16 C17 C1F C1E C16 C02 C00 C00 C00 C00 C00
I/O Instruction PC138
Trigger X1 PC524
Trigger X2 PC524
Trigger X4 PC524
Trigger X8 PC524
C1X Latch PC518
Advance Time PC518
Clock SAR PC210
Storage Cycle PC012
SBO to Chan PC502
MPXPO Bus Out PC506
Control Out Pwrd PC510
Strobe Pwrd PC510
MPXPO Data In PC502
Service In PC518
Service Out Pwrd PC510
Check DBI 0
Exit Loop 1 Lth PC518
Multidevice Response PC518
Exit Loop 2 Lth PC518
SDR Low
SDR High
LSR
LSR SAR
Data
Device Address
Data

Note: The circled letters on these pages refer to the previous page.





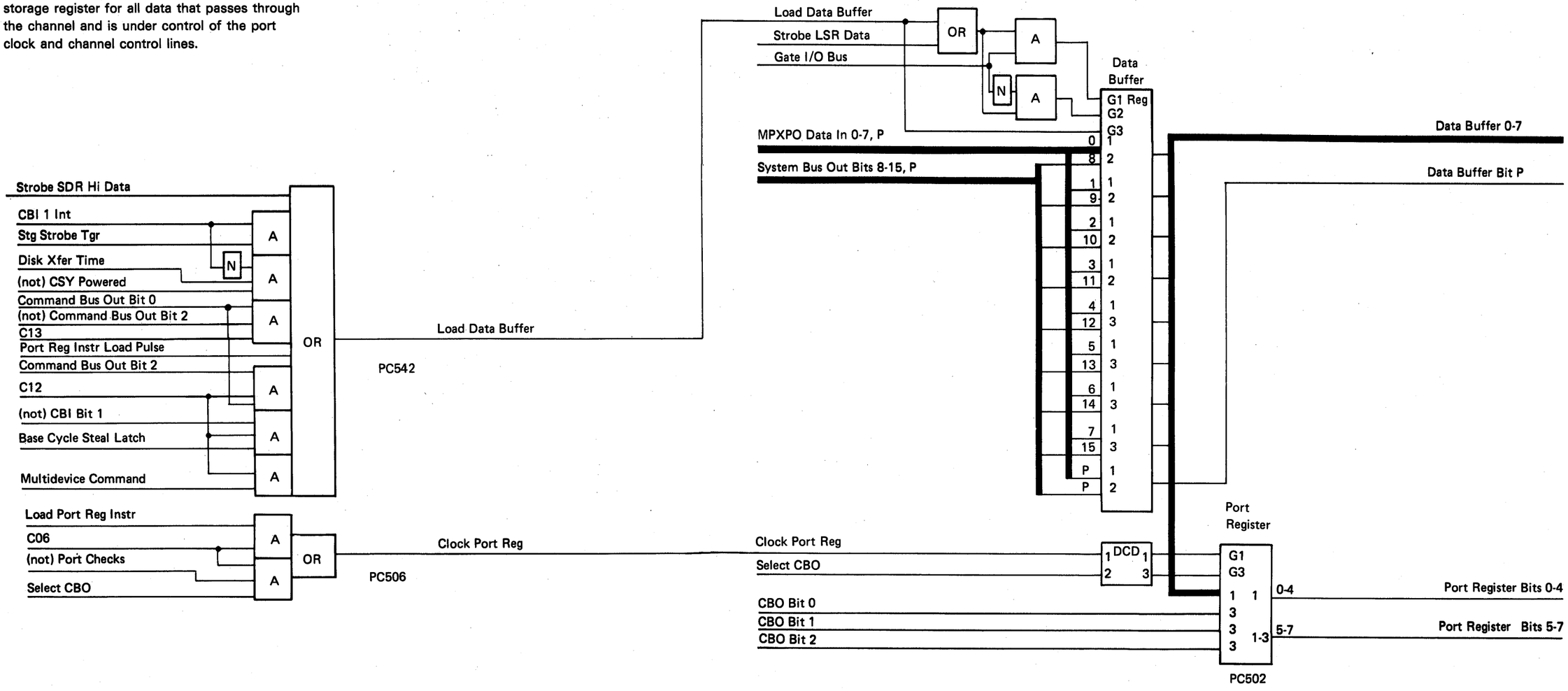

Storage Function J05
Control Storage Access J07
100-ns Osc Pwrd J04
System Reset M08
Write Stg High B05
Write Stg Low G05
A
N
Storage Function
S FL
R
R
300-ns Trigger
C FF
CD
R
Write Trigger
C FF
S
1CD
G1
R
R
150-ns Trigger
C FF
CD
R
R
S FL
R
PC012
Storage Cycle T
Board Tie-up
A*OR

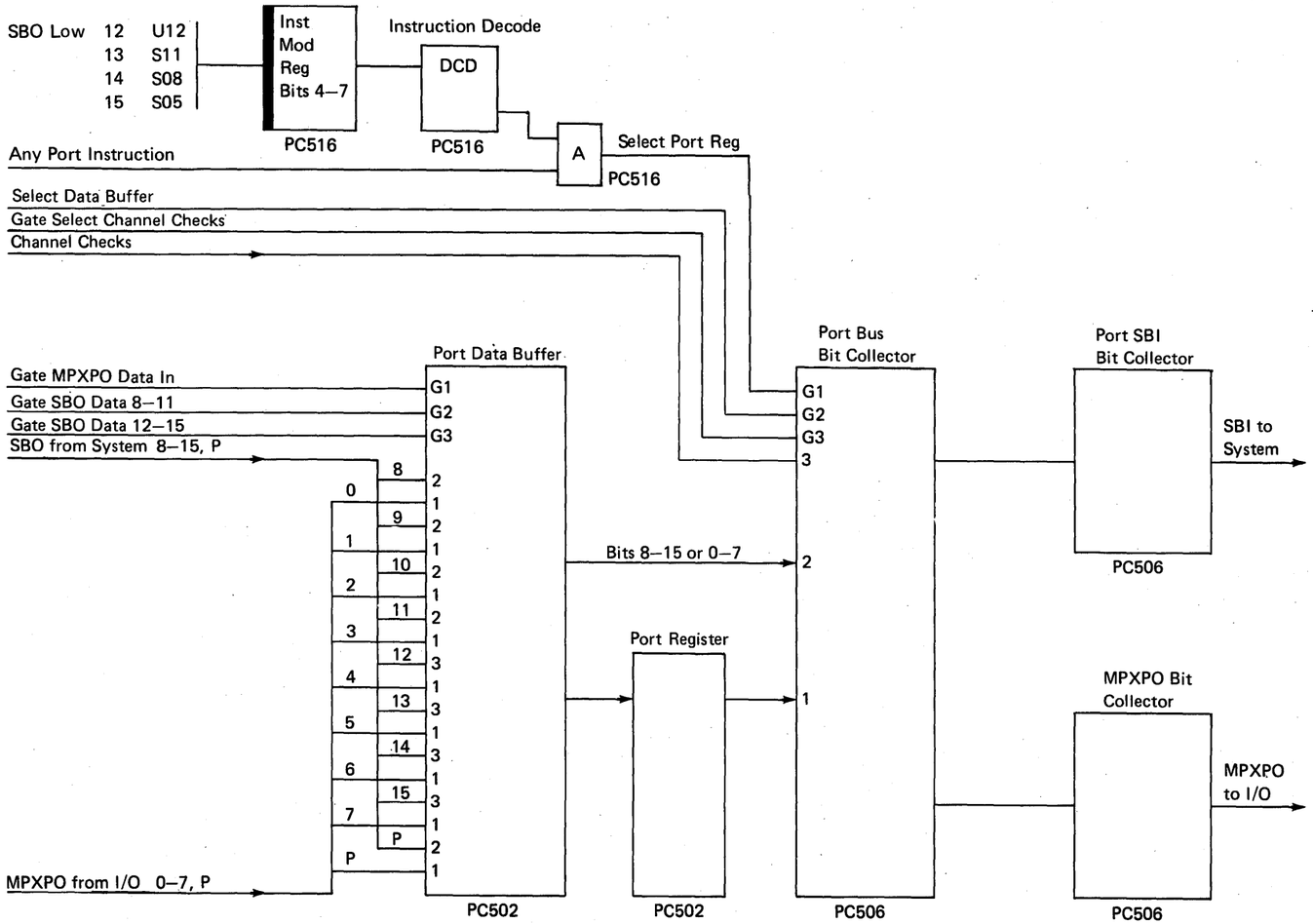

TGR X4
Port Instruction
Set Invalid Port Chk
C12
C02
Phase A
(not) I/O Instruction
C18
A
OR
A
OR
S FL
R
Advance Time M L
PC518
(not) I/O Instruction
(not) Cycle Steal Latch
C06
Phase A
(not) Any Port Instruction
I/O Instruction
A
A
OR
Reset Port Clock
PC522
(not) Advance Time
Phase A
(not) Valid Port Command
(not) Port Busy
Cycle Steal Latch
I/O Instruction
TGR X1
System Reset
A
A
A
OR
OR
S FL
R
T3 Lth Z
PC522

5

Data Buffer

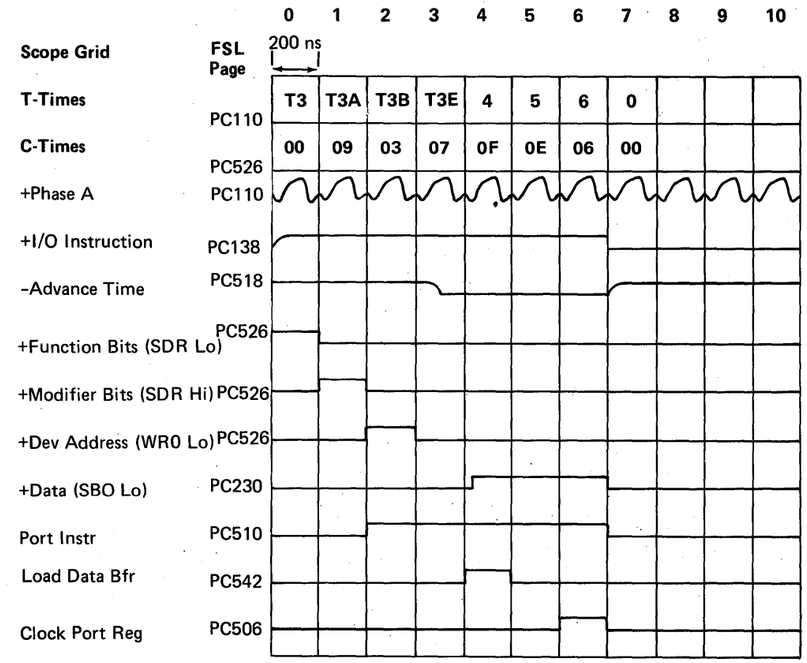
The data buffer is used as an intermediate storage register for all data that passes through the channel and is under control of the port clock and channel control lines.





Port Register

The port register is for diagnostic purposes and stores the device address and I/O command. When an error occurs, this information can be stored in a local storage work register and displayed on the CE panel.



A load port register instruction is used by the diagnostic supervisor in diagnostic mode to wrap the port register and check for correct bits.

Port Checks Register

Checks found by the port hardware are stored in the port checks register and can be loaded into a work register. These checks can then be displayed by the byte 0 lights on the CE panel by setting the Mode Selector switch to the Insn Step/Dply Chks position.

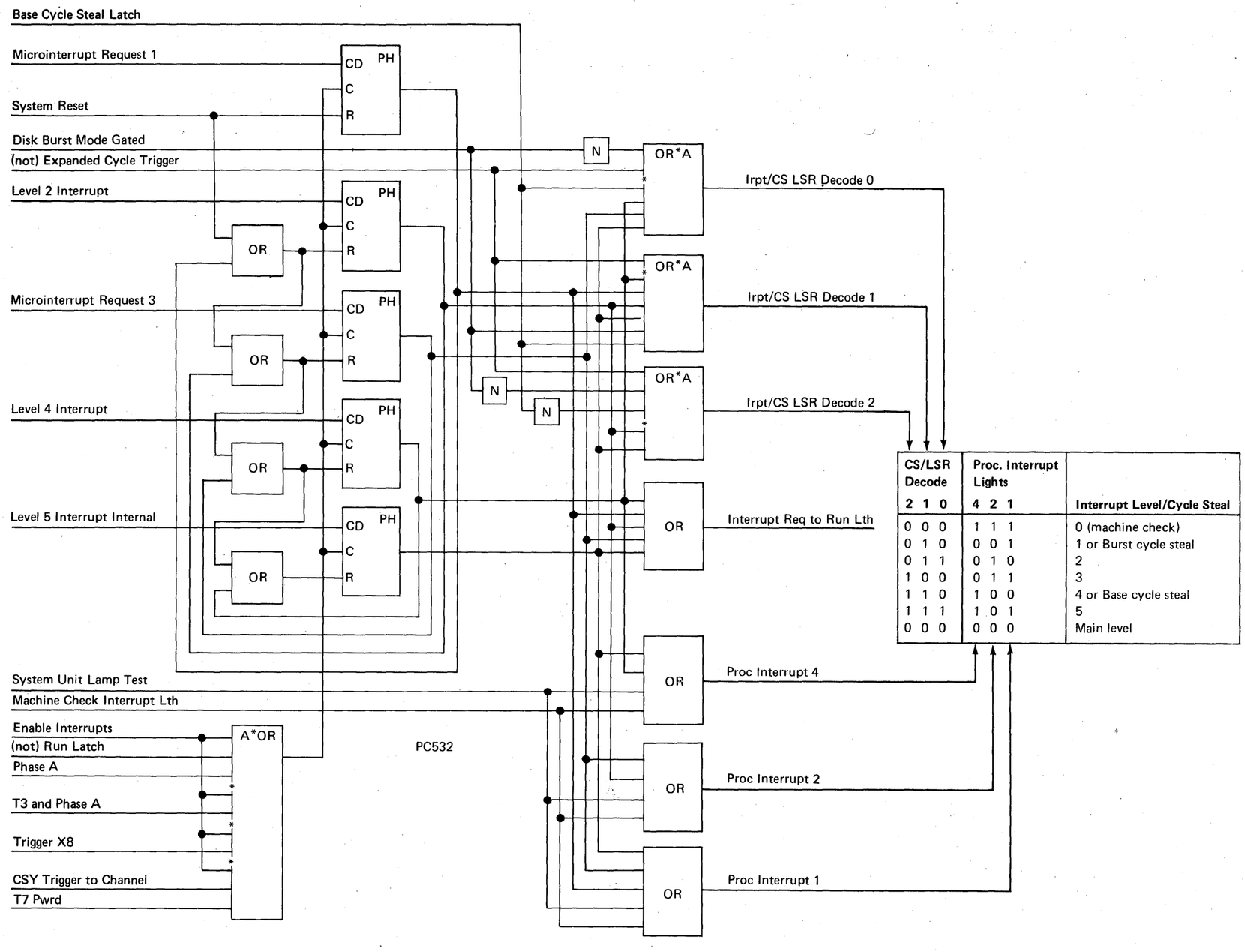
Port Decodes

Interrupt/Cycle Steal Priority Control for LSRs

The 'irpt/CS LSR decode 0, 1, and 2' lines are used to control local storage register selection bits 0, 1, 2, while executing instructions and during burst cycle steal or base cycle steal operations. These lines permit selection of one of the five groups of registers specified for interrupts and burst mode.

The interrupt and cycle steal indicators are used to display the active interrupt.

The 'interrupt req to run' latch is used to take the control processor out of the wait condition (caused by the processor wait instruction) when an interrupt request is found by the port.



CS/LSR Decode 2 1 0	Proc. Interrupt Lights 4 2 1	Interrupt Level/Cycle Steal
0 0 0	1 1 1	0 (machine check)
0 1 0	0 0 1	1 or Burst cycle steal
0 1 1	0 1 0	2
1 0 0	0 1 1	3
1 1 0	1 0 0	4 or Base cycle steal
1 1 1	1 0 1	5
0 0 0	0 0 0	Main level

Command Bus Out Decode

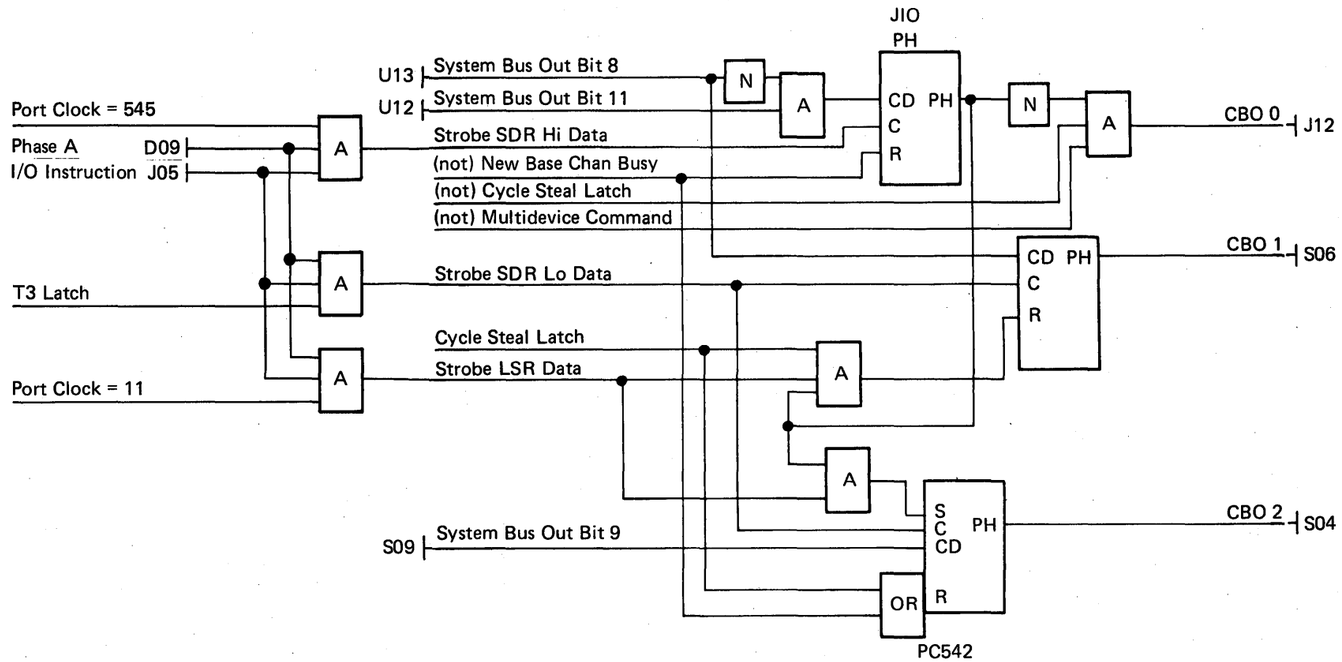
Control processor instructions to the I/O attachment are decoded from the 'system bus out (low)' lines and then sent to the I/O attachment as a command on the 'command bus out' lines. The commands are decoded as follows:

• I/O immediate instruction	Bits 8-11	CBO 0-2
– I/O load (IOL)	0000	100
– I/O sense (IOS)	0100	101
– I/O control load (IOCL)	1000	110
– I/O control sense (IOCS)	1100	111
– Sense interrupt level status byte (SILSB)	0101	001

• I/O storage instruction	Bits 8-11	CBO 0-2
– I/O store to control storage (RDCL, RDCH)	011X	100
– I/O load from control storage (WTCL, WTCH)	001X	101
– I/O store to main storage (RDM)	010X	100
– I/O load from main storage (WTM)	000X	101

Note: These instructions have the same command to the I/O attachment as a load or sense in the I/O immediate instruction.

• Jump on I/O condition instruction (bits 0-3)	Bits 8-11	CBO 0-2
– The op code is decoded as a jump-on-I/O-condition command and sent to the I/O attachment.	0011	011



CONTROL PROCESSOR/PORT CONTROLS

Port to Control Processor Lines

System Bus In–Nine Lines

This bus is 1 byte wide and moves data from the I/O device/port to the control processor during I/O sense and cycle steal operations.

Storage Cycle Request–One Line

This line signals the control processor to start the storage access sequence during a cycle steal mode operation.

Advance Time–One Line

This signal informs the control processor clocks to continue when stopped in either time T3 or time T6 of an I/O instruction or at time T3 for register control or main storage access instructions.

Block Processor Clock (BPC Tgr)–One Line

This signal comes from the port and stops the control processor from processing instructions so that a burst cycle steal or a base cycle steal mode operation can be performed.

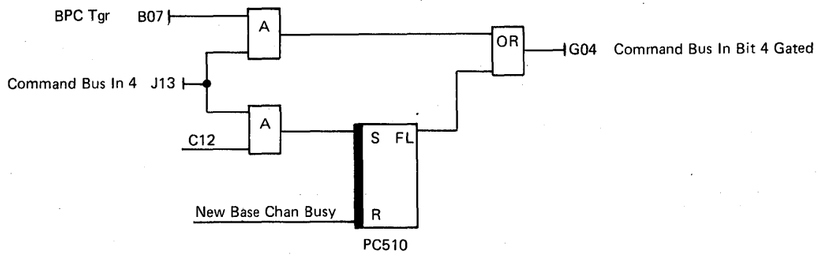
Interrupt/Cycle Steal LSR Decode–Three Lines

These lines control local storage register selection bits 0, 1, and 2 during instruction and cycle steal processing. This permits selection of one of the five groups of registers assigned to microinterrupts and cycle steals.

CBI Bit 4 Gated–One Line

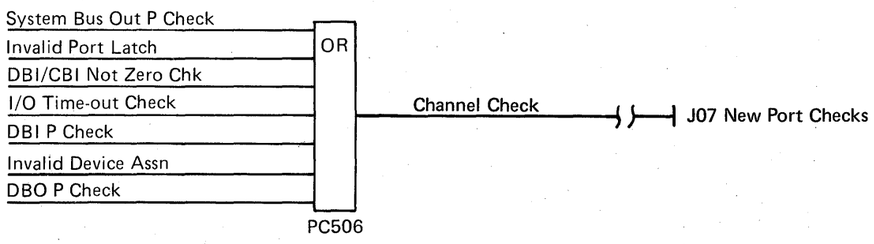
This line indicates that:

- Control storage is to be selected during a cycle steal.
- The condition specified by the jump-on-I/O-condition instruction is met.
- Parity on the 'MPXPO data in' lines is to be ignored.



New Channel Check–One Line

This line is sent from the port to inform the control processor that the check has been sensed.



Proc Interrupt 1, 2, 4–Three Lines

These indicators display the active interrupt level on the CE panel.

I/O Service Request–One Line

This line is reserved.

Interrupt Request to Run Latch–One Line

This line takes the control processor out of the wait state (caused by the control processor wait instruction) when a microinterrupt request is sensed by the port.

Control Processor to Port Lines

T4 Through T6–One Line

This line is a timing signal that occurs for the last part of an instruction. This signal is not present during a branch instruction.

System Bus Out–Nine Lines

This bus is 1 byte wide and goes from the control processor through the correct gates. The port can receive data from either control storage or main storage or the control processor local storage registers as needed during cycle steal and I/O command operations.

I/O Instruction–One Line

This line is active during a jump on I/O condition, I/O storage, or I/O immediate instruction from time T3 through time T6 of the control processor cycle.

Phase A–One Line

This is a signal from the control processor control card, which is 100 nanoseconds off and on. It becomes active 50 nanoseconds after the associated control processor clock becomes active.

Machine Check Interrupt–One Line

This line becomes active when there is an active check condition to the control processor.

CSY Trigger–One Line

This line becomes active 100 nanoseconds after the storage clocks in the control processor have started to run. The timing width is 300 nanoseconds. This signal resets a cycle steal request if the device that requested the cycle steal is being serviced.

System Reset–One Line

This line indicates to the attachment that all logic should be initialized to a start condition. This line becomes active during the power on reset condition or when the Reset switch on the CE panel is pressed. It is also activated when the Load switch on the operator panel is pressed. This reset is active for as long as either switch is pressed.

T7–One Line

This line signals the port that the control processor is in a wait state. The control processor can process a cycle steal or interrupt request during this time.

Lamp Test–One Line

This signal is generated at the CE panel and the channel activates the interrupt LED circuits.

PORT/ATTACHMENT CONTROLS

Port to Attachment Lines

MPXPO Bus Out–Nine Lines

These lines are used to transmit to the attachment:

- Device address/modifier bits
- Microinterrupt level/modifier bits
- Cycle steal acknowledge codes
- Control processor/storage data
- Port echoes during I/O sense and control sense functions

A parity bit is used to maintain odd parity on all moves to the attachment except when the interface is in even parity mode.

The 'MPXPO bus out' lines are deskewed and are maintained to be valid from the time the 'control out pwrd' ('service out pwrd') line is made active by the port until the I/O attachment de-activates the 'service in' line, which is sensed by the port.

Notes:

1. The port echoes the bits of the data/status byte on the 'MPXPO bus out' lines as received during a sense operation. The information can be used by the attachment to reset data/status indicators if needed. (This may be used as a reverse interface wrap for diagnostics.)
2. Contents of the bus lines, when control lines are not active, may not be correct and must not be used.
3. Even if data (Note 1) contains wrong parity (CBI bit 4 active), the port will generate valid parity on the echo data. The port will maintain odd parity during the jump-on-I/O-condition instruction 'service out pwrd' line request.

Control Out Pwrd–One Line

The rise of this line indicates that the 'MPXPO bus out' and the 'command bus out' lines can be strobed. The line ensures that the data on the 'MPXPO bus out' and 'command bus out' lines is valid and has been deskewed by the interface.

Once the I/O attachment makes the 'service in' line not active, the 'MPXPO bus out' lines are not valid and should no longer be strobed.

The 'control out pwrd' line, together with the 'service out pwrd' line, indicates a blast condition, which forces all attachments off the port interface.

The attachment must degate any information on:

- Command bus in
- MPXPO data in
- Service in
- Multidevice response

Service Out Pwrd–One Line

If data was sent to the port by the I/O attachment, the 'service out pwrd' line signals the attachment that the port is completed with the data and the ending sequence can be started. That is, the 'service in' line and any input data to the port can now be de-activated.

If data is being sent from the port to the I/O attachment, the 'service out pwrd' line signals the attachment that the 'MPXPO bus out' line contains valid data and can now be strobed. Once the I/O device attachment de-activates the 'service in' line, the 'MPXPO bus out' lines should no longer be strobed.

Outgoing lines, such as the 'MPXPO bus out' and the 'transfer error' lines, are deskewed by the port before the rise of the 'service out pwrd' line.

Command Bus Out 0, 1, 2–Three Lines

The 'command bus out' lines are valid at the interface from the rise of the 'control out pwrd' line until the fall of the 'service out pwrd' line at the port. The 'command bus out' line, together with the 'control out pwrd' line, indicates which data is on the 'MPXPO bus out' lines. The attachment operator who recognizes his code responds by making the 'service in' line active with the correct information gated on the 'MPXPO data in' and 'command bus in' lines.

The 'command bus out' lines are defined as follows:

Bits 0 1 2	
0 0 0	Not used.
0 0 1	Sense Interrupt Status–Determines which devices are requesting service on a given microinterrupt level.
0 1 0	Cycle Steal Response–The attachment cycle steal request is being serviced.
0 1 1	Jump–The control processor jumps if the I/O attachment responds with the jump on I/O condition met.
1 0 0	Load–Data is gated from the control processor LSR, control storage, or main storage.
1 0 1	Sense–Data is written into control storage, main storage, or the control processor LSR.
1 1 0	Control Load–Data is gated from the control processor LSR.
1 1 1	Control Sense–Data is written into the control processor LSR.

Strobe Pwrd–One Line

Note: All times shown below are for reference only. Operation of the system does not rely on these times, but on the sequence of these signals. This is a pulse that comes on 200 nanoseconds after the 'control out pwrd'/'service out pwrd' lines and pulses with a cycle of 800 nanoseconds and a length of 400 nanoseconds. This pulse de-activates after the rise/fall of the last 'service in' or 'multidevice response' line. A full pulse width is maintained. This pulse will rely on the device usage as follows:

1. If the device uses this line to generate the 'service in' line, the system will operate in a synchronized mode.
2. This line should be used by the I/O attachment to generate the correct data strobes/timing for loading information from the port and supply the needed gate/deskew timing for the port 'MPXPO data in'/'system bus in' lines before the rise/fall of the 'service in' line.

Data on the 'MPXPO bus out' lines will remain valid from the trailing edge of the last 'strobe pwrd' line for 100 nanoseconds. This will permit the last strobe to clock information into registers, latches, and so on.

Transfer Error–One Line

This dual-purpose line indicates a transfer error or a jump on I/O condition met echo ('JIO echo' line).

An active 'transfer error' line indicates to the attachment that not valid parity was sensed on the port or in the control processor. This line will not be activated during the 'command bus out' codes 5 and 7 when the I/O attachment makes active the 'CBI 4 gated' line (indicating not valid parity on the 'MPXPO data in' lines). It also will not be activated for the 'command bus out' code 1 (multidevice response).

A jump on I/O condition met echo ('JIO echo' line) indicates to the attachment that the control processor received the 'CBI 4 gated' line and the jump will be taken by the control processor. This enables testing of asynchronous I/O attachment conditions with the jump-on-I/O-condition instruction, and the attachment does not need to latch this line before making the 'service in' line active. Removal of this line follows the rules for all data and command lines.

Disk Burst Mode Gated–One Line

This line is active when the data moved is for the disk. The signal is activated by the port in response to the 'disk/dskt block processor clock' line when the control processor/port determines that the disk may start a burst mode operation (time T7 and the 'disk/dskt block processor clock' line and the port are not busy).

The signal will remain active until the 'disk/dskt block processor clock' line is de-activated. The 'disk burst mode gated' signal must be used to degate/gate the correct 'system bus in' signals into the control processor. When this signal is active, and not before, the disk can start its requested burst cycle.

Disk Strobe–One Line

This line becomes active at the trailing edge of a disk storage cycle with a length of 100-230 nanoseconds. On a storage-to-disk operation (CBI bit 1 active), data is valid at the disk attachment approximately 50 nanoseconds after the trailing edge of the 'CSY trigger' signal and should remain valid until the next disk storage cycle or until the 'disk/dskt block processor clock' line de-activates.

CSY Trigger–One Line

This line becomes active 100 nanoseconds after the storage clocks in the control processor have started to run. The timing width is 300 nanoseconds. This signal is used to reset a cycle steal request if the device that has requested the cycle steal is being serviced.

Attachment to Port Lines

MPXPO Data In–Nine Lines

These lines send data from the attachment to the port during I/O sense and cycle steal sense operations.

A parity bit is generated by the attachment to maintain odd parity for I/O sense and cycle steal sense. Data parity is checked unless the device activates the 'CBI bit 4' line (not valid parity in). During cycle steal, the attachment always sends valid parity on the 'MPXPO data in' lines. (The 'CBI bit 4' line has more than one purpose and is interpreted as a control storage move operation during cycle steal.)

During an I/O sense or cycle steal sense operation, when the parity is valid, the port 'MPXPO data in' lines must be held stable from the rise of the 'service in' line, when activated by the attachment, until the rise of the 'service out pwrd' line.

During an interrupt sense operation, the microinterrupt status bit must be held stable from the rise of the 'service in' line and the 'multidevice response' lines, until the rise of the 'service out pwrd' line.

Service In–One Line

All Operations

This line should be activated by the rise of the 'strobe pwrd' line and is used by the addressed attachment to signal the port that the command byte has been received by the attachment. If the command is a sense operation or cycle steal, this line informs the port that sense information is available to be strobed.

When the attachment de-activates the 'service in' line, it should no longer sample the 'MPXPO bus out' lines. The I/O attachment should not sample the 'command bus out' lines after it de-activates the 'service in' line.

Attachment To Port 'Service In' Change

When data is sent to the port, the data must be valid by the time the last 'strobe pwrd' pulse under the 'control out pwrd' line is de-activated (all measurements are made at the port card tab pins). All incoming lines must remain valid until the 'service out pwrd' line is sensed by the I/O attachment and must be de-activated by the attachment before de-activating the 'service in' line. An exception to the above rules is permitted on I/O sense, I/O control sense, and jump on I/O condition commands; on these commands, all lines must be removed by the I/O attachment (as seen at the channel tab pins) by the time the last 'strobe pwrd' line pulse de-activates (as seen at the channel tab pins).

Port to Attachment

When data is moved from the control processor, a local storage register, or control storage, the rise of the 'service in' line indicates that the command was received and the I/O attachment is ready to receive the second byte of information. If the operation is a cycle steal, it indicates that the cycle steal 'command bus in' lines are valid. When the 'service out pwrd' line has been received and the 'MPXPO bus out' lines have been strobed, the I/O attachment de-activates the 'service in' line.

Time-out Conditions

If the addressed device is not on the system, or if the 'MPXPO bus out' lines contain bad parity, none of the devices will answer the control out sequence. The port will time-out for such conditions. When the time-out sequence (5.4 microseconds) is completed, a not valid device address (bit 1) is set in the port checks register. A 'blast condition' line in the port clears all the incoming data and control lines from the I/O attachments.

If the addressed device first responds with a 'service in' line but fails to de-activate the 'service in' line when receiving a 'service out pwrd' line after a set length of time (5.4 microseconds), the port will time out. This condition is set in the port checks register, and the port uses a 'blast condition' line to clear all incoming data and control lines.

Microinterrupt Request–Five Lines

An interrupt is started by a device through its I/O attachment when the device needs a program response.

To ensure correct channel operation, this line should be reset by an I/O load or I/O control load function before de-activating the 'service in' line. Removal of an active request should follow the rules for degating port data and command lines.

Multidevice Response–One Line

This line is always held not active (minus) by each device. When a multidevice command occurs, this line, along with the 'service in' line, is used by the port to indicate when the last device on the port has received the command.

In response to the 'control out pwrd' and the 'command bus out' lines that identify a multidevice command, the device will decode the modifier field to see if the command is for the device. If information is needed from the device, the data is gated to the 'MPXPO data in' lines and the device activates the 'multidevice response' and 'service in' lines. Devices that do not respond with data are still needed to activate the 'multidevice response' and the 'service in' lines. When receiving the 'service out' line, the device must degate this data in and have zero skew relative to removal of the 'service in' line (if data was gated in) and de-activate the 'multidevice response' line.

Base Cycle Steal Request–One Line (Per Device)

A 'base cycle steal request' line supports an I/O attachment that has cycle steal ability and is connected to the port.

The I/O attachment makes active its 'base cycle steal request' line to start a cycle steal operation. This line should de-activate when the I/O attachment recognizes its acknowledge code on the 'MPXPO bus out' lines and before responding with the 'service in' line.

Disk/Dskt Block Processor Clock–One Line

This signal is active when the disk is moving data from or to storage.

Disk/Dskt (Load) BC Req–One Line

This line is used by the disk attachment to start burst cycle steal operations. It is also used by the diskette during the control storage initial program load (CSIPL) sequence and by the diskette level 2 attachment to start cycle steal operations.

Command Bus In (Bits 0, 1, 2, 3, 4, 5)–Six Lines

Bits 0, 1, 2, and 3 of the CBI are used to control the cycle steal operation and LSR selection. Bit 4 is a multiusage line. It indicates that the device is cycle stealing into or out of control storage, that 'MPXPO data in' lines contain valid parity during a sense command, or that the jump on I/O condition has been met. When the device is cycle stealing into or out of control storage, the low byte is selected by the CBI bit 0. This bit also controls the address update. Bit 5 indicates that the device has detected invalid parity on the 'MPXPO bus out' lines.

Bits 0 1 2 3 4 5	
0 0	[1]Cycle steal sense–No increment address
0 1	[1]Cycle steal load–No increment address
1 0	[1]Cycle steal sense–Increment address
1 1	[1]Cycle steal load–Increment address
0 0	[1]Cycle steal LSR select 0
0 1	[1]Cycle steal LSR select 1
1 0	[1]Cycle steal LSR select 2
1 1	[1]Cycle steal LSR select 3
1	Control storage/MPXPO data in has invalid parity or jump on I/O condition met
1	MPXPO data out parity check

[1]May be either burst cycle steal mode or base cycle steal mode

Direct Lines–Control Processor/Attachments

Power On Reset–One Line

This line is active when the Power switch on the operator panel is off. When the Power switch is turned on, this line remains active for 1 to 2 seconds and then becomes not active until the Power switch is turned off.

System Reset–One Line

This line indicates to the I/O attachment that all logic should be initialized to a start condition. This line becomes active during power on reset, or when the Reset switch on the CE panel is pressed or when the Load switch on the operator panel is pressed.

Control Storage Initial Program Load (CSIPL) Latch–One Line

This line, together with the CSIPL switch on the CE panel, is decoded by the disk or diskette to determine which device enters data during initialization.

CSIPL Cycle–One Line

The active state of this line selects the diskette, and the not active state selects the disk during the initial program load (IPL) sequence.

Interface Clock Times–Eight Lines

These lines go from the control processor to the I/O attachments and provide clock times to gate and control attachment functions. The clock lines are as follows:

- 100 ns
- 1 μs
- 4 μs
- 512 μs
- 1.02 ms
- 16.38 ms
- 131.1 ms
- 1,048 ms

Burst Cycle Steal Mode

The system uses a burst mode data transmission to support the high data rate of the disk.

The disk attachment activates the 'disk/dskt block processor clock' line, which forces the control processor to time T7. (If the control processor is executing an instruction, time T7 does not become active until the instruction is completed.)

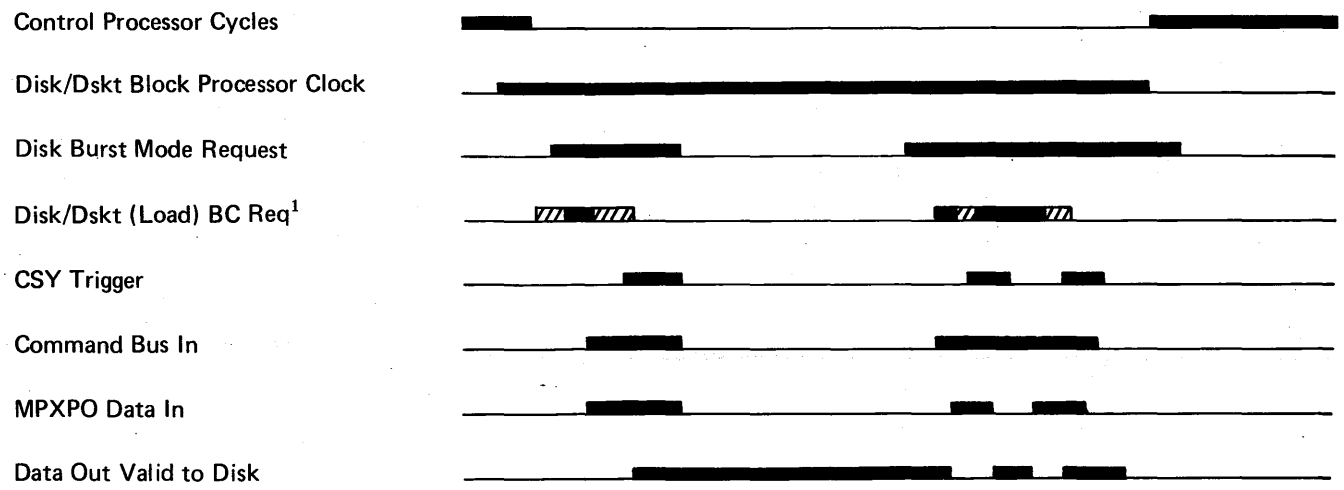
Once time T7 is active, the port makes active the 'disk burst mode gated' line and then the 'command bus in' line will be correctly set.

When time T7 and the 'disk burst mode gated' line are both active, the disk attachment activates the 'disk/dskt (load) BC req' line and puts the first byte of data on the 'data bus in' lines (incoming operation). The rise of the 'disk/dskt (load) BC req' line while the 'disk/dskt block processor clock' line is active generates a 'storage cycle request' line which, in turn, generates time T8 (clock SAR and X-reg). The burst cycle starts and the rise of the 'CSY trigger' line latches the data in the data buffer. This data is gated to the 'system bus in' lines and from there into the storage address indicated by the contents of the storage address register. Each time the 'disk/dskt (load) BC req' line is active, a byte of data is moved. If the 'disk/dskt (load) BC req' line is kept active, the control processor continues to take storage cycles at the maximum data transmission rate.

While data is being moved to the disk, the 'disk strobe' line clocks the data from the port data buffer into the data buffer in the disk attachment. The disk attachment then writes the data on the disk.

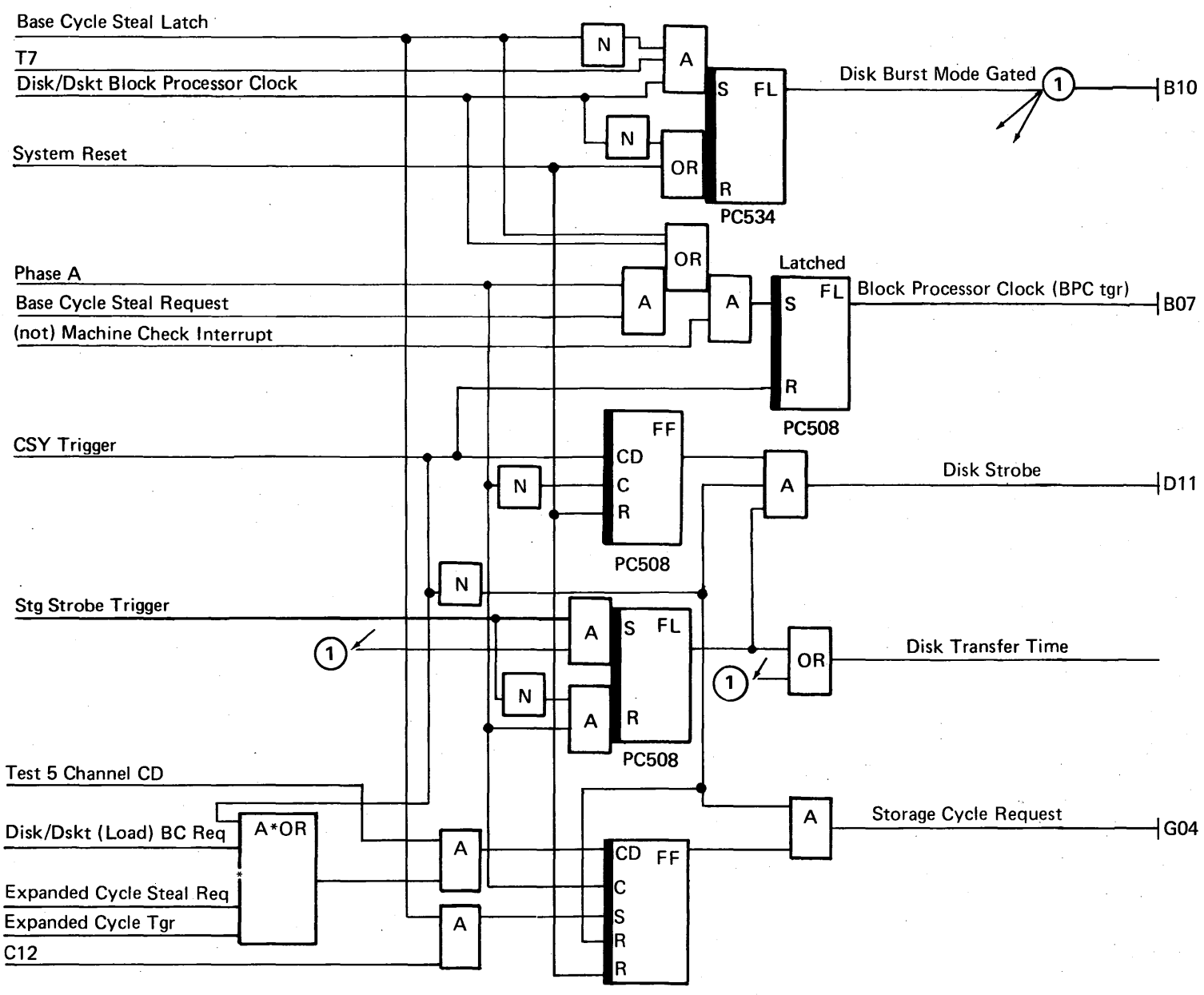
The diskette forces burst mode during CSIPL when loading the first 2K words from the diagnostic diskettes.

Disk Support Timing

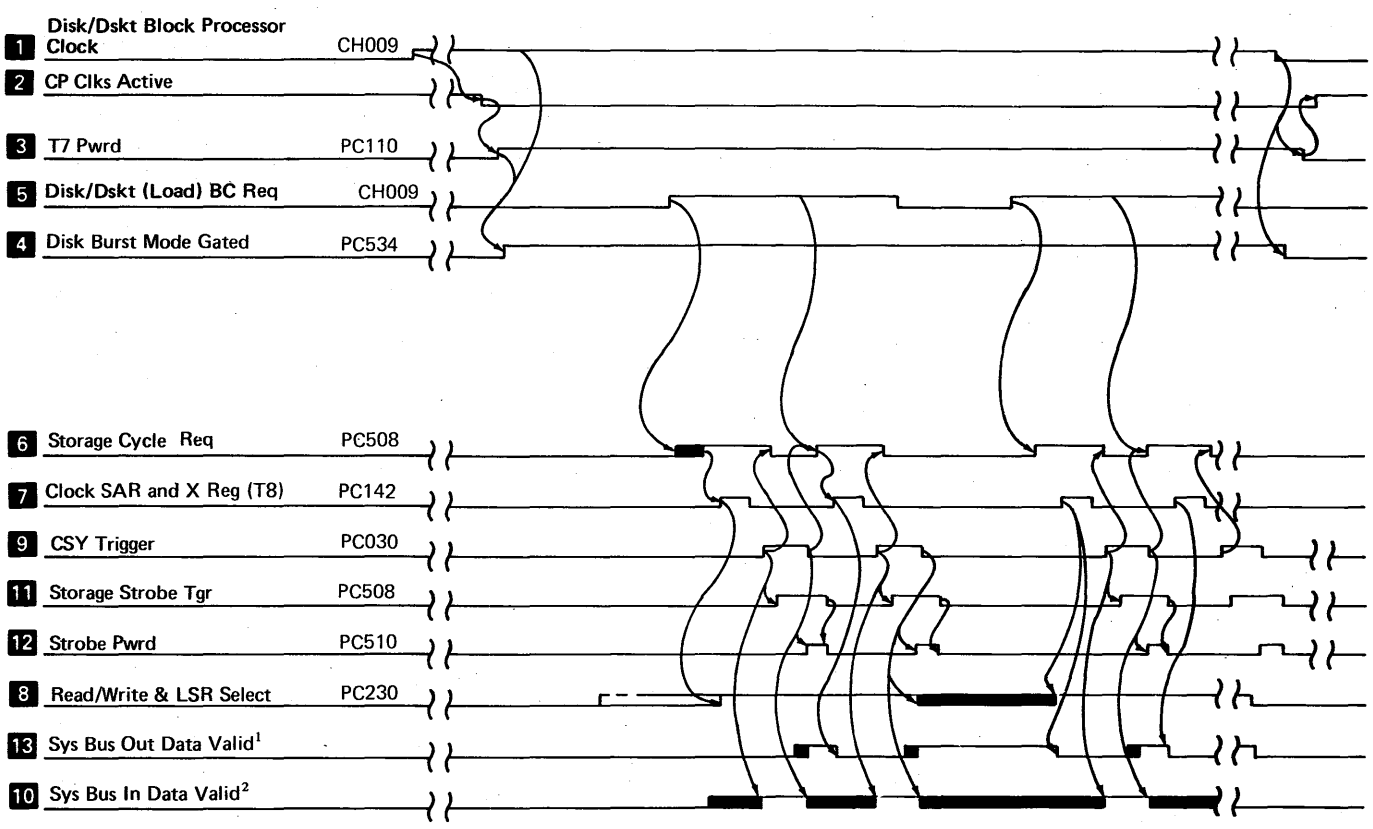


[1] BC = Burst Cycle

Disk Support Lines

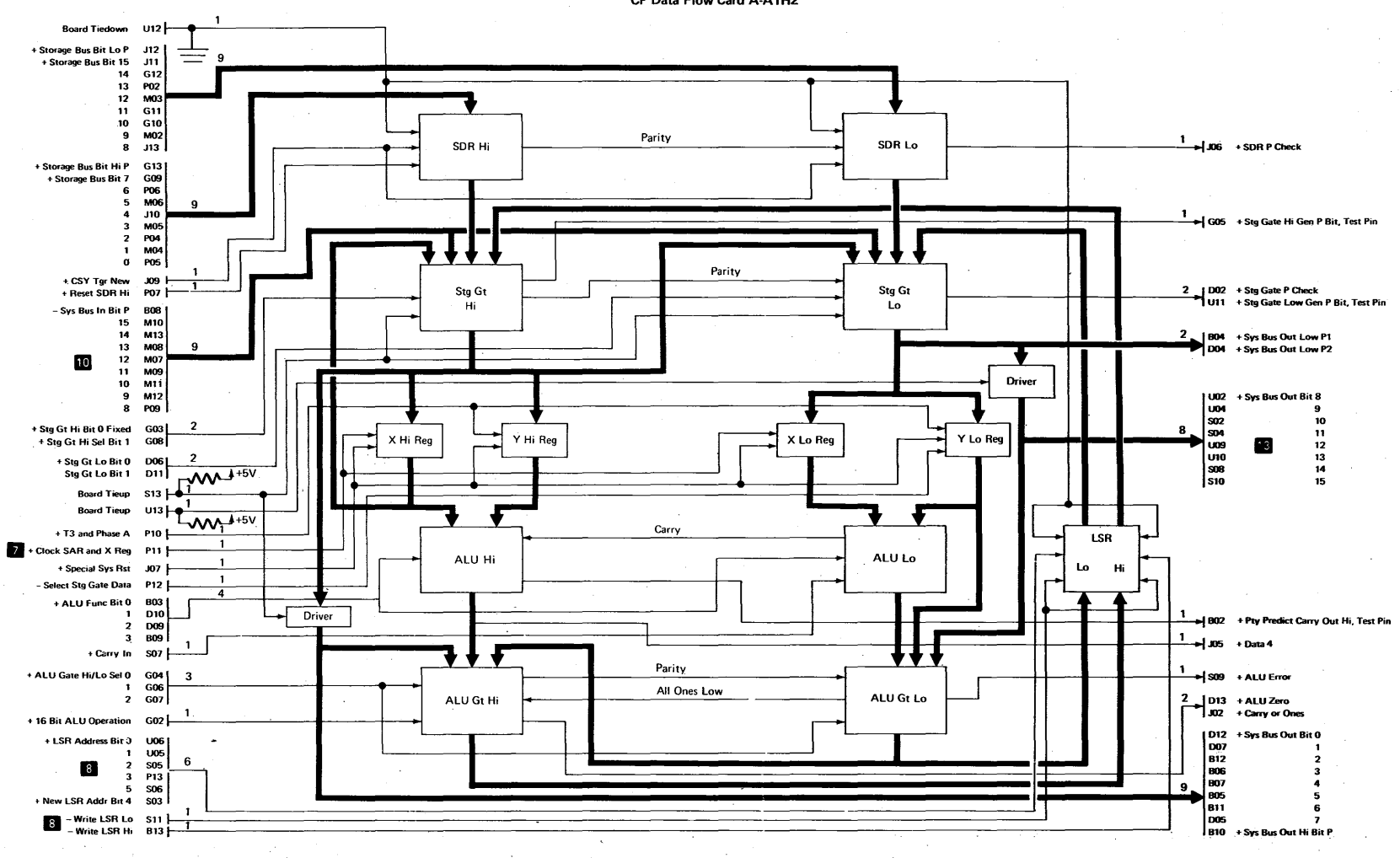


Burst Cycle Steal Mode (Operational Sequence)

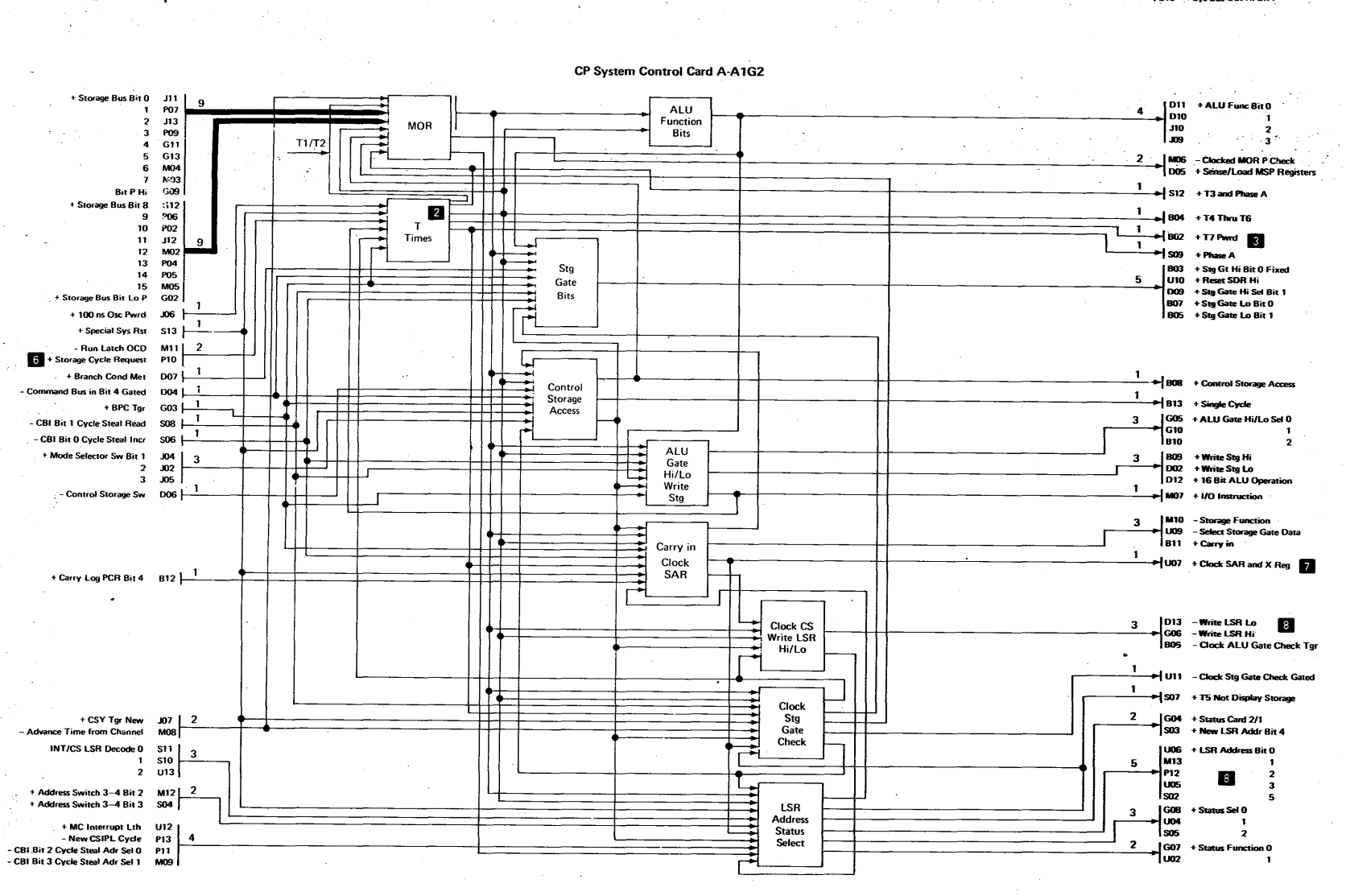


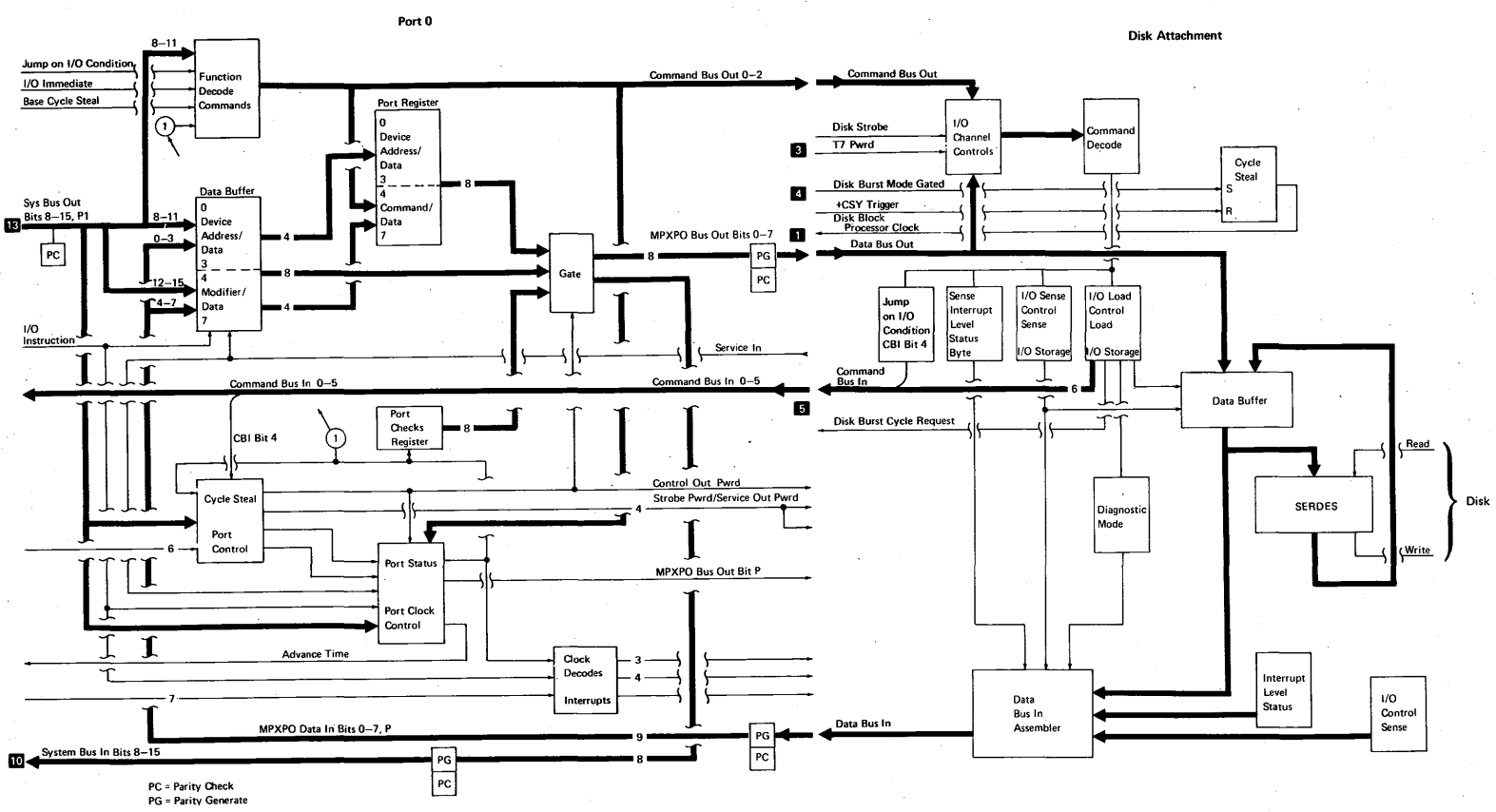
[1] Data is moved from the control processor to the disk.
[2] Data is moved to the control processor from the disk.

CP Data Flow Card A-A1H2

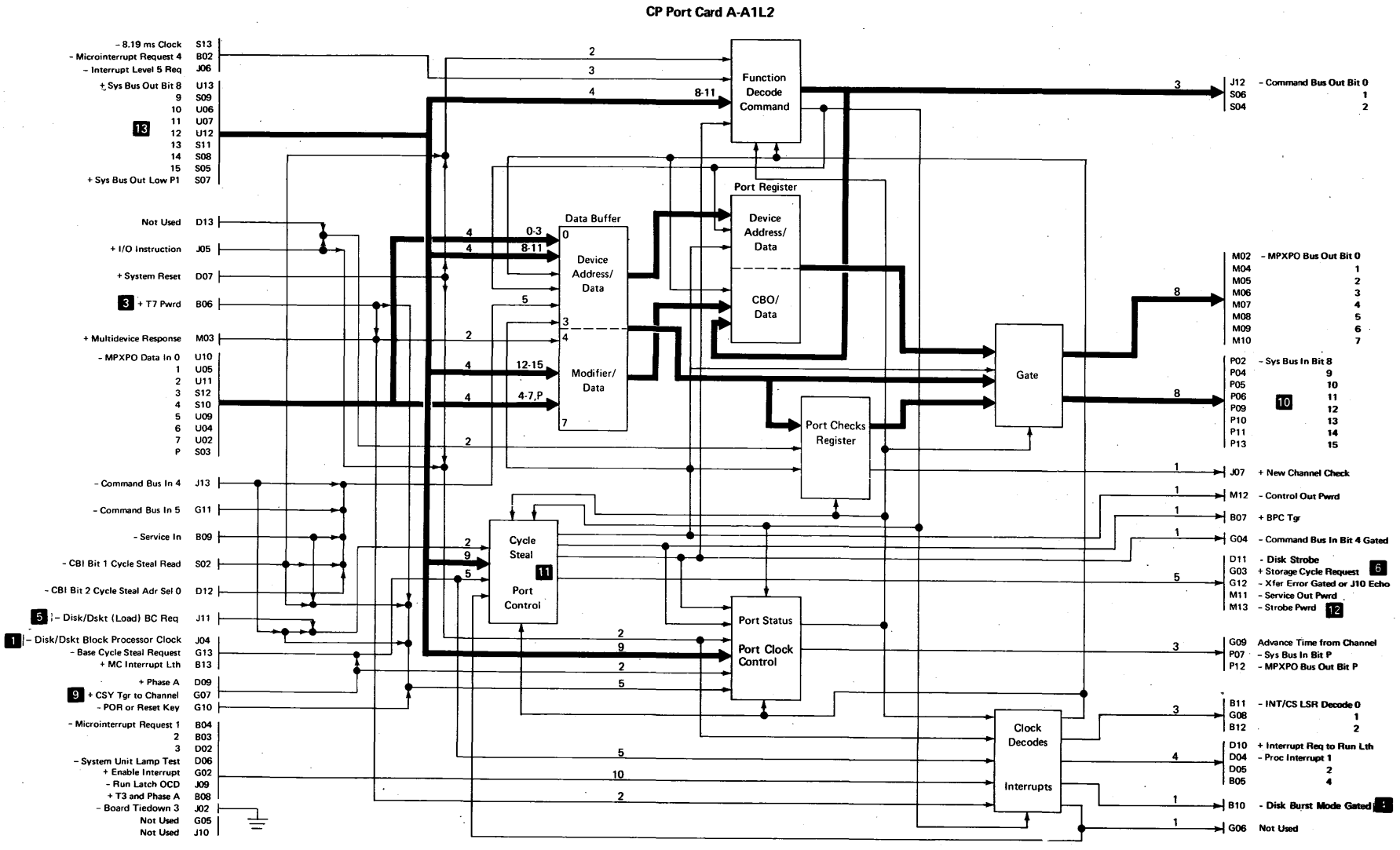


CP System Control Card A-A1G2

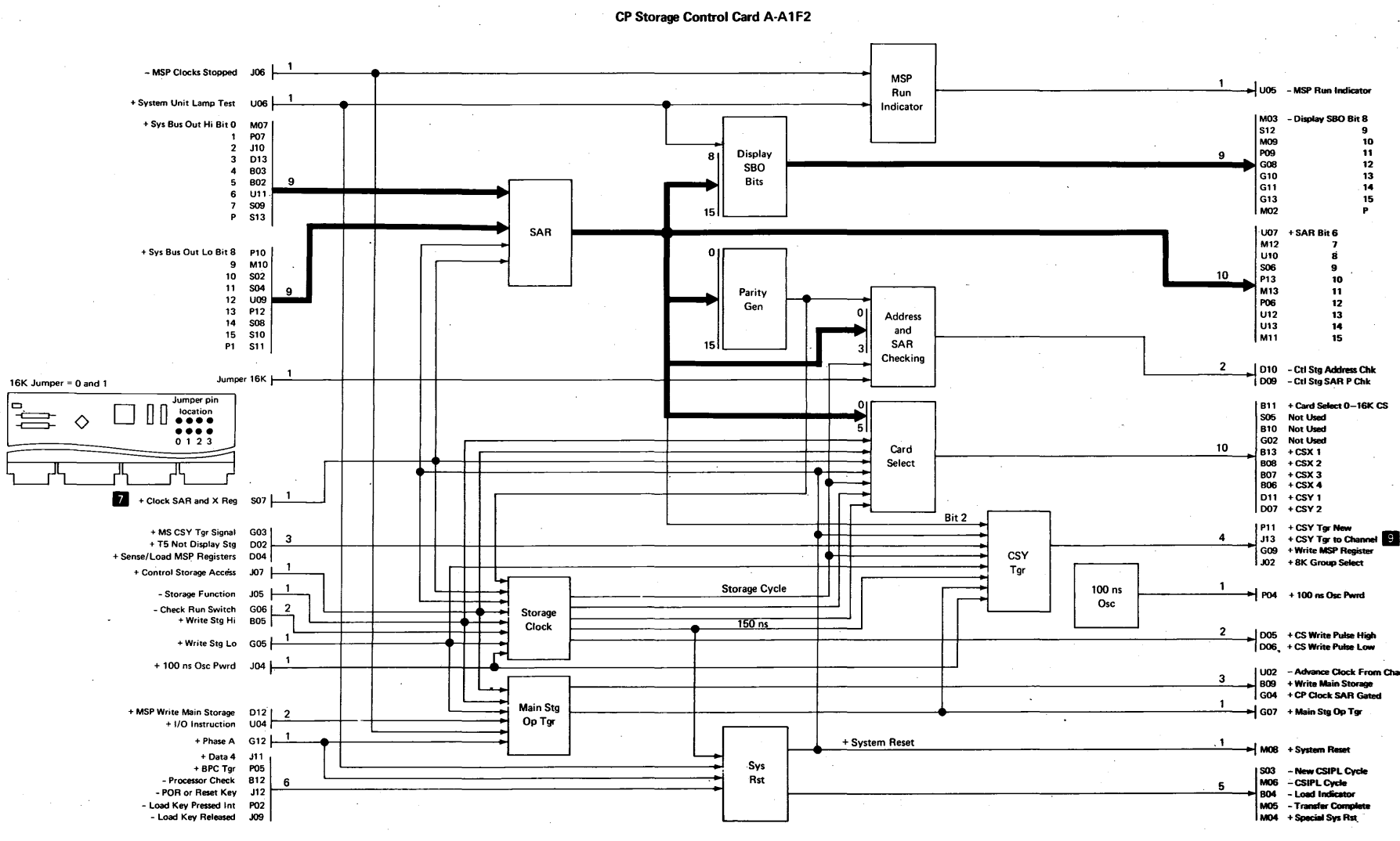




CP Port Card A-A1L2



CP Storage Control Card A-A1F2

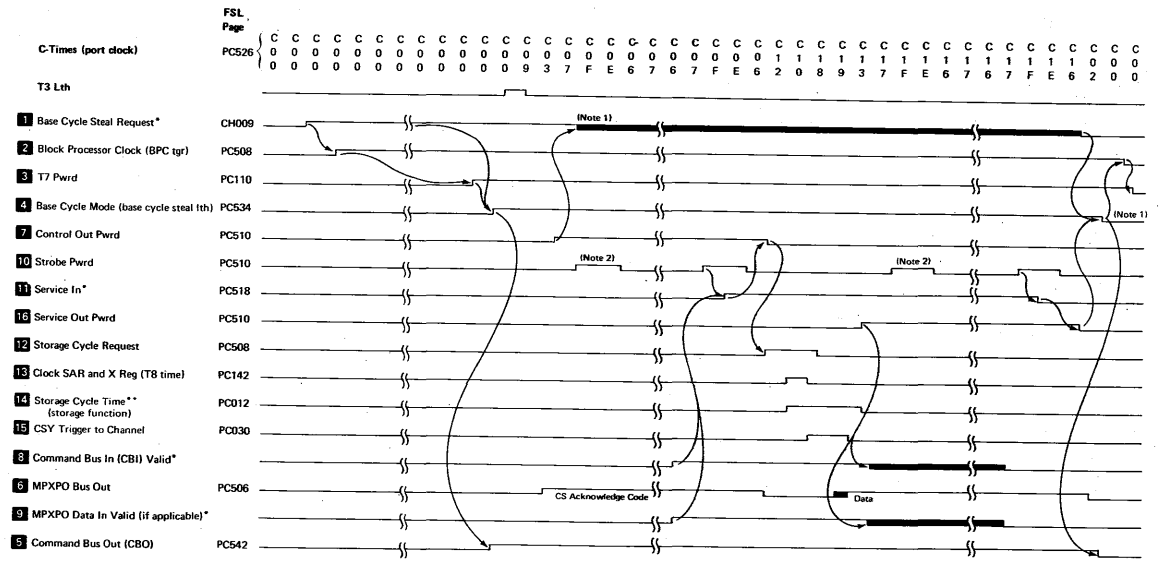


5

Base Cycle Steal Mode

Data can be moved between storage and a device attached to the port by the base cycle steal mode of operation. The port and I/O attachment use a timing sequence to move data as shown below. One byte of data is moved for each request. The cycle rate relies on the I/O attachment and the condition of the higher priority needs (burst cycle steal or interrupt level 1) of the system. The maximum possible data cycle rate is 1 byte per 3.5 microseconds. This mode has a system priority less than burst cycle steal mode but can be of any lower priority under I/O attachment control.

The work station attachment uses the base cycle steal mode of operation to move data from the control processor to the work stations.



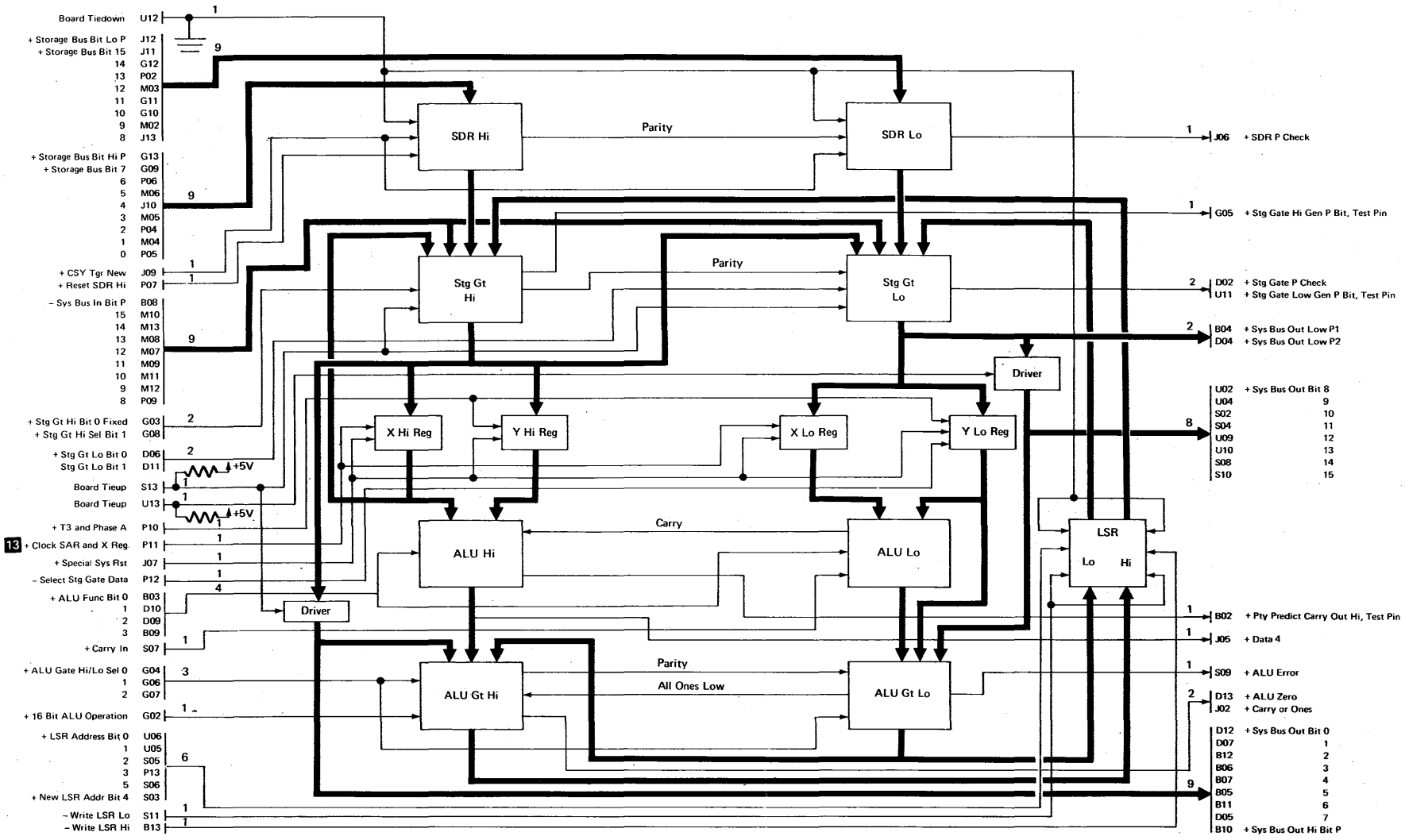
Notes:

1. This example shows only one base cycle steal occurring. The entire handshaking sequence would occur again if 'base cycle steal request' remained active beyond the time shown (provided no disk cycle steals were requested).
2. If the I/O device responds to 'control out pwrd' and 'service out pwrd' in synchronous operation, only one strobe will occur under each tag line. Otherwise, up to 7 strobes may occur in each portion of the sequence for asynchronous operation. If 8 strobes occur, a time-out occurs and a blast is generated.

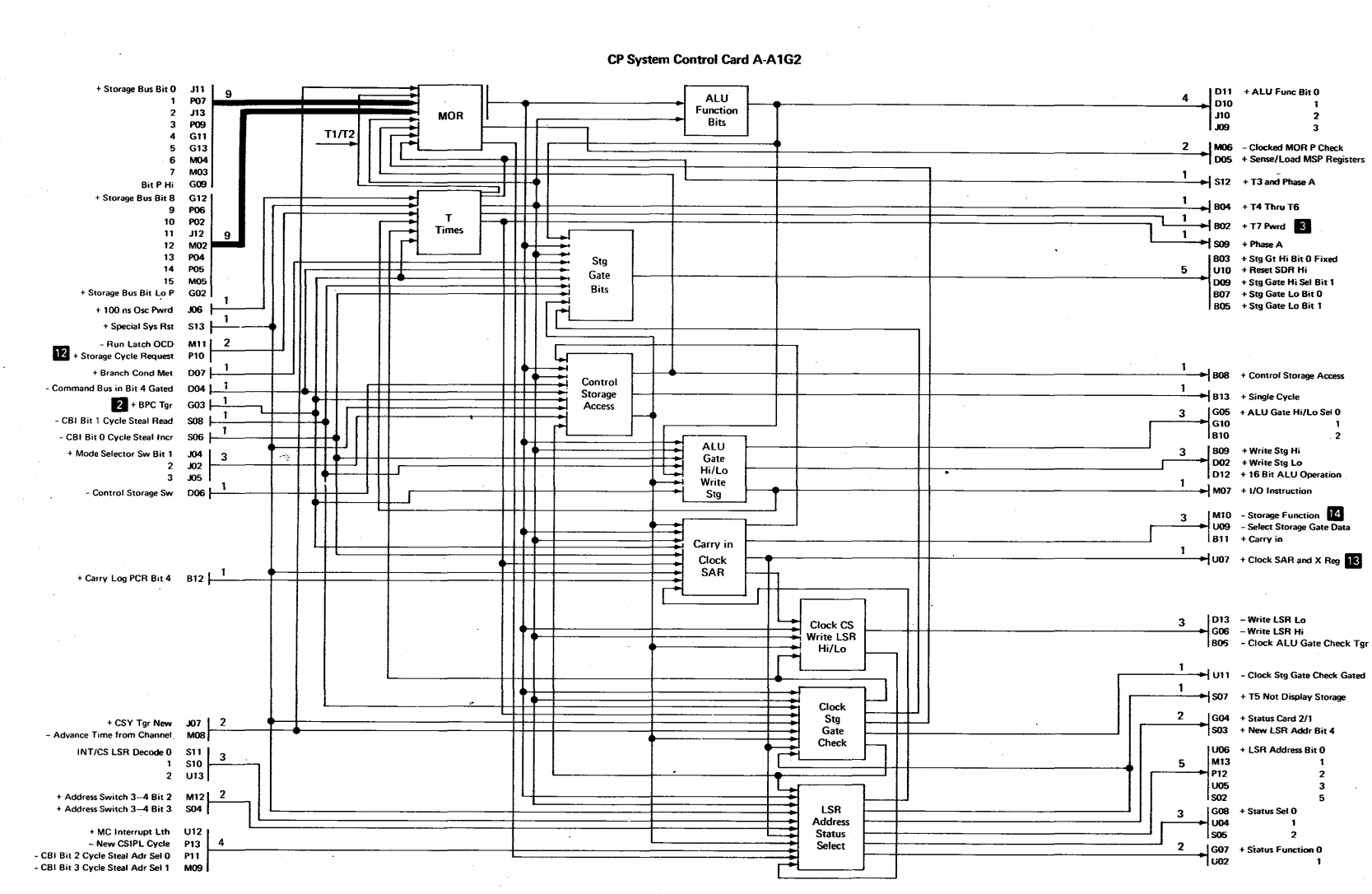
*Signifies signals for the device attachment to the base port card.
**The 'storage cycle time' consists of the time for loading the storage address register (T8), the time for accessing storage (X CSY Tgr), and a time for storing data to the I/O attachment.

Base Cycle Steal Mode (Operational Sequence)

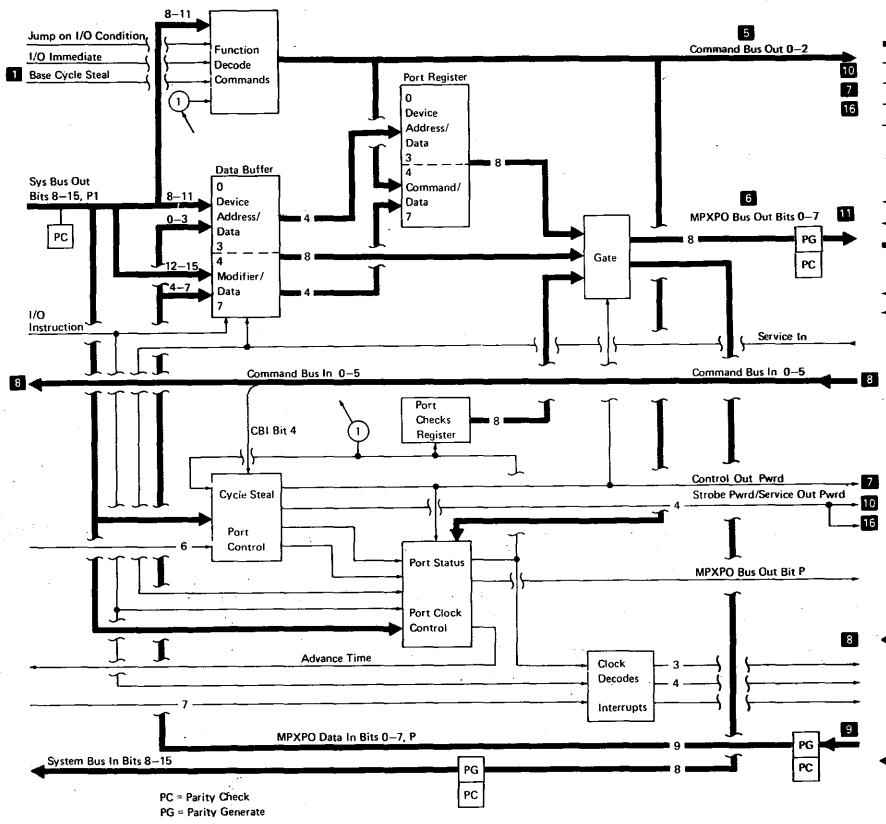
CP Data Flow Card A-A1H2



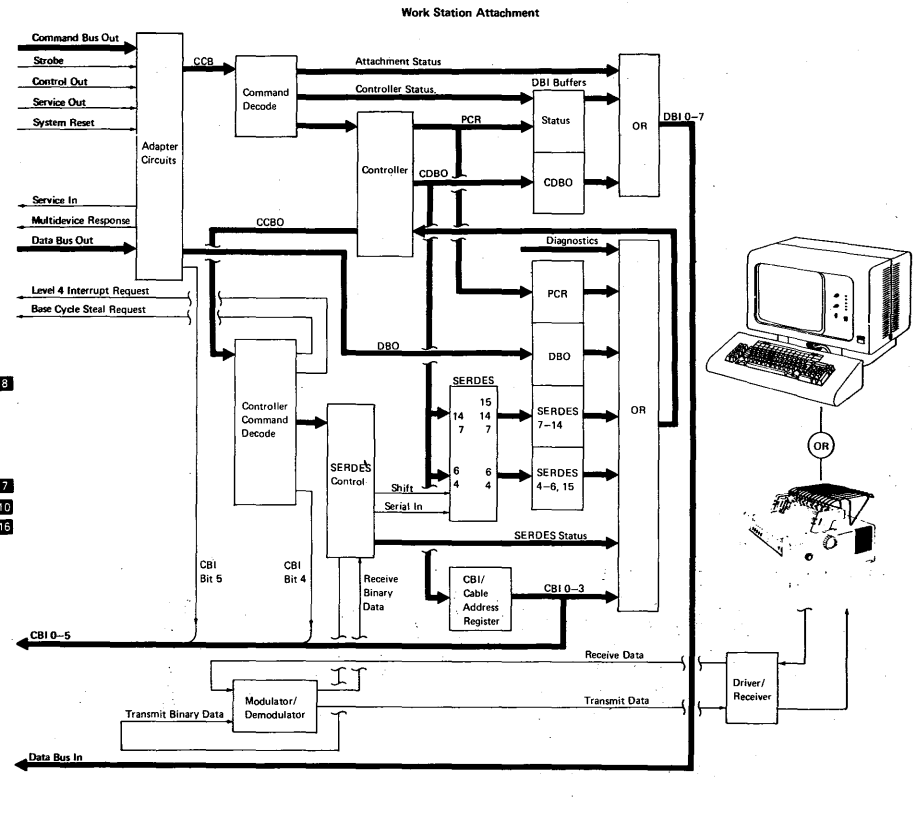
CP System Control Card A-A1G2



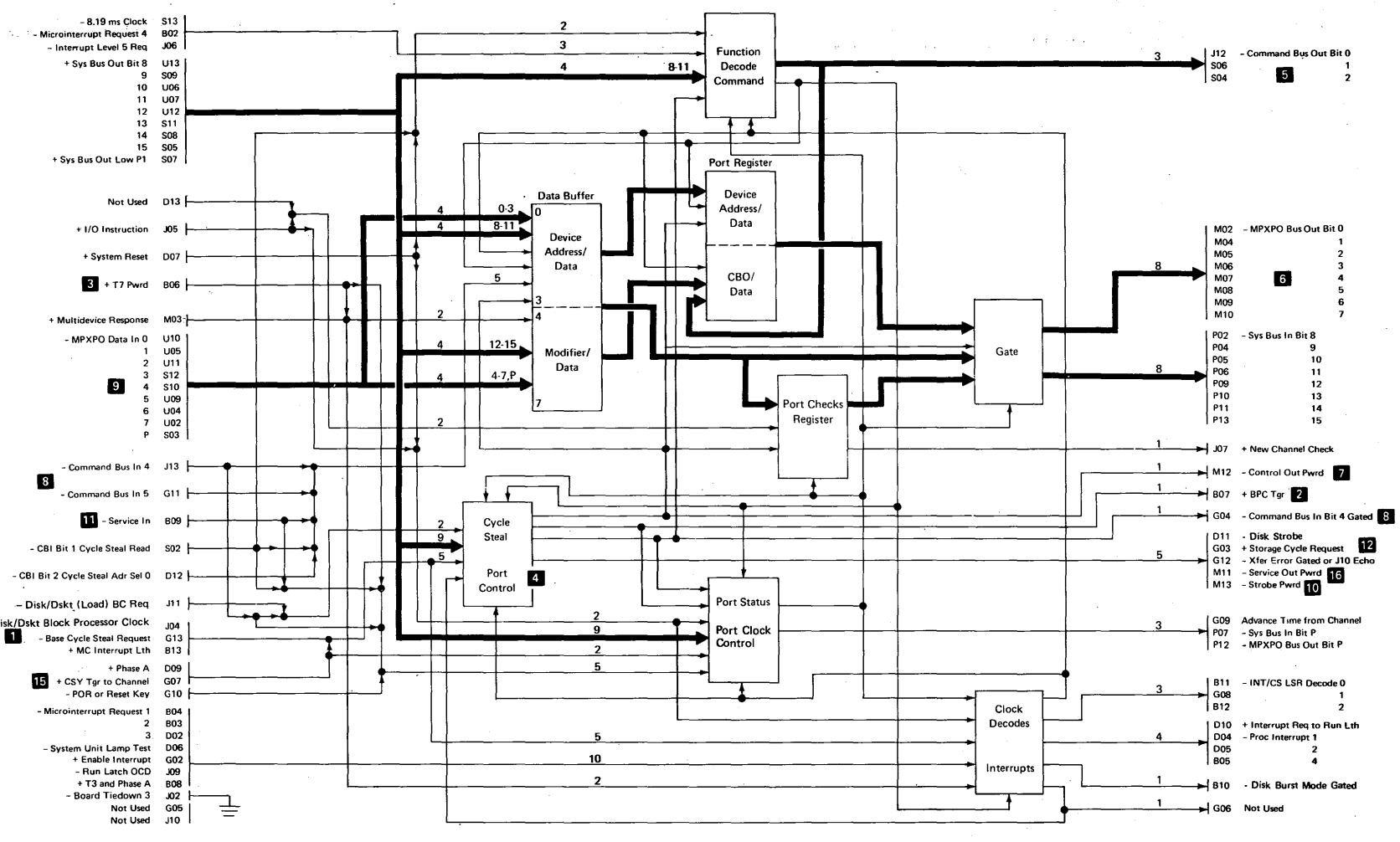
Port 0



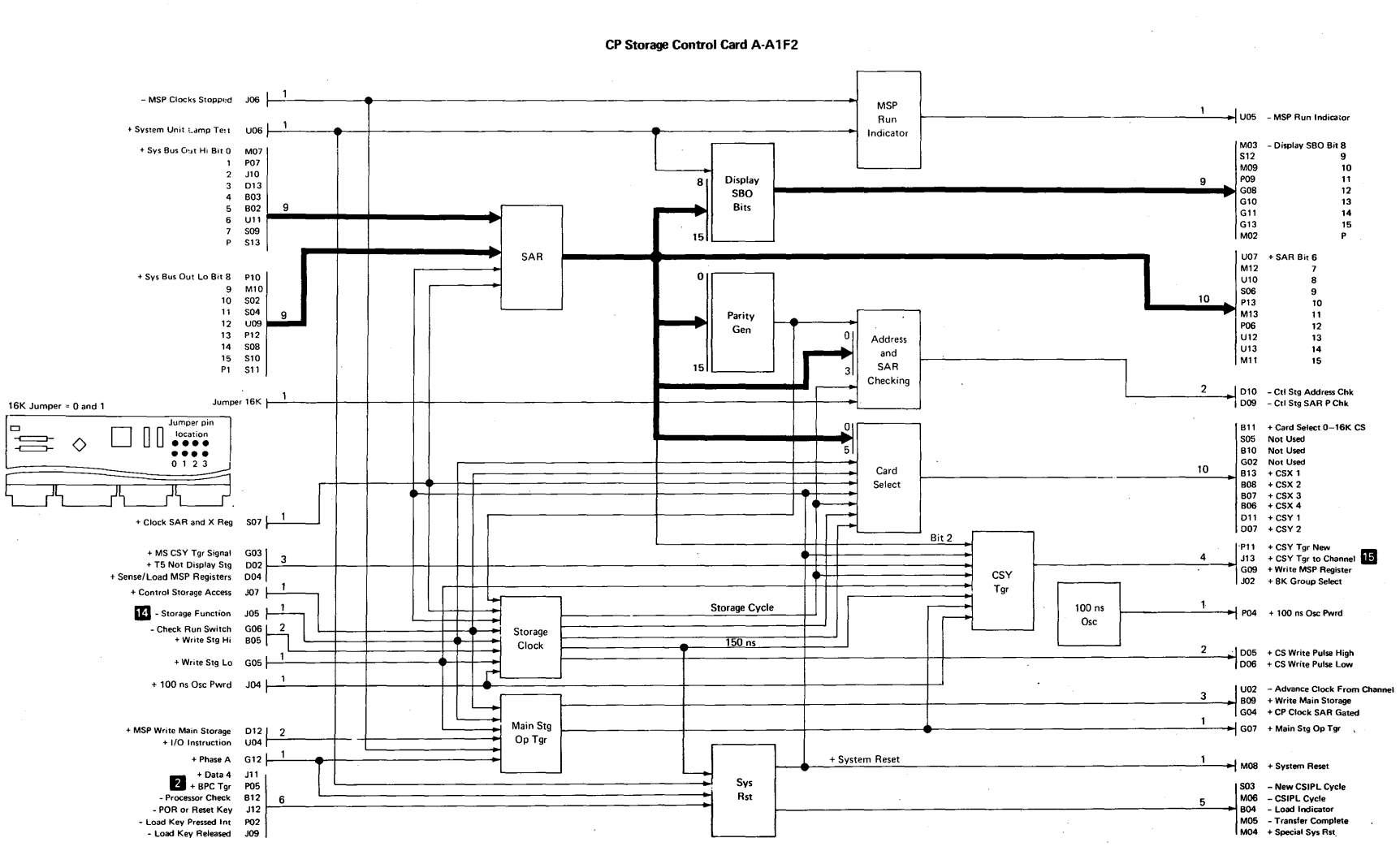
Work Station Attachment



CP Port Card A-A1L2



CP Storage Control Card A-A1F2



Microinterrupt Level Mode

All I/O devices that need processing can activate a microinterrupt to the system. The port is the means by which the system receives the interrupt.

The five interrupt request lines (IL 1-5) are made active by a device through its attachment whenever the device requires program interaction. To have proper interrupt operation, any request line should be reset by an I/O load or I/O control load function before the drop of the 'service in' line. Removal of an active request should follow the rules for degating the 'MPXPO data in' and 'command bus in' lines. (See the *Interrupts and Cycle Steal Requests* section of this manual.)

Channel Exerciser Loop Program

This loop program can be used to test the channel with the disk, line printer, or diskette.

Directions for entering and exercising the loop program are as follows:

1. Reset the PMR and CMR by momentarily grounding A-A1Q2D13.

2. Press the Reset switch on the CE panel (resets MAR to hex 0000) and load the following program:

Address	Instruction	Comment
0000	B960	Sense switches 1 and 2 into WR0(L)
0001	B569	Sense switches 3 and 4 into WR1(H)
0002	B909	Load data buffer with test data
0003	B941	Sense data buffer into WR1(L)
0004	0002	Branch

   Switches 1 and 2 select the device ID:

   A0 = disk
   E0 = printer

   Switches 3 and 4 contain the test data.

3. Select the device ID and test data in the switches, press the Reset switch and step through the program once. Upon stepping through:

   WR0(L) contains the device ID.
   WR1(H) contains the test data.
   WR1(L) contains the sensed data.

   Note: The sensed data for the printer will be the complement of the test data, due to the polarity hold circuitry in the printer adapter card.

4. Rotate the Mode Selector switch from the Insn Step/Dply LSR position to the Proc Run position, press the Reset switch and then the CE Start switch. The program will loop from hex 0002 to hex 0004.

5. Use the following loop program to test the diskette with the channel:

Address	Instruction	Comment
0000	B960	Sense switches 1 and 2 into WR0(L)
0001	BB48	Sense hex FF into WR0(H)
0002	0001	Branch

   Note: If the modifier of the instruction at hex address 0001 is changed to D, the sensed data will be hex F0; if the modifier is changed to E, the sensed data will be hex 0F.

COMMANDS

The three instructions that communicate with the processing unit, the port, and the I/O attachment are:

- I/O immediate
- I/O storage
- Jump on I/O condition

When executing the I/O command, the processing unit selects WR0 low from the local storage register stack for the current interrupt level and sends its contents to the channel and then to the port. The format of WR0 low is:

Device	WR0 Low Bits 0-3 4-7 Hex Address
Channel/port	0 0
Unit record MICR (1255)	5 0
Communications	8 0
Disk A	A 0
Disk B	B 0
Work station	C 0
Diskette	D 0
Line printer	E 0

The address part of WR0 low is replaced by the interrupt level hexadecimal value on a sense interrupt level status byte command. The instruction modifier field (bits 4-7 of the I/O instruction) and the device address link together and are sent over the port 'MPXPO bus out' and 'command bus out' lines to the correct I/O attachment.

The port register stores the last command and device address sent by the port. This information is not destroyed after an error is sensed, and a sample can be taken by the interrupt level 0 (machine check) routine to determine which device caused the error.

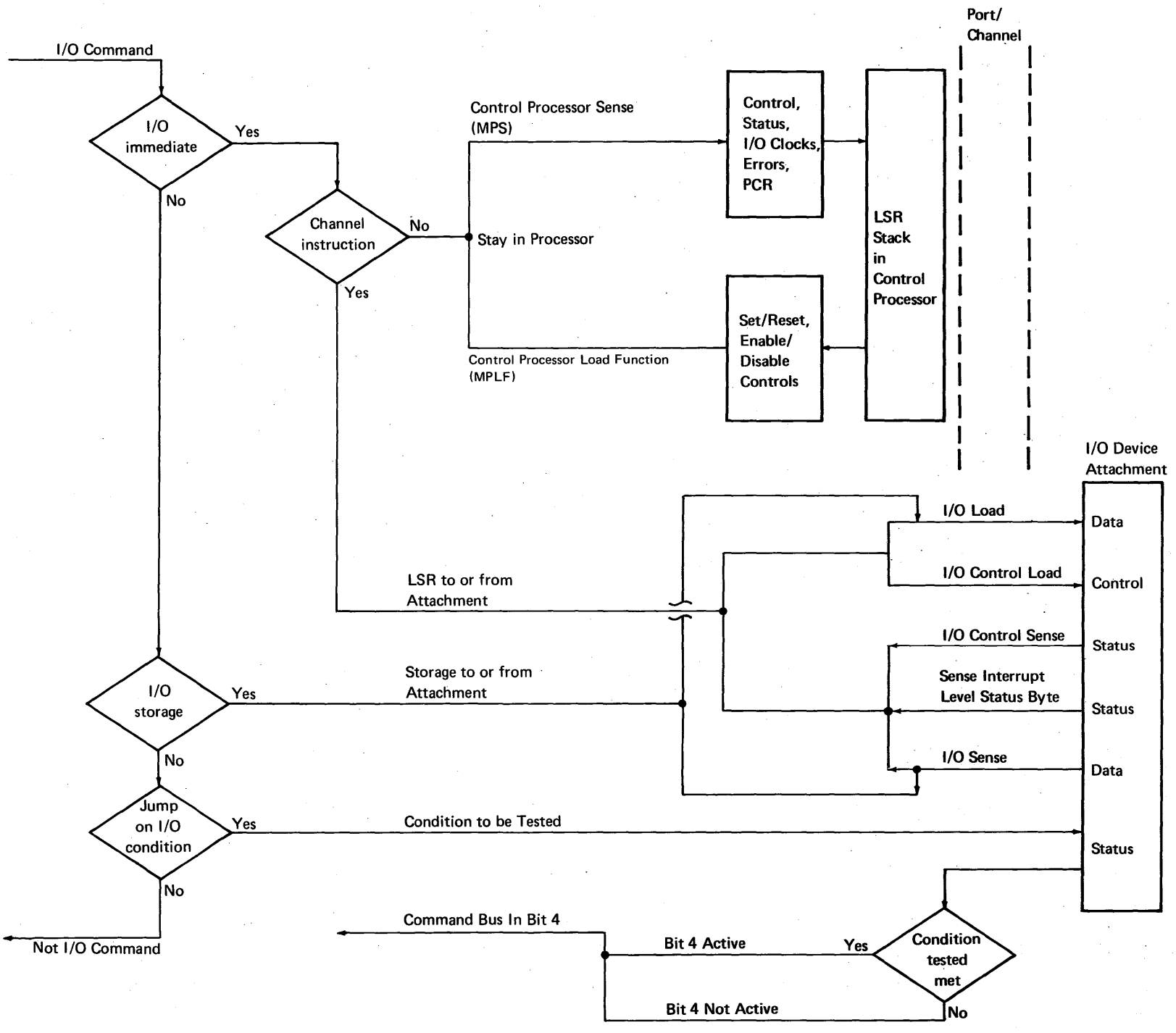
When diagnostic programs are run, the port register reads/writes data from/into local storage registers when the wrap routines are run. When the port register is used in diagnostic mode, preceding information about the device address and command bus out is destroyed.

The processing unit operates with odd parity; the port, however, can be set to either even or odd parity (see *I/O Load or I/O Control Load* later in this section).

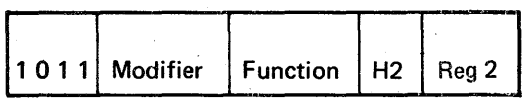
The I/O attachments use the 'CBI bit 4' line to:

- Show that the condition tested by the jump on I/O condition is met and the control processor should take the branch.
- Indicate not valid parity on the 'MPXPO bus out' lines.
- Indicate to the control processor when to address control storage during an I/O storage operation.

The 'transfer error' line is activated from the control processor to indicate a jump on I/O condition echo met (the control processor received the 'CBI bit 4' line correctly), and the branch will be taken. This line also indicates that a not valid parity was sensed during an I/O operation.



I/O Immediate



The I/O immediate instruction has four main functions:

- Move 1 byte of data between the local storage registers and the I/O devices
- Direct control of the channel and the I/O functions that may or may not include data movement
- Direct control of the control processor functions
- Direct control of the main storage processor functions

Modifier (Bits 4-7): The modifier bits rely on the device usage and are sent to the I/O attachment. These bits, along with the command bus out (CBO) bits, specify which task is to be done by the attachment.

Function (Bits 8-11): The function bits are sent to the port where they are decoded as one of the following commands: load, sense, control load, or control sense. This command is then sent to the I/O attachment on the 'command bus out' lines.

If bits 10 and 11 = binary 10, the command does not go to the port but remains in the control processor. For a bit definition of the sense information, see the control processor sense chart under *I/O Immediate* in the *Control Processor* section of this manual.

H2 (Bit 12): Selects the high- or low-order byte of the selected local storage register for the current interrupt level.

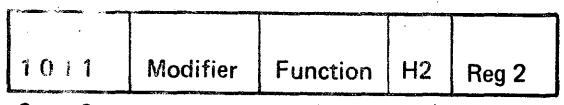
H2 = 0: Low-order byte

H2 = 1: High-order byte

Register 2 (Bits 13-15): Selects one of the eight work registers in the local storage register stack for the current interrupt level. This register is used for the byte of data or control information that is to be sent or received.

Note: For control processor load function (MPLF) instructions, bits 12-15 are used as a second set of modifier bits.

Load or I/O Control Load (IOL, IOCL)



This part of the I/O immediate instruction moves 1 byte of data or control information from a local storage register to the I/O attachment.

Modifier (Bits 4-7): The modifier bits are specified for the device and are sent to the I/O attachment with the command. These bits specify what is to be done with the data byte.

Function (Bits 8-11): The function bits are sent to the channel where they are decoded as either the load or control load command. This command is then sent to the I/O attachment on the 'command bus out' lines.

Bits 8-11 = 0000 for IOL

Bits 8-11 = 1000 for IOCL

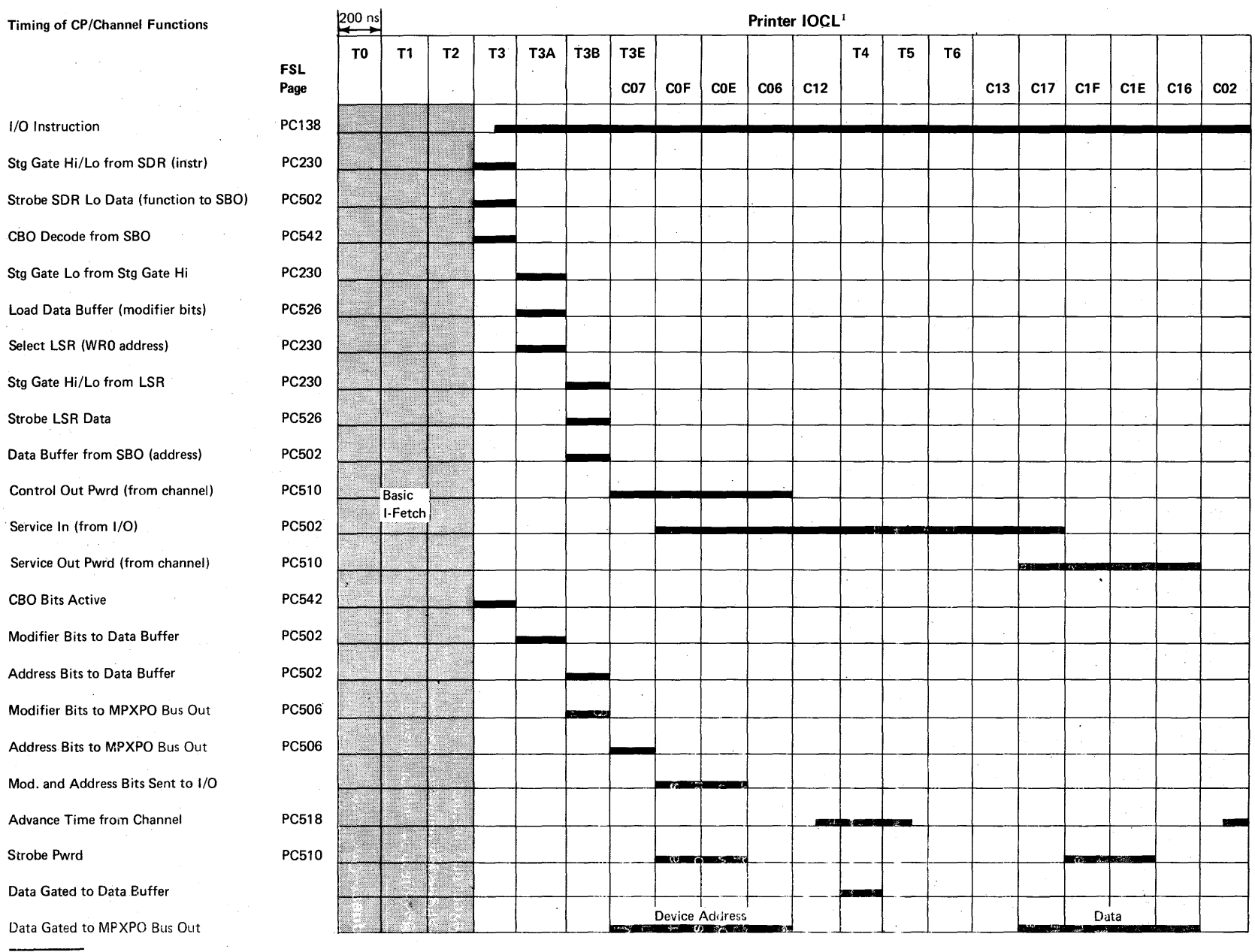
H2 (Bit 12): Selects the low- or high-order byte of the selected local storage register for the current interrupt level:

H2 = 0: Low-order byte

H2 = 1: High-order byte

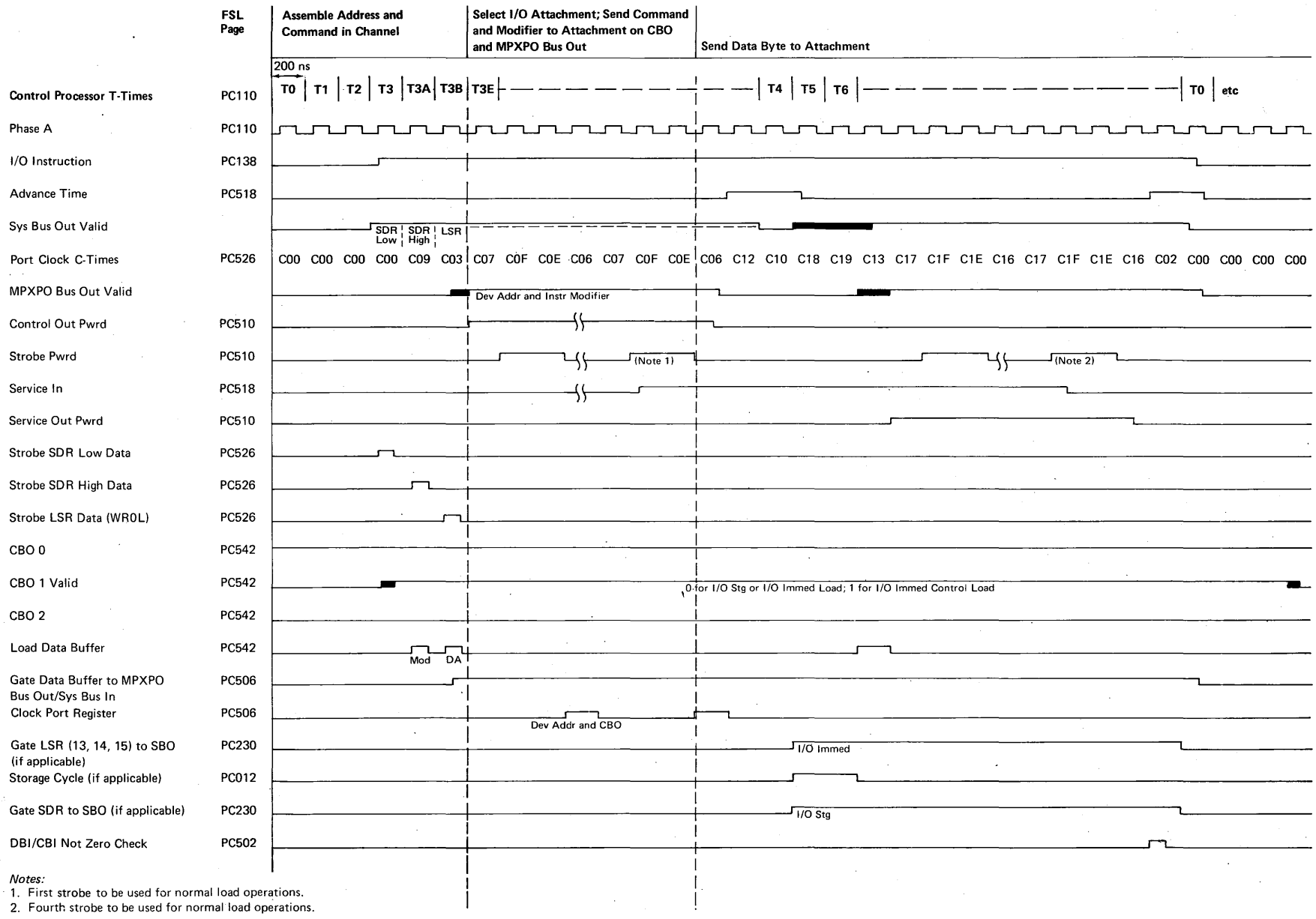
Register 2 (Bits 13-15): Selects one of the eight work registers in the local storage register stack for the current interrupt level. The selected register contains the byte of data or control information that is to be sent to the I/O attachment.

Timing of CP/Channel Functions



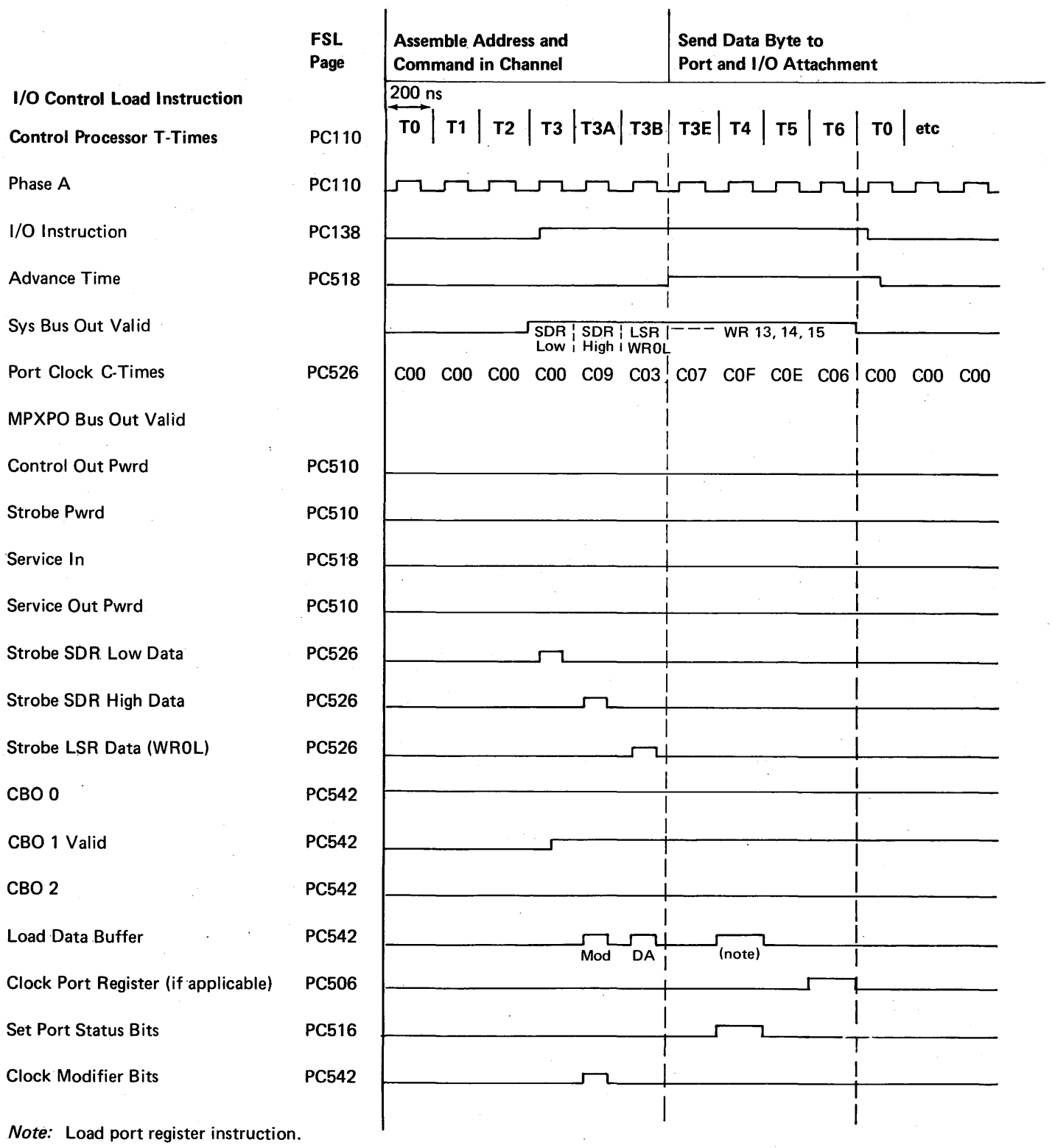
[1] See *Channel Exerciser Loop Program* in the *Channel* section of this manual for a program that can be used with this command.

I/O Load Instruction



Notes:
1. First strobe to be used for normal load operations.
2. Fourth strobe to be used for normal load operations.

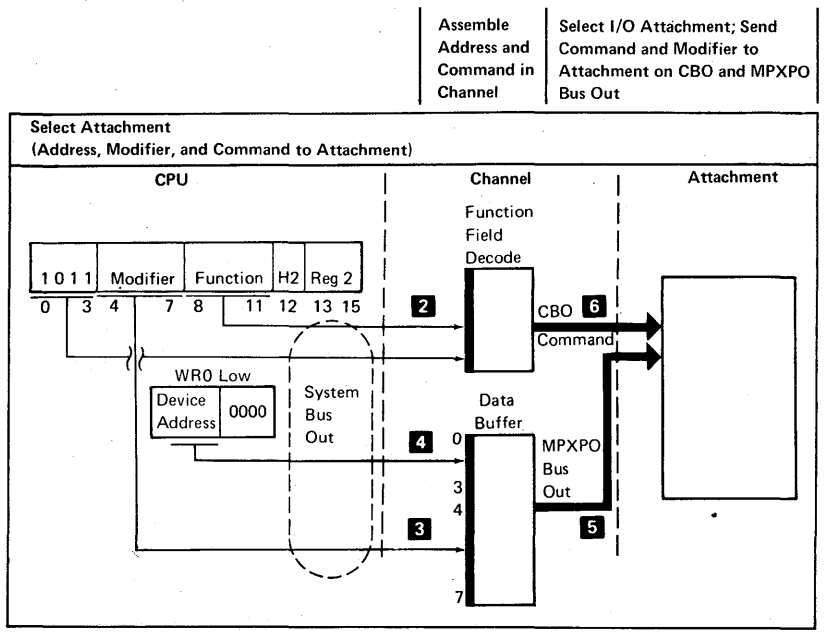
I/O Control Load Instruction

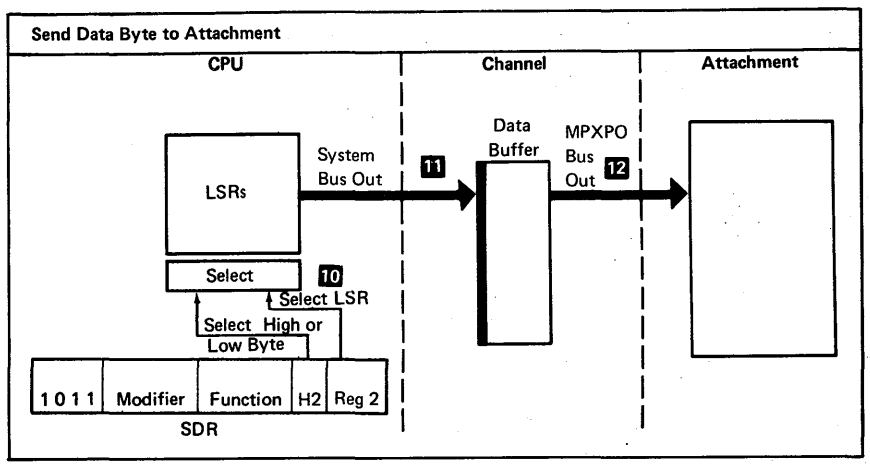


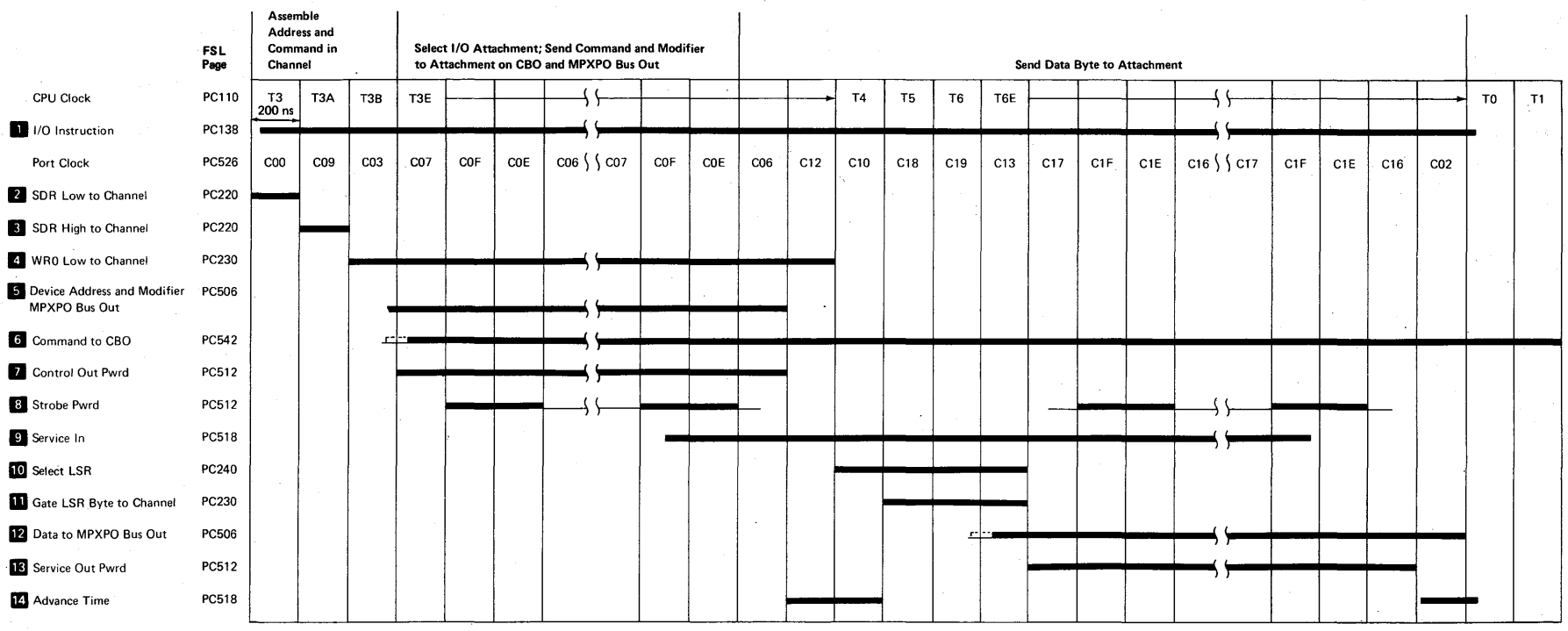
Note: Load port register instruction.

5

I/O Load (Big Picture)

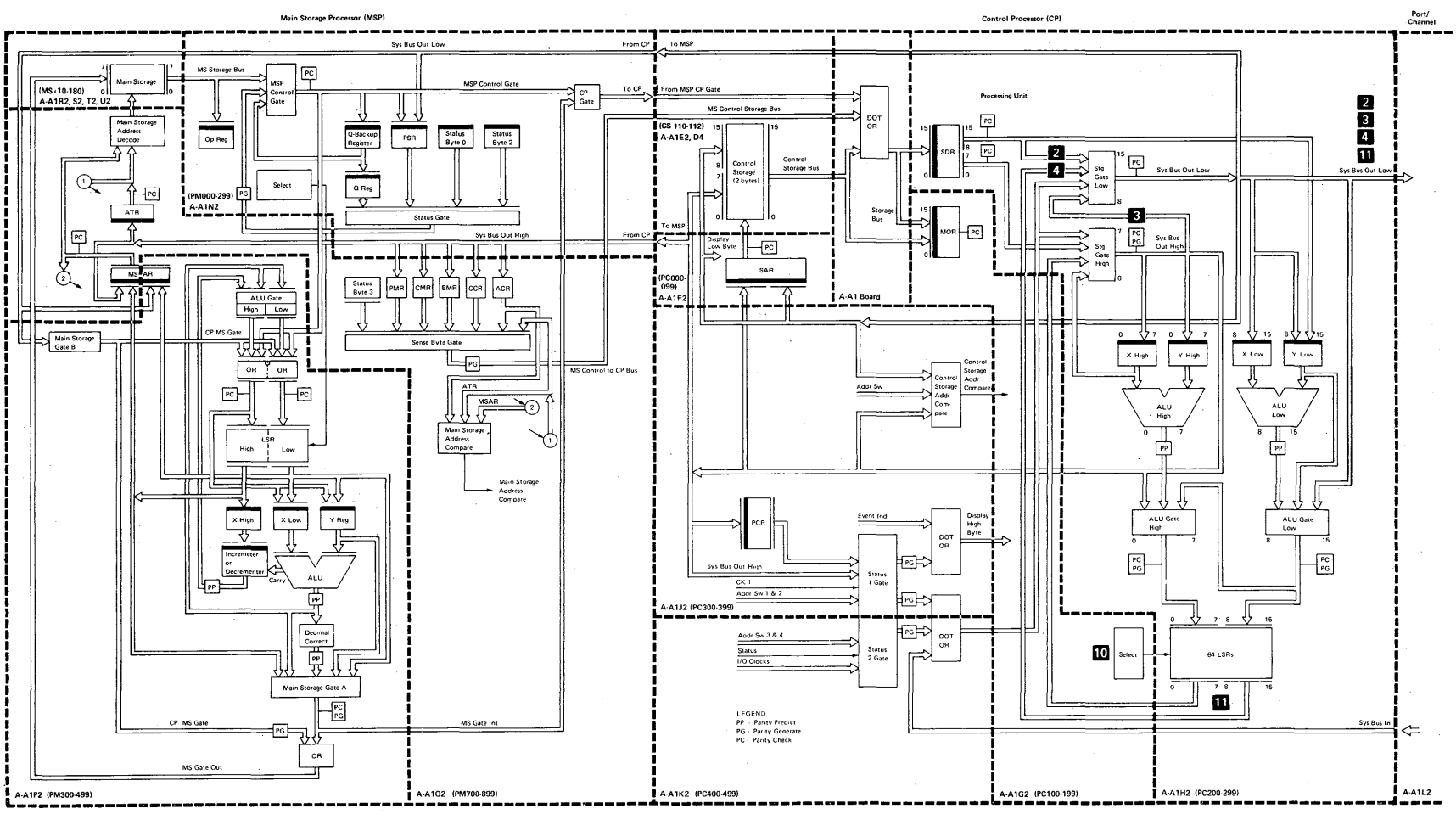




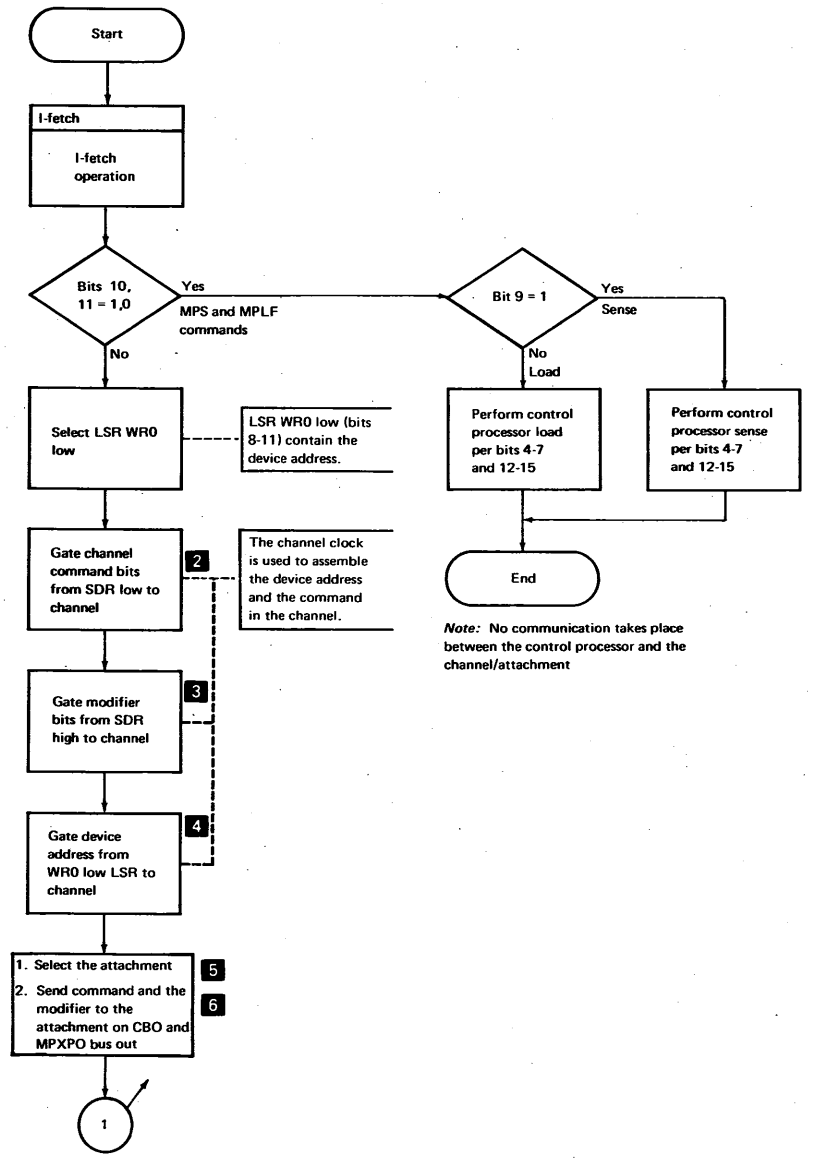


The first 'strobe pwrd' pulse after the rise of the 'control out pwrd' line signals the I/O attachment that the device address and the command information on the 'command bus out' and 'MPXPO bus out' lines are valid. The rise of the 'service in' line signals the port that the I/O attachment has taken the information from the 'command bus out' and 'MPXPO bus out' lines and is ready to receive data.

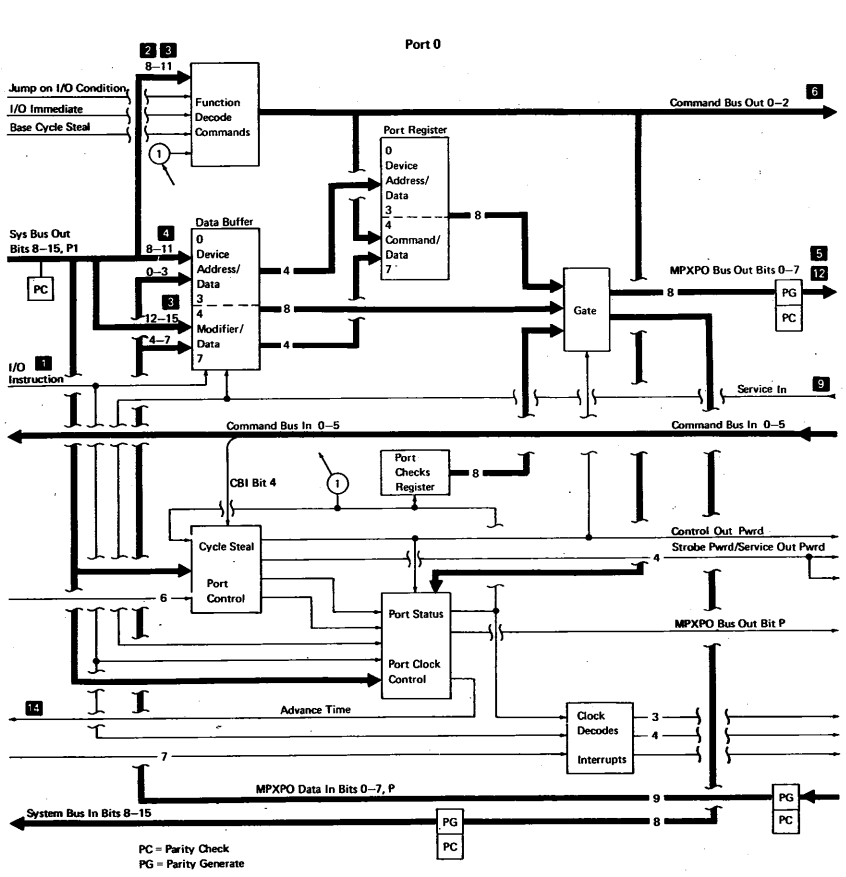
The first 'strobe pwrd' pulse after the rise of the 'service out pwrd' line signals the I/O attachment that the data byte on the 'MPXPO bus out' lines is valid. The fall of the 'service in' line signals the port that the I/O attachment has taken the data byte from the 'MPXPO bus out' lines.



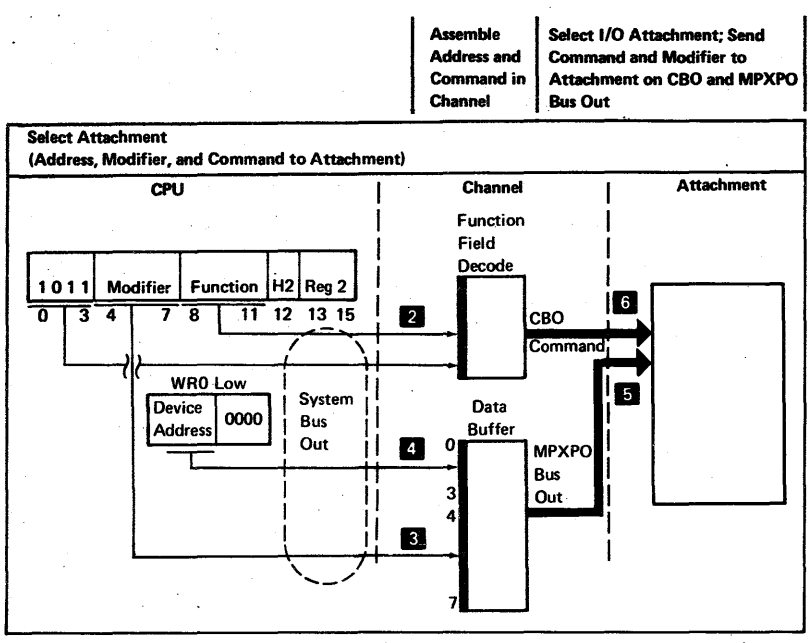
*Data flow bus lines may not pass through FRUs as shown

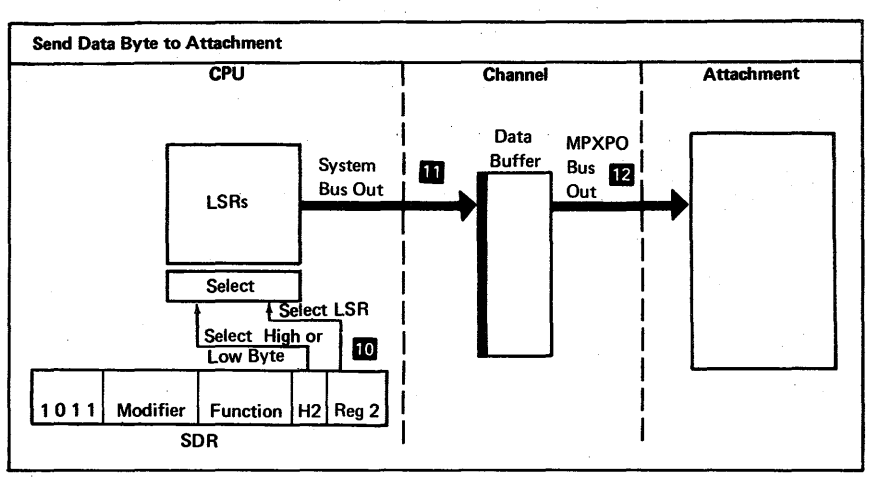


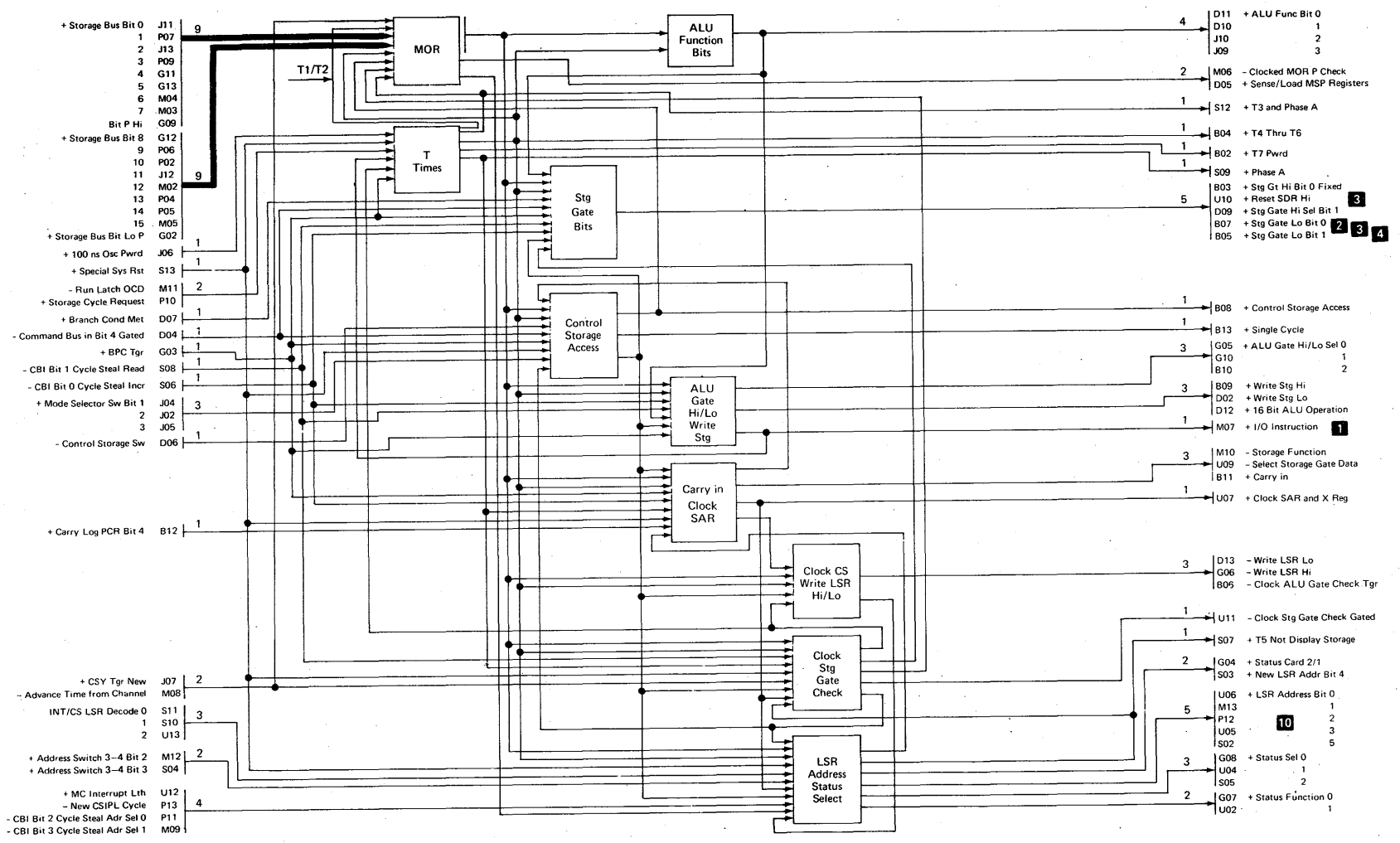
System Bus Out Function Bits 8 9 10 11	Command Bus Out 0 1 2	Command	Mnemonic
0 0 0 0	1 0 0	I/O Load	IOL
0 1 0 0	1 0 1	I/O Sense	IOS
0 1 0 1	0 0 1	Sense Interrupt Level Status Byte	SILSB
1 0 0 0	1 1 0	I/O Control Load	IOCL
1 1 0 0	1 1 1	I/O Control Sense	IOCS
0 0 1 1	0 1 1	Jump on I/O Condition	JIO
	0 1 0	Base Cycle Steal	



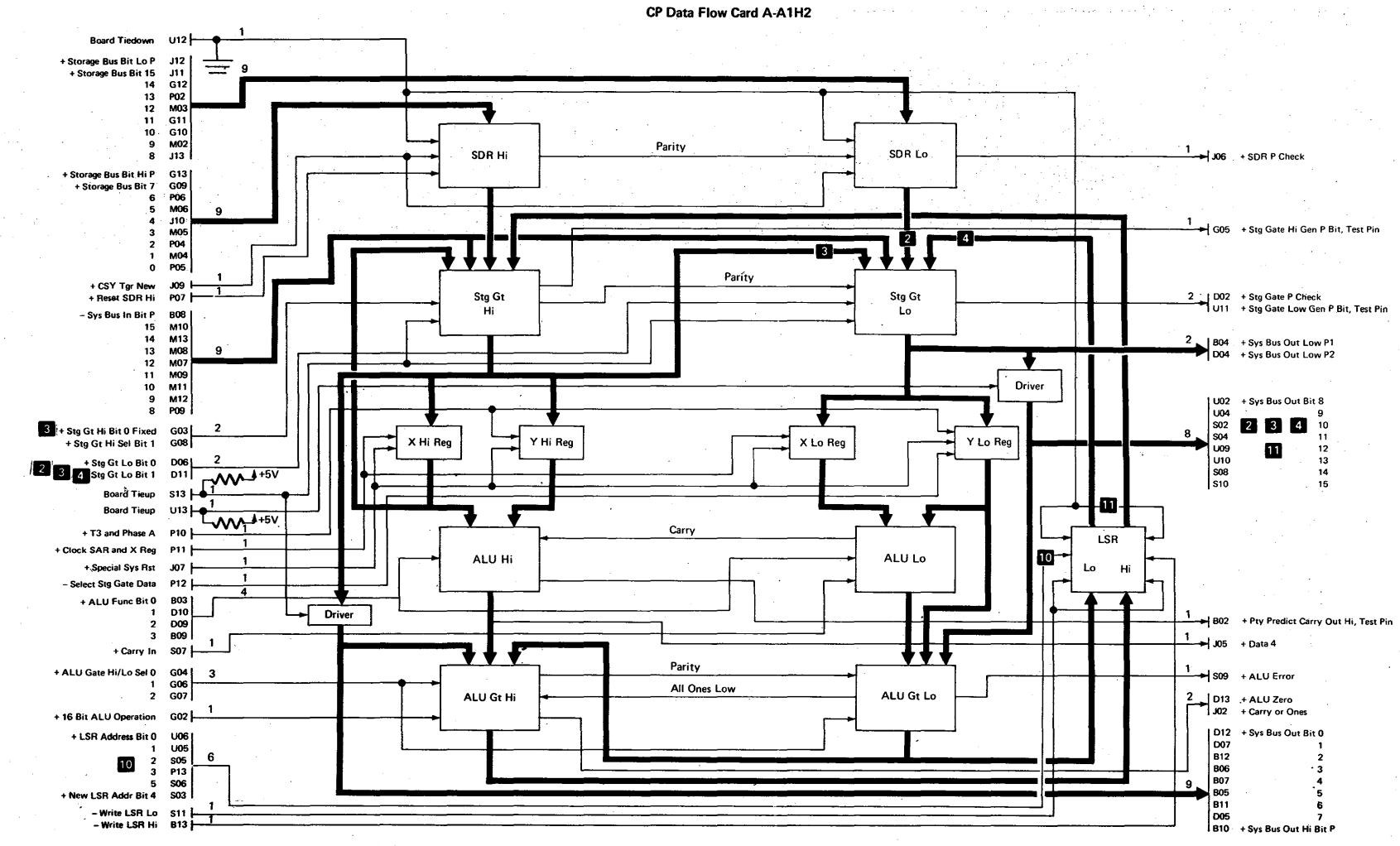
I/O Load (Detail)

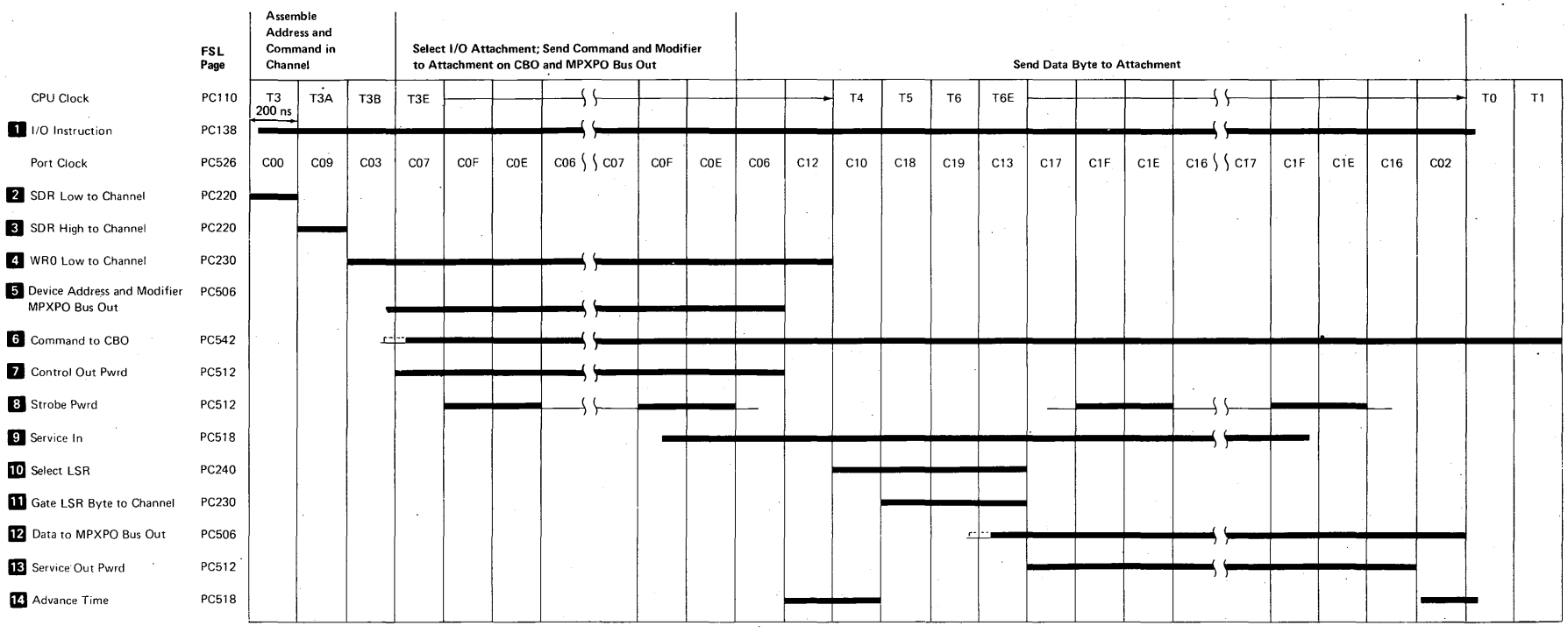






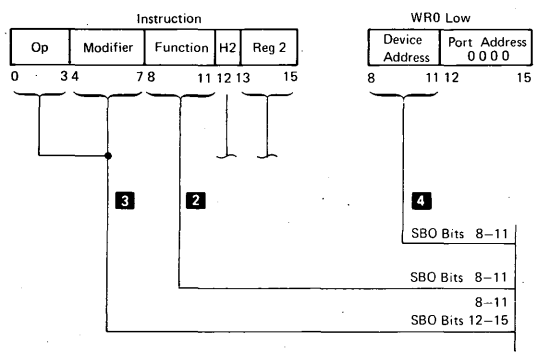
CP Data Flow Card A-A1H2

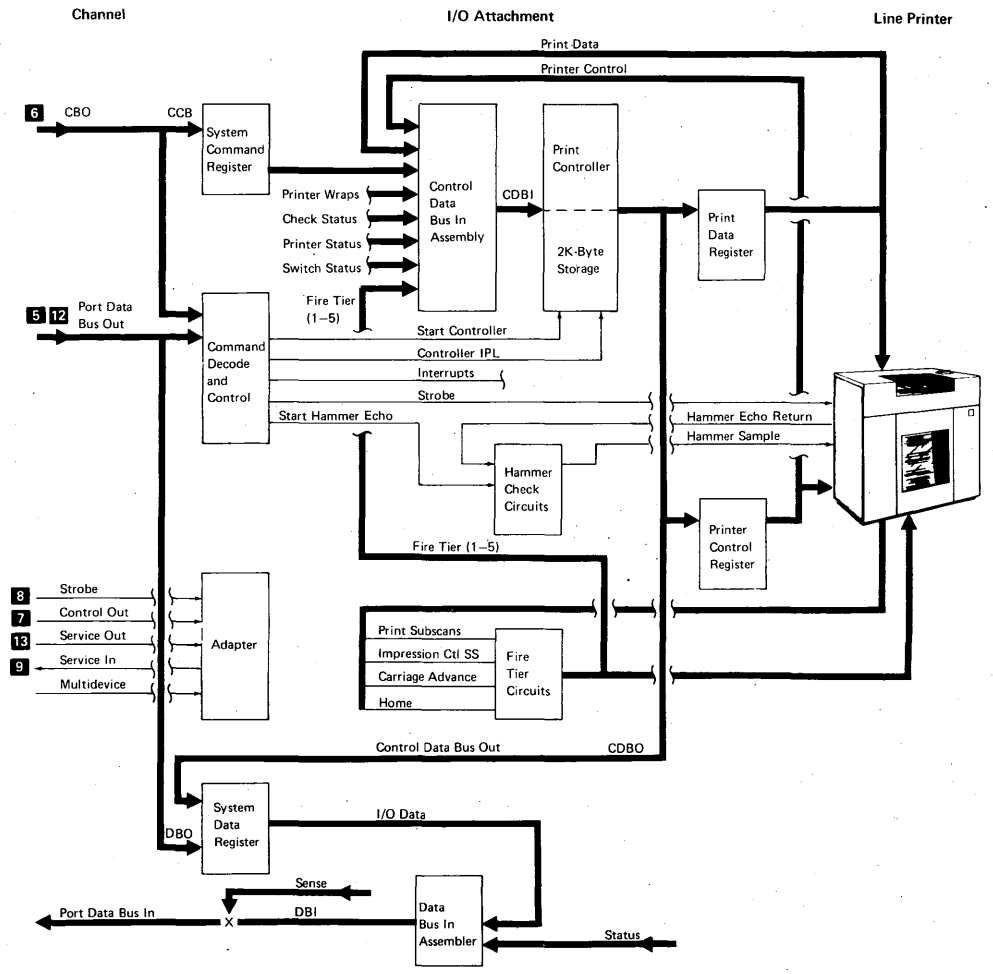


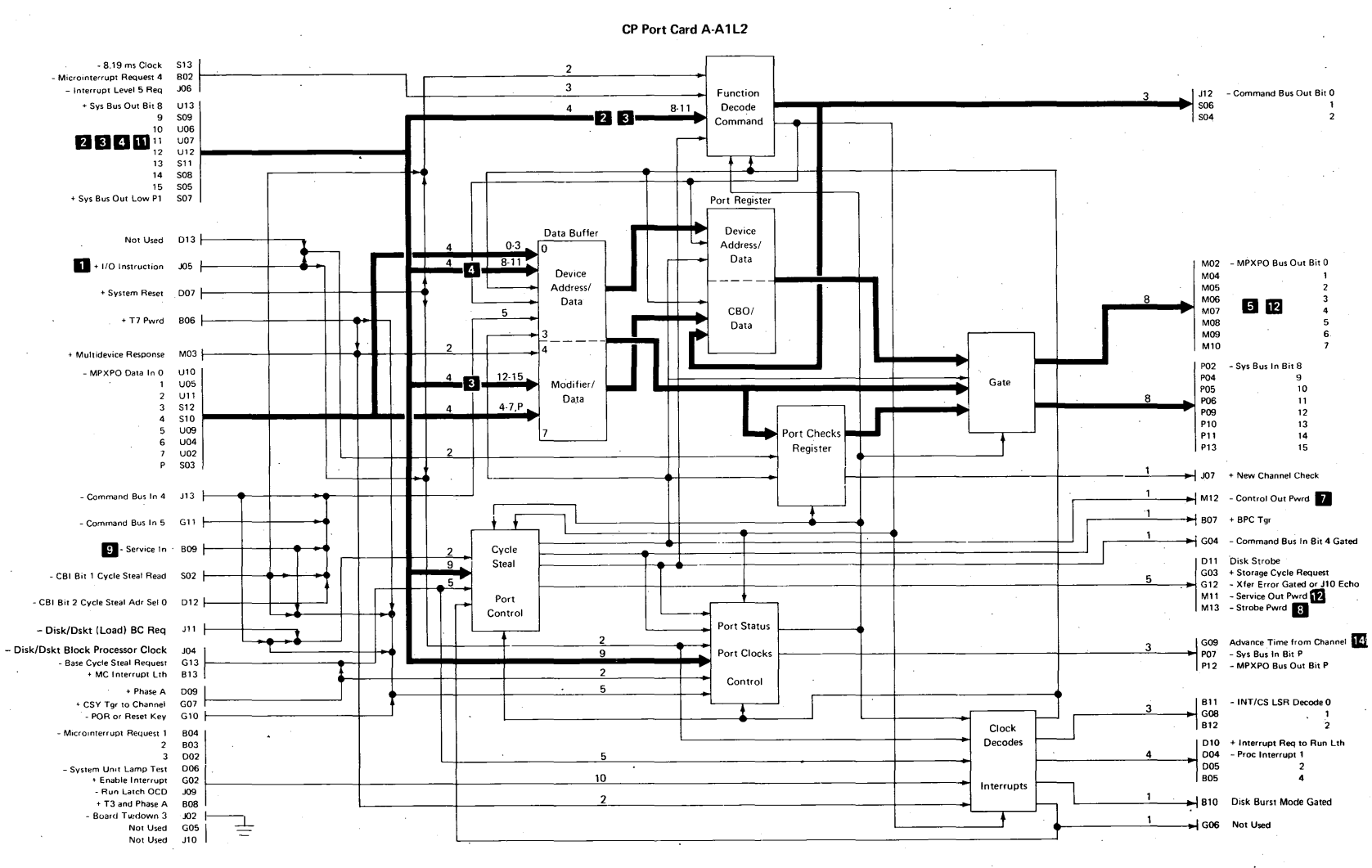


System Bus Out Function Bits 8 9 10 11	Command Bus Out 0 1 2	Command	Mnemonic
0 0 0 0	1 0 0	I/O Load	IOL
0 1 0 0	1 0 1	I/O Sense	IOS
0 1 0 1	0 0 1	Sense Interrupt Level Status Byte	SILSB
1 0 0 0	1 1 0	I/O Control Load	IOCL
1 1 0 0	1 1 1	I/O Control Sense	IOCS
0 0 1 1	0 1 1	Jump on I/O Condition	JIO
	0 1 0	Base Cycle Steal	

Storage Gate High		
Bit 0	**Bit 1**	**Register Gated Thru**
0	0	LSR High
0	1	SDR High
1	0	SBI Bits 8–15
1	1	X Reg High Bits 0–3 SDR Bits 4–7 Stg Gate High Bit P
Storage Gate Low		
Bit 0	**Bit 1**	**Register Gated Thru**
0	0	LSR Low
0	1	SDR Low
1	0	SBI Bits 8–15
1	1	Output Stg Gate High



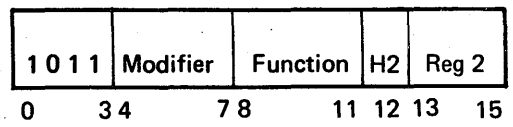




CP Port Card A-A1L2

5

I/O Sense or I/O Control Sense (IOS, IOCS)



This part of the I/O immediate instruction moves 1 byte of data or status type information from the I/O attachment to a local storage register.

Modifier (Bits 4-7): The modifier bits are specified by the device and are sent to the I/O attachment with the command. These bits specify which data byte is to be sent.

Function (Bits 8-11): The function bits are sent to the port where they are decoded as either the sense or control sense command. This command is then sent to the I/O attachment on the 'command bus out' lines.

Bits 8-11 = 0100 for IOS

Bits 8-11 = 1100 for IOCS

H2 (Bit 12): Selects the low- or high-order byte of the selected local storage register for the current interrupt level:

H2 = 0: Low-order byte

H2 = 1: High-order byte

Register 2 (Bits 13-15): Selects one of the eight work registers in the local storage register stack for the current interrupt level. The byte of data being sent from the I/O attachment is placed in this local storage register.

Timing of CP/Channel Functions

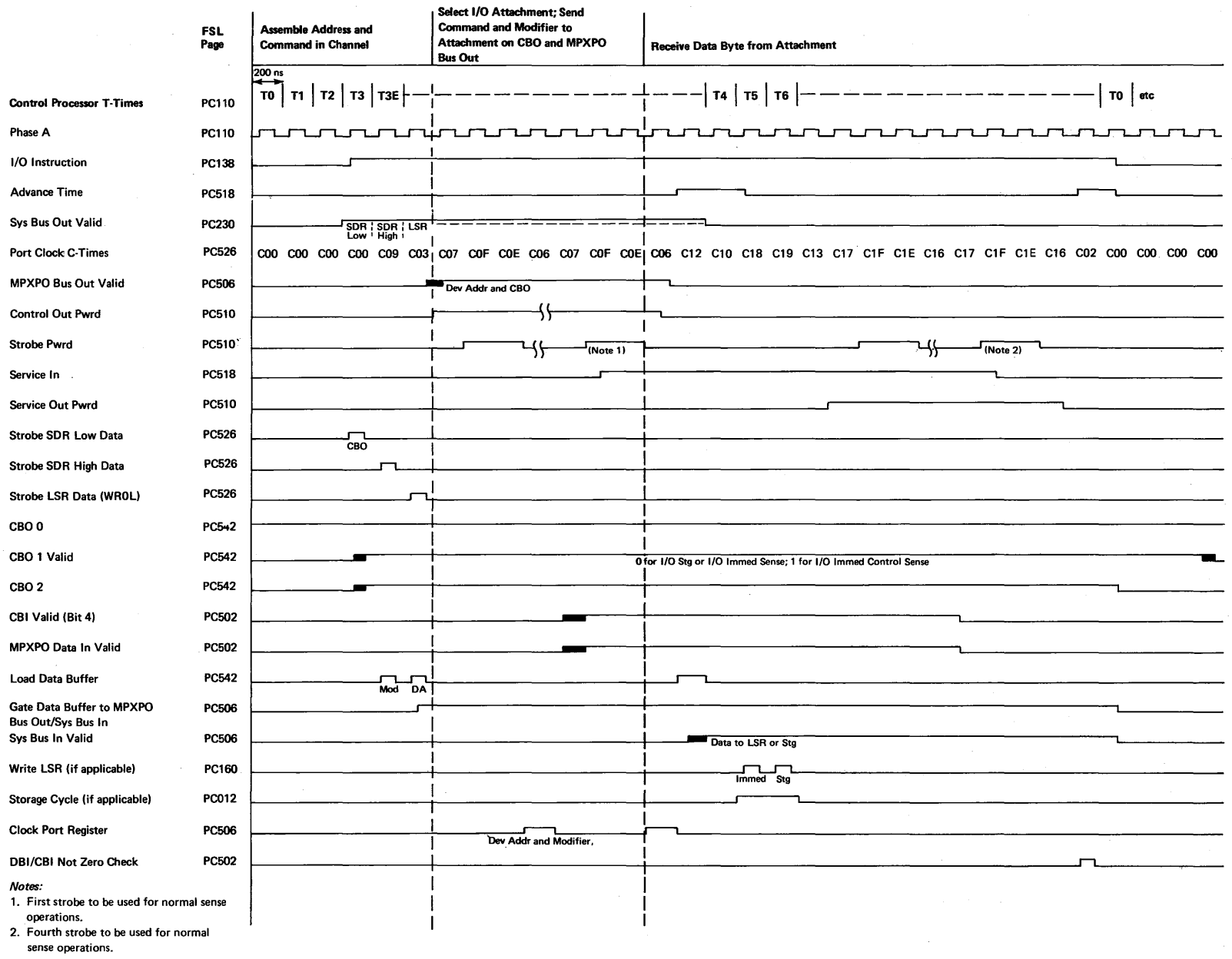
200 ns

Printer IOS[1]

	FSL Page	T0	T1	T2	T3	T3A	T3B	T3E C07	C0F	C0E	C06	C12	T4	T5	T6	C13	C17	C1F	C1E	C16	C02
I/O Instruction	PC138				▬	▬	▬	▬	▬	▬	▬	▬	▬								
Stg Gate Hi/Lo from SDR (instr)	PC230				▬																
Strobe SDR Lo Data (function to SBO)	PC502				▬																
CBO Decode from SBO	PC542				▬																
Stg Gate Lo from Stg Gate Hi	PC230					▬															
Load Data Buffer (modifier bits)	PC526					▬															
Select LSR (WR0 address)	PC230					▬															
Stg Gate Hi/Lo from LSR	PC230						▬														
Strobe LSR Data	PC526						▬														
Data Buffer from SBO (address)	PC502						▬														
Control Out Pwrd (from channel)	PC510		Basic I-Fetch					▬	▬	▬	▬										
Service In (from I/O)	PC502								▬	▬	▬	▬	▬	▬	▬	▬					
Service Out Pwrd (from channel)	PC510															▬	▬	▬	▬		
CBO Bits Active	PC542				▬																
Modifier Bits to Data Buffer	PC502					▬															
Address Bits to Data Buffer	PC502						▬														
Modifier Bits to MPXPO Bus Out	PC506						▬														
Address Bits to MPXPO Bus Out	PC506							▬													
Mod. and Address Bits Sent to I/O									▬	▬											
Advance Time from Channel	PC518												▬	▬							▬
Strobe Pwrd	PC510								▬	▬								▬	▬		
Data Gated to Data Buffer													▬								
Data Gated to MPXPO Bus Out								▬	▬	▬	▬										

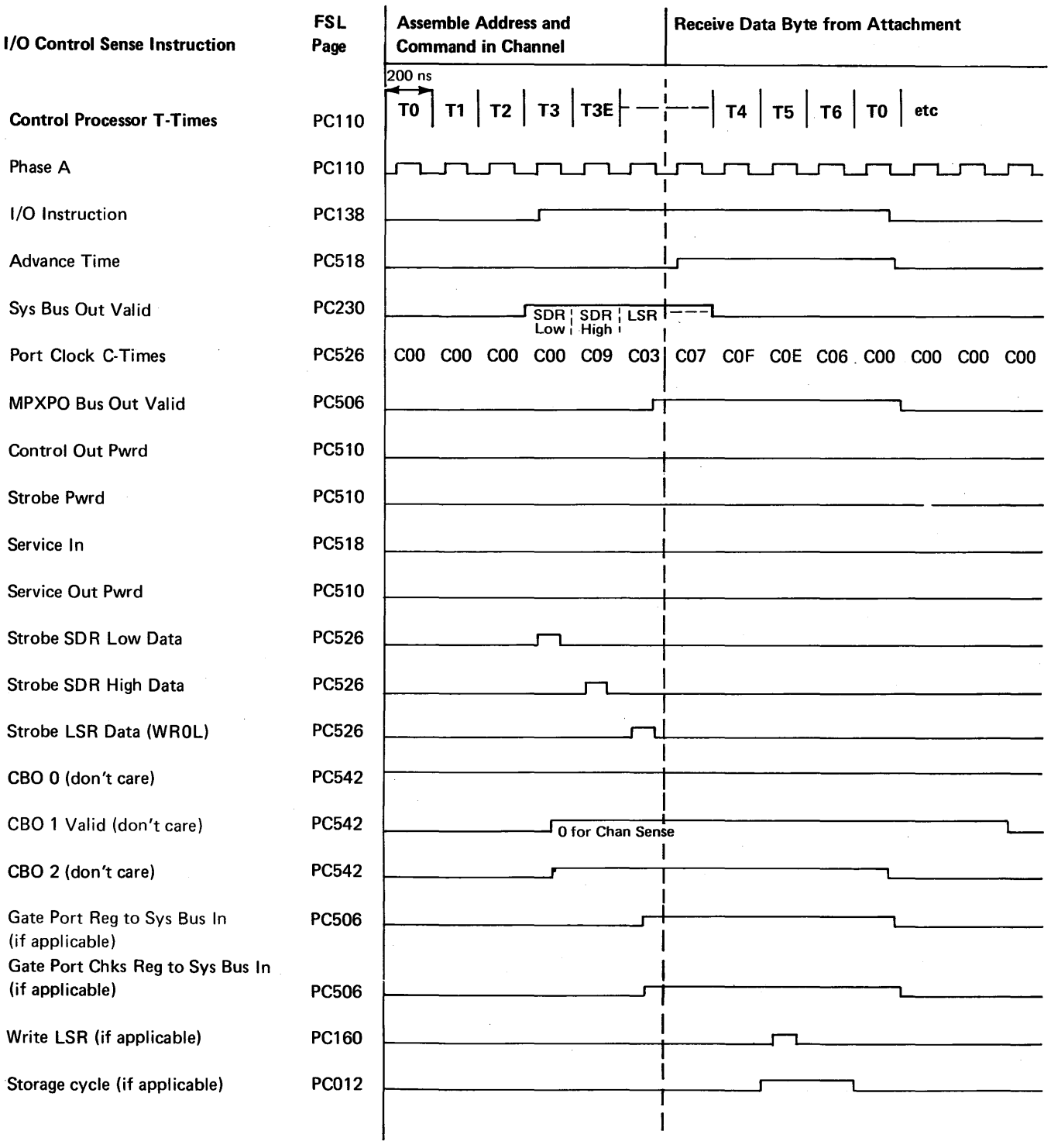
[1] See *Channel Exerciser Loop Program* in the *Channel* section of this manual for a program that can be used with this command.

I/O Sense Instruction



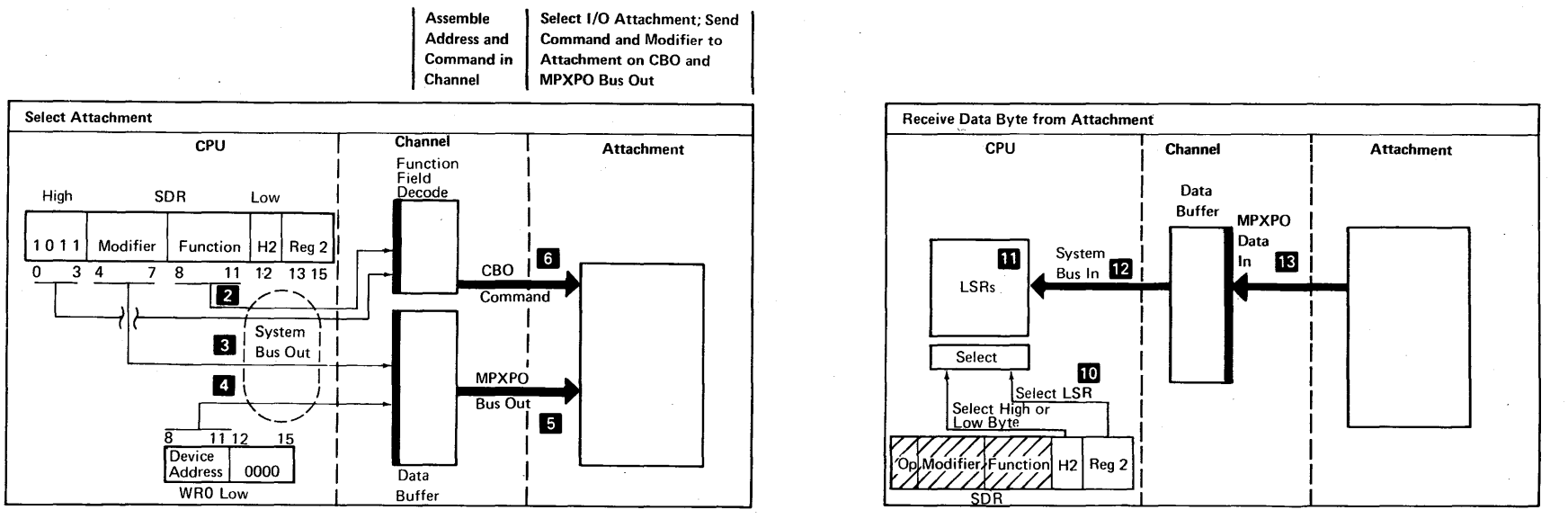
Notes:
1. First strobe to be used for normal sense operations.
2. Fourth strobe to be used for normal sense operations.

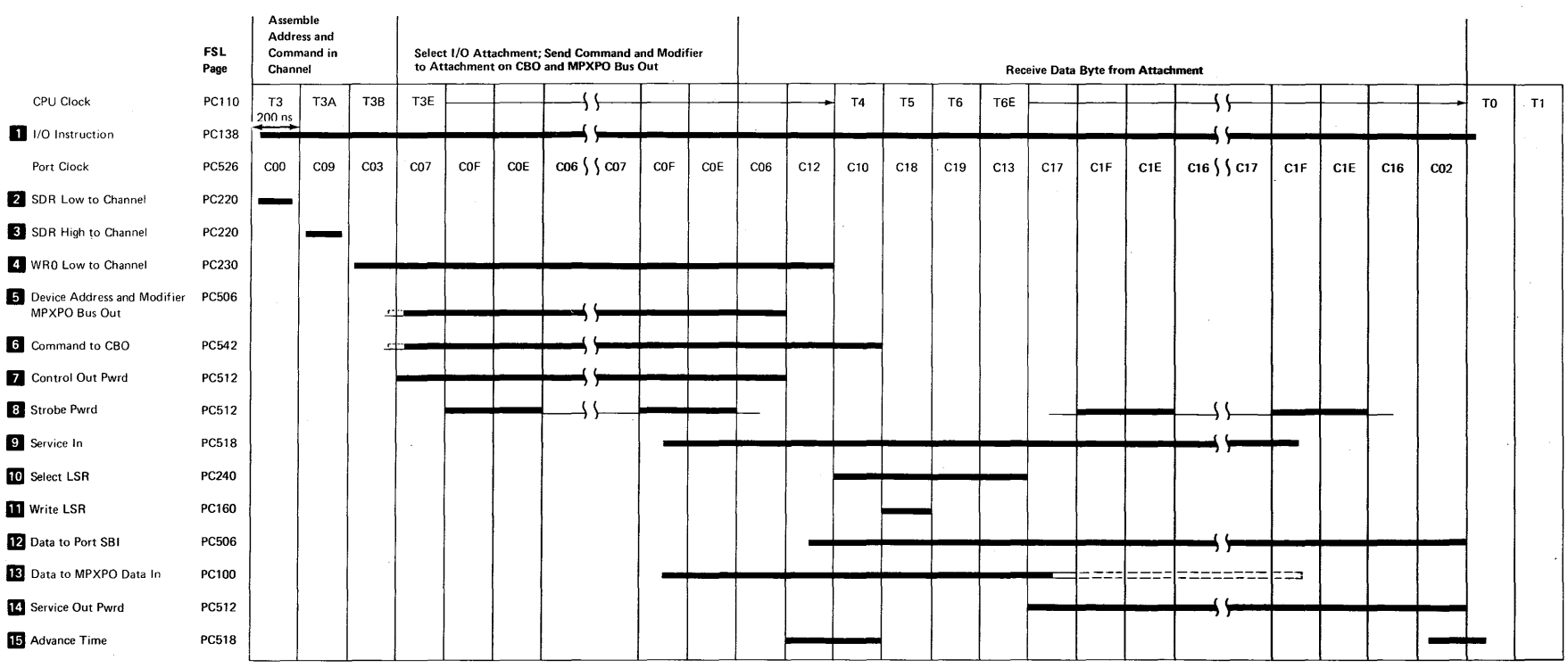
I/O Control Sense Instruction



5

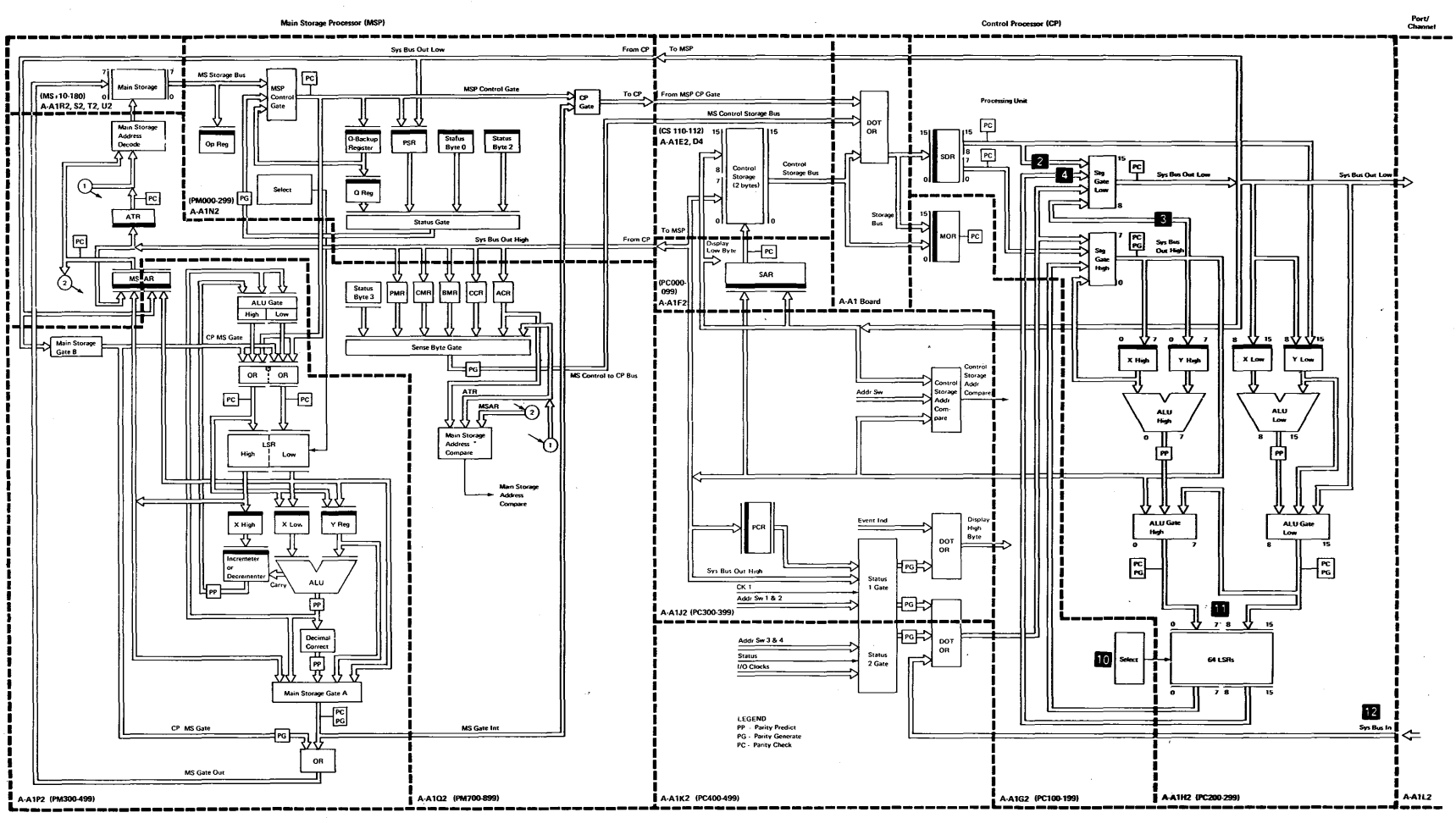
I/O Sense (Big Picture)



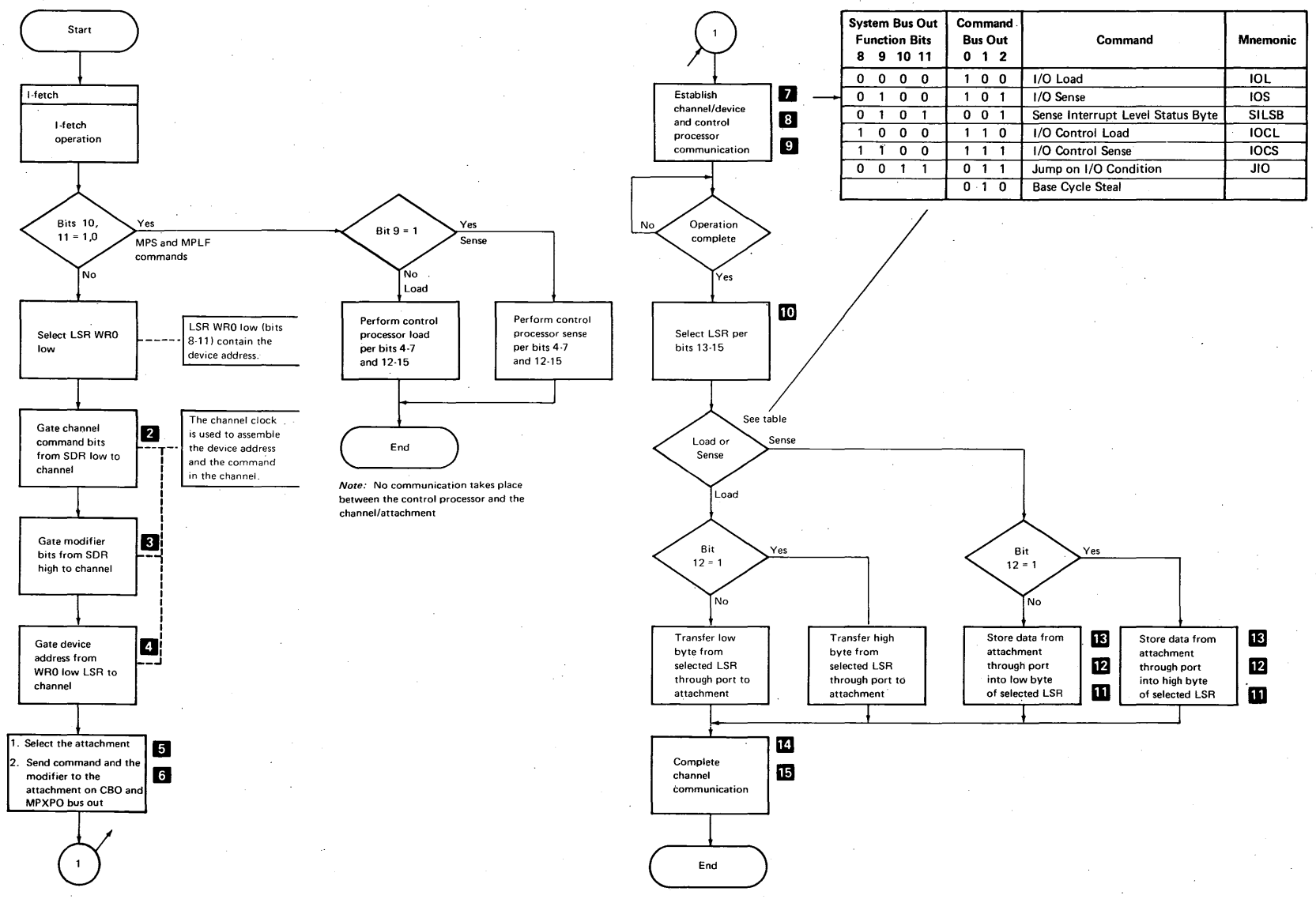


The first 'strobe pwrd' pulse after the rise of the 'control out pwrd' line signals the I/O attachment that the device address and the command information on the 'command bus out' and the 'MPXPO bus out' lines are valid.

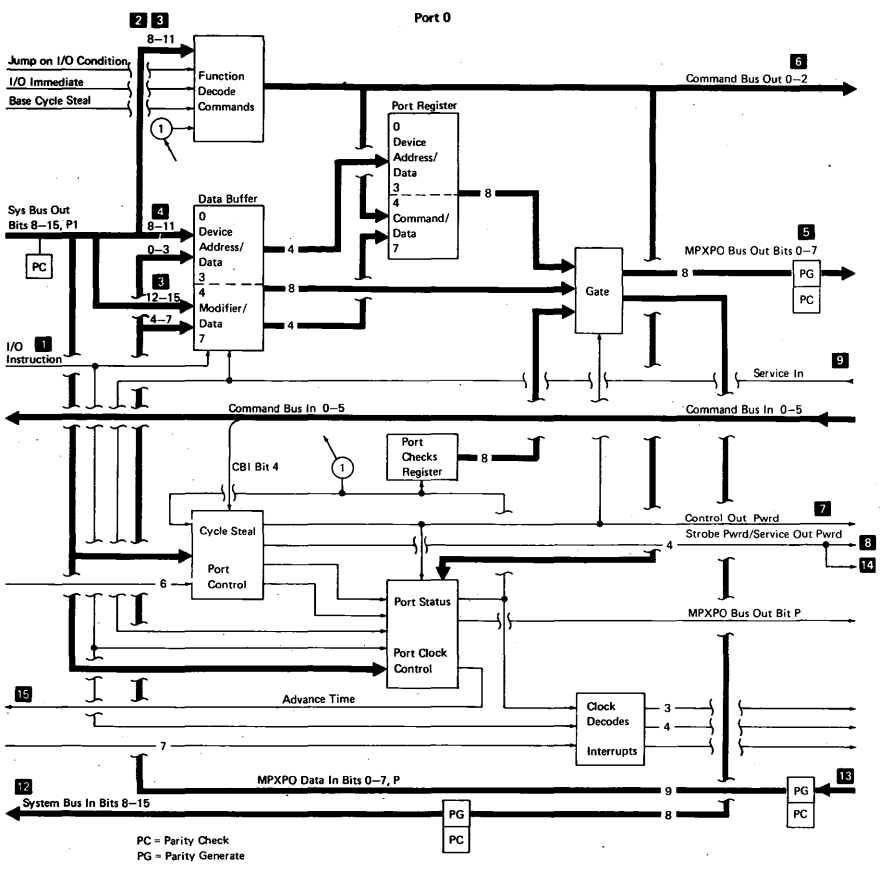
The rise of the 'service in' line signals the port that the I/O attachment has taken the information from the 'command bus out' and 'MPXPO bus out' lines. The rise of the 'service in' line also signals the port that the data byte on the 'MPXPO data in' lines is valid. The rise of the 'service out pwrd' line signals the I/O attachment that the channel has taken the byte from the 'MPXPO data in' lines.

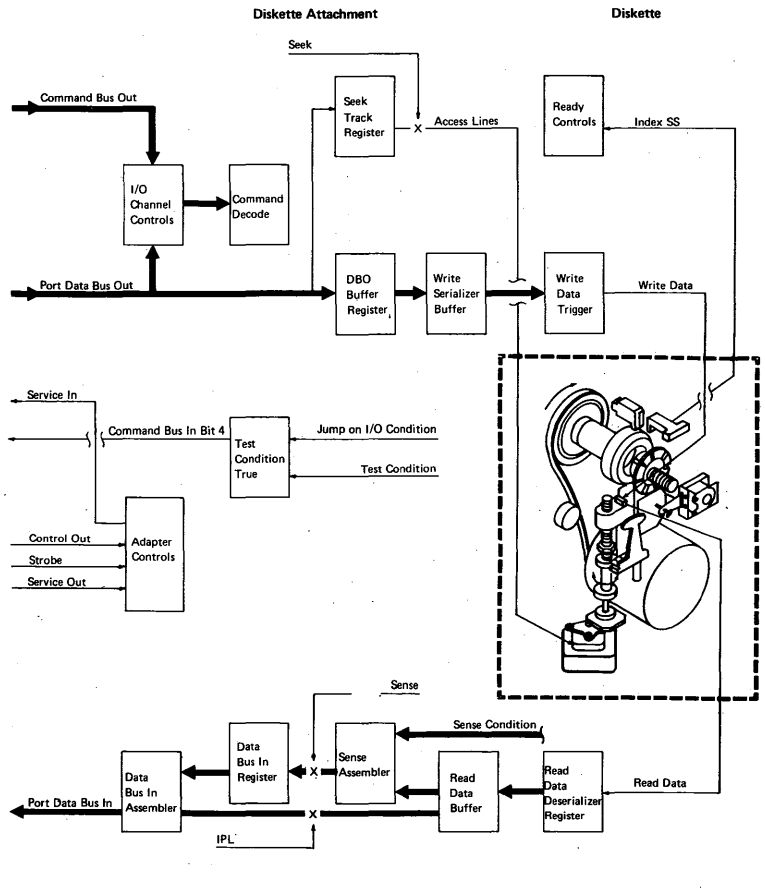


*Data flow bus lines may not pass through FRUs as shown



System Bus Out Function Bits 8 9 10 11	Command Bus Out 0 1 2	Command	Mnemonic
0 0 0 0	1 0 0	I/O Load	IOL
0 1 0 0	1 0 1	I/O Sense	IOS
0 1 0 1	0 0 1	Sense Interrupt Level Status Byte	SILSB
1 0 0 0	1 1 0	I/O Control Load	IOCL
1 1 0 0	1 1 1	I/O Control Sense	IOCS
0 0 1 1	0 1 1	Jump on I/O Condition	JIO
	0 1 0	Base Cycle Steal	

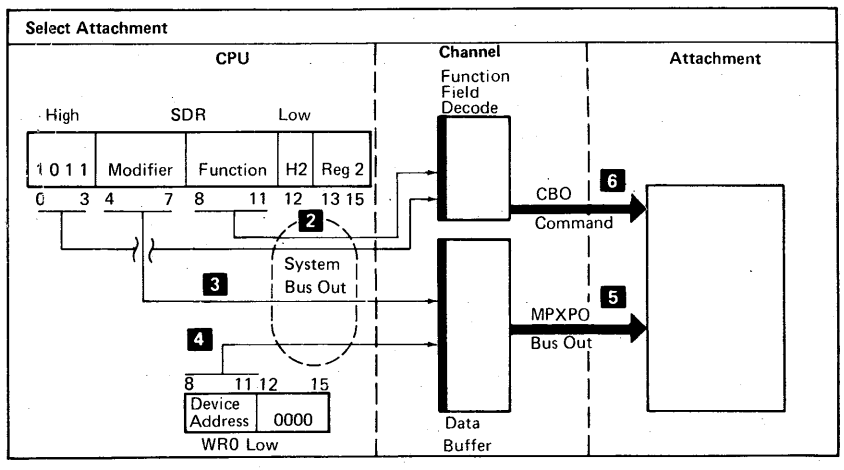


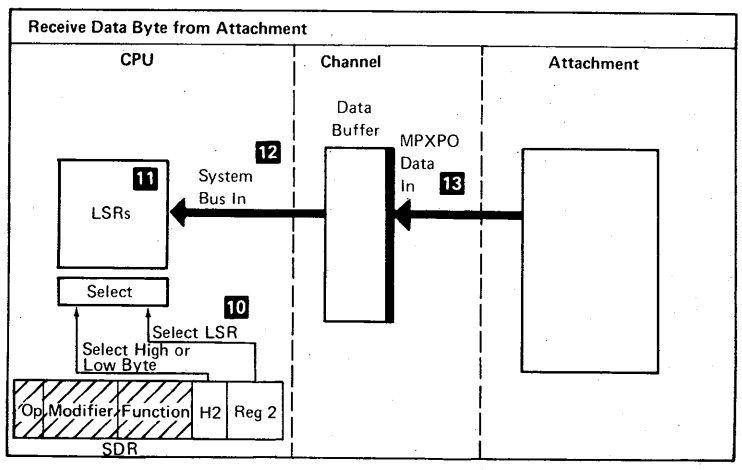


5

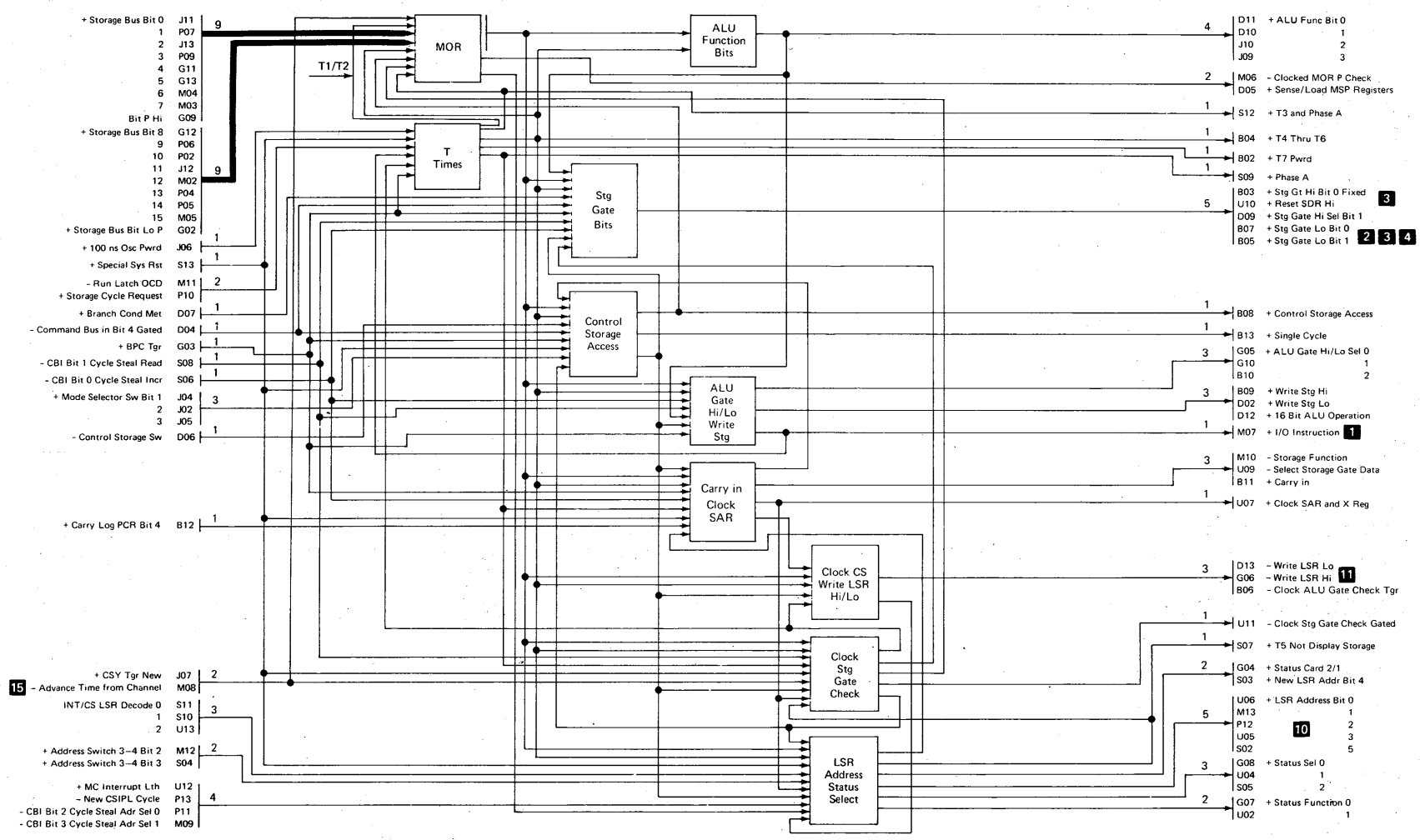
I/O Sense (Detail)

Assemble Address and Command in Channel	Select I/O Attachment; Send Command and Modifier to Attachment on CBO and MPXPO Bus Out

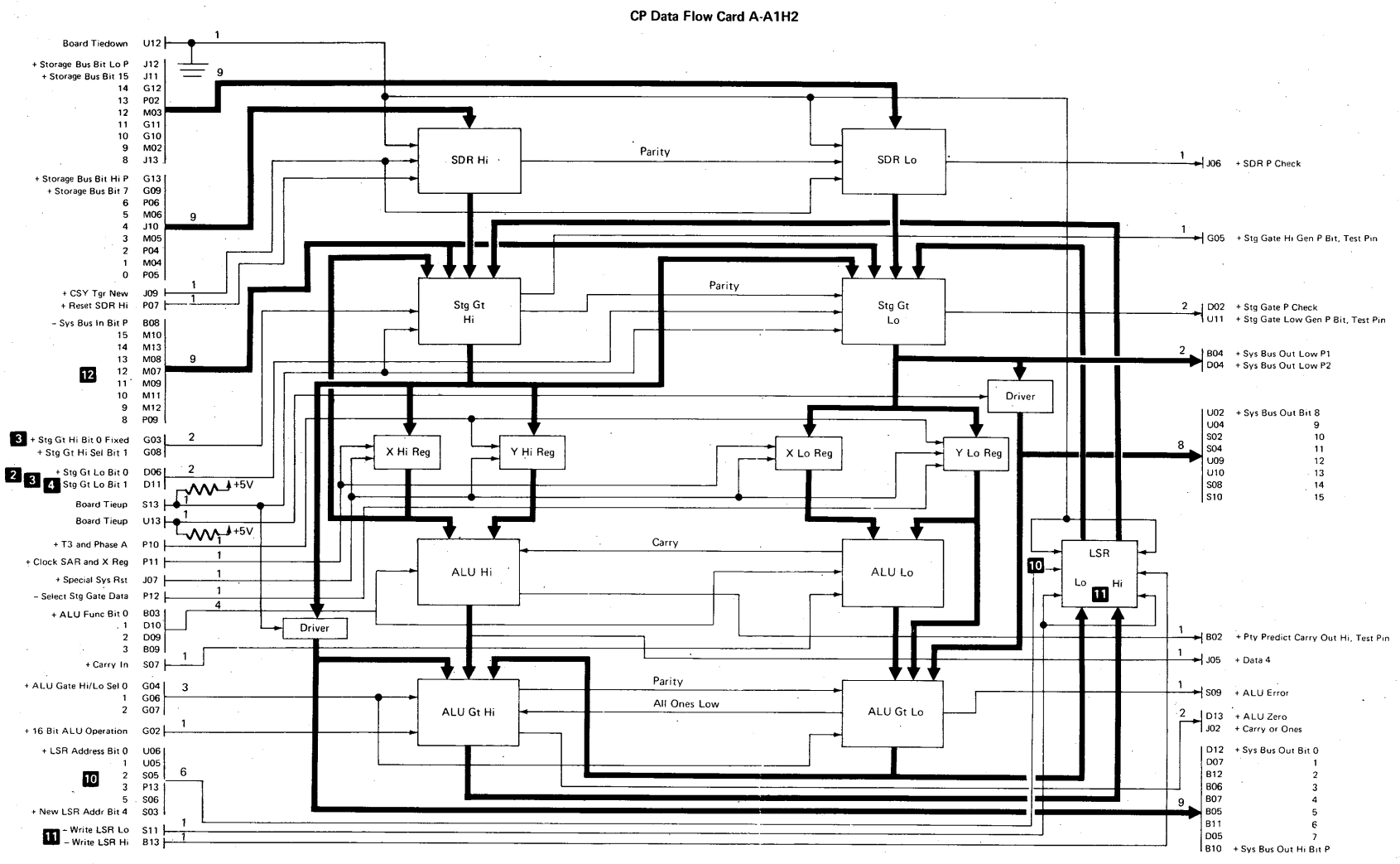


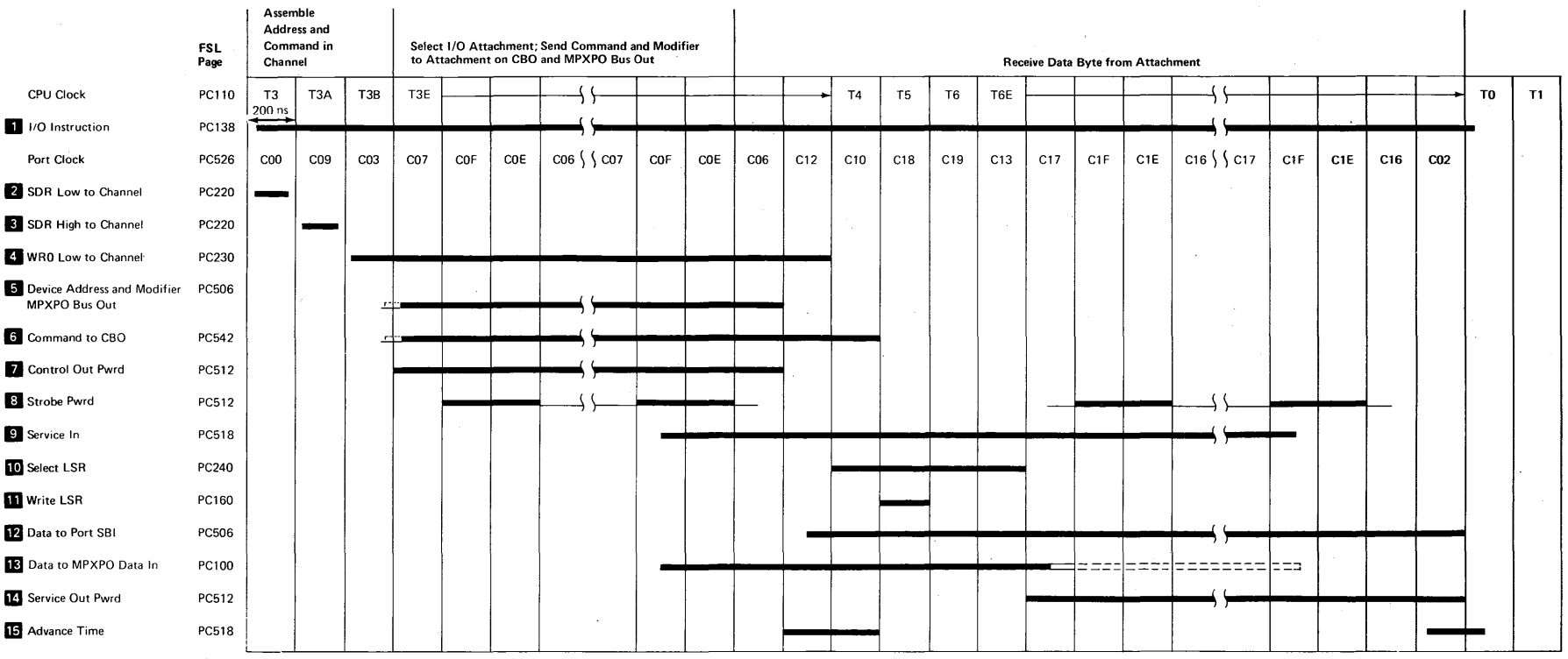


CP System Control Card A-A1G2

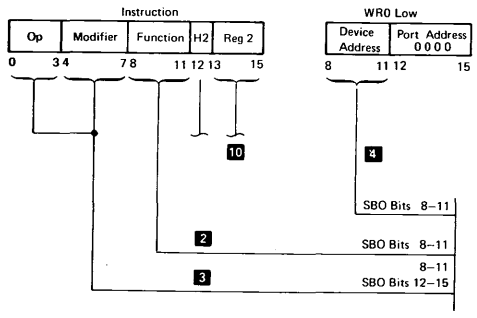


CP Data Flow Card A-A1H2

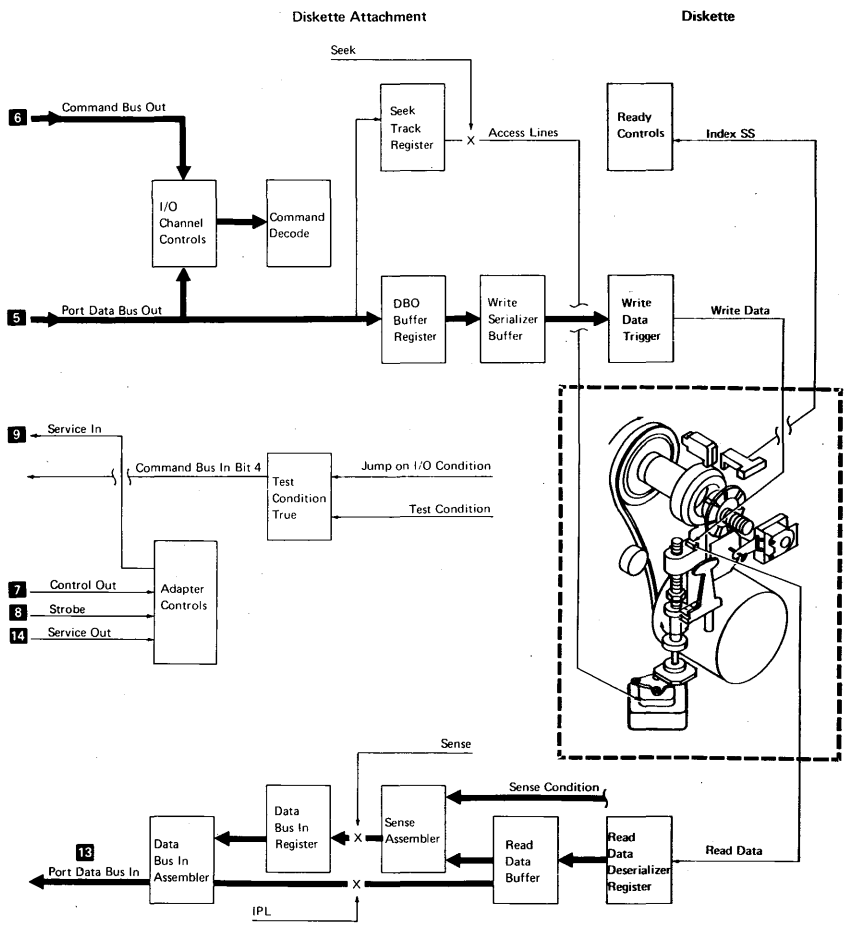


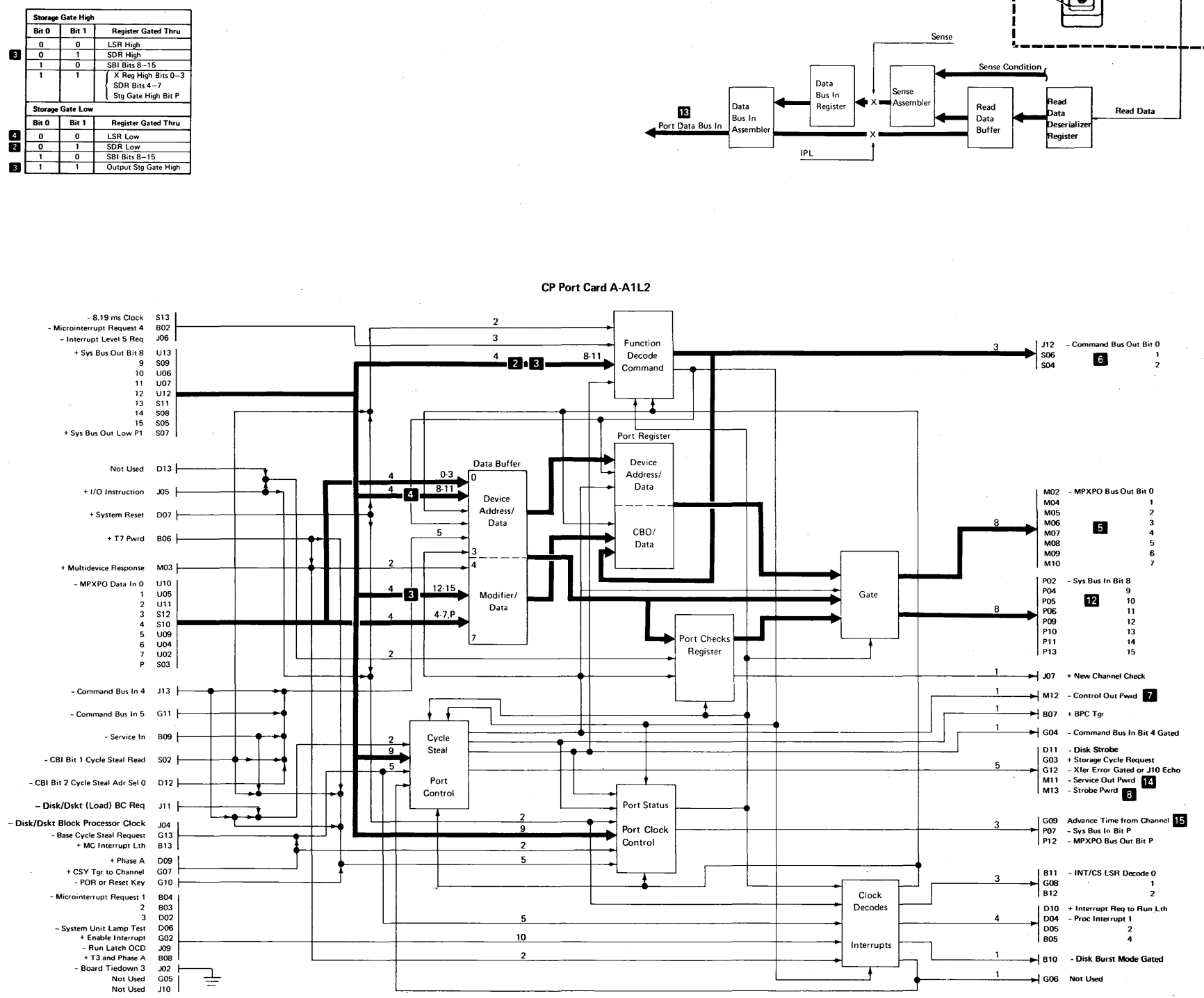


System Bus Out Function Bits 8 9 10 11	Command Bus Out 0 1 2	Command	Mnemonic
0 0 0 0	1 0 0	I/O Load	IOL
0 1 0 0	1 0 1	I/O Sense	IOS
0 1 0 1	0 0 1	Sense Interrupt Level Status Byte	SILSB
1 0 0 0	1 1 0	I/O Control Load	IOCL
1 1 0 0	1 1 1	I/O Control Sense	IOCS
0 0 1 1	0 1 1	Jump on I/O Condition	JIO
	0 1 0	Base Cycle Steal	



Storage Gate High		
Bit 0	Bit 1	Register Gated Thru
0	0	LSR High
0	1	SDR High
1	0	SBI Bits 8–15
1	1	X Reg High Bits 0–3; SDR Bits 4–7; Stg Gate High Bit P
Storage Gate Low		
Bit 0	**Bit 1**	**Register Gated Thru**
0	0	LSR Low
0	1	SDR Low
1	0	SBI Bits 8–15
1	1	Output Stg Gate High





CP Port Card A-A1L2

Sense Interrupt Level Status Byte (SILSB)

1011	Modifier	Function	H2	Reg 2
0 3	4 7	8 11	12	13 15

This function of the I/O immediate instruction moves 1 byte of status information from the I/O attachment to the selected local storage register. This status byte determines which devices are requesting service on a given interrupt level.

Modifier (Bits 4-7): The modifier bits are specified for each device and are sent to the I/O attachment with the command. These bits specify what is to be done with the data byte.

Function (Bits 8-11): The function bits are sent to the channel where they are decoded along with the operation code as a sense interrupt level status byte command. This command is then sent to the I/O attachment on the 'command bus out' lines.

Bits 8-11 = 0101

H2 (Bit 12): Selects the low- or high-order byte of the selected local storage register for the current interrupt level:

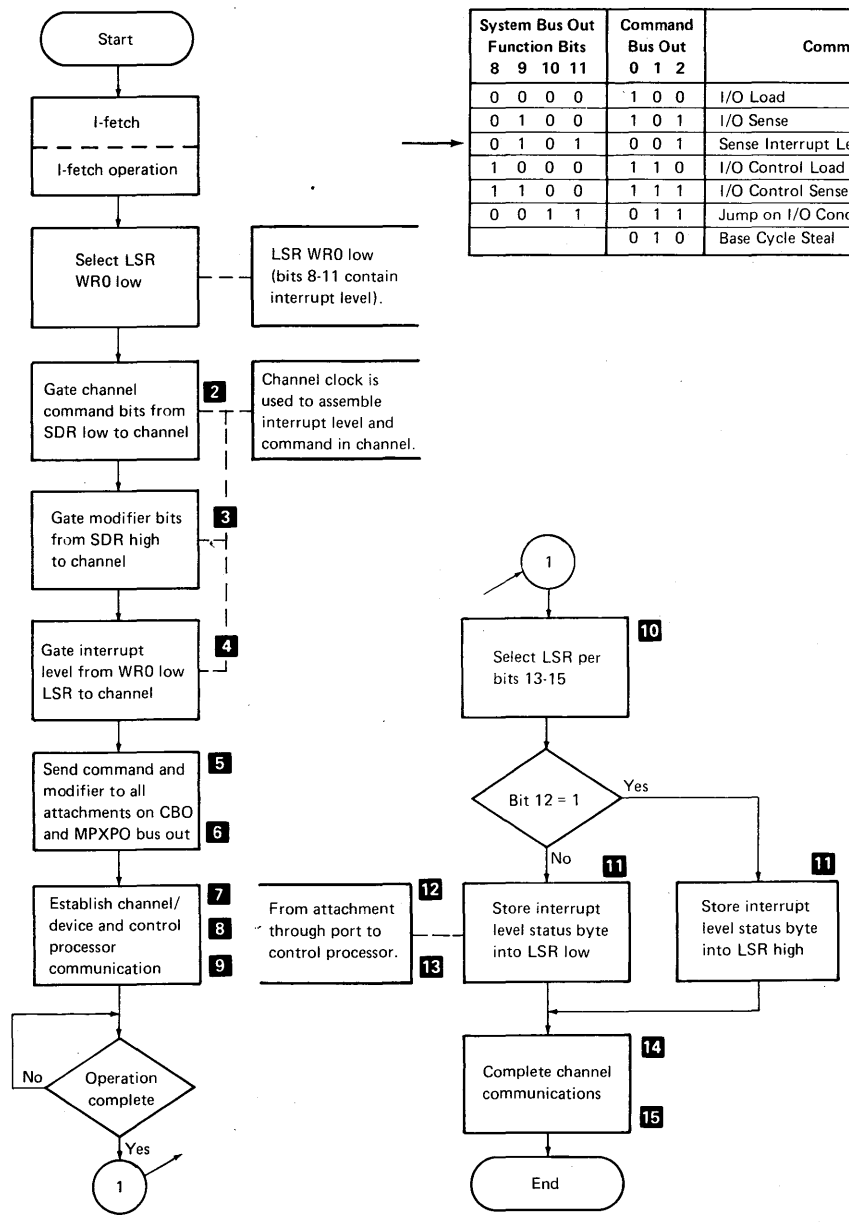
H2 = 0: Low-order byte

H2 = 1: High-order byte

Register 2 (Bits 13-15): Selects one of the eight work registers in the local storage register stack for the current interrupt level. The selected register stores the byte of status information (containing the device that caused the interrupt level) received from the I/O attachment.

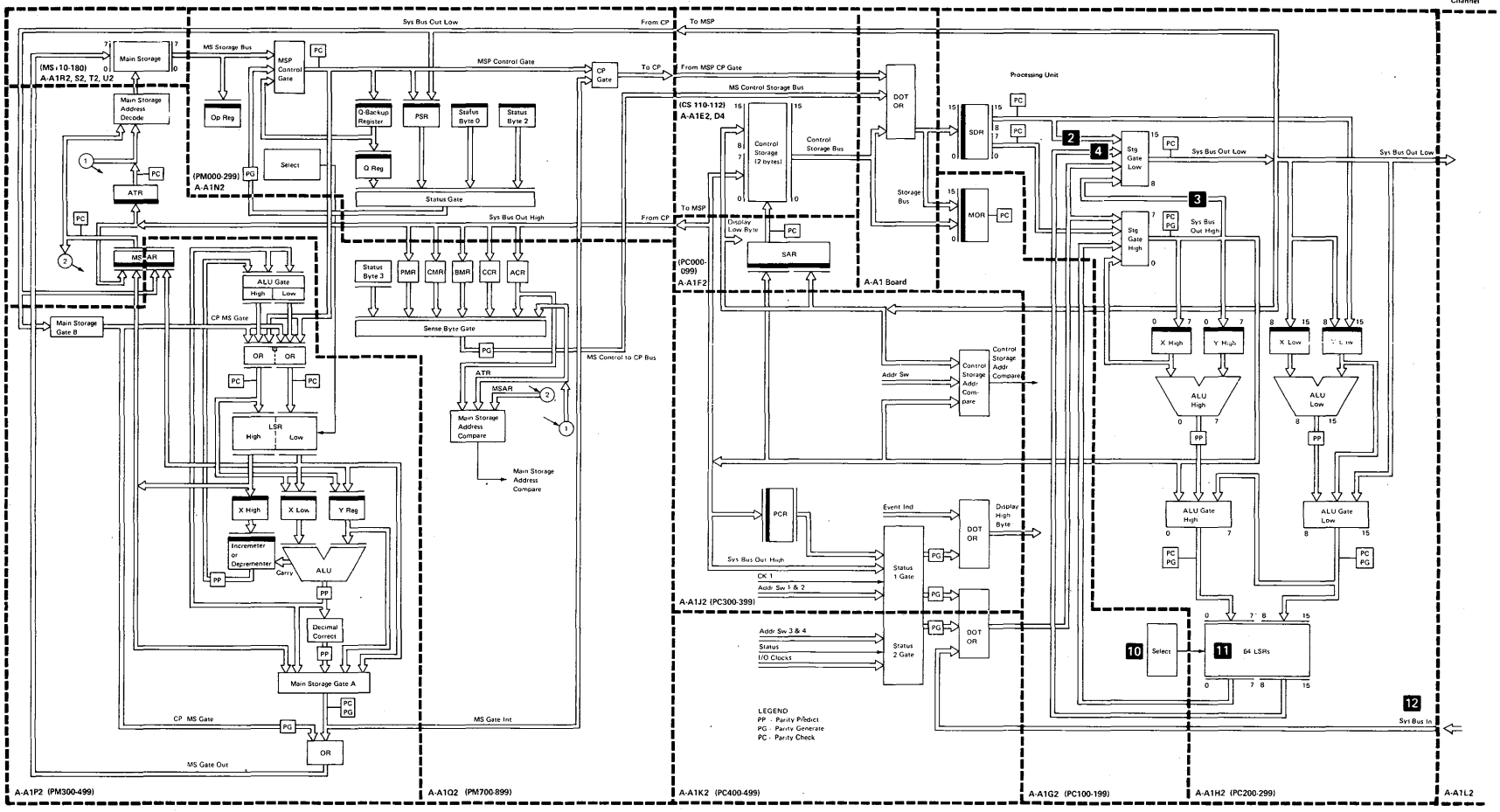
WR0 Low (Bits 8-11): Contains the interrupt level hexadecimal value used by the I/O attachment to select the byte of status information to be stored in the selected local storage register.

I/O Sense Interrupt Level Status Byte

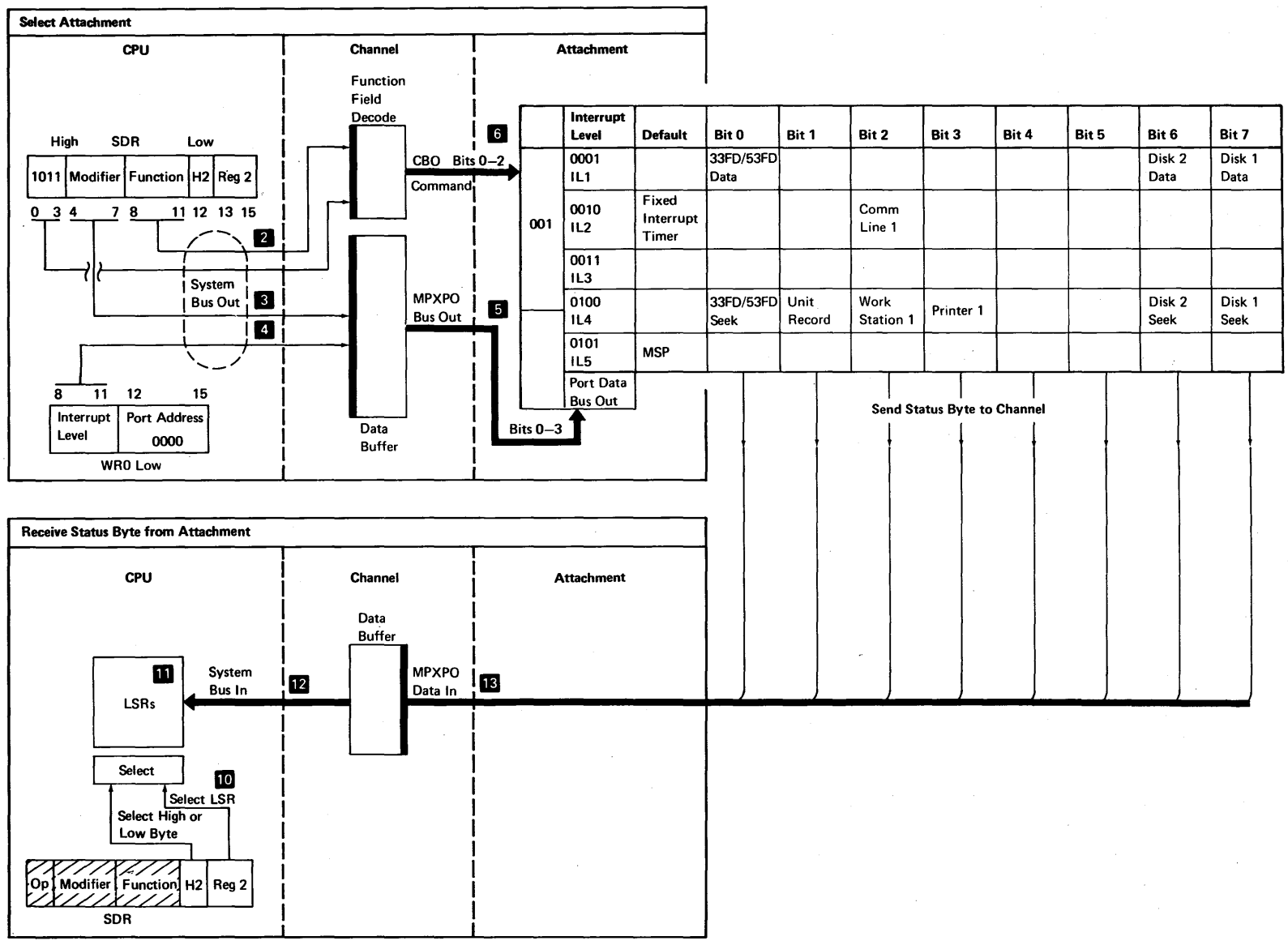


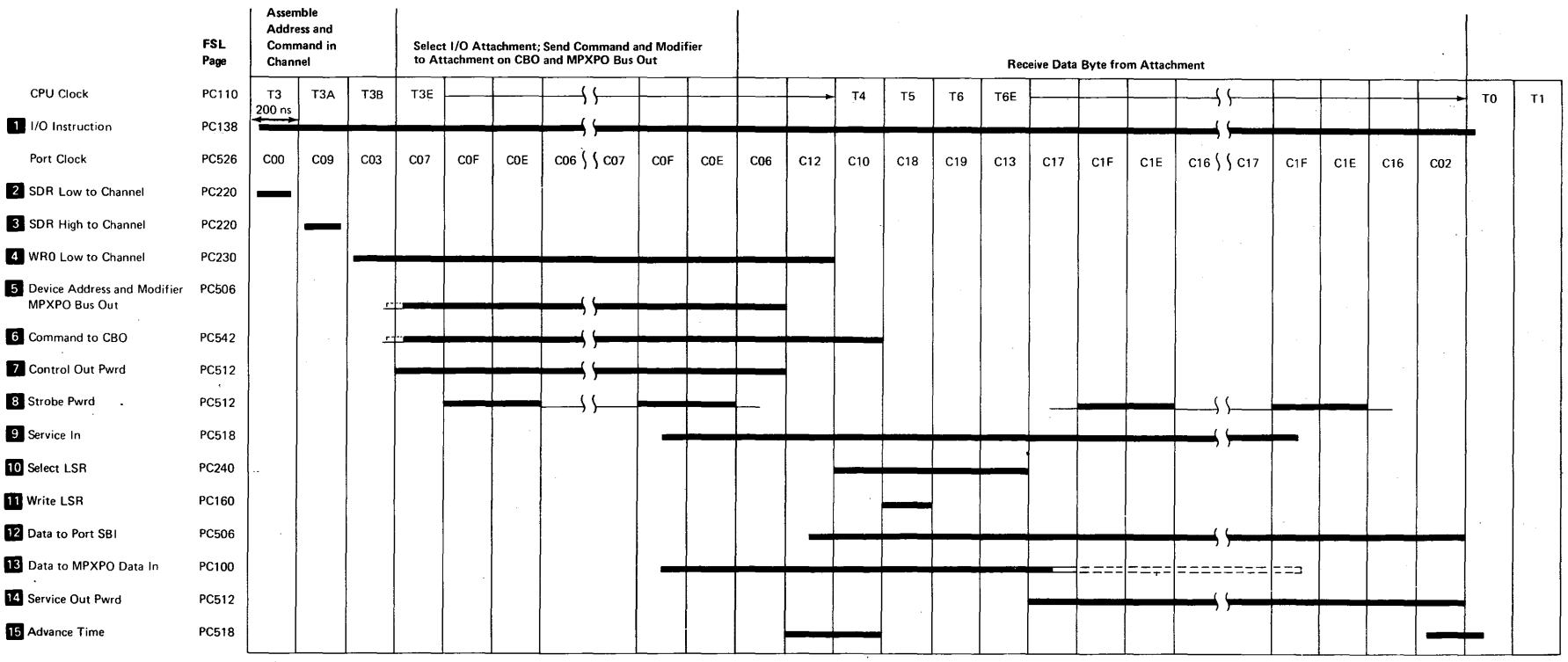
System Bus Out Function Bits 8 9 10 11	Command Bus Out 0 1 2	Command	Mnemonic
0 0 0 0	1 0 0	I/O Load	IOL
0 1 0 0	1 0 1	I/O Sense	IOS
0 1 0 1	0 0 1	Sense Interrupt Level Status Byte	SILSB
1 0 0 0	1 1 0	I/O Control Load	IOCL
1 1 0 0	1 1 1	I/O Control Sense	IOCS
0 0 1 1	0 1 1	Jump on I/O Condition	JIO
	0 1 0	Base Cycle Steal	

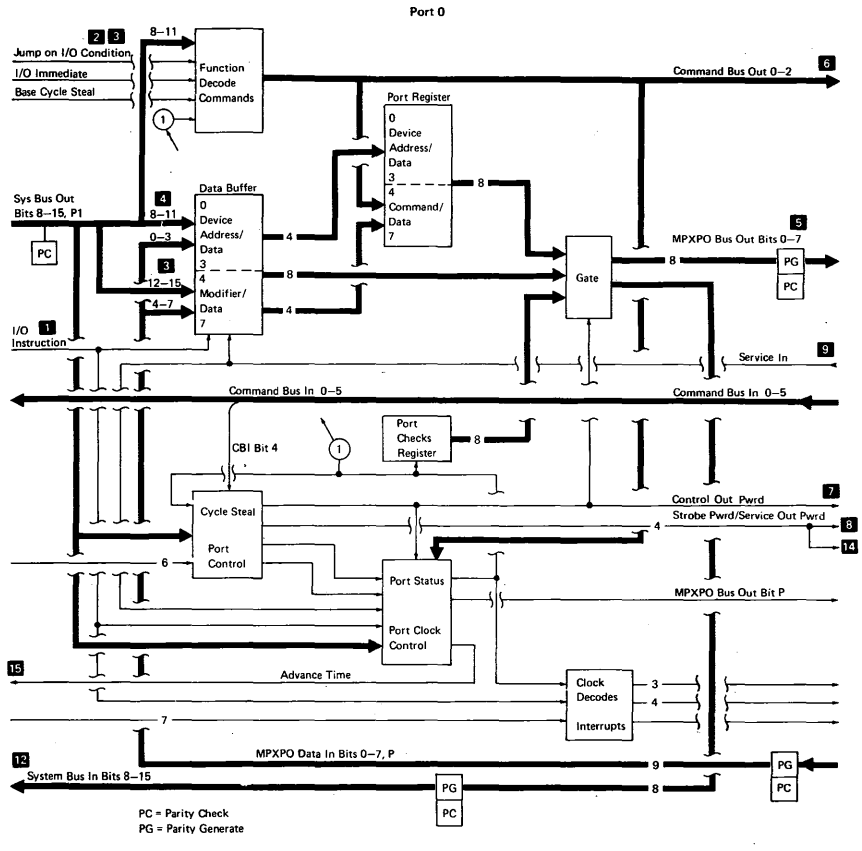
Sense Interrupt Level Status Byte (Big Picture)

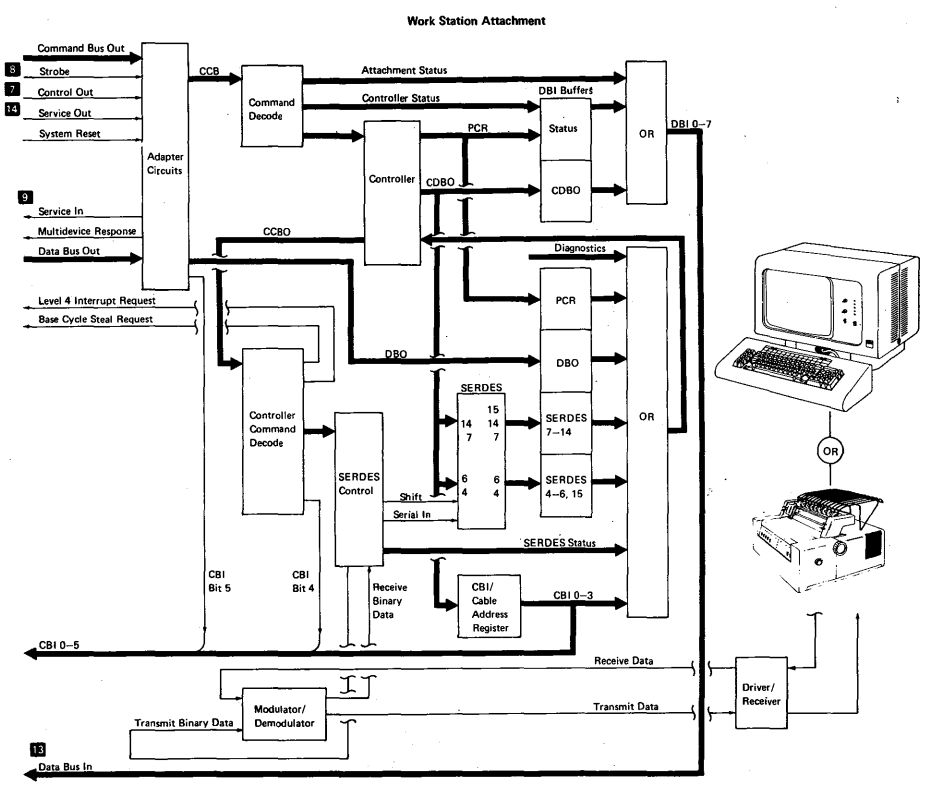


*Data flow bus lines may not pass through FRUs as shown

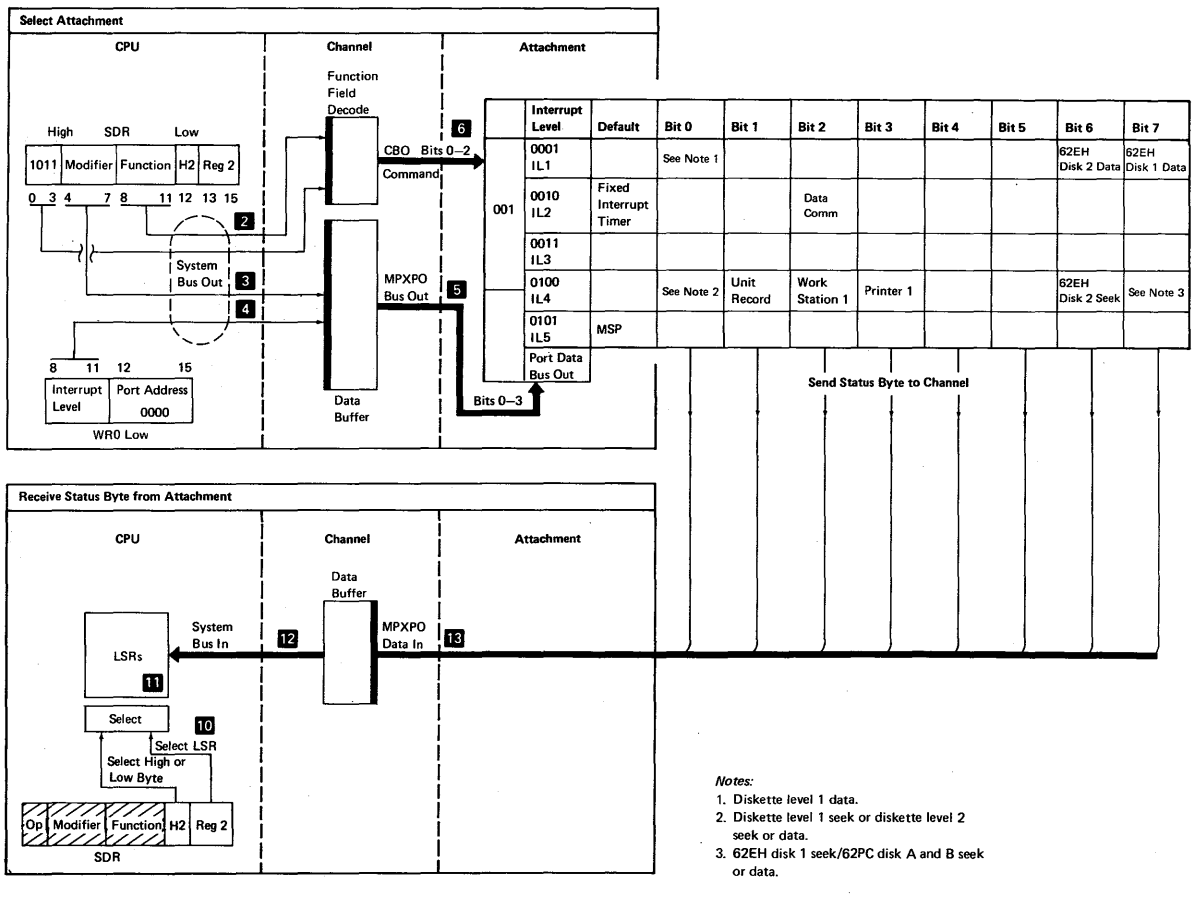

Select Attachment
CPU
Channel
Attachment
Function Field Decode
High SDR Low
1011 Modifier Function H2 Reg 2
0 3 4 7 8 11 12 13 15
System Bus Out
MPXPO Bus Out
CBO Bits 0–2
Command
Bits 0–3
Data Buffer
8 11 12 15
Interrupt Level
Port Address 0000
WR0 Low
Interrupt Level | Default | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7
001
0001 IL1 | 33FD/53FD Data | Disk 2 Data | Disk 1 Data
0010 IL2 | Fixed Interrupt Timer | Comm Line 1
0011 IL3
0100 IL4 | 33FD/53FD Seek | Unit Record | Work Station 1 | Printer 1 | Disk 2 Seek | Disk 1 Seek
0101 IL5 | MSP
Port Data Bus Out
Send Status Byte to Channel
Receive Status Byte from Attachment
CPU
Channel
Attachment
Data Buffer
LSRs
System Bus In
MPXPO Data In
Select
Select LSR
Select High or Low Byte
Op Modifier Function H2 Reg 2
SDR


FSL Page
Assemble Address and Command in Channel
Select I/O Attachment; Send Command and Modifier to Attachment on CBO and MPXPO Bus Out
Receive Data Byte from Attachment
CPU Clock PC110 T3 T3A T3B T3E T4 T5 T6 T6E T0 T1
200 ns
1 I/O Instruction PC138
Port Clock PC526 C00 C09 C03 C07 C0F C0E C06 C07 C0F C0E C06 C12 C10 C18 C19 C13 C17 C1F C1E C16 C17 C1F C1E C16 C02
2 SDR Low to Channel PC220
3 SDR High to Channel PC220
4 WR0 Low to Channel PC230
5 Device Address and Modifier MPXPO Bus Out PC506
6 Command to CBO PC542
7 Control Out Pwrd PC512
8 Strobe Pwrd PC512
9 Service In PC518
10 Select LSR PC240
11 Write LSR PC160
12 Data to Port SBI PC506
13 Data to MPXPO Data In PC100
14 Service Out Pwrd PC512
15 Advance Time PC518


Port 0
Jump on I/O Condition
I/O Immediate
Base Cycle Steal
Function Decode Commands
Command Bus Out 0–2
Port Register
Device Address/ Data
Command/ Data
Sys Bus Out Bits 8–15, P1
Data Buffer
Device Address/ Data
Modifier/ Data
MPXPO Bus Out Bits 0–7
Gate
I/O Instruction
Service In
Command Bus In 0–5
CBI Bit 4
Port Checks Register
Cycle Steal
Port Control
Control Out Pwrd
Strobe Pwrd/Service Out Pwrd
Port Status
Port Clock Control
MPXPO Bus Out Bit P
Advance Time
Clock Decodes
Interrupts
MPXPO Data In Bits 0–7, P
System Bus In Bits 8–15
PC = Parity Check
PG = Parity Generate

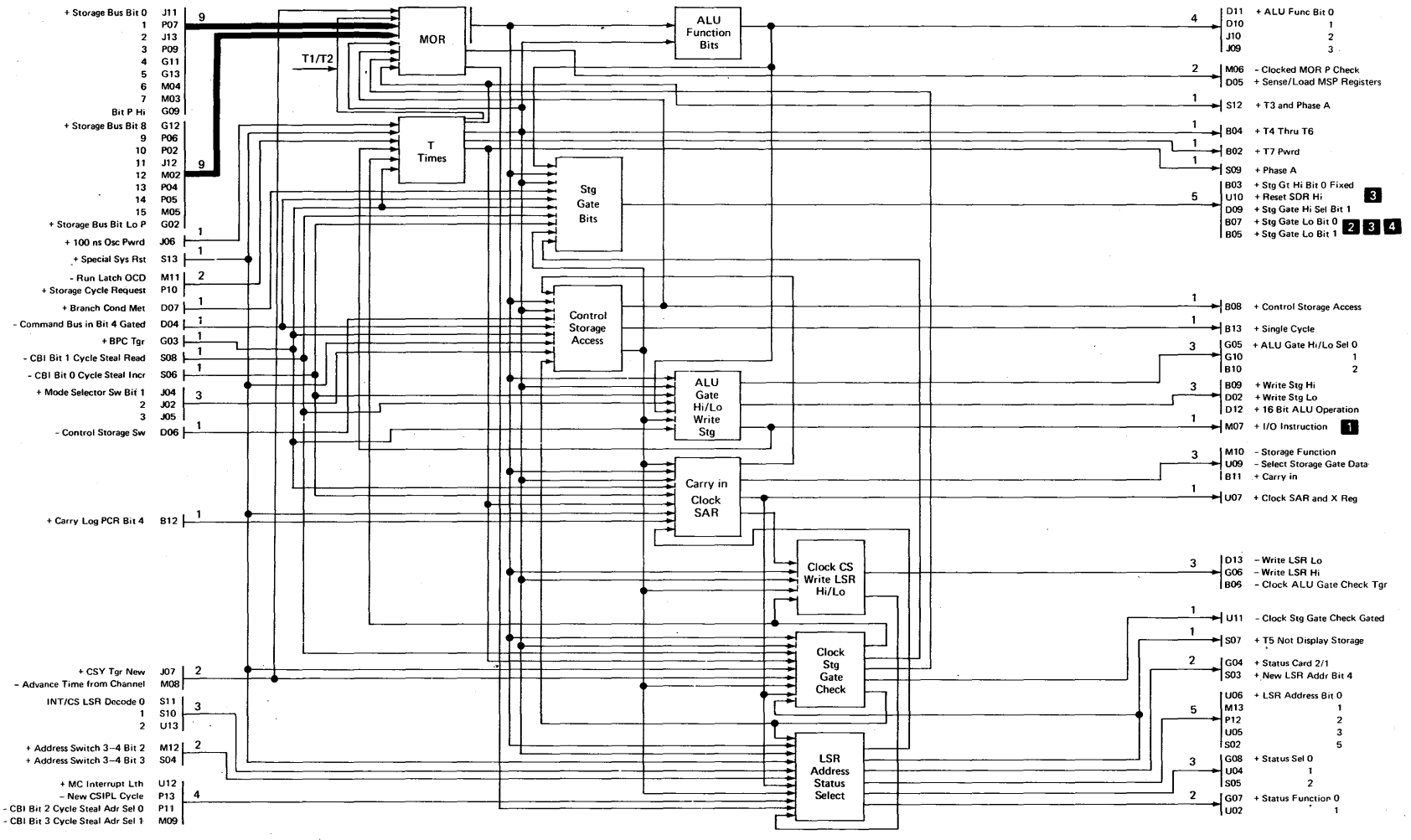

Work Station Attachment
Command Bus Out
Strobe
Control Out
Service Out
System Reset
Service In
Multidevice Response
Data Bus Out
Level 4 Interrupt Request
Base Cycle Steal Request
Adapter Circuits
CCB
Command Decode
Attachment Status
Controller Status
DBI Buffers
Status
CDBO
OR
DBI 0–7
Controller
PCR
CCBO
Diagnostics
DBO
Controller Command Decode
SERDES
SERDES Control
Shift
Serial In
SERDES 7–14
SERDES 4–6, 15
SERDES Status
CBI Bit 5
CBI Bit 4
Receive Binary Data
CBI/ Cable Address Register
CBI 0–3
CBI 0–5
Receive Data
Transmit Data
Transmit Binary Data
Modulator/ Demodulator
Driver/ Receiver
Data Bus In

Sense Interrupt Level Status Byte (Detail)

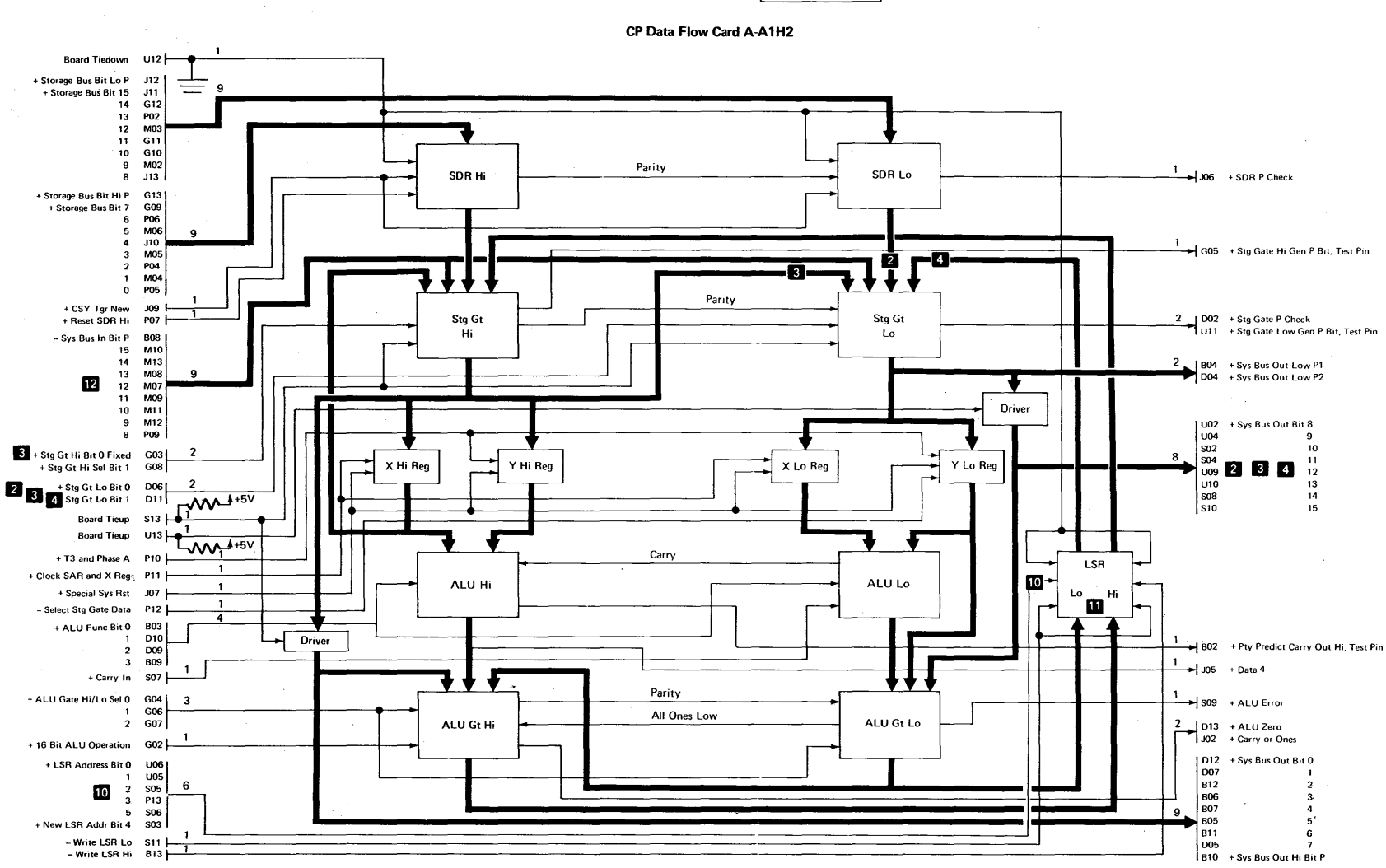


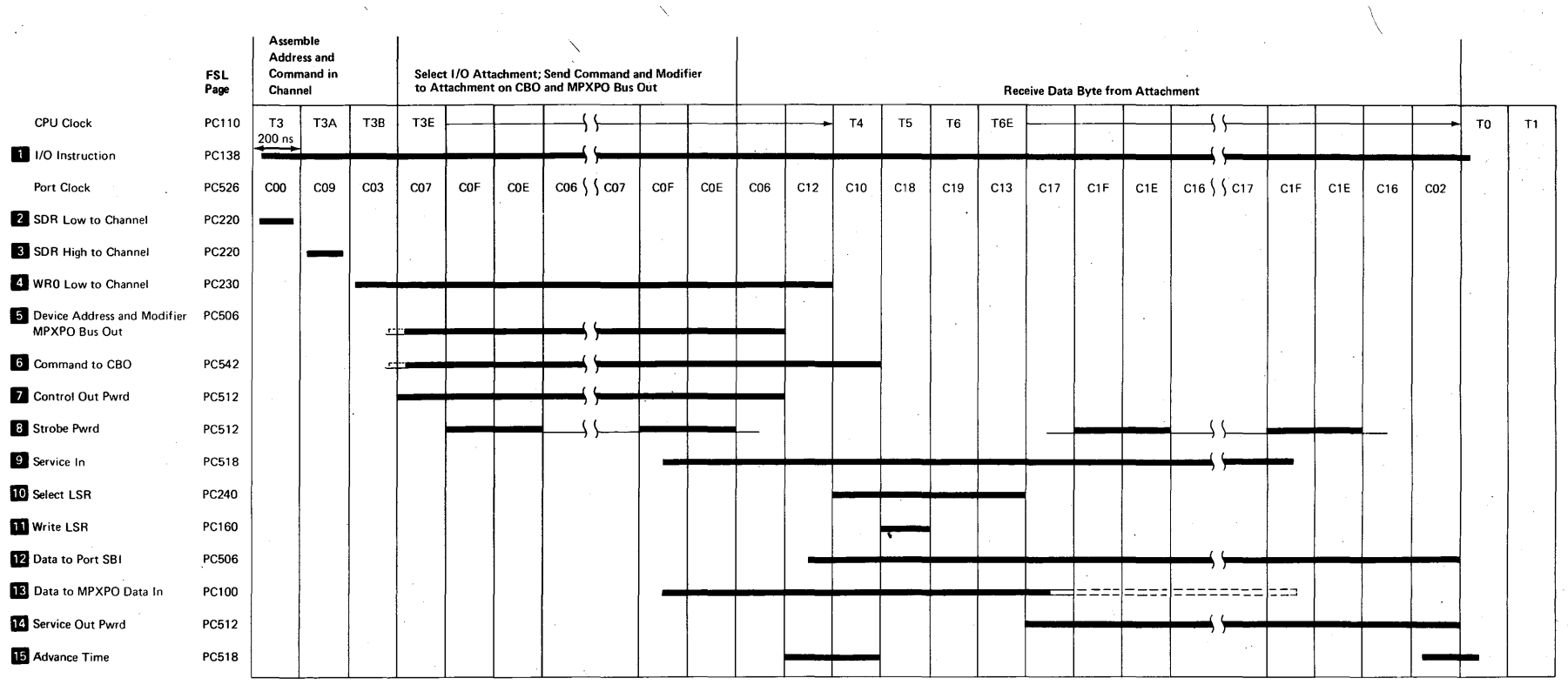
Notes:
1. Diskette level 1 data.
2. Diskette level 1 seek or diskette level 2 seek or data.
3. 62EH disk 1 seek/62PC disk A and B seek or data.

CP System Control Card A-A1G2



CP Data Flow Card A-A1H2

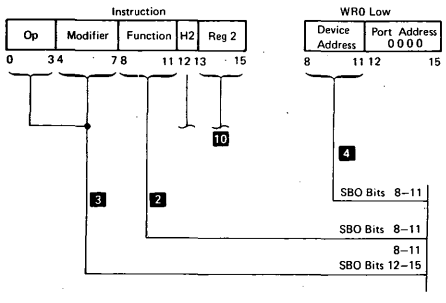


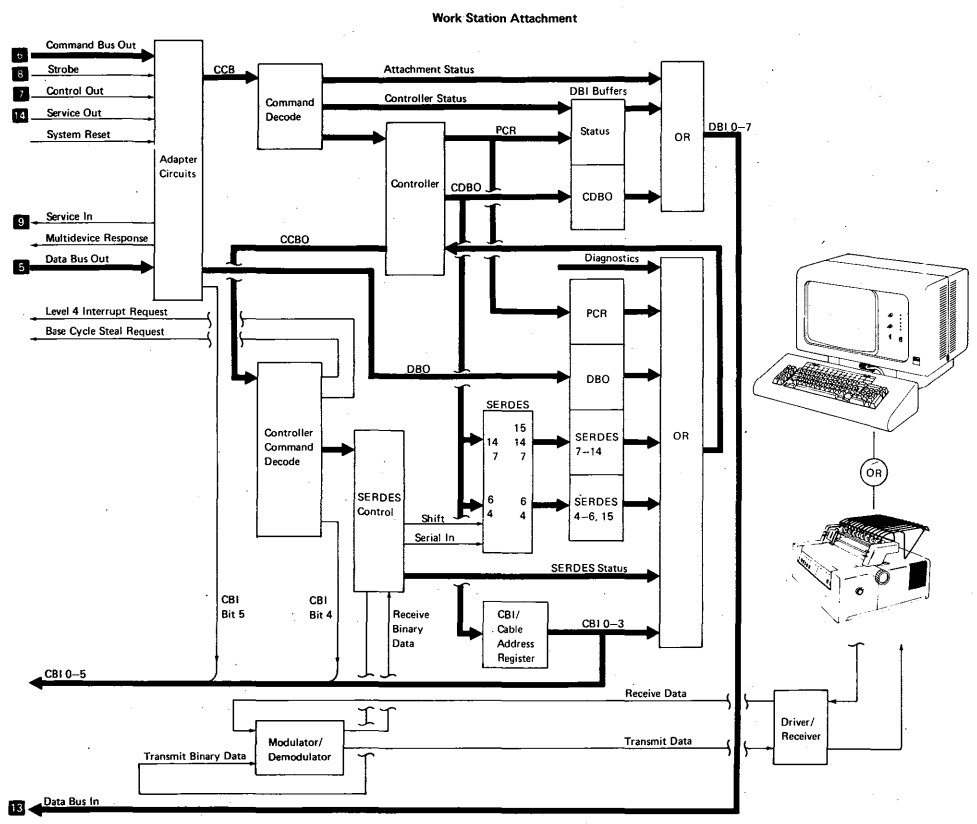


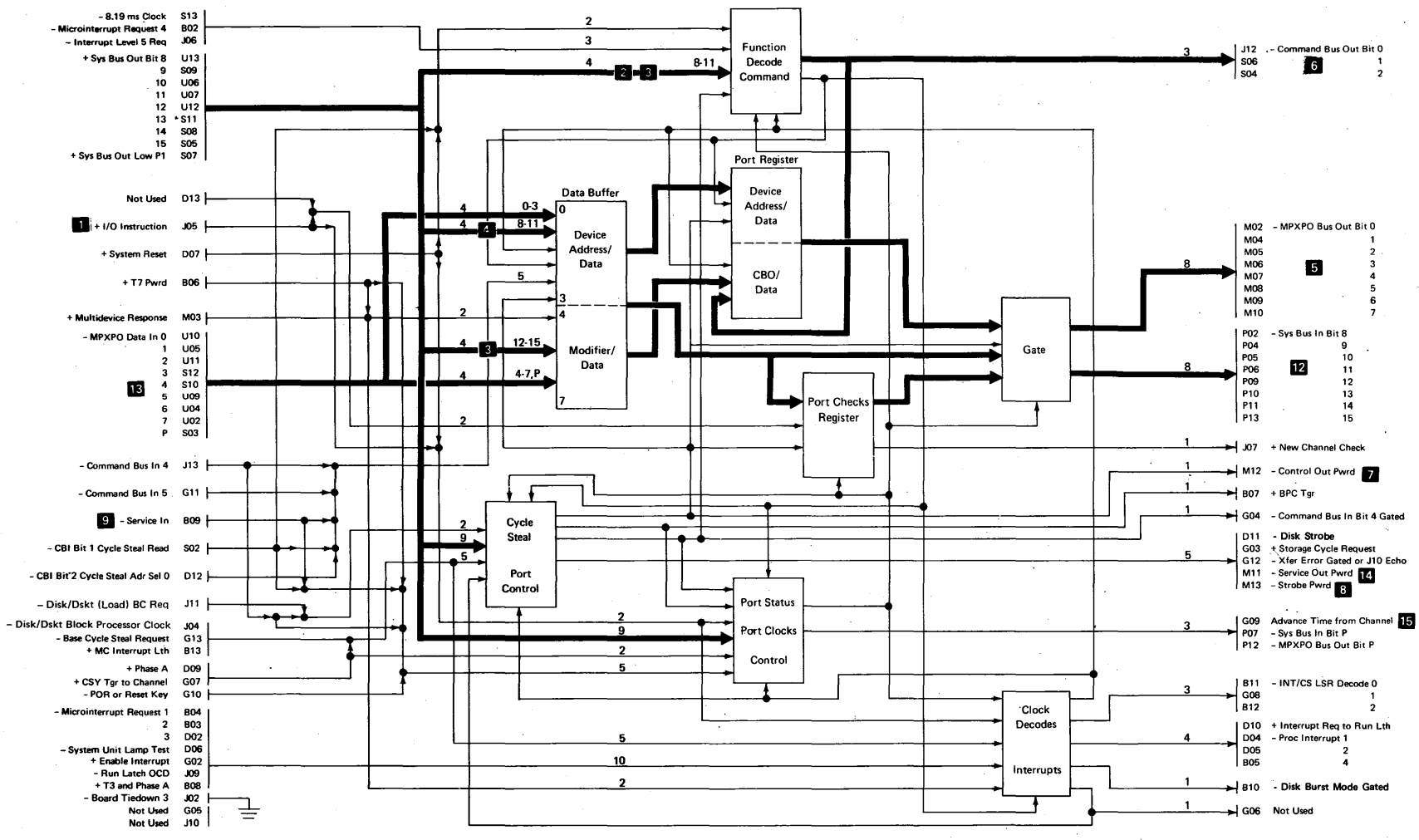
Storage Gate High		
Bit 0	Bit 1	Register Gated Thru
0	0	LSR High
0	1	SDR High
1	0	SBI Bits 8–15
1	1	X Reg High Bits 0–3 SDR Bits 4–7 Stg Gate High Bit P

Storage Gate Low		
Bit 0	Bit 1	Register Gated Thru
0	0	LSR Low
0	1	SDR Low
1	0	SBI Bits 8–15
1	1	Output Stg Gate High

System Bus Out Function Bits 8 9 10 11	Command Bus Out 0 1 2	Command	Mnemonic
0 0 0 0	1 0 0	I/O Load	IOL
0 1 0 0	1 0 1	I/O Sense	IOS
0 1 0 1	0 0 1	Sense Interrupt Level Status Byte	SILSB
1 0 0 0	1 1 0	I/O Control Load	IOCL
1 1 0 0	1 1 1	I/O Control Sense	IOCS
0 0 1 1	0 1 1	Jump on I/O Condition	JIO
	0 1 0	Base Cycle Steal	



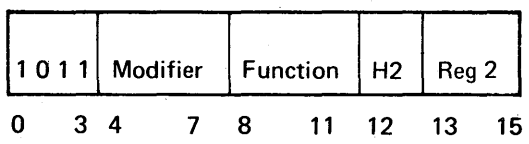




CP Port Card A-A1L2

5

Control Processor Load Function (MPLF)



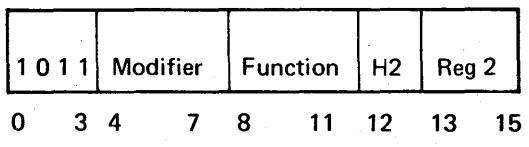
This function of the I/O immediate instruction does not go to the channel but remains in the control processor. It performs functions (such as loading registers), sets/resets conditions, and enables/disables conditions.

Modifier (Bits 4-7): Specifies the type of load function to be performed by the command.

Function (Bits 8-11): Decoded by the control processor as an internal load function when bits 10 and 11 are equal to binary 10.

Modifier 2 (Bits 12-15): Combines with bits 4-7 to specify the type of load function to be performed by the command.

Control Processor Sense (MPS)



This function of the I/O immediate instruction does not go to the channel but remains in the control processor. A byte of data is moved to a local storage register to be used by the program. The byte contains one of the following:

Console status

Address/Data switches 1-4

Processor condition register

Interrupt status

Modifier (Bits 4-7): Selects the byte of data or status to be moved to the selected local storage register.

Function (Bits 8-11): Decoded by the control processor as an internal sense function when bits 10 and 11 are equal to binary 10.

H2 (Bit 12): Selects the low- or high-order byte of the selected local storage register for the current interrupt level:

H2 = 0: Low-order byte

H2 = 1: High-order byte

Register 2 (Bits 13-15): Selects one of the eight work registers in the local storage register stack for the current interrupt level. The selected register stores the byte of data to be used by the program.

Control Processor Sense (MSP)

The contents of these bytes or switches are moved to an LSR. This data can then be used by the program.

4 5 6 7	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0 0 1 1 Interrupt status	Invalid logout					Interrupt code	Interrupt code	Interrupt code
0 1 0 0 Console status byte	Stop key	Main storage address compare	Overlap off	MSIPL device select switch	I/O request	Sys step mode	Go flag	Micro-interrupt check
0 1 0 1 Address/ Data switches 3 and 4	Switch 3 8	Switch 3 4	Switch 3 2	Switch 3 1	Switch 4 8	Switch 4 4	Switch 4 2	Switch 4 1
0 1 1 0 I/O clocks low byte	8.19 ms	16.38 ms	32.77 ms	65.54 ms	131.1 ms	262.1 ms	524.3 ms	1s
0 1 1 1 I/O clocks high byte	32 μs	64 μs	128 μs	256 μs	512 μs	1.02 ms	2.05 ms	4.10 ms
1 0 0 1 Address/ Data switches 1 and 2	Switch 1 8	Switch 1 4	Switch 1 2	Switch 1 1	Switch 2 8	Switch 2 4	Switch 2 2	Switch 2 1
1 0 1 0 CPU error byte	SDR P check	MOR P check	Storage gate P check	ALU gate P check	Control storage invalid addr/ SAR check	Microloop time-out/ SAR check	Main storage invalid addr/ MSAR check	Main storage exception/ MSAR check
1 0 1 1 PCR	Flag	Plus	Minus	Zero	Carry log	High log	Low log	Equal log

Control Processor Sense (Interrupt Status/Code)

The interrupt code indicates which hardware interrupt level the control processor was executing on when the error occurred that caused the logout. A decode of the interrupt code in terms of a hardware interrupt level is as follows:

Interrupt Code (Bits 5-7) Interrupt Level (Hex)	Hardware Interrupt Level
0	5
1	4/Base cycle steal
2	Base cycle steal/Burst cycle steal
3	3
4	2
5	1/Burst cycle steal
7	0/Main level

I/O Sense (IOS)

By checking channel check byte bit 6 = 1 (cycle steal check), the CE can determine if the interrupt was caused by a hardware level or a cycle steal operation.

IOS (Channel/Port)

	4 5 6 7	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Port Register	0 0 0 0	Data							
Sense Port Error Byte	0 0 0 1	MPXPO bus out	Invalid device address	DBI P check	I/O time-out check	CBI/DBI not zero	System bus out P check	Cycle steal check	Invalid port

I/O Storage (WTCL, WTCH, RDCL, RDCH, WTM, RDM)

WTCL (I/O load from control storage low)

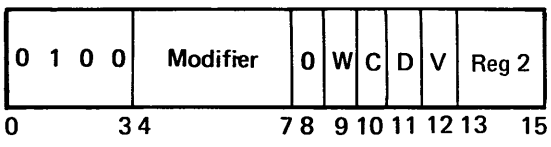
WTCH (I/O load from control storage high)

RDCL (I/O store to control storage low)

RDCH (I/O store to control storage high)

WTM (I/O load from main storage)

RDM (I/O store to main storage)



This instruction moves 1 byte of data between either main storage or control storage and the I/O attachment.

Modifier (Bits 4-7): Specifies the control field for the I/O attachment.

The field is moved to the attachment through the port. Bit 4 of this field is used in the control processor to select the high- or low-order byte of control storage. When main storage is being addressed, bit 4 is not used by the control processor.

Bit 8: Changes the operation code (bits 0-3). Bit 8 is always a 0.

W (Bit 9): Identifies the direction the data is to be moved.

W = 0: Read data from storage and move it to the I/O attachment

W = 1: Write data to storage from the I/O attachment

C (Bit 10): Selects main storage or control storage.

C = 0: Main storage

C = 1: Control storage

D (Bit 11): Indicates if the address in the local storage register (specified by bits 13-15) is to be increased or decreased.

D = 0: Increase the selected local storage register by the value of field V

D = 1: Decrease the selected local storage register by the value of field V

Note: Bits 8-11 are sent to the port where they are decoded as either the load command or the sense command. The command is then sent to the I/O attachment on the 'command bus out' lines.

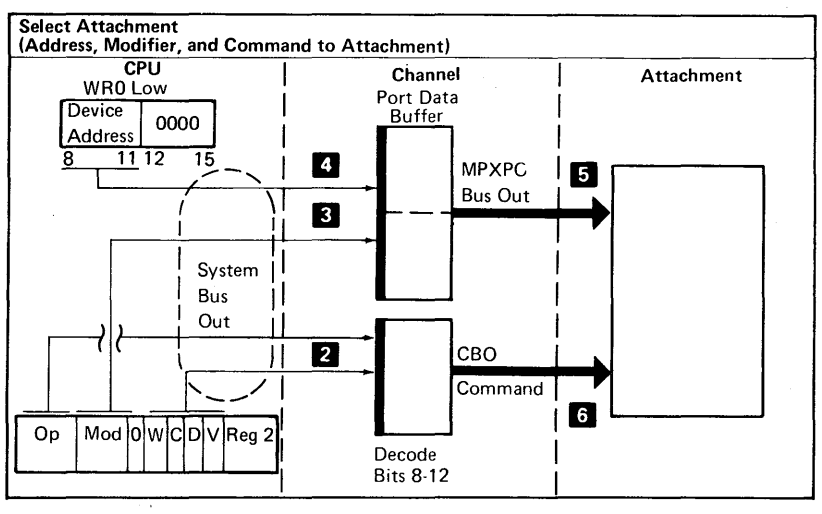
V (Bit 12): Indicates the amount the address in the local storage register (specified by bits 13-15) should be increased or decreased. If V = 0, the address in the selected local storage register is not changed. If V = 1, the address in the selected local storage register is decreased or increased by 1, as specified by the bit setting of field D.

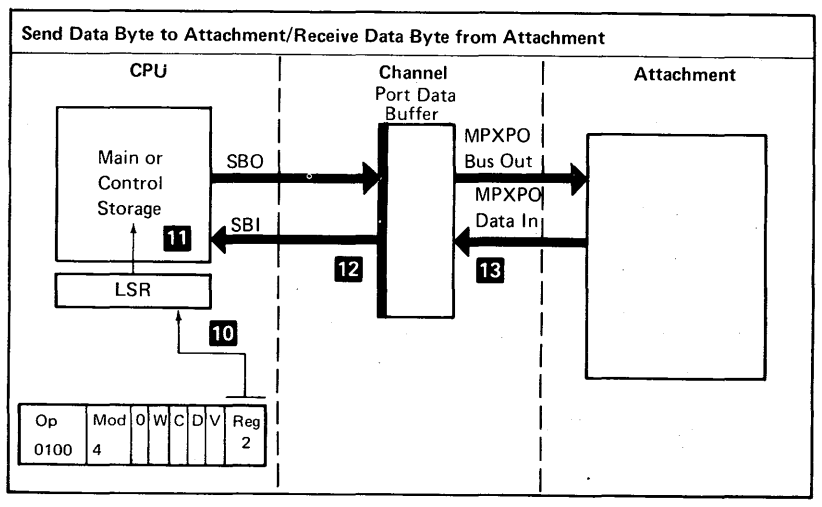
Register 2 (Bits 13-15): Selects one of the eight local storage registers assigned to the present interrupt level that contains the storage address needed to move the data. The address in the specified local storage register may be updated as specified by bit 11 (field D) and bit 12 (field V).

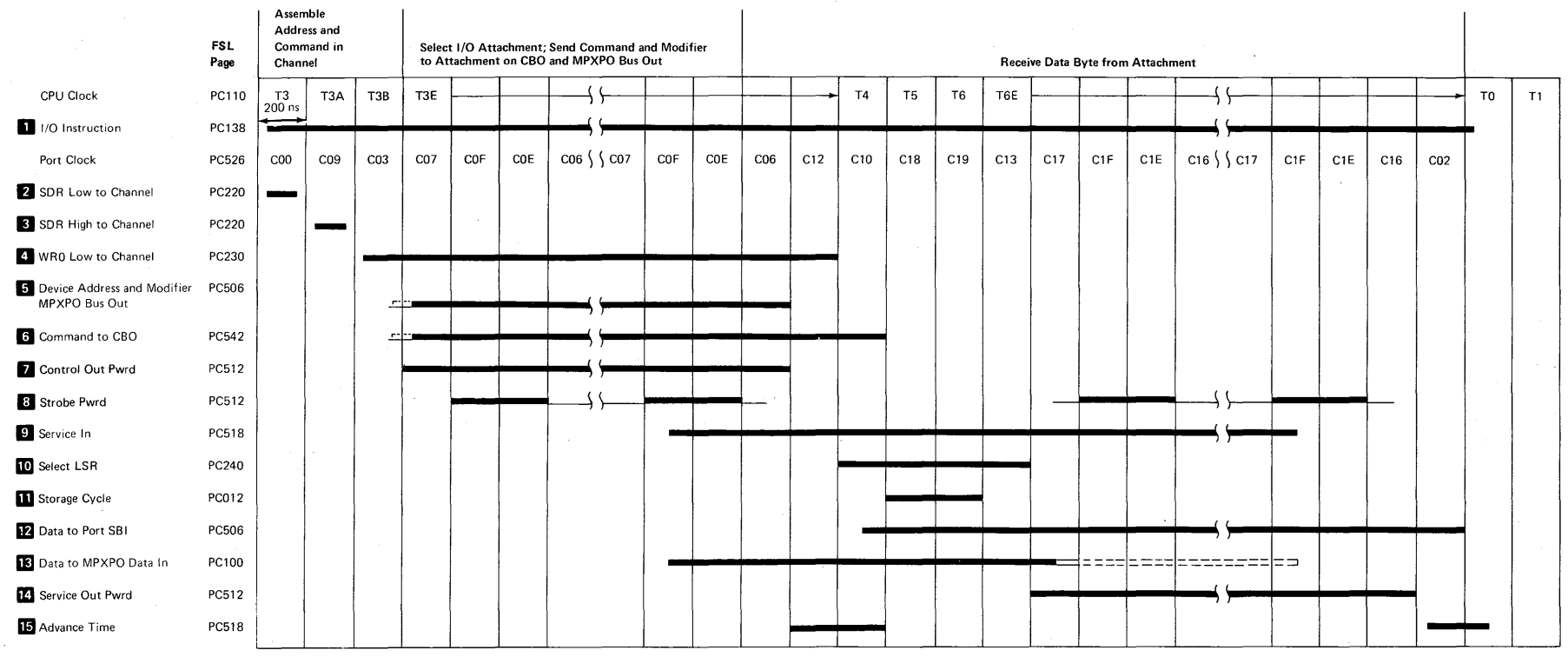
Bits 4 8 9 10 11 12	Mnemonic	Description
0 0 1 1 0 1	RDCL	I/O store to control storage,
1 0 1 1 0 1	RDCH	increase register 2 by 1
0 0 1 1 1 1	RDCL	I/O store to control storage,
1 0 1 1 1 1	RDCH	decrease register 2 by 1
0 0 1 1 0 0	RDCL	I/O store to control storage,
1 0 1 1 0 0	RDCH	no change to register 2
0 0 0 1 0 1	WTCL	I/O load from control storage,
1 0 0 1 0 1	WTCH	increase register 2 by 1
0 0 0 1 1 1	WTCL	I/O load from control storage,
1 0 0 1 1 1	WTCH	decrease register 2 by 1
0 0 0 1 0 0	WTCL	I/O load from control storage,
1 0 0 1 0 0	WTCH	no change to register 2
X 0 1 0 0 1	RDM	I/O store to main storage, increase register 2 by 1
X 0 1 0 1 1	RDM	I/O store to main storage, decrease register 2 by 1
X 0 1 0 0 0	RDM	I/O store to main storage, no change to register 2
X 0 0 0 0 1	WTM	I/O load from main storage, increase register 2 by 1
X 0 0 0 1 1	WTM	I/O load from main storage, decrease register 2 by 1
X 0 0 0 0 0	WTM	I/O load from main storage, no change to register 2

Legend for Bit 4:
X: Not used

I/O Storage (Load–Big Picture)

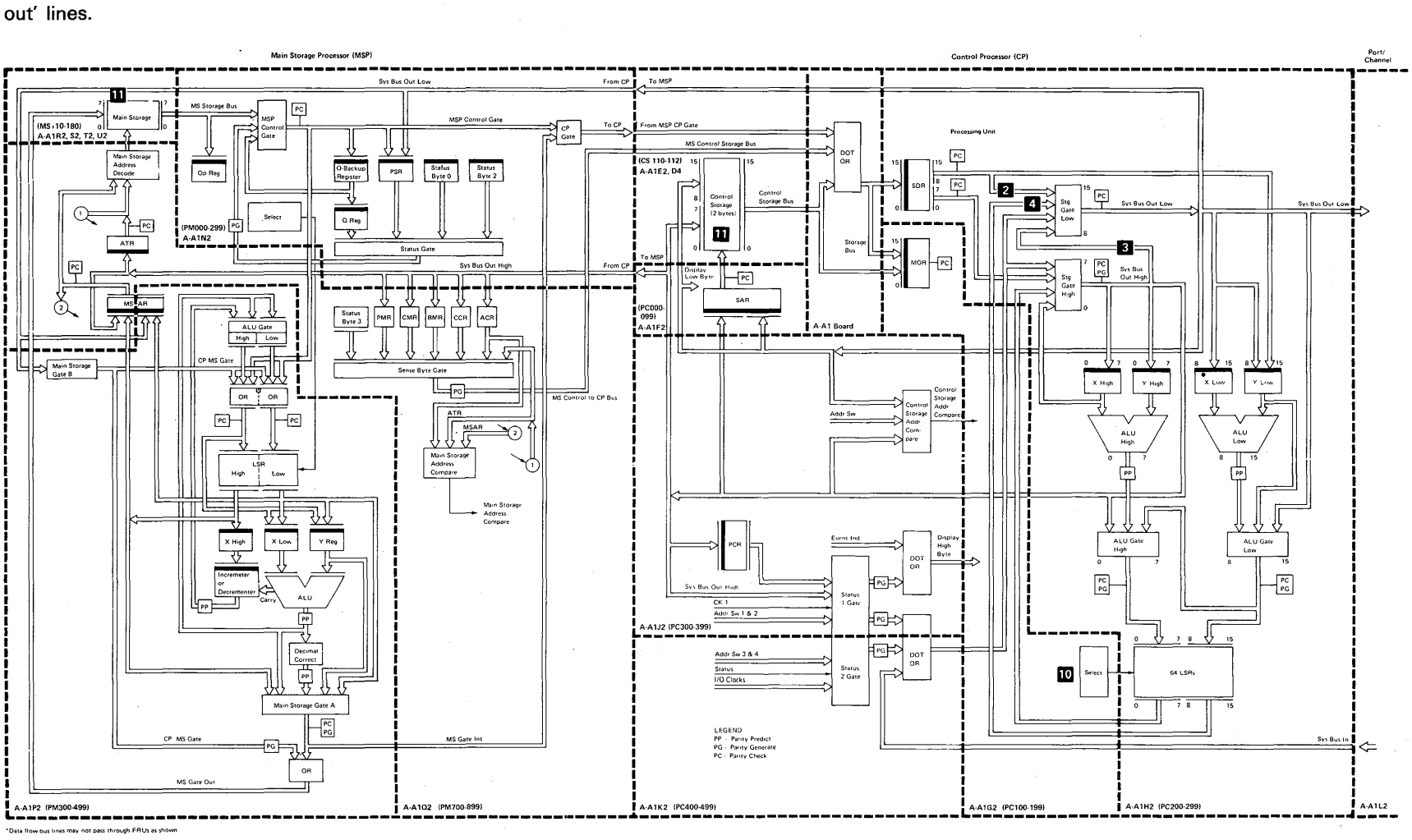




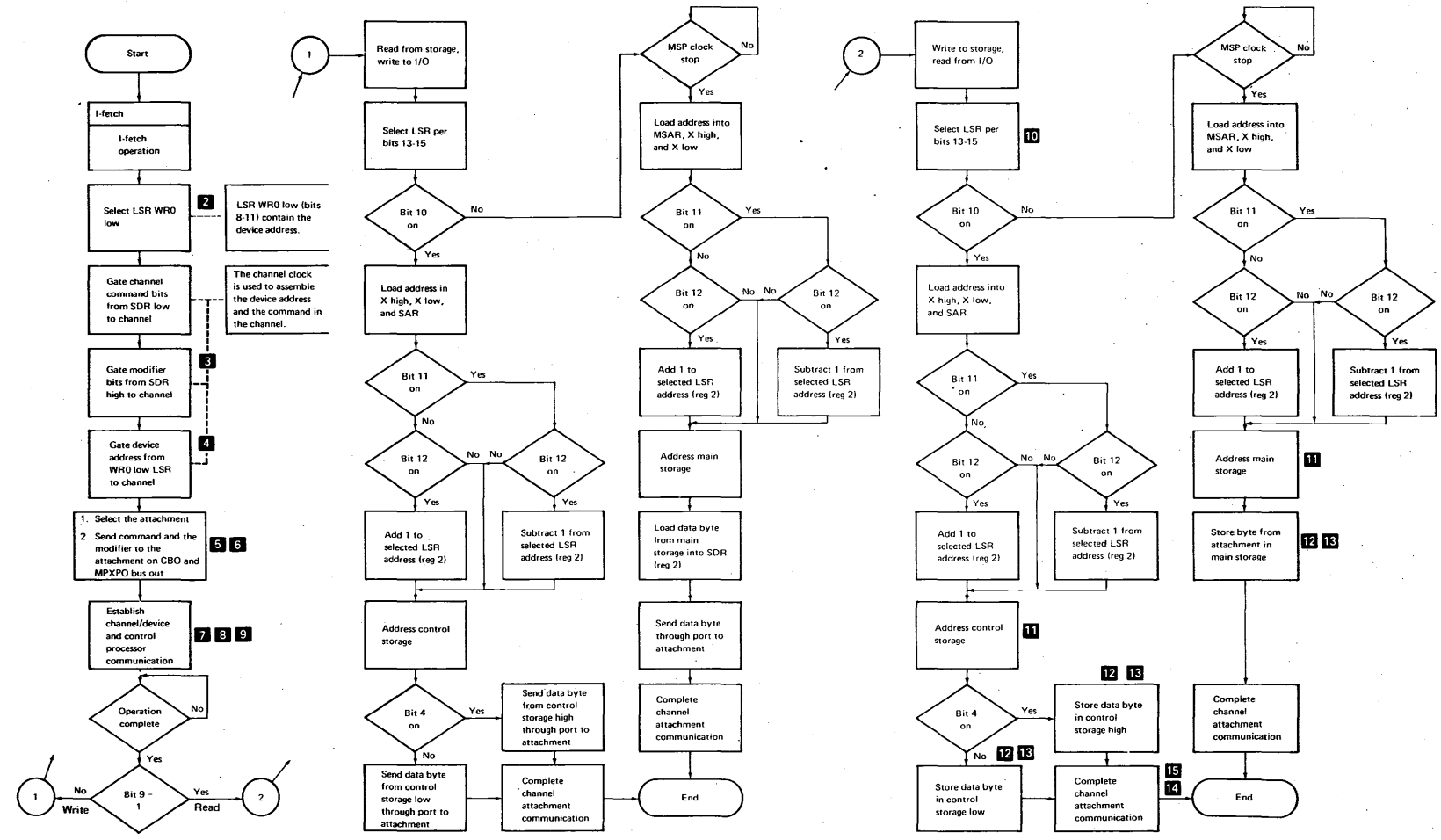


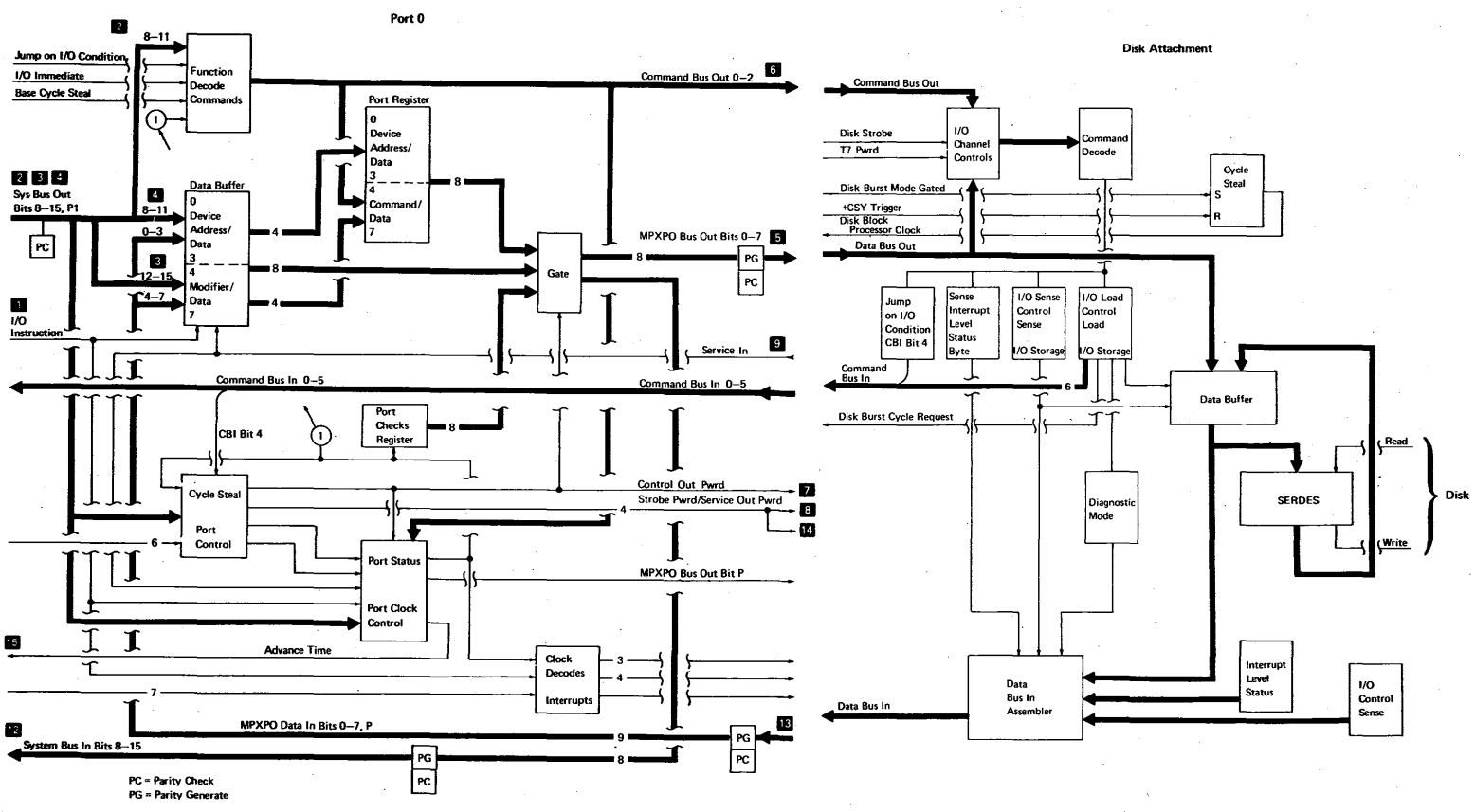
The first 'strobe pwrd' pulse after the rise of the 'control out pwrd' line signals the I/O attachment that the device address and the command information on the 'command bus out' and 'MPXPO bus out' lines are valid. The rise of the 'service in' line signals the port that the I/O attachment has taken the information from the 'command bus out' and 'MPXPO bus out' lines and is ready to receive data.

The first 'strobe pwrd' pulse after the rise of the 'service out pwrd' line signals the I/O attachment that the data byte on the 'MPXPO bus out' lines is valid. The fall of the 'service in' line signals the port that the I/O attachment has taken the data byte from the 'MPXPO bus out' lines.

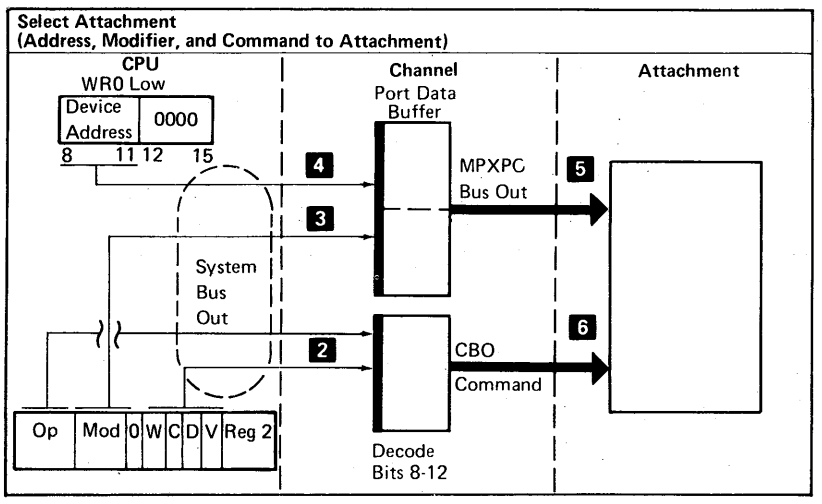


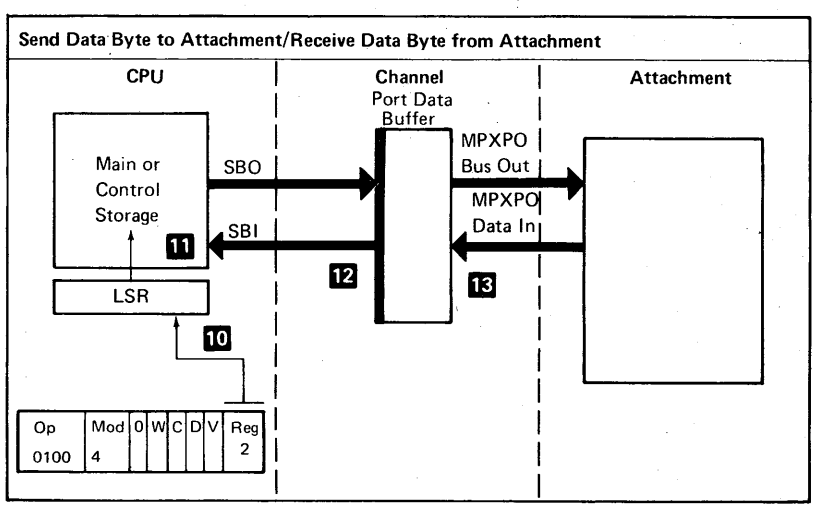
*Data flow bus lines may not pass through FRUs as shown


Start
I-fetch
I-fetch operation
Select LSR WR0 low
LSR WR0 low (bits 8-11) contain the device address.
Gate channel command bits from SDR low to channel
The channel clock is used to assemble the device address and the command in the channel.
Gate modifier bits from SDR high to channel
Gate device address from WR0 low LSR to channel
1. Select the attachment
2. Send command and the modifier to the attachment on CBO and MPXPO bus out
Establish channel/device and control processor communication
Operation complete
No
Yes
Bit 9 = 1
No
Write
Yes
Read
1
2
Read from storage, write to I/O
Select LSR per bits 13-15
Bit 10 on
No
Yes
Load address in X high, X low, and SAR
Bit 11 on
Yes
No
Bit 12 on
No
No
Bit 12 on
Yes
Yes
Add 1 to selected LSR address (reg 2)
Subtract 1 from selected LSR address (reg 2)
Address control storage
Bit 4 on
Yes
No
Send data byte from control storage high through port to attachment
Send data byte from control storage low through port to attachment
Complete channel attachment communication
End
MSP clock stop
No
Yes
Load address into MSAR, X high, and X low
Bit 11 on
Yes
No
Bit 12 on
No
No
Bit 12 on
Yes
Yes
Add 1 to selected LSR address (reg 2)
Subtract 1 from selected LSR address (reg 2)
Address main storage
Load data byte from main storage into SDR (reg 2)
Send data byte through port to attachment
Complete channel attachment communication
Write to storage, read from I/O
Select LSR per bits 13-15
Bit 10 on
No
Yes
Load address into X high, X low, and SAR
Bit 11 on
Yes
No
Bit 12 on
No
No
Bit 12 on
Yes
Yes
Add 1 to selected LSR address (reg 2)
Subtract 1 from selected LSR address (reg 2)
Address control storage
Bit 4 on
Yes
No
Store data byte in control storage high
Store data byte in control storage low
Complete channel attachment communication
MSP clock stop
No
Yes
Load address into MSAR, X high, and X low
Bit 11 on
Yes
No
Bit 12 on
No
No
Bit 12 on
Yes
Yes
Add 1 to selected LSR address (reg 2)
Subtract 1 from selected LSR address (reg 2)
Address main storage
Store byte from attachment in main storage
Complete channel attachment communication
End

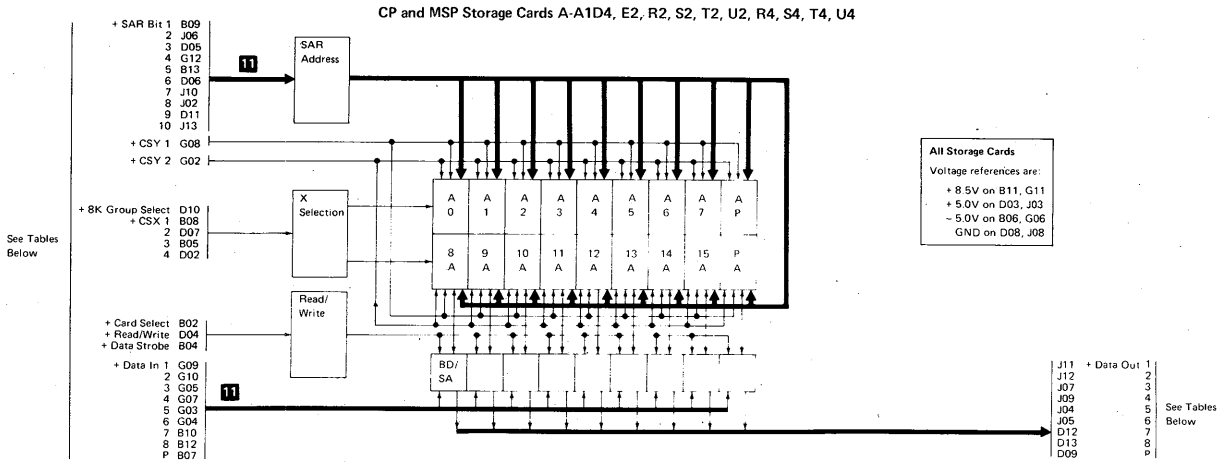

Port 0
Jump on I/O Condition
I/O Immediate
Base Cycle Steal
Function Decode Commands
Command Bus Out 0–2
Port Register
Device Address/ Data
Command/ Data
Data Buffer
Device Address/ Data
Modifier/ Data
Sys Bus Out Bits 8–15, P1
PC
I/O Instruction
Gate
MPXPO Bus Out Bits 0–7
PG
PC
Service In
Command Bus In 0–5
CBI Bit 4
Port Checks Register
Cycle Steal
Port Control
Control Out Pwrd
Strobe Pwrd/Service Out Pwrd
Port Status
Port Clock Control
MPXPO Bus Out Bit P
Advance Time
Clock Decodes
Interrupts
MPXPO Data In Bits 0–7, P
System Bus In Bits 8–15
PC = Parity Check
PG = Parity Generate
Disk Attachment
Command Bus Out
Disk Strobe
T7 Pwrd
I/O Channel Controls
Command Decode
Disk Burst Mode Gated
+CSY Trigger
Disk Block Processor Clock
Cycle Steal
S
R
Data Bus Out
Jump on I/O Condition CBI Bit 4
Sense Interrupt Level Status Byte
I/O Sense Control Sense
I/O Load Control Load
I/O Storage
Command Bus In
Disk Burst Cycle Request
Data Buffer
Diagnostic Mode
SERDES
Read
Write
Disk
Data Bus In Assembler
Interrupt Level Status
I/O Control Sense
Data Bus In

I/O Storage (Load-Detail)

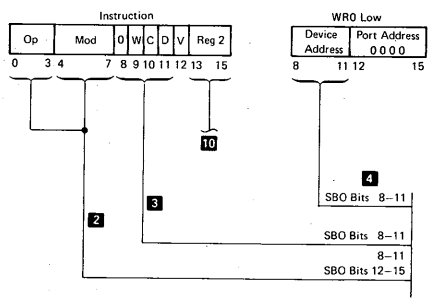




CP and MSP Storage Cards A-A1D4, E2, R2, S2, T2, U2, R4, S4, T4, U4



All Storage Cards
Voltage references are:
+ 8.5V on B11, G11
+ 5.0V on D03, J03
– 5.0V on B06, G06
GND on D08, J08



Card →	A1E2		A1D4		A1R2, T2, R4, T4		A1S2, U2, S4, U4	
+ Card Select	F2 B11	+ CS Card Select 0–16K	F2 B11	+ CS Card Select 0–16K	·	+ MS Card Select 0	·	+ MS Card Select 0
+ Read/Write	F2 D05	+ CS Write Pulse Hi	F2 D06	+ CS Write Pulse Lo	Q2 S10	+ MS Write Pulse Lo	Q2 S11	+ MS Write Pulse Hi
+ Data Strobe		+ Board Tieup		+ Board Tieup	Q2 S03	+ MS Data Strobe Lo	Q2 S04	+ MS Data Strobe Hi
+ 8K Group Select	F2 J02	+ 8K Group Select	F2 J02	+ 8K Group Select	Q2 U09	– MS 8K Group Select Lo	Q2 U09	– MS 8K Group Select Lo

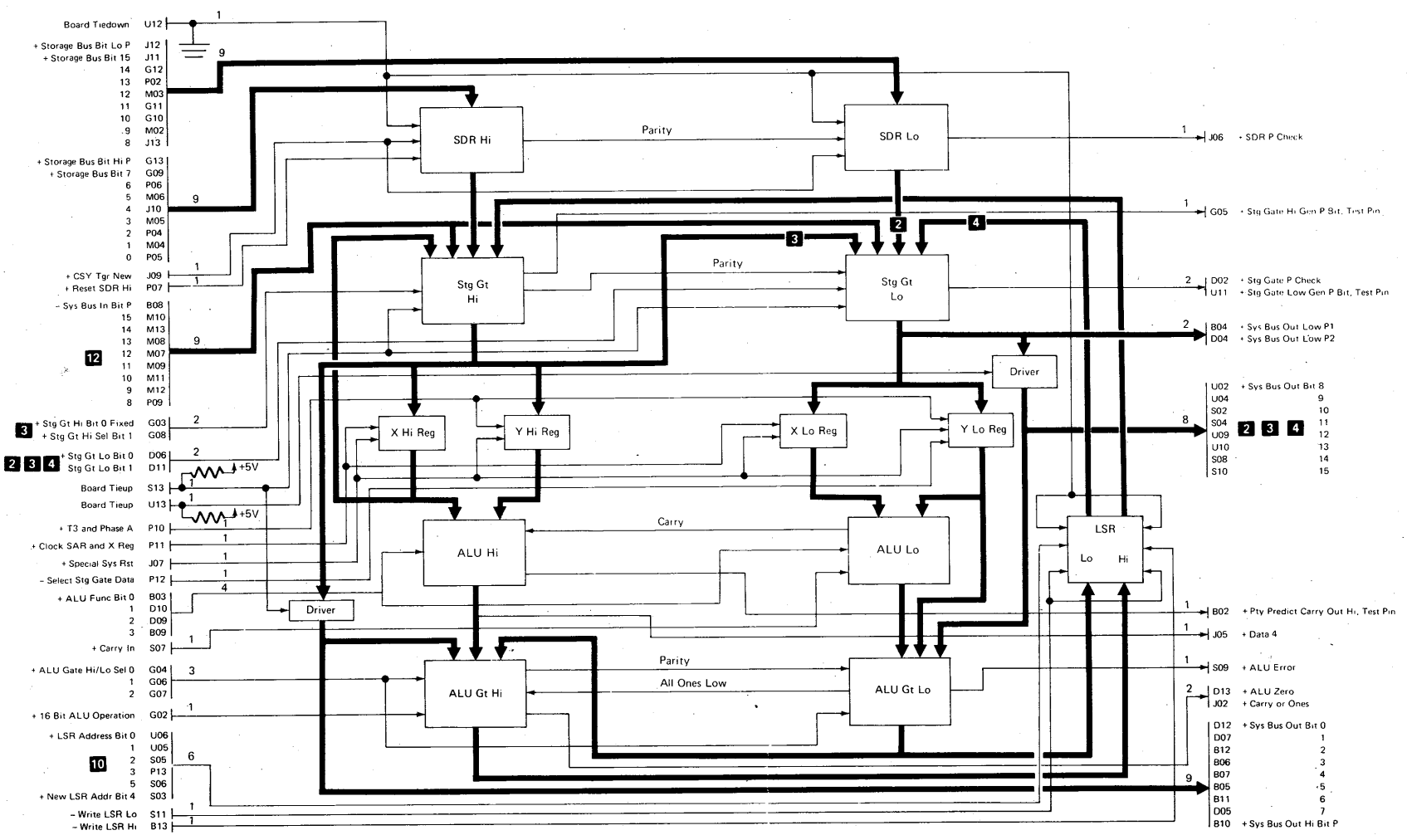
*Card ↓	+ Card Select		ATR 0 to 3
A1R2, S2	Q2U11	+ MS Card Select 0–32K	0000
A1T2, U2	Q2U12	+ MS Card Select 32–64K	0001
A1R4, S4	Q2U13	+ MS Card Select 64–96K	0010
A1T4, U4	Q2S13	+ MS Card Select 96–128K	0011

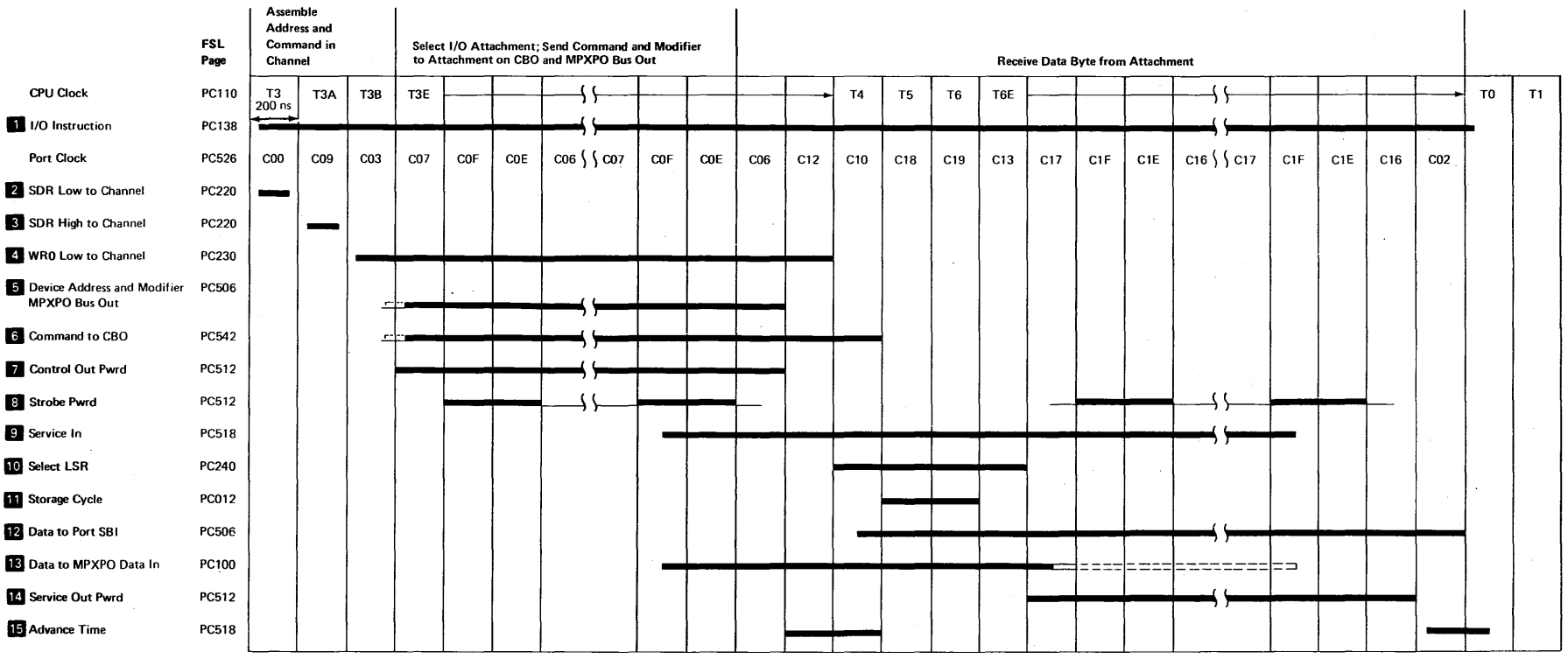
Card →	A1E2			A1D4			A1R2, S2, T2, U2, R4, S4, T4, U4		
+ Data Out 1	G2 J11	+ Storage Bus Bit	0	G2 G12	+ Storage Bus Bit	8	N2 G02	+ MS Storage Bus Bit	8
2	G2 P07		1	G2 P06		9	N2 G03		9
3	G2 J13		2	G2 P02		10	N2 G04		10
4	G2 P09		3	G2 J12		11	N2 J05		11
5	G2 G11		4	G2 M02		12	N2 J07		12
6	G2 G13		5	G2 P04		13	N2 G08		13
7	G2 M04		6	G2 P05		14	N2 J02		14
8	G2 M03		7	G2 M05		15	N2 G09		15
P	G2 G09		P Hi	G2 G02		Lo P	N2 J06		P
+ Data In 1	H2 D12	+ System Bus Out	0	H2 U04	+ System Bus Out Lo	8	P2 J02	+ MS Gt Out Bit	8
2	H2 D07		1	H2 U04		9	P2 J04		9
3	H2 B12		2	H2 S02		10	P2 G07		10
4	H2 B06		3	H2 S04		11	P2 J07		11
5	H2 B07		4	H2 U09		12	P2 G02		12
6	H2 B05		5	H2 U10		13	P2 G03		13
7	H2 B11		6	H2 S08		14	P2 G04		14
8	H2 D05		7	H2 S10		15	P2 G06		15
P	H2 B10	+ System Bus Out Hi Bit	P	H2 D04	+ Sys Bus Out Lo	P2	P2 B09		P

Card →	A1E2 & A1D4		A1R2,S2,T2,U2,R4,S4,T4,U4	
+ SAR Bit 1	F2 U07	+ SAR Bit 6	Q2 S06	+ MSAR Bit 6
2	F2 M12	7	Q2 S07	7
3	F2 U10	8	P2 B06	8
4	F2 S06	9	P2 B03	9
5	F2 P13	10	P2 B02	10
6	F2 M13	11	P2 B07	11
7	F2 P06	12	P2 D07	12
8	F2 U12	13	P2 D05	13
9	F2 U13	14	P2 B08	14
10	F2 M11	15	P2 D09	15
+ CSX 1	F2 B13	+ CSX 1	Q2 U04	+ MS CSX 1
2	F2 B08	2	Q2 U05	2
3	F2 B07	3	Q2 U06	3
4	F2 B06	4	Q2 U07	4
+ CSY 1	F2 D11	+ CSY 1	Q2 S08	+ MS CSY 1
2	F2 D07	2	Q2 S09	2

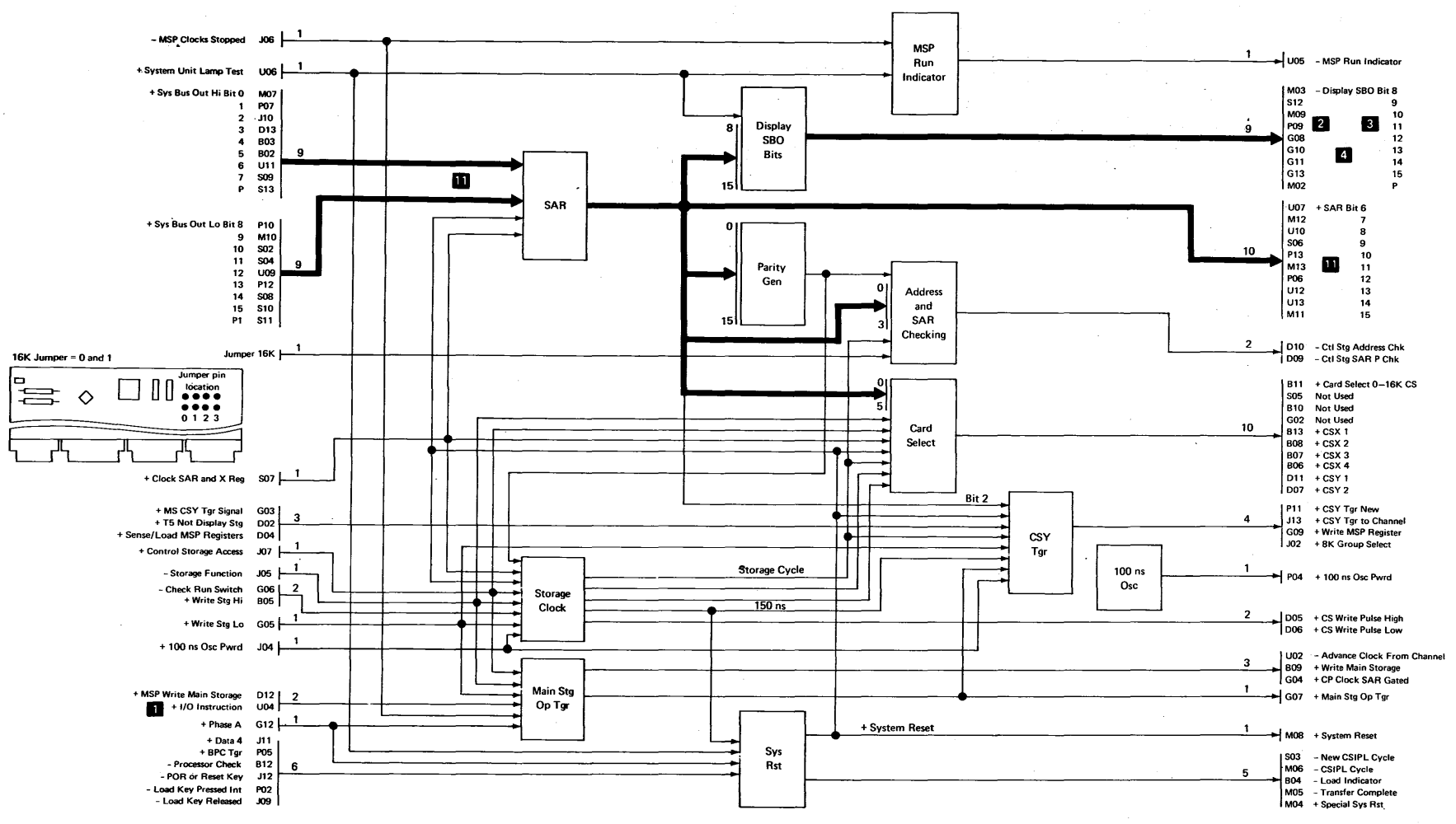
Storage Gate High		
Bit 0	Bit 1	Register Gated Thru
0	0	LSR High
0	1	SDR High
1	0	SBI Bits 8–15
1	1	X Reg High Bits 0–3 SDR Bits 4–7 Stg Gate High Bit P
Storage Gate Low		
Bit 0	**Bit 1**	**Register Gated Thru**
0	0	LSR Low
0	1	SDR Low
1	0	SBI Bits 8–15
1	1	Output Stg Gate High

CP Data Flow Card A-A1H2





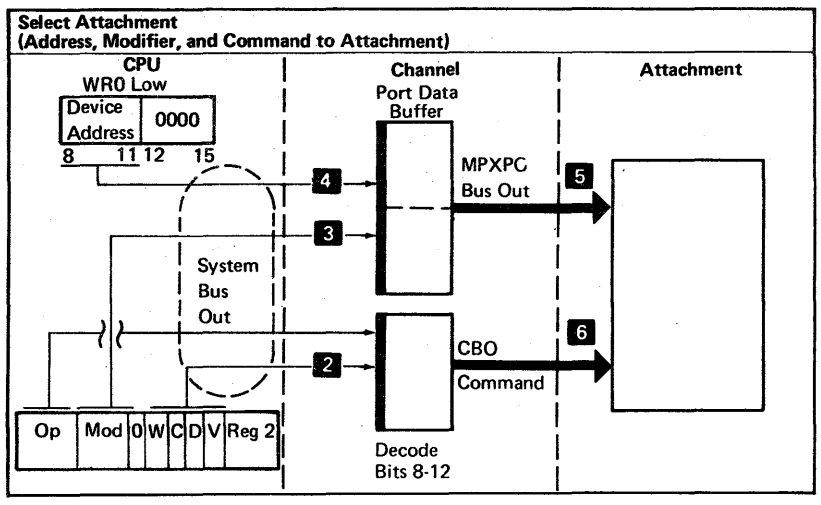
CP Storage Control Card A-A1F2

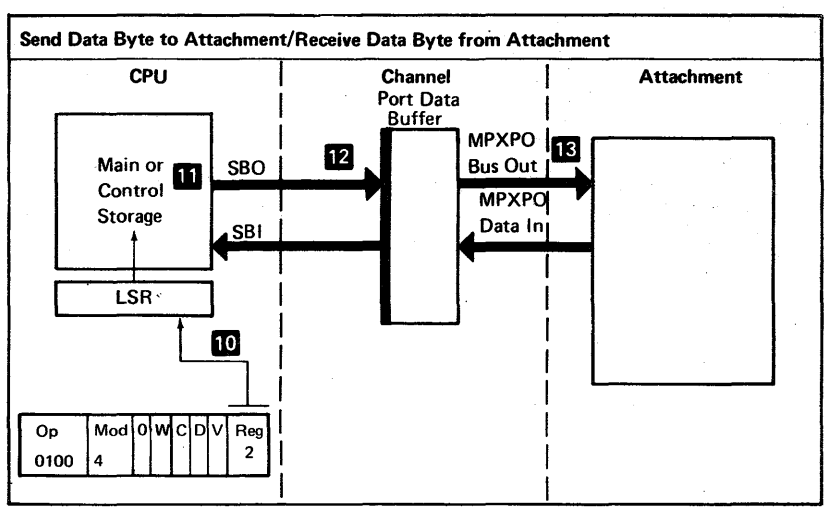


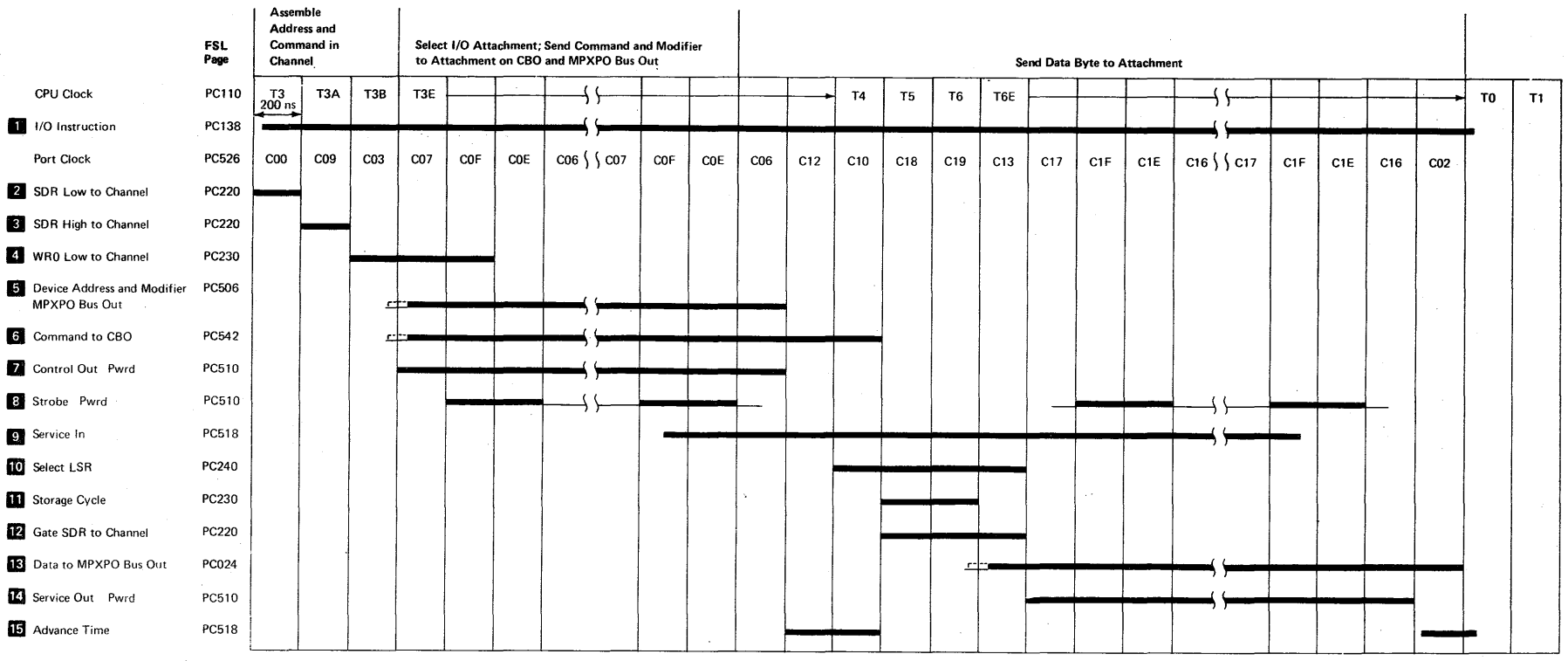
CP Port Card A-A1L2

5

I/O Storage (Sense–Big Picture)

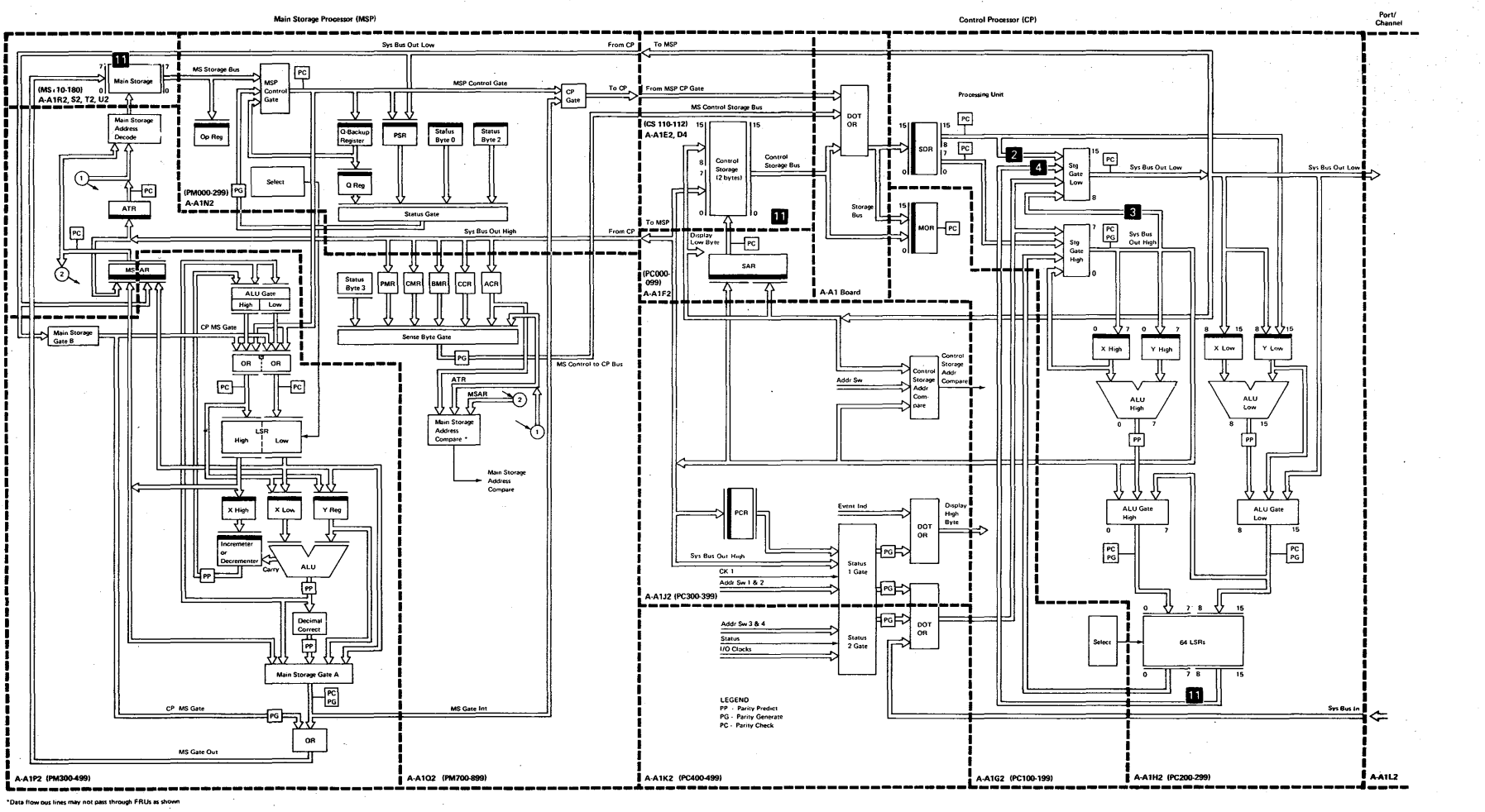




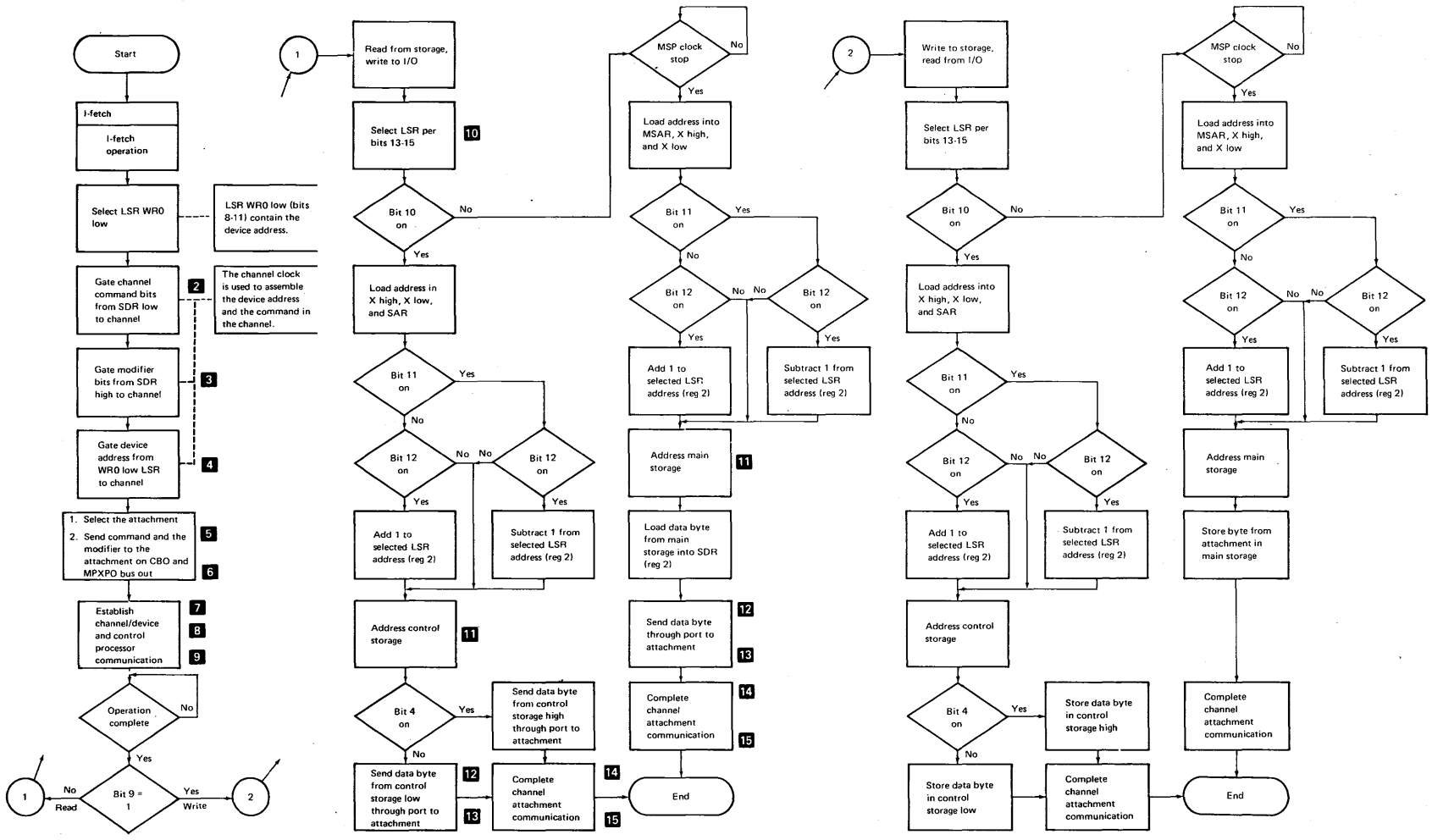


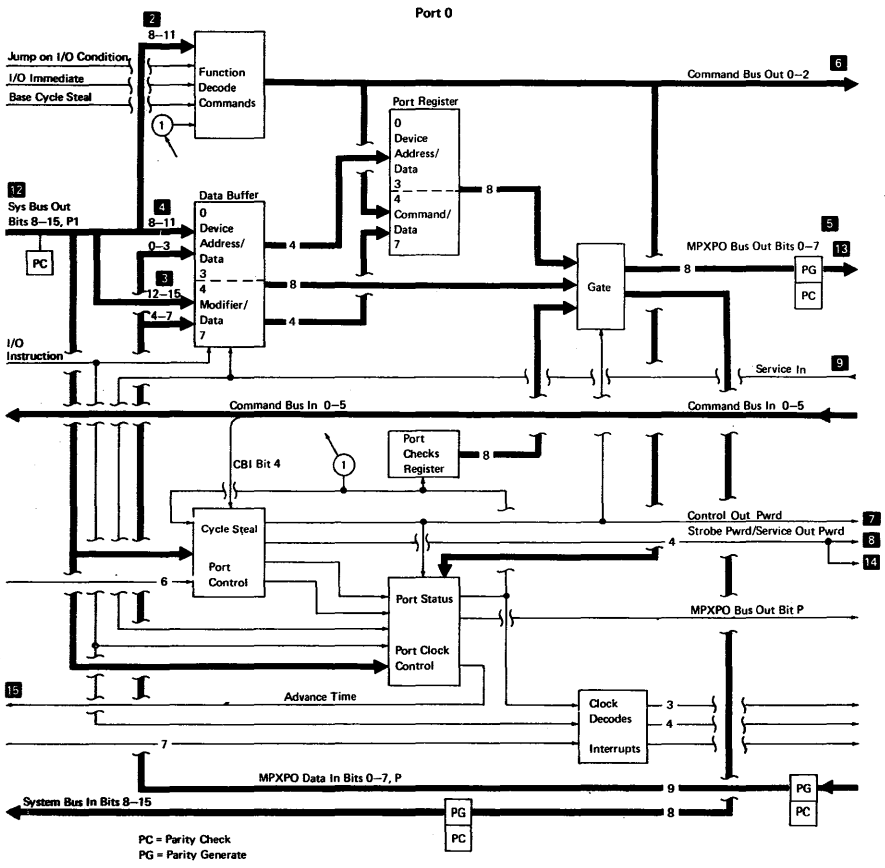
The first 'strobe pwrd' pulse after the rise of the 'control out pwrd' line signals the I/O attachment that the device address and the command information on the 'command bus out' and the 'MPXPO bus out' lines are valid.

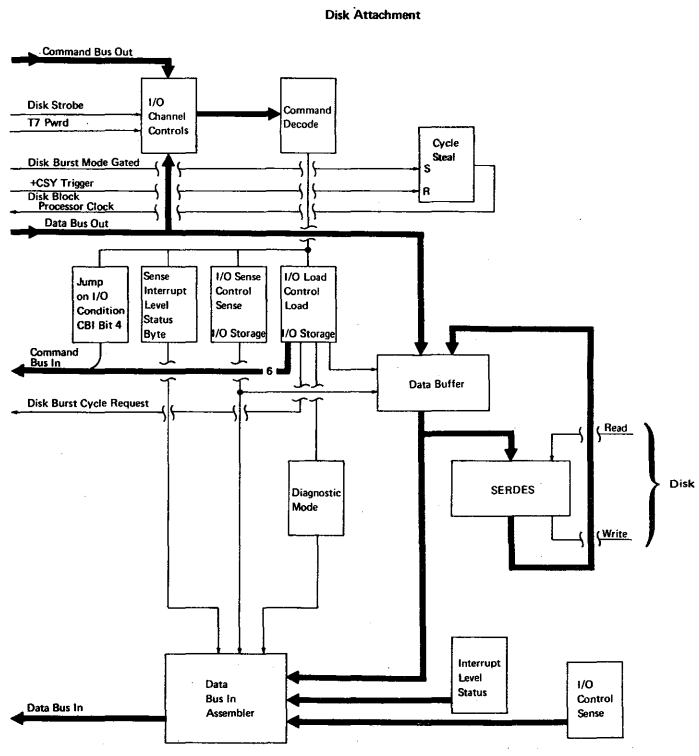
The rise of the 'service in' line signals the port that the I/O attachment has taken the information from the 'command bus out' and 'MPXPO bus out' lines. The rise of the 'service in' line also signals the port that the data byte on the 'MPXPO data in' lines is valid. The rise of the 'service out pwrd' line signals the I/O attachment that the channel has taken the byte from the 'MPXPO data in' lines.



*Data flow bus lines may not pass through FRUs as shown

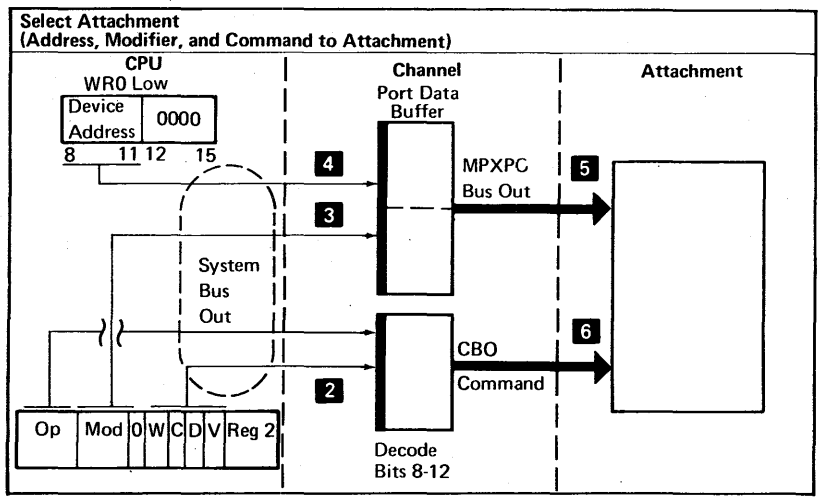

Start
I-fetch
I-fetch operation
Select LSR WR0 low
LSR WR0 low (bits 8-11) contain the device address.
Gate channel command bits from SDR low to channel
The channel clock is used to assemble the device address and the command in the channel.
Gate modifier bits from SDR high to channel
Gate device address from WR0 low LSR to channel
1. Select the attachment
2. Send command and the modifier to the attachment on CBO and MPXPO bus out
Establish channel/device and control processor communication
Operation complete
No
Yes
Bit 9 = 1
No Read
Yes Write
1
2
Read from storage, write to I/O
Select LSR per bits 13-15
Bit 10 on
No
Yes
Load address in X high, X low, and SAR
Bit 11 on
Yes
No
Bit 12 on
No
No
Bit 12 on
Yes
Add 1 to selected LSR address (reg 2)
Subtract 1 from selected LSR address (reg 2)
Address control storage
Bit 4 on
Yes
No
Send data byte from control storage high through port to attachment
Send data byte from control storage low through port to attachment
Complete channel attachment communication
MSP clock stop
No
Yes
Load address into MSAR, X high, and X low
Bit 11 on
Yes
No
Bit 12 on
No
No
Bit 12 on
Yes
Add 1 to selected LSR address (reg 2)
Subtract 1 from selected LSR address (reg 2)
Address main storage
Load data byte from main storage into SDR (reg 2)
Send data byte through port to attachment
Complete channel attachment communication
End
Write to storage, read from I/O
Select LSR per bits 13-15
Bit 10 on
No
Yes
Load address into X high, X low, and SAR
Bit 11 on
Yes
No
Bit 12 on
No
No
Bit 12 on
Yes
Add 1 to selected LSR address (reg 2)
Subtract 1 from selected LSR address (reg 2)
Address control storage
Bit 4 on
Yes
No
Store data byte in control storage high
Store data byte in control storage low
Complete channel attachment communication
MSP clock stop
No
Yes
Load address into MSAR, X high, and X low
Bit 11 on
Yes
No
Bit 12 on
No
No
Bit 12 on
Yes
Add 1 to selected LSR address (reg 2)
Subtract 1 from selected LSR address (reg 2)
Address main storage
Store byte from attachment in main storage
Complete channel attachment communication
End

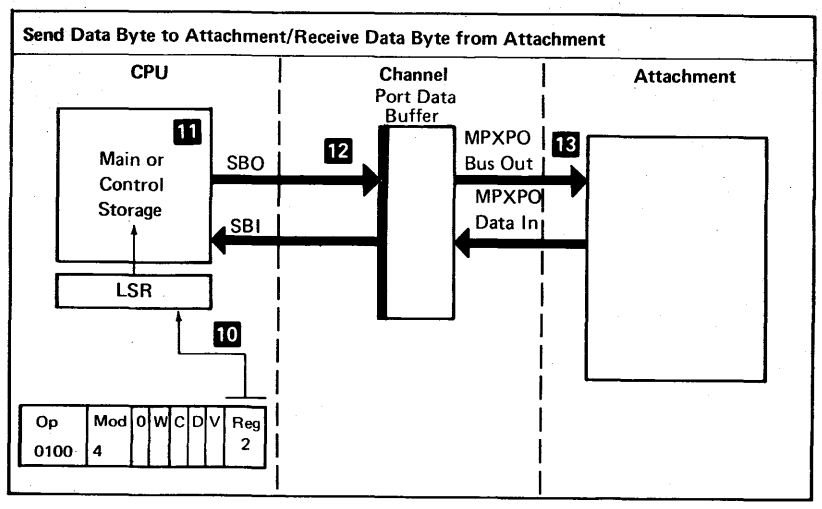

Port 0
Jump on I/O Condition
I/O Immediate
Base Cycle Steal
Function Decode Commands
Command Bus Out 0–2
Port Register
0
Device Address/ Data
3
4
Command/ Data
7
Sys Bus Out Bits 8–15, P1
PC
Data Buffer
0
Device Address/ Data
3
4
Modifier/ Data
7
8–11
0–3
12–15
4–7
Gate
MPXPO Bus Out Bits 0–7
PG
PC
I/O Instruction
Service In
Command Bus In 0–5
Command Bus In 0–5
CBI Bit 4
Port Checks Register
Cycle Steal
Port Control
Control Out Pwrd
Strobe Pwrd/Service Out Pwrd
Port Status
Port Clock Control
MPXPO Bus Out Bit P
Advance Time
Clock Decodes
Interrupts
MPXPO Data In Bits 0–7, P
System Bus In Bits 8–15
PG
PC
PC = Parity Check
PG = Parity Generate

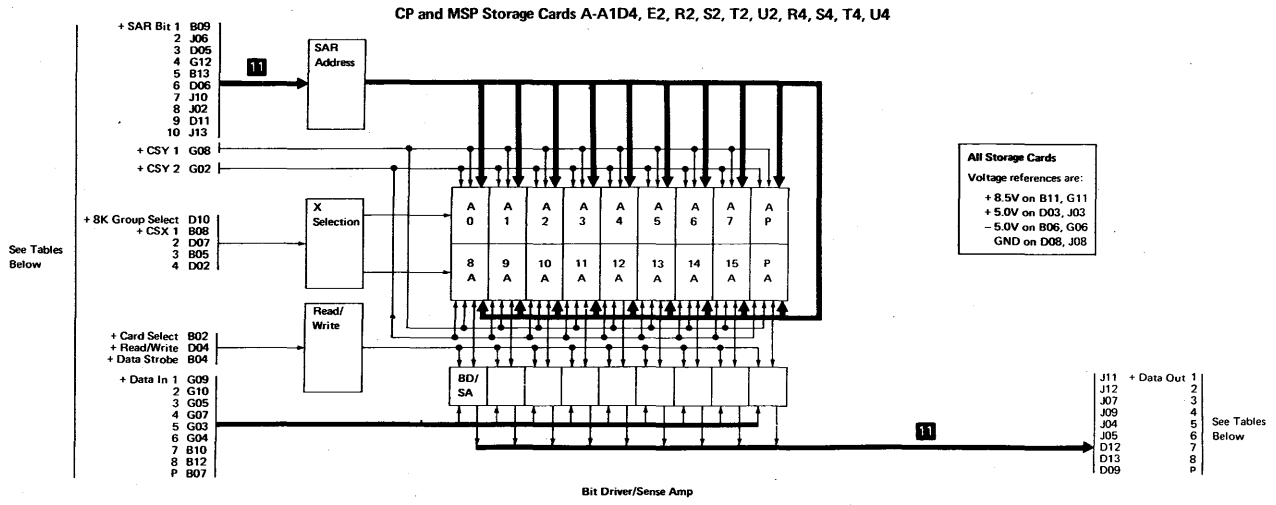

Disk Attachment
Command Bus Out
Disk Strobe
T7 Pwrd
I/O Channel Controls
Command Decode
Cycle Steal
S
R
Disk Burst Mode Gated
+CSY Trigger
Disk Block Processor Clock
Data Bus Out
Jump on I/O Condition CBI Bit 4
Sense Interrupt Level Status Byte
I/O Sense Control Sense
I/O Storage
I/O Load Control Load
I/O Storage
Command Bus In
Data Buffer
Disk Burst Cycle Request
Diagnostic Mode
SERDES
Read
Write
Disk
Data Bus In Assembler
Interrupt Level Status
I/O Control Sense
Data Bus In

5

I/O Storage (Sense-Detail)



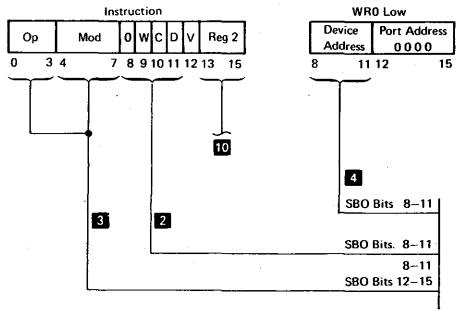




All Storage Cards

Voltage references are:

+8.5V on B11, G11
+5.0V on D03, J03
−5.0V on B06, G06
GND on D08, J08



Card →	A1E2			A1D4			A1R2, T2, R4, T4		A1S2, U2, S4, U4	
+ Card Select	F2 B11	+ CS Card Select 0–16K	F2 B11	+ CS Card Select 0–16K	-		+ MS Card Select 0	-	+ MS Card Select 0	
+ Read/Write	F2 D05	+ CS Write Pulse Hi	F2 D06	+ CS Write Pulse Lo	Q2 S10		+ MS Write Pulse Lo	Q2 S11	+ MS Write Pulse Hi	
+ Data Strobe		+ Board Tieup		+ Board Tieup	Q2 S03		+ MS Data Strobe Lo	Q2 S04	+ MS Data Strobe Hi	
+ 8K Group Select	F2 J02	+ 8K Group Select	F2 J02	+ 8K Group Select	Q2 U09		− MS 8K Group Select Lo	Q2 U09	− MS 8K Group Select Lo	

*Card ↓	+ Card Select		ATR 0 to 3
A1R2, S2	Q2U11	+ MS Card Select 0–32K	0000
A1T2, U2	Q2U12	+ MS Card Select 32–64K	0001
A1R4, S4	Q2U13	+ MS Card Select 64–96K	0010
A1T4, U4	Q2S13	+ MS Card Select 96–128K	0011

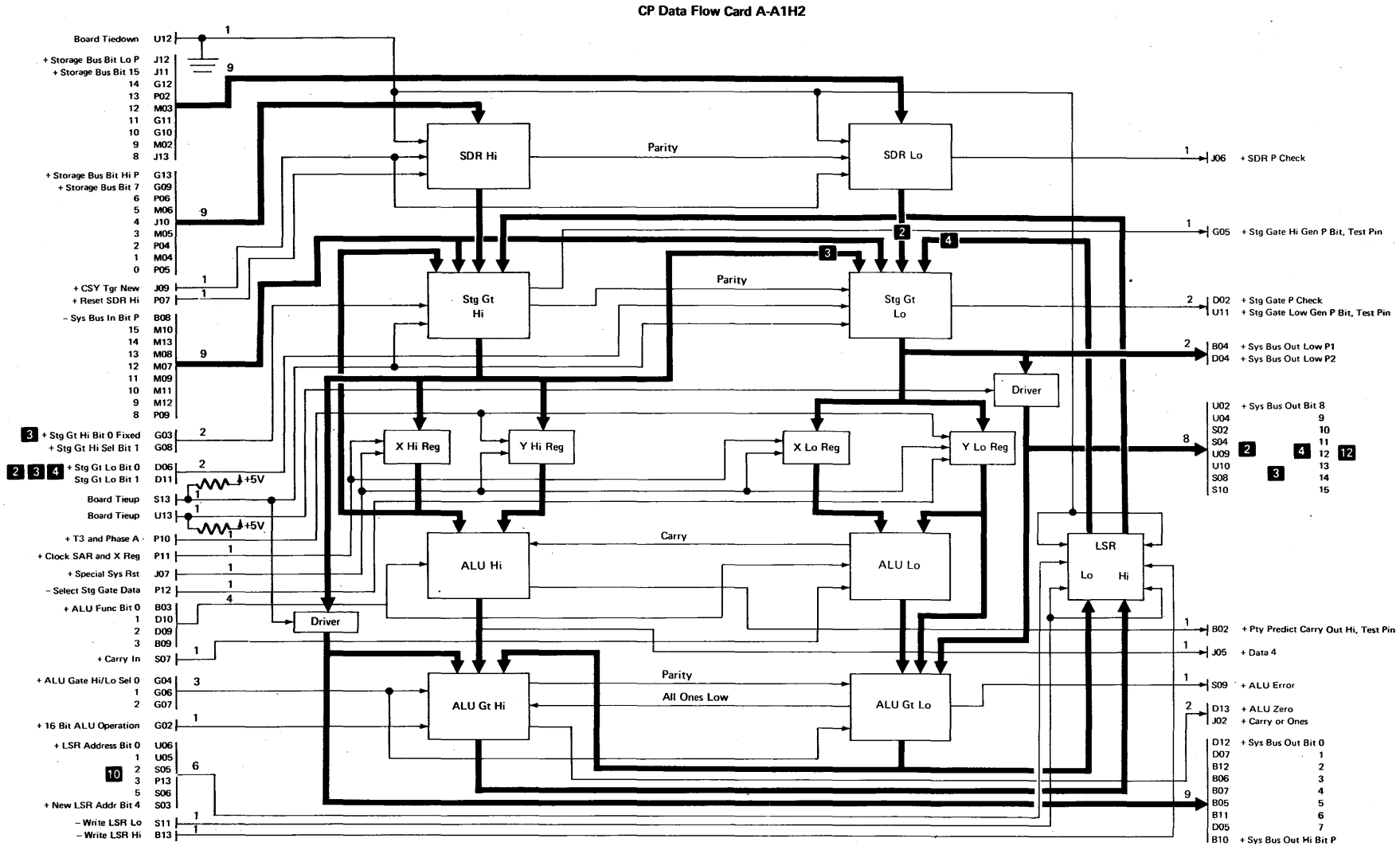
Card →	A1E2			A1D4			A1R2, S2, T2, U2, R4, S4, T4, U4		
+ Data Out 1	G2 J11	+ Storage Bus Bit	0	G2 G12	+ Storage Bus Bit	8	N2 G02	+ MS Storage Bus Bit	8
2	G2 P07		1	G2 P06		9	N2 G03		9
3	G2 J13		2	G2 P02		10	N2 G04		10
4	G2 P09		3	G2 J12		11	N2 J05		11
5	G2 G11		4	G2 M02		12	N2 J07		12
6	G2 G13		5	G2 P04		13	N2 G08		13
7	G2 M04		6	G2 P05		14	N2 J02		14
8	G2 M03		7	G2 M05		15	N2 G09		15
P	G2 G09		P Hi	G2 G02	-	Lo P	N2 J06		P
+ Data In 1	H2 D12	+ System Bus Out	0	H2 U04	+ System Bus Out Lo	8	P2 J02	+ MS Gt Out Bit	8
2	H2 D07		1	H2 U04		9	P2 J04		9
3	H2 B12		2	H2 S02		10	P2 G07		10
4	H2 B06		3	H2 S04		11	P2 J07		11
5	H2 B07		4	H2 U09		12	P2 G02		12
6	H2 B05		5	H2 U10		13	P2 G03		13
7	H2 B11		6	H2 S08		14	P2 G04		14
8	H2 D05		7	H2 S10		15	P2 G06		15
P	H2 B10	+ System Bus Out Hi Bit	P	H2 D04	+ Sys Bus Out Lo	P2	P2 B09		P

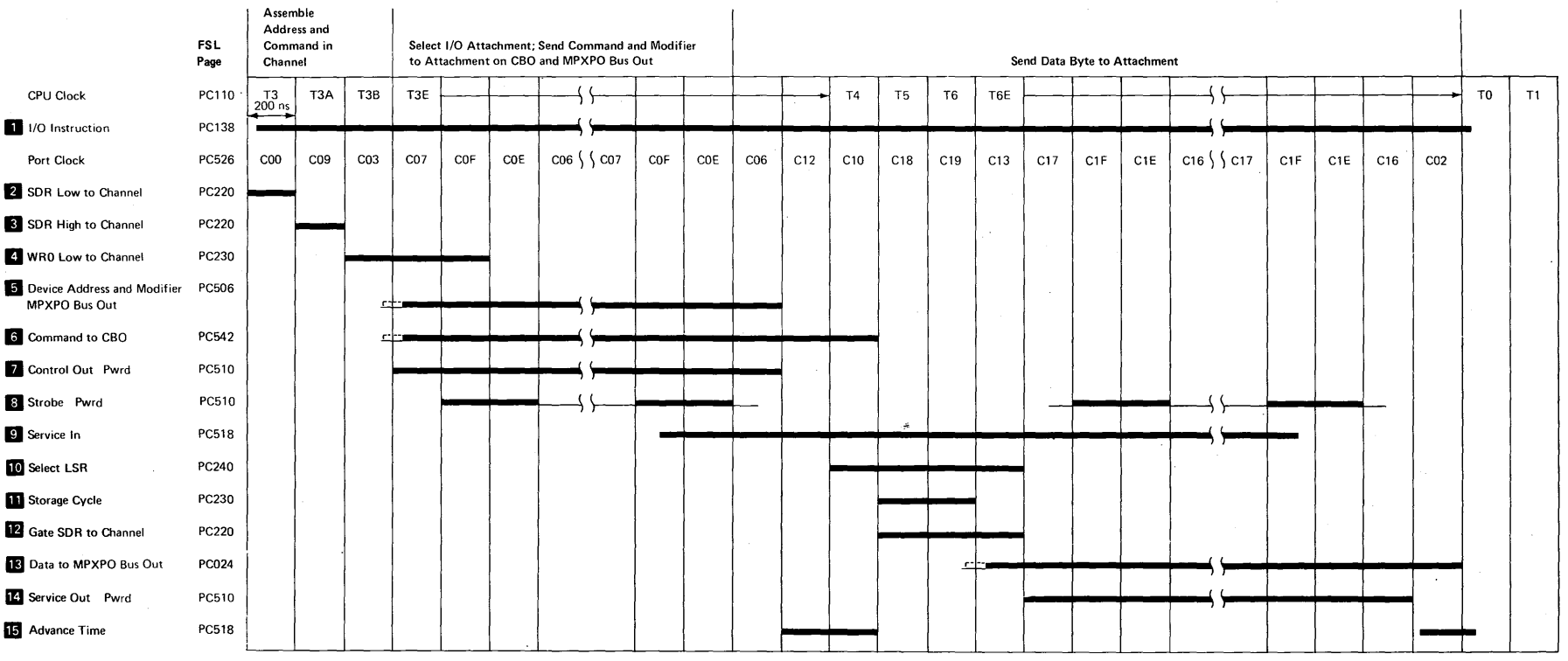
Card →	A1E2 & A1D4		A1R2,S2,T2,U2,R4,S4,T4,U4	
+ SAR Bit 1	F2 U07	+ SAR Bit 6	Q2 S06	+ MSAR Bit 6
2	F2 M12	7	Q2 S07	7
3	F2 U10	8	P2 B06	8
4	F2 S06	9	P2 B03	9
5	F2 P13	10	P2 B02	10
6	F2 M13	11	P2 B07	11
7	F2 P06	12	P2 D07	12
8	F2 U12	13	P2 D05	13
9	F2 U13	14	P2 B08	14
10	F2 M11	15	P2 D09	15
+ CSX 1	F2 B13	+ CSX 1	Q2 U04	+ MS CSX 1
2	F2 B08	2	Q2 U05	2
3	F2 B07	3	Q2 U06	3
4	F2 B06	4	Q2 U07	4
+ CSY 1	F2 D11	+ CSY 1	Q2 S08	+ MS CSY 1
2	F2 D07	2	Q2 S09	2

Storage Gate High		
Bit 0	Bit 1	Register Gated Thru
0	0	LSR High
0	1	SDR High
1	0	SBI Bits 8–15
1	1	X Reg High Bits 0–3 SDR Bits 4–7 Stg Gate High Bit P

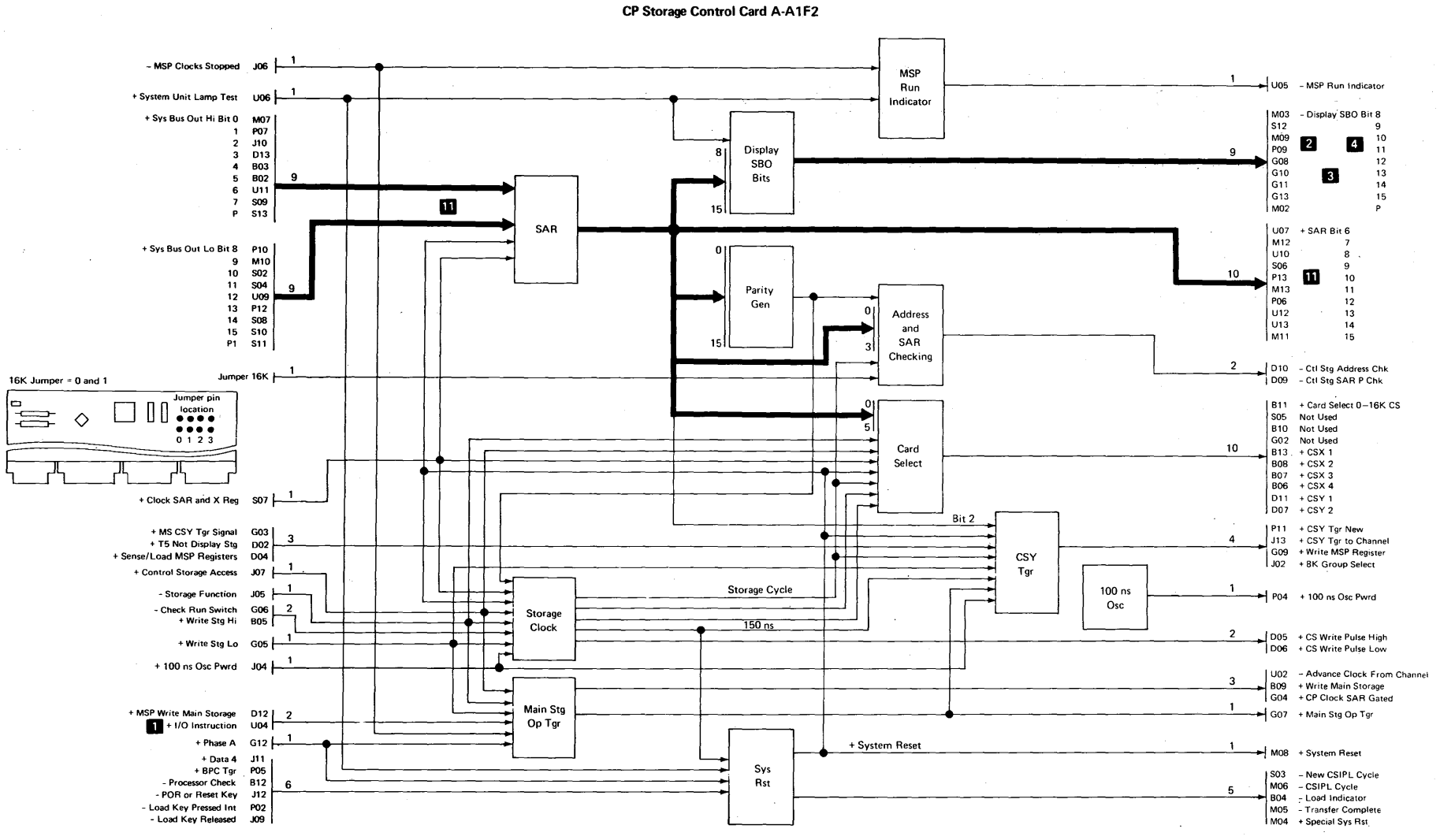
Storage Gate Low		
Bit 0	Bit 1	Register Gated Thru
0	0	LSR Low
0	1	SDR Low
1	0	SBI Bits 8–15
1	1	Output Stg Gate High

CP Data Flow Card A-A1H2

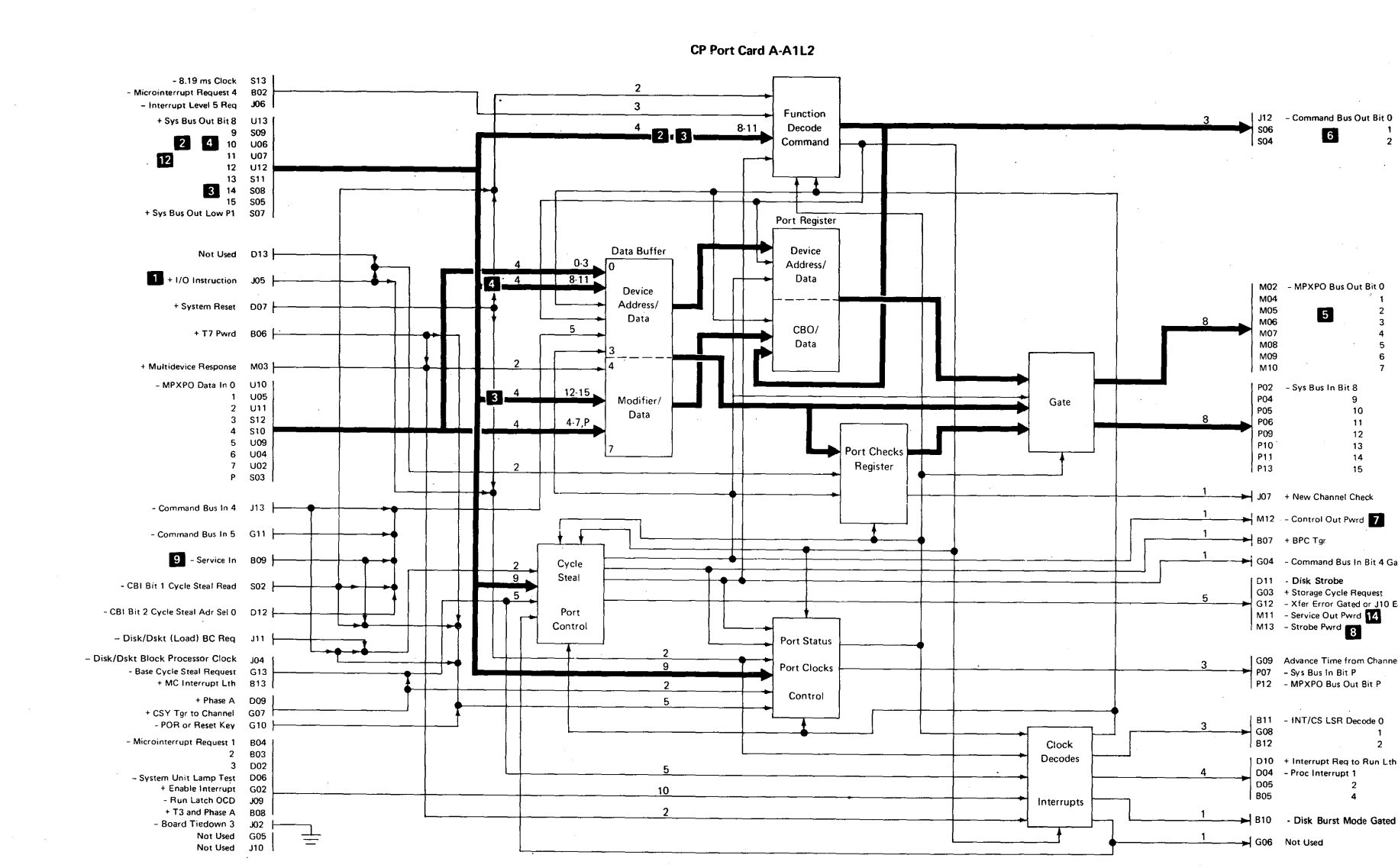




CP Storage Control Card A-A1F2



CP Port Card A-A1L2



5

Jump on I/O Condition (JIO)

0	0	1	1	Modifier	Page Address
0			3	4 7	8 15

This instruction tests I/O conditions. If the condition tested is active, this instruction causes a jump to the address specified by the page address (bits 8-15). If the condition tested is not active, the next sequential instruction is executed.

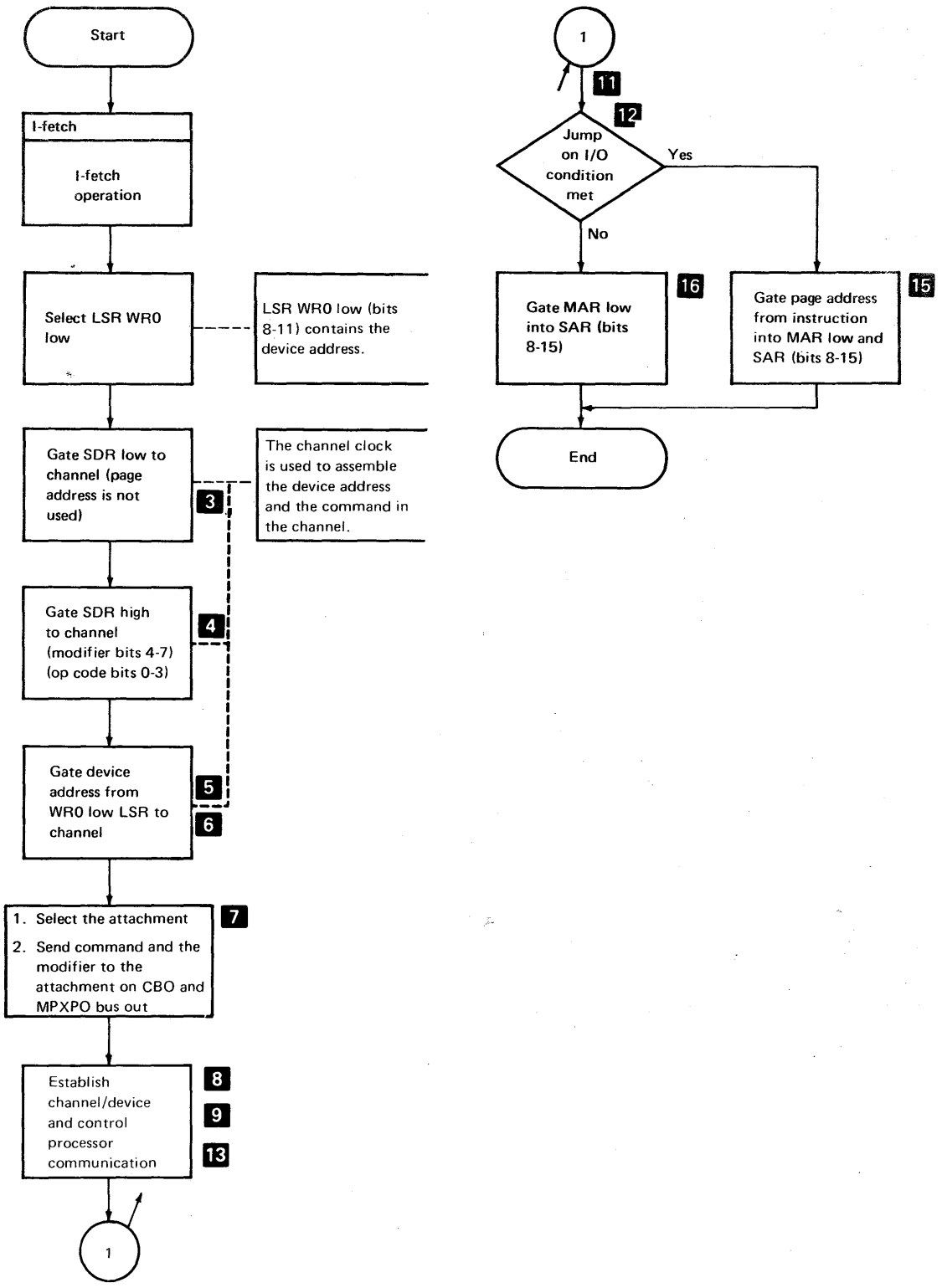
The operation code (bits 0-3) is sent to the port where the bits are decoded as a jump-on-I/O-condition command. This command is then sent to the I/O attachment through the port.

Modifier (Bits 4-7): Specifies the control field for the I/O devices. The I/O device being used determines how this field is used. The modifier field is moved to the I/O attachment through the port.

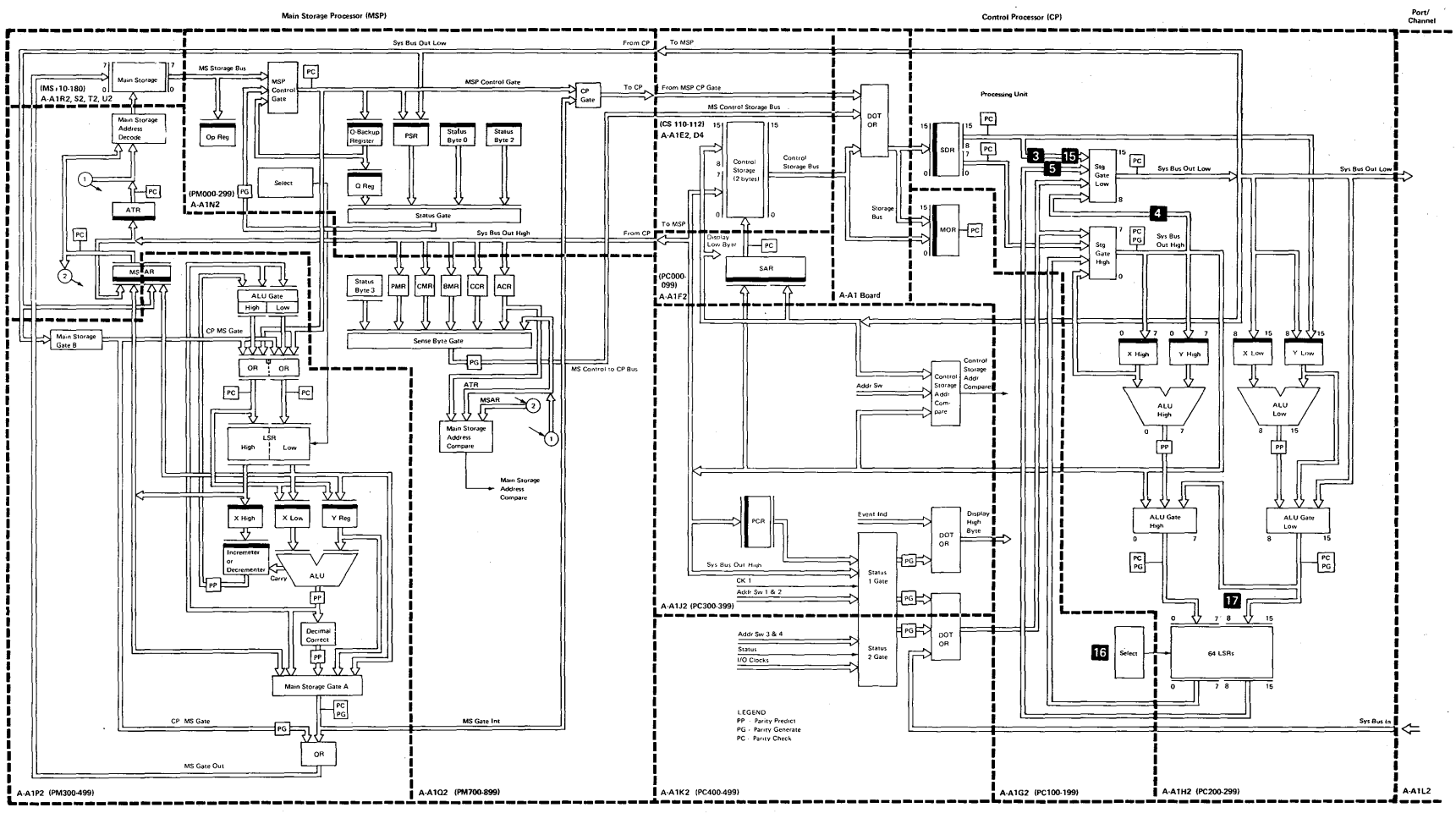
Some of the modifier combinations make a common code for those conditions that are used by most I/O attachments. The modifier usage is specified as follows:

Modifier Field Setting 4 5 6 7	Description
0 0 0 0	Adapter check
0 0 0 1	Adapter not ready
0 0 1 0	Busy condition 1
0 0 1 1	Busy condition 2
0 1 0 0	Interrupt enabled
0 1 0 1	Diagnostic real
0 1 1 0	Diagnostic not real
0 1 1 1 through 1 1 1 1	Available for I/O attachment needs

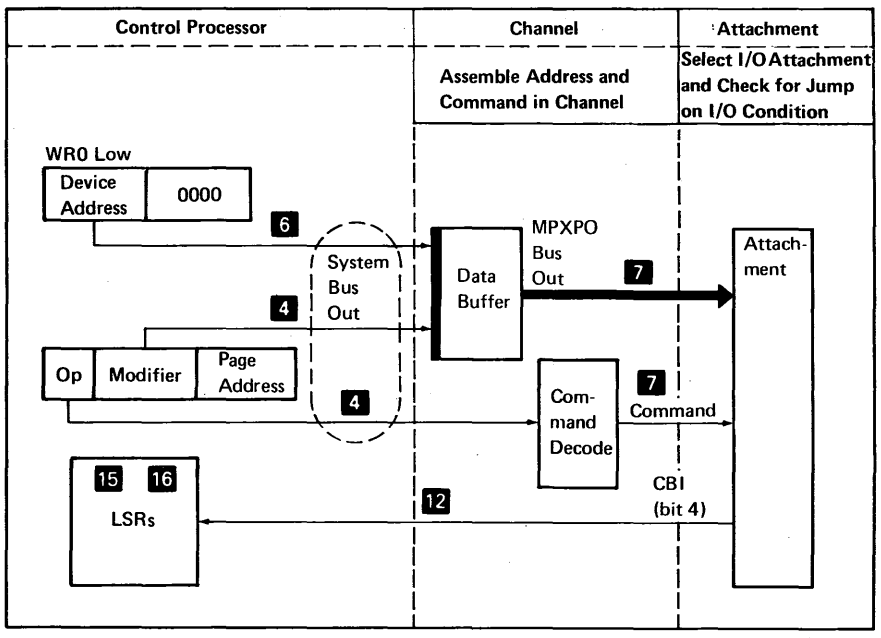
Page Address (Bits 8-15): Permits a jump inside a page boundary (256-word limit of hex 00 through hex FF) in control storage only. The page address must be located on the same page boundary as the jump on I/O condition. This field replaces the 8 low-order bits in the microaddress register if the I/O device indicates that the jump condition is met. The 'CBI bit 4' port line determines if the I/O condition is met.

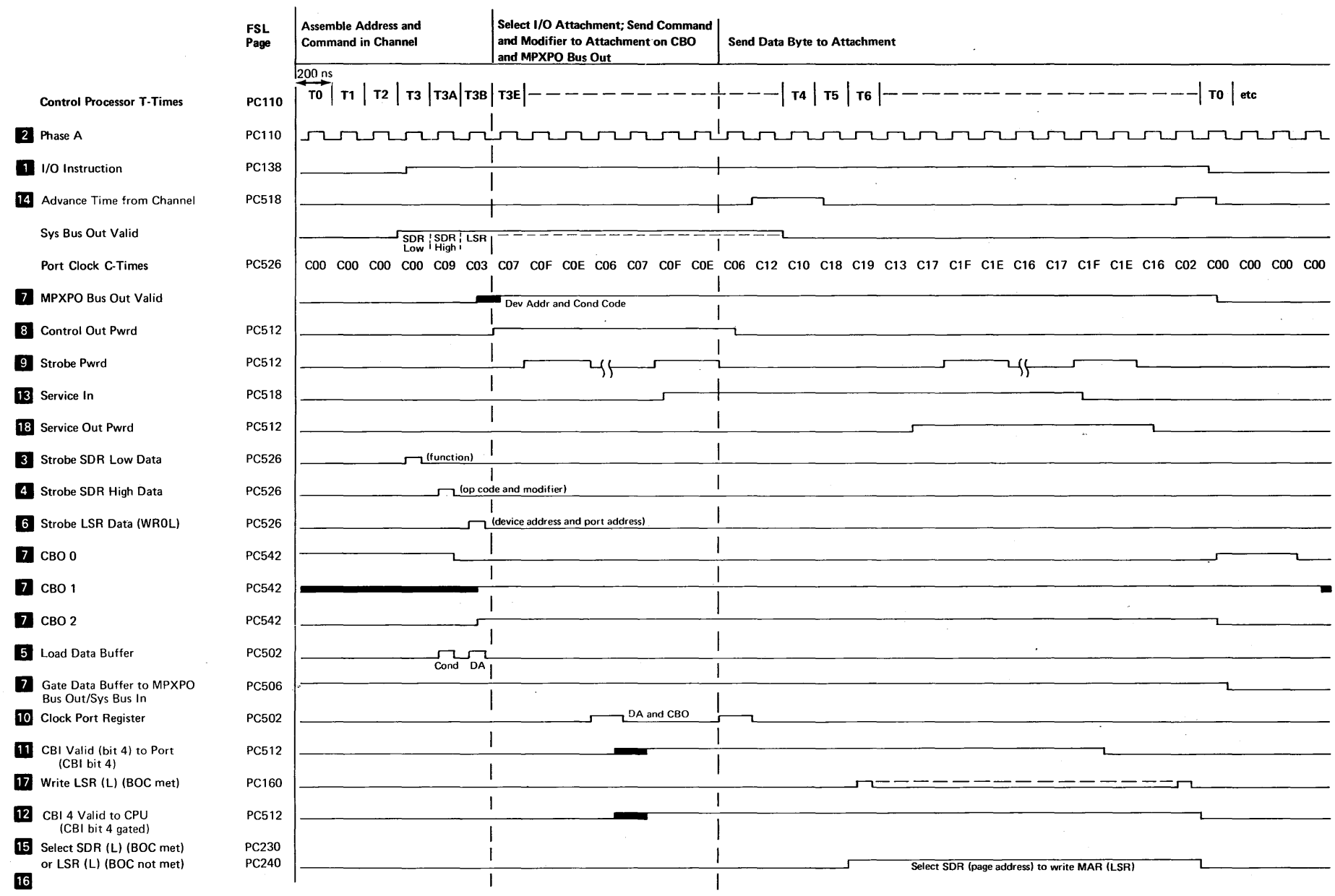


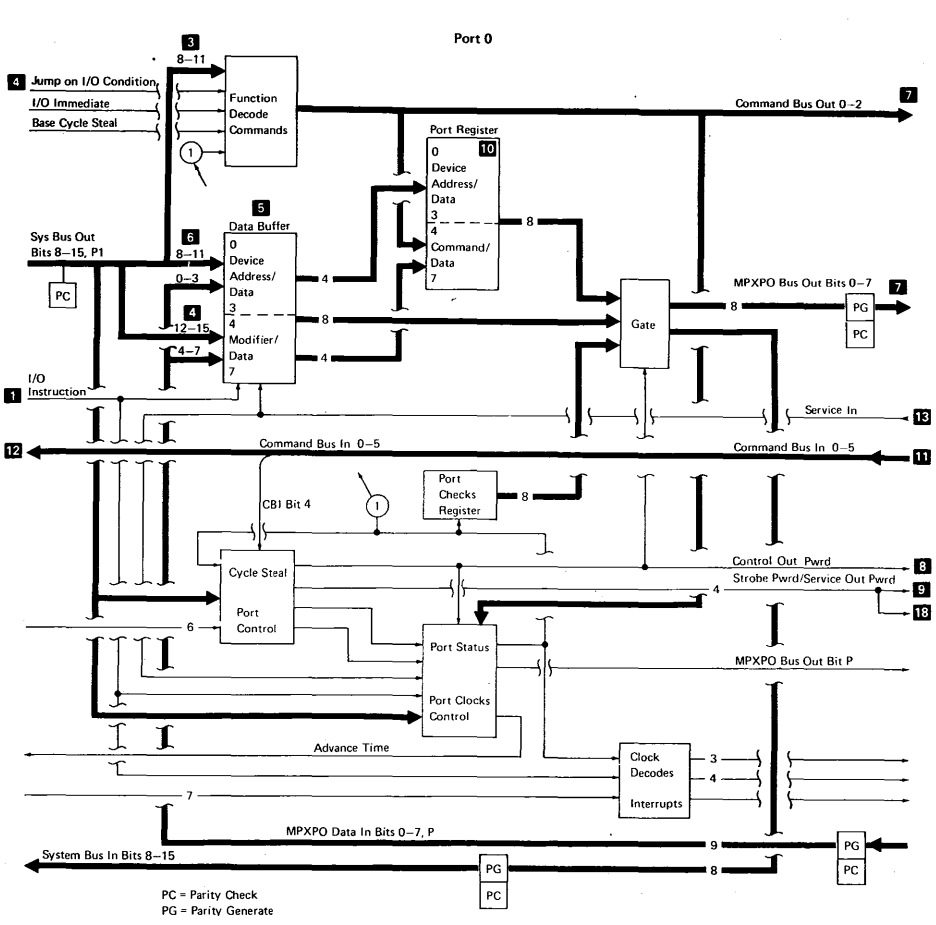
Jump on I/O Condition (Big Picture)

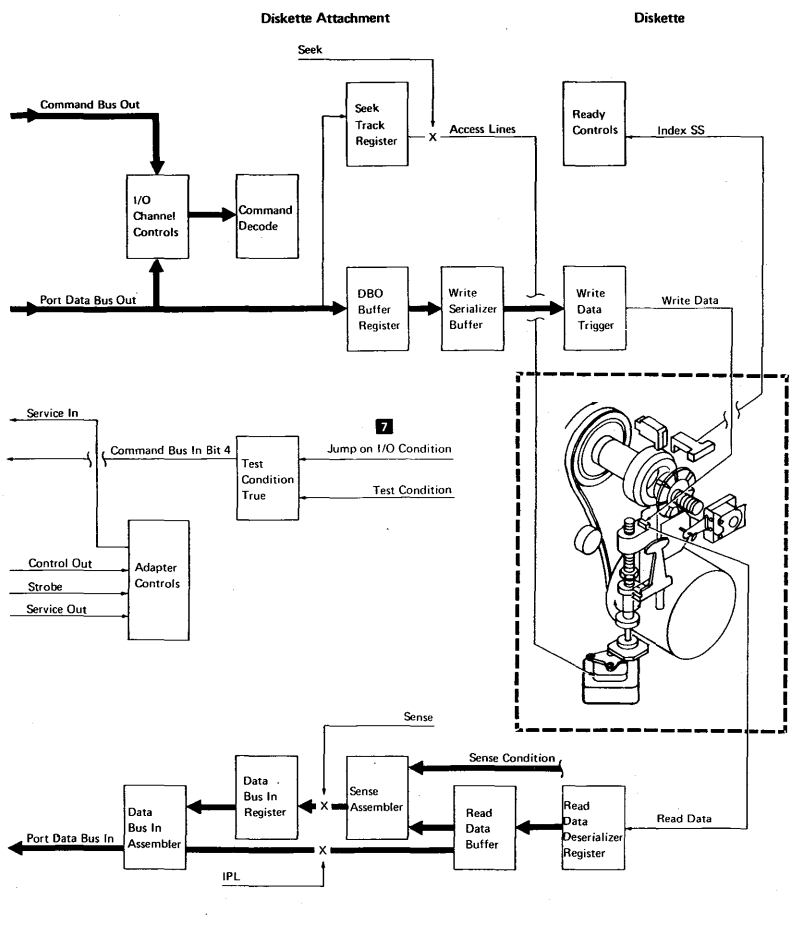


*Data flow bus lines may not pass through FRUs as shown


Control Processor
Channel
Attachment
Assemble Address and Command in Channel
Select I/O Attachment and Check for Jump on I/O Condition
WR0 Low
Device Address
0000
6
System Bus Out
4
Op
Modifier
Page Address
4
Data Buffer
MPXPO Bus Out
7
Attach-ment
Com-mand Decode
7
Command
15
16
LSRs
12
CBI (bit 4)

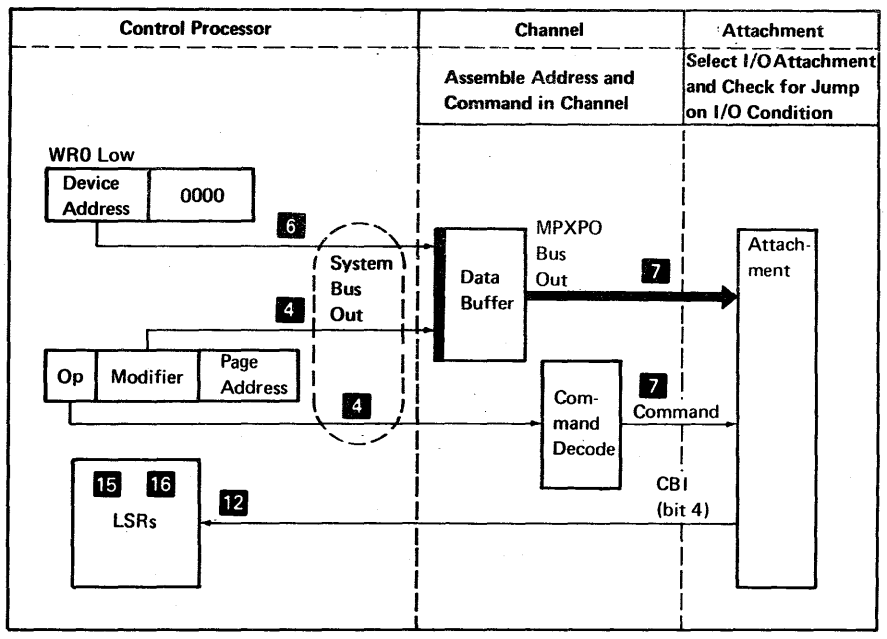

FSL Page
Assemble Address and Command in Channel
Select I/O Attachment; Send Command and Modifier to Attachment on CBO and MPXPO Bus Out
Send Data Byte to Attachment
200 ns
Control Processor T-Times
PC110
T0 T1 T2 T3 T3A T3B T3E T4 T5 T6 T0 etc
2 Phase A
PC110
1 I/O Instruction
PC138
14 Advance Time from Channel
PC518
Sys Bus Out Valid
PC518
SDR Low
SDR High
LSR
Port Clock C-Times
PC526
C00 C00 C00 C00 C09 C03 C07 C0F C0E C06 C07 C0F C0E C06 C12 C10 C18 C19 C13 C17 C1F C1E C16 C17 C1F C1E C16 C02 C00 C00 C00 C00
7 MPXPO Bus Out Valid
Dev Addr and Cond Code
8 Control Out Pwrd
PC512
9 Strobe Pwrd
PC512
13 Service In
PC518
18 Service Out Pwrd
PC512
3 Strobe SDR Low Data
PC526
(function)
4 Strobe SDR High Data
PC526
(op code and modifier)
6 Strobe LSR Data (WR0L)
PC526
(device address and port address)
7 CBO 0
PC542
7 CBO 1
PC542
7 CBO 2
PC542
5 Load Data Buffer
PC502
Cond
DA
7 Gate Data Buffer to MPXPO Bus Out/Sys Bus In
PC506
10 Clock Port Register
PC502
DA and CBO
11 CBI Valid (bit 4) to Port (CBI bit 4)
PC512
17 Write LSR (L) (BOC met)
PC160
12 CBI 4 Valid to CPU (CBI bit 4 gated)
PC512
15 Select SDR (L) (BOC met) or LSR (L) (BOC not met)
PC230
PC240
Select SDR (page address) to write MAR (LSR)
16


Port 0
3
8–11
4 Jump on I/O Condition
I/O Immediate
Base Cycle Steal
Function Decode Commands
1
Command Bus Out 0–2
7
Port Register
0 Device Address/ Data 3
4 Command/ Data 7
10
8
5
Data Buffer
Sys Bus Out Bits 8–15, P1
6
8–11
PC
0–3
4
12–15
4–7
0 Device Address/ Data 3
4 Modifier/ Data 7
4
8
4
Gate
MPXPO Bus Out Bits 0–7
8
PG
PC
7
I/O Instruction
1
Service In
13
12
Command Bus In 0–5
Command Bus In 0–5
11
CBI Bit 4
1
Port Checks Register
8
Cycle Steal
Port Control
6
Control Out Pwrd
8
Strobe Pwrd/Service Out Pwrd
4
9
18
Port Status
Port Clocks Control
MPXPO Bus Out Bit P
Advance Time
Clock Decodes
Interrupts
3
4
7
MPXPO Data In Bits 0–7, P
9
System Bus In Bits 8–15
PG
8
PC
PC = Parity Check
PG = Parity Generate

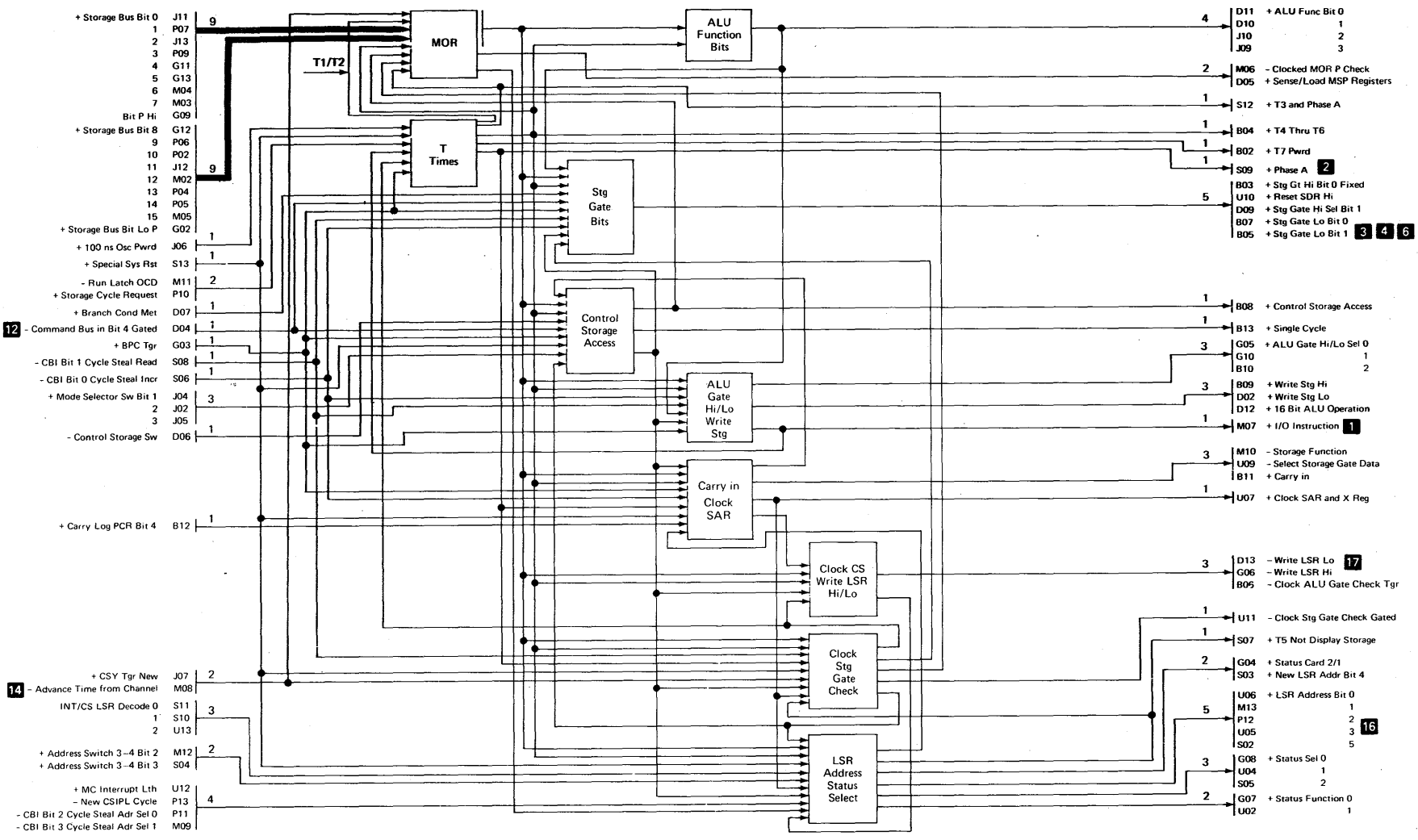

Diskette Attachment
Diskette
Seek
Command Bus Out
Seek Track Register
X
Access Lines
Ready Controls
Index SS
I/O Channel Controls
Command Decode
Port Data Bus Out
DBO Buffer Register
Write Serializer Buffer
Write Data Trigger
Write Data
Service In
Command Bus In Bit 4
Test Condition True
7
Jump on I/O Condition
Test Condition
Control Out
Strobe
Service Out
Adapter Controls
Sense
Sense Condition
Data Bus In Register
Sense Assembler
Read Data Buffer
Read Data Deserializer Register
Read Data
Data Bus In Assembler
Port Data Bus In
X
IPL

5

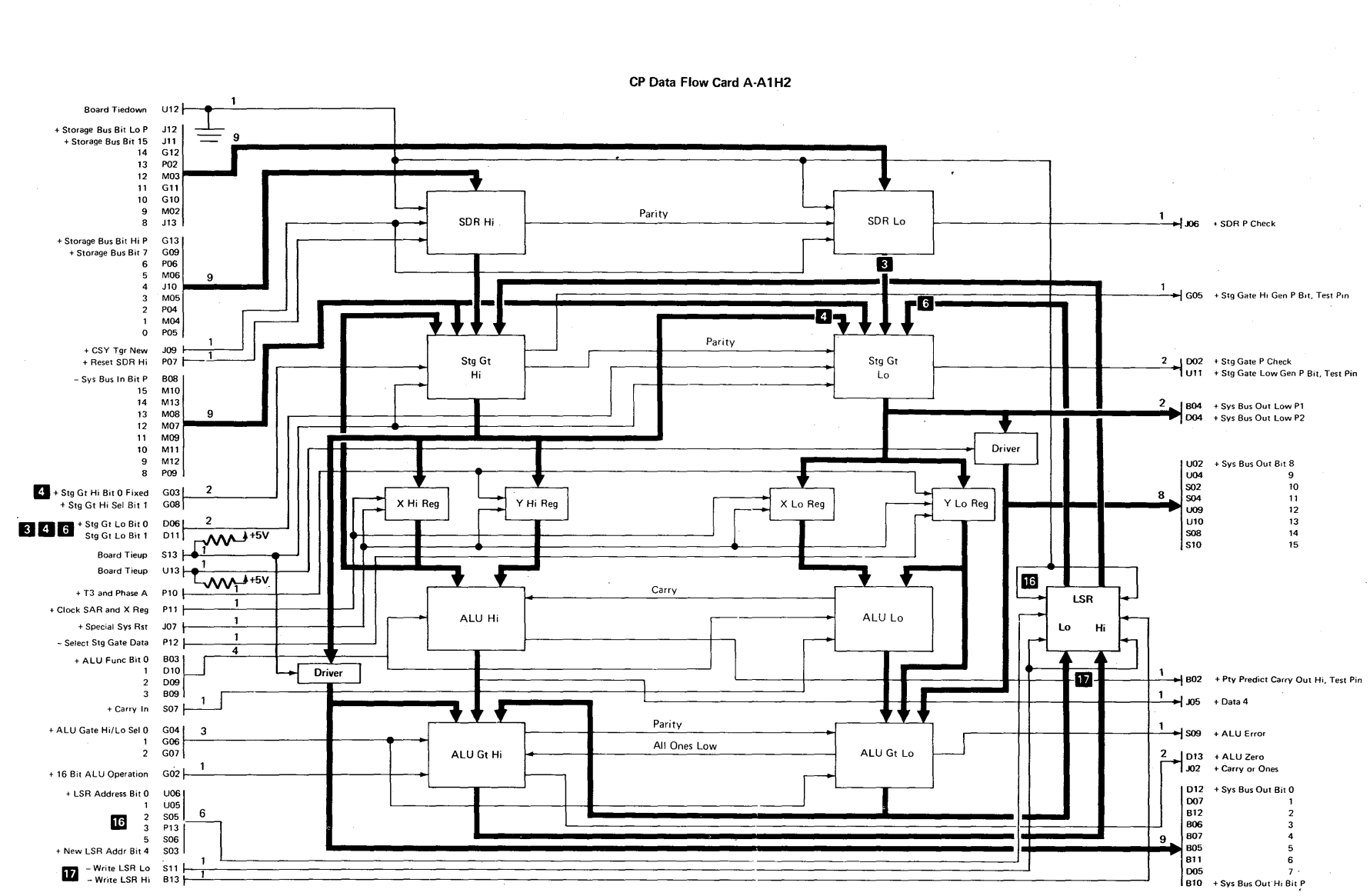
Jump on I/O Condition (Detail)

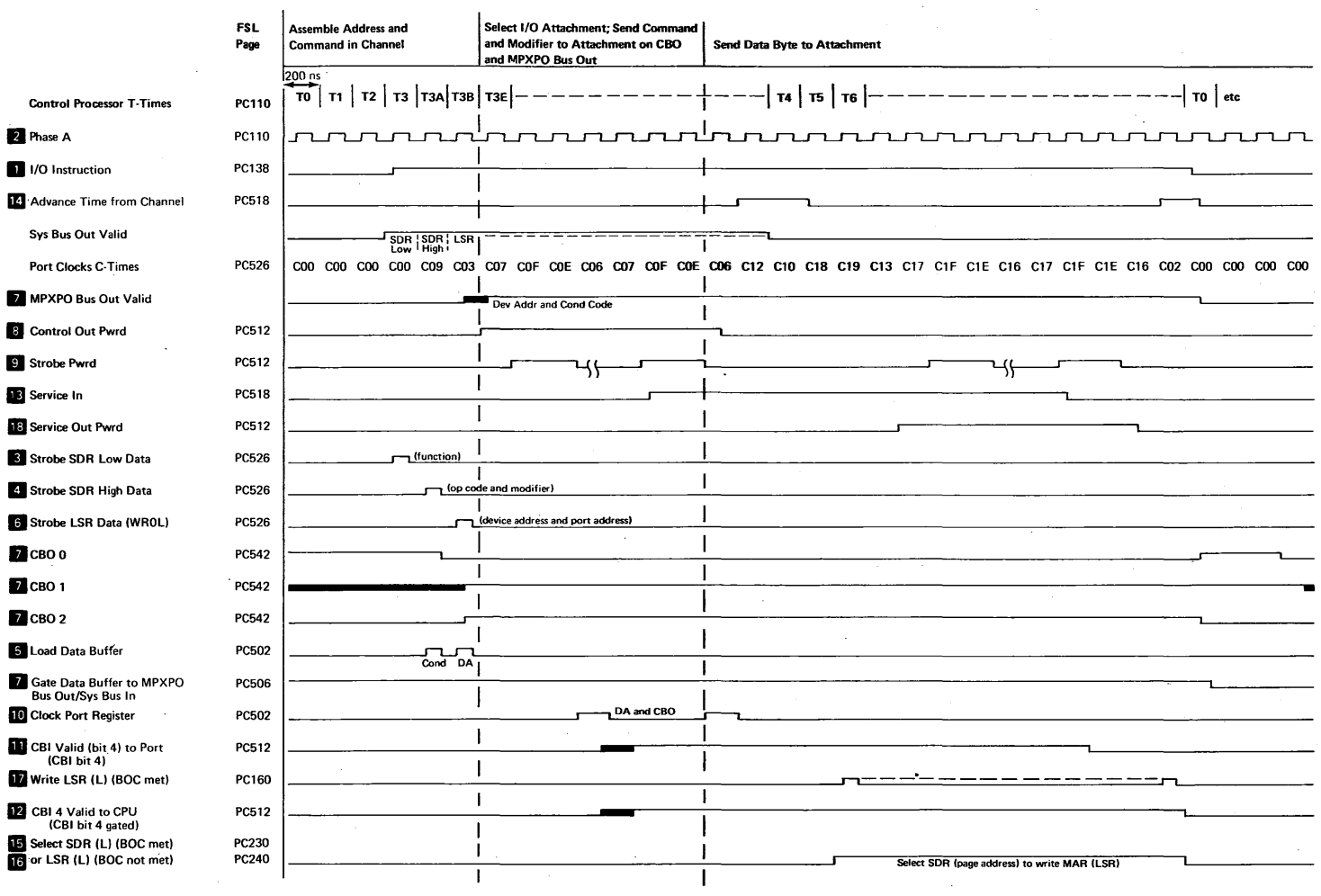


CP System Control Card A-A1G2

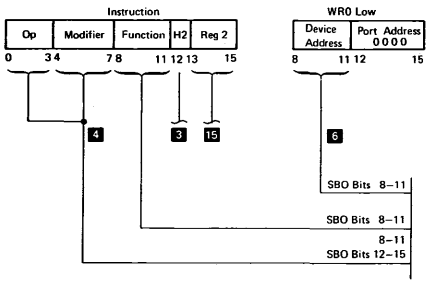


CP Data Flow Card A-A1H2

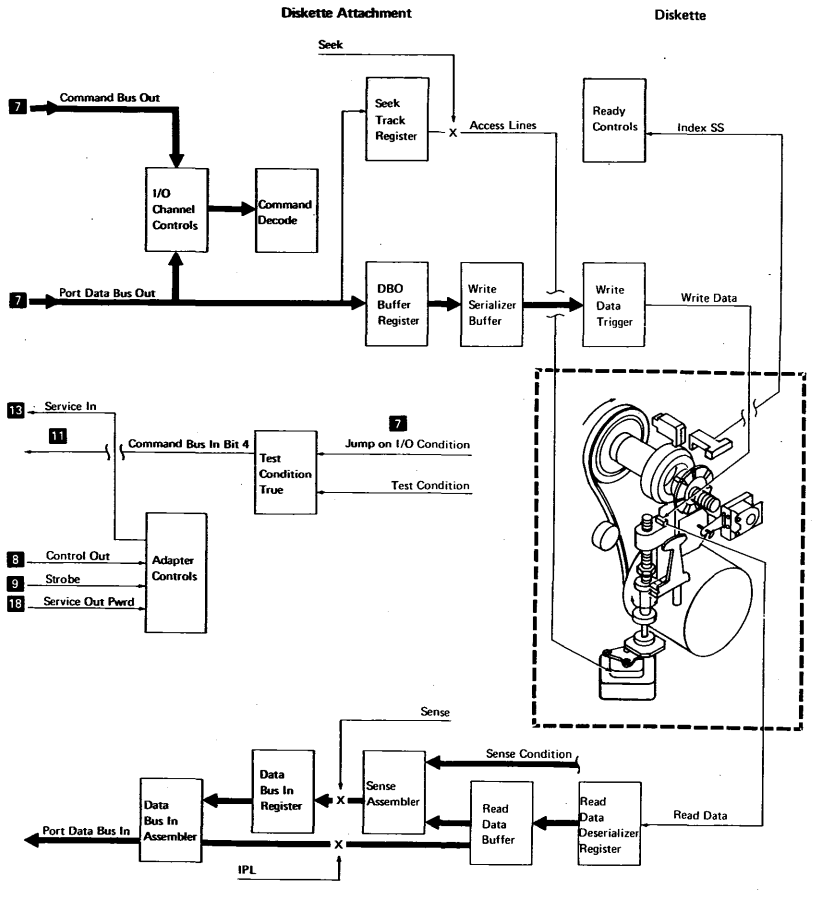




System Bus Out Function Bits 8 9 10 11	Command Bus Out 0 1 2	Command	Mnemonic
0 0 0 0	1 0 0	I/O Load	IOL
0 1 0 0	1 0 1	I/O Sense	IOS
0 1 0 1	0 0 1	Sense Interrupt Level Status Byte	SILSB
1 0 0 0	1 1 0	I/O Control Load	IOCL
1 1 0 0	1 1 1	I/O Control Sense	IOCS
0 0 1 1	0 1 1	Jump on I/O Condition	JIO
	0 1 0	Base Cycle Steal	



Storage Gate High		
Bit 0	Bit 1	Register Gated Thru
0	0	LSR High
0	1	SDR High
1	0	SBI Bits 8–15
1	1	X Reg High Bits 0–3 SDR Bits 4–7 Stg Gate High Bit P
Storage Gate Low		
Bit 0	**Bit 1**	**Register Gated Thru**
0	0	LSR Low
0	1	SDR Low
1	0	SBI Bits 8–15
1	1	Output Stg Gate High



CP Port Card A-A1L2

ERROR CONDITIONS

Blast Conditions

A blast condition is generated when a 'time-out check', 'invalid device address check', or 'CBI/DBI not zero check' line is detected by the port:

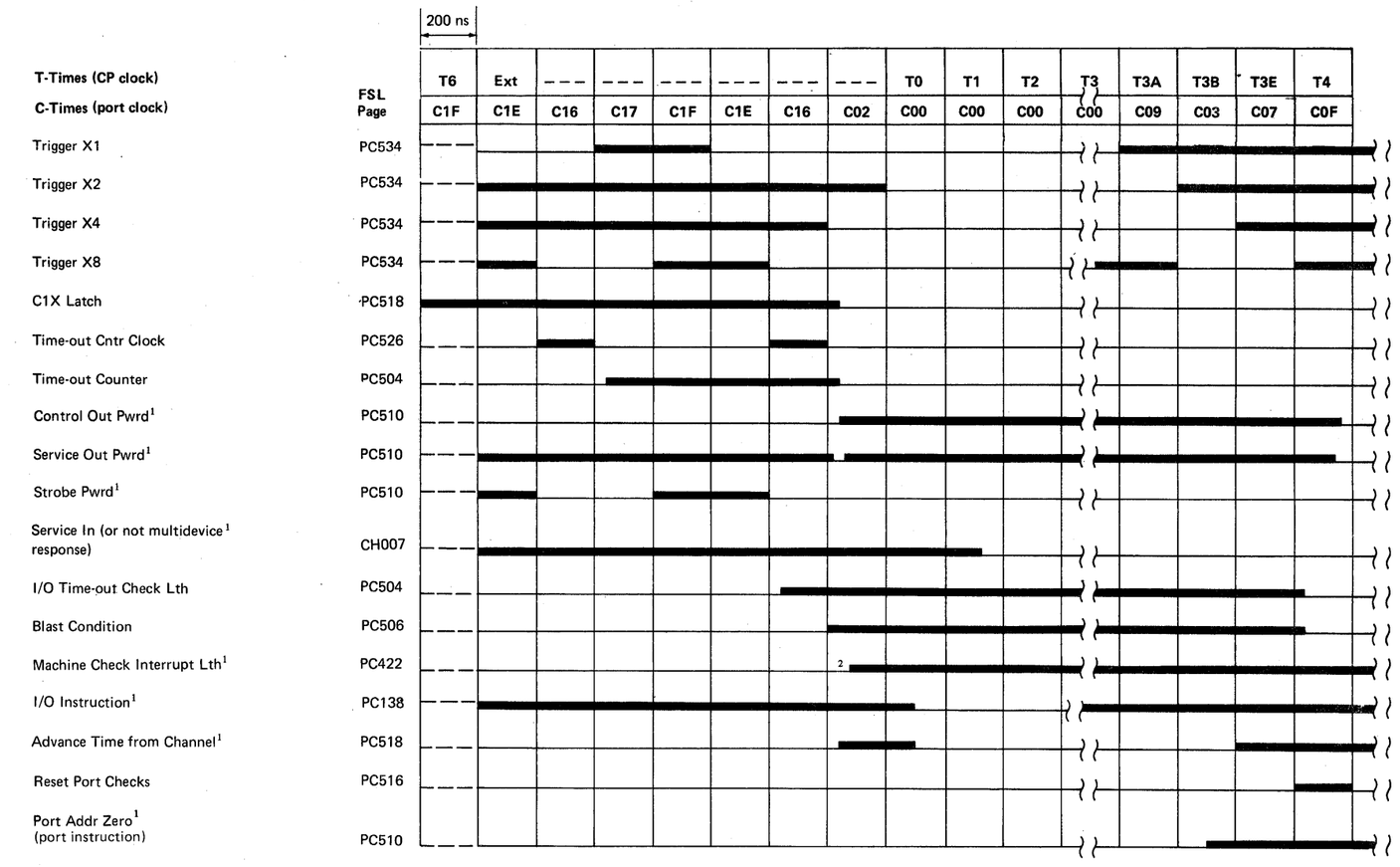
1. Time-out Check–Port check byte bit 3 is set if the adapter does not make the 'service in' line inactive in the allowed time (5.4 microseconds) after the 'control out pwrd' or 'service out pwrd' line becomes active.

2. Invalid Device Address Check–Port check byte bit 1 is set if the device addressed does not respond with an active 'service in' line within 5.4 microseconds after the 'control out pwrd' or 'service out pwrd' line becomes active.

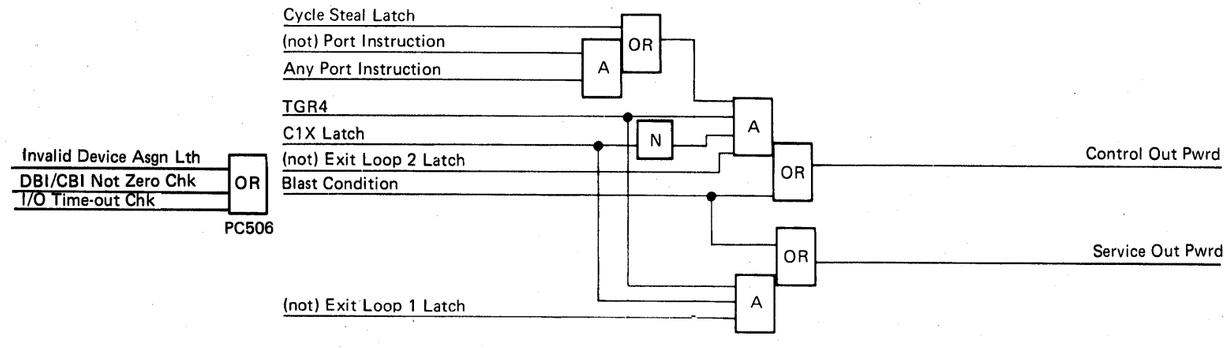
3. CBI/DBI Not Zero Check–The port sets the port check byte bit 4 if one or more of the 'MPXPO data in/CBI/service in/multidevice response' lines (except CBI bits 0 and 3) are found active 200 nanoseconds following the trailing edge of the last strobe pulse generated by the port during execution of an I/O instruction. This bit also gets set, when a time-out check occurs, if these lines have not been de-activated by the I/O attachment within 200 nanoseconds following the generation of the blast condition caused by the time-out check.

A blast condition causes all I/O devices to reset; it also sets interrupt level 0 (processor check condition except during CSIPL diagnostics mode, when machine check interrupt occurs). After de-activating the 'service out' line, the port checks that the 'MPXPO data in', 'command bus in', 'service in', and 'multidevice response' lines are all reset. If any of these lines is active, the port causes a blast condition by activating the 'service out' and 'control out' lines at the same time.

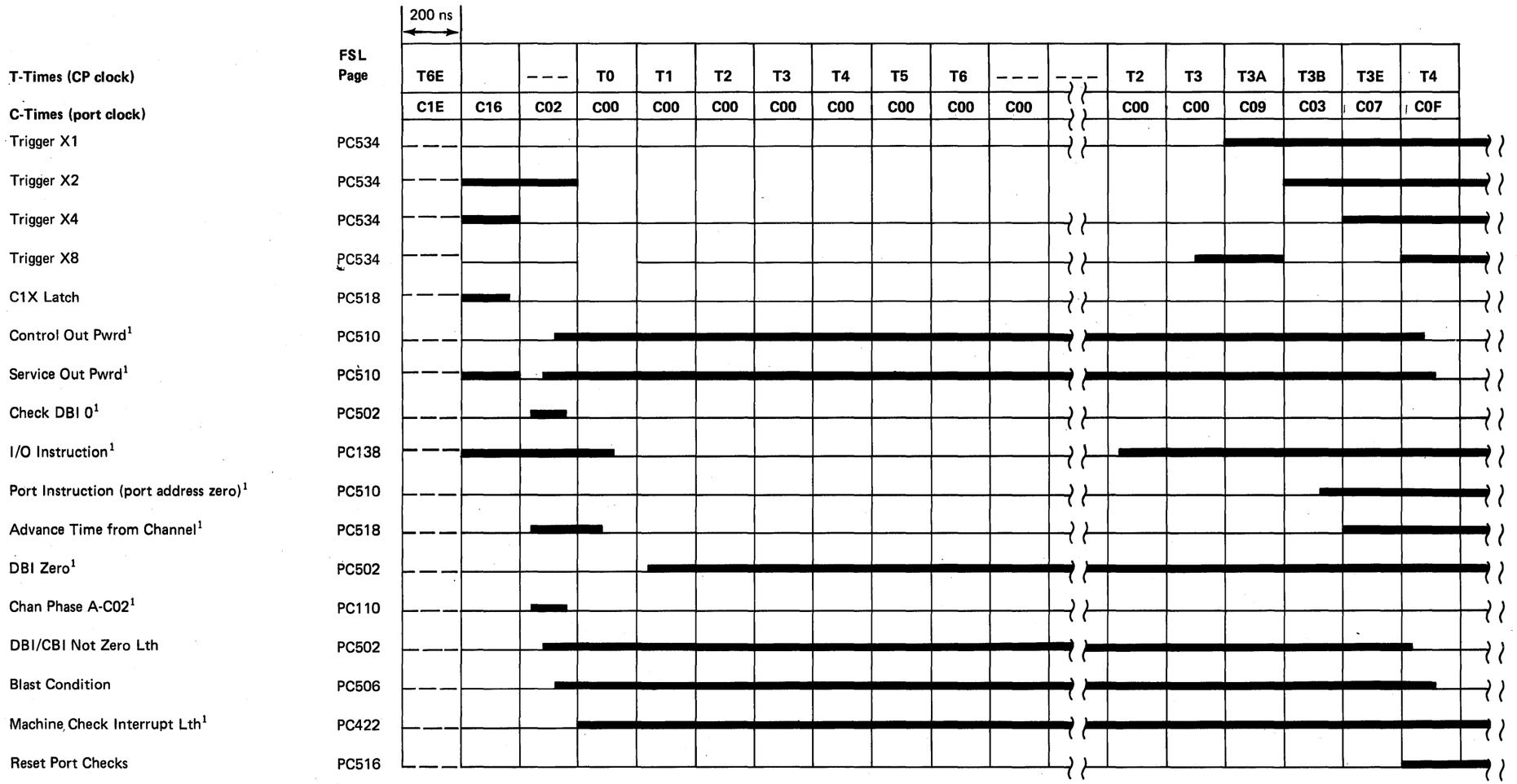
Blast Condition Because of Time-out Check



[1]This line can be probed.
[2]The timing shown here is for a blast condition during CSIPL diagnostic mode. During normal operation, the blast causes a processor check, which is subsequently reset by POR or the Reset key, or via an I/O instruction to the port during a subsequent CSIPL procedure.



Blast Condition Because Data Bus In Is Not Zero

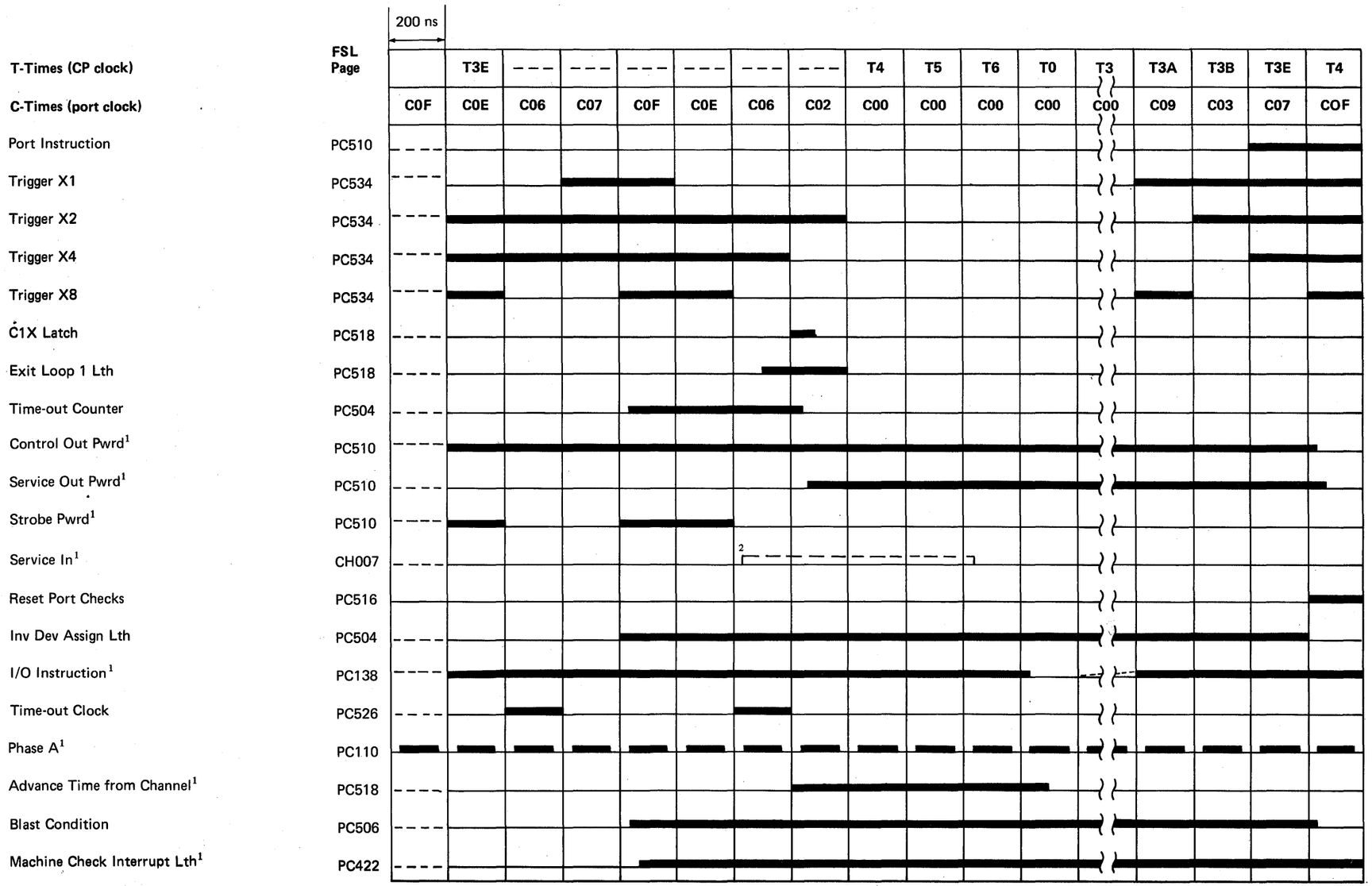


If DBI is not zero, the CPU loops in the machine check interrupt routine until a 7-second time-out occurs, which causes a processor check.

The timing shown here is for a blast condition during CSIPL diagnostic mode. During normal operation, the blast causes a processor check, which is subsequently reset by POR or the Reset key, or via an I/O instruction to the port during a subsequent CSIPL procedure.

[1] This line can be probed.

Blast Condition Because of Assigning the Wrong Device

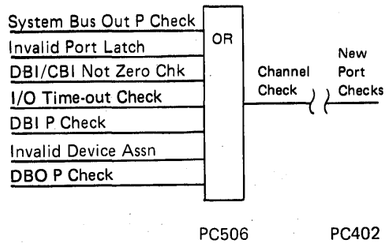


[1] This line can be probed.
[2] If 'service in' becomes active in this area, the blast condition will continue. The timing shown here is for a blast condition during CSIPL diagnostic mode. During normal operation, the blast causes a processor check which is subsequently reset by POR or the Reset key, or via an I/O instruction to the port during a subsequent CSIPL procedure.

Port Checks

Errors sensed by the port are stored in the port check register and cause a processor check. When the system operator does an IPL without powering off, the control processor moves the check information to control storage and logs the error on disk when the CSIPL is completed. The main storage instruction that caused an error condition is attempted again when possible, relying on the device and the condition.

The following checks are found by the port hardware. These checks are stored in the port checks register and can be loaded into a work register for log out to the disk. These checks can also be displayed by the CE Byte 1 lights on the CE panel by setting the Mode Selector switch to the Insn Step/Dply Chks position.

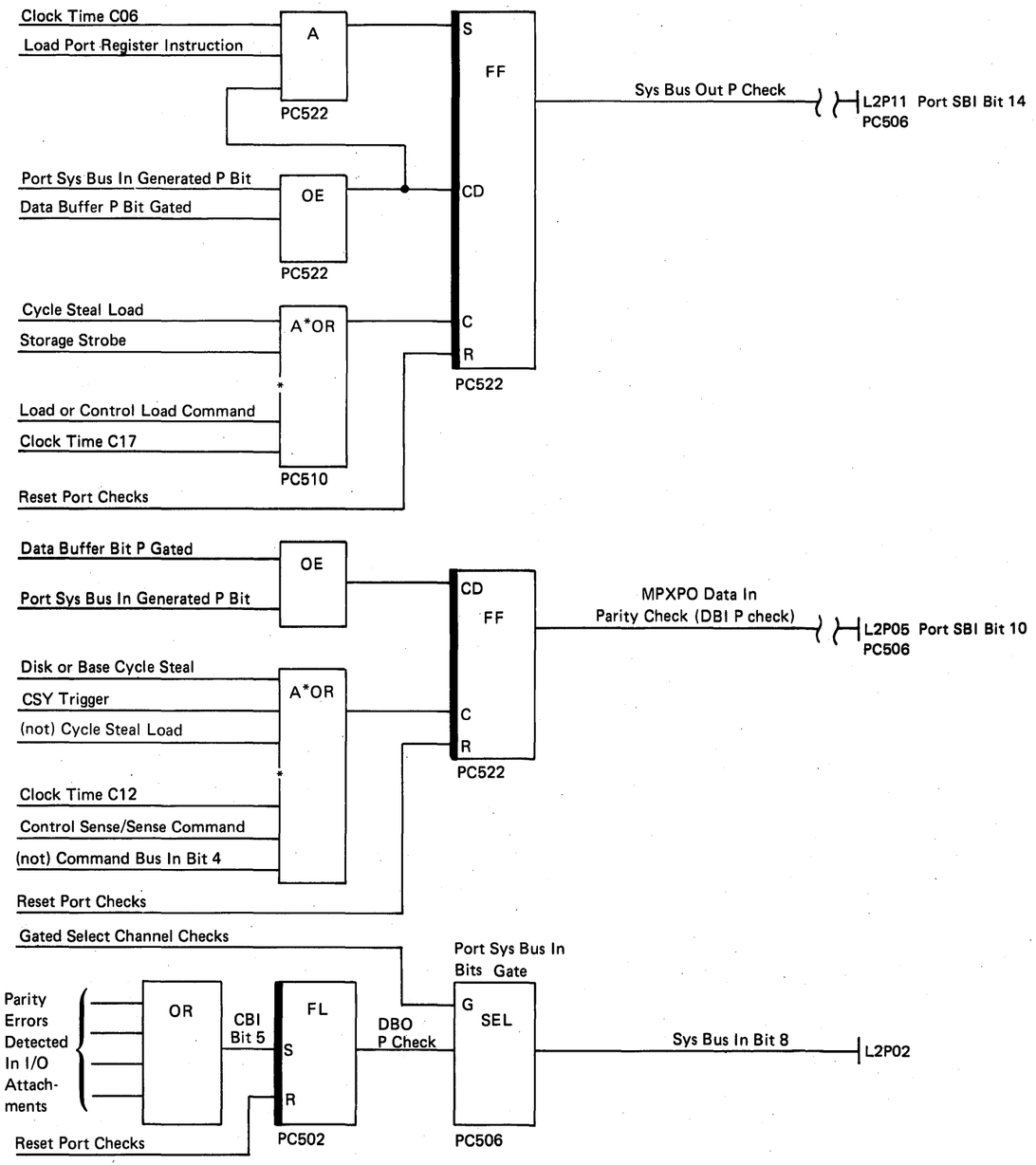


In addition to these checks, information about the last port operation is stored in the port register. This register contains the device address of the I/O attachment or the controller and the command (bits on the 'command bus out' lines) last executed by the channel. If any checks are present in the port register, changing the port register is inhibited until the error is reset. See *Commands* in the *Channel* section of this manual for decode of the device address, and see *Port Decodes* in the *Channel* section of this manual for the decode of the 'command bus out' lines.

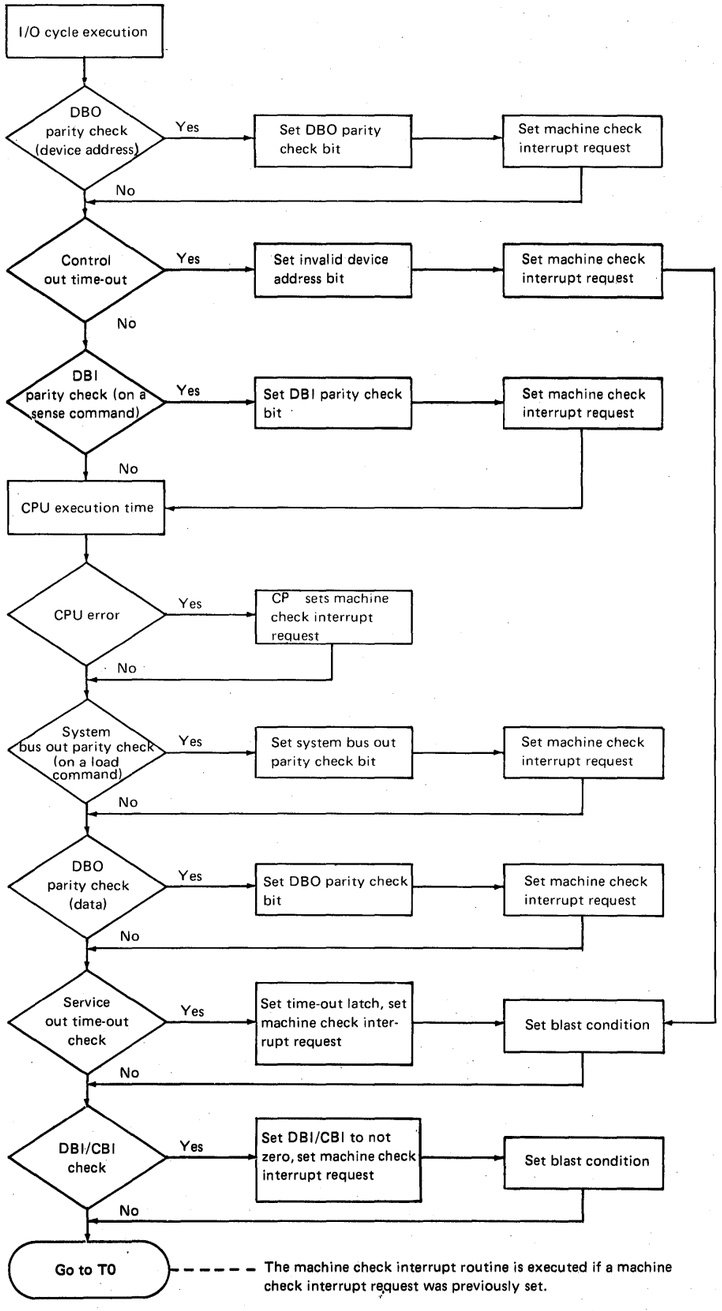
Port Error Byte (Display Byte 1)

Bit	Error	Cause
0	Data bus out parity check	Wrong parity was sensed by an attachment on the DBO bus (MPXPO bus out).
1	Incorrect device assigned	The port put an address on the DBO bus (MPXPO bus out), but no response was received from an attachment in the specified time. (The port activated the 'control out' line to address an attachment and the attachment did not respond by activating the 'service in' line in 5.4 μs.) This check also occurs if the DBO bus (MPXPO bus out) has wrong parity during the transmission of an address.
2	Data bus in parity check	Wrong parity was sensed by the port during the transmission of data from an attachment (MPXPO data in).
3	I/O time-out check	The channel sensed an error in the normal channel sequence. This check occurs if an attachment does not de-activate the 'service in' line in 5.4 μs after the rise of the 'service out' line.
4	Channel bus in/data bus in not zero	The I/O lines were not cleared in time. This check is made after the 'service out' line falls during T6 time and after a byte of data is transmitted to or from an attachment.
5	System bus out parity check	Wrong parity was sensed on the data sent from the processing unit to the port. (The check is made when the 'service out' line is active or when data is being sent to disk during a burst mode operation.)
6	Cycle steal operation check	Any processor or port parity check was sensed during a cycle steal operation.
7	Incorrect port	Bits 4-7 of work register 0 (high byte) were not 0000.

Check Generation



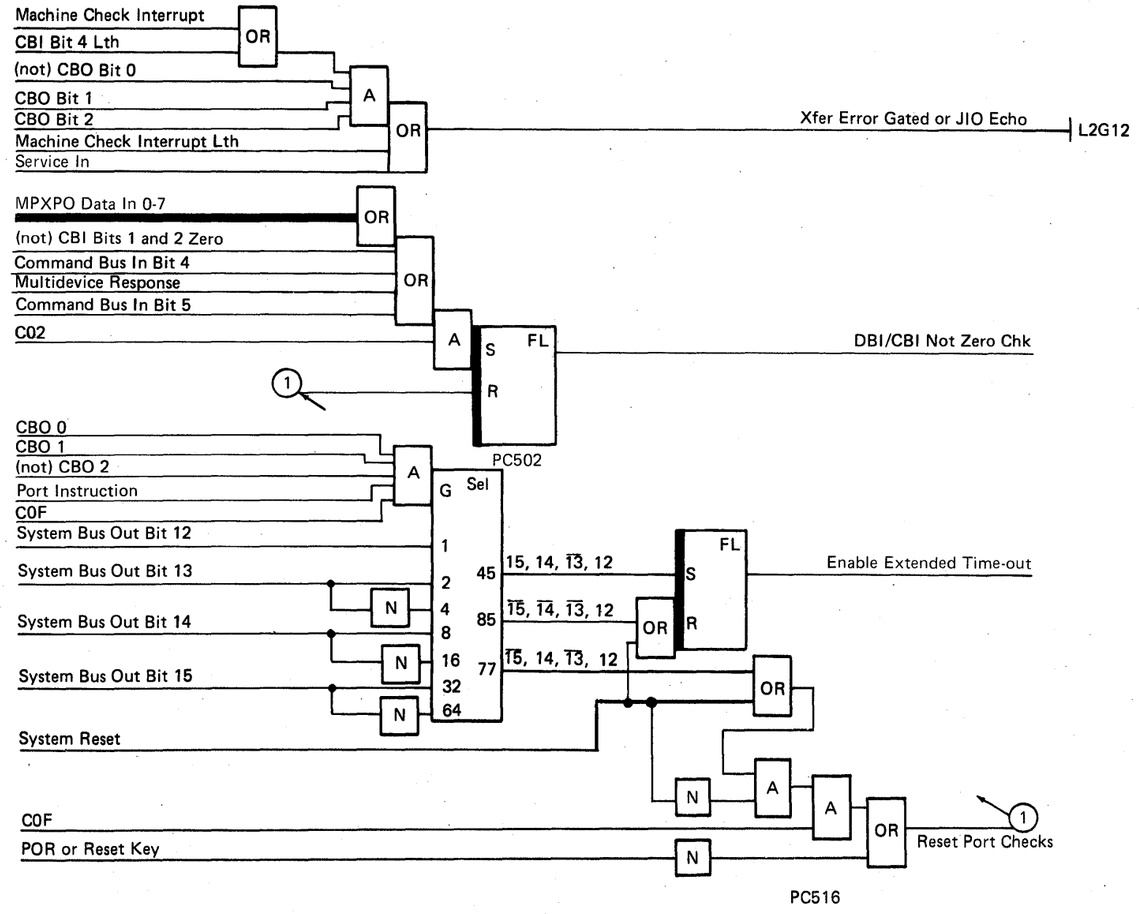
Port Error Handling Procedures



Transfer Error

An active 'transfer error' line indicates to the attachment that wrong parity was found in the port or in the control processor.

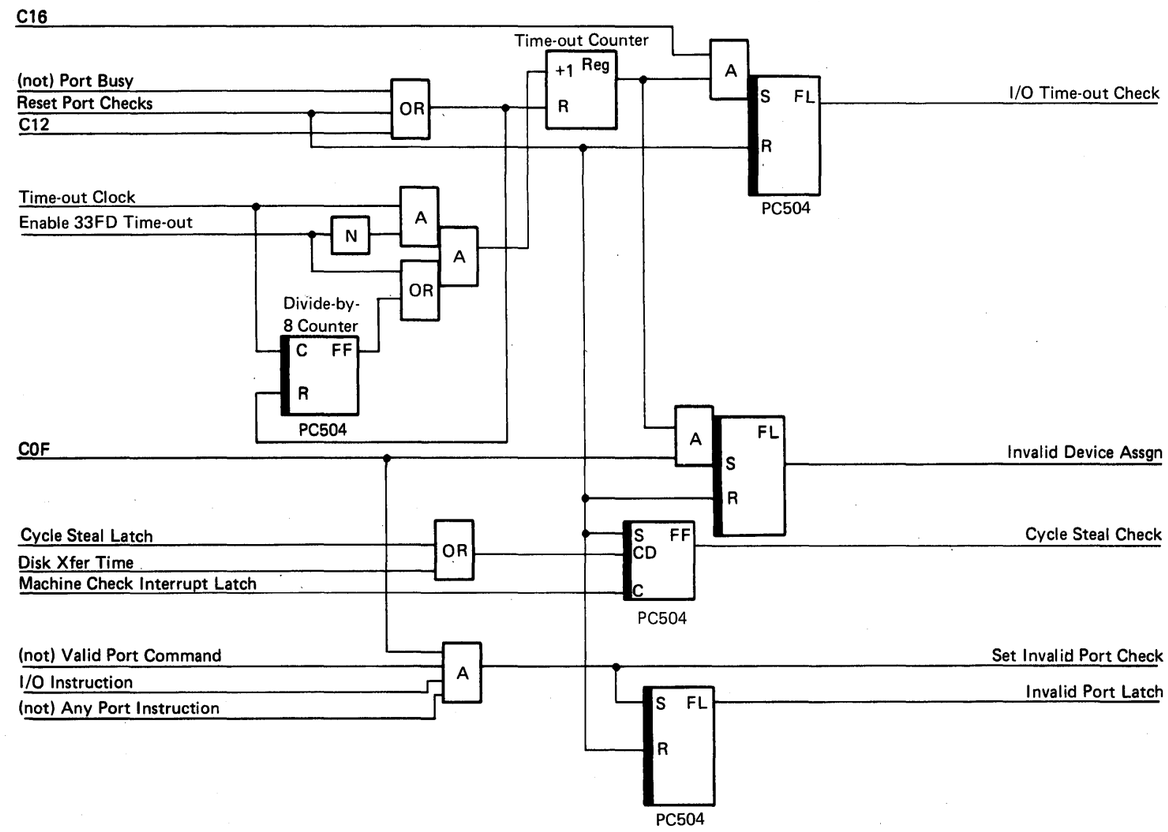
An active 'transfer error' line is also used to indicate an echo response to the adapter that the port received the I/O jump met (command bus in bit 4) and the branch will be taken by the control processor. This enables testing of asynchronous I/O device conditions with the jump-on-I/O-condition instruction and does not need the adapter to hold this line active before activating the 'service in' line.



Time-out Conditions

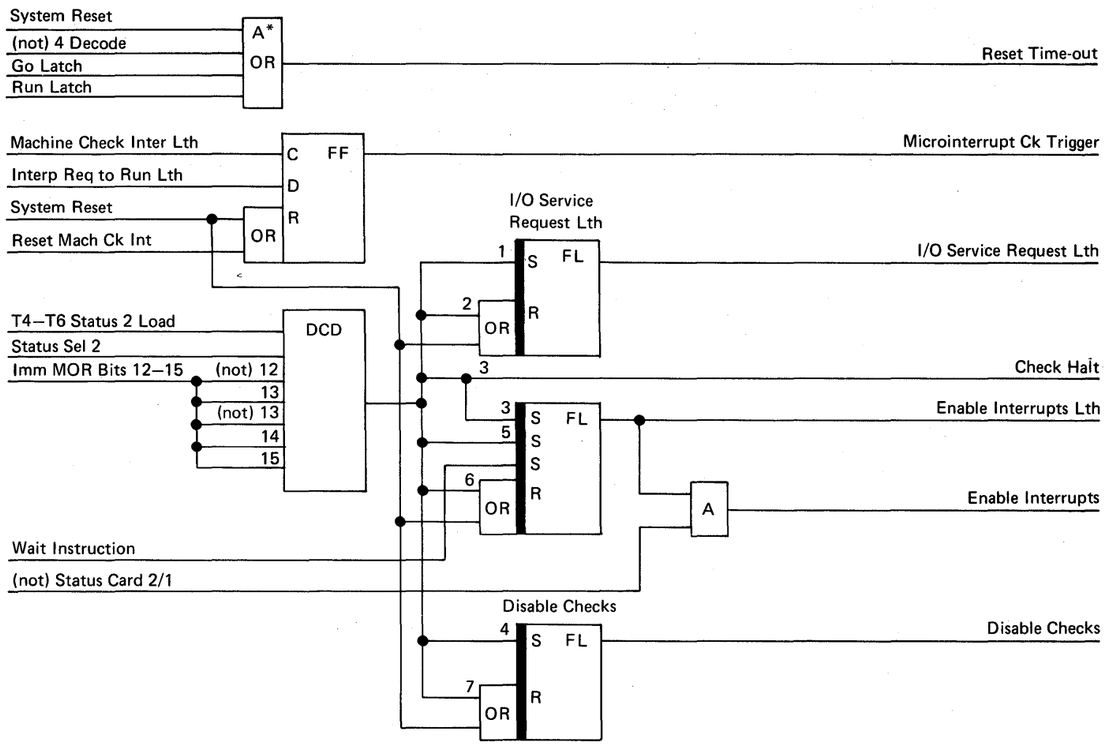
If the addressed device is not on the system or if port data out (MPXPO bus out) contains bad parity, none of the devices answers the control out sequence. Port times out under these conditions. At the end of the time-out sequence, the time-out condition is written in the port checks register (not valid device assigned). A blast is sent from the port and clears all incoming data and control lines from the I/O adapters and causes a processor check.

If the addressed device first responds with a 'service in' line but fails to de-activate the 'service in' line inside a specific time after receiving the 'service out' line, the port times out. This condition is written in the port status register and the port causes a blast condition, which clears all incoming data and control lines and causes a machine check interrupt.



Processor Check Halt

An MPLF instruction (hex BEA3-processor check halt) is a control processor I/O immediate instruction that stops the main storage processor after turning on the Processor Check light under program control. Areas of control storage that are not used are loaded with MPLF instructions. If, because of an error, the system branches to one of these not-used locations, the processor check halt causes the system to stop with a processor check and the Processor Check light to come on. This processor check halt instruction is also used by the control storage program to cause the system to stop (software check halt) when the control storage program determines that, because of some error condition, the system cannot continue to run.



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