

Contents

33FD/53FD DISKETTE DRIVE AND ATTACHMENT (Level 1)	8-1	ERROR CONDITIONS	8-50
INTRODUCTION	8-1	Fast Check	8-52
Diskette Addressing	8-1	Not Ready	8-52
33FD Diskette Drive	8-2	Missing Erase Current and Unexpected or Erase Current Present	8-53
33FD Diskette Drive Assembly	8-2	ID Not Found (Missing Record)	8-53
33FD Operating Sequences	8-3	Read Overrun Check	8-54
Frequency Modulation Read and Write Circuits	8-4	Write Overrun Check	5-54
Diskette 1 Format	8-5	Write Parity Check	8-54
53FD Diskette Drive	8-6		
53FD Diskette Drive Assembly	8-6		
53FD Operating Sequences	8-7		
Modified Frequency Modulation Read and Write Circuits	8-8		
Diskette 2D Format	8-9		
DATA FLOW OPERATIONS	8-11		
Seek Operations	8-12		
Seek Data Flow	8-13		
Read Operation	8-14		
Read Data Flow	8-17		
Write Operation	8-18		
Write Data Flow	8-19		
Find Sector Identification Operation	8-20		
Find Sector Identification Data Flow	8-23		
Write Sector Identification Operation	8-24		
Write Sector Identification Data Flow	8-25		
COMMANDS	8-26		
I/O Load Command	8-26		
I/O Sense Command	8-28		
I/O Control Load Command	8-30		
Write Byte or Write Address Mark Byte Command	8-32		
Write Data Trigger	8-34		
Write Cyclic Redundancy Character Byte Command	8-35		
Seek to Next Track Command	8-37		
Search for Address Mark Byte Command	8-38		
I/O Control Sense Command	8-40		
Sense Interrupt Level Status Byte Command	8-43		
Jump on I/O Command	8-44		
FUNCTIONAL UNITS	8-46		
Data Separator	8-46		
Index Counter	8-46		
Ready Counter	8-47		
Control Storage Initial Program Load Track Counter	8-47		
Write Clock and Write Bit Ring	8-47		
Read Clock and Read Bit Ring	8-47		
Cyclic Redundancy Character Shift Register	8-48		
Interrupt 1 and Interrupt 4 Requests	8-49		

33FD/53FD Diskette Drive and Attachment (Level 1)

INTRODUCTION

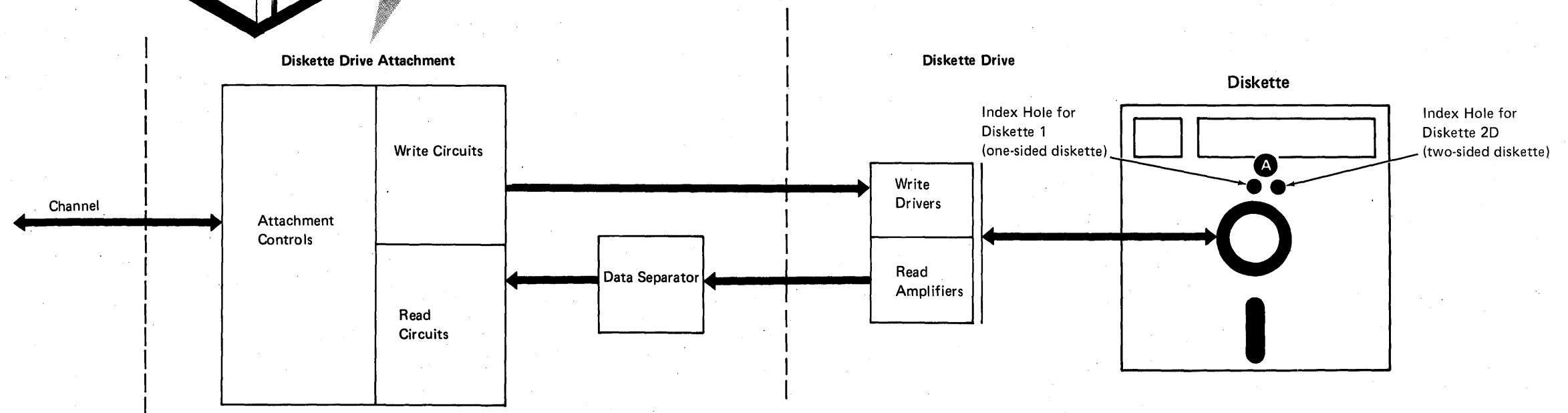
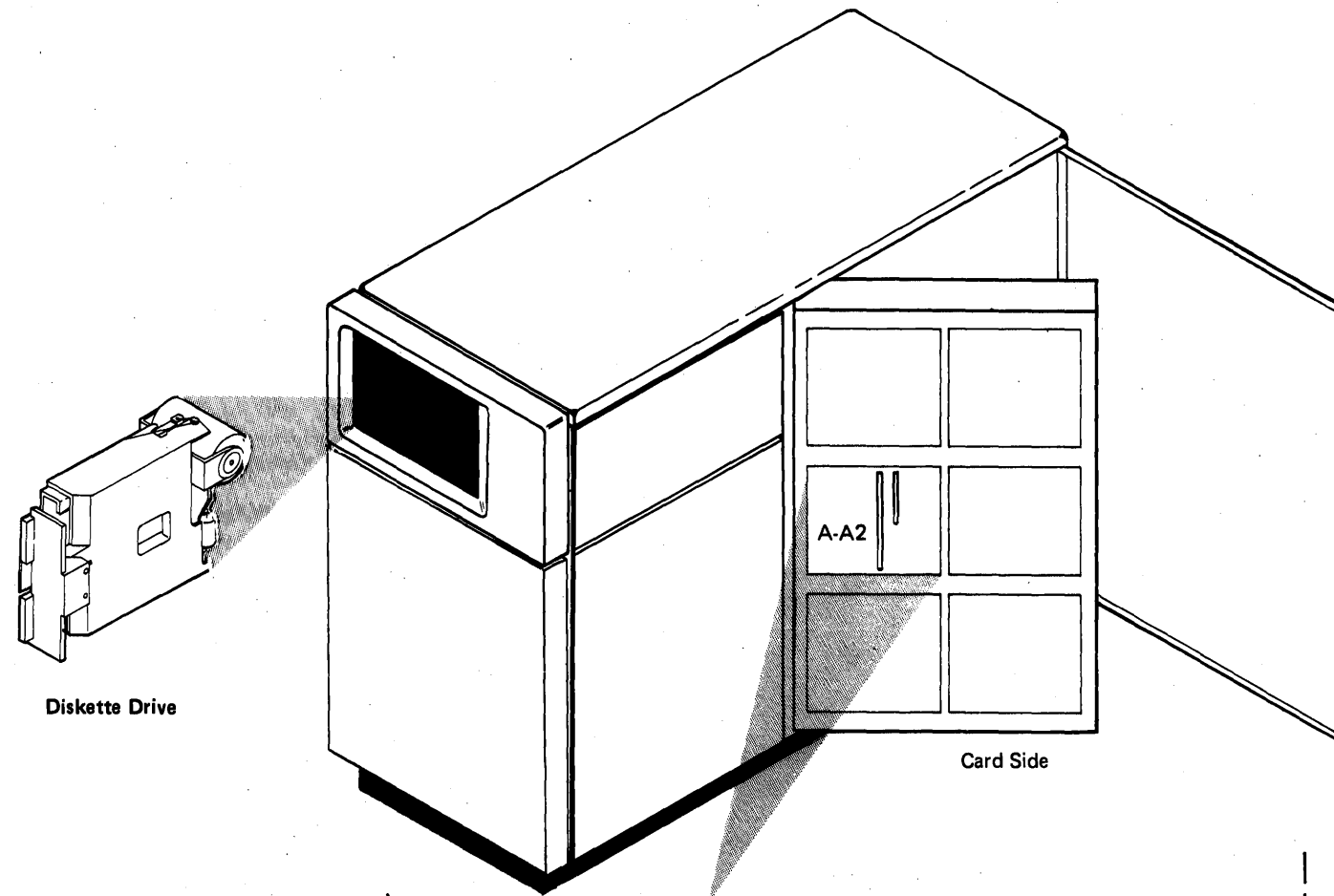
The diskette drive and diskette drive attachment are installed inside the 5340 System Unit. System/34 uses either a 33FD diskette drive or a 53FD diskette drive. The control storage program and the attachment control the diskette drive. The diskette drive can read a data track, write on a data track, or seek to a data track of a diskette.

The diskette drive has a continuously turning shaft that turns the diskette. A solenoid-loaded data head is moved to the correct data track by a stepper motor. The data head can then read or write the data tracks.

One side of the Diskette 1 (33FD/53FD diskette) and both sides of the Diskette 2D (53FD diskette) are used for recording. The two types of diskettes are identified by the physical location of the index hole **A**. When a Diskette 1 is inserted in a 53FD diskette drive, the circuits that sense the index hole prevent the use of the second side. A Diskette 2D cannot be used in a 33FD diskette drive.

There is one label cylinder, 74 data cylinders, and two alternative data cylinders per diskette. For more information, see *The IBM Diskette General Information Manual, GA21-9182*.

Instructions executed by the control processor are decoded into commands by the attachment. These commands start the read, write, and seek operations in addition to performing various control functions. An index hole in the diskette references the start of the first sector on the cylinder that the data head is over.



Diskette Addressing

Sequential Sector Addressing

The main storage program uses sequential sector addressing to identify a diskette data area. Sequential sector addressing starts at hexadecimal address 0001 (cylinder 1, data head 0, sector 1), increases by 1 for each following sector, and extends through the last sector on cylinder 74. Cylinder 0 cannot be addressed by sequential sector addressing.

The control storage program changes sequential sector addresses to actual sector addresses for all operations. See the *Data Areas Handbook* for more information on diskette addressing.

Actual Sector Addressing

If sequential sector addressing is not used, actual sector addressing is used. The user supplies the 5-byte CHRNX field. This method of addressing must be used to address cylinder 0 (the volume label and volume table of contents).

33FD Diskette Drive

33FD Diskette Drive Assembly

When the cover **A** of the 33FD diskette drive is open, the diskette can be inserted or removed.

When the cover is closed, the spring-loaded collet **B** centers and holds the diskette to the drive hub.

The data head load actuator assembly **C** is a magnet and an armature. During a read or write operation, the magnet is active and makes the pressure pad arm push the diskette against the data head. At the same time, the armature puts a slight pressure on the diskette envelope, which cleans the diskette. When not reading or writing, the data head load actuator is not active and holds the pressure pad assembly away from the diskette to decrease wear on the diskette surface and the data head.

When the cover is closed, the continuous light from the light-emitting diode **D** points toward the phototransistor. Every time the diskette turns, the index hole in the diskette lets the light from the light-emitting diode reach the phototransistor. The phototransistor sends index pulses to the diskette drive attachment.

The preload spring **E** pushes the leadscrew to ensure that the data head is aligned with the diskette.

The upper-limit stop **F** stops the data head from going past track 76. The lower-limit stop **G** stops the data head from being driven lower than track 00.

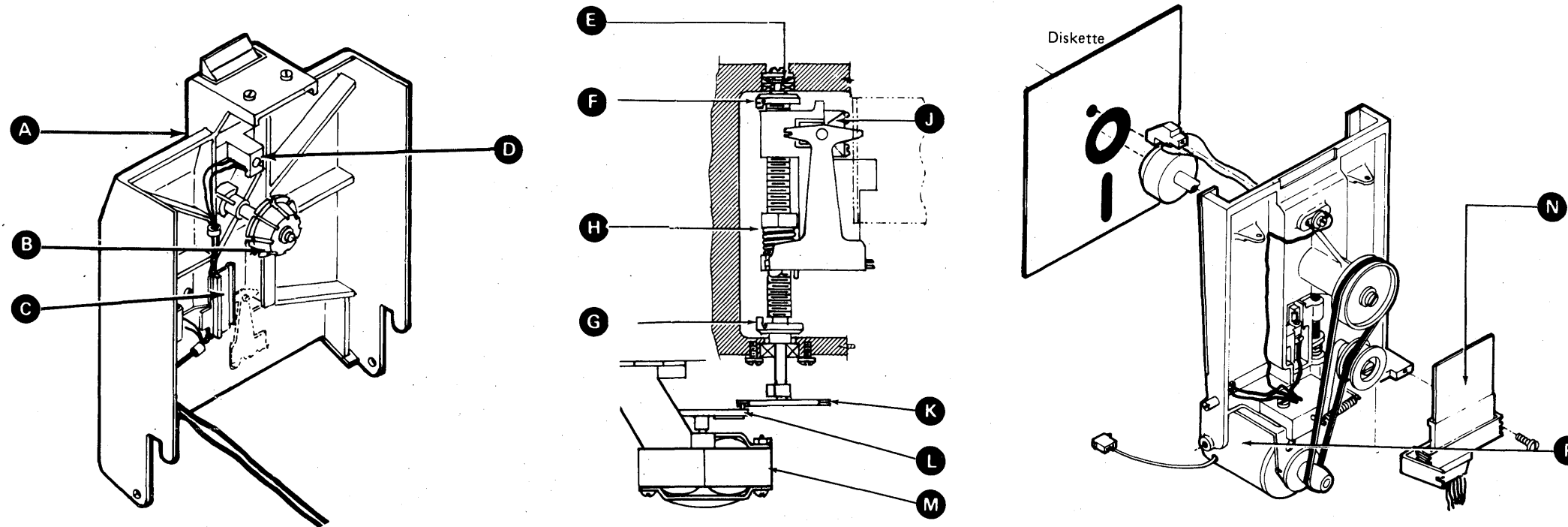
The leadscrew nut and spring **H** push against the data head and carriage assembly to ensure that the data head is aligned with the diskette.

The data head **J** can either read data from the diskette or erase and write data on the diskette.

The stepper motor wheel **L** is on the end of the stepper motor shaft. The stepper motor **M** turns in steps of 90 degrees in either direction under the control of access pulses. The stepper motor wheel engages the leadscrew wheel **K**. When the stepper motor wheel turns 90 degrees, it turns the leadscrew wheel 90 degrees. The data head carriage assembly then moves up or down one track on the diskette.

The circuits for the stepper motor, the data head load actuator, and the data head are on the file control card **N**. The amplifier circuits for the phototransistor and data head are also on the file control card. The file control card circuits and test pins face out.

The drive motor **P** turns the diskette at a speed of $360 \pm 2.5\%$ revolutions per minute with the head loaded.



33FD Operating Sequences

Diskette Operation

The following events make the diskette operational:

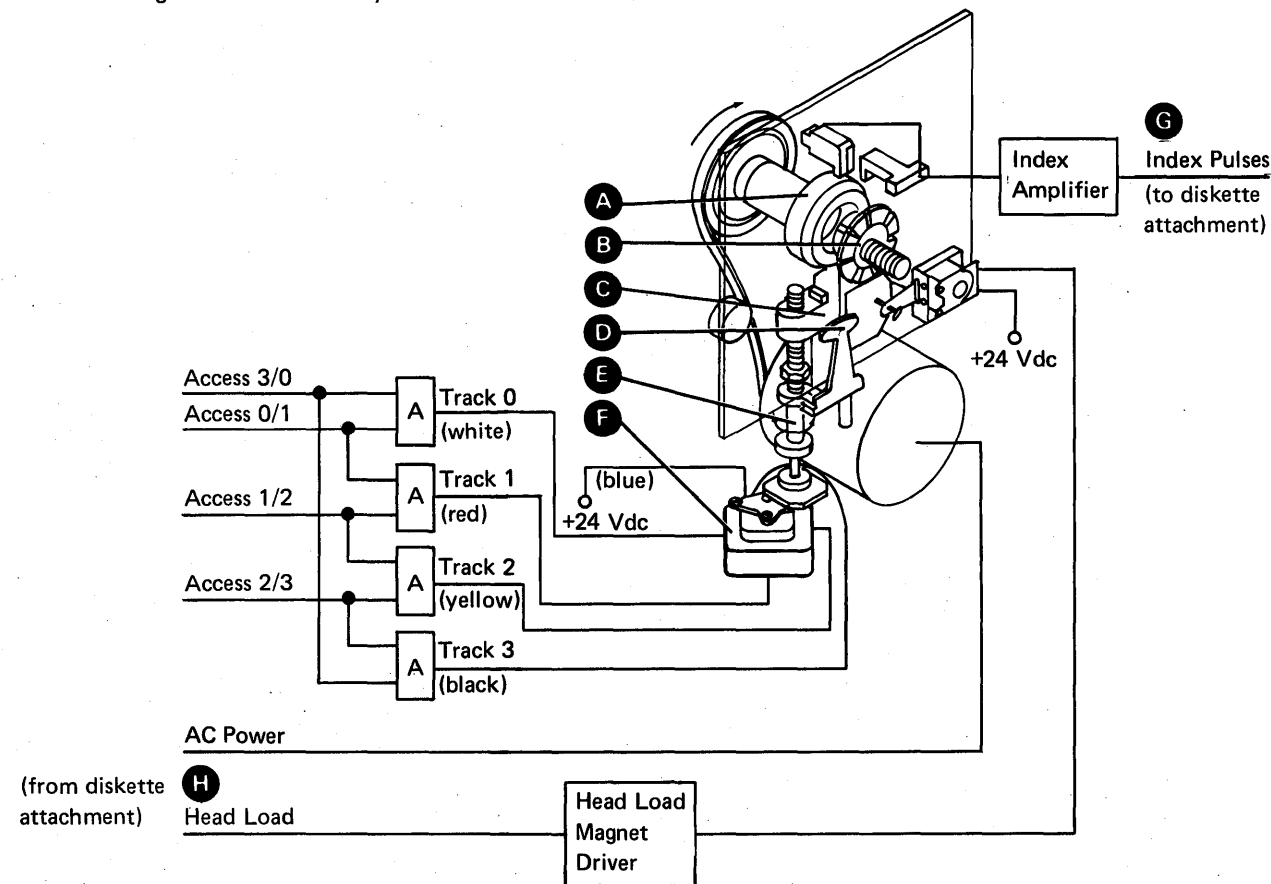
1. When system power is on, the diskette drive motor turns continuously.
2. When the diskette is inserted in the diskette drive and the cover assembly is closed, the collet assembly **B** clamps the diskette to the drive hub **A**. The diskette then starts turning.
3. When the diskette is up to speed and the heads are loaded, index pulses **G** are sensed once every 166.7 (+4.27, -4.06) milliseconds. The attachment uses these pulses to ensure that the diskette is turning at the correct speed, thereby sensing the diskette-ready condition.

Seek Operation

To move the data head to the desired track:

1. The control storage program issues a recalibrate operation (a minimum of 76 seeks to cylinder 0). Diskette ready is activated if the diskette speed is OK.
2. Two access lines are activated at the same time for a minimum of 57.4 milliseconds to seek one track **L**. (A seek does not change the head load condition.) A 98.4-millisecond delay is added after the last seek to allow for head settling.

Example: The chart shows the data head moving from track 2 to track 6. The access lines are activated for a minimum of 57.4 milliseconds to move the data head across each track, and 98.4 milliseconds **M** to allow the data head to settle on the last track.



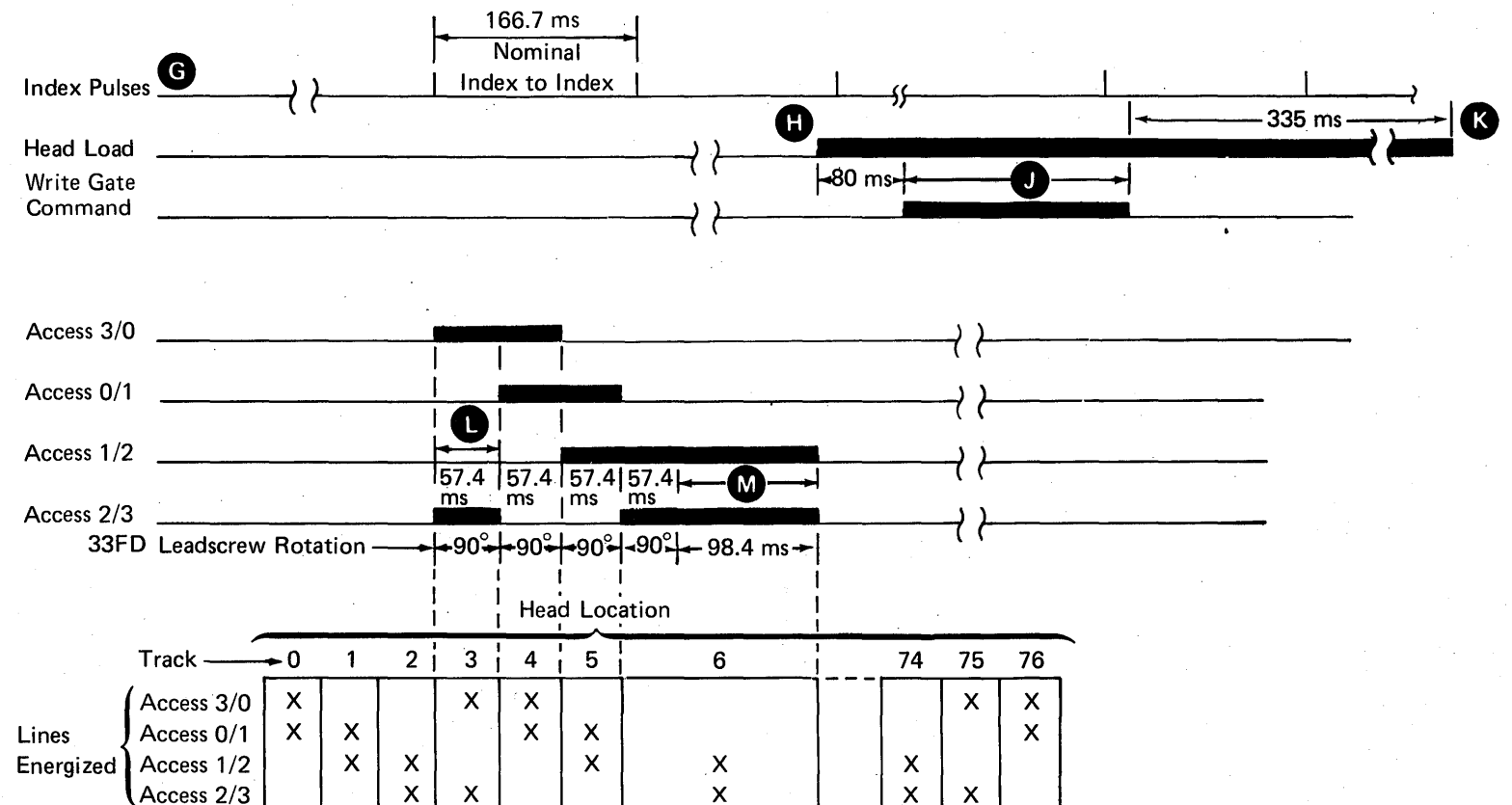
3. For each access operation, the stepper motor **F** turns the leadscrew **E** 90 degrees clockwise or counterclockwise. This moves the data head one track position. Turning the leadscrew clockwise (looking into the unit from the front of the machine) moves the carriage out (toward the front).

Read or Write Operation

To load the data head and write on or read from the diskette:

1. The control storage program issues a data head load command **H** before a read or write operation. This causes the pressure pad **D** to push the diskette against the data head **C**. Data is valid after 80 milliseconds (time for the data head to load).
2. The control storage program issues a read or write command **J**.

3. The control storage program issues a command to unload the heads **K** 335 milliseconds after a seek, read, or write operation is complete (if no other operation is issued during the 335 milliseconds). This decreases wear on the diskette and the data head. The 335-millisecond delay occurs because during normal diskette use, the next diskette operation usually starts during the 335-millisecond delay. Therefore, the data head does not have to be loaded before each operation.



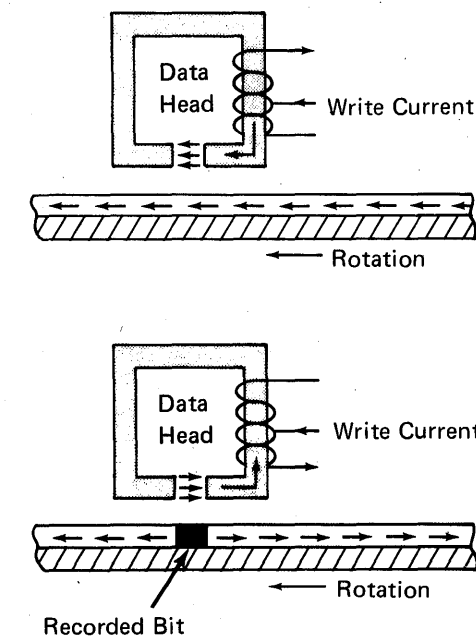
Frequency Modulation Read and Write Circuits

Writing

During a write operation, a clock bit (identifies the start of a bit cell) or a 1-bit (data) is recorded by reversing the direction of the current in the data head coil, which reverses the direction of the magnetic flux in the gap. When the direction of the flux reverses on the diskette surface, either a clock bit or a 1-bit is recorded.

Writing Data Bits

For each change on the 'diskette write data' line **A**, a clock bit or a 1-bit is written on the diskette. No change between clock bits represents a 0-bit (not a 1-bit). Level changes on the 'diskette write data' line cause the current in the data head to be switched, which results in a polarity change on the diskette track. Therefore, a polarity change on the diskette represents a clock bit or a 1-bit. The time from 1 clock bit to the next clock bit is a bit cell and is approximately 4 microseconds long. Data bits are written in the center of the bit cell.

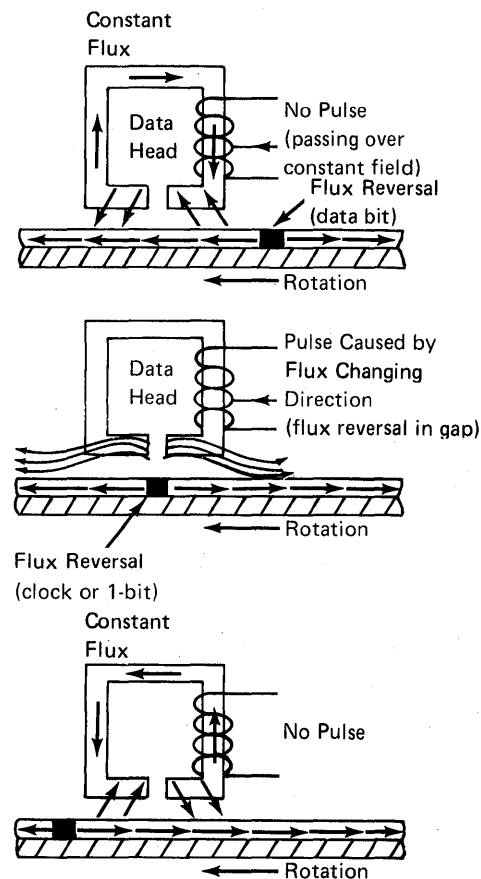


Reading

During a read operation, with the recording surface magnetized in one horizontal direction, constant flux flows and the coil senses no output voltage. However, when a recorded clock bit or 1-bit (180 degrees horizontal flux reverse) passes the gap, the flux moving through the ring and coil also reverses and causes a voltage output pulse.

Reading Data Bits

Bits represented on the 'diskette write data' line **A** as level changes are represented on the '33FD raw read data' line **B**, when read, as positive pulses with an approximate width of 150 nanoseconds. During a read operation, clock bits and data are separated in the variable frequency oscillator card.



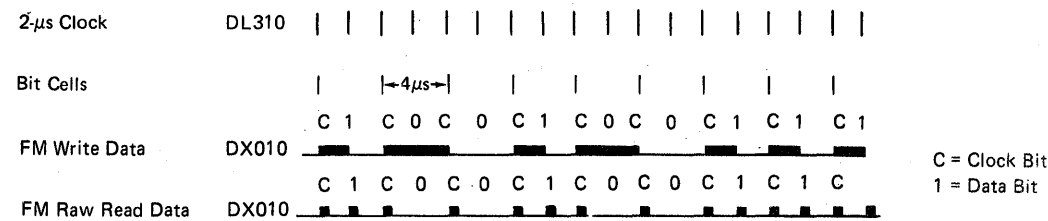
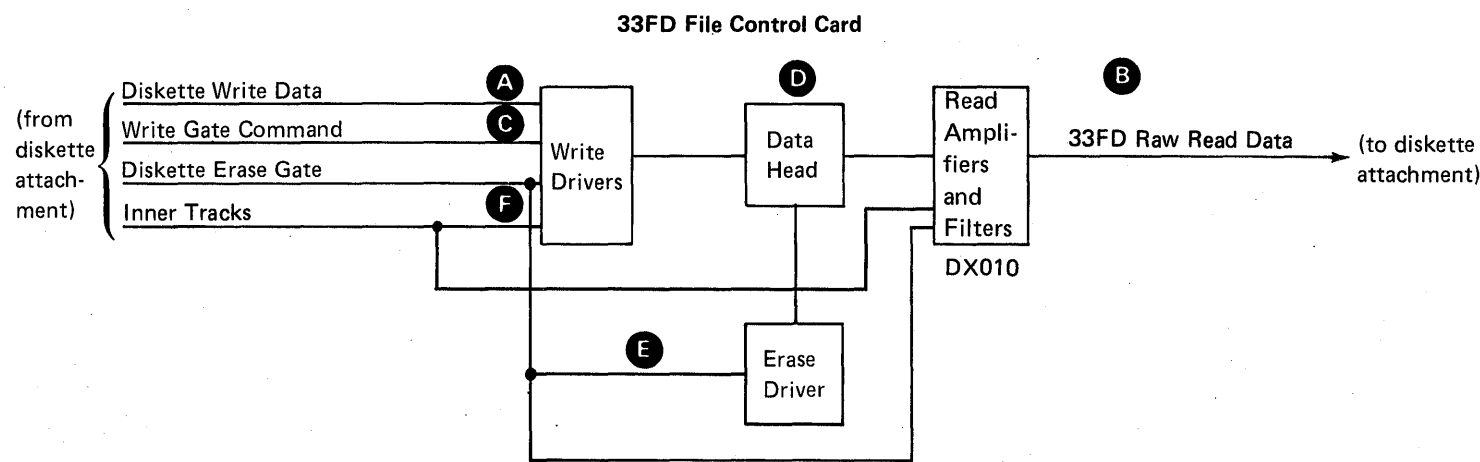
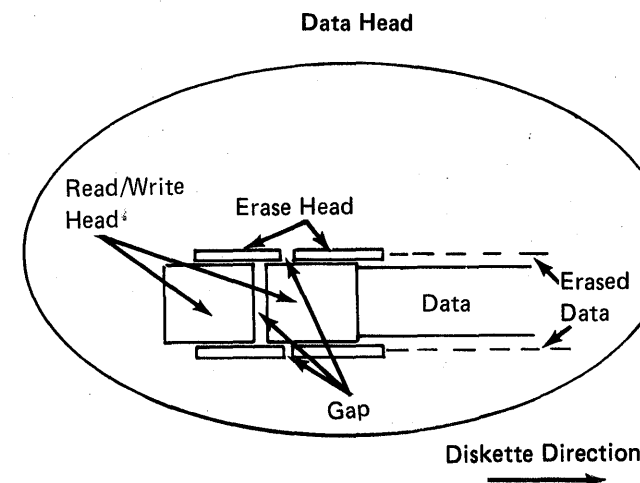
Controls

The 'write gate command' line **C** is active during a write operation. This line lets current flow through the data head **D** and de-activates the read circuits.

The 'diskette erase gate' line **E** also is active during a write operation. This line causes the edges of each data track to be erased, which leaves a gap between tracks (removes old data that may exist between tracks).

When the 'write gate command' line is not active, the write circuits are not gated and the read circuits are ready to read.

The 'inner tracks' line **F** is active from track 43 through track 76. When this line is active during a write operation, the write current through the data head is decreased because the bit density increases toward the center tracks and, therefore, less write current is needed. When this line is active during a read operation, read filters compatible with tracks 43 through 76 are enabled.



The above 1001 0011 represents hex 93.

Diskette 1 Format

There are 77 tracks written in frequency modulation mode on the Diskette 1 surface. A track is a circular path on the surface of the diskette. The tracks are numbered 00 through 76. Track 00 is the outside track and track 76 is the inside track. Of the 77 tracks, only 74 tracks are data tracks. Track 00 is a label track; tracks 75 and 76 are reserved and are used in place of tracks that become damaged.

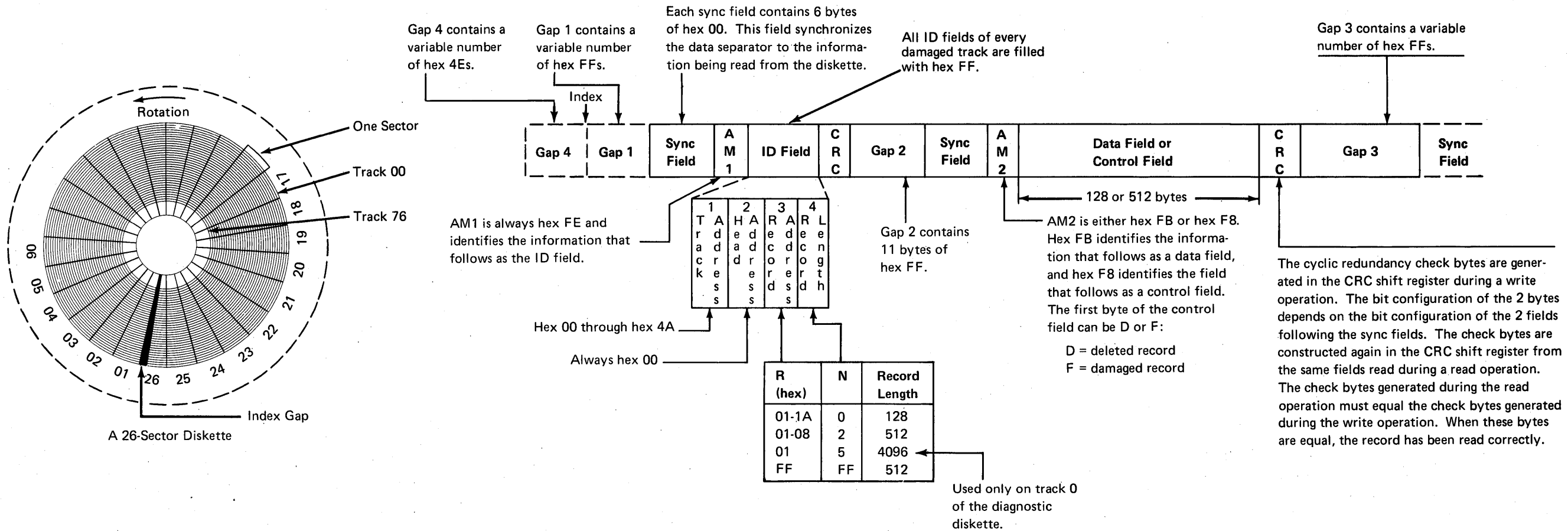
The damaged track is flagged by writing binary 1's in all ID fields of that track. The ID that would have been used on the damaged track is written in the ID field of the next physical track. When the ID field of a damaged track is read, the data head automatically moves to the next higher numbered physical track.

Each track is divided into either 8 or 26 sectors. The data stored in 1 sector is a record. When the tracks are divided into 8 sectors, each record is 512 bytes long; when tracks are divided into 26 sectors, each record is 128 bytes long. Diskettes with 74 data tracks that are divided into 8 sectors per track have 303,104 bytes of data; diskettes with data tracks that are divided into 26 sectors per track have 246,272 bytes of data.

Some diagnostic programs write one 4,096-byte sector in frequency modulation mode on a track. Therefore, record length can be 128, 512, or 4,096 bytes. The value of n recorded in the record length byte indicates the record length.

Each sector on the diskette has its track and sector identification (address) recorded at the physical location of the sector on the diskette.

Diskettes that contain recorded sector identification fields (addresses) for each sector are known as initialized diskettes. Each sector has two parts; the first part contains the sector identification field, and the second part contains the data record or the control record field.



53FD Diskette Drive

53FD Diskette Drive Assembly

When the cover **A** of the diskette drive is open, the diskette can be inserted or removed. When the cover is closed, the collet **B** centers and clamps the diskette to the drive hub.

The belt **G**, the drive motor **E**, the drive pulley **J**, and the idler assembly **H** turn the diskette at $360 \pm 2.5\%$ revolutions per minute with the heads loaded.

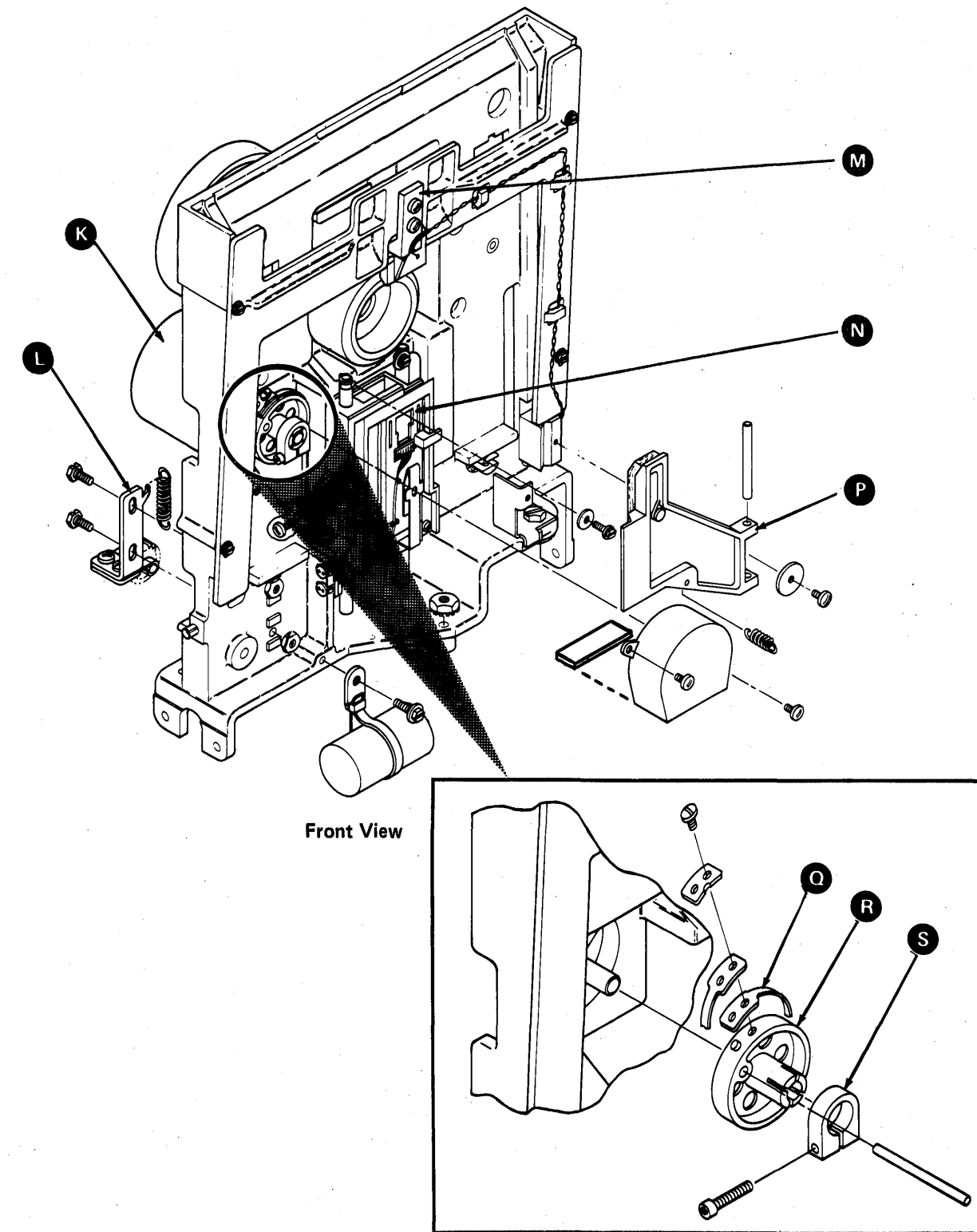
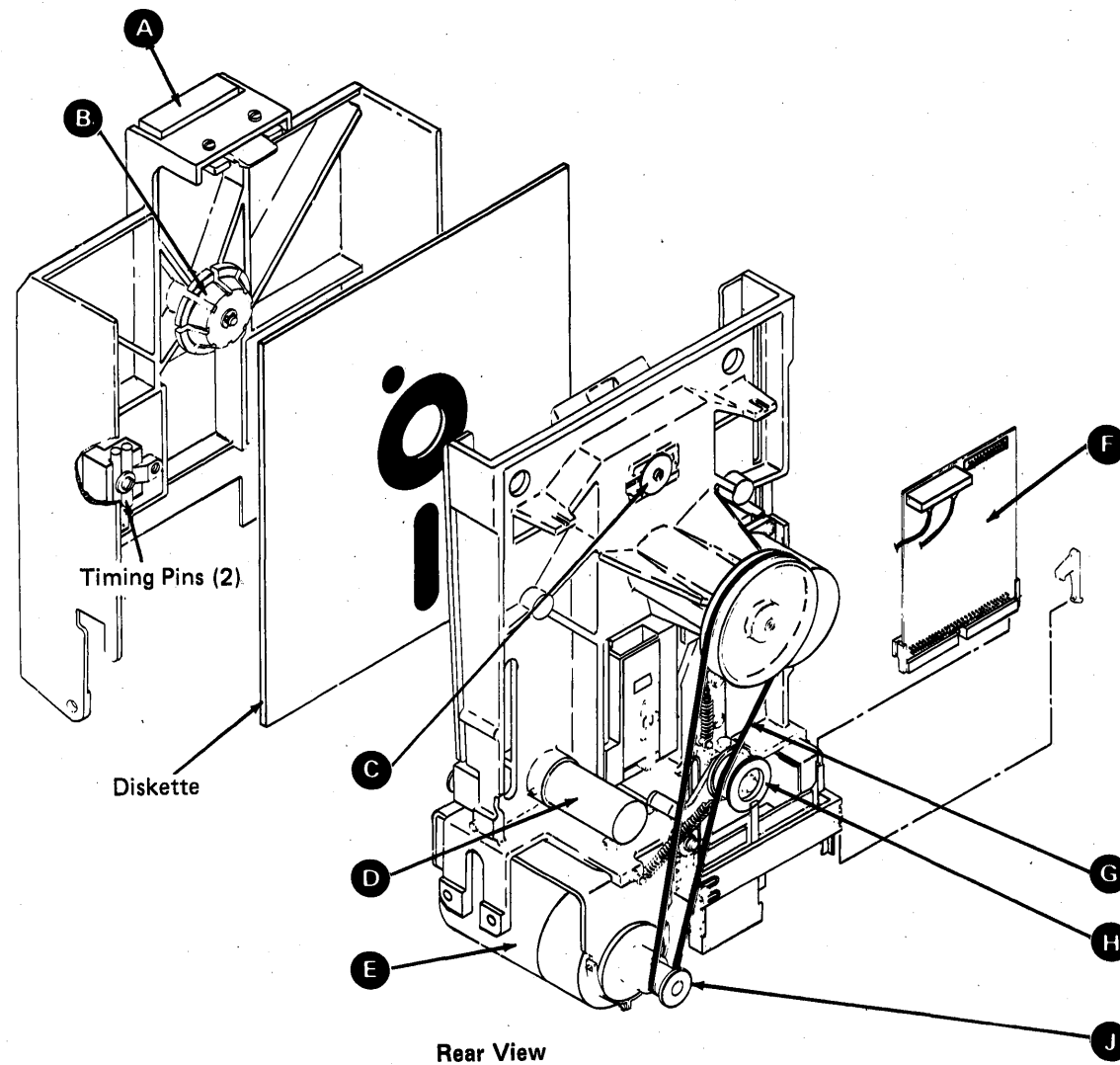
The stepper motor **K** turns in either direction under control of access pulses. The stepper motor pulley **R**, the stepper motor pulley clamp **S**, the stepper drive band **Q**, and the stepper idler assembly **L** move the data heads across the diskette surface.

Two data heads are on a common carriage assembly **N** and move under control of the stepper motor. The data heads read data from and write new data on a diskette.

The data head load solenoid **D** causes the bail **P** to load the data heads.

The two light-emitting diodes **M** and the two phototransistors **C** work together to sense the diskette index and identify the type of diskette inserted (Diskette 1 or Diskette 2D).

The diskette drive control card **F** has the drive circuits for the stepper motor, the data head load solenoid, and the write and erase functions. The card also has the amplifiers for the data heads and the light-emitting diode and phototransistor circuits.



53FD Operating Sequences

Diskette Operation

The following events make the diskette operational:

1. When system power is turned on, the diskette drive motor starts turning **A**.
2. When the diskette is inserted in the diskette drive and the cover assembly is closed, the collet **B** clamps the diskette to the drive hub. The diskette then starts turning.
3. When the diskette is up to speed and the heads are loaded, index pulses **G** are sensed once every 166.7 (+4.27, -4.06) milliseconds. The attachment uses the index pulses to ensure that the diskette is turning at the correct speed, thereby sensing the diskette-ready condition.

Seek Operation

To move the data heads to the desired cylinder:

1. The control storage program issues a recalibrate operation (76 seeks to cylinder 0). Diskette ready is activated if the diskette speed is OK. Seeking is done by activating the two access lines to the stepper motor **F**. This moves the head/carriage assembly **E** in (toward the hub) or out (away from the hub). Activating two sequential access lines turns the stepper motor a distance equal to 1 cylinder **L**.

2. Two access lines are activated at the same time for a minimum of 8.2 milliseconds to seek one track **L**. (A seek does not change the head load condition.) A 32.8-millisecond delay is added after the last seek to allow for head settling.

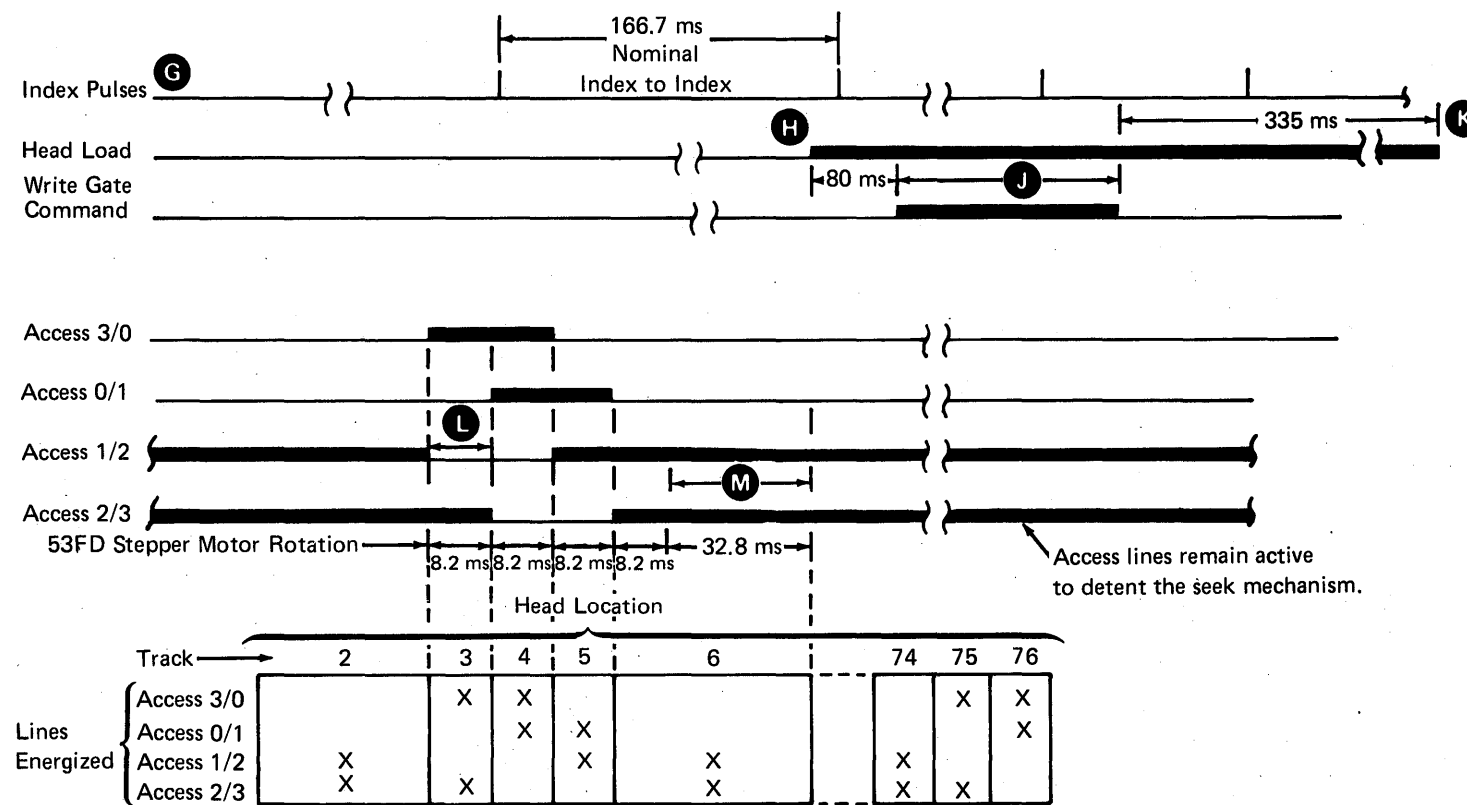
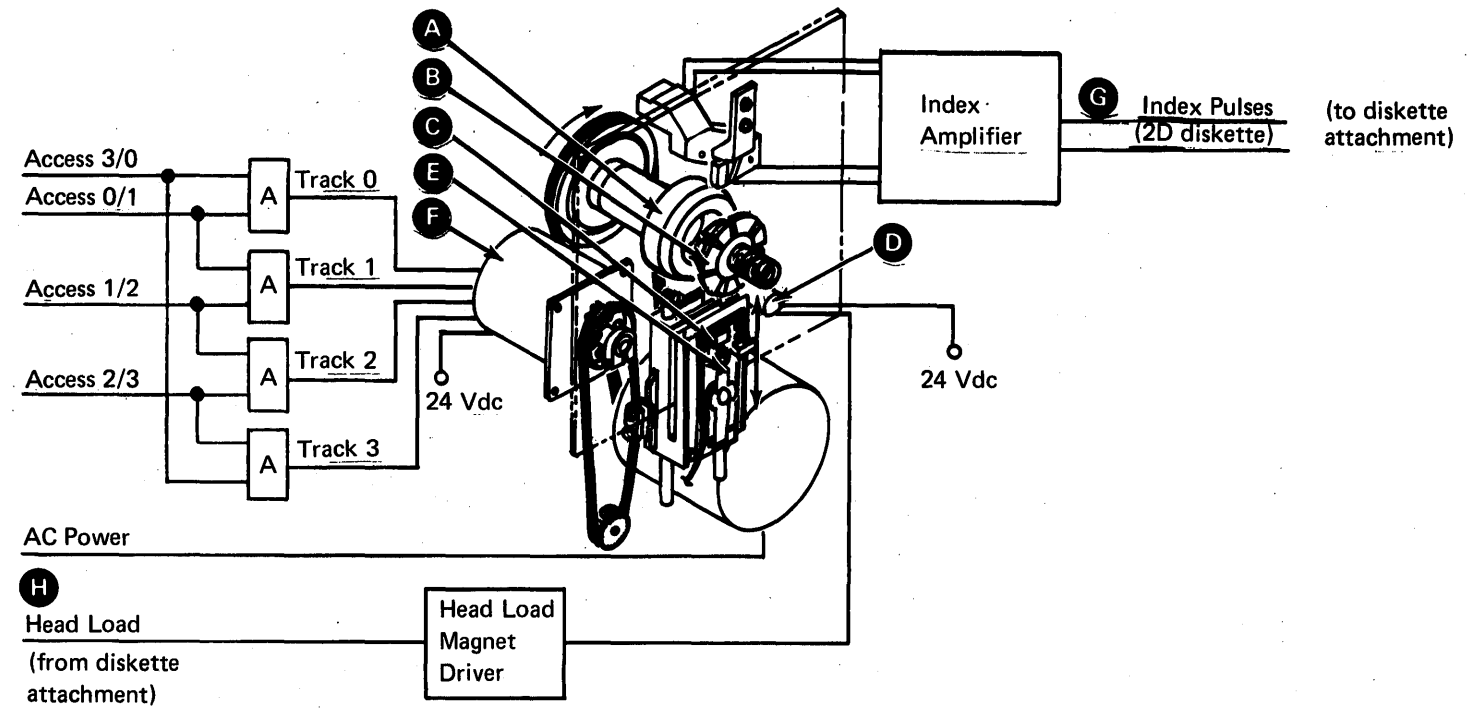
Example: The chart shows the data heads moving from track 2 to track 6. The access lines are activated for a minimum of 8.2 milliseconds to move the data heads across each track, and 32.8 milliseconds **M** to allow the data heads to settle on the last track.

3. At the end of a seek operation, two access lines remain active. The two access lines keep the stepper motor stopped, which keeps the data heads on track.

Read or Write Operation

To load the data heads and write on or read from the diskette:

1. The control storage program issues a data head load command **H** before a read or write operation. This activates the data head load solenoid **D**, which pushes the data heads **C** against the diskette. Data is valid after 80 milliseconds (time for the data heads to load).
2. The control storage program issues a read or write command **J**.
3. The control storage program issues a command to unload the heads **K** 335 milliseconds after a seek, read, or write operation is complete (if no other operation is issued during the 335 milliseconds). This decreases wear on the diskette and the data heads. The 335-millisecond delay occurs because during normal diskette use, the next diskette operation usually starts during the 335-millisecond delay. Therefore, the data heads do not have to be loaded before each operation.



Modified Frequency Modulation Read and Write Circuits

Note: The 53FD can also read and write in FM mode. See *Frequency Modulation Read and Write Circuits* earlier in this section.

Writing

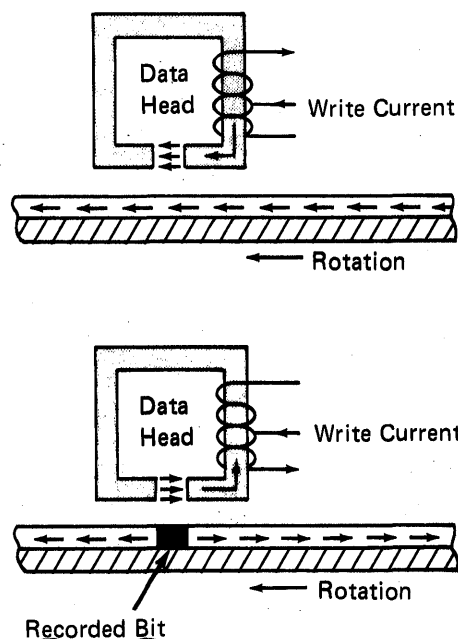
During a write operation, a clock bit or a 1-bit (data) is recorded by reversing the direction of the current in the data head coil, which reverses the direction of the magnetic flux in the gap. When the direction of flux reverses on the diskette surface, either a clock bit or a 1-bit is recorded.

Writing Data Bits

For each change on the 'diskette write data' line (A), a clock bit or a 1-bit is written on the diskette.

Data bits (1-bits) are always written in the center of the bit cell. If two bit cells in a row do not contain data bits, a clock (sync) bit is written at the start of the second bit cell. By writing hexadecimal 8B, data bits and clock bits can be shown.

These changes cause the current in the data head to be switched, which results in a polarity change on the diskette track.

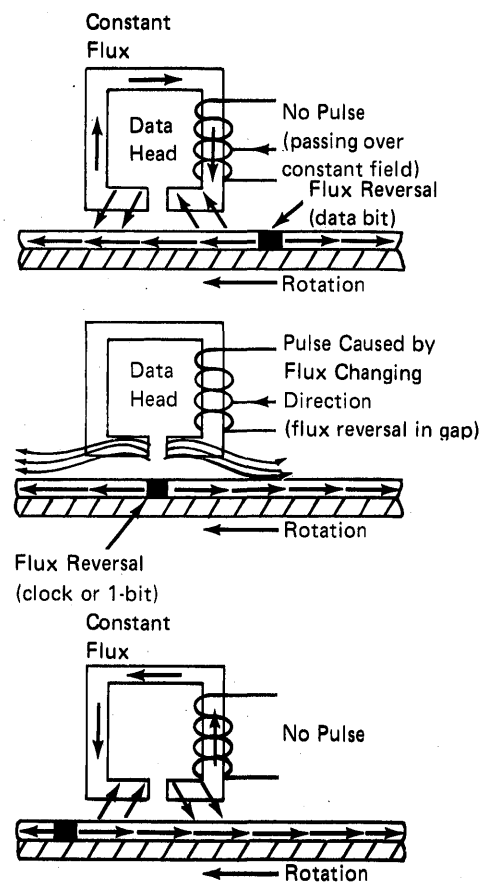


Reading

During a read operation, with the recording surface magnetized in one horizontal direction, constant flux flows and the coil senses no output voltage. However, when a recorded clock bit or 1-bit (180 degrees horizontal flux reverse) passes the gap, the flux moving through the ring and coil also reverses and causes a voltage output pulse.

Reading Data Bits

When data is read from the diskette (B), the read clock is synchronized to the incoming data by the variable frequency oscillator sync field. This field is 12 bytes of clock bits.



Controls

The 'select head 1' line (C) selects either head 1 or head 0.

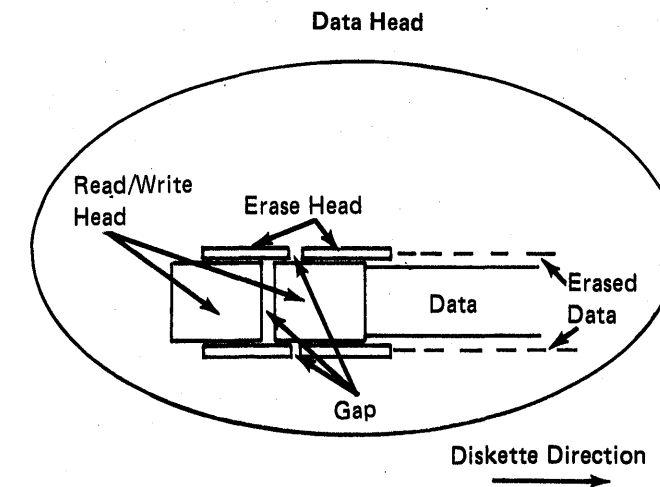
The 'write gate command' line (D) is active during a write operation. This line lets current flow through the selected data head (E) and de-activates the read circuits.

The 'diskette erase gate' line (F) also is active during a write operation. This line causes the edges of the data track to be erased, which leaves a gap between tracks (removes old data that may exist between tracks).

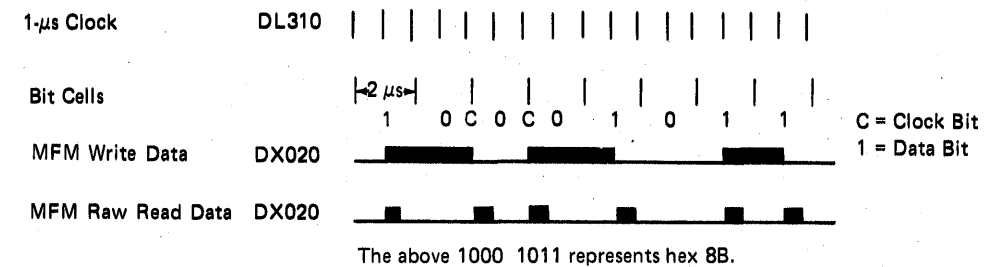
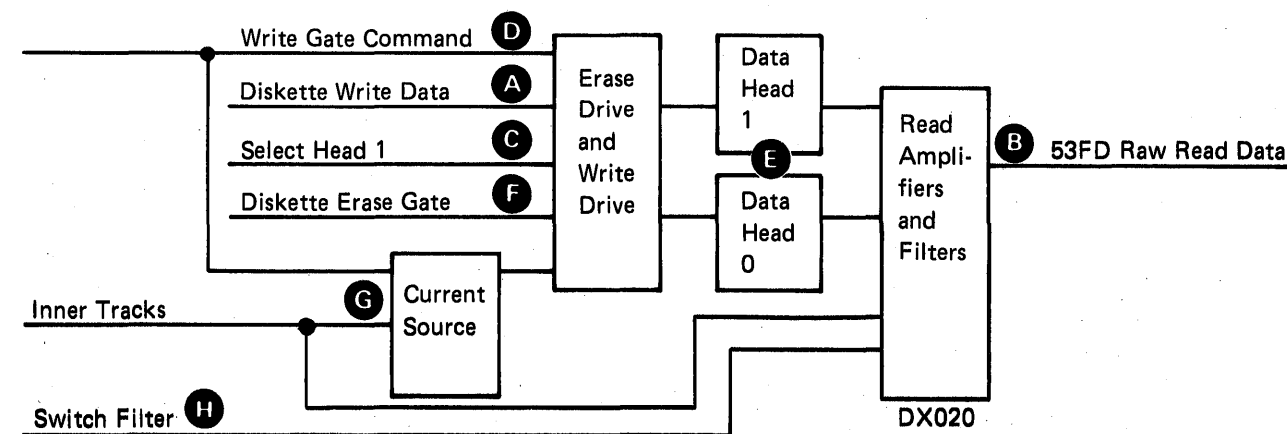
When the 'write gate command' line is not active, the write circuits are not gated and the read circuits are ready to read.

The 'inner tracks' line (G) is active from track 43 through track 76. When this line is active during a write operation, the write current through the data head is decreased because the bit density increases toward the center tracks and, therefore, less write current is needed. When this line is active during a read operation, read filters compatible with tracks 43 through 76 are enabled.

The 'switch filter' line (H) is active from track 60 through track 76. When this line is active during a read operation, read filters compatible with tracks 60 through 76 are enabled. This line is not used during a write operation.



53FD File Control Card



Diskette 2D Format

There are 77 tracks written in modified frequency modulation mode on each side of the Diskette 2D surface. A track is a circular path on the surface of the diskette. Two tracks, one on each side of the diskette, that can be read or written without moving the data head make up a cylinder. The cylinders are numbered 00 through 76. Cylinder 00 is the outside cylinder and cylinder 76 is the inside cylinder.

Of the 77 cylinders, only 74 cylinders are data cylinders. Track 0 of cylinder 00 is a label track written in FM mode. Track 1 of cylinder 00 is an extension of the label track written in MFM mode. Cylinders 75 and 76 are reserved and are used in place of cylinders that become damaged.

The damaged cylinder is flagged by writing binary 1's in all ID fields of that cylinder. The ID that would have been used on the damaged cylinder is written in the ID field of the next physical cylinder. When the ID field of a damaged cylinder is read, the data head automatically moves to the next higher numbered physical cylinder.

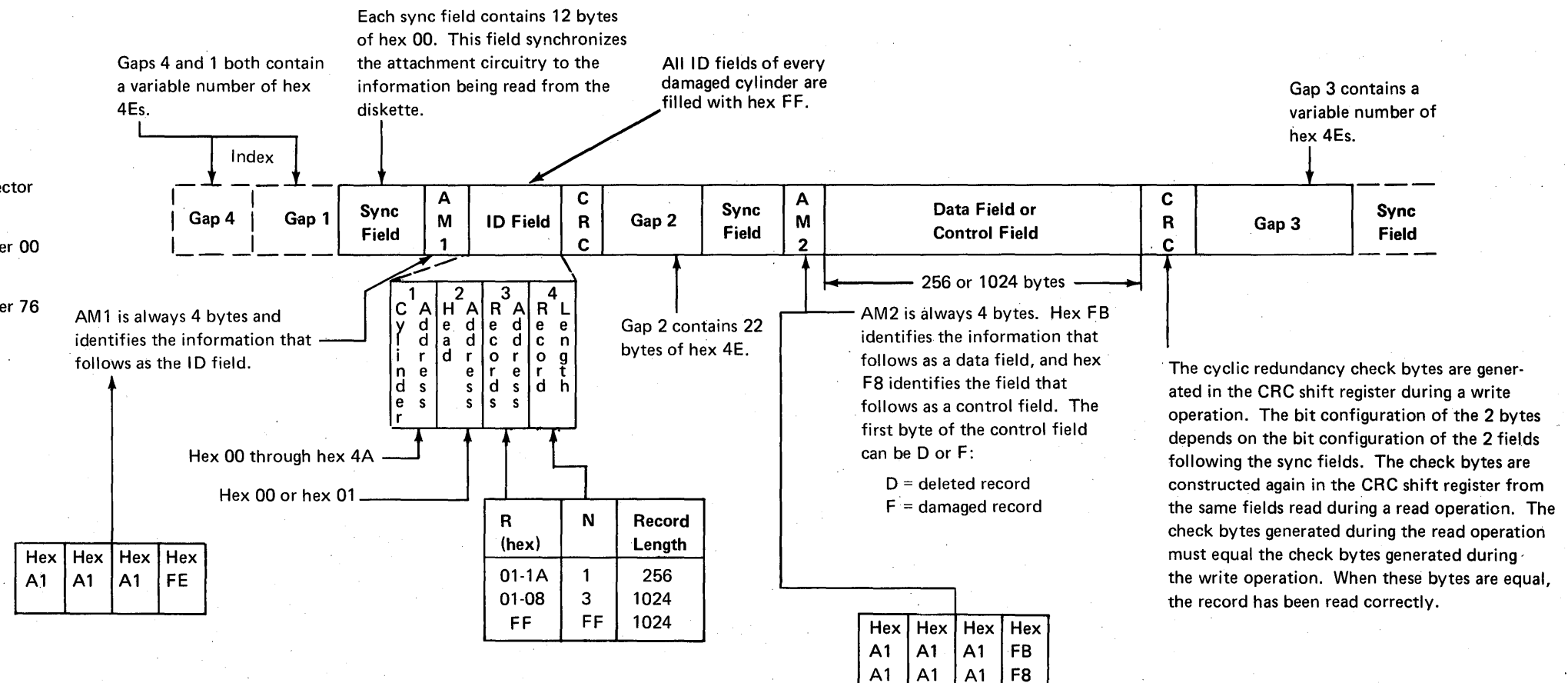
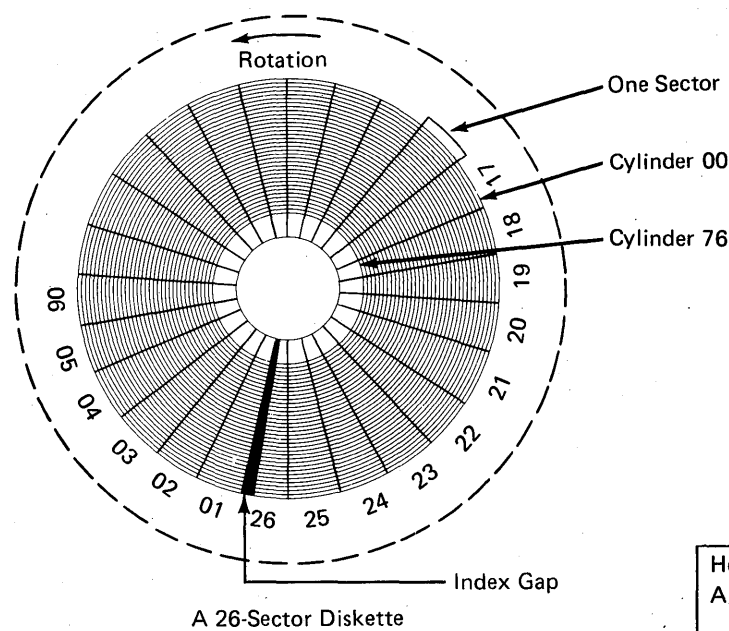
Each track is divided into either 8 or 26 sectors:

Format	Sectors per Track	Bytes per Sector for FM (Diskette 1)	Bytes per Sector for MFM (Diskette 2D)
2	8	512	1,024
1	26	128	256

The data stored in one sector is a record. Data can be recorded in frequency modulation mode on a Diskette 1 by either the 33FD or the 53FD diskette drive; or, data can be recorded in modified frequency modulation mode on a Diskette 2D by the 53FD diskette drive.

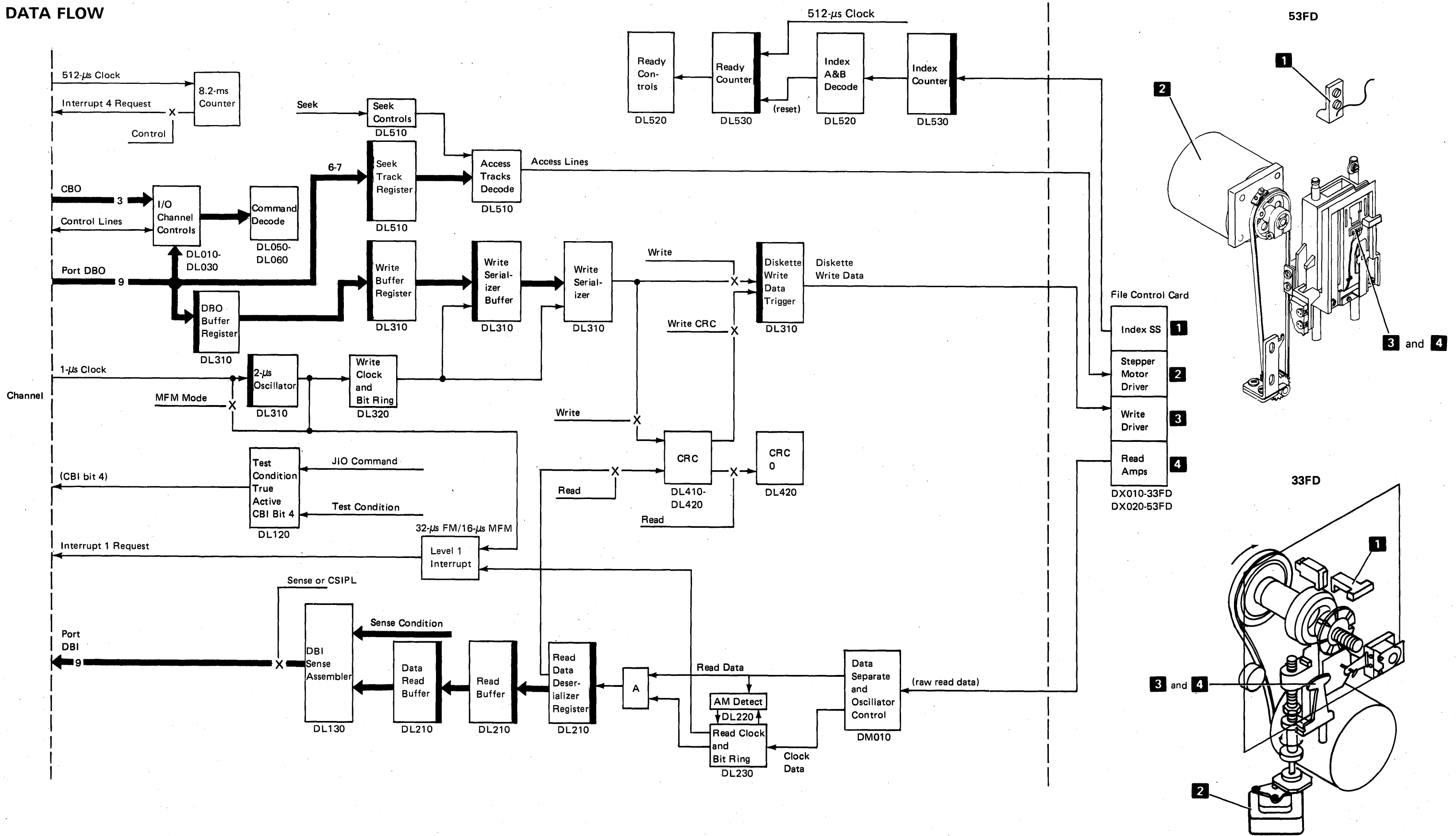
The contents of each sector are described as follows:

- Some diagnostic programs write one 4,096-byte sector in frequency modulation mode on track 00. Therefore, record length can be 128, 256, 512, 1,024, or 4,096 bytes. The value of n recorded in the record length byte indicates the record length.
- Each record on the diskette has its track and sector address recorded at the physical location of the record on the diskette.
- Diskettes that contain recorded sector identification fields (addresses) for each sector are known as initialized diskettes. Each sector has two parts; the first part contains the sector identification field, and the second part contains the data record or the control record field.



This page intentionally left blank.

DATA FLOW



OPERATIONS

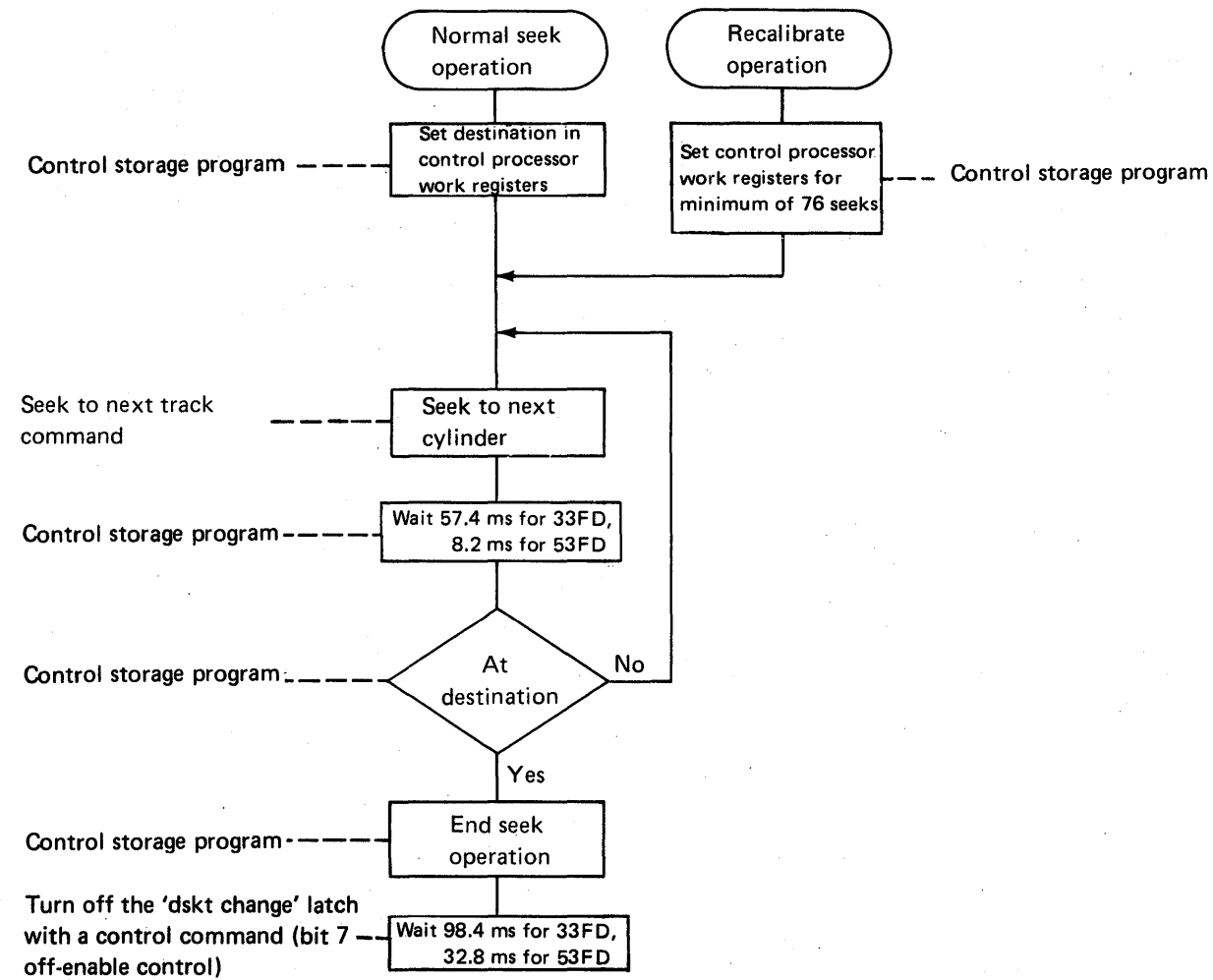
Seek Operations

The diskette drive seek operations are:

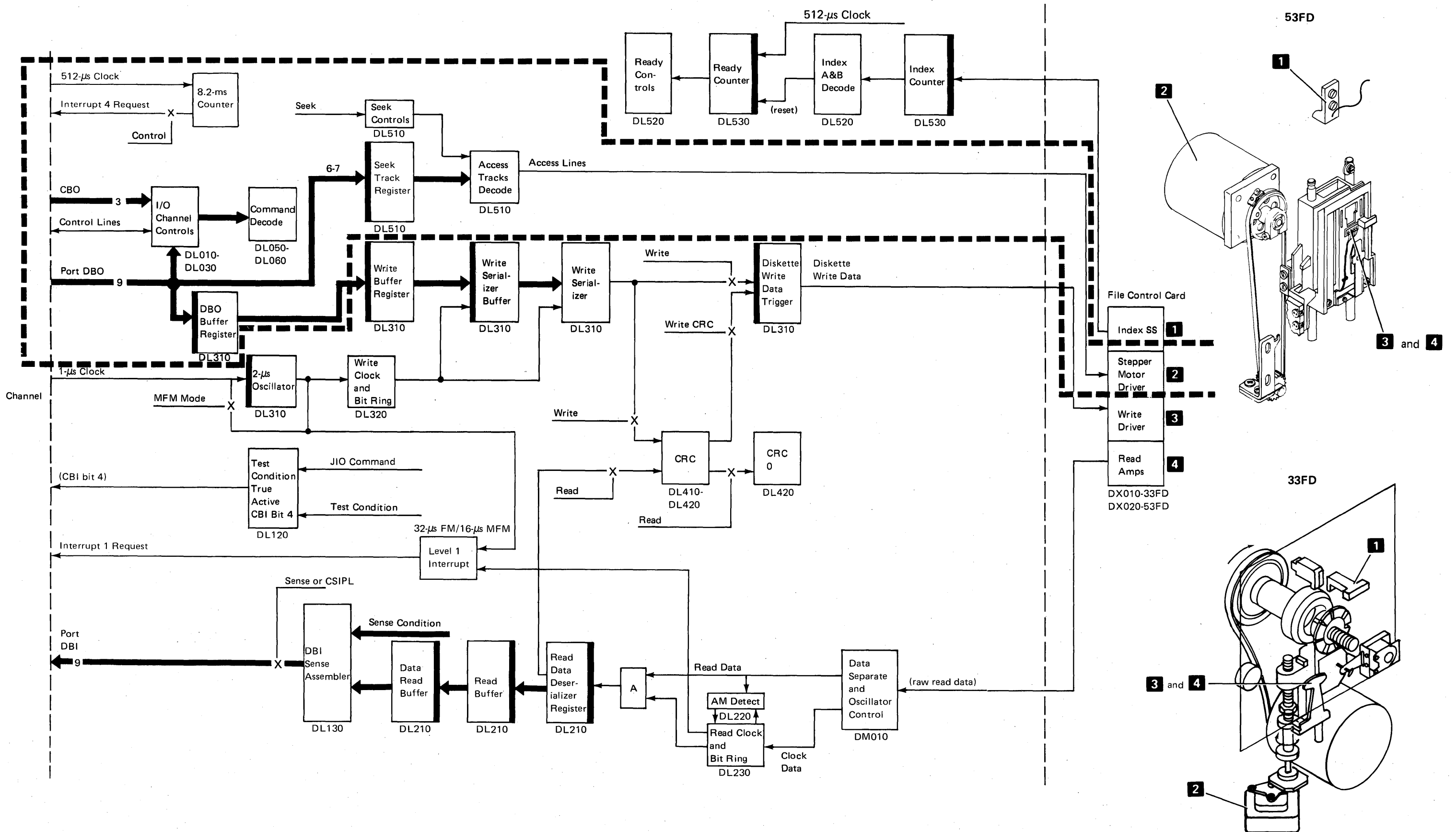
- Normal Seek: Seek from the present known cylinder to a specified cylinder.
- Recalibrate: Seek from the present location (location not known) to cylinder 00.

In either case, the control storage program controls the seek operation. The control storage program must know the cylinder location of the data head(s) before starting the operation (except for recalibration) and also must know the specified cylinder. The control processor issues a seek command, which starts a seek operation. The seek operation moves the data head(s) one cylinder per command until the specified cylinder is reached or the operation is ended.

The recalibrate operation is necessary when the cylinder location of the data head is not known. The control storage program sets up a reverse seek of a minimum of 76 cylinders. Because there are only 77 cylinders on the diskette, this reverse seek is enough to drive the data head(s) to cylinder 00 from any location. After driving the data head(s) to cylinder 00, the access mechanism comes against the lower-limit stop.



Seek Data Flow



Read Operation

The flowchart describing the reading of one sector from the diskette is shown on the next page. For more details on the read operation, see *Read Data Flow* later in this section.

The major control in the attachment for the read operation is the 'read data command' latch. This latch is on twice to read one sector (assuming a good identification field and data field): once to find and read the sector identification field, and once to find and read the data field. In either case, the 'read data command' latch remains on until the cyclic redundancy check bytes are read.

After the reading of bytes has started, the control storage program must take 1 byte once each 32 microseconds in frequency modulation mode or once each 16 microseconds in modified frequency modulation mode. If the control storage program does not take the bytes quickly enough, a read overrun error occurs.

The read clock and read bit ring synchronize the attachment to the data being read. The read clock runs continuously except in diagnostic step mode. The read bit ring, however, runs only from the time an address mark byte is found until the cyclic redundancy check bytes have been read.

The 'byte sync found' latch turns on when the first data bit of the address mark byte is read. This latch remains on until the 'read data command' latch is reset or until the attachment has determined that the byte being read is not a valid address mark.

Valid address marks for frequency modulation mode are hexadecimal FE, F8, or FB without read clock pulses at bit ring 2, 3, and 4 times. Hexadecimal FE is the address mark before the identification field; hexadecimal F8 is the address mark before a control field; and, hexadecimal FB is the address mark before a data field. An address mark that is not valid is one that:

- Is missing data bit 0, 1, 2, 3, or 4
- Is missing a clock bit ring 1, 5, 6, or 7 time
- Has a clock pulse at bit ring 2, 3, or 4 time

The first byte following a control address mark can be either a D or an F:

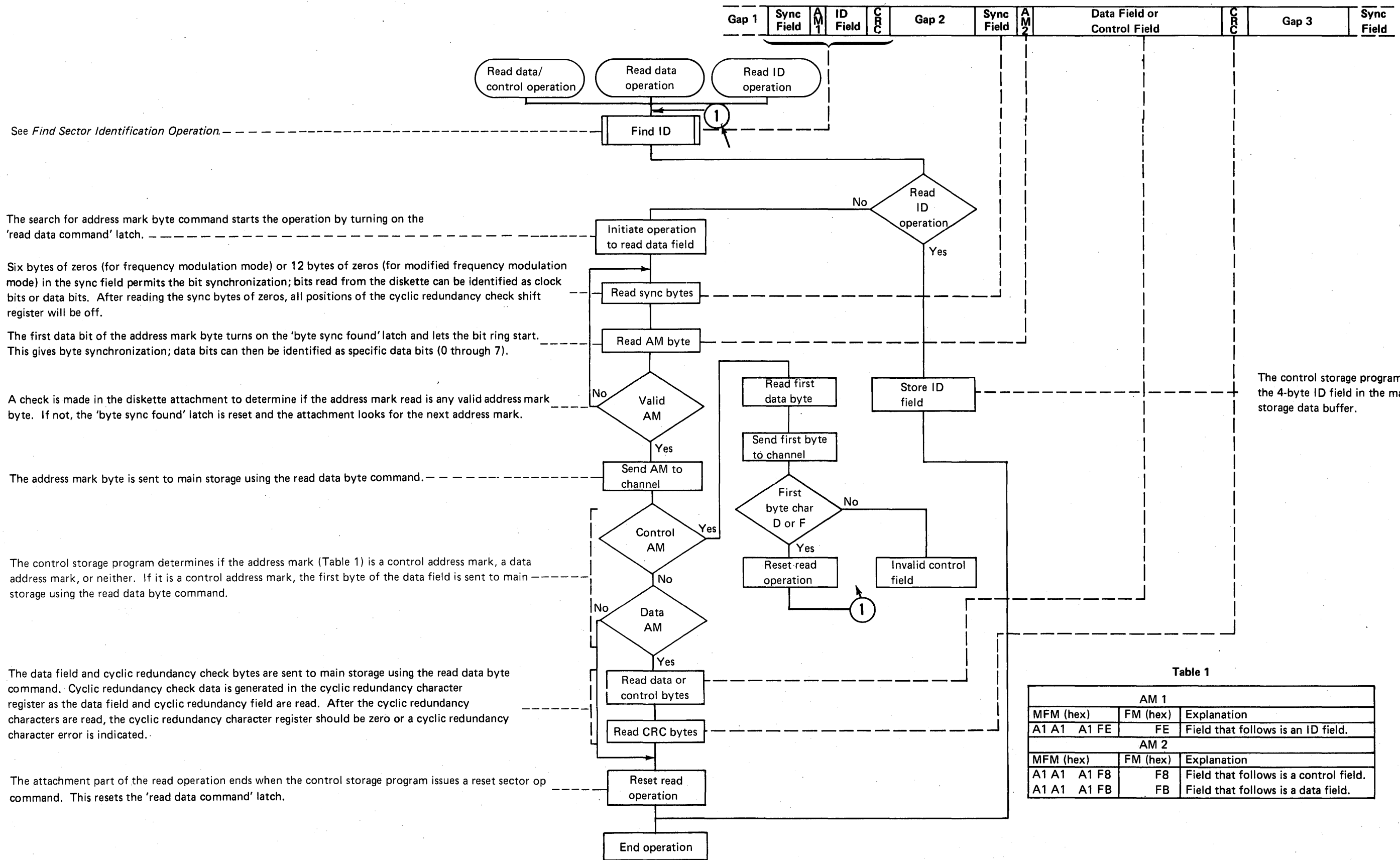
D = deleted record

F = damaged record

Valid address marks for modified frequency modulation mode are 4 bytes long. The first 3 bytes are hexadecimal A1's with missing clock bit 5. The fourth byte can be hexadecimal FE, F8, or FB. Hexadecimal FE is the address mark before the identification field; hexadecimal F8 is the address mark before a control field; and, hexadecimal FB is the address mark before a data field. The first byte following a control address mark can be either a D or an F:

D = deleted record

F = damaged record



See Find Sector Identification Operation.

The search for address mark byte command starts the operation by turning on the 'read data command' latch.

Six bytes of zeros (for frequency modulation mode) or 12 bytes of zeros (for modified frequency modulation mode) in the sync field permits the bit synchronization; bits read from the diskette can be identified as clock bits or data bits. After reading the sync bytes of zeros, all positions of the cyclic redundancy check shift register will be off.

The first data bit of the address mark byte turns on the 'byte sync found' latch and lets the bit ring start. This gives byte synchronization; data bits can then be identified as specific data bits (0 through 7).

A check is made in the diskette attachment to determine if the address mark read is any valid address mark byte. If not, the 'byte sync found' latch is reset and the attachment looks for the next address mark.

The address mark byte is sent to main storage using the read data byte command.

The control storage program determines if the address mark (Table 1) is a control address mark, a data address mark, or neither. If it is a control address mark, the first byte of the data field is sent to main storage using the read data byte command.

The data field and cyclic redundancy check bytes are sent to main storage using the read data byte command. Cyclic redundancy check data is generated in the cyclic redundancy character register as the data field and cyclic redundancy field are read. After the cyclic redundancy characters are read, the cyclic redundancy character register should be zero or a cyclic redundancy character error is indicated.

The attachment part of the read operation ends when the control storage program issues a reset sector operation command. This resets the 'read data command' latch.

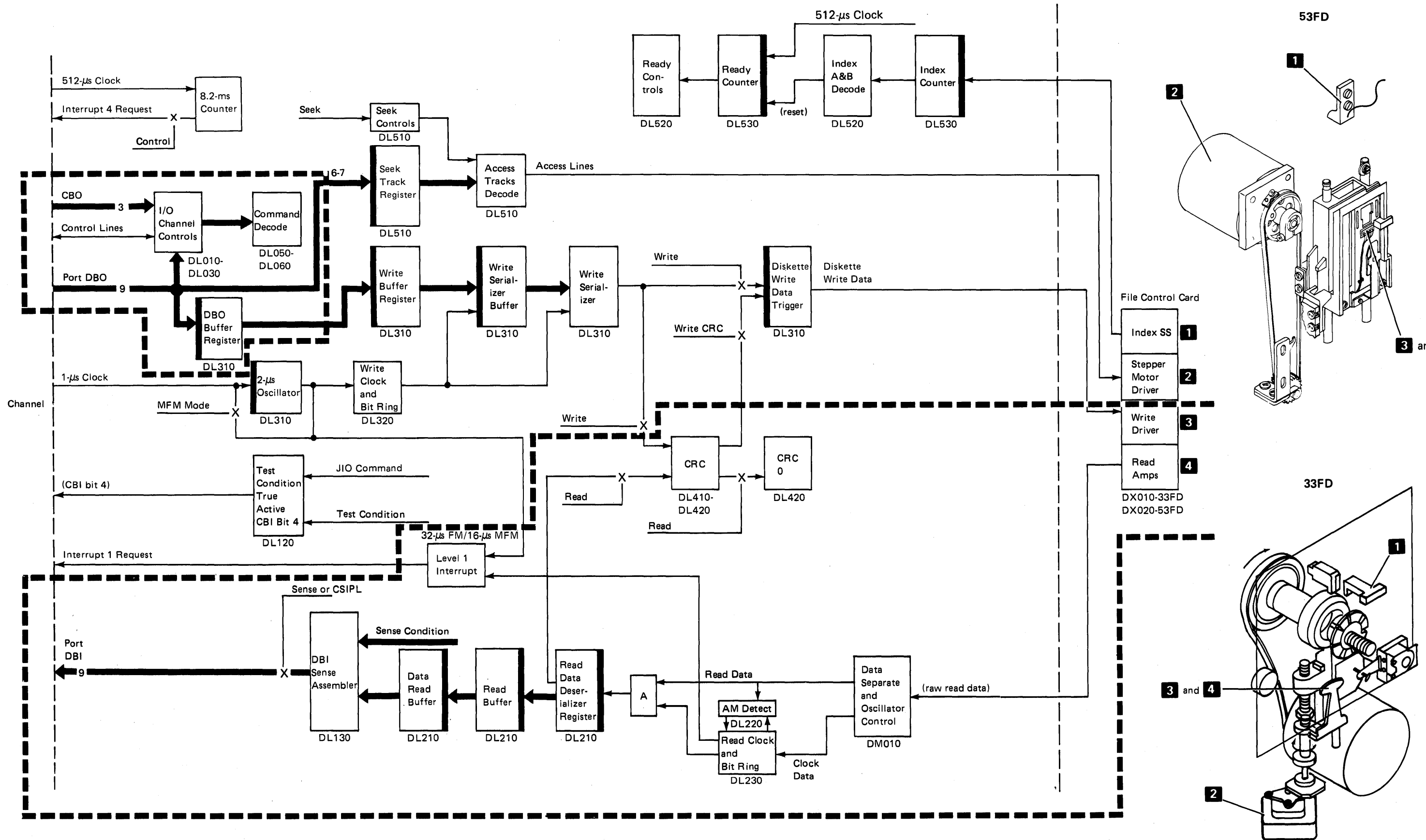
The control storage program stores the 4-byte ID field in the main storage data buffer.

Table 1

AM 1			
MFM (hex)	FM (hex)	Explanation	
A1 A1	A1 FE	FE	Field that follows is an ID field.
AM 2			
MFM (hex)	FM (hex)	Explanation	
A1 A1	A1 F8	F8	Field that follows is a control field.
A1 A1	A1 FB	FB	Field that follows is a data field.

This page intentionally left blank.

Read Data Flow



Diskette Drive and Attachment (Level 1) 8-17

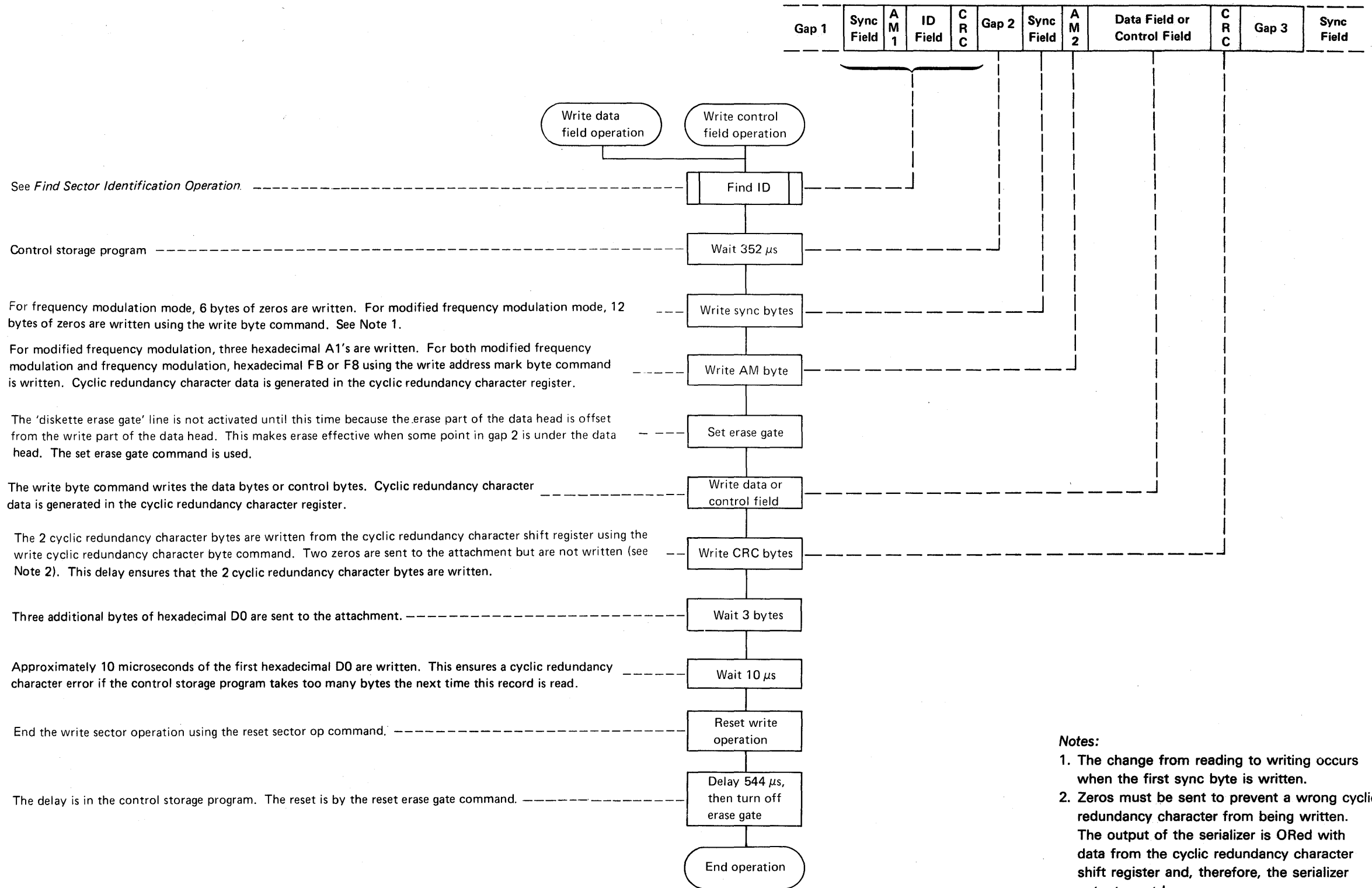
Write Operation

When writing one sector on the diskette, the fields written are controlled by the control storage program. One command is needed for each byte written. The control storage program also controls the needed delays.

After the writing of bytes has started, the control storage program must supply bytes quickly enough so they may be written once every 32 microseconds in frequency modulation mode or once every 16 microseconds in modified frequency modulation mode. If the control storage program does not send bytes quickly enough, a write overrun error occurs.

The major control in the attachment for the write operation is the 'write gate' latch. The 'write gate' latch remains on from the time the first sync byte is written until after the last cyclic redundancy check byte is written. The write clock and write bit ring run as long as the 'write gate' latch is on.

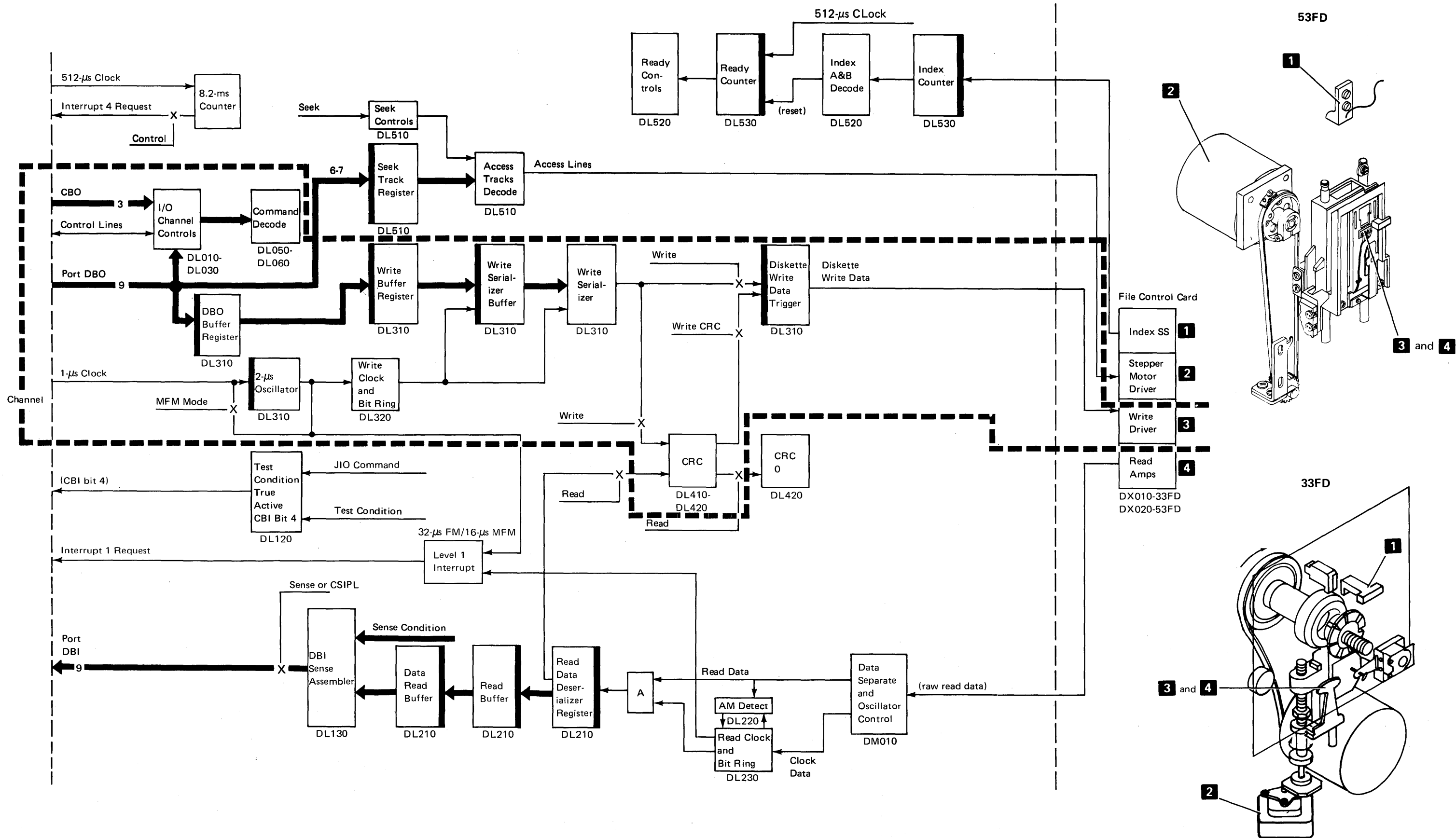
The write operation writes a record and reads the record that was written and compares it to the original record.



Notes:

1. The change from reading to writing occurs when the first sync byte is written.
2. Zeros must be sent to prevent a wrong cyclic redundancy character from being written. The output of the serializer is ORed with data from the cyclic redundancy character shift register and, therefore, the serializer output must be zeros.

Write Data Flow



Diskette Drive and Attachment (Level 1) 8-19

Find Sector Identification Operation

The find sector identification operation proceeds as follows:

1. The attachment synchronizes the read clock and read bit ring with the bits being read from the diskette.
2. The control storage program sends the sector identification field to the control processor.
3. The control storage program compares the sector identification field being searched for and the one found.

This flowchart describes the find sector identification operation. This operation can be started with the heads at any position on the diskette. The operation continues reading from the diskette until a valid address mark is found or until the control storage program determines that the sector identification being searched for is not on the track being read.

The major controls in the attachment for the find sector identification operation are the 'read data command' latch and the 'byte sync found' latch. The 'read data command' latch remains on until the last cyclic redundancy character byte of the sector identification field has been read. The 'byte sync found' latch turns on when the first data bit of the address mark is read. This latch is on until the attachment determines that the byte being read is not a valid address mark.

The valid address mark before the identification field (see Table 1 in the flowchart) for frequency modulation mode is hexadecimal FE without read clock pulses at bit ring 2, 3, and 4 times. Hexadecimal FE is the address mark before the identification field; hexadecimal F8 is the address mark before a control field; and, hexadecimal FB is the address mark before a data field. An address mark that is not valid is one that:

- Is missing data bit 0, 1, 2, 3, or 4
- Is missing a clock bit at bit ring 1, 5, 6, or 7 time
- Has a clock pulse at bit ring 2, 3, or 4 time

The controls for the find sector identification operation are shown in the flowchart.

The valid address marks before the identification field for modified frequency modulation mode are 4 bytes long. The first 3 bytes are hexadecimal A1's with missing clock bit 5.

The fourth byte is hexadecimal FE (see Table 1 in the flowchart) without read clock pulses at bit ring 2, 3, and 4 times. An address mark that is not valid is one that:

- Is missing data bit 0, 1, 2, 3, or 4
- Is missing a clock bit at bit ring 1, 5, 6, or 7 time
- Has a clock pulse at bit ring 2, 3, or 4 time

For more information, see *Find Sector Identification Data Flow* later in this section.

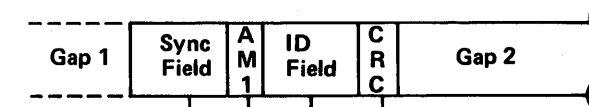
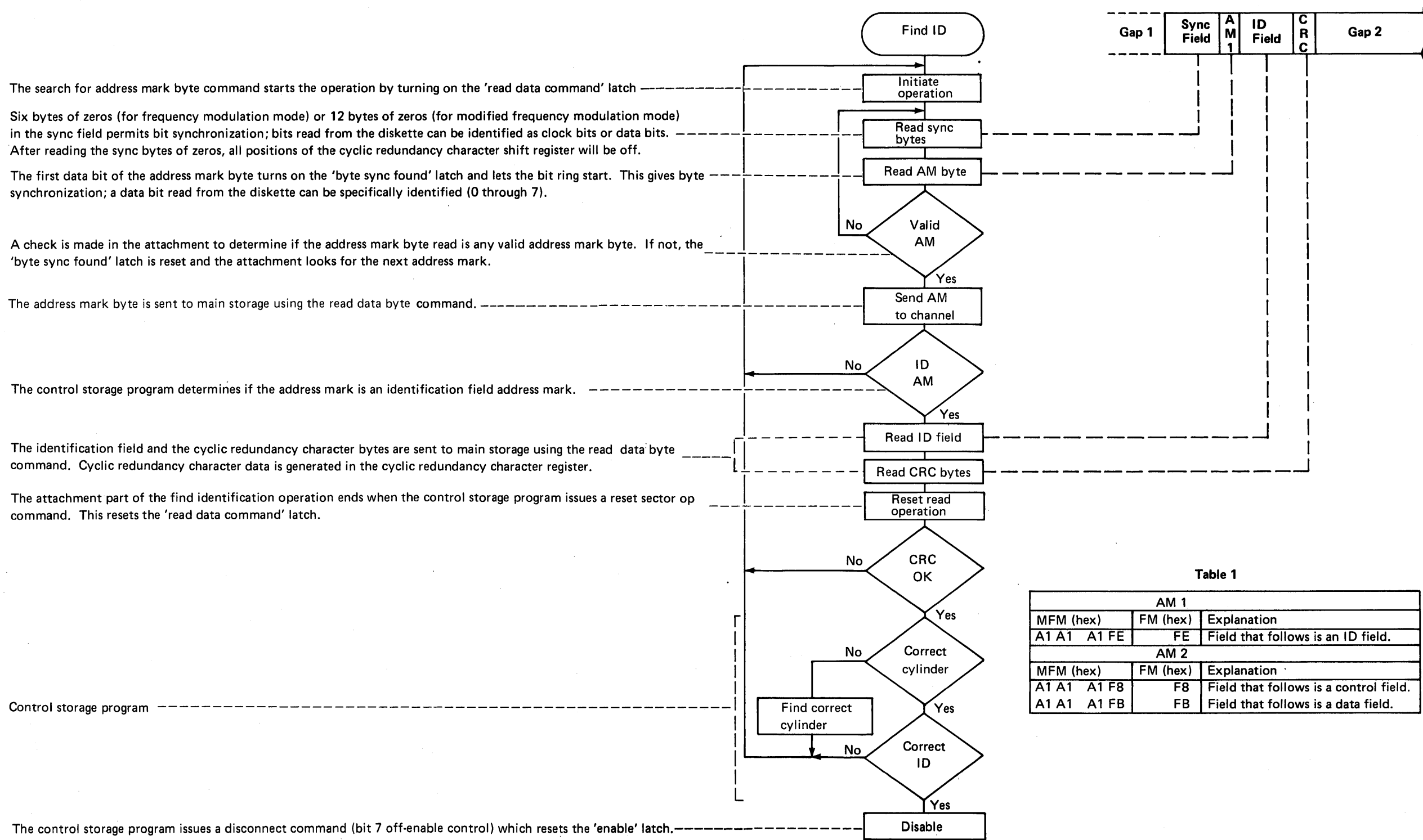
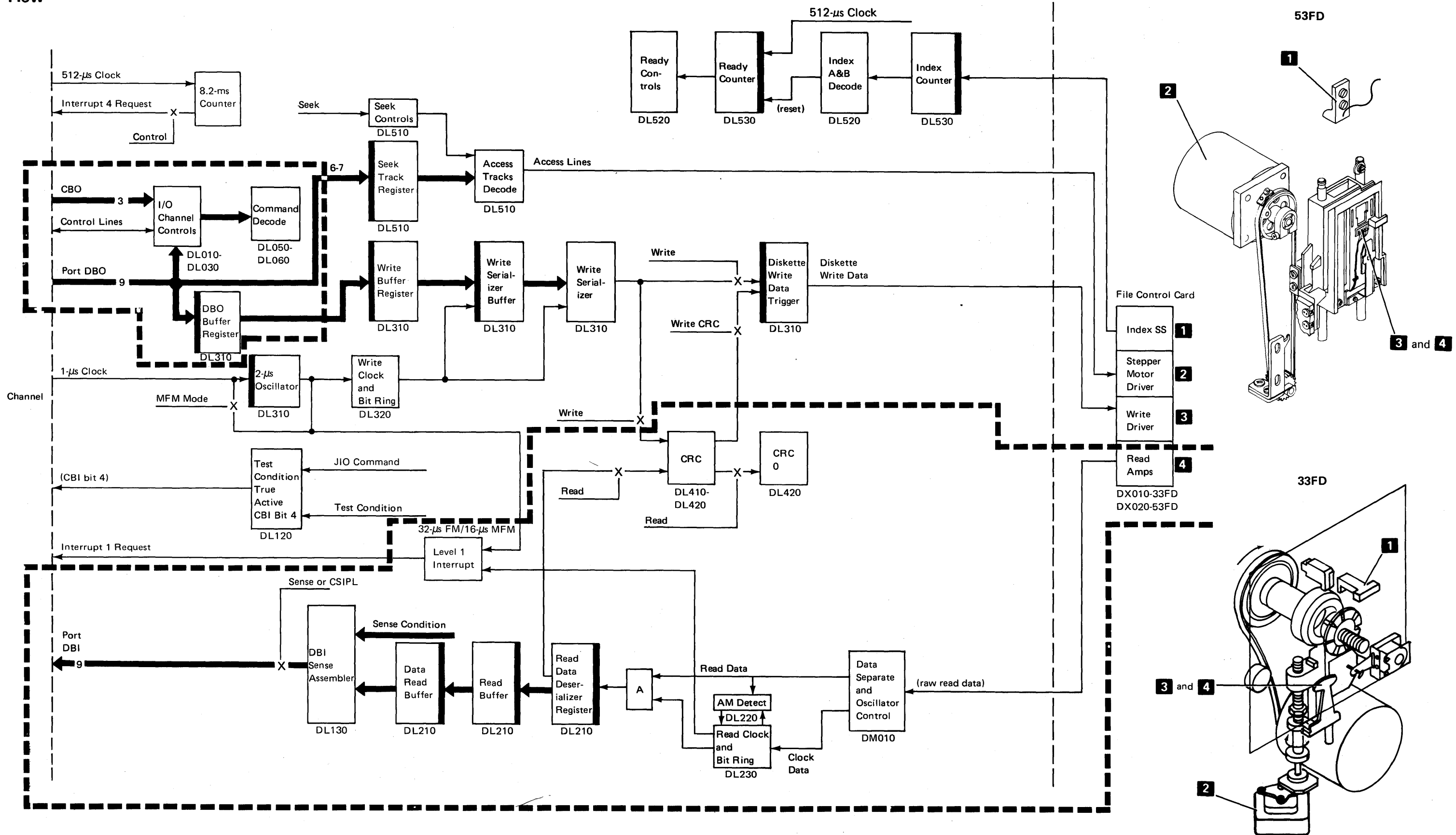


Table 1

AM 1		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 FE	FE	Field that follows is an ID field.
AM 2		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 F8	F8	Field that follows is a control field.
A1 A1 A1 FB	FB	Field that follows is a data field.

This page intentionally left blank.

Find Sector Identification Data Flow



Diskette Drive and Attachment (Level 1) 8-23

Write Sector Identification Operation

This flowchart describes the write sector identification operation. This operation is used during initialization of a diskette. During this operation, an 8- or 26-sector format is initialized. During the initialization process, each data field is written with the same data field

from main storage. The data flow for the write sector identification operation is the same as for the write operation and is shown on the next page.

Write sector identification is controlled by the control storage program. After writing has started, the control storage program must

supply bytes quickly enough so they may be written once every 32 microseconds for frequency modulation mode or once every 16 microseconds for modified frequency modulation mode. If the control storage program does not send bytes quickly enough, a write overrun error occurs.

The major control in the attachment for the write sector identification operation is the 'write gate' latch. The 'write gate' latch remains on from the time the first bytes are written until the last 2 cyclic redundancy check characters are written. Hexadecimal 4E's are written in the last gap before the index. When the index is

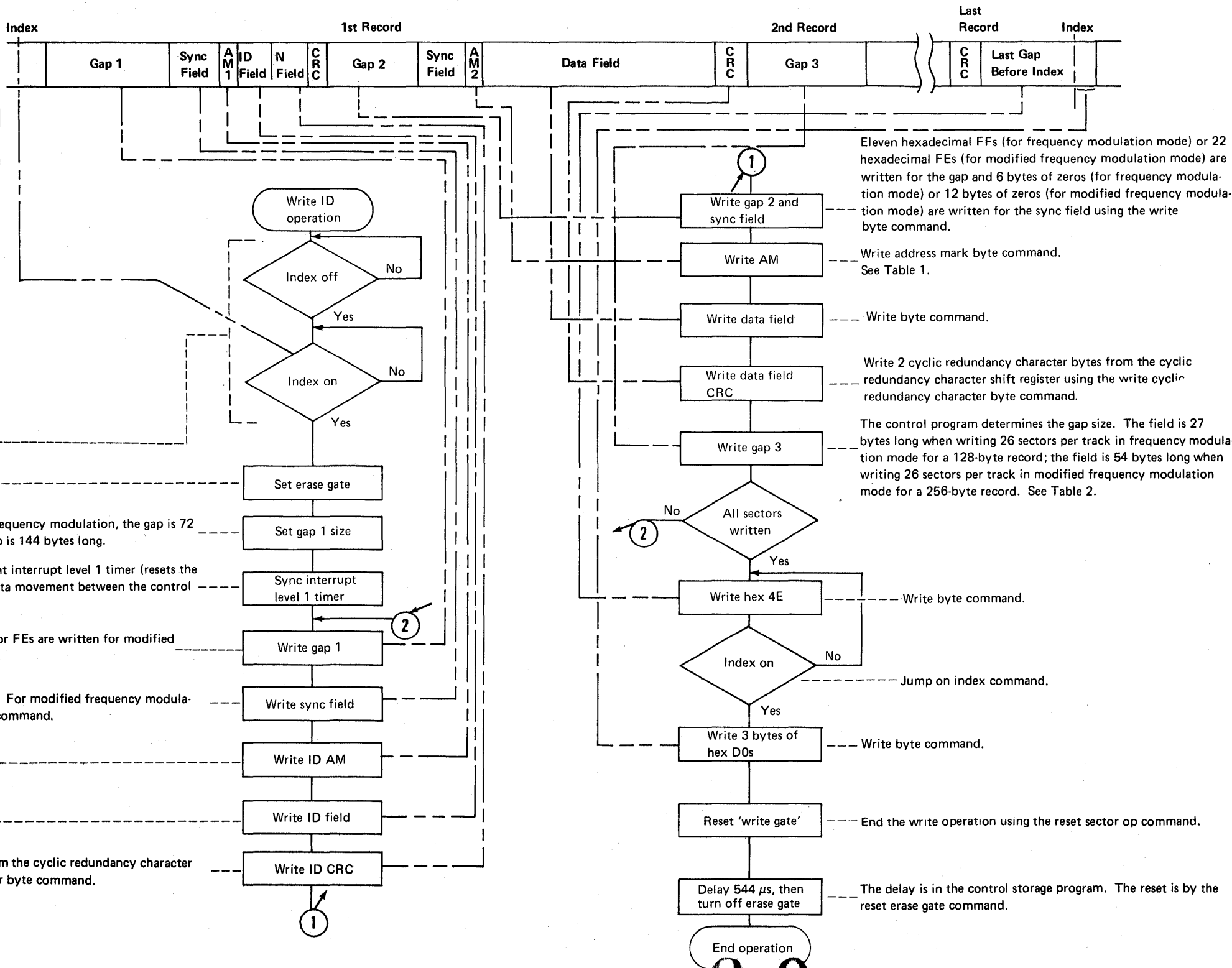
sensed, the 'write gate' latch is reset. The write clock and write bit ring run as long as the 'write gate' latch is on.

Table 1

AM 1		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 FE	FE	Field that follows is an ID field.
AM 2		
MFM (hex)	FM (hex)	Explanation
A1 A1 A1 F8	F8	Field that follows is a control field.
A1 A1 A1 FB	FB	Field that follows is a data field.

Table 2
Number of Sectors in Track

Bytes in Data Field	N Field	FM		MFM	
		FM	MFM	FM	MFM
128	0	26	27	27	54
256	1	8	8	58	116
512	2	8	8	58	116
1024	3	8	8	58	116
512	FF	8	8	58	116
1024	FF	8	8	58	116



Jump on I/O index pulse on command.

Set erase gate command.

The control storage program determines gap size. For frequency modulation, the gap is 72 bytes long. For modified frequency modulation, the gap is 144 bytes long.

The control storage program synchronizes the attachment interrupt level 1 timer (resets the timer) with the write bit ring zero. This synchronizes data movement between the control storage program and the attachment.

Hexadecimal FFs are written for frequency modulation or FEs are written for modified frequency modulation using the write byte command.

For frequency modulation, 6 bytes of zeros are written. For modified frequency modulation, 12 bytes of zeros are written using the write byte command.

Write address mark byte command. See Table 1.

Write byte command.

The 2 cyclic redundancy character bytes are written from the cyclic redundancy character shift register using the write cyclic redundancy character byte command.

Eleven hexadecimal FFs (for frequency modulation mode) or 22 hexadecimal FEs (for modified frequency modulation mode) are written for the gap and 6 bytes of zeros (for frequency modulation mode) or 12 bytes of zeros (for modified frequency modulation mode) are written for the sync field using the write byte command.

Write address mark byte command. See Table 1.

Write data field

Write 2 cyclic redundancy character bytes from the cyclic redundancy character shift register using the write cyclic redundancy character byte command.

The control program determines the gap size. The field is 27 bytes long when writing 26 sectors per track in frequency modulation mode for a 128-byte record; the field is 54 bytes long when writing 26 sectors per track in modified frequency modulation mode for a 256-byte record. See Table 2.

Write hex 4E

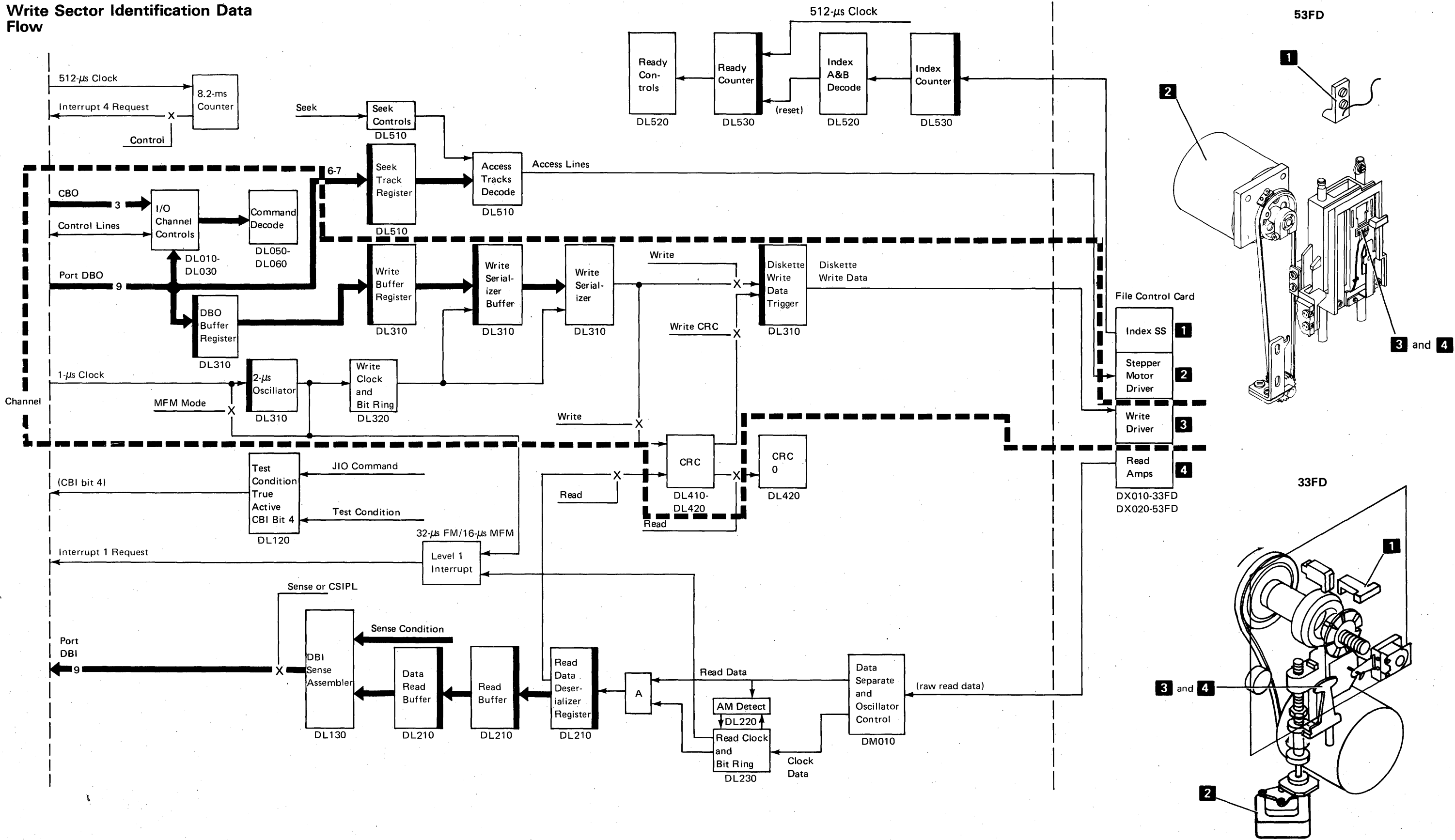
Jump on index command.

Write 3 bytes of hex D0s

Reset 'write gate'

The delay is in the control storage program. The reset is by the reset erase gate command.

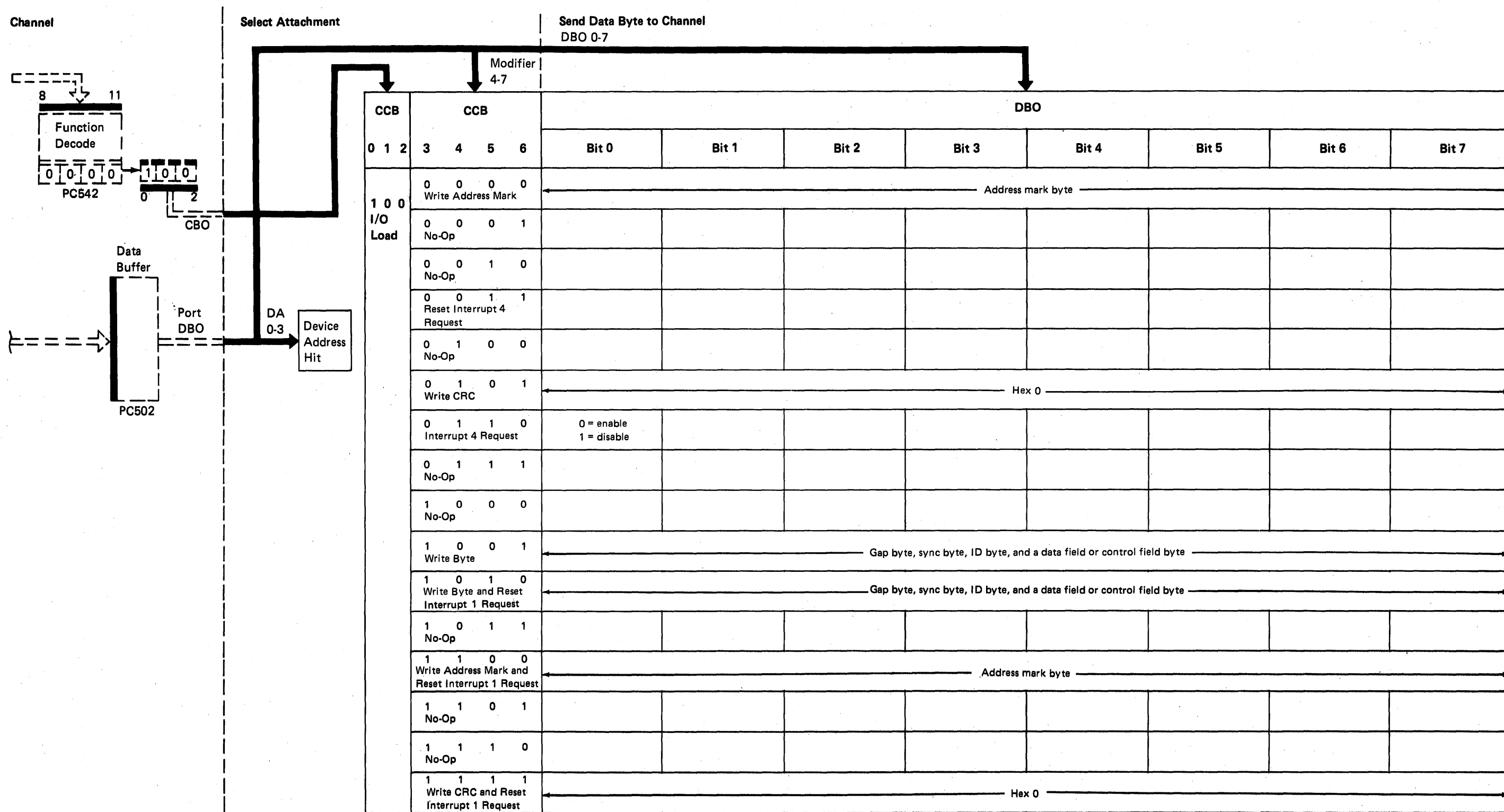
Write Sector Identification Data Flow



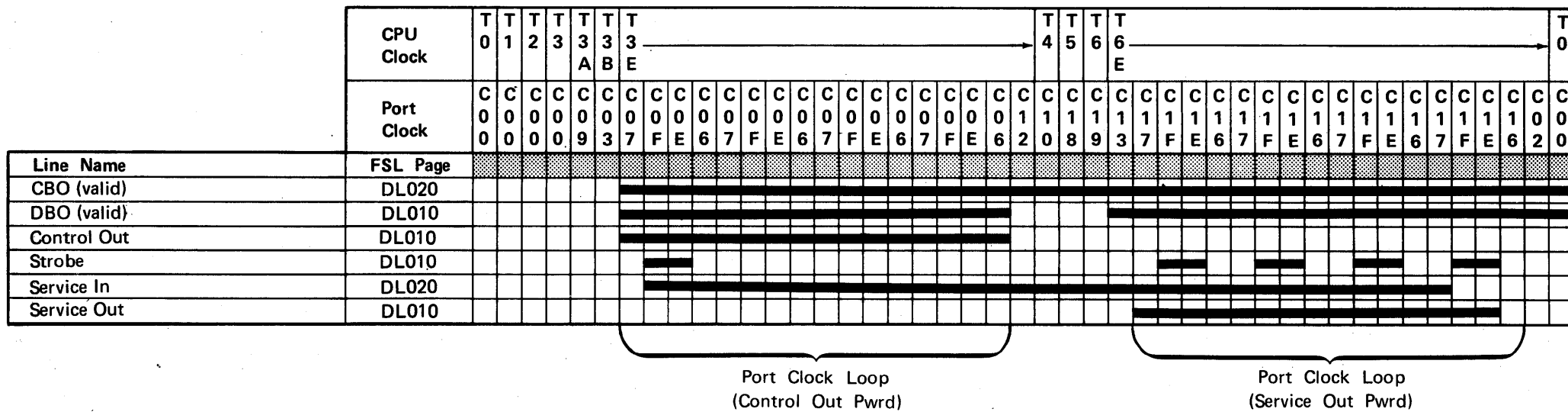
COMMANDS

I/O Load Command

The I/O load command sends 1 byte of information from the control processor to the attachment. See *Commands* in the *Channel* section of this manual for a description of how this command is executed.

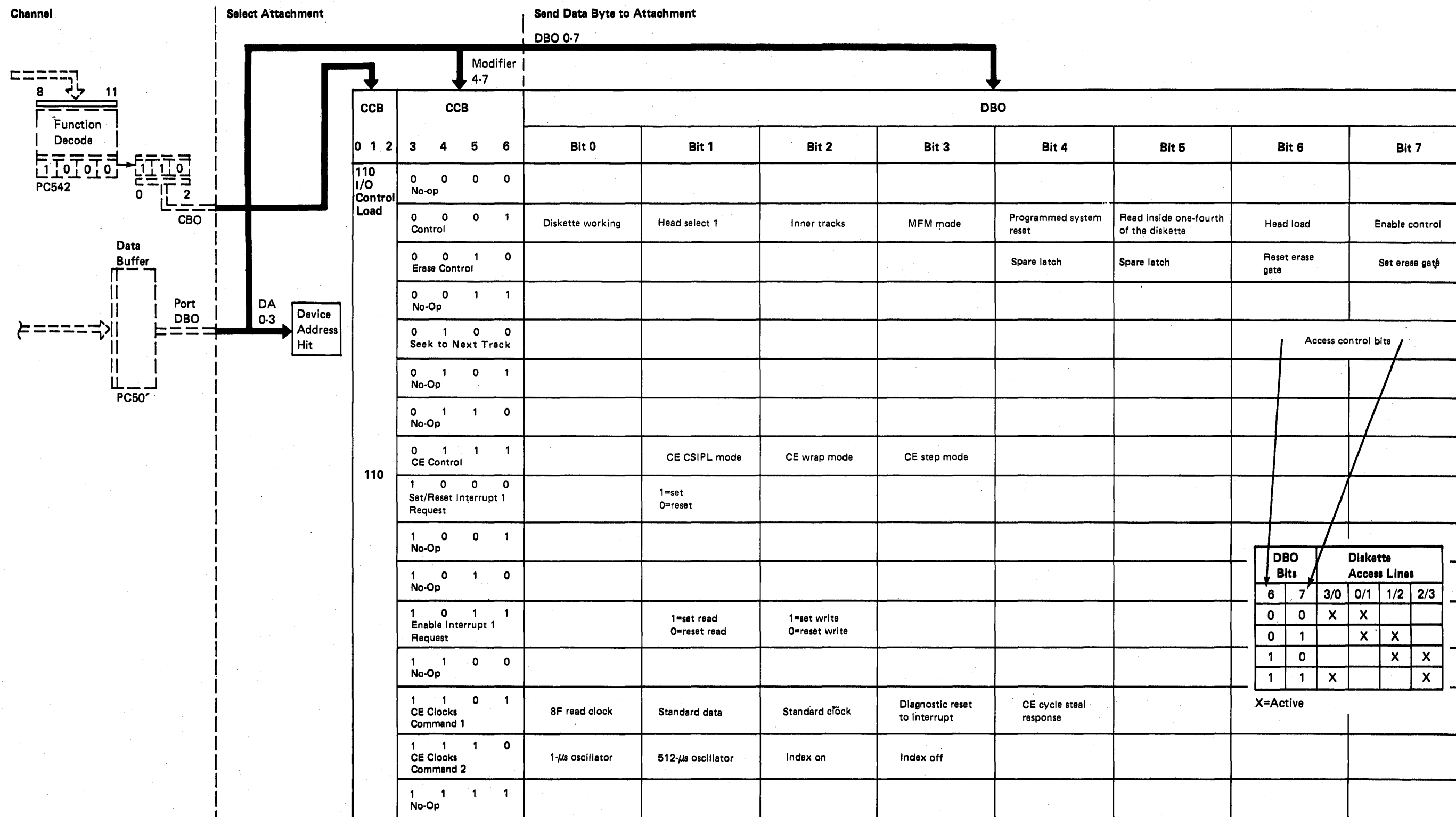


Modifier (DBO 4-7)	DBO Bits	Command	Action Taken	FSL Page
0 0 0 0	0-7	Write address mark	Sets the 'write AM' latch. This gates the address mark write buffer.	DL061
0 0 1 1	—	Reset interrupt 4 request	Resets the 'interrupt 4 request' latch.	DL071
0 1 0 1	0-7	Write CRC	Sets the 'write CRC' latch. This allows writing the 'write CRC' byte from the CRC register.	DL061
0 1 1 0	0	Interrupt 4 request	Turns the 'seek/head load enable' latch on. This enables the 'interrupt 4 request' latch.	DL071
1 0 0 1	0-7	Write byte	Sets the 'write gate' latch on. This starts the write bit ring and gates the writing of the gap byte, sync byte, ID byte, and a data field or control field byte.	DL061
1 0 1 0	0-7	Write byte and reset interrupt 1 request	Sets the 'write gate' latch on. This starts the write bit ring and gates the writing of the gap byte, sync byte, ID byte, and a data field or control field byte. Also, resets the 'interrupt 1 request' latch.	DL072
1 1 0 0	0-7	Write address mark and reset interrupt 1 request	Gates the writing of the address mark and resets the 'interrupt 1 request' latch.	DL072
1 1 1 1	0-7	Write CRC and reset interrupt 1 request	Gates the writing of 1 CRC character byte and resets the 'interrupt 1 request' latch.	DL072

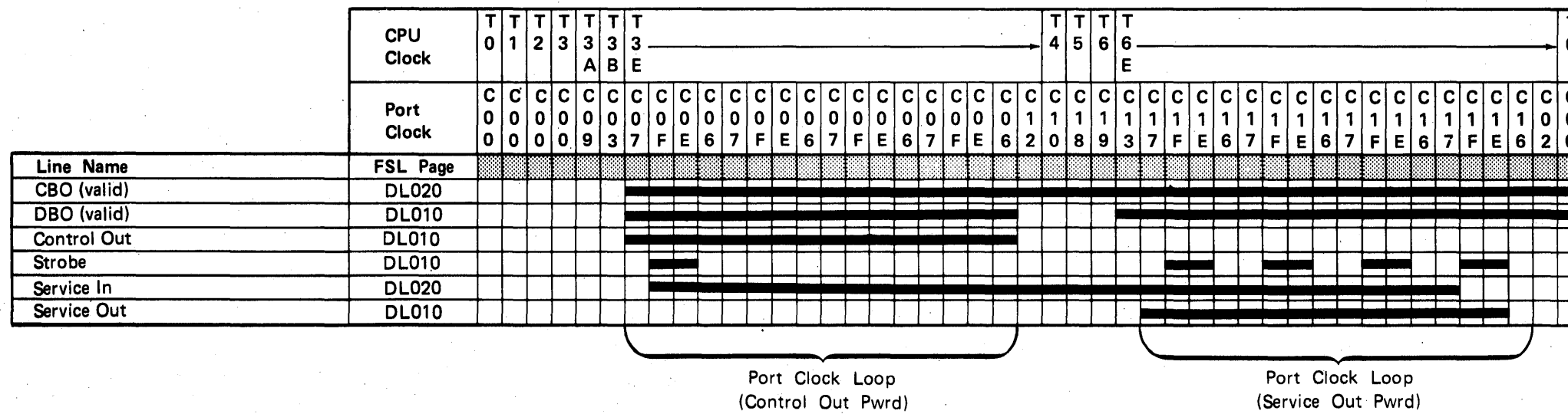


I/O Control Load Command

The I/O control load command sends 1 byte of control information from the control processor to the attachment. See *Commands* in the *Channel* section of this manual for a description of how this command is executed.



Modifier (DBO 4-7)	DBI Bits	Command	Action Taken	FSL Page
0 0 0 1	0-7	Control	Sends 1 byte of control information from the control processor to the attachment.	DL061
0 0 1 0	4-7	Erase control	Sets or resets the 'erase gate' latch. This gates erase current to the data head during write operations.	DL061
0 1 0 0	6-7	Seek to next track	Controls the stepper motor drive lines. One seek to next track command moves the data head one track in either direction.	DL510
0 1 1 1	1,2,3	CE control	Sets various CE control latches for diagnostic purposes.	DL050
1 0 0 0	1	Set/reset interrupt 1 request	Sets and resets the 'interrupt 1 request' latch. DBO bit 1 on = set, DBO bit 1 off = reset.	DL072
1 0 1 1	1,2	Enable interrupt 1 request	Enables or disables the 'enable read interrupt' latch or the 'enable write interrupt' latch.	DL072
1 1 0 1	0-4	CE clocks command 1	Sets or resets various control latches for diagnostic purposes.	DL050
1 1 1 0	0-3	CE clocks command 2	Generates various advance pulses for diagnostic purposes.	DL050



Write Byte or Write Address Mark Byte Command

This command starts the following sequence of events:

1. The attachment receives a write byte or a write address mark byte command.
2. A data byte or an address mark byte is received on the data bus out and set in the data bus out buffer. A write byte command can write a gap byte, a sync byte, an identification byte, and a data byte or a control byte. A write address mark byte command can write only an address mark.
3. The byte is sent from the data bus out buffer to the write buffer.
4. The byte is sent to the serializer, and then the byte and the clock bits are written on the diskette.
5. The write address mark byte command drops 3 of the clock bits in frequency modulation mode and 1 of the clock bits in modified frequency modulation mode.

The I/O load command is received on the command bus out and remains there until the byte to be written is received by the attachment. The device address and modifier are received on the data bus out. The modifier is set in the modifier register and used later with the I/O control load command to set the 'write gate' latch on. At write clock 0 and 1, the data byte is sent to the write buffer. The 'write gate' latch remains on during the write operation. At the end of the write operation, the 'write gate' latch is reset by a reset sector op command.

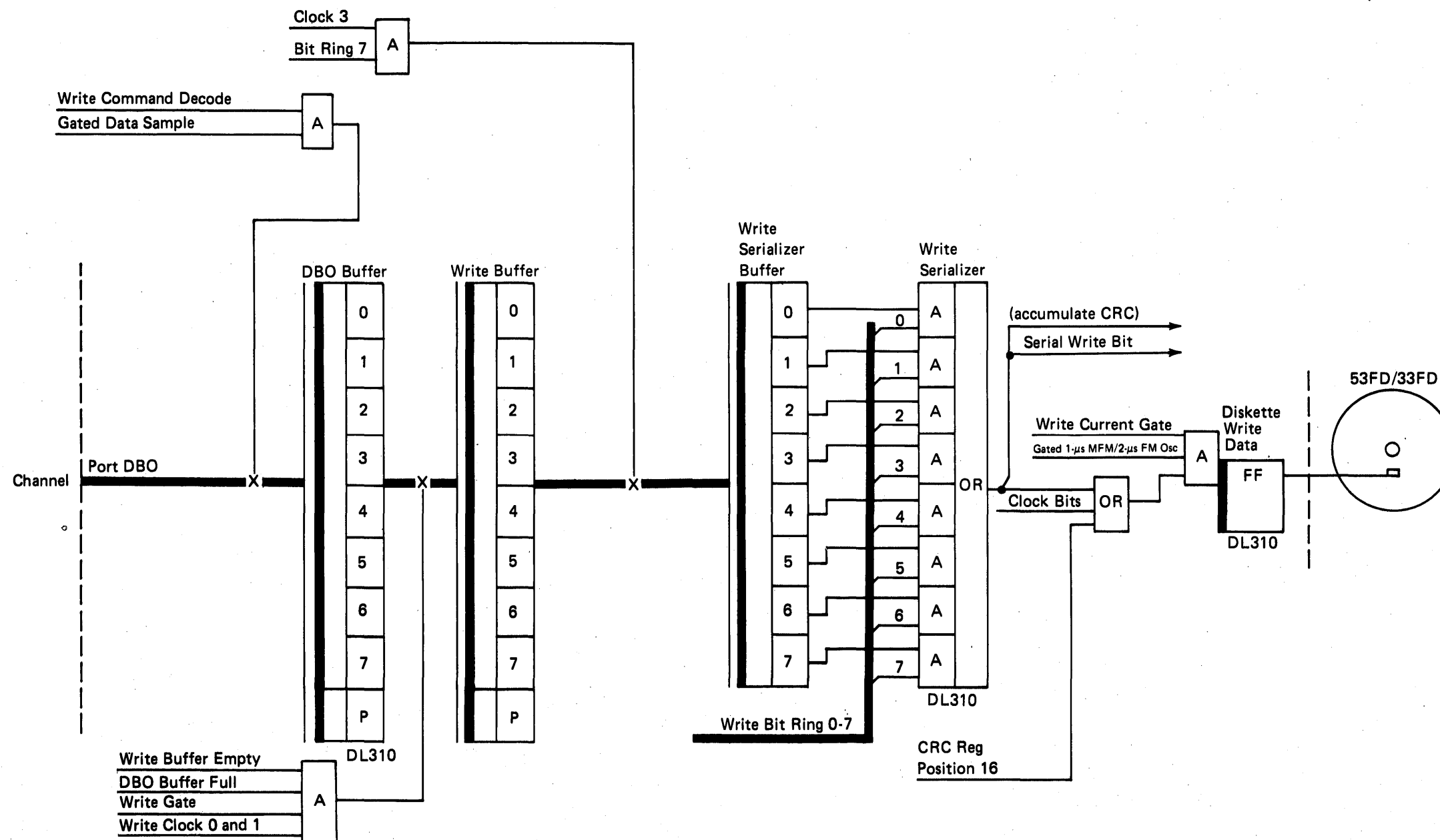
The byte is received on the data bus out and set in the data bus out buffer. At the same time, the 'write gate' latch is set and the write clock and the write bit ring are started. The write bit ring has been held reset to 6 by the 'write current gate' line de-activated. At write clock 0 and 1, the byte is sent to the write buffer. At bit ring 7 and clock 3, the byte is sent to the write serializer buffer.

Note: The 'write gate' latch is on if bytes have already been written.

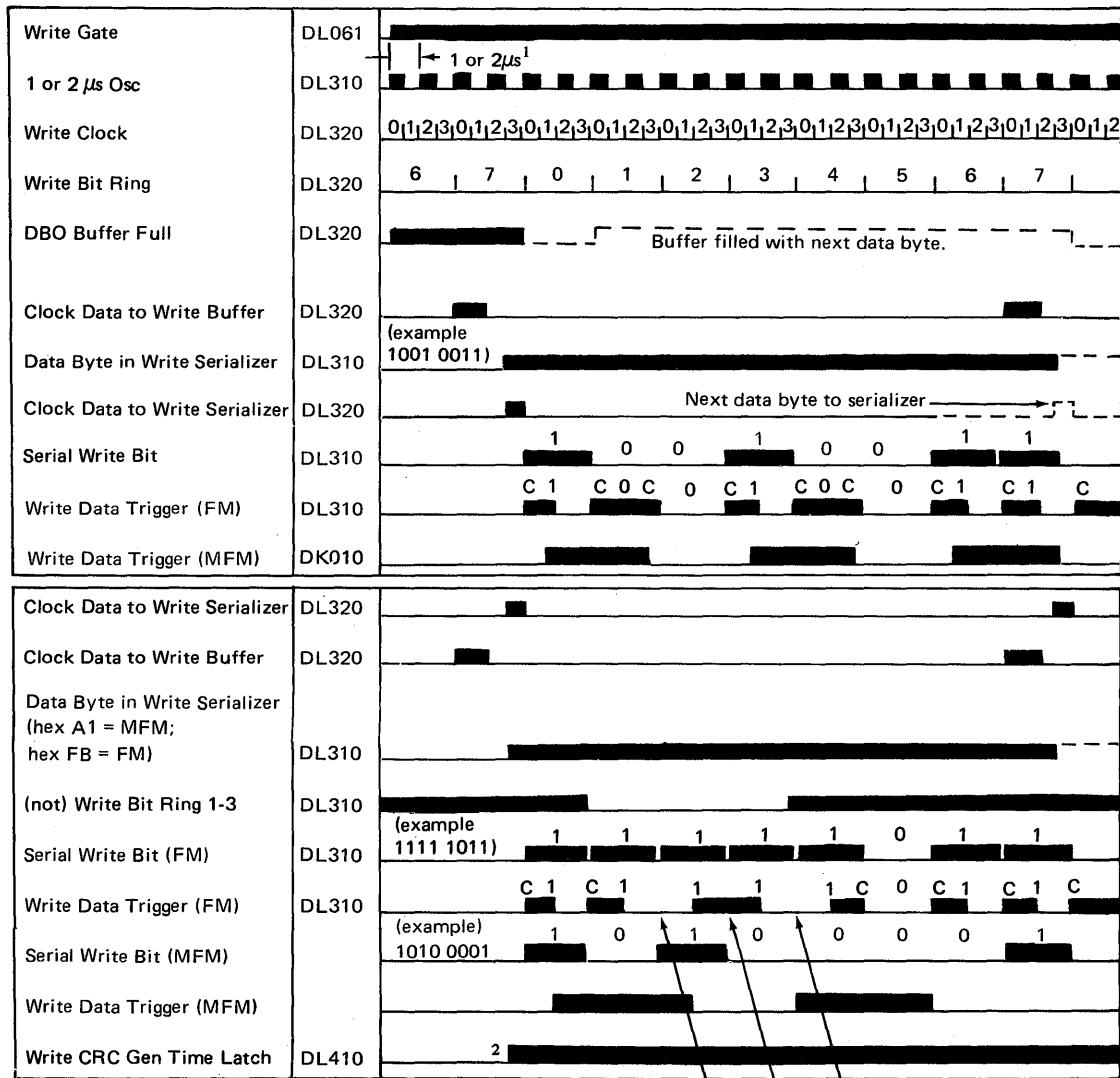
Bits are gated one at a time through the serializer, ORed with clock bits, and sent to the write trigger. Each shift on the input to the trigger causes the trigger to turn from on to off or from off to on, which in turn causes the write current through the data head to change direction.

The 1 or 3 clock bytes that are missing when the address mark byte is written are used later during a read operation for byte synchronization.

All bytes written are also sent to the cyclic redundancy character shift register.



The following chart shows the serializing and writing of the gap byte, sync byte, identification byte, data byte or control byte, and the address mark byte. The 'write gate' latch is repeated from the preceding timing chart as a point of reference.



Write gap byte, sync byte, ID byte, and a data or control byte.

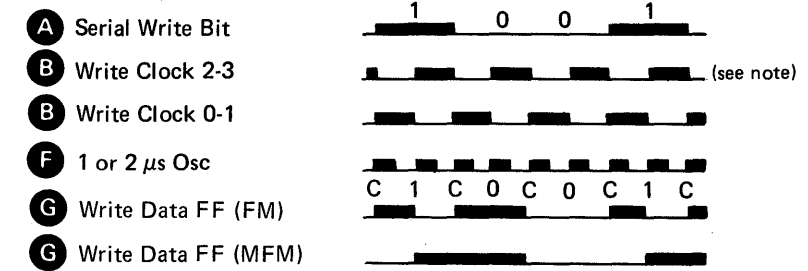
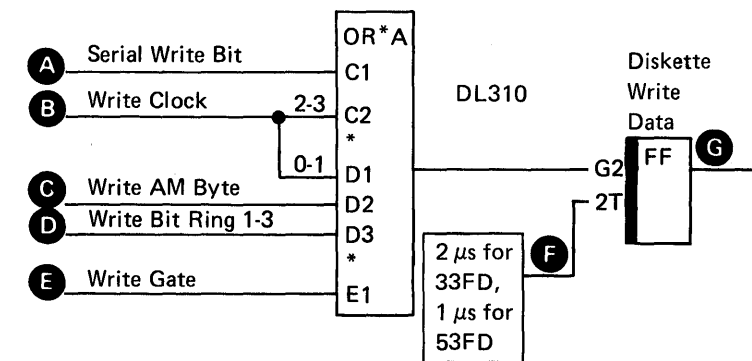
Write AM byte.

¹ 1 μs for 53FD, 2 μs for 33FD.

² Allows CRC shift register to accumulate CRC bytes.

Write Data Trigger

- A** Active to write data bits.
- B** 2-3 active to write clock bits; 0-1 active to write data bits.
- C** Not active during the write byte command. Gates the writing of data bits and clock bits.
- D** When active, causes 1 or 3 clock bits not to be written during the write address mark byte command.
- E** Always active when writing.



Note: Gate to FF remains active long enough for clock bits to be written at these times.

Write Cyclic Redundancy Character Byte Command

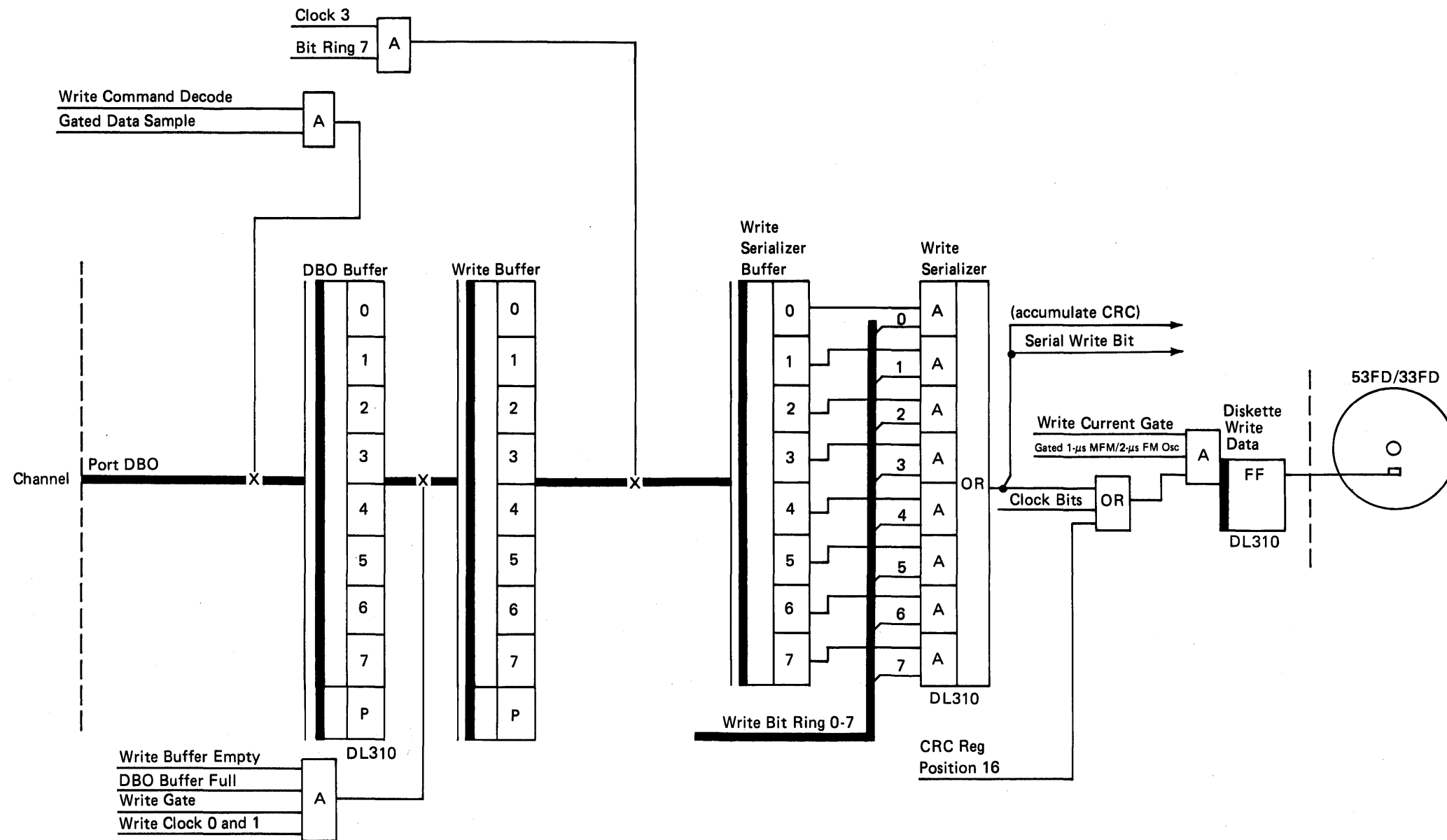
This command starts the following sequence of events:

1. The control storage program issues five write cyclic redundancy character byte commands to write the cyclic redundancy character.
2. The first two commands have data bytes of hexadecimal 00. The last three commands have data bytes of hexadecimal D0.
3. As the cyclic redundancy character shift register is advanced, it is ORed with each byte of hexadecimal 00. (00 is used so that only the cyclic redundancy character shift register bytes are written.) Each time position 16 is turned on, a cyclic redundancy character bit is written on the diskette. Both cyclic redundancy characters are written on the diskette.
4. The last 3 bytes of hexadecimal D0 are sent to the attachment to shift the first 2 bytes of hexadecimal 00 through the attachment. The attachment writes the first 3 bits of the first hexadecimal D0 on the diskette.
5. A reset sector op command resets write gate and stops the writing of any more bits.

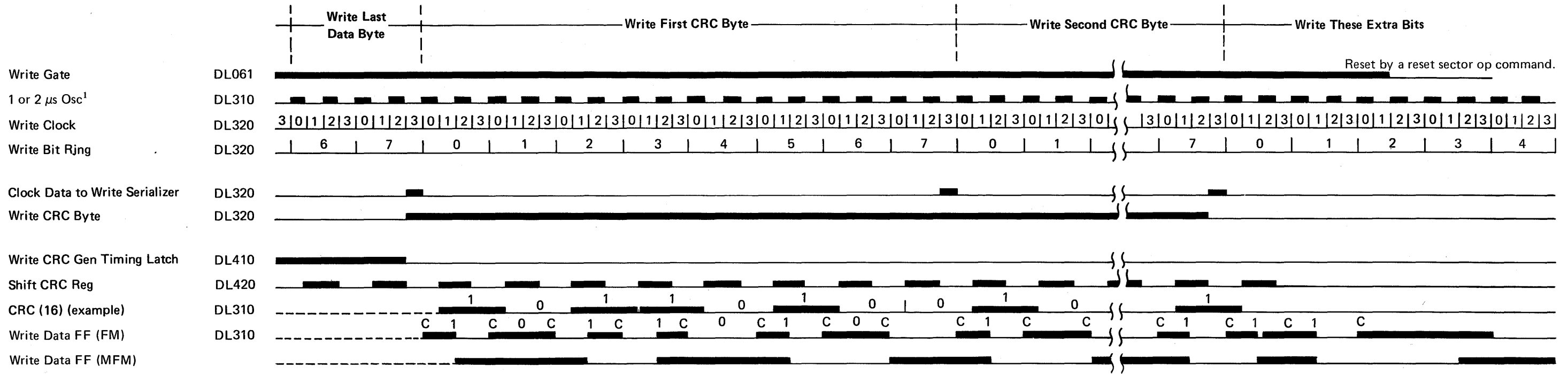
The first part of the write cyclic redundancy character byte command is the same as for the write byte command. The byte on the data bus out (must be hexadecimal 00) is set into the data bus out register. Just as in a write data byte command, the contents of the data bus out buffer are sent to the write serializer. The output of the write serializer is ORed with the cyclic redundancy character register position 16. Therefore, the data bus out byte must be hexadecimal 00 so the correct cyclic redundancy character byte is written.

Two write cyclic redundancy character byte commands must be sent in order to write all 16 bits (2 bytes) of the cyclic redundancy check character.

To permit the cyclic redundancy character bytes to be written, 3 bytes of hexadecimal D0 are sent to the attachment using the write byte command. These three commands place a hexadecimal D0 in the data bus out buffer, the write buffer, and the write serializer buffer. A reset sector op command follows and resets the 'write gate' latch. If writing in frequency modulation mode, before resetting the 'write gate' latch, 3 extra clock bits are written. If writing in modified frequency modulation mode, 3 data bits are written. This ensures correct reading (during a read operation) of the last cyclic redundancy character bit.



See the write byte timing chart for the first part of this command. As a point of reference, the hexadecimal 00 is set into the data bus out write buffer at this time as the last data byte is being written.



¹53FD is 1 μs, 33FD is 2 μs.

Seek to Next Track Command

This command starts the following sequence of events:

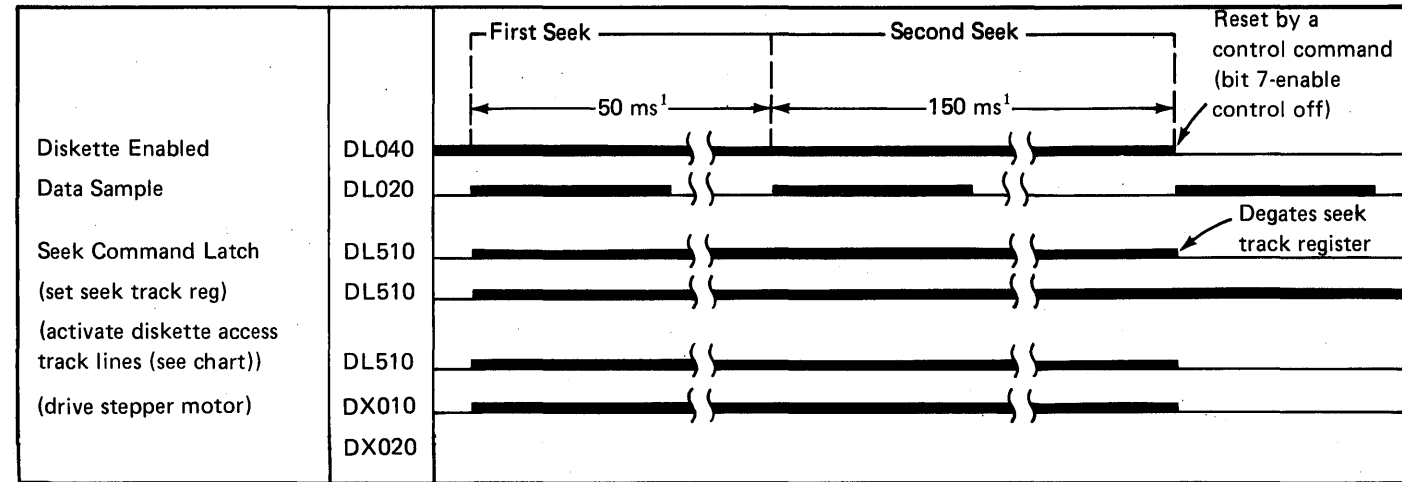
1. The attachment receives a seek to next track command.
2. Control information to move the head to the next track is received on the data bus out.
3. The data head is moved one track by turning the stepper motor shaft one step.

A seek to next track command starts the seek operation, which moves the data head one track in either direction. The control storage program must know where the data head is and place the correct data byte on the data bus out. Bits 6 and 7 control the access lines to the diskette drive stepper motor. (See the access chart.)

The first part of the operation is the standard sequence for the I/O control load command. At sample time, the attachment sets the 'seek command' latch and data bits 6 and 7 are set in the track address register. The output of the track address register selects the correct diskette drive access lines and moves the data head one track.

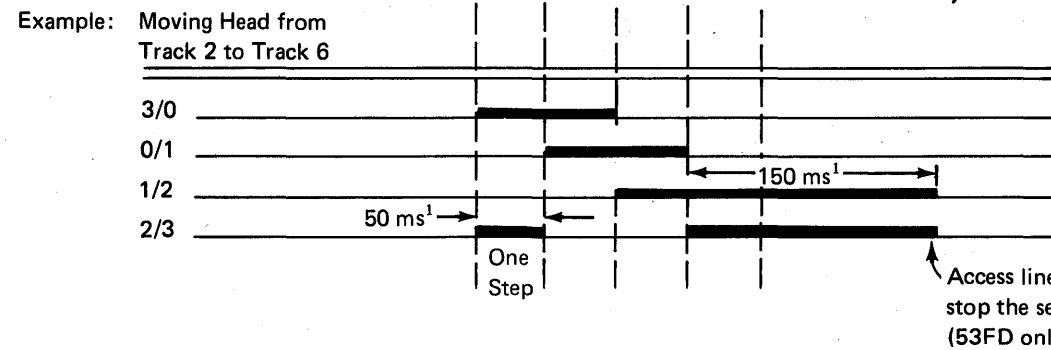
If the data head must be moved one more track, the control storage program issues another seek to next track command after 8.2 milliseconds (53FD) or after 50 milliseconds (33FD). When the control storage program issues that last seek, it waits 41 milliseconds (53FD) or 150 milliseconds (33FD) and then issues a control command with bit 7 off, which resets the seek.

A disconnect command resets the 'diskette enabled' latch, which in turn resets the 'seek command' latch and ends the 33FD seek operation. During 53FD operation, the '2 headed drive' line keeps the access lines active after a seek to electrically stop the stepper motor that holds the head on track.



Access Chart

Move Head to Track →	0	1	2	3	4	5	6
DBO Bits {6	0	0	1	1	0	0	1
{7	0	1	0	1	0	1	0
Access Lines Energized {3/0	X			X	X		
{0/1	X	X			X	X	
{1/2		X	X			X	
{2/3			X	X			X



¹ For the 33FD, 50 ms to seek, 100 ms for seek mechanism to stop. 150 ms to seek and stop on last track of a many-track seek.

For the 53FD, 8.2 ms to seek, 32.8 ms for seek mechanism to stop. 41 ms to seek and stop on last track of a many-track seek.

Search for Address Mark Byte Command

This command starts the following sequence of events:

1. The attachment receives a search for address mark byte command.
2. This command starts a read operation by turning on the 'read data command' latch.
3. The attachment searches for a sync field and an address mark byte.
4. The data separator, the read clock, and the read bit ring are synchronized.
5. The address mark byte is deserialized and placed in the read data buffer.

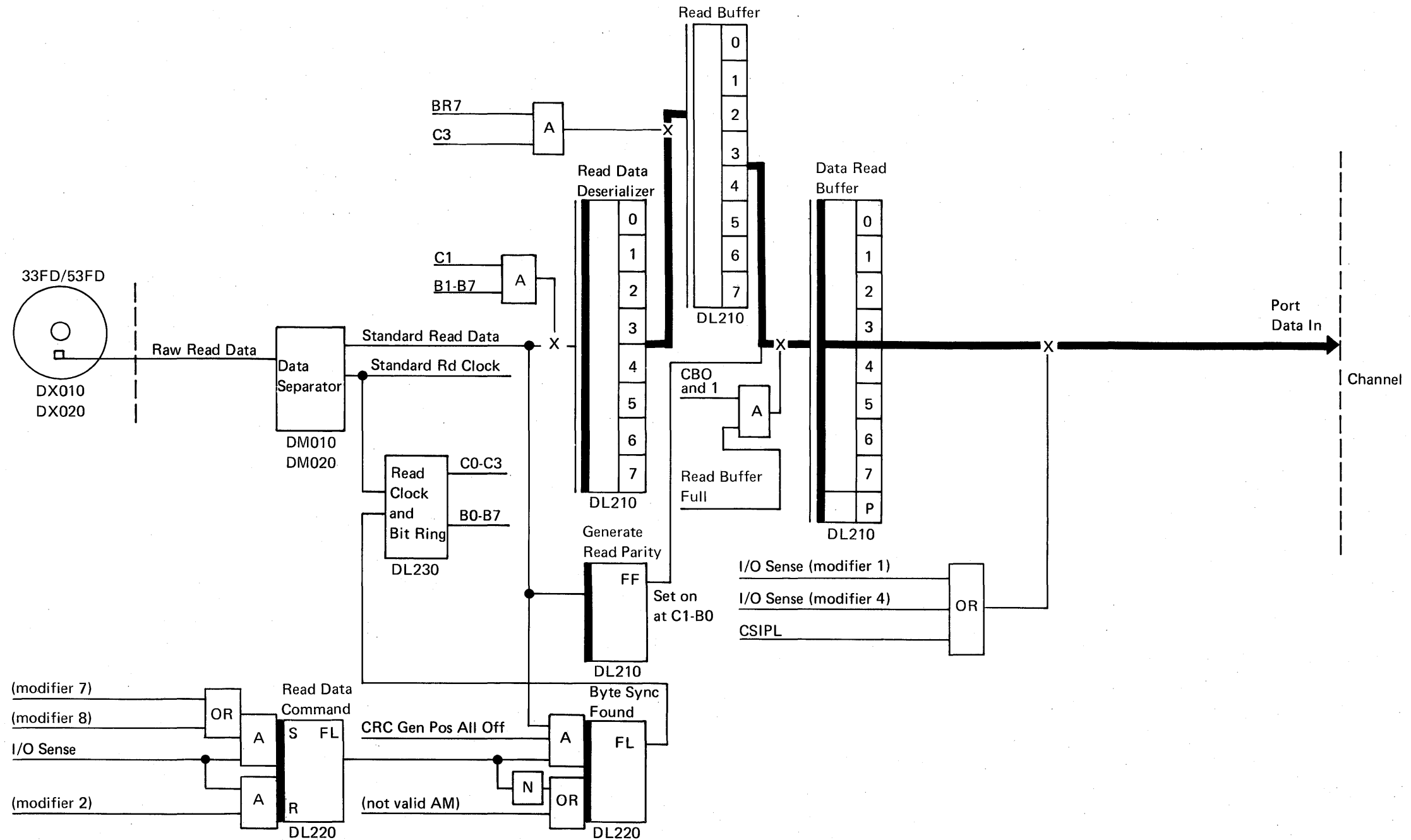
The search for address mark byte command is used to start the reading of the sector identification field or the data field of a record. It causes the bytes read to move through the read data deserializer and into the read buffer. The sense data byte command sends each byte of data to main storage.

The first part of this command is the standard sequence for the I/O control load command. At command sample time, the 'read data command' latch is set and the search for a sync field starts. After 16 consecutive zeros are read, the field is assumed to be a sync field. Sixteen zeros sent to the cyclic redundancy character circuits turn off all positions of the cyclic redundancy character shift register.

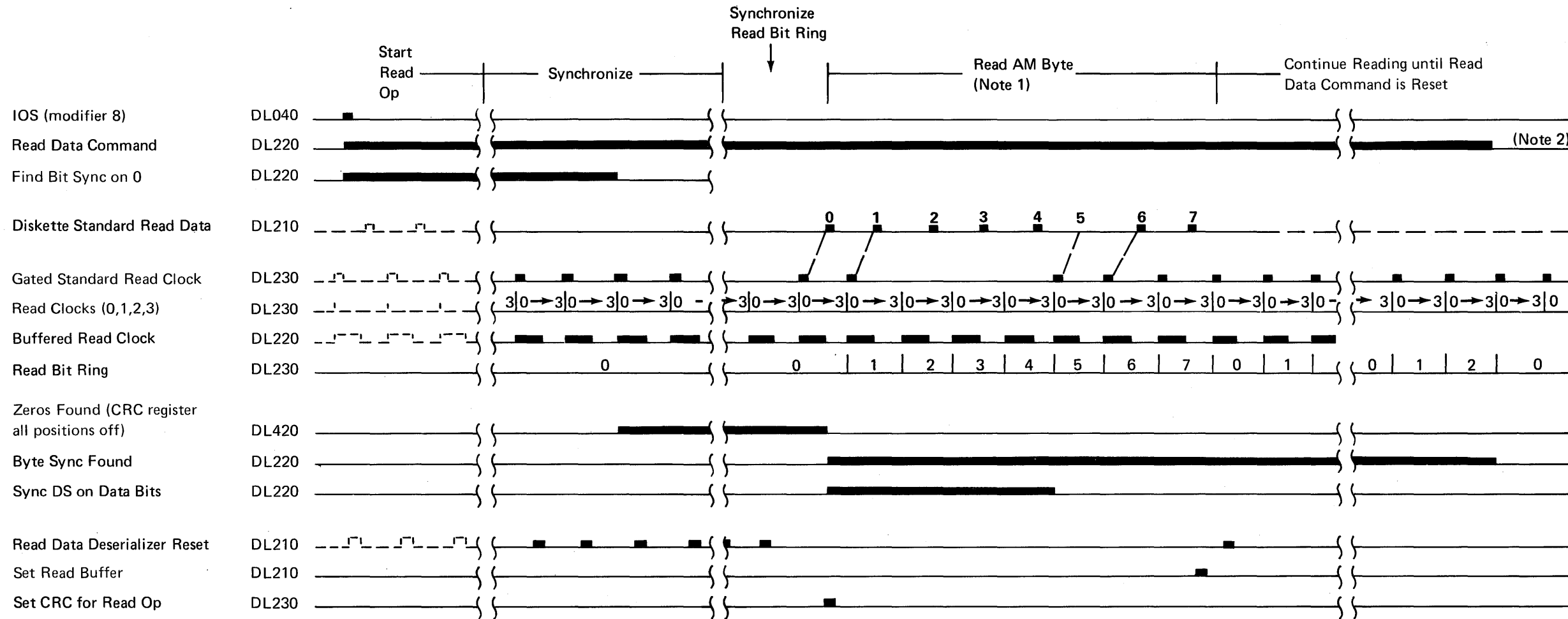
The search then continues for the first data bit of the address mark. This bit turns on the 'byte sync found' latch and permits the read bit ring to start running. In addition, the cyclic redundancy character shift register is initialized for reading by turning on all positions of the cyclic redundancy character shift register.

If a valid address mark is found, the 'byte sync found' latch is left on and reading of data starts. If a valid address mark is not found, the 'byte sync found' latch is turned off and the attachment looks for another sync field.

After the address mark byte is read into the deserializer, the byte is sent to the read buffer. A sense data byte command gates this byte out of the data read buffer and on to main storage.



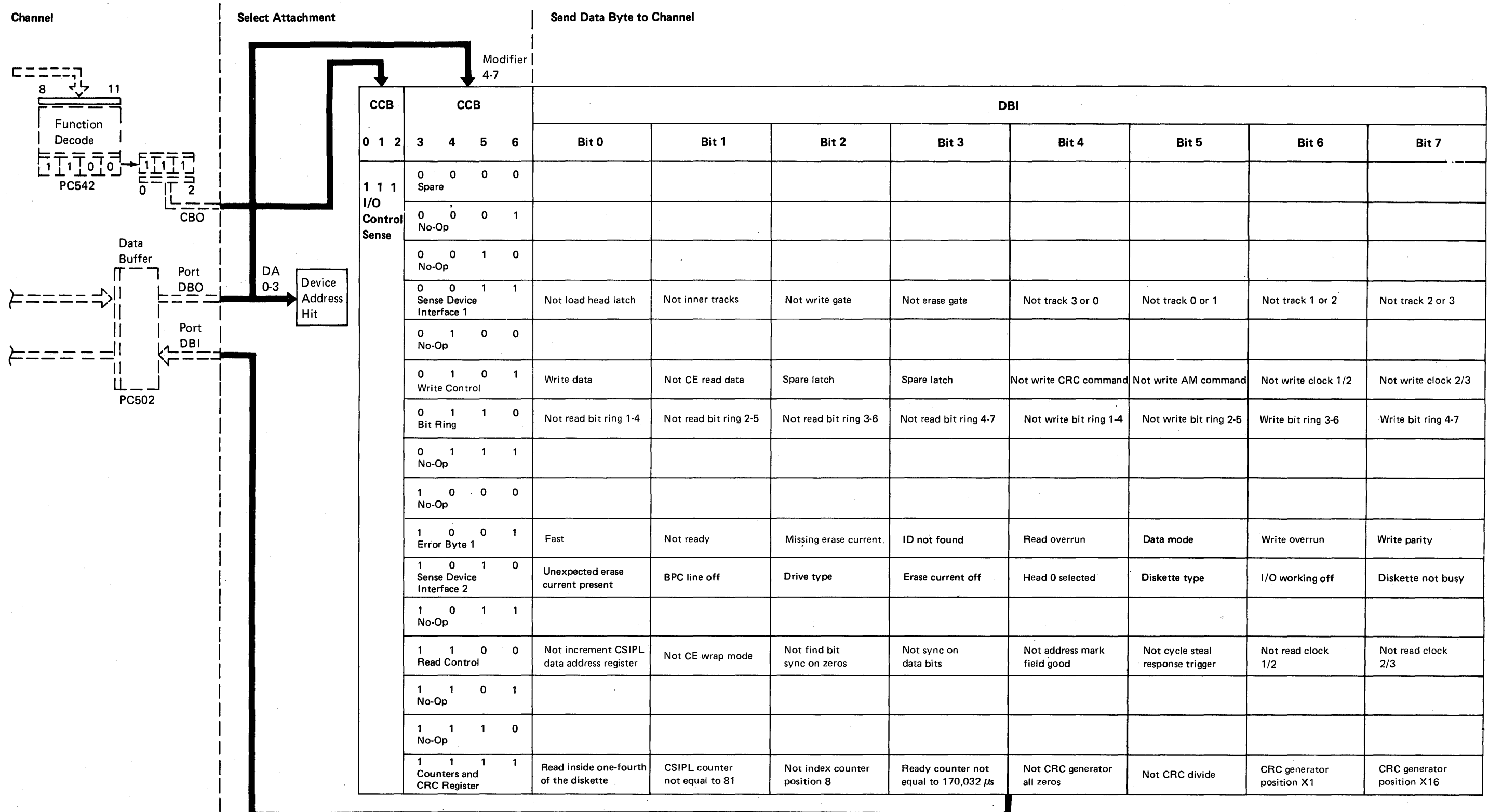
Normal synchronization between the diskette and the data separator is done by synchronizing the clock bits. However, when reading the address mark during bit ring 2, 3, and 4 times, there are no clock bits and the data separator is synchronized to the data bits. This is done by activating the 'sync DS on data bits' line.



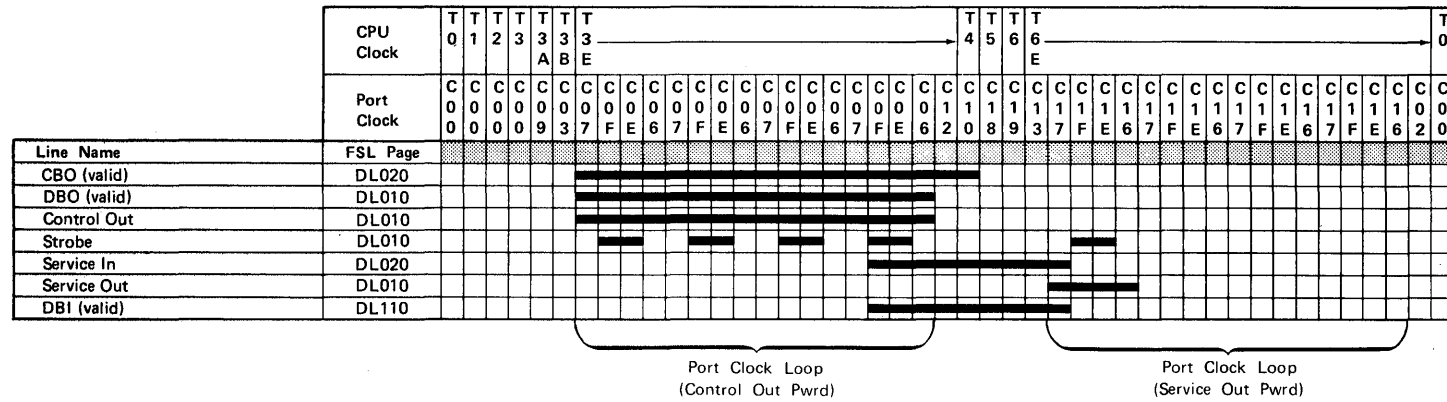
- Notes:**
1. AM byte example is hex FB.
 2. Read operation is ended by a reset sector op command.

I/O Control Sense Command

The I/O control sense command sends 1 byte of control information from the attachment to the control processor. See *Commands* in the *Channel* section of this manual for a description of how this command is executed.



The following timing chart shows the sequence of the I/O control sense command.



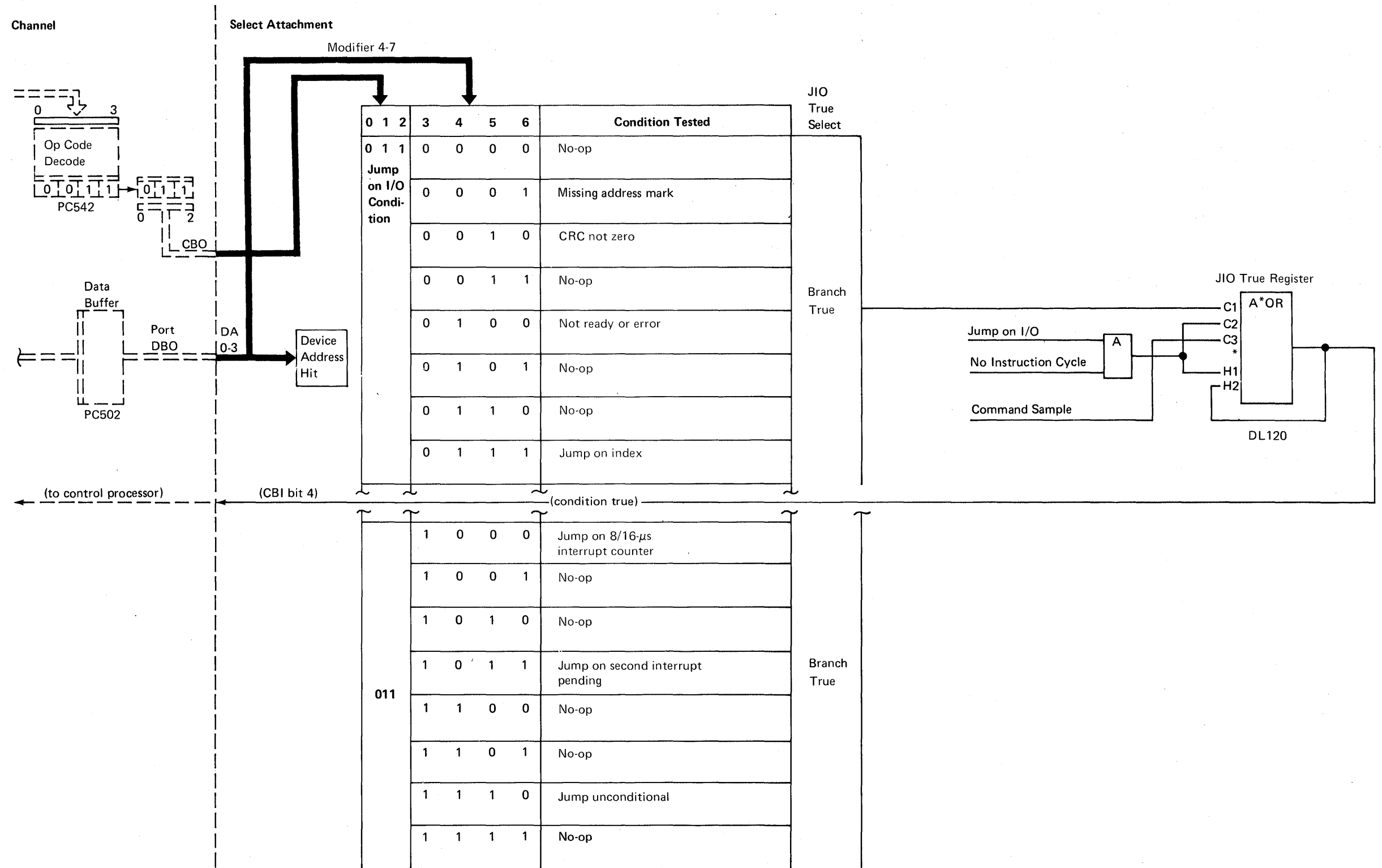
This chart shows the control sense action taken.

Modifier (DBO 4-7)	DBI Bits	Command	Action Taken	FSL Page
0 0 1 1	0-7	Sense device interface 1	Sends 1 byte of interface status information from the attachment to the control processor. Each bit indicates the status of a specific line.	DL130
0 1 0 1	0-7	Write control	Sends 1 byte of control information from the attachment to the control processor.	DL130
0 1 1 0	0-7	Bit ring	Sends 1 byte of the read bit ring and write bit ring information from the attachment to the control processor.	DL230
1 0 0 1	0-7	Error byte 1	Sends 1 byte of error information to the control processor.	DL130
1 0 1 0	0-7	Sense device interface 2	Sends 1 byte of interface status information from the attachment to the control processor.	DL130
1 1 0 0	0-7	Read control	Sends 1 byte of control information from the attachment to the control processor.	DL130
1 1 1 1	0-7	Counters and CRC register	Sends 1 byte of counter and CRC information to the control processor.	DL130

This page intentionally left blank.

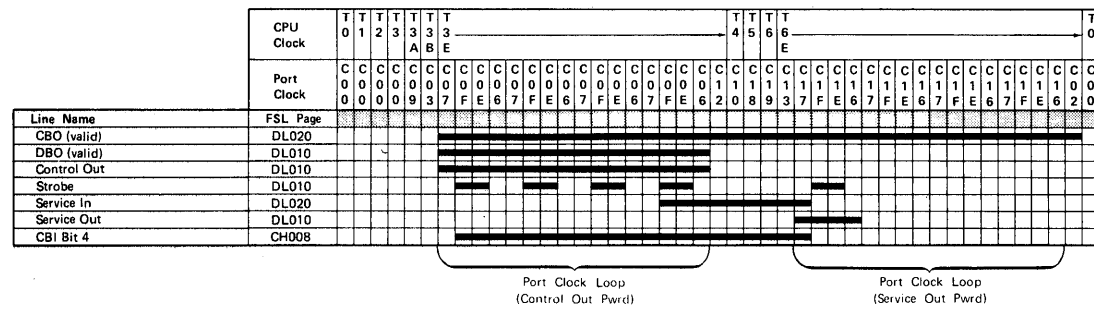
Jump on I/O Command

The jump on I/O command tests the attachment for a specific condition, as shown in this figure. If the condition is active, a positive response is sent to the control processor by activating the 'CBI bit 4' line. See *Commands* in the *Channel* section of this manual for a description of how this command is executed.



The jump on I/O command is divided into two parts:

1. Commands with modifiers of hexadecimal 0 through hexadecimal 7. These commands test the attachment for a specific condition. If the condition is active, a positive response is sent to the control processor by activating the 'CBI bit 4' line. In this attachment, the 'CBI bit 4' line is named 'diskette C Stg/W/OP/Br'.
2. Commands with modifiers of hexadecimal 8 through hexadecimal F. These commands perform specific functions such as setting or resetting a latch. No jump test is made for this group.



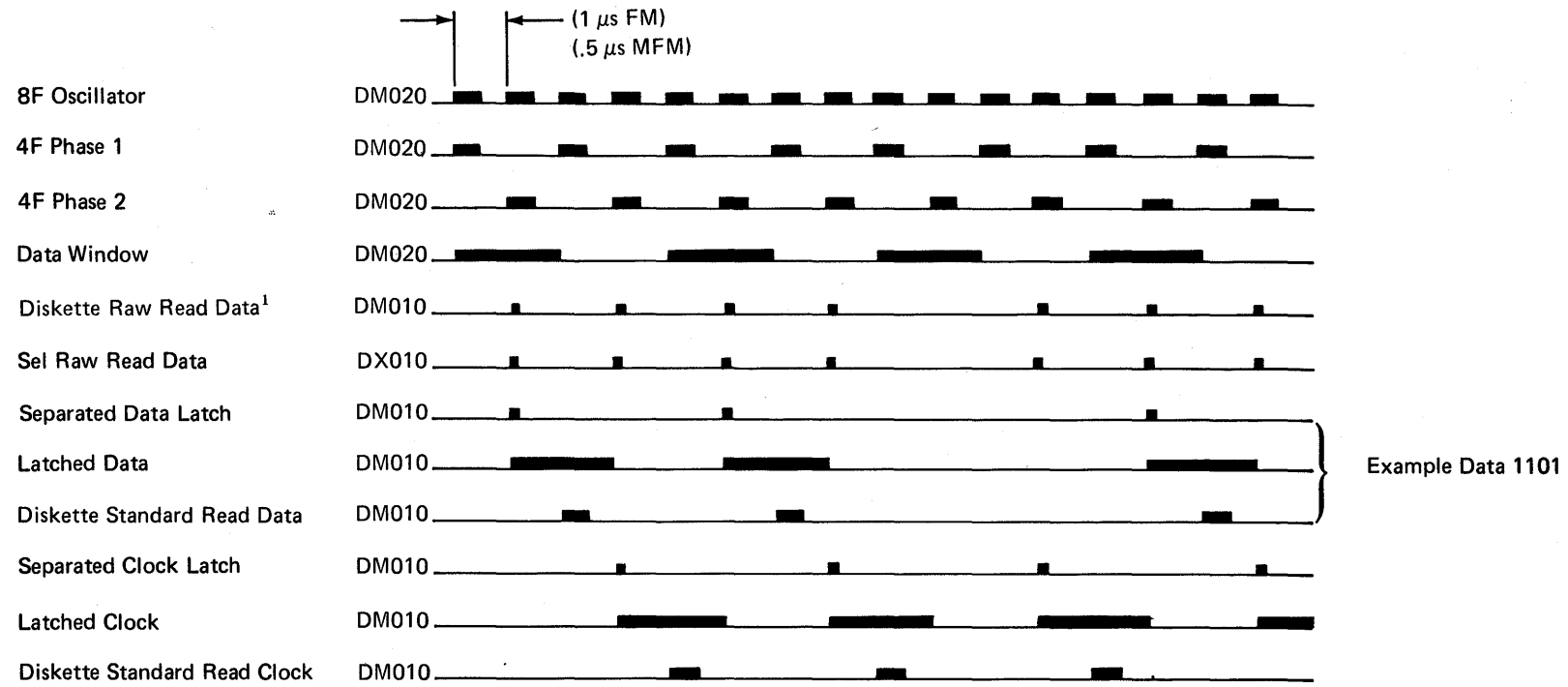
Modifier (DBO 4-7)	CBI Bit	Condition Tested	Action Taken	FSL Page
0 0 0 1	4	Missing address mark	Tests the 'AM byte good' latch. If the latch is off, CBI bit 4 is sent to the control processor.	DL120
0 0 1 0	4	CRC not zero	Tests the 'test CRC gen 0' latch. If the latch is off, CBI bit 4 is sent to the control processor.	DL120
0 1 0 0	4	Not ready or error	Tests for the following conditions: Not ready Running fast Read overrun Write parity check Write overrun Missing erase current Unexpected erase current present ID not found If any of these conditions is found, CBI bit 4 is sent to the control processor.	DL120 DL520 DL520 DL610 DL610 DL610 DL610 DL610 DL610
0 1 1 1	4	Jump on index	Tests the index singleshot. If singleshot is on, CBI bit 4 is sent to the control processor.	DL120
1 0 0 0	4	Jump on 8/16- μ s interrupt counter	Tests the 8/16- μ s counter. If the counter is on, CBI bit 4 is sent to the control processor.	DL120
1 0 1 1	4	Jump on second interrupt pending	Tests the 'second interrupt level 1 pending' latch. If the latch is on, CBI bit 4 is sent to the control processor.	DL120
1 1 1 0	4	Jump unconditional	CBI bit 4 is sent to the control processor.	DL120

FUNCTIONAL UNITS

Data Separator

The data separator separates data pulses from clock pulses.

The data separator oscillators have been synchronized with the 'diskette raw read data' line from the diskette. As a result, data pulses occur when the 'data window' line is active and clock pulses occur when the 'data window' line is not active.

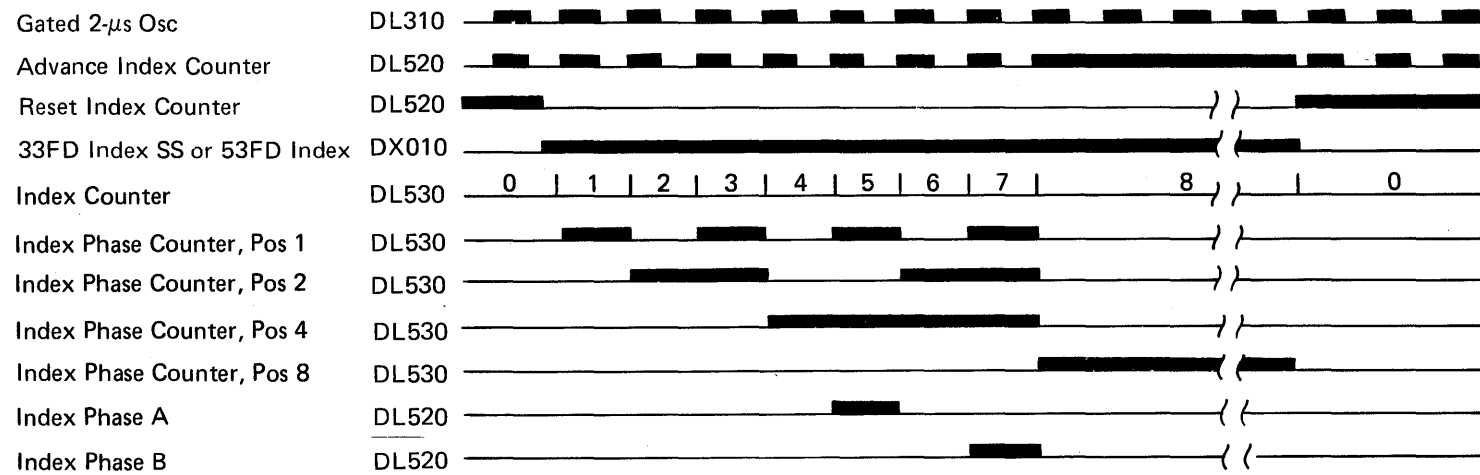


¹ FM data is shown. The data separator operates the same for MFM data.

Index Counter

Timing pulses generated from the index counter are used when the '33FD index SS' is active (for a 33FD diskette drive), or the '53FD index' line is active (for a 53FD diskette drive). The counter is reset to 0 and held reset until either of these lines is activated. Advance pulses then advance the counter until the count reaches 8. At this point, the advance pulses are stopped and the counter remains at 8 until the '33FD index SS' turns off or the '53FD index' line is de-activated. The counter is then reset to 0.

If the index pulse does not last until the counter reaches 4, the pulse is not a valid index pulse and the counter is reset.



Cyclic Redundancy Character Shift Register

The cyclic redundancy character shift register:

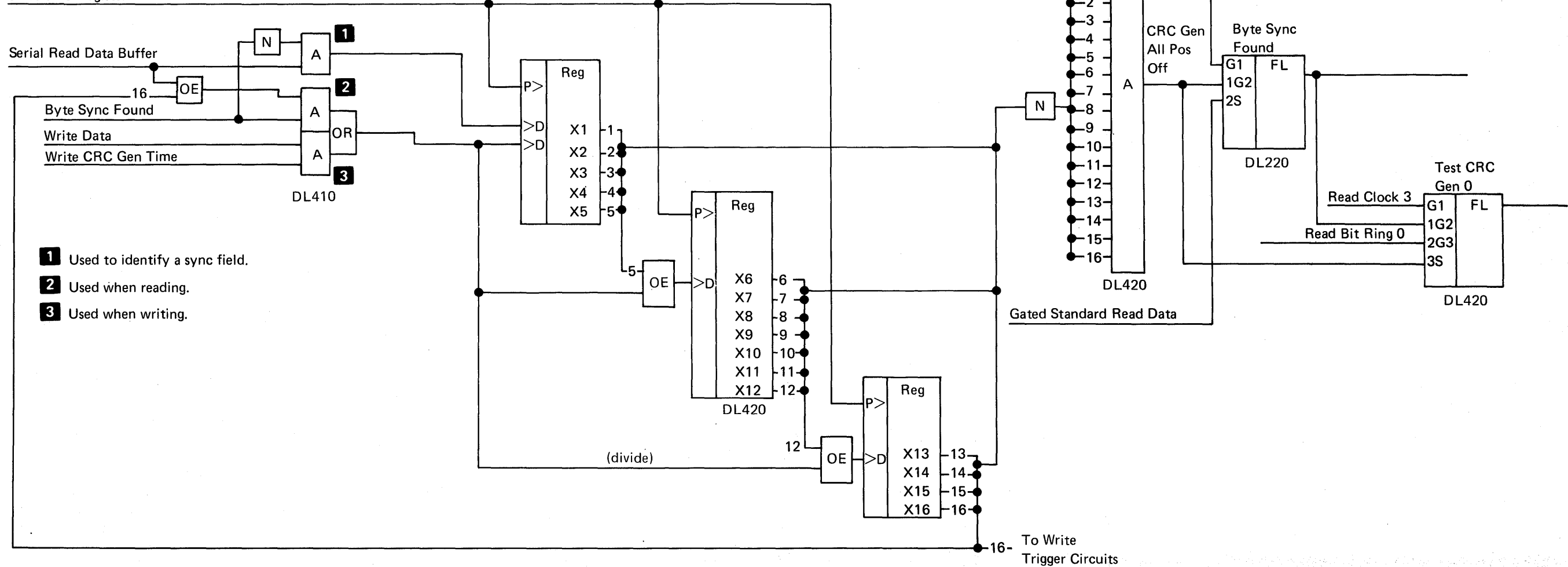
- Checks the reading of data
- Generates 2 cyclic redundancy character bytes when writing
- Identifies sync fields

When reading or writing, the cyclic redundancy character shift register functions as three separate shift registers connected by exclusive OR (OE) circuits. When the cyclic redundancy character shift register is used to identify sync fields, the bottom legs of the connecting exclusive ORs are never active and the three registers become a single, 16-position shift register.

A sync field is 6 bytes of clock bits (no data bits). Therefore, the AND circuit **1** is never made when reading a sync field. After reading 16 clock bits of a sync field, all positions of the shift register are off. The first data bit in the address mark byte following the sync field turns on the 'byte sync found' latch.

When reading or writing, the shift register functions as three separate parts. The moving of bits from one part to the next, or from the last part back to the first part, is controlled by the exclusive ORs. For example, position X6 can turn on with the shift pulse when position X5 is on or the 'divide' line is active; position X6 does not turn on if neither or both inputs to the exclusive OR are active.

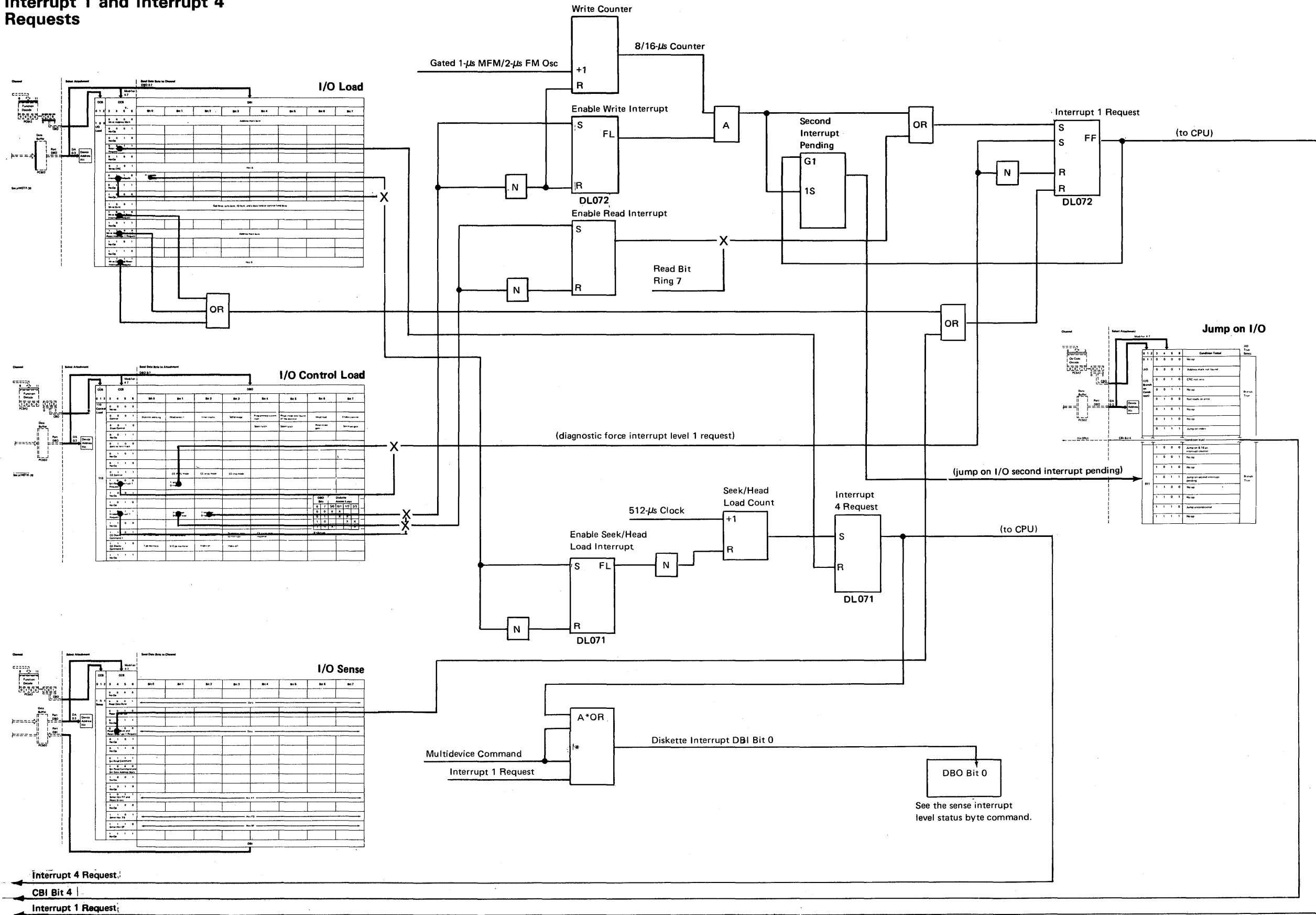
Shift CRC Register



- 1** Used to identify a sync field.
- 2** Used when reading.
- 3** Used when writing.

To Write Trigger Circuits

Interrupt 1 and Interrupt 4 Requests



ERROR CONDITIONS

Error conditions are detected by hardware and microcode. For a hardware-detected error, the control storage program determines if there is a drive error condition or a not-ready condition by issuing a jump-on-I/O-condition command with a modifier of hexadecimal 4. An I/O control sense command then determines the specific error.

For a microcode-detected error, the microcode tests for these conditions at various points in the I/O module to determine if the operation should be terminated.

The following chart shows the status bytes and bits, the error conditions, whether the errors are logged in ERAP, whether the errors are detected by hardware or microcode, and the corrective actions to be taken.

Byte	Bit	Error Condition	Logged in ERAP	Detected By		Corrective Action	Description of Corrective Actions
				Micro-code	Hard-ware		
0	0	Missing Data Address Mark	Yes	X		1	<ol style="list-style-type: none"> a. Retry the operation up to two times for a write operation and up to nine times for a read operation. b. If the retry is successful, log a temporary error indicating the number of retries required and return to processing. c. If the retry is not successful, log a permanent error.
	1	ID Cyclic Redundancy Check	Yes	X		1	
	2	Data Cyclic Redundancy Check	Yes	X		1	
	3	Cylinder Mismatch	No	X		2	
	4	Head Mismatch	Yes	X		4	
	5	Record Mismatch	Yes	X		4	
	6	Record Length Mismatch	Yes	X		4	
1	0	No Op Condition	Yes	X		1	<ol style="list-style-type: none"> a. Issue a seek to the logical cylinder desired, then issue the data operation again. b. Retry the operation three times. c. If the retry is successful, log a temporary error indicating the number of retries required and return to processing. d. If the retry is not successful, log a permanent error.
	1	Invalid Control Record Check	Yes	X		3	
	2	Write Verify Mismatch	Yes	X		1	
	5	Write Error	Yes	X		1	
2	0	Fast Check	Yes		X	1	<ol style="list-style-type: none"> a. Do a recalibrate operation and verify that the correct diskette is in the drive. b. If the failure continues, log a permanent error.
	1	Not Ready	No		X	4	
	2	Missing Erase Current	No		X	1	
	3	ID Not Found	Yes		X	1	
	4	Read Overrun Check	Yes		X	1	
	6	Write Overrun Check	No		X	1	
	7	Write Parity Check	No		X	1	
3	0	Unexpected Erase Current Present	Yes		X	1	
						3	Call a not-valid control record and return to processing.
						4	<ol style="list-style-type: none"> a. Do a recalibrate operation and verify that the correct diskette is in the drive. b. If the failure continues, log a permanent error.

Missing Data Address Mark (Byte 0, Bit 0):

During a read or verify operation, the physical location of the desired data record is located by its ID field. An ID hit occurs when the contents of the control storage program compare equally to the diskette ID field (CHRN).

The ID hit conditions the system to expect the next address mark to be a data address mark. If a valid address mark is decoded and it is not a data or control address, the missing data address mark bit is turned on.

ID Cyclic Redundancy Check (Byte 0, Bit 1):

As the ID field is read during a read, write, or verify operation, a CRC character (unique to the ID field) is accumulated in the attachment CRC register. When the ID CRC field is read, all positions of the CRC register will go to zero if the CRC character accumulated is correct for the ID field being read.

If the CRC register is not equal to zero at CRC check time, the ID cyclic redundancy check bit is turned on.

Data Cyclic Redundancy Check (Byte 0, Bit 2):

As the data record is read during a read or verify operation, a CRC character (unique to the data record) is accumulated in the attachment CRC register. When the data CRC field is read, all positions of the CRC register will go to zero if the CRC character accumulated is correct for the data field being read.

If this is a read or verify operation and the CRC register is not equal to zero at CRC check time, the data cyclic redundancy check bit is turned on.

Cylinder Mismatch (Byte 0, Bit 3): The control storage program specifies which cylinder will be selected during a data operation. During the ID search, a byte compare is done between the diskette C-byte of the CHRN characters and the specified system control storage byte. If a compare is not made, the cylinder mismatch bit is turned on.

Head Mismatch (Byte 0, Bit 4): The control storage program specifies which head will be selected during a read or write operation. During the ID search, a byte compare is done between the diskette H-byte of the CHRN characters and the specified system control storage byte. If a compare is not made, the head mismatch bit is turned on.

Record Mismatch (Byte 0, Bit 5): The control storage program specifies which record will be read on the diskette. During the ID search, a byte compare is done between the diskette R-byte of the CHRN characters and the specified system control storage byte. If a compare is not made, the record mismatch bit is turned on.

Record Length Mismatch (Byte 0, Bit 6): The ID field contains the cylinder address, head address, record address, and record length (CHRN). A record length may be 128, 256, 512, or 1,024 bytes. The value of N recorded in the ID field indicates the record length. If the record length found on the diskette does not match the specified record length in main storage, the record length mismatch bit is turned on.

No Op Condition (Byte 1, Bit 0): The desired diskette operation cannot be executed because a field of the input/output block (IOB) is not valid or is not compatible with the status of the hardware.

The no op condition bit is turned on if a diskette operation cannot be executed. Bits 0 through 3 of byte 0 are used to further describe the error.

Invalid Control Record Check (Byte 1, Bit 1): If during a read operation, the address mark following an ID field is decoded as a control address mark, the first byte of the control field must be a graphic D or F. The first byte immediately following the address mark is the control flag identifying the type of record. The character code for the graphic D (hex C4 for EBCDIC) indicates that this physical record has been logically deleted. The character code for the graphic F (hex C6 for EBCDIC) indicates that the physical record space contains a defect. Diskettes recorded in ASCII will have the ASCII bit patterns for the graphic D and F.

If the first byte of the read operation is not a graphic D or F, the invalid control record check bit is turned on.

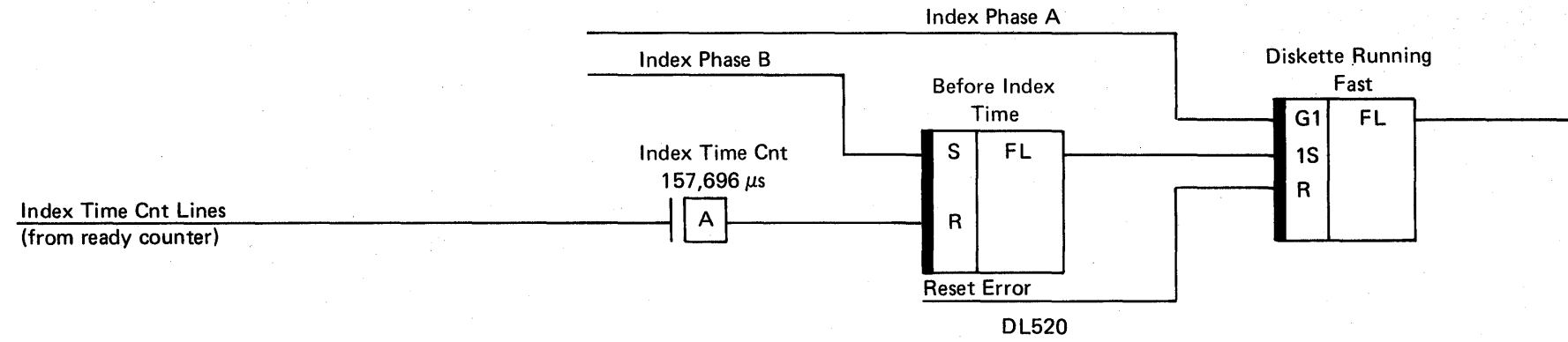
Write Verify Mismatch (Byte 1, Bit 2): A write verify operation is performed after every write operation. The data previously written is moved from the main storage data area to the attachment data buffer. The contents of the data buffer are compared bit by bit to the serial read data from the diskette data field. If a miscompare is detected, the write verify mismatch bit is turned on.

Write Error (Byte 1, Bit 5): If a write overrun, write parity, missing erase current, or unexpected erase current present error condition is detected during a write operation, the write error bit is turned on.

Fast Check

A fast-check condition occurs when the diskette is turning so quickly that index pulses occur more often than once every 157.7 milliseconds.

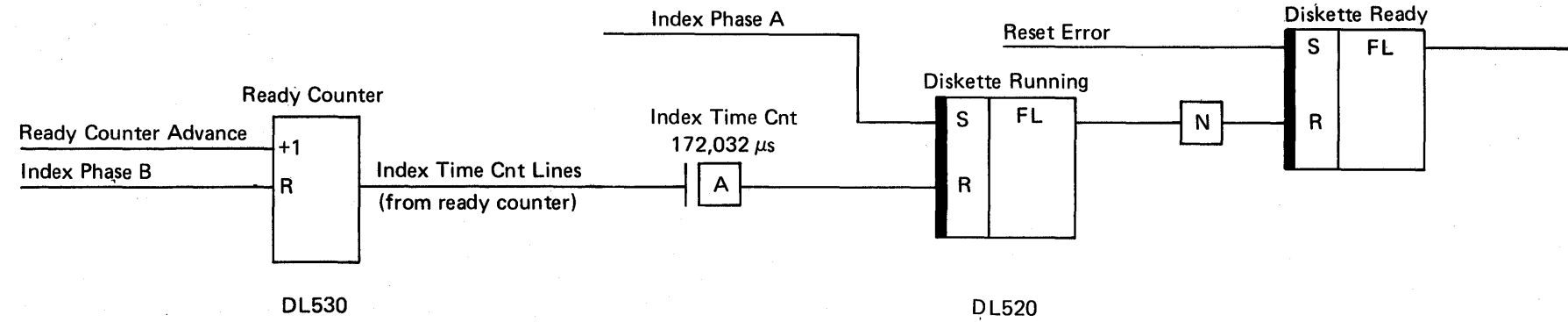
The 'before index time' latch is turned on by the 'index phase B' line. If the index counter has not counted to 161.7 milliseconds by the time the next 'index phase A' pulse occurs, the 'diskette running fast' latch is turned on.



Not Ready

A not-ready condition occurs when the diskette is turning so slowly that index pulses occur farther apart than once every 172 milliseconds.

The ready counter is reset by the 'index phase B' line. The counter is then permitted to advance. If the counter has not been reset again before it reaches 172 milliseconds, the 'diskette running' and 'diskette ready' latches are turned off.



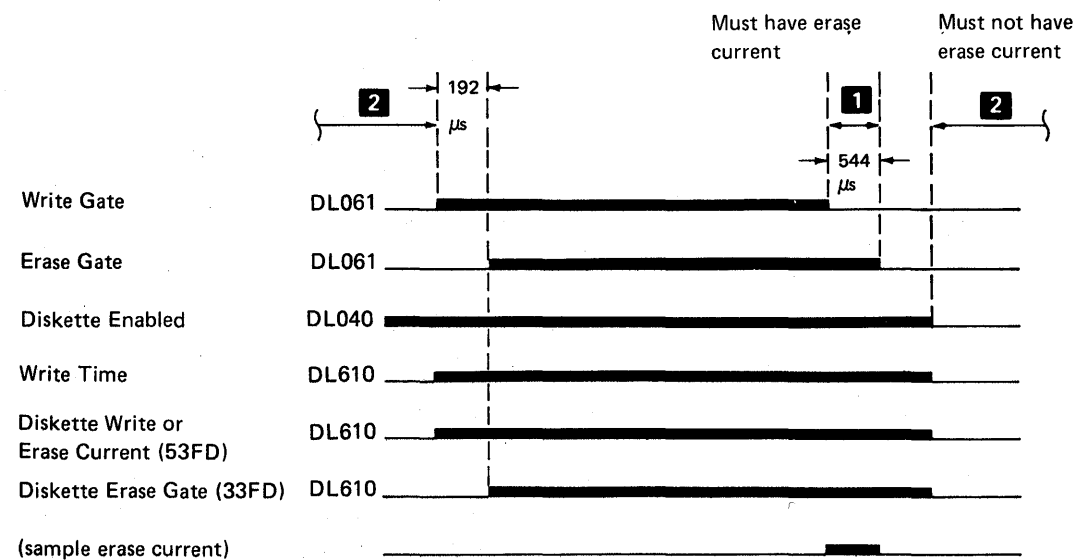
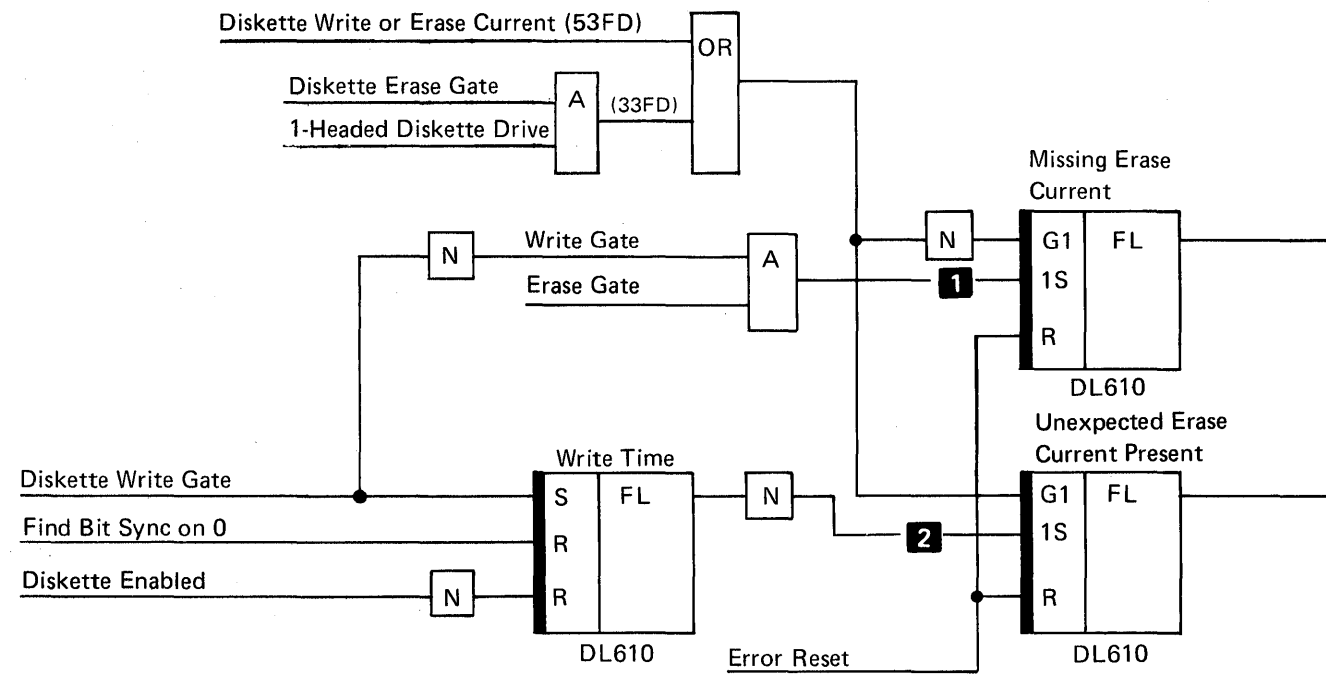
Missing Erase Current and Unexpected Erase Current Present

The 'missing erase current' latch can be set in two ways:

- For the 53FD, if the 'diskette write or erase current' line goes not active when the 'sample erase current' line is active.
- For the 33FD, if the 'diskette erase gate' line goes not active when the 'sample erase current' line is active.

The 'unexpected erase current present' latch can be set in two ways:

- For the 53FD, if the 'diskette write or erase current' line goes active and the 'write time' latch is off.
- For the 33FD, if the 'diskette erase gate' line goes active and the 'write time' latch is off.



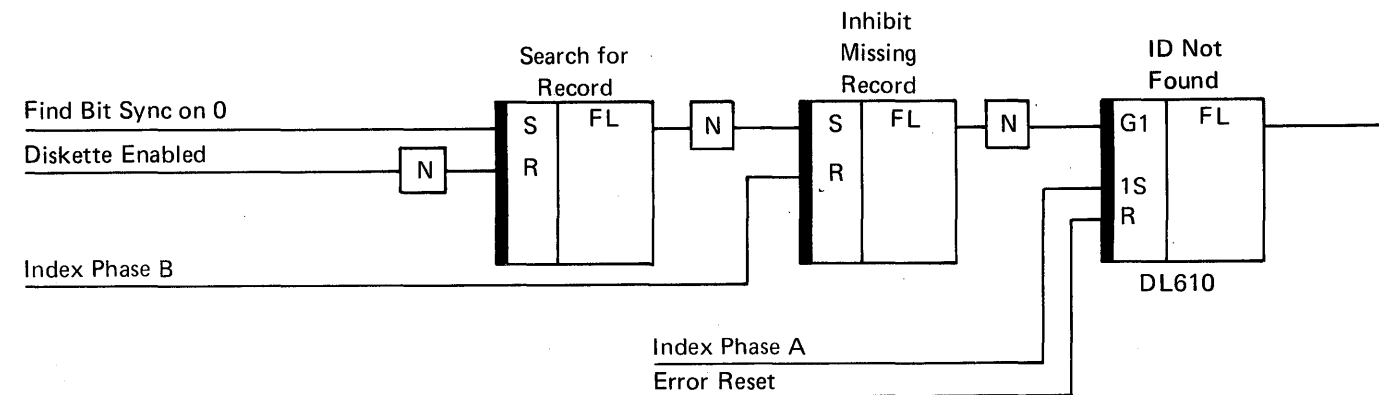
ID Not Found (Missing Record)

An ID-not-found condition occurs when the record being searched for is not found by the time two index pulses have been sensed.

A find sector identification operation is started by the search for address mark byte command. At the start of the search, the 'find bit sync on 0' line is activated and the 'search for record' latch turns on, removing the set to the 'inhibit missing record' latch. The next 'index phase B' pulse turns off the 'inhibit missing record' latch and generates a set gate for the 'missing record' latch.

When a sector identification field is found, the diskette is disabled. This resets the 'search for record' latch and turns on the 'inhibit missing record' latch. Therefore, the 'ID not found' latch cannot turn on.

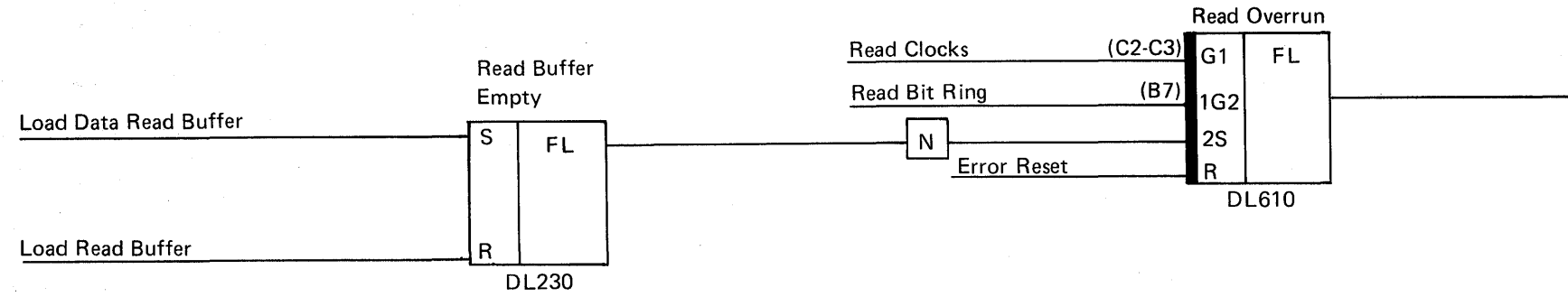
If a sector identification field is not found, the next 'index phase A' pulse sets the 'ID not found' latch.



Read Overrun Check

A read overrun check occurs when a byte of data from the read data deserializer is ready to be set into the read buffer but the control processor has not taken the byte that is now in the data read buffer.

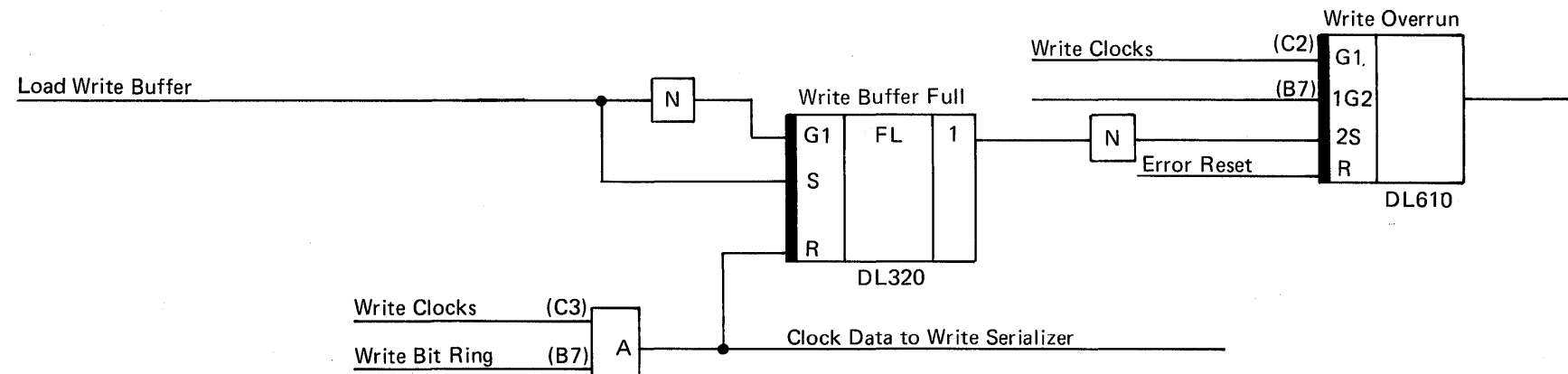
The contents of the read data deserializer are sent to the read buffer at B7-C3 time. If the contents of the data read buffer have not been sent to the control processor by B7-C2 time, the 'read overrun' latch is set.



Write Overrun Check

A write overrun check occurs when the attachment is ready to write a byte on diskette but the control storage program has not sent the byte to the attachment.

The contents of the write buffer are sent to the write serializer buffer at B7-C3 time. If the control processor has not responded in time with another byte, the 'write buffer full' latch is not set and at B7-C2 time the 'write overrun' latch is set.



Write Parity Check

A write parity check occurs when the byte gated out of the write serializer is not correct parity.

The data bits being written and the parity bit position of the write buffer are sent to the 'serial write parity' trigger. If there is an even number of bits, the trigger will be off and at B7-C2 time the 'write parity check' latch will be set.

