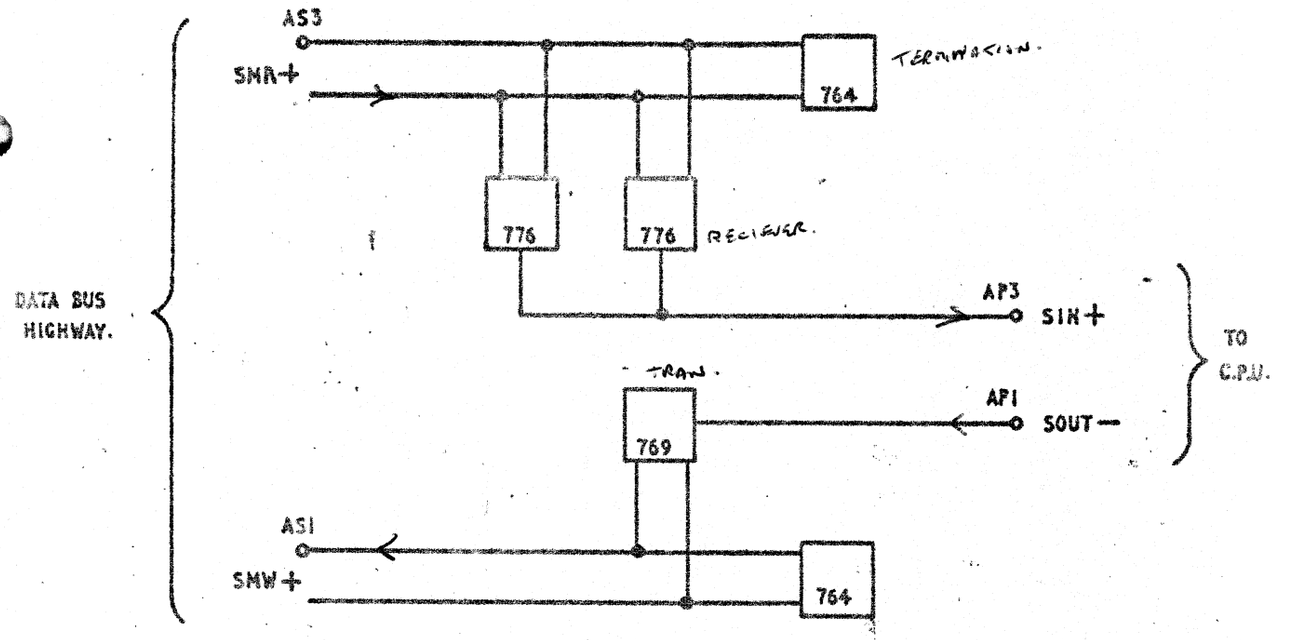
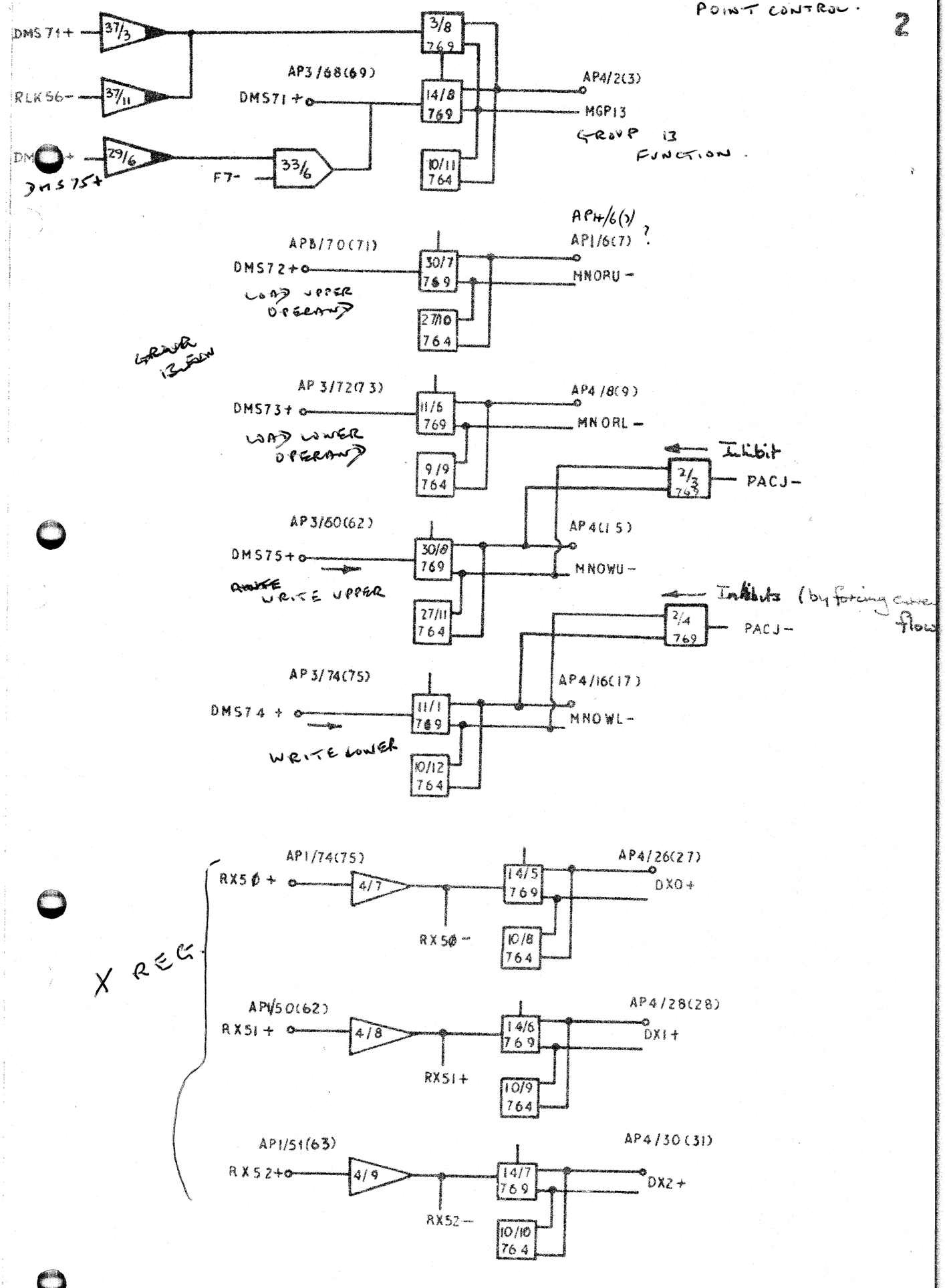
INDEX OF LOGICAL DRAWINGS FOR STORE EXTENSION UNIT (WGC05)

WGC05/1	DATA HIGHWAYS
" /2	F.P.U. CONTROL
" /3	F.P.U. CONTROL
" /4	F.P.U. CONTROL
" /5	F.P.U. CONTROL
" /6	STORE CONTROL
" /7	SMAC ADDRESS SCRAMBLE
" /8	SMAC ADDRESS SCRAMBLE & ADDRESS HIGHWAY
" /9	
" /10	INTER PROCESSOR INTERRUPT & FPU CONTROL.
" /11	STORE, BUS, & F.P.U. CABLING
" /12	1906/1904E BUS EQUIVALENT WAVEFORMS TO FFPU.



SMR+/SIN+	776	776	764	AS3/AP3	SMW+/SOUT−	769	764	ASI / API
0	25/1	26/1	19/1	2 (3)	0	17/1	13/1	2 (3)
1	25/2	26/2	19/2	4 (5)	1	17/2	13/2	4 (5)
2	25/3	26/3	19/3	6 (7)	2	17/3	13/3	6 (7)
3	25/4	26/4	19/4	8 (9)	3	17/4	13/4	8 (9)
4	25/5	26/5	19/5	10 (11)	4	17/5	13/5	10 (11)
5	25/6	26/6	19/6	14 (15)	5	17/6	13/6	14 (15)
6	25/7	26/7	19/7	16 (17)	6	17/7	13/7	16 (17)
7	25/8	26/8	19/8	18 (19)	7	17/8	13/8	18 (19)
8	23/1	24/1	19/9	20 (21)	8	16/1	13/9	20 (21)
9	23/2	24/2	19/10	22 (23)	9	16/2	13/10	22 (23)
10	23/3	24/3	19/11	24 (25)	10	16/3	13/11	24 (25)
11	23/4	24/4	19/12	26 (27)	11	16/4	13/12	26 (27)
12	23/5	24/5	19/13	28 (29)	12	16/5	13/13	28 (29)
13	23/6	24/6	18/1	30 (31)	13	16/6	12/1	30 (31)
14	23/7	24/7	18/2	32 (33)	14	16/7	12/2	32 (33)
15	23/8	24/8	18/3	34 (35)	15	16/8	12/3	34 (35)
16	21/1	22/1	18/4	36 (37)	16	15/1	12/4	36 (37)
17	21/2	22/2	18/5	38 (39)	17	15/2	12/5	38 (39)
18	21/3	22/3	18/6	40 (41)	18	15/3	12/6	40 (41)
19	21/4	22/4	18/7	42 (43)	19	15/4	12/7	42 (43)
20	21/5	22/5	18/8	44 (45)	20	15/5	12/8	44 (45)
21	21/6	22/6	18/9	46 (47)	21	15/6	12/9	46 (47)
22	21/7	22/7	18/10	48 (49)	22	15/7	12/10	48 (49)
23	21/8	22/8	18/11	52 (53)	23	15/8	12/11	52 (53)
24	20/1	20/2	18/12	54 (55)	24	14/1	12/12	54 (55)

N.B.
INHIBIT INPUTS ON 769/776 NOT WIRED.

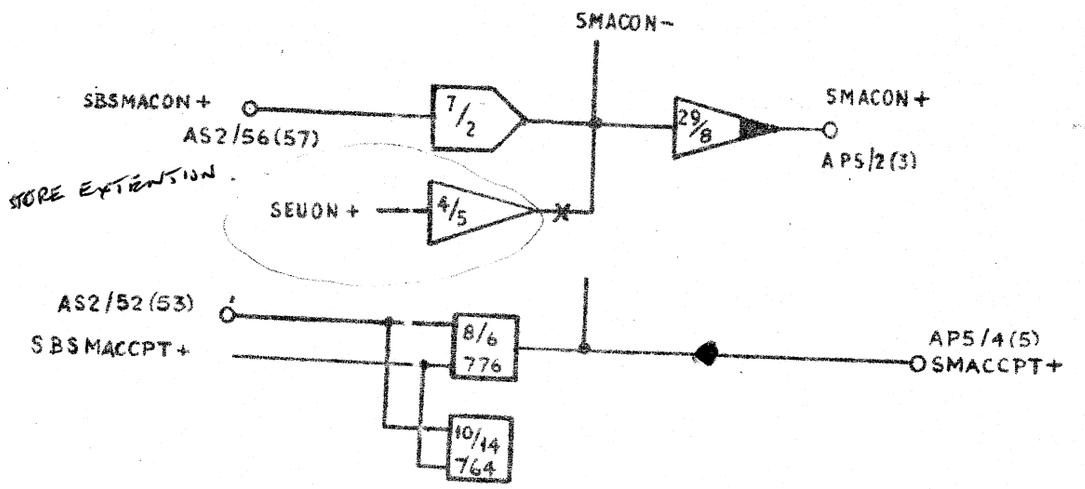


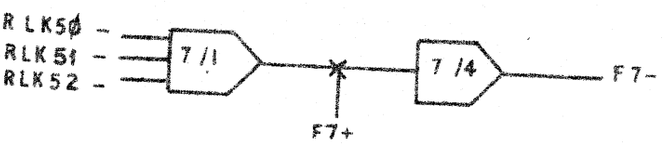
FLOATING POINT PRESENT.

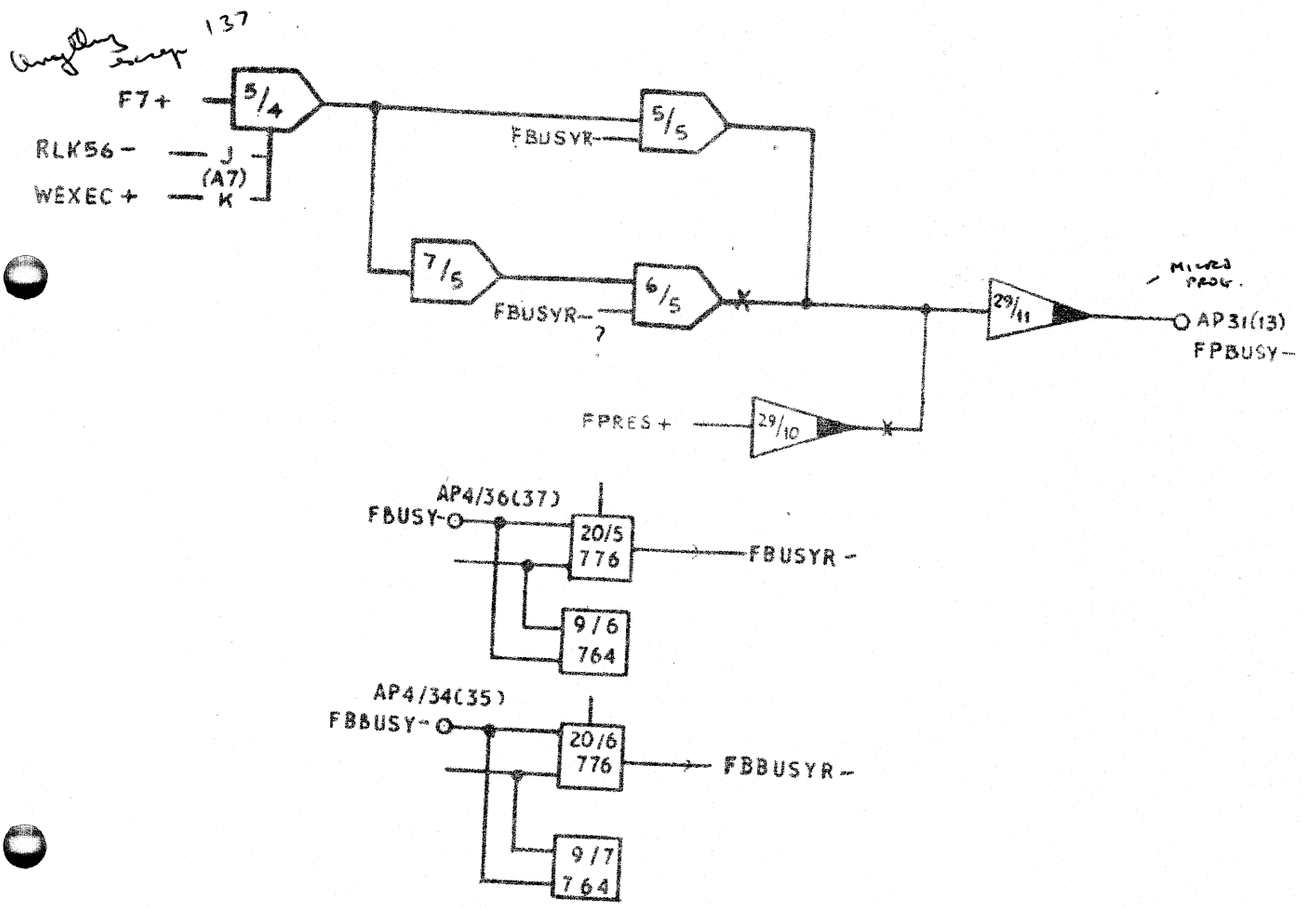
WGC05/2

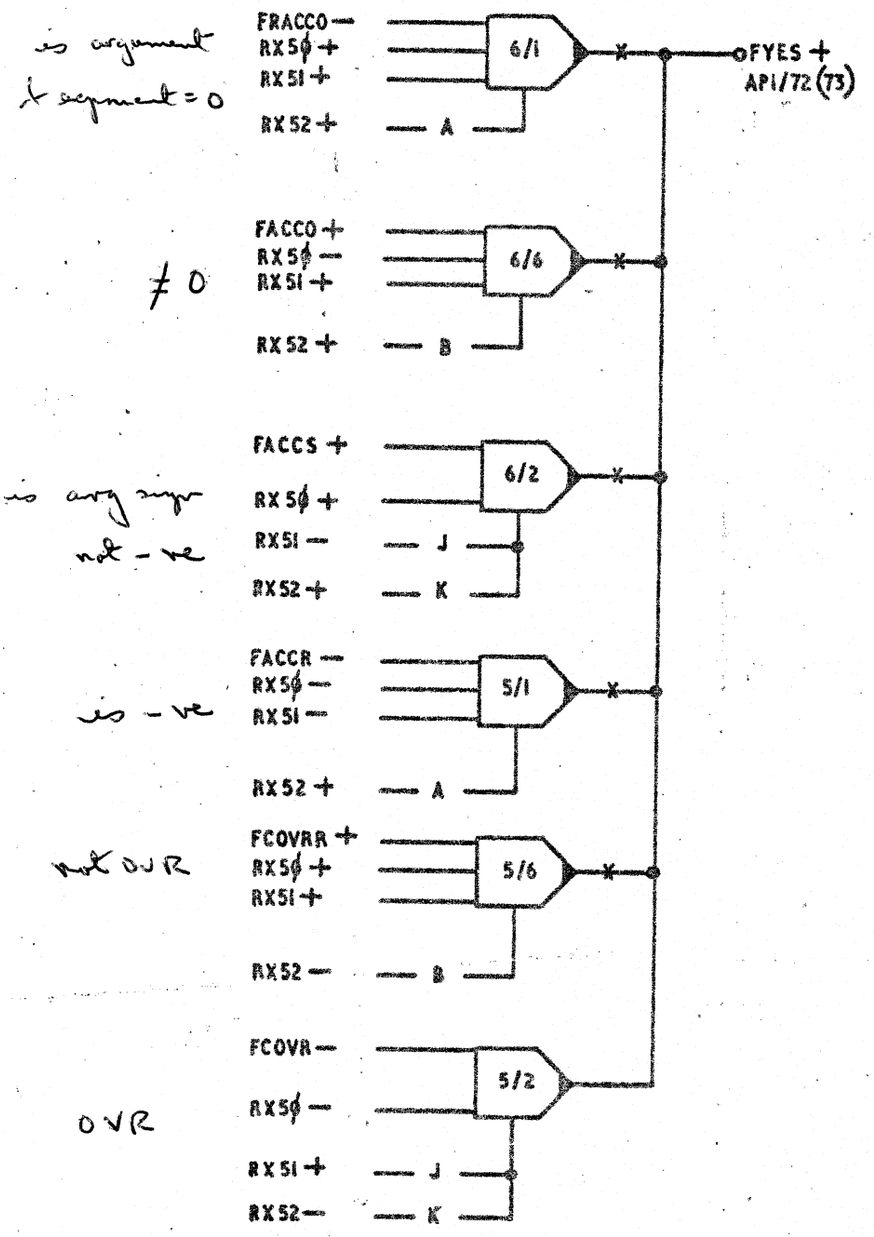
F.P.U. CONTROL

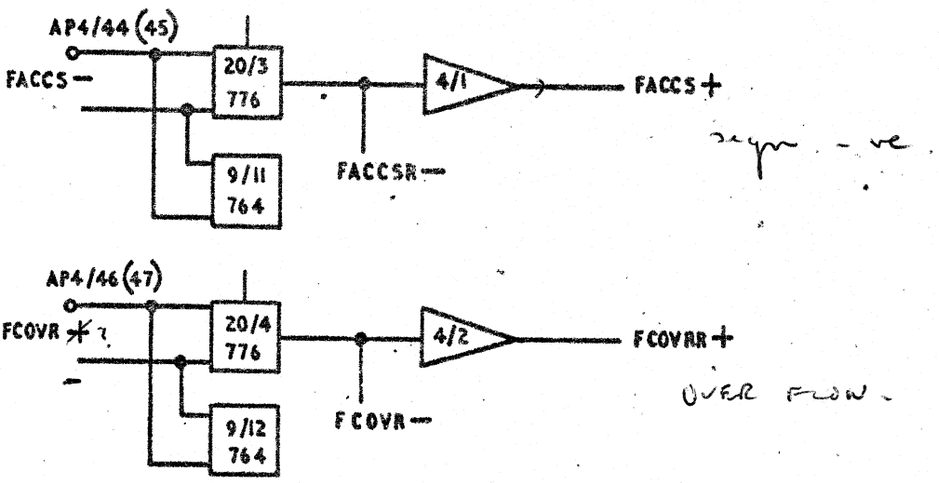
FLOATING POINT UNIT CONTROL.







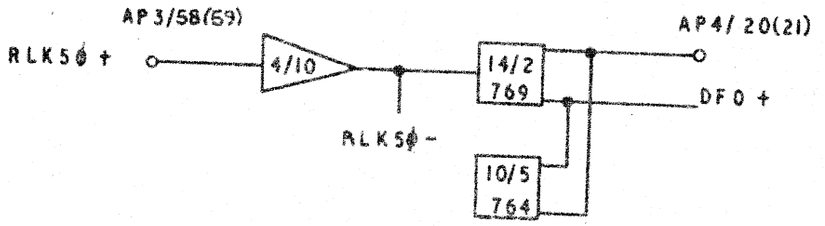


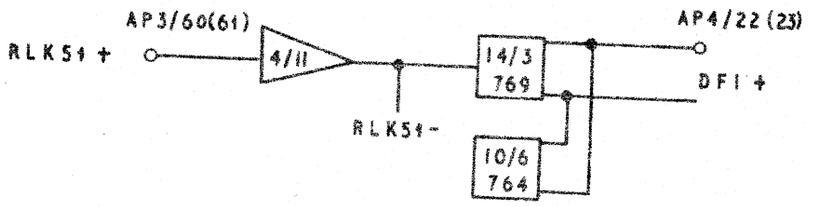


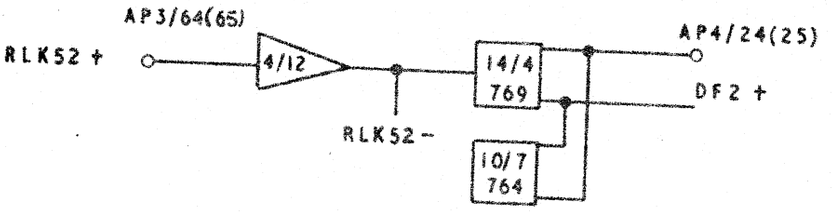
FPU. CONTROL.

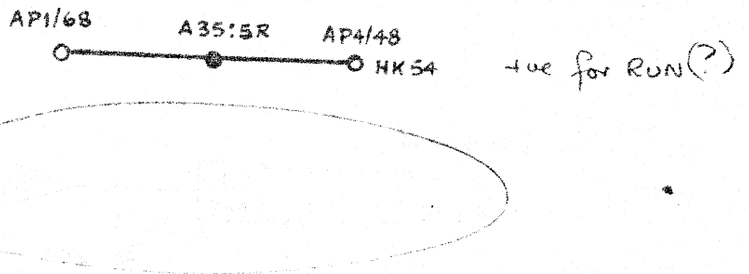
WGCϕ5/4

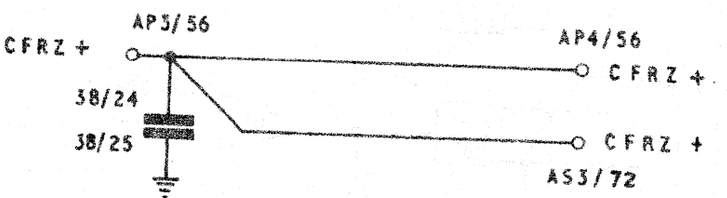
SUB.	ISS
	0749
E	7/6/67

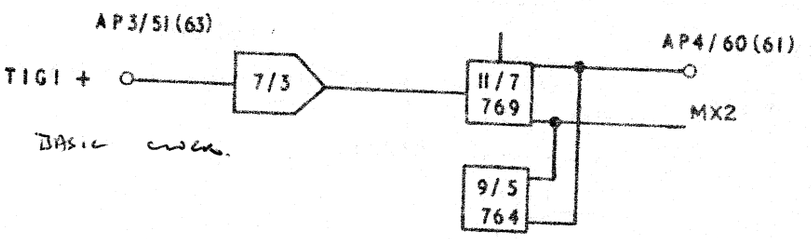

AP3/58(59)
RLK5Ø +
4/10
RLK5Ø -
14/2
769
10/5
764
AP4/20(21)
DF0 +

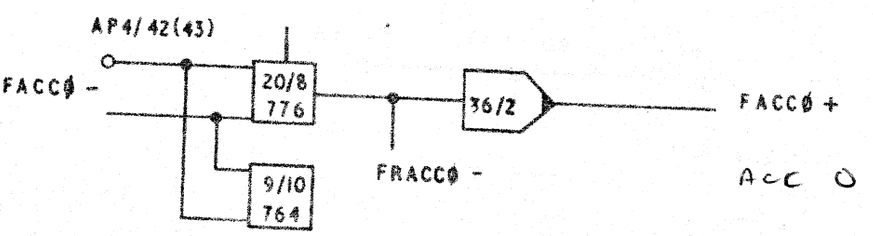

AP3/60(61)
RLK51 +
4/11
RLK51 -
14/3
769
10/6
764
AP4/22(23)
DF1 +

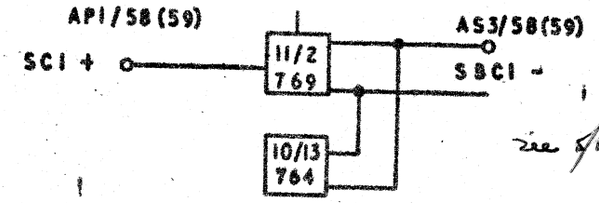

AP3/64(65)
RLK52 +
4/12
RLK52 -
14/4
769
10/7
764
AP4/24(25)
DF2 +


AP1/68
A35:5R
AP4/48
HK54
+ve for RUN(?)

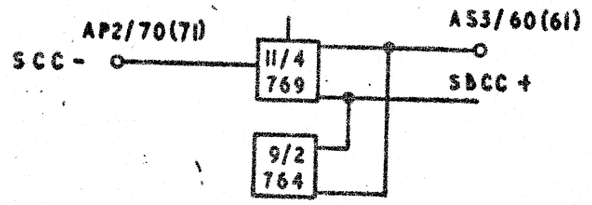

CFRZ +
AP3/56
38/24
38/25
AP4/56
CFRZ +
CFRZ +
AS3/72


AP3/51(63)
TIG1 +
7/3
BASIC CURR.
11/7
769
9/5
764
AP4/60(61)
MX2

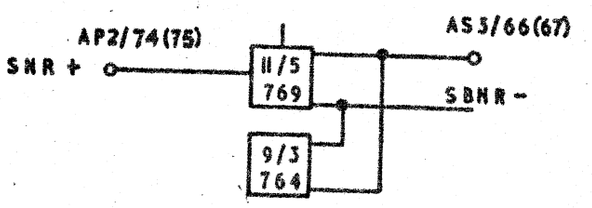

AP4/42(43)
FACCØ -
20/8
776
9/10
764
36/2
FRACCØ -
FACCØ +
Acc 0



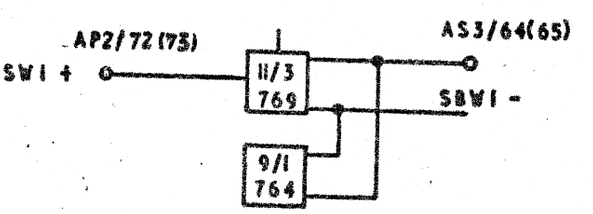
Cycle Initiate
see 5/10



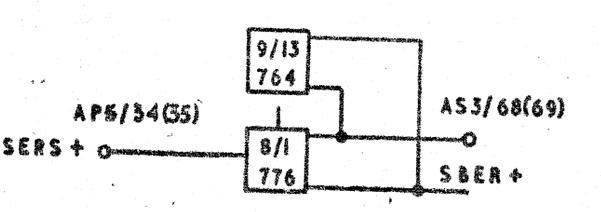
Cycle Continue



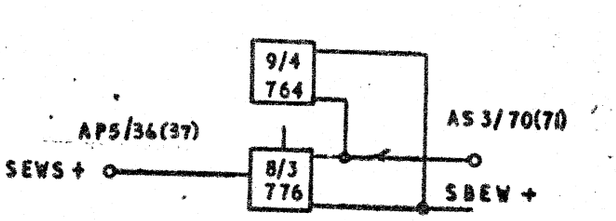
Non Restore



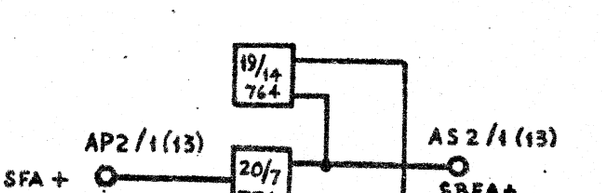
Write Initiate



End of Read



End of write

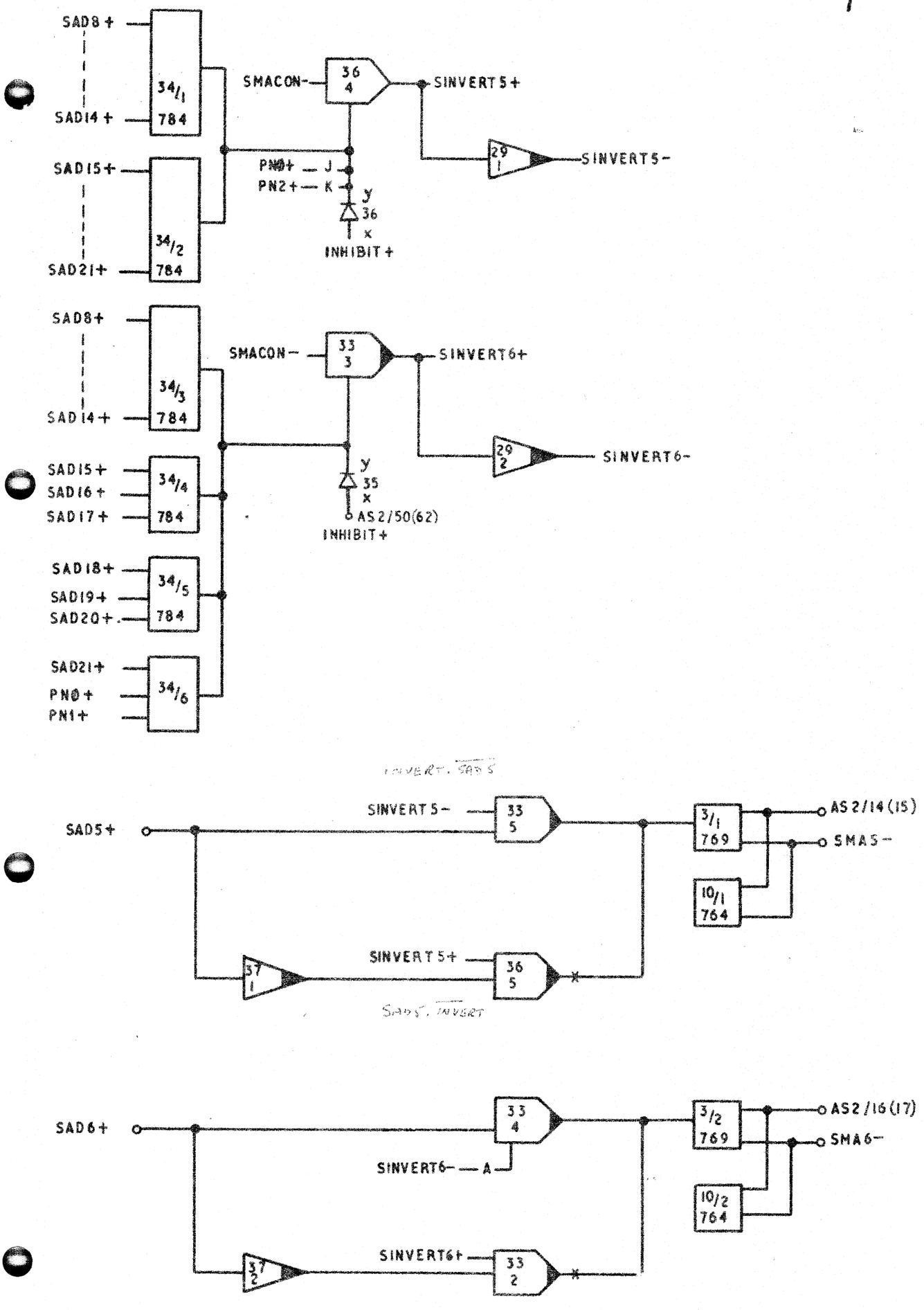


First strobe

CORE CONTROL

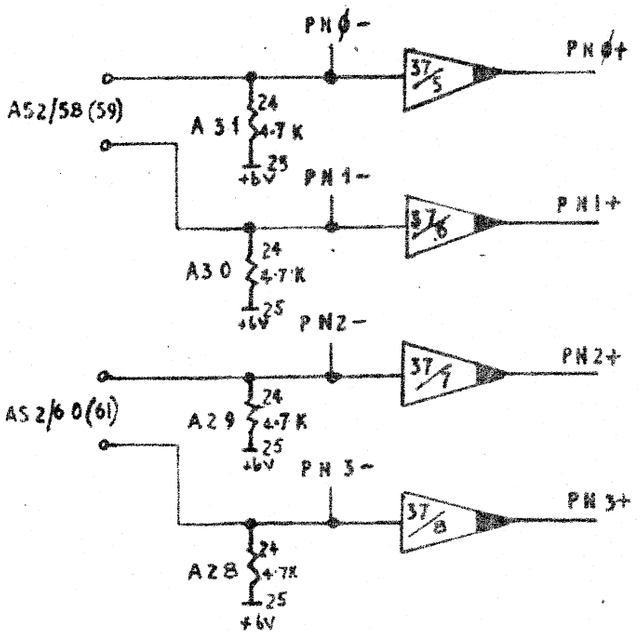
WGC Ø 5/6

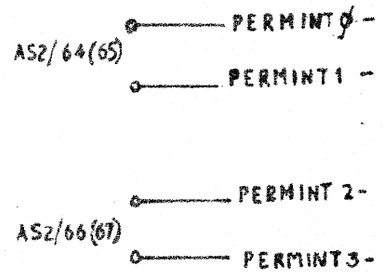
ISS	1	2
0749	0897	0950

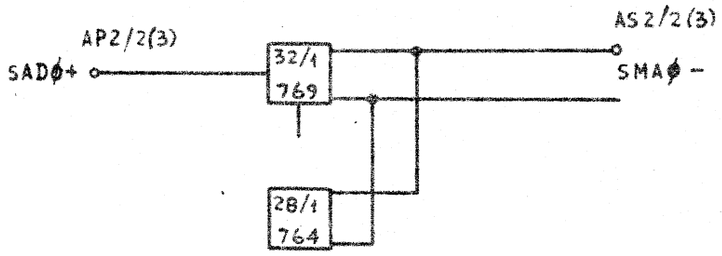


SMAC ADDRESS SCRAMBLE.

WGC 05/7.

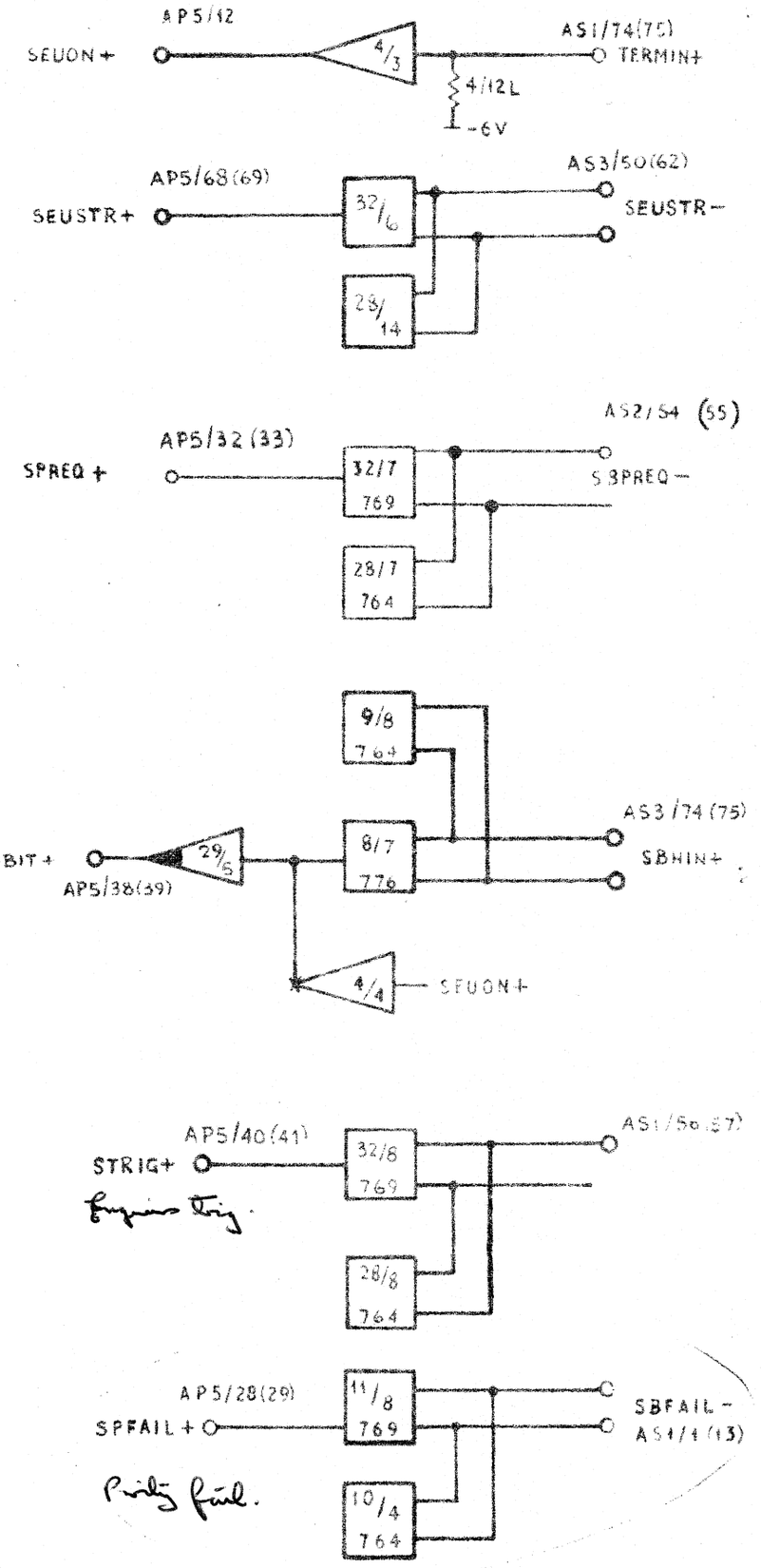


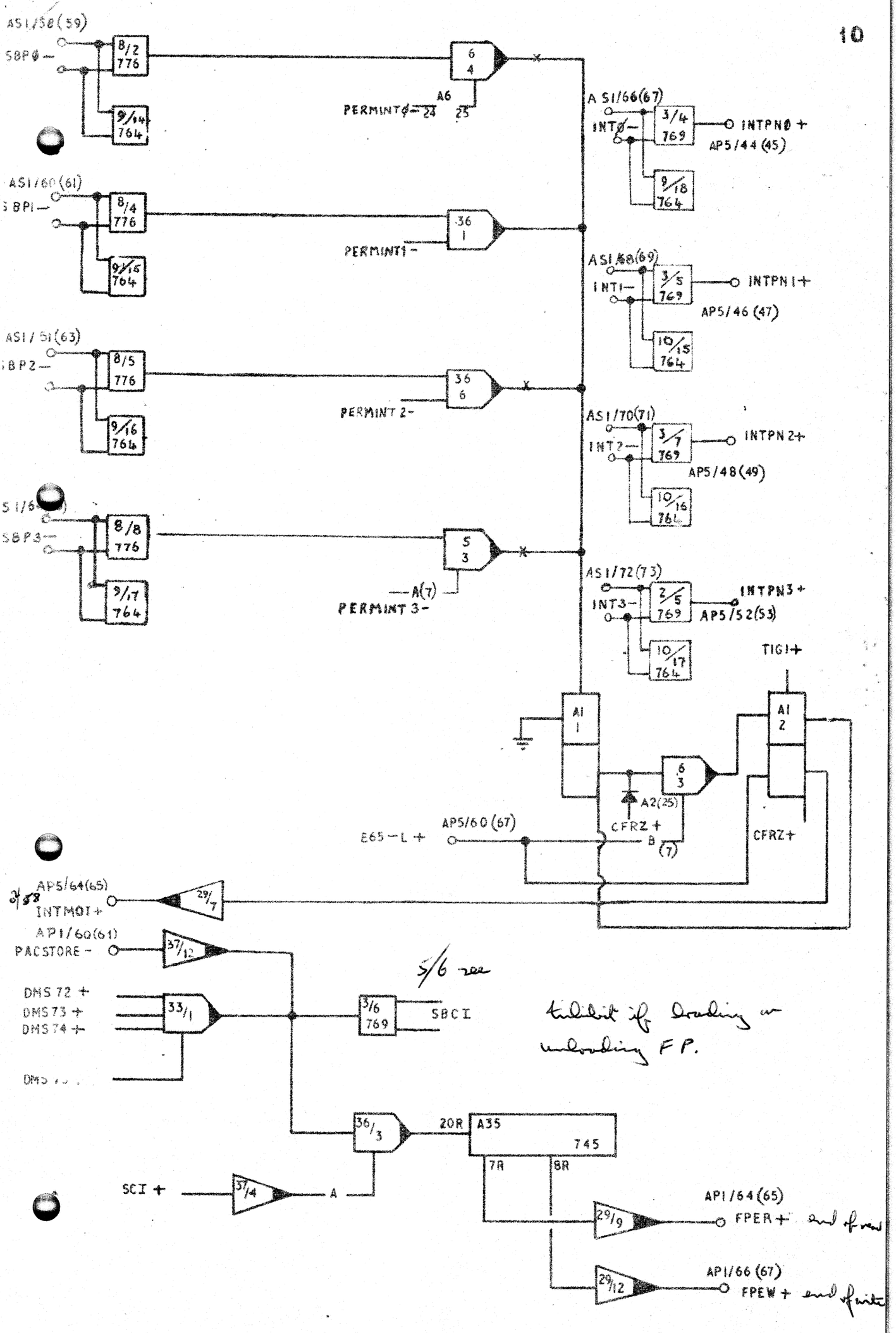




SAD / SMA	AP2 / AS2	769	764
0	2 (3)	32/1	28/1
1	4 (5)	32/2	28/2
2	6 (7)	32/3	28/3
3	8 (9)	32/4	28/4
4	10 (11)	32/5	28/5
–	–	–	–
–	–	–	–
7	18 (19)	3 /3	10/3
8	20 (21)	31/1	28/9
9	22 (23)	31/2	28/10
10	24 (25)	31/3	28/11
11	26 (27)	31/4	28/12
12	28 (29)	31/5	28/13
13	30 (31)	31/6	27/1

SAD / SMA	APS	AS2	769	764
14	6 (7)	32 (33)	31/7	27/2
15	8 (9)	34 (35)	31/8	27/3
16	10 (11)	36 (37)	30/1	27/4
17	14 (15)	38 (39)	30/2	27/5
18	16 (17)	40 (41)	30/3	27/6
19	18 (19)	42 (43)	30/4	27/7
20	20 (21)	44 (45)	30/5	27/8
21	22 (23)	46 (47)	30/6	27/9


AP5/12
SEUON+
4/3
AS1/74(75)
TERMIN+
4/12L
-6V
Stine extension unit
AP5/68(69)
SEUSTR+
32/6
28/14
AS3/50(62)
SEUSTR-
Stine extension
Unit
AS2/54 (55)
AP5/32 (33)
SPREQ+
32/7
769
28/7
764
SBPREQ-
Group 11. Logic.
9/8
764
8/7
776
SINHIBIT+
AP5/38(39)
29/5
AS3/74 (75)
SBHIN+
4/4
SEUON+
AP5/40(41)
STRIG+
Engine Trig.
32/8
769
28/8
764
AS1/50(57)
AP5/28(29)
SPFAIL+
11/8
769
10/4
764
SBFAIL-
AS1/4(13)
Priority fail.

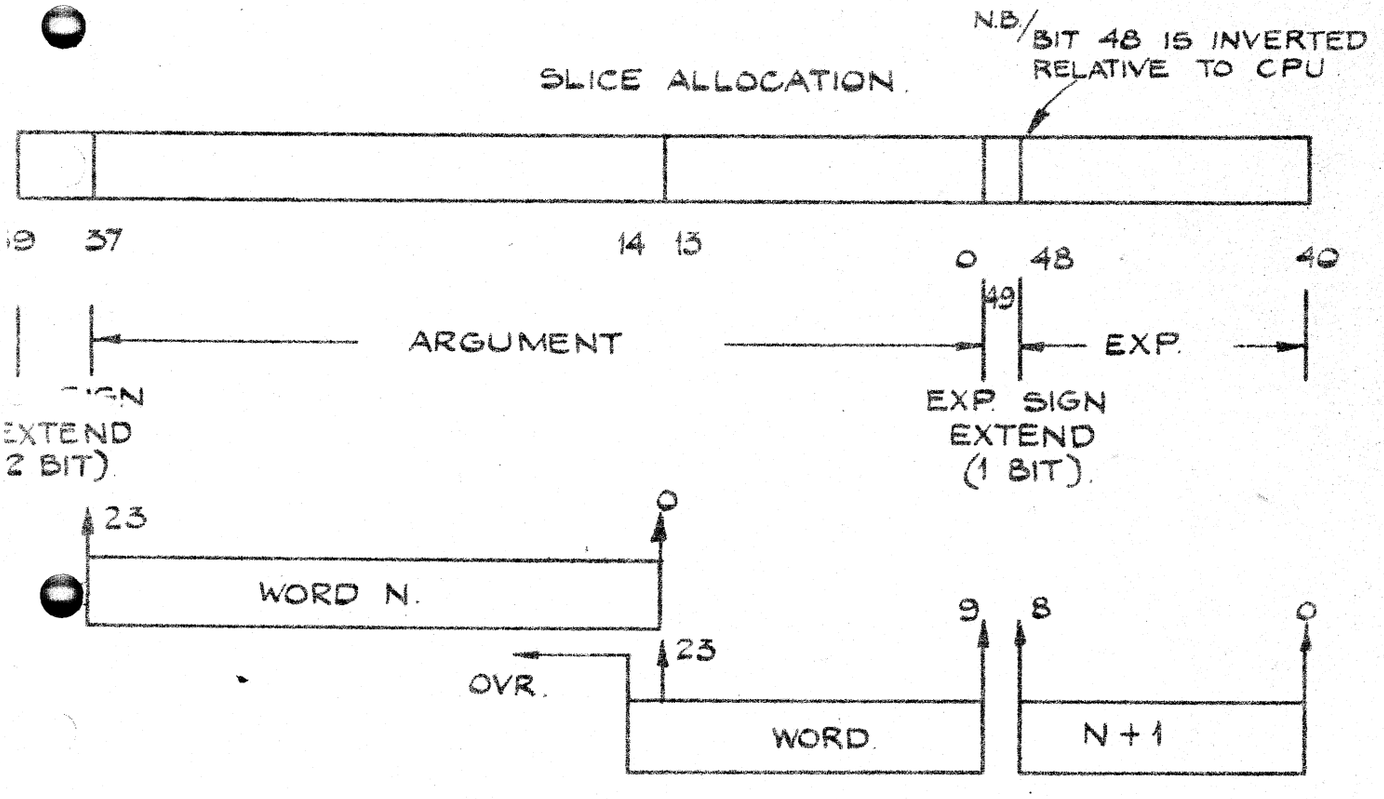


INTER PROCESSOR INTERRUPT AND FPU CONTROL

WGC05/10

DIAGRAM OF 1906/1904E BUS EQUIVALENT WAVEFORMS TO FFPU.

WORD N			WORD N+1		
1904 E	1906/FPU		1904 E	1906/FPU	
SMW =	SMR	SLICE	SMW =	SMR	SLICE
0 =	0	14	0 =	24	40
1	1	15	1	25	41
2	2	16	2	26	42
3	3	17	3	27	43
4	4	18	4	28	44
5	5	19	5	29	45
6	6	20	6	30	46
7	7	21	7	31	47
8	8	22	8	32	48
9	9	23	9	33	0
10	10	24	10	34	1
11	11	25	11	35	2
12	12	26	12	36	3
13	13	27	13	37	4
14	14	28	14	38	5
15	15	29	15	39	6
16	16	30	16	40	7
17	17	31	17	41	8
18	18	32	18	42	9
19	19	33	19	43	10
20	20	34	20	44	11
21	21	35	21	45	12
22	22	36	22	46	13
23	23	37	23	47	OVR



WGC 05/12

1905F FLOATING POINT UNIT - DELAY SETTINGS

1. FPER (SLOW STORES)

a) Insert *77777777 in *20

b) Do a manual 156 1 /0

c) FRZ

d) Do a manual 137 0 /0 on run

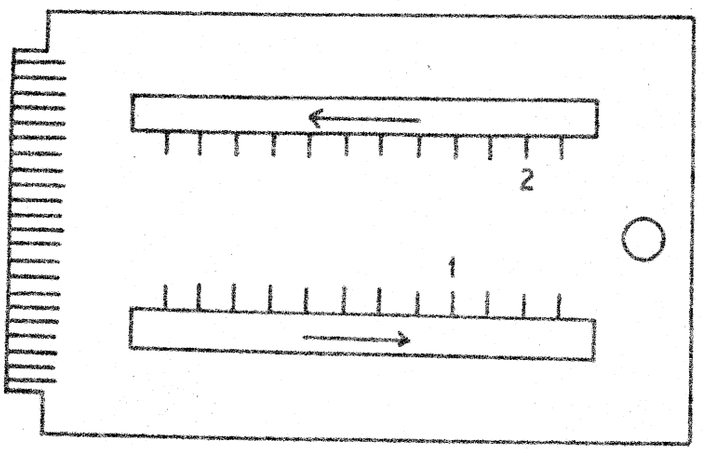
e) Trigger off 2G12/7 Door 2 -ve

f) Pick out the cycle initiate corresponding to Misc 75 (1F37/6 Door 1)

*** g) Set SINB- (2/C23/3) 50ns after SIN lines reset by measuring at Store Level Changers 2/C2,2/D2 for latest Bit by moving Tap 1 on A/35 (WGC 05)

2. FPEW

During same Misc 75 read cycle as above look at FUNLOAD+ (1/E20/1) and compare with O/P of (1E5/2).
Set FPEW so that FUNLOAD+ goes -ve not earlier than 25ns after (1/E5/2) has gone pos. by moving Tap 2 on A/35 (WGC 05)



No's = NOMINAL

745 Package
Position A/35 (WGC 05)

*** FPER (LOCKHEED STORES)

For the FAST STORE in basic position the EOR can be set as early as possible on Delay A/35.

SUB	155		
ACW	1554		
ACD			
DATE	16/10/68		