

10381 Bandley Dr. Cupertino, CA 95014 408-446-9779

7710 DISC DRIVE PRODUCT SPECIFICATION

8" 10MB SN 01746

> 7710.01-04 AUG. 1979



TABLE OF CONTENTS

Section	Heading	Page No.
1.0 2.0 3.0 3.1 3.2 3.3 3.4 3.4.1 3.4.2 3.4.3 3.4.4 3.5 3.5.1 3.5.2 3.5.3	INTRODUCTION GENERAL DESCRIPTION SPECIFICATIONS Operational Physical Dimensions Environmental Reliability Mean Time Between Failures Mean Time To Repair Preventative Maintenance Service Life Data Integrity Read Errors Write Errors Data Security	4 5 5 6 6 6 6 6 7 7 7 8 8
3.6 4.0 4.1 4.2 5.0 5.1 5.1.1 5.2 5.3 5.4 5.5 5.6 5.7 5.8 5.5 5.6 5.7 5.8 5.9 5.10 5.11 5.12 5.13 6.0 7.0 7.1 7.2 8.0 8.1 8.2	Address Errors FORMAT Format Definition Sector Selection SIGNAL INTERFACE COMMAND BUS Drive Commands Drive Status CMD R/W CMD SELECTØ, CMD SELECT1 CMD STROBE CMD ACK FAULT SEEK COMPLETE INDEX SECTOR R/W DATA SYS CLOCK SELECTED UNIT ADDRESS Terminators POWER INTERFACE PHYSICAL INTERFACE Signal Cable Connection Power Table Connection CONTROLS Sector Select and Unit Address Write Protect	8 8 8 11 12 12 13 18 21 21 21 22 22 23 23 23 23 23 23 23 23 23 23 23

7710.01-03 5/79



TABLE OF CONTENTS (Con't.)

<u>Section</u>	Heading	Page No.
9.0 9.1	INSTALLATION INSTRUCTIONS Unpacking	35 35
9.2	Mounting	35
9.3	Power	36
9.4	Interface	36
9.5	Carriage Release	36
10.0	HANDLING AND SHIPPING INSTRUCTION	40
APPENDIX A	Selector Selection for 7710 Disk Drives equipped with Logic Board Assembly No. 310071.	



FIGURES

Figure No.	Heading	Page No.
/ 1a	Short Format	9
4.16	Full Format	10
4.2	7710 Sector Format Selection Chart	11
5.1	Signal Lines	13
5.2	Command and Status Table	14
5.3	Head Addressing	15
5.4	Cylinder Address for Model 7710	15
5.5	Detectable Drive Faults	22
5.ба	TTL Signal Interface	24
5.6b	R/W DATA and SYS.CLOCK Interface	25
5.7a	Drive Select Command Cycle	26
5.7b	Drive Status Read Cycle	26
5.8a	Write Timing Diagram	28
5.8b	Read Timing Diagram	28
6.1.	Power Connector Wire Assignment	29
7.1	7710 Back Panel	31
7.2	7710 Interface Connections	32
8.1	Drive-Logic PC ASM	33
8.2	Unit Address Selection	34
8.3	Write Protection	35
9.1	7710 Drive Outline and Mounting Points	37
9.2	7710 Disc Drive Top View	38
9.3	7710 Disc Drive Bottom View	39

2



1.0 Introduction

This specification describes the characteristics and specifications of the 7710 Disc Drive and contains the information necessary to interface the 7710 to a controller.

2.0 General Description

The IMI 7710 Disc Drive is a fixed disc, sealed environment, "Winchester" technology drive. While not much larger than a floppy disc drive in size, it provides over 11 megabytes of storage (unformatted).

Its advanced technology base accomodates all major subassemblies. The low load, low mass "Winchester" type Read/Write heads are positioned with a linear voice coil actuator utilizing a closed loop, track following, servo system. The recirculating filtered air flow system within a sealed enclosure prevents contamination. The brushless D.C. drive motor with built-in disc spindle, motor electronics and speed control provides for universal 50/60 Hz operation.

Three printed circuit boards, Read/Write, Servo Control and Drive Logic are installed within the base and are interconnected with a back panel where all interface connections are made.

Primary features of the IMI 7710 Disc Drive are as follows:

- * Fixed Media (magnetically oriented and lubricated)
- * "Winchester" type recording features
- * Capacity 11.3 MB (unformatted)
- * Sealed environment, clean air filter system



- * Brushless D.C. Drive Motor
- Small size
- No scheduled maintenance
- 100 Watts power dissipation
- * All D.C. power
- * Selective Write Protect
- * Daisy chain up to 16 drives
- * VFO Data Separation standard

3.0 <u>Specifications</u>

3.1 Operational

Number of discs 2 Number of data surfaces 3 Number of tracks per surface (354 data, 4 diagnostic, 60 guardband) Number of data tracks per surface Bytes per track (unformatted) Bytes per cylinder (unformatted) Number of data cylinders Bytes per surface (unformatted) Bytes per drive (unformatted) Track density Bit density Rotational Speed Average latency Single track access time Average access time Maximum access time Data transfer rate Recording code

-5-

418 350 + 4 Alternates 10,800 32,400 350 3.78 MB 11.34 MB 300 TPI 5,868 BPI 3,500 RPM + 1% 8.33 ms 10 ms 50 ms 100 ms 648 KB/S-(5.1 Mega HZ Clock Rate) MFM

INTERNATIONAL MEMORIES. INCORPORATED

3.2

3.3

Heads per surface 1 3 Data heads Servo head 1 Start time 15 seconds (max.) 15 seconds (max.) Stop time Physical Dimensions Height 5.5" max. (13.97 cm) 8.57" max. (21.76 cm) Width 19.25" max. (48.89 cm) Length 22 lbs. (10 Kgm) Weight Environmental +50°F to 120°F Operating Temperature $(10^{\circ}C \text{ to } 50^{\circ}C)$ Operating Relative Humidity (no condensation) 20% to 80% R.H. Operating Altitude -1000 to +6000 ft. sea level Non Operating Temperature -40°F to 140°F $(-40^{\circ}C \text{ to } 60^{\circ}C)$ Non Operating Relative Humidity (no condensation) 10% to 90% R.H. $18^{\circ}F$ (10°C) per hour Temperature Variation (no condensation) Operating Vibration 0.1G (5 CPS linear increase to 100 CPS) Non Operating Vibration 1.0G (2 CPS linear increase to 100 CPS) Non Operating Shock 5.0G for 5 ms duration Reliability

3.4 <u>Reliability</u>

3.4.1 Mean Time Between Failures

MTBF is calculated to exceed 10,000 hours.

3.4.2 Mean Time To Repair

The MTTR will not exceed 0.5 hours.

-6-



3.4.3 Preventative Maintenance

There is no preventative maintenance required on the 7710 disc drive.

3.4.4 Service Life

The 7710 is designed and constructed to provide a useful life of 5 years before factory overhaul or replacement is required. Repair or replacement of major parts will be permitted during the 7710's lifetime.

3.5 Data Integrity

The following error rates assume that the 7710 is being operated within this specification and that errors caused by media defects or equipment failures are excluded.

3.5.1 Read Errors

Prior to determination of a read error rate, the data shall have been verified as written correctly and all media defects flagged.

a. Recoverable Error Rate - 1 in 10^{10} bits

The recoverable error rate is the number of errors encountered which are recoverable within 10 retries.

b. Unrecoverable Error Rate

An unrecoverable read error is one which cannot be read correctly within 20 retries (10 retries at each carriage offset). Unrecoverable read errors shall be considered as failures affecting MTBF.



3.5.2 Write Errors

Write errors can occur as a result of the following: write data not being presented correctly, media defects, or equipment malfunction. As such, write errors are not predictable as a function of the number of bits passed.

3.5.3 Data Security

The 7710 Disc Drive has several fault detection circuits to monitor conditions in the drive and to ensure that data is written on the disc properly and in the same pattern as generated by the attached controller. Data is protected by inhibiting Write Gate when a fault condition is detected. Data may be further protected by the customer through implementing the Write Protect switch.

3.6 Access Errors

There shall be no more than one positioning error in 10^6 seeks.

4.0 Format

4.1 Format Definition

The record format on the disc is determined by the controller. The index and sector pulses are available for use by the controller to indicate the beginning of a track or sector.

7710.01-03 5/79



Two typical formats have been defined for the 7710, they are illustrated in Figures 4.1a and 4.1b. Other formats are possible.

Figure 4.1a requires the least overhead (typically 39 bytes) but the header has to be re-written each time data is updated. Figure 4.1b does not require the header to be re-written, but overhead has increased to 70 bytes.

Format A

Header is always re-written each time data is updated.



Note: I.D. may be expanded by any number of bytes to suit the user. It may include flag bits to indicate write protect and/or defective sector. Sync Byte is Ø1 Hex. Read Gate must drop 1 byte before end of Postamble.

Figure 4.1a



Format B

Header is not re-written each data update.

FULL FORMAT



Note: I.D. may be expanded by any number of bytes to suit the user. It may include flag bits to indicate write protect and/or defective sector. Sync Bytes are Ø1 Hex. Read Gate must drop 1 byte before end of Postamble.

Figure 4.1b

7710-01-00 1/79



4.2 Sector Selection

NOTE: The sector selection described in this section is for 7710 Disk Drives equipped with "7710 Drive Logic" PCB Assembly No. 310036.

> This PCB has been superseded by "LOGIC BD" Assembly No. 310071 which is fully interchangeable with the preceeding Logic PCB. See Appendix A for the sector selection description for 7710 Disk Drives equipped with this Logic PCB.

Sector selection is done by setting the four mini dip switches located on the Drive Logic Card (see Figure 8.1).

The standard selectable options and switch settings are shown in Figure 4.2. All other sector lengths require a special PROM and are by special order only.

7710 SECTOR FORMAT SELECTION CHART

Sectors	Bytes Per	Se	cto	r Se	elect	Data Cap	acity - Fo	rmatted
Per	Sector	SW	itcl	n ((1A)	Format A	Format B	Data Bytes
Track	(Unformatted)	S ₁	s,	Sa	S _A	(MB)	(MB)	Per Sector
				<u> </u>				
2	5,400							
3	3,600							
4	2,700							
5	2,160							
6	1,800						*	
8	1,350						3	
9	1,200	C	0	0	0		9.68	1,024
10	1,080	0	0	С	С	10.75	1	1,024
12	900	0	С	С	C		1	
15	720	0	0	0	C			
18	600	0	0	С	0	a.68	9.68	512
20	540	C	0	С	C .			
24	450							
25	432						1	
27	400						1	
30	360	0	С	С	0		8.06	256
36	300	0	C	0	С	9.68		256
40	270	C	С	С	С		1	
45	240						•	
50	216	1					ŧ	
54	200	C	С	0	С		7.26	128
60	180	C	С	С	0	8.06		128
72	150						1	
90	120						i i	

Notes:

Figure 4.2

- 1) Entries in Sector Select column denote sector options selectable with standard PROM. Other sector lengths will be provided on a special order basis.
- 2) Switch: C = ON or Closed, O = OFF or Open

3) Use of number of sectors per track other than those listed as standard will result in an additional short sector being added to the number specified.



5.0 Signal Interface

The single interface cable communicates control, status, timing, clock and data between the controller and up to 16 drives. The 25 signal line bus connection is implemented using a 34 conductor flat cable which is readily daisy-chained to multiple drives. The Signal Lines are shown in Figure 5.1

The control and status transfer between the controller and drives is fully asynchronous. The bus signals use a strobe (CMD STROBE) and are acknowledged by CMD ACK.

The signals on the bus are standard TTL level (negative true, logical "1" = 0 to 0.7 V, logical " \emptyset " = 2.4 to 5.0 V), with the exception of R/W DATA, and SYS CLOCK, which use industry standard differential driver/receivers (SN 75107 and SN 75110) to ensure data integrity. Recommended interface circuits are shown in Figure 5.6 and interface timing is shown in Figures 5.7 and 5.8.

5.1 COMMAND BUS

The COMMAND BUS is an 8 bit bidirectional bus (identified as CMD BUSØ-CMD BUS7) that carries commands to the drive from the controller. This bus is open-collector TTL compatible with provision to attach a terminator on the last drive to allow stringing of multiple drives. Bus direction is controlled by the controller. The meaning of each bit in this bus depends upon the state of 3 other lines: CMD R/W; CMD SELECTØ: and CMD SELECT1 which define the 8 command bytes (CMD BYTE). 4 command bytes (CMD BYTE Ø-3) are for drive commands and 4 command bytes (CMD BYTES 4-7) are for drive status. Up to 32 bits of command and 32 bits of status can be transferred between the drive and the controller using these lines (see Figure 5.2). The drive ignores the state of the COMMAND BUS except when CMD STROBE is active. After CMD STROBE has gone active (200ns to 200 µs), the CMD ACK line is set to an active level.



5.1.1 Drive Commands

CMD BYTE Ø:

Bits 4-7

UNIT SELECT (USØ-US3) - The four unit select bits (USØ-US3) are used to address one of sixteen drives. Each drive has a 4-bit binary unit address preassigned by a 4-bit DIP switch on the drive logic board. Figure 8.2 shows switch settings for unit selection.







7710.01-00 1/79

-13-



COMMAND AND STATUS TABLE

	CMD BYTE	CMD R/W	CDM SEL1	CDM SELØ	CMD BUS 7	CMD BUS 6	CMD BUS 5	CMD BUS 4	CMD BUS 3	CMD BUS 2	CMD BUS 1	CMD BUS Ø
SC	ø	P	ø	P	US 3	US 2	US 1	US Ø	HSA 1	hsa ø	CAR 9	CAR 8
IMA NI	1	Ø	Ø	1	CAR 7	CAR 6	CAR 5	CAR 4	CAR 3	CAR 2	CAR 1	CAR Ø
IVE COM	2	Ø	1	ø	Servo Offset Reverse	Servo Offset Forward			Diag- nostic		Read Gate	Write Gate
DR	3	Ø	1	1							Rezero	Fault Clear
S	4	1	p	Ø	Speed Error	Illegal Addr.	R/W Fault	Servo Error	Re-Zero ing	Seek- ing	On Cyl.	Unit Ready
STATI	5	1	p	1	Guard Band			Write Prot'd.	PLÕ Error	POR		R/W Unsafe
ΙVΕ	6	1	1	Ø	PAR 7	PAR 6	PAR 5	PAR 4	PAR 3	PAR 2	PAR 1	PAR Ø
DR	7	1	1	1	UA 3	UA 2	UA 1	UA Ø	HAR 1	har ø	PAR 9	PAR 8

Notes:

1) USØ-3 = Unit Select 2) $CAR\emptyset-9$ = Cylinder Address Register 3Ĵ HSAØ-1 -Head Select Address 4) $HAR \emptyset - 1$ = Head Address Register 5) PARØ-9 = Present (Cyl.) Åddress Register6) UAØ-3 = Drive's preassigned unit select address 7) Space = Unused Bit (normally at logical zero) 8) Negative True Logic: Logical 1 = 0 to 0.7 V Logical $\emptyset = 2.4$ to 5.0 V



<u>Bits 2,3</u>

<u>HEAD SELECT ADDRESS (HSAØ-HSA1)</u> - The Head Select Address command is used to load the addressed head number into the Head Address Register. The Head Address Register is used to select one of three heads (one head per disc surface). Head addressing is shown in Figure 5.3

HEAD ADDRESSING

		HEAD ADDREDD	110	
	HEA RE	D ADDR. GISTER	HEAD	
1	HAR1	HARØ	SELECTED	
And a second reserves and a second second	Ø Ø 1 1	Ø 1 Ø 1	0 1 2 N/A	

Figure 5.3

Note: Head address validation is not performed by the drive. If validation is required, the check must be performed by the controller.

CMD BYTES Ø & 1:

Bits 0, 1 (CMD BYTE Ø) Bits 0-7 (CMD BYTE 1)

<u>CYLINDER ADDRESS REGISTER (CARØ-CAR9)</u> - Ten cylinder address bits (CARØ-CAR9) are used to address the drive's cylinder address register. CMD BYTE Ø contains bits CAR8, 9. CARØ-7 are in CMD BYTE 1. Possible addresses for the drive are shown in Figure 5.4.

			<u>_</u>	IL.	1 141	JEI	K /	101	JRE	:22	FUR	MUUI	1L	11	10
		(CAP	२	(B	ina	ary	1)				C/	٩R	(D	ecimal)
	9	8	7	6	5	4	3	2	1	0	İ	CYL	_ []	NDE	R/TRACKS
1	Ø	Ø	Ø	Ø	Ø	Л	Ø	Ø	Ø	Ø		Ŋ	0	0	
1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	ĺ	0	0	1	
	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø		Ŋ	0	2	
	Ø Ø Ø	1 1 1	9 9	1 1 1	Ø 1 1	1 Ø Ø	1 Ø Ø	1 Ø Ø	1 Ø Ø	1 Ø 1		3 3 3	555	1 2 3	354 data tracks total

CYLINDER ADDRESS FOR MODEL 7710

Figure 5.4

7710.01-00 1/79

-15-



The drive validates all cylinder addresses. An illegal address status bit is set when an address greater than 353 (decimal) is specified.

CMD BYTE 2:

<u>Bit Ø</u>

<u>WRITE GATE (CBØ)</u> Gates bidirectional differential R/W Data line to the drive as "WRITE DATA" as well as enables Write Drivers to write onto the data surface of the disc.

Bit 1

<u>READ GATE (CB1)</u> enables digital READ DATA to be transmitted by the drive onto the bidirectional differential R/W Data line to the control unit.

Bit 2

NOT USED

Bit 3

DIAGNOSTIC causes the drive unit to ignore R/W UNSAFE condition while any other CMD BYTE 2 drive command is active.

Bit 4

NOT USED

Bit 5

NOT USED

Bit 6

OFFSET FORWARD causes the actuator to offset the read/write heads 0.0001016 mm (400 microinches) away from the normal on-cylinder position, in the direction towards the spindle. During the offset operation, ON CYLINDER



goes false until the offset position is reached. ON CYLINDER remains true while the read/write heads are returning to the nominal on cylinder position. OFFSET FORWARD may be used in the ERP (Error Recovery Procedure).

Bit 7

OFFSET REVERSE causes the actuator to offset the read/write heads 0.0001016 mm (400 microinches) away from the normal on-cylinder position, in the direction away from the spindle. During the offset operation, ON CYLINDER goes false until the offset position is reached. ON CYLINDER remains true while the read/write heads are returning to the nominal on-cylinder position. OFFSET REVERSE like OFFSET FORWARD may be used in the ERP.

CMD BYTE 3:

<u>Bit Ø</u>

FAULT CLEAR resets the selected drives fault status flip-flops.

<u>Bit 1</u>

<u>REZERO</u> causes the actuator to position the read/write heads to cylinder 000 and resets the head and cylinder registers to zero. The ON CYLINDER status is cleared at the start of the REZERO command. REZERO command also clears any servo error or R/W fault. SEEK.COMPLETE is generated at the end of REZERO command.

Bits 2-7

NOT USED



5.1.2 Drive Status

CMD BYTE 4:

Bit Ø

<u>UNIT READY</u> - This signal being true indicates the drive has no FAULT and is ready to read, write or seek.

Bit 1

ON CYLINDER - This signal indicates the completion of a successful seek operation.

Bit 2

<u>SEEKING</u> - This signal indicates the drive is in the process of seeking to a new cylinder address.

Bit 3

<u>REZEROING</u> - This signal indicates the drive is processing a REZEROING command.

Bit 4

<u>SERVO ERROR</u> - This signal being true indicates the selected drive has detected a SEEK ERROR condition in the drive. The following conditions, detectable by the drive, are the possible causes for a SEEK ERROR:

- a) Seek Incomplete
- b) Rezero Incomplete
- c) Invalid Address
- d) Guard Band Detected

Except for Invalid Address and Guard Band Detected, servo error causes servo to go to "disable" state which can be reenabled only with REZERO command or Power Up Reset. FAULT CLEAR also resets Servo Error status



signal provided condition causing Servo Error is no longer present.

Bit 5

 $\frac{R/W}{FAULT}$ -This signal indicates when one of the following R/W fault conditions is detected:

- a) Multiple head selected.
- b) Write current with no write data.
- c) Write current with no write gate.

 R/W FAULT is cleared by the FAULT CLEAR or REZERO command.

Bit 6

ILLEGAL ADDRESS - This signal indicates that the CAR address is greater than 353 (decimal).

Bit 7

<u>SPEED ERROR</u> - This signal indicates that the disc motor speed is outside of 3600 RPM \pm 10%.

CMD BYTE 5:

Bit Ø

<u>R/W UNSAFE</u> - This signal indicates that a FAULT signal (see 5.6) is detected.

Bit 1

NOT USED

Bit 2

<u>POWER ON RESET (POR)</u> provided a 12-15 second delay time to allow the drive motor to come up to speed and reset all internal logic to a known state.

INTERNATIONAL MEMORIES, INCORPORATED

<u>Bit 3</u>

<u>PLO ERROR</u> - This signal indicates that the servo phase lock oscillator is not in sync with the servo clock pulses derived from the servo clock track.

Bit 4

WRITE PROTECT - This is a status signal sent to the controller which indicates the drive is operating in a read only mode. WRITE PROTECT will prevent a write operation. The WRITE PROTECT function is made available to the user via pins on the back panel. See 8.2.

Bits 5, 6

NOT USED

<u>Bit 7</u>

<u>GUARD BAND</u> - This signal indicates that the drive is outside the data track area.

CMD BYTES 6 & 7:

Bits Ø-7 (CMD BYTE 6) Bits Ø,1 (CMD BYTE 7)

PRESENT ADDRESS REGISTER (PARØ-PAR9) - The PAR indicates the binary address of the present cylinder address.

CMD BYTE 7:

Bits 2, 3

<u>HEAD ADDRESS REGISTER (HARØ-HAR1)</u> - The HAR indicates the binary address of the present head address.



Bits 4-7

<u>UNIT ADDRESS (UAØ-UA3)</u> - These four bits indicate the binary unit select number preassigned by the 4 bit DIP switch in the drive (see Figure 8.1).

5.2 CMD R/W

The CMD R/W line defines which direction the COMMAND BUS is operating relative to the controller. A logical "1" on CMD R/W indicates that the controller is reading one of four status bytes from the selected drive. A logical "Ø" on CMD R/W indicates that the controller is writing one of four command bytes to the selected drive. CMD R/W is asserted 200 ns before the CMD STROBE goes active and must remain unchanged until CMD STROBE goes active and must remain unchanged until CMD STROBE goes inactive.

5.3 CMD SELECTØ, CMD SELECT1

The CMD SELECTØ line is the least significant bit of command/status bus address, and CMD SELECT1 is the most significant bit of command/status bus address. The controller encodes these 2 lines for one of four command or status bytes (depending on CMD R/W) currently being sent or received on the COMMAND BUS.

CMD SELECTØ and CMD SELECT1 are negative true logic levels. CMD SELECTØ and CMD SELECT1 are asserted 200 ns before the CMD STROBE goes active and must remain valid until CMD STROBE goes inactive.

5.4 CMD STROBE

CMD STROBE is the initiating strobe of the control handshake, and is generated by the controller and sent to all disc drives on the bus. The selected drive will respond by accepting a command byte or placing a status byte on the

INTERNATIONAL MEMORIES, INCORPORATED

COMMAND BUS and returning an acknowledge (CMD ACK) to the controller. When a command byte is being written to the drive. the drive logic delays latching of the command to insure that all COMMAND BUS lines have reached the proper level before the command is captured. CMD STROBE is a negative true level.

5.5 CMD ACK

The CMD ACK signal is generated by the drive in response to CMD STROBE and indicates that the drive has responded to the bus operation by latching the command byte (CMD R/W low), or placing the requested status byte on the COMMAND BUS (CMD R/W high). CMD ACK is a negative true level and returns to an in-active level (high) after CMD STROBE goes inactive.

5.6 FAULT

The FAULT signal is generated by the drive whenever a fault condition exists as outlined in Figure 5.5. This line is cleared by a FAULT CLEAR or a REZERO command.

When FAULT goes true, the write circuits are inhibited immediately to prevent destruction of customer data. Figure 5.5 lists the conditions which can be detected by the drive causing a FAULT signal to be generated.

FAULT is asserted only when the drive is selected. FAULT is a negative true level signal.

DETECTABLE DRIVE FAULTS

Multiple Heads Selected Write Current with No Write Data Write Current with No Write Gate Write Gate with No On Cylinder Indication Phase Locked Oscillator Sync Error

Figure 5.5



5.7 SEEK COMPLETE

The SEEK COMPLETE signal is generated by the drive whenever a SEEK command has been successfully completed or a servo error is encountered aborting seek operation. SEEK COMPLETE may be generated by multiple drives and is located by polling status. SEEK COMPLETE is a negative true pulse of $3-5 \ \mu$ s duration.

5.8 INDEX

This signal is derived from a pattern on the servo track and is generated by the drive once every disc revolution (16.67 msec) for approximately 3 μ sec. The leading edge of INDEX defines the start of sector 000.

5.9 SECTOR

The SECTOR signal is generated by the currently selected drive and is active for approximately 3 μ sec. The disc is formatted using hard sectoring. The number of data bytes per sector is switch selectable (Figures 4.2 and 8.1). SECTOR is a negative true level signal.

5.10 R/W DATA

R/W DATA is a bidirectional differential signal that transmit NRZ read data from the currently selected drive to the controller when READ GATE is active, and NRZ write data to the drive when WRITE GATE is active. The differential line pair driver, receiver and termination are shown in Figures 5.6a and 5.6b.

5.11 SYS CLOCK

SYS CLOCK is a differential signal that transmit a 5.184 MHz clock to the controller for both read and write clock. During read operation, SYS CLOCK is synchronized to the data transitions through the data separator's VFO, so that the rising edge of clock is accurately centered on



the NRZ data cell. During write operation, SYS CLOCK is locked to the PLO, which is locked to the servo surface sync bit transitions. The controller uses the leading edge of SYS CLOCK to generate NRZ write data to the drive to ensure proper data encoding.

5.12 SELECTED UNIT ADDRESS

SELECTED UNIT ADDRESS consists of four (4) TTL compatible lines (SEL.UNIT.ADDR. \emptyset -SEL.UNIT.ADDR.3) carrying signals generated by the currently selected drive, and represents the binary value of that drive's unit select address number.



TYPICAL DRIVER SN7438 or equivalent TYPICAL RECEIVER SN 74LS14 or equivalent

Figure 5.6a



R/W DATA & SYS CLOCK INTERFACE



Note: Decoupling capacitors $(0.1 \ \mu f \ typical)$ are required on +5V and -5V power supply pins for each driver or receiver chip.

Figure 5.6b

7710.01-00 1/79

-25-



Figures 5.7a and 5.7b show timing relationships of pertinent signals for the COMMAND and STATUS cycles, respectively.

DRIVE SELECT COMMAND CYCLE





DRIVE STATUS READ CYCLE



Figure 5.7b



5.13 Terminators

A termination resistance as shown in Figure 5.6a is required at each end of the signal interface cable. This resistance is supplied on the drive by the 2 terminating resistor packs inserted on the Back Panel. If the drive is not used as a single drive or the last drive in a daisy-chain, these two terminators should be removed.

The terminating resistor packs are CTS Part No's. 760-1-R100 - and 761-5-R220/330(or equivalent). They are inserted into connectors on the Back Panel (Figure 7.1) with pin no. 1 in the lower left corner of the socket, as viewed from the rear of the drive.



Figures 5.8a and 5.8b show the timing relationship of pertinent signals for Write and Read operations. Positive "true" logic applies to these diagrams.

WRITE TIMING DIAGRAM 25 Bytes of Zero's - 38.6 μs Sync Byte WRITE GATE Write Data (R/W DATA) HEADER/DATA SYS CLOCK 96.5 ns Nom.* * Based on Spindle Speed Data changes on positive edge of 3600 RPM. 193 ns Nom.* of SYS CLK. Figure 5.8a READ TIMING DIAGRAM READ GATE 96.5 ns Nom.* 193 ns Nom.* SYS CLOCK



Data changes on Negative edge of SYS CLK.

* Based on Spindle Speed of 3600 RPM Figure 5.8b



6.0 Power Interface

The following DC power must be provided to the drive:

+ 5.0 ± 0.25 VDC @ 4.0A Max., 50 MV ripple +12.0 ± 0.60 VDC @ 0.5A Max., 50 MV ripple -12.0 ± 0.60 VDC @ 0.5A Max., 50 MV ripple -5.0 ± 0.25 VDC @ 3.0A Max., 50 MV ripple +24.0 ± 2.5 VDC @ 4.0A Max., (peak starting) 2.0A Typical running 50 MV ripple through 50 MHz

The 10 pin DC power connector is assigned as follows: (See Figures 6.1 and 7.1)

POWER CONNECTOR WIRE ASSIGNMENT

10	+ 5 V
9	+ 5 V
8	GROUND
7	GROUND
6	+ 12 V
5	- 12 V
۵	- 5 V
3	N/C
2	+ 24 V RETURN
1	+ 24 V

Figure 6.1



7.0 Physical Interface

7.1 Signal Cable Connection

The Signal Cable utilizes a 34 conductor flat cable. The connector plugs directly onto the back panel of the 7710 drive. Connection locations on the back panel (Figure 7.1) are marked with silk screen outline on the panel and pin 1 (cable reference band lead) of the connector mates with pin C or D 119 on the back panel, pin 2 of the connector with pin C or D 120 on the back panel, pin 3 of the connector with pin C or D 117, etc.

For the Signal Cable pins rows C and D are common. Daisy-chain connection is accomplished by either using separate cables between each drive or a single daisy-chain cable. Connection is made by either one or both of the above back panel locations

A recommended connector is AMP P/N 88550-1 or equivalent, and for the cable, Spectra Strip P/N 4550240-34, or equivalent. See Figure 7.2 for Signal Cable Connector pin assignments.

7.2

Power Cable Connection

A 10 conductor power cable connector is attached to the corresponding jack on the back panel of the 7710 drive. The recommended connector housing is AMP P/N 1-640431-0. Numbers 18-20 AWG standard wire is recommended for the power cable. (See Figure 7.1)



7710 BACK PANEL



Figure 7.1



7710 INTERFACE CONNECTIONS

Interface Connector AMP P/N 88550-1 or equivalent. Interface Cable (25 feet max.) SPECTRA STRIP P/N 4550240-34 or equivalent.

S	I	GN	A	L	С	0	٧N	E	CT	I	ONS	

(CONNECTO)R	CONNECTO	R
	PIN	SIGNAL LINE	PIN	
	01	GROUND	01	
	02	GROUND	02	
Н	03	SPARE*	03	7
	04	SPARE*	04	
0	05	-SEL UNIT ADDR 3	05	7
	06	-SEL UNIT ADDR 2	06	
S	07	+R/W DATA	07	1
	80	-R/W DATA	08	
Т	09	-SEL UNIT ADDR 1	09	0 .
	10	-SEL UNIT ADDR Ø	10	
	11	+SYS CLOCK	11	
	12	-SYS CLOCK	12	
	13	GROUND	13	
	14	GROUND	14	
	15	-SECTOR	15	D
С	16	-INDEX	16	
	17	-SEEK COMPLETE	17	I
0	18	-FAULT	18	
-	19	-CMD STROBE	19	S .
Ν	20	-CMD R/W	20	-
	21	-CMD SELECT Ø	21	C
Т	22	-CMD SELECT 1	22	
•	23	SPARE*	23	
R	24	SPARE*	24	
	25	-CMD ACK	25	
0	26	SPARE*	26	n
J.	27	-CMD BUS 6	27	0
I	28	-CMD BUS 7	28	R
-	29	-CMD BUS 4	29	
1	30	-CMD BUS 5	30	T
-	31	-CMD BUS 2	31	1
F	32	-CMD BUS 3	32	v
-	33	-CMD BUS Ø	33	v
D	34	-CMD BUS 1	34	F

- * Note: Spare lines are all jumpered to ground at the drive.
- ** Note: Pin 01 of the Signal Interface Cable corresponds to pin 119 on the 7710 Back Panel Assembly. The cable reference band lead of the flat cable connects to connector pin 1.

Figure 7.2

7710.01-04 8/79



8.0 <u>Controls</u>

8.1 Sector Select and Unit Address

There are two customer selectable DIP switches on the 7710 Drive Logic PCB. These are the Sector Select Switch (4 binary positions) and Unit Address Switch (4 binary positions). The location of these switches are as shown in Figure 8.1 below.

The exact function and settings for the Sector Select Switch is described in Section 4.2. The Unit Address Switch is set as shown in Figure 8.2.



DRIVE LOGIC PC ASM

Figure 8.1

-33-



DRIVE		UNIT AL	DDRESS	
UNIT	SW1	SW2	SW3	SW4
ŋ	С	С	С	С
1	С	Ċ	С	0
2	Ċ	Ċ	Ō	Ċ
3	Ċ	č	Õ	Õ
4	Č	õ	č	õ
5	Č	õ	Č	Õ
ĥ	č	õ	õ	Č
7	Č	õ	õ	õ
8	Ő	Č	č	Č
q	ñ	č	Č	Õ
10	õ	Č	õ	Č
11	Õ	č	õ	Õ
12	Ő	ñ	č	Č
13	0 0	ñ	ř	õ
14	ñ	ň	ň	č
15		0	0	õ
IJ	0	U	0	U

UNIT ADDRESS SELECTION

Note: C = switch on (Switch Depressed) O = switch off

Figure 8.2

8.2 Write Protect

The Write Protect function is made available to the user through a user supplied remote switch connected to the appropriate pins on the back panel. The remote switch selects the appropriate grounding of Pins C-15 and C-13 to the GROUND Pin C-1 as shown in Figure 8.3. (See also Figure 7.1)



WRITE	PROT	ECTION
and the second sec	and the second se	the second s

 WRITE P CONNEC PIN C-15	ROTECT TION PIN C-13	SURFACE PROTECTED					
0 C C 0	С 0 0	Surface Ø Only Surface 1 Only All Three Surfaces No Write Protect On Any Surface					

Note: C = Switch ON between GROUND (C-1) and indicated pin

0 = Switch OFF between GROUND (C-1)
 and indicated pin

Figure 8.3

- 9.0 Installation Instructions
 - 9.1 Unpacking

Stand box on end. Open end flaps. Remove inner box and lay flat. Open both ends of inner box. Push unit through to support surface. Do not drop.

9.2 <u>Mounting</u>

The 7710 is designed for mounting on slides, and mounting holes are provided as shown in Figures 9.1 and 9.2.

The 7710 may be operated horizontally (on its base) or vertically on either side. It is not to be operated upside down or on end.

7710.01-00 1/79

-35-



The 7710 draws cooling air through the bottom. Cut-outs in the sides (near front of unit) provide for adequate air flow when mounted on the flat solid surface. Insure that air flow is not restricted. (See Figure 9.3).

9.3 Power

Voltages and connection points are shown in Figures 7.1 and 9.2. All power should be supplied at the same time, and different voltages should be up within 20 msec of each other (See Section 6.0 and 7.2).

9.4 Interface

The location of the interface lines are shown in Figure 7.1. See Section 5.0 for interface definitions and specifications.

9.5 Carriage Release

The head carriage is provided with a carriage lock to protect the disc surfaces during shipment or relocation. ALWAYS UNLOCK THE CARRIAGE LOCK PRIOR TO APPLYING POWER TO THE UNIT. ALWAYS LOCK THE CARRIAGE LOCK PRIOR TO MOVING OR SHIPPING THE UNIT.



7710 DRIVE OUTLINE AND MOUNTING POINTS



Figure 9.1

NOTE: All dimensions in inches unless indicated.





Figure 9.2

-38-





Figure 9.3



10.0 Handling and Shipping Instructions

- 10.1 The 7710 has an exposed spindle ground strap on the underside of the unit. Always place the unit on a flat smooth surface. <u>DO NOT</u> slide the unit on a rough surface as the ground strap may catch and be damaged.
- 10.2 The 7710 is provided with a carriage lock to protect the disc surfaces during shipment. ALWAYS UNLOCK THE CARRIAGE LOCK PRIOR TO APPLYING POWER TO THE UNIT. ALWAYS LOCK THE CARRIAGE LOCK PRIOR TO MOVING OR SHIPPING THE UNIT.
- 10.3 The 7710 should be protect from undue shock and vibration. During shipment the unit should be packaged in its original shipping container (or equivalent) unless the equipment in which it is installed is shipped in a manner which provides similar shipping protection.



APPENDIX A

Sector Selection for 7710 Disk Drives equipped with Logic Board Assembly No. 310071.

1. SECTOR SELECTION

Sector selection for disk drives equipped with the Logic PCB identified as "LOGIC BD ASM 310071" is accomplished by appropriate setting of mini dip switches and is described in this technical note.

The dip switches are located as shown in Figure 1.

A10 SECTOR SELECTION SWITCHES 1 8 A7	UNIT ADDRESS SWITCH	TO BACK PANEL CONN.

DRIVE LOGIC PCB ASM NO. 310071

Figure 1

Sector selection switch settings for the more common sector lengths are shown in Figure 2. The determination of switch settings for other sector lengths is described in Section 2.

	7710 SECTOR SELECTION CHART								
Sectors Per Track	Bytes Per Sector (Unformatted)	Switch A7 S ₁ S ₂ S ₃ S ₄ S ₅ S ₆ S ₇ S ₈	Switch A10 S ₁ S ₂ S ₃ S ₄ S ₅ S ₆ S ₇ S ₈ S ₉ S ₁₀ S ₁₁ S ₁₂	Data Capacity - Formatted Format A Format B Data Bytes (MB)* (MB)* Per Sector					
9	1.200	0 0 0 1 0 0 0 0		9.68 1.024					
10	1,080	10010000	1 1 0 1 1 0 0 0 0 1 0 0	10.75 1.024					
12	900	1 1 0 1 0 0 0 0	1 0 0 0 0 0 1 1 1 0 0 0						
15	720	0 1 1 1 0 0 0 0	1 1 1 0 0 1 1 0 1 0 0 0						
18	600	10001000	1 1 0 1 0 1 0 0 1 0 0 0	9.68 9.68 512					
19	568	0 1 0 0 1 0 0 0	1 1 0 1 1 0 0 0 1 0 0 0	10.21 512					
20	540	1 1 0 0 1 0 0 0	101100001000						
30	360	10111000	1 1 0 0 1 1 0 1 0 0 0	8.06 256					
33	326	0 0 0 0 0 1 0 0	0 1 0 0 0 1 0 1 0 0 0 0	8.87 256					
36	300	1 1 0 0 0 1 0 0		9.68 256					
40	270	1 1 1 0 0 1 0 0	1 1 1 0 0 0 0 1 0 0 0						
54	200	10101100	101001100000	7.26 128					
60	180	1 1 0 1 1 1 0 0	100110100000	8.06 128					
64	168	1 1 1 1 1 0 0	1 1 0 0 1 0 1 0 0 0 0 0	8.60 128					

- NOTES: 1. Logical "O" = Switch is Off Logical "1" = Switch is On
 - 2. * Representative formats are desribed in Section 4.1 of the 7710 Disk Drive Product Specification.
 - 3. For Logic Board Assembly No. 310071

FIGURE 2

A-2

MEMORIES.



2. DETERMINATION OF SECTOR SELECTION SWITCH SETTINGS

This section describes the sector selection switch algorythim. Common switch settings are shown in Figure 2. This algorythim should be used if the sector sizes shown in Figure 2 are not of the required size.

Each track has a capacity of 10800 bytes. The formula is:

 $\frac{10800}{N} = \frac{I + R}{N}$

Where:

N = The number of sectors needed.

I = Is an even integer and is the number of bytes per sector.

R = The additional number of bytes in the last sector (N-1).

The switch referred to as A-7 sets the number of sectors per track. Switch A-10 sets the number of bytes per sector. The setting of each is calculated using the above formula.

In the following example the setting of both switches will be calculated using the above formula.

Example:

Switch A-10 counts PLO clocks thus as there are two PLO clocks to each byte of data the formula is:

$$(A-10)bin = (\frac{1}{2} - 1)dec.$$

So for 18 sectors the following would hold:

$$\frac{10800}{N} = \frac{I + R}{N}$$

Where:

N = 18 sectors per track I = 600 bytes per sector R = 0 (no remainder)

Thus, the setting for A-10 would be:

For N = 18

(A-7)bin = (N-1)dec. = (18-1)dec. = (17)dec.

Now convert 17 decimal to binary and set A-7 accordingly. The resulting setting would be:



SWI	sw2	sw3	sw4	sw5	swб	sw7	sw8				
O N	0 F F	0 F F	0 F F	O N	0 F F	0 F F	0 F F				
And	the s	ettin	g for	swit	ch A-	10 wa	buld b	e:			
For	I = 6	00									
(A-1	l0)bin	. = ($\frac{1}{2} - 1$)dec.	= (<u>6</u>	- 00	1)dec	. = (299)de	ec.	
			2			2					
Now	conve	rt 29	9 dec	imal	to bi	nary	and s	et A-	10 to	the f	ollowing
swl	sw2	sw3	sw4	sw5	swб	sw7	sw8	sw9	sw10	sw11	sw12
0	0	0	0	0	0	0	0	0	0	0	C
N	N	F	N	F	N	F	F	11	F	F	F
0 N	O N	0 F F	O N	0 F F	O N	0 F F	0 F F	0 N	0 F F	0 F F	G F F