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2-LINE AND 8-LINE COMMUNICATIONS MULTIPLEXORS

PROGRAMMING MANUAL

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PREFACE

This manual presents programming information for the 2-Line and 8-Line Communications Multiplexors (COMM MUX). The COMM MUX provides an interface between a multiplexor bus or selector channel and a variety of asynchronous data sets in either the 2-wire half duplex (HDX) or the 4-wire full duplex (FDX) mode. Chapter 1 provides a general description of the COMM MUX, configuration data, and a simplified block diagram. Chapter 2 provides data format information, programming instructions and operational considerations. The appendices contain sample programs for both 16-bit and 32-bit processors.

The following documents provide additional information for the COMM MUX user:

32-Bit Series Reference Manual, Publication Number 29-365

Model 7/32 User's Manual, Publication Number 29-405

Model 8/32 User's Manual, Publication Number 29-428

16-Bit Series Reference Manual, Publication Number 29-398

16-Bit Processor User's Manual, Publication Number 29-509

2-Line and 8-Line Communications Multiplexors Maintenance Manual, Publication Number 29-650

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CHAPTER 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

This manual contains a description of the Communications Multiplexor (COMM MUX) (Product Numbers M47-104 and M47-105) and the necessary information to program the system. The COMM MUX provides an interface between a multiplexor bus or selector channel and a variety of asynchronous data sets in either the 2-wire half-duplex (HDX) or the 4-wire full-duplex (FDX) mode. See Figure 1-1. Because of the wide variety of data sets and terminals available, the potential user must determine which COMM MUX is suitable for his given application and network. This manual assumes that the reader is familiar with the I/O structure of Interdata processors.

The communications multiplexor is available in two versions. The 2 line version is contained on a single 7-inch printed circuit board and the 8 line version is contained on a 15-inch printed circuit board. Each line has two consecutive addresses: an even address for the receive side and an odd address for the transmit side. If strapped for 2-wire mode, both sides respond to either address; however, it is standard practice to use the even address. An interrupt flip-flop is associated with each side. Each 2-wire or 4-wire line can be programmed to adapt the character format and baud rate to a wide variety of data sets and their associated terminals. See the 2-Line and 8-Line Communications Multiplexors Maintenance Manual, Publication Number 29-650, for strapping information.

1.2 CONFIGURATION

The COMM MUX is designed for use on any Interdata 16 bit or 32 bit processor. Since the COMM MUX board is treated as simply another device controller, no special chassis are needed. Any number of boards may be used up to the maximum address capability.

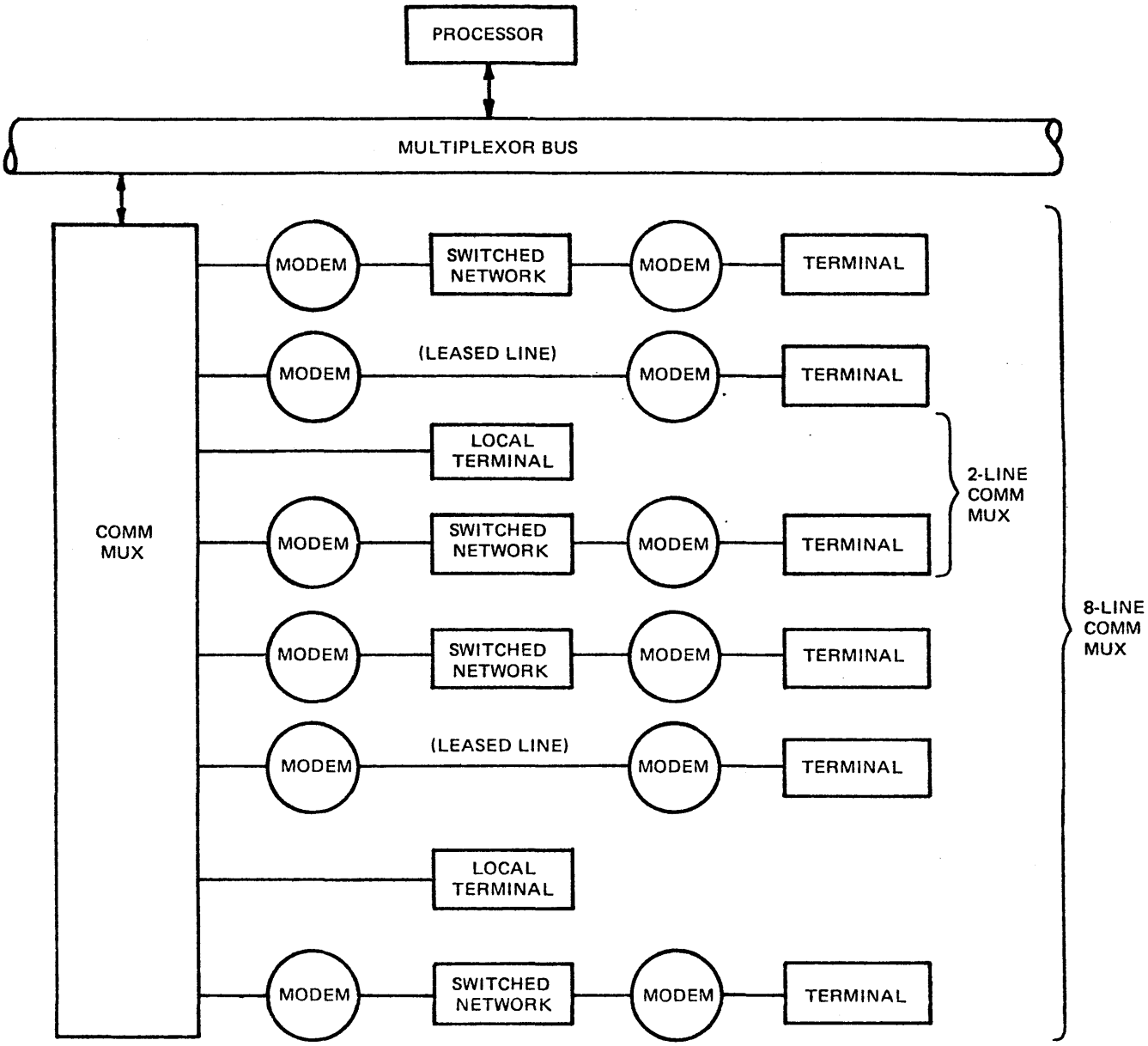


Figure 1-1 COMM MUX Block Diagram

CHAPTER 2
COMMUNICATIONS MULTIPLEXOR PROGRAMMING

2.1 DATA FORMAT

The fixed, optional, and programmable features of the 2-line and 8-line COMM MUX boards are described in the following sections.

2.1.1 Specifications

The following is a list of COMM MUX specifications:

- Baud Rates - The following groups of baud rates are provided:

  Group 1: 50, 110, 1,800, 2,400
  Group 2: 75, 134.5, 2,000, 3,600
  Group 3: 150, 600, 4,800, 9,600
  Group 4: 300, 1,200, 7,200, 19,200

  Group selection is a strappable option as described in the COMM MUX Maintenance Manual, Publication Number 29-650. Within a group, baud rate selection is under program control.

- Maximum number of lines -2 lines or 8 lines per COMM MUX; any combination of 2-wire/ 4-wire.

- Character format - The following three independent variables on the character format are programmable:

  Character size - 5, 6, 7, or 8 data bits.
  Parity - Odd, even, or none.
  Stop bits - One or two.

- RS-232C Interface

VOLTAGE	BINARY	SINGLE LINE	CONTROL
+5V TO +15V	0	SPACE	ON
-5V TO -15V	1	MARK	OFF

- Data Set Control (Programmable)

  a. Data terminal ready (CD) - Program control is provided over CD to allow for automatic call reception, disconnect, and lockout.

NOTE

Parentheses indicate RS-232C designations for indicated functions.

  b. Reverse channel transmit (SA)* - Permits a supervisory signal to be transmitted over a secondary data path while simultaneously receiving data.

  c. Request to send (CA) - Active to maintain the COMM MUX in the transmit mode. In 2-wire operation, the inactive state maintains the COMM MUX in the receive mode.

  d. Data terminal busy* - Enables the make busy feature when available.

- Data set status - The following lines from the data set affect the status bits: CLEAR TO SEND (CB), CARRIER (CF), RING (CE), REVERSE CHANNEL RECEIVE (SB), and DATA SET READY (CC).

- Echoplex - A programmable feature for transmitting received data back to the data set in addition to assembling the character.

- Other features - The COMM MUX provides a double-buffered character to permit a full character "grab time." The hardware automatically generates and transmits the start bit in the Receive mode, and it must be present for at least one-half a bit time before the character assembly commences to reduce the noise susceptibility of the system.

- Method of transmission - Serial, asynchronous by character, synchronous by bit.

- Distortion:

  Transmit - The transmit data distortion is +3% per character.

  Receive - The COMM MUX adjusts the data sampling strobe with each character received and tolerates a data bit distortion of +43%. In addition, the long term transmission rate may vary by +5%.

*Optional features in some data sets.

2.1.2 Transfer Format

Asynchronous operation requires all characters to be preceded by one start bit (=0) and have at least one stop bit (=1) appended after the last data bit or the parity bit, if selected. The start and stop bits delineate characters. A typical format for the Teletypewriter (110 Baud) is shown in Figure 2-1.

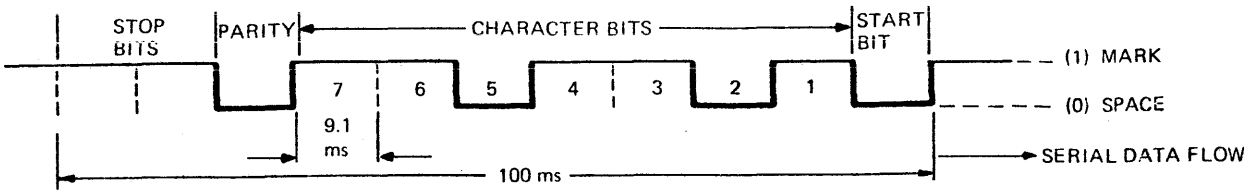


Figure 2-1 Typical ASCII Character Format

NOTE

To send 7 useful bits of information, 11 code elements (bits) are required. Therefore, to send 70 bits of useful information per second, the system must operate at 110 baud.

The hardware generates the single start bit and the character size/parity and number of stop bits are under program control.

2.1.3 Order of Transmission

Figure 2-2 shows the order of transmission to and from the communication line.

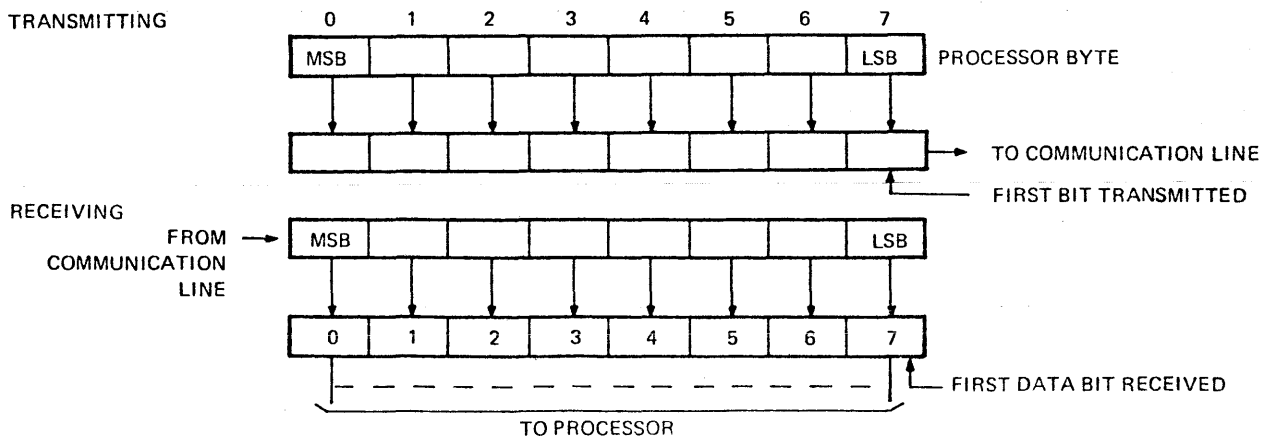


Figure 2-2 Order of Transmission for Transmitting/Receiving

NOTE

Some terminals require the MSB to be transmitted (or received) first. For such terminals, the program should present the data with the MSB of the data in position 7 of the byte; this may be performed through the translation option of the auto-driver channel on 32-bit processors.

2.2 PROGRAMMING INSTRUCTIONS

The COMM MUX continually multiplexes signals being transferred across up to 8 separate lines. Each line requires its own individual separate format characteristics while in use. Processor line drivers must be programmed differently for each type of line use. The drivers incorporate processor I/O instructions to communicate with the COMM MUX and to affect appropriate COMM MUX register changes as required for each line type. The following paragraphs describe the instructions.

2.2.1 COMM MUX Program Instructions

Sense Status (SS or SSR)

The Sense Status instruction is used to determine if character transfers are complete and correct, and to interrogate the associated data set status.

Output Command (OC or OCR)

The Output Command instruction is used to answer or disconnect calls, to set the COMM MUX in the receive or transmit mode, and to select the character format. Two command bytes are required to perform these functions.

Write Data (WD or WDR)

The Write Data instruction is used to load the output character into the COMM MUX Data Register.

Read Data (RD or RDR)

The Read Data instruction is used to read an assembled character into the processor.

Acknowledge Interrupt (AI or AIR)

The Acknowledge Interrupt instruction is used to service interrupts. Execution of this instruction returns the address and status of an interrupting line. This instruction is used only for the 16-Bit Processors.

2.2.2 Communication Instructions

The COMM MUX accommodates the communication instructions in the communication processors (Models 50, 55, 60).

2.2.3 Auto Driver Channel (ADC)

The COMM MUX may be used with ADC on the 32-bit processors.

2.2.4 Status and Command Bytes

Table 2-1 contains the COMM MUX Status and Command Byte Data.

TABLE 2-1 COMM MUX STATUS AND COMMAND BYTE DATA

BIT NUMBER / INSTRUCTION		8	9	10	11.	12	13	14	15
COMM MUX STATUS		OV	PF or CL2S	FR ERR	RCR	BSY	EX	CARR OFF	RING
COMM MUX COMMAND 1	RCV	DIS	EN	DTR	ECHO-PLEX	RCT or DTB	TRANS LB	WRT or RD	1
	SND	DIS	EN						
COMM MUX COMMAND 2		CLKB	CLKA	BIT SEL		STOP BIT	PARITY		0

2.2.4.1 COMM MUX Status Instruction Bits

Refer to Figure 2-3 for COMM MUX - Data Set Communication lines.

OV* The overflow status bit is set to ONE if the previously received character is not read before the present character is assembled. Double-character buffering in the COMM MUX permits a full-character "grab-time". The overflow status bit can be ONE in the receive side only. It is reset at the next end of character, only if the failure condition disappears (i.e., is cleared by a read data instruction). The character causing overflow is assembled and the previous character is lost.

PF* In the read mode, this bit is ONE when the received parity disagrees with the programmed parity. If parity is not selected via an output command, this bit remains ZERO. Once set, the PF status bit remains set until the failure condition disappears (i.e., a character with correct parity is assembled).

CL2S The lack of clear to send signifies that the modem can no longer transmit data. In the write mode, this status bit set indicates that clear to send (CB) is not being received from the data set. See Figure 2-3. This condition also forces BSY=1 on the transmit side. A transition from CL2S=0 to CL2S=1 causes an interrupt if enabled.

FR ERR* The framing error status bit is set to ONE to indicate that the received character has no stop bit(s). That is, the line is in the space state instead of the mark state at stop bit time. If the character has two stop bits, only the first is tested, and the character assembly terminates after the first stop bit. If a framing error occurs, the character is assembled. A ZERO character can signify the beginning of a line break sequence. In the case of a line break (prolonged SPACE), if the line remains spacing, only the first character is assembled. Subsequent SPACE characters are not assembled until a MARK to SPACE transition is received. Note that because of this characteristic where the line break facility is being employed, a line break decision must be based on a single ZERO character with framing error. Once set, this bit remains set until the assembly of a character with a stop bit.

RCR REVERSE CHANNEL RECEIVE (SB) is an option in some 2-wire data sets (e.g., 202C). This status bit is set if the reverse channel line from data set is ON. This bit is reset if the reverse channel line from data set is OFF. If the data set does not have the reverse channel option, this status bit is always inactive. Either transition of this signal causes an interrupt, if enabled.

* These status bits are set at end of character time when the busy bit is ZERO. Since resetting busy causes an interrupt (if enabled), these bits do not generate individual interrupts. At this point, a read data instruction must be issued to set the busy bit.

BSY — If the busy status bit is set, the following occurs:

1. Data set ready (CC) from the data set is OFF (EX=1).
2. Character is not assembled in read mode.
3. Clear to send (CB) is OFF (CL2S=1) in write mode.
4. When the interface has not yet transmitted, the last character is in the write mode.

If the busy status bit is reset, the interface can transfer data in the read/write mode. An interrupt is generated, if enabled, when the busy status bit changes from a ONE to a ZERO. When an overflow occurs in the read mode, the busy status bit is reset to ZERO and a read data instruction must be issued to set the busy bit to its correct (ONE) state.

EX — Examine=OV+PF+DATA SET READY + FRERR. This bit is disabled in FDX on the write side. Loss of DATA SET READY (CC) cannot be detected on the write side in FDX operation. On the receive side, DATA SET READY is indicated by busy and examine being ONE.

CARR OFF — CARR OFF is ONE to indicate that no valid incoming data is being received. In the receive side, this bit is ONE to indicate that CARRIER (CF) is not being received from the data set (see Figure 2-3). In the write mode, this status bit is ZERO when REQUEST TO SEND (CA) is active. If enabled, a transition of this status bit in either direction causes an interrupt.

RING — RING is ONE when the RING (CE) signal from the data set is active. This indicates the receiving of a call. An interrupt is generated, if enabled, when RING changes to ONE. In 4-wire operation, RING is always ZERO on the transmit (send) side. The ring status represents the present state of the equivalent data set signal. See Figure 2-3.

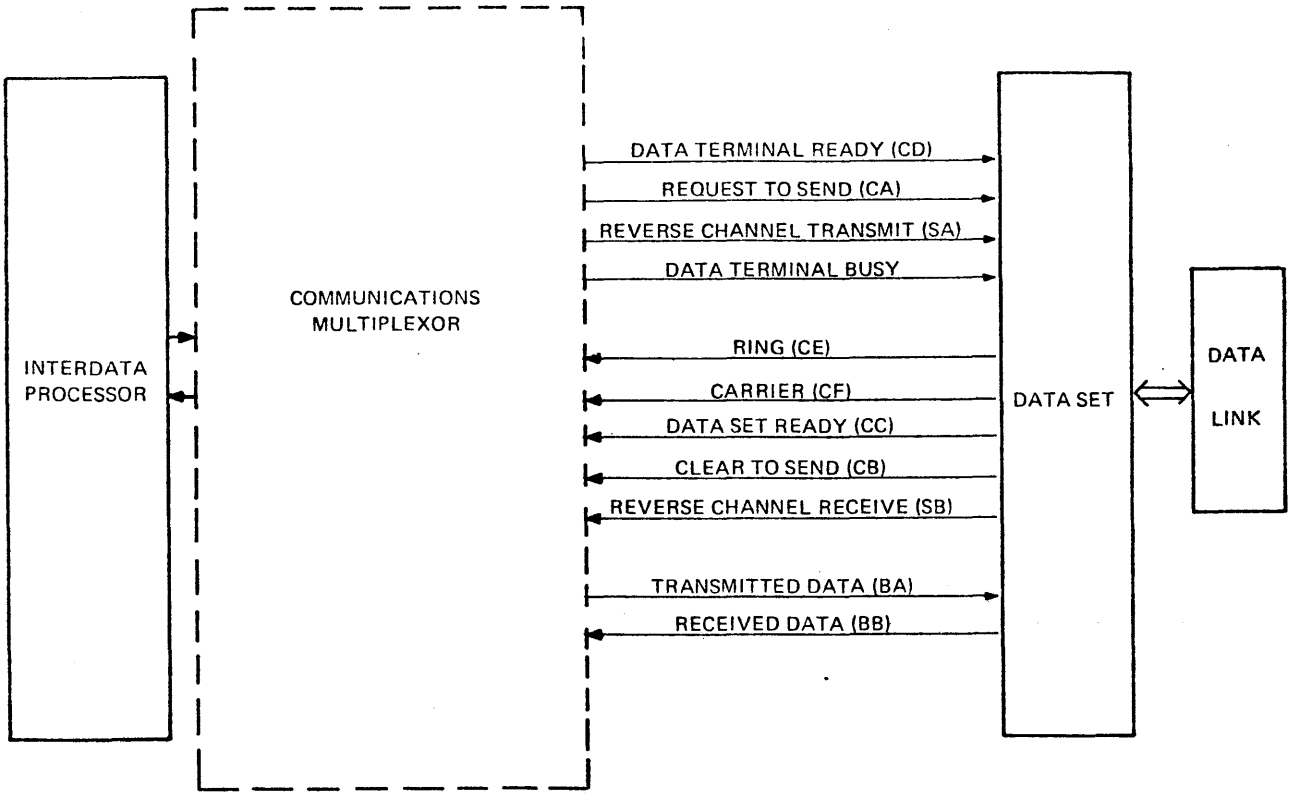


Figure 2-3 Comm Mux Data Set Communication Lines

2.2.4.2 COMM MUX Command 1 Instructions Bits

The COMM MUX needs two 1-byte output command instructions, Command 1 and Command 2. The Command 1 instruction byte sets up the interrupt conditions and the modem controls. In the Command 1 instruction, the DTR, ECHOPLEX, RCT/DTB, TRANS LB, and WRT/RD bits are shared by the transmitter and receiver. The EN/DIS bits, however, are separate for transmit and receive sides. The Command 1 instruction bits are as follows:

DIS,EN If the disable bit is reset and the enable bit is set, interrupts are enabled. Interrupts are queued if the disable bit is set and the enable bit is reset. If both the disable bit and the enable bit are set, interrupts are disarmed (no interrupts are queued); but, if both are reset, no change occurs.

In 2-wire operation, the unused side interrupts remain disarmed. The used side interrupts can be enabled or disabled. In 4-wire operation, these bits must be independently programmed as follows.

- To change EN/DIS on the receive side, issue a command with the WRT/RD bit = 0.

- To change EN/DIS on the transmit side, issue a command with the WRT/RD bit = 1.

- The WRT/RD bit is gated to the data set as REQUEST TO SEND. Therefore, in 4-wire operation, a command with WRT/RD = 0 must be followed with a command WRT/RD = 1 to ensure that REQUEST TO SEND does not deactivate.

DTR — DATA TERMINAL READY (CD) to the data set. When this command bit is set, CD is turned ON, allowing answering an incoming call automatically. This line must be ON to permit the data set to enter and remain in the data mode. When this bit is reset, it does not permit automatic answering of an incoming call and causes an existing connection to disconnect if held reset for a period specified by the manufacturer of the data set. See Figure 2-3.

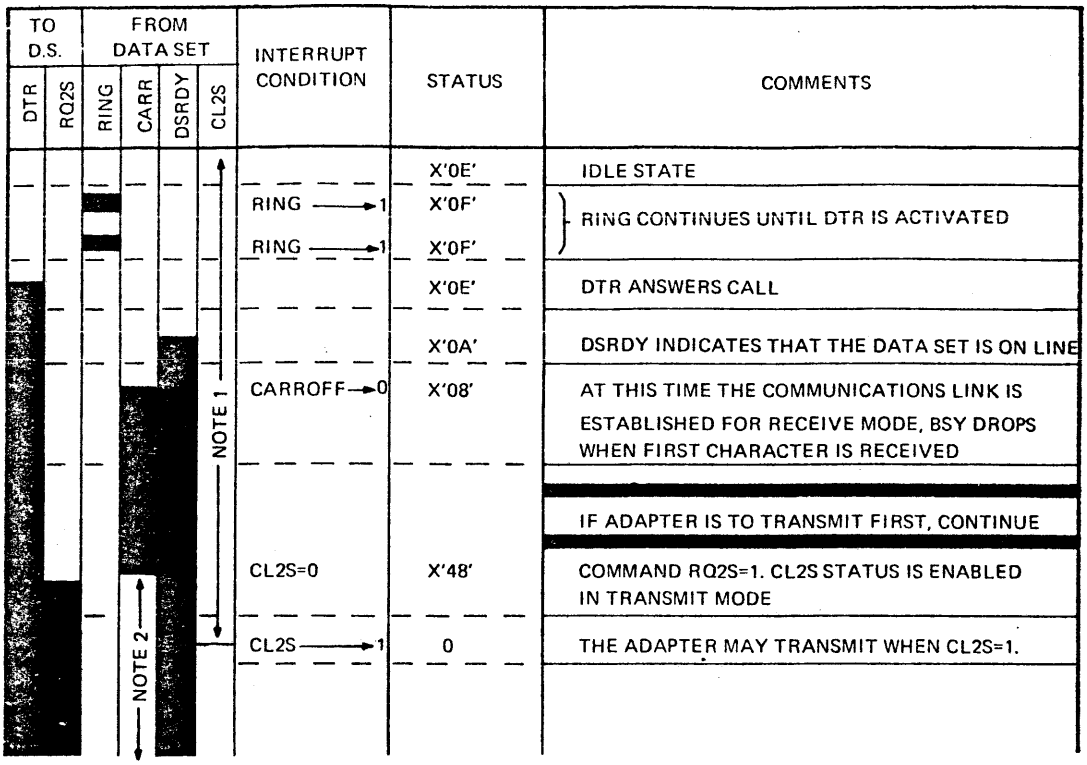
ECHO-PLEX — When this bit is set, data received from the data set is transmitted back to the data set on the TRANSMITTED DATA (BA) line. See Figure 2-3. The COMM MUX also assembles the character as in the normal data mode. This feature is normally used for 4-wire FDX operation in the read mode to provide visual verification at the terminal of the data received by the computer. This command must not be issued to the transmit side. In the 2-wire HDX read mode, the RQ2S line is not active. If the associated data set requires RQ2S to be active, the data does not pass to the communication link. This bit takes effect immediately. Therefore, a write to read (with echo-plex) mode change requires transmitting X'FF' (an ASCII DEL character) as the last character.

RCT/DTB — Reverse Channel Transmit (RCT) (SA) is optional on 202C-type data sets. Data Terminal Busy (DTB) is optional on 103-type data sets. See Figure 2-3. For reverse channel transmit option, this command bit is gated directly to the secondary transmitted data (SA) line. See Figure 2-3. When this bit is set, RCT is OFF, i.e. reverse channel is not transmitted. When this bit is reset, RCT is ON, i.e. reverse channel is transmitted. For data sets equipped with the data terminal busy option, the reset condition of this command bit will "busy-out" the terminal; thus, not allowing a call to be answered and returning the busy signal to the calling terminal.

TRANS LB — When this bit is set, a continuous SPACE is transmitted to the data set. This condition overrides the echo-plex feature. If this command is issued while data is being transmitted, the transmitted data is mutilated.

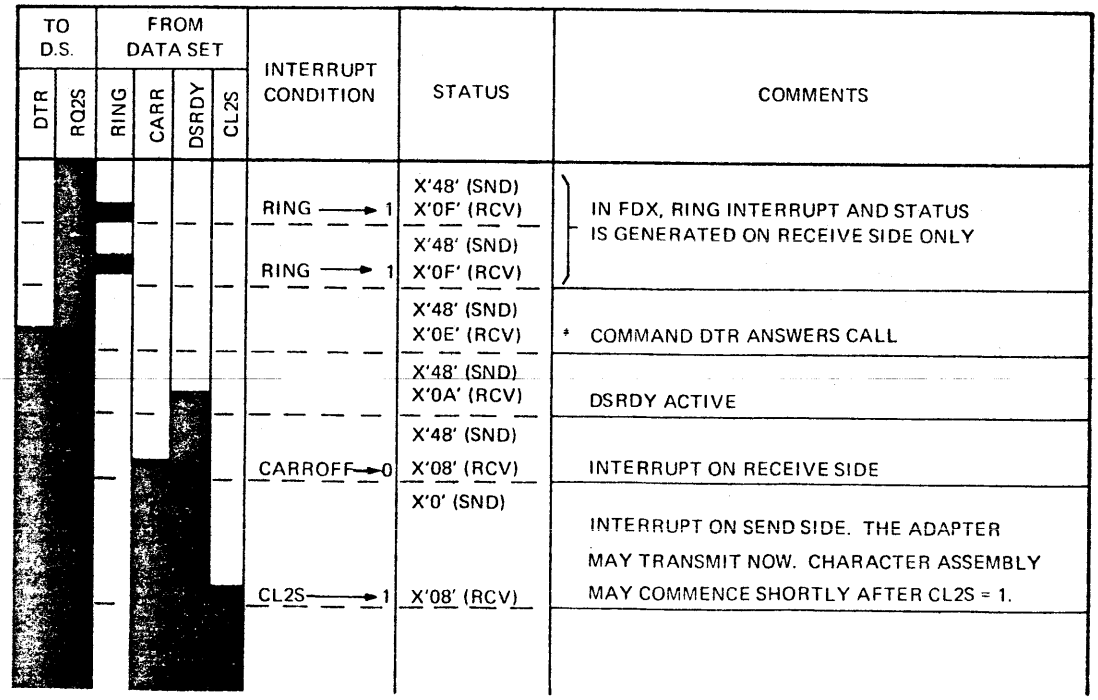
WRT/RD This command bit controls REQUEST TO SEND (CA) to the data set. See Figure 2-3. When this bit is set, REQUEST TO SEND is gated to the data set if DATA SET READY* (CC) is active. When this bit is reset, the hardware deactivates REQUEST TO SEND (CA) after the following delays: If character transfers are in progress, the hardware ensures that the last character has been transmitted, then delays one millisecond to permit the last data bit to clear the data set before dropping REQUEST TO SEND (CA) except as noted under ECHO-PLEX. BSY is set during this line turn-around and does not reset until a character is received. However, $\overline{\text{CL2S}}$, CARR OFF, RING, RCR, and DSRDY may still generate interrupts, if enabled. See Figures 2-4 and 2-5. In 2-wire operation, setting this bit places COMM MUX in the Write mode; resetting this bit places COMM MUX in the Read mode. In 4-wire operation, this bit is normally programmed set except noted under DIS, EN above.

*DATA SET READY (CC) does not appear in the status byte on the Transmit side in FDX operation. It should be noted here that one must rely on the receive side of the adaptor for notification of the loss of Data Set Ready (CC). Loss of Data Set Ready on the transmit side in FDX operation does not cause an interrupt. It does, however, hold Busy high thus preventing any more end of character interrupts.



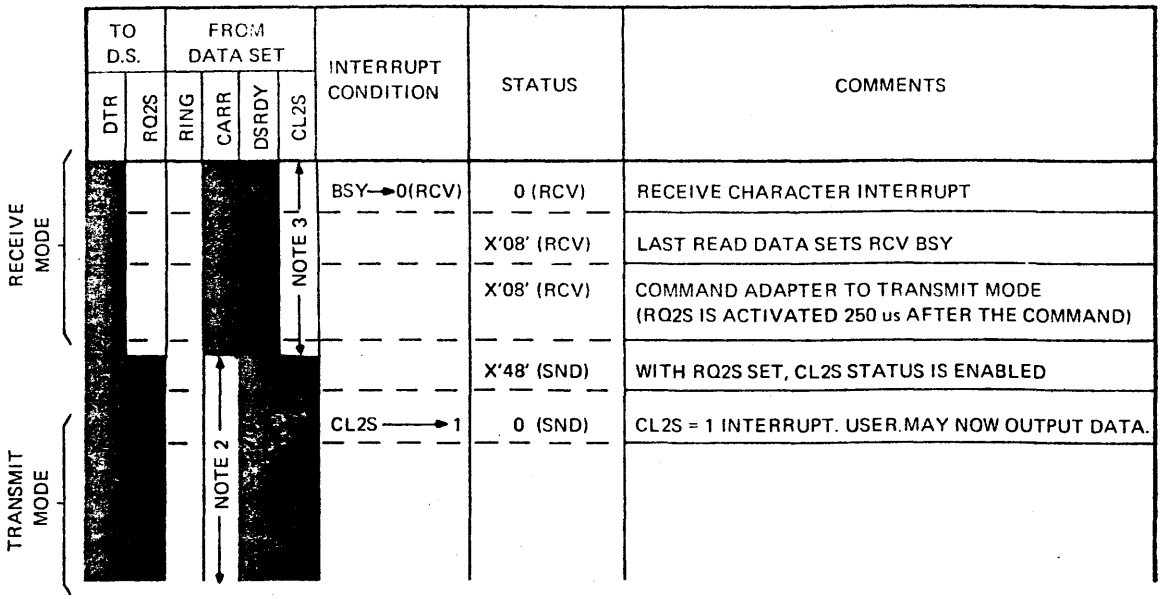
NOTE 1: CL2S IS DE-ACTIVATED WHEN RQ2S = 0
NOTE 2: CARR IS DE-ACTIVATED WHEN RQ2S = 1 (CARR OFF = 0)
NOTE 3: THE STATUS SHOWN ONLY REFLECTS THE LINE CONDITIONS, NOT PF, OV, OR FR ERR. IN ADDITION REVERSE CHANNEL IS IGNORED SINCE THIS IS SUBJECT TO USER'S PROTOCOL.
NOTE 4: IF DTR IS SET WHEN RING OCCURS, THE CALL WILL BE ANSWERED AUTOMATICALLY (RING TERMINATES AND DSRDY BECOMES ACTIVE).

Figure 2-4A Answering Calls HDX, 2-Wire Mode (202-Type Data Set)



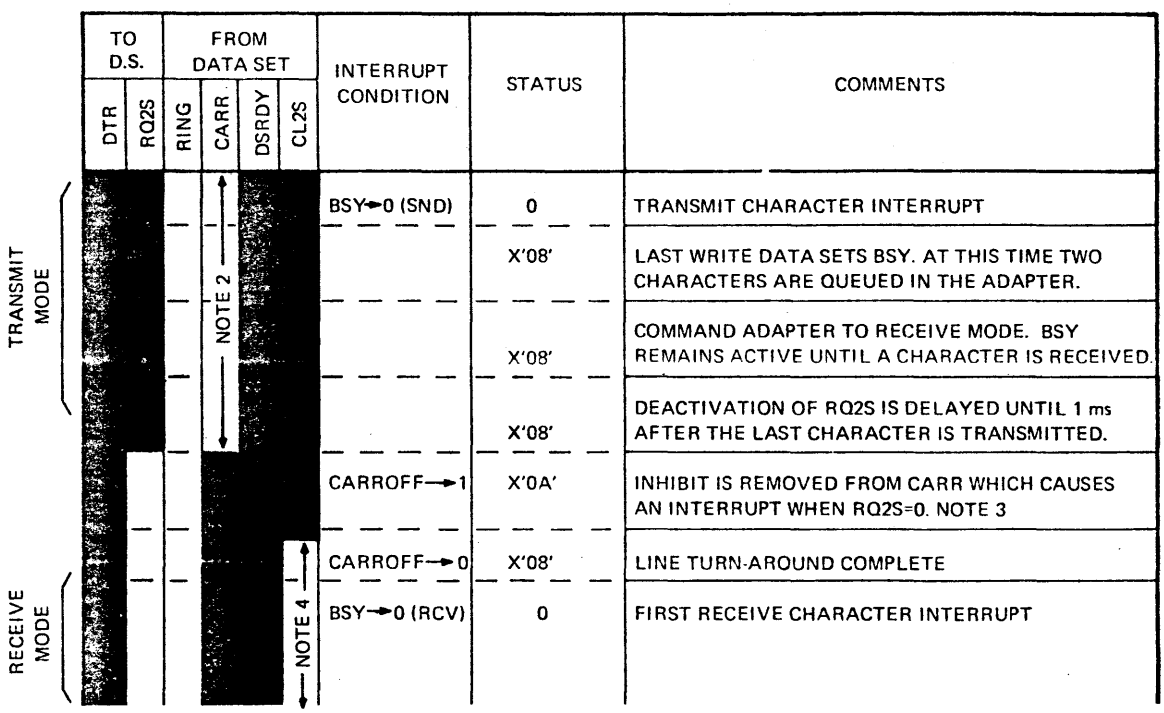
NOTE 1: CARR OFF AND DSRDY FORCED LOW ON TRANSMIT SIDE.
NOTE 2: REVERSE CHANNEL NOT APPLICABLE IN FDX (RCR = 0)

Figure 2-4B Answering Calls FDX, 4-Wire Mode (103-Type Data Set)



NOTE 1: INITIAL CONDITIONS; CONNECTION ESTABLISHED AND ADAPTER IS RECEIVING CHARACTERS.
NOTE 2: CARR OFF STATUS FORCED INACTIVE AND CARRIER INTERRUPTS INHIBITED.
NOTE 3: CL2S STATUS FORCED INACTIVE AND CL2S INTERRUPTS INHIBITED.

Figure 2-5A Line Turn-Around Write/Read (202-Type Data Set)



NOTE 1: INITIAL CONDITIONS: CONNECTION IS ESTABLISHED AND ADAPTER IS TRANSMITTING CHARACTERS.
NOTE 2: CARR OFF STATUS FORCED INACTIVE AND CARRIER INTERRUPTS INHIBITED.
NOTE 3: WITH A 103 TYPE DATA SET, CARRIER MAY BE PRESENT CONTINUOUSLY IN WHICH CASE THE CARROFF 1 INTERRUPT WILL NOT OCCUR AFTER DEACTIVATING RQ2S.
NOTE 4: CL2S STATUS FORCED INACTIVE AND CL2S INTERRUPTS INHIBITED.

Figure 2-5B Line Turn-Around Read/Write (202-Type Data Set)

2.2.4.3 COMM MUX Command 2 Instruction Bits

The Command 2 instruction byte sets up the Universal Asynchronous Receiver/Transmitter (UART) and the Baud Rate Generator within the COMM MUX. The Command 2 instruction bits are as follows:

CLKB, CLKA — Without strapping, each COMM MUX normally is set to allow for the Group 4 baud rates as shown below. As described in the COMM MUX Maintenance Manual, Publication Number 29-650, any one of groups 1, 2, and 3 may optionally be chosen instead by proper strapping during installation. The CLK bits (CLKB and CLKA) within the Command 2 instruction select one of the four baud rates within the installed group as follows:

STRAP OPTION	CLK BITS		BAUD RATE
	CLKB (Bit 8)	CLKA (Bit 9)	
	0	0	50
	0	1	110
	1	0	1,800
Group 1	1	1	2,400
	0	0	75
	0	1	134.5
	1	0	2,000
Group 2	1	1	3,600
	0	0	150
	0	1	600
	1	0	4,800
Group 3	1	1	9,600
	0	0	300
	0	1	1,200
	1	0	7,200
Group 4	1	1	19,200

BIT SELECT — These bits select the number of data bits/character (not including parity).

BIT		NUMBER OF DATA BITS
10	11	
0	1	5
0	1	6
1	0	7
1	1	8

If fewer than eight data bits are selected when a write data is issued in the write mode, the data must be right-justified and unused bits are "Don't Care." In the read mode, when a read data is issued, the character is presented to the processor right-justified with unused bits forced to the ZERO state.

STOP BIT 0=1 Stop Bit
1=2 Stop Bits

When the line is programmed for two stop bits, the COMM MUX transmits both. However, the receiver only samples the first stop bit.

PARITY These bits select odd, even, or no parity.

BIT		PARITY
13	14	
1	0	ODD
1	1	EVEN
0	X	NONE

In the write mode, if parity is enabled (Bit 13=1), the COMM MUX generates and transmits the selected parity.

In the read mode, if parity is enabled, the COMM MUX compares the received parity with the selected parity and generates the PF status if a disagreement is detected.

If parity is disabled (Bit 13=0), the hardware ignores parity. When transmitting, the hardware appends stop bit(s) after the last data bit and, when receiving, disables the parity detection circuit.

NOTE

The least significant bit (Bit 15) of the command byte must be a 1 or 0 as indicated to permit the hardware to distinguish between the two commands. Command 2 should never be issued while data transfer is in progress.

2.3 OPERATIONS

COMM MUX programmers must consider the programming sequences for specific line types, interrupt control logic, initialization procedure, and device numbers.

2.3.1 Programming Sequences

The following paragraphs illustrate switched line, leased line, and half-duplex operation.

2.3.1.1 Switched Line Operation

To originate a call, the operator depresses the TALK key on the data set and dials the desired number. When the call is answered, a carrier is heard (being sent by the data set receiving the call). The operator then depresses the DATA key.

The operator can now hang up and depress the AUTO key to return the equipment to automatic receive following this call. When the DATA key is depressed (the data light remains lit for the duration of the call), the EX status bit resets (DATA SET READY) (CC) as does the CARR OFF status bit. The EX status bit does not reset if the last state was an overflow, framing error, or parity error. The COMM MUX should be initialized to the read mode and thus be interrupted by the receiving carrier. When CARR OFF resets, the COMM MUX should be switched to the write mode to transmit data. Following the call, both sets (originating and receiving) should be issued a command read with DTR reset to disconnect. This procedure is typical, but not necessary. The user can design his own hand-shaking sequence. Figures 2-4 and 2-5 show timing sequences for answering calls and line turnaround. The following is offered for general information only. With wide variations between data set characteristics and common carrier procedures, the operating procedures may have to be modified. The user should ensure that the characteristics of the devices connected to the COMM MUX are compatible with the descriptions in this specification.

In Figure 2-4A, DTR and RQ2S are initially OFF. The status is X'0E' before RINGing commences. The RING causes an interrupt and a status of X'0F'. The RING status bit is set for the period of the RING from the data set.

When RING resets, the status is X'0E' and another interrupt is generated each time RING $\longrightarrow$ 1. RING continues until the program sets DTR to answer the call. Shortly after DTR is set, the data set responds with DSRDY=1), causing EX $\longrightarrow$ 0. The status at this time is X'0A' (BSY=1 and CARR OFF=1).

When the data link is established, the data set turns CARR ON thus generating an interrupt and a status of X'08' (BSY=1). If the adapter remains in the receive mode, busy stays active until a character is received. If the adapter is to transmit first, the program turns RQ2S ON (command with the WRT bit set). With RQ2S ON, the data set responds with $\overline{\text{CL2S}}$=1. Since this bit is initially reset, an interrupt is generated when RQ2S is turned ON and another interrupt is generated when the data set responds with $\overline{\text{CL2S}}$=1. The adapter may now transmit.

Figures 2-4 and 2-5 assume ideal conditions. For example, in a typical switched network environment, more than one interrupt may be generated as carrier is initially established, or the received data from the local data set may be active during a connect or disconnect sequence. These problems can be attributed to the type (manufacturer) of data set used, the options implemented in the data set and the switched network. In particular, if the received data from the data set is active before carrier is established, the COMM MUX commences to assemble a "garbled" character. This can result in a receive busy interrupt with any or all of the character status bits set (PF, FRERR, OV). These status bits will then remain set until a read data is executed (to set BSY and reset OV) and a valid character is received (to reset PF and FRERR).

2.3.1.2 Leased Line Operation

Because a connection is permanently established in leased line operation, no dial-up or disconnect is needed. Both stations are normally initialized to the read mode. Either end can originate a transfer by going into the write mode, which causes the receiving station to interrupt when the carrier appears. Upon receiving characters, the receiving end is in the read mode and a data transfer takes place. The exact hand-shaking protocol is up to the user.

2.3.1.3 Half-Duplex Operation

In half-duplex operation, only one terminal can transmit at any one time. To change the direction of transmission, the channel must be turned around. The question arises as to who indicates channel turn-around. The convention is normally held that the processor turns the line around when it has a message to transmit. Data sets (e.g. 202C type) normally used in half-duplex operation, may be equipped with the reverse channel option which is used to signal the requirement to reverse the direction of transmission or to break the data flow. An important operating convention affecting reverse channel operation results from the presence of echo suppressors in long-distance lines. These suppressors normally disallow transmission of an echo.

In data communications, the echo suppressor must be disabled, as it must be possible to transmit simultaneously in both directions (main channel and reverse channel). The echo suppressor becomes re-enabled if the tone on the line is absent for a period exceeding 100 milliseconds. To prevent the re-enabling of the echo suppressor, the convention should be adopted that the reverse channel is held ON (high) when the main channel is OFF and vice versa. This convention ensures that a tone is on the line at all times.

The reverse channel is normally held ON when the processor is accepting data. The processor signals its desire to transmit by lowering (OFF) the reverse channel and switching to the write mode. A program delay should normally be introduced to allow the terminal on the other end to turn its reverse channel ON and enable its read mode. This delay is a function of the terminal on the other end. This delay can be 200 to 1200 milliseconds. If the device at the other end is set up to indicate through the reverse channel signaling that it is ready to receive data, this can be used instead of a program delay. When the processor is transmitting, a break condition sent from the terminal to signify that the terminal wants to transmit is signified by the receive reverse channel going from ON (high) to OFF (low). The processor should then raise its reverse channel lead high (ON) and transfer to the read mode. The interface automatically introduces the necessary time delay before presenting data to the processor to ensure valid data transfer and not transition noise.

2.3.2 Interrupts

The COMM MUX has interrupt control logic that scans all interrupt sources in the system. This logic has the following characteristics (see Table 2-2 for interrupt conditions):

- If an interrupt is detected, the hardware assigns priority to the line with the lowest address. In 4-wire operation, this is always the receive side.
- When an interrupt is detected on the transmit or receive side of a given line in 2-wire operation, the address of the receive side (even) is always returned.
- In 2-wire operation, the side not being used has interrupts disarmed (not queued).
- If an interrupt is present on an enabled line, it can become queued in the interrupt scanner even if the interrupt is disabled before it is serviced. This condition can result in an interrupt from a disabled line. Servicing this interrupt clears the attention flip-flop on this line while disabled. Software is designed to ignore any interrupt from the device once it is disabled.

TABLE 2-2 INTERRUPT CONDITIONS

INTERRUPT CONDITION	HDX	FDX	
		REC	TRANS
RING ——→ 1	X	X	
CARR OFF ——→ 1	X(RD)	X	
CARR OFF ——→ 0	X(RD)	X	
RCR ——→ 1	X	X	
RCR ——→ 0	X	X	
DSRDY ——→ 0	X	X	
*BSY ——→ 0	X	X	X
$\overline{CL2S}$ ——→ 1	X(WRT)		X

* An interrupt is also generated in 2-wire operation when going from READ to WRITE mode if $\overline{CL2S}$ initially equals a 0, i.e., $\overline{CL2S}$ going from a ZERO to a ONE causes a BSY interrupt.

2.3.3 Initialization

When the initialize pushbutton on the display panel is depressed (or power failure restart sequence), the OV, PF, and FR ERR status bits cannot be guaranteed. Because of this, the programmer should ignore these bits on the first interrupt. The COMM MUX should be issued an output command to disable interrupts. Because an interrupt line may be active upon initialize or power up, execute a number of interrupt acknowledge instructions at that time. Also, a read data should be issued to all receivers to ensure that the busy bit equals a ONE.

The command bits DTR, ECHOPLEX, RCT, TRANS LB and WRT/RD are reset to their inactive state.

2.3.4 Device Number

The COMM MUX has contiguous addressing with the lowest address X'10'. This is a switch option. Two consecutive addresses are assigned to each 4-wire line, with the even address for the receive side and the odd address for the transmit side. In 2-wire operation, each side responds to either address. In 4-wire operation, only one Command 2 is required. Command 2 should never be issued while a character transfer is in progress because it may mutilate the character (transmit or receive).

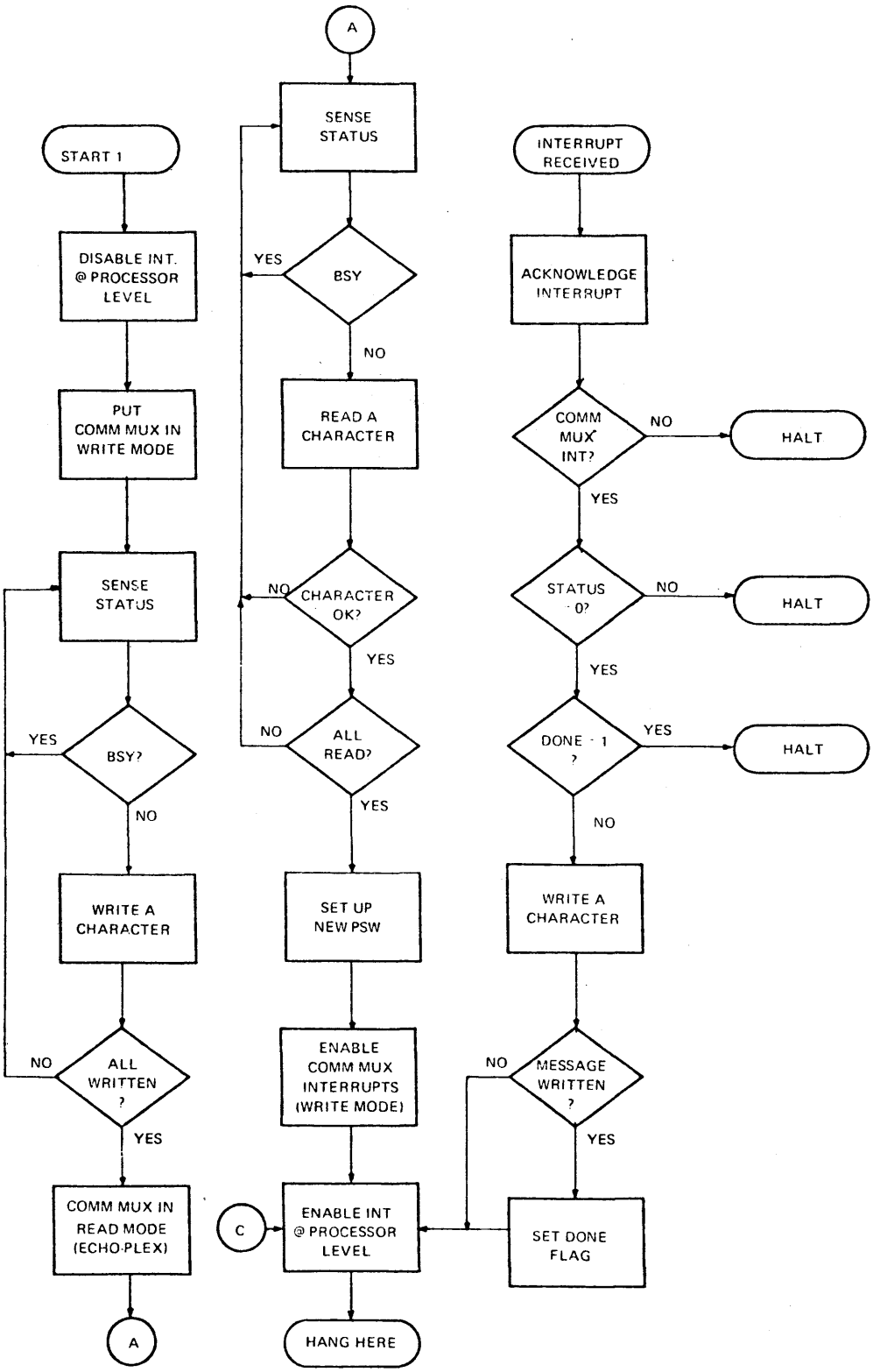
2.3.5 Sample Programs

Appendix A and Appendix B contain sample flow charts and program listings for 16-bit and 32-bit processors, respectively.

APPENDIX A
SAMPLE PROGRAM FOR 16-BIT PROCESSORS

Local Terminal Half-Duplex COMM MUX Operation

The following flow chart and program listing is for local terminal, half-duplex COMM MUX operation. The example specifies 2-wire mode with data transfer to a specified output device using sense status loops and interrupts. The message 'TYPE 1234567890' is output using a sense status loop. The COMM MUX is put into the read mode with echo-plex enabled. A user input 10-character message is read using a sense status loop. When the complete message is received, the COMM MUX is put in the write mode with interrupts enabled, and the message 'CORRECT!' is output under interrupts. The last write interrupt is cleared.


START 1
DISABLE INT. @ PROCESSOR LEVEL
PUT COMM MUX IN WRITE MODE
SENSE STATUS
BSY?
YES
NO
WRITE A CHARACTER
ALL WRITTEN ?
NO
YES
COMM MUX IN READ MODE (ECHO-PLEX)
A
A
SENSE STATUS
BSY
YES
NO
READ A CHARACTER
CHARACTER OK?
NO
YES
ALL READ?
NO
YES
SET UP NEW PSW
ENABLE COMM MUX INTERRUPTS (WRITE MODE)
C
ENABLE INT @ PROCESSOR LEVEL
HANG HERE
INTERRUPT RECEIVED
ACKNOWLEDGE INTERRUPT
COMM MUX INT?
NO
HALT
YES
STATUS 0?
NO
HALT
YES
DONE - 1 ?
YES
HALT
NO
WRITE A CHARACTER
MESSAGE WRITTEN ?
NO
YES
SET DONE FLAG

```
      COMM MUX PROGRAMMING EXAMPLES FOR 16- BIT PROCESSOR       PAGE   1  16:49:09  07/12/78

PROG= *NONE-     ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

                                  1           PROG  COMM MUX PROGRAMMING EXAMPLES FOR 16- BIT PROCESSOR        CM160010
                                  2           CROSS                                                            CM160020
                                  3           TARGT 16                                                         CM160030
                                  4           WIDTH 120                                                        CM160040
                                  5  *                                                                         CM160050
                                  6  * THESE EXAMPLES DEMONSTRATE SEQUENCES TO PROGRAM THE                    CM160060
                                  7  * COMMUNICATIONS MUX IN VARIOUS ENVIRONMENTS. THE TERMINAL AND           CM160070
                                  8  * THE  COMM MUX INTERFACE SHOULD BE STRAPPED/CONNECTED                   CM160080
                                  9  * AS MENTIONED IN THE INDIVIDUAL EXAMPLES.                               CM160090
                                 10  *                                                                         CM160100
                                 11  * REGISTER ASSIGNMENTS                                                   CM160110
                                 12  *                                                                         CM160120
0000 0001                        13  MSG       EQU   1              MESSAGE START ADDRESS                     CM160130
0000 0004                        14  CHAR      EQU   4              CHARACTER BEING TRANSFERRED               CM160140
0000 0005                        15  WORK      EQU   5              WORK REGISTER                             CM160150
0000 0006                        16  DONE      EQU   6              EXAMPLE DONE FLAG                         CM160160
0000 0007                        17  DEV       EQU   7              MUX HDX ADDRESS                           CM160170
0000 0008                        18  STAT      EQU   8              MUX STATUS                                CM160180
0000 0009                        19  REPEAT    EQU   9              EXAMPLE START ADDRESS                     CM160190
0000 000F                        20  LINK      EQU   15             LINK REGISTER                             CM160200
                                 21  *                                                                         CM160210
                                 22  *                                                                         CM160220
0000 0004                        23  EX        EQU   4              EX BIT IN STATUS BYTE IS ONE              CM160230
0000 0008                        24  BSY       EQU   8              BSY BIT IN STATUS BYTE IS ONE             CM160240
0000 0008                        25  CARRY     EQU   8              CARRY FLAG IN PSW IS ONE                  CM160250
                                 26  *                                                                         CM160260
```

```
COMM MUX PROGRAMMING EXAMPLES FOR 16- BIT PROCESSOR       PAGE   2  16:49:09  07/12/78

LOCAL TERMINAL, HALF-DUPLEX  COMM MUX OPERATION

                                28  *                                                                    CM160280
                                29  *  TTY, CRT OR GDT SHOULD BE INTERFACED THROUGH MUX HDX INTERFACE     CM160290
                                30  *  CRT/GDT SHOULD BE STRAPPED FOR HALF-DUPLEX OPERATION              CM160300
                                31  *  THE FOLLOWING EXAMPLE IS FOR 16-BIT PROCESSOR                     CM160310
                                32  *  START EXECUTION @ START1                                          CM160320
                                33  *                                                                    CM160330
                                34  *  WRITE CHARACTERS & READ KEYS USING SENSE STATUS LOOP              CM160340
                                35  *  WRITE CHARACTERS UNDER INTERRUPT CONTROL                          CM160350
                                36  *                                                                    CM160360
                                37  *                                                                    CM160370
0000R  0766                     38  START1   XAR   DONE,DONE                                             CM160380
0002R  9556                     39           EPSR  WORK,DONE          DISABLE INT @ PROCESSOR LEVEL      CM160390
0004R  C890 0000R               40           LDAI  REPEAT,START1                                        CM160400
0008R  4870 00BER               41           LH    DEV,DEVADR         GET  COMM MUX DEVICE ADDRESS       CM160410
000CR  DE70 00C0R               42           OC    DEV,SECOND         SET  MUX AS PER SECOND COMMAND     CM160420
0010R  DE70 00C1R               43           OC    DEV,DISWRT         WRITE MODE                         CM160430
0014R  C810 00C4R               44           LDAI  MSG,MSG1           (MSG) = MESSAGE START ADDRESS      CM160440
                                45  *                                                                    CM160450
0018R  D341 0000                46  EXMP1A   LB    CHAR,0(MSG)                                          CM160460
001CR  41F0 00A2R               47           BAL   LINK,OUTCHR        OUTPUT A CHARACTER                 CM160470
0020R  2611                     48           AIS   MSG,1                                                CM160480
0022R  C510 00D8R               49           CLAI  MSG,MSG1END                                          CM160490
0026R  2087                     50           BLS   EXMP1A             LOOP TILL 'TYPE 1234567890' OUTPUT CM160500
0028R  DE70 00C2R               51           OC    DEV,DISRD          SELECT READ MODE (ECHO-PLEX)       CM160510
002CR  9B75                     52           RDR   DEV,WORK           DUMMY READ TO SET BSY              CM160520
002ER  41F0 00AER               53           BAL   LINK,DELAY         LINE TURN AROUND DELAY             CM160530
0032R  0711                     54           XAR   MSG,MSG                                              CM160540
                                55  *                                                                    CM160550
0034R  41F0 0092R               56  EXMP1B   BAL   LINK,READ          READ A KEY CODE WHEN DEPRESSED     CM160560
0038R  D441 00CBR               57           CLB   CHAR,TYPED(MSG)    COMPARE WITH THE EXPECTED          CM160570
003CR  4230 003CR               58           BNE   *                                                    CM160580
0040R  2611                     59           AIS   MSG,1                                                CM160590
0042R  C510 000A                60           CLAI  MSG,10                                               CM160600
0046R  2089                     61           BLS   EXMP1B             LOOP TILL 10 DIGITS TYPED          CM160610
                                62  *                                                                    CM160620
                                63  * WRITE UNDER INTERRUPT CONTROL                                      CM160630
                                64  *                                                                    CM160640
0048R  C850 006AR               65           LDAI  WORK,INT                                             CM160650
004CR  4060 0044                66           STA   DONE,X'44'         SET UP NEW PSW FOR                 CM160660
0050R  4050 0046                67           STA   WORK,X'46'         IMMEDIATE INTERRUPT                CM160670
0054R  C810 00D8R               68           LDAI  MSG,MSG2                                             CM160680
0058R  DE70 00C3R               69           OC    DEV,ENWRT          ENABLE INT  @ MUX LEVEL 1 PENDING  CM160690
005CR  41F0 00AER               70           BAL   LINK,DELAY         LINE TURNAROUND DELAY              CM160700
0060R  C850 4000                71  EXMP1C   LDAI  WORK,X'4000'                                          CM160710
0064R  9545                     72           EPSR  CHAR,WORK          ENABLE INT @ PROCESSOR LEVEL       CM160720
0066R  4300 0066R               73           B     *                                                    CM160730
                                74  *                                                                    CM160740
                                75  * IMMEDIATE INTERRUPT IS RECEIVED                                    CM160750
                                76  *                                                                    CM160760
006AR  9F58                     77  INT      AIR   WORK,STAT          ACKNOWLEDGE AN INTERRUPT           CM160770
006CR  0557                     78           CLAR  WORK,DEV           COMPARE DEVICE THAT INTERRUPTED    CM160780
006ER  4230 006ER               79           BNE   *                                                    CM160790
0072R  0888                     80           LDAR  STAT,STAT          STATUS SHOULD BE ZERO (BSY = 0)    CM160800
```

COMM MUX PROGRAMMING EXAMPLES FOR 16- BIT PROCESSOR PAGE 3 16:49:09 07/12/78

LOCAL TERMINAL, HALF-DUPLEX COMM MUX OPERATION

```
0074R  4230 0074R          81          BNZ   *                                                    CM160810
0078R  0866                82          LDAR  DONE,DONE                                            CM160820
007AR  4230 00B6R          83          BNZ   HALT                 HALT IF DONE                    CM160830
                           84  *                                                                  CM160840
007ER  DA71 0000           85          WD    DEV,0(MSG)           WRITE A CHARACTER               CM160850
0082R  2611                86          AIS   MSG,1                                               CM160860
0084R  C510 00E6R          87          CLAI  MSG,MSG2END                                          CM160870
0088R  4280 0060R          88          BL    EXMP1C               LOOP TILL 'CORRECT !' OUTPUT    CM160880
008CR  2461                89          LIS   DONE,1               SET DONE FLAG                   CM160890
008ER  4300 0060R          90          B     EXMP1C               ACKNOWLEDGE LAST INTERRUPT      CM160900
                           91  *                                                                  CM160910
                           92  *                                                                  CM160920
0092R  9D78                93  READ    SSR   DEV,STAT             SENSE  COMM MUX STATUS          CM160930
0094R  4240 00B6R          94          BTC   EX,HALT              HALT IF 'EX' IS SET             CM160940
0098R  2083                95          BTBS  BSY,3                LOOP IN 'BSY'                   CM160950
009AR  9B74                96          RDR   DEV,CHAR             READ CHARACTER WHEN BSY DROPS   CM160960
009CR  C440 007F           97          NAI   CHAR,X'7F'           REMOVE PARITY BIT               CM160970
00A0R  030F                98          BR    LINK                 RETURN                          CM160980
                           99  *                                                                  CM160990
00A2R  9D78               100  OUTCHR  SSR   DEV,STAT                                             CM161000
00A4R  2081               101          BTBS  BSY,1                LOOP ON BSY                     CM161010
00A6R  9A74               102          WDR   DEV,CHAR                                             CM161020
00A8R  9D78               103          SSR   DEV,STAT                                             CM161030
00AAR  2081               104          BTBS  BSY,1                WAIT FOR MUX TO BECOME NOT BUSY CM161040
00ACR  030F               105          BR    LINK                 RETURN                          CM161050
                          106  *                                                                  CM161060
00AER  0755               107  DELAY   XAR   WORK,WORK                                            CM161070
00B0R  2651               108          AIS   WORK,1                                               CM161080
00B2R  2281               109          BFBS  CARRY,1                                              CM161090
00B4R  030F               110          BR    LINK                                                 CM161100
                          111  *                                                                  CM161110
00B6R  2451               112  HALT    LIS   WORK,1                                               CM161120
00B8R  915F               113          SLHLS WORK,15              WORK = X'8000'                  CM161130
00BAR  9515               114          EPSR  MSG,WORK             HALT PROCESSOR                  CM161140
00BCR  0309               115          BR    REPEAT                                               CM161150
                          116  * CONSTANTS & MESSAGES USED IN ABOVE EXAMPLES                       CM161160
                          117  *                                                                  CM161170
00BER  0010               118  DEVADR  DCX   10                   COMM MUX HDX ADDRESS            CM161180
00C0R  F8                 119  SECOND  DB    X'F8'                                                CM161190
                          120  *                                  8 DATA BITS/CHAR, 2 STOP BITS,  CM161200
                          121  *                                  NO PARITY CHECK.                CM161210
00C1R  AB                 122  DISWRT  DB    X'AB'                DISABLE INT, WRITE MODE         CM161220
00C2R  B9                 123  DISRD   DB    X'B9'                DISABLE INT, READ WITH ECHO-BACK CM161230
00C3R  6B                 124  ENWRT   DB    X'6B'                ENABLE INT, WRITE MODE          CM161240
                          125  *                                                                  CM161250
00C4R  5459 5045 2031 3233 126  MSG1    DC    C'TYPE 1234567890',X'0D0A'                         CM161260
00CCR  3435 3637 3839 3020
00D4R  0D0A
00D6R  0D0A               127          DC    X'0D0A'                                              CM161270
       0000 00D8R         128  MSG1END EQU   *                                                    CM161280
       0000 00CBR         129  TYPED   EQU   *-13                                                 CM161290
00D8R  0D0A               130  MSG2    DC    X'0D0A',C'CORRECT',X'2121',X'0D0A'                   CM161300
00DAR  434F 5252 4543 5420
```

```
00E2R  2121
00E4R  0D0A
       0000 00E6R          131  MSG2END  EQU   *                    CM161310
                           132  *                                  CM161320
00E6R                      133           END                       CM161330
```

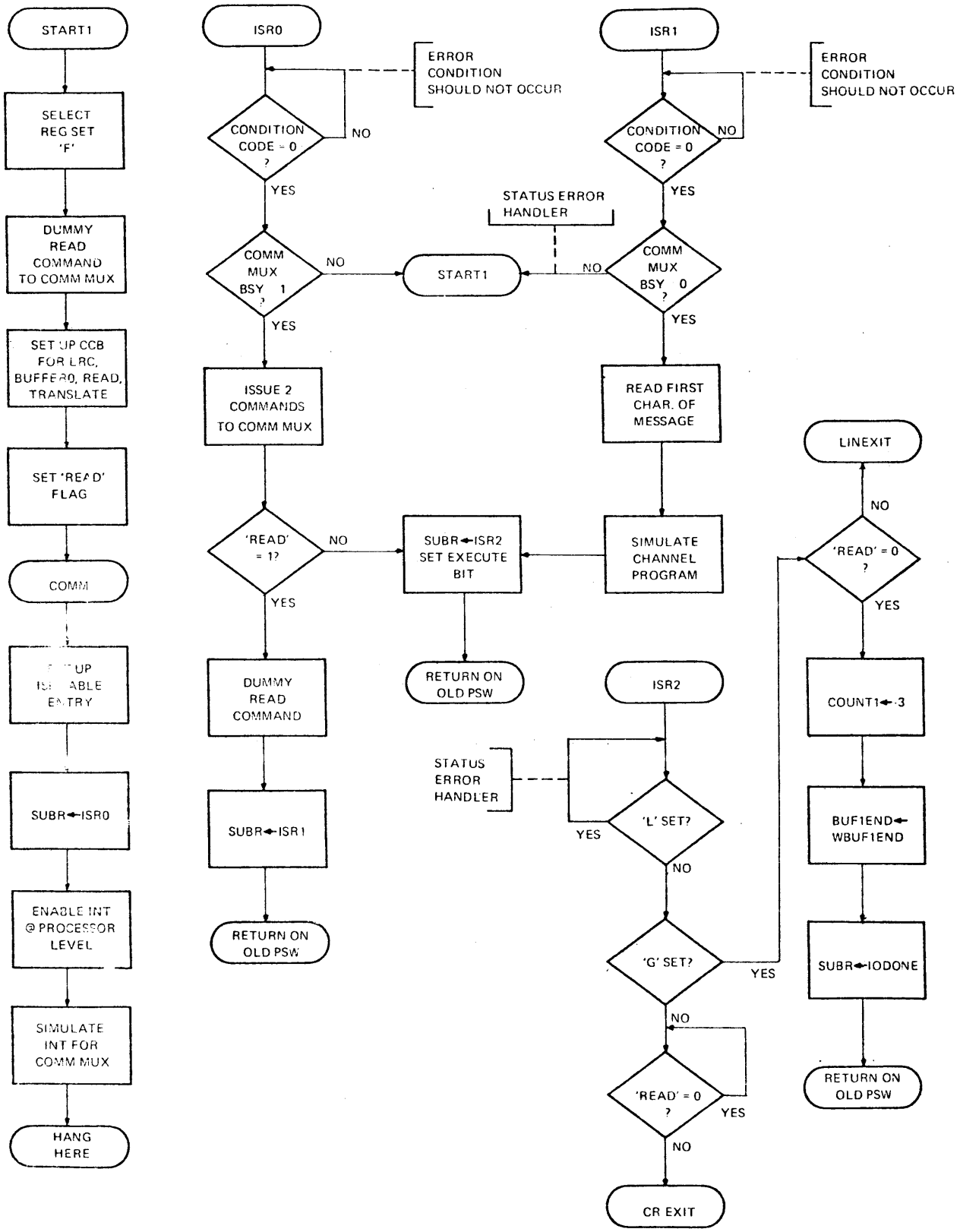
```
    COMM MUX PROGRAMMING EXAMPLES FOR 16- BIT PROCESSOR       PAGE   5  16:49:09  07/12/78

    LOCAL TERMINAL, HALF-DUPLEX  COMM MUX OPERATION

ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

START OPTIONS:  T=16,CROSS,ERLST,

   NO CAL ERRORS
   NO CAL WARNINGS
    2 PASSES

 ABSTOP     0000 0000
 ADC        0000 0002
 BSY        0000 0008          24*    95    101    104
 CARRY      0000 0008          25*   109
 CHAR       0000 0004          14*    46     57     72     96     97    102
 DELAY      0000 00AER         53     70    107*
 DEV        0000 0007          17*    41     42     43     51     52     69     78     85     93     96    100    102
                               103
 DEVADR     0000 00BER         41    118*
 DISRD      0000 00C2R         51    123*
 DISWRT     0000 00C1R         43    122*
 DONE       0000 0006          16*    38     38     39     66     82     82     89
 ENWRT      0000 00C3R         69    124*
 EX         0000 0004          23*    94
 EXMP1A     0000 0018R         46*    50
 EXMP1B     0000 0034R         56*    61
 EXMP1C     0000 0060R         71*    88     90
 HALT       0000 00B6R         83     94    112*
 IMPTOP     0000 00E6R
 INT        0000 006AR         65     77*
 LADC       0000 0001
 LINK       0000 000F          20*    47     53     56     70     98    105    110
 MSG        0000 0001          13*    44     46     48     49     54     54     57     59     60     68     85     86
                               87    114
 MSG1       0000 00C4R         44    126*
 MSG1END    0000 00D8R         49    128*
 MSG2       0000 00D8R         68    130*
 MSG2END    0000 00E6R         87    131*
 OUTCHR     0000 00A2R         47    100*
 PURETOP    0000 0000R
 READ       0000 0092R         56     93*
 REPEAT     0000 0009          19*    40    115
 SECOND     0000 00C0R         42    119*
 START1     0000 0000R         38*    40
 STAT       0000 0008          18*    77     80     80     93    100    103
 TYPED      0000 00CBR         57    129*
 WORK       0000 0005          15*    39     52     65     67     71     72     77     78    107    107    108    112
                               113    114
```

APPENDIX B
SAMPLE PROGRAMS FOR 32-BIT PROCESSORS

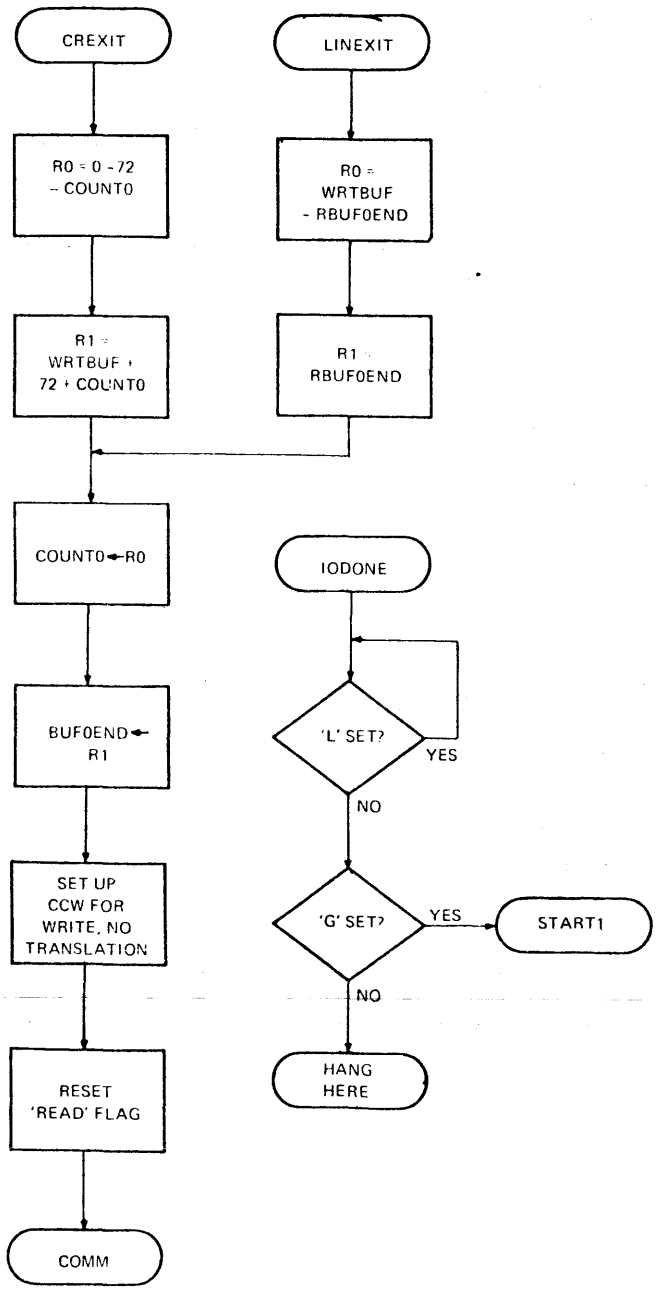
Example 1: Data Transfer Through Auto Driver Channel, 4-Wire Operation

The following flow chart and program listing is for data transfer through the Auto Driver Channel using 4-wire operation. A local terminal is used. A 10-character message is read from and written to the terminal. The example shows how to set up the interrupt service pointer table, to use the translation table, and to check for proper Auto-Driver Channel termination.

Example 1 (Continued)



Example 1 (Continued)



Example 1 (Continued)

```
        COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   1  11:10:15  08/16/78

PROG= CM32A      ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

                                 1  CM32A    PROG  COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        CM320010
                                 2           CROSS                                                          CM320020
                                 3           WIDTH 120                                                      CM320030
                                 4           TARGT 32                                                       CM320040
                                 5           NORX3                                                          CM320050
                                 6  *                                                                       CM320060
                                 7  *                                                                       CM320070
                                 8  *  USER INPUTS A MESSAGE OF UP TO 72 CHARACTERS THROUGH THE TERMINAL    CM320080
                                 9  * HOOKED TO THE COMMUNICATIONS MUX INTERFACE. A MESSAGE OF LESS THAN    CM320090
                                10  *  72 CHARACTERS MUST BE TERMINATED BY DEPRESSING 'CR' KEY TWICE. THE  CM320100
                                11  *  AUTO-DRIVER CHANNEL READS THE CHARACTERS & DOES ASCII TO ASCII      CM320110
                                12  *  TRANSLATION, AND GENERATES A BUFFER CALLED 'MESSAGE'.               CM320120
                                13  *  THEN CCB IS SET UP TO WRITE, FAST MODE, NO TRANSLATION. THE         CM320130
                                14  *  'CR', 'LF' OR JUST 'LF' IS OUTPUT FOLLOWED BY THE 'MESSAGE'        CM320140
                                15  *  BUFFER. THEN 'CR', 'LF' ARE OUTPUT.                                CM320150
                                16  *                                                                       CM320160
                                17  *  THE ENTIRE PROGRAM LOOPS ON ITSELF.                                CM320170
                                18  *                                                                       CM320180
                                19  *                                                                       CM320190
                                20  * REGISTER EQUATES                                                     CM320200
                                21  *                                                                       CM320210
                                22  *                                                                       CM320220
0000 0000                       23  R0       EQU   0                                                       CM320230
0000 0001                       24  R1       EQU   1                                                       CM320240
0000 0007                       25  DEV      EQU   7                                                       CM320250
0000 000D                       26  WORK     EQU   13                                                      CM320260
```

Example 1 (Continued)

```
COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   2  11:10:15  08/16/78

DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

                                   28  *                                                                  CM320280
000000I                            29          ORG   X'A00'                                               CM320290
                                   30  *                                                                  CM320300
                                   31  *                                                                  CM320310
000A00   C810 00F0                 32  START1  LHI   R1,X'F0'                                             CM320320
000A04   9501                      33          EPSR  R0,R1               REGISTER SET F                   CM320330
                                   34  *                                                                  CM320340
000A06   4870 0BB2                 35          LH    DEV,RCVADR          GET RECEIVE SIDE ADDRESS         CM320350
000A0A   9B7D                      36          RDR   DEV,WORK            DUMMY READ TO SET BUSY           CM320360
000A0C   4070 0BB0                 37          STH   DEV,DEVADR                                           CM320370
                                   38  *                                                                  CM320380
000A10   C810 F702                 39          LHI   R1,CCWSTA+TLATE                                      CM320390
000A14   4010 0B48                 40          STH   R1,CCW              LRC, BUFFER 0, READ, TRANSLATE   CM320400
000A18   E610 0BA7                 41          LDAI  R1,RBUFOEND                                          CM320410
000A1C   E600 0B60                 42          LDAI  R0,MESSAGE                                           CM320420
000A20   0BC1                      43          SAR   R0,R1                                                CM320430
000A22   4000 0B4A                 44          STH   R0,COUNTO                                            CM320440
000A26   5010 0B4C                 45          STA   R1,BUFOEND                                           CM320450
000A2A   D300 0DBE                 46          LB    R0,ENREAD           GET READ COMMAND                 CM320460
000A2E   D200 0BB4                 47          STB   R0,CMD                                               CM320470
000A32   24D1                      48          LIS   WORK,1                                               CM320480
000A34   40D0 0BAC                 49          STH   WORK,READ           SET FLAG                         CM320490
                                   50  *                                                                  CM320500
000A38   C810 0B48                 51  COMM    LHI   R1,CCB                                               CM320510
000A3C   2611                      52          AIS   R1,1                                                 CM320520
000A3E   4017 4700 00D0            53          STH   R1,ISPTAB(DEV,DEV)  SET UP ISP TABLE ENTRY           CM320530
000A44   2418                      54          LIS   R1,8                                                 CM320540
000A46   7610 0B48                 55          RBT   R1,CCW              RESET EX BIT                     CM320550
000A4A   C810 0AAC                 56          LHI   R1,ISR0                                              CM320560
000A4E   4010 0B5C                 57          STH   R1,SUBR             SUBROUTINE ADDRESS               CM320570
                                   58  *                                                                  CM320580
000A52   C810 40F0                 59          LHI   R1,X'40F0'                                           CM320590
000A56   9501                      60          EPSR  R0,R1               ENABLE INT @ PROCESSOR LEVEL     CM320600
000A58   4870 0BB0                 61          LH    DEV,DEVADR                                           CM320610
000A5C   E207 0000                 62          SINT  0(DEV)                                               CM320620
000A60   4300 0A60                 63          B     *                   HANG                             CM320630
                                   64  *                                                                  CM320640
                                   65  *  TO WRITE CR, LF OR JUST LF FOLLOWED BY MESSAGE & CR, LF.        CM320650
                                   66  *                                                                  CM320660
000A64   07C0                      67  CREXIT  XAR   R0,R0                                                CM320670
000A66   4810 0B4A                 68          LH    R1,COUNTO                                            CM320680
000A6A   CA10 0048                 69          AHI   R1,72                                                CM320690
000A6E   0BC1                      70          SAR   R0,R1                                                CM320700
000A70   FA10 0000 0B5E            71          AAI   R1,WRTBUF                                            CM320710
000A76   2306                      72          BS    OK                                                   CM320720
000A78   E610 0BA7                 73  LINEXIT LDAI  R1,RBUFOEND                                          CM320730
000A7C   E600 0B5E                 74          LDAI  R0,WRTBUF                                            CM320740
000A80   0BC1                      75          SAR   R0,R1                                                CM320750
000A82   4000 0B4A                 76  OK      STH   R0,COUNTO                                            CM320760
000A86   5010 0B4C                 77          STA   R1,BUFOEND                                           CM320770
000A8A   C810 F704                 78          LHI   R1,CCWSTA+WRITE     WRITE, NO TRANSLATION            CM320780
000A8E   4010 0B48                 79          STH   R1,CCW                                               CM320790
000A92   D300 0DC2                 80          LB    R0,ENWRT                                             CM320800
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Example 1 (Continued)

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      COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   3  11:10:15  08/16/78

      DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

000A96   D200 0BB4          81           STB   R0,CMD                                    CM320810
000A9A   4870 0DBC          82           LH    DEV,SNDADR                                CM320820
000A9E   4070 0BB0          83           STH   DEV,DEVADR                                CM320830
000AA2   07DD               84           XAR   WORK,WORK                                 CM320840
000AA4   40D0 0BAC          85           STH   WORK,READ          RESET FLAG             CM320850
000AA8   4300 0A38          86           B     COMM                                      CM320860
                            87 *                                                         CM320870
                            88 *  COME HERE AFTER SINT                                   CM320880
                            89 *                                                         CM320890
000AAC   42F0 0AAC          90 ISR0      BTC   C+V+G+L,*                                 CM320900
000AB0   C330 0008          91           THI   3,8                                       CM320910
000AB4   4330 0A00          92           BZ    START1                                    CM320920
000AB8   DE20 0DC3          93           OC    2,SECOND            SET UP FOR  COMM MUX  CM320930
000ABC   DE20 0BB4          94           OC    2,CMD               ISSUE COMMAND         CM320940
000AC0   48D0 0BAC          95           LH    WORK,READ                                 CM320950
000AC4   4330 0AD4          96           BZ    ISR01                                     CM320960
000AC8   9B2D               97           RDR   2,WORK              SET BSY               CM320970
000ACA   E6D0 0AE4          98           LDAI  WORK,ISR1                                 CM320980
000ACE   40D0 0B5C          99           STH   WORK,SUBR           TO READ A MESSAGE     CM320990
000AD2   1800              100           LPSWR R0                                        CM321000
                           101 *                                                         CM321010
000AD4   F6D0 0B04         102 ISR01     LDAI  WORK,ISR2                                 CM321020
000AD8   40D0 0B5C         103           STH   WORK,SUBR           TO WRITE THE MESSAGE  CM321030
000ADC   24D8              104           LIS   WORK,8                                    CM321040
000ADE   75D0 0B48         105           SBT   WORK,CCW            SET EX BIT            CM321050
000AE2   1800              106           LPSWR R0                                        CM321060
                           107 *                                                         CM321070
                           108 * COME HERE TO READ FIRST CHARACTER                       CM321080
                           109 *                                                         CM321090
000AE4   42F0 0AE4         110 ISR1      BTC   C+V+G+L,*                                 CM321100
000AE8   C330 0008         111           THI   3,8                                       CM321110
000AEC   4230 0A00         112           BNZ   START1                                    CM321120
000AF0   9B2D              113           RDR   2,WORK              READ FIRST CHARACTER OF MESSAGE  CM321130
000AF2   E3D0 0B48         114           SCP   WORK,CCB            PUT IT IN BUFFER      CM321140
000AF6   4300 0AD4         115           B     ISR01                                     CM321150
                           116 *                                                         CM321160
                           117 *                                                         CM321170
000AFA   1800              118 IGNORE    LPSWR R0                                        CM321180
                           119 *                                                         CM321190
                           120 *                                                         CM321200
000AFC   07DD              121 CR        XAR   WORK,WORK                                 CM321210
000AFE   40D0 0B48         122           STH   WORK,CCW            RESET EX BIT          CM321220
000B02   1800              123           LPSWR R0                                        CM321230
                           124 *                                                         CM321240
                           125 *                                                         CM321250
                           126 *  COME HERE AFTER ADC TERMINATION                        CM321260
                           127 *                                                         CM321270
000B04   4210 0B04         128 ISR2      BTC   L,*                                       CM321280
000B08   4220 0B18         129           BTC   G,BUFULL                                  CM321290
000B0C   48D0 0BAC         130           LH    WORK,READ                                 CM321300
000B10   4330 0B10         131           BZ    *                                         CM321310
000B14   4300 0A64         132           B     CREXIT                                    CM321320
000B18   48D0 0BAC         133 BUFULL    LH    WORK,READ                                 CM321330
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Example 1 (Continued)

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      COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   4  11:10:15  08/16/78

      DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

000B1C   4230 0A78            134            BNZ   LINEXIT                                    CM321340
000B20   C8D0 FFFD            135            LHI   WORK,-3            TO OUTPUT CR, LF, NULL, NULL.  CM321350
000B24   40D0 0B52            136            STH   WORK,COUNT1                                 CM321360
000B28   E6D0 0BAB            137            LDAI  WORK,WBUF1END                              CM321370
000B2C   50D0 0B54            138            STA   WORK,BUF1END                               CM321380
000B30   C8D0 0B3A            139            LHI   WORK,IODONE                                CM321390
000B34   40D0 0B5C            140            STH   WORK,SUBR                                  CM321400
000B38   1800                 141            LPSWR R0                                         CM321410
                              142  *                                                          CM321420
                              143  *  COME HERE WHEN ALL I/O OPERATION IS OVER                 CM321430
                              144  *                                                          CM321440
                              145  *                                                          CM321450
000B3A   4210 0B3A            146  IODONE    BTC   L,*                                       CM321460
000B3E   4220 0A00            147            BTC   G,START1                                   CM321470
000B42   4300 0B42            148            B     *                                          CM321480
                              149  *                                                          CM321490
000B48                        150            ALIGN ADC                                        CM321500
                              151  *---------------------------------                       CM321510
                              152  *                                                          CM321520
         0000 0B48            153  CCB       EQU   *                                        CM321530
000B48   0000                 154  CCW       DCX   0                                        CM321540
000B4A   0000                 155  COUNT0    DCX   0                                        CM321550
000B4C   0000 0000            156  BUF0END   DC    0                                        CM321560
000B50   00C0                 157  CHKWORD   DCX   0                                        CM321570
000B52   0000                 158  COUNT1    DCX   0                                        CM321580
000B54   0000 0000            159  BUF1END   DC    0                                        CM321590
000B58   0000 0BB8            160            DC    A(TLATETAB)                              CM321600
000B5C   00C0                 161  SUBR      DCX   0                                        CM321610
                              162  *                                                          CM321620
                              163  *---------------------------------                       CM321630
                              164  *  BUFFERS                                               CM321640
                              165  *                                                          CM321650
000B5E   0D                   166  WRTBUF    DB    13                                       CM321660
000B5F   0A                   167            DB    10                                       CM321670
000B60                        168  MESSAGE   DS    72                                       CM321680
         0000 0BA7            169  RBUF0END  EQU   *-1                                      CM321690
000BA8   0D0A                 170            DCX   0D0A,0                                   CM321700
000BAA   0000
         0000 0BAB            171  WBUF1END  EQU   *-1                                      CM321710
                              172  *---------------------------------                       CM321720
                              173  *                                                          CM321730
                              174  *  EQUATES                                               CM321740
                              175  *                                                          CM321750
         0000 F700            176  CCWSTA    EQU   X'F700'                                  CM321760
         0000 0004            177  WRITE     EQU   X'0004'                                  CM321770
         0000 0002            178  TLATE     EQU   X'0002'                                  CM321780
                              179  *                                                          CM321790
         0000 00D0            180  ISPTAB    EQU   X'D0'                                    CM321800
         0000 0008            181  C         EQU   8                                        CM321810
         0000 0004            182  V         EQU   4                                        CM321820
         0000 0002            183  G         EQU   2                                        CM321830
         0000 0001            184  L         EQU   1                                        CM321840
                              185  *                                                          CM321850
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Example 1 (Continued)

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COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   5  11:10:15  08/16/78
DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

                                186  *                                                    CM321860
                                187  *  CONSTANTS                                        CM321870
                                188  *                                                    CM321880
                                189  *                                                    CM321890
000BAC   0000 0000              190  READ      DC    0                                    CM321900
000BB0   0000                   191  DEVADR    DCX   0                                    CM321910
000BB2   0010                   192  RCVADR    DCX   10                                   CM321920
000BB4   00                     193  CMD       DB    0                                    CM321930
                                194  *                                                    CM321940
                                195  *-----------------------------------                CM321950
                                196  *                                                    CM321960
000BB8                          197            ALIGN ADC+ADC                              CM321970
                                198  *                                                    CM321980
000BB8                          199  TLATETAB  DO    13                                   CM321990
000BB8   057D                   200            DC    T(IGNORE)                            CM322000
000BBA   057D                   200            DC    T(IGNORE)
000BBC   057D                   200            DC    T(IGNORE)
000BBE   057D                   200            DC    T(IGNORE)
000BC0   057D                   200            DC    T(IGNORE)
000BC2   057D                   200            DC    T(IGNORE)
000BC4   057D                   200            DC    T(IGNORE)
000BC6   057D                   200            DC    T(IGNORE)
000BC8   057D                   200            DC    T(IGNORE)
000BCA   057D                   200            DC    T(IGNORE)
000BCC   057D                   200            DC    T(IGNORE)
000BCE   057D                   200            DC    T(IGNORE)
000BD0   057D                   200            DC    T(IGNORE)
000BD2   057E                   201            DC    T(CR)                                CM322010
000BD4                          202            DO    9                                    CM322020
000BD4   057D                   203            DC    T(IGNORE),T(IGNORE)                  CM322030
000BD6   057D
000BD8   057D                   203            DC    T(IGNORE),T(IGNORE)
000BDA   057D
000BDC   057D                   203            DC    T(IGNORE),T(IGNORE)
000BDE   057D
000BE0   057D                   203            DC    T(IGNORE),T(IGNORE)
000BE2   057D
000BE4   057D                   203            DC    T(IGNORE),T(IGNORE)
000BE6   057D
000BE8   057D                   203            DC    T(IGNORE),T(IGNORE)
000BEA   057D
000BEC   057D                   203            DC    T(IGNORE),T(IGNORE)
000BEE   057D
000BF0   057D                   203            DC    T(IGNORE),T(IGNORE)
000BF2   057D
000BF4   057D                   203            DC    T(IGNORE),T(IGNORE)
000BF6   057D
         0000 0BF8              204  TABLE     EQU   *                                    CM322040
000BF8                          205            DO    32                                   CM322050
000BF8   8020 8021              206            DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2  CM322060
000BFC   8022 8023              206            DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C00   8024 8025              206            DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C04   8026 8027              206            DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
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Example 1 (Continued)

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      COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   6  11:10:15  08/16/78

      DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

000C08   8028 8029            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C0C   802A 802B            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C10   802C 802D            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C14   802E 802F            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C18   8030 8031            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C1C   8032 8033            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C20   8034 8035            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C24   8036 8037            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C28   8038 8039            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C2C   803A 803B            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C30   803C 803D            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C34   803E 803F            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C38   8040 8041            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C3C   8042 8043            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C40   8044 8045            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C44   8046 8047            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C48   8048 8049            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C4C   804A 804B            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C50   804C 804D            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C54   804E 804F            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C58   8050 8051            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C5C   8052 8053            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C60   8054 8055            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C64   8056 8057            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C68   8058 8059            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C6C   805A 805B            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C70   805C 805D            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C74   805E 805F            206          DB    X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C78                        207          DO    16                                      CM322070
000C78   057D                 208          DC    T(IGNORE),T(IGNORE)                     CM322080
000C7A   057D
000C7C   057D                 208          DC    T(IGNORE),T(IGNORE)
000C7E   057D
000C80   057D                 208          DC    T(IGNORE),T(IGNORE)
000C82   057D
000C84   057D                 208          DC    T(IGNORE),T(IGNORE)
000C86   057D
000C88   057D                 208          DC    T(IGNORE),T(IGNORE)
000C8A   057D
000C8C   057D                 208          DC    T(IGNORE),T(IGNORE)
000C8E   057D
000C90   057D                 208          DC    T(IGNORE),T(IGNORE)
000C92   057D
000C94   057D                 208          DC    T(IGNORE),T(IGNORE)
000C96   057D
000C98   057D                 208          DC    T(IGNORE),T(IGNORE)
000C9A   057D
000C9C   057D                 208          DC    T(IGNORE),T(IGNORE)
000C9E   057D
000CA0   057D                 208          DC    T(IGNORE),T(IGNORE)
000CA2   057D
000CA4   057D                 208          DC    T(IGNORE),T(IGNORE)
000CA6   057D
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Example 1 (Continued)

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      COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   7  11:10:15  08/16/78

      DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

000CA8   057D                  208            DC    T(IGNORE),T(IGNORE)
000CAA   057D
000CAC   057D                  208            DC    T(IGNORE),T(IGNORE)
000CAE   057D
000CB0   057D                  208            DC    T(IGNORE),T(IGNORE)
000CB2   057D
000CB4   057D                  208            DC    T(IGNORE),T(IGNORE)
000C36   057D
                               209  *                                                    CM322090
                               210  *                                                    CM322100
000CB8                         211            DO    13                                   CM322110
000CB8   057D                  212            DC    T(IGNORE)                            CM322120
000CBA   057D                  212            DC    T(IGNORE)
000CBC   057D                  212            DC    T(IGNORE)
000CBE   057D                  212            DC    T(IGNORE)
000CC0   057D                  212            DC    T(IGNORE)
000CC2   057D                  212            DC    T(IGNORE)
000CC4   057D                  212            DC    T(IGNORE)
000CC6   057D                  212            DC    T(IGNORE)
000CC8   057D                  212            DC    T(IGNORE)
000CCA   057D                  212            DC    T(IGNORE)
000CCC   057D                  212            DC    T(IGNORE)
000CCE   057D                  212            DC    T(IGNORE)
000CD0   057D                  212            DC    T(IGNORE)
000CD2   057E                  213            DC    T(CR)                                CM322130
000CD4                         214            DO    9                                    CM322140
000CD4   057D                  215            DC    T(IGNORE),T(IGNORE)                  CM322150
000CD6   057D
000CD8   057D                  215            DC    T(IGNORE),T(IGNORE)
000CDA   057D
000CDC   057D                  215            DC    T(IGNORE),T(IGNORE)
000CDE   057D
000CE0   057D                  215            DC    T(IGNORE),T(IGNORE)
000CE2   057D
000CE4   057D                  215            DC    T(IGNORE),T(IGNORE)
000CE6   057D
000CE8   057D                  215            DC    T(IGNORE),T(IGNORE)
000CEA   057D
000CEC   057D                  215            DC    T(IGNORE),T(IGNORE)
000CEE   057D
000CF0   057D                  215            DC    T(IGNORE),T(IGNORE)
000CF2   057D
000CF4   057D                  215            DC    T(IGNORE),T(IGNORE)
000CF6   057D
         0000 0CF8             216  TABLEH   EQU   *                                    CM322160
000CF8                         217            DO    32                                   CM322170
000CF8   8020 8021             218            DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2  CM322180
000CFC   8022 8023             218            DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D00   8024 8025             218            DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D04   8026 8027             218            DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D08   8028 8029             218            DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D0C   802A 802B             218            DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D10   802C 802D             218            DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
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Example 1 (Continued)

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COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   8  11:10:15  08/16/78

DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

000D14   802E 802F          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D18   8030 8031          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D1C   8032 8033          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D20   8034 8035          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D24   8036 8037          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D28   8038 8039          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D2C   803A 803B          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D30   803C 803D          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D34   803E 803F          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D38   8040 8041          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D3C   8042 8043          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D40   8044 8045          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D44   8046 8047          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D48   8048 8049          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D4C   804A 804B          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D50   804C 804D          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D54   804E 804F          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D58   8050 8051          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D5C   8052 8053          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D60   8054 8055          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D64   8056 8057          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D68   8058 8059          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D6C   805A 805B          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D70   805C 805D          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D74   805E 805F          218          DB    X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D78                      219          DO    16                                      CM322190
000D78   057D               220          DC    T(IGNORE),T(IGNORE)                     CM322200
000D7A   057D
000D7C   057D               220          DC    T(IGNORE),T(IGNORE)
000D7E   057D
000D80   057D               220          DC    T(IGNORE),T(IGNORE)
000D82   057D
000D84   057D               220          DC    T(IGNORE),T(IGNORE)
000D86   057D
000D88   057D               220          DC    T(IGNORE),T(IGNORE)
000D8A   057D
000D8C   057D               220          DC    T(IGNORE),T(IGNORE)
000D8E   057D
000D90   057D               220          DC    T(IGNORE),T(IGNORE)
000D92   057D
000D94   057D               220          DC    T(IGNORE),T(IGNORE)
000D96   057D
000D98   057D               220          DC    T(IGNORE),T(IGNORE)
000D9A   057D
000D9C   057D               220          DC    T(IGNORE),T(IGNORE)
000D9E   057D
000DA0   057D               220          DC    T(IGNORE),T(IGNORE)
000DA2   057D
000DA4   057D               220          DC    T(IGNORE),T(IGNORE)
000DA6   057D
000DA8   057D               220          DC    T(IGNORE),T(IGNORE)
000DAA   057D
000DAC   057D               220          DC    T(IGNORE),T(IGNORE)
```

Example 1 (Continued)

```
      COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   9  11:10:15  08/16/78

      DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

000DAE   057D
000DB0   057D                  220            DC    T(IGNORE),T(IGNORE)
000DB2   057D
000DB4   057D                  220            DC    T(IGNORE),T(IGNORE)
000DB6   057D
                               221  *                                                          CM322210
                               222  *                                                          CM322220
                               223  * CONSTANTS USED IN ABOVE EXAMPLES                        CM322230
                               224  *                                                          CM322240
000DB8   0000                  225  READING   DCX   0              READ FLAG                   CM322250
000DBA   0010                  226  RECADR    DCX   10             COMM MUX RECEIVE ADDRESS    CM322260
000DBC   0011                  227  SNDADR    DCX   11             COMM MUX SEND ADDRESS       CM322270
000DBE   79                    228  ENREAD    DB    X'79'          ENABLE,ECHO,READ            CM322280
000DBF   B9                    229  DISRD     DB    X'B9'          DISABLE,ECHO,READ           CM322290
000DC0   AB                    230  DISWRT    DB    X'AB'          DISABLE,WRITE               CM322300
000DC1   3B                    231  RQ2S      DB    X'3B'          REQUEST TO SEND (WRT/RD = 1) CM322310
000DC2   6B                    232  ENWRT     DB    X'6B'          ENABLE,WRITE                CM322320
000DC3   F8                    233  SECOND    DB    X'F8'                                      CM322330
                               234  *                            2 STOP BITS, NO PARITY CHECK CM322340
000DC4                         235            END                                              CM322350
```

Example 1 (Continued)

```
    COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE  10  11:10:15  08/16/78

    DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

START OPTIONS:  T=32,CROSS,ERLST,

   NO CAL ERRORS
   NO CAL WARNINGS
    2 PASSES

 ABSTOP    0000 0DC4
 ADC       0000 0004        150    197    197
 BUF0END   0000 0B4C         45     77    156*
 BUF1END   0000 0B54        138    159*
 BUFULL    0000 0B18        129    133*
 C         0000 0008         90    110    181*
 CCB       0000 0B48         51    114    153*
 CCW       0000 0B48         40     55     79    105    122    154*
 CCWSTA    0000 F700         39     78    176*
 CHKWORD   0000 0B50        157*
 CMD       0000 0BB4         47     81     94    193*
 COMM      0000 0A38         51*    86
 COUNT0    0000 0B4A         44     68     76    155*
 COUNT1    0000 0B52        136    158*
 CR        0000 0AFC        121*   201    213
 CREXIT    0000 0A64         67*   132
 DEV       0000 0007         25*    35     36     37     53     53     61     62     82     83
 DEVADR    0000 0BB0         37     61     83    191*
 DISRD     0000 0DBF        229*
 DISWRT    0000 0DC0        230*
 ENREAD    0000 0DBE         46    228*
 ENWRT     0000 0DC2         80    232*
 G         0000 0002         90    110    129    147    183*
 IGNORE    0000 0AFA        118*   200    203    203    208    208    212    215    215    220    220
 IMPTOP    0000 0000I
 IODONE    0000 0B3A        139    146*
 ISPTAB    0000 00D0         53    180*
 ISR0      0000 0AAC         56     90*
 ISR01     0000 0AD4         96    102*   115
 ISR1      0000 0AE4         98    110*
 ISR2      0000 0B04        102    128*
 L         0000 0001         90    110    128    146    184*
 LADC      0000 0002
 LINEXIT   0000 0A78         73*   134
 MESSAGE   0000 0B60         42    168*
 OK        0000 0A82         72     76*
 PURETOP   0000 0000P
 R0        0000 0000         23*    33     42     43     44     46     47     50     67     67     70     74     75
                             76     80     81    100    105    118    123    141
 R1        0000 0001         24*    32     33     39     40     41     43     45     51     52     53     54     55
                             56     57     59     60     68     69     70     71     73     75     77     78     79
 RBUF0END  0000 0BA7         41     73    169*
 RCVADR    0000 0BB2         35    192*
 READ      0000 0BAC         49     85     95    130    133    190*
 READING   0000 0DB8        225*
```

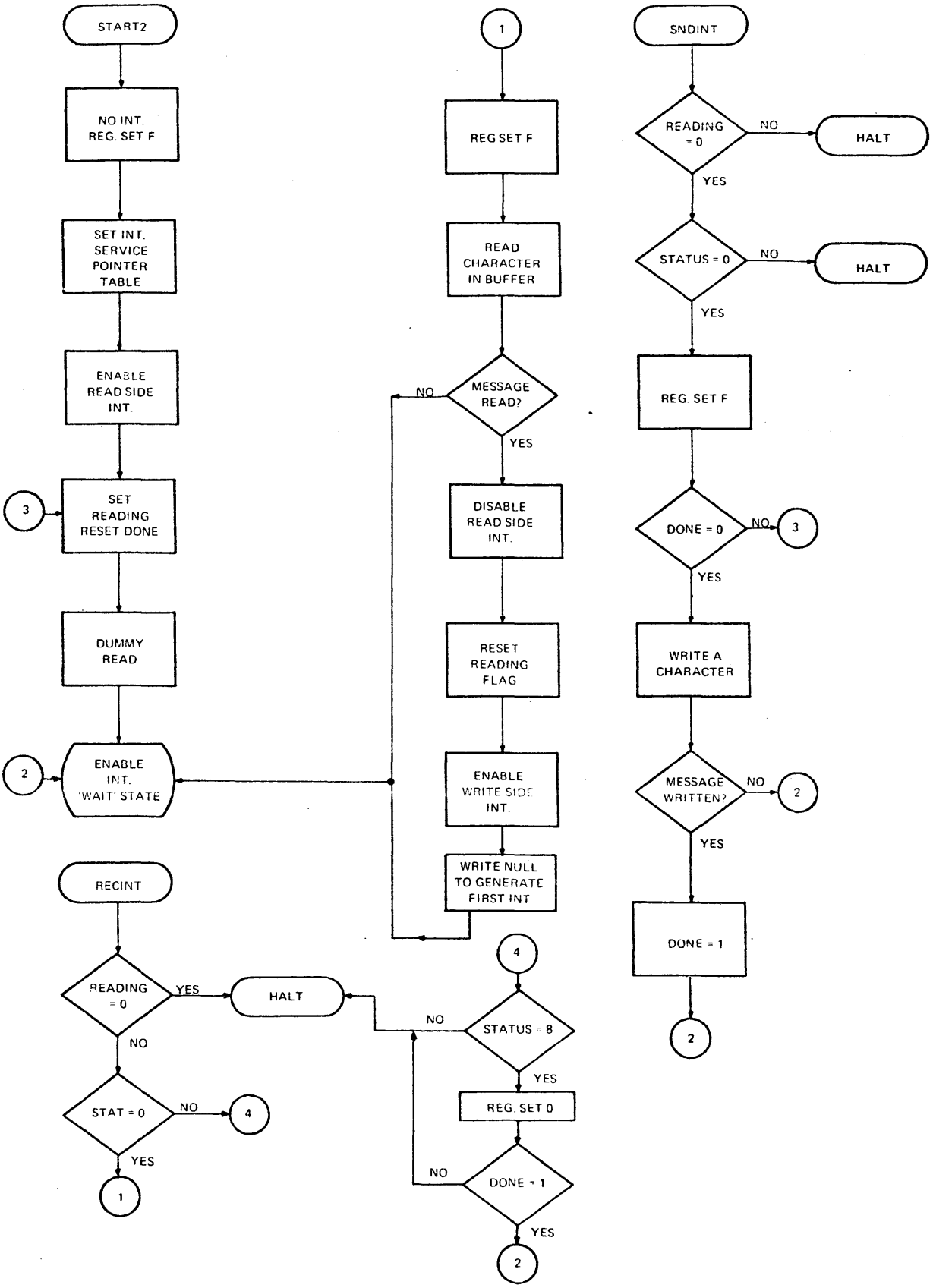
Example 1 (Continued)

```
   COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE  11  11:10:15  08/16/78

   DATA TRANS THRU AUTO DRIVER CHANNEL 4 WIRE OPERATION

RECADR     0000 0DBA        226*
RQ2S       0000 0DC1        231*
SECOND     0000 0DC3         93    233*
SNDADR     0000 0DBC         82    227*
START1     0000 0A00         32*    92    112    147
SUBR       0000 0B5C         57     99    103    140    161*
TABLE      0000 0BF8        204*   206    206
TABLEH     0000 0CF8        216*   218    218
TLATE      0000 0002         39    178*
TLATETAB   0000 0BB8        160    199*
V          0000 0004         90    110    182*
WBUF1END   0000 0BAB        137    171*
WORK       0000 000D         26*    36     48     49     84     84     85     95     97     98     99    102    103
                            104    105    113    114    121    121    122    130    133    135    136    137    138
                            139    140
WRITE      0000 0004         78    177*
WRTBUF     0000 0B5E         71     74    166*
```

Example 2: Local Terminal Full-Duplex COMM MUX Operation

The following flow chart and program listing is for local terminal full-duplex COMM MUX operation. In this example, the data transfer is under interrupt control. A 10-character message is read from and written to the terminal. The last write side interrupt is cleared.

Example 2 (Continued)



Example 2 (Continued)

```
      COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   1  14:10:39  08/16/78

PROG= CM32B      ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

                                 1  CM32B    PROG  COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        CM322360
                                 2           CROSS                                                         CM322370
                                 3           WIDTH 120                                                     CM322380
                                 4           TARGT 32                                                      CM322390
                                 5           NORX3                                                         CM322400
                                 6  *                                                                      CM322410
                                 7  *                                                                      CM322420
```

Example 2 (Continued)

```
COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   2  14:10:39  08/16/78

LOCAL TERMINAL, FULL DUPLEX  COMM MUX OPERATION

                                 9  *                                                                    CM322440
                                10  *  THE TERMINAL SHOULD BE INTERFACED THROUGH COMM MUX FDX INTERFACE   CM322450
                                11  *  THE FOLLOWING EXAMPLE IS FOR 32-BIT PROCESSOR                     CM322460
                                12  *  START EXECUTION @ START                                           CM322470
                                13  *                                                                    CM322480
                                14  *  READ 10 KEYS & WRITE THOSE 10 CHARACTERS UNDER INTERRUPT CONTROL  CM322490
                                15  *                                                                    CM322500
                                16  *                                                                    CM322510
                                17  *  REGISTER ASSIGNMENTS                                              CM322520
                                18  *                                                                    CM322530
          0000 0000             19  DONE     EQU   0                  EXAMPLE DONE FLAG                 CM322540
          0000 0002             20  DEV0     EQU   2                  COMM MUX RECEIVE ADDRESS          CM322550
          0000 0003             21  DEV1     EQU   3                  COMM MUX SEND ADDRESS             CM322560
          0000 0003             22  R3       EQU   3                  STATUS OF INTERRUPTING DEVICE     CM322570
          0000 0004             23  MSG      EQU   4                  MESSAGE ADDRESS                   CM322580
          0000 0005             24  STAT     EQU   5                  COMM MUX STATUS                   CM322590
          0000 0008             25  BSY      EQU   8                                                    CM322600
          0000 000A             26  R10      EQU   10                                                   CM322610
          0000 000B             27  R11      EQU   11                 WORK REGISTER                     CM322620
          0000 000C             28  R12      EQU   12                 WORK REGISTER                     CM322630
          0000 000D             29  WORK     EQU   13                                                   CM322640
                                30  *                                                                    CM322650
000000I                         31           ORG   X'A00'                                                CM322660
000A00    F8D0 0000 00F0        32  START    LI    WORK,Y'F0'                                           CM322670
000A06    954D                  33           EPSR  MSG,WORK           NO INT, REG SET F                 CM322680
                                34  *                                                                    CM322690
                                35  * SET UP INTERRUPT SERVICE POINTER TABLE                            CM322700
                                36  *                                                                    CM322710
000A08    E640 0AF6             37           LDAI  MSG,HALT                                             CM322720
000A0C    E6A0 00D0             38           LDAI  R10,X'D0'                                            CM322730
000A10    24B2                  39           LIS   R11,2                                                CM322740
000A12    E6C0 02CE             40           LDAI  R12,X'2CE'                                           CM322750
000A16    404A 0000             41  EXMP2A   STH   MSG,0(R10)         SET UP ENTIRE TABLE WITH 'HALT'   CM322760
000A1A    C1A0 0A16             42           BXLE  R10,EXMP2A                                           CM322770
                                43  *                                                                    CM322780
000A1E    4820 0AFC             44           LH    DEV0,RECADR        GET BOTH ADDRESSES                CM322790
000A22    4830 0AFE             45           LH    DEV1,SNDADR                                          CM322800
000A26    DE20 0B05             46           OC    DEV0,SECOND        SET UP  COMM MUX                  CM322810
000A2A    08A2                  47           LR    R10,DEV0           SET UP 2 TABLE ENTRIES FOR        CM322820
000A2C    0AAA                  48           AAR   R10,R10            RECEIVE & TRANSMIT DEVICES.       CM322830
000A2E    C8D0 0A62             49           LHI   WORK,RECINT                                          CM322840
000A32    40DA 00D0             50           STH   WORK,X'D0'(R10)                                      CM322850
000A36    08A3                  51           LR    R10,DEV1                                             CM322860
000A38    0AAA                  52           AAR   R10,R10                                              CM322870
000A3A    C8D0 0AC8             53           LHI   WORK,SNDINT                                          CM322880
000A3E    40DA 00D0             54           STH   WORK,X'D0'(R10)                                      CM322890
                                55  *                                                                    CM322900
000A42    0700                  56  REPEAT2  XAR   DONE,DONE                                           CM322910
000A44    E640 0B0A             57           LDAI  MSG,MSG33                                            CM322920
000A48    4040 0AFA             58           STH   MSG,READING          RESET FLAG                      CM322930
000A4C    DE20 0B00             59           OC    DEV0,ENREAD          ENABLE READ SIDE INT, FCHO MODE CM322940
000A50    DE20 0B03             60           OC    DEV0,RQ2S                                            CM322950
000A54    9B2D                  61           RDR   DEV0,WORK            DUMMY READ TO SET BSY           CM322960
```

Example 2 (Continued)

```
COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   3  14:10:39  08/16/78

LOCAL TERMINAL, FULL DUPLEX  COMM MUX OPERATION

000A56   F8D0 0000 C0F0      62  EXMP2B   LI     WORK,Y'C0F0'        ENABLE INT & HALT TILL DEPRESSION     CM322970
000A5C   95AD                63           EPSR   R10,WORK            OF A KEY INTERRUPTS                   CM322980
000A5E   4300 0A5E           64           B      *                                                         CM322990
                             65  *                                                                         CM323000
                             66  * RECEIVE SIDE HAS INTERRUPTED                                            CM323010
                             67  *                                                                         CM323020
000A62   48A0 0AFA           68  RECINT   LH     R10,READING         HALT IF RECEIVE SIDE INTERRUPTS       CM323030
000A66   4330 0A66           69           BZ     *                   WHEN 'READING' FLAG IS RESET          CM323040
000A6A   0833                70           LR     R3,R3               (R3) = RECEIVE SIDE STATUS            CM323050
000A6C   4330 0A8A           71           BZ     TEST1                                                     CM323060
000A70   C530 0008           72           CLHI   R3,8                                                      CM323070
000A74   4230 0AF6           73           BNE    HALT                                                      CM323080
000A78   C8D0 00F0           74           LHI    WORK,X'F0'                                                CM323090
000A7C   95AD                75           EPSR   R10,WORK                                                  CM323100
000A7E   0800                76           LR     DONE,DONE                                                 CM323110
000A80   4230 0AF6           77           BNZ    HALT                                                      CM323120
000A84   2401                78           LIS    DONE,1                                                    CM323130
000A86   4300 0A56           79           B      EXMP2B                                                    CM323140
         0000 0A8A           80  TEST1    EQU    *                                                         CM323150
000A8A   F8D0 0000 00F0      81           LI     WORK,Y'F0'                                                CM323160
000A90   95AD                82           EPSR   R10,WORK            REGISTER SET F                        CM323170
000A92   2401                83           LIS    DONE,1                                                    CM323180
000A94   DB24 0000           84           RD     DEV0,0(MSG)         READ BYTE INTO MESSAGE BUFFER         CM323190
000A98   2641                85           AIS    MSG,1                                                     CM323200
000A9A   F540 0000 0B14      86           CLAI   MSG,MSG33END                                              CM323210
000AA0   4280 0A56           87           BL     EXMP2B              LOOP TILL 10 KEYS ARE READ IN.        CM323220
                             88  *                                                                         CM323230
                             89  * TO WRITE THE MESSAGE JUST READ IN                                       CM323240
                             90  *                                                                         CM323250
000AA4   DE20 0B01           91           OC     DEV0,DISRD          DISABLE READ SIDE INTERRUPTS          CM323260
000AA8   DE20 0B03           92           OC     DEV0,RQ2S                                                 CM323270
000AAC   E640 0B06           93           LDAI   MSG,MSG3                                                  CM323280
000AB0   2400                94           LIS    DONE,0                                                    CM323290
000AB2   4000 0AFA           95           STH    DONE,READING        RESET FLAG                            CM323300
000AB6   DE30 0B04           96           OC     DEV1,ENWRT          ENABLE WRITE SIDE INTERRUPTS          CM323310
000ABA   9A30                97           WDR    DEV1,DONE           WRITE NULL TO GENERATE FIRST INT.     CM323320
000ABC   F8D0 0000 C0F0      98  EXMP2C   LI     WORK,Y'C0F0'                                              CM323330
000AC2   95AD                99           EPSR   R10,WORK            ENABLE INT @ PROCESSOR LEVEL & HALT   CM323340
000AC4   4300 0AC4          100           B      *                                                         CM323350
                            101  *                                                                         CM323360
                            102  * TRANSMIT SIDE HAS INTERRUPTED                                           CM323370
                            103  *                                                                         CM323380
000AC8   48A0 0AFA          104  SNDINT   LH     R10,READING                                               CM323390
000ACC   4230 0ACC          105           BNZ    *                                                         CM323400
000AD0   0833               106           LR     R3,R3               STATUS SHOULD BE ZERO                 CM323410
000AD2   4230 0AD2          107           BNZ    *                                                         CM323420
000AD6   F8D0 0000 00F0     108           LI     WORK,Y'F0'                                                CM323430
000ADC   95AD               109           EPSR   R10,WORK            REGISTER SET F                        CM323440
000ADE   DA34 0000          110           WD     DEV1,0(MSG)                                               CM323450
000AE2   2641               111           AIS    MSG,1                                                     CM323460
000AE4   F540 0000 0B18     112           CLAI   MSG,MSG3END                                               CM323470
000AEA   4280 0ABC          113           BL     EXMP2C                                                    CM323480
000AEE   DE30 0B02          114           OC     R3,DISWRT                                                 CM323490
```

Example 2 (Continued)

```
     COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   4  14:10:39  08/16/78

     LOCAL TERMINAL, FULL DUPLEX  COMM MUX OPERATION

000AF2  4300 0A42          115            B      REPEAT2                                    CM323500
000AF6  4300 0AF6          116  HALT      B      *                                          CM323510
                           117  *                                                         CM323520
                           118  *                                                         CM323530
                           119  * CONSTANTS USED IN ABOVE EXAMPLES                        CM323540
                           120  *                                                         CM323550
000AFA  0000               121  READING   DCX    0                  READ FLAG              CM323560
000AFC  0010               122  RECADR    DCX    10                 COMM MUX RECEIVE ADDRESS CM323570
000AFE  0011               123  SNDADR    DCX    11                 COMM MUX SEND ADDRESS  CM323580
000B00  79                 124  ENREAD    DB     X'79'              ENABLE,ECHO,READ       CM323590
000B01  B9                 125  DISRD     DB     X'B9'              DISABLE,ECHO,READ      CM323600
000B02  AB                 126  DISWRT    DB     X'AB'              DISABLE,WRITE          CM323610
000B03  3B                 127  RQ2S      DB     X'3B'              REQUEST TO SEND (WRT/RD = 1) CM323620
000B04  6B                 128  ENWRT     DB     X'6B'              ENABLE,WRITE           CM323630
000B05  F8                 129  SECOND    DB     X'F8'                                     CM323640
                           130  *                                 2 STOP BITS, NO PARITY CHECK CM323650
000B06  FFFF               131  MSG3      DCX    FFFF                                      CM323660
000B08  0D0A               132            DC     X'0D0A'                                   CM323670
000B0A                     133  MSG33     DS     10                 10 CHARACTER MESSAGE BUFFER CM323680
        0000 0B14          134  MSG33END  EQU    *                                         CM323690
000B14  0D0A               135            DC     X'0D0A'                                   CM323700
000B16  0000               136            DCX    0                  2 NULL CHARACTERS      CM323710
        0000 0B18          137  MSG3END   EQU    *                                         CM323720
                           138  *                                                         CM323730
000B18                     139            END                                              CM323740
```

Example 2 (Continued)

```
    COMM MUX PROGRAMMING EXAMPLES FOR 32-BIT PROCESSOR        PAGE   5  14:10:39  08/16/78

    LOCAL TERMINAL, FULL DUPLEX  COMM MUX OPERATION

ASSEMBLED BY CAL 03-066R05-00   (32-BIT)

START OPTIONS:  T=32,CROSS,ERLST,

   NO CAL ERRORS
   NO CAL WARNINGS
    2 PASSES

 ABSTOP     0000 0B18
 ADC        0000 0004
 BSY        0000 0008          25*
 DEV0       0000 0002          20*    44      46      47      59      60      61      84      91      92
 DEV1       0000 0003          21*    45      51      96      97     110
 DISRD      0000 0B01          91    125*
 DISWRT     0000 0B02         114    126*
 DONE       0000 0000          19*    56      56      76      76      78      83      94      95      97
 ENREAD     0000 0B00          59    124*
 ENWRT      0000 0B04          96    128*
 EXMP2A     0000 0A16          41*    42
 EXMP2B     0000 0A56          62*    79      87
 EXMP2C     0000 0ABC          98*   113
 HALT       0000 0AF6          37     73      77     116*
 IMPTOP     0000 0000I
 LADC       0000 0002
 MSG        0000 0004          23*    33      37      41      57      58      84      85      86      93     110     111     112
 MSG3       0000 0B06          93    131*
 MSG33      0000 0B0A          57    133*
 MSG33END   0000 0B14          86    134*
 MSG3END    0000 0B18         112    137*
 PURETOP    0000 0000P
 R10        0000 000A          26*    38      41      42      47      48      48      50      51      52      52      54      63
                               68     75      82      99     104     109
 R11        0000 000B          27*    39
 R12        0000 000C          28*    40
 R3         0000 0003          22*    70      70      72     106     106     114
 READING    0000 0AFA          58     68      95     104     121*
 RECADR     0000 0AFC          44    122*
 RECINT     0000 0A62          49     68*
 REPEAT2    0000 0A42          56*   115
 RQ2S       0000 0B03          60     92     127*
 SECOND     0000 0B05          46    129*
 SNDADR     0000 0AFE          45    123*
 SNDINT     0000 0AC8          53    104*
 START      0000 0A00          32*
 STAT       0000 0005          24*
 TEST1      0000 0A8A          71     80*
 WORK       0000 000D          29*    32      33      49      50      53      54      61      62      63      74      75      81
                               82     98      99     108     109
```

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