PERKIN-ELMER

SERIES 3200 PROCESSORS
SELECTOR CHANNEL (SELCH)
(35-732M02)

Maintenance Manual

47-096 R00

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PREFACE

The selector channel (SELCH) is a direct memory access interface (DMAI) that provides a direct means of communication between input/output (I/O) device controllers and the memory system. It is connected to the memory system via the direct memory access (DMA) bus. The I/O device controllers are connected to a SELCH by a private bus and only respond through their SELCH. This manual covers the installation and maintenance of the Perkin-Elmer Series 3200 SELCH. Chapter 1 provides the installation information including strapping. Chapter 2 contains the bus protocol information. Chapter 3 contains data path information. Chapter 4 contains maintenance information. Appendixes A to E provide strapping options for the 3210, 3220, 3230, 3240 and 3250XP Processors.

The following manuals provide more detailed information on the 3210, 3220, 3230, 3240 and 3250XP systems:

- 3210 Installation and Maintenance Manual
- 3220 Processor Maintenance Manual
- 3230 Installation and Maintenance Manual
- 3240 Maintenance Manual
- 3250XP Installation and Configuration Manual

For information on the contents of all Perkin-Elmer 32-bit manuals, see the 32-Bit Systems User Documentation Summary.

CHAPTER 1
INSTALLATION

1.1 INTRODUCTION

This chapter provides information necessary for the installation of the Perkin-Elmer Series 3200 Selector Channel (SELCH) (02-630) in a Series 3200 Digital System.

The SELCH must have access to three buses: the multiplexor (MUX) bus between the processor and the SELCH, the direct memory access (DMA) bus between the memory system and the SELCH and the private bus between the SELCH and the input/output (I/O) devices connected to the SELCH (see Figure 1-1).

Series 3200 Digital Systems can accommodate multiple SELCHs.

The MUX bus and the DMA bus are connected to all SELCHs. In the Model 3240 and 3250XP Digital Systems, there can be up to four distinct DMA buses. Each DMA bus services a maximum of eight SELCHs. In the Model 3210, 3220 and 3230 Systems, there is a single DMA bus that is connected to all SELCHs.

Each SELCH has its own private bus which is connected to its I/O devices.

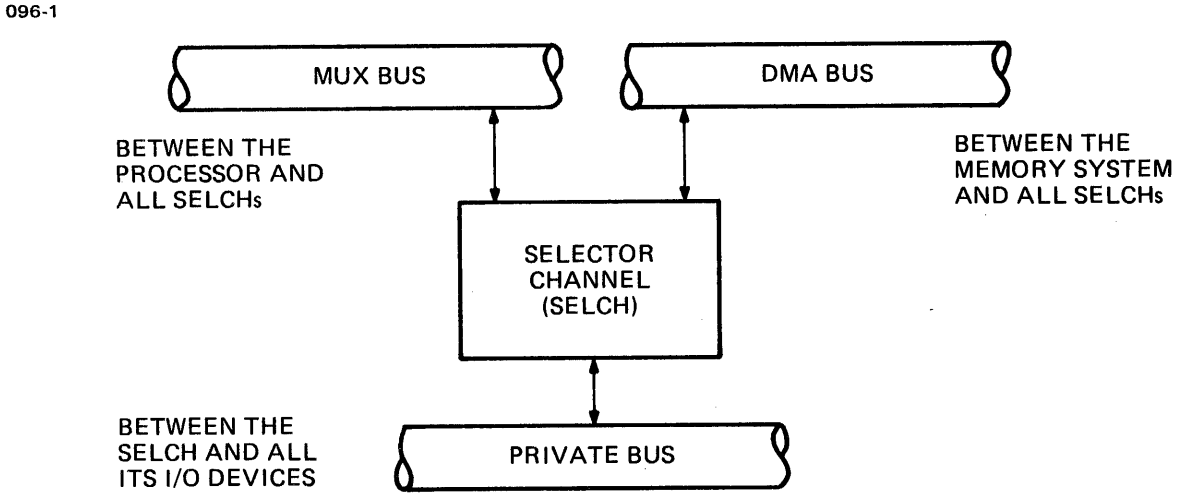


Figure 1-1 SELCH Bus Interface

1.2 SPECIFICATIONS

The SELCH is contained on a 390mm x 378mm (15 3/8in x 14 7/8in) printed circuit (PC) board. The device consumes a maximum of 6.0A at 5.0VDC.

1.3 INSTALLATION IN SERIES 3200 DIGITAL SYSTEMS

This section contains the necessary information to install the SELCH in Series 3200 Systems.

1.3.1 Models 3210, 3220 and 3230 Processors

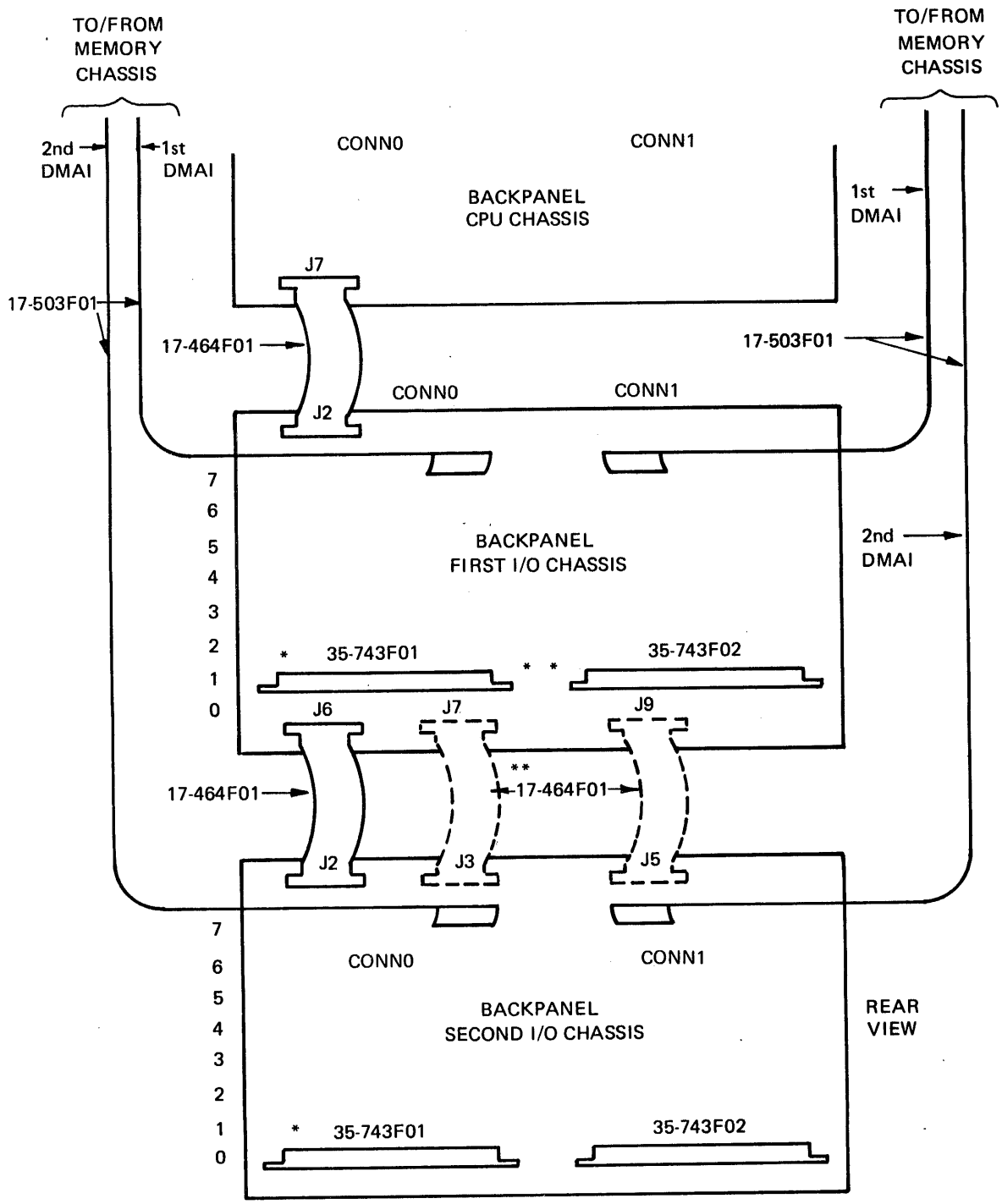
The SELCH can be installed in any even-numbered chassis slot (i.e., 0, 2, 4 or 6) of the DMA bus. The DMA bus starts at either slot 2 of the processor chassis or slot 7 of the I/O expansion chassis. The DMA bus can be extended to another I/O expansion chassis through cables, but the bus length is limited to eight feet. Seven DMA devices can be installed on the DMA bus. These devices can be any combination of SELCHs or custom DMA devices. To terminate a DMA bus in the Model 3210 and 3220 Systems, install a 35-572 terminator at the second slot from the end of the DMA bus and install a 35-548 terminator at the end of the DMA bus.

1.3.2 Models 3240 and 3250XP Processors

The SELCH can be installed in chassis slots 1, 3, 4, 5 or 7 of the DMA bus. The DMA bus starts at slot 7 of the I/O expansion chassis. The Model 3230, 3240 and 3250XP Processors can have up to four direct memory access interfaces (DMAIs) from memory. Each DMAI is connected, via two 17-503 F01 cables, to a DMA bus in an I/O chassis and can service up to eight SELCHs in a single or double I/O chassis configuration (see Figure 1-2).

1.3.3 Backpanel Wiring Models 3220 and 3240

At installation, it is necessary to cut the MUX bus wiring between the valid SELCH slot accepting the SELCH and the next higher-numbered slot on connector one (CONN1). The receive acknowledge/transmit acknowledge (RACK0/TACK0) "daisy-chain" wiring on the backpanel is rerouted according to Figure 1-3. The lower-numbered card slots in the chassis become part of the private SELCH bus on CONN1 only.



*FOR SINGLE I/O DMAI/DMA BUS OPERATION (8 CHANNELS) INSTALL TWO 35-743 DMA BUS TERMINATORS IN SLOT 0 ON BOTH CONN 0 AND CONN 1

**FOR DUAL I/O CHASSIS DMAI/DMA BUS OPERATION (16 CHANNELS) ADD TWO 17-464F01 CABLES AND REMOVE THE TWO TERMINATORS FROM THE 1st I/O CHASSIS SLOT 0 AND THE 2nd DMAI 17-503F01 CABLES

Figure 1-2 Models 3240 and 3250XP Installation DMA Bus/DMAI Interconnection

To install a SELCH in slot 4:

1. Remove all wires from CONN1, between slots 4 and 5, on pins 11 through 26, rows 1 and 2 (see backpanel map on Functional Schematic 35-732 M02 D08, Sheet 1 and Figure 1-3).

2. Remove the wire between 222-0001 and 122-0700.

3. Remove the RACK0/TACK0 jumper between pins 122 and 222 on both the CONN0 and CONN1 and RPC0/TPC0 jumper, between pins 137 and 237 on CONN0 of slot 4.

4. Connect 122-0700 to 222-0501.

5. Install the SELCH into slot 4 of the chassis. The private SELCH bus now appears on the CONN1 side of slots 4, 3, 2, 1 and 0. All slots on the CONN0 side and slots 7, 6 and 5 on the CONN1 side remain standard MUX bus slots.

   On the Model 3220 System, install 35-433 terminators at the end of every MUX and I/O bus. On the Model 3240 System, install 35-758 terminators at the end of every MUX and I/O bus.

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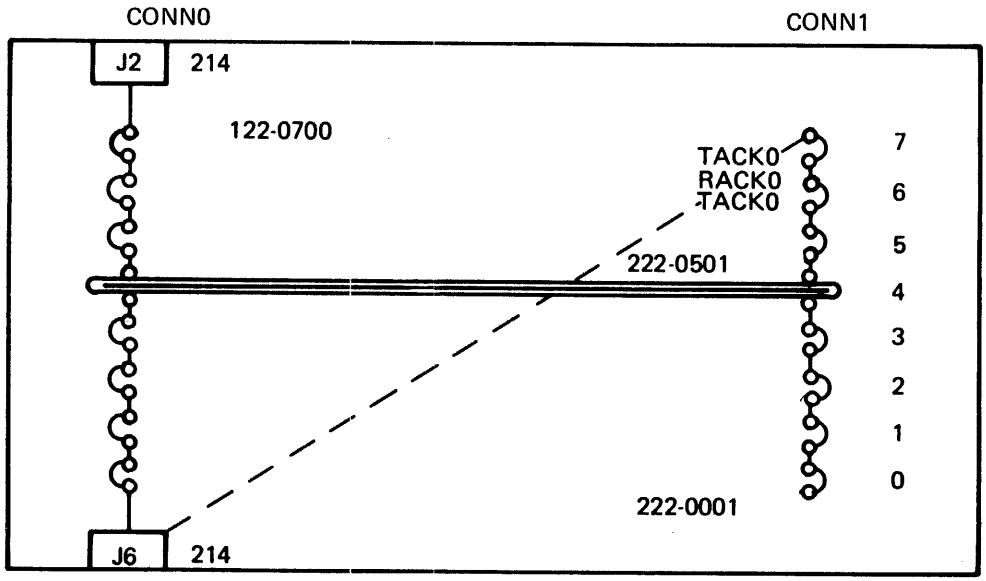
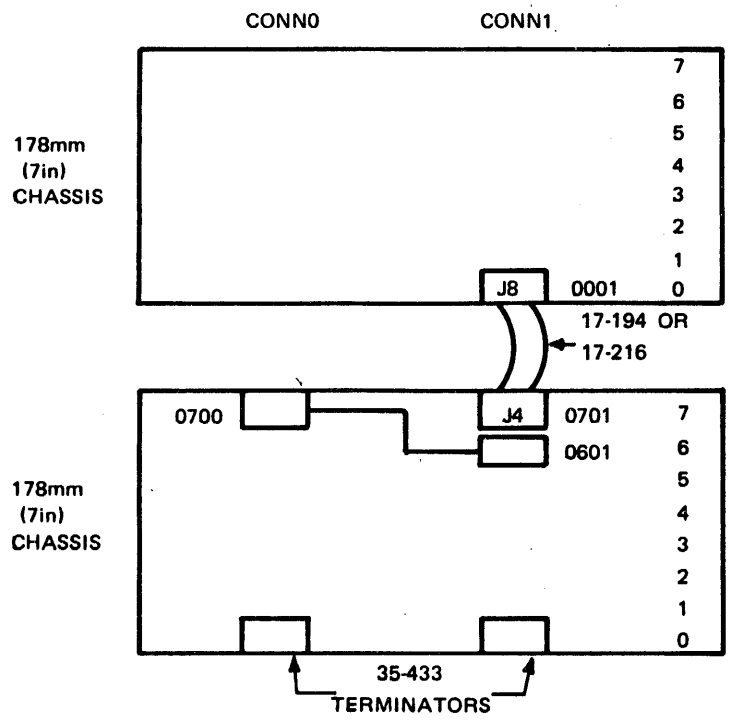


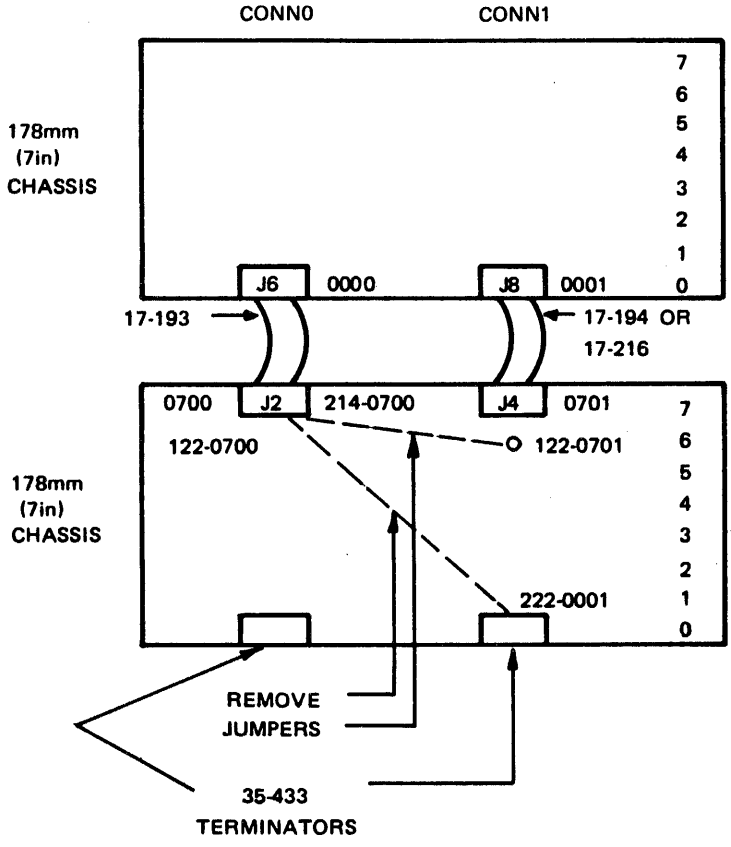
Figure 1-3 Backpanel Modification for Model 3220 and 3240 Systems

1.3.4 Cabling

Necessary cabling for the SELCH depends on the system's physical configuration. When the SELCH bus must be extended to another chassis, a number of cable configurations can be used (see Figure 1-4). Bus lengths should be minimized and should not exceed 30 inches (three expansion chassis).



CONNECTS TWO ADJACENT 178mm (7in) CHASSIS. THE PRIVATE SELCH BUS APPEARS AT BOTH CONNECTORS 0 AND 1 OF THE LOWER CHASSIS. NOTE THE DATA CHANNEL DOES NOT APPEAR IN THE LOWER CHASSIS.



USED TO CONNECT TWO ADJACENT 178mm (7in) CHASSIS. THE MULTIPLEXOR BUS APPEARS AT CONNECTOR 1. WHEN USING THIS CONFIGURATION, THE FOLLOWING WIRING CHANGES TO THE RACK0/TACK0 DAISY CHAIN MUST BE MADE TO THE LOWER CHASSIS. REMOVE 214-0700 TO 122-0701 AND 222-0001 TO 122-0700 AND ADD 214-0700 TO 122-0700.

Figure 1-4 Models 3210, 3220 and 3230 Cabling

1.3.4.1 Extended Direct Memory Access (EDMA) Bus Extension

To extend the EDMA bus to an expansion chassis on a Model 3210, 3220 and 3230 System, it is necessary to add the following wires to the expansion chassis backpanel:

- 128-0701 to 128-0604
- 227-0701 to 227-0601
- 129-0701 to all slots

1.3.5 Address Straps

The preferred address of the SELCH is X'0F0' (10-bit address). The stakes for address strapping are located on CONN3 at the front of the board (see Figure 1-5). The inner row of pins is marked 0 or 1. The outer row of pins is marked 06 through 15, corresponding to the 10 address bits. Strap each address bit to the adjacent 0 or 1 pin as desired to form the SELCH address.

1.4 SELECTOR CHANNEL (SELCH) STRAP OPTIONS

This section contains nine subsections that provide information on SELCH strap options.

1.4.1 Address Space Allocation for 1MB or 16MB (Board Location 06J) (Sheet Location 12E2)

Address space allocation for each of the four memory systems is determined from strap options on the SELCH. Each memory system's address space must be zero or a multiple of 64kB up to a maximum of 1MB or a multiple of 1MB up to a maximum of 16MB. Address assignments must be contiguous and the four memory banks are assigned address space in ascending order.

There are two 19-032 decoders on the SELCH which decode the four most significant address bits. Each output of the decoder allocates 64kB or 1MB depending on the addresses to bank decoder strapping. The 16 outputs with wire wrap stakes are marked 00 through 15. The five stakes adjacent to them are marked M00, M10, M20, M30 (for the four memory banks) and NON (for all nonexistent memory). The address space allocation should be strapped according to system configuration (see Figures 1-6 and 1-7).

1.4.2 Memory Busy or Memory Select Strapping (Board Location 07K) (12F5)

Memory busy or memory strapping information is provided in Appendixes A, B, C, D and E.

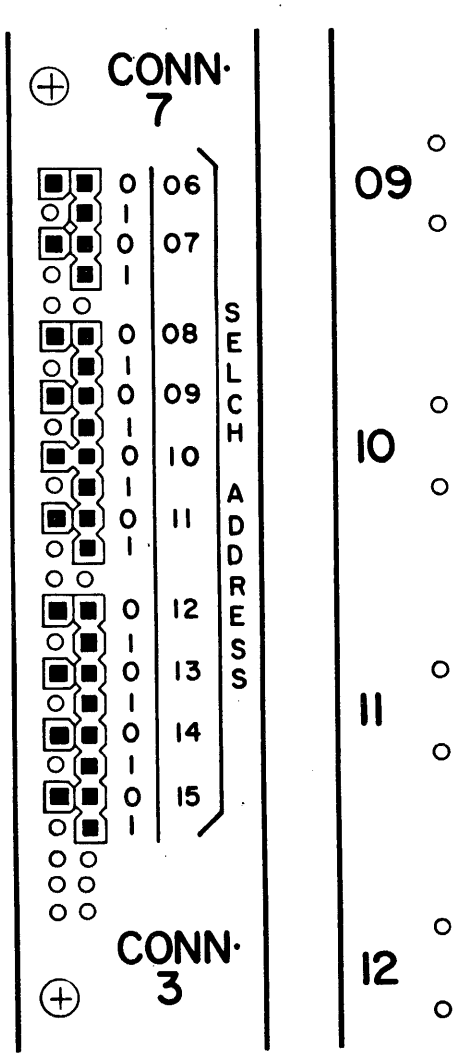


Figure 1-5 Address Strapping

1.4.3 Memory Address to Bank Space Decoders Strapping (Board Location 07H) (10M1)

This strapping determines the weight of the 16 outputs of the 19-032 decoders used in address space allocation (see Appendixes A through E).

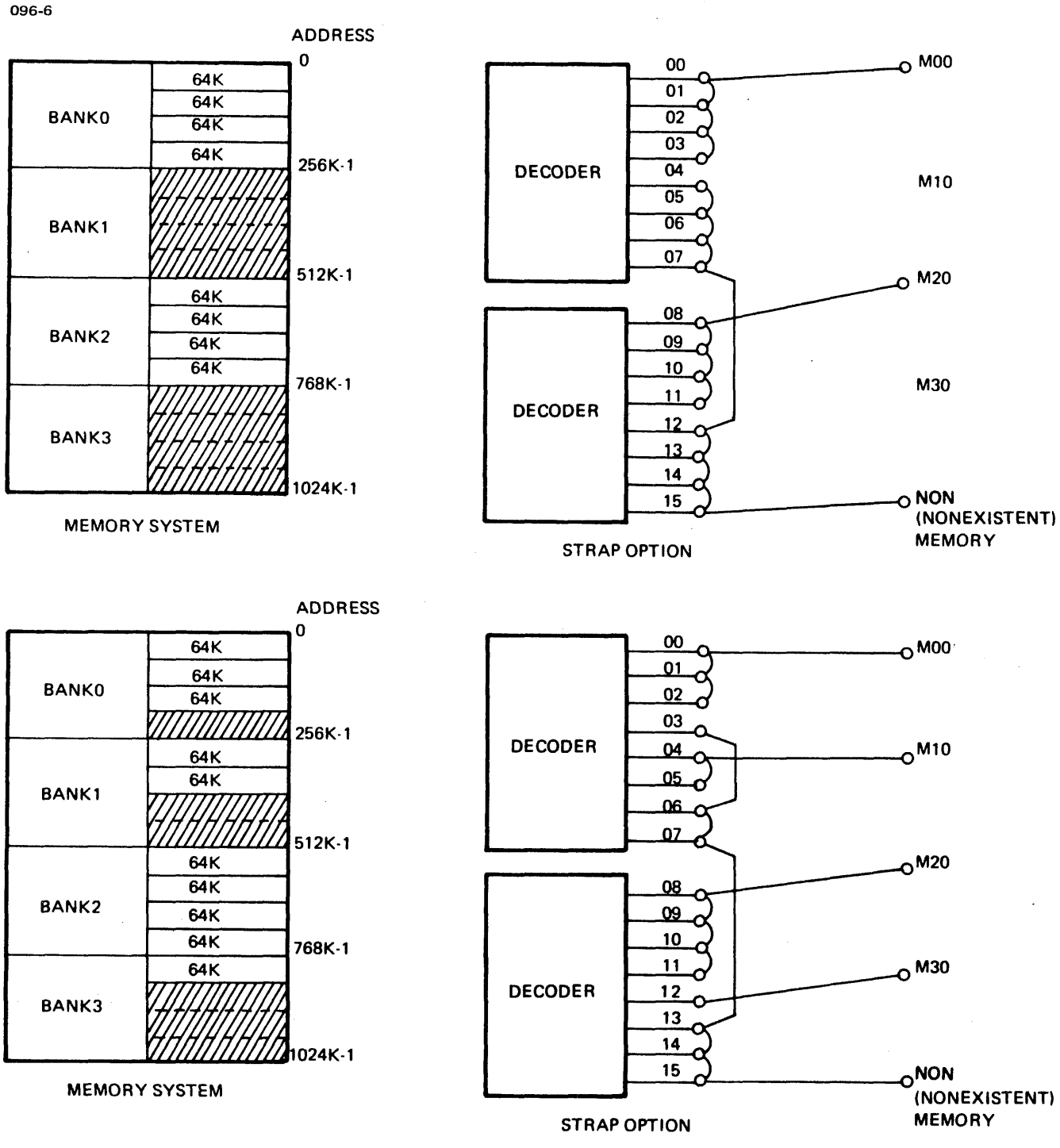


Figure 1-6 Address Allocation (1MB)

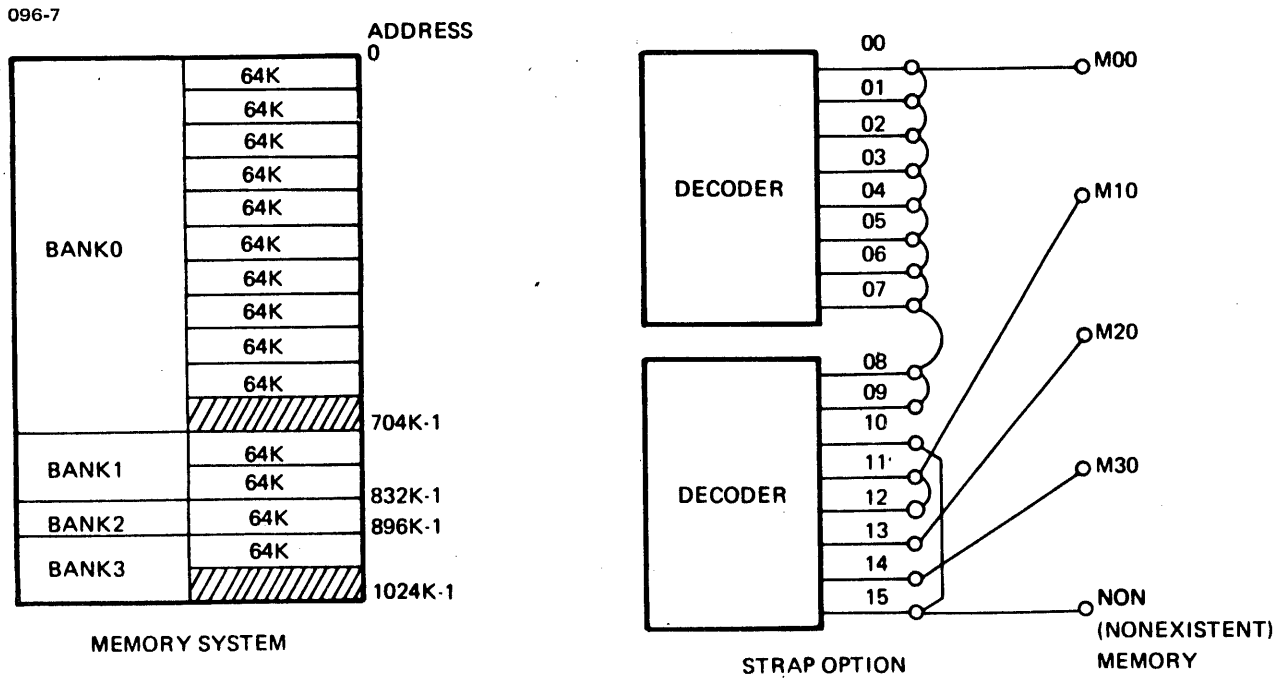
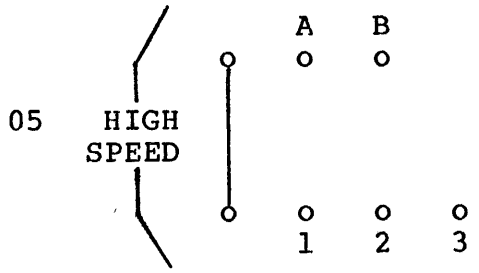


Figure 1-6 Address Allocation (1MB) (Continued)

1.4.4 High-Speed Protocol (Board Location 00A) (7M7)

The following strap allows the SELCH to eliminate the status sense before a data transfer on the private bus, if the I/O device is designed to run in this manner.

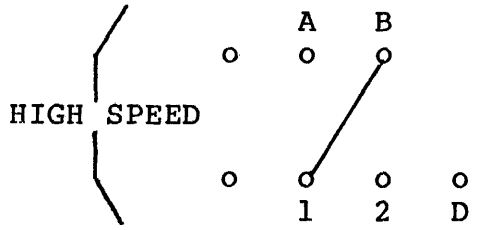


1.4.5 GADR0 Strapping

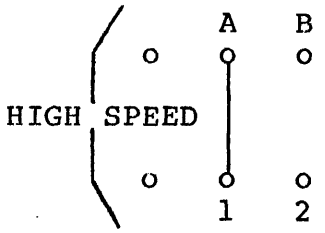
On the Model 3210, 3220 and 3230 Systems, MBSY is a bidirectional signal and the memory select lines are put in the tri-state mode (see Appendixes A through E).

1.4.6 Adjusting the Clock (Board Location 00A) (15H8)

The clock is adjusted by placing a strap from pin 1 to pin B, putting a probe on the wire wrap stake at location 001E10 and adjusting the variable capacitor at location 01E for an 80ns period.



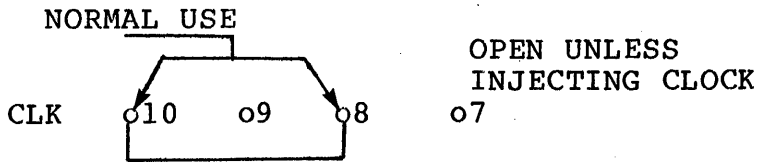
Once the clock is adjusted, the strap from pin 1 to pin B is removed and replaced by a strap from pin 1 to pin A (as shown below). This strap remains on the board.



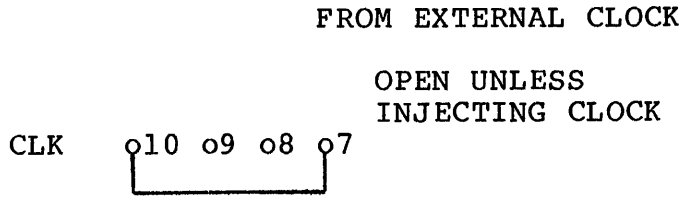
1.4.7 IM40 Strapping (Board Location 00A) (14A3)

For the Model 3210, 3220 and 3230 Systems, a strap runs from pin 2 to pin B. For the Model 3240 and 3250XP systems, a strap runs from pin 2 to pin C. See Appendixes A through E.

1.4.8 Injecting External Clock



Normally there is a strap between pin 8 to pin 10 (board number). To inject an external clock in the system, pin 7 is strapped to pin 10 and the external clock is connected to pin 8.



1.4.9 ID Bits Strapping (Board Location CONN4) (13B6)

See Figure 1-7 and Appendixes A through E for information on ID bit strapping.

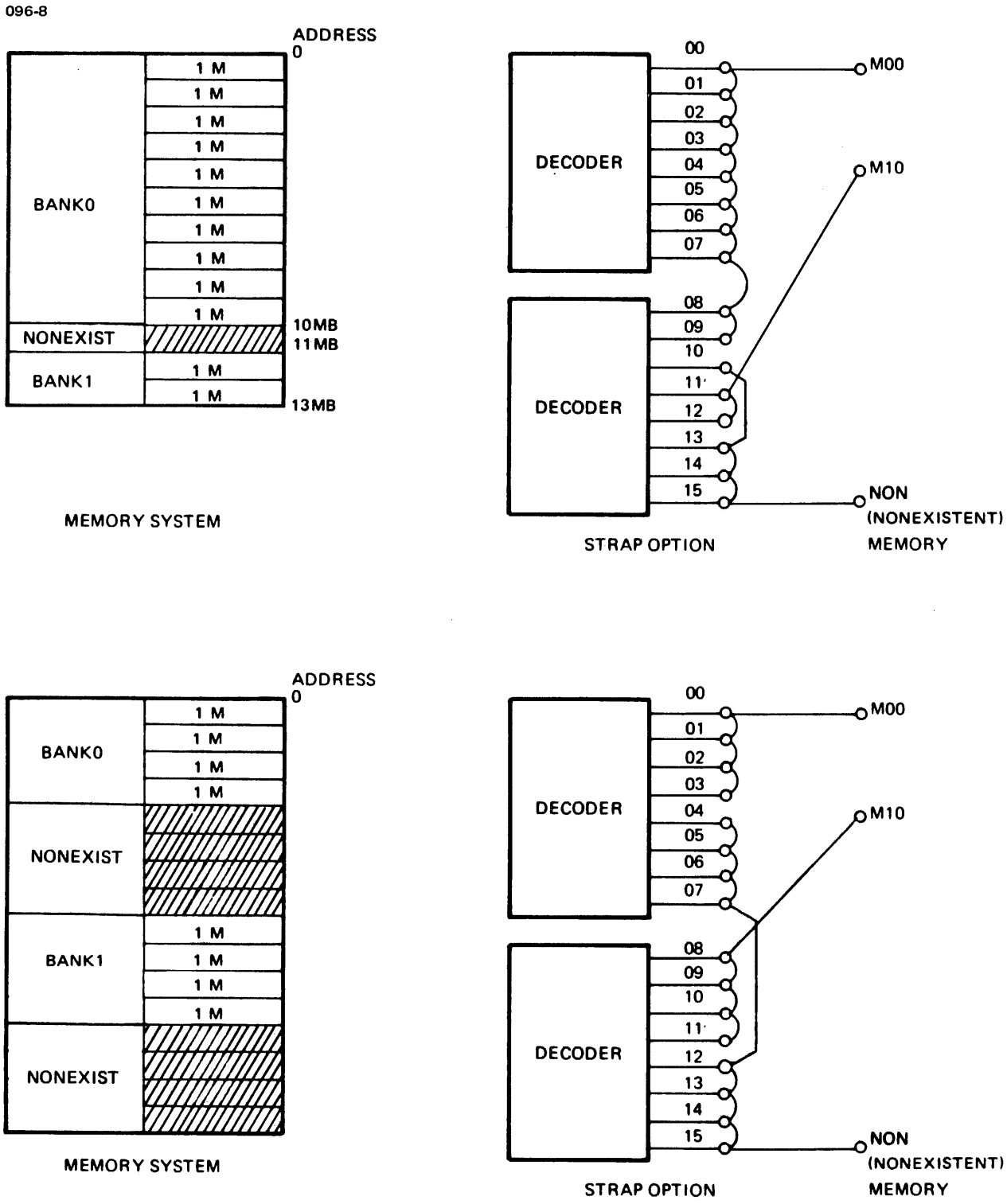


Figure 1-7 Address Allocation (16MB)

CHAPTER 2
BUS PROTOCOLS

2.1 INTRODUCTION

Figure 2-1 shows the Perkin-Elmer Series 3200 Selector Channel (SELCH) interfacing to three buses. The multiplexor (MUX) bus connects the SELCH to the processor, the private bus connects the SELCH to device controllers, and the direct memory access (DMA) bus connects the SELCH to the memory system.

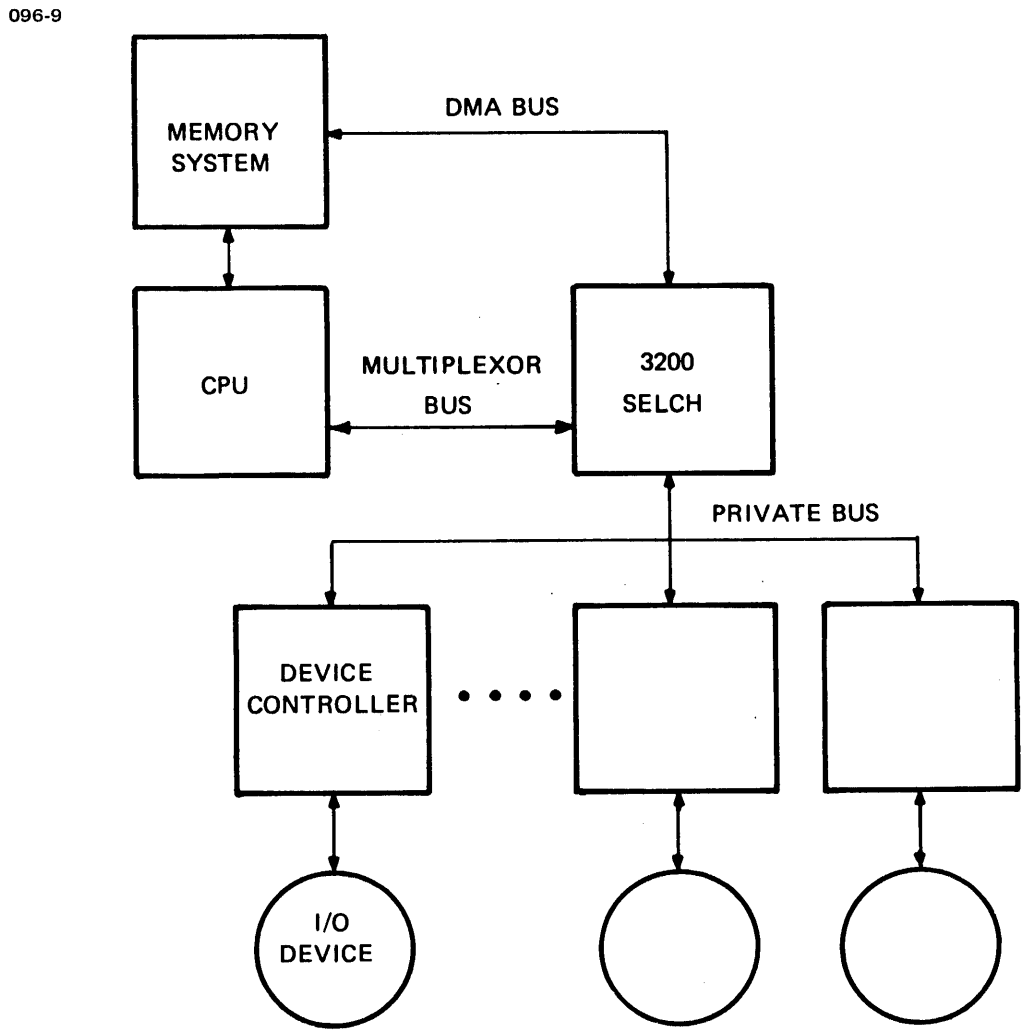


Figure 2-1 Series 3200 SELCH Interface Diagram

The MUX bus and the private bus are similar in operation but differ in mnemonic designation. The private bus has a P preceding the first letter of the mnemonic. For example, data available (DA0) on the MUX bus becomes private data available (PDA0) on the private bus. Any bus that uses the MUX bus protocol can be referred to as an input/output (I/O) bus.

The DMA bus provides direct memory access between the SELCH and memory.

2.2 SCOPE

This chapter covers the operation and signal definition of the I/O bus, the MUX bus, the private bus and the DMA bus.

2.3 INPUT/OUTPUT (I/O) BUS CHARACTERISTICS

The MUX (I/O) bus is the primary data/control channel between the processor and the system I/O devices. The processor initiates, monitors and responds to all system I/O devices via MUX (I/O) bus operation sequences. Data transfers between the processor and the system I/O devices can either be performed directly by the processor over the MUX (I/O) bus, or controlled indirectly by the processor, using a DMA data transfer device such as the SELCH.

2.3.1 Input/Output (I/O) Bus Operations

All sequences on the MUX bus consist of at least two operations; a device address and data/command/status are multiplexed onto one physical set of data lines. There are six types of operations that occur on the MUX bus:

1. Address selects the desired I/O device.

2. Command transfers a command byte from the processor to the selected I/O device. The command byte is the primary element for control of I/O devices by the processor.

3. Status transfers a status byte from the selected I/O device to the processor. The status byte is the primary element for interrogation/monitoring of the I/O device by the processor.

4. Data available (data byte/halfword) transfers an 8-bit data byte or 16-bit data halfword from the processor to the selected I/O device.

5. Data request (data byte/halfword) transfers an 8-bit data byte or 16-bit data halfword from the selected I/O device to the processor.

6. Interrupt/acknowledge transfers the address of an interrupting I/O device to the processor.

2.3.2 Input/Output (I/O) Bus Definitions

The I/O bus is a byte or halfword-oriented I/O system which communicates with a maximum of 1,023 peripheral devices. The I/O bus consists of 27 signal lines: 16 bidirectional data lines, 7 control lines, 3 test lines and an initialize line. Table 2-1 shows the signal lines in the I/O bus.

NOTE

All the signal lines listed in Table 2-1 are applicable to private I/O buses generated by the I/O system. Each signal mnemonic on the private bus has a P prefix for identification.

TABLE 2-1 MULTIPLEXOR BUS SIGNAL LINES

TYPE	MNEMONIC	DIRECTION PROCESSOR ⟷ DEVICE	NUMBER
Data lines	D000:150	⟷	16 lines
Control lines	ADRS0	→	1 line
	SR0	→	1 line
	DR0	→	1 line
	DA0	→	1 line
	CMD0	→	1 line
	RACK0	(daisy-chain) →	1 line
	CLO70	→	1 line
Test lines	SYN0	←	1 line
	ATN0	←	1 line
	HW0	←	1 line
Initialize line	SCLR0	→	1 line

2.3.2.1 Data Lines

This brief section provides a description of the 16 data lines on the I/O bus.

- D000:150

  The 16 low-active data lines (D000 through D150) are used to transfer, in parallel, an 8-bit byte or 16-bit halfword of data between the I/O bus source and the device controller. In the case of an 8-bit data byte, the data byte is transferred on the least significant eight data lines (D080 through D150). The data bus is located on backpanel pins 111 through 218.

2.3.2.2 Control Lines

The 7 control lines on the I/O bus are defined in this section.

- Address (ADRS0)

  This low-active control line is activated by the I/O bus source to all device controllers. It is accompanied by an 8- or 10-bit device address on the data lines, to select one device controller for subsequent I/O transfers (backpanel pin 219).

- Status Request (SR0)

  This low-active control line is activated by the I/O bus source to the previously selected device controller. The device controller gates its status byte onto the data lines (backpanel pin 119).

- Data Request (DR0)

  This low-active control line is activated by the I/O bus source to the previously selected device controller. The device controller gates a byte or halfword of data onto the data lines (backpanel pin 120).

- Data Available (DA0)

  This low-active control line is activated by the I/O bus source to the previously selected device controller, accompanied by a byte or halfword of data on the data lines (backpanel pin 221).

- Command (CMD0)

  This low-active control line is activated by the I/O bus source to the previously selected device controller, accompanied by a command byte on the data lines (backpanel pin 220).

- Interrupt Acknowledge (RACK0)

  This low-active control line is activated by the I/O bus source to the device controllers in a serial "daisy chain" fashion. The first device controller in the priority chain having an interrupt pending (as RACK0 is received) inhibits propagation of TACK0 to lower priority devices and gates its device address onto the data lines (backpanel pins 122 and 222).

- Early Power Fail Warning (CL070)

  This low-active control line is activated by the I/O bus source to all the device controllers when a power fail condition is detected by the processor. This control line is held active until the initialize (SCLR0) signal is activated (backpanel pin 121).

2.3.2.3 Test Lines

Three I/O bus test lines are described here.

- Synchronize (SYN0)

  This low-active test line is activated by the device controller to inform the I/O bus source that the device has properly recognized and responded to a control line signal. For an address operation, SYN0 is activated only by the device controller being addressed. SYN0 is not activated by any device controller in response to the CL070 control line. For status request, data request, command and data available operations, SYN0 is activated only by the currently selected device controller (backpanel pin 123).

- Attention (ATN0)

  This low-active test line is activated by any device controller to inform the I/O bus source that the device controller has an interrupt pending. The device controller holds this test line active until it has received an interrupt acknowledge (RACK0) control line signal. Several device controllers can activate ATN0 concurrently (backpanel pin 223).

- Halfword (HW0)

  This low-active test line is activated by a halfword-oriented device controller at all times while it is addressed. A byte-oriented device controller must not activate this test line (backpanel pin 226).

2.3.2.4 Initialize Line

The single initialize line is defined in this section.

- Initialize (SCLR0)

  This low-active line is activated during a system shutdown, power up or initialization operation (backpanel pin 126).

With the exception of the serial RACK0/TACK0 line, all I/O bus signal lines are connected in parallel to all device controllers on the I/O bus. Figure 2-2 summarizes the I/O bus data line formats for each individual bus sequence.

2.4 MULTIPLEXOR (MUX) BUS PROTOCOL

Communications over the I/O bus are performed on a request/response basis.

1. The processor addresses a device controller by placing a 10-bit address on the data lines and activating the address (ADRS) control line. The device controller whose address corresponds to the 10-bit address responds by setting its address flip-flops and returning a synchronize (SYN) signal to the processor. All other device controllers reset their address (ADRS) flip-flops. Once a device controller is addressed, it remains so until another device is addressed or until the system is initialized. The addressed device controller responds to all subsequent activity on the I/O bus until another controller is addressed.

2. The processor gives the I/O instruction by placing the command on the data lines (D080:150) and activating the command (CMD0) control line. The device returns SYN0 to signify that it has received the command.

   If the I/O instruction involves transferring data from the processor to the device controller, the processor places data on the data lines and activates the data available (DA) control line. The addressed device responds with a SYN after it has received the data. The processor removes DA when it receives SYN.

3. If the I/O instruction involves transferring data from the device controller to the processor, the processor activates the data request (DR) control line. It then waits for the device controller to respond by placing a byte or halfword of data on the data lines and activating SYN. When the processor receives SYN, it accepts the data and removes the DR.

In all cases, the device controller removes the SYN whenever the processor removes the control line.

Figure 2-2 illustrates the timing for the MUX bus. These timing diagrams apply for halfword (D000:150) or byte (D080:150) devices.

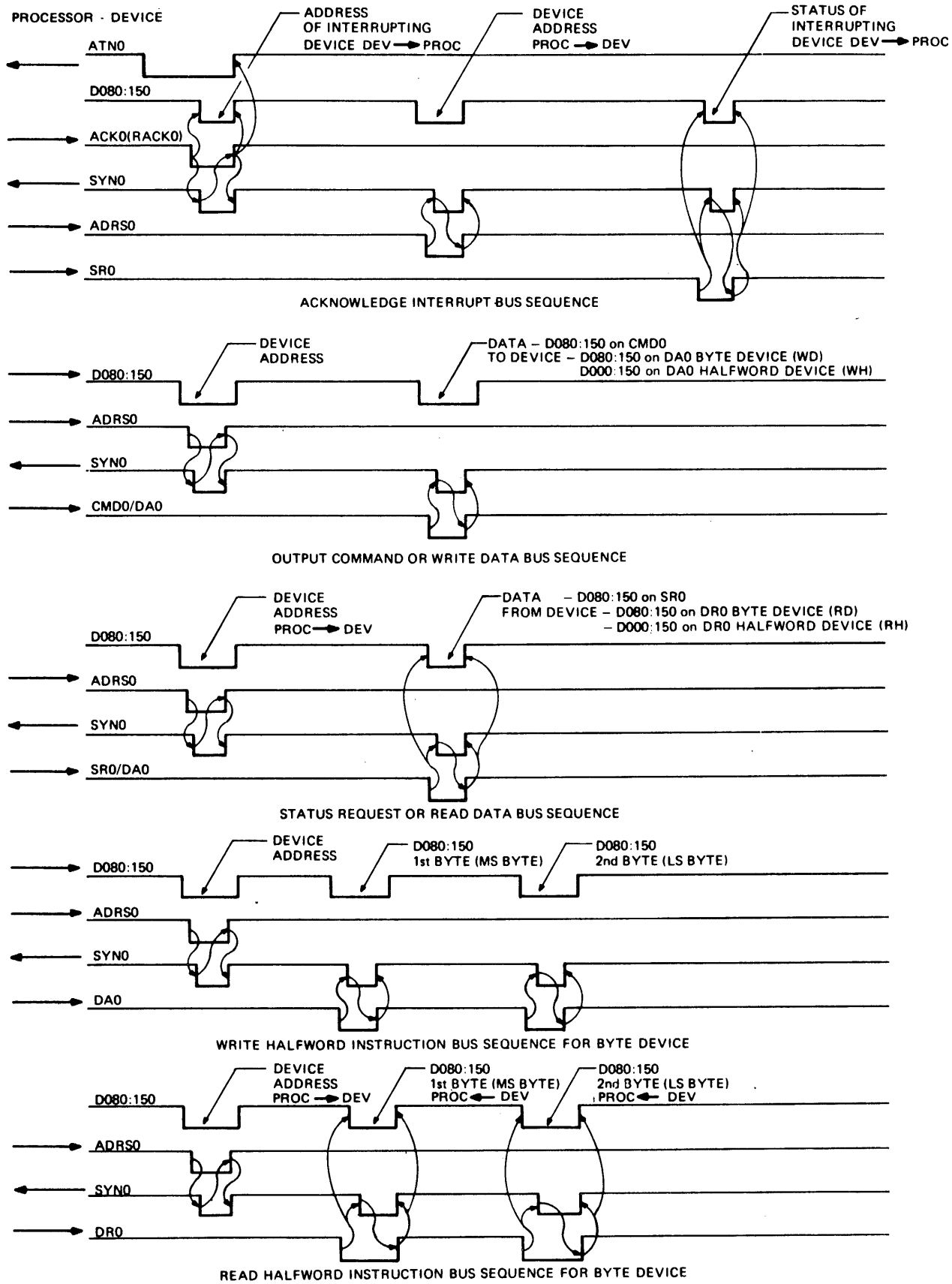


Figure 2-2 Bus Sequence for Byte or Halfword Device

2.5 PRIVATE BUS

Whenever the SELCH is idle, the private SELCH I/O bus becomes a regenerated MUX bus. When the SELCH is started (via an output command with the SELCH GO bit set to it), the SELCH bus is disconnected from the MUX bus and a special I/O handshake sequence begins, with the selected device controller on the private SELCH bus. There are two types of SELCH I/O handshake procedures, normal and high-speed. These are described in the following paragraphs. In both cases, the desired device controller is selected before the data transfer begins, by the processor performing an I/O operation (typically an output command) to the desired device controller on the private SELCH bus, then issuing an output command GO to the SELCH. As the address portion of the output command sequence to the SELCH is being performed, address match at the SELCH is used to inhibit the private SELCH bus address (PADRS0) control line. This causes the previously selected device controller to remain selected.

2.5.1 Normal Selector Channel (SELCH) Handshake Procedure

Normal SELCH handshake I/O timing is shown in Figure 2-3. As the SELCH transfer begins, the SELCH activates private status request (PSR0) to the selected device controller. The controller responds by gating its status byte onto the private SELCH bus data lines and then activating private SYNC return (PSYN0). BSY (bit 12 of the status byte) controls the period between individual data transfers. BUSY is active at all times when the controller is not ready to transfer data. The SELCH holds PSR0 active until PD120 deactivates (indicating the controller is now ready to transfer data); until PD130, PD140, or PD150 activate (indicating bad status); or until the processor halts the SELCH.

After PD120 deactivates, a data transfer takes place; in read mode, private data request (PDR0) is activated and the controller gates a byte or halfword of data onto the private SELCH bus. It then activates PSYN0. In the write mode, the byte or halfword of data is gated onto the private data lines by the SELCH, then private data available (PDA0) is activated. The controller activates PSYN0 after it accepts the data. In both read and write modes, the state of private halfword (PHW0) controls whether a byte or halfword data transfer takes place. The selected device controller activates PHW0 if it is a halfword-oriented device; with PHW0 active, the SELCH transfers successive halfwords of data to or from the controller. With PHW0 inactive, the SELCH transfers successive bytes of data to or from the controller.

After the data transfer takes place, the SELCH continues by repeating the status check/data transfer sequence until the memory data buffer is completed or the transfer is prematurely terminated due to bad controller status.

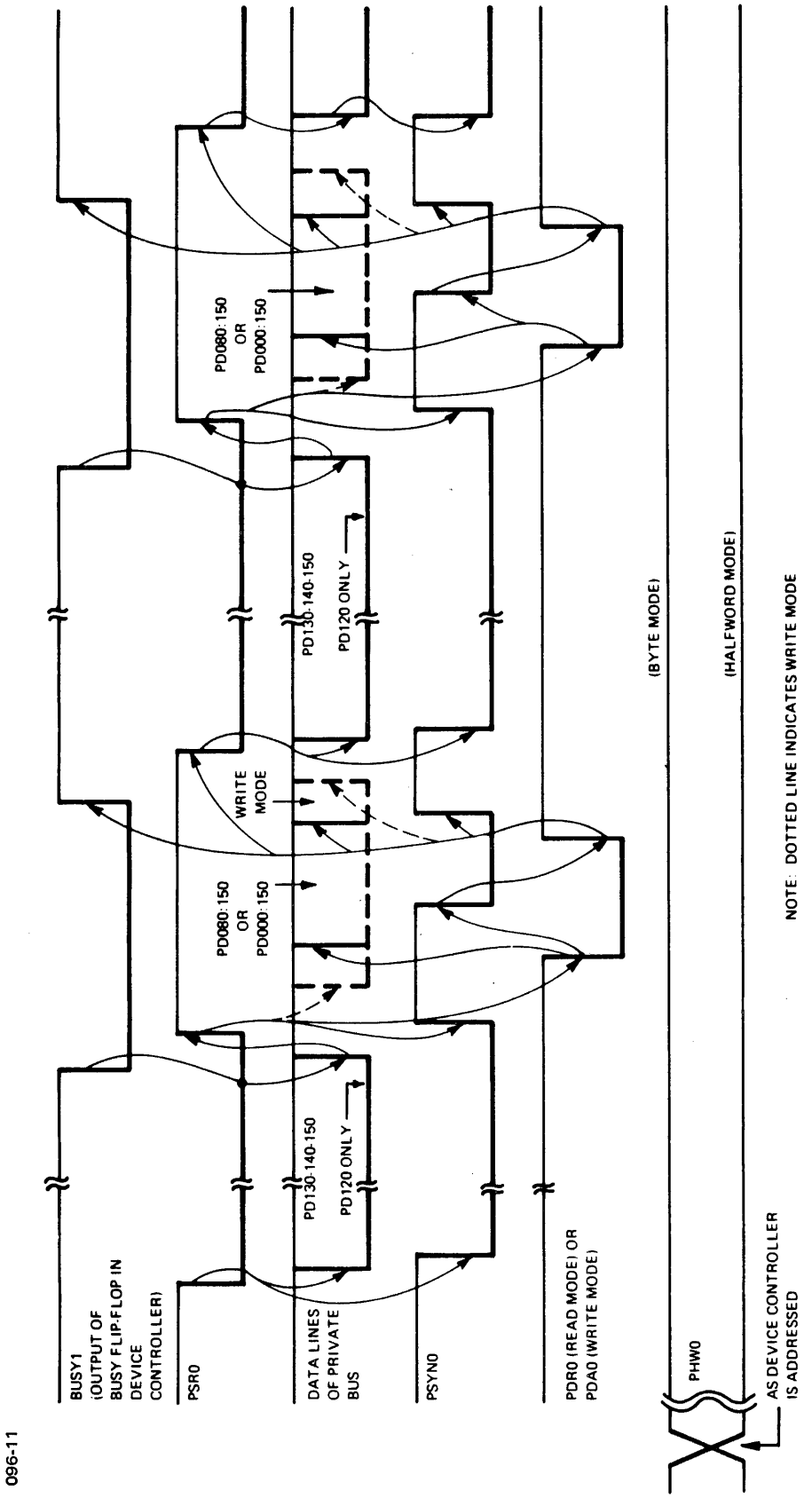


Figure 2-3 Normal SELCH Handshake Timing

Maximum data throughput can be calculated by using the following formula:

$$X = \frac{B}{.73 + 2\ (Sn + Sm)}$$

Where:

X = transfer rate in MB/second

B = bytes per DA/DR pulse

B = 1 for byte devices

B = 2 for halfword devices

Sn = SYNC return turnon delay time in microseconds

Sm = SYNC removal delay time in microseconds (Sn and Sm are measured at the SELCH PSYN0 input)

NOTE

This formula assumes no I/O switch or SCC between the SELCH and the device controller.

2.5.2 High-Speed Selector Channel SELCH Protocol

The high-speed handshake protocol supports device controllers which sustain higher throughputs than are achievable using the normal procedure. This is achieved by eliminating the status check operation and streamlining the data transfer procedure. Table 2-2 shows the three additional control/test signals required for the high-speed protocol.

TABLE 2-2 HIGH-SPEED PROTOCOL SIGNAL LINES

TYPE	MNEMONIC	DIRECTION SELCH⟷DEVICE	NUMBER
Control line	SBSY0	⟶	1 line
Test lines	SNS0	⟵	1 line
	SCHK0	⟵	1 line

- SELCH Busy (SBSY0)

  This low-active control line is activated by the SELCH to the previously selected device controller, indicating that a SELCH block data transfer is in progress. This line uses backpanel pin 224-1.

- Switch to New Sequence (SNS0)

  This low-active test line is activated by the previously selected device controller to the SELCH to specify that the controller supports the new protocol. It remains active at all times while the device controller is selected. This line uses backpanel pin 124-1.

- Status Check (SCHK0)

  This low-active test line is activated by the previously selected device controller to the SELCH to indicate the occurrence of a bad status condition (bad status = S13 + S14 + S15). This line can be activated only while either PDA0 or PDR0 is active and at least 50ns before the device controller activates PSYN0. Once activated, it must remain active until after SBSY0 deactivates. This line uses backpanel pin 225-1.

  All the control and test lines listed above are connected in parallel to all devices on the SELCH bus.

  Figure 2-4 shows the high-speed protocol data transfer timing. As a read mode SELCH transfer begins, the SELCH activates private data request (PDR0). When the device controller is ready to transfer a byte or halfword of data (as BSY1 deactivates), the controller gates the data onto the private SELCH bus, then activates PSYN0. The SELCH responds by accepting the data and deactivating PDR0, causing the controller to deactivate the private data lines and PSYN0. This handshake procedure is repeated until the data transfer terminates.

  As a write mode SELCH transfer begins, the SELCH gates the data byte or halfword onto the private data lines, then activates private data available (PDA0). When the controller is ready to accept the data (as BSY1 deactivates), the controller latches the data and then activates PSYN0. The SELCH responds by deactivating PDA0, causing the controller to deactivate PSYN0. This handshake procedure is repeated until the data transfer terminates.

  In both read and write modes, the device controller can terminate the data transfer by activating status check (SCHK0) after PDR0 or PDA0 is activated but before PSYN0 is activated (see Figure 2-5). SCHK0 must remain active until the SELCH deactivates SELCH busy (SBSY0). As in normal protocol, the private halfword (PHW0) line controls whether the data transfer is performed in byte or halfword mode.

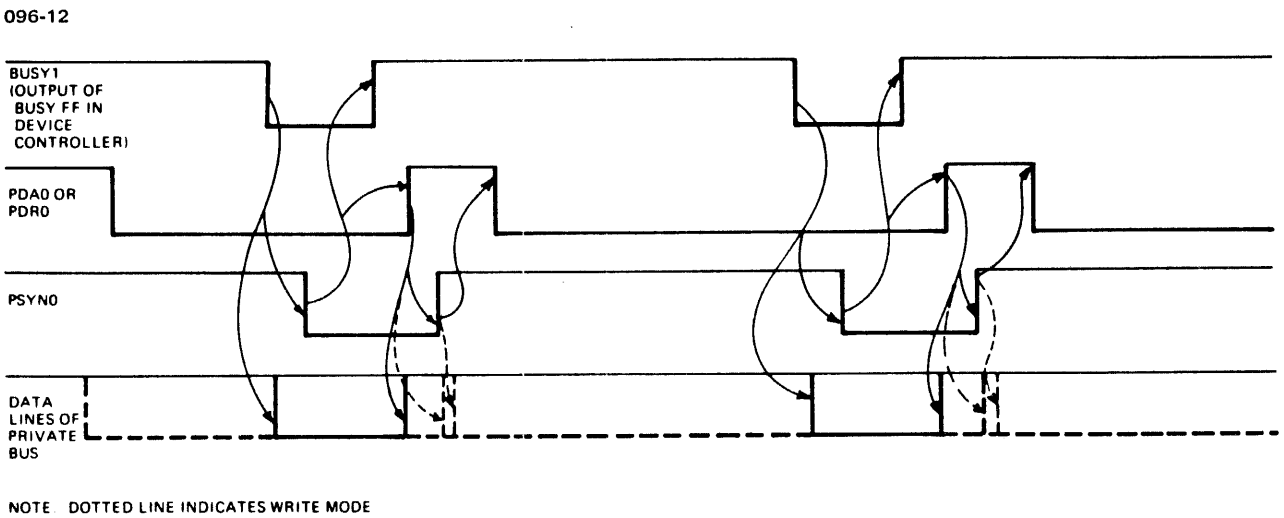


Figure 2-4 High-Speed Protocol Data Transfer Timing

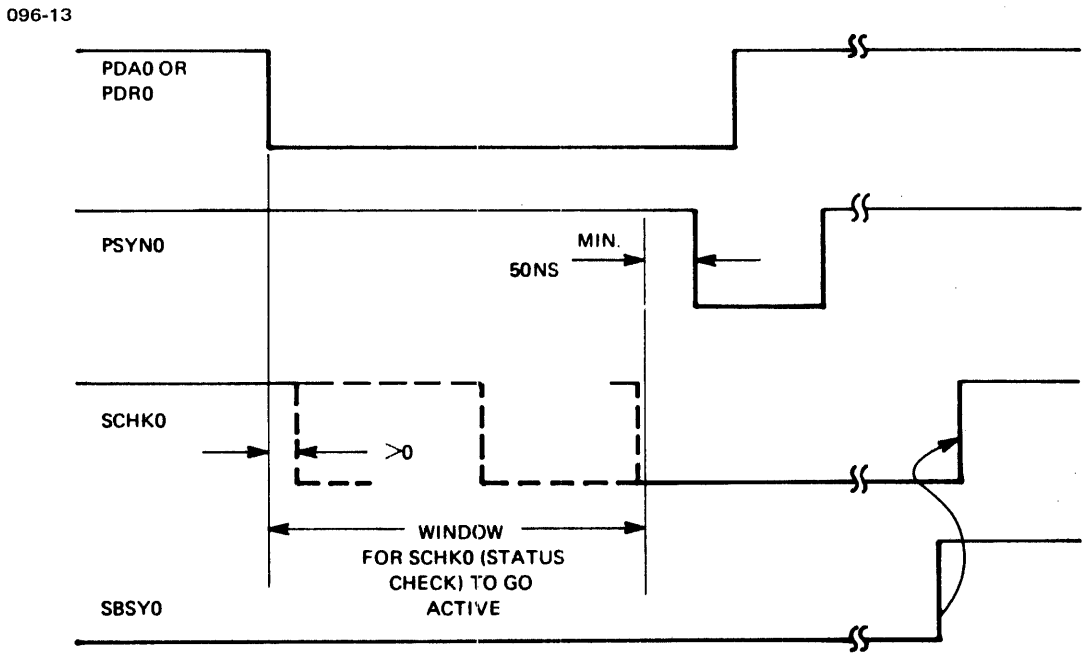


Figure 2-5 Termination of SELCH Data Transfer

Maximum data throughput can be calculated by using the following formula:

$$X = \frac{B}{.390 + 2\,(Sn + Sm) + DA}$$

Where:

X = transfer rate in MB/second

B = bytes per DA/DR pulse

B = 1 for byte devices

B = 2 for halfword devices

Sn = SYNC return turnon delay time in microseconds

Sm = SYNC removal delay time in microseconds (Sn and Sm are measured at the SELCH PSYNO input)

DA = .075 for write to device,
0 for read from device

NOTE

This formula assumes no I/O switch between the SELCH and the device controller.

2.6 DIRECT MEMORY ACCESS (DMA) BUS

The activities on the DMA bus can be broken up into three areas: bus acquisition, setup of memory system for transfer and data transfer.

The protocol for bus acquisition maximizes data rate flow by ensuring that the memory bank the SELCH intends to use exists and is not busy, before allowing the SELCH to request the bus. This ensures that the DMA bus is not tied up for a memory bank that is not ready to respond to a SELCH. Because of this bus data rate maximizing, it is imperative that the bank strapping be done correctly. When two SELCHs have a DMA bus request pending, the higher priority SELCH is granted the DMA bus. Once the SELCH is selected, it sets up the memory system with the necessary information for a data transfer; that is, a read from memory or write to memory. If it is a read from memory, the SELCH gives up the DMA bus so that the memory system can put the data on the bus. If it is a write to memory, the SELCH places the data on the DMA bus. In either case, the transfer is oriented around quadword (four 32-bit word) boundaries. DMA bus signal line definitions are listed in Table 2-3.

TABLE 2-3 DMA BUS SIGNAL LINES

TYPE	NAME	DIRECTION SELCH / MEMORY SYSTEM	NUMBER OF LINES
DATA	DMA000:150		16 lines
COMMAND	DMA160:170		2 lines
ADDRESS	DMX080:110		4 lines
ADDRESS	DMX120:150		4 lines
CONTROL	XREQ0		1 line
CONTROL	TPC0	(daisy-chain)	1 line
CONTROL	QUE0		1 line
CONTROL	SOT0		1 line
CONTROL	LMRQ0		1 line
CONTROL	LOAD0		1 line
CONTROL	ID000:020		3 lines
CONTROL	M0SEL:M1SEL*		2 lines
CONTROL	M0BZ0:M3BZ0**		4 lines
CONTROL	ANS0		1 line

* M0SEL and M1SEL are in tri-state mode on the Model 3210, 3220 and 3230 Systems.

** M0BZ0:M3BZ0 are unidirectional on the Model 3240 and 3250XP Systems (from SELCH to memory System.)

- Start of Transmission (SOT0)

  This signal grants the DMA bus to the selected SELCH.

- Local Memory Request Queued (LMRQ0)

  Used on Model 3210, 3220 and 3230 Systems to inform the processor that the SELCH wishes to use memory bank 0.

- Load (LOAD0)

  Low-active signal. When the SELCH is writing to memory, LOAD0 indicates that the halfword on DMA000:150 is valid. When reading from memory, it means to send more data.

- Identification Bits (ID000:020)

  Low-active 4-bit field that allows the memory system to identify each SELCH. When a SELCH first acquires the DMA bus and puts out the starting address, it also identifies itself with three ID bits. When the memory system transmits ANS0, the 3-bit ID field identifies which SELCH receives ANS0 for the Model 3240 and 3250XP Systems only.

- Memory Bank Select (MOSEL:M1SEL)

  Low-active 2-bit signal from the SELCH that identifies which memory bank is accessed by the SELCH.

- Memory Busy (MOBZ0:M3BZ0)

  Low-active 4-bit bidirectional line that identifies which bank is being communicated with. These lines are unidirectional on the Model 3240 and 3250XP Systems.

- Direct Memory Data Lines (DMA000:150)

  Low-active bidirectional data bus between memory system and SELCH. When transferring starting address to memory, DMA bits 000:140 are the 15 least significant address bits and DMA150 is the read/write command.

- Direct Memory Address Lines (DMX080:110)

  Low-active address lines that carry the most significant nibble (4 bits) of the 24-bit address field.

- Direct Memory Address Lines (DMX120:150)

  Low-active bidirectional and bipurpose lines. When transferring a starting address to memory system, these lines are the second most significant nibble (4 bits) of the 24-bit address field.

  When data is being received from the memory system, DMX bit 12 indicates a memory malfunction; DMX bit 13 indicates parity fail; and DMX140:150 indicates which memory bank this data is coming from.

- Request (XREQ0)

  Low-active signal that means the SELCH wishes to use the DMA bus.

- Queue (QUE0)

  Low-active signal that freezes the status of the SELCHs.

- Receive Priority Chain/Transmit Priority Chain (RPC0/TPC0)

  Priority chain that ripples down the backpanel until it reaches the first SELCH that has a request active.

- Answer Synchronize (ANS0)

  Low-active signal generated by memory when the SELCH is transferring data, to indicate it can handle more data. When the SELCH is receiving data, this signal means data is valid.

- Direct Memory Command Lines (DMA160:170)

  Low-active bits that, together with DMA150, form the 3-bit command field.

2.6.1 Direct Memory Access (DMA) Bus Acquisition

Figure 2-6 shows DMA bus acquisition.

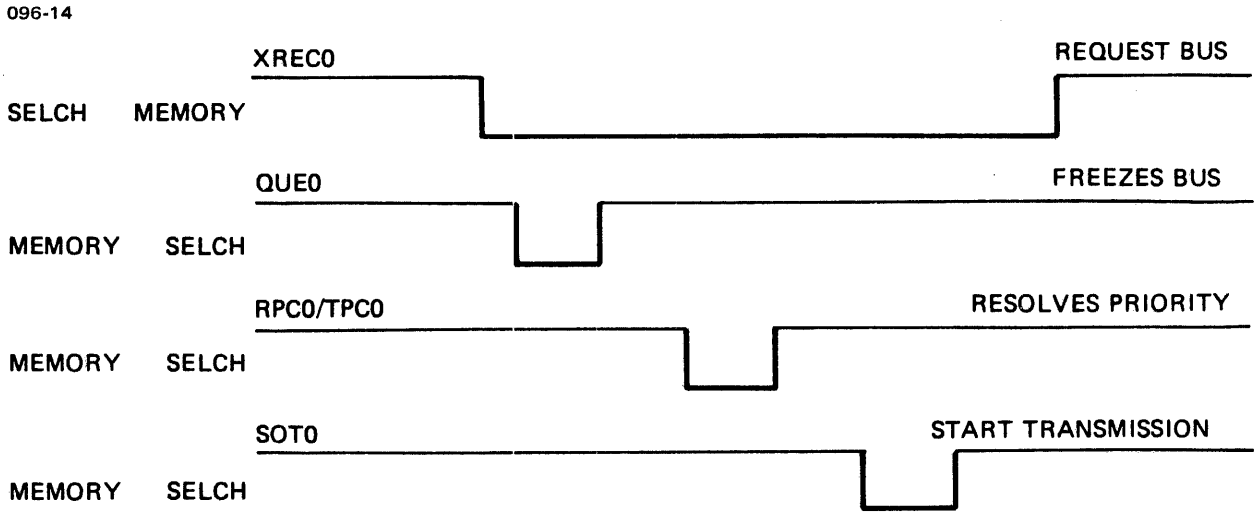


Figure 2-6 DMA Bus Acquisition

When the SELCH requires the DMA bus, it determines if the memory bank it intends to communicate with is busy. If it is not busy, the SELCH activates a request for the DMA bus (XREQ0). The XREQ0 signal is an OR-tied line that is held active as long as a SELCH intends to use the DMA bus.

When the memory system receives XREQ0, it activates QUE0, which freezes the state of all DMA bus devices.

The receive priority chain/transmit priority chain (RPC0/TPC0) is activated by the memory system. RPC0/TPC0 propagates down the backpanel in a daisy-chain fashion. The highest priority SELCH with a pending request, when frozen by QUE0, receives RPC0 and stops the TPC0 from continuing down the backpanel.

The memory system is now aware that the requesting SELCH received RPC0/TPC0. The memory system sends out start of transmission (SOT0) which gives the DMA bus to the SELCH that terminated RPC0/TPC0.

2.6.2 Memory System Read/Write

Figure 2-7 shows the memory system setup for read from memory and write to memory.

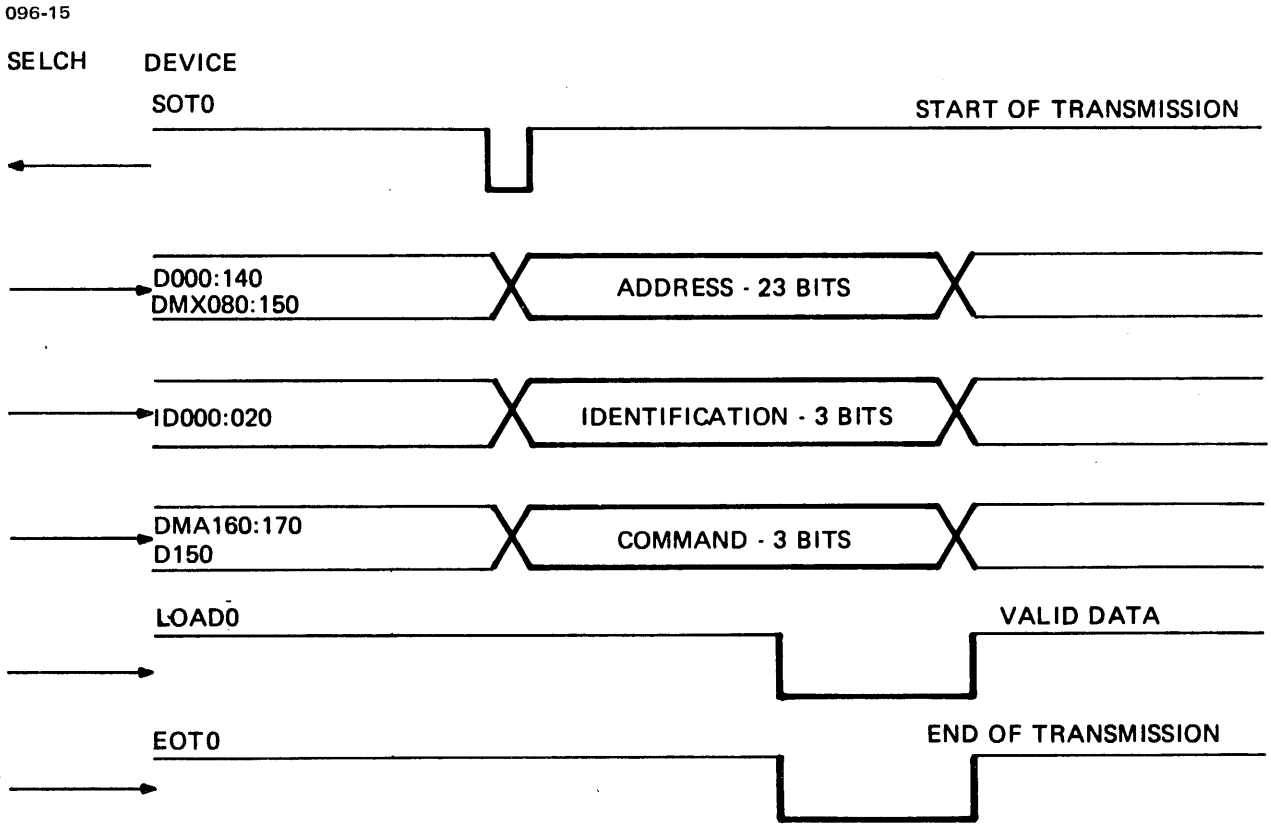


Figure 2-7 Memory System Read/Write Operation

When a SELCH receives SOT0, it sets up the memory system for a data transfer. This is accomplished by putting the starting 24-bit address, the SELCH's 3-bit ID code and the 3-bit instruction on the appropriate lines, and by activating LOAD0 (valid data). The memory system is now ready for data transfer.

If the 3-bit command is a read from memory, the SELCH surrenders the bus to the memory system by activating end of transmission (EOT0). The memory system puts the data on the bus; it can also service another SELCH and then give the original SELCH the requested data. This mode of operation is called deferred response and is transparent to the user. Deferred response allows a second SELCH to use the DMA bus while part of the memory system is filling up the buffer with data requested by the first SELCH. When the buffers are full and the second SELCH is off the bus, the first SELCH receives its data. Once a SELCH has asked for data from the memory system and gives up the bus, it waits until the data comes back.

If the 3-bit command is a write to memory, the SELCH puts the data on the DMA data bus and starts transmitting the data. The SELCH operates on quadword bursts (four 32-bit words). When the SELCH has finished the burst, it activates EOT0 to signal that it has finished with the DMA bus.

2.6.3 Data Transfer

The DMA bus has a 16-bit data bus. The normal mode of operation is to transfer or receive a four fullword burst in eight 16-bit transfers. The only exception is when the starting or the ending address of a burst does not fall on a quadword boundary (see Figure 2-8).

When the beginning address does not fall on a quadword boundary, the SELCH automatically lines itself up on quadword boundaries. For example, if the starting address is X...X6, the SELCH transfers or receives one halfword and surrenders the bus. After it requests and is granted the bus, the starting address is X...X8. Because this address is on a fullword boundary, the SELCH transmits a burst of two fullwords. At the end of the two-word burst, the address is at X..X(X-1) 0 and all subsequent bursts, except the last one, are quadword bursts (see Figure 2-9).

If the final address does not end on a quadword boundary, the SELCH terminates in a similar manner on quadword boundaries. For example, if the final address is XX...X8, and the SELCH is eight halfwords from completing its entire data transfer, the SELCH performs a burst of two fullwords and then gets off the bus. The address is XX...X6 and, after requesting and receiving the DMA bus, the SELCH transfers/receives the last halfword; the memory address then matches the final address.

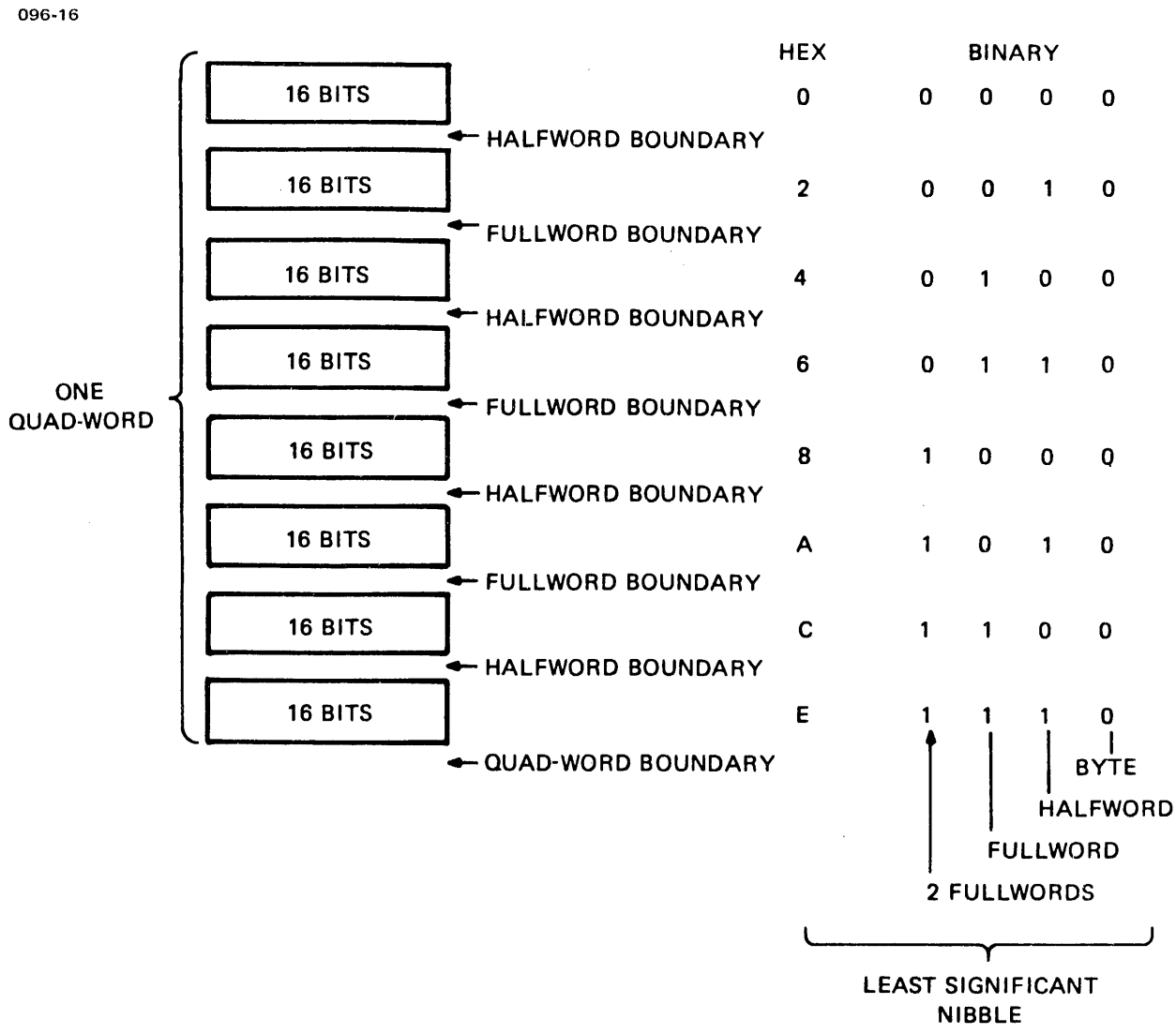
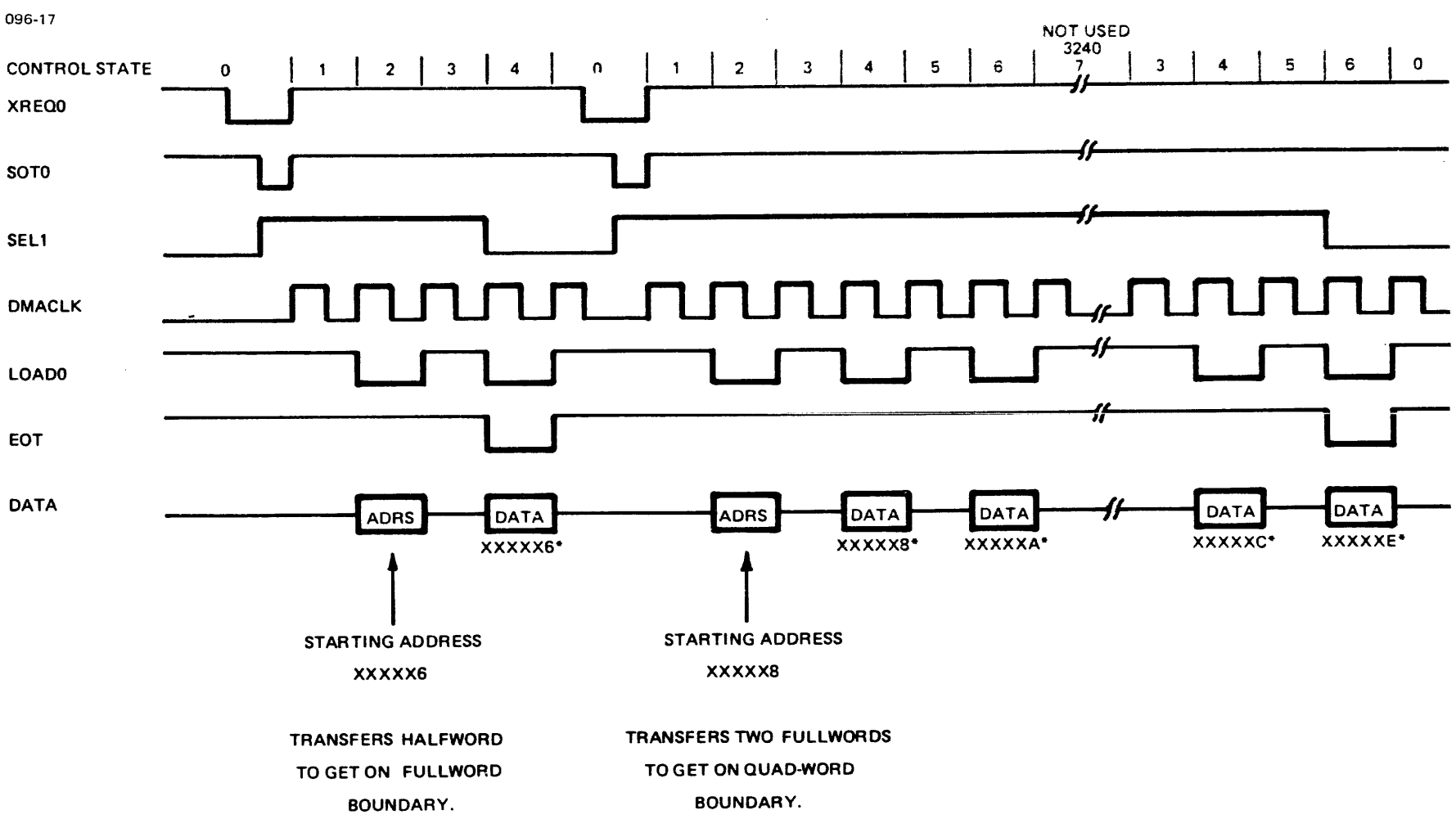


Figure 2-8 Quadword Boundary



*MEMORY LOCATION THAT DATA WILL BE TRANSFERRED INTO.

Figure 2-9 Write Data Transfer not on Quadword Boundary

CHAPTER 3
DATA PATHS

3.1 INTRODUCTION

This chapter covers the selector channel (SELCH) data paths in the idle mode, the loading and unloading of the address registers and the memory read and write.

3.2 IDLE MODE

The Perkin-Elmer Series 3200 SELCH in the idle mode acts as a bus buffer for the multiplexor (MUX) bus. The SELCH is in the idle mode after initialization or after any input/output (I/O) instruction to the SELCH is executed while not busy. It is characterized by the state of the following control flip-flops.

The SELCH address (AD1) flip-flop is reset (5J2), the busy (BSY1) flip-flop is reset (7N7) and the MUX SELCH (MSC1) flip-flop is set (7N8) (see Functional Schematic 35-732M02D08).

Figure 3-1 shows that when the SELCH is idle, the MUX bus is tied to the private bus. This is accomplished by the idle mode control flip-flops. The control line gate (CLG1=MSC1) (AD0) (6C7), when active, gates the MUX bus control lines to the private bus control lines. When CLG1 is not active, the control lines generated by the SELCH are gated with the private bus.

The data paths of the idle SELCH are referred to as the most significant byte and least significant byte. Figure 3-2 shows the most significant byte. These bits are almost exclusively used for data transfer with a halfword I/O device; the only exception is that bits DO60 and DO70 are used to return the SELCH address's two most significant bits (MSBs).

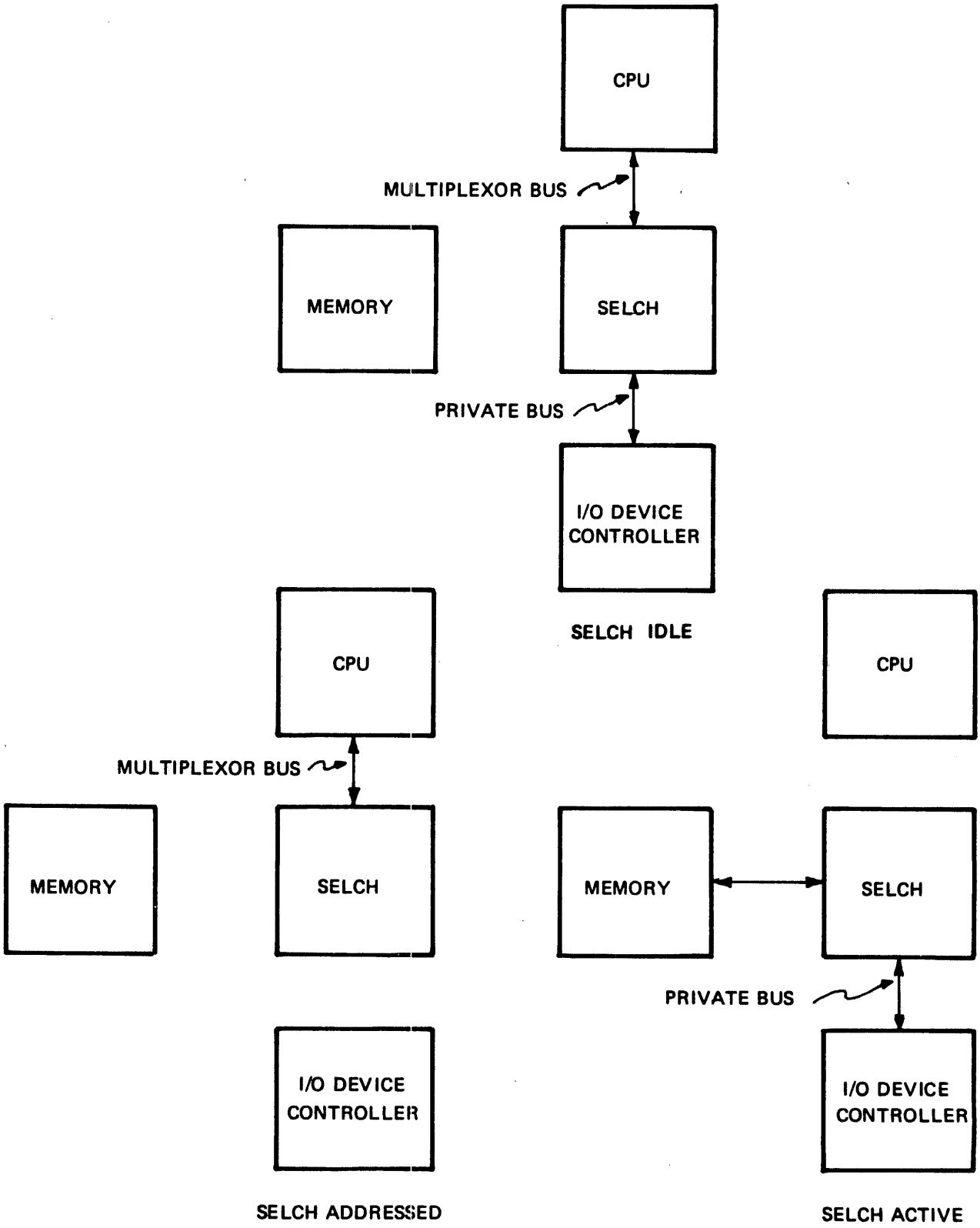
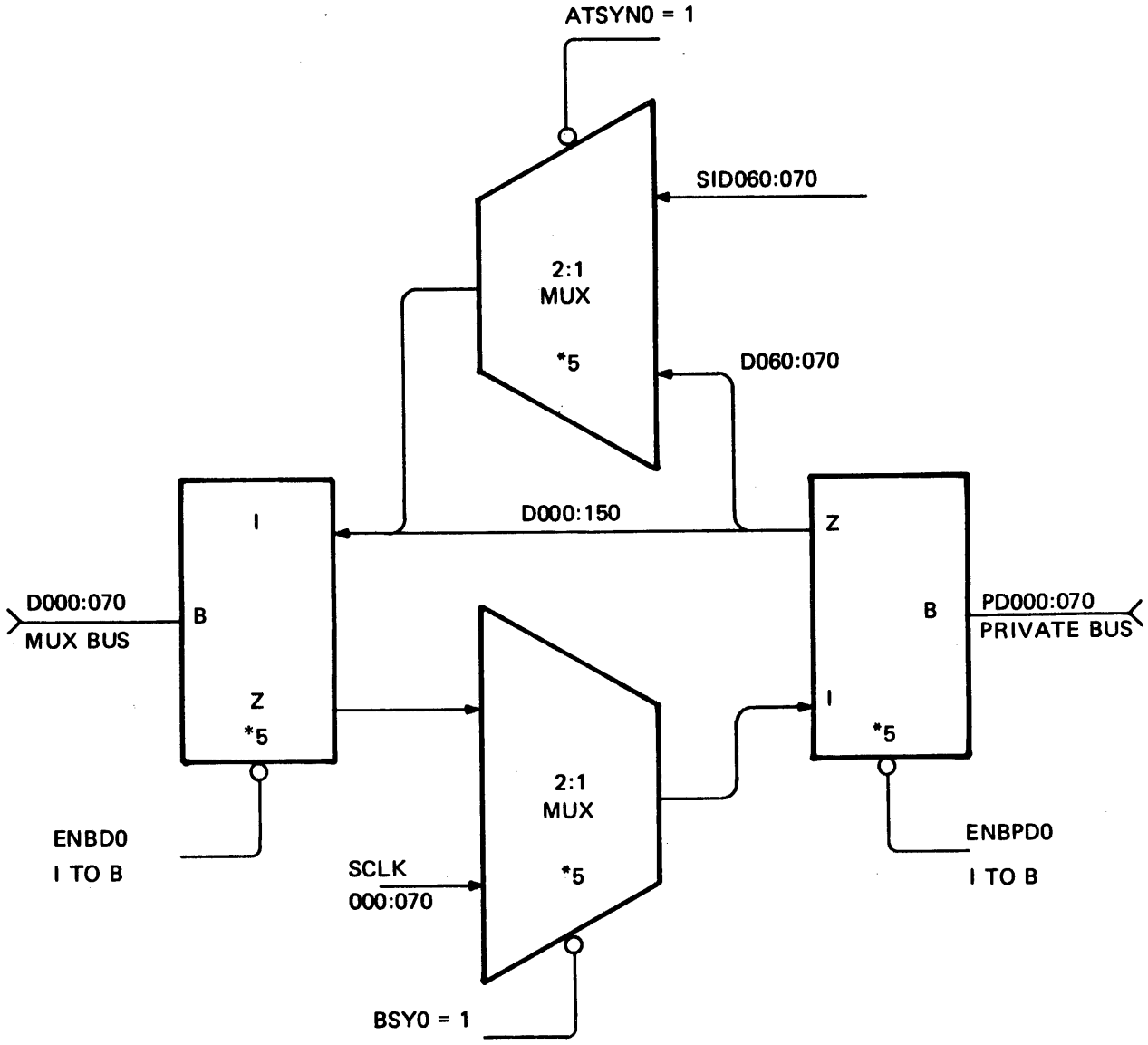


Figure 3-1 SELCH Bus Interface



*FUNCTIONAL SCHEMATIC SHEET NUMBER

Figure 3-2 SELCH Most Significant Byte Data Path

3.2.1 Most Significant Byte Data Path

Figure 3-2 shows the data path of the most significant byte.

If data from the MUX bus is transmitted to the private bus, ENBD0 goes inactive (high), gating the B input MUX bus to the output of the transceivers. The data (one byte), goes through the two-to-one multiplexor (MPX), which is controlled by BSY0 and is input at the I input to the private bus transceivers. (If the SELCH is busy, the stack output is vectored to the private bus.) When ENBD0 is inactive, ENBPD0 is active. This causes the data at the I input to be transmitted to the B output. The data is now on the private bus. If data is being transferred from the private bus to the MUX bus, ENBPD0 is inactive, gating the B input of the transceivers to the Z output. Six bits of the byte go directly to the MPX transceiver. The remaining two bits are vectored through a two-to-one MPX, which is controlled by ATSYN0 (interrupt request) and then to the MPX transceiver.

3.2.2 Least Significant Byte Data Path

Figure 3-3 shows the data paths of the least significant byte.

When the SELCH is not busy (idle) the MPX connects the Z port of the MUX bus transceivers with the I port of the private bus transceivers and the Z port of the private bus transceivers with the I port of the MUX bus transceivers.

The ENBD0 and ENPD0 functions are identical to those of the most significant bytes. There is an additional control signal on the MPX transceiver. In the idle mode, MSC0 equals zero; therefore, this signal is low when the SELCH is idle. When the SELCH is active, MSC0 equals one and if ATSYN0 (interrupt) or status request (SR0) goes active, the I input to the B output of the MPX transceivers is enabled.

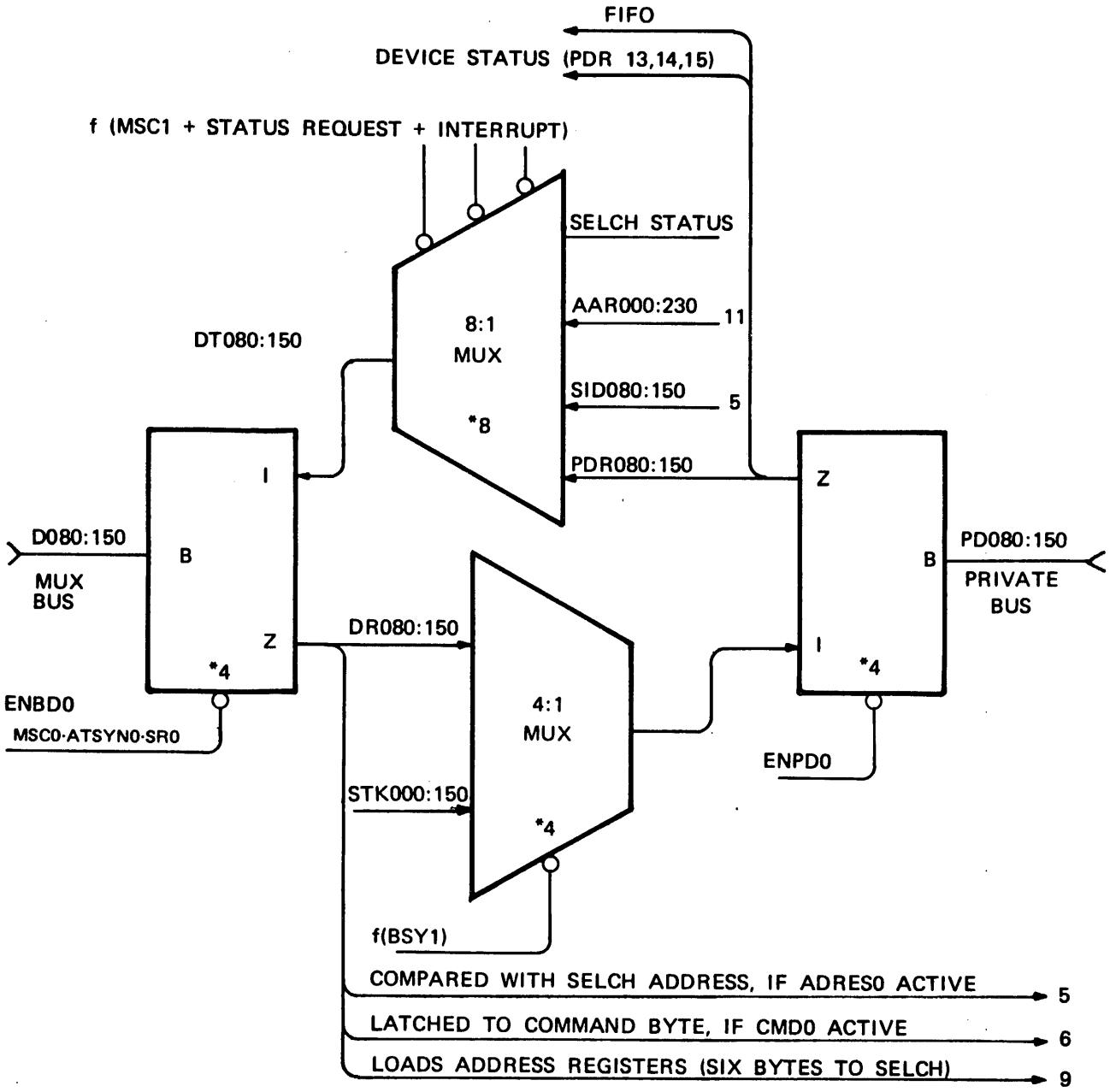


Figure 3-3 SELCH Least Significant Byte Data Path

3.3 LOADING AND UNLOADING THE ADDRESS REGISTER

In the initialization sequence from the processor to the SELCH, the starting and final address of the transferred memory block is loaded into the SELCH. The starting address is loaded into two counters, auxiliary address register (AAR000:230) and the memory address register (MAR000:230). The final address is loaded into the final address register (FAR000:230). For every transfer between the memory and the SELCH, the MAR counter is incremented and compared to the FAR. If a match occurs, the SELCH stops transferring data with the memory system. Similarly, every time data is transferred between the SELCH and the I/O device controller, the AAR is incremented and compared to the FAR. If a match occurs, the SELCH stops transferring data with the I/O device controller.

Figure 3-4 shows the data flow and control logic for the loading of the MAR, AAR and the FAR. If the transfer takes place in the lower 64kB of memory address, only four bytes are needed: two bytes for AAR/MAR and two bytes for FAR. If the transfer takes place at an address higher than 64kB, six bytes are needed: three bytes for AAR/MAR and three bytes for FAR.

The timing diagram for the loading of the registers with six bytes is shown in Figure 3-5. The processor sends the 3-byte AAR with the most significant byte first and the least significant byte last. The 3-byte FAR is sent in the same order.

Figure 3-5 and Table 3-1 show the 6-byte ripple from one register to the next on every DAG0; the only peculiarities are that the FAR000:070 register is not in series with the other registers and it is loaded directly from the fourth clock (only on the fourth DAG0 is LFARX0 active). As there are only five registers in series, the fifth clock fills the AAR with the proper address. ARLD0 inhibits the AAR counter from receiving the sixth clock. After the FAR contains the final address, and the AAR counter contains the starting address, MARCLK0 clocks in the contents of the AAR into the MAR counters.

If using only a 2-byte storing and finishing address, the same sequence is used except that only four bytes are read in and PGO0 zeros out the most significant byte of each address.

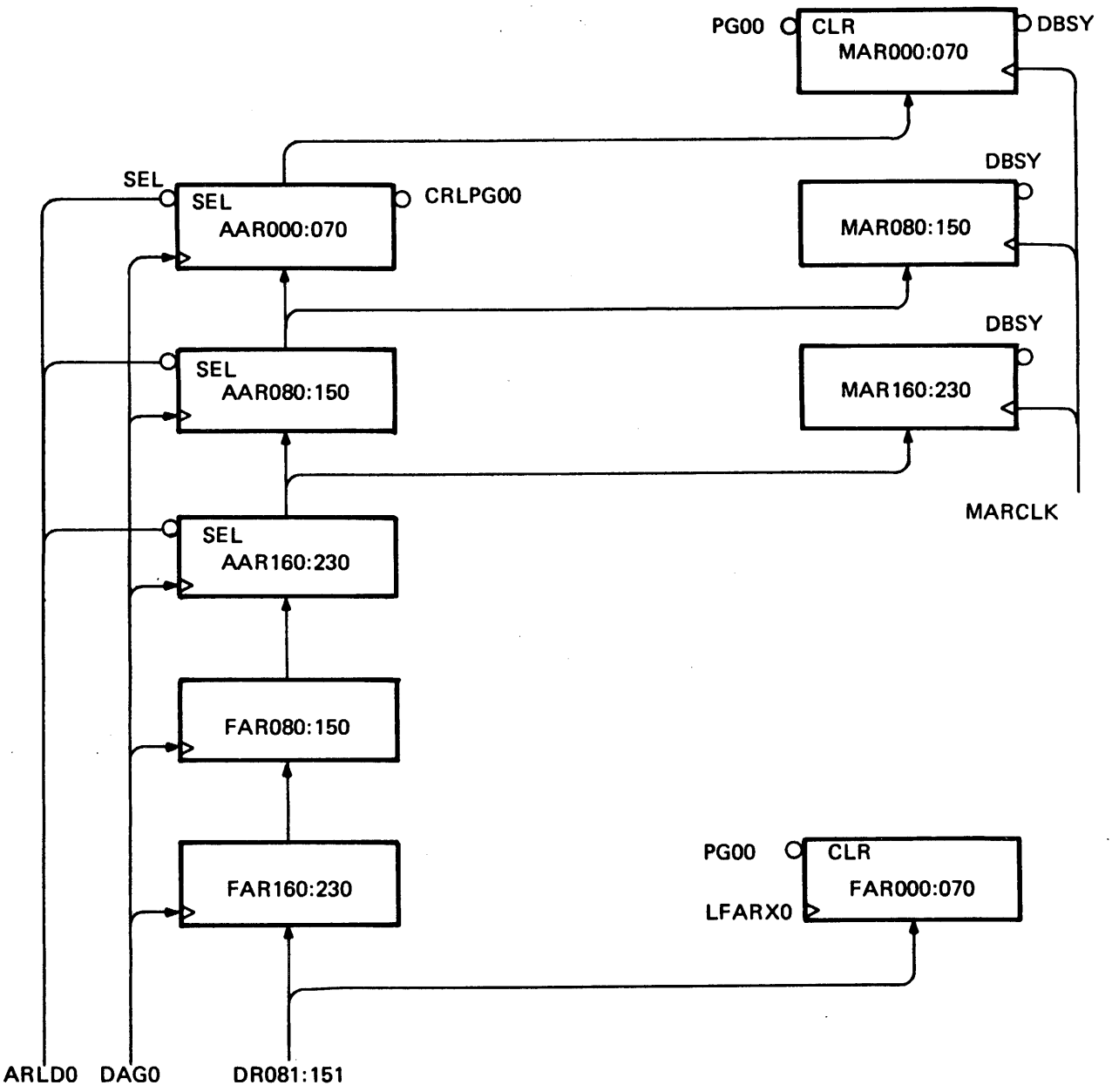


Figure 3-4 Register Data Flow

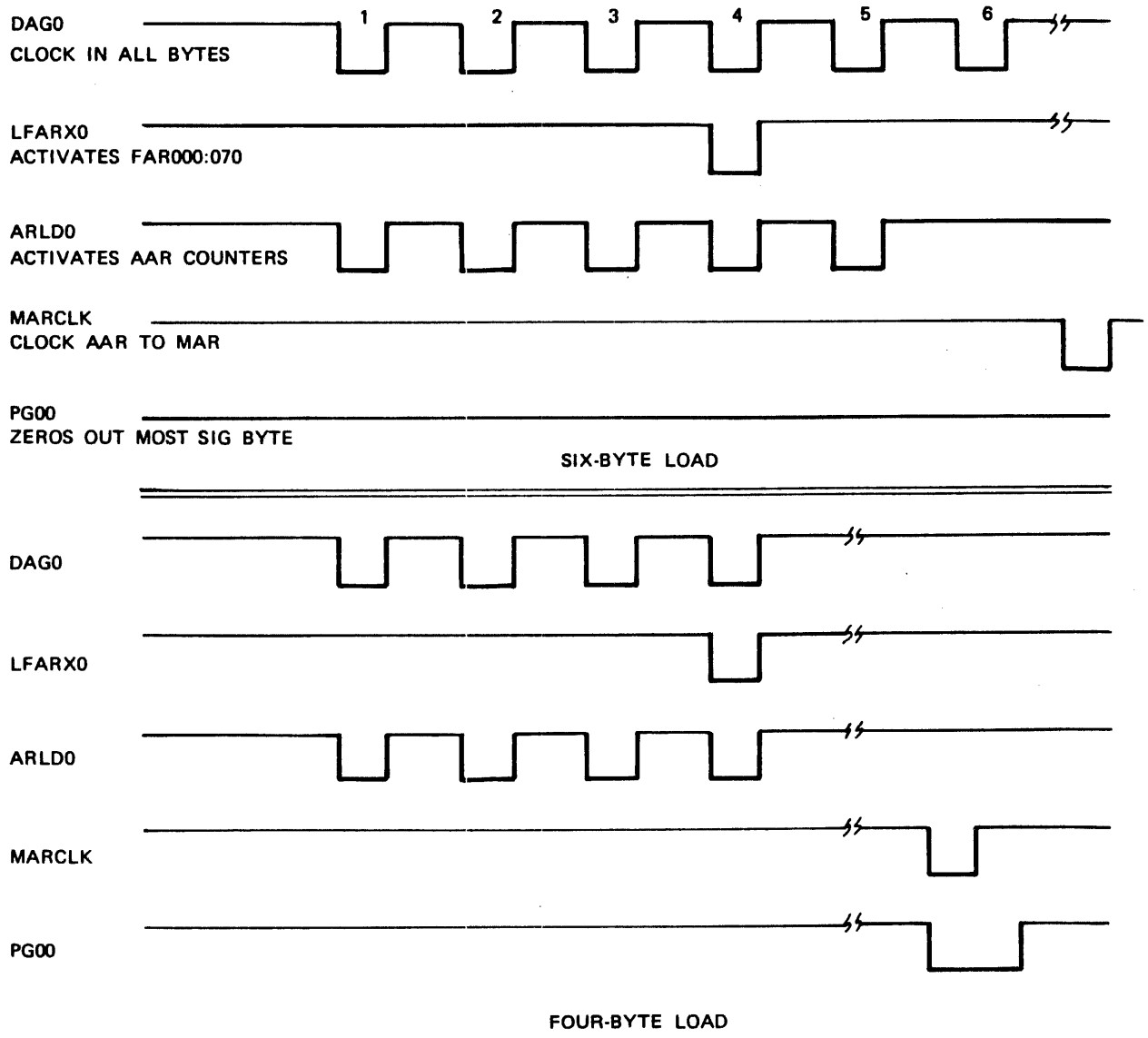


Figure 3-5 Register Loading Timing

TABLE 3-1 LOADING ADDRESS REGISTER (DATA FLOW)

BYTE	AAR000:070	AAR080:150	AAR160:230	FAR000:070	FAR000:150	FAR160:230
1	X	X	X	X	X	1
2	X	X	X	X	1	2
3	X	X	1	X	2	3
4	X	1	2	4	3	4
5	1	2	3	4	4	5
6	1	2	3	4	5	6

3.4 MEMORY WRITE

During a memory write operation, the basic data flow is from the private bus to the first-in/first-out (FIFO) register and then to the DMA bus. The FIFO buffers the direct memory access (DMA) bus from the private bus. This allows the private bus to run in a halfword mode or byte mode and the DMA bus to run in a quadword burst mode.

Figure 3-6 shows the memory write data paths. Data from the device is on the B input to the private bus transceiver; ENPB0 is inactive (high) so the data propagates to the Z output. There are two ways data can be vectored into the FIFO (STCK) depending upon whether the I/O device is a halfword device or a byte device. If the I/O device is a halfword device, the data appears on PD000:150. ENPB0 is high (on a memory write) and the data is vectored to the Z output of the private bus transceivers. The least significant byte goes directly to the two-to-one MUX/LATCH to be latched in by LDBL0. The most significant byte goes to a two-to-one MUX. Private halfword (PHW0A) is active so the two-to-one MUX vectors the byte to the two-to-one MUX/LATCH. The most significant byte is latched in with LDBH0. LDBL0 and LDBH0 go active simultaneously.

If the I/O device is a byte device, only PD080:150 has valid data. The most significant byte is read in first and appears on the Z output of the private bus transceivers. PHW0A is now inactive and the most significant byte from the data bus appears at the inputs of both two-to-one MUX/LATCHs. LDBH0 goes active, so the most significant byte is latched into the two-to-one MUX/LATCH that held the most significant byte. Similarly, the next byte from the device, the least significant byte, appears at the input to both two-to-one MUX/LATCHs. This time LBDL0 goes active, so the least significant byte is latched into the two-to-one MUX/LATCH that held the least significant byte. From this point on, it does not matter if the I/O device is a halfword or byte device. In either case, a two-to-one MUX/LATCH holds the least significant byte and the other two-to-one MUX/LATCH holds the most significant byte.

From the two-to-one MUX/LATCH the data is loaded into the FIFO on load stack (LDSTK1). The FIFO is 16 halfwords deep. After eight halfwords have been written into the stack, there is enough data stored to send a quadword burst to memory.

GADR0 gates the starting memory address onto the DMA bus and then goes inactive to allow the eight halfwords from the FIFO to vector through to the DMA bus. Data is clocked out of the FIFO on every STCKCLK0 and latched on every DMACK0. Throughout the entire write operation, ENBDMA0 has been active allowing whatever was on the I input of the DMA transceiver to be output to the B outputs of the transceiver.

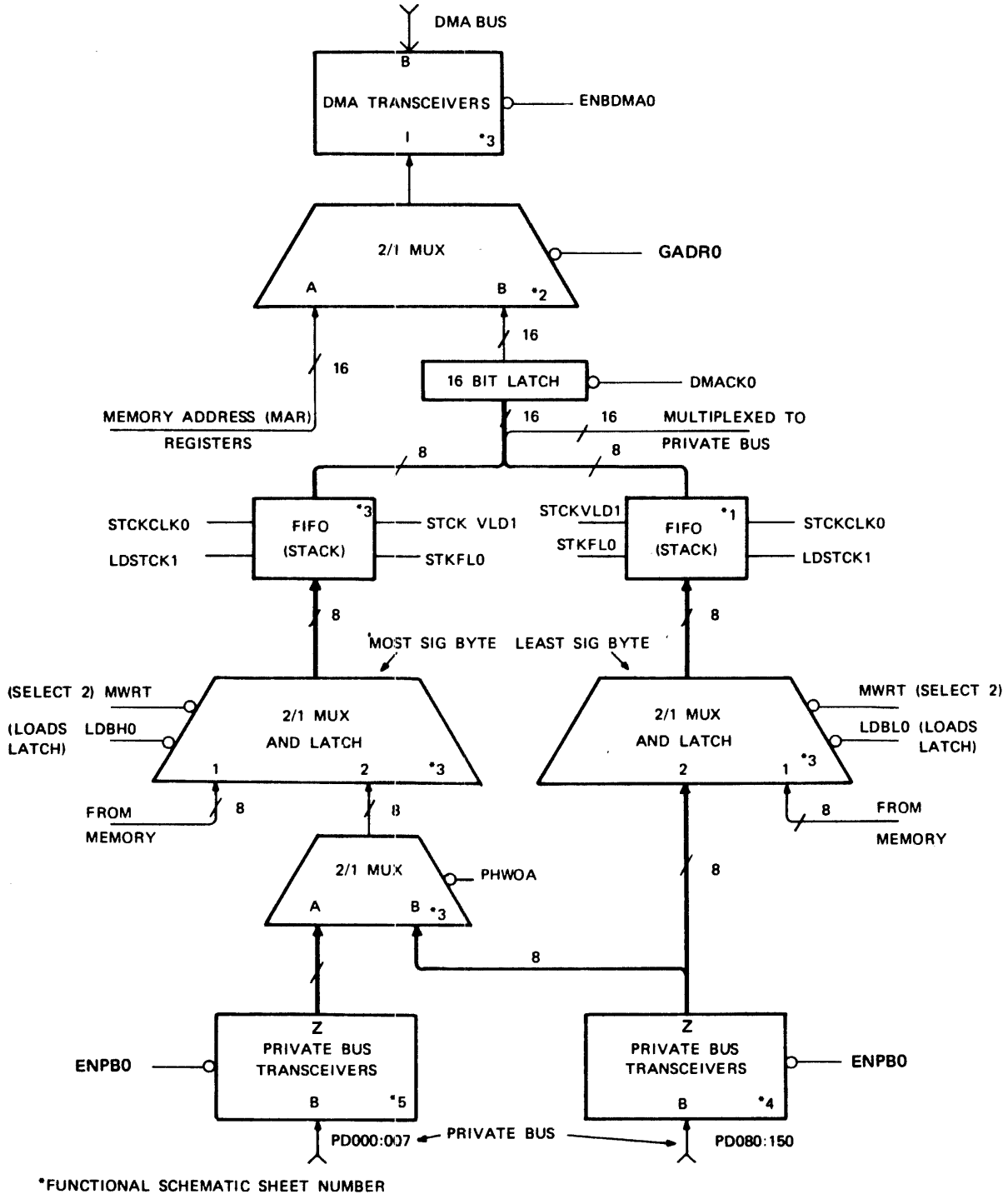


Figure 3-6 Memory Write

3.5 MEMORY READ

During a memory read operation, the basic data flow is from the memory system (DMA bus) to the FIFO and then to the I/O device (private bus). The FIFO acts as a buffer so that a quadword (16 bytes) can be read from the memory system at a fast transfer rate and then written to the I/O device at a slower speed.

Figure 3-7 shows the memory read data paths. ENBDMA0 is inactive on a memory read. Therefore, the data on the DMA bus appears at one of the inputs to the two-to-one MUX/LATCH. Memory write (MWRT) is not active so the DMA data is selected and latched when LDBH0 goes active. When load stack (LDSTCK1) goes active, the data is loaded into the FIFO. Because of the quadword operation of the DMA bus, eight halfwords are loaded in one burst. Data ripples through the FIF0 and is valid on the output a short time later. The least and the most significant bytes of data are connected to two of the inputs of a three-to-one MUX. In addition, the most significant byte is vectored over to the input of a two-to-one MUX. How the data gets to the private bus from this point is determined by whether the I/O device is a halfword device or a byte device.

In a byte I/O device, the data must be sent to the least significant byte of the private bus in 1-byte transfers, with the most significant byte first and the least significant byte second. This is done by the three-to-one MUX selecting the byte at the 1 input and, after the I/O device has read it, selecting the 2 input. The selection on the three-to-one MUX is a function of the private halfword (PHW) and BSY. The signal that does the actual storing is AAR 23, the least significant bit of the address. It toggles every time a byte is read.

In a halfword I/O device, the least significant byte is always selected by the three-to-one MUX. The most significant byte is selected on the two-to-one MUX by BSY0 inactive. Data is transmitted through the private data transceiver when ENPB0 is active.

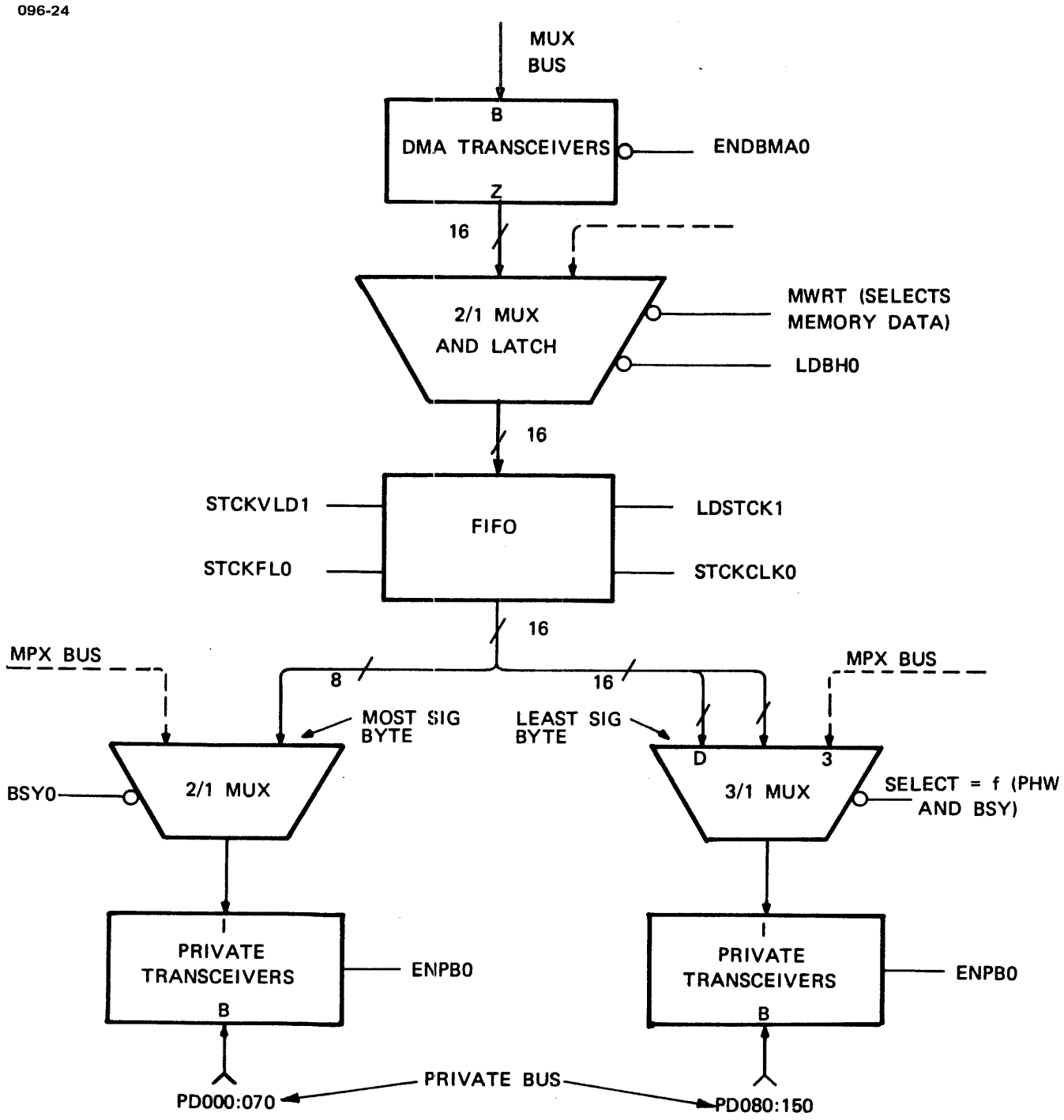


Figure 3-7 Memory Read

CHAPTER 4
MAINTENANCE

4.1 INTRODUCTION

The selector channel (SELCH) is a direct memory access (DMA) interface between input/output (I/O) device controllers and processor memory systems. Once initiated, the SELCH performs data transfers to or from the memory and the I/O device, independent of processor control. To start the data transfer, the processor sets up the I/O device controller, loads the SELCH with the starting and final addresses of the block to be transferred, the type of transfer (read or write) and issues a GO command. The SELCH then performs the data transfer without further direction from the processor. When the transfer is completed, the processor is notified by an interrupt from the SELCH.

The SELCH is complete in one 38.2cm (15in) printed circuit (PC) board and occupies one slot in a system chassis. The SELCH provides the drivers, receivers and terminators for the private SELCH bus. The private bus originates at connector 1 (CONN1) of the SELCH slot and extends to each slot below it in the system chassis. The private bus can be extended to other chassis as required.

4.2 SCOPE

This chapter describes the SELCH in its various modes: setup, memory read, memory write and termination. The multiplexor (MUX) channel bus and the DMA bus are referenced.

4.3 SELECTOR CHANNEL (SELCH) STATUS AND COMMAND BYTE

When the SELCH is addressed, it is read by the processor activating status request. If the SELCH is busy doing a DMA transfer, only the busy bit is active.

The SELCH command byte is latched in the SELCH when the processor command (CMD) control signal is received by the SELCH (command GO is not latched).

Upon termination of the data transfers, the processor is notified by an interrupt and by the inactive state of the SELCH busy bit of the status byte. SELCH status and command byte data are shown in Table 4-1. A description of each bit follows.

TABLE 4-1 SELCH STATUS AND COMMAND BYTE DATA

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE			MEMORY MAL-FUNCTION	MEMORY PARITY FAIL	BUSY			
COMMAND BYTE		EXTENDED ADDRESS READ	READ	GO	STOP	SELCH STATUS		

STATUS BYTE SIGNALS (SHEETS 7:13)	BOARD LOCATION	DEFINITION
BUSY	06D08	This bit is set by command GO. It remains set while the SELCH is in the process of transferring data. It is cleared by initialize command STOP, normal termination and error abortion. When this bit is cleared, an interrupt is generated.
MEMORY MALFUNCTION	08E05	This bit is set when the memory interface recognizes a malfunction. It is stored in the SELCH for subsequent evaluation by the processor; however, the transfer is not interrupted. It is cleared by initialize or command GO.
MEMORY PARITY FAIL	08F11	This bit is set when the memory interface recognizes a parity failure. It is stored in the SELCH for subsequent evaluation by the processor; however, the transfer is not interrupted. It is cleared by initialize or command GO.

COMMAND BYTE
SIGNALS (SHEET 7)

READ	00B06	This command changes the SELCH mode from write to read. In read mode, data is transmitted from the active device on the SELCH and written into memory. Whenever a data transmission has been completed, the SELCH is placed in the write mode. Each time a read operation is required, a read command must be issued.
GO	07B05	This command initiates a data transmission and can be issued at the same time the read/write mode is established.
STOP	02E01	This command halts any data transmission in progress and initializes the SELCH for starting a new operation. It must be given when the SELCH terminates.

NOTE

A stop command issued to a busy SELCH will not set the MSC1 flip-flop, therefore, not allowing communication to devices on the SELCH private bus. The SELCH must be addressed a second time to allow communications under the above conditions.

SELCH STATUS	03E01	When this bit is set, the SELCH status is always returned on an SR or SS instruction to the SELCH. When reset, the current SELCH definition applies (i.e., when the SELCH is idle, the device status is returned with the BUSY bit forced to a zero. When the SELCH is transferring data, only the BUSY bit is returned. The SELCH becomes idle only after initialize or any I/O instruction to the SELCH is executed).

EXTENDED ADDRESS READ	03E09	When this bit is set, the SELCH returns a 3-byte final address to the processor if RD or RDR, followed by RH or RHR instructions, are executed. The most significant byte is returned first. When this bit is reset, the SELCH returns a 2-byte final address to the processor if two successive RD or RDR instructions are executed. The most significant byte is returned first. Before issuing RD or RH instructions to read the final address, a STOP command must be issued to ensure that the SELCH is in the initialized state.

4.4 DEVICE DATA TRANSFERS

This section pertains to device data transfers which include SELCH busy and control circuits private bus.

4.4.1 Selector Channel (SELCH) Busy

When the processor issues a GO command to the SELCH, the trailing edge of command gate (CMG1) (6L1) fires a 19-042 one shot resulting in a command GO pulse (CMDGO1) (7F6). This pulse sets the busy bit, prevents the processor from communicating with the active device on the private bus and starts the transfers to the device and to the memory (see Functional Schematic 35-732M02D08).

4.4.2 Control Circuits Private Bus

When the SELCH is given an output command GO, it immediately assumes control of the active device on the private bus and begins data transfers. Each data transfer cycle consists of a sense status (SS) and a data read/data write. Device data transfers operate independently of memory transfers, governed only by the status of the FIFO stack; that is, before a write to the device can be done, the stack must be valid and before a read from the device can be done, the stack must not be full.

4.4.2.1 Read Mode

When the SELCH is controlling transfers to/from the device, it continuously alternates a status transfer with a data transfer until all data has been transferred to/from the device (see Figure 4-1). When the processor issues a command to GO, CMDG0 sets the status transfer (SX1) flip-flop (8N8). This activates the private status request (PSR0) control line on the private bus. When the device returns the SYNC signal (PSYN0), the SELCH examines the four least significant bits (LSBs) of the status byte as follows. PSYN1 (8A8) is delayed approximately 50ns to allow the data to settle. The leading edge of delayed private SYNC (DPS1) (8F8) is gated with the status returned by the device. If all four bits are reset, meaning the device is not busy and there are no error conditions, the data transfer (DX1) flip-flop (8S6) is set and PSR0 is made inactive. When the device releases PSYN0, DPS0 goes high and the private data request (PDR1) (8S6) control line becomes active if the stack is not full. PDR1 also resets the SX1 flip-flop. When the device responds to PDR0 with PSYN0, DPS1 resets the DX1 flip-flop, PDR1 is made inactive, and the device releases PSYN0. The trailing edge of DPS0 fires the end of data transfer (EDX1) (15F5) one shot, which in turn activates SSX0 and another cycle is initiated. This process continues until a match (IOMCH1) between the AAR and FAR is detected. IOMCH1 (9N4) inhibits further data transfers by preventing SSX0 from being activated.

Data to be read from the device is received at the PD transceivers and loaded into the input buffer. If the active device performs halfword transfers, then the clock pulses at both halves (high byte and low byte) of the input buffer are made active with the leading edge of DPS1. The LSB of the auxiliary address register (AAR) (AAR231) is used for byte steering if the active device is byte-oriented. When loading the AAR, it is necessary that AAR191 be zero if the data is to be properly aligned in memory. When AAR231=0, the byte read from the device is loaded into the most significant portion of the input buffer by LDBH0 (15H1). When AAR231=1, the byte read from the device is loaded into the least significant portion of the input buffer by LDBL0 (15H2). Each time LDBL0 is made active, the contents of the input buffer are transferred into the stack by the LDSTK1 signal (15N1). LDSTK1 is a 50ns pulse derived from LDBL0. It is delayed approximately 40ns after the leading edge of LDBL0 to allow the data to settle at the stack inputs.

The AAR is incremented with each byte that is transferred. If the active device is byte-oriented, the AAR is incremented by the trailing edge of EDX0 (11L5). If the device performs halfword transfers, the AAR is incremented twice within each data transfer cycle; once by EDX0 and once by the gate (11M6) whose logic is PHW1 PDAR1 (PSYN1 DPS0). Note that when a match is detected, IOMCH0 (11G9) prevents the AAR from changing value by disabling the 19-070 counters.

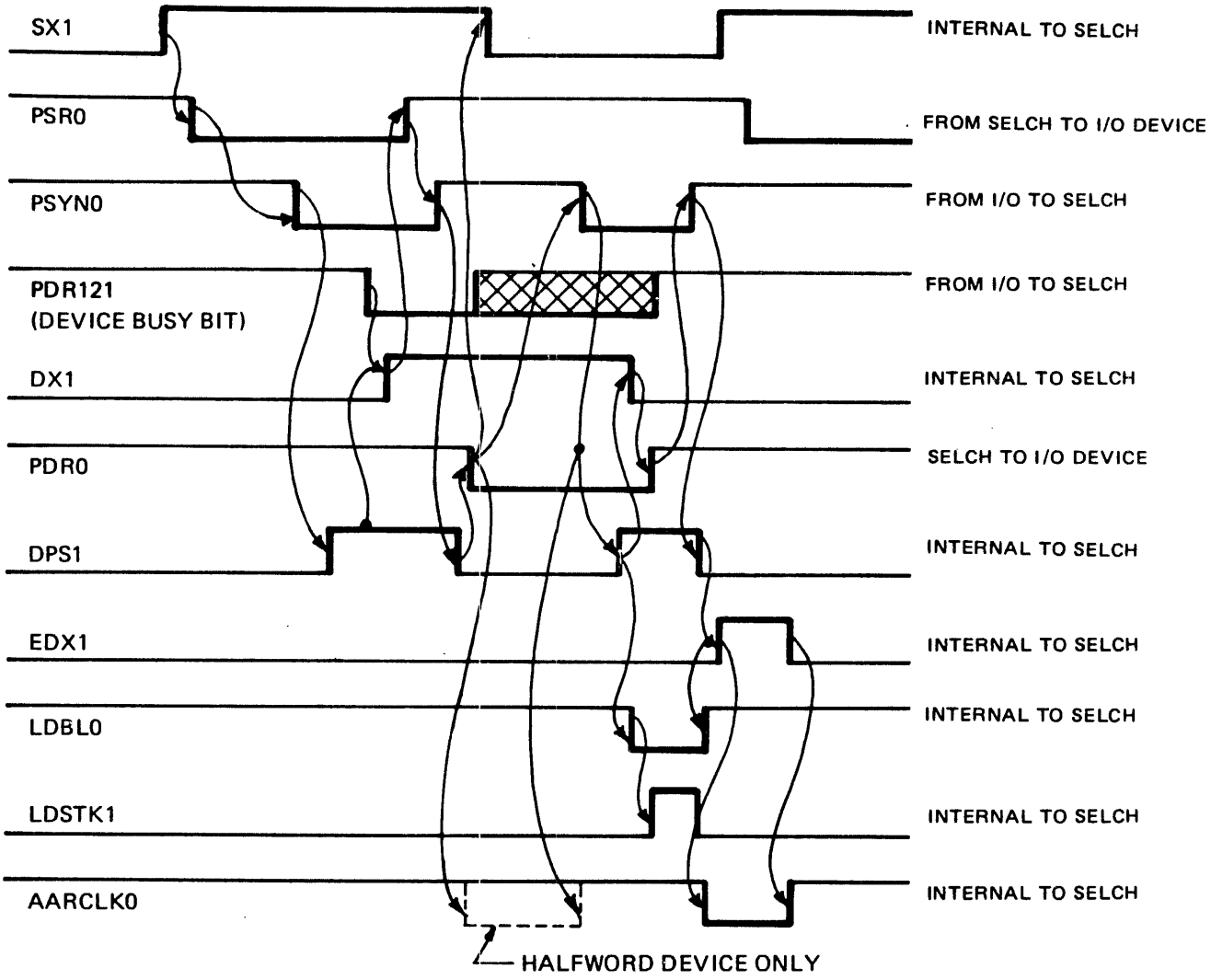


Figure 4-1 Private Bus Control Read from Device Timing Diagram

4.4.2.2 Write Mode

The SELCH private bus control circuit operates in a similar manner as the read mode (see Figure 4-2). The differences are described in the following paragraphs. At the end of a status transfer, DPS0 sets the GPD1 (8J9) flip-flop which enables the private data bus transceivers (ENBPD0) (6K4). GPD1 is delayed to permit setting of the data and then enables the private data available (PDA1) (8S9) control line. When the device returns SYNC, DPS1 resets the DX1 flip-flop, disabling the PDA1 control line. When the device releases the PSYN0 control line, DPS0 fires the EDX1 one shot beginning a new cycle.

Data at the output of the stack is changed by the trailing edge of STKCLK0 (15H2). If the active device performs halfword transfers, STKCLK0 is active in every data transfer cycle. If the device is byte-oriented, AAR231 is used for byte steering and the stack outputs are changed after two bytes have been transferred. In either case, STKCLK0 is formed directly from the DPS1 signal.

The AAR is incremented exactly as discussed in Section 4.4.2.1.

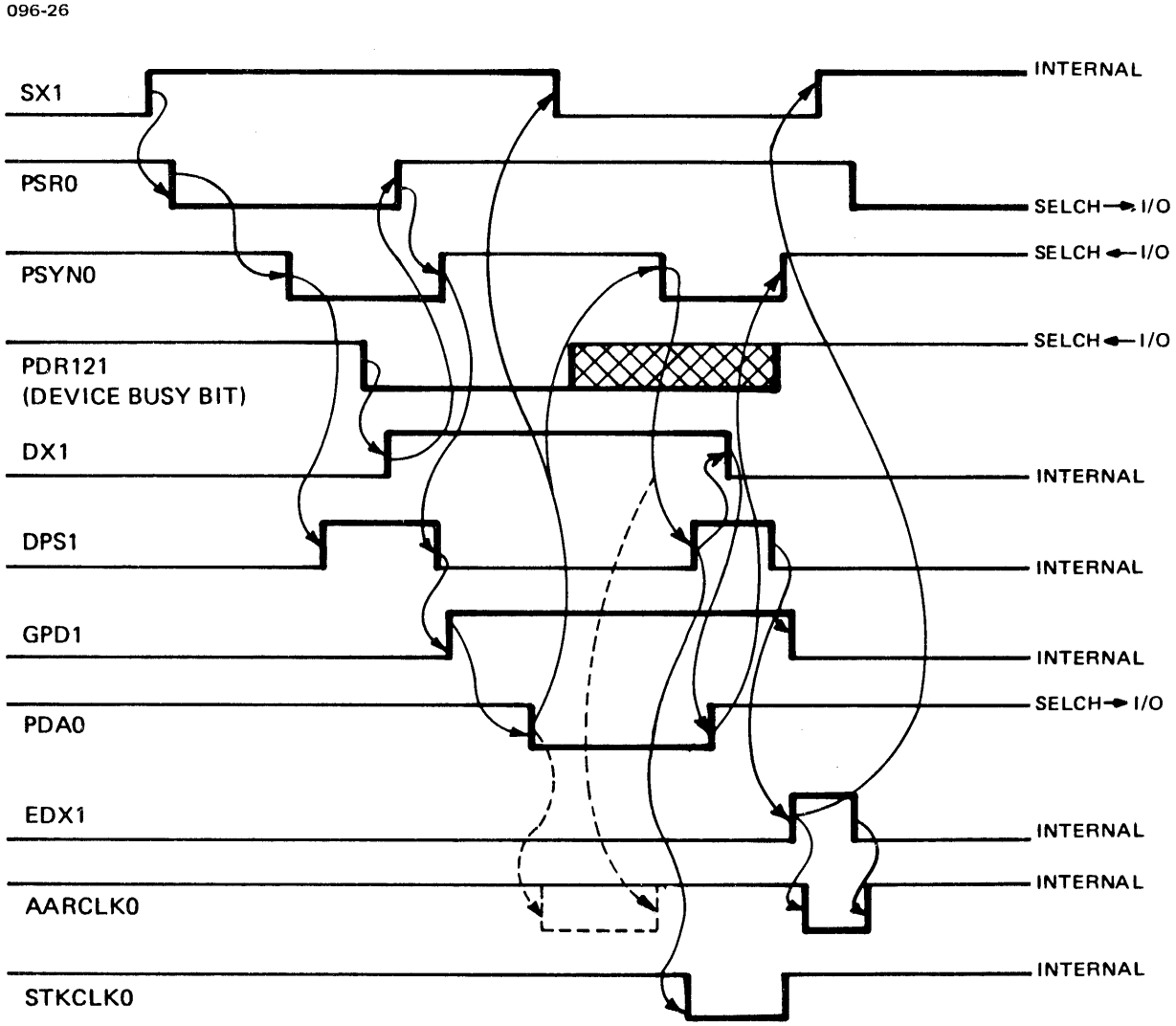


Figure 4-2 Private Bus Control Write to Device Timing Diagram

4.5 DIRECT MEMORY ACCESS (DMA) BUS TRANSFERS

This section explains DMA bus transfers which includes data paths and DMA bus control circuits.

4.5.1 Data Paths

In the write mode (memory read), when the processor issues an output command GO, the SELCH immediately requests access to the memory and proceeds to fill the stack. As data is written to the device and space becomes available in the stack for additional data, the SELCH again requests the memory to refill the stack. This procedure continues until the memory address register (MAR) matches the final address register (FAR) (HWMCH0) (10K2) and DMA bus transfers terminate. The data read from the memory is received at the DMA bus transceivers (2G1:G9) and loaded into the input buffer for transfer to the stack.

In the read mode (memory write), data is read from the device and loaded into the stack. When the data has fallen through the stack, the stack is considered valid and data transfers to the memory can begin. The stack outputs are loaded into a high-speed data buffer (2B1:B9) which is gated onto the DMA bus through the transceivers at the appropriate time. When the MAR matches the FAR, the SELCH terminates.

4.5.2 Bus Control Circuits

The SELCH performs DMA bus transfers in the quadword burst mode (see Chapter 1 for strapping instructions).

4.5.2.1 Bus Acquisition

When the SELCH has determined that it is necessary to transfer data to/from memory, the DMARQ1 (14R8) flip-flop is set. This begins a handshake sequence with the processor to acquire the bus for data transfer.

Figure 4-3 is a timing diagram of the bus acquisition sequence. The sequence is initiated when the SELCH activates XREQ0 (12L6). Before XREQ0 can be made active, two conditions must be met:

1. The memory system to which a request has been made must not be busy.

2. The SELCH must not be selected for transfer.

Two 19-032, 1/10 decoders (12C1:C4) monitor the four most significant bits (MSBs) of the MAR. The output of these decoders are strapped to define each memory system boundary (M0, M1, M2 and M3) in blocks of 64kB for the Model 3210, 3220 and 3230 Systems and blocks of 1MB for the Model 3240 and 3250XP Systems. See Chapter 1 for strapping instructions. The four bits designating the memory system are encoded to PAGE01 and PAGE11 (12M4) in the Model 3240 System (the Model 3220 System uses M0BZ1 through M3BZ1).

The 19-069 multiplexor (MPX) (12M2) examines each memory busy signal and PAGE01 and PAGE11 select the appropriate memory busy signal at its output. Therefore, MBZ1 (12M2) always notifies the SELCH if the memory system to which it is about to transfer is busy. If the SELCH is not transferring data, the select flip-flop (SEL1) (12M8) is reset. These conditions, plus the presence of DMARG1, make the DREQ1 (12L5) gate high and XREQ0 active.

When the processor receives XREQ0, it sends a queue pulse (QUE0) (12C8) to freeze the request status of all DMA bus devices. The leading edge of QUE0 loads DREQ1 into the first contention flip-flop (12F8) and the trailing edge of QUE0 loads the request into the second contention flip-flop. All requesting devices now have these flip-flops set and all devices not having a request on the bus have these flip-flops reset. Next, the processor transmits a priority chain pulse (RPC0) (12C9). The highest priority device which has been queued captures the RPC0 pulse and sets the third stage request flip-flop. If the SELCH has not been queued, RPC0 is transmitted to the next device as TPC0 (12J9). If the SELCH is transferring to local memory, M01 (12H2) is high and local memory request (LMRQ0) (12K6) is active. Contention being resolved, if the memory is not busy, the processor sends a start of transmit (SOT0) (12J9) pulse. SOT0 sets the select flip-flop and the SELCH begins transmission.

096-27

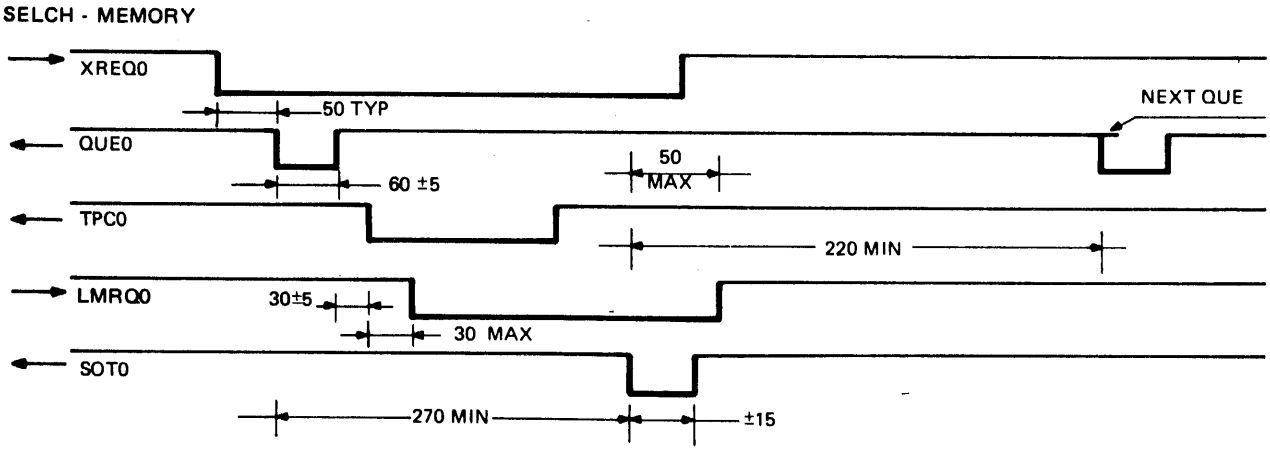


Figure 4-3 DMA Bus Acquisition Sequence Timing Diagram

4.5.2.2 Data Transfers

When the SELCH is selected for data transfer, the internal clock (DMACLK1) (15N8) is activated starting the control sequences for the data transfer. The control required to implement the data transfer is programmed in two of the 19-199 programmable logic arrays (PLA) and with each DMACLK1 pulse, the PLA outputs are latched (14G1:G8) and the internal program is advanced to the next control state. Figure 4-4 is a control state diagram of SELCH data transfers. There are eight control states used to implement the four types of data transfers. A brief description of each type of transfer follows.

In the memory read, halfword mode, the leading edge of SOT0 sets the select (SEL1) flip-flop, and since the SELCH is in the idle control state zero (CS01), the gate at 15F7 starts DMACLK1. The first transition of DMACLK1 places the SELCH in control state one (CS1), where the following control signals become active (see Figure 4-5).

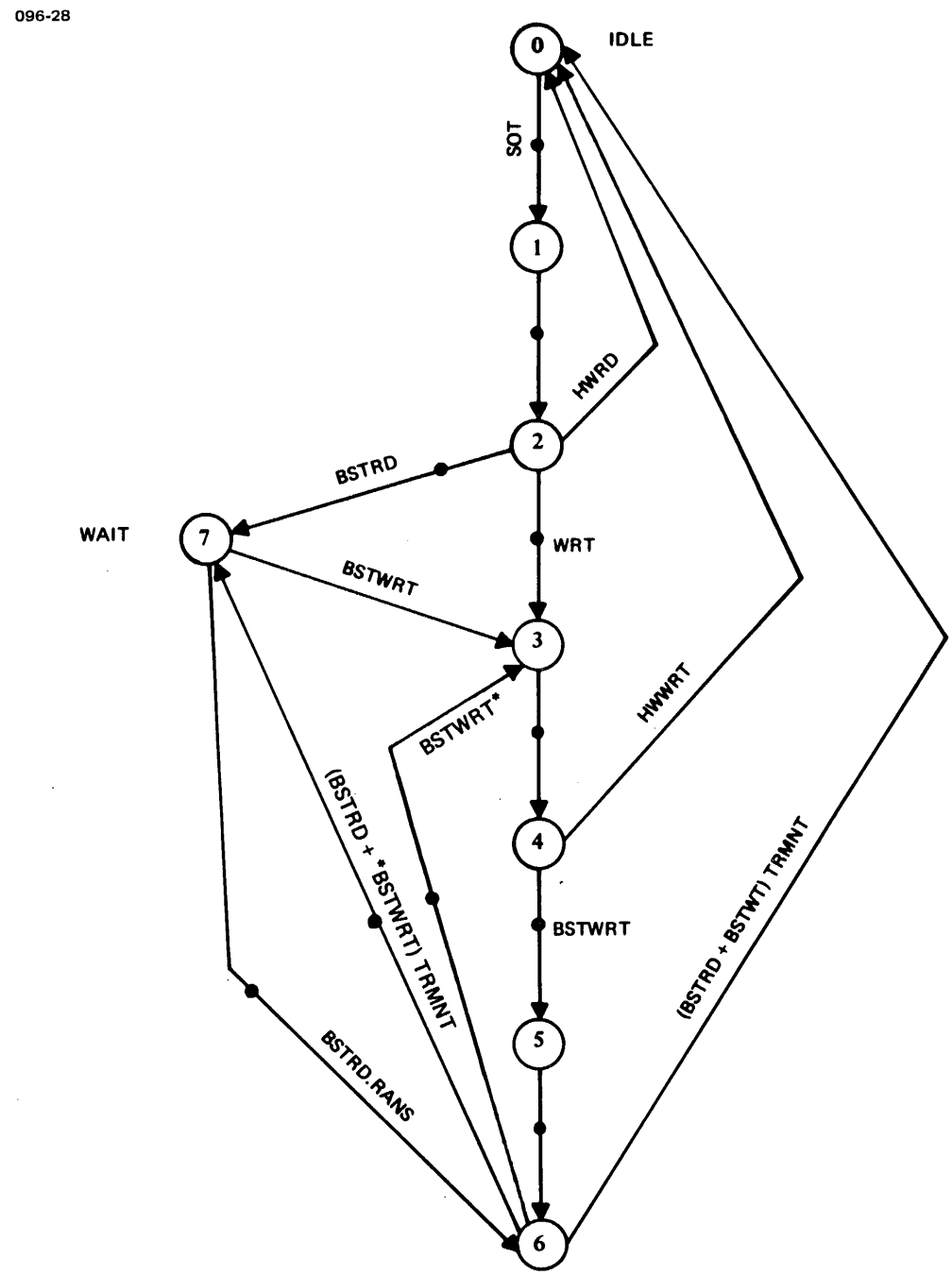
The GADR0 (2C2) signal selects the MAR on the MUXs to the DMA bus. The ENBDMA0 signal (2H1) enables the DMA bus transceivers.

During CS1, MAR is gated to the DMA bus. On the next DMACLK1, the SELCH is placed in CS2 where the MAR is still gated to the idle (CS01) state.

The SELCH is now waiting for the requested data from the memory. Data is gated to the DMA bus by the processor memory system and an answer (ANS0) pulse is transmitted with the data. To ensure that the data is intended for SELCH, the ANS0 is decoded as follows. When the SELCH becomes selected, the leading edge of SEL1 loads the encoded PAGE01 and PAGE11 into a register (13C8) for temporary storage. When the data read from memory is gated to the DMA bus, DMX140 and DMX150 are encoded to reflect the memory system from which the data has been sent. These are compared to the stored PAGE01 and PAGE11 and if they are the same the input to the flip-flop at 13H7 is high. When the answer pulse is received, the leading edge of ANSR1 (13H7) loads this flip-flop and the decoded answer is formed from the RANS0 (13K7) gate.

To ensure that the SELCH does not decode answers intended for other devices, a wait for answer (W4ANS1) flip-flop (13L5) is set during control state one. The W4ANS1 flip-flop is double rank flip-flop designed to permit two ANS0 signals to be decoded (for burst mode) prior to resetting the W4ANS1 flip-flop. On the transition to control state zero, the reset wait for answer (RW4ANS0) signal (13J6) becomes active. The leading edge of the decoded RANS1 resets the first flip-flop and the trailing edge of RANS0 resets the W4ANS1 flip-flop. When W4ANS1 is low, the answer (13H7) decoding flip-flop is held low and received answers cannot be decoded.

In the Model 3240 and 3250XP Systems, an additional feature is used to decode ANSl. The SELCH's ID bits are sent back from the memory system to the SELCH. When the SELCH gets a match on ID bits, it responds to the answer.



*BSTWRT on Model 3210, 3220 and 3230 Systems goes from 6 to 7
BSTWRT on Model 3240 and 3250XP Systems goes from 6 to 3

Figure 4-4 Control State Diagram - DMA Transfers

- Memory Read, Burst Mode

  The MAR is gated to the DMA bus in control states 1 and 2 (see Figure 4-5). In control state 2, LOAD0 and EOT0 are sent. The W4ANS1 flip-flop has been set. From control state 2, the SELCH proceeds to control state 7, a burst mode wait state. On the transition to control state 7, DINH1 (15E8) becomes active and DMACLK1 is inhibited by the gate at 15F8 until the first ANS0 is received. The leading edge of RANS0 starts DMACLK1, resulting in two clock pulses. The first pulse sends the SELCH to control state 6 where either a LOAD0 or an EOT0 is transmitted to the processor. In this case, the signal sent is used to notify the processor if additional data is required. If another fullword of data is desired, LOAD0 is sent. If no additional data is desired, EOT0 is sent. If another fullword is requested, the next clock pulse returns the SELCH to control state 7 to wait for another pair of ANS0 signals. If the EOT0 is sent, the next clock sends the SELCH to control state 0, terminating the burst transfer. The second ANS0 received would then reset the W4ANS1 flip-flop.

- Memory Write, Burst Mode

  The address is sent to the processor during control states 1 and 2 and a LOAD0 is sent with the address (see Figure 4-6). On the transition from control state 2 to 3, the data register is loaded from the stack with the first halfword of the burst transfer. This is gated to the DMA bus during control states 3 and 4 and a LOAD0 is sent during control state 4. On the transition from control state 4 to 5, the data register is loaded with the second halfword of the burst. This is gated to the bus during control states 5 and 6 and a LOAD0 is sent during control state 6. To terminate burst transfer, an EOT0 is also sent during control state 6 and the SELCH returns to the idle state, control state 0. To send additional data, the SELCH proceeds to control state 7, the wait state. The W4ANS1 flip-flop is set and DINH1 inhibits DMACLK1. When the processor sends an ANS0, indicating it is ready to accept additional data, the leading edge of RANS0 starts the clock and the SELCH proceeds from control state 7 to control state 3. During control states 3, 4, 5 and 6, the next two halfwords are read from the stack, loaded into the data register, and sent to the memory. This procedure continues until the burst is terminated with an EOT0 in control state 6 and the SELCH returns to control state 0.

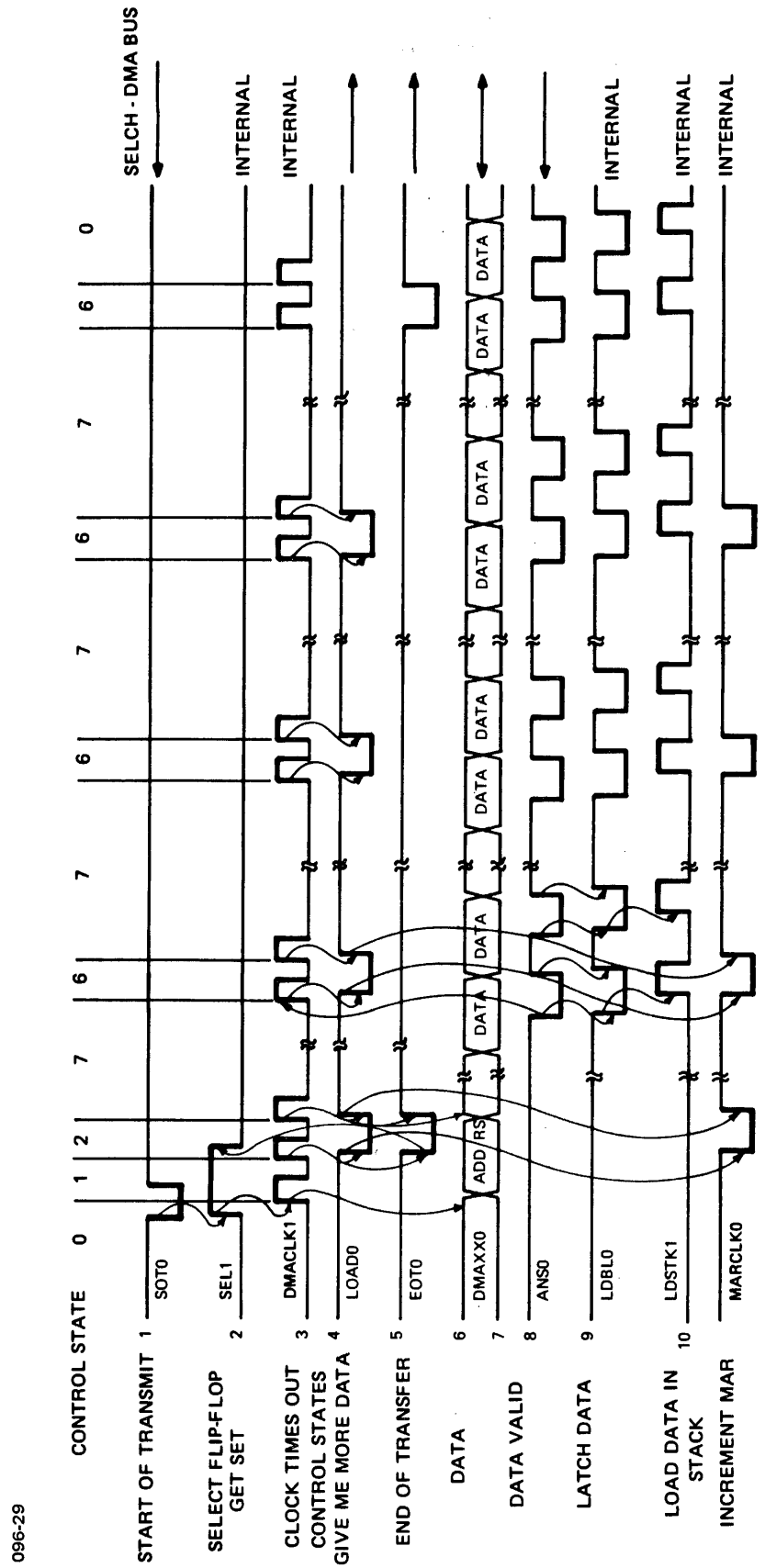


Figure 4-5 DMA Transfer, Memory Read

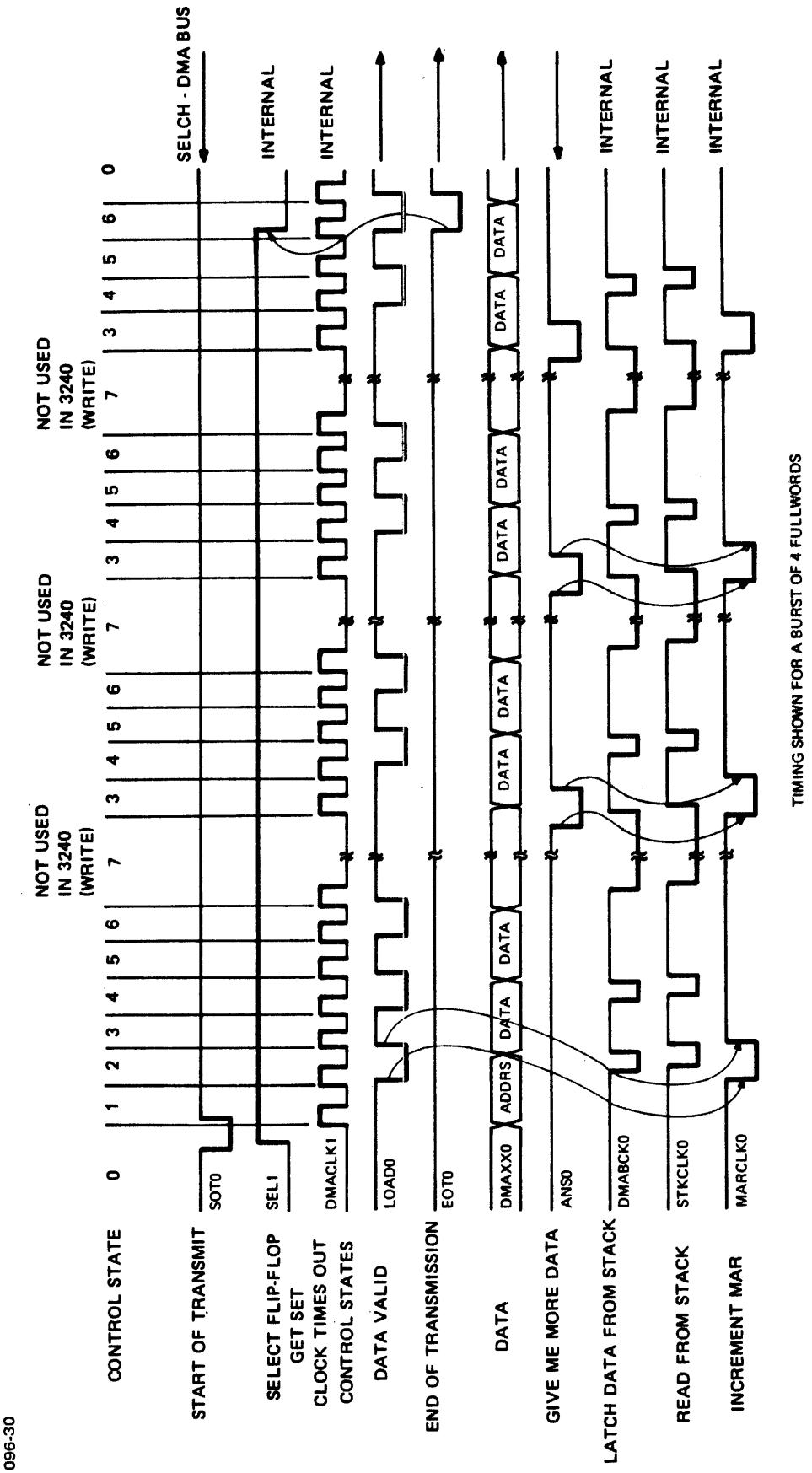


Figure 4-6 DMA Transfer, Memory Write

Termination of a burst transfer (read and write) can result from any of the following:

1. Crossing memory system boundary (XBNDRY1). The next fullword to be transferred would necessitate crossing a memory system boundary (one quadword boundary). The SELCH terminates the transfer and requests access to the memory system into which it has crossed.

2. Address match (FWMCH0, HWMCH0). The address contained in the MAR matches the final address contained in the FAR. This condition signals an end to all memory transfers.

3. Unusual conditions (TERM1). There are four other conditions not normally encountered which would force termination of a burst and all other activity (SELCH returns to idle mode). They are:

   a. Initialize (CLO71)

   b. STOP command

   c. ACRY0 - The AAR has incremented to the largest possible value. This prevents wraparound in memory transfers.

   d. NOMEM0 - The MAR is pointing to an address of nonexistent memory.

PLA programs are presented in Tables 4-2 and 4-3. See Sheet 14 of the 35-732M02D08 schematics to obtain correlation of the truth table to SELCH signals. The tables specify the outputs of the PLA with respect to their inputs.

TABLE 4-2 PLA PROGRAM TABLE (19-199F06) LOC 04A

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_M	$\bar{I}_M$	DON'T CARE	PROD TERM PRESENT IN F_P	PROD TERM NOT PRESENT IN F_P	ACTIVE HIGH	ACTIVE LOW
H	L	–	A	•	H	L
NOTE: ALL UNUSED INPUTS MUST BE PROGRAMMED AS DON'T CARE			NOTE: OUTPUT FUNCTION ENTRIES ARE INDEPENDENT OF PROGRAMMED OUTPUT PRIORITY		NOTE: OUTPUT PRIORITY PROGRAMMED ONCE ONLY	

NO.	DMF1N1 15	S ≥ B 14	XBNDRY1 13	IM40 12	STCKVL01 11	HLT101 10	IOMCH1 9	HWMCH0 8	FARZZ0 7	FWMCH0 6	TERM1 5	MWFF1 4	MWRT1 3	(1) CSA1 2	(2) CSB1 1	(4) CSC1 0	7	DMFINA (H) 6	SXREQ (H) 5	DMFIN (H) 4	HW (H) 3	SW4ANSO (H) 2	ENBDMA (H) 1	GADRI (H) 0
0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	L	L		•	•	•	•	•	A	A
1	-	-	-	-	-	-	-	-	-	-	-	-	H	-	H	L		•	•	•	•	•	A	•
2	-	-	-	-	-	-	-	-	-	-	-	L	H	-	L	H		•	•	•	•	•	A	•
3	-	-	-	-	-	-	-	-	-	-	-	-	H	H	H	H		•	•	•	•	•	A	•
4	-	-	L	H	-	-	-	-	-	H	L	-	H	L	H	H		•	•	•	•	•	A	•
5	-	-	L	H	-	-	-	H	L	L	L	-	H	L	H	H		•	•	•	•	•	A	•
6	-	-	-	-	-	-	-	-	-	-	-	-	L	H	L	L		•	•	•	•	A	•	•
7	-	-	-	-	-	-	-	-	-	-	-	L	H	H	L	L		•	•	•	•	A	•	•
8	-	-	-	-	-	-	-	-	H	L	-	-	-	L	H	H		•	•	•	A	•	•	•
9	-	-	-	-	-	-	-	L	-	-	-	H	H	L	L	H		•	•	•	A	•	•	•
10	-	-	-	-	-	-	-	L	-	-	-	H	L	L	L	L		•	•	A	•	•	•	•
11	-	-	-	-	-	-	-	L	L	-	-	-	L	H	H	H		•	•	A	•	•	•	•
12	-	-	-	-	-	-	H	L	-	-	-	H	H	L	L	L		•	•	A	•	•	•	•
13	-	-	-	-	L	H	L	-	-	-	-	-	H	L	L	H		•	•	A	•	•	•	•
14	-	-	-	-	-	-	H	L	L	-	-	-	L	L	H	H		•	•	A	•	•	•	•
15	-	-	-	-	L	H	L	-	-	-	-	-	H	L	H	H		•	•	A	•	•	•	•
16	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		•	•	A	•	•	•	•
17	L	H	-	-	-	L	-	-	-	-	L	-	L	-	-	-		•	A	•	•	•	•	•
18	L	-	-	-	H	-	-	-	-	-	L	H	H	-	-	-		•	A	•	•	•	•	•
19	L	H	-	-	-	-	-	-	-	-	L	L	H	-	-	-		•	A	•	•	•	•	•
20	L	L	-	-	H	H	H	-	-	-	L	L	H	-	-	-		•	A	•	•	•	•	•
21	-	-	-	-	L	H	-	-	-	-	-	-	H	L	L	L		A	•	•	•	•	•	•
22	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		•	•	•	•	•	•	•
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0. (CS01 + CS11)→ GADR1 · ENBDMA1
1. (CS21 + CS31) · MWT1 → ENBDMA1
2. (CS41 + CS51) · MWT1 · HW0 → ENBDMA1
3. CS71 · MWT1 → ENBDMA1
4. CS61 · MWT1 · TERM0 · FWMCH0 · IM401 · XBNDRY0 → ENBDMA1
5. CS61 · MWT1 · TERM0 · FWMCH1 · FAR221 · HWMCH0 · IM401 · XBNDRY0→ ENBDMA1
6. CS11 · MRD1 → SW4ANS1
7. CS11 · MWT1 · HW0 → SW4ANS1
8. CS61 · FWMCH1 · FAR220 → SHWFF1
9. CS41 · MWT1 · HW1 · HWMCH1 → SAWFF1
10. CS01 · MRD1 · HW1 · HWMCH1→SDMFIN1
11. CS71 · MRD1 · FAR221 · HWMCH1 → SDMFIN1
12. CS01 · MWT1 · HW1 · HWMCH1 · IOMCH1 → SDMFIN1
13. CS41 · MWT1 · HW1 · IOMCH0 · HLTIO1 · STKVLD0 → SDMFIN1
14. CS61 · MWT1 · FAR221 · HWMCH1 · IOMCH1 → SDMFIN1
15. CS61 · MWT1 · IOMCH0 · HLTIO1 · STKVLD0 → SDMFIN1
16. DMFIN1 → SDMFIN1
17. MRD1 · TERM0 · HLTIO0 · (SEQB1 + SGTRB1) · DMFIN0 → SREQ1
18. MWT1 · HW1 · TERM0 · STKVLD1 DMFIN0 → SREQ1
19. MWT1 · HW0 · TERM0 · (SEQB1 + SGTRB1) DMFIN0 → SREQ1
20. MWT1 · HW0 · TERM0 · IOMCH1 · HLTIO1 · STKVLD1 · SEQB0 · SGTRB0 DMFIN0 → SREQ1
21. CS01 · MWT1 · HLTIO1 · STKVLD0→ SDMFIN1A

TABLE 4-3 PLA PROGRAM TABLE (19-199F07) LOC 03A

PROGRAM TABLE ENTRIES				
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_M	I_M	DON'T CARE	PROD TERM PRESENT IN F_P	PROD TERM NOT PRESENT IN F_P	ACTIVE HIGH	ACTIVE LOW
H	L		A		H	L
NOTE: ALL UNUSED INPUTS MUST BE PROGRAMMED AS DON'T CARE			NOTE: OUTPUT FUNCTION ENTRIES ARE INDEPENDENT OF PROGRAMMED OUTPUT PRIORITY		NOTE: OUTPUT PRIORITY PROGRAMMED ONCE ONLY	

	PRODUCT TERM																											
	INPUT VARIABLE (1_{in})																			OUTPUT FUNCTION								
NO.	15	14 IM401	13	12	11	10 XBNDRY	9	8 HWMCH0	7 FARZZ0	6 FWMCH0	5 TERM1	4 HWFF1	3 HWRT1	2 CSA1	1 CSB1	0 CSC1	7 RW4ANS	6 DINHI	5 LDMAB	4 LOAD	3 EOT	2 CSA	1 CSB	0 CSC
														1	2	4			ACTIVE LEVEL			1	2	4			
																	H	H	H	H	H	H	H	H				
0	–	–	–	–	–	–	–	–	–	–	–	L	L	L	H	L	•	A	•	•	•	A	A	A				
1	–	–	–	–	–	–	–	–	–	–	–	L	H	L	L	H	•	•	•	•	•	A	•	A				
2	–	–	–	–	–	L	–	–	–	H	L	–	L	L	H	H	•	A	•	•	•	A	A	A				
3	–	L	–	–	–	L	–	–	–	H	L	–	H	L	H	H	•	A	A	•	•	A	A	A				
4	–	H	–	–	–	L	–	–	–	H	L	–	H	L	H	H	•	•	•	•	•	A	A	•				
5	–	–	–	–	–	L	–	H	L	L	L	–	L	L	H	H	•	A	•	•	•	A	A	A				
6	–	L	–	–	–	L	–	H	L	L	L	–	H	L	H	H	•	A	A	•	•	A	A	A				
7	–	H	–	–	–	L	–	H	L	L	L	–	H	L	H	H	•	•	•	•	•	A	A	•				
8	–	–	–	–	–	–	–	–	–	–	–	–	H	H	H	L	•	•	•	A	•	•	•	A				
9	–	–	–	–	–	–	–	–	–	–	–	–	H	H	L	H	•	•	•	A	•	•	A	A				
10	–	–	–	–	–	–	–	–	–	–	–	–	L	H	H	H	•	•	•	•	•	•	A	A				
11	–	–	–	–	–	–	–	–	–	–	–	–	H	L	H	L	•	•	•	•	•	A	A	•				
12	–	–	–	–	–	–	–	–	–	–	–	–	H	H	H	H	•	•	•	•	•	A	A	•				
13	–	–	–	–	–	–	–	–	–	–	–	–	–	H	L	L	•	•	•	A	•	•	A	•				
14	–	–	–	–	–	–	–	–	–	–	–	–	–	L	L	L	•	•	•	•	•	A	•	•				
15	–	–	–	–	–	–	–	–	–	–	–	–	L	H	L	L	•	•	•	•	A	•	•	•				
16	–	–	–	–	–	–	–	–	–	–	–	H	H	H	H	L	•	•	•	•	A	•	•	•				
17	–	–	–	–	–	H	–	–	–	–	–	–	H	H	L	H	•	•	•	•	A	•	•	•				
18	–	–	–	–	–	–	–	–	–	–	H	–	H	H	L	H	•	•	•	•	A	•	•	•				
19	–	–	–	–	–	–	–	–	H	L	–	–	H	H	L	H	•	•	•	•	A	•	•	•				
20	–	–	–	–	–	–	–	L	L	L	–	–	H	H	L	H	•	•	•	•	A	•	•	•				
21	–	–	–	–	–	H	–	–	–	–	–	–	L	H	H	H	•	•	•	•	A	•	•	•				
22	–	–	–	–	–	–	–	–	–	–	H	–	L	H	H	H	•	•	•	•	A	•	•	•				
23	–	–	–	–	–	–	–	–	H	L	–	–	L	H	H	H	•	•	•	•	A	•	•	•				
24	–	–	–	–	–	–	–	L	L	L	–	–	L	H	H	H	•	•	•	•	A	•	•	•				
25	–	–	–	–	–	L	–	–	–	H	L	–	L	H	H	H	•	•	•	A	•	•	•	•				
26	–	–	–	–	–	L	–	H	L	L	L	–	L	H	H	H	•	•	•	A	•	•	•	•				
27	–	–	–	–	–	–	–	–	–	–	–	–	H	H	L	L	•	•	A	•	•	•	•	•				
28	–	–	–	–	–	–	–	–	–	–	–	L	H	H	H	L	•	•	A	•	•	•	•	•				
29	–	H	–	–	–	L	–	–	–	H	L	–	H	H	L	H	•	•	A	•	•	•	•	•				
30	–	H	–	–	–	L	–	H	L	L	L	–	H	H	L	H	•	•	A	•	•	•	•	•				
31	–	–	–	–	–	–	–	–	–	–	H	–	L	–	H	H	A	•	•	•	•	•	•	•				
32	–	–	–	–	–	–	–	–	H	L	–	–	L	–	H	H	A	•	•	•	•	•	•	•				
33	–	–	–	–	–	–	–	L	L	L	–	–	L	–	H	H	A	•	•	•	•	•	•	•				
34	–	–	–	–	–	–	–	–	–	–	–	H	L	L	H	L	A	•	•	•	•	•	•	•				
35	–	–	–	–	–	H	–	–	–	–	–	–	L	–	H	H	A	•	•	•	•	•	•	•				
36																												
37																												
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39																												
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41																												
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43																												

0. CS21 · MR01 · HW0 → CS71 · DINH1
1. CS41 · MWT1 · HW0 → CS51
2. CS61 · MRD1 · TERM0 · FWMCH0 · XBNDRY0 → CS71 · DINH1
3. CS61 · MWT1 · TERM0 · FWMCH0 · XBNDRY0 · IM400 → CS71 · LDMAB1 · DINH1
4. CS61 · MWT1 · TERM0 · FWMCH0 · XBNDRY0 · IM401 → CS31
5. CS61 · MRD1 · TERM0 · FWMCH1 · FAR221 · HWMCH0 · XBNDRY0 → CS71 · DINH1
6. CS61 · MWT1 · TERM0 · FWMCH1 · FAR221 · HWMCH0 · XBNDRY0 · IM400 → CS71 · LDMAB1 · DINH1
7. CS61 · MWT1 · TERM0 · FWMCH1 · FAR221 · HWMCH0 · XBNDRY1 · IM401 → CS31
8. CS31 · MWT1 → CS41 · TLOAD1
9. CS51 · MWT1 → CS61 · TLOAD1
10. CS71 · MRD1 → CS61
11. CS21 · MWT1 → CS31
12. CS71 · MWT1 → CS31
13. CS11 → CS21 · TLOAD1
14. CS01 → CS11
15. CS01 · MRD1 → TEOT1
16. CS31 · MWT1 · HW1 → TEOT1
17. CS51 · MWT1 · XBNDRY1 → TEOT1
18. CS51 · MWT1 · TERM1 → TEOT1
19. CS51 · MWT1 · FWMCH1 · FAR220 → TEOT1
20. CS51 · MWT1 · FWMCH1 · FAR221 · HWMCH1 → TEOT1
21. CS71 · MRD1 · XBNDRY1 → TEOT1
22. CS71 · MRD1 · TERM1 → TEOT1
23. CS71 · MRD1 · FWMCH1 · FAR220 → TEOT1
24. CS71 · MRD1 · FWMCH1 · FAR221 · HWMCH1 → TEOT1
25. CS71 · MRD1 · TERM0 · FWMCH0 · XBNDRY0 → TLOAD1
26. CS71 · MRD1 · TERM0 · FWMCH1 · FAR221 · HWMCH0 → TLOAD1
27. CS11 · MWT1 → LDMAB1
28. CS31 · MWT1 · HW0 → LDMAB1
29. CS51 · MWT1 · TERM0 · FWMCH0 · XBNDRY0 · IM401 → LDMAB1
30. CS51 · MWT1 · TERM0 · FWMCH1 · FAR221 · HWMCH0 · IM401 → LDMAB1
31. (CS61 + CS71) · TERM1 · MRD1 → RW4ANS1
32. (CS61 + CS71) · MRD1 · FWMCH1 · FAR220 → RW4ANS1
33. (CS61 + CS71) · MRD1 · FWMCH1 · FAR221 · HWMCH1 → RW4ANS1
34. CS21 · MRD1 · HW1 → RW4ANS1
35. (CS61 + CS71) · MRD1 · XBNDRY1 → RW4ANS1

4.5.2.3 Bus Request Logic

The logic for making requests to the memory is programmed into the 19-199F07 PLA and is derived from the status of the FIFO stack. As data is loaded into and/or removed from the stack, the MAR and the AAR are incremented to reflect completion of the data transfer. The 19-133 4-bit adder (13E4) performs a subtraction between the four LSBs of the MAR and the AAR (AAR-MAR = S). The result, S, is interpreted as follows:

1. In the memory read mode, data is loaded into the stack from the memory and subsequently transferred to the active device. The MAR is always larger than or equal to the AAR until a match occurs. Therefore, S always reflects (in number of halfwords) the available, or empty, stack locations.

2. In the memory write mode, the converse is true. The AAR is always larger than or equal to the MAR and S reflects the number of halfwords present in the stack.

The resultant sum, S, is compared to the burst size strap option and the mode of operation strap option. Three signals are generated from the comparison (13K4):

1. SGTRB1 - when active means S is greater than the burst size

2. SEQB1 - when active means S is equal to the burst size

3. SLTB1 - when active means S is less than the burst size

A request is made whenever S is greater than or equal to the burst size. This ensures that in memory read mode there are enough stack locations available for a burst transfer and in memory write mode enough data has been written into the stack for the burst transfer.

4.6 TERMINATION

When the SELCH has completed its data transfers, the delayed busy (DBSY1) (7N2) signal becomes inactive and fires the set attention (SETATN0) (7K4) one shot. The SELCH attention (SATN1) flip-flop is set and an interrupt is sent to the processor.

Normal termination occurs when the SELCH has successfully transferred all of its data. In the memory read mode, this occurs when the last byte of data has been transferred to the device. When transferring the last byte of data, IOMCH1 is active and when the EDX1 one shot is fired, the halt I/O (HLTIO1) flip-flop (15N5) is set. This signal resets the BSY1 flip-flop (7N7) and DBSY1 becomes inactive, firing the SETATN0 one shot.

In the memory write mode, the HLTIO1 flip-flop is set before completion of the memory transfers. BSY1 is reset by HLTIO0 but DBSY1 is prevented from becoming inactive by the MWTHLT0 gate being active. When the memory transfers are completed (the stack emptied), the DM finish (DMFIN1) flip-flop (14H7) is set and it resets the HLTIO1 flip-flop. MWTHLT0 then becomes inactive and DBSY1 fires the SETATN0 one shot.

Abnormal termination can occur from two sources. TERM1 (7N2) resets BSY1, and, if there is no DMA activity (DMACT0) (7G3), DBSY1 is reset. The other means of termination result from bad status received from the active device when the SELCH is in the midst of a status transfer. Bad status (BADST0) (15K7) sets the HLTIO1 flip-flop and prevents the DX1 flip-flop from being set. HLTIO clears BSY1 and, if in memory read mode, it clears DBSY1. If in the memory write mode, the valid data in the stack must be transferred to the memory. When this has been done, DMFIN1 is set, HLTIO1 is reset, and then DBSY1 is reset.

4.7 MNEMONICS

The following is a list of mnemonics found in the SELCH. A brief description of each mnemonic and the 35-732M02D08 schematic location signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR00l:19l	Auxiliary address register	Sheet 11
ACRY0	Carry out from AAR	11E2
AD1	Address flip-flop - active when SELCH is addressed	5J2
ADRS0	Address control line from MPX bus	6A4
ANS0	Answer control line - signals that data from memory is available	2N9
ARLD0	When active, permits loading of the AAR	11N4
ATN0	Attention to processor	6A5
ATSYN0	Attention SYNC - generated by acknowledge attention from the processor	6N5
BADST0	Bad status returned from the device while transferring	15J7
BSTSZ01:21	Burst size - number of fullwords to be transferred in each memory access	13F6
BSY1	Busy - indicates SELCH is transferring data	7N7
CLG1	Control line gate - gates MPX bus control lines to private bus	6C7
CLRS0	Clear SELCH - initializes SELCH	7N1
CLO70	Power failure clear	6A4
CMD0	Command control line from MPX bus	6A2
CMDG01	Command GO initiates the transfer	7F6
CMG0	Command control gated with AD1	6L2
CS01	Control state zero of a DMA data transfer	14N3

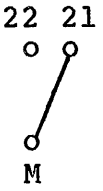
MNEMONIC	MEANING	SCHEMATIC LOCATION
D000:150	Data lines from MUX bus	Sheet 4
DA0	Data available control line from MPX bus	6A3
DAG0	Data available control line gated with AD1 and BSY1	6L2
DBSY1	Delayed busy - delays interrupt to processor until memory accesses are complete	7N2
DINH1	Inhibits clock during wait state of memory transfers	14H4
DMA000:170	DMA bus data lines	Sheet 2
DMACLK1	Clock for memory transfers	Sheet 15
DMACT0	Indicates DMA activity	14R9
DMARQ1	DMA bus request flip-flop	14R8
DMFIN1	Indicates DMA transfers are completed	14H8
DMX080:150	DMA bus extended data lines	2N2:2N3
DPS1	Private SYNC control line delayed	8F8
DR0	Data request control line from MPX bus	6A2
DREQ1	Indicates SELCH is requesting the memory	12L5
DRG0	Data request control line gated with AD1 and BSY1	6L2
DT081:151	Data lines returned to processor	Sheet 8
DX1	Data transfer flip-flop	8S6
EDX0	End of data transfer one shot	15E5
EOBST1	End of burst - indicates appropriate number of full-words have been transferred to the memory	13K2
EOT0	End of transmission signal for DMA transfers	13R8
ENBD0	Enables MUX bus data line drivers	6L3
ENBPD0	Enables private bus data line drivers	6M4
EXRD1	Extended read - set in command byte when three bytes are required to read the final address	7E1
FAR001:191	Final address register - address of last location in memory to be accessed	Sheet 9
FWMCH0	Fullword match - memory address matches the FAR on a fullword boundary	10L2
GPD1	Gate private data - enables private bus data line drivers during writes to device	8J9

MNEMONIC	MEANING	SCHEMATIC LOCATION
HLTI01	Halt I/O flip-flop	15N5
HW0	Halfword control line sent to processor MUX bus	6N8
HWFF1	Halfword flip-flop - set when SELCH is to perform a halfword DMA bus transfer	14R7
HWMCH0	Halfword match - the necessary address matches the FAR on a halfword boundary	10L3
HWMD1	Halfword mode	13F5
IOMCH1	I/O match - indicates the AAR matches the FAR	9N4
ID000:020	ID bits - identifies each SELCH to memory system	13B16
LDBH0	Load data buffer high	15H1
LDBL0	Load data buffer low	15H2
LDSTK1	Load STK1	15N1
LFARX0	Load FAR001:031	11N4
LMRQ0	Load memory request queued	12L6
LOAD0	Load signal on DMA transfer	2N9
M00:M30	Memory banks 0:3	Sheet 12
M0BZ0:M3BZ0	Memory busy	Sheet 12
MAR001:181	Memory address register	Sheet 10
MARCLK0	Memory address register clock	13DF2
M0SEL0/MISEL0	Memory select - indicates which memory bank is being addressed	Sheet 2
MMF1	Memory malfunction status bit	13R1
MRD1	Memory read command bit	7F5
MWRT1	Memory write command bit	7F4
MSC1	Multiplexor-SELCH control flip-flop	7N8 7N8
NOMEM0	No memory - indicates MAR is pointing to nonexistent memory	12G4
PADRS0	Private address control to SELCH private bus	6F5
PATN0	Private attention from device	6A9
PCL070	Private power fail control line	6F8
PCMD0	Private command control line	6F6
PD000:150	Private data lines	Sheet 4
PDA0	Private data available control line	6F6
PDR0	Private data request control line	6F7

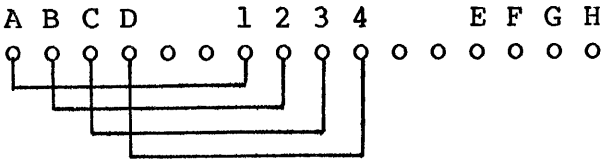
MNEMONIC	MEANING	SCHEMATIC LOCATION
PF1	Memory parity failure status bit	13R2
PHW0	Private halfword control line	6J8
PSR0	Private status request control line	6F7
PSYN0	Private SYNC from device	6A9
PTACK0	Private transmit acknowledge to private bus	6N6
QUEQ	Queue - to resolve contention for DMA bus	12C8
RACK0	Receive acknowledge from MUX bus	6G5
RPC0	Receive priority chain pulse from DMA bus	12C9
SID081:151	SELCH 10-bit address	5A2:5A6
SCLR0	System clear	7J2
SEL1	Select flip-flop - when active SELCH selected for DMA transfer	12M8
SELSTS1	SELCH status command bit	7E2
SOT0	Start of transmission pulse from DMA bus	12J9
SR0	Status request control line	6L1
SRG0	Status request control line gated with AD1	6A2
STK001:151	FIFO stack data outputs	3A9:3L9
STKCLK0	FIFO stack clock - removes data from the stack	15H2
STKFL0	Stack full signal	3K1
STKVLD1	Stack valid signal	3N1
SYN0	SYNC to MUX bus	6A5
SX1	Status transfer flip-flop	8M8
TACK0	Transmit acknowledge to MUX bus	6N7
TERM1	Terminate the transfer	7N2
TPC0	Transmit priority chain pulse to DMA bus	12J9
UAARH0	Unload AAR041:111	11M1
UAARL0	Unload AAR121:191	11M1
UAARX0	Unload AAR001:031	11M2
W4ANS1	Wait for answer	13M5
XBNDRY1	Indicates SELCH is about to cross a memory system boundary	13H9
XREQ0	Request DMA bus for service	12L6

APPENDIX A
MODEL 3210 SYSTEM STRAPPING

MEMORY BUSY
(Board Location 07K)

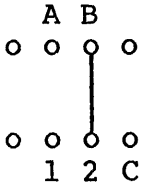


ADDRESS TO BANK DECODERS
(Board Location 07H)

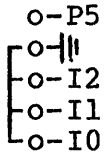


GATED ADDRESS
(Board Location 00T)

IM40
(Board Location 00A)



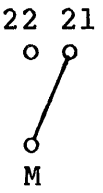
IDENTIFICATION (ID) CODE
(CONN4)



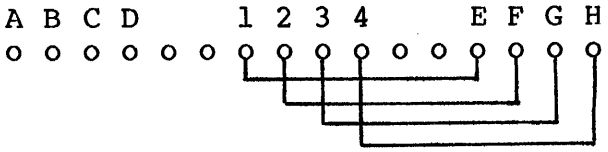
ADDRESS WRAP
(Board Location 12F)

APPENDIX B
MODEL 3220 SYSTEM STRAPPING

MEMORY BUSY
(Board Location 07K)

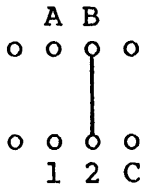


ADDRESS TO BANK DECODERS
(Board Location 07H)

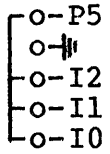


GATED ADDRESS
(Board Location 00T)

IM40
(Board Location 00A)



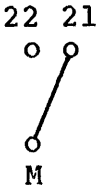
IDENTIFICATION (ID) CODE
(CONN4)



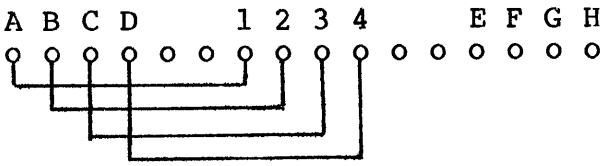
ADDRESS WRAP
(Board Location 12F)

APPENDIX C
MODEL 3230 SYSTEM STRAPPING

MEMORY BUSY
(Board Location 07K)

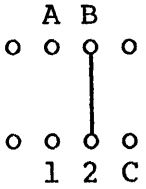


ADDRESS TO BANK DECODERS
(Board Location 07H)

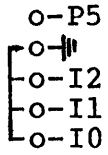


GATED ADDRESS
(Board Location 00T)

IM40
(Board Location 00A)



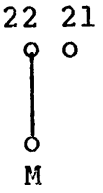
IDENTIFICATION (ID) CODE
(CONN4)



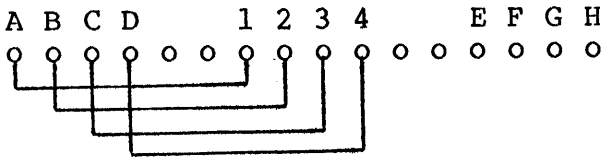
ADDRESS WRAP
(Board Location 12F)

APPENDIX D
MODEL 3240 SYSTEM STRAPPING

MEMORY BUSY
(Board Location 07K)

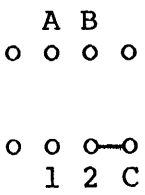


ADDRESS TO BANK DECODERS
(Board Location 07H)

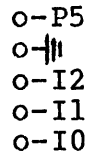


GATED ADDRESS
(Board Location 00T)

IM40
(Board Location 00A)



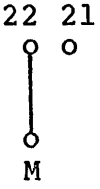
IDENTIFICATION (ID) CODE
(CONN4)



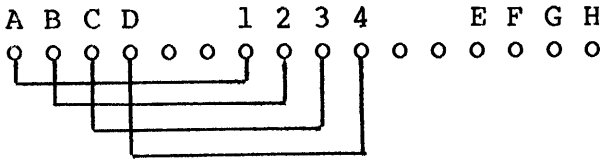
ADDRESS WRAP
(Board Location 12F)

APPENDIX E
MODEL 3250 SYSTEM STRAPPING

MEMORY BUSY
(Board Location 07K)

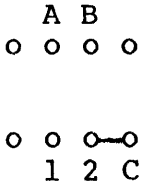


ADDRESS TO BANK DECODERS
(Board Location 07H)



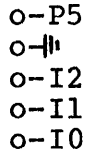
GATED ADDRESS
(Board Location 00T)

IM40
(Board Location 00A)



IDENTIFICATION (ID) CODE
(CONN4)

MUST BE UNIQUE ON DMA BUS



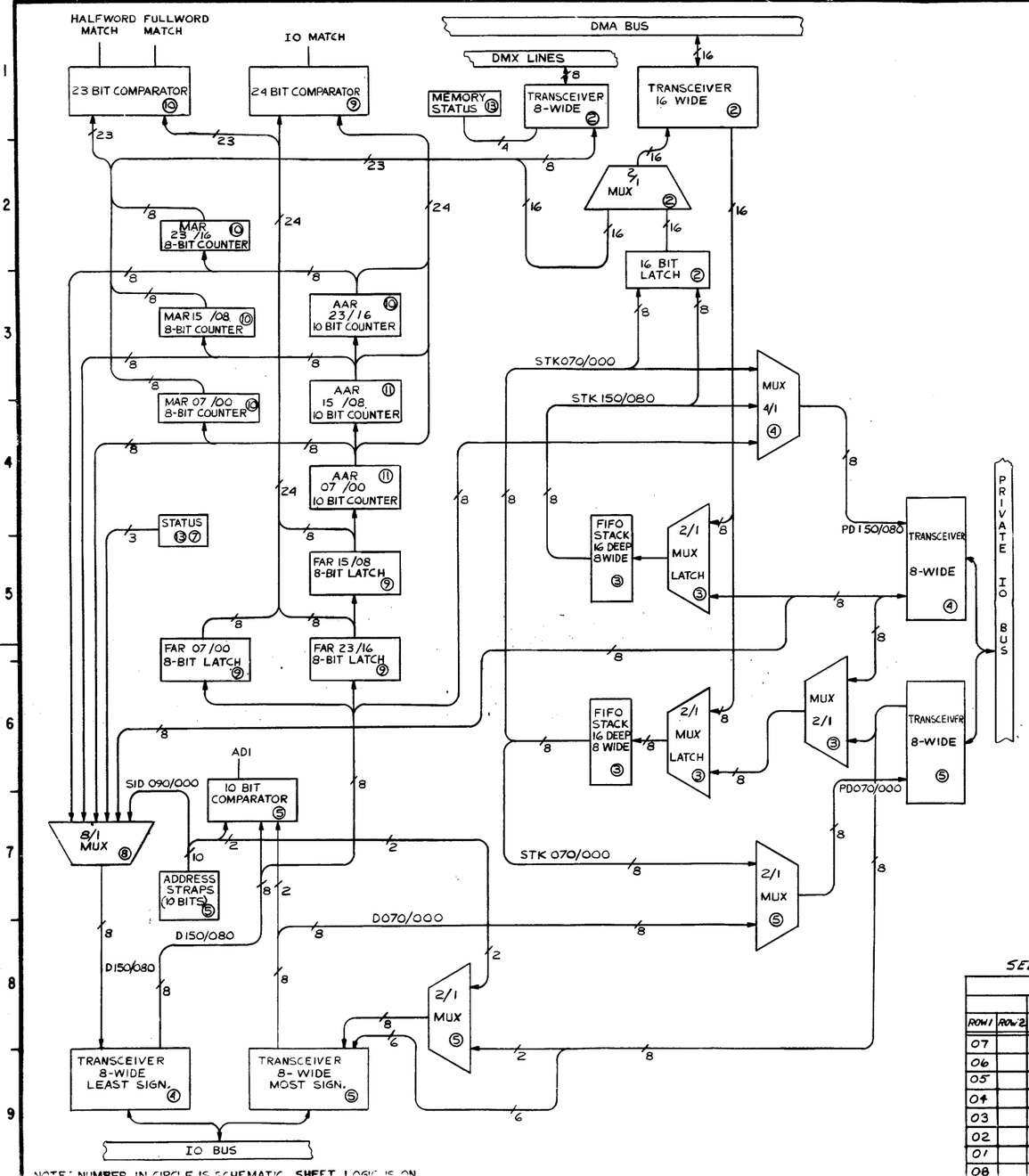
ADDRESS WRAP
(Board Location 12F)

INDEX

S

T,U,V

W,X,Y,Z



NOTE: NUMBER IN CIRCLE IS SCHEMATIC SHEET LOGIC IS ON

SEE SHT16 FOR STRAPPING INFOR.

TABLE OF SPARES		
REF. DESIGNATION	PART NUMBER	SPARE OUTPUT NUMBER
00A	19-125	03
00D	19-155	12,06
01C	19-058	08
01D	19-058	08
03D	19-055	08
06C	19-058	12
06D	19-016	03
06K	19-154	04
09D	19-154	06
09J	19-058	08
09T	19-154	12
10D	19-064	07,09
10S	19-015	02
11C	19-154	12
11T	19-125	08,06,11
12F	19-172	06
13A	19-160	03
13B	19-017	06,08
14B	19-016	06,08,11
14C	19-154	06

TEST POINTS				
ROW1	ROW2	DESIG.	MNEMONIC	SHT. LOC.
07			ADO	5J2
06			DXI	8R6
05			MSCO	7N9
04			BSYI	7N7
03			SELI	12M7
02			MWRTI	7F4
01			SXI	8N8
08			STKFLO	3K1
00			STKVLDI	3N1

BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2	TERM. NO.	CONN
P5	GND	41	
GND	GND	40	
		39	
		38	
DMA17O	GND	37	
DMA15O	DMA16O	36	
DMA13O	DMA14O	35	
GND	DMA12O	34	
DMA11O	DMA10O	33	
DMAO9O	DMAO8O	32	
DMAO7O	DMAO6O	31	
DMAO5O	GND	30	
DMAO3O	DMAO4O	29	
DMAO1O	DMAO2O	28	
GND	DMAOOO	27	
SCLRO	PHWO	26	
	SCHKO	25	
SNSO	XBSYO	24	
PSYNO	PATNO	23	
	PTACKO	22	
PCLO7O	PDAO	21	
PDRO	PCMDO	20	
PSRO	PADRSO	19	
PDI4O	PDI5O	18	
PDI2O	PDI3O	17	
PDIOO	PDIIO	16	
PDO8O	PDO9O	15	
PDO6O	PDO7O	14	
PDO4O	PDO5O	13	
PDO2O	PDO3O	12	
PDOOO	PDO1O	11	
	DMXI4O	10	
DMXI5O	DMXI2O	09	
DMXI3O	GND	08	
M3BZO	M2BZO	07	
M1BZO	M0BZO	06	
LOADO	ANSO	05	
LMRQO	GND	04	
SOTO	EOTO	03	
XREQO	QUEO	02	
GND	GND	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
		39	
		38	
RPCO	TPCO	37	
GND		36	
		35	
		34	
DMXIOO	DMXI1O	33	
DMXO8O	DMXO9O	32	
IDO1O	IDO2O	31	
IDOOO		30	
		29	
MOSELO	MISELO	28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
CLO7O	DAO	21	O
DRO	CMDO	20	
SRO	ADRSO	19	
DI4O	DI5O	18	
DI2O	DI3O	17	
DIOO	DIIO	16	
DO8O	DO9O	15	
DO6O	DO7O	14	
DO4O	DO5O	13	
DO2O	DO3O	12	
DOOO	DO1O	11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
P5	GND	00	

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISIONS			
	INIT	DATE	
PRE PRODUCTION APPROVAL	DEV	4-1-84	
RELEASED FOR PRODUCTION ENG. [illegible]		DATE 11/30/84	

AREA J2 SPARE GATE 06C-12 WAS 19-017. AREA M9, BOARD REV WAS R06 REV'D SHT'S 1,2,6-8,10&12.

MF	[illegible]	5975	MS	7-1-85	R01

AREA M9, BOARD REV WAS R01. REV'D SHTS 1, 3&8

DB	[illegible]	6053	N	6-29-85	R02

AREA R6, MANUAL WAS 29-727

JT	[illegible]	6047	E	9-11-85	R03

USED IN MANUAL: 47-096

UNLESS OTHERWISE SPECIFIED

SCALE: NONE

TOLERANCE: .XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

DIMENSIONS ARE IN INCHES

NAME		TITLE	DATE
R. Goodman	E. JOHNSON	DES/DFT	8-17-84
R. CERO		SUPV	11-30-84
E. GREENSTEIN		CHK	11-30-84
R. BOYD		ENG	11-30-84
W. LEPOW		MGR	11-30-84
R. BARKER		QC	11-30-84

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
3200 SELCH

TASK 03071

DWG 35-732M02 R03 D08

SHT 1-16

REVISION	C3	01	01			01	01	02		01		01				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

NOTES: 1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4W, ± 5%.

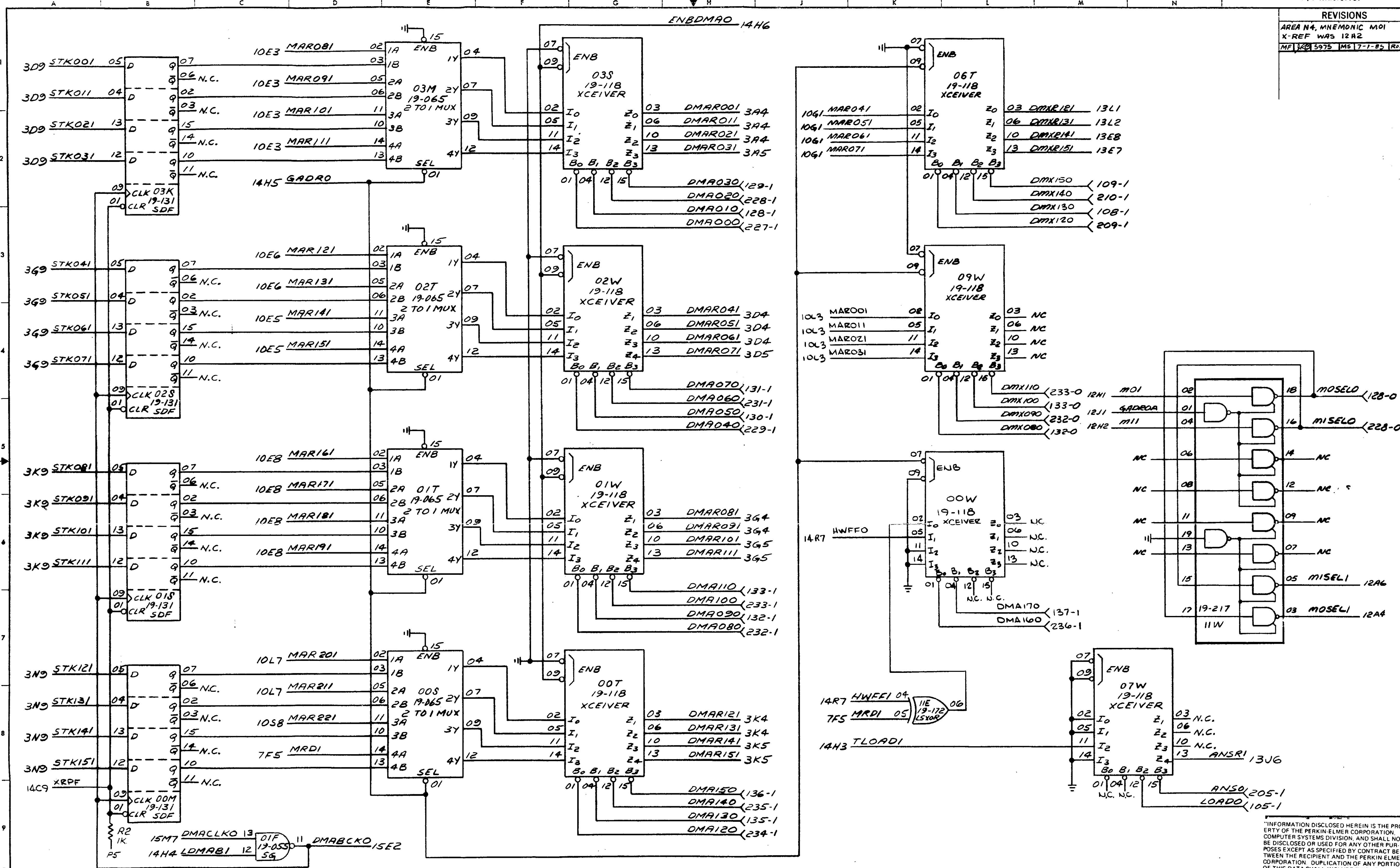
SELCH 35-732 M02	R02
BOARD	REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

I RUNNING 44-131 40579

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
AREA N4, MNEMONIC M01 X-REF WAS 12A2
MF 5975 MS 7-1-85 R01



ENBDMAO 14H6
03K 19-131 SDF
02S 19-131 SDF
01S 19-131 SDF
00M 19-131 SDF
03M 19-065 2 TO 1 MUX
02T 19-065 2 TO 1 MUX
01T 19-065 2 TO 1 MUX
00S 19-065 2 TO 1 MUX
03S 19-118 XCEIVER
02W 19-118 XCEIVER
01W 19-118 XCEIVER
00T 19-118 XCEIVER
06T 19-118 XCEIVER
09W 19-118 XCEIVER
00W 19-118 XCEIVER
07W 19-118 XCEIVER
11W 19-217
01F 19-055 5G
11E 19-172 LS XOR
3D9 STK001
3D9 STK011
3D9 STK021
3D9 STK031
3G9 STK041
3G9 STK051
3G9 STK061
3G9 STK071
3K9 STK081
3K9 STK091
3K9 STK101
3K9 STK111
3N9 STK121
3N9 STK131
3N9 STK141
3N9 STK151
14C9 XRPF
R2 1K
P5
15M7 DMACLKO
14H4 LDMAB1
DMABCKO 15E2
14H5 GADRO
10E3 MAR081
10E3 MAR091
10E3 MAR101
10E3 MAR111
10E6 MAR121
10E6 MAR131
10E5 MAR141
10E5 MAR151
10E8 MAR161
10E8 MAR171
10E8 MAR181
10E8 MAR191
10L7 MAR201
10L7 MAR211
10S8 MAR221
7F5 MRDI
DMAR001 3A4
DMAR011 3A4
DMAR021 3A4
DMAR031 3A5
DMA030 129-1
DMA020 228-1
DMA010 128-1
DMA000 227-1
DMAR041 3D4
DMAR051 3D4
DMAR061 3D4
DMAR071 3D5
DMA070 131-1
DMA060 231-1
DMA050 130-1
DMA040 229-1
DMAR081 3G4
DMAR091 3G4
DMAR101 3G5
DMAR111 3G5
DMA110 133-1
DMA100 233-1
DMA090 132-1
DMA080 232-1
DMAR121 3K4
DMAR131 3K4
DMAR141 3K5
DMAR151 3K5
DMA150 136-1
DMA140 235-1
DMA130 135-1
DMA120 234-1
10G1 MAR041
10G1 MAR051
10G1 MAR061
10G1 MAR071
DMXR121 13L1
DMXR131 13L2
DMXR141 13E8
DMXR151 13E7
DMX150 109-1
DMX140 210-1
DMX130 108-1
DMX120 209-1
10L3 MAR001
10L3 MAR011
10L3 MAR021
10L3 MAR031
DMX110 233-0
DMX100 133-0
DMX090 232-0
DMX080 132-0
14R7 HWFF0
DMA170 137-1
DMA160 236-1
14R7 HWFE1
7F5 MRDI
14H3 TLOADI
ANSR1 13J6
ANS0 205-1
LOAD0 105-1
12H1 M01
12J1 GADROA
12H2 M11
MOSEL0 128-0
MISEL0 228-0
MISEL1 12A6
MOSEL1 12A4

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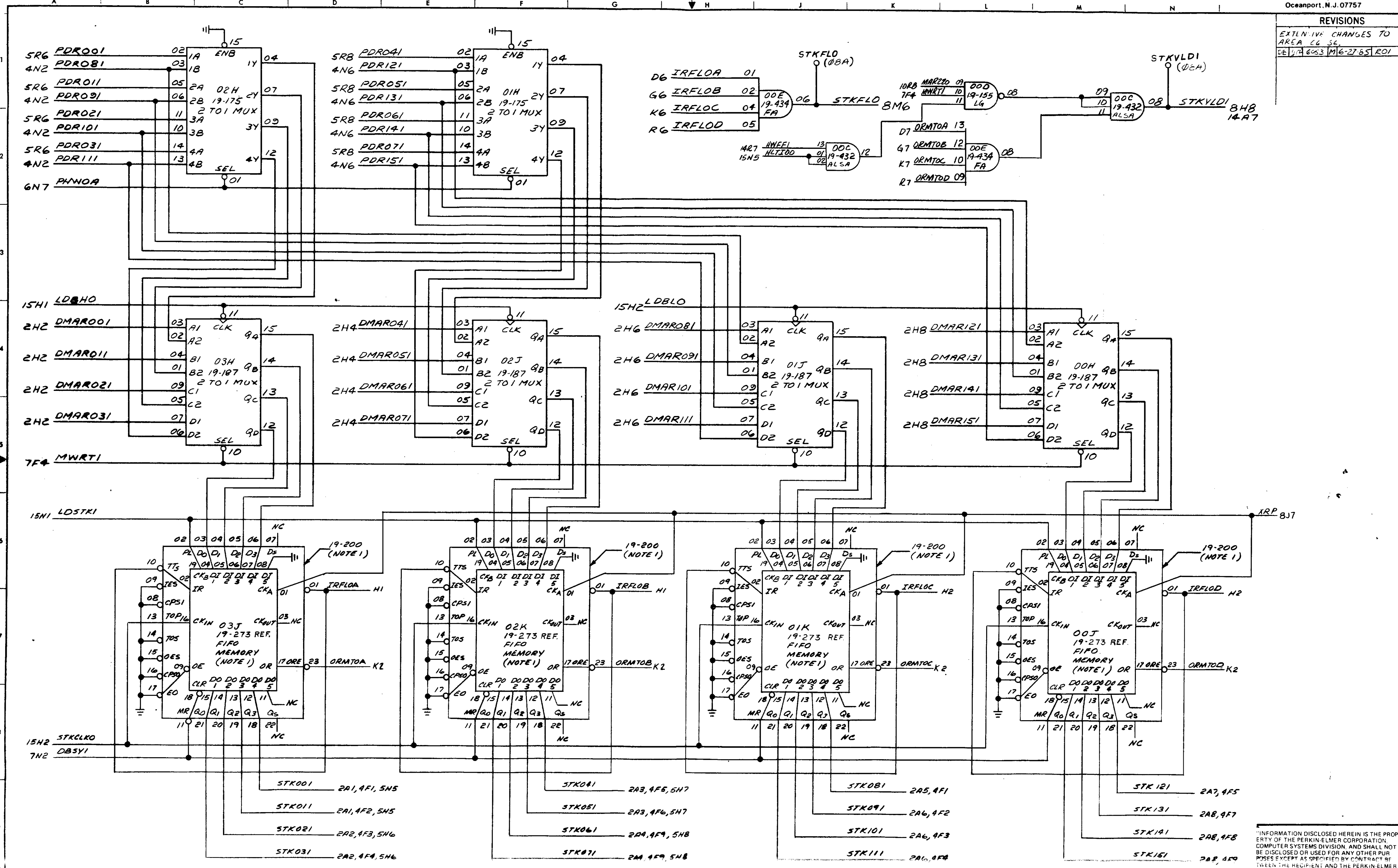
SCALE—	NAME	TITLE	DATE	TITLE
	DSTINE	DRAFT		FUNCTIONAL SCHEMATIC 3200 SELCH
		CHK		03071
		ENGR		35-032M02R0D08 — SHEET 2-16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

EXTENSIVE CHANGES TO AREA C6 ... | 6053 | M | 6-27-85 | R01


5R6 PDR001
4N2 PDR081
5R6 PDR011
4N2 PDR091
5R6 PDR021
4N2 PDR101
5R6 PDR031
4N2 PDR111
6N7 PHWOA
02H 19-175 2 TO 1 MUX
5R8 PDR041
4N6 PDR121
5R8 PDR051
4N6 PDR131
5R8 PDR061
4N6 PDR141
5R8 PDR071
4N6 PDR151
01H 19-175 2 TO 1 MUX
D6 IRFLOA
G6 IRFLOB
K6 IRFLOC
R6 IRFLOD
STKFLO (Ø8A)
00E 19-434 FA
STKFLO 8M6
10R8 MAR220
7F4 MWRT1
00D 19-155 LG
14R7 WWEF1
15N5 HLTIOO
00C 19-432 ALSA
D7 ORMTOA
G7 ORMTOB
K7 ORMTOC
R7 ORMTOD
00E 19-434 FA
STKVLD1 (Ø8A)
00C 19-432 ALSA
STKVLD1 8H8 14A7
15H1 LDBHO
2H2 DMAR001
2H2 DMAR011
2H2 DMAR021
2H2 DMAR031
03H 19-187 2 TO 1 MUX
2H4 DMAR041
2H4 DMAR051
2H4 DMAR061
2H4 DMAR071
02J 19-187 2 TO 1 MUX
15H2 LDBLO
2H6 DMAR081
2H6 DMAR091
2H6 DMAR101
2H6 DMAR111
01J 19-187 2 TO 1 MUX
2H8 DMAR121
2H8 DMAR131
2H8 DMAR141
2H8 DMAR151
00H 19-187 2 TO 1 MUX
7F4 MWRT1
15N1 LDSTK1
XRP 8J7
19-200 (NOTE 1)
03J 19-273 REF. FIFO MEMORY (NOTE 1)
IRFLOA H1
ORMTOA K2
02K 19-273 REF. FIFO MEMORY (NOTE 1)
IRFLOB H1
ORMTOB K2
01K 19-273 REF. FIFO MEMORY (NOTE 1)
IRFLOC H2
ORMTOC K2
00J 19-273 REF. FIFO MEMORY (NOTE 1)
IRFLOD H2
ORMTOD K2
15H2 STKCLKO
7N2 DBSY1
STK001 2A1,4F1,5H5
STK011 2A1,4F2,5H5
STK021 2A2,4F3,5H6
STK031 2A2,4F4,5H6
STK041 2A3,4F5,5H7
STK051 2A3,4F6,5H7
STK061 2A4,4F9,5H8
STK071 2A4,4F9,5H8
STK081 2A5,4F1
STK091 2A6,4F2
STK101 2A6,4F3
STK111 2A6,4F4
STK121 2A7,4F5
STK131 2A8,4F7
STK141 2A8,4F8
STK151 2A8,4F9

NOTES: 1. P/N 19-200 OR 19-273 MAY BE USED IN POSITIONS 03J, 02K, 01K, AND 00J DEPENDING ON AVAILABILITY. MIXING OF 19-200'S AND 19-273'S ON THE SAME UNIT IS NOT RECOMMENDED. CONNECTIONS ARE AS SHOWN FOR 19-200 I.C. (OUTER BOX) AND 19-273 I.C. (INNER BOX).

SCALE — | DRAFT: QSTINE

TITLE: FUNCTIONAL SCHEMATIC 3200 SELCH

35-732M02R01D08 | SHEET 3 OF 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

6L3 ENBDO

14W 19-118 XCEIVER
8C1 DT081
8C4 DT091
8G1 DT101
8G4 DT111
115-0 D080
215-0 D090
116-0 D100
216-0 D110
DR081 F1, 5C2, 9H5
DR091 F3, 5C3, 7B1, 9H6
DR101 F3, 5C3, 7B4, 9H6
DR111 F5, 5C3, 7B5, 9H6
11L5, 13D2

13W 19-118 XCEIVER
8K1 DT121
8K4 DT131
8N1 DT141
8N4 DT151
117-0 D120
217-0 D130
118-0 D140
218-0 D150
DR121 F6, 5C5, 7B3, 9A2, 9H7
DR131 F7, 5C5, 7B2, 9A3, 9H8
DR141 F8, 5C5, 9A3, 9H8
DR151 F9, 5C5, 9A3, 9H8

7N9 MSCO
6N5 AT$YNO
6L1 SRGO
07A 19-059 SA

6N7 PWWOA
11L7 AAR230
05F 19-153 LSG

XRP 8J6
05F 19-153 LSG

7N7 BSY1
7F4 MWRT1
09H 19-160 LSA

5H7 BSYWT1

3D9 STK001
3K9 STK081
D2 DR081
3D9 STK011
3K9 STK091
D2 DR091
4 TO 1 MUX

3D9 STK021
3K9 STK101
D2 DR101
3D9 STK031
3K9 STK111
D2 DR111
4 TO 1 MUX

3G9 STK041
3N9 STK121
D4 DR121
3G9 STK051
3N9 STK131
D4 DR131
4 TO 1 MUX

3G9 STK061
3N9 STK141
D5 DR141
3G9 STK071
3N9 STK151
D5 DR151
4 TO 1 MUX

04J 19-177
04K 19-177
04H 19-177
05H 19-177

04W 19-118 XCEIVER
PDR081 3A1, 8A1
PDR091 3A1, 8A3
PDR101 3A2, 8D1
PDR111 3A2, 8D3
PD110 216-1
PD100 116-1
PD090 215-1
PD080 115-1
TWO RM 1 330
21-099F09
P5

6M4 ENBPDO

04T 19-118 XCEIVER
PDR121 3D1, 8H1, 8F6
PDR131 3D1, 8H3, 15E7
PDR141 3D2, 8L1, 15E7
PDR151 3D2, 8L3, 15E7
PD150 218-1
PD140 118-1
PD130 217-1
PD120 117-1
TWO RM 1 330
21-099F09
P5

SCALE –	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	KRISTINE	DRAFT	
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC 3200 SELCH

TASK NO. C2071
DWG NO. 35-932M02 DOB
SHEET OF 4—16

BRUNING 44231 24538

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

NOTES:
1. SEE SHEET 16 FOR STRAPPING INFORMATION.

SCALE—
TOLERANCE: XXX ± .005, .XX ± .02, .X ± .05, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
ASTINE	DRAFT	
	CHK	
	ENGR	

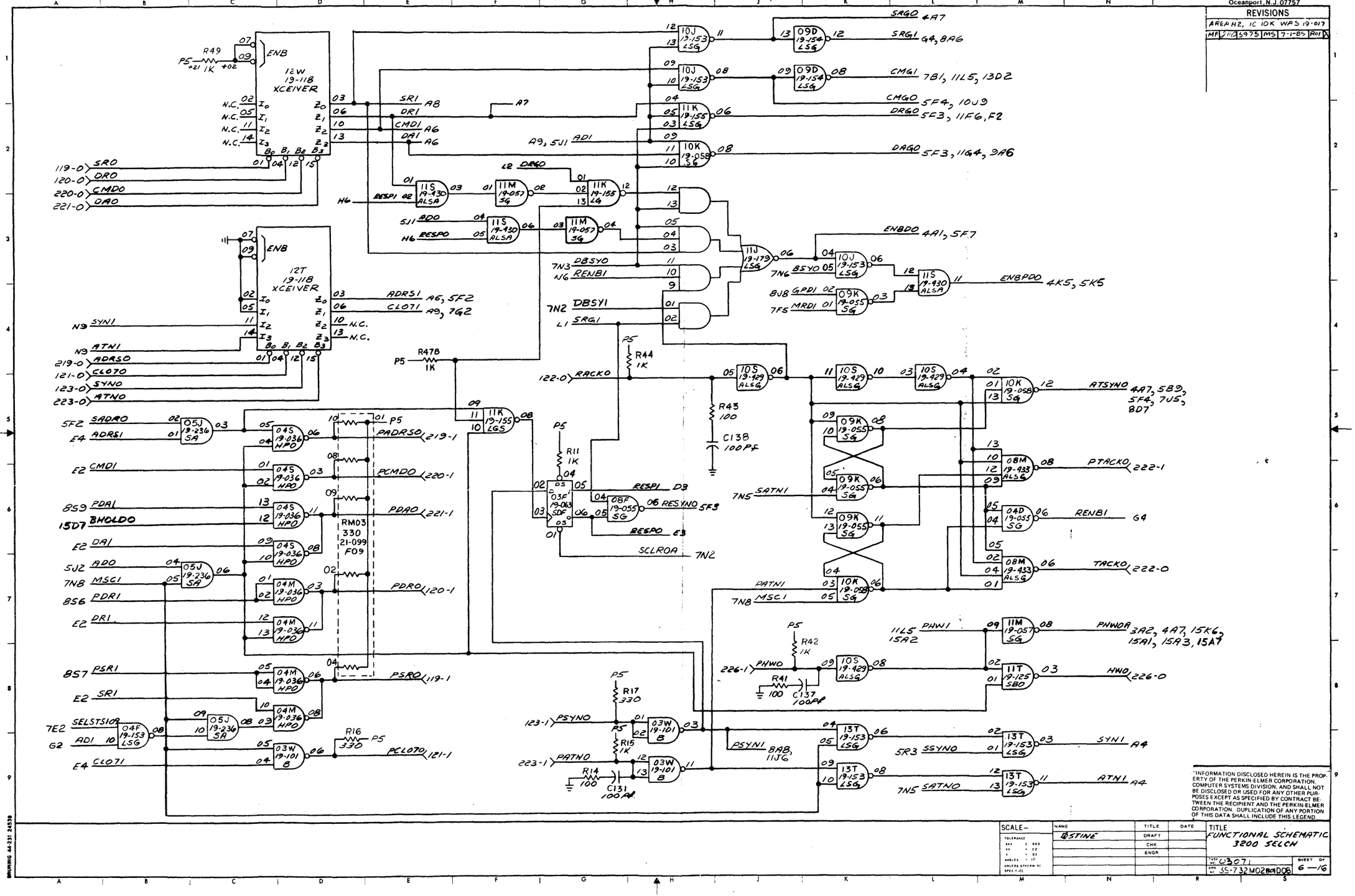
TITLE
FUNCTIONAL SCHEMATIC
3200 SELCH

TASK NO 03071
DWG NO 35-732M02 D08
SHEET 5 OF 16

RUNNING 44231 24538

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA H2, IC 10K WAS 19-017				
MF	JNA5975	MS	7-1-85	R01



SCALE–	NAME	TITLE	DATE	TITLE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	WESTINE	DRAFT		FUNCTIONAL SCHEMATIC 3200 SELCH
		CHK		
		ENGR		
				TASK NO. 03071
				DWG NO. 3S-732M02B4D06 SHEET OF 6—16

BRUNING 44-231 24539

PERKIN ELMER
Computer Sysiems Division
Oceanport, N.J. 07757

REVISIONS				
AREA H2, ADDED X-REF 63 TO IC 014-3. IC 09E-02 WAS MNEMONIC XRP, X-REF 8J6.				
MR	MS 5975	MS	7-1-85	R01

P5 R8 1K
4D2 DR091 — 03E 19-165 LSDF — EXRD1 11K1
6L1 CMG1 — N.C.
N2 SCLR0A
4D5 DR131 — SELSTS1 8A6, 6A8
SELSTS0 8A7
4D4 DR121 — N.C.
4D2 DR101
N8 MSC1 — 07F 19-155 LSG — 00B 19-055 SG — MWRT1 3A5, 4A9, 8M6, 13D1, 13K8, 14A2, 15G5, 3K1
MWRT1 Ø(ØBA)
11G4 DARG0 — MRD1 2D8, 2K8, 6J4, 8H8, 13D1, 13L1, 14K8, 15E3
4D2 DR111 — 05J 19-236 SA
R26 P5 6.8K
N.C. — EXC EXR — 07B 50ns 19-042
10MB SETG01 — CMDG01 8F6, 14K8
5R2 XRPC
XRPB 15N5
15E5 EDX1 — 09B 19-062 SDF — N.C.

01A 19-153 LSG — SSTOP1 12L3
11G4 DARG0 — SSTOP0 G3
01A 19-153 LSG
6E4 CL071 — 09F 19-057 SG
12G3 NOMEMO — 09E 19-156 LSG
11M3 ACRY0
J2 SSTOP0
01C 19-058 SG
N6 BSY0 — 05E 19-061 SB
14R9 DMACT0
14H8 SDRQ0
15N5 HLTI01 — 03D 19-055 SG

SETATN0
R2A 1K P5
12C 19-059 SA — 01A 19-153 LSG — 03D 19-055 SG — CLRS0A 10S9, 14F3
D7 SCLR0 — 10T 19-236 SA — CLRS0 11G5, 13L7, 14R8, 15K5
SCLR0A B2, J8, 5F2, 11A7, GH7, 12C9, 13L3, 10J5, 13M4
DBSY1 3A8, 8H2, 10A2, 14F8, 6G4
11H 19-153 LSG — TERM1 14A2
09F 19-057 SG — DBSY0 6G3
MWTHLT0 14K3
R09 P5 6.8K
N.C. — EXC EXR — 02F 50ns 19-042
P5 R10 1K
15B5 XRPA — N.C.
6N5 ATSYN0 — 02E 19-165 LSDF — SATN1 6J6
N9 MSC0 — SATN0 6L9

15N5 HLTI00 — 05E 19-061 SB — BSY0 G3, J8, 6J4, 5J8
BSY1 Ø(ØBA)
06D 19-055 SG — BSY1 4A8, 8A9
00A 19-125 SB0 — LEA BSY0 224-1 FOR HIGH SPEED PROTOCOL EIA ØBA — SEE NOTE 1
SEE NOTE 1
R1 1K P5
06C 19-058 SG — MSC1 8A4, 6A7, 6J7, 8A6
MSC0 Ø(ØBA)
06D 19-055 SG — MSC0 H6, 4A7, 8A7, 5D9
CMDG00 13L3

SCLR0 H2
126-0 — 11S 19-430 ALSA — EXTCLRØ — 09T 19-154 LG — 08S 19-125 SOB — PSCLR0 1126-1
E64 — R1A 1K — P5
E65

5J2 SGADO — 14C 19-154 LSG — 04F 19-153 LSG
N6 BSY0
N2 SCLR0A

SEE NOTE 1

NOTE:
1. SEE SHEET 16 FOR STRAPPING INFORMATION.

SCALE —	NAME	TITLE	DATE
TOLERANCE .XX ± .01, .X ± .02, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	ØSTINE	DRAFT	
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC 3200 SELCH
TASK NO. 03071
DWG NO. 35-732M02R01D08
SHEET OF 7 — 16

BRUNING 44-231 2453H

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
AREA J8, IC 06C WAS 19-017. AREA J6 DELETED X-REF 7H2 FROM MNEMONIC XRP					
MF	11	C5975	MS	7-7-5	R01
AREA J7, ADDED X-REF 3R6 TO MNEMONIC XRP					
DB	100	6059	M	7-2-85	R02 X

4N2 PDR081 — 07 ENB — 05 DT081 4A2 — 06 N.C. — 12H 19-173 LSTTL — SEL DATA 8 TO 1 MUX
11J1 AAR001
11E3 AAR081
11E8 AAR161
5A2 SID081

4N2 PDR101 — 07 ENB — 05 DT101 4A2 — 06 N.C. — 12J 19-173 LSTTL — SEL DATA 8 TO 1 MUX
11J1 AAR021
11E3 AAR101
11E8 AAR181
5A3 SID101
13N1 MMF1

4N6 PDR121 — 07 ENB — 05 DT121 4A4 — 06 N.C. — 12K 19-173 LSTTL — SEL DATA 8 TO 1 MUX
11E1 AAR041
11E6 AAR121
11L8 AAR201
5A4 SID121
7N2 DBSY1

4N6 PDR141 — 07 ENB — 05 DT141 4A5 — 06 N.C. — 12M 19-173 LSTTL — SEL DATA 8 TO 1 MUX
11E1 AAR061
11E5 AAR141
11L8 AAR221
5A5 SID141

4N2 PDR091 — 07 ENB — 05 DT091 4A2 — 06 N.C. — 13H 19-173 LSTTL — SEL DATA 8 TO 1 MUX
11J1 AAR011
11E3 AAR091
11E8 AAR171
5A3 SID091

4N2 PDR111 — 07 ENB — 05 DT111 4A2 — 06 N.C. — 13J 19-173 LSTTL — SEL DATA 8 TO 1 MUX
11J1 AAR031
11E3 AAR111
11E8 AAR191
5A4 SID111
13N2 PF1

4N6 PDR131 — 07 ENB — 05 DT131 4A4 — 06 N.C. — 13K 19-173 LSTTL — SEL DATA 8 TO 1 MUX
11E1 AAR051
11E6 AAR131
11L8 AAR211
5A5 SID131
15N5 HLTI00 — 05 — 04 09A 19-059 SA — 06
A9 BSY1 — 03 SA

4N6 PDR151 — 07 ENB — 05 DT151 4A5 — 06 N.C. — 13M 19-173 LSTTL — SEL DATA 8 TO 1 MUX
11E1 AAR071
11E5 AAR151
11L8 AAR231
5A6 SID151

7N8 MSC1 — 14H 19-155 LSG — 12
6L1 SR&1
7E2 SELSTS1 — 11H 19-153 LSG — 08
7E3 SELSTS0 — 14H 19-155 LSG — 06
7N9 MSC0
11M1 UAARXO — 14H 19-155 LSG — 08
11M1 UAARLO
11M1 UAARHO — 14J 19-156 LSG — 08
5F3 SELSRG0
5F3 DEVSRG0 — 14J 19-156 LSG — 06
6R5 ATSYNO

P5 — R13 1K — SNS0 — R12 100 — C130 100PF — 03W 19-101 B — OPTI E8, F7, 15G5
06E 19-154 LSG — 02 OPTOA V7, 15A7

PSYNOA — D3 23-034 — 06E 19-154 LSG
6U9 PSYN1 — 06D 19-055 SG — 06
7N7 BSY1
K5
L4 4.7uh 35NS — R28 330 — C136 47 PF

4N6 PDR121 — 06E 19-154 LSG — 04
N.C. — 09
S7 PSR1
15J7 BADSTO
7F6 CMDG01
D7 OPT1
15E4 EDX1
11A9 INHIB0
07D 19-062 SG — 08

03 — 09F 19-057 SG — 04 — DPS0 M6, 11K7
D7 OPT1 — 07E 19-155 LSG — 08 — DPS1 15G6
J6 XRP
5G DX1 — P5 D1 16C 19-165 LSD2 CK0 DC — 09 — N.C. — 13

15A1 DXDPS1 — 09A 19-059 SA — 06E 19-154 LSG
P5 — R24A 1K — 06B 19-155 LSG
3R6,4C7,E8 XRP — R23A 1K — P5
07E 19-155 LSG — 06
D8 OPTOA — 08B 19-155 LSG — 08
9N4 IOMCH0

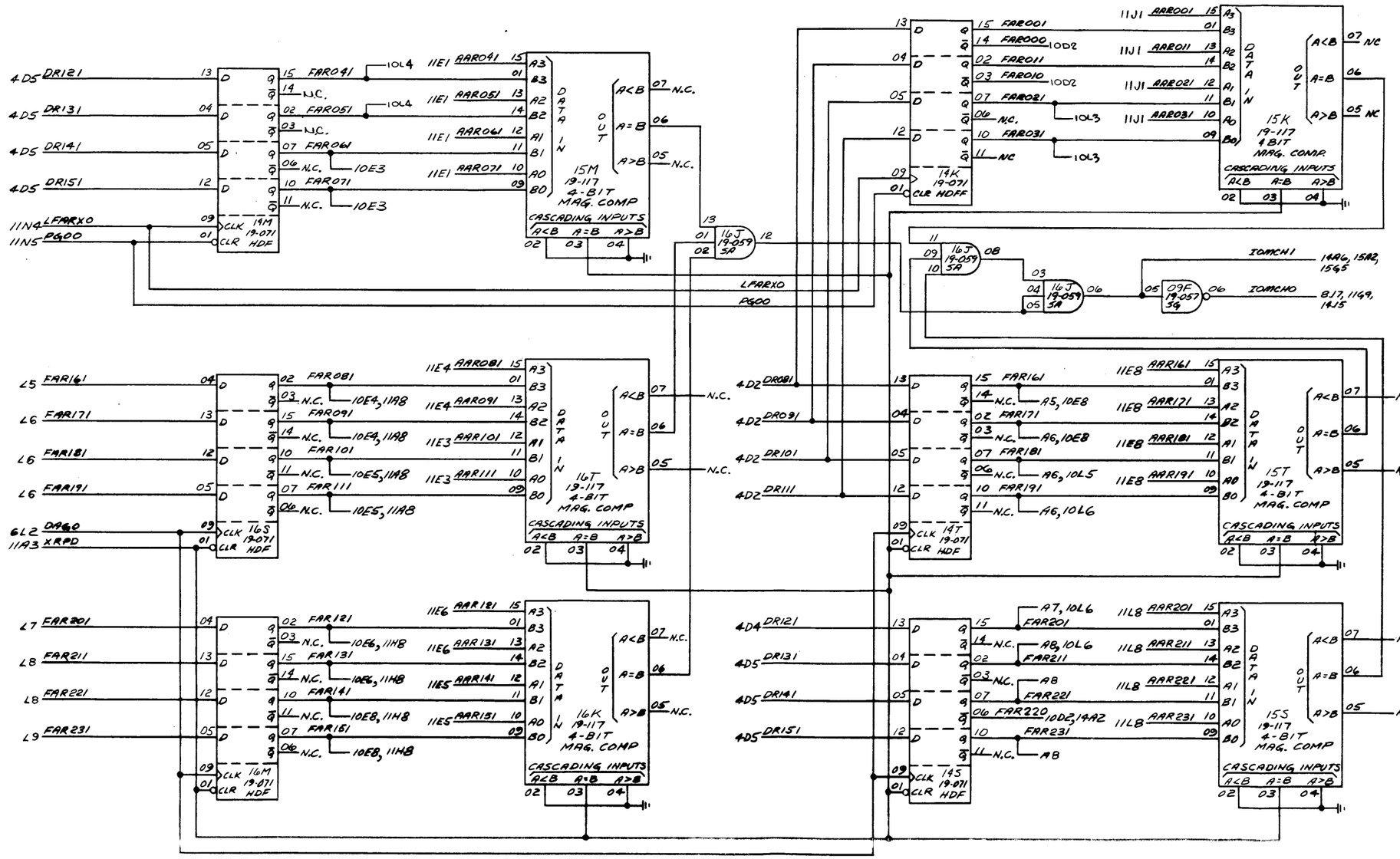
7F5 MRDI — 06C 19-058 SG — 06 — D2 23-034 — L3 15uh — C134 220PF — R25 470 — 06E 19-154 LSG — 08
3N1 STKVLDI
6PD1 6J4
06E 19-154 LSG — 10

3K1 STKFLO — 12A 19-934 — 08 — PDR1 6A7
7F4 MWRT1
F8 DPS0
DX1 — DX1 F8
06B 19-155 LSG — 12
07E 19-155 LSG — 08
06B 19-155 LSG — 08
13A 19-160 LSA — 06 — PSR1 F6, 6A8 15G6
SX1 — SX1 (08A)
06B 19-155 LSG — 06
07E 19-155 LSG — 12
06F 19-159 LS0R — 11 — PDAR1 11L6, 15G4
PDAL 6A6
13A 19-160 LSA — 11

SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE .XX ± .005, .X ± .02, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	ASTINE	DRAFT		FUNCTIONAL SCHEMATIC 3200 SELCH
		CHK		
		ENGR		
				TASK NO 03071 — SHEET OF 8—16
				DWG NO 35732N02.R02008

BRUNING 44.231 24538

REVISIONS



SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .1, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	C. MICHAELS	DRAFT	
		CHK	
		ENGR	

TITLE: FUNCTIONAL SCHEMATIC 3200 SELCH

03071

35-732M02 DO8

SHEET 9 OF 16

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
AREA R8. ADDED X-REF 3K1 TO MNEMONIC MAR220					
MF	1.42	5975	MS	7-1-85	RMK

11N5 PG00

11E1 AAR071
11E1 AAR061
11E1 AAR051
11E1 AAR041
13G2 MARCLKO
7N2 DBSY1
P5 R55 1K
11E3 AAR111
11E3 AAR101
11E3 AAR091
11E3 AAR081
11E5 AAR151
11E5 AAR141
11E6 AAR131
11E6 AAR121
12C9 SCLR0B
11EB AAR191
11EB AAR181
11EB AAR171
11EB AAR161

13F 19-070 4-BIT CNTR
13E 19-070 4-BIT CNTR
16F 19-070 4-BIT CNTR
16D 19-070 4-BIT CNTR

MAR071 L1, 2L2
MAR061 L1, 2L2
MAR051 L1, L4, 2L2
MAR041 L1, L3, 2L2

L3 MAR001
9L2 FAR000
L3 MAR011
9L2 FAR010
9K8 FAR220
R8 MAR221
11E 19-172 LSXOR

P5 R47A 1K
11D 19-156 LSG
11C 19-154 LSG

FWMCH0 14A2
HWMCH1 14A5
HWMCH0 14A2, 14A4

MAR111 2C2
MAR101 2C2
MAR091 2C1
MAR081 2C1
MAR151 2C4
MAR141 2C4
MAR131 2C3
MAR121 2C3
MAR191 L6, 13A8 2C6, 13A3
MAR181 L5, 2C6
MAR171 2C6
MAR161 2C5

9D3 FAR061
9D4 FAR071
9D5 FAR081
9D6 FAR091
9D6 FAR101
9D6 FAR111
9D8 FAR121
9D8 FAR131
9D8 FAR141
9D9 FAR151
9K5 FAR161
9K6 FAR171

15H 19-117 4-BIT MAG. COMP. CASCADING INPUTS
16H 19-117 4-BIT MAG. COMP. CASCADING INPUTS
15J 19-117 4-BIT MAG. COMP. CASCADING INPUTS

11B 19-059 SA

11H1 AAR031
11H1 AAR021
11H1 AAR011
11H1 AAR001

16E 19-070 4-BIT CNTR

MAR031 L2, 2J4
MAR021 L2, 2J4, E2
MAR011 L2, 2J4, E2
MAR001 L2, 2J4, E2

07H
G1 MAR071 E8 (H)
G1 MAR061 E7 (G)
G1 MAR051 E6 (F)
G1 MAR041 E5 (E)
MAR031A 12A1
MAR021A 12A1
MAR011A 12A1
MAR001A 12A1
L3 MAR031 (D) E4
L3 MAR021 (C) E3
L3 MAR011 (B) E2
L3 MAR001 (A) E1
SEE NOTE 1

9L3 FAR021
9L4 FAR031
G1 MAR041
9D2 FAR041
G1 MAR051
9D3 FAR051
11F 19-117 4-BIT MAG. COMP. CASCADING INPUTS

7N2 SCLR0A
11LB AAR211
11LB AAR201

12E 19-070 4-BIT CNTR

EB MAR181
9K6 FAR181
EB MAR191
9K6 FAR191
MAR201
9K7 FAR201
MAR211
9K8 FAR211
12B 19-117 4-BIT MAG. COMP. CASCADING INPUTS

2C8, 13A4 MAR211
2C7, 13A4 MAR201
12C 19-059 SA

7B6 SETGO1
11D8 AAR221
14A7 HWFF1
14A7 HWFF0
09H 19-160 LSA
10H 19-153 LSG
11C 19-154 LSG
11B 19-059 SA

11D 19-013 CR K O

MAR221 D3, 2D8
MAR220 13D4, 14J4, 3K1
CLR0A 7N1
CLK1B1 14K7

6L2 CN60

N.C.

NOTES; 1. SEE SHEET 16 FOR STRAPPING INFORMATION

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	ASTINE	DRAFT	
		CHK	
		ENGR	

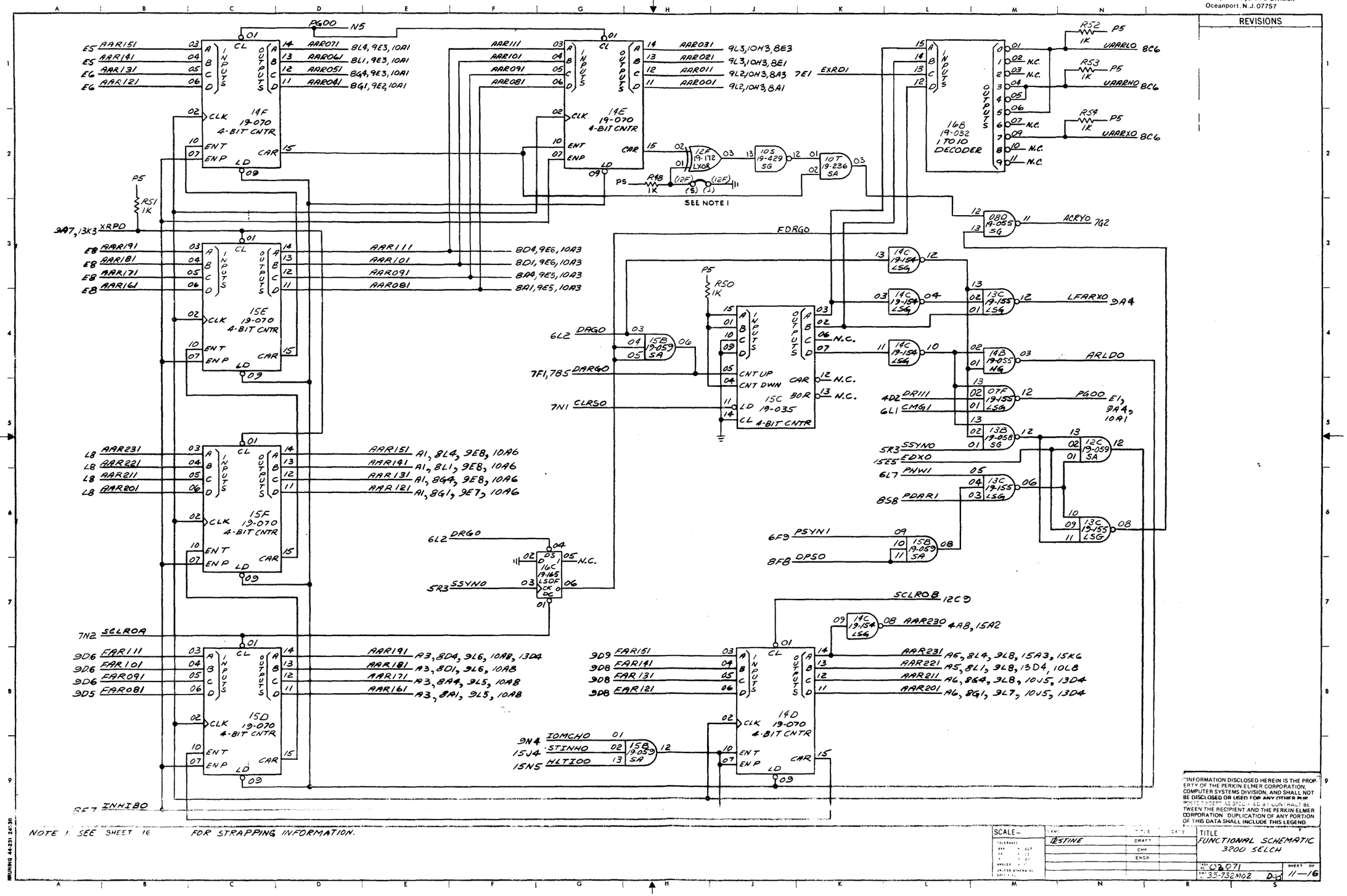
TITLE: FUNCTIONAL SCHEMATIC 7200 SELCH

TASK NO. 0407 | SHEET OF 10—16

DWG NO. 35-732M02K01D08

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



NOTE 1. SEE SHEET 16 FOR STRAPPING INFORMATION.

SCALE	–
DESTINE	DRAFT
	CHK
	ENGR
TITLE	FUNCTIONAL SCHEMATIC 3200 SELCH
DWG NO.	02071
REV	D
SHEET	11 OF 16

BRUNING 44-231 24-30

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
AREA H1, ADDED X-REF 2N4 TO MNEMONIC M01
MF [illegible] 5975 MS 7-1-85 ROI

07J 19-032 1 OF 10 DECORER

06H 19-032 1 OF 10 DECODER

06J

07K 19-068 AND-OR-INVERTER

06W 19-118 XCEIVER

06S 19-069 8 TO 1 MUX

SEE NOTE 1

"SEL" LED1 33-027

NOTES. 1. SEE SHEET 16 FOR STRAPPING INFORMATION.

	NAME	TITLE	DATE
SCALE–	@STINE	DRAFT	
		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC 3200 SELCH

DWG NO 03071 SHEET OF 12—16

DWG NO 35-732M02R01.03

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

7D5 MRDI
14H3 TLOADI
7F4 MWRTI
14H5 GADRI
14R7 HWFFI
06A 19-062 SG
MARCLKO 10A6

14G2 CSCØ
14H1 CSBIA
14H1 CSAI
14R7 HWFFO
12A 19-434 FA

6L1 CMGI
4D2 DRIII
5R3 SSYNO

10C7 MAR211 — 11C 19-154 LG
10C7 MAR201 — 11C 19-154 LG
10E8 MAR191 — 11C 19-154 LG
09T 19-154 LG
09T 19-154 LG
09T 19-154 LG

11L8 AAR221
1058 MAR200
11L8 AAR211
11L8 AAR201
11E8 AAR191
13D 19-133 4-BIT ADDER
XRPD 11B3
N.C.

12D 19-117 4-BIT MAG COMP CASCADING INPUT
SGTRBI 14A7
SEQBI 14A7
SLTBI 14K4

09S 19-127 XORS
09S 19-127 XORS
09S 19-127 XORS

P5 R24 1K
14H6 ENBDMAO
(@5A) I0
(@5A) I1
I2 P5 (@5A)
I3 N.C.
MODULE I.D. CODE STRAP
SEE NOTE 1
10W 19-118 XCEIVER
B0 B1 B2 B3
130-0 IDOOO
131-0 IDO10
231-0 IDO20
N.C.

12N4 PAGEO1
12N4 PAGE11
10E8 MAR191
N.C.
12N7 SEL1
1267 XRPE
08K 19-071 HDF

2R2 DMXR151
2R2 DMXR141
08J 19-127 XORS
08J 19-127 XORS
08J 19-127 XORS
09S 19-127 XORS
08J 19-127 XORS
08J 19-127 XORS

09M 19-128 SG
P5 R37 1K
09J 19-058 SG
XBNDRY1 14A3,14A7

2M2 DMXR121
7F5 MRDI
M6 RANSI
08D 19-055 SG
R30 1K P5
09E 19-043 CK
NMFI 8D2

2R2 DMXR131
7N9 CMD&00
7N2 SCLR0A
09H 19-160 LSA
09C 19-043 CK
PFI 8D4

2U8 ANSRI
M5 W4ANSI
09C 19-043 CK
N.C.

14H6 SW4ANSO
14H4 RW4ANSO
10C 19-043 CK
N.C.

08D 19-055 SG
RANSI J1,14K6
08D 19-055 SG
RANSO 15E1, 15E8

7N2 CLR50
09H 19-160 LSA

7F4 MWRTI
14H2 TEOTI
09J 19-058 SG
WTEOTO 14K7
08S 19-125 SBO
EOTO (203-1

08F 19-055 SG
P5 R34 1K
09E 19-043 SDF
IANSRI 15E8
IANSRO 15E8, 14H9
00A 19-125 SBO
P5 R21 330Ω
(224-4) LED 2 PARITY FAIL INDICATOR
33-027
(223-4)
7N2 SCLR0A
11M 19-057 SG
P5 R31 1K (@6A)
(@6A) PARCLR
W4ANSI G7 14H9
10C 19-043 CK
N.C.

NOTE 1. SEE SHEET 16 FOR STRAPPING INFORMATION.

SCALE—
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

	NAME	TITLE	DATE
	@STINE	DRAFT	
		CHK	
		ENGR	

TITLE
FUNCTIONAL SCHEMATIC
3200 SELCH

TASK NO. 03071 SHEET OF
DWG NO. 35-732M02 DOB 13 —16

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

SEE NOTE 1

7F4 MWRT1
R7 HWFF1
7N2 TERM1
10L2 FWMCH0
9K8 FAR220
10L2 HWMCH0
N.C.
13J9 XBNDRY1
N.C.
N.C.
N.C.
N.C.
PS R18 1K

03A 19-199 F07 PLA

CSA1 13A2
CSB1
CSC0 13A2
CSB0

(SEE NOTE 2)
008 19-055 SG — 11 CSB1A 13A2

02C 19-055 SG — 03 CSA0A
N.C.
TE0T1 13K8
TE0T0 12H8

02A 19-131 SDF
15M8 DMACLK1
7N1 CLRS0A

TLOAD1 2K8, 13A1
N.C.
LDMAB1 2C9
N.C.
RINH1 15E8
N.C.
N.C.
RW4ANS0 13L6

02B 19-131 SDF

04E 19-059 SA — CS01 15E7

7N3 MWTHLT0 — 02C 19-055 SG
10L2 HWMCH0
10S8 MAR220 — 04F 19-153 LSG

13K5 SLTB1
9N4 IOMCH0
R9 DMACT0

02D 19-132 SG

10L3 HWMCH1
13N6 RANS1

GADR1 13C1, 12H1
GADR0 2D2
N.C.
ENBDMR0 2H1, 13A5
N.C.
SW4ANS0 13L5
N.C.

05B 19-131 SDF

03A 19-199 F07 PLA

9N4 IOMCH1
15N5 HLTI01
3N1 STKYLR1
H9 IM401
13J9 XBNDRY1
V7 DMFIN1
13K4 SGTRB1 — 06F 19-159 LSOR
13K4 SEQB1

09A 19-199 F06 PLA

05 09F 19-153 LSG — 06
04

DMFIN1 A7, 15G6
N.C.

03A 19-043 SDF CK D DC

1059 CLK1B1 — 00B 19-055 SG
13R8 WTEOT0
7R5 MRD1
7F6 CMDG01
12S4 NOMEM0 — 07F 19-155 LSG

07A 19-059 SA

12 DS D 1 03C 19-043 SDF CK Q DC 08 HWFF0 2K7, 10M9, 13A2
09 HWFF1 A2, 2KB, 10V8, 13D2, 3J2
13 CLRS0 7N2

04C 19-058 SG — DMARQ1 12H5

SDRQ0 7G3
D1 23-034
L1 4.7uH
C128 100pF
R3 470

7N2 DBSY1

04E 19-059 SA — 08

02C 19-055 SG — 06
09
04C 19-058 SG — 08

12N8 SELO

04C 19-058 SG — 12

02E 19-059 SA — 12 DMACT0 J5, 7G3

R19 22K
C132 100pf
PS

EXC EXR
15J16 STEREO
2A9 XRPF
05C 700ns 19-042

SC4 XRPE
03F 19-043 SDF
NC
NC
15M5 FINCLR0

A7 IM401 — 00C 19-132 ALSA — 06
13M5 W4ANS1
13N4 IANSR0

02C 19-055 SG — 11

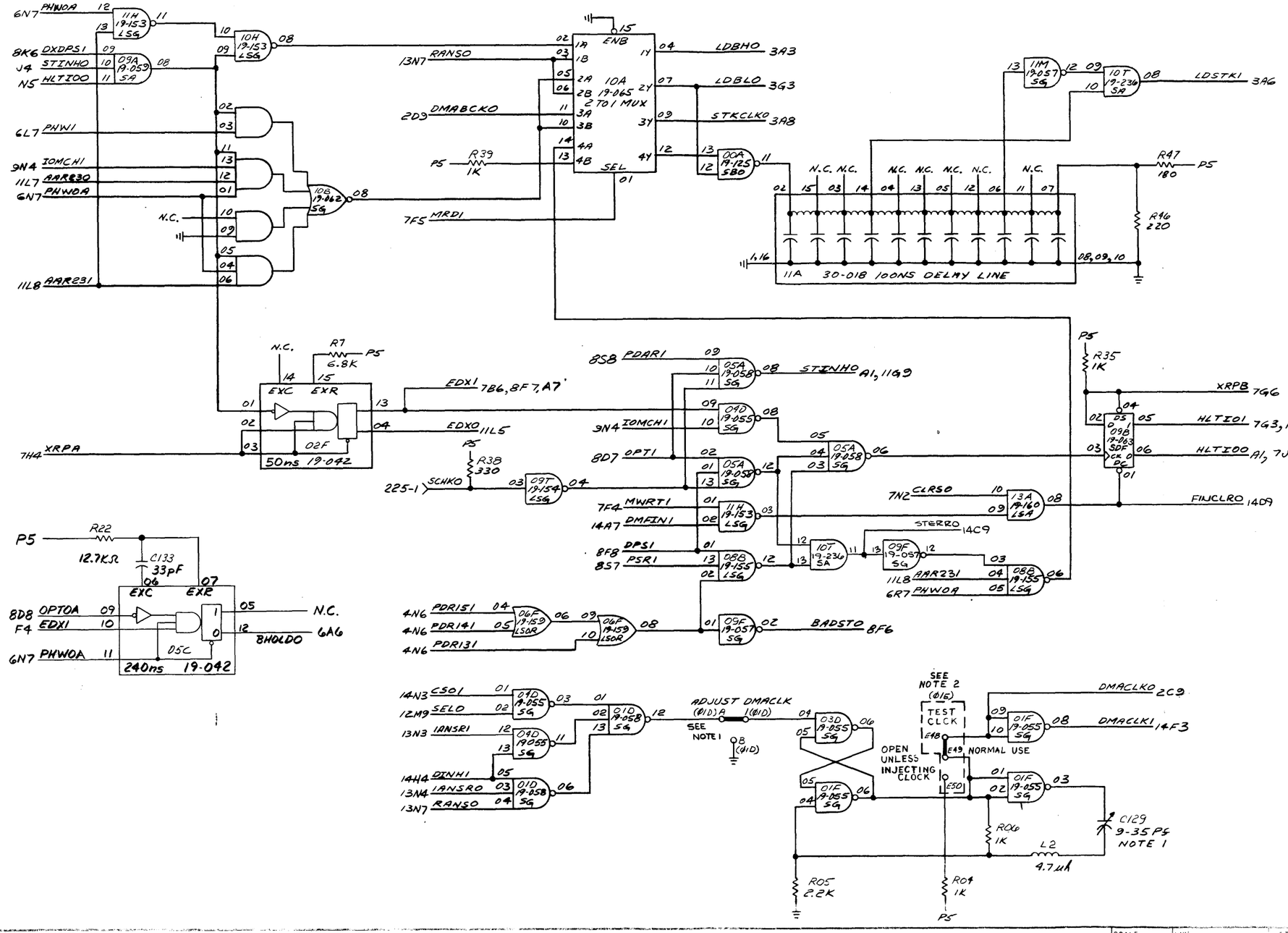
NOTES;
1. SEE SHEET 16 FOR STRAPPING INFORMATION.
2. CSA = 1BIT
CSB = 2BIT
CSC = 3BIT

SCALE–	NAME	TITLE	DATE	TITLE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPEC'F'D	ADSTINE	DRAFT		FUNCTIONAL SCHEMATIC 3200 SELCH
		CHK		
		ENGR		
				REF NO 03071
				DWG NO 35-732M02 008
				SHEET OF 14—16

RUNNING 44231 24938

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



NOTES:
1. ADJUST DMACLK1 FOR A PERIOD OF 80NS ±10%.
2. SEE SHEET 16 FOR STRAPPING INFORMATION.

SCALE—	NAME	TITLE	DATE
	DESIGNED	FUNCTIONAL SCHEMATIC 3200 SERIES	
	DRAWN		
	CHK		
	ENGR		
	PROJ NO 02071		SHEET OF 15—16
	DWG NO 35-732M02	008	

BRUNING 44-231 24538

DEVICE ADDRESS				
FROM	TO	LOC. SHT	LOC. BRD	COMMENTS
	E15-1	5	11A	} 0 (X'0F0')
E15	E15-0			
	E14-1			} 0
E14	E14-0			
	E13-1			} 0
E13	E13-0			
	E12-1			} 0
E12	E12-0		11A	
E11	E11-1		10A	} 1
	E11-0			
E10	E10-1			} 1
	E10-0			
E09	E09-1			} 1
	E09-0		10A	
E08	E08-1		09A	} 1
	E08-0			
	E07-1			} 0
E07	E07-0			
	E06-1			} 0
E06	E06-0	5	09A	

DMA CLOCK				
FROM	TO	LOC. SHT	LOC. BRD	COMMENTS
NORMAL USE	CLK	15K8	01E	NORMAL USE
A	1	15H7	01D	
B	1	15H7	01D	ADJUSTMENT
O.U.I.C.	CLK	15K8	01E	EXTERNAL
NORMAL USE	(EXT. SOURCE)	15K8	01E	SOURCE INJECT

HIGH SPEED PROTOCOL - XBSY				
FROM	TO	LOC. SHT	LOC. BRD	COMMENTS
E1A	E2A	7M7	00A	NEW
REMOVE STRAP				OLD

RESET STAKES				
FROM	TO	LOC. SHT	LOC. BRD	COMMENTS
PARCLR	-||-	13M4	06A	PARITY ERRORS
E64	E65	7	01A	EXT. CLEAR

MODULE I.D. CODE				
FROM	TO	LOC. SHT	LOC. BRD	USED ON
I0	I1	13A6	05A	GND='0'
I1	I2			FOR
I2	-||-			3210 & 3230
I0	I1			P5='1'
I1	I2			FOR
I2	IP5			3220
I0	-||- OR IP5			X'0' TO X'7'
I1	-||- OR IP5			FOR
I2	-||- OR IP5	13A6	05A	3240 & 3250

MEMORY BANK DECODER				
FROM	TO	LOC. SHT	LOC. BRD	USED ON
H	4	10	07H	3220
G	3			
F	2			
E	1	10	07H	
S	J	11H2	12F	
S	J	REMOVE		3210, 3230, 3240, 3250
D	4	10	07H	
C	3			
B	2			
A	1	10	07H	

SYSTEM TYPE 3210, 3220 & 3230				
FROM	TO	LOC. SHT	LOC. BRD	COMMENTS
W	X	12J1	08W	GATED ADDRESS
Z	Y	12J1	08W	
B	2	14A3	04A	IM40
M	V	12G5	07K	MEMORY BUSY

SYSTEM TYPE 3240 & 3250				
FROM	TO	LOC. SHT	LOC. BRD	COMMENTS
W	Z	12J1	08W	GATED ADDRESS
X	Y	12J1	08W	
C	2	14A3	04A	IM40
M	T	12G5	07K	MEMORY BUSY

MEM. ADDRESS ALLOCATION (SHT. 12)				
COMMENTS	FROM	BRD LOC	TO	BRD LOC
BANK 0	00	06J	M00	05K
	01			
	02			
	03		M01	
BANK 1	04			
	05			
	06		M02	
	07			
BANK 2	08			
	09			
	10		M03	
	11			
BANK 3	12			
	13			
	14		NON	05K
	15	06J		

REVISIONS

NOTES 1. SEE 29-727 MANUAL FOR FURTHER INFO.

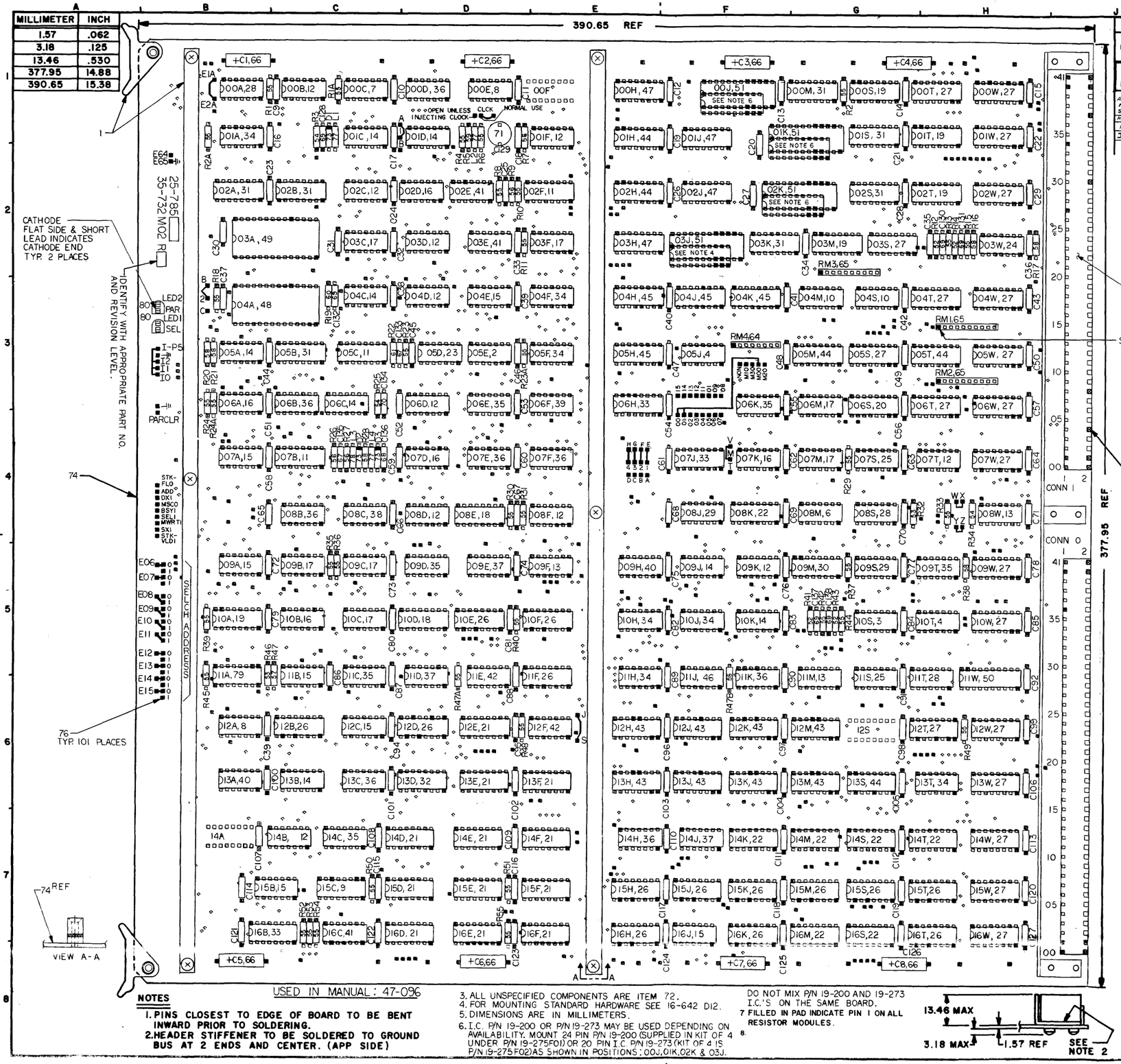
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE FUNCTIONAL SCHEMATIC 3200 SFLCH (STRAPPING INFORMATION)

DRAFTER: R. GOODMAN
DATE: 8-21-84

TASK 03071
DWG 35-732 M02 D08
SHT 16-16

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.95	14.88
390.65	15.38



USED IN MANUAL : 47-096

NOTES

1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
2. HEADER STIFFENER TO BE SOLDERED TO GROUND BUS AT 2 ENDS AND CENTER. (APP SIDE)
3. ALL UNSPECIFIED COMPONENTS ARE ITEM 72.
4. FOR MOUNTING STANDARD HARDWARE SEE 16-642 D12.
5. DIMENSIONS ARE IN MILLIMETERS.
6. I.C. P/N 19-200 OR P/N 19-273 MAY BE USED DEPENDING ON AVAILABILITY. MOUNT 24 PIN P/N 19-200 (SUPPLIED IN KIT OF 4 UNDER P/N 19-275F01) OR 20 PIN I.C. P/N 19-273 (KIT OF 4 IS P/N 19-275F02) AS SHOWN IN POSITIONS: 00J, 01K, 02K & 03J.
7. FILLED IN PAD INDICATE PIN 1 ON ALL RESISTOR MODULES.
8. DO NOT MIX P/N 19-200 AND 19-273 I.C.'S ON THE SAME BOARD.

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	[illegible]	10/5/84
PROD	[illegible]	10/5/84

RELEASED FOR PRODUCTION

MFG. ENG. [illegible] DATE 11/30/84

AREA G8, DELETED NOTE 8, "PH. NYLON SCREW TO BE MOUNTED TO CENTER STANDOFF OF FRONT AND MIDDLE STIFFENERS ON SOLDER SIDE ONLY." REFLECTED 80486 CHANGE

MF	JRB	5975	MS	7-1-85	A01
AREA G8 MANUAL WAS 29-727					
JT	JRB	6047	R	9-11-85	R02

RESISTOR	R1-R55
	RM1-RM4
INDUCTOR	L1-L4
DIODE	D1-D3, L.E.D.1, L.E.D. 2
CAPACITOR	C1-C138
INTEGRATED CIRCUIT	00A-16W
COMPONENT	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED

SCALE: 2/1

TOLERANCE:

DIMENSIONS ARE IN MILLIMETERS

.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
R.W.G. E.JOHNSON	DES/DFT	2-9-84
R. CERO	SUPV	4-5-84
	CHK	
R. BOYD	ENG	11-30-84
B. LEPOW	MGR	11-30-84
R. BARKER	QC	11-30-84

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE **ASSEMBLY PRINTED CIRCUIT BOARD** 3200 SELCH

TASK 03071

DWG 35-732M02 R02 E03

SHT 1-1

METRIC

CAUTION
PRINTED CIRCUIT PATHS AND PADS ARE SHOWN FOR REFERENCE INFORMATION ONLY.
PERKIN-ELMER'S INTERNAL REFERENCE

PERKIN-ELMER

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