Publication Number H29-277R09

METRIC

M47-000 and M47-001 SYNCHRONOUS DATA SET ADAPTER MAINTENANCE MANUAL

Consists of:

Installation Specification	02-252A20
Maintenance Specification	02-252A21
Schematic	02-252R09D08

PERKIN-ELMER

Computer Systems Division
2 Crescent Place
Oceanport, N.J. 07757

PAGE REVISION STATUS SHEET

PUBLICATION NUMBER H29-277

TITLE M47-000 and M47-001 Synchronous Data Set Adapter Maintenance Manual

REVISION R09 DATE October 1979

PAGE	REV.	DATE
i/ii	R08	5/79
02-252A20 Synchronous Data Set Adapter 201/ 301 Installation Specification		
1	R00	7/72
2	R00	7/72
3	R00	7/72
4	R00	7/72
5	R00	7/72
6	R00	7/72
02-252A21 Synchronous Data Set Adapter 201/ 301 Maintenance Specification		
1	R00	7/72
2	R00	7/72
3	R00	7/72
4	R00	7/72
5	R00	7/72
6	R00	7/72
7	R00	7/72
8	R00	7/72
9	R00	7/72
10	R00	7/72
11	R00	7/72
12	R00	7/72
13/		
14	R00	7/72
02-252D08 Functional Schematic Data Set Adapter 201/301		
1-9	R09	10/79

PAGE	REV.	DATE

PAGE	REV.	DATE

A1598

PREFACE

This manual contains the information required to install and maintain the Perkin-Elmer Synchronous Data Set Adapter (201/301). The installation specification contains a general description, unpacking, strapping options, mother-board and cable installation and ordering information. The maintenance specification contains block diagram analysis, a functional schematic analysis, a circuit analysis, timing, maintenance, adjustment and test information, and a mnemonics list. A functional schematic is also included.

SYNCHRONOUS DATA SET ADAPTER (201/301) INSTALLATION SPECIFICATION

1. GENERAL

The Synchronous Data Set Adapter (Product Number M47-000 and M47-001) is a one mother-board controller that adapts the Multiplexor Channel Bus to the Bell 201 A/B or 301 A/B Data Set or the equivalent. It contains the serial/parallel converters, character buffers, level converters, and control circuits for full or half duplex operation of the Data Set. The difference between the 201 version (Product Number M47-000) and the 301 version (Product Number M47-001) is the type of level converters and connecting cables supplied which interface to the Data Set.

2. UNPACKING

When the Data Set Adapter is shipped in a Perkin-Elmer rack, installation is already complete. The installation may be checked by following this specification. When the Data Set Adapter is shipped separately, remove the packing material carefully, inspect for damage, and continue the installation, following this specification.

3. STRAP OPTIONS

Options are connected at the factory. To change strapped options refer to Figure 1 and 02-252D08, Sheets 6 and 7.

4. MOTHER-BOARD INSTALLATION

The Synchronous Data Set Adapter may be installed into any standard I/O slot. Remove the RACK0/TACK0 strap between back panel Pin 122-1 and 222-1 at the location assigned to the adapter.

5. CABLE INSTALLATION

5.1 201 Data Set Adapter (35-413)

Refer to Figure 2. Install the 17-197 cable 3.05m (10 ft) between the left hand connector on the 35-413 board and the 14-090 connector plate at the rear of the rack. Note that the cable connector slips through the hole in the plate so the plate is sandwiched between the connector and the metal hood.

Mount a pair of connector spacers (16-038) on the connector side of the plate and secure the spacers, connector, plate, and hood with the 4/40 - $\frac{1}{4}$ inch PHMS (ASA B1.1 - 1960) provided.

Install the optional 17-050 cable, or equivalent, between the connector plate and the Data Set. Fasten the cable to the connector spacers provided at the data set and at the computer connector plate. The 17-050 cable is supplied by Perkin-Elmer as an option.

The cable may be ordered from Perkin-Elmer as follows:

Product Number	Part Number	Length
10-054	17-050F02	15.24m (50 ft)

TABLE A — LOCATED NEAR IC A96

OPTION	CHAR FORMAT	SEND LAST BIT DETECTOR STRAPS			
		FROM	TO	FROM	TO
U	6 DATA + NO PARITY	S1	SA1	S2	SE1
V	6 DATA + PARITY	S1	SA0	S2	SB1
W	7 DATA + NO PARITY	S1	SA0	S2	SB1
X	7 DATA + PARITY	S1	SB0	S2	SC1
Y	8 DATA + NO PARITY	S1	SB0	S2	SC1
Z	8 DATA + PARITY	S1	SC0	S2	SD1

TABLE B — LOCATED NEAR IC A 94

OPTION	CHAR FORMAT	RECEIVE LAST BIT DETECTOR STRAPS			
		FROM	TO	FROM	TO
U	6 DATA + NO PARITY	R1	RA1	R2	RE1
V	6 DATA + PARITY	R1	RA0	R2	RB1
W	7 DATA + NO PARITY	R1	RA0	R2	RB1
X	7 DATA + PARITY	R1	RB0	R2	RC1
Y	8 DATA + NO PARITY	R1	RB0	R2	RC1
Z	8 DATA + PARITY	R1	RC0	R2	RD1

STRAP OPTIONS FOR DUPLEX, PARITY AND MISC.

TABLE C

FUNCTION	ACTION	FROM	TO	BOARD LOCATION
HALF DUPLEX	STRAP	HDX0	G	IC A66
	STRAP	0	A	IC A41
FULL DUPLEX	STRAP	0	B	IC A41
PARITY	STRAP	SP1	SP2	IC A63
NO PARITY	STRAP	RP	G	IC A81
	STRAP	SP1	G	IC A63
IF DATA SET DOES NOT HAVE RING OPTION	STRAP	RIN	+	IC A61
IF DATA SET DOES NOT HAVE DIBIT CLOCK OPTION	STRAP	DCT	G	IC A61

Figure 1. 201/301 Data Set Adapter Strap Options
(Sheet 1 of 2)

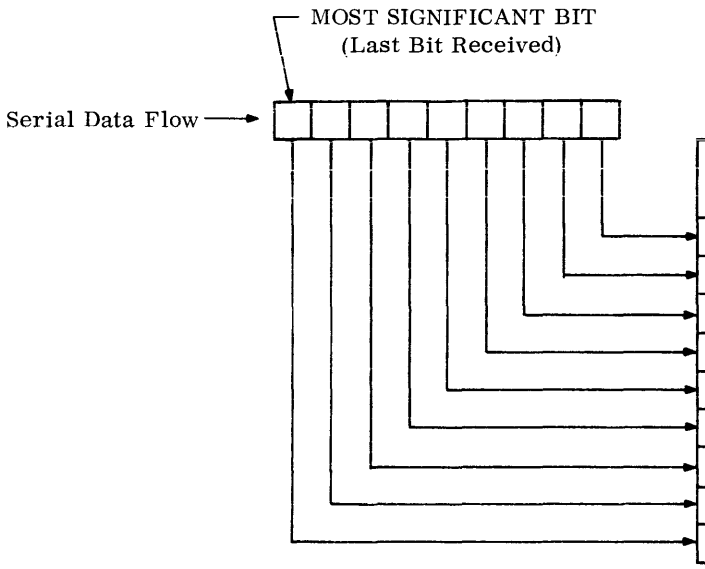


TABLE D
LOCATED NEAR IC A7

Connect Pin No. (-) To one of three options below

FROM	TO		
	1	0	"Don't Care"
(102)	001	002	+
(104)	003	004	+
(106)	005	006	+
(108)	007	008	+
(110)	009	010	+
(112)	011	012	+
(114)	013	014	+
(116)	015	016	+
(118)	017	018	+

TABLE E LOCATED NEAR IC A7

RECEIVE BUFFER REGISTER CONNECT ( ) TO PIN NO.								
OPTION	(115)	(113)	(111)	(109)	(107)	(105)	(103)	(101)
U	G	G	017	015	013	011	009	007
V	G	G	015	013	011	009	007	005
W	G	017	015	013	011	009	007	005
X	G	015	013	011	009	007	005	003
Y	017	015	013	011	009	007	005	003
Z	015	013	011	009	007	005	003	001

Figure 1. 201/301 Data Set Adapter Strap Options
(Sheet 2 of 2)

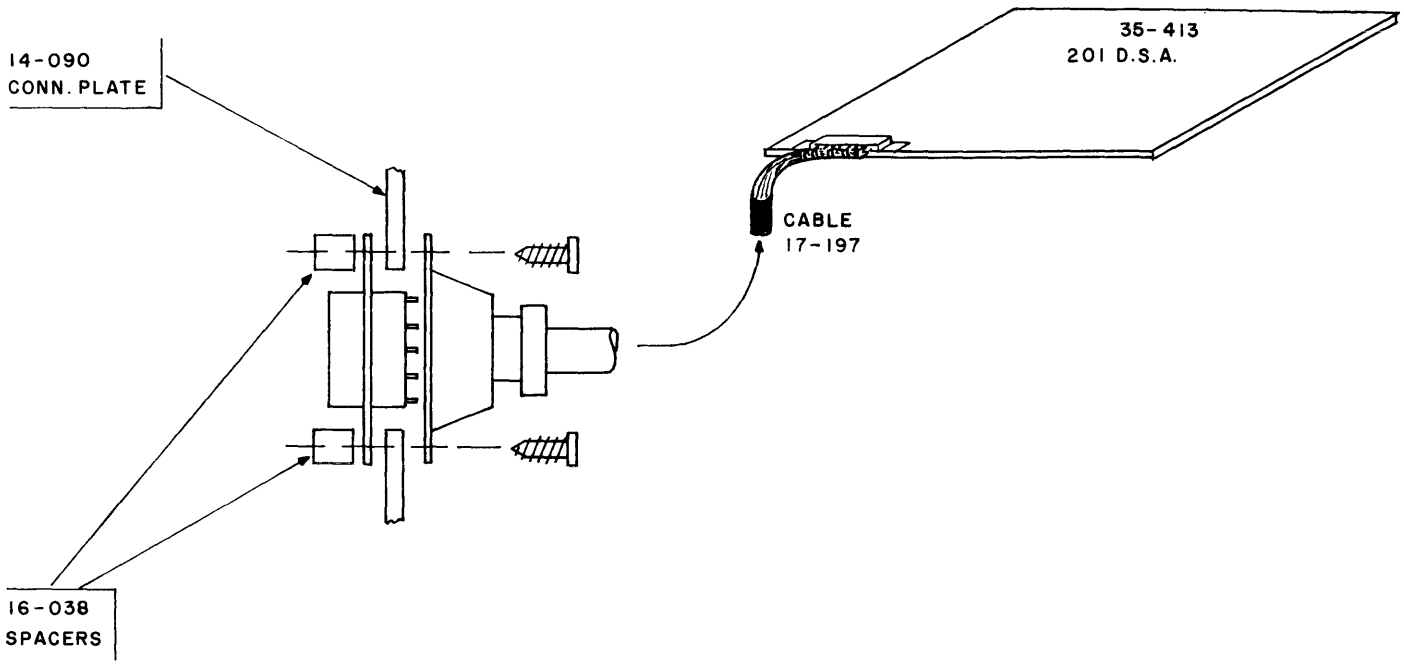


Figure 2. 201 Data Set Adapter Cable Installation

5.2 301 Data Set Adapter (35-414)

Refer to Figures 3, 4, and 5. Install the 17-198 cable 3.05m (10 ft) between the coax connectors CF through CA located on the right hand side on the 35-414 board and the 14-090 connector plate at the rear of the rack.

Install the 17-083 cable, or equivalent, between the connector plate and the data set. Fasten the cable to the connector spacer provided at the data set and at the computer connector plate.

This cable is supplied by Perkin-Elmer as an option. If the customer supplies this cable, he should refer to Figure 5 for connector plug specification to assure proper mating with the Perkin-Elmer back plate connector.

The cable may be ordered from Perkin-Elmer as follows:

Product Number	Part Number	Length
10-056	17-083F02	15.24m (50 ft)

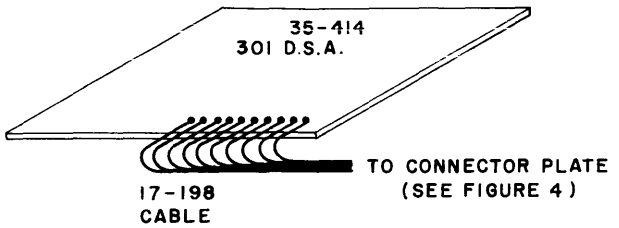
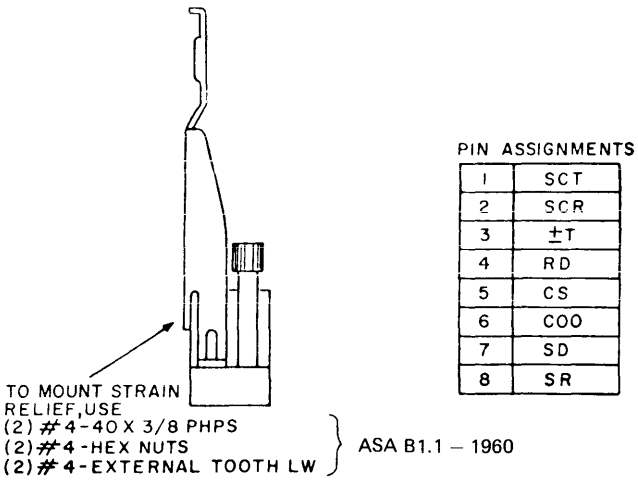
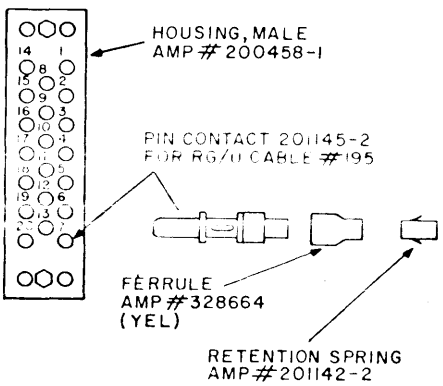
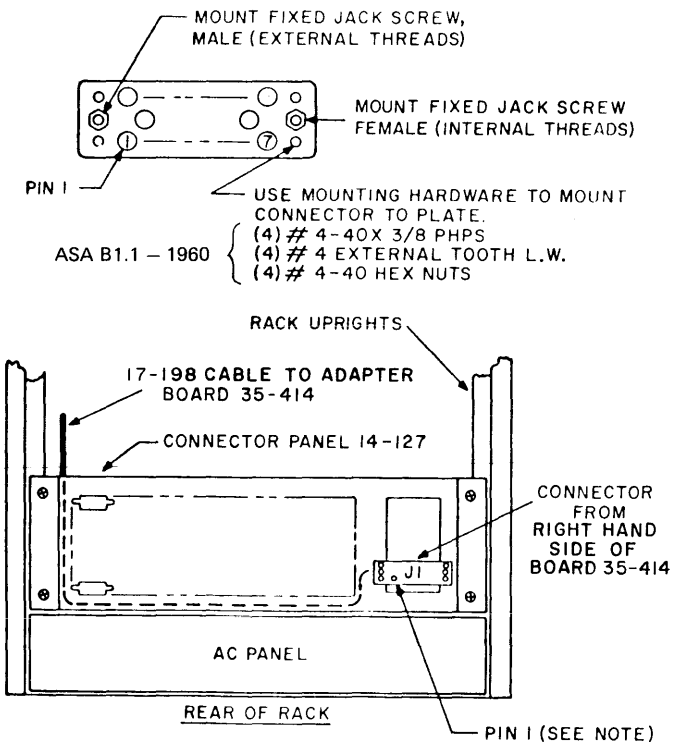


Figure 3. 301 Data Set Adapter Cable Information

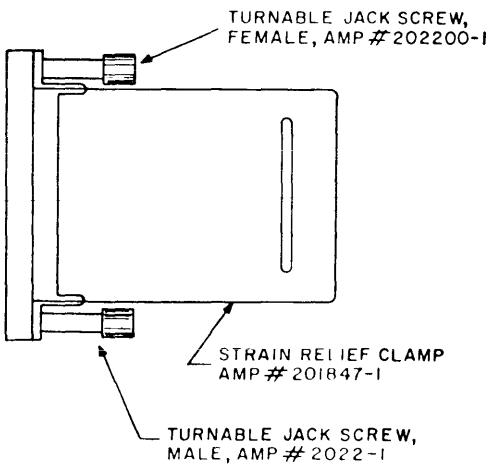






NOTE:
SEE CONNECTOR MOUNTING INFORMATION ABOVE. MOUNT CONNECTOR ON BOTTOM SET OF HOLES AND EXPAND UPWARDS AS REQUIRED. (TOTAL 5 CONNECTORS)

Figure 4. 301 Data Set Adapter Connector Information



CUSTOMER TO SUPPLY MALE HOUSING W/PIN CONTACTS AS SHOWN ABOVE. CRIMP TOOL #45639-2 IS REQUIRED TO CRIMP WIRE AND PIN CONTACT SPECIFIED ABOVE.

Figure 5. 301 Data Set Adapter Wiring Connector To Back Plate From Data Set

SYNCHRONOUS DATA SET ADAPTER (201/301) MAINTENANCE SPECIFICATION

1. INTRODUCTION

The Synchronous Data Set Adapter provides an interface between the Multiplexor Bus of a Perkin-Elmer Digital System and a half or full duplex synchronous data set. The 201 version of the adapter (35-413) meets EIA RS-232C specifications for connection to a 201 A/B Data Set or equivalent. The 301 version (35-414) meets necessary standards for connection to a 301B Data Set or equivalent.

Data transfer between the Synchronous Data Set and the Data Set Adapter is in the Bit Serial Mode with a synchronizing bit clock supplied by the Data Set for both sending and receiving. The Data Set Adapter also contains circuits to generate and detect control signals necessary to set up, take down, and supervise the data communications channel, and to provide proper status and interrupt information to the computer.

The 201 Data Set Adapter and the 301 Data Set Adapter differ in speed of operation, cable requirements, signal receivers and drivers, and certain control signals.

2. SCOPE

This specification covers the normal synchronous operation of the Data Set Adapter for Half-Duplex (HDX) and Full-Duplex (FDX) modes. It does not describe communication message procedures and techniques, since the Adapter is essentially transparent to characters passing through it. The only exception is the SYNC character detection and control used to decide which bits in the continuous bit stream are to be grouped together as a character. Special variations which require electrical and/or mechanical modification of the Adapter are not covered here. This specification provides a common building block for such special systems. The text of this specification applies equally to both the 201 Data Set Adapter and the 301 Data Set Adapter except where noted otherwise.

3. BLOCK DIAGRAM ANALYSIS

The Block Diagram for the 201/301 Data Set Adapter is shown in Functional Schematic 02-252D08.

Note that the Data Set Adapter is basically divided into two main parts, "Send" and "Receive". The Block Diagram is marked with "S" and "R" to show this division. The Full/Half Duplex Control determines whether the Send and Receive circuits are active independently (HDX) or simultaneously (FDX).

In the Receive Logic, data and bit clock pulses from the Data Set are converted from bipolar signals to DTL levels. The data enters the Shift Register and moves through it under control of the Receive Clock. After every data shift, the contents of the Shift Register are examined by the SYNC Character Detect circuit which is wired to recognize a particular pattern specified by the customer. This information is used to establish the initial message SYNC and to identify SYNC characters within the message. When the message SYNC has been established, the Bit Counter provides End of Character (EOC) and Last Bit (LASTB) pulses. The pulses gate the Shift Register into the Buffer Register and Control Parity circuit. The Buffer is subsequently gated to the Multiplexor Bus. The Buffer Active (BA) flip-flop provides the proper Busy status and interrupts. It also detects the Overflow (OV) condition if the Buffer has not been unloaded before the Shift Register assembles another character.

With the Parity Option, the parity of an assembled character is compared with a Programmable Parity Mode (odd/even) flip-flop, and a Parity Fail (PF) flip-flop is set if disagreement is detected. The PF condition is cleared by the System Initialize signal or any command to the Receive Logic.

For the Send or Write Mode, data from the Multiplexor Bus is loaded into the Buffer Register, gated to the Shift Register by the EOC pulse, and shifted to the bipolar data driver by the Data Set Send Clock. If the Buffer is empty when the Shift Register requires a new character, the OV flip-flop is set. The OV condition is cleared either by System Initialize, switching back to the Read Mode (Half-Duplex), or by any command to the Send Logic. The controller accepts a Read Mode command (HDX) while transmitting, but delays execution until both Buffer and Shift Registers are emptied.

With the Parity Option, parity is computed as the data bits are transmitted. After the last data bit is transmitted, the Parity Mode and Transmit Parity flip-flops gate the proper parity into the serial data stream to the Data Set.

The bipolar receivers convert the Data Set control signals to the DTL levels for RING, CARRIER, CLEAR TO SEND (CL2S), DATA SET RDY, DIBIT CLOCK (DCT), RECEIVE and TRANSMIT CLOCKS. These signals establish and terminate the connection, and appear in the controller status and interrupt circuits. Bipolar drivers convert the REQUEST TO SEND (RQ2S), DATA TERMINAL READY (DTR), and TRANSMIT DATA (TRANS) signals from DTL levels to the bipolar levels required by the Data Set.

Customer options are specified to indicate the number of data bits per character (6, 7, or 8), Parity Option, Half or Full-Duplex operation, and the code for SYNC Character.

The total number of bits in the character controls the length of the counter sequence and the time of gating the Shift Register to the Buffer Register. If the Parity Option is specified, the parity is generated and checked. However, the received parity bit is not loaded into the buffer.

The SYNC Character Code specified by the customer (using the same format as the data) can vary between six and nine bits in length. These options are not incorporated into the functional variations for the format wiring.

4. FUNCTIONAL SCHEMATIC ANALYSIS

This section relates to Functional Schematic 02-252D08. Note that most mnemonics throughout the schematic have a prefix of "S" or "R" indicating Send or Receive respectively. For simplicity of description, the following text refers to most of these mnemonics without the prefixes as their definitions are the same. They differ only in connection to their respective logic. When strapped for Full-Duplex, the Data Set Adapter is in both the Send and Receive Modes simultaneously. When strapped for Half-Duplex, the Data Set Adapter activates either the Receive logic or Send Logic separately. The schematic sheet number and grid location for referenced circuits are shown in parentheses.

4.1 Addressing

The Data Set Adapter is strapped to recognize two consecutive device addresses in the Full-Duplex Mode. To the Processor, the Data Set Adapter appears as two separate devices; one for Receiving, and one for Sending. Note that the Receive address must always be even, while the Send address must always be odd. The Perkin-Elmer preferred addresses are X'0E' (Receive) and X'0F' (Send)(1M1-1M5).

If the Data Set Adapter is to be operated in the Half-Duplex Mode, the address must be strapped to the same even address. The Perkin-Elmer preferred address is X'0E'.

4.2 Command Gates and Flip-Flops (Sheets 2 and 3)

The Status and Command bits are assigned as shown in 02-252A22, Synchronous D.S.A. Programming Specification. The Command gates and flip-flops include the gates to clear and set the DSBL/DSRM flip-flops (2G7) from data lines D08 and D09, the Synchronization Mode (SYNMD) flip-flop (3D8) which is cleared by (RCMG1)(D111), the Data Terminal Ready (RDY) flip-flop (2F2) under control of line D12, the Write Storage (WT) flip-flop (2F5) controlled by lines D141 and D151, and the Send-Receive flip-flop (2C7).

In the Half-Duplex Mode, the Send-Receive flip-flop (2C8) is slaved to the WT flip-flop when entering the Write Mode, but delays execution of the Read Mode Command since it is not cleared until both the Buffer and Shift Registers are emptied (WT0)(SBA0)(SE0C1). The SYNMD flip-flop is held cleared in the Write Mode to guarantee its state when the controller is switched to the Read Mode (Half-Duplex Only).

When the RDY flip-flop (2F2) is set, (CMG)(D131) initiates a timer, DSCN (2G2), which forces DTR0 low for at least 150 milliseconds. This causes the Data Set to break the connection ("Hang-up"). An interrupt occurs at the end of the disconnect timing. This disconnect timer will not be started if the RDY flip-flop is reset.

4.3 BSY, Status and Interrupt Cireuits (Sheets 2, 3, and 4)

The status and interrupt circuits collect signals from various parts of the controller to interrupt the Processor when action by the program is required.

During normal transfer of data, BSY (4A1, 4A2) is false (low) whenever a data transfer can occur; i.e. BA=1 in the Read Mode (3N5), BA=0 in the Write Mode (BA=Buffer Active)(3N3). The BSY bit is forced true during the 150 millisecond disconnect timing, or when CLEAR TO SEND is missing in the Write Mode or after a Read Mode Command (Half-Duplex) while the controller is emptying the Buffer and Shift Registers.

An interrupt condition sets one of the flip-flops in location 4B5. These are ORed to provide RSATN1 which sets the ATN flip-flop. Note that when operating Full-Duplex, two ATN flip-flops (2J7, 2J9) are used which queue separate interrupts from the Send and Receive logic. When operating Half-Duplex, all interrupts are queued in the Receive ATN flip-flop.

4.4 Gate Generators, BA and OV Flip-Flops (Sheets 1 and 3)

The Buffer Active flip-flops (3N3, 3N5) and the Overflow flip-flops (3N1, 3N4) control the parallel data transfer. In the Send Logic, the Buffer Register (1L9) is loaded by LSBR1 (due to a WD Instruction) and unloaded by SEOC1. The SBA flip-flop toggles set or clear with the trailing edge of these pulses. An Overflow occurs when the EOC pulse finds the Buffer full. On the Receive side, if the CARRIER signal disappears (GCARR1 low), no new overflows are detected, but any previous overflows are still recorded by the ROV flip-flop.

The EOC1 signal pulse occurs at the end of the Last Bit (LSTB1) signal from the Bit Counter circuit. This is discussed later.

The Reset (RST0/1) circuit generates a pulse and DC reset for the Bit Counter flip-flops. In the Read Logic, it is DC reset by A0 while the controller is in the SYNCH Search Mode (SYNMD0)(SC1). When synchronization is obtained, the RBA, ROV, and Character Counter flip-flops are allowed to operate when A0 goes high. A pulse reset occurs when the controller switches from the Read Mode to the Write Mode (Half-Duplex only). This establishes a known starting state of the SBA and SOV flip-flops and guarantees one character time to load the Buffer Register (WD Instruction) before the first EOC1 pulse occurs. The OV flip-flop could be set if the Bit Counter is not phased to the Read/Write Mode Switch.

4.5 Bit Counters, Last Bit Detectors, and SYNC Detector (Sheet 3)

The Bit Counters (3B2, 3B5), Last Bit Detectors (3G3, 3G5), and SYNC flip-flop (3B8) are shown on Sheet 3. The five stage Bit Counters are toggled by the GCLK1 signal. The true and false states of the four stages are available for wiring to the Last Bit gates according to the customer format options (Sheet 5).

In the Receive logic, the output from the SYNC Character gate (1E8) is active (low) whenever the Shift Register contains the SYNC Character code specified by the customer. With SYNC1 active, the RSYNC flip-flop is set with REOC at the same time the Buffer Register is loaded from the Shift Register. The state of the RSYNC flip-flop appears in Bits 13 and 10 of the status byte. In the Read/SYNC Search Mode, the Bit Counter is held clear by A0 and there are no REOC pulses present. However, the first active condition of the SYNC line sets the SYNMD flip-flop which removes the A0 reset from the Receive Bit Counter. This permits REOC to set the RSYNC status.

The Clear Counter signal (A0) is removed and character synchronization is established. Subsequent SYNC characters are counted by the Processor to check the validity of the message SYNC state.

If the proper number of SYNC characters is not received, the controller may again be placed in the SYNCSCH (SYNC Search) Mode. For the Write Mode, the SC1 line is high to clear the SYNC flip-flop (Half-Duplex only).

In the Receive logic, the setting of the SYNMD flip-flop clears the Shift Register to provide a clear register for receiving the next character. On Power Up, the System Initialize signal clears the Receive Shift Register to eliminate it from accidentally containing the SYNC Character when power is first applied. For this reason, an all zeroes SYNC character is not valid.

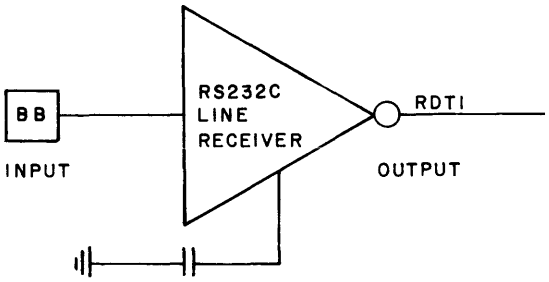
4.6 Bipolar Receivers and Drivers (Sheet 4)

Note that the 201 Data Set Adapter Receivers and Drivers are distinctly different from those used for 301 Data Set Adapter operation. See Figures 1,2,3, and 4.

Cable connections to the RS-232C Receivers and Drivers are made through a standard connector for the 201 Data Set Adapter and coax-connectors at the end of the mother-board for the 301 Data Set Adapter.

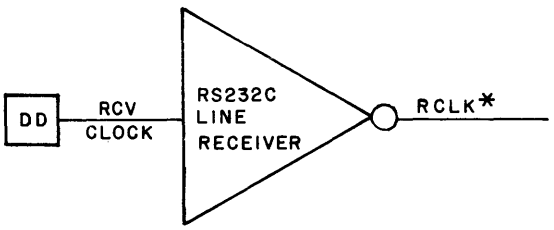
The Send and Receive Clocks (TCLK, RCLK) are gated by the Data Set Ready (DSRDY1) and Read/Write condition (SC0, CL2S1) to form gated clocks (RGCLK0, SGCLK0). These are used individually by the Parity Circuit, SYNC, Character gates, the Shift Registers, and Bit Counters. Clocks from the Data Set are designated such that the falling edge of CLK always indicates the time for data shifting.

Receive Data is enabled by SC0 for use by the Shift Register and Parity circuits. The CARRIER OFF condition, which is only valid in the Read Mode, is disabled by SC in the Write Mode (Half-Duplex only).



INPUT	STATE	OUTPUT
+V	SPACE LOGIC-0	0V
-V	MARK LOGIC-1	+5V

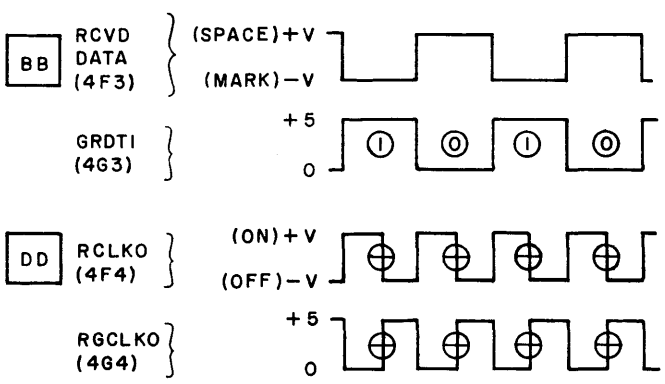
RS232C BIPOLAR DATA LINE



INPUT	STATE	OUTPUT
+V	ON	0V
-V	OFF	+5V

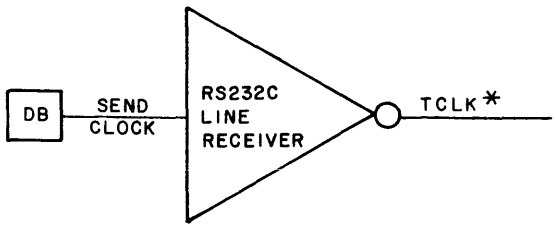
RS232C BIPOLAR CONTROL LINE

* LOGIC STATE TO BE DETERMINED BY TRANSITION REQUIRED TO SHIFT DATA



NOTE:
⊕ = SHIFT POINT FOR RCVD DATA

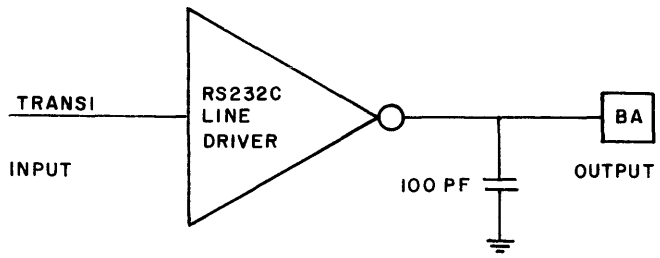
Figure 1. 35-413, 201 D.S.A. Receive Timing



INPUT	STATE	OUTPUT
+V	ON	0V
-V	OFF	+5V

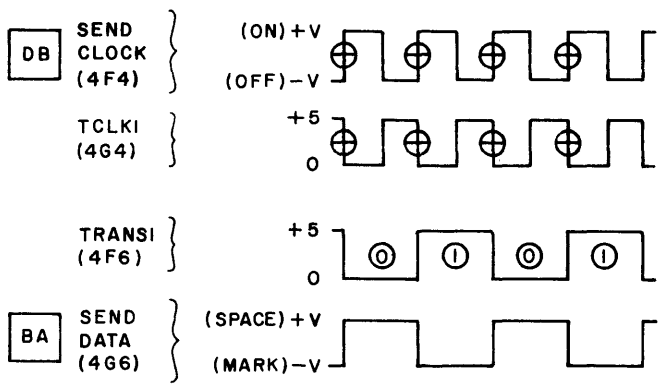
RS232C BIPOLAR CONTROL LINE

* LOGIC STATE TO BE DETERMINED BY TRANSITION REQUIRED TO SHIFT DATA.



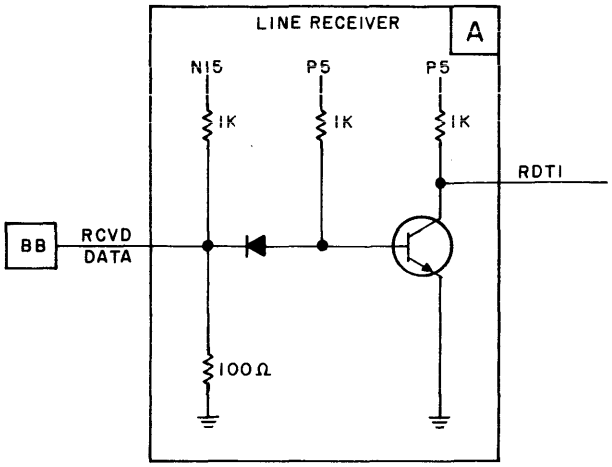
INPUT	STATE	OUTPUT
0V	SPACE LOGIC-0	+V
+5V	MARK LOGIC-1	-V

RS232C BIPOLAR DATA LINE



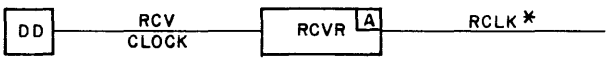
NOTE:
⊕ = SHIFT POINT FOR SEND DATA

Figure 2. 35-413, 201 D.S.A. Transmit Timing



INPUT	STATE	OUTPUT
≥23 ma	SPACE LOGIC-0	0V
≤ 5 ma	MARK LOGIC-1	+5V

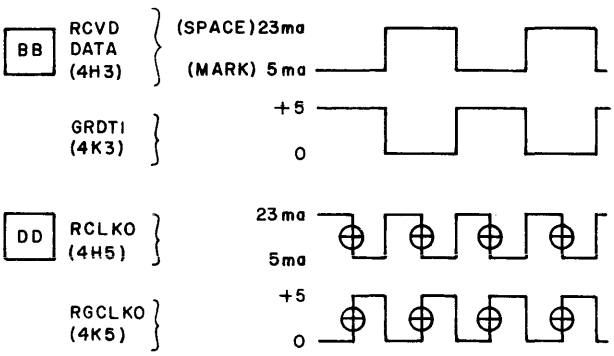
COAX RECEIVER



INPUT	STATE	OUTPUT
≥23 ma	ON	0V
≤ 5 ma	OFF	+5V

COAX RECEIVER

* LOGIC STATE TO BE DETERMINED BY TRANSITION REQUIRED TO SHIFT DATA.



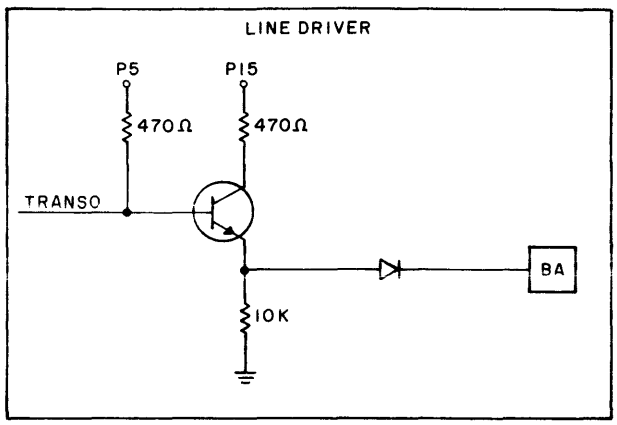
NOTE:
⊕ = SHIFT POINT FOR RCVD DATA

Figure 3. 35-414, 301 D.S.A. Receive Timing

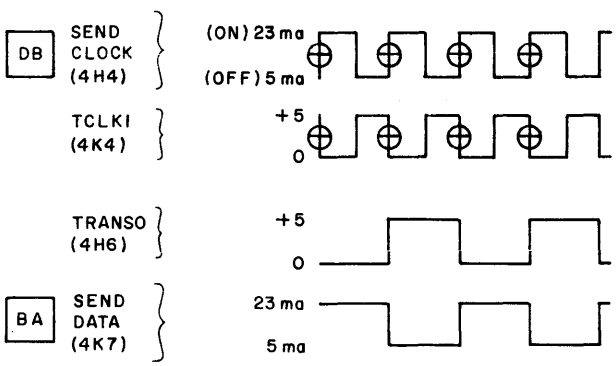
INPUT	STATE	OUTPUT
≥23 ma	ON	0V
≤ 5 ma	OFF	+5V

COAX RECEIVER

* LOGIC STATE TO BE DETERMINED BY TRANSITION REQUIRED TO SHIFT DATA.



OUTPUT	STATE	INPUT
≥23 ma	SPACE LOGIC-0	0V
≤5 ma	MARK LOGIC-1	+5V



NOTE:
⊕ = SHIFT POINT FOR SEND DATA

Figure 4. 35-414, 301 D.S.A. Transmit Timing

4.7 Shift Registers and Buffer Registers (Sheet 1)

Serial data from the bipolar receive logic enters the flip-flop at 1B8 and is shifted progressively through the nine stages of the Receive Data Register.

The parallel output from the Receive Shift Register is available in double-rail form on eighteen lines. These are wired to the Receive Buffer Registers according to the customer specified format option and to the SYNC Character Detection gate (1E8). When there are less than eight data bits in a character format, the data is right-justified in the Buffer. The least significant bit is shown in the Buffer Register at 1E2. The Parity bit is not loaded into the buffer. Data in the buffer is gated to the DXX0 lines.

4.8 Synchronization Character Detector and Request Generator (Sheets 1, 2, 3, and 4)

The SYNC Character Detect gate (1E8) is wired to the Shift Register output according to the format and code information supplied by the customer. It is enabled by SC0 (1C9) before and after the establishment of the message SYNC condition (SYNMD). The output, (SYNC1) feeds the Receive SYNC flip-flop (3B8).

In the Write logic, the first Dibit Clock (DCT1) from the Data Set after Data Set Ready (DSRDY0) is used to set the Request-to-Send (RQ2S) flip-flop (2L4). This gives the shortest delay in the Data Set response on the Clear-to-Send (CL2S) signal which follows. In Half-Duplex, returning to the Read Mode removes the RQ2S signal by toggling the RQ2S flip-flop reset after a one millisecond delay. Note that the Read Mode (Half-Duplex) is determined by the SC flip-flop (2H4), not the WT flip-flop (2F5) which follows the CMG1 signal.

4.9 Parity Generate and Check (Sheets 2 and 3)

In the Send logic, data from the least significant bit of the Shift Register (D071) is coupled to the TRANS1 line (2M1) as soon as CL2S1 is received from the Data Set. After the last data bit is transmitted, SLSTB1 disables the connection to the Shift Register and generates a Send Parity bit according to the contents of the SODD and Send Parity flip-flops (3H8). The SODD flip-flop is under program control to produce odd or even parity on the transmitted data.

When data enters the Data Set into the Read logic, it enters the Shift Register through the Receive Data flip-flop (1C8). At the same time, the Receive Parity flip-flop (3H8) counts the number of ONEs in the character appearing on the GRDT1 line. At the end of the Last Bit time, the gates at 3J8 compare the contents of the Receive Parity and the RODD flip-flops and sets the Receive Parity Fail (RPF) flip-flop (3J8) when disagreement is detected. The Receive Parity flip-flop is cleared at the end of every character period with RP0 so each character is handled separately. The RPF flip-flop is cleared when any RCMG0 signal is sent to the Adapter or if the Adapter is in the SYNSCH Mode.

5. CIRCUIT ANALYSIS (Sheet 4)

5.1 Bipolar Receiver 201 Data Set Adapter

The RS-232C Bipolar Line Receiver (4G2, 4G5) accepts signals greater than ±3V and less than ±25V. The Bipolar Receiver meets the 3000 ohm impedance level and incorporates external capacitive filters. The output operates into DTL circuits with OV and +5V levels. Eight receiver circuits, 19-047, are mounted directly on the mother-board. Receiver timing is shown in Figure 1.

5.2 Bipolar Transmitter 201 Data Set Adapter

The bipolar signals sent to the Data Set are produced by RS-232C Bipolar Line Drivers (4G6, 4G7). This circuit is fed by DTL levels and is a single DTL load. Transmit timing is shown in Figure 2.

5.3 Receiver 301 Data Set Adapter

The 301 Line Receiver (4J1, 4J5) accepts signals of $\leq$ 5ma for a +5 volt output, and $\geq$ 23ma for a 0 volt output. The Line Receiver meets the 95 ohm impedance necessary to terminate the 17-198 coax cable. The output operates into DTL circuits with 0 volt and +5 volt levels. Receiver timing is shown in Figure 3.

5.4 Driver 301 Data Set Adapter

The signals sent to the Data Set are produced by a converter (4J7) using an emitter-follower NPN transistor circuit. This circuit is fed by DTL levels and is a single DTL load. Transmit timing is shown in Figure 4.

6. TIMING

6.1 Receive Mode Timing 201 Data Set Adapter (Sheets 2, 3, and 4)

Waveforms for a 2000 bits/second (baud) rate with nine bits/character (eight data plus parity) which show the relationship between the Clock (RCLK1) and other important signals are shown on Figure 5. The data changes when the clock goes positive and is strobed into the Shift Register on the negative clock transition. The Bit Counter, which produces the RLSTB1 and EOC1 pulses, also changes state with the negative clock transition.

The time between the EOC1 pulses is 4.5 milliseconds for the example shown in Figure 5, but other data rates and/or formats will change the clock and character timing.

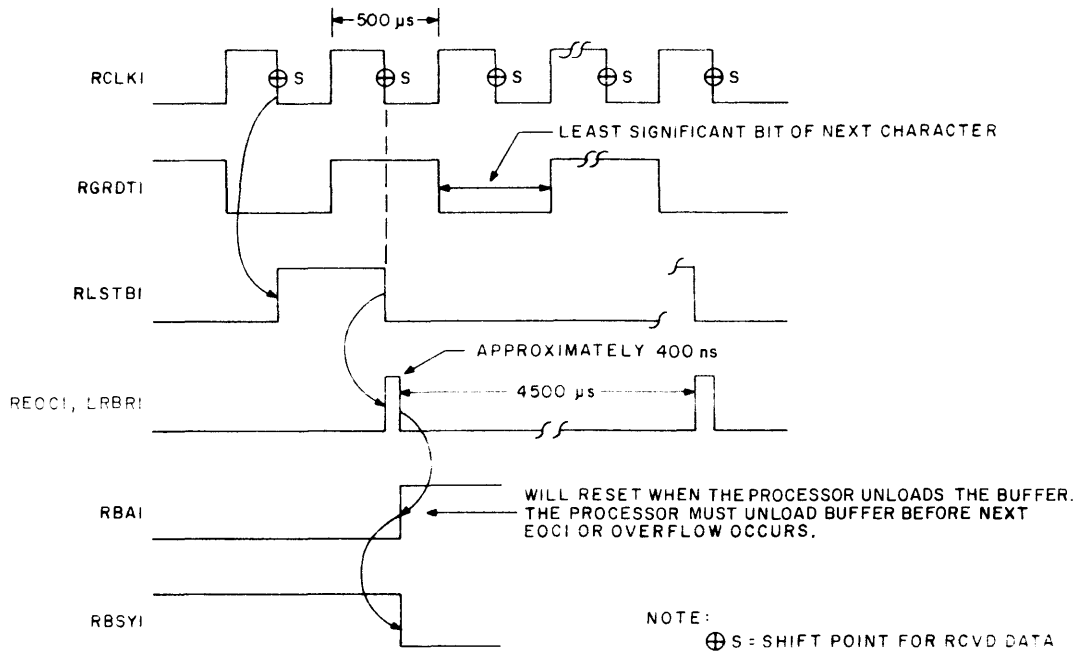


Figure 5. Receive Timing for 2000 Baud

6.2 Write Mode Timing 201 Data Set Adapter

The waveforms for transmitting data to the Data Set show how the negative clock transition controls shifting and counting within the Adapter. The Shift Register is cleared with a short (approximately 400 nanoseconds) pulse and is parallel loaded with the EOC1 pulse. The transmit waveforms for 2000 baud operation are shown in Figure 6.

6.3 Mode Change Timing (Half-Duplex Only)

The Mode Change waveforms are shown in Figure 7. When a Write to Read Mode change occurs, the contents of the Buffer and Shift Registers must be transmitted to the Data Set before the change can be executed. The CMG1 signal could occur after the last buffer unload or after the last buffer load. In either case, the mismatch between the WT (2F5) and SC (2C7) forces a BSY=1 condition which continues into the Read Mode until the Buffer receives a character from the Shift Register.

For the Read-to-Write Mode change, the Adapter sends a Request to Send (RQ2S) signal to the Data Set and waits for the Clear to Send (CL2S) signal. During this period, the Adapter is Busy. With the arrival of CL2S, the TCLK1 signal is activated and BSY=0. During the first character period, the previous contents of the Shift Register are sent to the Data Set while the Processor loads the Buffer Register with the first SYNC character. The first EOC1 pulse loads this into the Shift Register and leaves the Buffer available for another load. Note that after the clock starts, a full character period is available to load the Buffer without creating an overflow condition.

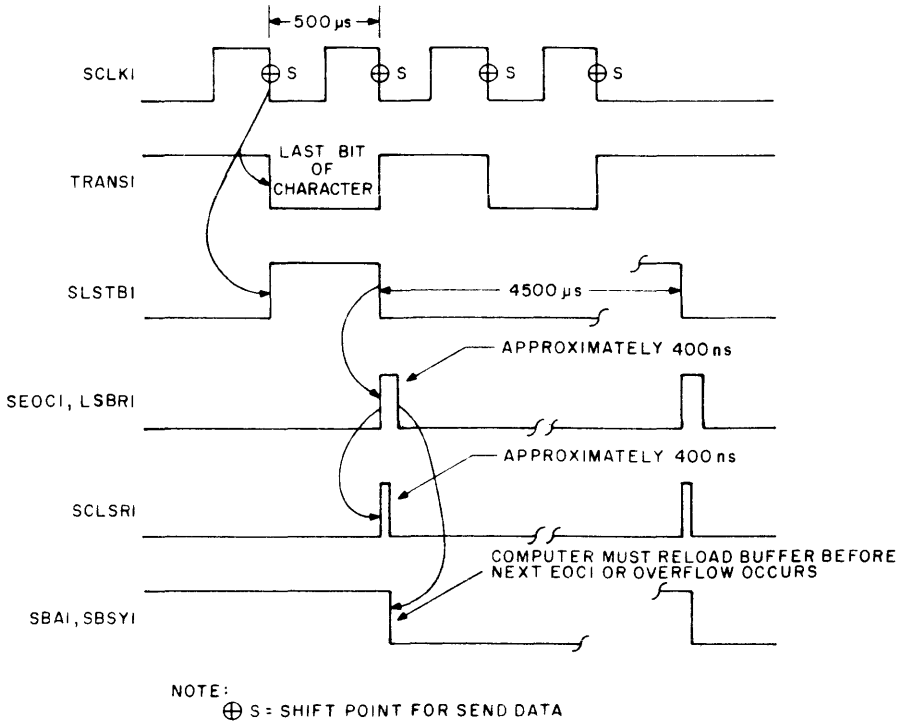


Figure 6. Transmit Timing for 2000 Baud

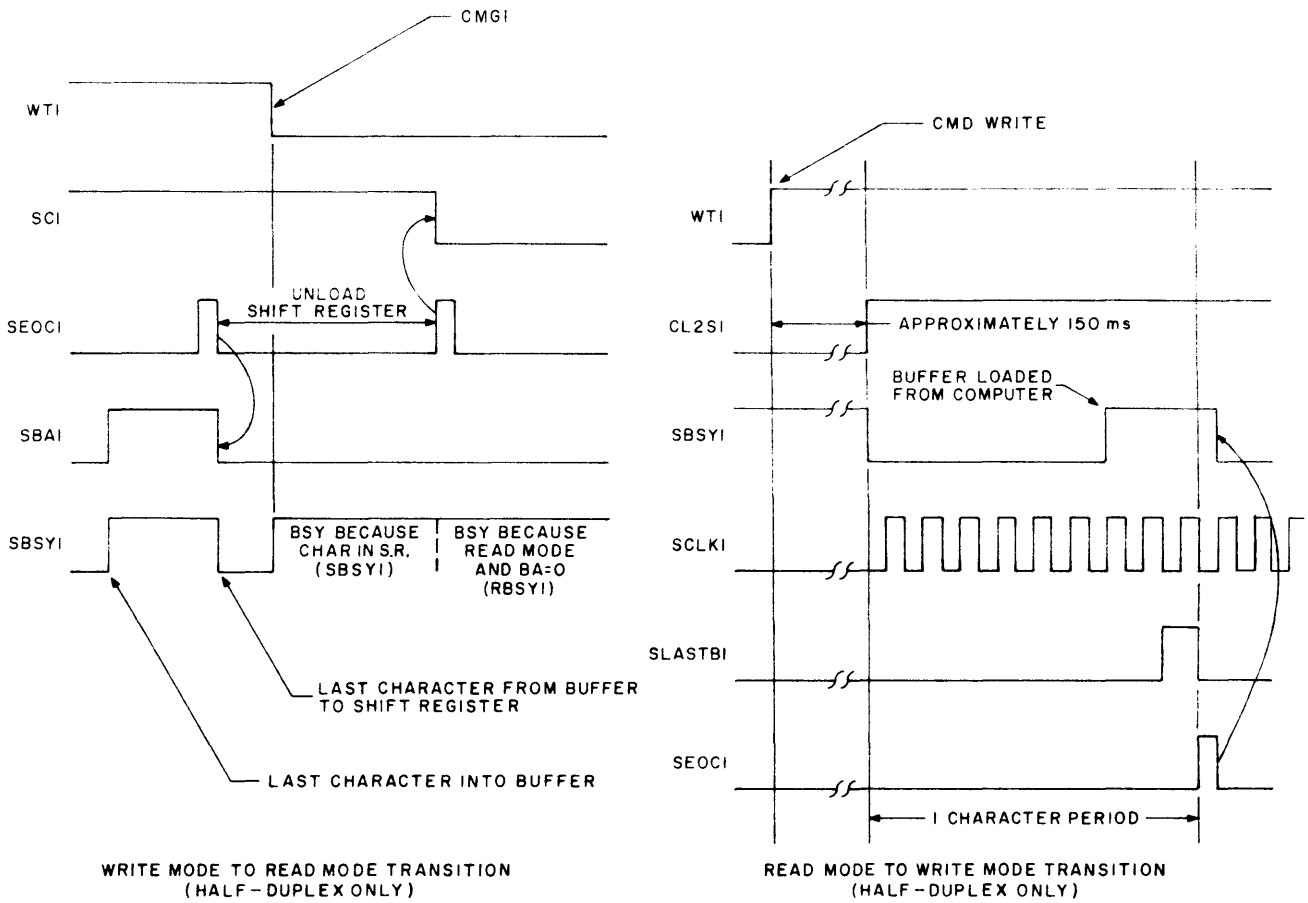


Figure 7. Mode Change Timing

6.4 Receive Mode Timing 301 Data Set Adapter

Waveforms for 40.8K baud with nine bits/character (eight data plus parity) are shown in Figure 8. The received data changes when the clock goes positive and is strobed into the Shift Register on the negative clock transition. The Bit Counter, which produces the RLSTB1 and EOC1 pulses, also changes state with the negative clock transition.

The time between the EOC1 pulses is 221.4 microseconds for the example shown in Figure 8, but other data rates and/or formats will change the clock and character timing.

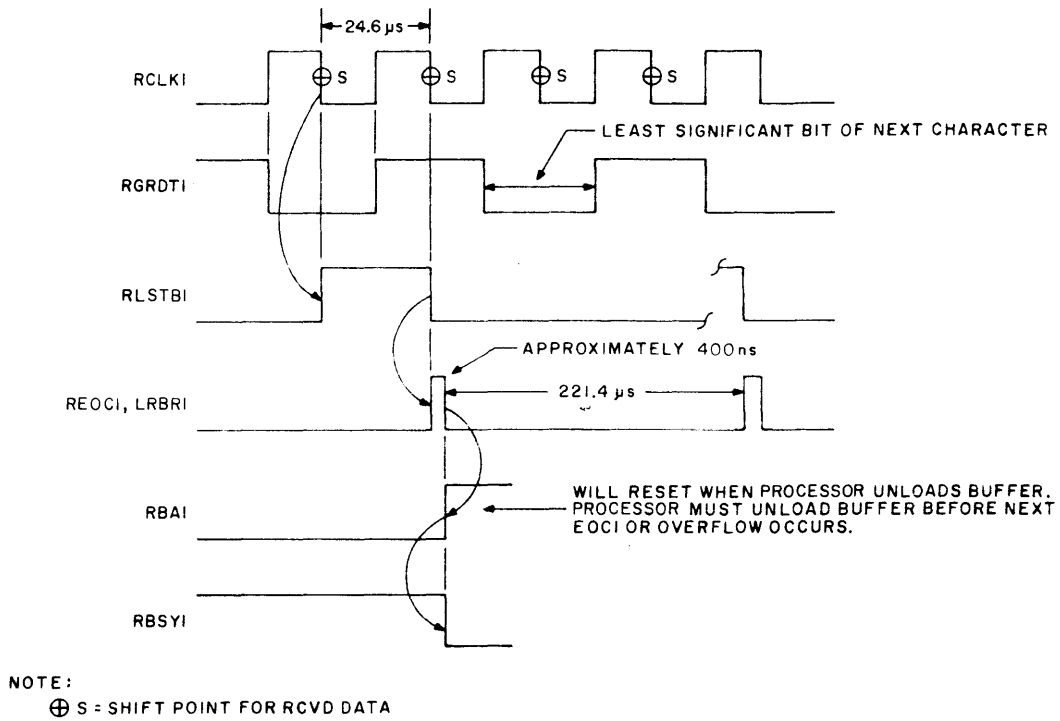


Figure 8. Receive Timing for 40,800 Baud

6.5 Write Mode Timing 301 Data Set Adapter

The waveforms for transmitting data to the Data Set show that the negative clock transition controls shifting and counting within the adapter. The Shift Register is cleared with a short (approximately 400 nanoseconds) pulse and is parallel loaded with the EOC1 pulse. The transmit waveforms for 40,800 baud operation are shown on Figure 9.

6.6 Mode Change Timing 301 Data Set Adapter

Same as 201 Data Set Adapter. See Section 6.3.

7. MAINTENANCE, ADJUSTMENTS, AND TESTS

Since the Data Set supplies the Send and Receive Clocks, there are no adjustments to the Data Set Adapter. Counters derive pulse trains within the Adapter and are not sensitive to data rate. The 02-252 Synchronous Data Set Adapter (201/301) is tested with Program Number 06-132.

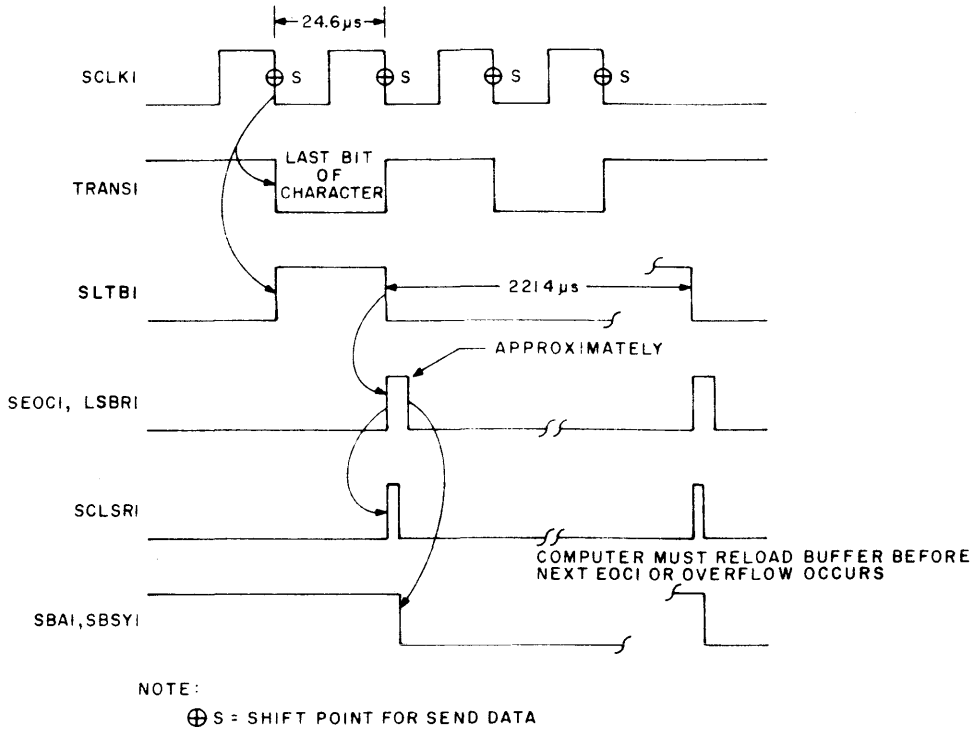


Figure 9. Transmit Timing for 40,800 Baud

8. MNEMONICS

The following list provides a brief description of each mnemonic found in the Synchronous Data Set Adapter. The 02-252D08 source of each signal is also provided. Note that many mnemonics are prefixed with an "S" or "R" in the schematics denoting Send or Receive. These mnemonics have the same definition in their respective logic. Example:

SAD	Address flip-flop for Send logic
RAD	Address flip-flop for Receive logic

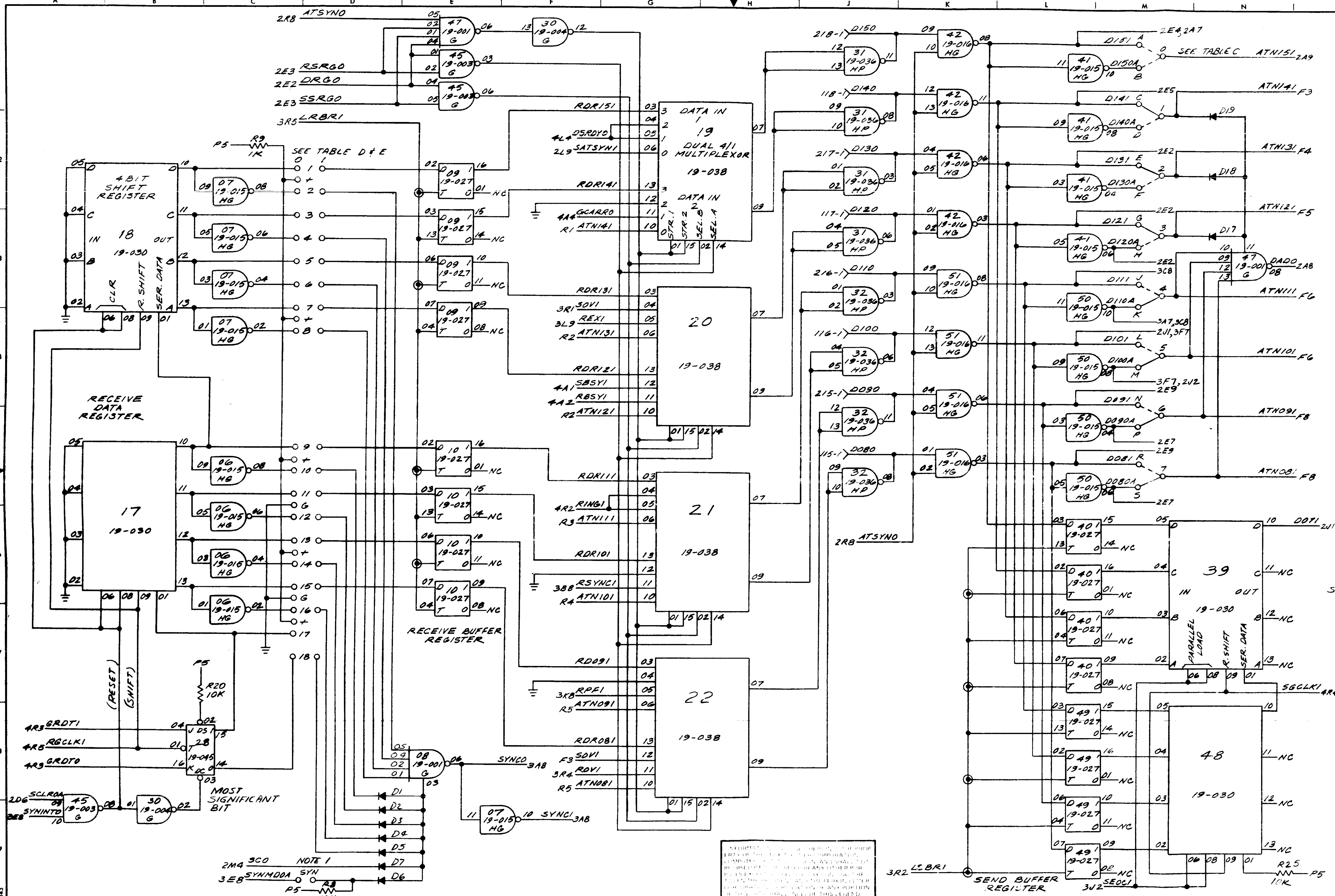
MNEMONIC	MEANING	SCHEMATIC LOCATION	
		Send	Receive
ADRS0	Address Control Line on MPX Bus	2A1	2A1
A0	Active for SYNC Search or SCLR		3F9
ATN0	Attention Queue flip-flop	2M6	2M6
ATNXX1	Send/Receive Interrupt Lines	1N1-1N5	1N1-1N5
ATSYN0	Attention SYNC	2R8	2R8
CL2S	Clear to Send from Data Set		4R5
CMD0	Command Control line from MPX Bus	2A4	2A4

MNEMONIC	MEANING	SCHEMATIC LOCATION	
		Send	Receive
DAD0	Address Decoded	1N3	1N3
DA0	Data Available Control Line from MPX Bus	2A4	
DCT	Dibit Clock from Data Set		4R3
DR0	Data Request Control Line from MPX Bus		2A2
DSCN	Disconnect flip-flop	2J2	2J2
DSRDY	Data Set Ready from Data Set		4R4
DTR0	Data Terminal Ready to Data Set	2J2	
DXX0	Data Lines to/from MPX Bus	1J1-1J5	1J1-1J5
D071	Send Shift Register Serial Output	1N6	
FDCMG0	Full Duplex Command Gate	2H5	2H5
FDRC1	Full Duplex Receive Mode Execute		2M4
FDX0	Full Duplex Gate	2G3	2G3
GCARR	Gated Carrier from Data Set		4R1
GRDT	Gated Received Data		4R3
HDX0	Half Duplex Option	2F3	2F3
LRBR1	Load Receive Buffer Register		3R5
LSBR1	Load Send Buffer Register	3R2	
PRES0	Parity Reset		3K9
RACK0	Received Acknowledge from MUX Bus	2F6	2F6
RAD	Address flip-flop for Receive logic		2C7
RATN1A	Receive Attention		2R7
RATSYN0	Receive Attention SYNC		2L8
RAX-REX	Receive Last Bit Detect		3F6-3F4
RBA	Receive Buffer Active flip-flop		3N6
RBSY1	Receive Busy Status Bit		4A2
RCV1	Receive Enable for Data Request, Status and Command Gates		2C7
RDRXX1	Receive Data from Data Set		1F1-1F8
RDSRM0	Receive Disarm flip-flop		2F7
REOC	Receive End of Character		3J6

MNEMONIC	MEANING	SCHEMATIC LOCATION	
		Send	Receive
REX1	Receive Examine		3L9
RGCLK	Gated Receive Clock from Data Set		4R4
RING	Ring Detection from Data Set		4R2
RINT	Receive Interrupt		4E2
RODD	Receive Even/Odd Parity flip-flop		3H7
ROV	Receive Overflow flip-flop		3N4
RPATN0	Receive Private Attention		4E5
RPF1	Receive Parity Fail flip-flop		3K8
RP0	Receive Parity		3L7
RQ2S	Request to Send to Data Set	2N5	
RSATN1	Receive Set Attention		4E5
RSREQ0	Receive Status Request		3N9
RSYNC	Receive SYNC flip-flop		3B8
RTERM0	Receive Terminate		3N8
RXFER0	Receive Transfer Command		2A2
R1	Active for Receive Address		2A7
SAD	Address flip-flop for Send Logic	2C8	
SATN1A	Send Attention	2R9	
SATSYN0	Send Attention SYNC	2L8	
SAX-SEX	Send Last Bit Detect	3F3-3F1	
SBA	Send Buffer Active flip-flop	3N3	
SBSY1	Send Busy Status Bit	4A1	
SC	Send Mode Execute flip-flop	2M4	
SCLR0	System Clear - Initialize Signal	2A6	2A6
SEOC	Send End of Character	3J3	
SDSRM0	Send Disarm flip-flop	2F9	
SGCLK	Gated Send Clock from Data Set		4R4
SINT	Send Interrupt	4E1	
SLSTB1	Send Last Bit Condition	3G2	
SND1	Send Enable for Data Request, Status and Command Gates	2C8	

MNEMONIC	MEANING		
SOV	Send Overflow flip-flop	3N1	
SPATN0	Send Private Attention	4F1	
SR0	Status Request Control Line from MPX Bus	2A3	2A3
SSREQ0	Send Status Request	3N8	
STERM0	Send Terminate	3N7	
SYNC	Sync Character Gate		1F8
SYNINT0	Sync Interrupt		3E8
SYNMD	Sync Mode flip-flop		3E8
SYN0	I/O Sync Signal to MPC Bus	2G1	2G1
SXFER0	Send Transfer Command	2A3	
S1	Active for Send Address	2A8	
TACK0	Transmit Acknowledge out of Adapter	2M6	
TRANS	Transmit Data to Data Set	2R1	
WT1	Write Mode flip-flop		2H5

Computer Systems Division



REVISIONS					
REVISED SHTS 2,4,5					
WZ	RC	3141-001		2-1-73	R01
REVISED SHTS 1,2,3, 4 7,9 & 5. REV OF PC BDS IN INDEX LOC S8 WAS R02					
EM	RC	1670			R02
REVISED SHTS 2,4 & 8, REV. OF 35-414 LOC S8 WAS R03					
BG	RC	1691		2-23-73	R03
REVISED SHTS 4 & 9 & 1 35-414 WAS R04 LOC S8					
EM	RC	1692		1/13/73	R04
REVISED NOTE 1 ON SH 5					
TCP	WH	1839		3-4-73	R05
REVISED SHTS 2 & 4. LOC S8 35-413 WAS R03, 35-414 WAS R05 ADDED 35-413M01 & 35-414M01					
BG	WH	2054		2/11/74	R06
REVISED SHTS 4 & 7. LOC S8 35-413 M01 WAS R01					
	WH	2298	—	12-3-79	R07
REV'D SHT'S 2 & 4 IN AREA A8 35-413 M01 & 35-414 M01 WERE R03 & R01 RESPECTIVELY.					
BP		3892	M	5-11-79	R08
REVISED SHT. 3. AREA S8, 35-413M01 WAS R04 & 35-414M01 WAS R03.					
BP	F.T.	4070	R	10-29-79	R09

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION

201 DSA	35-413 R04
301 DSA	35-414 R06
201 DSA	35-413M01 R05
301 DSA	35-414M01 R04

NOTE
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

NOTES 1. NORMALLY NOT STRAPPED. STRAP TO INHIBIT SYNC STATUS IN DATA MODE.

REV LEVEL	9	5	3	7	3		3		
SHEET NO	1	2	3	4	5	6	7	8	9

NAME	TITLE	DATE
E ROE	DRAFT	1-21-72
R FERO	CHK	12 72
	ENGR	
	DIR ENG	

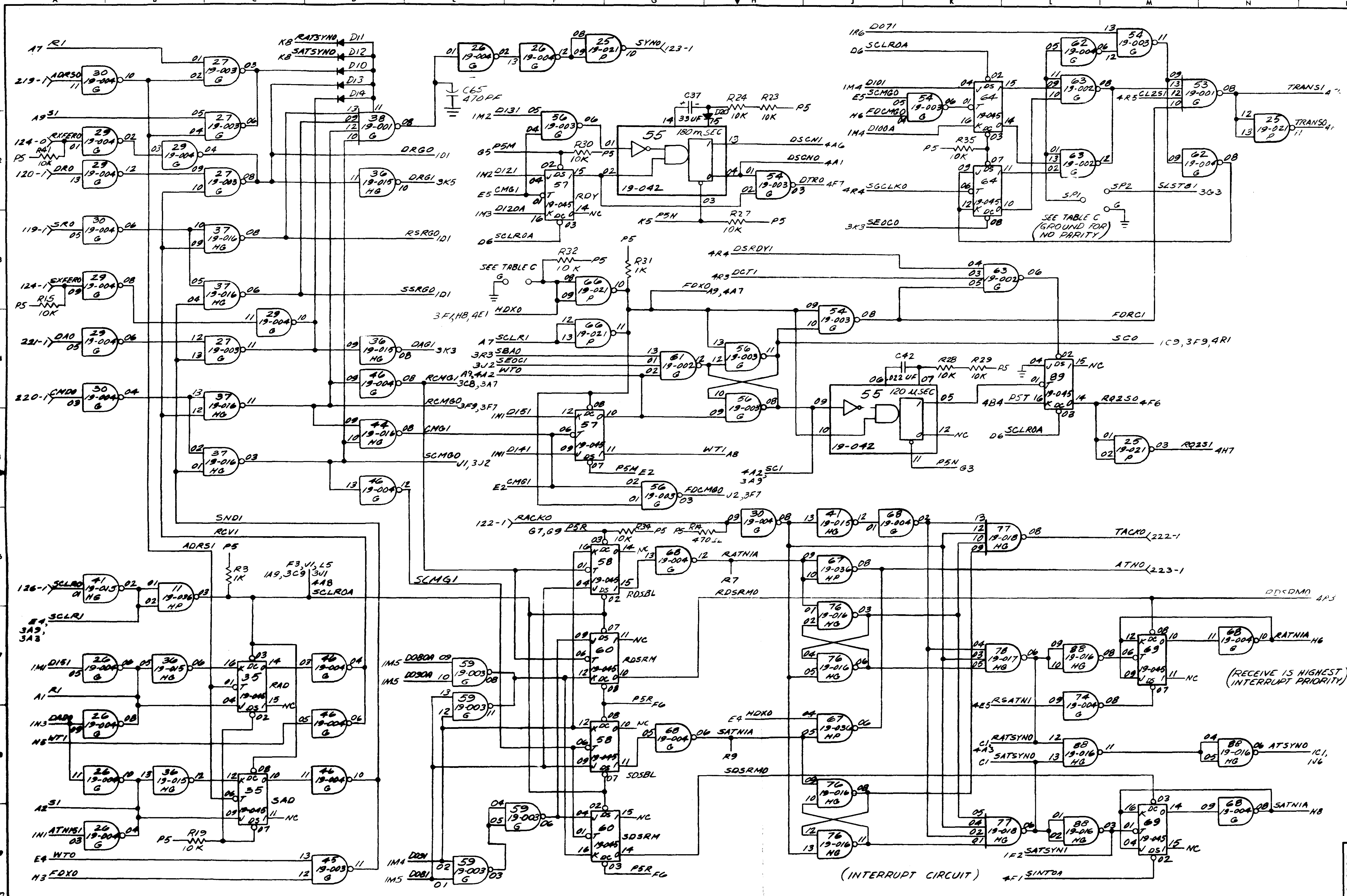
TITLE FUNCTIONAL SCHEMATIC DATA SET ADAPTER 201/301

TASK NO. 03141

DWG NO. 02-252R09D08

SHEET 1 OF 9

BRUNING 44-231 15043



REVISIONS					
REVISED CIRCUITY LOCATION R6, C6					
WZ	RC	3141-001		2-1-73	R01
DELETED: CONN. SCMGI TO 5A-06 & 64-01 LOC K1. ADDED: 3F1 TO HDXO LOC E4. ADDED C65 LOC. E1. LOC 84 REV PIN 2 & 13 IC 37					
EM	RC	1670			R02
LOC L4 19-045 PINS 4 & 16 WERE REVERSED.					
BG	RC	1691		2-23-73	R03
LOC A9 WTO WAS SCO					
BG		2054			R04
CROSS REF. AT C6 WAS 4A9					
BP		3892	M	5-11-79	R05

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	1-25-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC DATA SET ADAPTER 201/301

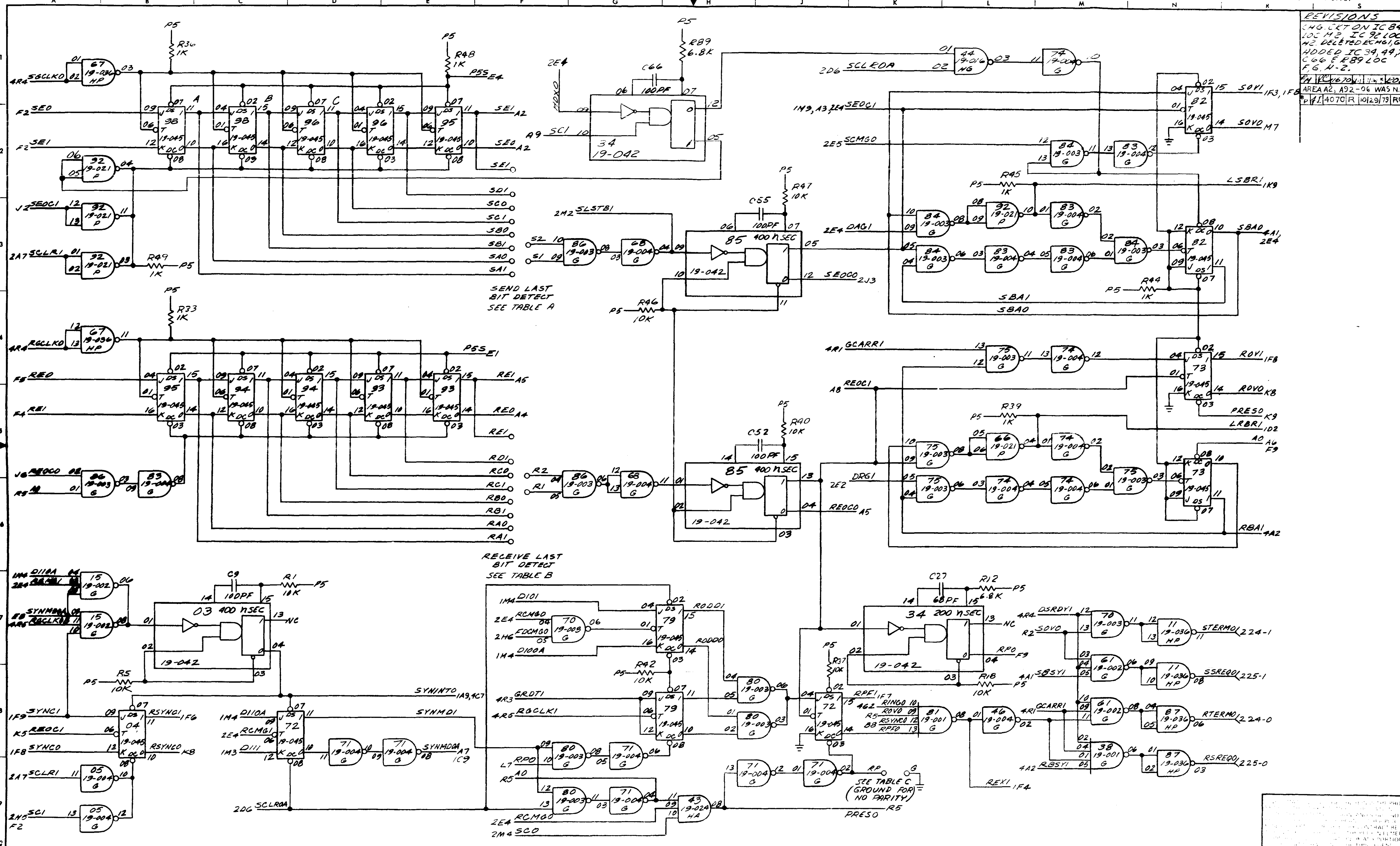
TASK NO. 03141

DWG NO. 02-252 R05D08

SHEET 2 OF 9

BRUNING 44-231 15043

PERKIN ELMER
Computer Systems Division
Oceanport N.J. 07757



NOTES

NAME	TITLE	DATE
E ROE	DRAFT	1-27-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC DATA SET ADAPTER 201/301

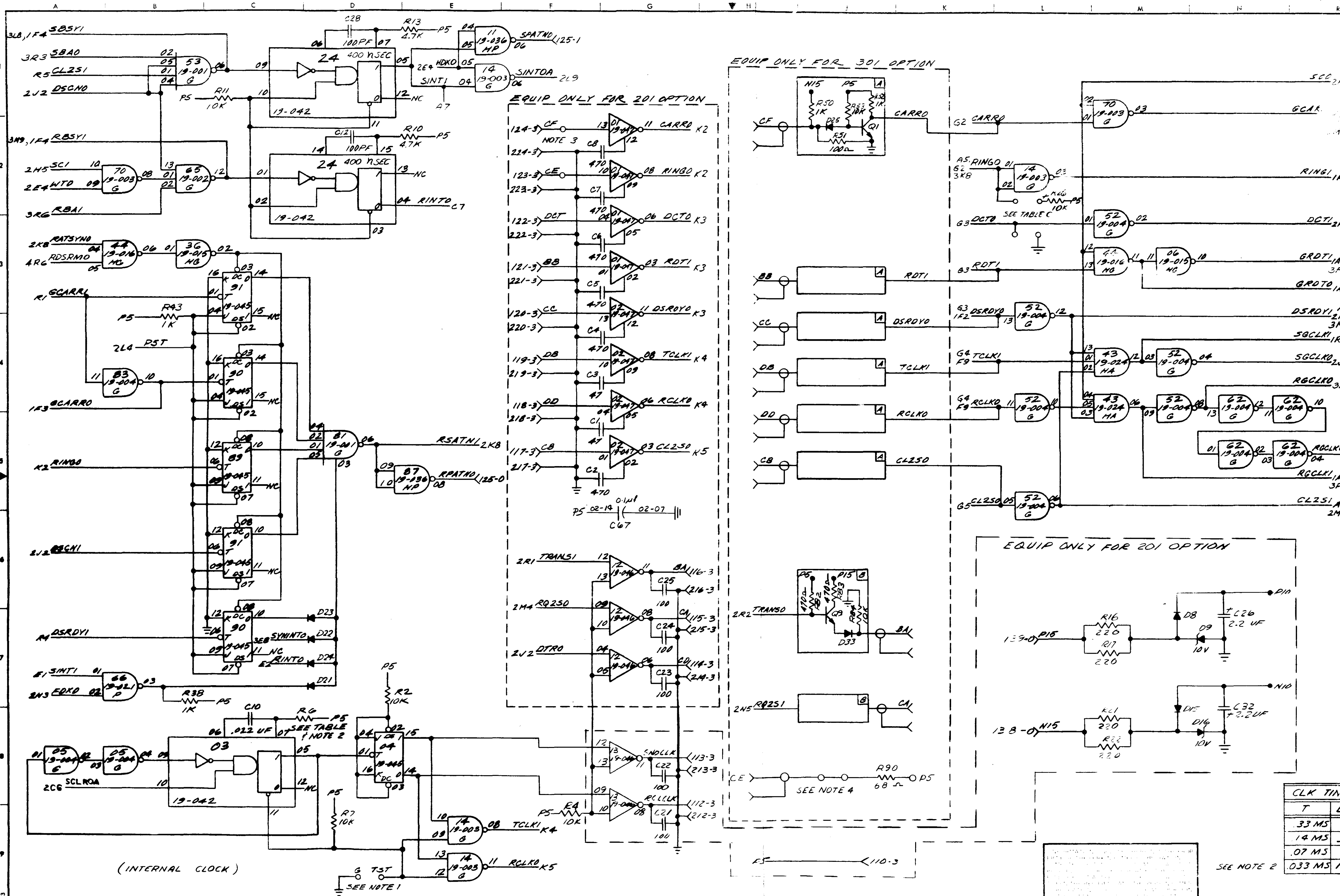
TASK NO. 03141

DWG NO. 02-252 F03008

SHEET 3 OF 9

BRUNING 44-231 15043

PERKIN ELMER
Computer Systems Division
Oceanport N J 07757



REVISIONS					
REVISED CIRCUITY LOCATION A3.					
WZ		3141-001		2-1-73	R01
CHG LOC L7 & 8 P/N 139-0 & 138-0 WAS 102-0 & 202-0 RESP. LOC A9 NOTE 2 R6 WAS 4.7K					
		1670			R02
ADDED CKT IN LOC J8, ADDED NOTE 4, LOC K2 ADDED RINGO ON 19-004 LOC J2 R50-R53 WAS R49-R52, LOC J7 R82-R84 WAS R81-R83					
BG		1691		2-27-73	R03
REMOVED COMPONENTS C21, C22, C26, C32, D8 D9, D15 D16, R16, R21, A13 & CONN 3 LOC N7, G8 FOR 301 OPTION ONLY & R17 & R22					
KM		1692		4/17/73	R04
LOC L2, GATE 14 WAS 19-004					
BG		2054		2/28/74	R05
AREA G5 ADDED C67 ON 19-097. AREA F4 C1 & C3 WERE 970pf					
		2298	—	11-13-74	R06
SCL ROA TEMINATED FROM PIN 11 IN AREA A8					
BP		3892	M	5-11-79	R07

CLK TIMING TABLE		
T	BAUD	R6
.33 MS	1.7 K	47 K
.14 MS	3.5 K	20 K
.07 MS	7 K	10 K
.033 MS	17 K	4.7 K

SEE NOTE 2

NOTES

1. FOR PROCESSOR TO PROCESSOR INTERFACE GND IN ONE ADAPTER. GND FOR NORMAL OPERATION. REMOVE FOR OFF-LINE TEST PROG.
2. UNLESS OTHERWISE SPECIFIED EQUIP WITH 10K FOR R6. OTHER BAUD RATES OBTAINED BY CHANGING BOTH R6 & C10 USE FORMULA: BAUD $= \frac{1}{T} \approx .3RC$, WHERE $4.7K \leq R \leq 50K$.
3. CE & CF MAY BE DISABLED BY TYING THE CF TO + (+15V) & TYING CE TO - (-15V). THESE ARE FEED-THRUS LABELLED ON THE P.C. BOARD.
4. FOR 301 TESTING ONLY

NAME	TITLE	DATE
E. ROE	DRAFT	1-31-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC DATA SET ADAPTER 201/301

TASK NO. 03141

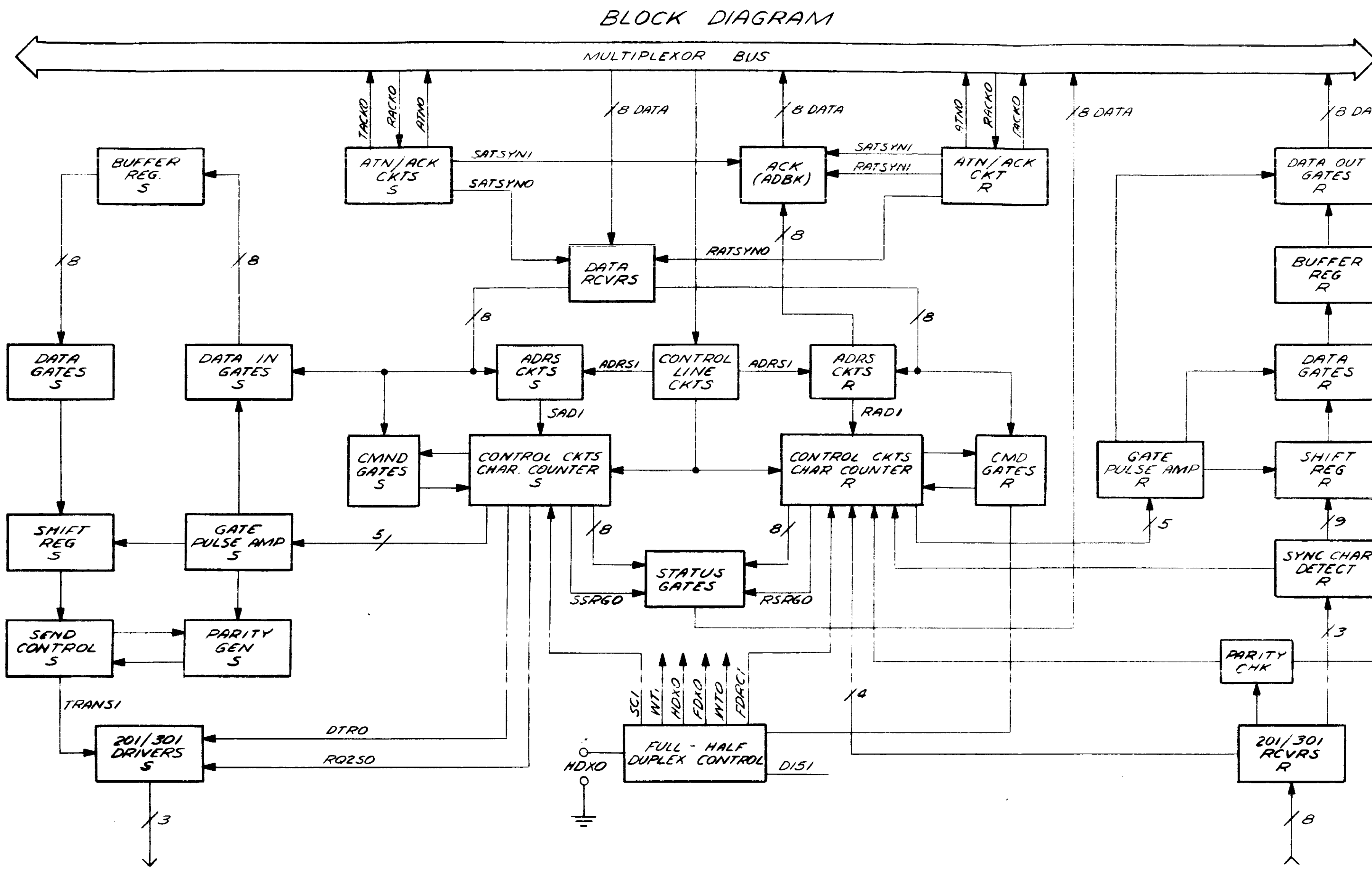
DWG NO. 02-252 R07 D08

SHEET 4 OF 9

BRUNING 44-231 15043

PERKIN ELMER
Computer Systems Division
Oceanport, N.J 07757

BLOCK DIAGRAM



REVISIONS					
REVISED CONNECTIONS ON CABLE 17-197					
WZ		3141-001		2-1-73	R01
CHG BACK PANEL MAP SIGNAL ON PINS 138-0 & 139-0 WERE NOT SPEC'D. DELETE P15 FROM 1Z-0 DELETE N15 FROM 2O2-0					
EM	RC	1670			R02
NOTE 1 OPTION X (7 DATA ETC WAS OPTION Z (8 DATA ETC					
TCP		1839		9-4-73	R03

BACK PANEL MAP			
ROW 1	ROW 2	TERM NO.	CONN
P5	GND	41	
GND	GND	40	
		39	
		38	
		37	
		36	
		35	
		34	
		33	
		32	
		31	
		30	
		29	
		28	
		27	
SCLRO		26	
SPATNO	SSREQO	25	
SXFERO	STERMO	24	
SYNO	ATNO	23	
RACKO	TACKO	22	1
	DAO	21	
DRO	CMDO	20	
SRO	ADRSO	19	
DI40	DI50	18	
DI20	DI30	17	
DI00	DI10	16	
DO80	DO90	15	
		14	
		13	
		12	
		11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
P15		39	
N15		38	
		37	
		36	
		35	
		34	
		33	
		32	
		31	
		30	
		29	
		28	
		27	
		26	
RPATNO	RSREQO	25	
RXFERO	RTERMO	24	
		23	
		22	0
		21	
		20	
		19	
		18	
		17	
		16	
		15	
		14	
		13	
		12	
		11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
P5	GND	00	

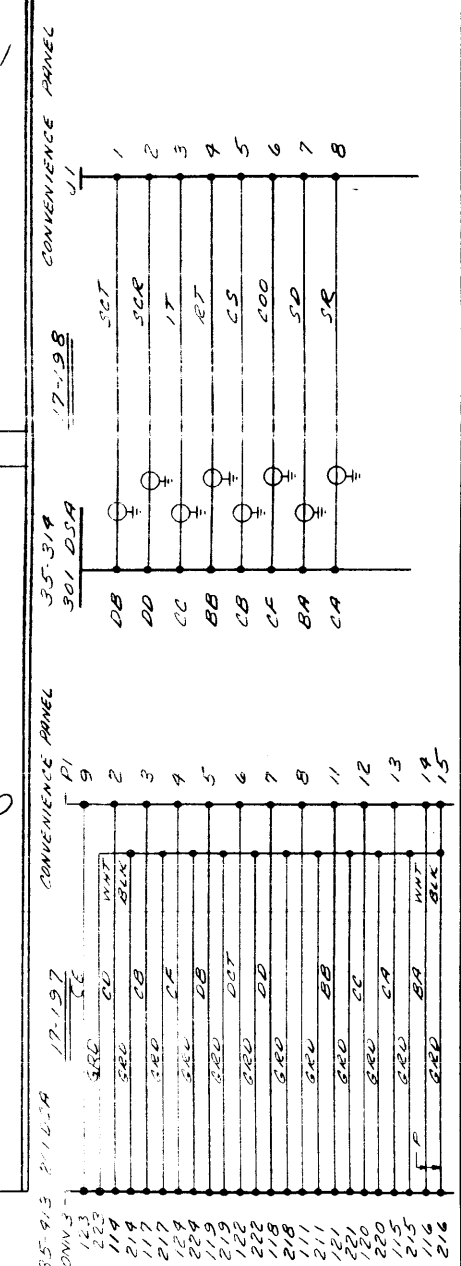


TABLE A BOARD LOCATION A86					
OPTION	CHARACTER FORMAT	SEND LAST BIT DETECTOR STRAPS			
		FROM	TO	FROM	TO
U	6 DATA + NO PARITY	S1	SA1	S2	SE1
V	6 DATA + PARITY	S1	SA0	S2	SB1
W	7 DATA + NO PARITY	S1	SA0	S2	SB1
X	7 DATA + PARITY	S1	SB0	S2	SC1
Y	8 DATA + NO PARITY	S1	SB0	S2	SC1
Z	8 DATA + PARITY	S1	SC0	S2	SD1

TABLE B BOARD LOCATION A84					
OPTION	CHARACTER FORMAT	RECEIVE LAST BIT DETECTOR STRAPS			
		FROM	TO	FROM	TO
U	6 DATA + NO PARITY	R1	RA1	R2	RE1
V	6 DATA + PARITY	R1	RA0	R2	RB1
W	7 DATA + NO PARITY	R1	RA0	R2	RB1
X	7 DATA + PARITY	R1	RB0	R2	RC1
Y	8 DATA + NO PARITY	R1	RB0	R2	RC1
Z	8 DATA + PARITY	R1	RC0	R2	RD1

TABLE C STRAP OPTIONS FOR DUPLEX, PARITY & MISC.				
FUNCTION	ACTION	FROM	TO	BOARD LOCATION
HALF DUPLEX	STRAP	HDXO	G	A66
	STRAP	O	A	A41
FULL DUPLEX	STRAP	O	B	A41
PARITY	STRAP	SP1	SP2	A63
NO PARITY	STRAP	RP	G	A81
	STRAP	SP1	G	A63
IF DATA SET DOES NOT HAVE RING OPTION	STRAP	RIN	+	A61
IF DATA SET DOES NOT HAVE DIBIT CLK OPTION	STRAP	DCT	G	A61

TABLE D BOARD LOCATION A7

MOST SIGNIFICANT BIT

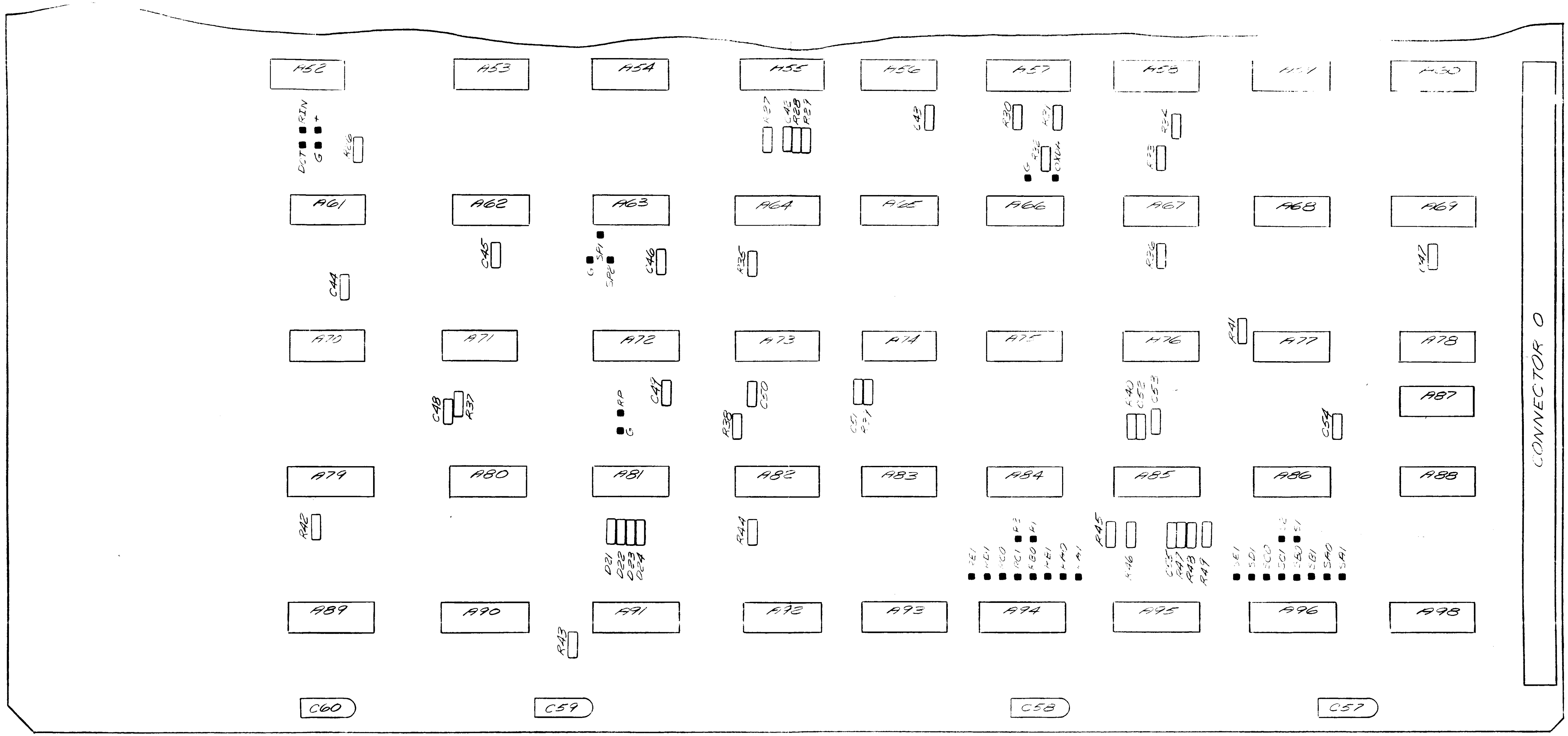
SYNC CHARACTER DETECT CONNECT ( ) TO 1 OF 3 OPTIONS BELOW			
FROM	TO 1	TO 0	DONT CARE
(102)	001	002	+
(104)	003	004	+
(106)	005	006	+
(108)	007	008	+
(110)	009	010	+
(112)	011	012	+
(114)	013	014	+
(116)	015	016	+
(118)	017	018	+

TABLE E BOARD LOCATION A7								
RECEIVE BUFFER REGISTER CONNECT ( ) TO PIN ___								
OPTION	(115)	(113)	(111)	(109)	(107)	(105)	(103)	(101)
U	G	G	017	015	013	011	009	007
V	G	G	015	013	011	009	007	005
W	G	017	015	013	011	009	007	005
X	G	015	013	011	009	007	005	003
Y	017	015	013	011	009	007	005	003
Z	015	013	011	009	007	005	003	001

NOTES
1 FACTORY WIRED FOR:
OPTION X (7 DATA + PARITY)
SYNC CHARACTER X '16'
ADDRESS = X '0E'

NAME	TITLE	DATE
W. ZILLGER	DRAFT	1-31-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
DATA SET ADAPTER 201/301
TASK NO. 03141
DWG NO. 02-252 R03 D08
SHEET 5 OF 9

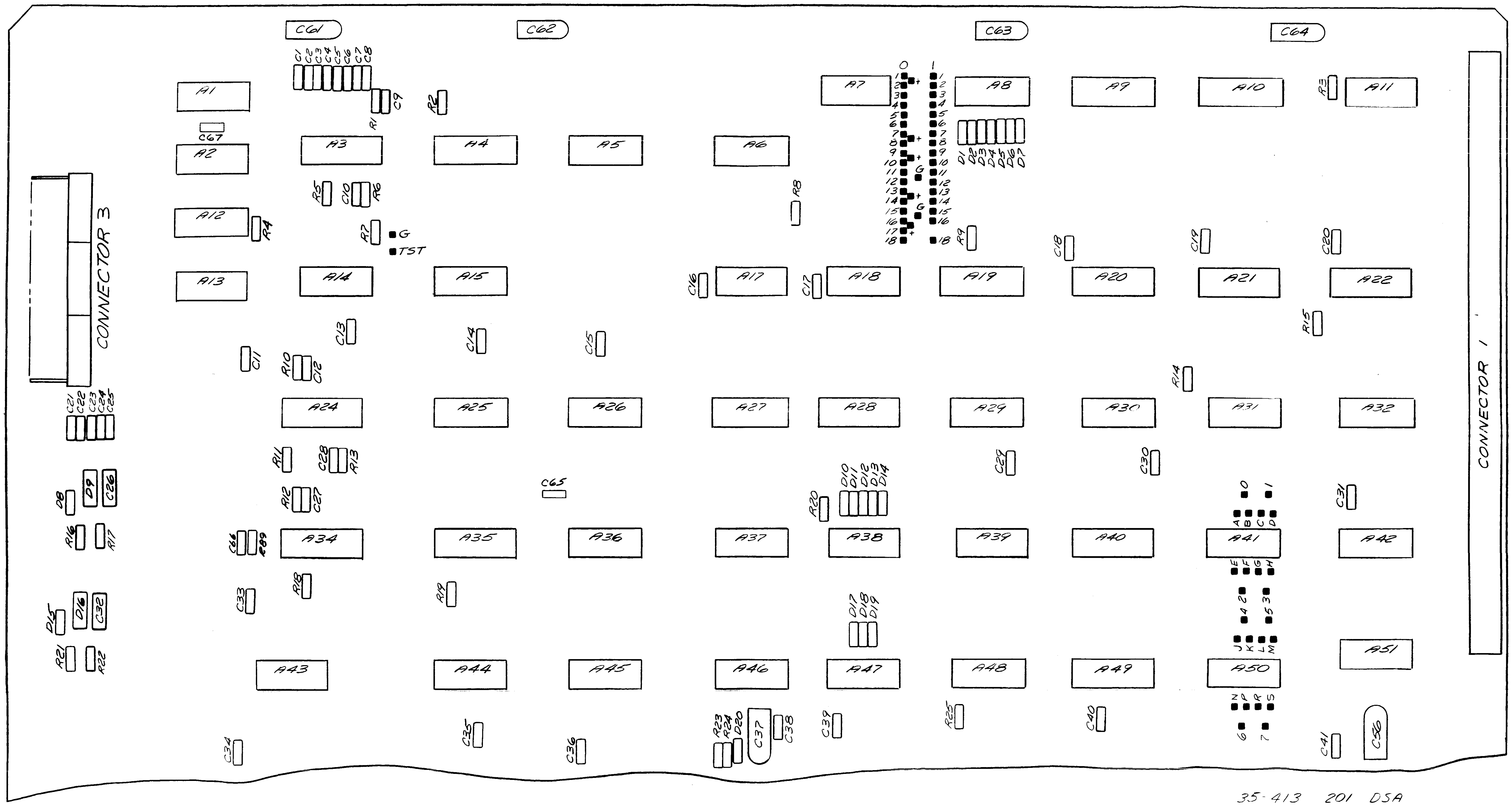


35-413 201 DSA

COMPONENT	REFERENCE DESIGNATION
CAPACITOR	C1 THRU C66
RESISTOR	R1 THRU R49
DIODE	D1 THRU D20
I.C	A1 THRU A15, A17 THRU A22, A24 THRU
	A92 A94 THRU A96, A98

NOTES

NAME	TITLE	DATE	
	DRAFT	8/72	TITLE FUNCTIONAL SCHEMATIC DATA SET ADAPTER 201/301
	CHK		
	ENGR		TASK NO 03141
	DIR ENG		DWG NO 02-252 D08 · SHEET 6 OF 9



NOTES

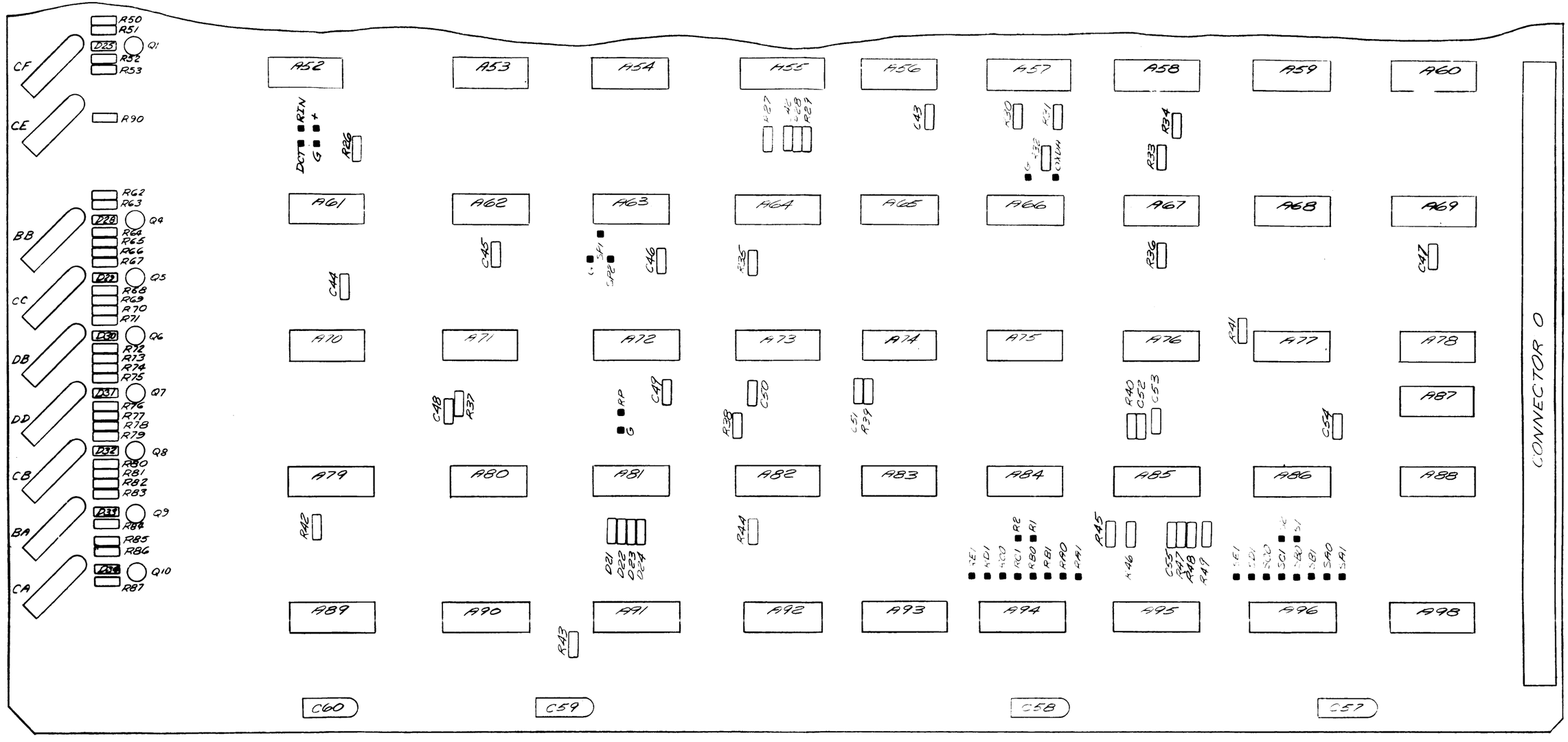
ADDED C65, C66 & R89 LOC C&G6				
EM	RC	1670	2-1-71	E02
ADDED C67 LOC. C2.				
	JEH	2344	12-3-74	E03

NAME	TITLE	DATE
R. EDWARDS	DRAFT	8-4-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
DATA SET ADAPTER 201/301

TASK NO. 03141
DWG NO. 02-252 R03 D08
SHEET 7-9

BRUNING 44-231 16042



35-414 301 OSA

COMPONENT	REFERENCE DESIGNATION
CAPACITORS	C1 THRU C22, C26 THRU C65
RESISTORS	R1 THRU R16, R18 THRU R21, R23 THRU R53, R62 THRU R87, R89 R90
DIODES	D1 THRU D25, D28 THRU D34
TRANSI. TORS	Q1, Q4 THRU Q10
I.C.'S	A2 THRU A11, A13 THRU A15, A17 THRU A22, A24 THRU A32, A34 THRU A96, A98.

NOTES

REVISIONS
ADDED R90, REF DESIGN. FOR RES. ADDED R83, R90, C64 AND C65

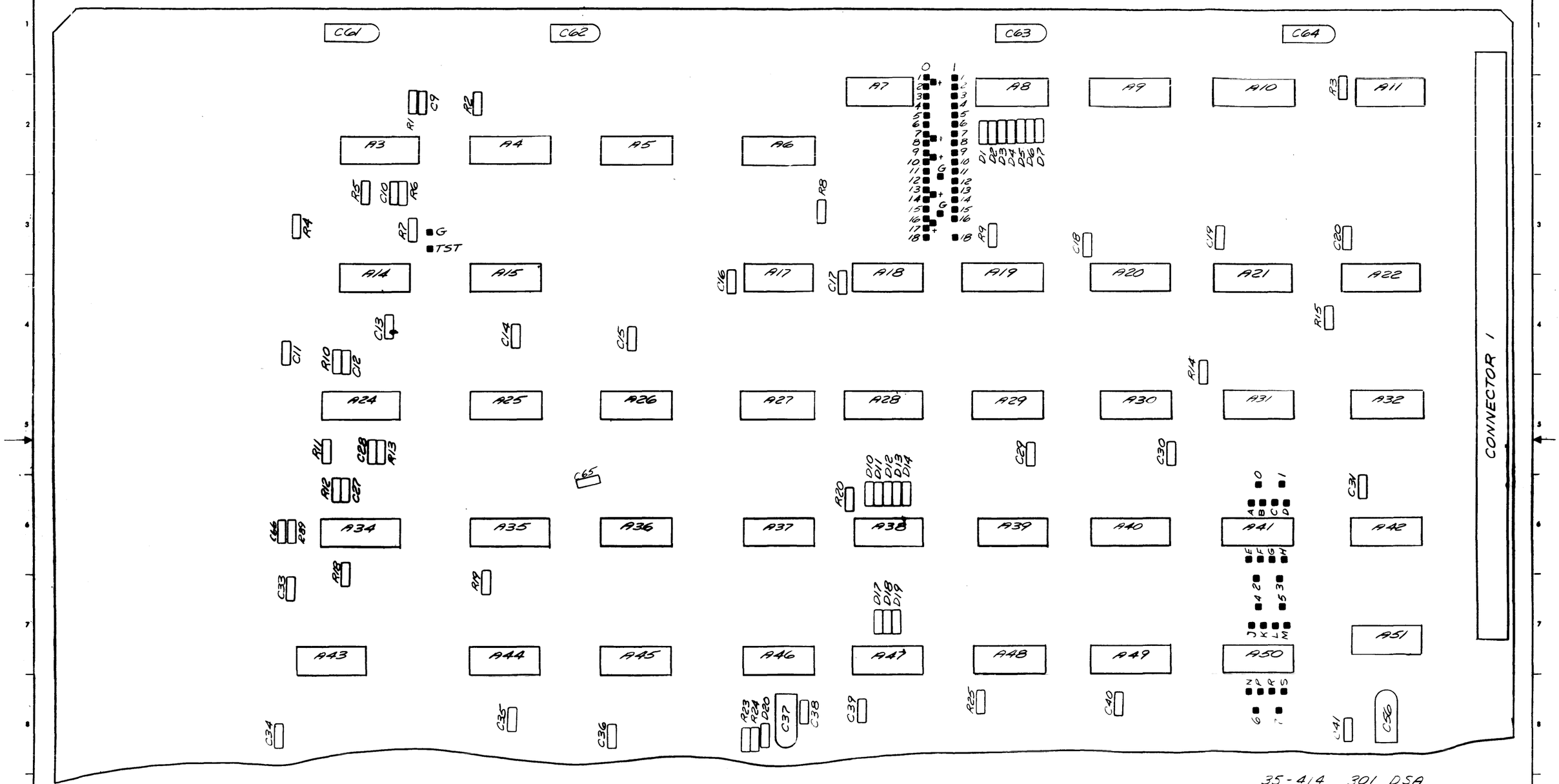
BY	NO.	DATE	REV
BG	1691	2-23-73	R03

FUNCTIONAL SCHEMATIC
DATA SET ADAPTER 201/301

03141
02-252 R03 DOB 8-9

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport N J 07757



35-414 301 DSA

NOTES				
	ADDED R89, C65 & C66 LOC C8G6	CONN 3 & A13 LOC A2-A7	EDWARDS	5-4-72
	REMOVED COMPONENTS C21, C22, C26, C32, D8, D9, D15, D16, R16 & R21			

FUNCTIONAL SCHEMATIC
DATA SET ADAPTER 201/301
03M1
02-252 RD 4 D08
SHEET 9 OF 9

BRUNING 44-231 19042