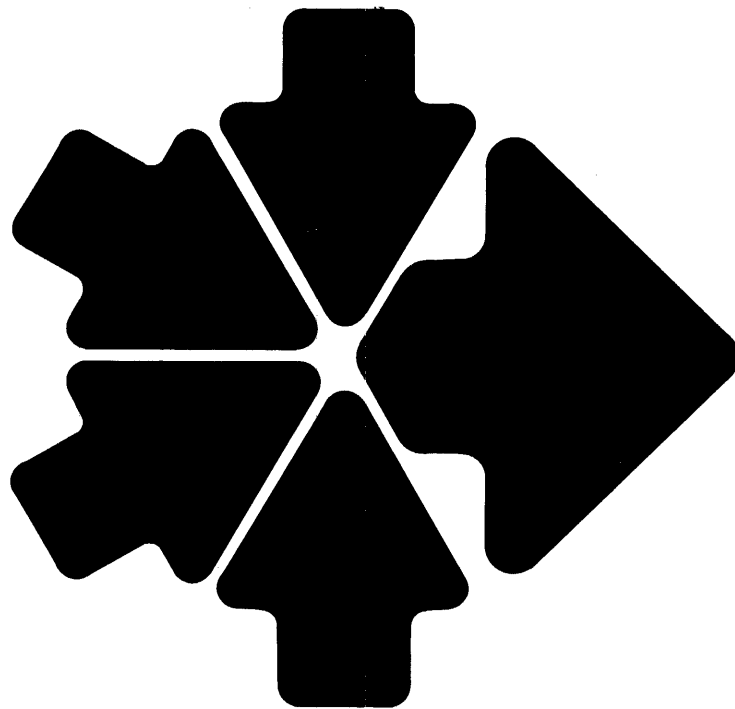


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SMD 2180
STORAGE MODULE
CONTROLLER/FORMATTER
USER'S GUIDE



We Stay Ahead Of Our Competition . . .

So You Can Stay Ahead Of Yours.

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STORAGE MODULE
CONTROLLER/FORMATTER
USER'S GUIDE

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SMD 2180 USER'S GUIDE

The SMD 2180 is an Intelligent Storage Module Controller/Formatter, using bipolar microprocessor (8X300) technology. It plugs directly into the MULTIBUS and is a Bus Master during data transfers, using a variable burst length DMA technique. It directly connects via industry standard A and B cables to from one to four storage module drives which are available from a number of manufacturers. The SMD 2180 can control any type of SMD, CMD, MMD, FMD, or any other drive with a SMD compatible interface.

Devices on the MULTIBUS may command the SMD 2180 to perform a disk function, such as READ or WRITE a sector (or more) of data into or out of System Memory. All such functions have an extended list of parameters to define the exact function to be performed. This list is called the IOPB (I/O Parameter Block) and is found in common memory, that is, memory accessible to both the requesting device, such as a CPU, and the SMD 2180. In order to cause a disk function to be performed, simply build the IOPB in memory, write a pointer to the IOPB into the Address Registers and a "Go" to the Command Register. The function is automatically completed by the SMD 2180. Both an "Operation Done" interrupt and "Done Status" are provided.

In the following sections, the details of operation and the various options are explored, with extensive use of Figures. (FOR CONVENIENCE, ALL FIGURES ARE FOUND IN APPENDIX A.)

This document is a basic User's Guide for the most fundamental of operations, and makes no attempt to discuss File Management Systems, Disk Operating Systems and other such elaborate program structures.

It may be of value to note that the popular HDC 1880 cartridge disk controller operates as a proper subset of the SMD 2180. Software written for the HDC 1880 will run on the SMD 2180 so long as the file management software recognizes the increased number of sectors and/or cylinders available on the SMD compatible device with respect to those available on the cartridge disk device. Some additional error types are also identified for the SMD device.

I/O REGISTERS

The four input registers and one output register of the SMD 2180 are shown in Figure 1. The registers are referred to as R0, R1, R2 and R3 and are accessed via the IN and OUT (or equivalent) instructions. The absolute I/O address can be selected via the "S1" Dip Switches (See Figure 5). The least significant two bits of the address select one of the four registers.

The IOPB address pointer registers, R1, R2, and R3, must be loaded with a 20-bit memory pointer to the first byte of the IOPB, and are write-only registers.

R0 is both READ and WRITE (STATUS and COMMAND, respectively). The COMMAND Register (R0) format is shown in Figure 1(b). Two functions are performed: CLEAR INTERRUPT and GO.

To clear a pending "Operation Done", interrupt and turn off the "OPER DONE" status bit, write a 02 to R0.

To start a new function specified in the IOPB (pointed to by R1, R2 and R3), write a GO (01) to R0. The user may also write a "CLEAR INT" and "GO" (03) to R0, if desired. The SMD will first clear the interrupt (and status bit), then proceed to execute the command and finally, set the new interrupt (and status bit).

NOTE: It takes approximately 30 μ sec for the SMD 2180 to recognize and respond to "CLEAR INT" or "GO".

The STATUS Register (R0) has two operation status bits and four drive status bits (See Figure 1). The "BUSY" bit indicates when the SMD is busy performing an operation. The "OPERATION DONE INTERRUPT STATUS" bit indicates when a disk operation has been completed. A visual indicator (LED 1) also indicates a pending interrupt. Further information is also found in the IOPB. An interrupt-driven system will typically check the status bit to verify that the disk was the source of an interrupt. More information regarding the interrupts is provided in a later section.

A system that doesn't use interrupts (STATUS Driven) will typically have no need for the STATUS Register and will use the "STATUS CODE" in the IOPB.

The four MSBs of the STATUS Register indicate the READY STATUS of each of up to four separate SMD DRIVES and can be observed at anytime.

I/O PARAMETER BLOCK

The format of the I/O Parameter Block (IOPB) is shown in Figure 2. Although some commands don't need certain parameters, the format of the IOPB is consistent.

COMMAND CODE

A byte that identifies the nature of the operation to be performed. A list of command codes is found in Figure 4.

STATUS CODE

Once a disk command is accepted, operation status is provided. Figure 4 shows three possible status indicators.

80H = Operation Successful, ready for next command

81H = Operation in progress, busy

82H = Error on last command

The user generally initializes the IOPB with a 00 in the STATUS Byte to indicate that the operation has not yet been acknowledged.

ERROR CODE

If STATUS CODE = 82H, it provides one of the error codes found in Appendix B. If STATUS CODE = 80H, it provides the number of automatic RETRYs required before successful completion of the operation. The upper four bits indicate the number of restores and the lower four bits represent the number of retrys after the seek.

UNIT/CYLHI SELECT

Identifies one of four units and the most significant bits of the cylinder number.

CYLINDER SELECT

The eight least significant bits of the starting cylinder number in Binary. Multisector transfers may overlap cylinder boundaries.

STARTING SECTOR

The eight-bit number (0-N) of the starting sector of the operation. Sector numbering is optimized to improve rotational timing efficiency for multisector transfers.

NOTE: The sector and cylinder numbers start from 00

SECTOR COUNT	The eight bit number (1-256) of the sequentially numbered sectors to transfer. A "0", implies a count of 256. "IMPLIED SEEKS" are Automatic when crossing a cylinder or head boundary.
BUFFER MEMORY ADDRESS	The twenty bit address of the memory input or output buffer. The effective address is determined by the REL bit of the XMB as shown in Figure 3. Memory buffers may be allocated anywhere in system-accessible memory space.
HEAD SELECT	Selects the head to be used. The head address is determined by the type of SMD compatible drive being used.
CONTROLLER I/O ADDRESS	<u>Must</u> contain the same I/O address (bits A ₂ - A ₇), as selected by the Dip Switch S1.
BYTES/TRANSACTIONS	Specifies the number of bytes (1-256) to be transferred per MULTIBUS transaction (burst DMA). Allows a bus overhead-to-maximum bus latency trade-off. Most commonly used number is 16 (Decimal). A "0" implies 256 bytes.
LINK/MEMORY ADDRESS TO NEXT IOPB (XMB/MSB/LSB)	The link (LK) bit enables automatic linking. If LK is set (1), the 20-bit effective address points to the next IOPB.

Since the STATUS CODE, and ERROR CODE bytes of the IOPB are updated by the SMD, the IOPB must reside in RAM, although the operating program may reside in PROM.

INTERRUPTS

A software driver for the SMD may be either interrupt-driven or status-driven. A real-time operating environment or a Multi-user system will commonly be interrupt-driven. A single-user oriented software environment will commonly be status-driven.

For an Interrupt-driven system, the interrupt level (INT 0 - INT 7) should be selected via dip switch S2 (See Figure 5). Only one of the eight switches should be thrown to the "ON" position.

For status-driven systems, interrupts may be disabled by throwing all switches of S2 to the "OFF" position.

For systems with a common interrupt line, such as SBC 80/10 based systems, the interrupt handler must poll each device to determine the source of the interrupt. For Polled interrupt systems, the "OPERATION DONE INTERRUPT" Status bit is provided. A visual indicator (LED 1) is also provided on the front of the controller to indicate a Pending Interrupt.

The Interrupt is reset by writing either a "CLR INT" (02) or "CLR INT" and "GO" (03) to the command (RO) register. The interrupt will not be reset until 30 μ sec after receipt of the command.

OPTIONS

Four (4) sets of straps and two (2) 8 bit dip switches are provided to allow flexibility of configuration in a system. Figure 6 (a) and 6 (b) describe the proper usage of the BPRN/ (ABC) option and BPRO/ (DEF) option, respectively.

The BPRN/ option allows for various BUS MASTER PRIORITY arrangements, including both serial and parallel bus priority resolution schemes. When using the serial scheme, the backplane should be strapped as shown in Figure 6 (d). Intel warns that no more than three (3) Bus Masters be daisy-chained in the serial approach (based on use of the SBC 86/12 CPU).

When using external parallel Bus priority resolutions, any number of MASTERS can be employed. The SMD 2180 provides all Bus signals necessary for use in such a scheme, and is used exactly like any other Bus Master.

The BPRO/ (DEF) option (See Figure 6 (b)) allows for use of a SBC 80/10 with the SMD 2180, and possibly another MASTER. The SBC 80/10 must be the lowest priority device and the SMD 2180 must be the next highest priority device. This allows correction of an error in BPRO (sic) Signal polarity on the SBC 80/10 card (which makes it not strictly MULTIBUS compatible).

In general, it is good practice to make the DISK DRIVE a relatively high (if not the highest) priority device in a system.

WARNING: Some Intel supplied card cage/Backplanes use pull-up/pull-down terminating resistors on both BCLK/ and CCLK/ (MULTIBUS pins 13 and 31 respectively). Intel's SBC 80/10 CPU cannot drive these signals since the default strap (as it comes from the factory) ties both signals, and therefore their terminators in parallel. All bus MASTERS (Including the SMD 2180 require BCLK/ to operate.) One must either remove the terminating resistor from one or both signals OR remove the strap tying the signals together on the board. The latter suggestion is the easiest, but will not work if anything requires CCLK/. Interphase suggests removing both sets of terminators unless the bus is expanded beyond eight (8) card slots. The problem is less serious for SBC 80/20, SBC 80/30 and SBC 86/12, since a heavier driver is used on these boards, although a heavily loaded system may still overload the signal.

The M1 strap selects whether a standard SMD is used or a BASF 8" Winchester drive (with SMD option) is used. A standard SMD drive would have 20160 bytes per track whereas the BASF has 13,440 bytes per track unformatted. M2 allows selection or deselection of the Dual Port option available on many SMD compatible drives. M3 strap is used to select the "increment by head" or "increment by cylinder" whenever a track boundary is crossed during a multisector operation.

Figure 5 shows the use of the on board dip switches for selection of interrupt level, I/O Address, and sector size.

SOFTWARE INTERFACE CONSIDERATIONS

The SMD 2180 is exceptionally simple to use. It is essentially automatic in nature, including soft error recovery, and executes MACRO (operation oriented) commands. The software operating environment may be characteristically one of two types, Interrupt-drive or Status-driven.

STATUS-DRIVEN SYSTEMS

Single-user/Single task systems are typically Status-driven; that is once a command is given the program waits for completion of the command, as indicated by observing STATUS, before proceeding to the next operation. This arrangement is perfectly adequate for many systems and is the simplest to implement. For such systems the interrupt is disabled using on-board dip switches S2, as shown in Figure 5.

STATUS-driven systems have no need for the STATUS hardware register (R0), unless DRIVE READY STATUS is of interest, and operate by observing the STATUS CODE byte of the IOPB. When the IOPB is originally written in system memory, the STATUS CODE and ERROR CODE bytes are initialized to 0. When the SMD 2180

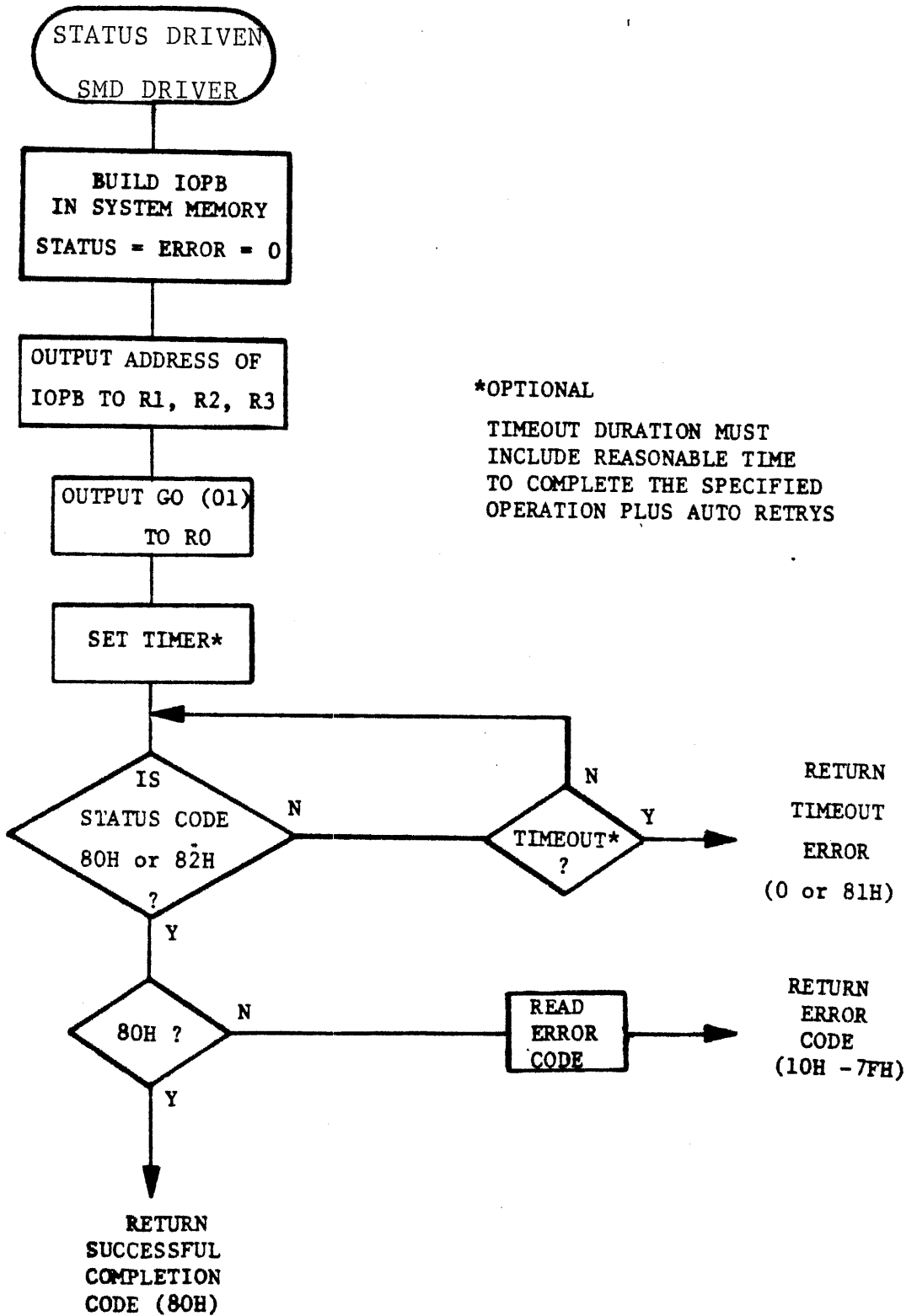
recognizes the "GO" command (01 output to RO), it puts operation status in the STATUS CODE byte. A 81H indicates BUSY (operation in progress), 80H indicates READY FOR NEXT COMMAND (operation successfully completed), and a 82H indicates ERROR ON LAST COMMAND. If an error is indicated, the ERROR CODE byte indicates the nature of the error as defined in Appendix B, and more fully described in the ERROR RECOVERY section.

The only routine precaution that should normally be taken in a STATUS-driven system is a timeout to protect against system hangups. The SMD 2180 has internal timeouts to protect against disk drive oriented hangups and MULTIBUS access timeouts, once the command is accepted, typically 30 μ sec. after issuing the command.

The following flowchart indicates operation of the SMD 2180 in a STATUS-driven system. The timeout is optional and its implementation is determined by system hardware, which normally includes a real time clock (which may run on an interrupt level even though the system is status-driven), or a hardware interval timer. If used as shown in the flowchart, the timeout duration should take into consideration the normal time to complete the given operation, including retries.

Many systems use a fixed location to hold the IOPB to be used by the SMD 2180. In such systems, it is not necessary to rewrite R1, R2 and R3 for each transaction. Except in systems that may routinely have one or more disk drives turned off, or where an operator is required to change a removable cartridge, the Drive READY STATUS bits of RO are seldom observed after initial power ON.

Should a drive be NOT READY at the time of an attempted operation,
a specific error code is returned.



TYPICAL STATUS-DRIVEN SMD HANDLER

INTERRUPT-DRIVEN SYSTEMS

Multi-user/Multi-task and some Real Time systems, are typically Interrupt-driven; that is, once the command is given, the other programs in the system proceed to run and the CPU is notified of completion (successful or not) of the disk function via an interrupt. There must obviously be an interrupt handler program, and the disk task is generally one of a number of tasks scheduled by a Real Time Operating System of some type. The interrupt level is selectable via dip switch S2, can be verified (in a polled-interrupt environment) by reading the hardware STATUS register bit 1 (See Figure 1), and can be reset by outputting a "CLEAR INTERRUPT" (02) to R0, OR, if more work is to be done immediately, by writing a "CLEAR INTERRUPT" and "GO" to R0.

The program must still check the STATUS CODE of the IOPB to determine success of the operation. All ERROR CODES retain the same meanings as in a STATUS-driven system. If multiple tasks, or even multiple CPUs in a multiprocessor system are to have a single task or the operating System itself handle intimate scheduling of disk activities.

In addition to the "OPERATION DONE" interrupt-status bit of register R0 (bit 1), a "DISK BUSY" status bit of R0 (bit0) is provided. It indicates that the SMD 2180 is currently busy doing some operation, and is not available for starting a new command. R0-R3 are, of course, available to any BUS MASTER (CPU or otherwise) on the BUS. If more than one CPU in a multiprocessor system is to have direct access to the SMD 2180, some contention resolution mechanism should be employed, other than simply observing the "DISK BUSY" bit. Recall that it takes

about 30µsec from the time that the SMD 2180 recognizes a "GO" command until the "DISK BUSY" bit goes true. It also takes about 30µsec for the "CLEAR INT" command to remove both the hardware interrupt and the Interrupt Status bit. Care should be taken to not re-enable interrupts in the interrupt handler until at least 30µsec after clearing the interrupt.

A multi-task (but single CPU) system can allow the various tasks to contend for disk access, using the "DISK BUSY" bit (so long as the TASK is not interruptable before the "GO" command), but it is generally advisable to either use a separate DISK HANDLER TASK or have the disk interface handled by the DOS. In such cases, the TASK or DOS will generally provide an elegant command queueing mechanism.

While it may appear that the SMD 2180 is more difficult to use in an interrupt environment, the complexities are really generated by the rest of the system, and not the SMD 2180. The flowchart of the driver is essentially the same as in the Status-driven environment, except that the timeout and reactivations of the TASK are generally handled by the operating system rather than the tight STATUS check program loop of the STATUS-driven system.

AUTOMATIC ERROR RECOVERY

Error Recovery is automatic in the SMD 2180. Errors are considered either as "hard" (non-recoverable) errors, or "soft" (recoverable) errors. Hard error types are described in Appendix B. They include parametric errors, which make the command invalid, disk or bus timeout errors, incorrectly written data

or header field errors, or other conditions which preclude successful disk operation. They may include indications of physical imperfection on the disk platter, whether permanent or removable via reformatting the track or surface.

Before declaring the error to be hard, and therefore, reported as an unsuccessful transaction, the SMD 2180 assumes the error to be soft and attempts to recover.

Soft errors may be caused by momentary transients or by poor head positioning. If the operation is a "READ", the SMD 2180 tries on eight (8) successive revolutions to read the data. If still unsuccessful, it will do a RESTORE, RE-SEEK to the proper cylinder, and up to eight (8) more tries. If still unsuccessful, it declares the error hard and reports it. This allows a disk to gracefully degrade, as may be caused by various types of mistreatment or a high noise environment. In order that the user may know that the disk or system is degrading, before it fails, retry statistics as provided. If the operation is successful, the "ERROR CODE" byte takes the form shown in Figure 4. The upper four (4) bits indicate the number of RESTORES (0 or 1) required, and the lower four (4) bits indicate the number of retries required (0 to 8). These statistics may be used as seen fit by the programmer, and indicate no lack of reliability of the reported data, which must pass stringent security measures before being transferred into memory.

MULTISECTOR TRANSACTIONS/IMPLIED SEEKS

The IOPB allows for transactions longer than one sector. Just as the head need not be positioned (using a "SEEK") prior to issuing a "READ" or "WRITE", the user need not be concerned with head location in multisector transactions that encompass more than one track. Any number of SEEKS may be IMPLIED in a single IOPB transaction so long as only one surface of one platter is used or only one cylinder is used per IOPB. Refer to the discussion of the M3 strap option. Multisector transactions imply transfer of sequentially numbered sectors, starting at the "STARTING SECTOR" byte in the IOPB and continuing for the number of sectors in the "SECTOR COUNT" byte (1-256, with "0" implying 256).

The SMD 2180 employs a physically staggered sector numbering system to optimize the time to transfer multiple sectors of data on to or off the disk. Refer to Figure 8 for the various options.

The terms, "TRACK" and "CYLINDER", are sometimes confusing. The term, "CYLINDER", is an industry-standard term referring to the visualization of the Disk system as a series of concentric cylinders, encompassing any number of disk platters stacked on top of each other. Most platters have both a top and bottom recording surface and a magnetic head for each surface. The term, "Track", refers to a specific "CYLINDER" on a given surface of a given platter. The two (2) terms are commonly used interchangeably throughout industry literature. Some drives have multiple heads per surface which may be moved in tandem to decrease the Seek time to an "effective cylinder". The actual configuration and Head/cylinder/surface mapping is determined by the type of drive.

BAD TRACK MAPPING

The MAP command (85H) allows the user to map a bad track on any surface to a specifiable spare track on any other surface. It can be invoked by the user upon detection of the failure to properly format a track during the formatting cycle. When the MAP command is invoked, a special IOPB must be built to specify the track that is bad and the spare track that is to be substituted for it. Refer to Figure 9. The special IOPB specifies the current track and the target track.

The SMD 2180, upon detection of this command, will first format the bad track with a special format that indicates that it is a bad track plus an encoded pointer that indicates which track is to be substituted for it. Then the controller will seek to the target track and format it to be the logical replacement of the bad track. All of the appropriate seeks to perform this operation are implied and are handled by the controller board.

In subsequent normal operation, whenever the logical track is bad that was referenced, the controller will first seek to the bad track, will discover by reading of the special header that it was bad and then will perform another seek to the track that was substituted for the bad one. All of this is totally transparent to the user, except for the additional seek items required to perform the operation.

This function can effectively relieve the File Management software of this time consuming and irritating task.

INCREMENT BY HEAD OR CYLINDER

The SMD 2180 allows the user to specify whether a multisector transaction that overlaps a track boundary will increment to either the next head or the next cylinder. This is accomplished with the M-3 strap option. With M-3 strap in place, the controller will increment to next head number when crossing a track boundary. When not in place, the controller will increment to next cylinder when crossing a track boundary.

Incrementing to the next head is particularly useful when the user is moving multiple tracks of data and does not want to incur the additional time it takes to do a one track seek in most drives. The head switching time is usually much less than the head movement time in most drives. This may not be very useful or desirable when used in conjunction with those drives that have both fixed and removable media or those drives with a relatively small number of heads.

READ SWITCH COMMAND

For convenience of troubleshooting a new board that is first being installed in a system, the user may, via the IOPB, read the status of the on board sector size switches and the M1, M2 and M3 strap option switches. The Read Switch Command (86H) will read all the switches and encode them as they appear in Figure 10. This byte of data is then written into the IOPB at byte 2. A switch that is connected will be a logic 1.

SEEK COMMAND (OVERLAPPED SEEKS)

All commands to the SMD 2180 that may require head movement are implied seeks. The Seek Command differs in execution from the others in that when it is invoked, it will initiate a seek but will not wait for the completion within the drive before the controller returns back to the user. This mechanism allows the user to perform "overlapped seeks" in a multiple unit system. The user may initiate a seek on one unit then switch to another unit to perform reads or writes while the first unit is doing the head movement.

LINKED IOPBs

Single or multisector transactions may be automatically linked by setting the "LK" bit in the IOPB to "1" and providing a pointer to the next IOPB.

Set up and start the transaction as always. Only the pointer to the first IOPB is written into the address registers. As soon as the first IOPB is accepted, the "STATUS CODE" byte in that IOPB is set to "BUSY" (81H). At the end of the transaction of the first IOPB, its Status byte is set to 80H (or 82H, if in error) in the IOPB, but no interrupt is generated (RO will continue to indicate "BUSY"). If the "LK" is set, the next IOPB is fetched and its "STATUS CODE" byte is set to "BUSY". At completion of that transaction, the "STATUS CODE" byte indicates 80H (or 82H, if in error), and so on until the "LK" bit is not set OR any hard-error is seen in any transaction. In either case, the interrupt, if selected, is generated to indicate completion, successful or not.

In the case of a successfully completed transaction, all "STATUS CODE" bytes in all linked IOPBs will be set to 80H (ready for next command -- no error). Only the last IOPB need be checked because any hard-error in the chained transaction will abort the transaction.

In the case of any hard-error, the user may see where the transaction was aborted by observing the "STATUS CODE" byte in the sequential IOPBs. If an 80H is seen, there was no error.

If an 82H is seen, this is where the chain was broken. All subsequent IOPBs will still show "0" for status to indicate they have not been acknowledged. If the user is interrupted and RO shows "OPERATION COMPLETE", the last IOPB alone will indicate either success or abortion (or Error, if encountered in the last IOPB transaction). Typically, the user will remember only the first and last IOPBs. The last to indicate success, and the first to allow tracking down the problem, if an error occurs. A Status-Driven user may either set a long timeout and observe only the last IOPB, or chose to follow completion of each IOPB in succession.

DATA BUS WIDTH

The SMD 2180 can operate in an 8 bit, 16 bit, and mixed Multibus system. If the BUS bit of the SMD address register (R1) is a 1, the IOPB is in 16 bit System Memory and a 16 bit wide access is made to fetch the IOPB. If it is 0, the IOPB is in 8 bit System Memory. The BUS bits in the XMB bytes (Bytes 7 and 13) of the IOPB can also refer to either 8 or 16 bit data. Accordingly, it is entirely possible to have a mixed system where the normal system memory is 16 bit data and some memory mapped peripheral device buffer is 8 bits wide, or vice versa. It is a requirement in most Multibus systems that any 16 bit word be located on an even address boundary. Care must be taken to ensure that the memory pointers in the IOPB be an even address if word mode is employed. The SMD 2180 will do a check on any pointer in the word mode and will force itself to fall back and run in the byte mode (8 bit) if a pointer starts on an odd address boundary.

ADDRESSING MODES

The SMD 2180 is capable of DMA access to anywhere in the 1 Mbyte address space (20 Address Lines) of the Multibus. Two modes of achieving the 20 bits are provided as shown in Figure 3.

If the REL bit of the XMB byte(s) (either byte 7 or 13) in the IOPB is a 0 (Absolute Mode), the 4 least significant bits of the XMB are the 4 most significant bits of the effective 20 bit address. If the REL bit is 1 (RELATIVE MODE) the effective address is calculated by adding the given address to the segment address (shifted left 4 places). This is most useful in a system using a CPU with "PAGE MODE" addressing such as the SBC 86/12. It can, however, be used in any system for such things as multiprogram memory partitions, dynamic memory allocation (memory management) driver system and the like.

When the relative addressing mode is used, the 4 least significant bits of the XMB are ignored. It should be noted that the hardware address registers (R1-R3) must always point to the absolute location of the IOPB. When the absolute mode is used in the IOPB (bytes 7 and/or 13), the last two bytes (16 and 17) of the IOPB are irrelevant, and can be ignored. Therefore, software written to run on the HDC 1880 (cartridge disk controller) will still operate on the SMD, so long as the file management system recognizes the increased number of available sectors and/or cylinders available on the SMD device with respect to the cartridge system.

HINTS ON USE OF "GO" AND "CLR INT"

The Command Register (RO), as shown in Figure 1, has two bits. The "CLR INT" bit clears the interrupt and its associated Status Bit and LED indicator. The "GO" bit starts the transaction specified by the IOPB.

If the system is interrupt-driven, the interrupt handler must normally reset the source of interrupt while interrupts are still disabled. The user may either simply set or pulse the "CLR INT" bit. If pulsed, the bit must stay on for at least 10 μ sec. Most users will simply toggle the Command Register between a "CLR INT" (02) and a "GO"(01).

Status-driven systems (interrupt disabled) don't require resetting of the interrupt. If the user wishes to observe the operation complete LED, which would otherwise stay on permanently, a combination "CLR INT" and "GO" (03) may be issued. The interrupt bit (and LED 1) is cleared first. This combination command may also be used by an interrupt handler if it wishes to start the next command immediately.

FORMATTING

Before any disk surface may be used to READ or WRITE a sector of data, the surface must be formatted. The formatting operation stores record header information to allow verification of head position before a READ or WRITE to anyplace on the disk. The SMD 2180 "FORMAT" instruction (Command Code = 84H) automatically formats a single track, according to parameters in the IOPB.

To format a surface of a disk platter, one must write a simple iterative program loop, which increments the cylinder select byte of the IOPB and issues a Format Command. Maximum cylinder number varies from drive to drive.

After formatting a surface, it is good practice to "RESTORE" and then "VERIFY" each track, again using a iterative program loop. This merely verifies that all headers have been correctly written and that all data fields are free of defects.

A special feature of the "FORMAT" command allows filling of the data fields with a user definable byte. Since the "FORMAT" uses no memory buffer, the buffer address pointer bytes are not used, as such. The user may specify the fill data by putting the data pattern in the LSB of the buffer address pointer (byte 9).

SYSTEM START-UP CONSIDERATIONS

Although the sequencing of power to the drive and the SMD 2180 is not normally relevant, it is good practice to apply power to the SMD 2180 before the "LOAD" cycle of the disk is activated. Loss of power to the SMD 2180 will deactivate all drive signals. On power up, the STATUS Register (R0), but not the actual interrupt, is indeterminate. The user should first write a 00 to the command register (R0), do a "RESET" command, wait for the DRIVE READY STATUS bit(s) in R0 to go true (this is entirely optional since the SMD 2180 will check STATUS before attempting the next operation in any case), and finally do a "RESTORE" command. Observe the STATUS byte in the IOPB to indicate completion of both the "RESET" and "RESTORE". Be sure to build the complete IOPB, including the I/O address byte, and point the registers R1, R2, and R3 to the IOPB. No other initialization is required. The "RESET" command forces the microcode of the controller to start at 0, and can be invoked at anytime by the user.

IN-CIRCUIT EMULATION

The SMD 2180 will work under in-circuit emulation. One must, however, be aware of certain peculiarities of ICE 80 when used with a SBC 80/10 CPU in a target system, which includes any other BUS MASTER, including the SMD 2180. While it is emulating, the ICE presents a true representation of an 8080 to the target system. While it is not emulating, however, the representation is not valid, and since the 8080 normally controls the bus indirectly via HLDA and other signals, the BUS will lock up. As a result, the ICE should not be single-stepped or break-pointed while the SMD 2180 (or any other Bus Master) is in the middle of an operation on the BUS, i.e., after giving a "GO" command, but before sensing completion.

APPENDIX A

FOR CONVENIENCE, ALL FIGURES ARE PROVIDED
IN THIS SECTION, WHICH MAY BE DETACHED
FOR EASE OF REFERENCE.

1(a)

	WRITE	READ	ADR1	ADRO*
R0	COMMAND	STATUS	0	0
R1	XMB } IOPB MEMORY	---	0	1
R2	MSB } ADDRESS	---	1	0
R3	LSB } REGISTERS	---	1	1

XMB = Extended memory byte (only four [4] least significant bits)

*I/O address bits ADR2 - ADR7 of R0 are defined by dip switch S1 (See Figure 5)

1(b)

COMMAND (R0)	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	CLR INT	GO
STATUS (R0)	7	6	5	4	3	2	1	0
	R4	R3	R2	R1	0	0	OPER DONE INT	BUSY

NOTE: R1 - R4 are the unit ready status bits of Storage Module units 1-4, respectively. (R = 0 = Unit not ready, R = 1 = Unit Ready)

1(c)

XMB (R1)	0	0	BUS	0	A13	A12	A11	A10
----------	---	---	-----	---	-----	-----	-----	-----

BUS = 0 =: 8 BIT DATA BUS

BUS = 1 =: 16 BIT DATA BUS

FIGURE 1: I/O REGISTERS

Byte #

0	COMMAND CODE	SEE FIGURE 4							
1	STATUS CODE*	SEE FIGURE 4							
2	ERROR CODE*	APPENDIX B							
3	UNIT/CYLHI SELECT	U ₄	U ₃	U ₂	U ₁	C ₁₁	C ₁₀	C ₉	C ₈
4	CYLINDER SELECT	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀
5	STARTING SECTOR	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	S ₀
6	SECTOR COUNT	# of Sectors (Binary 1 - 255)							
7	XMB } MSB } Buffer LSB } Memory Address	0	0	BUS	REL	A ₁₃	A ₁₂	A ₁₁	A ₁₀
8		A _F	A _B	A _D	A _C	A _B	A _A	A ₉	A ₈
9		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
10	HEAD SELECT	H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀
11	CONTROLLER I/O ADDRESS	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	0	0
12	BYTES/TRANSACTION	Bus Burst Length (Binary)							
13	LK - XMB } MSB } Next LSB } IOPB Address	LK	0	BUS	REL	A ₁₃	A ₁₂	A ₁₁	A ₁₀
14		A _F	A _E	A _D	A _C	A _B	A _A	A ₉	A ₈
15		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
16	MSB } LSB } ADDRESS SEGMENT (OPTIONAL)	A _F	A _E	A _D	A _C	A _B	A _A	A ₉	A ₈
17		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀

*Updated by SMD. May be initialized to "0" by the requesting program.

LK =: LINK FLAG

LK = 0 = Don't Link

LK = 1 = Auto link to next IOPB

BUS =: BUS TYPE

BUS = 0 = 8 BIT DATA BUS

BUS = 1 = 16 BIT DATA BUS

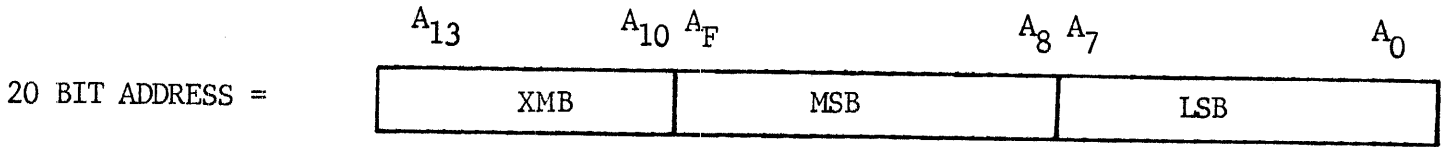
REL =: ADDRESSING MODE

REL = 0 = ABSOLUTE ADDRESSING

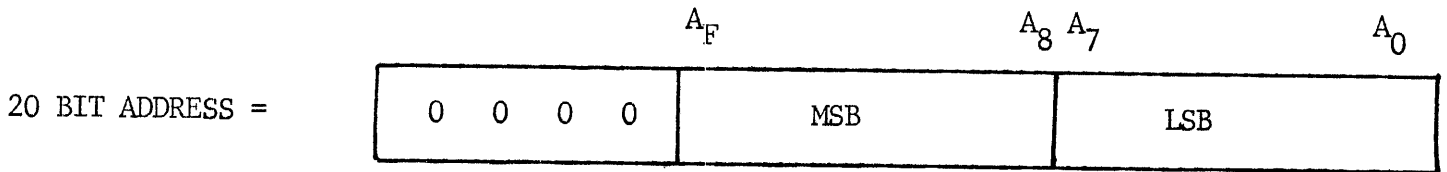
REL = 1 = RELATIVE ADDRESSING

FIGURE 2: IOPB

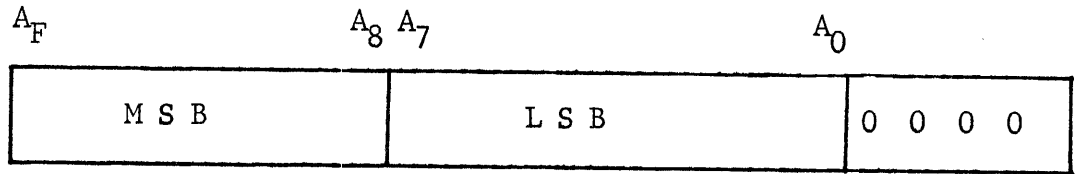
ABSOLUTE ADDRESSING MODE



RELATIVE ADDRESSING MODE



PLUS



(ADDRESS SEGMENT)

NOTE: ALL ADDRESS LINE SUBSCRIPTS ARE HEXADECIMAL

FIGURE 3: ADDRESSING MODES

COMMAND CODES

81	READ **
82	WRITE **
83	VERIFY **
84	FORMAT TRACK **
85	MAP **
86	READ SWITCH
89	RESTORE
8A	SEEK
8B	ZERO SECTOR **
8F	RESET

**MULTISECTOR COMMANDS WITH IMPLIED SEEKS

IOPBs MAY BE CHAINED TOGETHER FOR AUTOMATIC SEQUENTIAL EXECUTION.

STATUS CODES*

80	Operation Successful Ready for next command
81	Operation in progress, Busy
82	Error on Last Command

* INITIALIZE TO "0"

ERROR CODE FOR SUCCESSFULLY COMPLETED OPERATIONS

7	4	3	0
Number of Auto RESTORES		Number of Auto RETRYs	

Note: All numbers are Hexadecimal

SMD 2180

SWITCH SETTINGS

S2

1	INT 0
2	INT 1
3	INT 2
4	INT 3
5	INT 4
6	INT 5
7	INT 6
8	INT 7

INTERRUPT LEVEL SELECT:

Select the desired interrupt level by throwing one (and only one) switch to the "ON" position.

For no interrupt, set all switches to the "OFF" position.

S1

1	ADR 2
2	ADR 3
3	ADR 4
4	ADR 5
5	ADR 6
6	ADR 7

I/O ADDRESS SELECT:

Set the switches to match the I/O address used.

Address bit = 0 Switch "OFF"
Address bit = 1 Switch "ON"

S1

7	SCTS 0
8	SCTS 1

SECTOR SIZE SELECT:

Select the desired sector size by setting the switches as shown:

		SCTS 0	SCTS 1	M1
128 bytes	=	OFF	OFF	X
256 bytes	=	ON	OFF	X
512 bytes	=	OFF	ON	X
512 bytes (FOR CDC Lark)	=	ON	ON	OUT

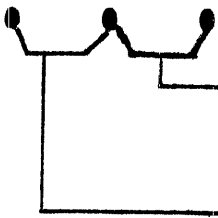
X=Don't care.

FIGURE 5: ON BOARD DIP SWITCHES

6 (a)

BPRN/ OPTION

F E D



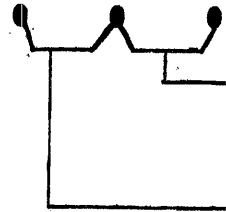
E to D
If Disk is the Highest Priority in a serial Bus Priority System

F to E
If Disk not highest priority OR in a parallel bus priority system

6 (b)

BPRO/ POLARITY OPTION

A B C



B to C
No inversion (SBC 80/05, SBC 80/20, SBC 80/30, SBC 86/12, BLC 80/30)

A to B
Invert BPRO/ (SBC 80/10, BLC 80/10, BLC 80/11, BLC 80/12, BLC 80/14)

6 (c)

●M1●

M1 = No Jumper = Standard SMD
= Jumper = BASF Drive

●M2●

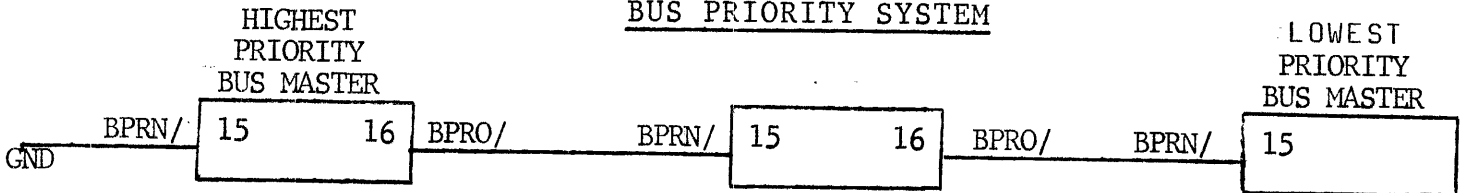
M2 = No Jumper = No Dual Porting
= Jumper = Dual Port

●M3●

M3 = No Jumper = Increment by Cylinder
= Jumper = Increment by Head

6 (d)

BACKPLANE STRAPPING IN A SERIAL BUS PRIORITY SYSTEM



*Not necessary if E - D is made

NOTE: If a SBC 80/10 is used in a Serial Priority System, it MUST be the lowest priority and the SMD 2180 MUST be the next highest priority.

NOTE: A valid BCLK/ (pin 13) signal is required for bus synchronization. A problem with some Intel-provided backplanes when used with a SBC 80/10 is described in the OPTION STRAPS section.

FIGURE 6: OPTION STRAPS

UNIT SELECTION

The jumpers designated H-I-J and K-L-M are used in conjunction with the unit number in the IOPB to select one of sixteen units. Since the IOPB can only address one of four disk drives, the jumpers are used to determine which group of four drives is to be selected.

	JUMPERS		UNIT NUMBERS
1.	I-J	L-M	0 - 3
2.	I-J	K-L	4 - 7
3.	H-I	L-M	8 -11
4.	H-I	K-L	12 -15

For example, if the jumpers are set as in #1, and the unit number byte in the IOPB is 20H, then Unit #1 is selected.

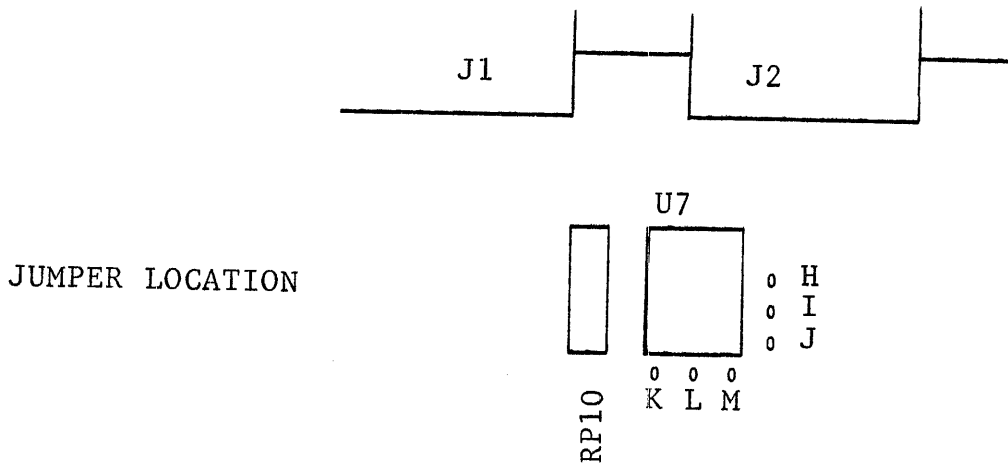


FIGURE 7: UNIT SELECTION

SMD DRIVE (20160 Bytes/Track)

<u>M1</u>	<u>SW 1-8</u>	<u>SW 1-7</u>	<u>Bytes/Sector</u>	<u># of Sectors/Track</u>
OUT	OFF	OFF	128	104
OUT	OFF	ON	256	64
OUT	ON	OFF	512	34
OUT	ON	ON	512	32 ;LARK

BASF DRIVE (13440 Bytes/Track)

<u>M1</u>	<u>SW 1-8</u>	<u>SW 1-7</u>	<u>Bytes/Sector</u>	<u># of Sectors/Track</u>
IN	OFF	OFF	128	76
IN	OFF	ON	256	44
IN	ON	OFF	512	22

FIGURE 8: SMD DRIVE & BASF DRIVE

ALTERNATE TRACK FORMAT:

The IOPB for the alternate track format is as follows:

IOPB	0	---	85H
	1	---	**
	2	---	**
	3	---	Current Cylinder High & Unit Number
	4	---	Current Cylinder Low
	5	---	XX
	6	---	Target Head
	7	---	Target Cylinder High
	8	---	Target Cylinder Low
	9	---	Target Cylinder Fill Character
	10	---	Current Head
	11	---	**
	12	---	**
	13	---	**
	14	---	**
	15	---	**
	16	---	**
	17	---	**

XX = Don't Care

** = Remains the Same

FIGURE 9: SMD 2180 ALTERNATE TRACK FORMAT

INCREMENT BY HEAD:

If the M3 strap is in, the controller will change to the next head instead of the next track when transferring past the last sector of the current track.

READ SWITCHES COMMAND:

When given an 86H command, the controller will read the status of the on board sector size switches and the M1, M2, and M3 straps. This information will be returned in the error code byte of the IOPB. The status byte will read 82H, unless all the switches and straps are off, in which case it will read 80H.

IOPB BYTE 2:

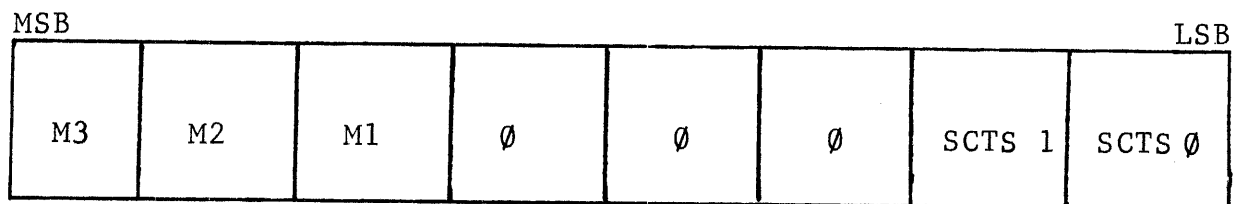


FIGURE 10: READ SWITCH COMMAND (86H)

APPENDIX B

ERROR CODES

APPENDIX B: ERROR CODES

CODE

10 DISK NOT READY

The disk's Ready signal output is tested at the beginning of any command requiring a head movement, i.e., all commands except RESET. Error X'10' is posted if the disk is not ready.

11 INVALID DISK ADDRESS

The unit select bits in the IOPB are examined for the presence of one and only one unit select bit set. Checked on all commands except RESET.

12 SEEK ERROR

All commands except RESET may cause a seek operation to be initiated. The SMD issues a seek command to the disk drive, and, on completion, reads the HEADER of the appropriate sector to verify the location of the head. If wrong, the SMD will execute a Restore and then re-seek the target track. The header will be read again and if the track is still wrong the SMD will post error '12' (Seek Error).

NOTE: All codes are hexadecimal.

13. CHECK SUM ERROR-DATA FIELD

The computed check sum on the data did not agree with the check sum appended to the data on the disk. Eight retries are made before this error is reported.

14 INVALID COMMAND CODE

The command code, byte 0 in the IOPB, was not valid.

15 INVALID TRACK IN IOPB

The target track in the IOPB, byte 3 and 4 in the IOPB, was not accepted as valid by the disk drive. Detected on command strings that cause a seek. The SMD actually sends the track data to the disk and the disk returns (SEEK ERROR). This will happen if the track specified was greater than the capacity of the drive being used. Note that this condition may also cause "FAULT" condition in some drives and should be cleared by issuing a "Restore Command".

APPENDIX B: ERROR CODES

CODE

16 INVALID SECTOR IN COMMAND

The target sector in IOPB, byte 4 in the IOPB, was greater than the capacity of the drive. This check is performed after the seek has been done.

17 SPARE

18 BUS TIMEOUT

Bus acquisition was not made within 1msec. of a request, OR XACK was not received with 1msec. of a MRDC/,MWTC/ or IOWTC/.

19 WRITE ERROR

During a write operation and after the "WRITE GATE" signal has been activated, if the SMD write logic fails in such a manner that it does not request a new byte of data within 1msec., the operation is terminated and error '19' is posted. If at the conclusion of an otherwise successful write sequence the disk is found to be "NOT READY", the SMD posts error '19'. This applies to the WRITE FORMAT command also. No retrys are attempted.

1A DISK WRITE PROTECTED

Posted when attempts are made to write to a disk that is write protected.

1B UNIT NOT SELECTED

A unit select was made and the unit failed to respond with UNIT SELECTED.

1C NO ADDRESS MARK - HEADER FIELD

This error is posted if no sync information is found in the header of the target sector. Eight retrys will be attempted.

1D NO DATA MARK - DATA FIELD

This error is posted if no sync character is detected in the data field or if no data is seen (within the timeout period) prior to or after a good sync sequence. Eight retrys will be made.

APPENDIX B: ERROR CODES

CODE

- 1E UNIT FAULT
A FAULT condition exists in a selected unit, the FAULT should be cleared by a Restore Command.
- 1F DATA OVERRUN TIMEOUT
Error posted if a good sync sequence is detected during a read operation, but at some subsequent point data is not received within the timeout interval. Eight retries will be made.
- 20 SURFACE OVERRUN
Error induced by a long sector count causing the SMD to auto increment the target track greater than its capacity. No retries are made.
- 21 ID FIELD ERROR - WRONG SECTOR READ
The Sector ID information in the header field does not match the target sector value. Eight retries will be made.
- 22 ID FIELD CHECK SUM ERROR
The computed check sum of the header field does not match the check sum read from the disk. Eight retries will be made.
- 23 SPARE
- 24 SPARE
- 25 SPARE
- 26 NO SECTOR PULSE
The sector pulse is missing from a selected unit.

APPENDIX B: ERROR CODES

CODE

27 DATA OVERRUN

A fault caused by missing TX or RX clock.

28 NO INDEX PULSE ON WRITE FORMAT

During a Write Format operation, the SMD looks for the index pulse from the disk. If not found within 65msec. the error is posted. No retrys.

29 RECORD NOT FOUND

If at any point during a read or write type operation the target sector is not found, this error is posted. No retrys.

2A ID FIELD ERROR - WRONG HEAD

The head number read from the disk in the header field was wrong. Eight retrys will be made.

2B INVALID SYNC IN DATA FIELD

The first byte read from the data field was not a valid sync character. Eight retrys will be made.

2C INVALID SYNC IN HEADER FIELD

The first byte read from the header field was not a valid sync character. Eight retrys will be made.

2D SEEK TIMEOUT ERROR

A seek was made and an ON-CYLINDER response did not occur within a specified timeout.

2E BUSY TIME-OUT

2F NOT ON-CYLINDER AT BEGINNING OF A SEEK

30 RTZ TIMEOUT

A Restore command was executed and an ON-CYLINDER did not occur within specified timeout period.

31 FORMAT OVERRUN ON DATA

APPENDIX C

BASF 6172 Eight Inch Winchester Drive
Configuration Notes

SECTOR SIZE SELECTION

Switch P-10 on the back of the BASF 6172 Drive determines the sector size, as shown in the following table. The size should be selected with the drive power turned off. Remember to set the corresponding switch positions on the SMD 2180 controller.

BYTES/SECTOR	SECTORS/TRACK	P10-1	P10-2	P10-3	P10-4
128	76	OFF	ON	ON	OFF
256	44	OFF	ON	OFF	ON
512	22	OFF	ON	OFF	OFF

UNIT ADDRESS SELECTION

Switch 3-E determines the unit number decoded by the BASF drive, as is shown below. The unit number must fall within the range of units selected by option pin jumpers I-J-K-L on the SMD 2180.

<u>UNIT NUMBER</u>	<u>3E-4</u>	<u>3E-3</u>	<u>3E-2</u>	<u>3E-1</u>
0	OFF	OFF	OFF	OFF
1	OFF	OFF	OFF	ON
2	OFF	OFF	ON	OFF
3	OFF	OFF	ON	ON
4	OFF	ON	OFF	OFF
5	OFF	ON	OFF	ON
6	OFF	ON	ON	OFF
7	OFF	ON	ON	ON
8	ON	OFF	OFF	OFF
9	ON	OFF	OFF	ON
10	ON	OFF	ON	OFF
11	ON	OFF	ON	ON
12	ON	ON	OFF	OFF
13	ON	ON	OFF	ON
14	ON	ON	ON	OFF
15	ON	ON	ON	ON

WRITE PROTECTION

Each of the three surfaces may be independently write protected by turning on the corresponding position of Switch 6-E.

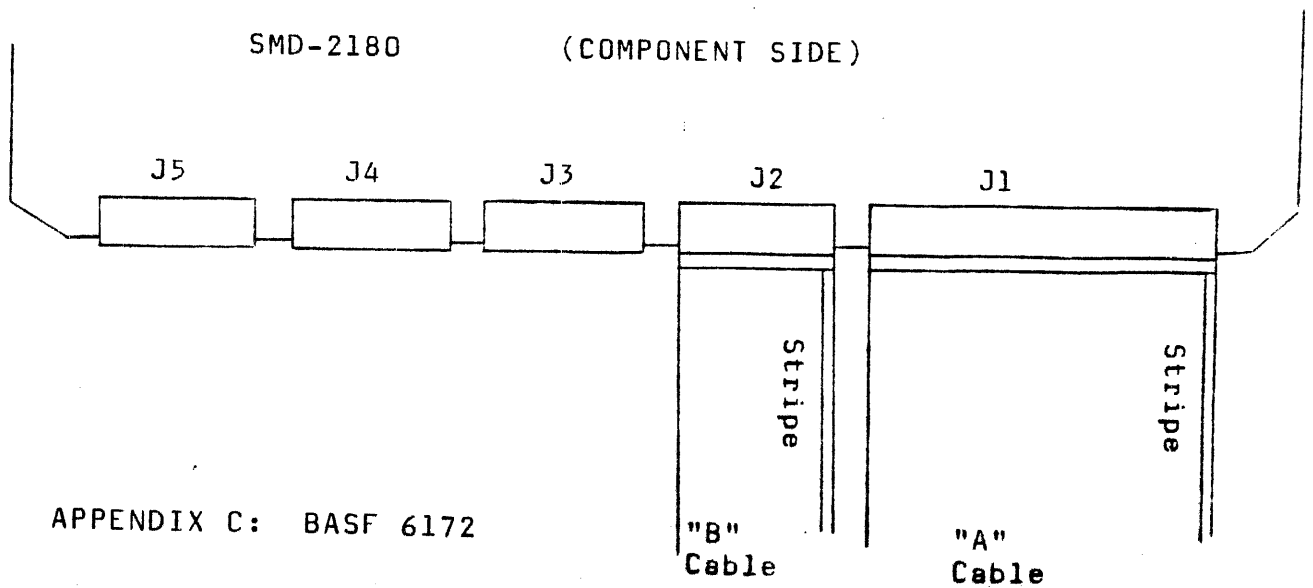
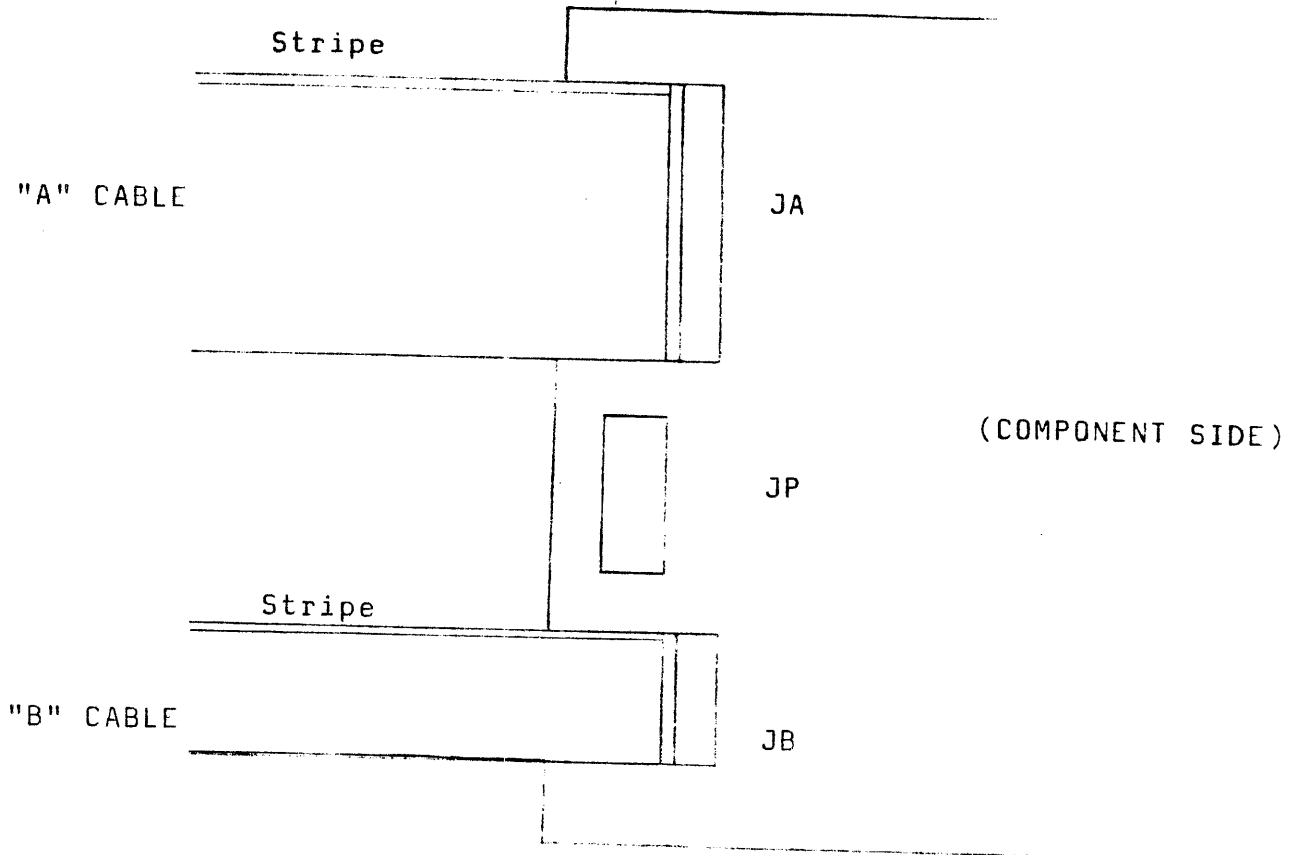
as is shown below:

POSITION	SURFACE
6E-1	0
6E-2	1
6E-3	2

APPENDIX C: BASF 6172

SMD 2180 USERS GUIDE

BASF DRIVE



PHYSICAL SPECIFICATIONS FOR SMD 2180

HEIGHT : 6,75" (to ejector)

WIDTH : 12.0"

THICKNESS: .50"

WEIGHT : 14 oz.

POWER REQUIREMENT: 5vdc \pm 5% , 3.75 amps.

-5vdc \pm 5% , .6 amps.*

CONNECTORS: Bus: Card Edge, 86 pins on .156 center

SMD: "A" Cable - 60 pins

"B" Cable - 26 pins each

Maximum Cable Length : 50 feet

OPERATING TEMPERATURE : 0° - 55° C

* NOTE : THE -5VOLT SUPPLY IN SUCH SYSTEMS MAY NOT SUPPLY SUFFICIENT CURRENT FOR THE SMD DRIVERS AND RECEIVERS. IF THE -5 DROPS BELOW -4.5 WHEN THE SMD DISK CONTROLLER IS INSTALLED, THE -5 CURRENT IS NOT SUFFICIENT.

APPLICATION NOTE 1: 20 BIT ADDRESS

Some back planes do not include the necessary 2.2K pull up resistors on ADDR 10-13 (HEX), the upper four bits of a 20 bit address. Attempting to use 20 bit addressing can cause strange problems on these units. To insure these lines are pulled up, remove all cards in system and check back plane pins 28, 30, 32 and 34 for +5V.

APPLICATION NOTE 2: -5V SUPPLY

Systems not supplying -5V or having an inadequate -5V may necessitate the use of a separate regulator card. The -12V used in the system is regulated down to -5V. This will supply -5 @ 1.0A to pins 9/10 on the system bus.

TYPICAL -5V REGULATOR CARD

