VME-QIC2/X
Cartridge Tape Controller
Hardware Reference Manual

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PREFACE

This manual describes the Integrated Solutions VME-QIC2/X Cartridge Tape Controller board. The text provided in this manual includes a product overview, specifications, configuration information, and programming information. The manual is divided into five sections:

SECTION 1: This section describes the general features and architecture of the VME-QIC2/X tape controller board.

SECTION 2: This section lists the VME-QIC2/X specifications.

SECTION 3: This section provides information regarding the VME-QIC2/X switch and jumper configuration options.

SECTION 4: This section describes the VME-QIC2/X tape controller software interface.

SECTION 5: This section describes the VME-QIC2/X real time clock software interface.

APPENDIX A: This appendix describes the VME-QIC2/X variable length record header block format.

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SECTION 1: INTRODUCTION

1.1 Features

Integrated Solutions' VME-QIC2/X offers a quarter-inch cartridge tape controller and real time clock on a single VMEbus-compatible printed circuit board. The VME-QIC2/X board supports a QIC-02-compatible† quarter-inch cartridge tape transport on a VMEbus-based computer system and offers the following high performance features:

- 48 Kbytes of on-board data buffer for sustained high data transfer rates
- Supports a QIC-02 compatible tape unit
- Optional variable size record support to emulate start/stop tape units
- Programming interface employing packet processing
- Real time clock/calendar (RTC) with battery backup

1.1.1 Data Buffer

The VME-QIC2/X features a 48-KByte data buffer to maximize the throughput of the streaming tape subsystem by minimizing data overruns. Overruns occur due to a mismatch between the sustained data transfer rates of the cartridge tape unit (high) and the overall system (usually much lower). With streaming tape units, overruns result in severe performance degradation. The time required for repositioning (usually from one to two seconds) reduces the effective data transfer rate of a streaming tape unit (90 Kbytes per second for 90 IPS drives) significantly. With the VME-QIC2/X, a tape subsystem can easily operate at up to 90 Kbytes per second throughput.

1.1.2 Variable Size Records

The tape controller reads and writes 512-byte blocks (as defined in the QIC-02 specification), but also provides support for variable size logical records. To support variable length logical records, the VME-QIC2/X writes an internally generated header block (see Appendix A) at the beginning of each logical record. This header block contains the length of the logical record in bytes and the number of 512-byte data blocks. On read operations, the header block allows the tape controller to track the length of the logical records on the tape. This method of variable length record support means the VME-QIC2/X operates more efficiently when writing longer records since there is a fixed amount of overhead per record. Variable length record support is required in order to adequately emulate industry standard half-inch tape drives which support variable block sizes.

1.1.3 Programming Interface

The VME-QIC2/X tape controller software interface corresponds very closely to the DEC TS11 interface (a DEC half-inch start/stop tape controller interface). Consequently, operating system TS11 drivers can be easily adapted for use with the VME-QIC2/X.

† The terms VME-QIC2/X and QIC-02 are used throughout this manual. VME-QIC2/X is the name of the Integrated Solutions' cartridge tape controller. QIC-02 is a streaming cartridge tape unit interface specification and is used to designate units adhering to this specification.

The VME-QIC2/X communicates with the host CPU via four VMEbus word locations that function as device registers. These device registers are the first four words on a 16-word boundary. Three word locations function as device registers for the tape controller, while the fourth word supports the RTC (Sections 4 and 5 of this manual provide more detailed software interface information regarding the tape controller and RTC, respectively).

The VME-QIC2/X tape controller uses a mechanism called *packet processing* in order to receive commands from the host as well as to return subsystem status to the host. With packet processing, the host creates command packets in system memory that supply the VME-QIC2/X with commands and their associated parameters. The CPU then writes the address of the command packet into the VME-QIC2/X tape controller device registers. When the VME-QIC2/X receives a command packet address, it retrieves the command packet from system memory via DMA transfer and executes the command. Upon completion of the command, tape subsystem status is written to the Status Register, which can be read by the host CPU. Additional status information in the form of a message packet is provided via DMA transfer from the VME-QIC2/X to a previously defined location in system memory called the message buffer.

The commands and subcommands directly supported by the VME-QIC2/X Tape Controller include the following:

Write Characteristics
Read Next
Write Next
Write Tape Mark
Position
  Space Records Forward
  Space Records Reverse
  Skip Tape Marks Forward
  Skip Tape Marks Reverse
  Rewind
Get Status
Tape Subsystem Initialize

1.1.4 Real Time Clock

The RTC consists of a CMOS clock/calendar, lithium battery, micropower crystal oscillator, and power failure detection and cutover circuits. The lithium battery will power the clock for approximately five years before a replacement is required.

1.2 Architecture

The major functional elements of a fully configured VME-QIC2/X board include the following:

- Control microprocessor (Z8002B)
- 48-KByte data buffer
- EPROM-resident firmware and diagnostics
- VMEbus interface logic (Bus Request/Grant, Address Decode, Interrupt Request)
- CMOS RTC with battery backup

1.2.1 Control Microprocessor

The high speed Z8002B 16-bit microprocessor directly controls all communications across the VMEbus host interface and all operations of the tape unit. Use of a 16-bit microprocessor gives the VME-QIC2/X a high level of functionality in order to offload the host CPU.

1.2.2 Data Buffer

All data is transferred between the tape unit and main memory through an on-board 48-Kbyte buffer memory implemented with 8K x 8 static RAMs. Using this RAM, a caching algorithm avoids overruns, which typically occur with non-buffered controllers.

1.2.3 EPROM

All VME-QIC2/X operations are controlled and monitored by the firmware which resides in EPROM. The firmware can easily be changed in the field if upgrades are ever necessary.

1.2.4 VMEbus Interface

The VME-QIC2/X interfaces with the VMEbus as either a 24 or 32 address bit, 16 data bit master† and either a 16, 24, or 32 address bit, 16 data bit slave†† (as defined in the *VMEbus Specification Manual*, Motorola part number MVMEBS/D1). The VMEbus interface logic on the VME-QIC2/X board provides interfacing capability consistent with the VMEbus specification for the following VME-defined functional modules:

1. Data Transfer Bus Requester-- This is the bus acquisition interface based on a Bus Request/Bus Grant protocol. There are actually four priority levels (0-3) of these lines defined on the VMEbus. Each level supports a *daisy chain propagation* priority scheme among multiple requesters on that level. Prioritization also exists among levels, with highest priority going to Level 3. Levels 0 through 3 may be jumper selected on the VME-QIC2/X.
2. Data Transfer Bus (DTB) Master-- This is the ability to initiate data transfer cycles across the VMEbus DTB. Once acquisition of the bus has occurred, the VME-QIC2/X may directly access the host memory (an A24/D16 or A32/D16 master selection is via jumpers as described in Section 3).
3. Interrupter-- The Interrupter performs three tasks. It asserts the selected interrupt request line, supplies a status/ID (vector) byte to the data bus when its request has been acknowledged, and propagates the interrupt acknowledge daisy chain signal if not requesting the acknowledged level of interrupt. There are seven levels (1–7) of interrupt request supported on the VMEbus, with Level 7 being the highest priority. The VME-QIC2/X allows jumper selection of one level from Levels 4–7; Levels 1–3 are not selectable.
4. Slave-- This is the ability to respond to an access attempt by a master. Determination of an attempt to access is based on recognition of a certain address range and the appropriate address modifiers (A16/D16, A24/D16, or A32/D16 slave operations may be selected via jumpers as described in Section 3).

1.3 Slave Addressing

The VME-QIC2/X board utilizes 16 one-word VMEbus locations (currently only the first four word locations are defined). The addressing may be set for 16-bit (short I/O), 24-bit (standard), or 32-bit (extended) addressing.

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† A24/D16 or A32/D16 master

†† A16/D16, A24/D16, or A32/D16 slave

SECTION 2: SPECIFICATIONS

This section provides performance specifications and operating requirements for the VME-QIC2/X.

2.1 Form Factor

The VME-QIC2/X form factor is standard double-sized VMEbus - 160mm x 233.33mm.

2.2 Compatibility

The VME-QIC2/X plugs into a VMEbus based system and supports a QIC-02-compatible quarter-inch cartridge tape drive. The VME-QIC2/X interfaces with the VMEbus as defined in the *VMEbus Specification Manual*, Motorola part number MVMEBS/D1 (configuration jumpers and switches associated with DTB requester levels, interrupt levels, DTB master and slave are discussed in Section 3). Tables 2-1 and 2-2 provide the pin assignments and signal mnemonics for the VME-QIC2/X VMEbus connectors P1 and P2, respectively.

The VME-QIC2/X controller attaches to the QIC-02 compatible quarter-inch cartridge tape drive via a 50-pin connector, J1. Table 2-3 provides the J1 connector pin assignments.

2.3 Tape Controller Software Interface

The VME-QIC2/X software interface corresponds closely to the DEC TS11 interface. Consequently, UNIX or other operating system TS11 drivers can be easily modified (if required) for use with the VME-QIC2/X.

2.4 Transfer Rate

The VME-QIC2/X controller supports data transfer rates up to 90 KBytes/second.

2.5 Real Time Clock

The real time clock (RTC) consists of a CMOS clock/calendar, lithium battery, micropower crystal oscillator, and power failure detection and cutover circuits. A new battery will power the clock for approximately five years. The real time clock register handles all commands and data necessary for clock/calendar functions.

2.6 Indicators

The VME-QIC2/X board has four LEDs. The functions of these LEDs are as follows:

- DS1 – QIC-02 Exception (EXC*) signal (on indicates active)
- DS2 – QIC-02 Ready (RDY*) signal (on indicates active)
- DS3 – Reserved
- DS4 – Diagnostics (see Section 2.7)

Table 2-1. VMEbus Connector P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK†	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK†	A17
22	IACKOUT*	SERDAT†	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*†	A10
29	A02	IRQ2*†	A09
30	A01	IRQ1*†	A08
31	-12V†	+5V STDBY†	+12V†
32	+5V	+5V	+5V

NOTE

An asterisk following a signal name indicates that the signal is true when the signal is low.

† VMEbus signals, but no connection on VME-QIC2/X board.

Table 2-2. VMEbus Connector P2 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	n/c†	+5V	n/c
2	n/c	GND	n/c
3	n/c	n/c	n/c
4	n/c	A24	n/c
5	n/c	A25	n/c
6	n/c	A26	n/c
7	n/c	A27	n/c
8	n/c	A28	n/c
9	n/c	A29	n/c
10	n/c	A30	n/c
11	n/c	A31	n/c
12	n/c	GND	n/c
13	n/c	+5V††	n/c
14	n/c	D16††	n/c
15	n/c	D17††	n/c
16	n/c	D18††	n/c
17	n/c	D19††	n/c
18	n/c	D20††	n/c
19	n/c	D21††	n/c
20	n/c	D22††	n/c
21	n/c	D23††	n/c
22	n/c	GND	n/c
23	n/c	D24††	n/c
24	n/c	D25††	n/c
25	n/c	D26††	n/c
26	n/c	D27††	n/c
27	n/c	D28††	n/c
28	n/c	D29††	n/c
29	n/c	D30††	n/c
30	n/c	D31††	n/c
31	n/c	GND	n/c
32	n/c	+5V	n/c

† n/c means not connected on the VME-QIC2/X board.

†† VMEbus signals, but no connection on the VME-QIC2/X board.

Table 2-3. I/O Port Connector J1 Pin Assignments†

Pin Number	Signal Mnemonic	Signal Name
2	–	Reserved
4	–	Reserved
6	–	Reserved
8	–	Reserved
10	–	Reserved
12	HB7*	Data Bus 7
14	HB6*	Data Bus 6
16	HB5*	Data Bus 5
18	HB4*	Data Bus 4
20	HB3*	Data Bus 3
22	HB2*	Data Bus 2
24	HB1*	Data Bus 1
26	HB0*	Data Bus 0
28	ONL*	On Line
30	REQ*	Request
32	RST*	Controller Reset
34	XFR*	Transfer
36	ACK*	Acknowledge
38	RDY*	Ready
40	EXC*	Exception
42	DIR*	Direction
44	–	Reserved
46	–	Reserved
48	–	Reserved
50	–	Reserved

† All odd pins on the J1 connector are connected to ground.

2.7 Diagnostics

The VME-QIC2/X board has an automatic self test at power on with LED indication upon successful completion (i.e., DS4 comes on at reset and is turned off following successful completion of the self test). LED DS4 is under firmware control. DS4 can mean any one of the three following things depending on its signal pattern:

1. After a power up when the tape unit is idle, DS4 flashes with an approximate 1/2-second on, 1/2-second off signal pattern.
2. When the tape unit is rewinding the tape or executing the tape retension command, DS4 flashes with a faster rate of approximately 1/5-second on, 1/5-second off signal pattern.
3. When the tape controller has detected a fatal error condition either at power on or while operating, it continuously flashes a fatal error signal pattern. The patterns (a combination of short and long flashes) and their corresponding definitions are provided in Table 2-4. The tape controller remains in the fatal error mode until a subsystem Reset command is issued to the controller. Each repetition of the error pattern is followed by approximately a one-second pause.

Table 2-4. DS4 Fatal Error Signal Patterns

Code	LED Indication	Failure
0000	short, short, short, short	Memory Bank 0 (RAMs at U39 and U40)
0001	short, short, short, long	Memory Bank 1 (RAMs at U37 and U41)
0010	short, short, long, short	Memory Bank 2 (RAMs at U38 and U42)
0011	short, short, long, long	No RAM in Bank 0
0100	short, long, short, short	NMI received by Z8002 when not on the bus - hardware problem
0101	short, long, short, long	Drive error at power up.
0110	short, long, long, short	An attempt to get the tape drive to BOT failed.
1000	long, short, short, short	Invalid vectored interrupt vector - hardware problem
1001	long, short, short, long	Detected VMEbus IACK with no interrupt pending - hardware problem

2.8 Addressing

The VME-QIC2/X uses four one-word control registers. Three words function as tape controller device registers, while the fourth word is the control register for the real time clock/calendar. The control register map is shown in Figure 2-1. Although only the first four registers shown in the register address map are defined, the VME-QIC2/X still occupies a 16-word address space. The remaining address locations are reserved and cannot be assigned to other functions since the VME-QIC2/X bus drivers are enabled during accesses to these other locations.

VMEbus Base Address	Write	Read
Base Adrs.†	TCPR	TCPR
Base Adrs. +2	TXCPR	TSSR
Base Adrs. +4	Clock Register	Clock Register
Base Adrs. +6	ATXCPR	Reserved
Base Adrs. +8	Reserved	Reserved
Base Adrs. +10	Reserved	Reserved
Base Adrs. +12	Reserved	Reserved
Base Adrs. +14	Reserved	Reserved
Base Adrs. +16	Reserved	Reserved
Base Adrs. +18	Reserved	Reserved
Base Adrs. +20	Reserved	Reserved
Base Adrs. +22	Reserved	Reserved
Base Adrs. +24	Reserved	Reserved
Base Adrs. +26	Reserved	Reserved
Base Adrs. +28	Reserved	Reserved
Base Adrs. +30	Reserved	Reserved

Figure 2-1. VME-QIC2/X Control Register Map

2.9 Address Modifiers

The VME-QIC2/X can be configured to respond (as a VMEbus slave) to a variety of short, standard, or extended supervisory and non-privileged accesses. These different configurations are jumper and switch selectable as described in Section 3.

2.10 Electrical Requirements

The VME-QIC2/X requires 3.5 amps of +5 Vdc ±5%.

2.11 Environmental Requirements

The VME-QIC2/X environmental requirements are as follows:

Temperature:

0 to 50 degrees centigrade (operating)
-40 to 65 degrees centigrade (non-operating)

Humidity:

10 to 95 percent (non-condensing)

† Refer to Section 3 for VME-QIC2/X VMEbus base address configurations.

2.12 VMEbus Specified Options

The VME-QIC2/X board provides the following options in accordance with the VMEbus specifications:

Master Data Transfer Options

Any one of A24:D16 or A32:D16 (Stat)
TOUT = Any one of 16, 32, 64, or 128 microseconds (Stat)

Slave Data Transfer Options

Any one of A16:D16, A24:D16, or A32:D16 (Stat)

Arbiter Options (not applicable)

Requester Options

Any one of R(0), R(1), R(2), R(3) (Stat)

Interrupt Handler Options (not applicable)

Interrupter Options

Any one of I(4), I(5), I(6), I(7) (Stat)

SECTION 3: CONFIGURATION

This section describes how to configure the VME-QIC2/X board. There are 19 jumper pairs located on the VME-QIC2/X, J2 through J20. There are also two switch banks, SW1 and SW2. SW1 is a four-bit DIP switch, while SW2 is a 10-bit DIP switch. The functions and configuration of these jumpers and switches are discussed in the subsections that follow. Figure 3-1 is a layout of the VME-QIC2/X board that shows the locations of the configuration jumpers and switches. The factory default configurations are shown in boldface type.

3.1 VMEbus Request Level (J2–J9 and J11–J14)

Jumpers J2–J9 and J11–J14 are used to select the VMEbus request level to be used for VMEbus data transfer bus (DTB) master cycles. There are four VMEbus request levels, Levels 0 through 3. The jumper configurations for each level are provided in Table 3-1. All other configurations are illegal.

Table 3-1. VMEbus Request Levels

Bus Request Level	Jumpers Installed
Level 0	J2, J4, J6, J8-1 to J9-1, J8-2 to J9-2, and J11
Level 1	J2, J4, J6-1 to J7-1, J6-2 to J7-2, J8, and J12
Level 2	**J2, J4-1 to J5-1, J4-2 to J5-2, J6, J8, and J13**
Level 3	J2-1 to J3-1, J2-2 to J3-2, J4, J6, J8, and J14

3.2 VMEbus Cycle Timeout (J15–J18)

Jumpers J15–J18 are used to select the VMEbus cycle timeout for VMEbus DTB master cycles. Only one of the four jumpers should be installed. The jumper configurations and corresponding timeout values are given in Table 3-2.

Table 3-2. VMEbus Cycle Timeouts

Timeout	Jumper Installed
J18	16 microseconds
J17	**32 microseconds**
J16	64 microseconds
J15	128 microseconds

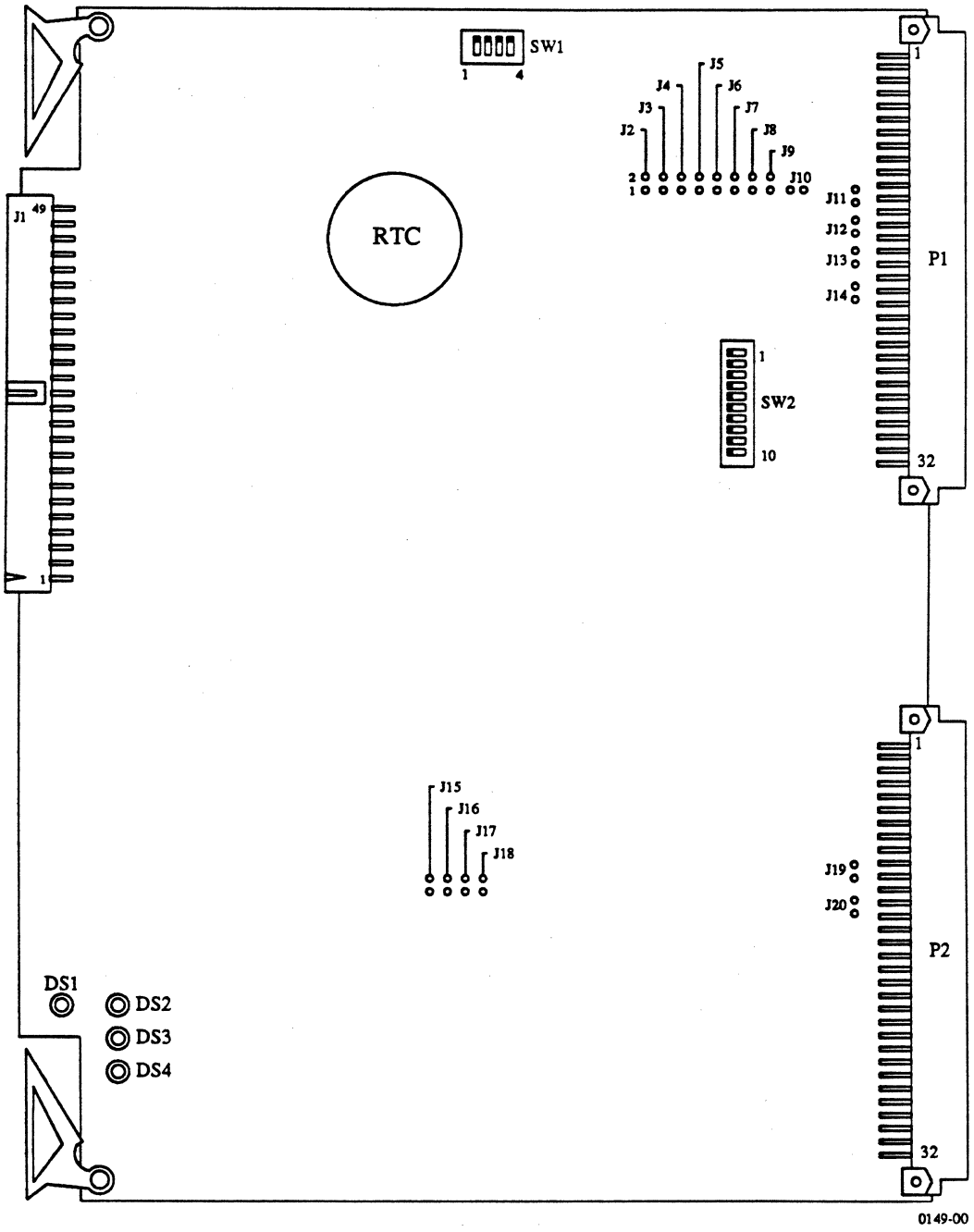

Figure 3-1. VME-QIC2/X Board Layout

3.3 VMEbus Interrupt Level (SW1-3 and SW1-4)

Switches SW1-3 and SW1-4 control the VMEbus interrupt request level. The VME-QIC2/X can request an interrupt at interrupt Levels 4, 5, 6, or 7 on the VMEbus. The switch setting for each of the valid VME-QIC2/X interrupt request levels are provided in Table 3-3.

Table 3-3. VMEbus Interrupt Levels

SW1-3	SW1-4	VME Interrupt Level
open	open	Level 7
open	closed	Level 6
closed	open	Level 5
closed	**closed**	**Level 4**

3.4 VMEbus Interrupt Vector (SW1-1)

Switch SW1-1 is used to select the VMEbus base interrupt vector that is generated in response to VMEbus interrupt acknowledge cycles. The two possible base interrupt vectors and the corresponding switch configurations are supplied in Table 3-4. The actual interrupt vector used can be calculated as follows: [base interrupt vector + (VMEbus interrupt level -4)].

Table 3-4. VMEbus Base Interrupt Vectors

SW1-1	VMEbus Base Interrupt Vector
open	**94 hex**
closed	98 hex

3.5 DTB Master Cycle Address Modifiers (SW1-2 and J10)

Switch SW1-2 and jumper J10 are used to select the VMEbus address modifier that is generated for VMEbus DTB master cycles. The switch and jumper configurations and the corresponding address modifiers are given in Table 3-5.

Table 3-5. DTB Master Cycle Address Modifiers

SW1-2	J10	Address Modifier
open	**jumper**	**3D hex (Standard supervisor data)**
open	no jumper	39 hex (Standard user data)
closed	jumper	0D hex (Extended supervisor data)
closed	no jumper	09 hex (Extended user data)

NOTE

If the controller is configured to generate standard (24-bit) address modifiers (i.e., SW1-2 is open), but a 32-bit address is supplied (i.e., the MSB is non-zero), the address modifier generated will be changed to the corresponding extended address modifier.

3.6 VMEbus Slave Address Configurations (J19, J20, and SW2)

Jumpers J19, J20, and switch SW2 are used to select the VMEbus addresses to which the VME-QIC2/X controller will respond. J19, J20, SW2-1, and SW2-10 are used to select the address modifiers. They also select the most significant one, three, or five nibbles of the short (A16), standard (A24), or extended (A32) addresses, respectively (see Table 3-6). SW2-2 through SW2-9 are used to select the values for the second and third nibbles of the addresses to which the controller will respond. In Table 3-6 the letter *X* in the address means that the particular nibble of the VMEbus address is ignored. A question mark (?) means that the particular nibble of the VMEbus address is selected by SW2-2 through SW2-9.

Table 3-6. J19, J20, SW2-1, and SW2-10 Configurations

SW2-1	SW2-10	J19	J20	Address Modifier (Hex)	Address (Hex)	Notes	Slave Mode
closed	**closed**	**jumper**	**jumper**	**3D,3E**	**XXFFF??X**		**A24**
closed	closed	jumper	no jumper	2D	XXFFF??X	Invalid	
closed	closed	no jumper	jumper	39,3A,3D,3E	XXFFF??X		A24
closed	closed	no jumper	no jumper	3D	XXFFF??X		A24
closed	open	jumper	jumper	3D,3E	XXXXF??X	Invalid	
closed	open	jumper	no jumper	2D	XXXXF??X		A16
closed	open	no jumper	jumper	39,3A,3D,3E	XXXXF??X	Invalid	
closed	open	no jumper	no jumper	3D	XXXXF??X	Invalid	
open	closed	jumper	jumper	3D,3E	XXDFF??X		A24
open	closed	jumper	no jumper	2D	XXDFF??X	Invalid	
open	closed	no jumper	jumper	39,3A,3D,3E	XXDFF??X		A24
open	closed	no jumper	no jumper	3D	XXDFF??X		A24
open	open	jumper	jumper	09,0A,0D,0E	FFFFF??X		A32
open	open	jumper	no jumper	09,0A,0D,0E	XFFFF??X		A32
open	open	no jumper	jumper	0D,0E	FFFFF??X		A32
open	open	no jumper	no jumper	0D,0E	XFFFF??X		A32

Switches SW2-2 through SW2-9 select nibbles two and three of the address to which the controller will respond. The switch address bit correspondence is provided in Table 3-7. A closed switch is used to select a zero for the corresponding address bit, while an open switch selects a one for the corresponding address bit.

Table 3-7. SW2-2 through SW2-9 Switch Settings

Address Bit	Switch	Default Position (XXXXX55X)
A11	SW2-5	**closed**
A10	SW2-2	**open**
A9	SW2-3	**closed**
A8	SW2-4	**open**
A7	SW2-9	**closed**
A6	SW2-6	**open**
A5	SW2-7	**closed**
A4	SW2-8	**open**

SECTION 4: TAPE CONTROL SOFTWARE INTERFACE

4.1 Overview

The VME-QIC2/X utilizes command packets, stored in system memory, to receive commands from a host. Some commands have various subcommands called modes. The device interface registers are used to initiate command packet processing and to retrieve basic status. This section describes register manipulation and provides an overview of the packet protocols (the format used to transfer commands, data, and extended status). Table 4-1 provides a command summary. A detailed description of each command is contained in Section 4.4.

Table 4-1. VME-QIC2/X Command Summary

Command Name	Mode Name/Description
GET STATUS	Get Status (update the extended status registers in the message buffer in memory)
READ†	Read Data
WRITE CHARACTERISTICS	Load Message Buffer Address and Set Device Characteristics
WRITE	Write Data
POSITION†	Space Records Forward Space Records Reverse Skip Tape Marks Forward Skip Tape Marks Reverse Rewind
FORMAT	Write Tape Mark
INITIALIZE	Controller Initialize

† The QIC-02 specification does not allow a tape write operation to occur after a tape read operation has been started, except immediately following a file mark. Consequently, the appending of data to an existing file is impossible. This means that once a Space Records Forward command has been done, write operations are not permitted unless a file mark has just been encountered. The Space Records Reverse command is implemented on the VME-QIC2/X by rewinding the tape and then spacing forward the appropriate number of files and/or records. This command has the same restriction that once a space records reverse is done, no write operations are permitted unless the tape has been positioned just past a file mark boundary. Since the Skip Tape Marks Forward command always leaves the tape at a file mark boundary, the above restrictions do not apply to it. The Skip Tape Mark Reverse command is implemented by first rewinding the tape and then skipping forward the appropriate number of tape marks. Since the Skip Tape Mark Reverse operation always positions the tape just before a tape mark (logically), the command can never be followed immediately by a tape write operation.

The VME-QIC2/X tape subsystem uses four device registers to support tape control functions. These registers occupy three VMEbus word locations. The device registers are

- Status Register (TSSR)
- Command Pointer Register (TCPR)
- Extended Command Pointer Register (TXCPR)
- Alternate Extended Command Pointer Register (ATXCPR)

The TCPR and TXCPR (or ATXCPR) form a 30-bit (or 32-bit) register that is loaded from the VMEbus to initiate an operation. The TCPR is a read/write register; the TXCPR and ATXCPR are write-only registers. To initiate a command, the TXCPR or ATXCPR should be loaded by a word (16-bit) VMEbus write with the high-order portion of the command pointer. Subsequently, the TCPR should be loaded by a word (16-bit) VMEbus write with the low-order portion of the command pointer. The command pointer is then used by the VME-QIC2/X to retrieve the command packet from system memory. The contents of the command packet instruct the controller regarding the operations to be performed. The command packet also defines any function parameters such as a data buffer address, byte count, record count, and modifier flags.

The TSSR is a 16-bit read-only register maintained by the VME-QIC2/X. Major tape controller and drive status are contained in this register.

When a command is to be processed, a command packet must first be assembled in system main memory. The command packet ranges in length from one word to four words long, although four words are always read by the controller. All command packets must begin on a word boundary (even address). The words in the command packet can be thought of as the contents of three registers:

- Command Register (CMDR)
- Data Pointer Register (DPR)
- Byte Position Count Register (BPCR)

The CMDR contains the code for one of the commands listed in Table 4-1. The DPR, a two-word (32-bit) field, contains the address of the data buffer to be processed. It consists of a low-order address word containing the low order 16 bits of the data pointer, followed by a high-order address word containing the high order 16 bits of the data pointer. When the command does not involve a data buffer, the two DPR words are not used in the command packet, and the BPCR immediately follows the CMDR.

When the command is processed by the VME-QIC2/X, a message buffer located in system memory returns status information to the host. The VME-QIC2/X requires that the message buffer address be supplied via a Write Characteristics command, the first command issued following an Initialize. Until a Write Characteristics command is issued, all other commands will be rejected.

The BPCR is used to indicate the number of bytes to be read or written during a data transfer. It is also used to specify the number of records in a Space Records command or the number of tape marks in a Skip Tape Marks command. The CMDR specifies the function to be executed by the VME-QIC2/X.

4.2 Register Definitions

The VME-QIC2/X tape subsystem maintains four registers on the VMEbus and four more remote registers in the message buffer area of system memory. The VME bus registers are

- TCPR
- TXCPR
- ATXCPR
- TSSR

The remote registers in the message buffer are Extended Status Registers 0-3 (XST0 - XST3). Register formats and bit definitions for all of these registers are contained in the sections that follow.

4.2.1 Command Pointer Register (TCPR)

The TCPR is a 16-bit write-only VMEbus register located at the first VMEbus address (VMEbase). This register should be written only with a 16-bit VMEbus operation to specify the low-order 16 bits of the command pointer. (The high-order bits of the command pointer should have previously been written to the TXCPR or ATXCPR register.) The VME-QIC2/X responds whenever the TCPR location is written, but the controller is only activated if the Subsystem Ready (SSR) bit in the TSSR is set. If SSR is not set, the Register Modification Refused (RMR) bit in the TSSR is set, and the new command pointer is ignored.

The TCPR register is illustrated in Figure 4-1; the bits are defined in Table 4-2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00

Figure 4-1. TCPR Register Format

Table 4-2. TCPR Register Bit Definitions

Bit	Name	Definition
15	P15	Command Pointer Bit 15
14	P14	Command Pointer Bit 14
13	P13	Command Pointer Bit 13
12	P12	Command Pointer Bit 12
11	P11	Command Pointer Bit 11
10	P10	Command Pointer Bit 10
9	P09	Command Pointer Bit 9
8	P08	Command Pointer Bit 8
7	P07	Command Pointer Bit 7
6	P06	Command Pointer Bit 6
5	P05	Command Pointer Bit 5
4	P04	Command Pointer Bit 4
3	P03	Command Pointer Bit 3
2	P02	Command Pointer Bit 2
1	P01	Command Pointer Bit 1
0	P00	Command Pointer Bit 0

4.2.2 Extended Command Pointer Register (TXCPR)

The TXCPR is a 16-bit write-only VMEbus register located at the VMEbus base address + 2 (VMEbase + 2). This register should be written with a 16-bit VMEbus operation to specify the high-order 14 bits of the 30-bit command pointer. The low-order 16 bits of the command pointer should subsequently be written to the TCPR register. The TXCPR need not be reloaded for subsequent command pointers, unless the contents must be altered. (When modified, it must be loaded prior to loading the TCPR.) The TXCPR is cleared by an Initialize.

As implied by the bit assignments, when the TXCPR is written to by the host CPU, one of two possible operations may occur. The first operation results in a subsystem initialization. The subsystem initialization occurs when Bit 15 is set to 1 (if Bit 14 is also set to 1, a tape retension operation also occurs). Second, the host CPU can write the most significant 14 bits of a 30-bit command packet pointer address to TXCPR Bits 0 through 13. In this case Bits 15 and 14 must both be 0. The VME-QIC2/X responds whenever the TXCPR location is loaded. With the exception of the Initialize operation, data is only accepted when the SSR bit in the TSSR is set. If SSR is not set, the Register Modification Refused (RMR) bit in the TSSR is set, and the new data is ignored. The TXCPR register is illustrated in Figure 4-2 and the bits are defined in Table 4-3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INIT	RET	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16

Figure 4-2. TXCPR Register Format

Table 4-3. TXCPR Register Bit Definitions

Bit	Name	Definition	Bit	Name	Definition
15	INIT	When set to 1, this bit causes an Initialize	7	P23	Command Pointer Bit 23
14	RET	When set to 1, this bit causes a Retension Tape operation (if Bit 15 is also 1)	6	P22	Command Pointer Bit 22
13	P29	Command Pointer Bit 29	5	P21	Command Pointer Bit 21
12	P28	Command Pointer Bit 28	4	P20	Command Pointer Bit 20
11	P27	Command Pointer Bit 27	3	P19	Command Pointer Bit 19
10	P26	Command Pointer Bit 26	2	P18	Command Pointer Bit 18
9	P25	Command Pointer Bit 25	1	P17	Command Pointer Bit 17
8	P24	Command Pointer Bit 24	0	P16	Command Pointer Bit 16

4.2.3 Alternate Extended Command Pointer Register (ATXCPR)

The ATXCPR is a 16-bit write-only VMEbus register located at the VMEbus base address + 6 (VMEbase + 6). This register should be written with a 16-bit VMEbus operation to specify the high-order 16 bits of the 32-bit command pointer. The low-order 16 bits of the command pointer should subsequently be written to the TCPR register. The ATXCPR need not be reloaded for subsequent command pointers, unless the contents must be altered. (When changed, it must be loaded prior to loading the TCPR.) The ATXCPR is cleared by an Initialize.

The ATXCPR and TXCPR are duplicate ways to load the upper 16 bits of the command pointer. Unlike the TXCPR, Bits 15 and 14 of the ATXCPR are the most significant two bits of the command pointer. Consequently, when using the ATXCPR, an Initialize and a Retension Tape operation cannot be initiated by setting these bits. The ATXCPR format is illustrated in Figure 4-3 and the bits are defined in Table 4-4.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16

Figure 4-3. ATXCPR Register Format

Table 4-4. ATXCPR Register Bit Definitions

Bit	Name	Definition	Bit	Name	Definition
15	P31	Command Pointer Bit 31	7	P23	Command Pointer Bit 23
14	P30	Command Pointer Bit 30	6	P22	Command Pointer Bit 22
13	P29	Command Pointer Bit 29	5	P21	Command Pointer Bit 21
12	P28	Command Pointer Bit 28	4	P20	Command Pointer Bit 20
11	P27	Command Pointer Bit 27	3	P19	Command Pointer Bit 19
10	P26	Command Pointer Bit 26	2	P18	Command Pointer Bit 18
9	P25	Command Pointer Bit 25	1	P17	Command Pointer Bit 17
8	P24	Command Pointer Bit 24	0	P16	Command Pointer Bit 16

4.2.4 Status Register (TSSR)

The TSSR is a sixteen bit read-only VMEbus register located at the VMEbus base address + 2 (VMEbase + 2). The TSSR contains the major status of the drive and controller. The TSSR register format is illustrated in Figure 4-4 and the bit definitions are contained in Table 4-5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC	0	0	RMR	NXM	NBA	0	0	SSR	ONL	0	0	TC2	TC1	TC0	0

Figure 4-4. TSSR Register Format

Table 4-5. TSSR Register Bit Definitions

Bit	Name	Definition
15	SC	Special Condition — When set, indicates that the last command was not completed without incident: either an error was detected or an exception condition (e.g., tape mark, reverse motion at BOT, etc.) occurred. Also set by the error bits in TSSR: RMR and NXM. Indicates that the Termination Class (TC) bits are nonzero (unless RMR is the only error — see RMR). SC is cleared by initialize.
14	—	Not used; always set to 0.
13	—	Not used; always set to 0.
12	RMR	Register Modification Refused — Set when the TCPR, TXCPR, or ATXCPR is written from the VMEbus and Subsystem Ready (SSR) is not set. Causes the SC bit to be set, but no TC (the VME-QIC2/X never sees the data written). RMR setting indicates a fatal controller or software bug.
11	NXM	Non-existent memory — Set when trying to do a DMA transfer to/from memory and a VMEbus error occurs (BERR* is asserted). May occur when fetching a command packet, fetching or storing data, or storing the message packet.
10	NBA	Need Buffer Address — When set, indicates that the VME-QIC2/X needs a message buffer address. Set by Initialize.† Cleared during the Write Characteristics command (if a valid address was given). If NBA is set and any command other than Write Characteristics is given, the operation is terminated with Function Reject status.
9-8	—	Not used; always set to 0.
7	SSR	Subsystem Ready — When set, indicates that the VME-QIC2/X is not busy and is ready to accept a new command pointer. Cleared by writing the TCPR with a new command pointer. Also cleared by Initialize, then set upon completion.
6	ONL	On-Line — When set, indicates that the tape transport is off line and unavailable for any commands requiring tape motion. This bit causes a TC 3 (results in Nonexecutable Function (NEF) status). This bit does not indicate the current status of the transport; it is updated only upon command completions.

(continued on next page)

† The NBA bit is also set when a new tape cartridge is inserted into the tape drive.

Table 4-5. TSSR Register Bit Definitions (*continued*)

Bit	Name	Definition
5-4	—	Not used; always set to 0.
3-1	TC<2:0>	Termination Class Code — Each of the eight possible values of this three-bit field represents a particular class of errors or exceptions. The conditions in each class have similar significance and recovery procedures (where applicable). The codes are 0 Normal Termination 1 Attention Condition 2 Tape Status Alert 3 Function Reject 4 Unrecoverable Error — Tape position lost. 5 Unrecoverable Error — Tape position lost. 6 Unrecoverable Error — Tape position lost 7 Fatal Controller Error
0	—	Not used, always set to 0.

4.2.5 Extended Status Register 0 (XST0)

XST0 appears as the fourth word in the message buffer returned by the VME-QIC2/X upon completion of a command. The XST0 register is illustrated in Figure 4-5. Bits are defined in Table 4-6.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	0	ONL	IE	0	1	WLK	BOT	EOT

Figure 4-5. XST0 Register Format

Table 4-6. XST0 Register Bit Definitions

Bit	Name	Definition
15	TMK	Tape Mark Detected — Set whenever a tape mark is detected during a Read, Space or Skip command, and also as a result of the Write Tape Mark command.
14	RLS	Record Length Short — This bit indicates that either the record length was shorter than the specified byte count on read operations, a Space Records operation encountered a tape mark or BOT before the count was exhausted, or a Skip Tape Marks command was terminated by encountering BOT or a double tape mark (if that operational mode is enabled, see LET and ESS) prior to exhausting the position counter.

(continued on next page)

Table 4-6 XST0 Register Bit Definitions *(continued)*

Bit	Name	Definition
13	LET	Logical End of Tape — Set only on the Skip Tape Marks command when either two contiguous tape marks are detected, or when moving off of BOT and the first record encountered is a tape mark. The setting of this bit does not occur unless this mode of termination is enabled through use of the Write Characteristics command.
12	RLL	Record Length Long — When set, indicates that the record read was longer than the byte count specified. (This bit is always 0 in RAW mode.)
11	WLE	Write Lock Error — When set, indicates that a write operation was issued, but the mounted tape cartridge write protect rotary switch was set to *SAFE* (write protected).
10	NEF	Nonexecutable Function — When set, indicates that a command could not be executed due to one of the following conditions: • The command specified reverse tape direction, but the tape was already at BOT. • Any command, except Get Status or Initialize, was issued when the transport was off line. • Any Write command was issued when the tape cartridge write protect rotary switch was set to SAFE (also causes write lock status - WLE).
9	ILC	Illegal Command — Set when a command is issued and either its command field or its mode field contains codes that are not supported by the VME-QIC2/X.
8	ILA	Illegal Address — Set when a command specifies an odd address where an even one is required.
7	—	Not used; always set to 0.
6	ONL	On Line — When set, indicates that the attached tape transport is on line and operable. When clear and a command requiring motion is issued, causes NEF (TC 3).
5	IE	Interrupt Enable — Reflects the state of the IE bit supplied on the last command.
4–3	—	Not used; always set to 0.
2	WLK	Write Locked — When set, indicates that the mounted tape cartridge write protect rotary switch is in the SAFE position. The tape is, therefore, write protected.
1	BOT	Beginning of Tape — When set, indicates that the tape is (logically) positioned at the BOT holes in the tape.
0	EOT	End of Tape — This bit is set whenever the tape is (logically) positioned at or beyond the EOT holes in the tape. Does not reset until the tape passes over the detector in the reverse direction under program control. If the controller is read buffering (prereading records from tape automatically) and the EOT holes are seen, this bit is not set until the system actually requests the record associated with the EOT. EOT on write causes uncorrectable error status (TC6).

4.2.6 Extended Status Register 1 (XST1)

XST1 appears as the fifth word in the message buffer returned by the VME-QIC2/X upon completion of a command. The XST1 register is shown in Figure 4-6. Bits are defined in Table 4-7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	UNC	0

Figure 4-6. XST1 Register Format

Table 4-7. XST1 Register Bit Definitions

Bit	Name	Definition
15–2	—	Not used; always set to 0.
1	UNC	Uncorrectable Data or Hard Error — Set in response to the tape transport reporting of a read/write error to indicate that an uncorrectable data error has occurred (causes TC6).
0	—	Not used; always set to 0.

4.2.7 Extended Status Register 2 (XST2)

XST2 appears as the sixth word in the message buffer returned by the VME-QIC2/X upon completion of a command. The XST2 register is illustrated in Figure 4-7. The 16 bits of the XST2 register are not used and are always set to 0. Note that the low-order eight bits of this register have special meaning for the Write Characteristics command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-7. XST2 Register Format

4.2.8 Extended Status Register 3 (XST3)

XST3 appears as the seventh word in the message buffer returned by the VME-QIC2/X upon completion of a command. The XST3 register is illustrated in Figure 4-8; the bits are defined in Table 4-8.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	REV	0	0	0	0	RIB

Figure 4-8. XST3 Register Format

Table 4-8. XST3 Register Bit Definitions

Bit	Name	Definition
15-6	—	Not used; always set to 0.
5	REV	Reverse — Set when the current operation causes reverse tape motion; clear when operation is forward or rewind.
4-1	—	Not used; always set to 0.
0	RIB	Reverse into BOT — When set, indicates that a Space or Skip command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion halts at BOT.

4.3 Packet Processing

The CPU passes control information to the VME-QIC2/X via a command packet (see Figure 4-9) located in system main memory. Similarly, the controller returns status information to the host via a message packet also located in system main memory. A command is initiated by the CPU writing the location of the command buffer into the TXCPR (or ATXCPR) and TCPR registers. The controller then becomes busy, fetches the command and associated parameters from the command buffer, executes the command, stores the status into the message buffer, interrupts the host (if so programmed), and becomes idle. The CPU then examines the TSSR and the extended status in the message buffer to determine the success or failure of the command. Every command is handled in this basic manner. The following sections discuss buffer control and message buffer format.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACK	Device Dependent			Mode Code				IE	0	0	Command Code				
Low-Order Data Pointer Address A<15:0>															
High-Order Data Pointer Address A<31:16>															
Count Parameter															

Note: Not all words are required for all commands.

Figure 4-9. Command Packet Format

4.3.1 Buffer Ownership and Control

To prevent the controller from updating the message buffer while the CPU is reading it, or the CPU from updating the command buffer while the controller is reading it, the concept of ownership is defined. Each buffer may be owned by either the controller or the CPU. A buffer must only be modified by the current owner. Ownership of a buffer may only be transferred by its current owner. There are four combinations of transferring the two buffers in the two directions (see Table 4-9):

- Command Buffer: CPU to controller (by the CPU)
- Command Buffer: controller to CPU (by the controller)
- Message Buffer: CPU to controller (by the CPU)
- Message Buffer: controller to CPU (by the controller)

An Initialize aborts any current operation and gives ownership of both the command buffer and the message buffer to the CPU.

Table 4-9. Buffer Ownership Transfers

Buffer	Direction	Transfer Method
Command Buffer	CPU to the Controller	The CPU transfers ownership of the command buffer to the controller by writing the address of the command buffer into the TXCPR (or ATXCPR) and the TCPR registers. This clears the SSR bit in the TSSR.
Command Buffer	Controller to the CPU	The controller transfers ownership of the command buffer back to the CPU by depositing a message packet (in the message buffer) that has the Acknowledge (ACK) bit set in the message header word. After the message is deposited by the controller, it sets the SSR bit in the TSSR to indicate that the message is in the message buffer. If the message does not contain the ACK bit set, the CPU knows that the controller did not see the last command buffer and that the CPU still owns the command buffer. The command may be re-issued by the CPU.
Message Buffer	CPU to the Controller	The CPU transfers ownership of the message buffer to the controller by setting the ACK bit in the command buffer and then initiating the command by writing the command buffer address into the TXCPR (or ATXCPR) and the TCPR. If the command buffer does not contain the ACK bit, the controller knows that the CPU did not see the last message buffer and the controller still owns it. In this case, the controller, in response to the CPU writing into TCPR sets SSR and performs an interrupt (if the Interrupt Enable (IE) is set) without sending out a message.
Message Buffer	Controller to the CPU	The controller transfers ownership of the message buffer to the CPU by writing the message buffer, setting the SSR bit and interrupting if IE is set. This typically happens at the end of a command.

During normal command processing, the ownership of both buffers passes simultaneously, first from CPU to controller (at the start of command processing, when the CPU writes a command pointer into the TXCPR or ATXCPR and the TCPR register), and then from controller to CPU (upon completion of the command).

4.3.2 Message Packet Format

Figure 4-10 illustrates the format of the message packet. This format is used for all messages. The message consists of a header word, a data field length word, a residual byte/record/tape-mark count word, and four extended status registers. Table 4-10 describes the message packet. Tables 4-11 and 4-12 provide the termination class code and message code descriptions, respectively.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Reserved			Class Code							Message Type				
ACK	0	0	0	C	C	C	C	0	0	0	m	m	m	m	m
Reserved								Data Field Length							
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0
RBCPR															
XST0															
XST1															
XST2															
XST3															

Figure 4-10. Message Packet Format

Table 4-10. Message Packet Field Definitions

Word	Bit	Description
1	15	ACK (Acknowledge) — This bit is set by the VME-QIC2/X to inform the CPU that the command buffer is now available for subsequent command packets.
1	14-12	Reserved — These bits are reserved for future enhancements. They always appear as zero.
1	11-8	Class Code Field — These bits define the class of failure determined for the rest of the message buffer when the message type field is not indicating a normal END message. The codes are described in Table 4-12.
1	7-5	Not used, always set to 0.

(continued on next page)

Table 4-10. Message Packet Field Definitions (*continued*)

Word	Bit	Description
1	4-0	Message Type Code — This field indicates the format and length of message packets. For the VME-QIC2/X, the message type is of the form 10*xxx* (indicates that the message contains a header word, and then *xxx* data/status words containing status relevant to the TC code returned). This field indicates the general type of message contained in the buffer and is related to the termination class code appearing in the TSSR register (see Table 4-11).
2	15-8	Not used; always set to 0.
2	7-0	Data Field Length — This field specifies how many bytes of information follow this word in the message packet. This field contains a value of 10 (00001010), indicating that the packet contains the RBPCR plus four extended status registers.
3	15-0	Residual Byte/Record/File Count Register — After a Read command, this word contains the difference between the number of bytes specified in the command and the number of bytes actually transferred from tape. In other words, this register indicates by how much the tape record fell short of the expected length. After a Space Records or Skip Tape Marks command, this register contains the difference between the number of records or tape marks specified in the count word of the command and the number of records or files actually skipped. Note that spacing and skipping operations can terminate before the count is exhausted for a variety of reasons (e.g., tape mark, BOT).
4	15-0	Extended Status Register 0 — See Section 4.2.4 for a description of this register.
5	15-0	Extended Status Register 1 — See Section 4.2.5 for a description of this register.
6	15-0	Extended Status Register 2 — See Section 4.2.6 for a description of this register.
7	15-0	Extended Status Register 3 — See Section 4.2.7 for a description of this register.

Table 4-11. Termination Class Code Descriptions

Message Type	Class Code	Definition
—	0000	Not used.
FAIL	0001	Illegal Command (ILC), Illegal Address (ILA), or Need Buffer Address (NBA) on function reject (TC3).
FAIL	0010	Write-Lock Error (WLE) or Non-Executable Function (NEF) on function reject (TC3).

Table 4-12. Message Code Descriptions

Termination Class Code	Message Type	Definition
0,2	10000	End
3	10001	Fail
4,5,6,7	10010	Error

4.3.3 General Status Handling Information

Table 4-13 summarizes the relationship between the termination class code (appearing in the TSSR register) and the message type code (appearing in the header word of the message buffer after a message packet has been deposited by the controller).

Table 4-13. Termination Class/Message Type Relationship

TC2-0 Value	Message Type	Meaning
0	END	Normal Termination — The operation completed without incident.
1	—	Not currently supported.
2	END	Tape Status Alert — A status condition is encountered that may have significance to the program. Bits of interest in the extended status registers include TMK, EOT, RLS, RIB, LET, and RLL.
3	FAIL	Function Reject — The specified function was not initiated. Bits of interest include ONL, BOT, WLE, NEF, ILA, and ILC.

(continued on next page)

Table 4-13. Termination Class/Message Type Relationship (*continued*)

TC2-0 Value	Message Type	Meaning
4–6	ERROR	Unrecoverable Error — Tape position has been lost. No valid recovery procedures exist. Bits of interest include WLK, EOT, NXM, and UNC.
7	ERROR	Fatal Subsystem Error — The subsystem is incapable of properly performing commands, or at least its integrity is seriously questionable.

The following points should be noted in reference to status and error handling:

1. Error bits in the TSSR register (SC and RMR) are cleared by successfully loading a command pointer into the TCPR register and by successfully depositing an END message.
2. All commands (even the Get Status command) clear the internal copy of each error bit in the extended status registers. Therefore a Get Status command does not return the error bits as set up by a previous tape operation.
3. A read operation that immediately encounters a TMK does not transfer any data and gives a Tape Status Alert termination. The TMK and RLS status bits are set, and the RBPCR word in the message buffer contains the original byte count.
4. A space records operation automatically terminates when a tape mark is traversed, and the TMK status bit is set. Also, RLS is set if the record count is not decremented to zero.
5. A skip tape marks operation automatically terminates when two consecutive tape marks are encountered and the Enable Skip Stop (ESS) mode is enabled via the Write Characteristics command. RLS is set if the count is not decremented to zero. The same is also true if a tape mark is the first record off BOT and both the ESS and ENB bits were set in the previous Write Characteristics data word.
6. Every Write, Write Tape Mark, and Erase command that is executed after EOT results in an Unrecoverable Error termination.
7. A Space Reverse or Skip Tape Marks Reverse command that encounters BOT after the operation is underway results in a tape status alert termination (the RIB status bit is set).
8. If a Space Records Reverse or Skip Tape Marks Reverse command is issued while the tape is already at BOT, a function reject (nonexecutable function) status is returned.
9. When a Rewind command is issued, the termination message and interrupt does not occur until the tape reaches BOT and has stopped. If the tape is already at BOT when the command is issued, the transport is still commanded to rewind to ensure proper tape positioning.
10. Certain failures can result in no interrupt even though the specified command had IE set. These failures include Nonexistent Memory Error (NXM), since the failure could have occurred before the IE bit was fetched from the command packet.

4.4 Commands

The following sections describe the general command format. Then, each command is described in detail.

4.4.1 Command Packet Definitions

Logically, a command packet is composed of four 16-bit words; one to four of which are used, depending on the type of command and the amount of information the controller needs to proceed with execution (all commands cause four words to be fetched by the controller; unused words are ignored). All command packets begin with a command packet header word (see Figure 4-11). The format of this word is the same for all commands; the encoding of the various fields within the word distinguishes one command from another. Table 4-14 defines the fields within the header word. The following sections describe each command in detail, along with its specific command packet format.

Certain bits of the header word and other words within the command packet are not defined for all commands. When building the command packet, all undefined bits should be set to 0. If any undefined bit is not 0 for a command, the command is not executed, and is terminated with a Function Reject (TC 3).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode							Command				
ACK	1	0	SWB	m	m	m	m	IE	0	0	0	c	c	c	c

Figure 4-11. Command Packet Header Word Format

Table 4-14. Command Packet Header Word Bit Definitions

Bit	Name	Function
15	Acknowledge (ACK)	This bit should be set when issuing a command and the CPU owns the message buffer. Its function is to inform the VME-QIC2/X that the message buffer is now available for any pending or subsequent message packets. This passes ownership of the message buffer to the controller.
14-12	Device Dependent Bits	These three bits perform functions applicable to particular commands. The bit definitions are as follows: — Bit 14 is not used and should always be set to 1. — Bit 13 is not used and should always be set to 0. SWB Swap Bytes (Bit 12) — When cleared, instructs the VME-QIC2/X to alter the sequence of storing and retrieving tape data bytes from the CPU memory. When SWB is 1, the *first* byte in a word is the least significant byte (bits 7–0). When SWB is 0, the industry standard method is specified in which the first byte of a word is considered to be the most significant byte (bits 15–8). Figure 4-12 shows the positions of the bytes in the case of a Forward Read or Write with even byte count. Figure 4-13 shows the positions of the bytes in the case of a Forward Read with odd byte count.

(continued on next page)

Table 4-14. Command Packet Header Word Bit Definitions (*continued*)

Bit	Name	Function
11-8	Command Mode Field	This field acts as an extension to the command code field and allows further specification of device commands. Valid command modes include the following: Read (0000) – Read Forward Write Characteristics (0000) Write (0000) – Write Data Position 0000 – Space Records Forward 0001 – Space Records Reverse 0010 – Skip Tape Marks Forward 0011 – Skip Tape Marks Reverse 0100 – Rewind (Record Count ignored)
7	IE	This field defines the state of interrupt enable as follows: 0 = interrupt disable 1 = interrupt enable
6-5	—	Not used, always set to 0.
4-0	Command Code	This field defines the major command category. It is used together with the command mode field to specify the command. Valid commands and corresponding codes are as follows: 01111 Get Status 00001 Read 00100 Write Characteristics 00101 Write 01000 Position 01001 Format 01011 Initialize

Swap Bytes = 1
Buffer Address = 1000 hex
Byte Count = 8 bytes

1000	1	0
1002	3	2
1004	5	4
1006	7	6

Swap Bytes = 0
Buffer Address = 1000 hex
Byte Count = 8 bytes

1000	0	1
1002	2	3
1004	4	5
1006	6	7

Swap Bytes = 1
Buffer Address = 1001 hex
Byte Count = 8 bytes

1000	0	
1002	2	1
1004	4	3
1006	6	5
1008		7

Swap Bytes = 0
Buffer Address = 1001 hex
Byte Count = 8 bytes

1000		0
1002	1	2
1004	3	4
1006	5	6
1008	7	

Note: Byte 0 indicates the byte nearest to BOT.

Figure 4-12. Memory/Tape Data Byte Positioning (Case 1)

Swap Bytes = 1
Buffer Address = 1000 hex
Byte Count = 7 bytes

1000	1	0
1002	3	2
1004	5	4
1006		6

Swap Bytes = 0
Buffer Address = 1000 hex
Byte Count = 7 bytes

1000	0	1
1002	2	3
1004	4	5
1006	6	

Swap Bytes = 1
Buffer Address = 1001 hex
Byte Count = 7 bytes

1000	0	
1002	2	1
1004	4	3
1006	6	5

Swap Bytes = 0
Buffer Address = 1001 hex
Byte Count = 7 bytes

1000		0
1002	1	2
1004	3	4
1006	5	6

Note: Byte 0 indicates the byte nearest to BOT.

Figure 4-13. Memory/Tape Data Byte Positioning (Case 2)

4.4.2 Get Status Command

Figure 4-14 illustrates the Get Status command packet. This command causes a message packet to be deposited in the message buffer area in order to update the extended status registers. However, after the end of any command, the VME-QIC2/X automatically updates the extended status registers. Therefore, the Get Status command is generally only used when a status register update is desired with no tape motion.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl ACK	Device Dependent			Mode				IE			Command				
	1	0	0	0	0	0	0		0	0	0	1	1	1	1
Not Used															

Figure 4-14. Get Status Command Packet

4.4.3 Read Command

Figure 4-15 illustrates the command packet for a read operation. There is one mode of operation, Read Forward (mode 0000). A TS11 Read Retry (mode 0010) causes an illegal command status (ILC).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode							Command				
ACK	1	0	SWB	0	0	0	0	IE	0	0	0	0	0	0	1
Low-Order Data Pointer Address															
A15															A0
High-Order Data Pointer Address															
A31															A16
Buffer Extent (byte count) (16-bit unsigned value)															

Figure 4-15. Read Command Packet

The command packet for a read contains four words: a header word, two words specifying the memory address of the buffer where the data will be stored, and a buffer extent (byte count) word specifying the number of bytes in the data buffer and the number of bytes to be read. A byte count of 0 specifies that 65,536 (64K) bytes are to be read. The third word in the packet specifies the high order address bits of the data buffer pointer, while the second word specifies the low order address word.

4.4.3.1 Blocked Mode

The read operation is assumed to be for a logical record of known length. Therefore, the correct record byte count (fourth word of the packet) must be known. If the byte count exactly equals the logical record length, normal termination occurs. If the logical record is shorter than the specified byte count, the RLS error bit in XST0 is set and a Tape Status Alert termination occurs. If the logical record on tape is larger than the byte count the RLL error bit in XST0 is set and a Tape Status Alert termination again occurs. However, in this case, only the number of bytes specified in the byte count field is transferred to the data buffer. Also, any read operation that encounters a tape mark does not transfer any data. In this case, the TMK and RLS bits are set and a Tape Status Alert termination is returned.

4.4.3.2 RAW Mode

In RAW mode[†], the number of 512-byte blocks read is (specified byte count + 511) ÷ 512 (the byte count rounded up to the next multiple of 512)/512. However, only the specified number of bytes are transferred to the host (extraneous bytes are discarded). If the subsystem is unable to read the specified number of blocks due to encountering a file mark, the TMK and RLS bits are set and a Tape Status Alert termination is returned. In this case, the number of bytes transferred is the specified number minus the value returned in the residual byte count field (this value should always be a multiple of 512).

[†] RAW mode is supported by VME-QIC2/X firmware versions 4.3 and later.

4.4.4 Write Characteristics Command

Figures 4-16 and 4-17 illustrate the Write Characteristics command packet format and characteristics data format, respectively. The objective of this command is to inform the VME-QIC2/X of the location and size of the message buffer and to define certain operating parameters. The message buffer must be at least seven contiguous words long and it must be located on a word boundary.

The Write Characteristics command also transfers a characteristics mode word to the controller and an additional control word. The characteristics mode word causes specific actions for certain operational modes. The bits for this word are defined in Table 4-15.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode							Command				
ACK	1	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
Low-Order Characteristic Data Address															
A15															A0
High-Order Characteristic Data Address															
A31															A16
Buffer Extent (byte count) (16-bit unsigned value)															

Figure 4-16. Write Characteristics Command Format — Command Packet

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Low-Order Message Buffer Address															
A15															A0
High-Order Message Buffer Address															
A31															A16
Message Buffer Extent (byte count) (16-bit unsigned value >= 14)															
0	0	0	0	0	0	0	0	ESS	ENB	0	0	RAW	Q11	FMT	0

Figure 4-17. Write Characteristics Command Format — Characteristic Data

Table 4-15. Characteristics Mode Data Word Bit Definitions

Bit	Name	Definition
15-8	—	Not used. These bits are not checked by the VME-QIC2/X. Their state does not affect operation but they should be set to 0.
7	ESS	Enable Skip Tape Marks Stop — When set, this bit instructs the controller to stop and set the LET status bit during a Skip Tape Marks command when a double tape mark (two contiguous tape marks) is detected. Setting this bit also enables operation of the ENB bit. When set to 0, the Skip Tape Marks command terminates only on tape mark count exhausted or if it runs into BOT.
6	ENB	Enable Tape Mark Stop Off BOT — This bit is meaningful only if the ESS bit is set. When both bits are set, the tape is at BOT, a Skip Tape Marks command is issued, and the first record seen is a tape mark, the controller halts the operation and sets the LET status bit in XST0. If this bit is clear under the same conditions, the controller merely counts the tape mark and continues.
5-4	—	Not used, always set to 0.
3	RAW	RAW mode — When set, this bit instructs the controller to operate in raw data mode. When clear, the controller will operate in blocked mode (using logical tape records to emulate variable size records).
2	Q11	QIC-11 mode — When set, this bit instructs the controller to initialize the tape drive to operate in QIC-11 mode. The controller does this by issuing a Set Format command (Hex 26) if FMT is set. When reset, the controller initializes the drive to operate in QIC-24 mode. Again, initialization is achieved by issuing a Set Format command (Hex 27) if FMT is set. If FMT is reset, this bit is ignored and no Set Format commands are issued to the drive.
1	FMT	Enable Format — When set, causes format selection to occur using extended QIC-02 Set Format commands.†
0	—	Not used, always set to 0.

† Write Characteristics commands with FMT set should only be issued while the tape is at BOT. If such commands are issued at other times, an illegal command (ILC) termination may occur.

The characteristic data buffer must begin on an even address. If Bit 0 of the second packet word is nonzero, the function is not executed, but is terminated with a Function Reject. In this case, no message packet is stored, but an interrupt is generated if the IE bit is set.

The Write Characteristics command clears the NBA bit in the TSSR register, indicating that a valid message buffer has been specified, if all the following conditions are met:

- The command was not rejected because of nonzero bits in reserved or unused fields within the first three command packet words.
- The fourth packet word (byte count) contains at least a count of six to allow the first three characteristic data words to be fetched.
- The first two data words specify a valid even address (word boundary).
- The third data word contains a value of 14 or greater (specifying the length of the message buffer).

If any of the above conditions are not met, then the NBA bit is set (even if it was already clear from a previous valid Write Characteristics command) and no further message packets are deposited.

Note that if the byte count word in the command packet is less than seven, the characteristic mode data word is not fetched, causing the current values of the characteristic mode bits stored in the controller to be retained.

4.4.5 Write Command

Figure 4-18 illustrates the command packet for a Write. There is one mode of operation, Write Data (mode 0000). A TS11 Write Data Retry (mode 0010) always returns an illegal command status (ILC).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode							Command				
ACK	1	0	SWB	0	0	0	0	IE	0	0	0	0	1	0	1
Low-Order Data Buffer Address															
A15															A0
High-Order Data Buffer Address															
A31															A16
Buffer Extent (byte count) (16-bit unsigned value)															

Figure 4-18. Write Command Packet

The command packet for a Write contains four words: a header word, two words specifying the address of the buffer in memory where the data to be written onto tape is stored, and a buffer extent (byte count) word specifying the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of 0 specifies that 65,536 (64K) bytes are to be written.

If a Write command is executed at or beyond the EOT holes, the data is not written, and a TC6 termination occurs. EOT remains set until passed in the reverse direction. If the subsystem is unable to write the specified number of bytes due to encountering EOT, an uncorrectable error status is returned.

In RAW mode the number of 512-byte blocks written is (specified byte count + 511) + 512 (the specified byte count rounded up to the next multiple of 512)/512. The extraneous bytes are junk. In Blocked mode a 512-byte header record (see Appendix A) is written, plus the specified number of bytes rounded up to the next multiple of 512 bytes. The filler bytes are junk. This group of 512-byte blocks is a single logical record.

CAUTION

The QIC-02 specification allows changing modes from read to write only at BOT or immediately following a tape mark. Consequently, write mode commands (Write or Write Tape Mark) should only be issued at the appropriate time. Issuing these commands at other times causes unpredictable results.

4.4.6 Position Command

Figure 4-19 illustrates the Position command packet. This command causes the tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to BOT. The tape mark/record count is the second word of the command packet. This word is ignored for a Rewind command. The allowable mode field codes and their functions are described in Table 4-16.

Table 4-16. Functions of the Mode Field Codes (Position Command)

Mode	Function
0000	Space Records Forward
0001	Space Records Reverse
0010	Skip Tape Marks Forward
0011	Skip Tape Marks Reverse
0100	Rewind (Record Count Ignored)

1514	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Ctl	Device Dependent			Mode							Command				
ACK	1	0	0	m	m	m	m	IE	0	0	0	1	0	0	0
Tape Mark/Record Count (16-bit unsigned value)															

Figure 4-19. Position Command Packet

The Space Records operation skips over the number of records (logical records in blocked mode, physical 512-byte records in RAW mode) specified in the record count word of the command packet. However, the operation automatically terminates, with a TSA termination code, when a tape mark is traversed. (The tape mark is included in the record count.) Also, the RLS status bit in XST0 is set if the record count is not decremented to zero and the residual field reflects the number of records not skipped.

A Skip Tape Marks command skips over the number of tape marks specified in the tape mark count word of the command packet. However, the operation automatically terminates if a double tape mark (two contiguous tape marks) is encountered and the ESS bit was set in the previous Write Characteristics command. Termination also occurs if a tape mark is the first record off of BOT and the ESS and ENB bits were both set in the previous Write Characteristics command. RLS is set if the tape mark count is not decremented to zero and the residual field reflects the number of tape marks not skipped.

A Space Records Reverse or Skip Tape Marks Reverse, which runs into BOT, sets the Reverse into BOT (RIB) status bit and causes a TSA termination. If one of these reverse commands is issued while the tape is already positioned at BOT, the NEF error bit is set and Function Reject termination returned; in this case, the tape does not move.

The Space Records Reverse and Skip Tape Marks Reverse commands both cause a tape rewind operation. Following the rewind operation, the Space Records Reverse command spaces forward by first skipping the required number of tape marks, then reading the required number of records forward.

NOTE

Since the QIC-02 specification does not allow a tape write operation to occur after a tape read operation (other than immediately following a file mark), the Space Records Reverse command cannot be followed by a write operation unless it positions the tape immediately following a tape mark.

After the required rewind operation, the Skip Tape Mark Reverse command moves the tape forward the appropriate number of tape marks. Since the Skip Tape Marks Reverse command always positions the tape just before a tape mark (logically), the command can never be followed immediately by a tape write operation.

When a Rewind command is issued, the interrupt (if enabled) does not occur until the tape reaches BOT and has stopped.

4.4.7 Format Command

Figure 4-20 illustrates the Format command packet. Note that the second word is present, but it is not used in the command. This command writes a tape mark. Write Tape Mark (mode 0000) is the only allowable mode field code. A TS11 Write Tape Mark Retry (mode 0010) causes an Illegal Command Status (ILC).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode						Command					
ACK	1	0	0	0	m	m	m	IE	0	0	0	1	0	0	1

Figure 4-20. Format Command Packet

In all cases, executing a Format command at or beyond EOT causes an uncorrectable error (TC6) termination. The EOT bit remains set until the EOT marker is passed in the reverse direction.

4.4.8 Initialize Command

Figure 4-21 illustrates the Initialize command packet. This command performs the same as a write into the TXCPR register with Data Bit 15 set to 1. It resets the entire tape subsystem just like a system reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ctl	Device Dependent			Mode							Command				
ACK	1	0	0	0	0	0	0	IE	0	0	0	1	0	1	1

Figure 4-21. Initialize Command Packet

SECTION 5: RTC SOFTWARE INTERFACE

The Clock register which is used for RTC programming is located at VMEbus base address + 4 (VMEbase + 4). The structure of this one-word register is shown in Figure 5-1. The bit definitions are provided in Table 5-1. The clock functions supported are

- Read clock register from buffer
- Write clock register to buffer
- Update clock buffer from clock hardware
- Update clock hardware from clock buffer

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MC	CLK	HW	RW	CREG				Value							

Figure 5-1. Clock Register Format

For clock operations both MC and CLK are set. Programming is accomplished by commands to read and write elements of a clock buffer along with commands to update the buffer and clock hardware. The clock hardware is implemented with an MM58274 clock chip and the software interface buffer is an array of bytes that can be selected by the index code given in CREG (see Table 5-1).

Table 5-1. Clock Register Bit Definitions

Bit	Name	Function
15	MC	Mode Control is always set to 1 for clock operations. It is cleared on command completion.
14	CLK	Clock Select is always set to 1 for clock operations.
13	HW	The Hardware bit affects clock hardware. HW must be cleared to read from or write to the clock buffer. HW must be set to program the hardware clock or to update the clock buffer with the current time.
12	R/W	Read/Write is set to 1 for a write operation and cleared to 0 for a read.

(continued on next page)

Table 5-1. Clock Register Bit Definitions (*continued*)

Bit	Name	Function
11-8	CREG	Clock Registers and their corresponding index codes are as follows:
		0000 Ten thousandths of seconds (2 BCD digits)
		0001 Hundredths and tenths of seconds (2 BCD digits)
		0010 Seconds (2 BCD digits)
		0011 Minutes (2 BCD digits)
		0100 Hours (2 BCD digits)
		0101 Day of week (1 BCD digits)
		0110 Day of month (2 BCD digits)
		0111 Month (2 BCD digits)
		1000 Year (2 BCD digits)
		1001 Leap year (lower nibble matches the MM58274 leap year register format)

In order to read the clock buffer the HW and RW bits must be clear. The index of the quantity desired should be written to the CREG field of the Clock register. For example, if you want to read *hours*, you should write a value of four to the CREG. When the MC bit is clear, indicating the completion of the operation, the value in the lower byte of the Clock register is the value at the given index of the clock buffer.

NOTES

- Ten thousandths and hundredths of seconds always read as 0.
- While polling the Clock Register waiting for MC to be cleared, the register should only be polled approximately once every 500 microseconds.

In order to write the clock buffer, the HW bit must be clear and the RW bit set. The index and value of the time unit which is to be modified should be in the CREG and the lower byte of the Clock register. For example, in order to write 41 minutes, the CREG should be 0011 (minutes byte) and the value should be 01000001 (41).

To program the hardware clock or update the clock buffer with the current time, the HW bit should be set. With HW set, RW set to 1 programs the clock hardware with the values in the clock buffer; RW as 0 updates the clock buffer from the hardware.

The lower nibble of Byte 9 (leap year) matches the MM58274 leap year register format (see Table 5-1). The leap year counter (Bits 2 and 3) should be loaded with the number of years since the last leap year. For example, if 1980 were the last leap year, a clock programmed in 1982 should have a value of two stored in the leap year counter.

Bit 1 of Byte 9 sets the time as AM or PM when 12-hour mode is used. Bit 1 should be 0 if 24-hour mode is used.

Table 5-2. Leap Year Byte Format

Function	Byte 9 (lower nibble) Bit 3	Bit 2	Bit 1	Bit 0	Comments
Leap year counter	X	X			A value of 0 = a leap year
AM/PM (12-hour mode)			X		0=AM 1=PM
12/24-hour select bit				X	0=12-hour mode 1=24-hour mode

APPENDIX A: VARIABLE RECORD FORMAT

The tape controller reads and writes 512-byte blocks (as defined in the QIC-02 specification), but also provides support for variable size records. To support variable length records, the VME-QIC2/X writes an internally generated header block at the beginning of each variable length record. This header block is shown in Figure A-1. Word 0 of the header block always contains A1FE. Word 1 contains the file number (beginning with 0001). Word 2 contains the record number within the file (beginning with 0000). Word 3 provides the length of a logical record in bytes. Word 4 is the block count (number of data blocks). The remainder of the 512 bytes in the header block are garbage.

Word 0	Word 1	Word 2	Word 3	Word 4	Remaining Bytes
A1FE	File number	Record number within file	Logical record count	Block Count	XXXX

Figure A-1. Variable Length Record Header Block Format

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Please comment on how this manual can be improved: _____

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