

**ADM 3A/3A+ Dumb Terminal®
Video Display Unit
Maintenance Manual**

**LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION
901 EAST BALL ROAD, ANAHEIM, CALIFORNIA 92805**

**ADM 3A/3A+
Dumb Terminal®**



LEAR SIEGLER, INC.

**MAINTENANCE
MANUAL**

TABLE OF CONTENTS

SECTION	PAGE
I GENERAL DESCRIPTION	1-1
1.1 INTRODUCTION	1-1
1.2 PURPOSE AND USE	1-1
1.3 OPERATIONAL DESCRIPTION	1-1
1.3.1 Keyboard	1-1
1.3.2 Input/Output (I/O) Port	1-2
1.3.3 ADM 3A Control Logic	1-2
1.3.4 Display Memory	1-3
1.3.5 CRT Display Monitor	1-3
1.4 PHYSICAL DESCRIPTION	1-3
1.5 SPECIFICATIONS	1-3
1.5.1 Send/Receive Modes	1-3
1.5.2 Character Format	1-3
1.5.3 Word Structure	1-3
1.5.4 Data Entry and Overflow	1-8
1.5.5 Configuration Control	1-8
1.6 OPTIONAL FEATURES	1-8
1.6.1 Lower Case Characters	1-8
1.6.2 Answerback	1-8
1.6.3 Numeric Keypad	1-8
1.6.4 20mA Current Loop on Extension Port	1-8
1.6.5 Split Baud Rate	1-8
1.6.6 Beep Defeat	1-8
1.6.7 230 VAC	1-8
1.6.8 Alternate Configuration - Green Phosphor Screen	1-8
1.7 RELATED DOCUMENTS	1-8
II INSTALLATION	2-1
2.1 GENERAL	2-1

TABLE OF CONTENTS (cont'd)

SECTION	PAGE
2.2	SPECIAL SAFETY REQUIREMENTS 2-1
2.3	UNPACKING AND INITIAL INSPECTION 2-1
2.4	SITE REQUIREMENTS..... 2-1
2.5	INITIAL PREPARATION 2-2
2.5.1	Line Voltage Selection2-2
2.5.2	Configuration Control Switch Settings2-2
2.6	INTERFACE INFORMATION 2-2
2.6.1	RS-232C Modem Port Interface2-4
2.6.2	RS-232C Extension Port Interface2-4
2.7	INSTALLING THE ADM 3A 2-4
2.8	POWER TURN-ON AND TURN-OFF..... 2-12
2.9	CARE OF THE ADM 3A 2-14
2.9.1	Cleaning 2-14
2.9.2	Inspection 2-14
III	OPERATION..... 3-1
3.1	GENERAL 3-1
3.2	KEYBOARD OPERATIONS..... 3-1
3.3	INTERFACE CONTROL OPERATIONS 3-1
3.3.1	Data Communication Ports3-1
3.3.2	Request To Send Operation3-1
3.3.3	Secondary Channel Turnaround Operation3-4
3.3.4	Code Turnaround Operation3-4
3.4	PROGRAMMING CONSIDERATIONS 3-4
3.4.1	Remote CTRL Operation3-4
3.4.2	Remote Load-Cursor Operation3-4
3.5	GATED EXTENSION PORT OPERATION..... 3-5
IV	THEORY OF OPERATION 4-1
4.1	GENERAL 4-1
4.2	GENERAL FUNCTIONAL DESCRIPTION 4-1
4.2.1	Display Generation4-1
4.2.2	Display Refresh Operation4-1

TABLE OF CONTENTS (cont'd)

SECTION	PAGE
4.2.3	Monitor Video and Drive Circuits 4-3
4.2.4	Receiving and Storing Data 4-3
4.2.5	Cursor Generation 4-4
4.2.6	Keyboard Logic 4-4
4.2.7	Data Transmitter Logic 4-4
4.2.8	Interface Control Logic 4-4
4.2.9	CRT Display Monitor 4-4
4.3	LOGIC DESCRIPTION 4-4
4.3.1	General Clear Circuit 4-4
4.3.2	Display Counters 4-5
4.3.3	Row Counter and Offset Counter Logic 4-7
4.3.4	Column Counter Logic 4-8
4.3.5	Cursor Presentation Logic 4-10
4.3.6	Memory Address Logic 4-10
4.3.7	Refresh Memory and Character ROM Logic 4-15
4.3.8	Erase Logic 4-15
4.3.9	WRITE PULSE Logic 4-15
4.3.10	Keyboard Logic 4-17
4.3.11	Beeper Logic 4-19
4.3.12	Data Receive and Command Decoder Logic 4-19
4.3.13	Data Transmitter Logic 4-20
4.3.14	Video Blanking and Serializer Logic 4-22
4.3.15	Monitor Drive Logic 4-23
4.3.16	Baud Rate Select Logic 4-23
4.3.17	Interface Control Logic 4-24
	4.3.17.1 Code-Turnaround Control 4-24
	4.3.17.2 Reverse-Channel Control 4-24
4.3.18	Power Supplies 4-24
4.3.19	CRT Display Monitor Logic 4-25
4.3.20	ADM-3A Answer Back 4-29
4.3.21	ADM-3A Extension Port Current Loop 4-29
4.3.22	ADM-3A Numeric Pad 4-29
V	MAINTENANCE 5-1
5.1	GENERAL 5-1
5.2	INSTALLATION 5-1
5.3	ROUTINE MAINTENANCE 5-1
5.4	OPENING ADM-3A COVER 5-1
5.5	ADJUSTMENTS 5-1
5.5.1	Contrast Adjustment 5-1
5.5.2	Brightness Adjustment 5-3
5.5.3	Vertical Adjustment 5-3
5.5.4	Horizontal Adjustments 5-3

TABLE OF CONTENTS (cont'd)

SECTION	PAGE
5.5.5	Focus Adjustment 5-3
5.5.6	Centering 5-3
5.6	CORRECTIVE MAINTENANCE 5-4
5.6.1	Failure Analysis 5-4
5.6.2	Troubleshooting The Monitor 5-4
5.6.3	Removing and Replacing Monitor CRT and Subassemblies 5-5
5.6.4	Troubleshooting The Main Circuit board 5-5
5.6.5	Removing and Replacing The Main Circuit Board 5-5
5.6.6	Removing and Replacing Key Switch Contacts 5-10
VI	DRAWINGS 6-1
6.1	SCHEMATIC SHEET #2 - SYSTEM COUNTERS 6-1
6.2	SCHEMATIC SHEET #12 - INTERFACE CONTROL 6-2
6.3	SCHEMATIC SHEET #3 - CLEAR/ERASE LOGIC, OFFSET COUNTER, ROW COUNTER, BEEPER CIRCUIT 6-2
6.3.1	Clear/Erase Logic 6-2
6.3.2	Offset Counter 6-4
6.3.3	Row Counter 6-5
6.3.4	Beeper Circuit 6-5
6.4	SCHEMATIC SHEET #4 - COLUMN COUNTER, WRITE-PULSE LOGIC 6-6
6.4.1	Column Counter 6-6
6.4.2	Write-Pulse Logic 6-7
6.5	SCHEMATIC SHEET #5 - MEMORY ADDRESS GENERATION 6-7
6.6	SCHEMATIC SHEET #6 - DATA RECEIVER, CHARACTER DECODERS, LOAD-CURSOR SEQUENCE DETECTOR 6-9
6.6.1	Data Receiver 6-9
6.6.2	Character Decoders 6-9
6.6.3	Load-Cursor Sequence Detector 6-9
6.7	SCHEMATIC SHEET #7 - CLEAR CIRCUIT, READ BACK, MONITOR DRIVE SIGNALS, CURSOR GENERATION 6-10
6.7.1	Clear Circuit 6-10
6.7.2	Read Back 6-10
6.7.3	Monitor Drive Signals 6-10
6.7.4	Cursor Generation 6-12

TABLE OF CONTENTS (cont'd)

SECTION		PAGE
6.8	SCHEMATIC SHEET #8 - REFRESH MEMORY, CHARACTER GENERATORS, VIDEO SERIALIZER, TRANSMIT DATA MULTIPLEXERS	6-12
6.8.1	Refresh Memory	6-12
6.8.2	Character Generators	6-12
6.8.3	Video Serializer	6-13
6.8.4	Transmit Data Multiplexers	6-13
6.9	SCHEMATIC SHEET #9 - KEYBOARD CIRCUIT	6-13
6.10	SCHEMATIC SHEET #10 - DATA TRANSMITTER, CONTROL SECTION OF UART, CURRENT LOOP XMTR/RCVR, KEYBOARD LOCK CIRCUIT	6-15
6.10.1	Data Transmitter	6-15
6.10.2	Control Section of Uart	6-16
6.10.3	Current Loop XMTR/RCVR.....	6-16
6.10.4	Keyboard Logic	6-16
6.11	SCHEMATIC SHEET #11 - BAUD RATE GENERATION	6-17/18
VII	PARTS LIST	7-1
7.1	ADM 3A Replacement Parts Information	7-1
7.2	Monitor Replacement Parts Information	7-1
7.2.2	Returning Parts	7-1

TABLE OF CONTENTS (cont'd)

LIST OF FIGURES

FIGURE		PAGE
1-1	ADM 3A Video Display Terminal	viii
1-2	ADM 3A Data Flow Block Diagram	1-2
1-3	ADM 3A Graphic Character Set and CTRL Codes	1-6
1-4	Word Format Codes with Switch Configurations.....	1-7
2-1	ADM 3A Connector and Configuration Switch Locations	2-3
2-2	Typical ADM 3A Application	2-9
2-3	Modem and RS-232C Extension Interface Logic	2-10
2-4	Current Loop Interface Logic.....	2-11
2-5	ADM 3A Rear Panel Controls	2-12
2-6	ADM 3A+ Assy; From Engineering Drawing No. 131551	2-13
3-1	ADM 3A Standard Keyboard Operational Characteristics	3-3
4-1	ADM 3A Functional Block Diagram.....	4-2
4-2	CRT Display Monitor	4-3
4-3	Display Counters, Block Diagram	4-5
4-4	Display Counter Timing	4-6
4-5	Row Counter & Offset Counter Logic, Block Diagram.....	4-7
4-6	Clear Screen Timing	4-9
4-7	Logic Block Diagram	4-11
4-8	Memory Address Logic, Block Diagram	4-12
4-9	Organization of Display Data in Refresh Memory	4-14
4-10	Refresh Memory and Character ROM Logic, Block Diagram	4-16
4-11	Keyboard Logic Timing	4-18
4-12	Data Receiver Logic and Command Decoders.....	4-19
4-13	Data Transmitter Logic, Block Diagram.....	4-21
4-14	Video Blanking and Serializer Logic, Block Diagram	4-22
4-15	Baud Rate Select Logic, Block Diagram	4-23
4-16	Interface Timing for Code Turnaround	4-25
4-17	Interface Timing for Reverse-Channel Operation	4-26
4-18	ADM-3A Numeric Key Pad.....	4-30
5-1	Interface Connector Terminal Assignments	5-2
5-2	Inputs to Monitor, Timing Diagram	5-6
5-3	Monitor Voltage Waveforms	5-7
5-4	Monitor Video Board, Component Layout	5-8
5-5	Key Contact Removal/Replacement Illustration	5-11
5-6	Key Contact Removal/Replacement Illustration	5-11
5-7	Key Contact Removal/Replacement Illustration	5-12

TABLE OF CONTENTS (cont'd)

FIGURE		PAGE
5-8	Key Contact Removal/Replacement Illustration	5-12
5-9	Key Contact Removal/Replacement Illustration	5-13/14
5-10	Key Contact Removal/Replacement Illustration	5-13/14
6-1	Interface Timing for Reverse-Channel Operation	6-3
6-2	Interface Timing for Code Turnaround	6-4
6-3	Read Mode	6-11

LIST OF TABLES

TABLE		PAGE
1-1	ADM 3A Specifications	1-4
2-1	Baud Rate Switch Functions	2-4
2-2	Configuration Control Switch Functions	2-5
5-1	Main Circuit Board Connector Terminals.....	5-9

APPENDICES

APPENDIX		PAGE
A	PRODUCT CONFIGURATION	A1
	TIMING	A2
	MONITOR	A3
	P.C. BOARD ASSEMBLY	A4
B	SCHEMATICS	B1
C	OPTIONS	C1
	WIRING DIAGRAMS.....	C9
D	ZENITH SERVICE MANUAL	D1
E	ASCII CONTROL CODE CHART.....	E1
	OPERATORS QUICK REFERENCE CHART OF CONTROL AND OPERATORS CODES	E2
	OPERATORS QUICK REFERENCE CHART OF ABSOLUTE CURSOR POSITIONS	E3

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

PREFACE

This Maintenance Manual describes the function and operation of this ADM 3A Video Display Terminal. The instructions and information are presented to aid operational personnel in the installation, operation, and care of the ADM 3A. All operator controls are described in detail, and remote programming considerations are presented in sufficient detail to enable an experienced operator to use the equipment efficiently when confronted with nonstandard applications.

The major topics described in the manual include:

<i>Section I</i>	<i>General Description</i>
<i>Section II</i>	<i>Installation</i>
<i>Section III</i>	<i>Operation</i>
<i>Section IV</i>	<i>Theory of Operation</i>
<i>Section V</i>	<i>Maintenance</i>
<i>Section VI</i>	<i>Drawings</i>
<i>Section VII</i>	<i>Parts List</i>
<i>Appendix A</i>	<i>Timing Monitor Power Supply P.C. Board Assembly</i>
<i>Appendix B</i>	<i>Schematics</i>
<i>Appendix C</i>	<i>Options Wiring Diagrams</i>
<i>Appendix D</i>	<i>Zenith Service Manual</i>
<i>Appendix E</i>	<i>Operators Quick Reference Charts</i>
	<i>Index</i>

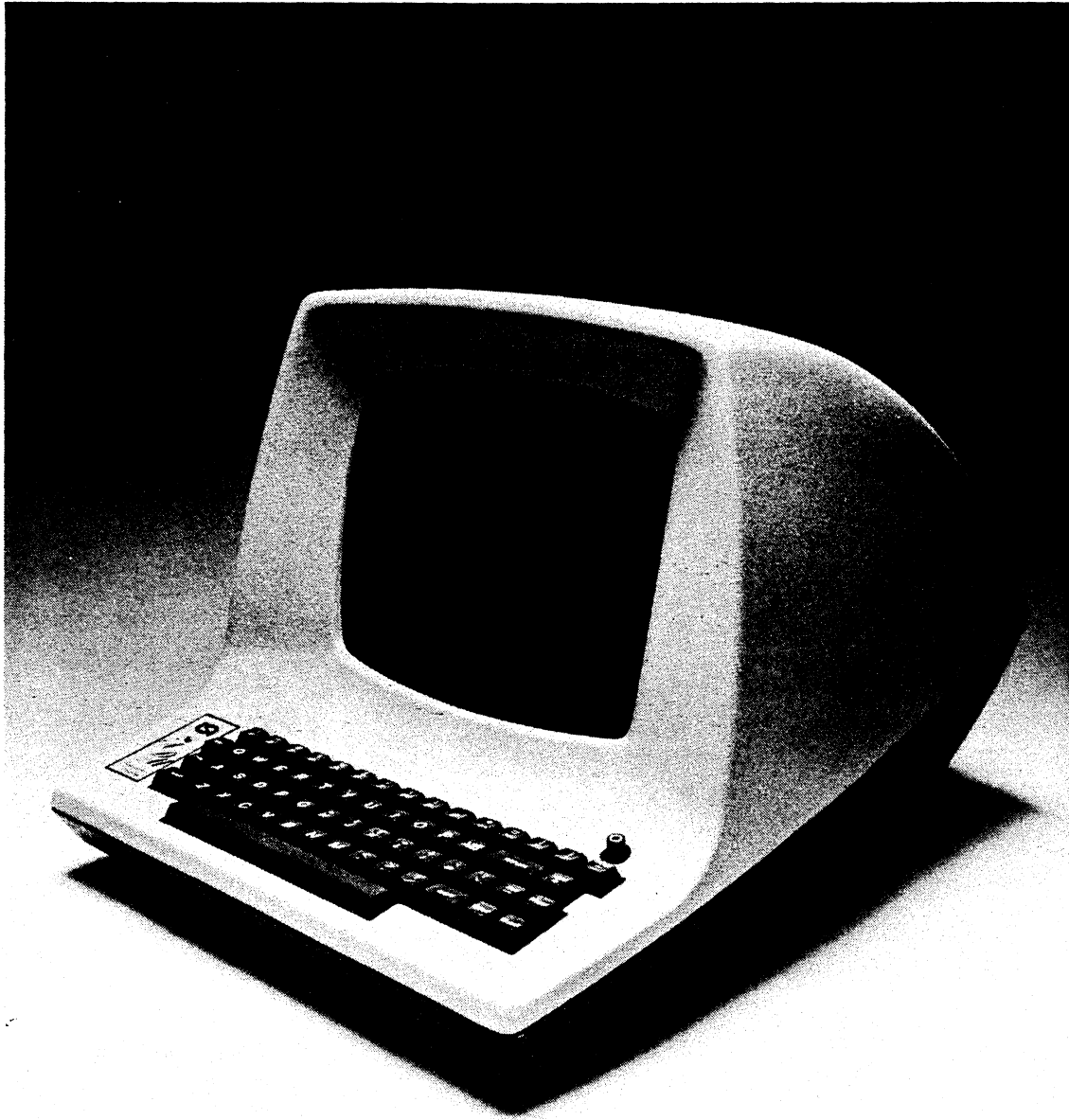


Figure 1-1. ADM 3A Video Display Terminal

SECTION I GENERAL DESCRIPTION

1.1 INTRODUCTION

This section of the manual describes the primary function of the Lear Siegler ADM 3A Video Display Terminal shown in figure 1-1. Other information in this section includes specifications, operating features and ranges, physical dimensions, and a list of available options.

1.2 PURPOSE AND USE

There are numerous applications of the ADM 3A, all involving the transfer of asynchronous data. In some applications, data transfer may be exclusively unidirectional; either from the ADM 3A to a host computer, or from the computer to the ADM 3A. However, a more frequent application of the ADM 3A, is one in which an operator communicates with the computer, and the computer reacts in accordance with its stored program.

The ADM 3A features the following general capabilities:

- Full 128 ASCII character set with 80 x 24 character nonglare display (12-line display is switch selectable)
- 11 communication rates in full-duplex and half-duplex send/receive modes
- Scrolling
- Absolute cursor positioning
- Variable 9-, 10-, or 11-bit word structure

- Selectable Auto New Line operation
- Selectable standard RS-232C or 20mA current-loop interface, with RS-232C extension interface for auxiliary devices. (Selectable keyboard lock or gated EXTENSION port). Optional current-loop interface on EXTENSION port.
- Special control character sequences.
- Selectable refresh rate

1.3 OPERATIONAL DESCRIPTION

The ADM 3A is an interactive device which is used to enter, display, and send information to a host computer, and to receive and display information from the computer. Using a keyboard similar to that of a teletypewriter, the operator may enter information which is immediately transmitted to the computer, and may be simultaneously displayed on a cathode ray tube (CRT). Data from the computer is received and displayed at baud rates as high as 19200 (the maximum baud rate when using the current loop option is 9600).

1.3.1 Keyboard

The keyboard contains 59 keys from which data entry and control functions are initiated. Each keystroke is encoded into a corresponding ASCII character which is immediately transmitted to the host computer. The character is also routed back to the CRT display: directly in half-duplex operation, or echoed from the host computer via the I/O interface in full-duplex operation.

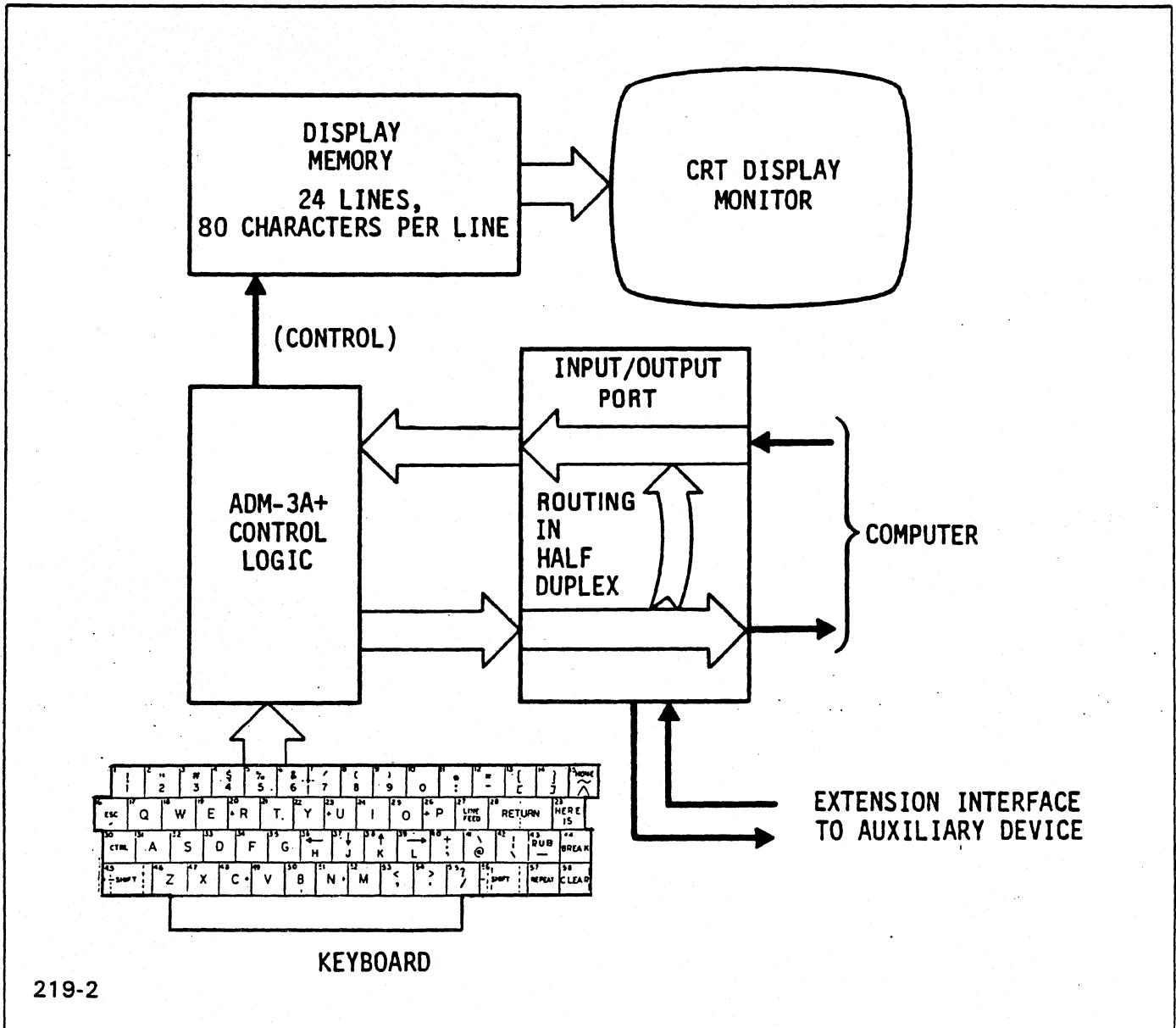


Figure 1-2. ADM 3A Data Flow Block Diagram

1.3.2 Input/Output (I/O) Port

The MODEM (I/O) port is the link, or interface, that handles the flow of data in both directions between the ADM 3A and the computer. It may be configured for either RS-232C or 20mA Current Loop operation.

1.3.3 ADM 3A Control Logic

The ADM 3A Control Logic interprets the control codes that originate either at the keyboard or host computer, and directs the activities of the ADM 3A accordingly. These activities include data handling, and formatting.

1.3.4 Display Memory

The display memory contains a random access memory (RAM), video logic and character generation circuits appropriate for controlling the CRT display. The memory is capable of holding 1920 characters, which are stored in sequentially scanned locations. The scanned data is then sent to the CRT for displaying. Input to the display memory consists of the data character codes from the I/O port or keyboard, under the control of signals from the control logic circuits.

1.3.5 CRT Display Monitor

The CRT display monitor is a rectangular screen measuring 12 inches diagonally. Data characters are displayed on 24 or 12 equally-spaced rows, each consisting of 80 (maximum) characters. The 80 character lines are displayed clearly at a refresh rate of either 50 or 60 Hz, corresponding to the AC line frequency.

1.4 PHYSICAL DESCRIPTION

The ADM 3A is a self-contained unit consisting of three major assemblies: (1) base and cover assembly, (2) main logic board and (3) the CRT monitor. The power transformer, a beeper, and intercomponent cabling are located on the base portion of the terminal. Supports and guide pins are also located on the base, and these are used for installing the main logic board.

The cover portion of the terminal contains the CRT monitor and its associated subassemblies. The cover is hinged to the base at the rear, and when swung open, all components of the ADM 3A are exposed.

The main logic board contains all other operating elements of the ADM 3A that are not contained in the CRT monitor and the base assembly. This includes the keyboard. The keyboard is made up of integrated key rows, or modules. It is built directly on the main logic board. The logic board rests on supports within the base, and is held in place by guide pins. Two connectors at the rear edge of the logic board provide the RS-232C/current loop interface and the RS-232C extension interface.

The CRT monitor consists of three subassemblies: (1) the CRT itself, (2) a printed circuit board that

contains most of the video circuitry, and (3) the flyback assembly. The monitor display screen measures 12 inches diagonally.

1.5 SPECIFICATIONS

The ADM 3A specifications are listed in table 1-1. In addition, several operational features, such as send/receive modes, character format, word structure, data entry and overflow, and configuration control are discussed in the paragraphs that follow. Specific operational information regarding configuration control, format and word structure, modes, etc., is contained in Section II of this manual.

1.5.1 Send/Receive Modes

Two-switch-selectable send/receive modes are available in the ADM 3A: half-duplex and full-duplex. In the half-duplex mode, each character is transmitted to the computer as it is entered on the keyboard and is simultaneously displayed on the CRT monitor.

In full-duplex operation, the ADM 3A can transmit and receive information in both directions simultaneously. Characters are transmitted as they are entered at the keyboard, but are displayed only upon reception. In order to display transmitted characters, they must be echoed back from the host computer or data set.

1.5.2 Character Format (Figure 1-3)

The standard ADM 3A character set contains 64 ASCII characters. Control characters are not displayed when they are generated. The displayable 64 ASCII characters consists of upper case letters, numerics and punctuation. When a nondisplayable lower case character is typed (lower case option not installed), a lower case code is transmitted, but the character displayed is upper case. The lower case option permits the display of 95 ASCII characters consisting of upper and lower case letters, numerics and punctuation.

1.5.3 Word Structure

The ADM 3A can transmit and receive data characters in any one of the asynchronous character formats shown in figure 1-4. These word format codes are selected by means of DIP switches located on the PC board.

Table 1-1. ADM 3A Specifications

DISPLAY FORMAT

24 lines x 80 characters
(12 x 80 switch selectable)

CRT SCREEN

12-inch (30.5 cm) diagonal, P4 Phosphor
with nonglare surface

REFRESH RATE

50 Hz or 60 Hz, depending on line
frequency (switch selectable)

HORIZONTAL SWEEP RATE

16.2 kHz

DISPLAY AREA

5.8 inches (14.7 cm) high x 8.3 inches
(21 cm) wide

CHARACTER SET, GENERATED

128 ASCII characters (with 32 control
characters)

CHARACTER SET, DISPLAYED

STANDARD: 64 ASCII Characters
OPTIONAL: 95 ASCII Characters

CHARACTER MATRIX

5 x 7 dot matrix 0.074 inch (1.88 mm)
wide x 0.188 inch (4.77 mm) high

CHARACTER FIELD

7 x 9 dot matrix 0.103 inch (2.62 mm)
wide x 0.241 inch (6.14 mm) high

CURSOR

CUR CTRL ON: 7 x 9 dot matrix. Reverse
image rectangle cursor.
Homes to upper left of
screen.

CUR CTL OFF: Double underline, 5 dots
wide. Homes to first
position of bottom line.

CURSOR CONTROLS

Two-key cursor controls; Backspace
CTRL H, Forespace **CTRL L**, Up
CTRL K, Down **CTRL J**, Home
CTRL HOME

KEYBOARD

59 keys, 26-letter alphabet with upper case,
numerics 0 through 9, punctuation, and
control. Two-key repeat operation at a rate
of 22 characters per second.

FUNCTIONAL CONTROL KEYS

Escape, Rubout (delete), Break, Return, Shift
Clear, Repeat, Line Feed, Control, Here Is.

TRANSMISSION MODES

Full Duplex, Half Duplex

COMPUTER INTERFACES (MODEM)

RS-232C point-to-point or 20mA current
loop.

DATA RATES

75, 110, 150, 300, 600, 1200, 1800, 2400,
4800, 9600, 19,200 (Current Loop to 9600)

PARITY

Even, odd, mark, space, or none

WORD STRUCTURE

Total Word Length: 9, 10, or 11 bits

Data: 7 or 8 bits (8th bit
0 or 1)

Start: 1 bit

Stop: 1 or 2 bits

EXTENSION INTERFACE

RS-232C EXTENSION Port for interfacing serial
asynchronous ASCII hard copy printer,
magnetic tape recorder, or other serial
asynchronous devices using selectable keyboard
lock or gated EXTENSION Port. (Selectable
keyboard lock or gated EXTENSION Port).

Table 1-1. ADM 3A Specifications (cont'd)

SWITCH SELECTABLE SETTINGS

All Available Baud Rates
Half/Full Duplex
RS-232C/Current Loop (MODEM)
Auto New Line ON/OFF
Upper Case/Lower Case (when lower case option installed)
Odd/Even Parity
7 or 8 Data Bits
1 or 2 Stop Bits
Parity/Inhibit
Bit 8 = 0 or 1
Keyboard Lock/Gated EXTENSION Port
Disable Keyboard Lock
Disable Clear Screen
Secondary Channel
Cursor Control
Local
103 Modem
202 Modem
Code (ETX or EOT)

OPERATING ENVIRONMENT

Temperature: 41°F to 122°F (5°C to 50°C)
Humidity: 5% to 95%, noncondensing
Altitude: 10,000 feet (3.048 km) maximum

POWER REQUIREMENTS

Standard: 115 VAC ± 10%, 60 ±3 Hz
60 Watts nominal
Optional: 230 VAC ± 10%, 50/60 ±3 Hz
60 Watts nominal
Heat Dissipation: 205 BTU per hour

DIMENSIONS AND WEIGHT

Width: 15.6 inches (39.6 cm)
Depth: 20.2 inches (51.3 cm)
Height: 13.5 inches (34.3 cm)
Weight: 32 pounds (14.5 kg)

OPTIONS

Lower Case (95 ASCII character set)
Answerback Memory
Numeric Keypad (detached)
20mA Current Loop on EXTENSION Port
Split Baud Rate
Beep Defeat
Output Cable
Green Phosphor Screen

HEX		CONTROL		GRAPHIC CHARACTER SET					
		0	1	2	3	4	5	6	7
BITS 4 3 2 1 ↓	BITS 7 6 5 →	0 ₀ 0	0 ₀ 1	0 ₁ 0	0 ₁ 1	1 ₀ 0	1 ₀ 1	1 ₁ 0	1 ₁ 1
0	0000	NUL	DLE	SP	0	@	P	`	p
1	0001	SOH	DC1	!	1	A	Q	a	q
2	0010	STX	DC2	"	2	B	R	b	r
3	0011	ETX	DC3	#	3	C	S	c	s
4	0100	EOT	DC4	\$	4	D	T	d	t
5	0101	ENQ	NAK	%	5	E	U	e	u
6	0110	ACK	SYN	&	6	F	V	f	v
7	0111	BEEP	ETB	'	7	G	W	g	w
8	1000	BS (←)	CAN	(8	H	X	h	x
9	1001	HT (TAB)	EM)	9	I	Y	i	y
A	1010	LF (↓)	SUB	*	:	J	Z	j	z
B	1011	VT (↑)	ESC	+	;	K	[k	{
C	1100	FF (→)	FS	,	<	L	\	l	!
D	1101	CR	GS	-	=	M]	m	}
E	1110	SO	RS (HOME)	.	>	N	^	n	~
F	1111	SI	US	/	?	O	-	o	*DEL (RUB)

CONTROL
CODES

DISPLAYABLE IN
STANDARD ADM 3A

DISPLAYABLE WITH
ADM 3A UPPER/LOWER
CASE DISPLAY OPTION

(GENERATED BY HOLDING
CTRL KEY WHILE TYPING
THE CORRESPONDING KEY
SHOWN IN COLUMNS 4
AND 5.)

219-3

Figure 1-3. ADM 3A Graphic Character Set and CTRL Codes

219-4

WORD FORMAT	FRONT PANEL SWITCHES					9-, 10-, OR 11-BIT WORD STRUCTURE												
	PAR	DATA	STOP	PARITY	BIT 8	BITS												
	POSITIONS					0	1	2	3	4	5	6	7	8	9	10		
Eleven-Bit Word with EVEN Parity and 2 STOP Bits	SW2	SW3	SW4	SW5	SW6	START										EVN PAR	STOP	STOP
	EVEN	7	2	PARITY	X													
Eleven-Bit Word with ODD Parity and 2 STOP Bits	SW2	SW3	SW4	SW5	SW6	START										ODD PAR	STOP	STOP
	ODD	7	2	PARITY	X													
Ten-Bit Word with EVEN Parity and 1 STOP Bit	SW2	SW3	SW4	SW5	SW6	START										EVN PAR	STOP	X
	EVEN	7	1	PARITY	X													
Ten-Bit Word with ODD Parity and 1 STOP Bit	SW2	SW3	SW4	SW5	SW6	START										ODD PAR	STOP	X
	ODD	7	1	PARITY	X													
Eleven-Bit Word with No Parity and 2 STOP Bits	SW2	SW3	SW4	SW5	SW6	START										1 OR 0	STOP	STOP
	X	8	2	INH	0 OR 1													
Ten-Bit Word with No Parity and 1 STOP Bit	SW2	SW3	SW4	SW5	SW6	START										1 OR 0	STOP	X
	X	8	1	INH	0 OR 1													
Eleven-Bit Word with EVEN Parity and 1 STOP Bit	SW2	SW3	SW4	SW5	SW6	START										1 OR 0	EVN PAR	STOP
	EVEN	8	1	PARITY	0 OR 1													
Eleven-Bit Word with ODD Parity and 1 STOP Bit	SW2	SW3	SW4	SW5	SW6	START										1 OR 0	ODD PAR	STOP
	ODD	8	1	PARITY	0 OR 1													
Nine-Bit Word with no Parity and 1 STOP Bit	SW2	SW3	SW4	SW5	SW6	START										STOP	X	X
	X	7	1	INH	0 OR 1													

Figure 1-4. Word Format Codes with Switch Configurations

1.5.4 Data Entry and Overflow

New data enters on progressive lines, from top to bottom. When the cursor is on the bottom line, line feed causes upward scrolling of the entire display page. When overflow occurs, the entire display page is scrolled upward one line as new data enters at the beginning of the new bottom line. If **AUTO NEW LINE** is not enabled, a CR/LF must be sent.

1.5.5 Configuration Control

Default conditions for the ADM 3A are established by the selected positions of 33 DIP switches, which are located on the main logic board. The switches are factory set in accordance with instructions established at the time of purchase of the ADM 3A. Section II of this manual shows the locations of these switches so that they may be checked and/or reset at the time of ADM 3A installation.

1.6 OPTIONAL FEATURES

The following features can be incorporated into the ADM 3A by installation of the appropriate option.

1.6.1 Lower Case Characters

This option provides the capability of displaying lower case characters.

1.6.2 Answerback

When installed, this option is activated by means of the **HERE IS** key. Momentarily pressing this key initiates an identification message (stored in a special ADM 3A memory) that identifies the terminal. The **HERE IS** key is included in the keyboard of the ADM 3A, but has no function if the Answerback option is not installed. Answerback is activated by a remote ENQ code.

1.6.3 Numeric Keypad

This option provides 14 keys for operators convenience. These keys consist of 10 numeric (0-9), 3 punctuation (- . ,) and **ENTER** (equivalent to **RETURN**) key.

1.6.4 20mA Current Loop on Extension Port

This option permits the **EXTENSION** port to be used in a current loop application.

1.6.5 Split Baud Rate

This option adds a 12-position rotary switch, adjacent to the **BAUD RATE** switches, that allows the ADM 3A to transmit at a specific baud rate (using the **BAUD RATE** switches) and receive at another baud rate (using the rotary switch).

1.6.6 Beep Defeat

For this option a switch is added to provide the capability of defeating or not defeating the **BEEP** signal.

1.6.7 230VAC

For this option, a 230-volt transformer and appropriate power cord are provided to make the ADM 3A suitable for 230-volt operation.

1.6.8 Alternate Configuration - Green Phosphor Screen

This option provides a green display screen which has a longer persistence than the standard screen.

1.7 RELATED DOCUMENTS

- a. ADM 3A/3A+ Maintenance Manual DP305.
- b. ADM 3A/3A+ Illustrated Parts Catalog DP705.

SECTION II INSTALLATION

2.1 GENERAL

Installation procedures involving unpacking, site requirements, initial set-up, and operation checkout of the ADM 3A are contained in this section of the manual.

2.2 SPECIAL SAFETY REQUIREMENTS

Observe normal safety procedures when installing the ADM 3A. No special safety requirements are imposed.

2.3 UNPACKING AND INITIAL INSPECTION

Each ADM 3A is thoroughly inspected and carefully packaged prior to shipment. Every precaution is taken to ensure that each unit is complete and ready for installation at the customer's site. However, it is recommended that each unit be inspected upon receipt for transit damage. Start by examining the exterior of the package for evidence of rough or careless handling; then perform a thorough visual inspection of the internal components and subassemblies. As a rule, most transportation companies will not honor claims for damage unless they are filed promptly; therefore, the following steps should be taken:

1. Verify that each item shown on the Sales Order Packing Slip has been included in the shipment. Contact LSI or your distributor immediately in the event of packing shortage.
2. Check to verify that the serial number of the unit corresponds to that shown on the invoice.
3. Check the hardware to determine if any

assemblies or screws were loosened during shipment. Tighten as required.

4. Inspect for dust or foreign material which may impair electrical contact when cable connections are made. Vacuum to remove any loose dirt.
5. Install and test operation of the ADM 3A as soon as possible after delivery. (This is very important since internal damage to the equipment cannot be determined by visual inspection alone.)
6. If, in your opinion, the equipment has been damaged - either internally or externally - notify the agent of the transportation company immediately, and ask him to make an inspection. If assistance is needed to describe the extent of the damage or the repairs that will be necessary, contact your local Sales and Service Office.

2.4 SITE REQUIREMENTS

The ADM 3A may be used conveniently in a normal office environment, as no special mounting provisions are required. However, it is recommended that a weather protected environment with an ambient temperature range of 41°F to 122°F (5°C to 50°C), and relative humidity of less than 95 percent be maintained for equipment use.

CAUTION

To prevent condensation from developing, allow the ADM 3A to temperature stabilize when changing locations. Condensation could develop in the unit and adversely affect the operation of the device.

Whenever the ADM 3A is physically moved to a warmer environment than its former location, be sure to allow sufficient time for the equipment to equalize with the warmer location before activating the terminal. Condensation developed by the temperature differential may possibly impair ADM 3A operation.

Refer to Section I of this manual for physical dimensions of the ADM 3A, as well as installation power and environmental parameters. The basic requirements for reliable installation of the ADM 3A are as follows:

- Table or desk mounting
- Standard three-pronged, 115-volt or 230-volt, power outlet
- Cable connection to the computer, modem, serial printer, or other auxiliary device. If connection to a remote computer is desired, a modem or data set may be required.

2.5 INITIAL PREPARATION

Initial preparation includes: making sure that the ADM 3A will not be plugged into an AC line power output that will damage the equipment; and checking and/or resetting the configuration control switches as necessary.

2.5.1 Line Voltage Selection

The ADM 3A is shipped properly connected for either 115-volt or 230-volt AC line power, as specified in the purchase order. Any change for operation from a different line voltage requires changing components in the ADM 3A, which should be accomplished only by authorized LSI Maintenance Personnel. (Unauthorized circuit or component changes invalidate the equipment warranty.)

2.5.2 Configuration Control Switch Settings

DIP switches located on the main logic board are provided for establishing the default state of selected terminal operating characteristics. These switches are initially set at the factory in accordance with customer requirements, as expressed on the Terminal Ordering Form. Any

required switch settings should be made before attempting to operate the terminal. Figure 2-1 shows the location and identity of the configuration control switches, as well as connector/pin designations. Tables 2-1 and 2-2 describe the function and factory setting of each switch.

WARNING

Dangerous voltages exist within the ADM 3A. Always disconnect the AC power cord before opening the ADM 3A case to access any internal components.

CAUTION

Set DIP switches ON or OFF using DIP Switch Setting Tool 857001. DO NOT use a ball point pen or pencil; the switches could become contaminated with conductive debris.

Access to the configuration control switches is obtained by opening the cover of the ADM 3A, as follows:

1. Disconnect the AC power cord from the source receptacle. Also disconnect any external cables, if connected.
2. Remove the two screws located under the front corners of the base and lift the cover upwards and to the rear of the terminal, until it rests on the table or desk supporting the equipment.

2.6 INTERFACE INFORMATION

The ADM 3A may be cabled directly to a local computer, or it may be connected via telephone data lines to a remote computer located almost anywhere. Remote computer connections usually require the use of a modem or data set. Figure 2-1 shows the connector/pin assignments for the MODEM and EXTENSION ports. Figure 2-2 shows typical ADM 3A application.

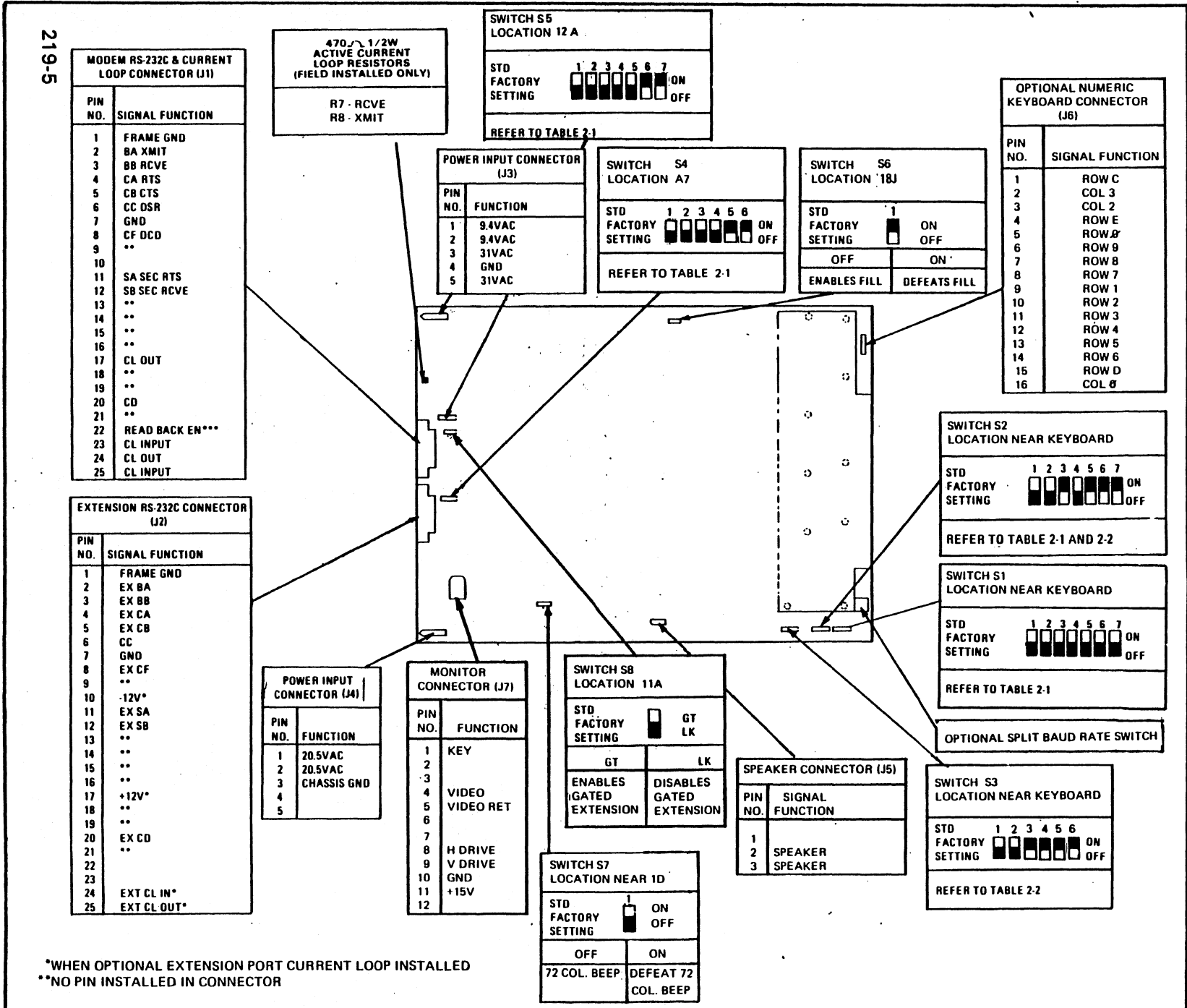


Figure 2-1. ADM 3A Connector and Configuration Switch Locations

Table 2-1. Baud Rate Switch Functions

SWITCH NO.	NAME	FUNCTION
S1-1	75 BAUD	BAUD RATE Switches for selecting MODEM port baud rate. SELECT ONE ONLY
S1-2	110 BAUD	
S1-3	150 BAUD	
S1-4	300 BAUD	
S1-5	600 BAUD	
S1-6	1200 BAUD	
S1-7	1800 BAUD	
S2-1	2400 BAUD	
S2-2	4800 BAUD	
S2-3	*9600 BAUD	
S2-4	**19200 BAUD	

*Factory Setting

**Not applicable for current-loop operation

2.6.1 RS-232C Modem Port Interface

The MODEM port interface is used to connect the terminal directly to a computer, modem, or data set in RS-232C or current-loop application. See figures 2-3 and 2-4.

2.6.2 RS-232C Extension Port Interface

The EXTENSION port interface extends the standard RS-232C capabilities of the ADM 3A by allowing the connection of a serial RS-232C peripheral.

The gated EXTENSION port mode, when selected by switch S8, allows selective transmission of data from the keyboard, in Half-Duplex mode, or the communication line through the EXTENSION port.

Note

The peripheral device that is attached to the EXTENSION port must operate at the same baud rate as the communication line.

2.7 INSTALLING THE ADM 3A

To install the ADM 3A, proceed as follows:

1. Verify that the POWER ON/OFF switch is OFF (figure 2-5).
2. Connect the interconnect cable(s) using the appropriate information in figures 2-1 and 2-2.
3. Set the configuration control switches to the positions desired. See table 2-2.
4. Set the appropriate (S1 or S2) switches for the desired baud rate. See table 2-1.
5. Connect the power cord to a grounded AC outlet.

Table 2-2. Configuration Control Switch Functions

SWITCH NO.	NAME	SETTING	FUNCTION
S2-5	HDX-FDX	ON	HDX: Places ADM 3A in half duplex mode. Each character is sent to the computer as it is entered on keyboard and displayed on CRT.
		OFF	FDX: Places ADM 3A in full-duplex mode. ADM 3A transmits and receives in both directions simultaneously. Each character must be echoed back from the host or modem to be displayed.
S2-6	RS 232-CL	ON	RS 232: Selects RS-232C interface for communication through MODEM connector.
		OFF	CL: Selects 20mA current-loop interface for communication through MODEM connector. Maximum baud rate for CL is 9600
S2-7	AUTO NL-OFF	ON	AUTO NL: Causes the cursor to move to the beginning of the next line automatically after the 80th character position is typed.
		OFF	Disables Automatic New Line Function. Each new character is written into the 80th position. A CR and LF are required.
S3-1	LC EN-UC	ON	LC EN: Causes generation of lower-case characters.
		OFF	UC: SHIFT key operational only for non-alphabetical character keys. Only upper-case characters are generated and displayed whether or not SHIFT key is depressed.
S3-2	PAR ODD-EVEN		NOTE This switch is active only when S3-5 is in PARITY (ON)
		ON	PAR ODD: Selects ODD parity
		OFF	EVEN: Selects EVEN parity

Table 2-2. Configuration Control Switch Functions (cont'd)

SWITCH NO.	NAME	SETTING	FUNCTION
S3-3	DATA 7-8	ON	DATA 7: Selects 7-bit data word
		OFF	8: Selects 8-bit data word
S3-4	STOP 1-2	ON	STOP 1: Selects 1 STOP bit
		OFF	2: Selects 2 STOP bits
S3-5	PARITY-INH	ON	PARITY: Enables parity bit after 7- or 8-bit data word.
		OFF	INH: No parity bit after 7- or 8-bit data word.
S3-6	BIT 8 0-1	ON	<p style="text-align: center;">NOTE</p> <p style="text-align: center;">This switch is active only when S3-3 is in position 8.</p> <p>BIT 8 0: Forces bit 8 to a zero value.</p> <p>1: Forces bit 8 to a one value.</p>
		OFF	
S4-1	12 LINE-24LINE	ON	12 LINE: Selects 12-line display
		OFF	24 LINE: Selects 24-line display
S4-2	50 Hz - 60 Hz	OFF	Selects 60 Hz refresh rate for data on CRT. Refresh rate should be set to correspond with powerline frequency.
		ON	Selects 50 Hz refresh rate
S4-3	DISABLE-CLR SCRN	ON	DISABLE: Prevents remote CTRL Z from clearing screen.
		OFF	CLR SCRN: Allows remote CTRL Z to clear screen.

Table 2-2. Configuration Control Switch Functions (cont'd)

SWITCH NO.	NAME	SETTING	FUNCTION
S4-4	DISABLE-KB LOCK	ON	DISABLE: Prevents keyboard from being locked.
		OFF	KB LOCK: Allows keyboard to be locked by remote control codes.
S4-5	UC DISP-U/L DISP	ON	UC DISP: Characters are displayed upper case only.
		OFF	U/L DISP: Characters are displayed upper and lower case when ADM 3A contains Lower-Case Option.
S4-6	SPACE-ADV	ON	SPACE: Selects destructive cursor. Space code always overwrites the display memory location under cursor and advances cursor.
		OFF	ADV: Selects nondestructive cursor between RETURN and subsequent LINE FEED. Cursor can be advanced with space code or key; however, space code does not overwrite display memory location. Cursor is destructive between LINE FEED and next RETURN.
S5-1 S5-2	EOT-OFF ETX-OFF	See Function	Only one switch may be active in conjunction with 202-type modem operation to select the primary channel turnaround code (See Function Description for S5-3 and S5-4).
S5-3	CODE-SEC	ON	Active only when S5-4 is ON. Used to select method of line turnaround for half-duplex operation as follows: CODE: Enables line turnaround using primary channel. Turnaround code may be either ETX or EOT.
		OFF	SEC: Enables line turnaround using secondary channel. Both S5-1 and S5-2 must be OFF.

Table 2-2. Configuration Control Switch Functions (cont'd)

SWITCH NO.	NAME	SETTING	FUNCTION
S5-4 S5-5 S5-6	202-OFF 103-OFF LOCAL-OFF	See Function	<p>Only one switch may be active at any time. Used to select one of the following methods of communicating with host computer.</p> <p>202: Enables connection to 202-type modem. Secondary channel or line turn-around code changes direction of data in primary channel.</p> <p>103: Enables connection to 103-type modem. CA (RTS) line is held high.</p> <p>LOCAL: Enables direct computer connection without modems. Request to Send (CA) line rises and falls with each character transmitted.</p> <p>All Switches OFF: CA (RTS) line is held low.</p>
S5-7	CUR CTL-OFF	ON OFF	<p>CUR CTL: Selects reverse block cursor. Cursor moves to HOME position.</p> <p>Selects double underlined cursor. Data entered from bottom of screen. No cursor addressing.</p>
S6	NORM-FILL	ON OFF	<p>FILL: Enables FILL function. Display is filled with zeros for test purposes.</p> <p>NORM: Disables FILL function.</p>
S7	ON-OFF	ON OFF	<p>Disables BEEP signal at column 72.</p> <p>Enables BEEP signal at column 72.</p>
S8	GT-LK	ON OFF	<p>GT: Enables gated EXTENSION port mode which allows ON/OFF control of the EXTENSION port.</p> <p>LK: Disables gated EXTENSION port mode which allows locking and unlocking of keyboard.</p>

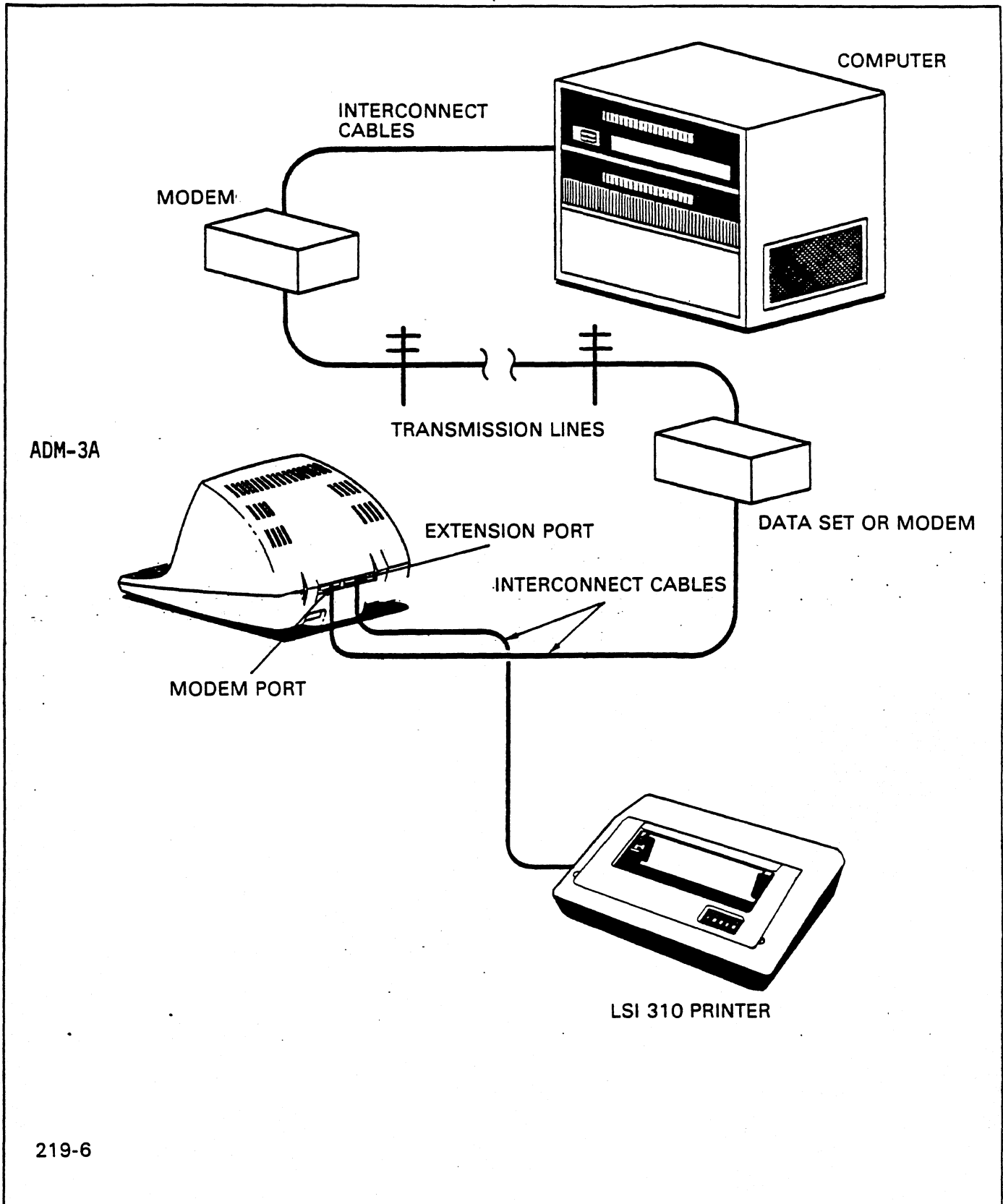


Figure 2-2. Typical ADM 3A Application

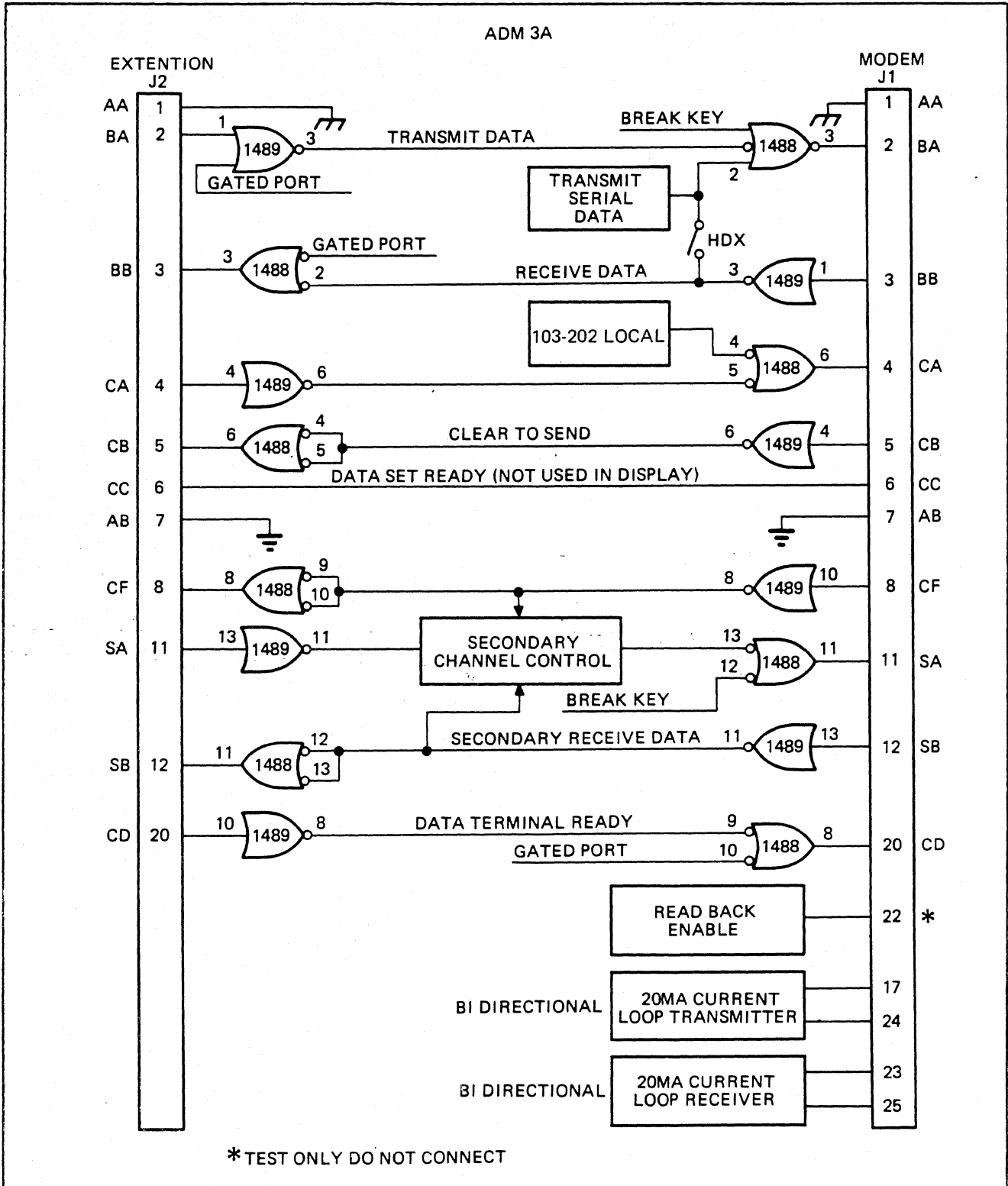
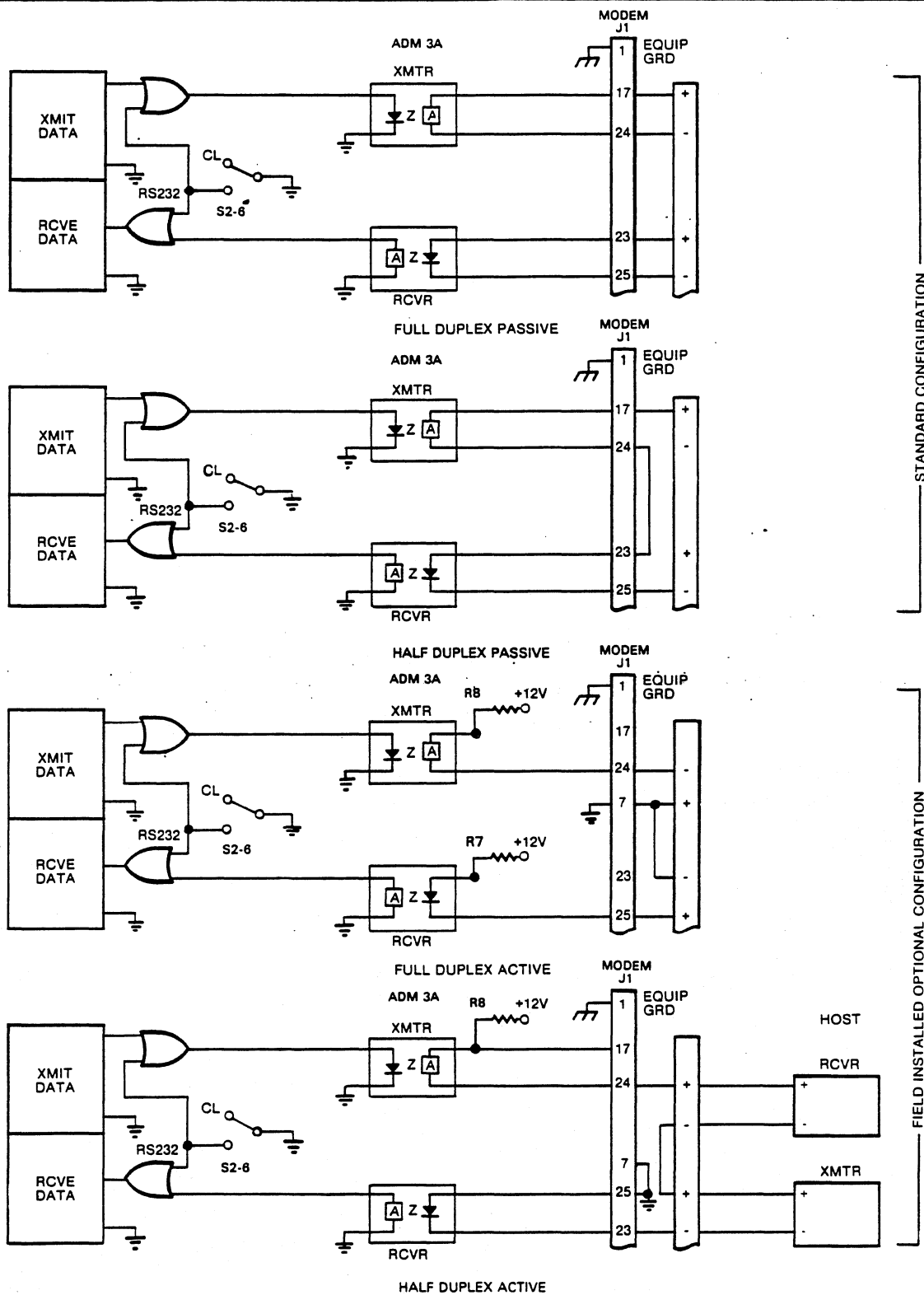


Figure 2-3. Modem and RS-232C Extension Interface Logic



219-8

FDX/HDX SWITCH MUST BE IN FDX POSITION FOR CURRENT-LOOP OPERATION

Figure 2-4. Current-Loop Interface Logic

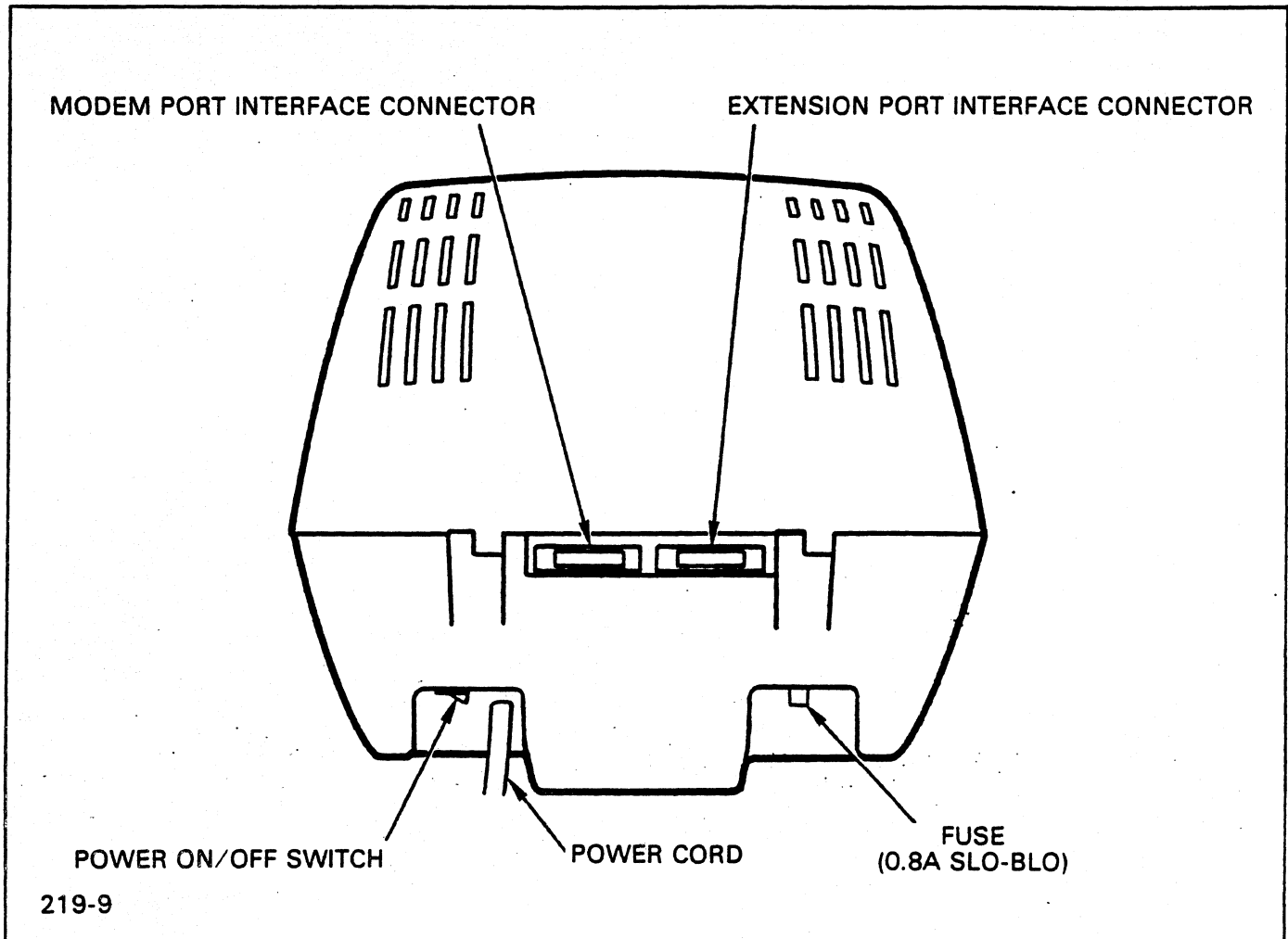


Figure 2-5. ADM 3A Rear Panel Controls

2.8 POWER TURN-ON AND TURN-OFF

CAUTION

Proceed as follows:

1. Set the POWER ON/OFF switch (figure 2-5) to the ON position.
2. Wait approximately 20 seconds for the unit to warm up.
3. If the CUR CTL-OFF switch (S5-7) is set to CUR CTL (ON) (table 2-2), a reverse block cursor should appear in the upper-left corner of the screen.
4. If the CUR CTL-OFF switch (S5-7) is set to OFF, a double underline cursor should appear in the bottom-left corner of the screen.

If power is recycled ON and OFF using the POWER ON/OFF switch, wait 10 seconds between the OFF and ON operations to ensure complete reset of the ADM 3A electronics.

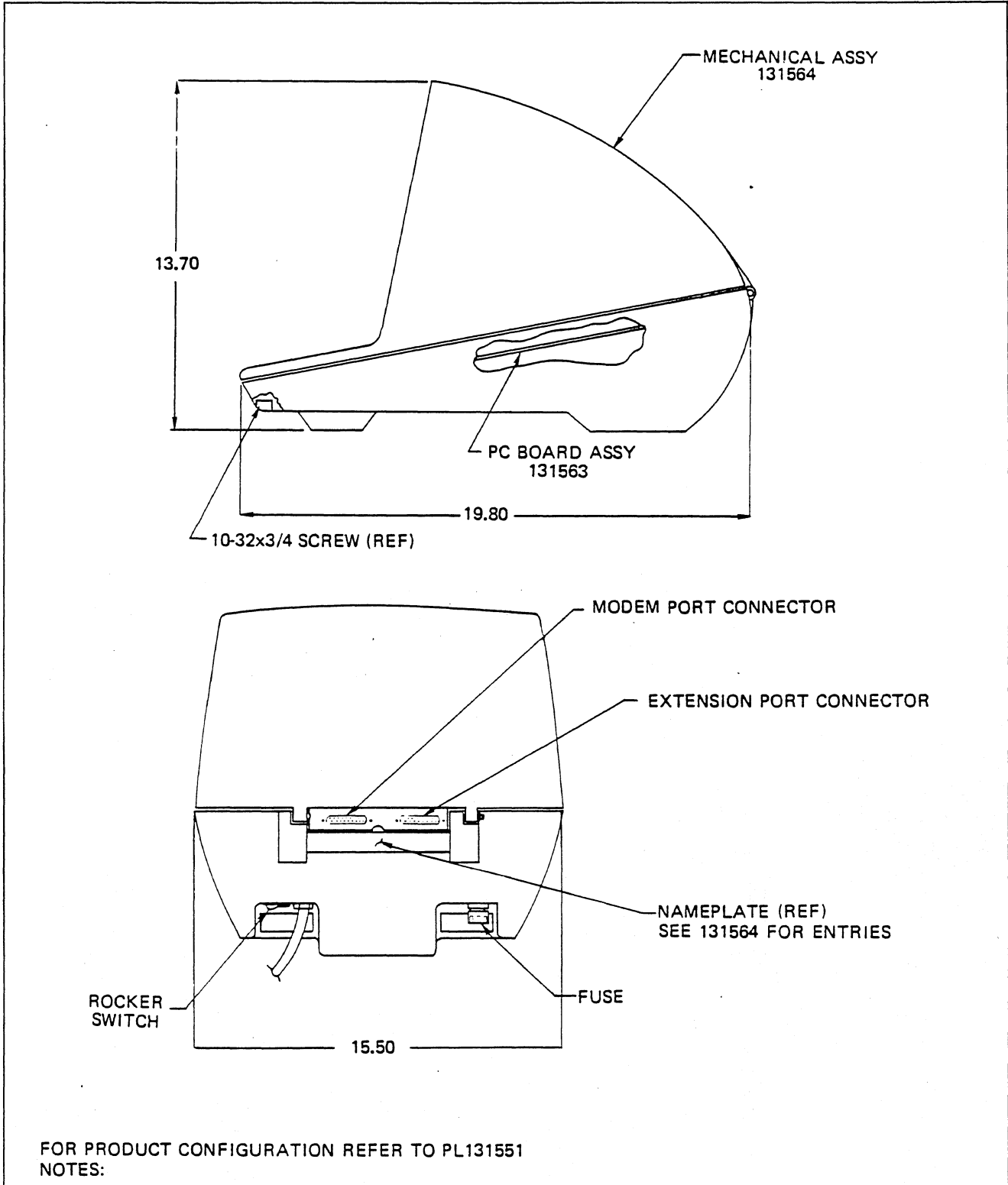


Figure 2-6. ADM 3A+ Assembly; From Engineering Drawing No. 131551

5. If the cursor does not appear, momentarily press the **CTRL HOME** keys. If this fails to produce the cursor, adjust the CONTRAST control on the front panel. The cursor should be present.

Note

If the Full-Duplex mode is selected, typing at the keyboard will not display characters unless echo-back from the host computer or modem is provided. If Half-Duplex mode is selected, data will be displayed only if CLEAR TO SEND is present or interface cable is disconnected.

2.9 CARE OF THE ADM 3A

This portion of the manual provides the required operator instructions pertaining to routine maintenance for the ADM 3A. Preventive maintenance procedures are limited primarily to cleaning and inspection steps.

2.9.1 Cleaning

At periodic intervals, clean the exterior housing and lightly dust the unit using a soft brush or damp lint-free cloth. However, paper towels may be substituted if desired. Remove smudges from the CRT exterior housing with conventional spray cleaners or alcohol. Do not use petroleum base cleaners, such as lighter fluid, as this could be harmful to the painted surface. Use only a lint-free soft cloth to clean the CRT screen. Be careful not to scratch the CRT screen, and do not use freon cleaners, alcohol, or ammonia.

2.9.2 Inspection

Periodically, inspect keyboard assembly for freedom of movement. Determine that the intensity of character trace on the CRT screen has not diminished. Any required mechanical or electrical adjustment should only be performed by an authorized Lear Siegler Service representative to insure warranty.

SECTION III OPERATION

3.1 GENERAL

The ADM 3A is used to enter, display, and send information to a host computer. It performs a similar function by accepting information from the host and displaying the information on the CRT screen. In this section of the manual, the various keys and specific control codes are described.

3.2 KEYBOARD OPERATIONS

The operator uses a keyboard very similar to the keyboard of a teletypewriter to enter data. Information typed by the operator may be displayed on the CRT screen immediately, as during half-duplex operation, or as an echo from the remote computer, as during full-duplex operation.

Figure 3-1 shows the layout of a standard ADM 3A keyboard. Functionally, the keyboard consists of displayable character keys and special function keys. Some of the special function keys can also be used in conjunction with certain displayable character keys to command specific control operations.

In the standard ADM 3A, 63 characters (plus space) are displayed. These characters include upper-case alphabet, numbers, punctuation marks, and most symbols. When a nondisplayable lower-case character is typed (S3-1 set to LCEN), a lower-case code is transmitted. However, the character is displayed as upper case. If the ADM 3A contains a Lower-Case Option, (S3-1 set to LCEN and S4-5 set to U/L DISP), 95 characters are displayed. These characters include upper- and

lower-case alphabet, numbers, punctuation, and all symbols.

Note

Typing at the keyboard always generates codes which are transmitted. However, in order for characters to be displayed and for control codes to affect the ADM 3A in FDX mode, the characters must be echoed back from the host computer. All display actions described below assume that the generated codes are properly echoed.

3.3 INTERFACE CONTROL OPERATIONS

3.3.1 Data Communication Ports

Communication between the ADM 3A and the host computer or modem is accomplished using the MODEM port. Transmission may be in one direction at a time, as in Half-Duplex operation; or in both directions simultaneously, as in Full-Duplex operation.

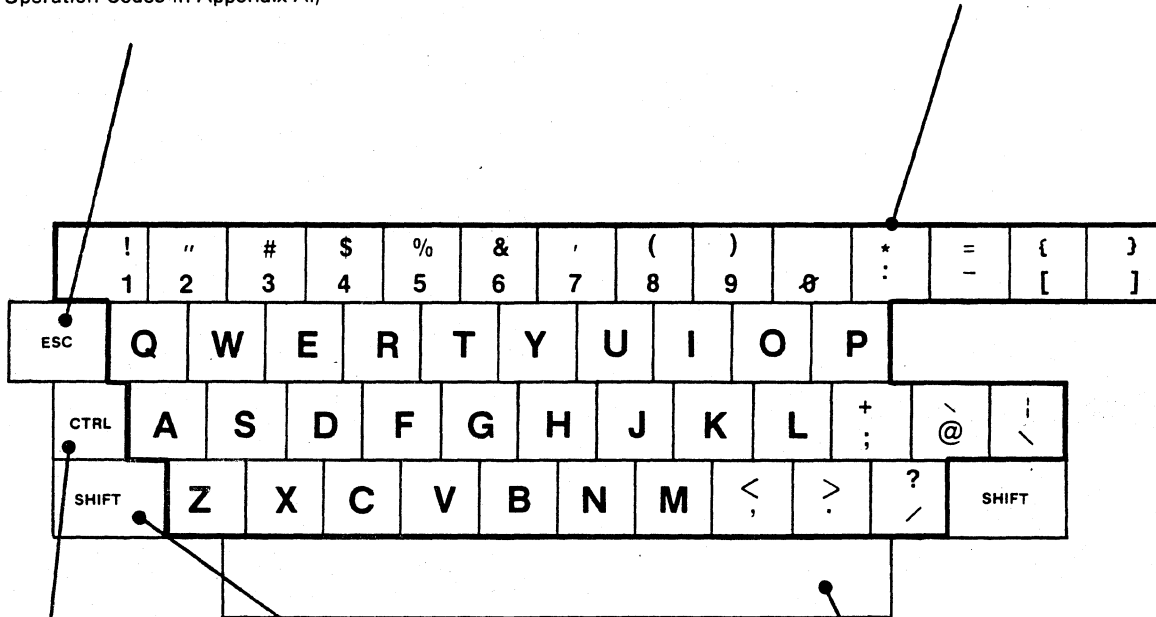
3.3.2 Request To Send Operation

The ADM 3A may receive data at any time over the RCVE line (BB). Data transmission is controlled by Clear to Send (CTS) over line CB.

Request to Send (RTS) is set (high) to inform the host that the ADM 3A wishes to transmit. If CTS (Clear to Send) is low, transmission is inhibited.

ESC is used in conjunction with displayable characters to produce an ESC sequence. (See Operators Quick Reference Chart of Control and Operation Codes in Appendix A.)

Alphanumeric, punctuation, and special character keys produce 64 (95 with Lower Case Option) displayable characters. Typing any of these keys with **SHIFT** depressed produces an upper case alpha character or the symbol imprinted on the upper portion of the key.

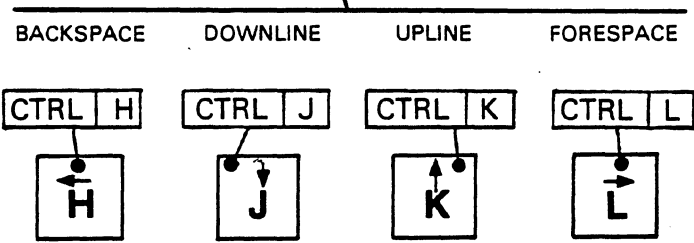


CONTROL is held down while typing an otherwise displayable character key to generate one of the 32 control codes. Only 14 control codes are applicable to ADM 3A operation. Refer to Operators Quick Reference Chart of Control Codes in Appendix A.

SHIFT must be held down while affected key is typed. Enables upper case alpha characters and symbols, as well as a shift in certain special operations. Refer to table 2-2 for function of S3-1.

SPACE bar advances cursor one space to the right each time bar is typed. Any character under cursor is replaced by a SPACE. (Exception: See Table 2-2, S4-6 Space-Adv.)

Two key operation moves the cursor incrementally in the specified direction as long as keys are depressed. Character under cursor, or characters passed over by cursor are not erased.



LINE FEED moves cursor to same column position of next lower line when CUR CTL-OFF switch (S5-7) is set to CTL (ON). If cursor on bottom line, entire display scrolls upward one line and cursor remains stationary.

When CUR CTL-OFF switch is set to OFF, all data entry is on bottom line, entire display scrolls upward one line and cursor remains stationary.

RUB transmits DEL (RUBOUT) character to the host computer. Cursor does not advance after typing **RUB**. May be used by host as a character erase code.

RETURN moves cursor to the first character position in the line containing cursor. If SPACE-ADV (S4-6) is set to ADV (OFF), space key is nondestructive between RETURN and subsequent LINE FEED. Cursor can be advanced, space codes do not override characters until LINE FEED is executed.

REPEAT allows characters or control functions to be repeated at 22 per second. The repeat rate is reduced to the transmission rate if the ADM 3A is operating at a baud rate less than 300 baud.

HOME typing **CTL HOME** moves cursor to first character position (upper left corner) when CUR CTL-OFF switch (S5-7) is set to CTL (ON).

When CUR CTL-OFF switch is set to OFF, cursor moves to first character position on bottom line. (Message is displayed in Half-Duplex Mode.)

HERE IS key is operational only if Answerback Option is installed. When typed, key transmits an identification message (stored in a special ADM 3A memory). The message is displayed in Half-Duplex.

BREAK causes the transmit data line to go positive (Spacing State) as long as the key is depressed.

CLEAR is operational only when **SHIFT** is held down. **SHIFT CLEAR** causes data to be erased from screen and from display memory. All 80 x 24 character positions are filled with SPACE codes. Cursor goes to HOME. CTRL Z from the host may be disabled by setting DISABLE-CLR SCRN switch (S4-3) to DISABLE.

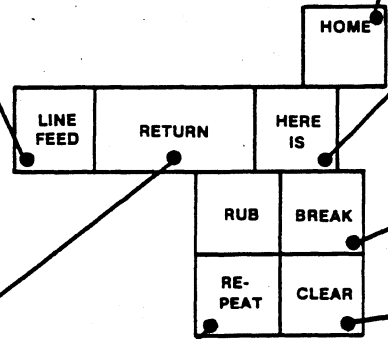


Figure 3-1. ADM 3A Standard Keyboard Operational Characteristics

RTS may be controlled in one of five ways, as follows:

1. RTS may originate from a peripheral device connected to the EXTENSION port.
2. RTS remains low if LOCAL (S5-6), 103 (S5-5), and 202 (S5-4) switches are all set to OFF (open).
3. LOCAL (S5-6) switch set to ON (closed): RTS rises before transmission of each character and falls when character has been transmitted.
4. 103 (S5-5) switch set to ON (closed): RTS remains high all the time.
5. 202 (S5-4) switch set to ON (closed): RTS is controlled through the ADM 3A interface in either code turnaround or reverse-channel turnaround operation. Transmission may be in only one direction at a time (Half-Duplex).

3.3.3 Secondary Channel Turnaround Operation

Secondary channel turnaround operation is enabled by setting switch 202 (S5-4) to ON and switch CODE - SEC (S5-3) to SEC (OFF). Both switches EOT (S5-1) and ETX (S5-2) must be set to OFF. In this operation, RTS is controlled by secondary channel signals, instead of turnaround codes on the primary channel.

ADM 3A transmission takes place when the host raises SEC RCVE (Secondary Receive Data) over line SB, and DCD (Carrier Detect) on line CF falls to indicate that the host has completed (character) transmission. RTS (Request to Send) over line CA goes high; the CTS (Clear to Send) over line CB from the host initiates ADM 3A transmission.

When SEC RCVE (Secondary Receive Data) over line SB goes low while DCD over line CF is high, RTS is unconditionally reset, thus inhibiting ADM 3A transmission.

SEC XMIT (Secondary Transmit Data) over line SA rises, allowing the host to transmit. Each time RTS switches between high and low, the ADM 3A

ignores any further commands or codes for approximately 250 milliseconds, to allow time for the host to propagate signals.

3.3.4 Code Turnaround Operation

Code turnaround operation is enabled by setting switch 202 (S5-4) and switch CODE - SEC (S5-3) to CODE (ON). Additionally either switch EOT (S5-1) or ETX (S5-2) must be set to ON. RTS over line CA is set (high) when DCD (Carrier Detect) over line CF falls as the result of decoding the ETX (EOT) code from the host, indicating that (character) transmission is complete. Data transmission from the ADM 3A may take place when CTS (Clear to Send) from the host over line CB is set (high).

When ETX (EOT), terminating each character, is again decoded, RTS (and CTS from the host) are reset to the marking state. ADM 3A transmission is inhibited, and the terminal will not recognize any further commands or codes for approximately 250 milliseconds, to allow time for the host to propagate its signal.

3.4 PROGRAMMING CONSIDERATIONS

3.4.1 Remote CTRL Operation

The host computer has full control over the ADM 3A. All control operations which are possible from the keyboard can also be executed from the computer by transmitting the appropriate CTRL codes. (Refer to the Chart of Control and Operation Codes in Appendix A). Displayable characters will be displayed, and valid control codes will be recognized and acted upon, in the same manner as that described for keyboard operations.

3.4.2 Remote Load-Cursor Operation

The computer may command the ADM 3A cursor to any absolute screen position, as shown in the Chart of Absolute Cursor Positions in Appendix E.

3.5 GATED EXTENSION PORT OPERATION

The RS-232C EXTENSION port provides a convenient method for attaching an auxiliary serial asynchronous device to the ADM 3A. The device may be an additional CRT terminal; however, a more common application is for a hard copy device such as a Lear Siegler Model 310 Printer. The EXTENSION port parallels the RS-232C MODEM port, such that any data sent to the terminal through the MODEM port is also passed through the EXTENSION port, unless the port is disabled using the gating function described below.

The gating function allows the host computer to turn the EXTENSION port ON and OFF, using control codes. This function is enabled by setting DIP switch S8 on the main logic board to the GT position. With S8 in this position, the CTRL O command disables the port, while CTRL N enables the port.

When a Model 310 Printer is connected to the EXTENSION port, several control and operation codes used for controlling ADM 3A operations will be passed through the port and affect printer operations also, as shown in the following chart:

COMMAND	ADM 3A	LSI MODEL 310 PRINTER
CTRL L	Increments Cursor by 1	Performs form feed
CTRL N	Enables EXTENSION port when in gated mode	Turns ON elongated print
CTRL O	Disables EXTENSION port when in gated mode	Turns OFF elongated print
CTRL K	Upline	Vertical tab

SECTION IV THEORY OF OPERATION

4.1 GENERAL

This section describes the manner in which the ADM 3A performs its different functions. Logic is first described with reference to an overall block diagram, and then each element shown in the block diagram is described with reference to specific illustrations and to logic diagrams contained in Section 6 of this manual (Drawings).

4.2 GENERAL FUNCTIONAL DESCRIPTION

The general organization of logic in ADM 3A is shown in figure 4-1. This figure divides ADM 3A logic into functional blocks and shows the relationships between blocks. It also indicates the sheet of the logic diagram on which logic in any block is detailed.

4.2.1 Display Generation

Signals that cause a display to be generated and maintained on the screen are furnished by a string of counters (display counter logic).

The first counter (the dot counter) is clocked by pulses from an oscillator. This clock is the primary timing signal in the ADM 3A. The purpose of the dot counter is to time the presentation of the sequential address to the character generator and the presetting of the video serializer. Each increment of the counter defines the position of a single dot in any line (dot row) of any character in the display. Any character is made up of a 5 x 7 array of dots (figure 4-2). A character position is seven dots wide and nine dots high to provide 2-dot spacing between characters both horizontally and vertically.

A single horizontal sweep of the CRT beam produces all dots in a given dot row for all characters in the character row. The character dot counter is incremented for every seventh dot column to define the position of each character in the row. At the end of each dot row, the line counter is incremented and the next dot row is scanned out. The character row counter is incremented by every ninth dot line to define the position of the next character row.

The four display counter outputs control memory addressing, character generation, and many other functions of ADM 3A logic.

4.2.2 Display Refresh Operation

Except when received data is being loaded, the contents of the refresh memory (an entire "page" of data) are continuously presented on the screen. Memory address logic requires only sequential character and row counts (CCn and RCn) to read out the memory contents to the storage latches.

Each character read from the refresh memory is stored for presentation to the ROM character memory (and to data transmitter logic for read-back test operation).

The ROM character generation decodes the stored USASCII-coded character and produces a five-bit output specifying dots to be displayed for each dot row. That is, the character is presented to the ROMs for each dot row as the character row is generated. The count CCn selects the dot pattern for each dot row.

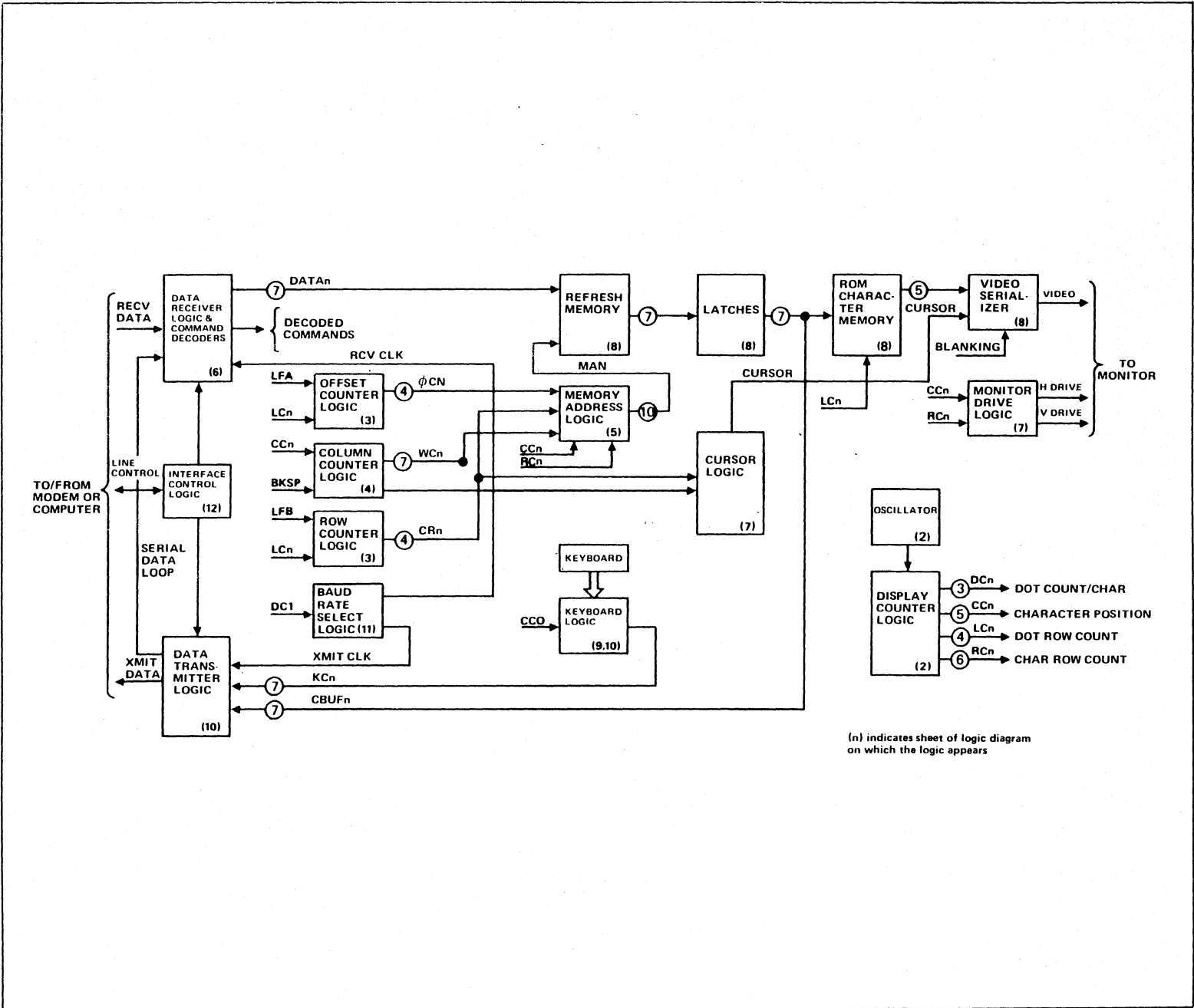


Figure 4-1. ADM 3A Interactive Display Terminal, Functional Block Diagram

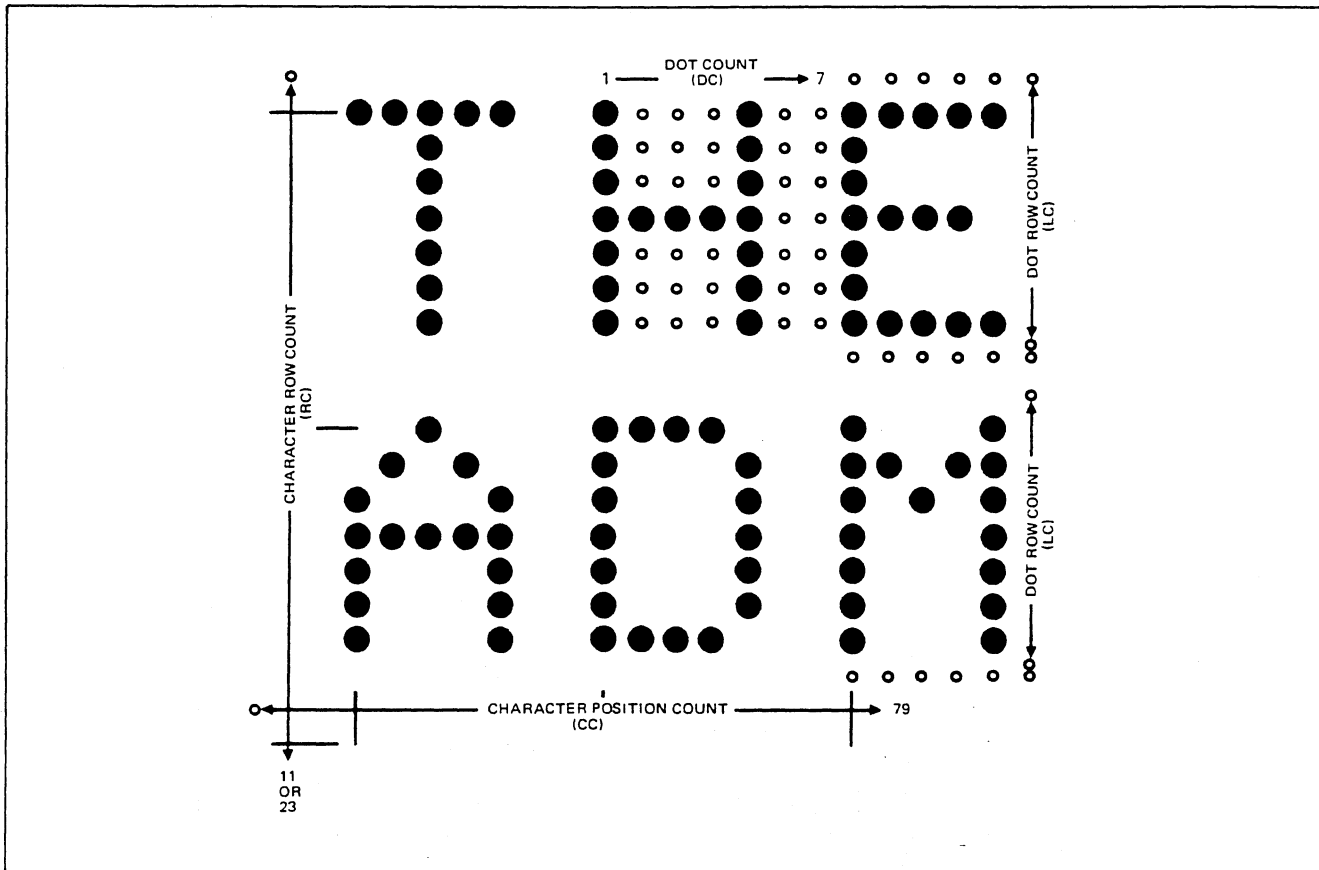


Figure 4-2. CRT Display Monitor

4.2.3 Monitor Video and Drive Circuits

The 5-bit dot row data read from the ROM character generator is presented to the monitor video circuits as a serial data stream, continuous except during CRT retrace periods. Character position and row counts are used to generate CRT sweep drive signals, with horizontal drive triggered by the start of each dot row, and vertical drive triggered when the character row count reaches 12 (standard) or 24 (optional).

4.2.4 Receiving and Storing Data

Data transmission rates are selected in the ADM 3A to match those devices on the other end of the line. Baud rates are derived from the LSB of the dot count, DC1. The receive

clock and the transmit clock may be the same or different rates (split baud rate option).

Received data is clocked into the refresh memory, which is addressed by memory address logic. The memory address, during loading, is formed by summing the Cursor Row Position Count (CR_n) which represents the true position of the cursor on the screen, and the Offset Count (OC_n), which represents the number of lines (since Reset) that the display has scrolled. The virtual address which is thus derived corresponds to the refresh address for that data row. The Refresh Address is determined by another circuit which sums the current Display Row Count (RC_n) and the Offset Count (OC_n).

Received commands are decoded and used to control ADM 3A logic. Commands include Line Feed, Backspace, Carriage Return, and other functions.

4.2.5 Cursor Generation

The cursor marks the position on the display in which the next character will appear. When the Cursor Control switch is in the OFF position, data will be entered in the bottom row; Line Feed will cause the display to roll upward. The cursor is formed by displaying five dots in the eighth and ninth dot rows of the character position in which it rests. Cursor information is ORed into video output logic along with character bits read from the ROMs.

When the Cursor Control is in the ON position, the reverse block cursor is a 7x9 dot figure containing the reverse image of the character upon which the cursor currently resides.

The cursor position code WCn is used to address the refresh memory in read-back test operation.

4.2.6 Keyboard Logic

The keyboard and associated logic are used to compose data for display and simultaneous transmission. As a character is typed by the operator, it appears (as KCn) at data transmitter logic, and (in half-duplex transmission) is loaded into the refresh memory for display. In full-duplex, communications characters originating at the keyboard appear on the display only if they are echoed back from the computer or modem.

4.2.7 Data Transmitter Logic

Data transmitter logic receives characters generated at the keyboard (or generated at optional answerback logic and put on KCn lines) and converts the seven-bit character into serial-bit form along with start, parity, and stop bits, and sends the formatted data word to the modem or computer.

In read-back test operation, the contents of the memory buffer (CBUFn) may be accepted for transmission in the same manner as data on the KCn lines.

4.2.8 Interface Control Logic

This logic controls Clear-to-Send and Request-to-Send exchanges between modem or computer and the ADM 3A. Either a code- turnaround or a reverse-channel system may be used to transfer control from one end of the communication line to the other.

Switches adapt the logic to interface with the common type 103 or 202 modems, or to operate under internal control.

4.2.9 CRT Display Monitor

The CRT display monitor employed in the ADM 3A is a solid-state unit for use in industrial and commercial installations where reliability and high-quality video reproduction are desired.

The monitor features printed circuit board construction for reliability and uniformity. All circuits of the TV monitor are transistorized.

4.3 LOGIC DESCRIPTION

The following paragraphs describe the operation of logic represented by each block in the overall block diagram, figure 4-1, as well as logic and circuits performing functions not indicated in figure 4-1. Refer to block and timing diagrams that accompany the text, as well as to the logic diagram included in Section 6 in this manual.

4.3.1 General Clear Circuit

Circuits shown on sheet 7 of the logic diagram cause all control logic in the ADM 3A to be initialized when applied power causes the +5V dc supply to rise.

As the supply voltage reaches trigger level of a retriggerable one-shot, the one-shot creates the reset signal CLEAR, which is distributed to ADM 3A logic through six inverters. In circuit board testing, the signal TESTER INITIALIZE simulates the action of the one-shot.

4.3.2 Display Counters

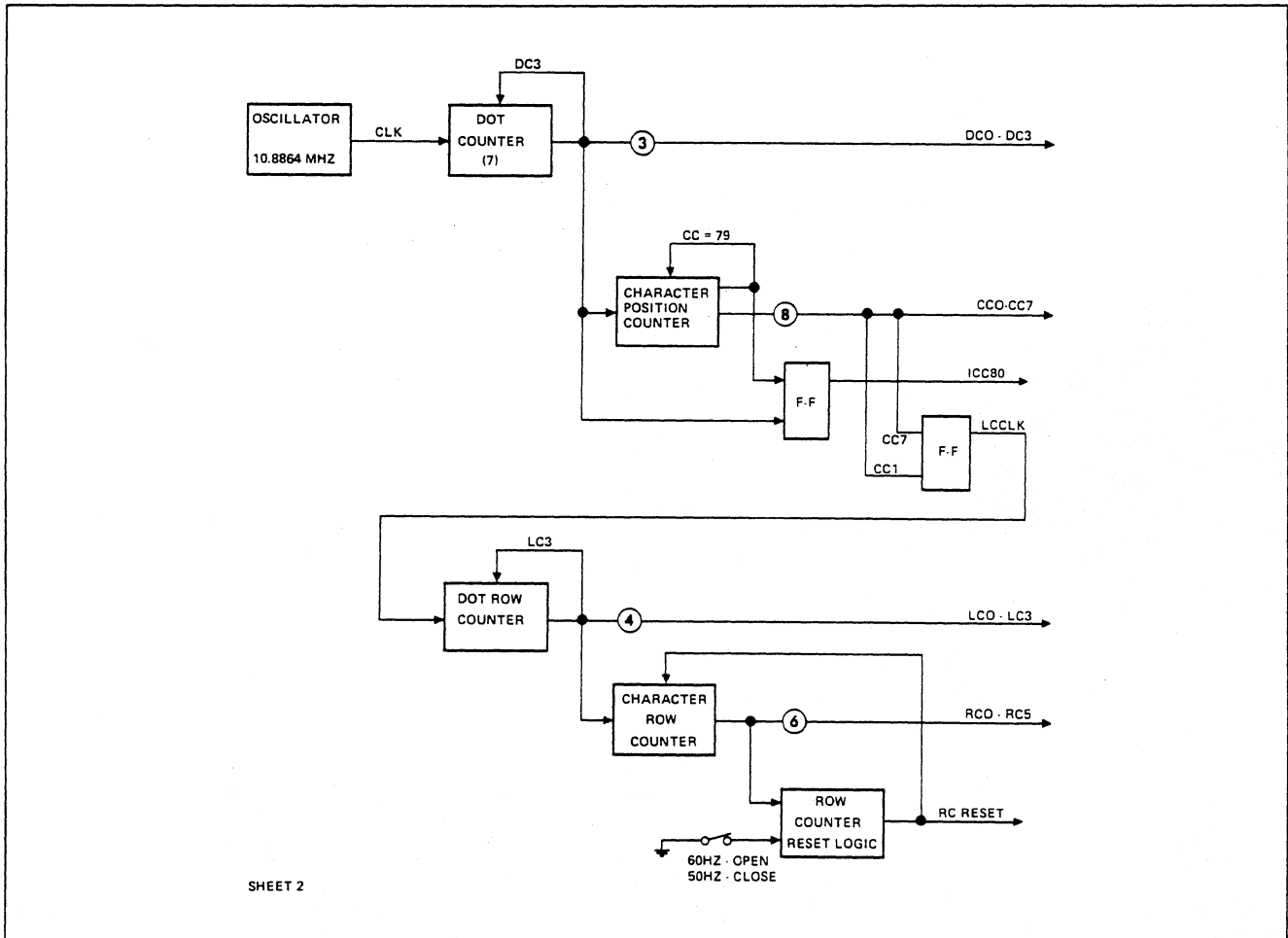
The display counters provide a count of dot positions and dot rows, character position in a character line, and character rows. These counts define the position of each dot in a character matrix, and the position of each character in the total display. Figure 4-3 is a block diagram of this logic, and timing is shown in figure 4-4.

The basic clock is a 10.884-MHz signal generated by a simple oscillator circuit. The clock frequency is twice the video frequency. The clock (CLK) drives the dot counter.

The dot counter counts the seven dot columns comprising each character. The character is preset to 10 at the count of zero, counts

through the overflow at 15, and is again preset at zero. Its final count, DC3, clocks successive addresses to the character ROMs, and triggers the character position counter.

The eight-stage character position counter controls the position of each character on the 80-character raster line, and controls horizontal retrace time. The counter provides a total count of 96 (80 counts for character position, and 16 counts for the retrace). The character position counter counts from zero to 79, presets to 240, counts through the overflow at 255, and then wraps to zero. Outputs CC0 through CC6 are binary counts, but CC7 has a value of 80. That is, CC7 is low while 80 character positions are counted, and high during retrace time.



SHEET 2

Figure 4-3. Display Counters, Block Diagram

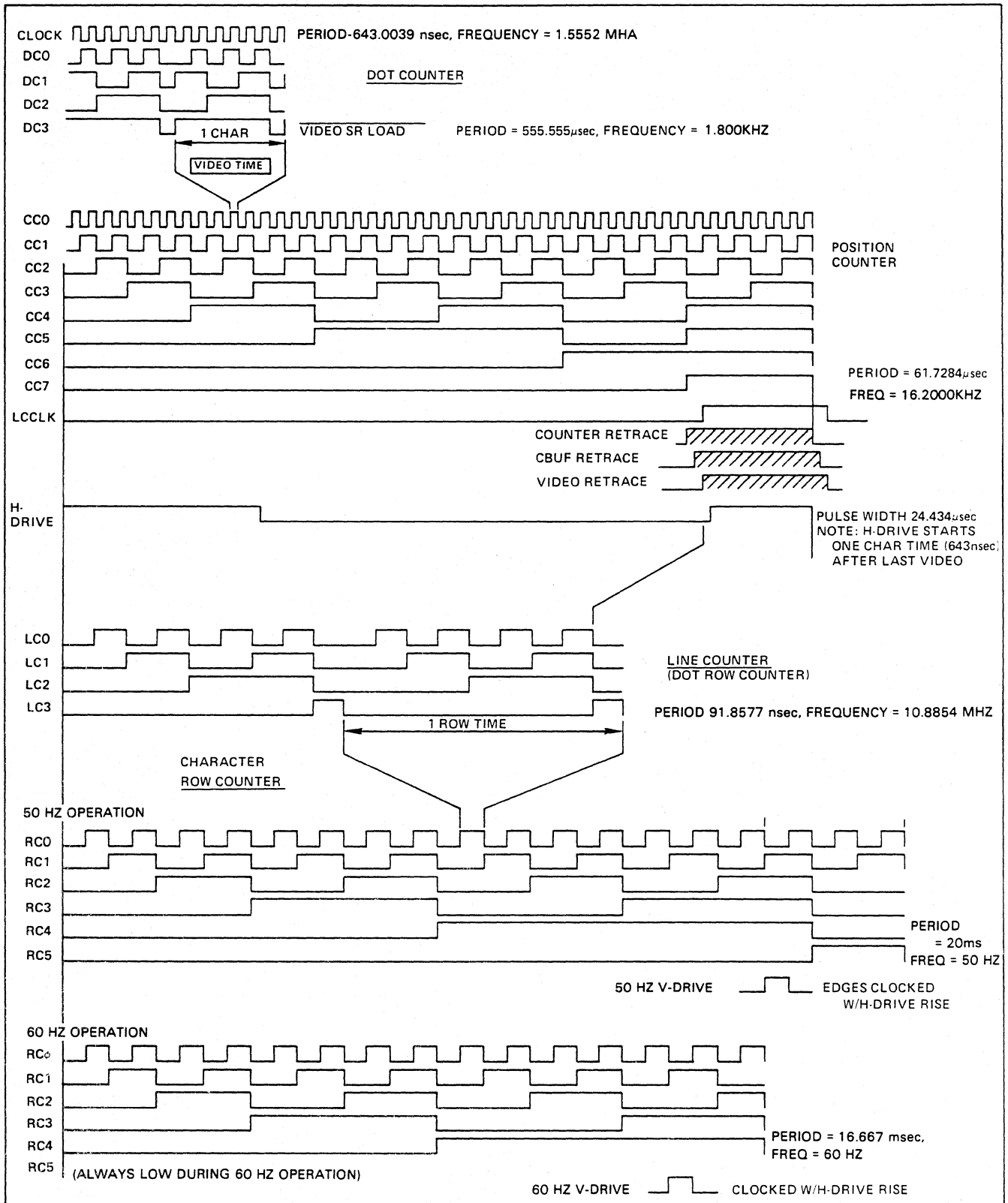


Figure 4-4. Display Counter Timing

A flip-flop produces the signal ECC80 for the first count of retrace time. ICC80 indicates the time at which a command at the I.O interface may be acted upon. The output of the LCCLK flip-flop clocks the character line counter.

The character line counter counts the lines that form each row of characters. The counter counts module nine. Counts 0 and 8 form spaces between characters, and dot rows are formed by counts 1 through 7. The last count, LC3, clocks the character row counter at a frequency of 1.8 KHz.

The character row counter counts the 24 character rows appearing vertically on the display, and counts through vertical retrace time (six counts for a 60-Hz power line, and 12 counts for a 50-Hz line). A switch (60 EN) sets up logic to produce RCRESET at the proper time, resetting the counter to zero to begin the next character row count.

4.3.3 Row Counter & Offset Counter Logic

The Row Counter (figure 4-5 and logic sheet 3) defines the actual row in which the cursor resides, and consequently, the row in which new data entered into memory will appear on the screen. This counter will be cleared to zero on 24-line, and on 12-line mode by a power-up clear, key-clear operation, or a clear screen command, irrespective of the position of the Cursor Control switch.

The Offset Counter relates absolute memory addresses, during data entry and refresh, to the virtual (apparent visual) row addresses which are generated by scrolling operations. The OC, like the RC, is initially cleared by any one of the clear-screen operations noted above, however, a sequence is then initiated by the START logic, which causes space-codes to be written into each character cell of

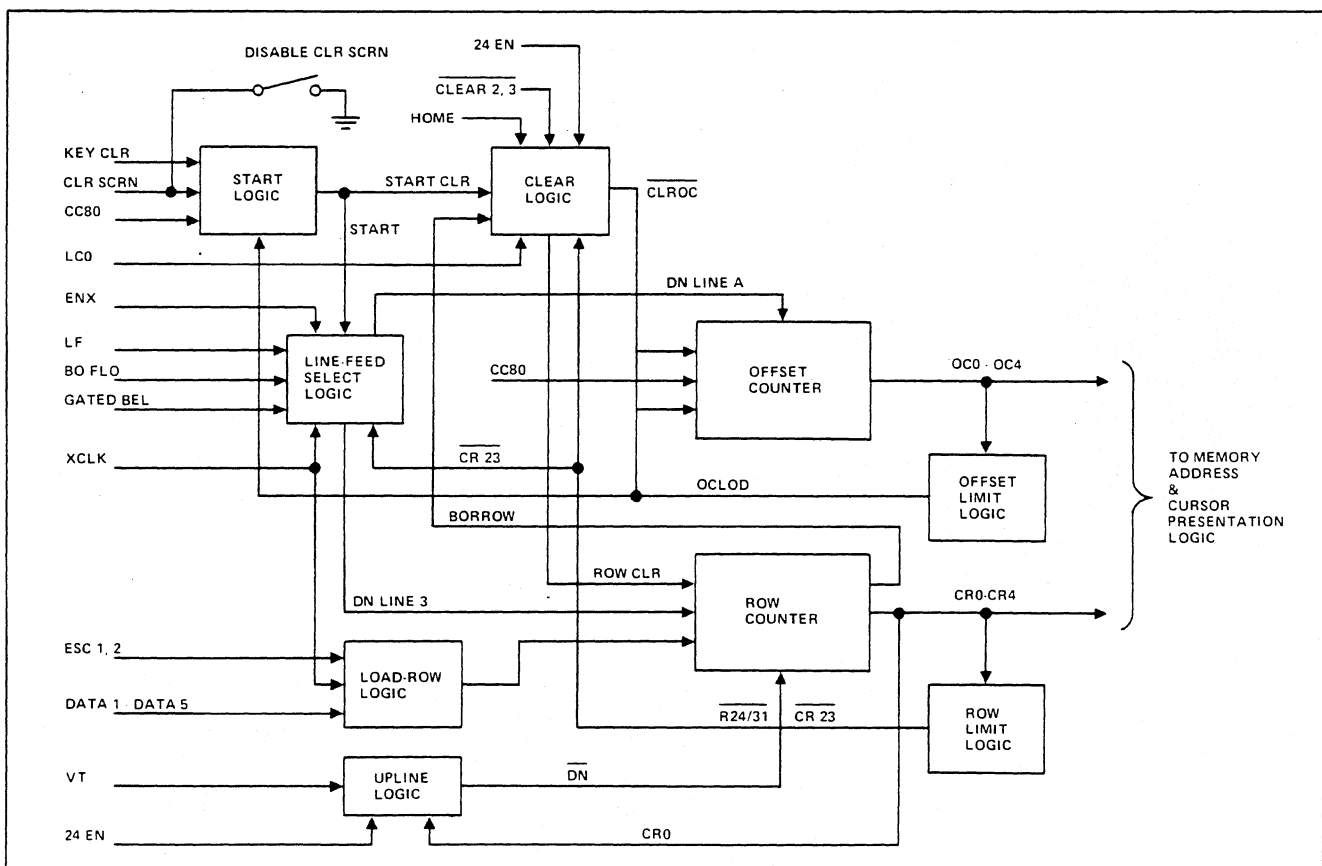


Figure 4-5. Row Counter & Offset Counter Logic, Block Diagram

the current row during first 80 character-periods of one line-scan period. At the end of the line-scan, CC80 will generate a line-feed signal, DNLINEA, which will increment the OC. The process is then repeated, with the OC pointing to the next row of memory addresses, which are also filled with space-codes.

After 24 such operations (12, if the 12/24 select switch is closed), the OCLOD signal is generated, which terminates the START operation, and freezes the OC at a count of zero (1, if in 12-line mode). At this point, both the Row and Offset counters will contain "minimum count" (zero in 24-line, and 1 in 12-line mode), and the true and virtual row-addresses will be the same (MS-A).

After completion of a clear operation, the Offset Counter will be disabled until the Row Counter has been advanced or set to 23 (bottom row). If the Cursor Control switch is open (\overline{ENX} true), line-feed signals (DNLINEB) will be sent to the Row Counter each CC80 time, until a count of 23 has been reached. At this point, the Row Counter will be disabled until either the Cursor Control switch is closed or another Clear is performed, and the Offset Counter will be enabled.

If the Cursor Control switch is closed, the Row Counter will remain at minimum count after a clear operation, and will respond to any downline, upline, Home and absolute (load cursor) row directives. In the same manner as when Cursor Control is off, downline directives which occur when the Row Counter is at 23 will be routed to the Offset Counter, causing it to increment, and scroll the entire display by adding a difference of one unit between the true and virtual row addresses.

Whereas the Offset Counter can only be incremented (DNLINEA), the Row Counter can be incremented, decremented, cleared or loaded with an absolute value (DNLINEB, VT, ROWCLR, LDROW). In the event a value in excess of 23 is loaded, the counter will be cleared to minimum count. If the Row Counter is decremented when it currently holds the minimum count, BORROW will occur, and the counter will be forced back to minimum count (ROWCLR). ROWCLR is also generated if a HOME (RS), directive is received.

Both counters, when in 12-line mode, have the least significant bit forced true, and all increment or decrement directives will affect only the higher order bits. In this mode, therefore, only odd virtual addresses will be accessible. Note, that scrolling the display will still produce only odd addresses, since the Offset Counter will count in units of two, which when "added" to the odd Row Count will still result in an odd virtual address.

Figure 4-65 shows the timing for the Clear Screen operation. The timing for Key Clear or power-on clear operations is identical to that shown, except that in the latter two situations, START is forced high without benefit of DOIT.

4.3.4 Column Counter Logic

The Column Counter (figure 4-8 and logic sheet 4) and its associated logic define the character-position of the cursor, irrespective of the current cursor mode. The counter is bidirectional, to accommodate both backspace and forespace operations, and is capable of being loaded, via an associated multiplexor, with either of two fixed values, or a variable position-code which is obtained as the last character of the four-part Load Cursor sequence.

Back-spacing (count-down) is affected only by a local or remote backspace command (BKSP), while forward-spacing may be accomplished by either a character-entry, a forespace command or a 'Read' operation. All received characters will cause a forespace after the character is written into memory, except control characters and the three non-control characters which follow ESC during a Load Cursor sequence. For both character-entry and forespace commands (FF), the counter is advanced during CC80 time. During Read operations (test only), a forespace is generated each time \overline{XLOAD} occurs, indicating, the initiation of character transmission.

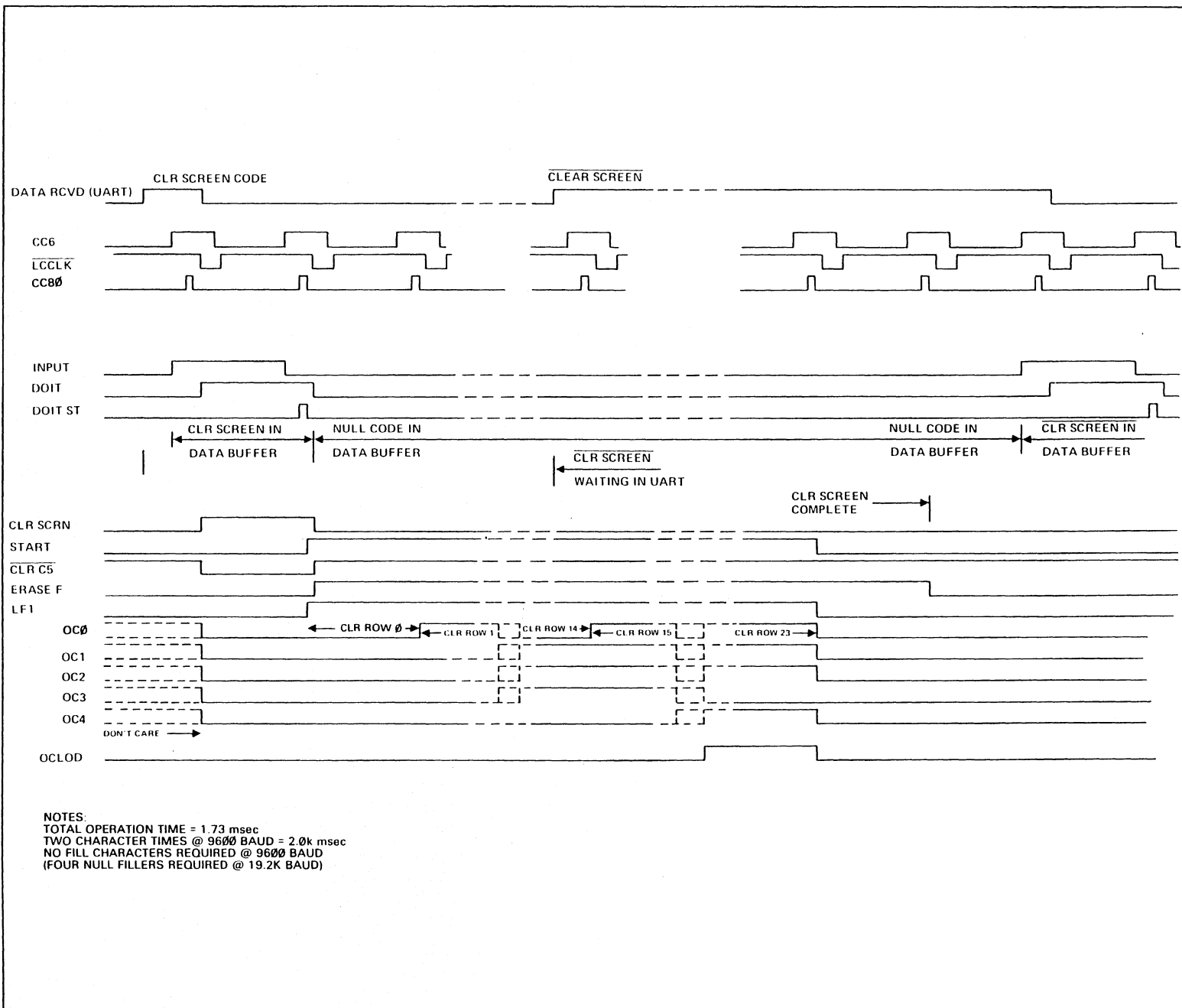


Figure 4-6. Clear Screen Timing

The Column Counter is cleared in any one of four situations:

- a. A Carriage Return (CR) command is received, either from the keyboard or a remote source.
- b. A Home (RS) command is received.
- c. An underflow occurs, due to attempts to back-space from column 0.
- d. A start-sequence is initiated by one of the power-up/clear operations.

When the Column Counter is incremented past the 80th column-count (code=79), an overflow signal is generated, causes an absolute count value to be loaded into the counter at the next LCCLK transition (CC81-time). If the Auto-New-Line switch is open, a 79₁₀ code will be loaded, forcing the cursor back to the last column position. If auto-newline is closed, a zero-code will be loaded (carriage return) and a line-feed enable signal (BOFLO) will be generated, to enable either the Row or Offset counter to be incremented.

When the code in the Column Counter reaches 71₁₀, the signal LINE END is generated. This signal, like a received BEL-code, will cause the Beeper to sound a tone, announcing the approach of the end-of-line. If the Cursor Control switch is on (ENX=true) and a Load Cursor sequence is performed, the Column counter multiplexor will select the DATA lines from the Received Data Buffer, and the Column-code on these lines will be loaded into the counter at CC80 time. The two most significant bits of the code (DATA6 and DATA7) are modified in order that ASCII codes space (040₈) through L/C "O" (137₈) are interpreted as column codes 000₈ through 117₈. In the event a translated code greater than 117₈ (79₁₀) is loaded, the OVERFLOW logic will force the counter either back to 117₈ (Auto-Newline OFF) or 000₈ (Auto-Newline ON).

4.3.5 Cursor Presentation Logic

The cursor logic (see figure 4-7 and logic sheets 7 & 8) performs the function of detecting the current character-cell in which the cursor resides, and mixing the coincidence signal with the character video to

obtain a representation determined by the Cursor-mode switch. The logic consists of a set of three comparators, a pair of unit-delay flip-flops and video mixing circuits. One comparator relates the current cursor row, as defined by the cursor Row Counter, to the Display Row Count. When coincidence occurs, an equality signal (ROWCOA) is generated.

If the Cursor Control switch is off, row-equality is forced true, since the cursor will always reside on the bottom line. If the switch is on, ROWCOA is gated to the two column comparators. The two column comparators relate the 7-bit WC counter code to the Display Column Count. When coincidence occurs, and ROWCOG is true indicating row-coincidence, an equality signal will be sent to the delay flip-flops. If the Cursor Control switch is off, the delay flip-flops will be enabled only during the period when the counters are scanning the two lines immediately below the 24th row of data, whereas in the on position the flip-flops will always be enabled. In the enabled condition, the flip-flops will delay the detected coincidence signal two character periods, to synchronize the cursor with the displayed characters on the screen.

With Cursor Control off, no additional mixing is required, since the double-underscore representation occurs during the period when no characters are being displayed. With Cursor Control on, the cursor coincidence signal (CURSOR) is gated with character-video data in an exclusive-OR element, causing the cursor to appear as a reverse image of the character in which position it resides.

4.3.6 Memory Address Logic

The logic group shown in figure 4-8 and logic sheet 5 performs all the functions related to reconciling the current entry-row (Cursor Row Counter) and virtual row (Offset Counter) positions to a physical row-address in memory, and additionally, converting the visual 80-character by 24-row visual format to a 64 by 30 byte memory array. The first task is accomplished by two five-bit and two two-bit

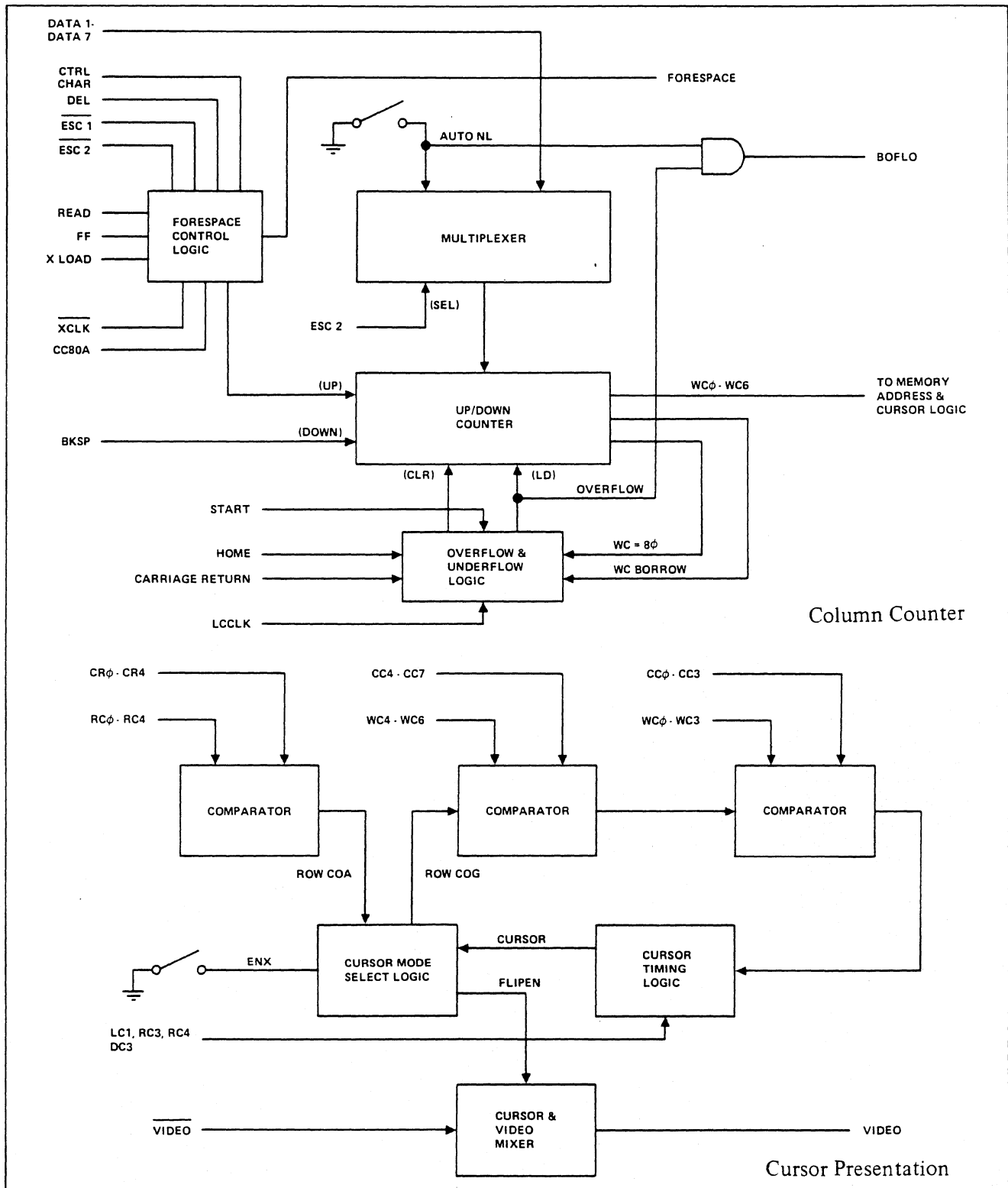


Figure 4-7. Logic Block Diagram

full adders, while the second is performed by a set of multiplexors.

The first five-bit adder produces a sum equal to:

$$\text{Display Row Count} + \text{Offset Count} + 1$$

This function provides the required relationship between current display rows and the virtual row-address during refresh scanning, in order that the data might be displayed on the proper row of the screen, consistent with the scroll-history since the

last clear-screen operation. If no scrolling has occurred, the offset count will be zero, and data for the top row of the display will be obtained at memory-row $(0 + 0 + 1 = 1)$. Likewise, data for display-row 22 will come from memory-row 23, and data for the bottom row will come from memory-row zero. One of the two-bit adders, plus associated gates, performs the function of reconciling sums greater than 23 to a 24-row universe, by adding an appropriate adjustment factor to all such sums $(23 + 0 + 1 = 24 \rightarrow 0)$.

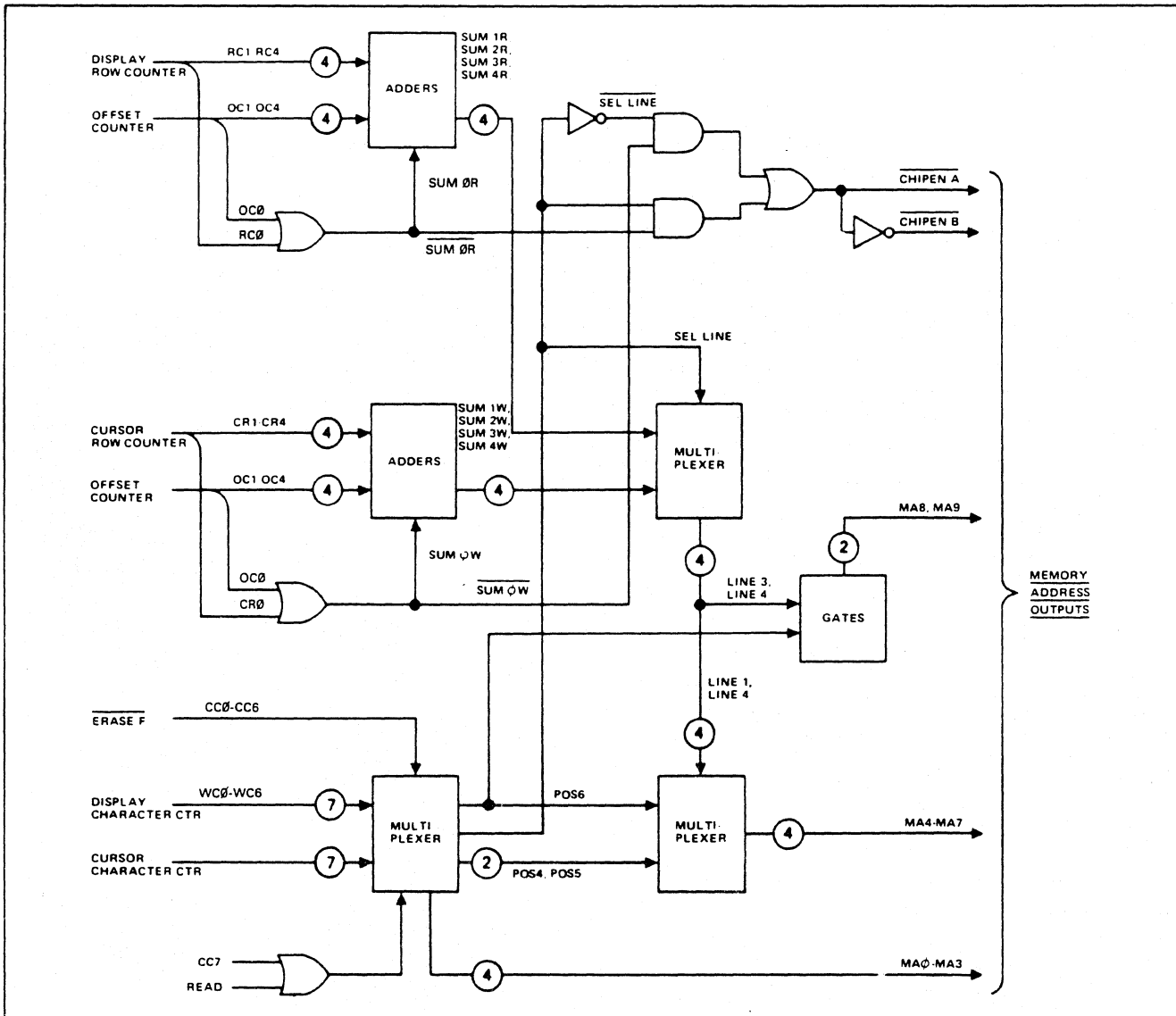


Figure 4-8. Memory Address Logic, Block Diagram

If the display has been scrolled one time, data for the top row will be obtained from memory-row 2 ($0 + 1 + 1 = 2$) and data for the bottom row from memory-row 1, thus, it can be demonstrated that all the data in memory will appear to have moved upward on the display by one row, after the scrolling operation, even though its actual physical location in memory is unchanged. The only physical alteration, in this example, occurs in memory-row 1, which is erased (see Section 4.3.8) during the scroll operation, leaving the new bottom row address locations clear for new data-entry.

Each subsequent scroll operation will, therefore, cause a successively higher memory-row address to assume the top display-row position, with the row previously associated with that position erased and "rolled" to the bottom position of the display.

The second five-bit adder produces a sum equal to:

$$\text{Cursor Row Count} + \text{Offset Count} + 1$$

This function reconciles the current cursor row-position, which is the row on which new data-entries must appear on the display, to the scroll-history, which determines the last memory-row that was erased and rolled to the bottom of the display. If no scrolling has occurred and the cursor is on the top row, the resultant sum will be memory-row 1, which is the desired row for data-entry, since that is the row from which data will be obtained for the top row of refresh. If the cursor were moved to the bottom row, the sum would be zero ($23 + 0 + 1 = 24 \rightarrow 0$), due to the action of a second adder and gate set which reconciles all $CR + OC + 1$ sums greater than 23 to values between 0 and 23. This also is consistent with the refresh adder-set, since any data entered under these circumstances will be routed to memory-row zero.

As scrolling occurs, the second adder group maintains the proper relationship between the cursor position and the virtual display-rows, such that data-entry will always occur in the memory-row which is displayed during the same row-scan time as the cursor. Consider as another example, a display

which has been scrolled six rows, after which the cursor is positioned to row 20. The memory-row actually displayed on row 20 will be:

$$20 + 6 + 1 = 27 \rightarrow 3$$

If an entry is made at the current position, the same summation will occur using the Cursor Row and Offset Counter values, and the entry will be made in row 3.

The multiplexor section of the Memory Address Logic manipulates the $CR + OC$ and $RC + OC$ sums derived above, plus the information from the Display Column Counter (CC0-CC7) and Cursor Column Counter (WC0-WC6) in order to resolve the 80 x 24 display matrix to a 64 x 30 memory matrix. The first-stage multiplexors distinguish between Refresh accesses to memory and write accesses, since the former are governed by the $RC + OC$ sum and the CC Counter information, while the latter are governed by the $CR + OC$ sum and the WC counter.

The time-period when CC7 is false is the active display-time for each scan-line, and therefore, defines Refresh-access time. During horizontal retrace, when CC7 is true, the memory is available for data-entry. During test read-back, the first-stage multiplexor is locked into the "Write" mode in order to expedite the transfer of information, since display functions are not necessary during this operation.

The most significant position of the CC/WC multiplexor is used as a selection signal for the SUMR/SUMW multiplexor, and in the write-phase will always cause selection of SUMW ($CR + OC$) for the LINE1 - LINE4 and Chip-Enable functions. In Refresh mode the SUMR ($RC + OC$) outputs will normally be selected, however, during Clear Screen or Line Erase (when scrolling) operations the term \overline{ERASEF} will force selection of the SUMW terms, in order that all erasures can take place during $\overline{CC7}$ time and thereby minimize the total time required for such operations (See Section 4.3.8).

The selected low-order column terms (MA0-MA3) require no additional modification, since the smallest increment of memory

allocated to a given line is 16 characters. The three high-order column terms (POS4-POS6) and the four high-order row terms (LINE1-LINE4), however must be modified to account for the maximum column-width of the memory matrix of 64 characters. Accordingly, the final multiplexor stage uses the column-term POS6 to distinguish between column-positions greater (or equal to) and less than 64. For positions less than 64, the high-order address functions MA4-MA9 are derived from POS4, POS5 & LINE1 - LINE4 respectively. This translation provides a direct relationship between a 24 x 64 section of memory, and that portion of the display

defined by 18WS 0-23 and columns 0-63. For column positions 64-79, POS6 switches the multiplexor to derive MA4-MA7 from LINE1-LINE4, respectively, and forces MA8 and MA9 true. This translation relates to 6 x 64 section of memory to the last 16 column positions of the 24 display rows, by allocating one-quarter of each memory-row, progressively, to the remainder of each display row. The chip-enable functions define even and odd display rows and memory-groups, and therefore, require no translation. The organization of display data in memory, is shown on figure 4-9.

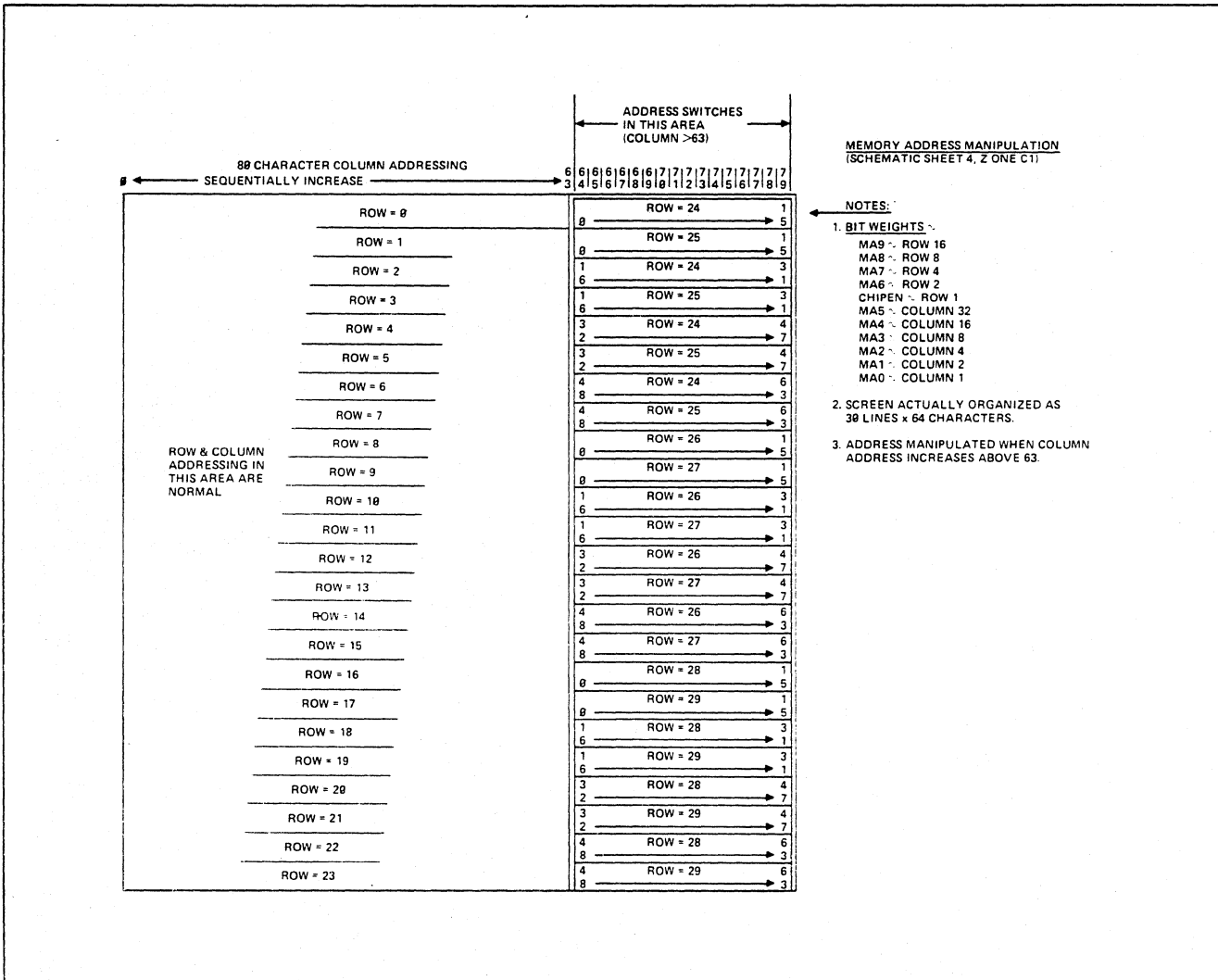


Figure 4-9. Organization of Display Data in Refresh Memory

4.3.7 Refresh Memory and Character ROM Logic

Figure 4-10 shows logic comprising the refresh memory, buffer latches, and character memory ROMs.

The refresh memory is made up of 2K, 7-bit semiconduction RAM devices in one of four configurations as follows:

- a. Six RAMs for upper-case only, 12-line display.
- b. Seven RAMs for upper/lower case, 12-line display.
- c. Twelve RAMs for upper-case only, 24-line display.
- d. Fourteen RAMs for upper/lower case, 24-line display.

A switch (UCEN) sets up the logic to operate with, or without, the lower-case RAMs. UCEN alters data to adapt the logic for either 6-bit codes (upper-case only) or 7-bit codes (upper/lower case). Term ERASEF causes the logic to force bit 6 high, creating a SPACE code in place of the received NUL code.

Data from the input buffer (DATA1-DATA7) is loaded into, or read from, the refresh memory by address lines MA0-MA9. The memory is clocked, for each character time, by WRITE PULSE.

CHIPENA is low as data is loaded into, or read from, RAMs, storing the 12 odd lines of display data. CHIPENB enables the RAMs storing the 12 even lines in a 24-line display.

At the end of each character period, DC3 clocks an addressed character into buffer latches which store the character to be encoded by the ROMs. The buffer latches are cleared by VIDEO BLANK. Because CBUF6 is normally inverted, however, a SPACE code, rather than NUL, is presented to the ROMs.

Two ROMs decode CBUF_n characters and produce a 5-bit output code that provides the dot pattern for each line in the character matrix. Each of the seven lines in the character matrix is identified by the line count LC0-LC2. The parallel-bit information output by the ROMs is serialized for presentation to the video monitor.

One ROM contains upper-case characters, and the other contains lower-case characters. Select logic senses states of CBUF6 and CBUF7 to enable either ROM device.

CBUF_n is available at data transmitter logic for transmission in read-back test operation.

4.3.8 Erase Logic

A display line is erased by the Logic shown on Schematic pages 3 and 4.

The ERASEF signal is turned on by SETERA. SETERA describes the condition in which both PGMOD & LFI are true, causing the offset counter to begin counting and the lines to scroll each time a line-feed is caused by the column counter overflowing (BLFLO).

ERASEF is turned off by CC80A after a single character row has been cleared, during scrolling.

However, when START is raised by a CLR SCRN Code, ERASEF remains high until START is turned off by an overflow of the offset counter. Consequently the entire screen is erased.

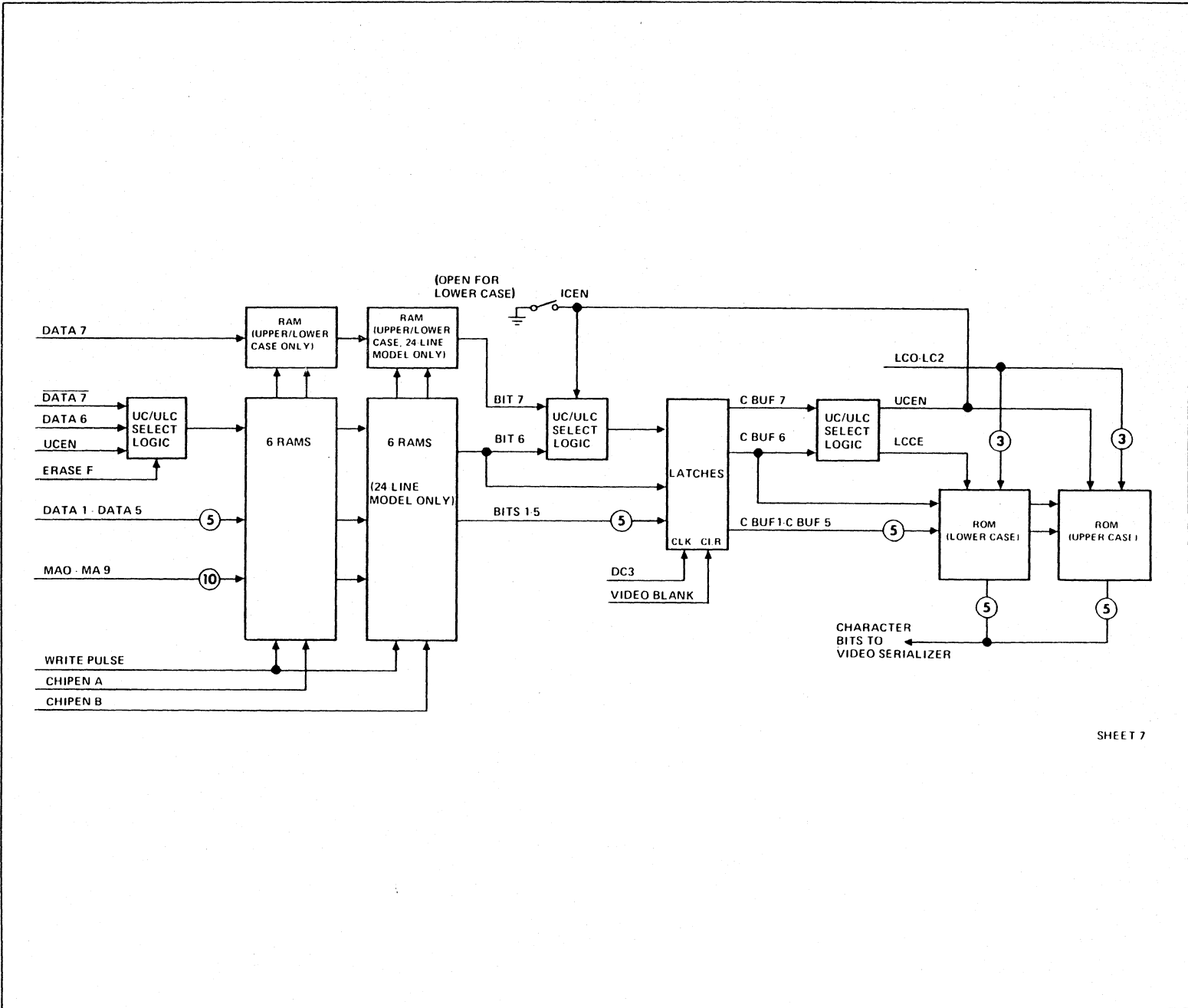
4.3.9 WRITE PULSE Logic

The WRITE PULSE signal clocks the refresh (RAM) memory. Logic that generates WRITE PULSE is shown in sheet 4 of the logic diagram.

WRITE PULSE consists of gated pulses clocked by dot count DC2, and is normally gated on by FORESPACE (the input of the cursor counter) or ERASE LINE.

The non-destructive space code feature allows writing a SPACE code (040s) into the RAM memory any time between a Line Feed (LF) code and Carriage Return (CR) code, with writing of SPACE inhibited between the CR code and the next LF code. This permits the computer or operator to write a display on the screen, issue a CR code, and space over the previously written data, with the cursor, without writing over the data.

The NO write signal inhibits FORESPACE so that WRITE PULSE is not generated during that period. A switch permits inhibiting the non-destructive space code feature.



SHEET 7

Figure 4-10. Refresh Memory and Character ROM Logic, Block Diagram

4.3.10 Keyboard Logic

Keyboard logic is shown on sheet 9 of the logic diagram (except for lock/unlock logic shown on sheet 10). Timing of keyboard logic functions is shown in figure 4-11.

The keyboard is encoded by generating the complete sequence of 7-bit USASCII codes at high speed, and trapping the code that matches a depressed key. The codes are generated continually and repetitively unless a key is pressed. The code sequence is clocked at a counter by KBCLK, which is the gated character rate signal CC0.

The four least-significant bits of the count (KC1-KC4) encode the 16 rows of the USASCII code chart. The three remaining bits (KC5-KC7) encode the eight columns of the chart.

When no key is depressed, KEY DATA is high and KBCLK cycles the counter, and bounce logic holds BOUNCE high. When a key is depressed and then the corresponding code appears on lines KC1-KC7, KEY DATA falls, preventing generation of further KDBCLK pulses so that the code is held on KCn lines. KEY DATA also causes GO to rise, causing bounce logic to count 900Hz RC0 pulses until a fifth pulse has completed a 5.56-msec delay period.

At the end of the key-bounce delay period, BOUNCE becomes true, inhibiting further counts of RC0. If the key is released, KEY DATA immediately rises and counter cycling resumes. If the key is held down, along with the REPT (Repeat) key, however, the high BOUNCE signal permits RCRESET pulses (at the ac power line frequency) to clock the bounce delay period, generating the GO signal at a rate of 12.5 characters per second at 60-Hz, or 10 characters per second at a 50-Hz line rate. Consequently, the character is repeated at that rate until either key is released.

The term THRE limits the repeat rate if the period of the selected baud rate creates a character time longer than the repeat cycle.

When the CTRL (control) key is pressed, bits KC6A and KC7A are forced to zero, forcing

any generated code into column 0 or 1 of the USASCII code chart. Bit KC5A selects either column 0 (when false) or column 1 (when true). For example, when the "R" key is pressed (0110010) along with CTRL, the effective code becomes control code DC2 (0010010).

With either SHIFT key depressed, bit 6 (KC6A) is inverted to select upper-case alpha characters (USASCII column 4 or 5, instead of column 6 or 7). Also, INVERT 5 selects codes in USASCII column 2 instead of column 3, to encode the "upper-case" symbols on numeral and symbol keys. Terms COL2 and COL3 identify those codes in the shift logic. Row 0 codes in columns 2 and 3 (SP and 0) are excluded from this action because they have no "upper case" functions.

The UPPER CASE key is used in units that do not include the lower-case alpha characters. When the key is depressed, use of the SHIFT key has no effect on alpha keys. Lower-case alpha codes are encoded in USASCII columns 6 and 7. Therefore, the gated term KC6 KC7 causes INVERT6 to maintain upper-case codes without use of the SHIFT key. Other codes in columns 4 through 7 are identified by KC7 SHIFT EN which permits normal shifting up and down.

The BREAK key is depressed to signal the computer that the operator wishes to terminate data transfer.

The BREAK function is maintained for as long as the key is held down. The signal BREAK appears at interface control logic where it forces the primary data transmit line to the "space" state if the unit is transmitting, or forces the secondary transmit line to the "mark" state if data is being received and the interface is in the secondary-channel mode of operation.

When the CLEAR key is pressed, and the SHIFT key is also depressed (SHIFT EN), KEY CLR clears keyboard lock logic, the refresh memory, and interface control logic.

The HERE IS key activates an optional Answer Back function which causes a unique, fixed message to be sent to the computer. The message, up to 32 characters long, is

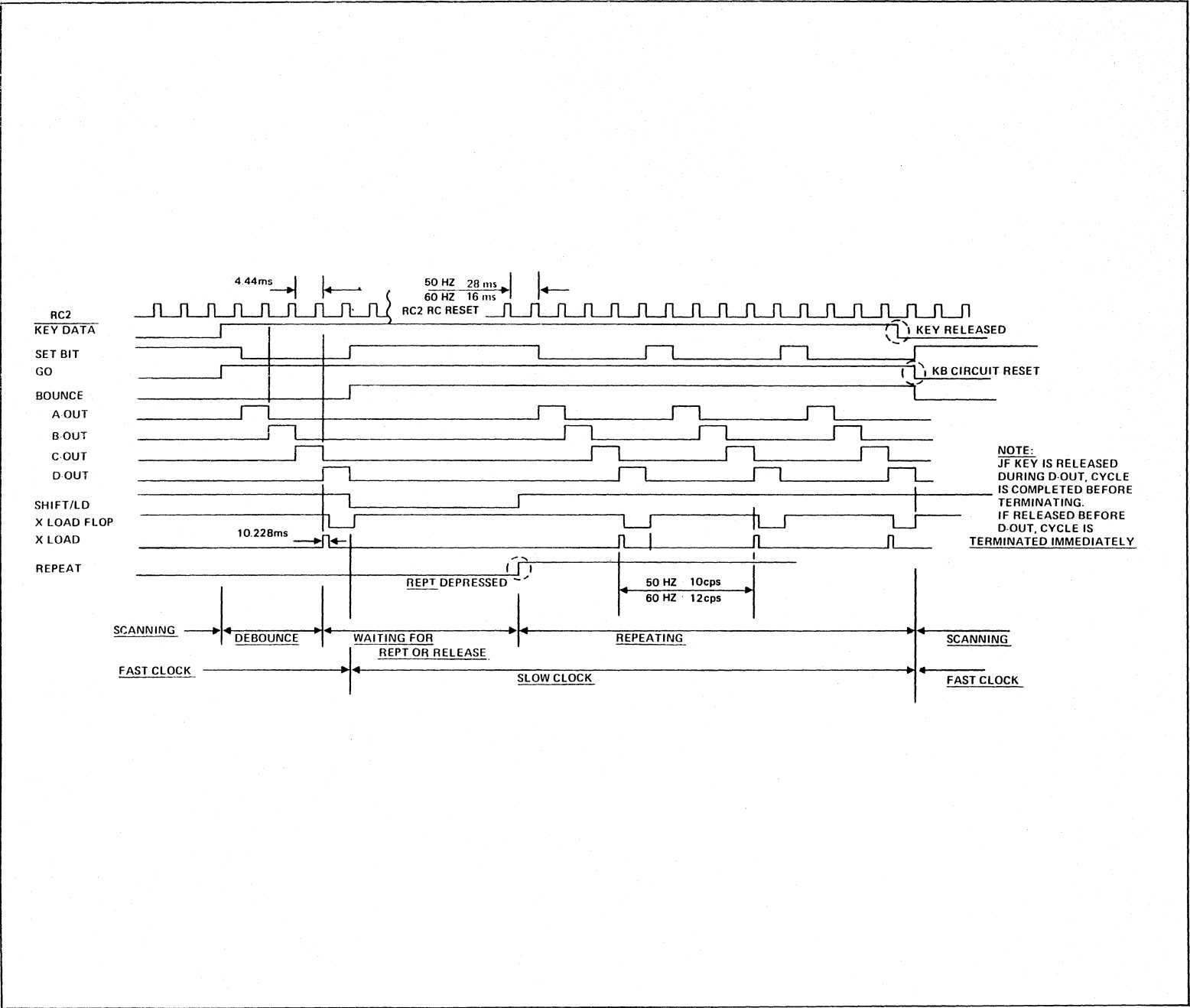


Figure 4-11. Keyboard Logic Timing

contained in a PROM device. Either the level from the HERE IS key, or an ENQ command received from the computer, causes the IDENT signal to activate logic on the Answer Back board.

Keyboard lock logic (sheet 5) permits the computer to enable or disable the keyboard logic. The KBLOCK signal is set-enabled locally by KEY CLR, or by the decoded UNLOCK command, and reset-enabled by the decoded LOCK command. Keyboard lock logic is clocked by CC80. KBLOCK prevents DOIT from generating GO, inhibiting any keyboard action. A switch permits holding KBLOCK true regardless of received LOCK commands.

4.3.11 Beeper Logic

Beeper logic (sheets 3 & 4 of the logic diagram) produces an audible signal as a near-end warning. The signal that drives the speaker is the character row rate LC2, which has a rate of 3.6 KHz.

The rate LC2 is enabled to the speaker during the "on" period of a one-shot circuit. The one-shot is triggered on by WRITE CHAR as the 71st character is written in any line (WC0 WC1 WC2 WC3 WC6). The one-shot is triggered when a BEL code is received at the I/O interface.

Because a read-back operation is initiated by BEL code, the term READ is used to disable the one-shot so that the BEL code cannot cause the audible signal.

The OVERFLOW signal is used to turn-off the one-shot when a baud rate higher than 2400 baud is used. Because the period of the one-shot is greater than the period between successive 71st characters in this case, the beeper would otherwise remain energized continuously while data is being received.

4.3.12 Data Receiver and Command Decoder Logic

This logic (figure 4-12, schematic 6 & 10) receives data from the computer through either a standard RS232 interface, or a current loop interface. Serial data is received through the RS232 interface by an RS232 receiver which sends the data to an OR circuit which also receives data from the current loop receiver.

The current loop receiver is a bipolar circuit and responds to current in either direction. The receiver comprises a rectifier/limiter which drives an optical coupler, and a single-transistor amplifier driven by the optical coupler. If the RS232/CL switch is open, the amplifier output appears at the OR logic that

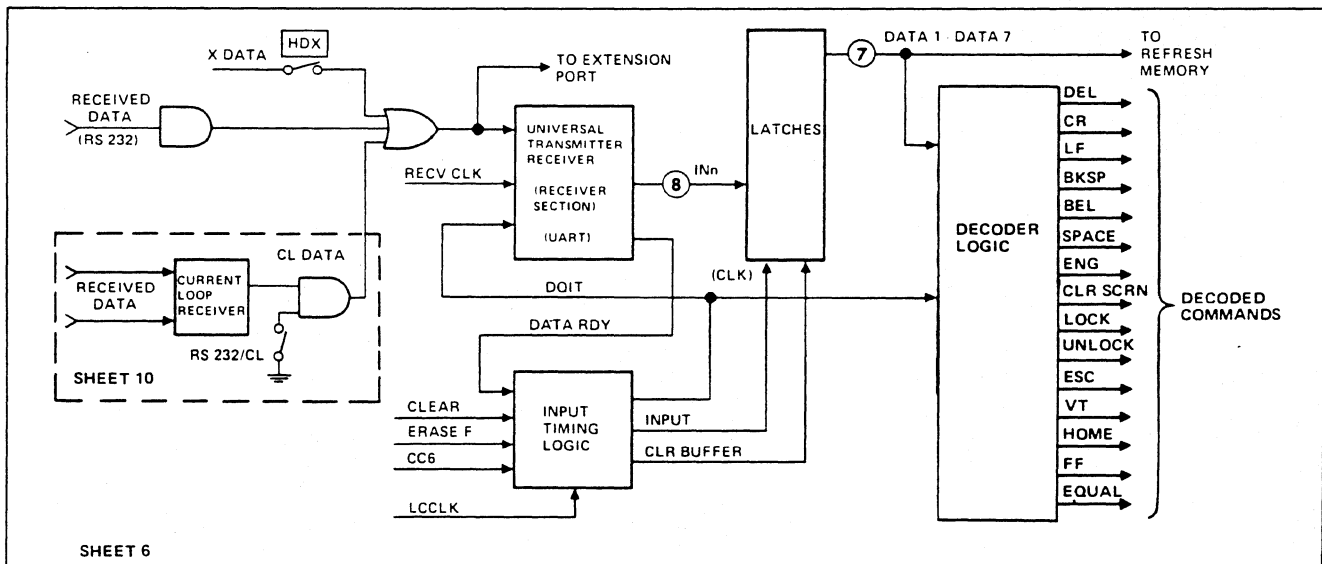


Figure 4-12. Data Receiver Logic and Command Decoders

furnishes the UART input.

A third input to the OR logic is data being transmitted from the ADM 3A (XDATA) and appears if the HDX (half duplex) switch is closed.

The received serial data, from whatever source, is clocked into the UART by RECV CLK (at the selected baud rate). In the UART, each received character is stored and presented in parallel-bit form to latches, with the most-significant bit appearing on the IN7 line. (IN8 is not used in the ADM 3A.)

The character stored in the UART is clocked into latches by INPUT as DATA RDY is output by the UART (unless ERASEF inhibits INPUT). INPUT rises when CC6 occurs at the end of every horizontal scan. Then LCCLK turns on DOIT, which remains on for the next full horizontal scan period during which the last received command is executed.

The data character stored in the latches is decoded to obtain the different control command signals. The three least-significant bits are used as chip-enable codes and are made effective by DOIT. Consequently, control commands are not effective until execution time.

4.3.13 Data Transmitter Logic

Data transmitter logic is shown in **figure 4-13** (schematic sheets 8, 10 & 12). Data that may be applied to the transmitter section of the UART are:

- a. Keyboard characters KCn, and XLOAD signal from keyboard logic, when READ is false (normal operation).
- b. Characters of the answer-back message, applied through KCn lines, when the answer-back option is included in the ADM 3A, and READ is false.
- c. The contents of the refresh memory buffer (CBUFn) when READ is true (in read-back test operation).

The UART XMIT CLK that clocks the UART is the gated XMIT CLK selected at baud rate select logic and is 16 times the baud rate. The UART is loaded from XDATA lines by LOART, which is normally high.

The UART XMIT CLK is enabled when CLR TO SEND appears at the interface, and further controlled by TRE. TRE and THRE are output by the UART. THRE falls when XDATA loads the holding register in the UART. If the serializer (which is loaded from the holding register) is empty, TRE is high. With the holding register full and the serializer empty, the UART automatically transfers the character into the serializer. At this time THRE rises, ready to accept the next character, and TRE falls to indicate that the serializer is busy. Both THRE and TRE are high when the UART holds no data.

Transmit clock logic is reset by the next Request to Send (RTS) signal from the interface.

Five switches permit formatting the transmitted character. First transmitted is always the Start bit, followed by the seven data bits (LBS first). The parity bit, odd or even, then follows (if enabled); followed by one or two Stop bits.

The serial bit stream is ORed to transmitter circuits through a gate which also receives data which may appear (from another device) at an extension port.

If the BREAK key is depressed, the XMIT DATA line is forced to the high (SPACE) level.

Data is sent through either the RS232 or current loop interface, depending on the position of the RS232/CL switch. The unselected interface maintains a marking level. The RS232 interface maintains a marking level. The RS232 interface comprises a simple driver. The current loop interface uses an optical coupler to couple the TTL data to an amplifier, and then through a diode output network to the current loop.

The optical coupler completely isolates the current loop transmitter from the ADM 3A. One leg of the current loop may be tied through a resistor to +12V dc to create a current source. As an alternative, a ground strap may be used instead of the resistor, to act as a sink for an external positive source, or a current source for an external negative voltage.

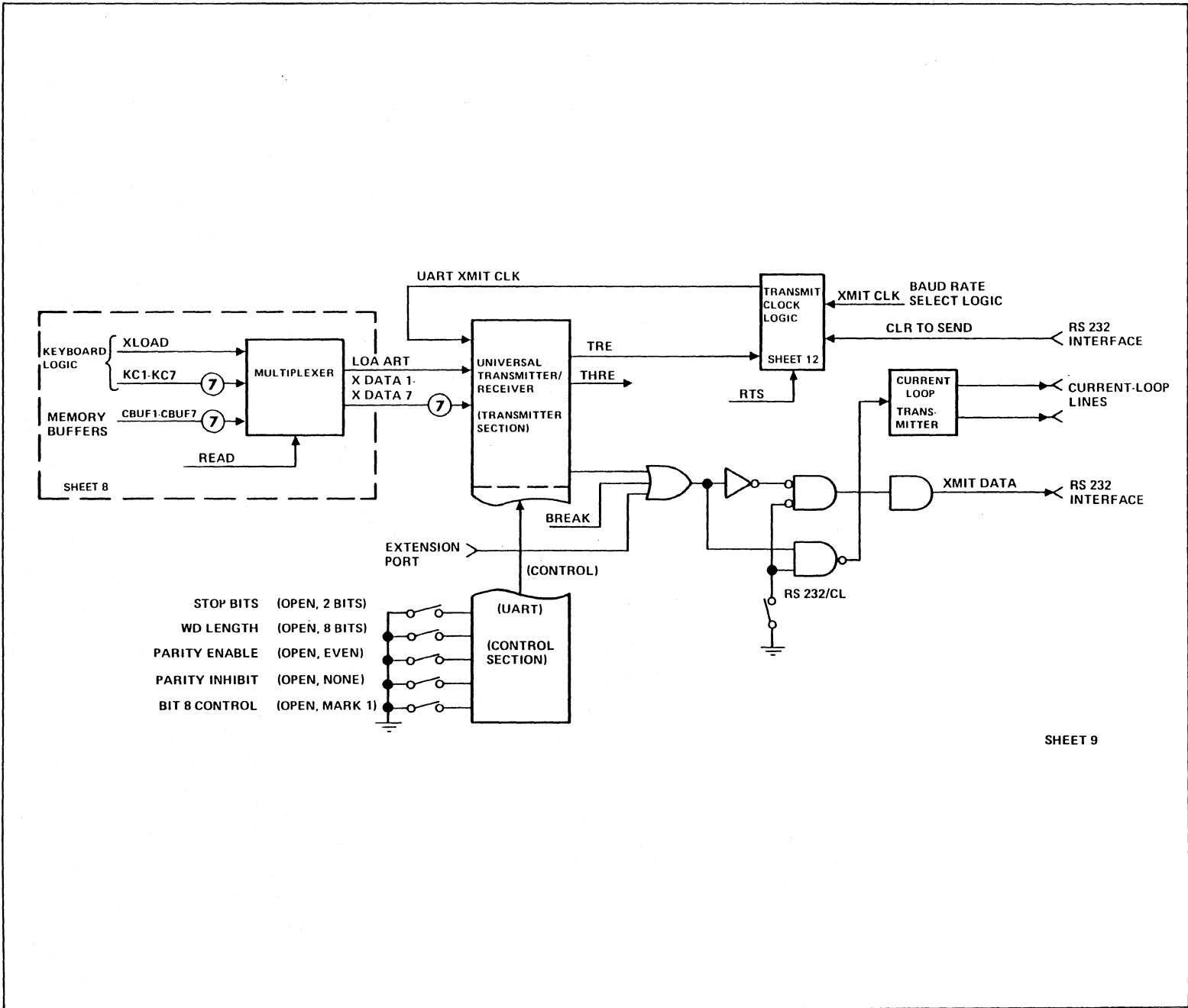


Figure 4-13. Data Transmitter Logic, Block Diagram

4.3.14 Video Blanking and Serializer Logic

Logic that controls blanking during horizontal and vertical retrace time, and converts the parallel-bit ROM outputs to a serial bit stream, is shown in figure 4-14.

Terms CC7 POS15, and RC5 control blanking for row counts of 32 and higher, and are effective only when the ADM 3A is operating at a vertical rate of 50-Hz (the count reaches only 29 in 60-Hz operation). for counts below 32, term RC=24/31 controls blanking.

Terms RC0 and 24EN cause all even-numbered character rows to be blanked if the ADM 3A is operating with a 12-line display.

In every case, VIDEO BLANK is clocked to the memory buffer latches by BDC3 as the current character is completed. VIDEO BLANK clears the buffer latches but, because bit 6 is normally inverted, the USASCII SPACE code is presented to the ROMs, instead of NUL.

During a read-back test operation, READ blanks the video but permits sending CBUFn data to transmitter logic.

The video serializer is an 8-bit shift register. Term DC3 loads it with the ROM output character bits every 643 nsec, and the bits are shifted (by CLK) at a rate of 10.8864 MHz. The shift register output is ORed with cursor information to produce the MONITOR VIDEO signal. The video level adjustment potentiometer is located at these circuits.

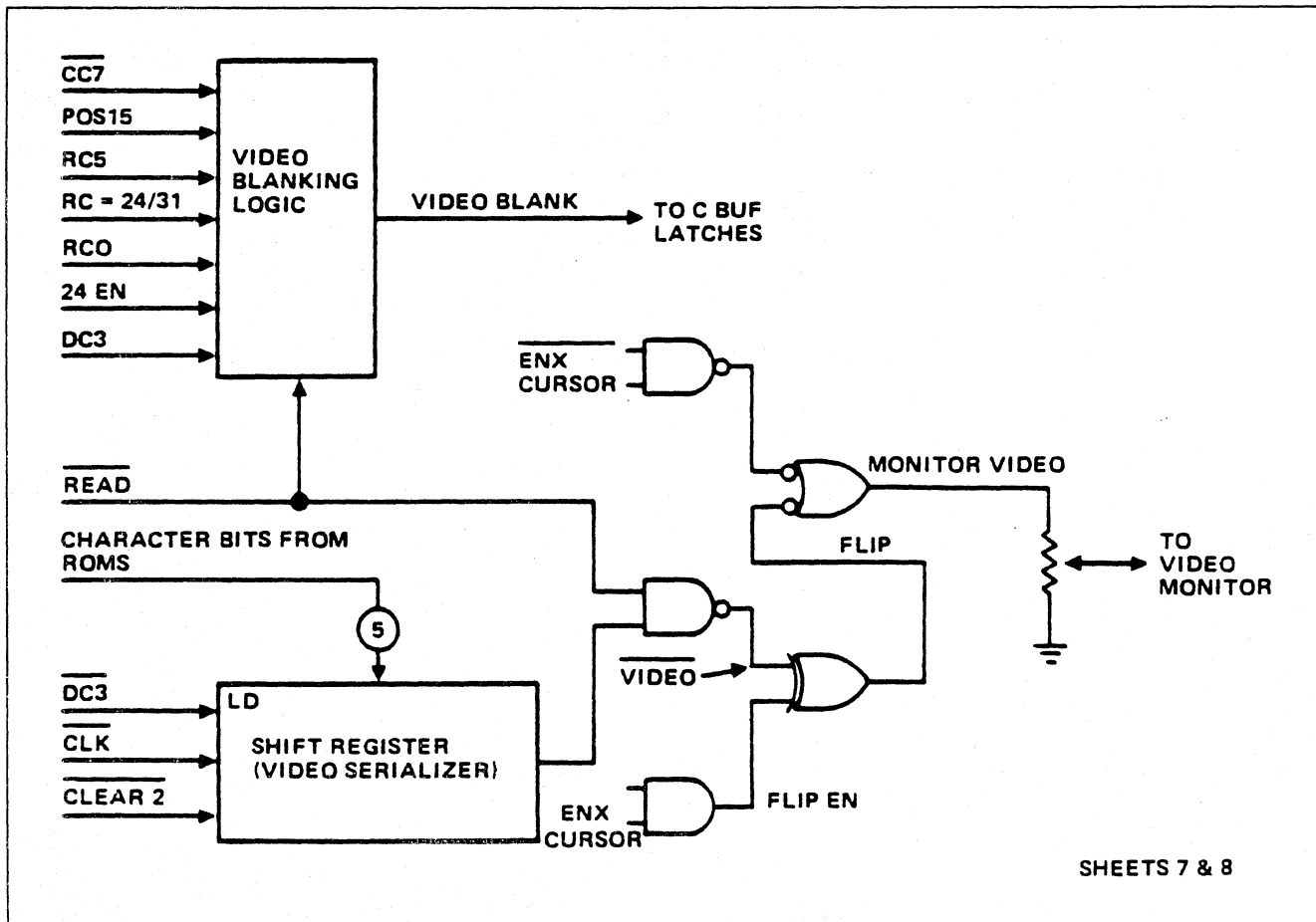


Figure 4-14. Video Blanking and Serializer Logic, Block Diagram

4.3.15 Monitor Drive Logic

This logic (shown on sheet 7 of the logic diagram) generates signals that trigger horizontal and vertical drive cycles in the monitor. To obtain the horizontal drive signal HDRIVE, character position counts are decoded to set HDRIVE false at the start of a row. HDRIVE is set true one count after the rise of CC7 to start the video retrace period.

The vertical drive cycle is begun by VDRIVE. This signal is generated by decoding character row counts RCn, and setting the VDRIVE flip-flop one count after the last character of the last line has been written. The flip-flop is clocked by the HDRIVE signal for the line just completed.

The level 60EN controls timing for 50-Hz or 60-Hz power lines. Refer to figure 4-4 for timing diagrams.

4.2.16 Baud Rate Select Logic

Figure 4-15 illustrates the logic used to generate and select baud rates for data transmission and reception.

The basic clock used in this logic is the 3.1104-MHz pulse stream DC1, which originates at the display dot counter. The 3 binary counters divide pulse rates by 5, 16 and 16 respectively, except when an 1800 or 110 baud rate is selected. These rates (from 75-19200 baud) are obtained from the counters and are selected by means of a BAUD RATE Switch.

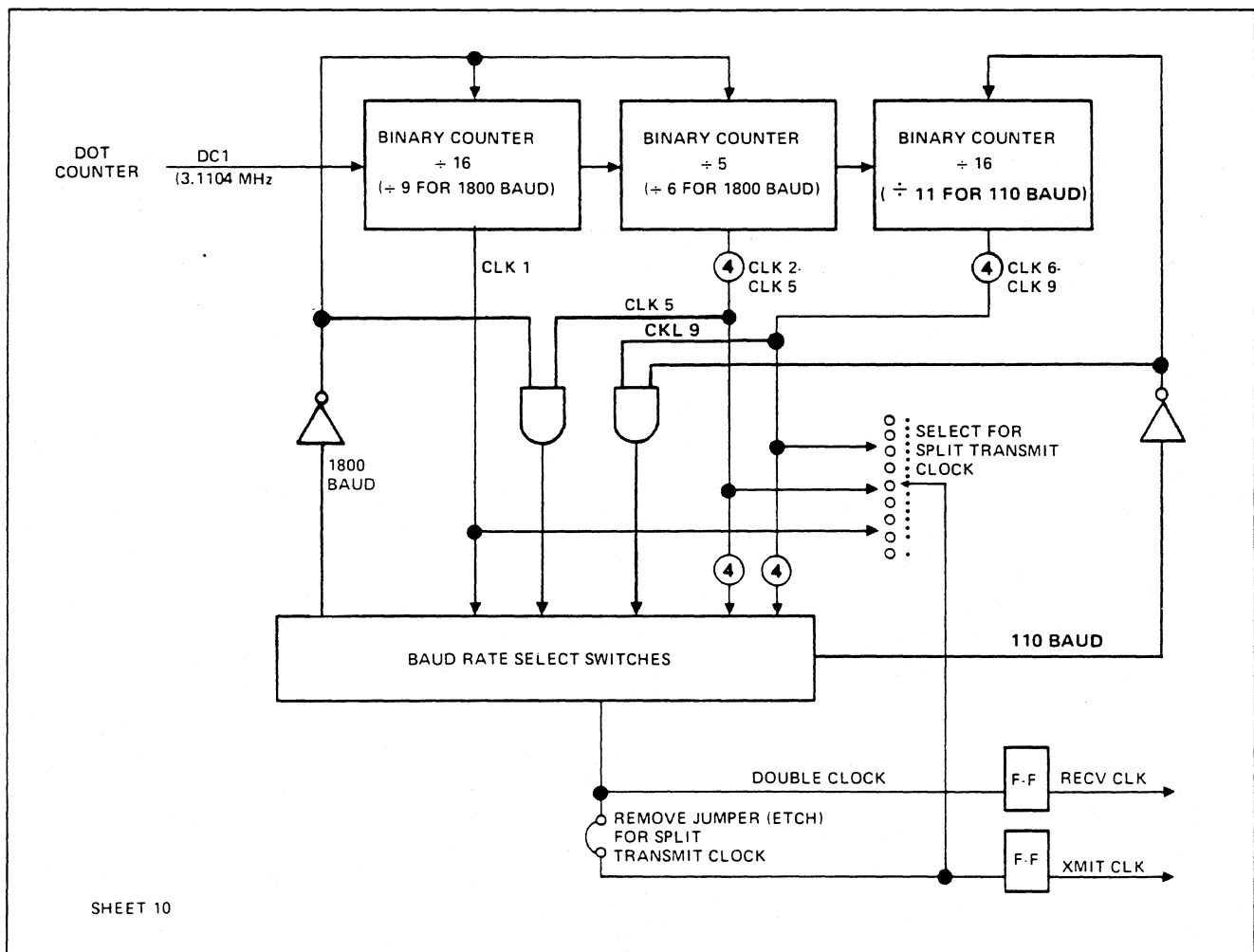


Figure 4-15. Baud Rate Select Logic, Block Diagram

When BAUD RATE switch 1800 is on, the 3 binary counters divide pulse rates by 6, 9 and 16 respectively and CLK5 is selected as the double clock.

When BAUD RATE switch 110 is on, the counters divide the pulse rate by 5, 16 and 11 respectively and CLK9 is selected as the double clock.

The double clock rate is divided by flip-flops to provide the RECV CLK and XMIT CLOCK signals. Normally, both flip-flops are clocked at the same rate. However, when a split clock is required, the XMIT CLOCK may be derived from another rate selected by means of a rotary switch located inside the ADM 3A case.

When the common clock is used, the rotary switch must be in position 12. When the split clock is used, the printed circuit joining clock inputs of both flip-flops must be cut.

Note

XMIT CLOCK can be split off only if the RECV CLICK is NOT set to 110 or 1800 baud.

4.3.17 Interface Control Logic

Interface control logic appears on sheet 12 of the logic diagrams. This controls request-to-send and clear-to-send communications for the ADM 3A.

CLR TO SEND (high) permits data transmission logic to produce UART XMIT CLK, sending data from the ADM 3. If CLR TO SEND falls while a byte is being transmitted, TRE maintains the transmit clock until the byte has been completed, and then falls to shut off the clock and return the line to the marking state.

REQ TO SEND (RTS) may be controlled in any of four ways, as follows:

- a. RTS may originate at an extension port.
- b. If switches 202, 103, and LOCAL are all open RTS remains low all the time.
- c. If only switch 103 is closed, RTS remains high all the time.

- d. If only the LOCAL switch is closed, signals THRE and TRE control RTS. RTS rises to transmit each character, and falls when the character has been shifted out of the ADM 3A.
- e. If only the 202 switch is closed, RTS may be controlled through the ADM 3A interface in either code-turnaround, or reverse-channel operation.

4.3.17.1 Code-Turnaround Control

Either an ETX code or an EOT code may be selected to initiate turnaround, depending on the position of the ETX-EOT switch. When the selected code appears in the input data, LATCHED CODE is set. When CARRIER DETECT falls (figure 4-16), indicating that the remote end of the line has dropped, RTS is set.

RTS is reset when ETX or EOT is again decoded, and the logic switches to the receive mode. Following a turnaround commands, no further command will be recognized for approximately 250 msec. This interval gives the modem time to propagate its signal. The interval is timed-out by two flip-flops and a counter, and the signal SBEN controls resetting of RTS.

4.3.17.2 Reverse-Channel Control

In reverse-channel operation RTS is controlled by SEC RECV DATA (SB) and CARRIER DETECT (CF) from the modem. When SB goes low, RTS is unconditionally reset (figure 4-17), switching the interface to receive data. In normal reverse-channel receive operation, CF is high at this time, causing SEC XMIT DATA to rise.

When the remote end of the line raises SB, and then drops its RTS (and CF), the ADM 3A turns on its RTS. The ADM 3A will then ignore further commands for a 250-msec period while the modem propagates its signals.

4.3.18 Power Supplies

AC Power is applied to the transformer through the ON/OFF switch on the rear of the ADM 3A. The different stepped-down ac voltages connect to the main circuit board through connectors J3 and J4.

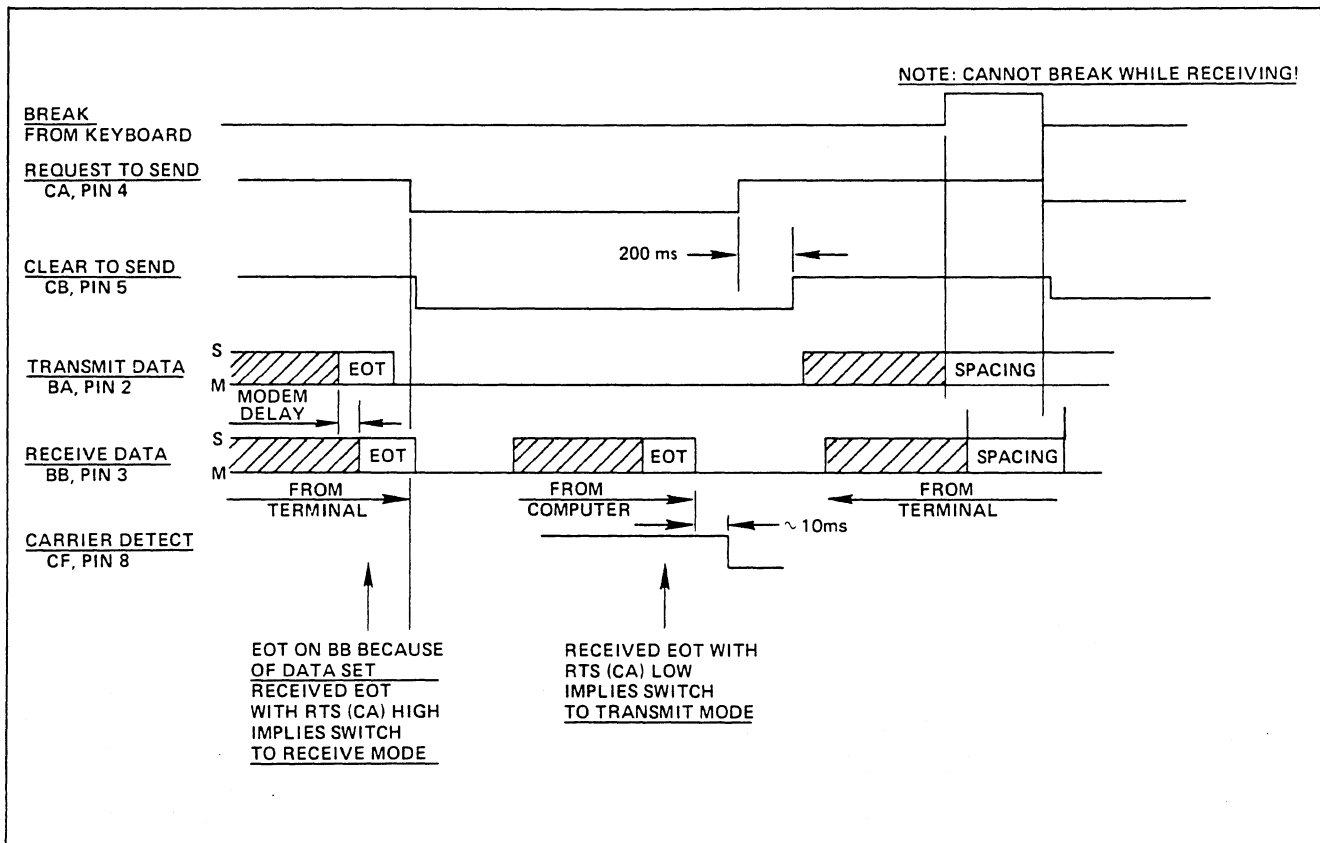


Figure 4-16. Interface Timing for Code Turnaround

Rectifiers, filter capacitors, and voltage regulators are all located on the main circuit board. Three type 7805 devices provide the +5V dc logic supply, and 7812, 7912 devices furnish 12V dc to operate memory devices and interface drivers.

A +15V dc supply required by the monitor is made up of a type 7815 device and a simple transistor shunt regulator. Located at the bottom of the terminal pan is a primary fuse. It is an 8/10 amp Slo-Blo 115V fuse or a .4 or 4/10 amp Slo -Blo 230V fuse.

4.3.19 CRT Display Monitor Logic VIDEO AMPLIFIER

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101 and its components comprise the video output driver with a gain of about 17. Q101, operating as a class B amplifier, remains cut off until a DC-coupled, positive-going signal arrives at its base and turns on the transistor. R111 adds series feedback and turns on the transistor. R111 adds series feedback which makes the terminal-to-terminal voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient temperature variations.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential

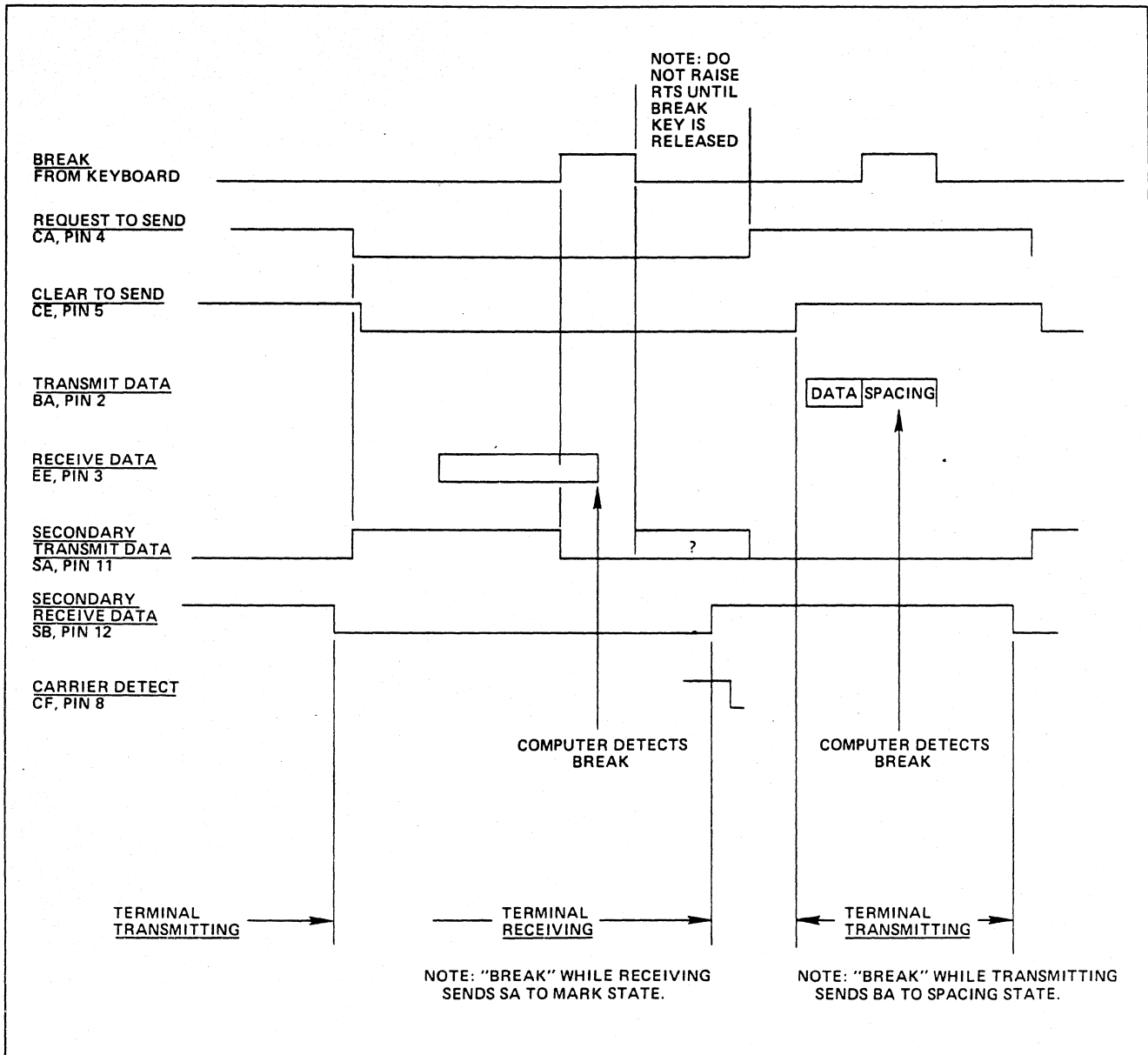


Figure 4-17. Interface Timing for Reverse-Channel Operation

at the grid and is varied by the brightness control.

VERTICAL DEFLECTION

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116 and Capacitors C105 and C106 form an RC network providing proper timing.

When power is applied, C105 and C106 charge exponentially through R115 and R116 until the voltage at the junction of R116 and C105 equals the anode "A" firing voltage. At this time, one of the unijunction's diodes that is connected between the anode and anode gate "G" becomes forward biased allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R120.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter. Therefore, the changing of firing points from one device to another, together with the temperature dependency of this parameter, is no longer a problem as it can be with conventional transistors.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113. At the time of the vertical interval, an external negative pulse is applied through R113, C104, and CR101 to the gate of Q102, causing the firing level of the unijunction to decrease.

The sawtooth voltage at the anode of Q102, is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104.

The output waveform from the unijunction oscillator is not suitable, as yet, to produce a satisfactory vertical sweep. Such a waveform would produce severe stretching at the top of the picture and compression at the bottom. C105 and C106 modify the output waveform to produce satisfactory linearity. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope. Slope change rate is determined by the position of the variable resistor R121.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power type transistor which operates as a class A amplifier. No output transformer is required since the output impedance of the transistor

permits a proper impedance match with the yoke connected directly to the collector. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

HORIZONTAL DEFLECTION

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. The circuitry associated with Q105 and Q106 has been designed to optimize the efficiency and reliability of the horizontal deflection circuits.

A positive going pulse is coupled through R127 to the base of Q105. The amplitude and duty cycle of this waveform must be as indicated in the electric specifications (Section 1.2) for proper circuit operation.

The drive stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driver Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

The horizontal output stage has five main functions: to supply the yoke with the correct horizontal scanning currents; develop a "C" VDC supply voltage for use with the CRT; develop a "B" VDC supply voltage for the video output stage; and develop a "D" VDC for the CRT bias.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, also serves to block DC currents through the yoke and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not describe the same arc.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by CR110. This produces

approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12 kV (9 and 12 inches) or 9 kV (5 inches), "C" VDC, and "B" VDC respectively. 12 kV or 9 kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier Q101.

LOW VOLTAGE REGULATED SUPPLY

All models use a series-pass, low voltage regulator designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240 V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VDC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

Operation of this regulator may be better understood by assuming a certain operation condition has caused the output voltage to increase above normal. This positive increase of voltage is transferred to the base of Q202 where it is compared to the zener of VR201. The increase of forward bias of Q202 causes the collector voltage to drop as a result of the increased collector current through R202. This voltage is directly coupled to the base of Q1 through Q201 where it causes Q1 to conduct less and brings the regulated voltage back to its proper state.

The short circuit protection or current limiting action can be explained as follows. Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of Q202 turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on. Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector voltage of Q203 which is detected by the base of Q201 and direct-coupled to the base of Q1 causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition. Circuit breakers and fuses are not fast enough to protect transistors.

4.3.20 ADM 3A Answer Back

The ADM 3A answer back option provides the transmission of a predetermined message of up to 32 characters in length. This message can be sent by depressing the "here is" key on the keyboard or by the computer command "ENQ". The message is stored in a read only memory (ROM) and is supplied at time of purchase. This message can be exchanged by LSI customer service.

4.3.21 ADM 3A Extension Port Current Loop

The extension port of the ADM 3A provides an auxiliary port for interfacing other

peripheral devices in a loop through or daisy chain environment.

The addition of current loop to this port adds to the flexibility and allows more devices to hook up in this manner.

The transmitted data output for current loop is on pin 25 of connector J-2 and does not supply current (external source). Received data is inputted on pin 2 and is internally grounded (Terminal ground).

4.3.22 ADM 3A Numeric Pad

The numeric pad option (figure 4-18) provides 14 keys for operator convenience. These keys consist of 10 numeric (0-9), 3 punctuation (-,.) and an "Enter" key. The codes associated with these are transmitted as such with the exception of "Enter" which transmits the ASCII character "RETURN".

Note

The numeric keys on the Key pad parallel the numeric on the standard Keyboard, therefore, if the shift key is depressed when using the keypad, the shifted characters will be generated as on the standard keyboard.

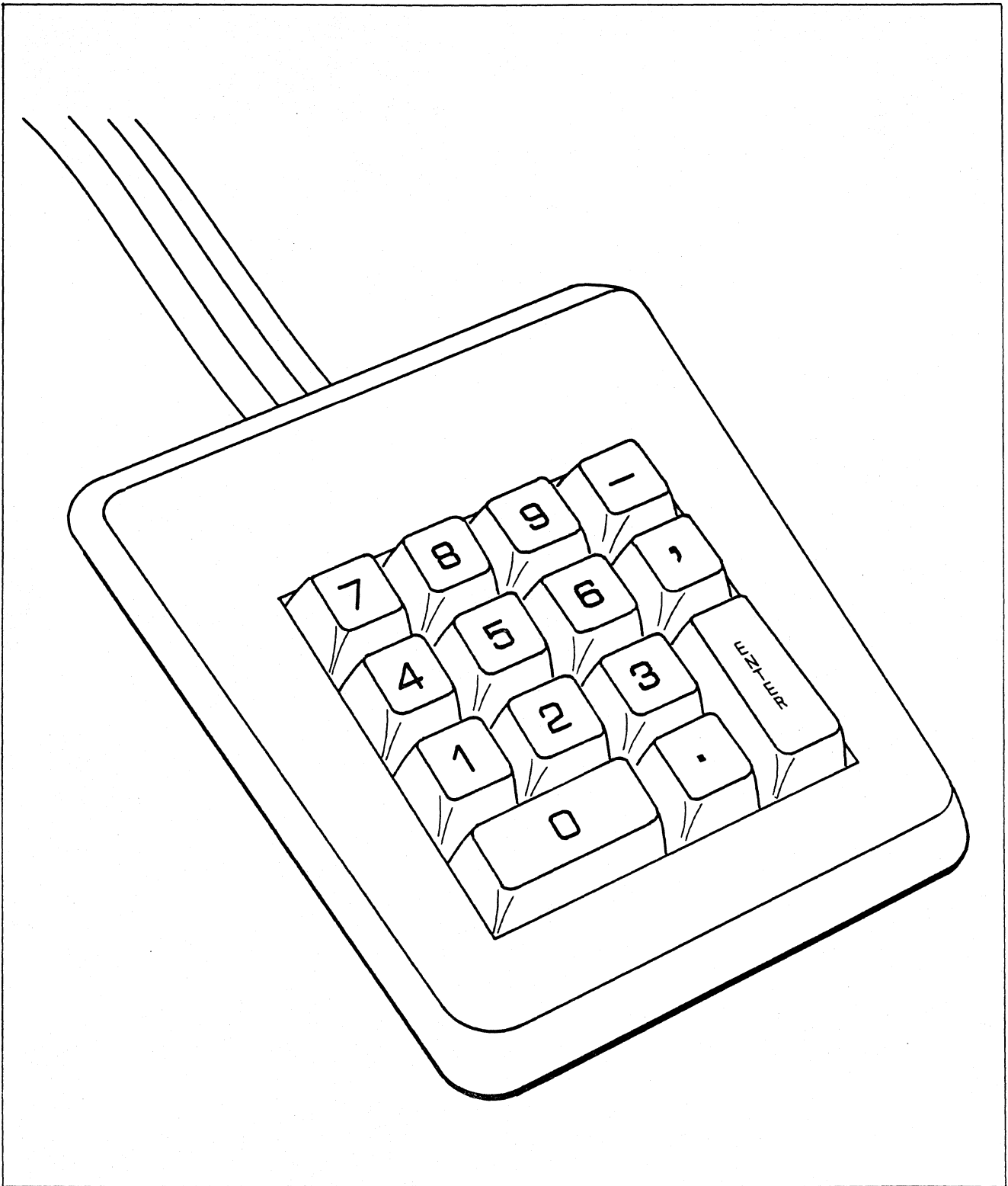


Figure 4-18. ADM 3A Numeric Key Pad

SECTION V MAINTENANCE

5.1 GENERAL

This section contains instructions and information for performing routine and corrective maintenance of the ADM 3A. It is assumed that the maintenance technician is thoroughly familiar with information in Section 1 and 4 of this manual.

5.2 INSTALLATION

It is assumed that the ADM 3A has been installed and set-up for operation in accordance with procedures outlined in Section 2. Any operating problem following installation should be approached initially by checking settings of internal switches and front panel switches located under the identification plate, and checking interface cables. Figure 5-1 shows assignments of terminals in interface connectors J1 and J2.

5.3 ROUTINE MAINTENANCE

The operator is expected to keep the exterior of the ADM 3A clean. The case should be cleaned using a household cleaner and a soft, damp lint-free cloth or paper towel. NEVER use a petroleum-base solvent such as lighter fluid which could damage the plastic or painted surface.

Be careful not to wipe dust into the keyboard, and don't let excessive spray cleaner run between the keys.

Other than cleaning, the ADM 3A needs no routine maintenance.

5.4 OPENING ADM 3A COVER

To remove the cover of the terminal (along with the monitor CRT) for access to adjustments or for other maintenance, proceed as follows:

- a. Remove the two phillips head screws located under the front corners of the terminal base.
- b. Lift the cover from the front, lifting it upward and rearward until it is lowered to rest on the table.
- c. To remove the cover from the base, disconnect the cable connecting the monitor to the printed circuit board, slide the cover toward the left on its hinge pins, and then remove the cover from the base.

Note

Note that all components on the ADM 3A circuit board are accessible for inspection and voltage measurement when the cover is fully open.

5.5 ADJUSTMENTS

All adjustments in the ADM 3A are associated with the CRT monitor.

5.5.1 Contrast Adjustment

Contrast may be adjusted for best viewing by the operator. The control is located at the upper right-hand corner of the keyboard.

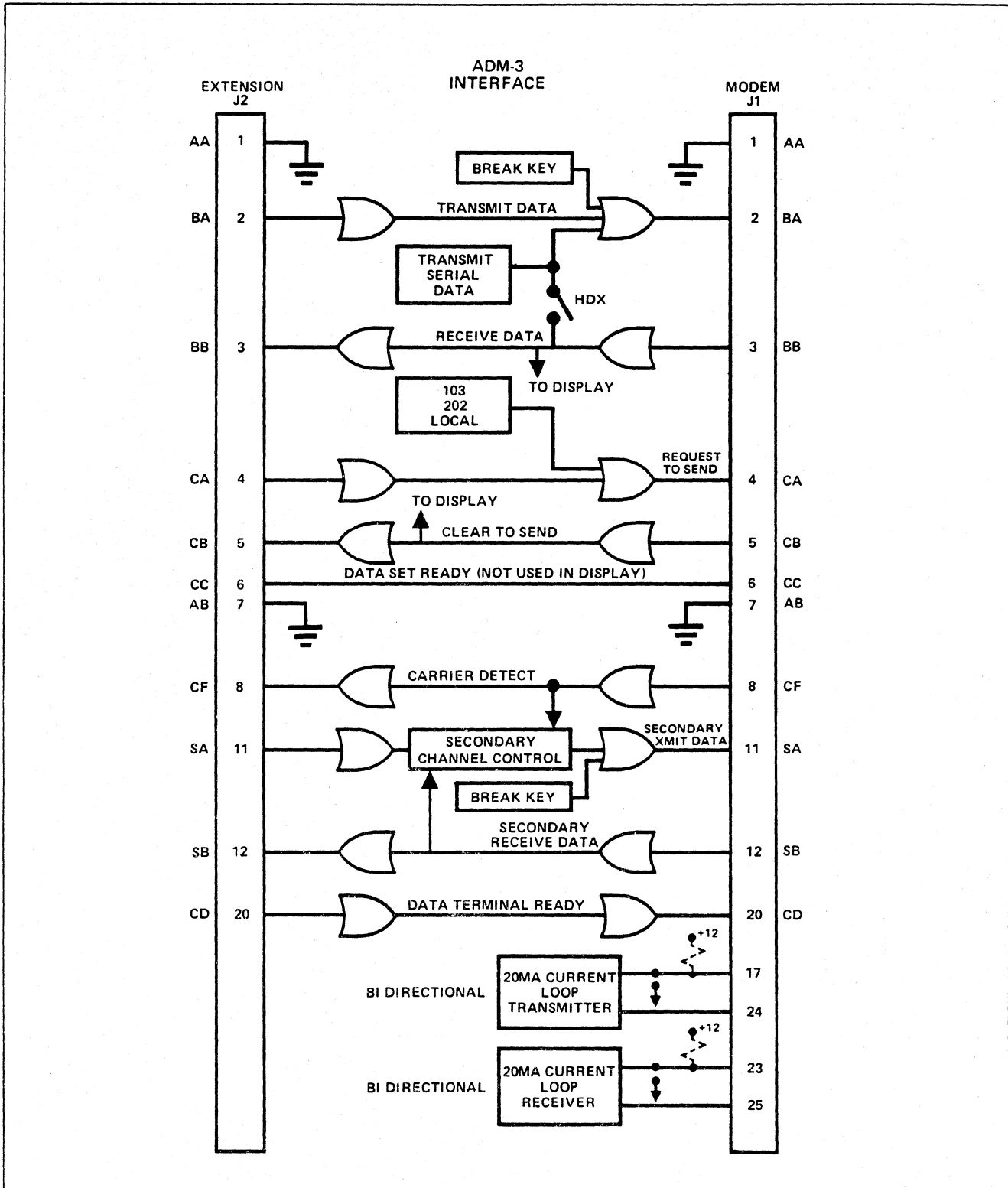


Figure 5-1. Interface Connector Terminal Assignments

5.5.2 Brightness Adjustment

The brightness (background intensity) control is located on the video board assembly within the ADM 3A cover.

WARNING

Brightness must be adjusted with power applied to the ADM 3A. To avoid hazardous electrical shock, adjust using a non-conductive screwdriver and considerable care.

Adjust brightness just to the level at which the white raster is extinguished. The optimum contrast can then be obtained when a video signal is applied.

5.5.3 Vertical Adjustment

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

- a. Apply video and synchronization signals to the monitor.
- b. Set the vertical frequency control (R116) near the mechanical center of its rotation.
- c. Adjust the vertical height control (R124) for desired height.
- d. Adjust the vertical linearity control (R121) for best vertical linearity.
- e. Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.
- f. Readjust the vertical frequency control (R116) until the picture rolls up slowly.
- g. Restore vertical drive to the monitor.
- h. Recheck height and linearity.

5.5.4 Horizontal Adjustments

Raster width is affected by a combination of the low voltage supply, width coil L101, and

the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

- a. Apply video and synchronization signals to the monitor. Insert the horizontal linearity sleeve about 2/3 of its length under the yoke. (If you received a monitor from the factory in which the placement of the linearity sleeve has been determined, make a mark on the sleeve and reinsert the sleeve to this mark when removal of the yoke and linearity sleeve are required.)

If the linearity sleeve is inserted farther than necessary, excessive power will be consumed and the horizontal output circuitry could be overstressed.

- b. Adjust the horizontal width coil (L101) for the desired width.
- c. Insert the linearity sleeve farther under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.
- d. Readjust L101 for proper width.
- e. Observe final horizontal linearity and width, and touch up either adjustment if needed.

No horizontal hold control is used in this monitor.

5.5.5 Focus Adjustment

The focus control (R107) adjusts best overall display focus. However, because of the construction of the gun assembly in the CRT, this control does not have a large affect on focus.

5.5.6 Centering

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

Do not use ring magnets to offset the raster from its nominal center position; this will degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

5.6 CORRECTIVE MAINTENANCE

Corrective maintenance consists of locating the cause of a malfunction and repairing it. The cause may be isolated only to the module level, with the failed module sent to a repair facility or returned to Lear Siegler for repair or replacement; or the user may choose to isolate the cause to the component level and replace the failed component.

Repairs at the component level should not be attempted except by trained personnel using suitable tools and test equipment.

5.6.1 Failure Analysis

Troubleshooting of the ADM 3A is straightforward and conventional. Suggested steps in troubleshooting are:

- a. **Get the facts.** Learn the state of the machine when the malfunction occurred. Look for operator error, blown fuses, or modem or computer failure.
- b. **Operate the ADM 3A to determine which functions have failed.** For example: Does it receive but not transmit? Has a single function (like Clear Screen or Backspace) failed? Intelligent use of this information will speed fault isolation.
- c. **Isolate the cause of the failure to a specific modulo** (for example, to the CRT, a keyboard row, the flyback assembly, or the main circuit board).
- d. If the failed module is to be repaired at the machine site, **further isolate the cause to a failed component** (or components). Refer to information in Section 4 and to the logic and assembly drawings in Section 6 of this manual.
- e. **Replace the failed module or component and test** by running the ADM 3A in the same mode of operation in which the failure occurred.
- f. **Record the symptoms, cause, trouble-shooting procedure, and mode of repair** for future reference.

Following are useful ideas to speed troubleshooting and repair:

- a. After warmup, the cursor should appear at its "home" position. If it does not, enter data from the keyboard (with the HDX/FDX switch in the HDX position) and see if it appears on the screen. If it does not, proceed to check power supply voltages, intensity and contrast control settings, clock and display counter operation, monitor sweep drive signals and monitor video and drive circuits, in that order.
- b. To verify operation of transmitter logic, simply see that data generated at the keyboard appears on the screen (HDX/FDX switch in the HDX position only!). This checks all transmitter logic except the inverter B7-10 and driver A9-3. To check FDX, create a short in pins 2 and 3 of the modem connector. This will also check the inverter B7-10 and the driver A9-3.
- c. It is possible to use internal turnaround switches (LOCAL, 103 and 202) to force Request to Send to either state, or put it under ADM 3A control. Intelligent use of these switches, and reference to **paragraph 4.3.16**, may simplify interface troubleshooting.

5.6.2 Troubleshooting the Monitor

Following is a guide to troubleshooting the CRT monitor. It is assumed that sweep drive and video signals from the main circuit board are normal (see **figure 5-2**).

- a. **Screen is dark.** Check settings of brightness and contrast controls. Check +15V dc supply at junction of R114 and R130. Check security of all monitor connectors.
- b. **No video.** Check setting of contrast control, check Q101 (refer to monitor schematic diagram in Section 6 of this manual).
- c. **Overheating** and excessive power consumption. Check horizontal linearity sleeve (**paragraph 5.5.5**). Check Q105 and Q106.

Refer to the monitor voltage waveforms (**figure 5-3**), and component layout (**figure 5-4**), and to cabling and schematic diagrams in **Section 6** of this manual.

5.6.3 Removing and Replacing Monitor CRT and Subassemblies

WARNING

Be sure to discharge anode voltage to ground before attempting to remove any monitor subassembly or CRT.

The monitor comprises the CRT with its steel mounting frame, the flyback assembly, and the circuit board.

To remove the CRT, proceed as follows:

- a. Unhook (at both ends) the spring that lies across the CRT.
- b. Remove connector from the base of the CRT.
- c. Remove the anode connector from the lower surface of the CRT.
- d. Using a socket wrench or screwdriver, loosen the clamps at both sides of the CRT frame until the clamps can be turned to clear the CRT frame.
- e. Grasping the CRT securely, lift it upward and out of the ADM 3A cover and set it aside.

To install a new CRT, follow the preceding steps in reverse order.

To remove the flyback assembly, proceed as follows:

- a. Disconnect anode connector from CRT.
- b. Disconnect Molex connector that connects flyback assembly to the monitor circuit board.
- c. Using a screwdriver, loosen the hex-head screw that clamps the flyback assembly to the molded cover.
- d. Lift flyback assembly upward until the screw clears the slot in the mounting plate, then remove assembly from the cover.

To remove the monitor circuit board, proceed

as follows:

- a. Remove the flyback assembly (refer to preceding steps).
- b. Disconnect all Molex connectors from the monitor circuit board.
- c. Slide circuit board from the slots in the molded cover and remove.

To replace monitor circuit board and flyback assembly, perform the preceding steps in reverse order.

5.6.4 Troubleshooting the Main Circuit Board

Troubleshooting of the main circuit board is based essentially on the principles outlined in **paragraph 5.6** — that is, the technician must be familiar with the theory of operation (**Section 4**) and must be equipped with suitable test equipment.

With the ADM 3A cover opened, all components on the main circuit board are accessible to probes and other test devices. Components are generally identified on the board; but reference may be made to the component layout drawing, and the logic diagrams in **Section 6** of this manual.

Table 5-1 lists connectors on the board and defines all terminal assignments.

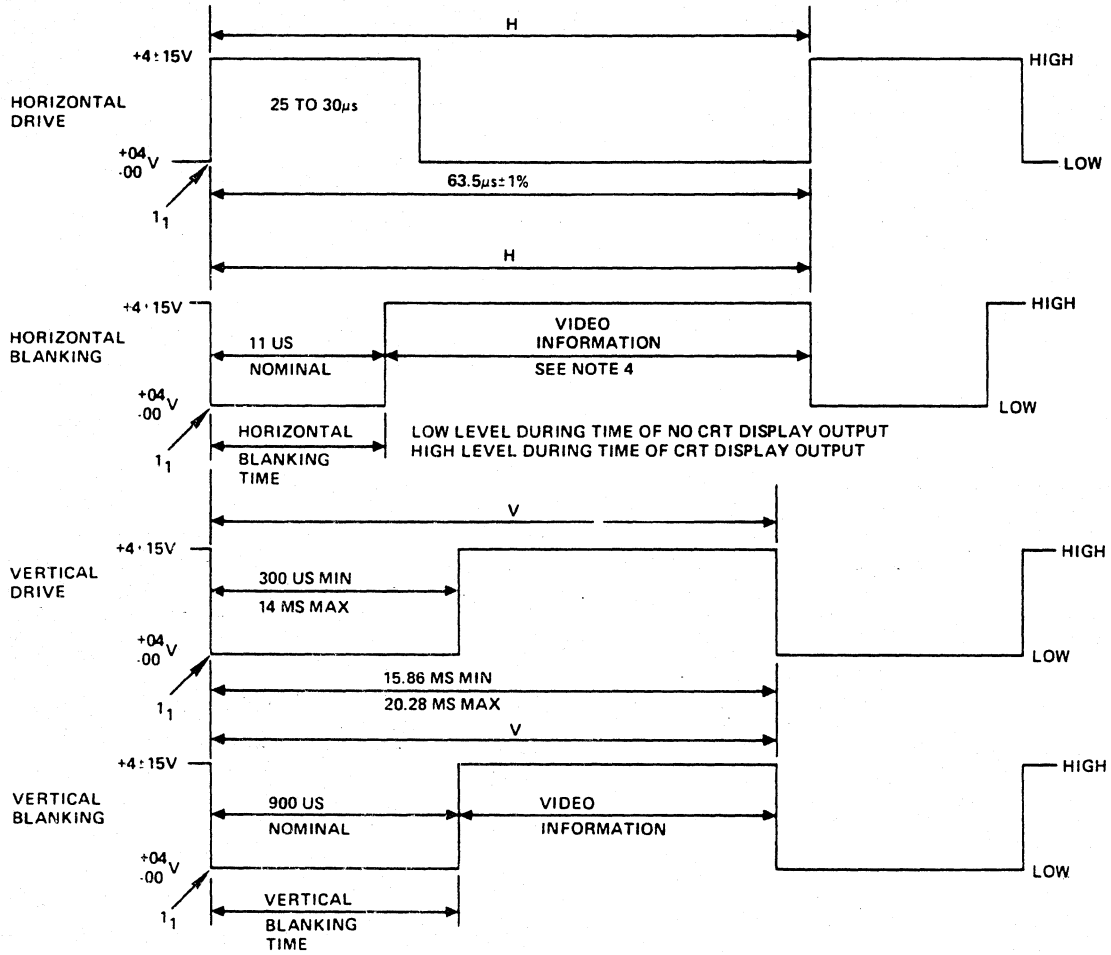
5.6.5 Removing and Replacing the Main Circuit Board

To remove the main circuit board, proceed as follows:

- a. Remove external cables from connectors J1 and J2 at the rear of the ADM 3A.
- b. Remove all cable connectors from the upper surface of the circuit board.
- c. Lift circuit board straight upward to clear the guide pins, then remove from the base.

Note that there are no fasteners to hold the circuit board, which is kept in place by the two steel guide pins and the closed cover.

Replace the circuit board by performing removal procedures in reverse order.

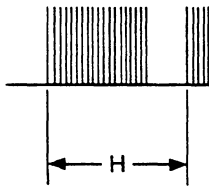


NOTES

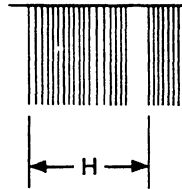
1. The leading edges of Drive and Blanking waveforms must start at time t_p . Nominal Blanking times should be observed.
2. H = time from start of one line to start of next line.
3. V = time from start of one field to start of next field.
4. Video pulse width should be equal to or greater than 100 nsec.

Figure 5-2. Inputs to Monitor, Timing Diagram

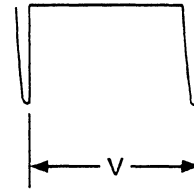
WAVEFORMS



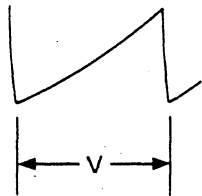
Q101-B
2.5V P-P



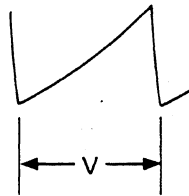
V1-CATHODE
20V P-P



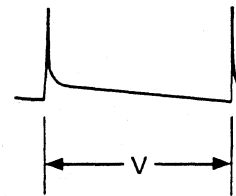
CR101-ANODE
3V P-P



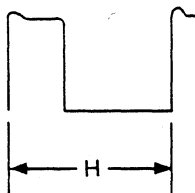
Q103-B
4.5V P-P



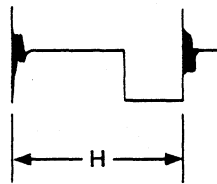
Q104-B
1.2V P-P



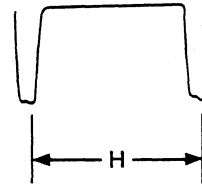
Q104-C
45V P-P



Q105-B
3V P-P



Q105-C
30V P-P



Q106-C
170V P-P

Figure 5-3. Monitor Voltage Waveforms

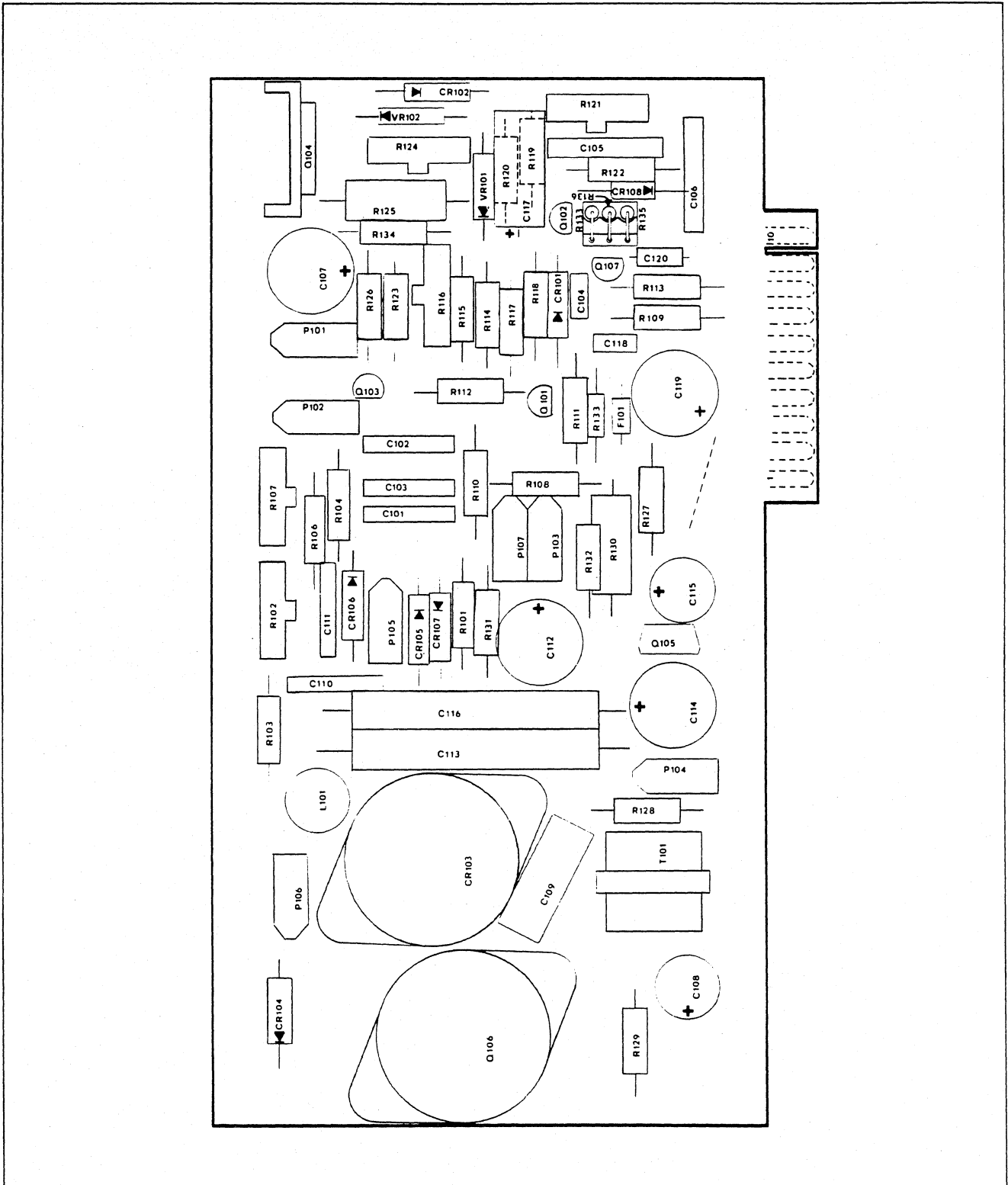


Figure 5-4. Monitor Video Board, Component Layout

Table 5-1. Main Circuit Board Connector Terminals

Connector/Symbol	Pin	Signal
RS232 Interface (J1)	1 2 3 4 5 6 7 8 9,10 11 12 13-16 17,24 20 18-22 23,25	Frame Ground BA (Transmit Data) BB (Receive Data) CA (Request to Send) CB (Clear to Send) CC (Data Set Ready) Signal Ground CF (Carrier Detect) (not used) SA (Secondary Transmit Data) SB (Secondary Receive Data) (not used) Current Loop Transmitter CD (Data Terminal Ready) (not used) Current Loop Receiver
RS232 Extension (J2)	1 2 3 4 5 6 7 8 9,10 11 12 13-19 20 21-25	Frame Ground BA (Transmit Data) BB (Receive Data) CA (Request to Send) CB (Clear to Send) CC (Data Set Ready) Signal Ground CF (Carrier Detect) (not used) SA (Secondary Transmit Data) SB (Secondary Receive Data) (not used) CD (Data Terminal Ready) (not used)
Low-Voltage AC Power (J3)	1,2 3,5 4	Input to +5V dc rectifier Input to +12V dc rectifier Ground
Monitor Low-Voltage AC Power (J4)	1,2	Input to +15V dc rectifier
Beep Speaker (J5)	1,2	Drive to beeper speaker
Keyboard Interface to 10-Key Pad (J6)	2,3,16 5,9,10 11,12,13 14,8,7 5,1,15,4	Col 3, 2, 0 Row 0, 1, 2 Row 3, 4, 5 Row 6, 7, 8 Row 9, C, D, E
Monitor Interface (J7)	1 2 3 4 5,6,7 8 10 11	Video to monitor Ground Horizontal drive to monitor Ground +15V dc to monitor

5.6.6 Removing and Replacing Key Switch Contacts

The tools required to remove the key switch contacts from the keyboard are:

insertion tool and guide
soldering iron (low temperature)
wicking device
short-nosed needle nose pliers
with serrated jaws

The procedure is as follows:

- a. Remove the solder from the contact (dewick) with a low-heat soldering iron so as not to damage circuit pads. The contacts will protrude about 1/32 inches beyond the back of the logic board. Make sure that the contacts are completely free of any solder by brushing them with your finger, the contacts should move freely.
- b. Turn the board over so that the keyboard is up.
- c. Remove the key top whose contacts need to be replaced.
- d. With the pliers, firmly grasp the plunger in the corner (see **figure 5-5**). Pull straight up with a firm pull.

CAUTION

The plunger is fragile; pulling to the side can break plunger or housing.

- e. Remove the spring.
- f. With the pliers, grasp the contact and pull vertically; remove both contacts.
- g. Place the insertion tool guide in the switch housing making sure that the keyway is toward the front of the keyboard (See **figure 5-6**.)
- h. Insert the solid contact (P/N 373-30052-2) in the insertion tool with the bend to the outside and the solder end up (see **figure 5-7**). Insert the split contact (P/N 373-30053-2) with the split end in first (see **figure 5-8**).
- i. Place the insertion tool into the guide matching keyway slot and key. Press the

tool firmly straight down until the contacts are seated firmly (the tool clicks). (See **figure 5-9**.)

- j. Remove the tool and the guide.
- k. Replace the spring.
 - l. Replace the plunger making sure that the bar is parallel with the contact opening. Work the plunger down slowly, separating the contacts with the crossbar of the plunger (see **figure 5-10**).
 - m. Press the plunger firmly down until it is seated (it clicks).
- n. Replace the key top.
- o. Turn the board over and verify that the contacts extend about 1/32 inch past the board.
- p. Resolder the contacts in place.

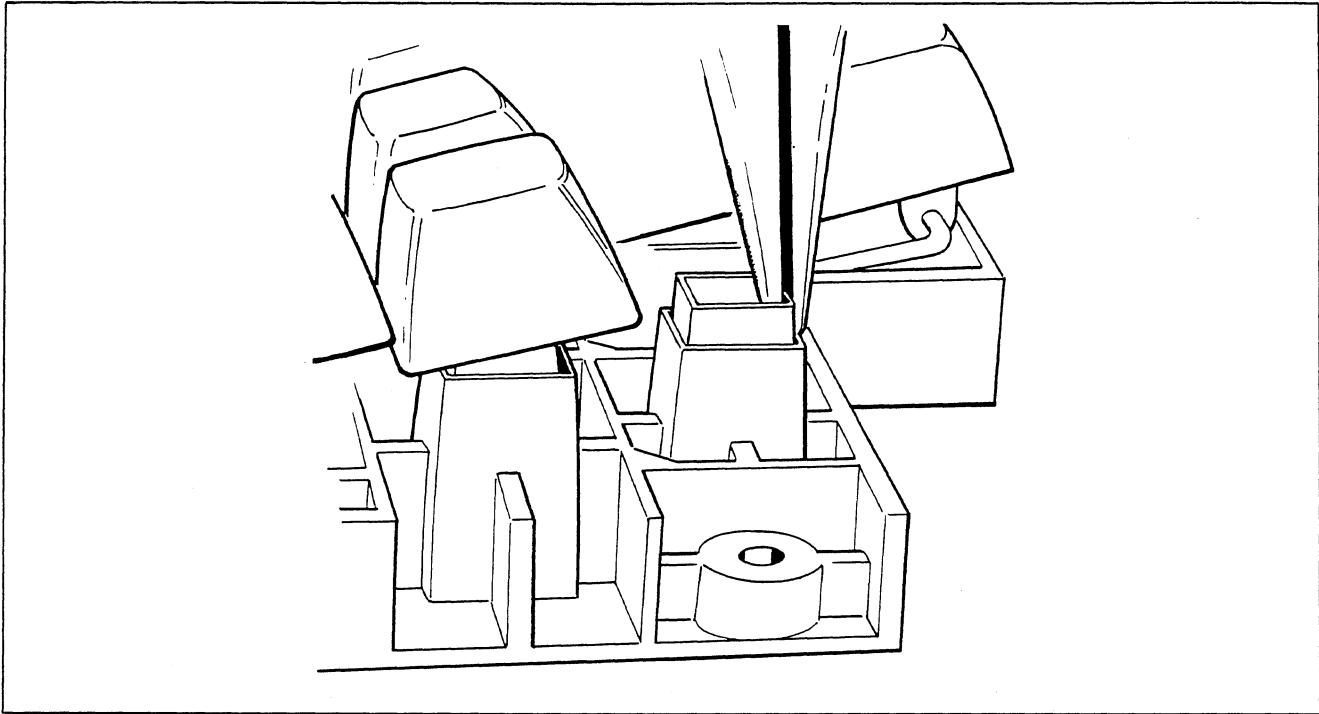


Figure 5-5.

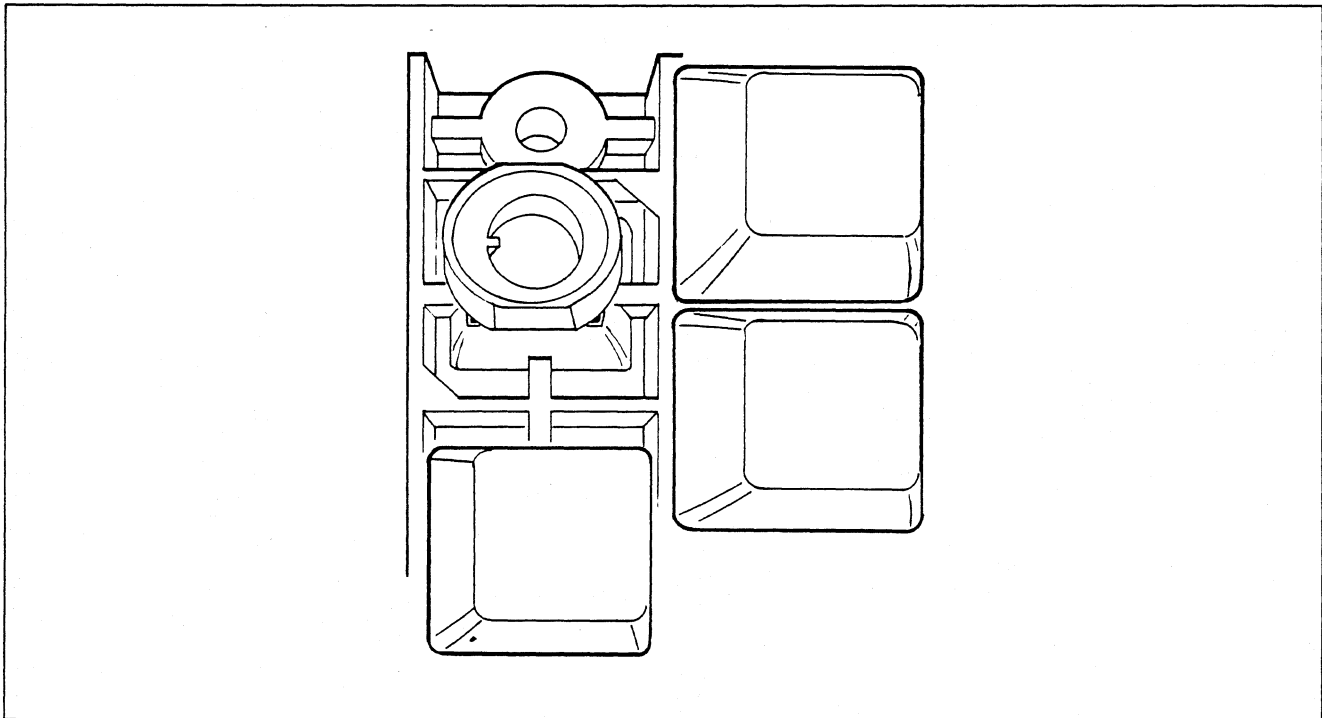


Figure 5-6.

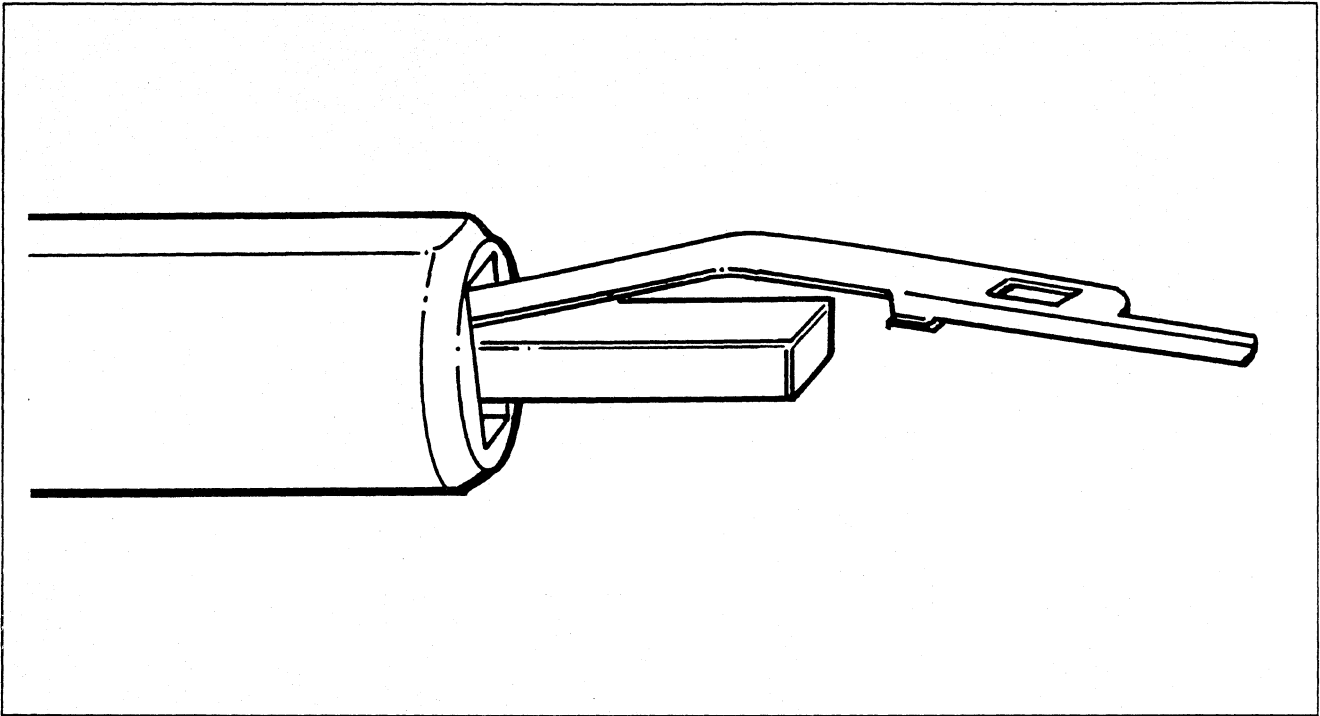


Figure 5-7.

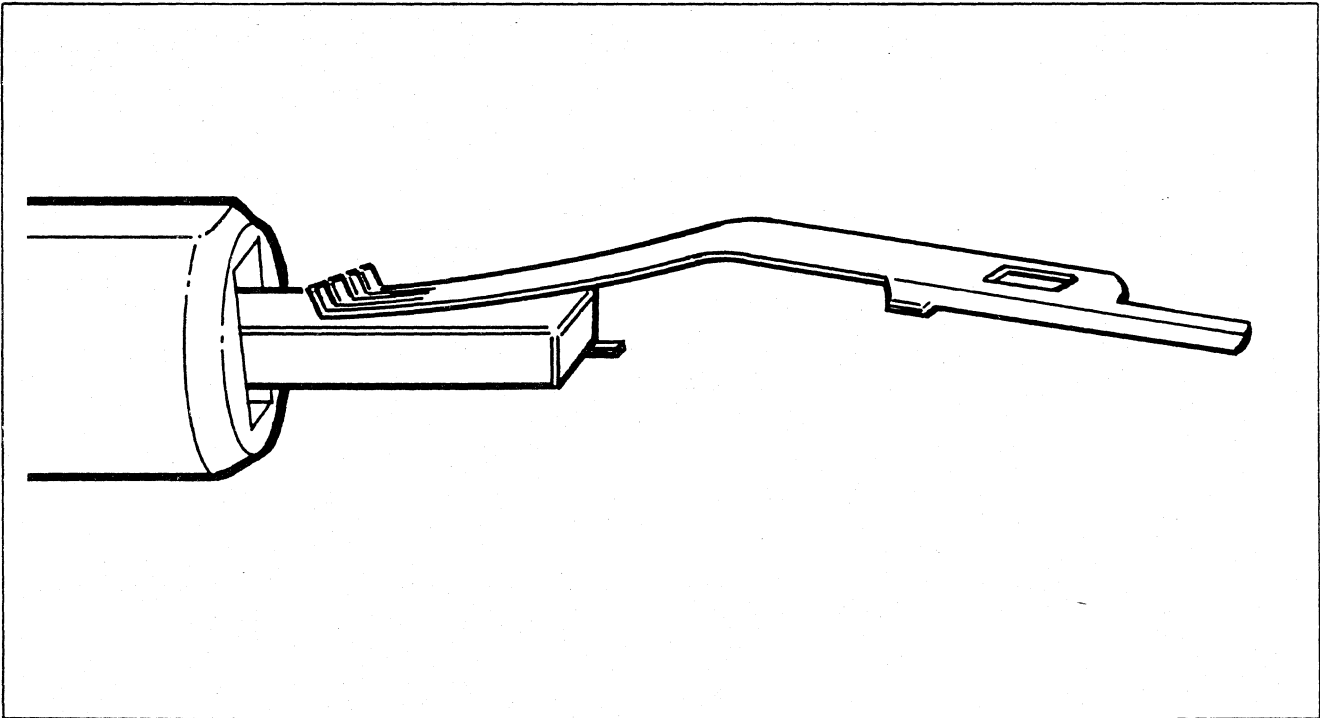


Figure 5-8.

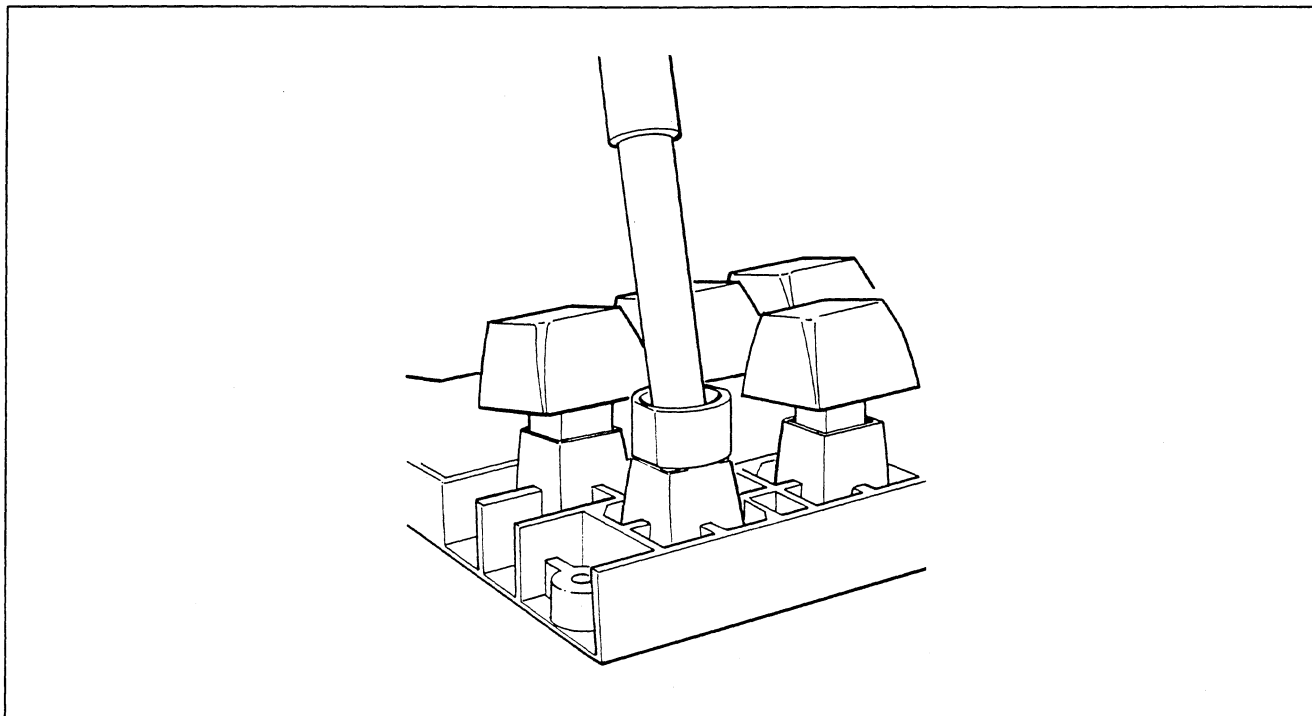


Figure 5-9.

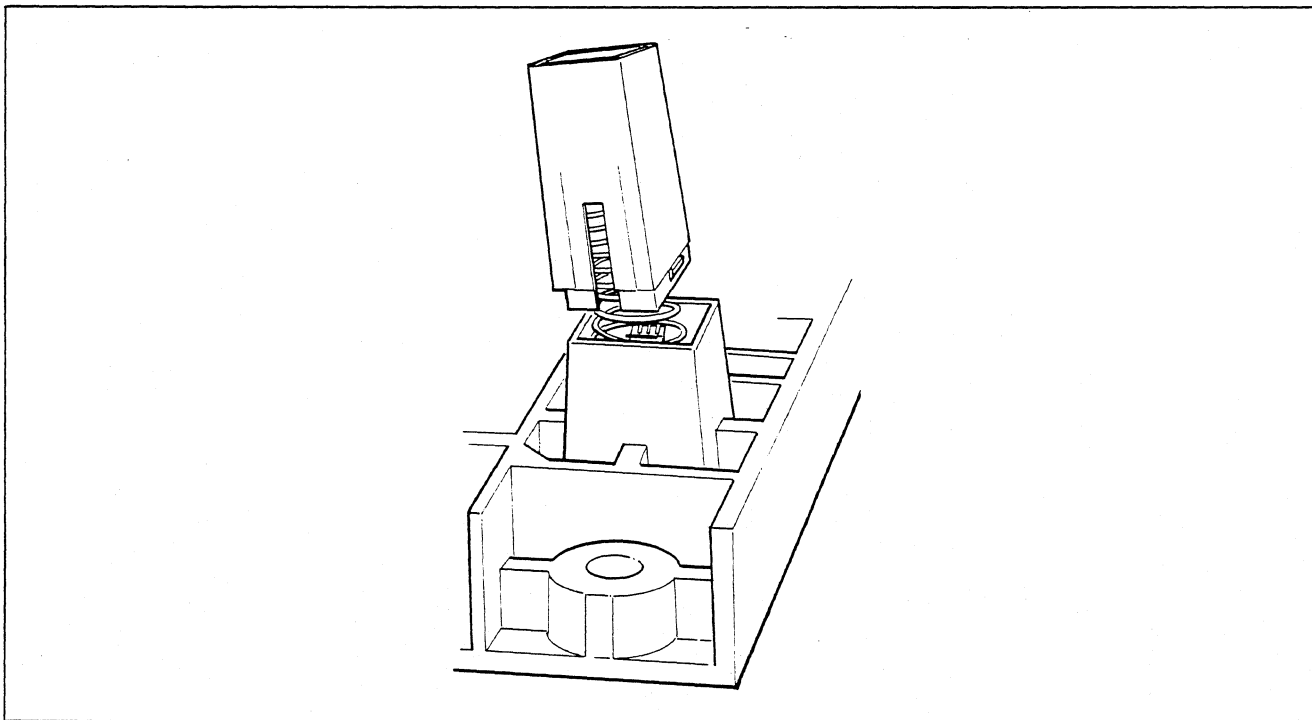


Figure 5-10.

SECTION VI DRAWINGS

This section contains drawings of the functional areas of the ADM 3A as well as a technical description of the logic in each area. The basic logic was presented in Section 4 (Theory of Operation).

6.1 SCHEMATIC SHEET #2 - SYSTEM COUNTERS

The oscillator located in zone D4 provides the basic clocking for the entire display unit. It oscillates at a frequency of 10.8864 MHz (period = 91.8577 nsec.) which is twice the frequency of the video going to the monitor. This clock also goes to the DOT counter which counts the seven dot positions horizontally in a character position. This DOT counter (74LS161 - zone D2) has seven different states. It begins its cycle by presetting to a count of 10, counts through the overflow at 15, and presets again at a count of 0. The purpose of this counter is to time the presentation of the sequential addresses to the character generator and the presetting of the video serializer. Its final output, $\overline{DC3}$, has a duty cycle of 85.7% and a frequency of 1.5552 MHz. It also is the clock to the next counter in line.

The CHARACTER counter (zone C3) has eight stages and is used to time the positioning of the eighty characters and the horizontal retrace time along one video raster line. The total division provided by this counter is 96, 80 for the video portion of the raster line and 16 for the horizontal retrace. The actual count goes from 0 to 79, presets to 240, and counts out to the overflow point at 255 and restarts another cycle for the next raster line. Stages labeled CC0 through CC6 are straight binary counts while CC7 actually

has a weight of 80. This means that all CHARACTER counter decodes less than 80 have CC7 low and all decodes 80 and higher have CC7 high. In practical usage, CC7 low indicates that the unit is operating in the video portion of the raster and CC7 high indicates horizontal retrace time.

The flip-flop labeled $\overline{ICC80}$ (zone C2) actually represents the decode CHAR COUNTER = 80 or one count into the horizontal retrace. This term is utilized internally to indicate the time when a command received from the normal I/O interface can be acted upon. The \overline{LCCLK} circuit (zone B1) provides the clock for the following counter.

The next counter is the LINE counter which counts the raster lines in one row of characters. This counter divides by nine and is a straight binary count. Counts 0 and 8 indicate the two raster lines vertically between two rows of characters while counts 1 through 7 are the raster lines during which the video is being generated. The final stage out of this counter provides the clock for the row counter and has a frequency of 1.800 kHz.

The ROW counter (zone A2) is a variable counter. Its purpose is to count the rows of characters appearing vertically down the screen. It also counts through the vertical retrace time. Its count changes from a division by 30 for 60 HZ refresh to a division by 36 to 50 HZ refresh. The 50/60 HZ switch is positioned according to the frequency of the primary input power line. The ROW counter progresses in a straight binary fashion up to its selected maximum count and presets to zero.

The tri-state buffers (74LS125) located in zones D3, C4 and A4 are for use of the automatic test equipment and essentially have no effect on the normal operation of the display unit.

6.2 SCHEMATIC SHEET #12 - INTERFACE CONTROL

This schematic essentially shows the request-to-send and clear-to-send operation for the ADM 3A. The flip-flop B2 (74LS74, zone D3) is the CLEAR TO SEND control flop. If clear to send is high at the RS232 level, then the UART transmit clocks are turned on and the unit can transmit at any time. If CTS falls during the time a byte is being transmitted, the ADM 3A will continue to transmit the remainder of that byte then shut down in the "marking" state.

There are four ways that REQUEST-TO-SEND can be controlled in the ADM 3A. First, RTS can be low all of the time which is accompanied by opening all three of the switches located in zone A2. Then RTS can rise before the transmission of that one character, and fall as soon as it clears the UART. This is done by closing the switch marked LOCAL. If the switch labeled 103 is closed, then RTS will be held high all of the time. A device setting on the extension port can also exercise RTS control through Pin 4 of connector J2. The last switch on this section is labeled "202". If this RTS CONTROL switch is closed, then one other selection must be made. The two choices are RTS control utilizing code turn-around and RTS under reverse channel control. This selection is made using switch in zone C4. If code turn is selected, then the actual code to be used must be specified. This is done by closing one of the two switches located on gate input J8-13 (74LS27, zone C4) which are labeled ETX or EOT. These are the only two selections provided for in the ADM 3A. When the selected code is received into the INPUT DATA BUFFER, this information is latched into flop B10-6 (74LS113, zone C3) labeled LATCHED CODE. This information is allowed to toggle flop C8-2 (zone B2) if CARRIER DETECT (zone B4) has gone low, indicating that the distant end has stopped transmission.

If another of the selected codes is then received, the unit will immediately switch to receive without waiting for carrier detect since our RTS was maintaining CARRIER DETECT high.

If reverse channel operation is selected, then the two inputs that control RTS are SECONDARY RECEIVE DATA and CARRIER DETECT (SB and CF respectively). If SB goes low, the ADM 3A will unconditionally switch to the receive mode (RTS low). If CF is also low, SECONDARY TRANSMIT DATA will go low. If CF is high, indicating that the distant end has turned on, SECONDARY TRANSMIT DATA (SA) will go high. This last condition is the normal receive condition in reverse channel operation. In order to switch to the transmit mode, the distant end controlling the terminal raises SECONDARY RECEIVE DATA (SB). Then, the only other condition that has to be met is that CARRIER DETECT (CF) must fall, indicating that the distant end has dropped its RTS. At that time, the ADM 3A will turn RTS on within 62 msec. In this reverse channel operation, if a command is given to turn RTS, then no further commands will be recognized for a period of approximately 250 msec. This gives the modem time to propagate its signals. This timing is accomplished with the counter and two flops. All controlling inputs and controlled outputs can be driven from the extension port.

6.3 SCHEMATIC SHEET #3 - CLEAR/ERASE LOGIC OFFSET COUNTER ROW COUNTER BEEPER CIRCUIT

6.3.1 Clear/Erase Logic

The Clear and Erase Logic (zones D1-D4, A1 & C4) performs the function of initializing the counters on power-up or other clear-screen operations and forcing a write-space action for a sufficient period to clear either a single line, or the entire screen. During power-up the functions CLEAR2 and CLEAR3 force flops F6-5 (START) and F6-10 (ERASEF) true, and flop K8-6 false. The latter functions, via gate C5-13, generates the signal $\overline{\text{CLROC}}$, which clears the Offset and Row Counters.

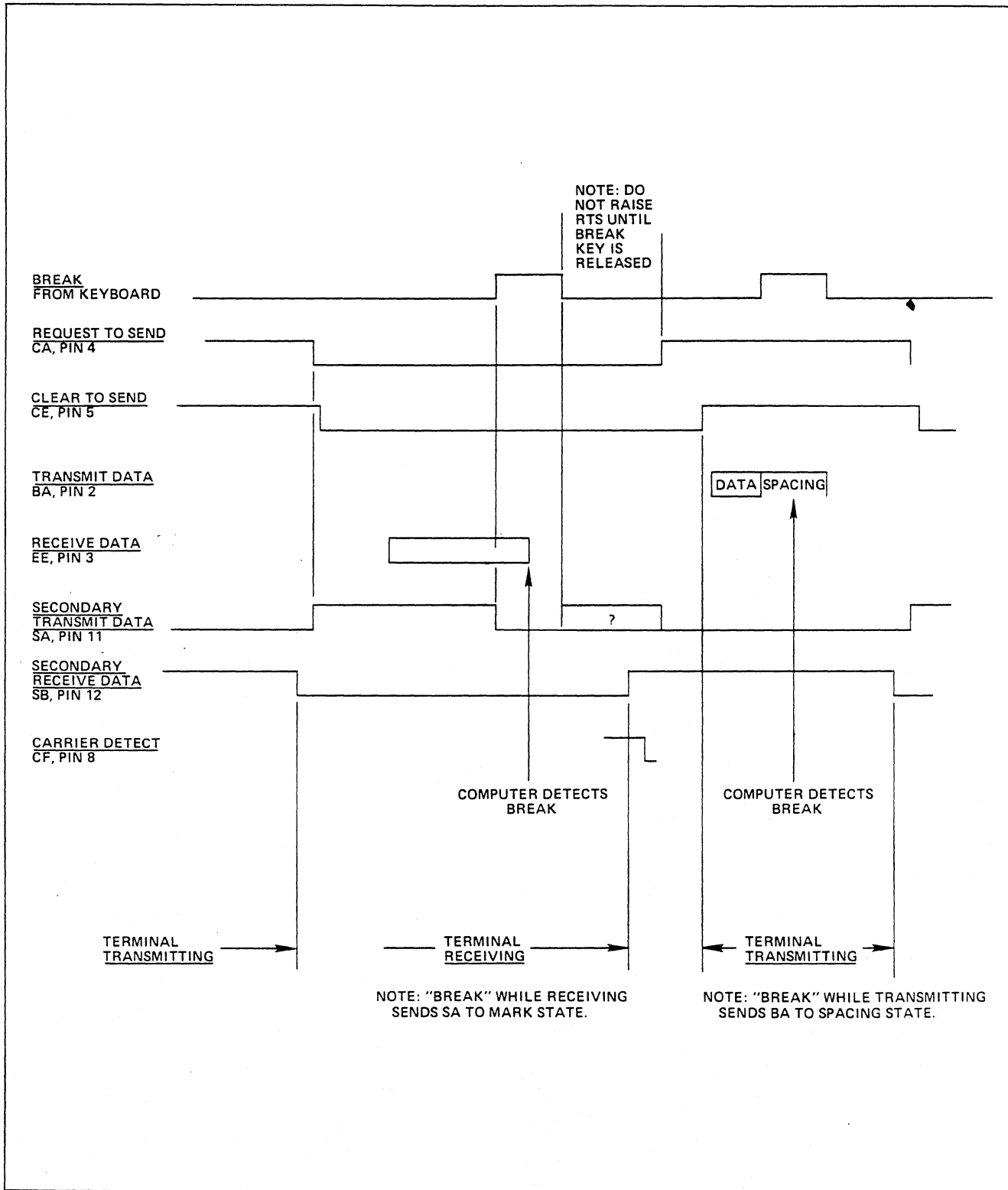


Figure 6-1. Interface Timing for Reverse-Channel Operation

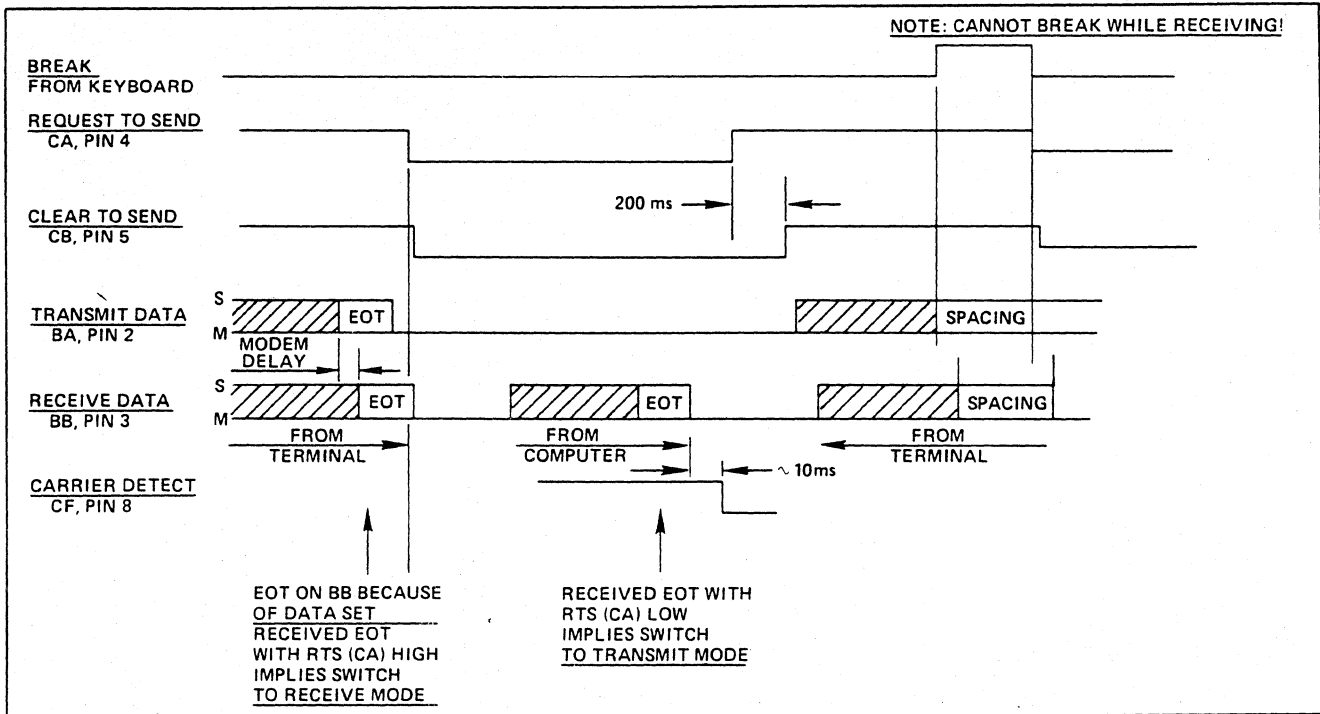


Figure 6-2. Interface Timing for Code Turnaround

If a key-clear (KEY CLR) operation is initiated from the keyboard, or a clear-screen command (CLR SCRN) is received, CLROC is generated directly, but the START and ERASEF flops are set in sequence by successive CC80A signals, the latter flop via the SETERA gate. The remaining erase function, which occurs when a line-feed is generated with the cursor on Row 23, does not affect the START flop. The SETERA signal, derived from CR23 and LF1, causes ERASEF to be set for one line-period. By the time the next CC80A signal occurs, LF1 will be false and START, also being false, will cause ERASEF to be reset. Gated with CC7 to form ERASE LINE, this function is used to clear the memory-row which was "rolled to the bottom" during a scrolling operation.

Clear-screen operations, however initiated, are terminated when the Offset Counter overflows, generating, OCLOD. The first CC80A signal after OCLOD resets START, and the next CC80A resets ERASEF. This action is necessary in order that memory-row 0 may be cleared.

6.3.2 Offset Counter

The Offset Counter and its associated logic (zones B1 and C1-C3) perform the dual function of defining the memory-row addresses during clear-screen operations and maintaining the scrolling history of the unit to facilitate the reconciliation of display row-positions to the physical memory-rows. Consisting of five counter stages (OC0-OC4), Row-23 detection logic (OCLOD) and Line-feed definition and vectoring logic (LF1, PGMOD, DNLIN EA), the OC will be enabled to react to line-feed directives whenever the unit is currently executing a clear-screen operation. (START TRUE) or the Cursor Row Counter (zones B2, B3) is in count-condition 23₁₀. In either situation, line-feeds derived either from START, LF (line feed command) or BOFLO (overflow from last column of the column-counter) will be translated in the term DNLIN EA, which will cause the OC to increment either one or two units, depending upon the position of the 12/24 Line-Select switch (zone A-3). In 24-line mode, OC0 will toggle at each DNLIN EA directive, with a

normal binary count propagated to the four upper stages of the counter. In 12-line mode, OC0 is forced true (odd-lines only) and each DNLINEA directive will then increment the upper stages one unit, causing an effective count-by-two operation. Whenever the value held in the OC reaches 23, OCLOD will become true, and the next line-feed will cause the counter to be loaded with a zero-count.

6.3.3 Row Counter

The Cursor Row Counter and its associated logic (zones A1-A4, B1-B4, D3 & D4) perform the task of maintaining the current display-row position of the cursor. Due to the mobility of the cursor, this counter is capable of being incremented, decremented, cleared or loaded with a code from the data-buffer which represents an absolute cursor row-position on the display. Like the Offset Counter, the Row Counter consists of five stages (CR0-CR4) capable of counting in the range 0 to 23; with the same provision for locking the LSB (CR0) into the true condition in 12-line mode, and counting module-2.

The Row Counter is allowed to increment in situations complementary to those for the Offset Counter, that is, when START is false and the row-count is other than 23. In these cases LF1, derived from the same three possible sources noted for the OC, will be translated into the Row Counter increment signal DNLINEB. One additional source of line-feed enabling is directed to the Row Counter, however, when the Cursor Control switch is open. In this situation, the Row Counter will increment continuously after START falls, until a count of 23 is reached. The counter will then be disabled so long as the switch is open (ENX false) and no further clear-screen operation are initiated. This characteristic of the counter effectively locks the cursor to the bottom row of the display, and directs all subsequent line-feeds to the Offset Counter.

If the Cursor Control switch is closed (ENX true), the upline and Load-Cursor functions will be enabled. The upline command signal, VT, will be invariably routed to the LSB of the Row Counter, as one of three possible clock-enabling terms (VT, LDROW, DNLINEB).

Unless CR0 is locked true by the 12/24 line select switch, it will toggle any time ESC2 is false; a situation which will occur at all times except during cursor-load operations. Decrementing the high-order (CR1-CR4) part of the counter will occur when either CR0 is false or the unit is in 12-line mode (DNSEL), and a VT command is issued.

The Row Counter may be cleared in one of four different situations. The first situation is that caused by one of the three clear-screen operations ($\overline{\text{CLROC}}$). The second case is that effected by a HOME command, permitted only when the Cursor Control switch is on. The third circumstance occurs whenever the counter is decremented past zero, in which case BORROW is used as a clock to set ROWCLR (zone D3). The last situation occurs whenever an attempt has been made to load an absolute row-count value greater than 23, causing the term $\overline{\text{R24/31}}$ to pull ROWCLR true. The jam-clear function is removed, either as the result of a DNLINEB (increment) signal, or during the load-row phase of a Load Cursor operation ($\overline{\text{LDROWEN}}$).

The Row Counter may be loaded to any value between zero and 23, provided the Cursor Control switch is on. The actual loading of row-data takes place during the third phase of the four-character sequence, defined by the condition when ESC1 and ESC2 are both true. In this situation, ROWCLR is reset, as described above, and a clocked load signal is directed to the LSB and four MSB's of the row counter ($\overline{\text{LDROW}} - \overline{\text{LDROWEN}} - \overline{\text{XCLK}}$). The information from the data-buffer, DATA1 - DATA 5, is then loaded into the counter.

6.3.4 Beeper Circuit

The circuits which produce an audible tone for operator signaling, are shown in zones C1-C2 & D1-D2, plus related gates at zones A2 & D1 of logic sheet 4. The duration of the tone is governed by the one-shot (zone C1) which is triggered either by receipt of a BEL code (BEL and CC80) or the occurrence of the LINE END function. The latter function occurs (see logic sheet 4) whenever the Cursor Column counter is advanced from column 71 to column 72. The frequency of the tone (3.6 KHz) is governed by

the modulating signal, LC2. The tone is cut off by clearing the one-shot (CLRBEL) whenever a READ operation is initiated, or an overflow (OVERFLOW) from the column counter occurs. The first case is necessitated by the fact that BEL is used in conjunction with the Read Back Enable function to initiate the readback operation; therefore, if the tone were not disabled in this situation, excessive noise would result during testing. The second situation is required, to prevent a continuous tone from occurring during high baud rate transmissions, since at rates higher than 2400 baud, re-triggering by the LINE END function would occur before the one-shot could normally time out.

6.4 SCHEMATIC SHEET #4 COLUMN COUNTER WRITE- PULSE LOGIC

6.4.1 Column Counter

The majority of the logic shown on sheet 4 (exclusive of zones D1-D4) is concerned with the task of managing the columnar position of the cursor. As described in the theory of operation, the counter is capable of being incremented, decremented, cleared and loaded with either one of two fixed position-codes or a code derived from data received via the UART and stored in the Data Buffer. Incrementing is effected in one of three ways:

1. As the result of a character-entry into memory.
2. As the result of receiving a Forespace (FF) command.
3. As the result of a start-transmit signal, when in the test-readback mode.

A forespace signal (FORESPACE, zone C1) will be generated for any character received, except Control character (CTRL CHAR), Delete codes (DEL) or characters which follow an Escape code, and constitute either part of the four-character sequence, or an illegal second-character. All possibilities excluded under the last classification are covered by the term NOLOAD, derived from ESC1 and ESC2. Evidence of receipt of a character is provided by the function XCLK,

which is derived from DOIT and CC80A. The Forespace command (FF) contains an implicit DOIT function, therefore, must only be combined with CC80A to form a properly gated signal (RTCURG) for direct ORing. The Readback increment (READ INC) function results from the transmission, rather than reception of a character, and therefore, is a combination of the Read-mode enabling signal (READ) and the initiate-transmit term (XLOAD). The Column Counter may only be decremented when a Backspace code (BKSP) is received by the unit. This function, containing an implicit DOIT gate, is fed directly to the count-down input of the counter.

The counter is cleared in one of four different situations. The first is occasioned by any of the Clear Screen operations (START), insuring that all post-clear action starts from the Home position. Receipt of either a Home command (HOME) or Carriage Return (CR) command will also clear the counter, however, the Home function is only recognized when the Cursor Control switch is on. The last situation which will elicit a counter-clear, is a decrement from Column-0. In this situation, the back-count will evoke a borrow (WC BORROW) from the counter, which is captured as UNDERFLOW, and used to force the counter back to column zero.

A multiplexor (zones C1-C4) is utilized in the Column Counter logic to control the source of data for loading into the counter. If the counter is incremented past column 79, the event is stored as OVERFLOW, and used to pulse the load-ports of the counter. The OVERFLOW term is also sent to the Offset and Row Counter increment logic, if the Auto-Newline switch is on. The information loaded into the counter by OVERFLOW, is also dependent upon the Auto-Newline switch, zero being loaded if the switch is on, and 79₁₀ if it is off. The multiplexor will always be switched to the A-ports during overflow processing, since the selection term (ESC2) cannot be true simultaneously with an increment (RTCUR) signal.

When a four-character cursor-load operation is initiated, the term ESC2 will be true during both the third and fourth phases, and will

switch the Column Counter Mux to the B-ports, enabling translated character-codes (DATA1 - DATA5, DATA6 & DATA67) to be loaded during the last phase (ESC1, ESC2, XCLK). The translation is required to allow the more common alphanumeric codes to be used, rather than control codes. Row codes in the range 0408 through 0678, and column code in the range 0408 through 1578 are translated, respectively, to codes in the range 0008 through 0278 and 0008 through 8878.

6.4.2 Write-Pulse Logic

Write pulses, which effect the storage into data-memory of the current contents of the Data Buffer, are generated by the logic in zones D1-D4, during two situations. One case is that precipitated by a line-erase operation (see SETERA, sheet-3) due to a clear-screen or scroll situation. In these circumstances, the term ERASE LINE will be generated during one or more complete line-scan periods, allowing 80 write-pulses to be enabled for each such period. In the second situation, a single write-pulse is enabled for each character clocked into the Data Buffer, as evidenced by the FORESPACE signal. The generation of a write-pulse, in this case, is conditioned by the presence of a SPACE code, and the position of the Disable Non-Destructive Space switch. If the switch is closed (disabled) a write-pulse will be enabled for every received character. If the switch is open, all SPACE codes encountered after a Carriage Return will cause inhibition of write-pulses, thereby preventing the entry of such codes into memory. The inhibit function will be cleared by the next Line Feed code.

The duration of the write-pulses is controlled by the write-clock (WRTCLK) flip-flop, which provides a pulse which occupies the last four dot-positions of each character period. The width, therefore, is 367 nanoseconds.

6.5 SCHEMATIC SHEET #5 - MEMORY ADDRESS GENERATION

The logic on this sheet provides four major functions related to the manipulation of the 1920 byte data memory address structure, to

facilitate data entry and data retrieval for display refresh. These functions are:

1. Reconciliation of the current cursor row-position with the scroll-history to generate a virtual entry-row address.
2. Reconciliation of the dynamic display row positions with the scroll-history, to virtual refresh-row addresses.
3. Selection of either entry or refresh row-address information in a manner consistent with the periodic demand requirements of the display.
4. Reconciliation of the 64 by 30 byte physical memory array with the 80 by 24 character array used by the display.

The generation of entry-row addresses is performed by a five-bit full adder set comprised of the elements in zones C4 & D2-D4. The adder combines the functions from the Cursor Row Counter (CR0-CR4) and those from the Offset Counter (OC0-OC4) in the manner:

$$\text{SUMW} = \text{CR} + \text{OC} + 1$$

The unit is added to the counter functions, in order that a unit in bottom-entry mode (cursor control switch off) will initially make access to row-address zero, consistent with the original ADM 3. If the Cursor Control switch is on, the memory-row initially available for data entry ("top row") will be row one. As the display is scrolled, and the Offset Counter incremented, the virtual row-address of each row, relative to the top-of-display will advance proportionately; for example, on a display which has been scrolled five times, with the cursor on the top row, the virtual entry row address will be six ($0 + 5 + 1$). As the cursor advances down the display, the contribution of the CR register to the sum will also increase. If the unit which was scrolled, as described in the example above, subsequently has its cursor moved the sixth row of the display, the virtual row address will be 12 ($6 + 5 + 1$).

The logic shown in zones D2 & D3 (SUM34W, SUM345W, SUM3WSC, SUM3WS, & SUM4WS) is charged with the task of reconciling the row sums from the CR & OC

adder, to an allowable address range of 0 to 23. This logic causes sums in the range 24-47 to effectively undergo a "subtract 24" operation.

The generation of refresh-row addresses is also performed by a five-bit adder and two-bit "range adjuster", comprised of the elements in zones A4, B4 and C2-C3. The second adder-set is functionally identified with the first, combining the contents of the Offset Counter (OC0-OC4) and the Refresh Row Counter (RC0-RC4) to form the sum:

$$\text{SUMR} = \text{OC} + \text{RC} + 1$$

As a consequence of this sum, a unit without scrolling history currently scanning along the top row of the display, will access row-address one, and as the scan progresses down the display, the indicated addresses will progress from 1-23, finally accessing row-address zero when the bottom row of accessing row-address zero when the bottom row of the display is being scanned. As the unit acquires a scroll-history, the virtual addresses will advance, relative to the display rows, with row-addresses previously associated with the top display-row rolled to the bottom and the contents erased, as described earlier. This procedure allows the data in memory to be visually advanced upward, row by row, without necessitating the actual relocation of that data in the physical memory.

In the same manner as that performed on entry-address sums, the row refresh-address sum (SUM0R-SUM5R) is reconciled to a 0-23 range by effectively subtracting 24 from sums in the range 24-47. (SUM34R, SUM345R, SUM3RS and SUM4RS).

The multiplexor-set, located at zones A2, A3, B2, B3, and C1-C3 perform the function of selecting refresh address, during active scan periods, and data-entry addresses during periods of horizontal retrace (C7 true). The complete refresh-address is comprised of SUM0R-SUM2R, SUM3RS, SUM4RS and the refresh column-count functions, CC0-CC6. The complete entry-address is comprised of SUM0W-SUM2W, SUM3WS, SUM4WS and the cursor column-count functions, WC0-WC6.

The result of the column-count selection is the function-group MA0-MA3, which form the low-order memory address terms directly, and POS4-POS6, which must undergo matrix conversion to derive the mid-range address terms. In addition, the term SEL LINE, which is always false during the data-entry phase, will be true during refresh except during line-erase operations (ERASEF). This exception is required, in order that data-entry row-addresses rather than refresh row-address be accessed, thereby allowing 80 space-codes to be written into the virtual memory-row associated with the current cursor position. The SEL LINE function switches the multiplexor in zone C6 to select the high-order row-definers SUM1W, SUM2W, SUM3WS & SUM4WS, or SUM1R, SUM2R, SUM3RS & SUM4RS. The resultant terms LINE1-LINE4, must be resolved into the physical memory matrix.

The low-order row-definers, SUM0W or SUM0R are selected for the chip-enable functions by the logic in zone D1. Since CHIPENA and CHIPENB point, respectively, to the odd and even rows of both display data and memory data, they are used directly in addressing data-memory, without modification.

Since the display matrix is 80 characters by 24 rows, the largest binary factor which can be used as a "common denominator" for matrix conversion, is 16. Removing this factor, the remaining column factor, 5, is considered as the sum of a four-unit and a one-unit factor. By recombining these factors as products of sums each column is considered as the sum of a 64-unit increment and a 16-unit increment. If 64 is chosen as one of two coordinates which define a rectangular array, the other coordinate, based on 1920 characters, becomes 30. The visual display, then, is apportioned into the 64x30 memory array as one 64x24 character block and one 64x6 character block, the latter further subdivided into 24 16-character increments. Each row, then, is comprised of the sum of one 64-character slice of the major block, plus one of the minor increments.

Resolution of the display matrix into the memory matrix, is accomplished in the

multiplexer (zones A1, B1, & D1) whose outputs are designated MA4-MA9, by utilizing that fact that whenever columns 64 through 79 are indicated, the term POS6 will be true, and for columns 0 through 63 it will be false. Accordingly, this term will select the "normal" binary column and row definers (POS4, POS5, LINE1-LINE4) when false, and the 16-character line-increment definers (LINE1-LINE4, MA8 and MA9 forced true) when true. If the unmodified address - definers, MA0-MA3 and CHIPENA are included in each array, it can be verified that POS6 false calls up an array of 16 columns by 4 increments by 6 rows, restricted by MA8 & MA9, to rows 24 through 29.

6.6 SCHEMATIC SHEET #6 - DATA RECEIVER CHARACTER DECODERS LOAD-CURSOR SEQUENCE DETECTOR

6.6.1 Data Receiver

All data admitted for interpretation or storage in the ADM 3A is routed initially, as a serial data-stream, into the UART, shown in zones A4, B4 & C4. The source of this data may be from either the Current Loop Receiver circuit (CL DATA from sheet 10), the RS232 Receive Circuit (RECEIVED DATA, zone D4) or transmitted data (XDATA from sheet 10). As shown in zone D4, RS232 data must be level-shifted in the 1489 receiver circuit (A10-3), and transmitted data can only be admitted if the Half-Duplex (FDX-HDX) switch is closed. Routed through the OR-gate (B5-6), the serial data is routed to both the UART and the Extension Port.

If the UART is clear (no overrun from the last character), the serial data will be clocked in at the proper baud-rate (RECV CLK, zone A4), and accumulated in accordance with the format-switch settings shown on sheet 10, zone C4. When a complete character has been accumulated, and is available in parallel (IN1-IN8), the term DATA RDY (zone A3) will go true. Framing, parity and overrun errors are ignored on the ADM 3A, therefore, the integrity of data rates, duty-cycles and formats must be guaranteed by the source device.

Unless the ADM 3A is currently executing a clear or erase operation (ERASEF low), the Data Ready signal from the UART will be synchronized with the system decoding and writing circuits by timing-signal CC6. The resultant signal (INPUT, zone A3) will strobe the parallel contents of the UART into the Data Buffer (zones B3, C3). The information in the buffer (DATA1-DATA7, DATA1-DATA7) is used directly for entry into memory, or routed to the decoder logic for interpretation of control functions.

6.6.2 Character Decoders

The character decoders (zones A1, B1-2, C1-2, D1-2) interpret the received data by analyzing the current 7-bit code in three stages. The first stage examines the three or four high-order bits (DATA4-DATA7), and resolves the character into an ASCII Column or Half-Column position. Columns 0 & 1 are used in most cases, since they define the ASCII Control characters. Additionally, column 3 and the half-columns, 4L and 7H are decoded, to aid in the analysis of "Equal," "Space" and "Delete" codes, respectively.

The second stage (zone B2) fully decodes the low-order three-bits of the character-code, to generate eight row identifiers (XX0-XX7), applicable to each of the 16 half-columns in the ASCII matrix. The first stage combines the column or half-column identifier, the row identifier, and where required, DATA4 (or DATA4), to provide half-column identification, resulting in a unique character identifier. Eight control characters plus the "displayable" SPACE and DELETE codes are decoded irrespective of the condition of the Cursor Control Switch. Four control characters (RS, VT, FF & ESC) and the EQUAL code, however, can only be decoded (DATA4A low), if the Cursor Control switch is on (ENX true).

6.6.3 Load-Cursor Sequence Detector

In order to execute the storage, in the Cursor Row and Column counters, of two bytes of information which represent the absolute

position of the cursor, a sequence detector is provided (zones D2-D4) which can:

1. Reset to the occurrence of an ESC code, and hold control until another character is received.
2. Verify the intent to load cursor data, if the second code is "Equals" (=), or abort the sequence if it is not.
3. Maintain control of the terminal until the two additional bytes of Row and Column data are received.
4. Vector the row and column data to the proper destinations.

These tasks are accomplished with a modulo-four counter (ESC1, ESC2), which is normally clear (ESC1, ESC2). If an ESC character is detected, ESC1 will be set true on the next received-character strobe (XCLK). The ESC code will cause FORESPACE (cursor advance) and data entry into memory to be inhibited. If the next character received is anything but EQUALS, ESC1 will be reset (RSESC1), thereby terminating the sequence. If it is EQUALS, ESC2 will be set true and ESC1 allowed to remain true. In both situations ESC1 true will cause inhibition of FORESPACE. The condition of ESC1 and ESC2 both true will cause the next character received to be interpreted as the Row code, and loaded into the Row Counter. It will also cause ESC1 to be reset on the next strobe. With ESC1 false and ESC2 true, FORESPACE will remain inhibited, and the next received character will be translated and loaded into the Column Counter. At the next strobe, ESC2 will be set false, and the sequence will be complete.

6.7 SCHEMATIC SHEET #7 - CLEAR CIRCUIT READ BACK MONITOR DRIVE SIGNALS CURSOR GENERATION

6.7.1 Clear Circuit

The DM74123 (retriggerable one-shot, D1), located in zone D4 provides the power on clear signal. The RC circuit is connected to the positive trigger input. Therefore, when the power is up and the capacitor finally charges to the input threshold, the one-shot triggers

off and creates the reset signal. This unit is unusual in that every single storage element in the system is reset with the CLEAR pulse except for the refresh memories. This was done to accommodate the automatic board testers. The signal labeled TESTER INITIALIZE, entering the circuit D2-1 (74LS00, zone C3) accomplishes the same function as the power on clear except that the signal is generated by the automatic tester. These two clearing sources are combined at D2-3 (74LS00, zone C3) and is called CLEAR. A positive level at this point is the clearing level. This signal is buffered through six inverters to create the negative-going CLEAR signal. Each inverter has only 10 loads and they were used instead of a power buffer because of automatic board tester restrictions.

6.7.2 Read Back

The flip-flop located in zone C4 (EZ-8, 74LS113) is part of the READ BACK feature. This flop can set only if pin 22 on the main I/O connector J1 is held to ground. READ BACK is a test only feature therefore only internal test cables should have this pin grounded. This function is initiated by issuing a USASCII BEL code (octal 007) through the normal data input which sets this flip-flop. The ADM 3A then responds by sending all data on the top line of the display from the cursor position to the end of the line inclusive. The screen is rolled one line but the data remains on the screen and the bottom line is not erased. The cursor remains on the last character position transmitted which is the last position on the line. The READ flip-flop is cleared at the end of the operation when the CURSOR register overflows.

6.7.3 Monitor Drive Signal

The monitor drive signals, HDRIVE and VDRIVE are generated in zones C1 and D1. The horizontal drive signal, HDRIVE never moves regardless of the position of the 50/60 Hz selection switch. However, the VDRIVE signal changes between 50 Hz and 60 Hz refresh in order to maintain the same relative position of the video display on the display screen. (See the MAIN TIMING DIAGRAM for the positioning of these drive signals.)

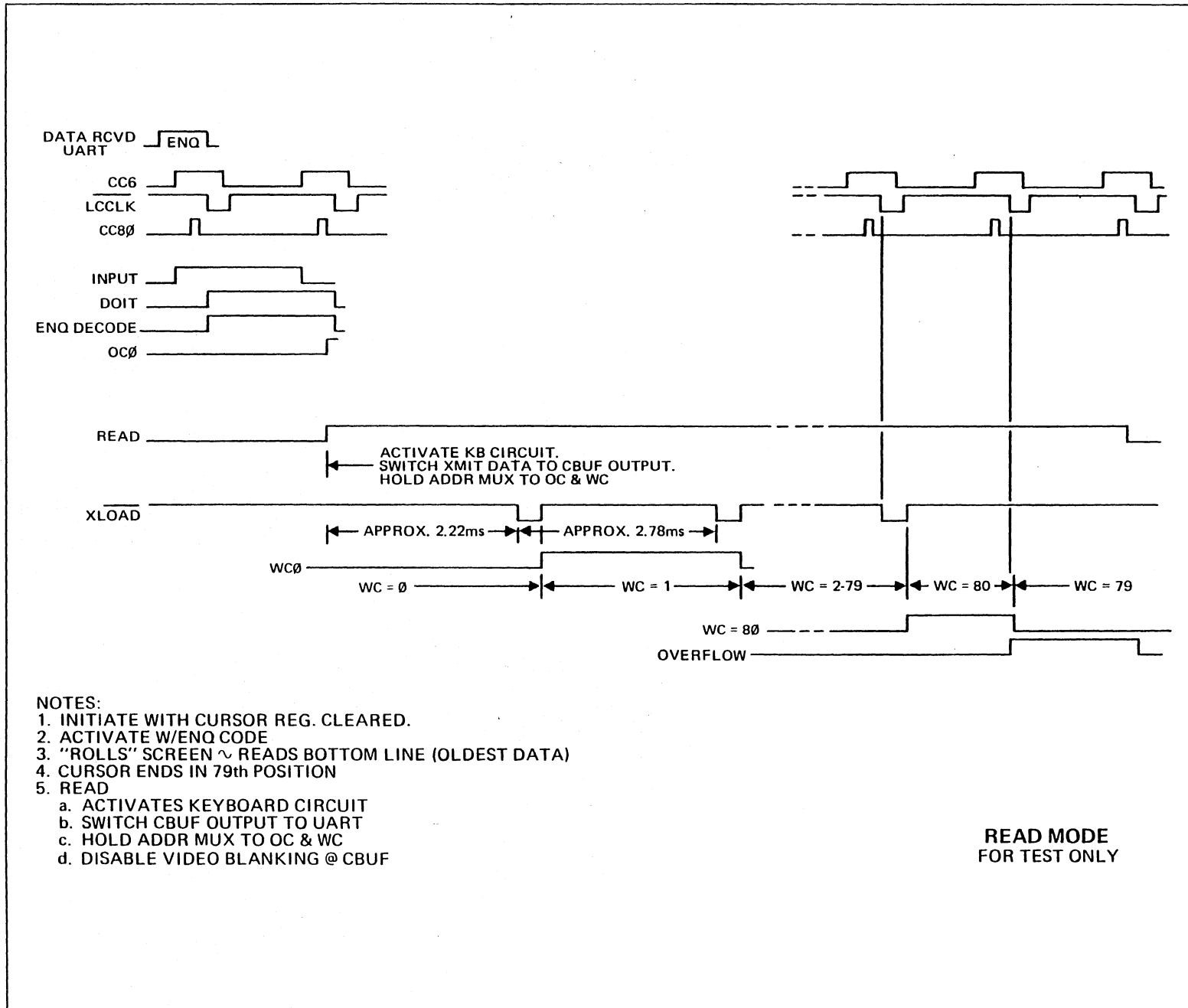


Figure 6-3. Read Mode

6.7.4 Cursor Generation

The circuits shown on zones A1-A4, B1-B4 and C1-C2 comprise the cursor generation and control logic. Three comparators are provided to continuously compare the cursor row and column counters with the corresponding display counters and generate a signal when all elements are in coincidence. The stage which compares CR0-CR4 with RC0-RC4 will be allowed to propagate its coincidence signal into the next stage, only if the Cursor Control switch is on (\overline{ENX} false). Otherwise, a continuous coincidence signal (ROWCO) is forced to the next stage, since the cursor will always reside below the bottom row. In the event one of the clear-screen operations is under way, START will hold ROWCOG low preventing any cursor comparison, thereby blanking the cursor.

When both row and column coincidence occur, a true output will be presented from the last comparator stage (E15-6). This signal is delayed by a pair of flip-flops for two character-periods, to synchronize the cursor with the video data, which is delayed two character periods in the course of accessing and processing. Whenever the Cursor Control switch is off (\overline{ENX} false) CURENA will be true only when the display row-count is greater than 23. This function is clocked by LC1 into the flip-flop E4-6 (CURSTOP), and combined with its output to form a signal (CUREN) which will be true only during the two line-scan periods immediately below the last row of data on the display.

If the Cursor Control switch is on, CUREN will be forced true continuously, allowing all coincidence signals to be propagated through the delay flip-flops. Coincidence will never occur outside the bounds of the data-display, since the cursor row and column counters are restricted to that area. The output of the delay flip-flops (CURSOR) will be mixed with video data in an exclusive -OR gate, if Cursor Control is on, resulting in a reverse image of the character over which the cursor resides. If Cursor Control is off (see sheet 8, zone A1), the double-underscore cursor signal will be admitted to the video driver in parallel with the non-inverted video signals (FLIP).

6.8 SCHEMATIC SHEET #8 - REFRESH MEMORY CHARACTER GENERATORS VIDEO SERIALIZER TRANSMIT DATA MULTIPLEXERS

6.8.1 Refresh Memory

The refresh memory is composed of 14-2101 RAMs which have 500 nsec access times. These RAMs are organized as a 2K by 7-bit memory which hold the 1920 USASCII codes for screen refresh. There are four configurations of memory in the ADM 3A. The first configuration is six RAMs which is used for the upper case only, 12 line display. Then seven RAMs are used for the upper/lower case, 12 line version. Twelve RAMs are required if upper case only, 24 lines. Then all 14 RAMs are installed if the fully configured upper/lower case, 24-line combination is desired.

The selection between 12 and 24 lines is made with a switch. (See sheet 3 zone A3). Zone A4 of this schematic has a switch labeled \overline{UCEN} which switches the unit from upper case only to upper/lower case display. The 74LS157 sections located in zones C4 and C3 (2:1 Mux, H7) alter the data properly for 7 bit USASCII to 6 bit USASCII for upper case only display. The output K12-12 (zone C4) selects between two sources for bit 6 storage. Upper case only display utilizes DATA7 while upper/lower cases uses DATA6. Gate H7-8 simply forces bit 6 to a high level when the ADM 3A is erasing a line. This converts the NULL code coming in to a proper SPACE code. The 74LS86 in zone C4 (k9-3) has the function of being able to clear the memory to zeros with the activation of a switch located internally.

6.8.2 Character Generators

The circuitry located above the refresh memory is used to blank the video display at selected times. This function is normally accomplished at the video serializer but was placed here to allow the automatic board tester to shut the video off without affecting the character generators or the video serializer.

The horizontal blanking is accomplished with gate C5-4 (zone D4, 74LS02). The term RC5, entering the circuit at C5-2 does the blanking for row counts 32 and higher. This signal is active only if the unit is operating at 50 Hz since the 60 Hz units reach a maximum count of 29. The term RC=24/31 accounts for the blanking immediately below the video and up to row count 31. Gate D4-3 (74LS02, zone D4) generates the term that blanks every other line if the ADM 3A is operating in the 12 line mode. The combined blanking term, called VIDEO BLANK and going to the clear inputs of the two 74LS175's (K13 and L13, zones B3 and C3) used as the character generator input buffers, is generated in the flop K8 (74LS74, zone D3). Notice that clearing the CBUF registers does not present a NULL code to the character generator inputs. The outputs associated with bit 6 are inverted. Therefore, when VIDEO BLANK is active, the CBUF outputs present a USASCII SPACE code to the character generators.

The two character generator ROMs are rather straightforward. The upper case ROM is a standard masked part (2513) but the lower case ROM is a custom masked part. The one unusual thing about this is that all of the address lines into the lower case character generator are inverted.

6.8.3 Video Serializer

The video serializer used is a 74166, eight bit shift register which is preset once every 643 nsec and shifted at an input clock rate of 10.8864 MHz. Gate K16-5 (74LS00, zone A1) is used to blank the video during a READ BACK operation. This is required because the CBUF registers are used to send memory data to the transmit USART without regard to its effect on the video display. Since the result is quite unusual, this gate was installed. Gate J9 (74LS00, zone A1) is used as the video driver.

6.8.4 Transmit Data Multiplexers

The two multiplexers (74LS157, K6 and L6, zones D1 and D2) are used to select between keyboard or refresh memory as the source of the data going to the transmit UART. The refresh memory is selected during the READ BACK operation and the keyboard output is selected at all other times.

6.9 SCHEMATIC SHEET #9 - KEYBOARD CIRCUIT

The keyboard is encoded utilizing a normal scanning-type circuit. The two counters (74LS293) located in zones D3 and D4 clock through all possible 128 USASCII codes. The four least significant bits are decoded through the 1 of 16 decoders (74LS154-L8) whose outputs appear as one side of the encoding matrix. The three most significant bits, K5 through K7, operate the selection inputs of the 8 to 1 multiplexer (74LS151-L9). The inputs of this multiplexer represent the second side of the encoding matrix. This encoding matrix has a direct relationship with the USASCII code chart. The outputs of the decoder represent the rows of the chart while the inputs of the multiplexer represent the columns. The key switches are then placed selectively within this matrix on the intersection that generates the lower case code associated with that particular switch.

The detection of a switch closure occurs in the following manner. When none of the keys are depressed (all switches open), the output of the multiplexer L9 is high and the clock (KBCLK) to the code generating counters is running. While KEY DATA is high, the signal labeled GO (zone C1) will be held low, which clears the shift register F1 (zone C2) and holds flop E2 (zone D1) in the key debouncing state. This is the normal idling state with the counters cycling, KEYDATA high, shift register F1 cleared, and BOUNCE low. When an encoded key is depressed, the counters continue cycling until the selected ROW and COL are simultaneously enabled. At this time the low level signal from the row decoder is propagated through the key switch, through the multiplexer, to gate E7 (zone B2) which effectively shuts off the clock to the code generating counters. When KEY DATA goes low, the signal labeled GO is enabled, thereby releasing the shift register and the Bounce flop. At this time the signal BOUNCE is low which enables every cycle of the clock RC0 to propagate through gate E3, located in zone D2, to the clock input of the shift register. This clock (900 Hz) determines the length of time allowed for the mechanical key switch to stop bouncing. It allows five cycles of this

clock to pass before the decision is made that the code is stable. At the end of these five cycles, the signal BOUNCE goes high which does two things. First, the clock input to the shift register is disabled through gate D2 at zone D2. Secondly, the SHIFT/LD line to the shift register is taken to the loading state by gate F5 in zone D2. The circuit is now waiting for one of two things to happen; the character key being released or the REPT key being depressed. In the event that the key is released, KEY DATA will immediately go high and the entire circuit will revert to the idling state. If the REPT key is depressed without releasing the first key, the SHIFT/LD line goes to the shift state because of F5-2 (zone D2). Notice now that when BOUNCE went high at the end of the first shift register cycle, the term RCRESET was allowed to gate the clock RC0 effectively cutting its rate to 60 Hz to 50 Hz depending on the position of the 50/60 Hz selection switch. This new clock rate will now determine the repeat rate from the keyboard. The shift register will now shift at the lower rate, generating a load pulse every time DOUT goes high and continuing until the REPT key is released or the primary key is released. The repeat rate is 12.5 char/sec at 60 Hz and 10 char/sec at 50 Hz. The term THRE into gate H5-5 (zone D2) is there to slow the repeat rate if the baud rate selected has a character time longer than the period of the repeat cycle. The terms READ and READ in this circuit are activated by the read-back circuit which is used for internal LSI testing only. In normal operation, the ADM 3A memory cannot be read by the computer. When the read-back is activated, the keyboard control circuit is fooled into thinking that it is repeating a code. The one difference is that the circuit now repeats utilizing the debouncing clock and not the slower clock. The data lines are naturally switched to the memory output which occurs on schematic sheet 8.

There are three methods by which the code normally generated by the scanning circuit can be altered. First, the depression of the CTRL key (zone A2) unconditionally drives bits 6 and 7 to the low state. This means that the code generated will be driven to columns 0 or 1 depending on the state of bit 5. This is the

means by which control codes, not on individual keys, are generated. The next way that the code can be altered is by inverting bit 5. This is used to create the shifted (upper case) codes in USASCII columns 2 and 3. Gate K10 (74LS00) in zone A4 identifies the code generated as a column 2 or 3 code. Row 0 is eliminated from this shifting because the SPACE code and ZERO code are not affected by the shift key. This is done at L10-9 (zone A3). The last way to alter the code is by inverting bit 6. This is used to shift from the lower case alpha codes in column 6 and 7 to the upper case codes in columns 4 and 5. There are two ways to effect this bit 6 inversion. The normal shift keys and the UPPER CASE ALPHA switch.

The UPPER CASE ALPHA switch is used on systems where no lower case alpha codes are tolerated. Therefore, while in this mode, the normal SHIFT keys have no effect on the alpha keys. Upper case alpha is always generated. This is accomplished at gate L10 (zone A3). L10-2 and L10-1 decode the fact that the code originates in columns 6 or 7. Notice that in the matrix above, the only codes in columns 6 or 7 are the twenty-six lower case alpha codes. The six remaining non-alpha codes are placed in columns 4 and 5. Therefore, the KC6 KC7 decode in gate L10 definitely picks out the lower case alpha codes. The normal SHIFT function for columns 4 through 7 is accomplished in gate K10 (zone B4). If KC7 is set, identifying it as columns 4 through 7, and the SHIFT key is depressed, bit 6 is unconditionally inverted.

The CLEAR key, located in zone A2, is utilized in conjunction with the SHIFT key to clear the refresh memory, clear the KEYBOARD LOCK circuit, and clear the I/O interface circuitry. This combination is done in gate L12 located in zone A1.

The BREAK key (zone B3) is used to signal the computer that I/O termination is desired. When depressed, this key has one of two effects, depending on whether the unit is in the transmit or receive mode. If the unit is transmitting when the BREAK is activated, the primary transmit data line (BA, pin 2) is driven to the "spacing" state for as long as the key is depressed. If the unit is receiving data

and is in the 202, reverse channel mode, the SECONDARY TRANSMIT DATA line (SA, pin 11) is driven to the "marking" state.

The last function on this sheet is the HERE IS circuit. If the ADM 3A has this option installed, the depression of this key initiates the transmission of a unique message to the computer. This message is contained in PROM in the option and can be up to 32 characters long. This transmission can also be activated with the receipt of an ENQ code from the computer. An ENQ code generated at the local keyboard will not be recognized because of the lockout circuit in zones A1 and A3. Locally generated characters will cause the flip-flop (KSDLY) to be set at the time the character is transmitted (XLOAD). The output KSDLY will be false until either a remote character is received, or the local character is acknowledged in half-duplex. At this time DOIT will reset the flop. The term KSDLY, in conjunction with the Enquiry-code (ENQ) will prevent a locally-generated ENQ from being recognized.

6.10 SCHEMATIC SHEET #10 - DATA TRANSMITTER CONTROL SECTION OF UART CURRENT LOOP XMTR/RCVR KEYBOARD LOCK CIRCUIT

6.10.1 Data Transmitter

The transmitter and control sections of the UART are shown on this schematic. Indicated on UART pins 26 through 32 are the seven bits which comprise the USASCII code. XDATA7 is the most significant bit and XDATA1 the least significant. This code to be transmitted to the line comes from one of three sources. In normal operation, the keyboard circuit and the ANSWER BACK option can generate the code. However, during testing the contents of the memory are sent through the UART during READ-BACK. Pin 40 of the UART is the transmitter clock input. The source of this clock comes from sheet 11 where it is controlled by CLEAR TO SEND (sheet 12, zone D3). If there is no CTS, this input will remain high. In normal operation, the clock on this line will be the

same as receive clock input. The frequency will be 16 times the desired transmit baud rate. However, with the split clock option, the transmit and receive rates can be different. The receive rate is always controlled by the main baud rate switches under the cover, while with the split speed option, the little rotary switch in front of the keyboard controls the transmit rate. This rotary switch is accessible only when the unit is open. All baud rates are available on this switch except for 1800 baud. With the split speed option, the selection of 1800 baud as the receive rate limits the selection of the transmit rate to 110 baud. No other baud rates are legal.

Pin 23 on the UART is the loading signal for the transmitter section. The normal state of this line is high and it only goes low when serial transmission of the data present on the XDATA input pins 26 through 32 is desired. The two sources of this loading signal are the keyboard circuit and the ANSWER BACK option board.

Two control signals are utilized from the transmitter section. These are TRANSMITTER HOLDING REGISTER EMPTY (THRE) and TRANSMIT REGISTER EMPTY (TRE). The UART utilized in this unit is buffered on the transmitter data input lines and therefore, when the loading signal is given on pin 23, the XDATA lines are transferred to a buffer register instead of directly to the serializer. When this buffer, called the TRANSMITTER HOLDING REGISTER is loaded, the signal THRE (zone A3) goes low. The transfer of the data from this buffer to the serializer is contingent on the transmitter clocks being present (CTS high) and the serializer being empty. If the serializer is empty, the signal TRE (zone B3) is high. If both conditions are present, the buffer data will be automatically transferred to the serializer on the next clock. At this time, TRE will go low to indicate that the serializer is being used. When both signals are high, the transmitter section is completely empty. These two UART signals are combined to create the "bouncing" REQUEST TO SEND signal selectable on the interface. When either of these signals, THRE or TRE, is low it will cause RTS to be high. Therefore, the RTS

signal will "surround" the transmitted character.

The last signal out of the UART transmitter section, is naturally, the serial data. This line marks in the high state and the indication of character starting is this line going low for the start bit of the character. The data bits in the following byte are then sent in a serial manner with the least significant bit first, through data bit 7, followed by the parity bit (if enabled) and the one or two stop bits. The data at this point is "true" data, that is a "one" is indicated by a high level and a "zero" by a low level. This data is then sent through gate C6 (zone A3). C6-4 accepts the signal from the BREAK key shown on drawing 9, zone B3. The depression of this key takes the transmit data line to the spacing (high) state. Input C6-3 accepts data generated by the device connected to the extension port and received by the 1489 EIA receiver A6 (zone A4). This combined data signal (C6-6, 74LS10, zone A3) is then sent to both the EIA and CURRENT LOOP transmitters. The selection of the transmitter to be used is governed by the switch schematically represented in zone C3 and labeled RS232/CL. This switch is physically located under the little plate next to the keyboard. When the switch is positioned to the left (closed), the EIA transmitter is selected. When one transmitter is selected, the unused transmitter will maintain a marking output to the outside world. Therefore, the RS232/CL switch can be used for "local" operation where data is desired out the extension port but not out of the main I/O port. The transmitted EIA data is level shifted through the 1488 A9 located in zone A1 and out to the EIA connector, pin 2.

6.10.2 Control Section of UART

The control section of the UART is also shown on schematic #10. The MASTER CLEAR is driven high when the UART is to be cleared (pin 21). There are five characteristics of the transmitted data that can be selected by the toggle switches under the panel. First is the STOP BIT SELECT input on pin 36. When this line is held low, one stop bit will be attached to the transmitted byte while a high signal will select two stop

bits. The next input controls the WORD LENGTH SELECT. A high input selects an 8 bit data word while a low level selects a 7 bit data word. UART pin 39 is EVEN PARITY ENABLE which it would do if this pin is allowed to go high. Odd parity is selected by moving the switch to the left and driving this input low. PARITY INHIBIT is located on UART pin 35. Parity generation is inhibited if the switch is to the right and the input is high. If this input is low then the UART control will read the parity selection input (pin 39). If this input is high, then pin 39 is ignored. The last control input is pin 33, BIT 8 CONTROL. This input is active only if the ORD LENGTH SELECT input (pin 38) is high and an 8 bit word is selected. This control input is then used to choose a "mark" or a "space" in the eighth data bit position.

6.10.3 Current Loop XMTR/RCVR

The last item on this sheet is the CURRENT LOOP transmitter/receiver combination. The current loop differs from the circuits in the ADM 1A and 2 primarily because it is bipolar. That is, current direction is immaterial. The transmitter and receiver can run completely isolated from the ADM 3A which is its normal operating mode. However, provision has been made inside the unit to tie one leg of the transmitter or receiver to +12 volts through a resistor to create a current source. As an alternative, a ground strap can be installed, in place of the resistor, to act as a current sink in the case of a positive external voltage source or as a current source in the event an external negative sink is provided. The CURRENT LOOP circuits operate over a range of 16 to 24mA, at a peak supply voltage of 20 VDC.

6.10.4 Keyboard Logic

The signals labeled LOCK and UNLOCK are used to control the KEYBOARD LOCK flip-flop located in zone D1 of this sheet. The code used to unlock the keyboard is a USASCII SO (octal 016) and the code used to lock is a USASCII SI (octal 017). The CLEAR SCREEN function is activated by USASCII SUB (octal 032). The SPACE decode is created in H2-4 (7402, zone A1) to recognize this code

for the nondestructive cursor feature. The USASCII ENQ is used to activate the ANSWER BACK option (if installed). This decode is combined with the depression of the HERE IS key on the keyboard schematic (sheet #8).

The flip-flop located in zone D1 is used to control the locking and unlocking of the keyboard circuit. Notice that there is a switch in the LOCK input to disable this feature if the particular application dictates that the USASCII SI code be used for other purposes. There are two ways to unlock a previously locked keyboard. The first is the receipt of the USASCII SO code. The keyboard can also be unlocked by the simultaneous depression of the SHIFT and CLEAR keys which generate the signal named KEY CLR.

6.11 SCHEMATIC SHEET #11 - BAUD RATE GENERATION

This schematic comprises the counters and associated logic, required for the generation of transmit and received clocking functions for the UART. For a given BAUD-rate at the interface and to the terminal, the UART must be supplied with a clock-train 16 times the frequency of the I/O serial pulse-train. For the highest available BAUD-rate (19,200), this requires a UART clock-rate of 307.2 Khz. For the lowest (75 baud) rate, the UART must be supplied with a 1.2 Khz clock. To accomplish the required frequency division, three counters are provided (zones D1-D4) which use as their primary input, the DC1 function from the dot-counter, which as a cyclic rate of 3.1104 Mhz. The three counters normally divide this signal, progressively by 5, 16 and 16. Accordingly, the output from the third stage of the first counter (CLK1, zone D3) will represent a division by 5, and have a cyclic rate of 622.08 Khz; approximately double the required UART clock rate for 19,200 baud. If the 19200 baud switch (zone B2) is closed, this signal (DOUBLE CLK) is routed to the Receive Clock (RECV CLK) Flip-flop, where it is divided by two, to provide a clock-rate of 311 Khz. This signal is approximately 1.2% higher than the ideal rate, but well within the accuracy requirements of contemporary communica-

tions links. Unless the etch-link is cut, to enable split baud rates, the same signal selected for the Receive Clock, is also sent to the Transmit Clock (XMIT CLK) flip-flop, for division by two.

Since most of the common baud-rates used with the ADM 3A are sub-multiples of 19200 baud, they are derived by progressively dividing the 622 Khz signal by 256 in the two remaining counters. The only rates which cannot be derived in this manner are 1800 baud and 110 baud. The former is generated by causing the first counter to divide by 6 instead of 5, and the second to divide by 9 rather than 16. The resultant division by 54 will provide a signal at the fourth stage (CLK5) of the second counter, with a cyclic-rate of 57.6 Khz, which is exactly the required double-clock frequency.

If a baud-rate of 110 is desired, the counters are forced to divide by 5, 16 and 11 for a combined division of 880. The resultant signal at the fourth stage (CLK9) of the final counter will have a cyclic rate of 3.534 Khz, which is 0.4% higher than the ideal double-clock frequency of 3.52 Khz.

In the event split baud rates are desired, the etch-link shown at zone B1 must be cut, and a rotary baud-rate switch (zone A2) must be installed. Due to the nature of non-standard division-string, the split-baud rate features cannot be used when either 110 or 1800 baud are selected.

SECTION VII PARTS LIST

Included in this section are lists of both the major components as provided by Lear Siegler and the general parts which are a part of the major components.

7.1 ADM 3A REPLACEABLE PARTS INFORMATION

Spare parts and renewal parts for the ADM 3A are available from Lear Siegler Data Products Division. When ordering parts, include the following information.

1. ADM 3A Serial Number
2. Part Description
3. LSI or Manufacturer's Part Number

Routine parts orders may be mailed to:

Lear Siegler, Inc.
Data Products Customer Service
714 North Brookhurst Street
Anaheim, California 92803

Emergency parts orders may be placed by telephoning:

Data Products Customer Service
Telephone (714) 774-1010

or by teletype to:

TELEX 65-5444
TWX 910-591-1157

7.2 MONITOR REPLACEMENT PARTS INFORMATION

7.2.1 Ordering Parts

Most parts contained in the monitor are available commercially from electronic parts

outlets. When it is necessary to order spare or replacement parts from BBRC, Miratel Division, include the part description, part number, model and serial number data of the monitor as listed on the serial number plate and, if applicable, the schematic reference number listed in the parts list. Orders for these parts should be sent to:

Ball Brothers Research Corporation
Miratel Division
1633 Terrace Drive
Roseville, Minnesota 55113

For rapid service:

Telephone area (612) 633-1742
or
Teletype area 910-563-3552

7.2.2 Returning Parts

When the monitor requires service or repair in accordance with the enclosed warranty, return the unit or part to:

Ball Brothers Research Corporation
Miratel Division
1633 Terrace Drive
Roseville, Minnesota 55113
Attn: Customer Service
Telephone area (612) 633-1742
Teletype area 910-563-3552

Unnecessary delays may be avoided when parts are returned to Miratel Division using the following procedures:

1. Package the unit or part in accordance with the method of shipment. Enclose a list of the material being returned and the reason for returning it.

2. Send the unit or part, transportation prepaid, to the address stipulated for returning parts.

All equipment and parts described in the warranty will be replaced, provided Miratel's examination discloses that the defects are within the limits of the warranty. If damage of defects are not within the limits of the warranty, the customer will be notified of the extent of repairs required and the cost. The unit will be repaired and returned upon agreement.

ADM-3A ASSEMBLY PARTS LIST 129450

LSI Part Number	Description
129450	ADM-3A Final Assembly
128214	Label, High Voltage
128565-23	Wire Assy, 15" Yellow
129452-3	Housing, Top
129452-5	Housing, Bottom
129453-3	Logo, ADM-3A
129454-3	Bracket, CRT Mount
129455-3	Cord, Power 115VAC
129455-5	Cord, Power 230VAC
129456-3	Nameplate (115V)
129456-5	Nameplate (230V)
129457-3	Legend, Switch
129458-3	Transformer, 115V
129458-5	Transformer, 230V
129459-10	Wire, 10.5"
129459-23	Wire, 23" Green
129470-11	Board Assy, ADM-3A
129479-1	Monitor, P4 Etch
128481-11	Cable, 18"
129482-3	Bracket, CRT Board Mount
129483-3	Clip, Retainer Bracket
129484-3	Screen
129485-3	Plate, Baffle
129486-3	Spacer
129487-1	Speaker
129494-3	Support, CRT
804011	Switch, TGC0411-TW-B
807001	O Ring, 214-060307-00-2303
809015	Connector, 03-09-1033
809023	Contact Amp 350418-1
821001	Screw, 10-32x7/16 Sems
821002	Screw, 10-32x3/4 Ph
821402	Screw, 4-40x3/16 Ph
821403	Screw, 4-20x5/16 Plastite
822001	Nut, 10-32 8041-NP Brass
823001	Washer 10
824001	Rivet, Pop AD66ABSLF
830001	Strain Relief, Heyco SR6N3-4
830002	Fastener, ABMM-AC
830003	Fastener, Cadle Panduit PLTIM-M
835002	Lug, RA873
839014	Sleeving, Shrink Fit 221x3/4
840001	Fuse, 313.80, 8 Amp Sioblo
840002	Holder, Fuse 342038L
129459-9	Wire, Ground

Monitor Parts List

Symbol	Description	Mfg.	Mfg. Part Number	BBRC Part Number
	Capacitor, Fixed; μ F Unless Otherwise Stated			
C1	3300; 60V, Electrolytic	BBRC		1-012-2156
C101	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C102	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C103	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C104	0.001 + 10%; 1000V, Ceramic Disc	ERIE	Type 801	1-012-0540
C105	0.47 + 10%; 100V, Mylar	PAK	MF830	1-012-1005
C106	0.47 + 10%; 100V, Mylar	PAK	MF830	1-012-1005
C107	500; 6V, Electrolytic	BBRC		1-012-2158
C108	100; 6V, Electrolytic	BBRC		1-012-2160
C109	0.022 + 10%; 400V, Mylar	SPRA	Type 225P	1-012-0800
C110	.1 + 10%; 200V, Mylar	PAK	MF580	1-012-0870
C111	0.02 + 20%; 1000V, Ceramic Disc	ERIE	Type 841	1-012-0780
C112	50; 50V, Electrolytic	BBRC		1-012-2157
C113	10 + 10%; 63V, Mylar	BBRC		1-012-1130
C114	200; 25V, Electrolytic	BBRC		1-012-2159
C115	50; 25V, Electrolytic	BBRC		1-012-2165
C116	20; 150V, Electrolytic	BBRC		1-012-1260
C117	6 μ f; 25V, Electrolytic	SPRA	TE1203	1-012-2066
C118	820pf + 5%; 500V, Dipped Mica	ARCO	Type DM	1-012-0482
C119	25; 50V, Electrolytic	BBRC		1-012-2193
C120	.01 + 20%; 1000V; Ceramic Disc	ERIE	Type 811	1-012-0740
C201	50; 50V, Electrolytic	BBRC		1-012-2157
C202	0.01 + 20%; 1000V; Ceramic Disc	ERIE	Type 841	1-012-0780
C203	50; 50V, Electrolytic	BBRC		1-012-2157
CR1	VS148, Bridge Rectifier	VARO	VS148	1-021-0413
CR2	H510, High Voltage Rectifier	VARO	H510	1-021-0424
CR101	1N3605	SYL	1N3605	1-021-0410
CR102	1N3605	SYL	1N3605	1-021-0410
CR103	1N4785	RCA	1N4785	1-021-0360
CR104	1N3279	DI	1N3279	1-021-0380
CR105	1N3279	DI	1N3279	1-021-0380
CR106	1N3279	DI	1N3279	1-021-0380
CR107	1N3279	DI	1N3279	1-021-0380
CR108	1N3605	SYL	1N3605	1-021-0410
F1	Fuse, 0.6A-250V, $\frac{1}{4}$ x $\frac{1}{4}$, Slo-Blo	LF	Type AGC	1-028-0244
or	Fuse, 0.6A-250V, $\frac{9}{32}$ x $\frac{1}{4}$, Slo-Blo (TV-B12)	BUSS	Type MDM	1-028-0245
F101	Fuse, 2A-125V, Picofuse	LF	276002	1-028-0247
L1	Vertical Choke	BBRC		6-003-0321
L101	Coil, Width	BBRC		1-016-0303
	TRANSISTOR			
Q1	2N3055	RCA	2N3055	1-015-1134
Q101	2N5830	MOT	2N5830	1-015-1172
Q102	D13T1	GE	D13T1	1-015-1157
	Resistor, Film: $\frac{1}{2}$ W + 5% Unless Otherwise Stated			
R133	4.7K; $\frac{1}{2}$ W			70-16-0472
R134	Not Used			
R135	22K			70-16-0223

Monitor Parts List (continued)

Symbol	Description	Mfg.	Mfg. Part Number	BBRC Part Number
R136	22K			70-16-0223
R137	33K; 1W Composition			1-001-2448
R201	1K			1-011-2270
R202	1K			1-011-2270
R203	10K			1-011-2294
R204	0.68 + 10%; 2W, Wirewound	IRC	Type BHW	1-011-2217
R205	1.5K			1-011-2274
R206	470			1-011-2262
R207	470			1-011-2262
R208	Var; 500 + 20%; 1/5W, Composition	CTS	Type 201	1-011-5604
R209	470			1-011-2262
	TRANSFORMER			
T1	Power	BBRC		1-017-5390
T2	High Voltage (TV-12C, TV-12, & TV-E12)	BBRC		6-003-0320
or	High Voltage (TV-B12, TV-TC12, & TV-C12)	BBRC		6-003-0325
or	High Voltage (TV-T12)	BBRC		6-003-0326
or	High Voltage (TV-D12)	BBRC		6-003-0333
T101	Horizontal Driver	BBRC		1-017-5338
VR101	1N758	T1	1N758	1-021-0180
VR102	VR56	ST	VR56	1-021-0420
	MISCELLANEOUS			
	Socket, CRT (TV12)	BBRC		1-022-0427
	Fuseholder, Extractor Post, Fuse Size: ¼x1¼	LF	342012	1-028-0210
	Fuseholder, Extractor Post, Fuse Size: 9/32x1¼ (TV-B12 Only)	BUSS	Type HCM	1-028-0246
	Low Voltage Circuit Board Assembly	BBRC		6-003-0459
	Main Chassis Circuit Board Assembly	BBRC		6-003-0500
	Main Chassis Circuit Board Assembly (TV-T12)	BBRC		6-002-0476
	Main Chassis Circuit Board Assembly (TV-TC12)	BBRC		6-002-0502
	Main Chassis Circuit Board Assembly (TV-C12)	BBRC		6-002-0504
	Main Chassis Circuit Board Assembly (TV12, Tektronics)	BBRC		6-002-0506
	Cable Assembly; 8 Inch	BBRC		
	Cable Assembly; 5 Inch	BBRC		6-004-0631
	Power Supply Module (TV-12, 120VAC)	BBRC		6-003-0371
	Power Supply Module (TV-12, 220VAC)	BBRC		6-003-0372
	Power Supply Module (TV-B12, 120VAC)	BBRC		6-003-0368
	Power Supply Module (TV-B12, 220VAC)	BBRC		6-002-0370
	Deflection Coil Assembly	BBRC		6-004-0314
	Deflection Coil Assembly (TV-B12)	BBRC		6-004-0321
V1	CRT, 12 Inch, P4 Phosphor	BBRC		1-014-0737
	Power Cable Assembly, 120VAC	BBRC		6-003-0645
	Power Cable Assembly, 200VAC	BBRC		6-003-0652

Monitor Vendor Codes and Locations

Code	Manufacturer	Location
BBRC	Ball Brothers Research Corporation, Miratel Division	Roseville, Minnesota
BUSS	Bussman Manufacturing	St. Louis, Missouri
CRL	Centralab	Milwaukee, Wisconsin
CTS	CTS Corporation	Elkhart, Indiana
DI	Diode, Inc.	Chatsworth, California
ERIE	Erie Technological Products, Inc.	Erie, Pennsylvania
GE	General Electric	Syracuse, New York
IRC	IRC Corporation	Philadelphia, Pennsylvania
LF	Littelfuse Company, Inc.	Des Plaines, Illinois
MALL	P. R. Mallory Company, Inc.	Indianapolis, Indiana
MOT	Motorola Semiconductor Products	Phoenix, Arizona
NPC	Neucleonics Products	Los Angeles, California
PAK	Paktron	Alexandria, Virginia
RCA	RCA Semiconductor Division	Harrison, New Jersey
SPRA	Sarkes Tarzian, Inc.	Bloomington, Indiana
SYL	Sylvania Electric Products	Seneca Falls, New York
TI	Texas Instrument	Dallas, Texas
VARO	Varo Corporation	Garland, Texas

P.C. Board Assembly, Answer Back

Ref. Des.	Description	LSI Part No.	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty. 01 011	Note
1	P.C. Board Assy., Answer Back	129489-01				
2	I/C	128348-02			1	
3	I/C	128348-74			1	
4	I/C	128348-93			1	
5	I/C	128348-113			2	
6	I/C	128348-157			4	
7	Capacitor .1 μ F	129329-104			2	
8	Capacitor 10 μ F	129469-106			2	
9	P.W. Board	129489-05			1	
10	Prom. 82S23 Type	129493			1	
11	Socket, 16 Pin		CA-16S-10SD	Circuit Assy.	3	
12	Socket, 18 Pin		CA18S-10SD	Circuit Assy.	2	

ADM-3A P.C. BOARD ASSEMBLY

LSI Part Number	Description
128348-1	IC
128348-123A	IC
128348-1488	IC
128348-1489	IC
128348-154	IC
128348-1602	IC
128348-166	IC
128348-25	IC
128348-2513	IC
128348-4102	IC
128348-78M12	IC
128348-7805	IC
128348-7815	IC
128348-79M12	IC
128518-101	Cap, DM 15-101
128518-225	Cap 2.2 uF
128518-334	Cap .33 uF
128533-101	Resistor
128533-102	Resistor
128533-103	Resistor
128533-183	Resistor
128533-201	Resistor
128533-241	Resistor
128533-271	Resistor
128533-393	Resistor
128533-471	Resistor
128533-473	Resistor
128533-7R5	Resistor
129329-104	Cap
129451-3	Keyboard ADM-3A
129467-0	IC
129467-10	IC
129467-11	IC
129467-112	IC
129467-113	IC
129467-125	IC
129467-13	IC
129467-151	IC
129467-157	IC
129467-161	IC
129467-175	IC
129467-193	IC
129467-195	IC
129467-2	IC
129467-20	IC
129467-27	IC

ADM-3A P.C. BOARD ASSEMBLY (Continued)

LSI Part Number	Description
129467-283	IC
129467-293	IC
129467-32	IC
129467-4	IC
129467-42	IC
129467-51	IC
129467-74	IC
129467-8	IC
129467-85	IC
129467-86	IC
129468-108	Capacitor
129468-189	Cap
129468-506	Cap
129469-106	Cap
129469-306	Cap
129469-358	Cap
129470-5	Board, PC
129472-510	Resistor
129473-5	Jackscrew, Rev. "A"
129474-3	Heatsink
129474-9	Heatsink
129476-241	Network, Resistor
129476-472	Network, Resistor
129476-512	Resistor, Network
129478	Connector
129496-3	Plate, Closure, Rev. "A"
801006	Pot, BM5874
802002	Socket CA16S10SD
802003	Socket, CA-18S-10SD
802006	Socket, CA24S10D
802008	Socket, CA40S10SD
803001	Resistor, PC5800
803002	Resistor, PC5802
804006	Switch, 435640-4
804007	Switch, 435640-1
804012	Switch, MSS1040D-1
806001	Knob, IRQ-5000-1-Blk
808001	Rectifier, Bridge MDA970-1
808002	Rectifier, Bridge W005M
808003	Diode, 1N914
808004	Diode, 1N4001
808006	Diode, 1N5231B
808007	Diode, 1N5338B
808008	Rectifier, Bridge WO2M
809001	Connector, 22-02-2041
809002	Connector, 22-02-2051

ADM-3A P.C. BOARD ASSEMBLY (Continued)

LSI Part Number	Description
809007	Connector, 09-18-5031
809008	Connector, 09-18-5051
809009	Connector, 09-18-5059
809012	Connector, 09-18-5121
810001	Transistor, 2N3904
810003	Transistor, 2N3906
810005	Transistor, 2N5986
811003	Crystal, 800A-10.8864MHz
819001	Isolator, Optical MCT-2
820002	Heatsink, 207-SB
821404	Screw, 4-40x3/8 Self-Tap PH
821601	Screw, 6x3/8 F504M
822401	Nut, 4 F557-7
823401	Washer, 4 MW 401M
823403	Washer, 4 Ext. Tooth
823601	Washer, 6 MW-423M
824010	Rivet, R3479x1/4
839001	Insulator, Mylar, 43-77-2
839003	Insulator, 97405 or 4x1/32
839012	Insulator, 7717-5
839013	Tape, Mylar, 1/2x5/8x.003
840003	Fuse, 273001 1 amp
840004	Holder, Fuse 281005

QTY REQD			LIST OF MATERIALS OR PARTS LIST				
			FIND NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
			1				
			2				
	2	3	3	2-350803-2	.250X .032 TAB RCPT	AMP	⚠
			4				
			5				
	1	6	6	03-09-1033	RCPT 3CKT	MOLEX	
	3	7	7	350417-1	TERM, .093 SCK	AMP	⚠
			8				
	1	9	9	31887-1	TERM, PIDG RING #10	AMP	⚠
	AIR	10	10	18AWG (16x30) BLK	WIRE, UL STYLE 1015	PVC	⚠
	AIR	11	11	22AWG (7x30) YEL	WIRE, UL STYLE 1015	PVC	⚠
			12				
	AIR	13	13	20AWG (10x30) GRN	WIRE, UL STYLE 1015	PVC	⚠

SCALE **A** SIZE
 CODE IDENT **98438**
129459
 SHEET **2**
 REV **C**

WIRE LIST

7-10

WIRE LIST (Continued)

LINE NO.	TERMINATION INFORMATION						WIRE INFORMATION					ROUTING	LGTH (IN)
	CABLE NO.	WIRE NO. OR COLOR	FROM		TO		FIND NO./NOTES				WIRE OR CABLE		
			REF DES	PIN	REF DES	PIN	FROM END		TO END				
							CONN	TERMINATION	CONN	TERMINATION			
1													
2		YEL	SPKR		P5	2	SOLDER	6	7	11		15"	
3		YEL	SPKR		P5	3	SOLDER		7	11			
4													
5													
6		GRN	GRN POINT		P4	3	9	CONN FIBER ON TRAYS	7	13		23"	
7													
8		BLK	S1	3	F1	END	3		3	10		10 1/2"	
9													
10													
11													
12													
13													
14													
15													
16													
17													
18													
19													
20													
21													
22													
23													
24													
25													

CODE NOTES:

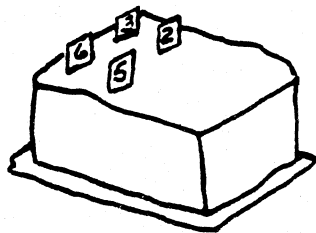
7-0601d (7-44)

SIZE	CODE IDENT		REV
A	98438	129459	C
SCALE		SHEET	3

WIRE LIST (Continued)

LINE NO.	CABLE NO.	TERMINATION INFORMATION					WIRE INFORMATION					ROUTING	LGTH
		WIRE NO. OR COLOR	FROM		TO		FIND NO./NOTES						
			REF DES	PIN	REF DES	PIN	FROM END		TO END		WIRE OR CABLE		
							CONN	TERMINATION	CONN	TERMINATION			
1	TRANSFORMER HOOK-UP (REF 129453)	YEL	T1	3	P3	1							
2		YEL		4		2							
3		RED		5		3							
4		RT/WH		6		4							
5		RED		7		5							
6													
7													
8													
9			ORN		8	F4	1						
10			ORN		9		2						
11													
12			BLK		1	S1	3						
13			BLK		2	F1	SIDE						
14													
15	PWR CORD 115 V (REF 129455)	BLK	PWR CORD		S1	2							
16		WHT			S1	5							
17		GRN			GRD POINT								
18													
19	PWR CORD 230 V (REF 129455)	BRN	PWR CORD		S1	2							
20		BLU			S1	5							
21		GN/YL			GRD POINT								
22													
23													
24													
25													

CODE NOTES:



REAR VIEW OF S1 (PWR SW)

SIZE A	CODE IDENT 98438	129459	REV C
SCALE		SHEET 4	

7-0001d (7-44)

WIRE LIST (Continued)

LINE NO.	CABLE NO.	TERMINATION INFORMATION					WIRE INFORMATION					ROUTING	LGTH
		WIRE NO. OR COLOR	FROM		TO		FIND NO./NOTES						
			REF DES	PIN	REF DES	PIN	FROM END		TO END		WIRE OR CABLE		
							CONN	TERMINATION	CONN	TERMINATION			
1	MONITOR HOOK-UP (REF 129481)	BRN	P7	1	MON F1	2							
2		RED		2		3							
3		ORG		3		4							
4		YEL		4		8							
5													
6		WHT		6		10							
7		GRN		7		5							
8		BLU		8		6							
9		VIO		9		9							
10		WHT		10		1							
11		BLK		11		7							
12													
13													
14													
15													
16													
17													
18													
19													
20													
21													
22													
23													
24													
25													

CODE NOTES:

7-0001d (7-64)

SIZE	CODE IDENT	REV
A	98438	B
SCALE		SHEET 5
		129459


APPENDIX A

REVISIONS

SYM	SHEET	DESCRIPTION	APPROVED	DATE
A		RELEASE PER DCN 1708 <i>en</i>	<i>J.D. Perkins</i>	12/2/80

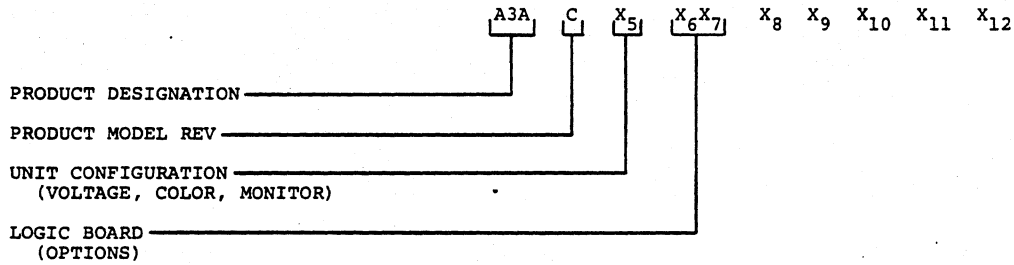
- 3. UNIT NOT CSA APPROVED.
 - 2. UNIT NOT UL APPROVED.
 - 1. ANY CONFIGURATION THAT IS NOT LISTED IS CONSIDERED AS A SPECIAL.
- NOTES UNLESS OTHERWISE SPECIFIED

RECORD OF REVISION STATUS OF EACH SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

		DR J PERKINS	12/2/80	 LEAR SIEGLER, INC. ELECTRONIC INSTRUMENTATION DIVISION, ANAHEIM, CALIF.	PRODUCT CONFIGURATOR ADM 3A	
		CHK <i>W. Perkins</i>	12/11/80			
		DSGN <i>J.D. Perkins</i>	12/1/80			
		ENGR				
		PROJ <i>A. Perkins</i>	12/1/80			
		REL <i>J.D. Perkins</i>	12/1/80			
ALL	END ITEM	APP'D <i>J.D. Perkins</i>	12/2/80	CODE IDENT NO	SIZE	REV
DASH NO.	NEXT ASSY	APP'D		98438	B	A
APPLICATION		DO NOT SCALE DRAWING		SCALE		SHEET 1 OF 2
						DISTR

[Handwritten scribble]

THE PRODUCT CODE CONFIGURATION FOR THE ADM-3A



X ₅	CODE	132504	UNIT CONFIGURATION	DASH NO.	SEE NOTE
1			115V-LT BLU/DK BLU-P4 MONITOR (WHITE)	-001	
2	EUROPEAN		230V-LT BLU/DK BLU-P4 MONITOR (WHITE)	-002	
3	CSA		115V-LT BLU/DK BLU-P4 MONITOR (WHITE)	-003	
4			115V-TAN/BRN . . . -P4 MONITOR (WHITE)	-004	
5	EUROPEAN		230V-TAN/BRN . . . -P4 MONITOR (WHITE)	-005	
6	CSA		115V-TAN/BRN . . . -P4 MONITOR (WHITE)	-006	
7					
8					
9					
A			115V-LT BLU/DK BLU-P4 MONITOR DIRECT ETCH (WHITE)	-00A	2
B	EUROPEAN		230V-LT BLU/DK BLU-P4 MONITOR DIRECT ETCH (WHITE)	-00B	
C	CSA		115V-LT BLU/DK BLU-P4 MONITOR DIRECT ETCH (WHITE)	-00C	3
D			115V-TAN/BRN . . . -P4 MONITOR DIRECT ETCH (WHITE)	-00D	2
E	EUROPEAN		230V-TAN/BRN . . . -P4 MONITOR DIRECT ETCH (WHITE)	-00E	
F	CSA		115V-TAN/BRN . . . -P4 MONITOR DIRECT ETCH (WHITE)	-00F	3
G			115V-LT BLU/DK BLU-PC110 MONITOR DATA VU (GREEN)	-00G	2
H	EUROPEAN		230V-LT BLU/DK BLU-PC110 MONITOR DATA VU (GREEN)	-00H	
I	CSA		115V-LT BLU/DK BLU-PC110 MONITOR DATA VU (GREEN)	-00I	3
J			115V-TAN/BRN . . . -PC110 MONITOR DATA VU (GREEN)	-00J	2
K	EUROPEAN		230V-TAN/BRN . . . -PC110 MONITOR DATA VU (GREEN)	-00K	
L	CSA		115V-TAN/BRN . . . -PC110 MONITOR DATA VU (GREEN)	-00L	3

X ₆ X ₇	CODE	132501	LOGIC BOARD	DASH NO.	SEE NOTE
00	STD BD			-000	
01	STD BD	LOWER CASE - SOCKETS & HEADERS		-001	
02	STD BD - SOCKETS & HEADERS - EXTENSION PORT CURRENT LOOP		-002	
03	STD BD	LOWER CASE - SOCKETS & HEADERS - EXTENSION PORT CURRENT LOOP		-003	
04	STD BD - SOCKETS & HEADERS		-004	


CODE IDENT NO.	SIZE	PL132500	REV
98438	B		A
SHEET			2

REVISIONS																	
SYM	SHEET	DESCRIPTION												APPROVED	DATE		
A		INC DCN 490												B. HYDEMAN	1-18-80		
B		INC DCN 566												J.E.K.			
C		INC DCN 590												B. HYDEMAN	2-11-80		
D		INC DCN 922												W. KELLY	5-23-80		
E		REVISED & REDRAWN PER DCN 1074 <i>2m 10-7-80</i>												L. SUJGER W. KELLY L. SUJGER W. KELLY	5-23-80 5-23-80 5-23-80 8-11-80		

NOTES:

- ANY CONFIGURATION THAT IS NOT LISTED IS CONSIDERED A SPECIAL. ENGINEERING MUST ASSIGN NUMBER.
- LSI PART NUMBER IS 131551 - X₅X₆X₇
(FROM PRODUCT CODE ABOVE)

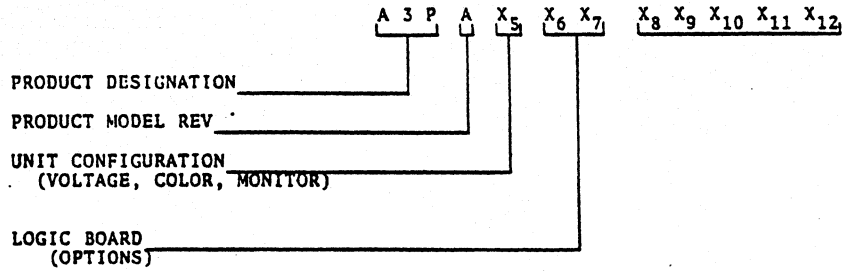
RECORD OF REVISION STATUS OF EACH SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

DR	<i>[Signature]</i>	<i>11/2/80</i>	 LEAR SIEGLER, INC. ELECTRONIC INSTRUMENTATION DIVISION, ANAHEIM, CALIF. CONFIGURATOR FOR ADM-3A+
CHK			
DSGN			
ENGR	<i>[Signature]</i>	<i>11/2/80</i>	
PROJ	<i>[Signature]</i>	<i>5/2/80</i>	
REL	<i>[Signature]</i>	<i>11/2/80</i>	
APP'D	<i>[Signature]</i>	<i>11/2/80</i>	
APP'D			

CODE IDENT NO	SIZE	REV
98438	B	E
PL 131551		

DASH NO.	NEXT ASSY	APPLICATION	DO NOT SCALE DRAWING	SCALE	SHEET 1 OF 2
					DISTR

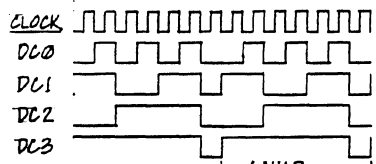
THE PRODUCT CODE CONFIGURATION FOR THE ADM-3A+



X ₅	CODE	131564	UNIT CONFIGURATION
1	-	.115V - LT BLU/DK BLU	- P4 MONITOR (WHITE) (ZENITH)
2	-	EUROPEAN 230V - LT BLU/DK BLU	- P4 MONITOR (WHITE) (ZENITH)
3	-	.CSA 115V - LT BLU/DK BLU	- P4 MONITOR (WHITE) (ZENITH)
4	-	.115V - TAN/BRN	- P4 MONITOR (WHITE) (ZENITH)
5	-	EUROPEAN 230V - TAN/BRN	- P4 MONITOR (WHITE) (ZENITH)
6	-	.CSA 115V - TAN/BRN	- P4 MONITOR (WHITE) (ZENITH)
7			
8			
9			
A	-	.115V - LT BLU/DK BLU	- PC110 MONITOR (GREEN) (BALL)
B	-	EUROPEAN 230V - LT BLU/DK BLU	- PC110 MONITOR (GREEN) (BALL)
C	-	.CSA 115V - LT BLU/DK BLU	- PC110 MONITOR (GREEN) (BALL)
D	-	.115V - TAN/BRN	- PC110 MONITOR (GREEN) (BALL)
E	-	EUROPEAN 230V - TAN/BRN	- PC110 MONITOR (GREEN) (BALL)
F	-	.CSA 115V - TAN/BRN	- PC110 MONITOR (GREEN) (BALL)
G			
H			

X ₆ X ₇	CODE	131563	LOGIC BOARD
0 0			STD RD
0 1			STD BD - EXT CL

CODE IDENT NO.	SIZE	REV
98438	B	E
PL 131551		
SHEET 2 of 2		



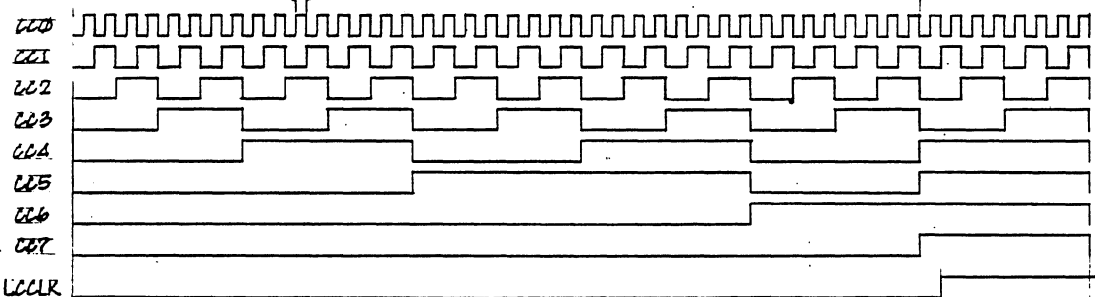
PERIOD=91.8577 msec, FREQUENCY=10.8864 MHz

DOT COUNTER

VIDEO S.R. LOAD PERIOD=643.0039 msec, FREQUENCY=1.5552 MHz

PROPERTY OF LITTON INDUSTRIES, INC. ALL RIGHTS RESERVED. THIS DOCUMENT IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE BY CONTROLLED INFORMATION. IT IS THE PROPERTY OF LITTON INDUSTRIES, INC. AND IS NOT TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM.

LTR	A
DWG NO.	131549
SIZE	C
CODE IDENT NO.	98438
SCALE	
SHEET	14



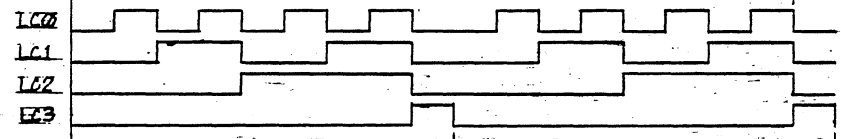
POSITION COUNTER

PERIOD=61.7284 usec
FREQ=16.2000 KHZ

COUNTER RETRADE
CBUF RETRADE
VIDEO RETRADE

PULSE WIDTH=24.434 usec
NOTE: HDRIVE STARTS ONE CHAR TIME (643 msec) AFTER LAST VIDEO

HDRIVE

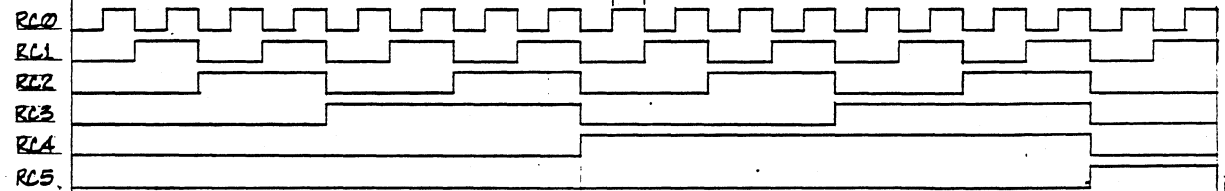


LINE COUNTER

PERIOD=555.555 usec, FREQUENCY=1.8000 KHZ

ROW COUNTER

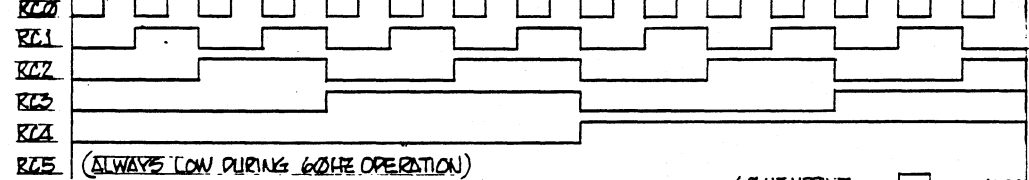
50 HZ OPERATION



PERIOD=20 ms
FREQ=50 HZ

50 HZ VDRIVE EDGES LOCKED W/HDRIVE RISE

60 HZ OPERATION



PERIOD=16.667 msec, FREQ=60 HZ

60 HZ VDRIVE CLOKED W/HDRIVE RISE

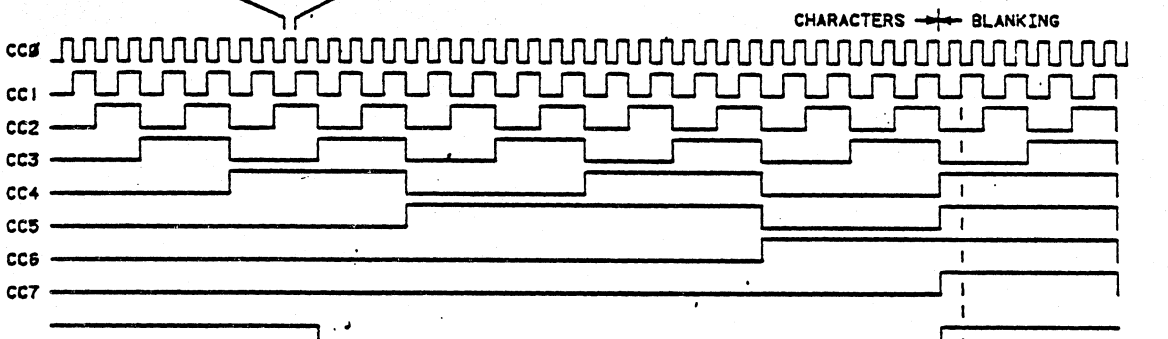
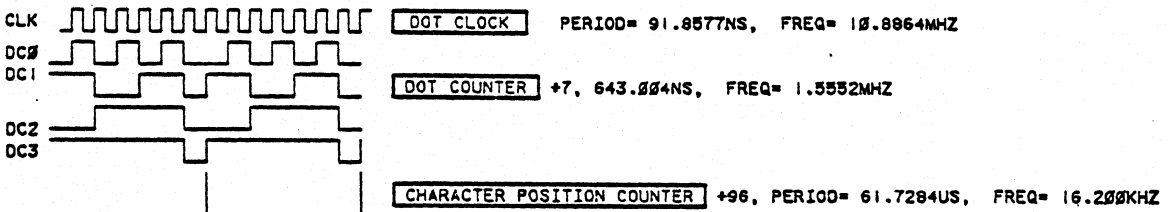
(ALWAYS LOW DURING 60 HZ OPERATION)

ADM-3 TIMING DIAGRAM

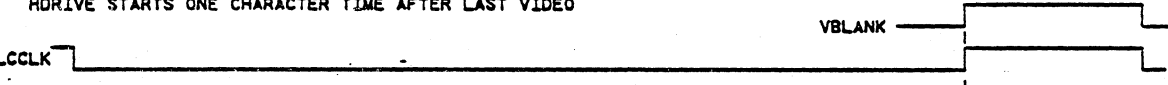
1
2
3
4

REVISIONS
DATE APPROVED

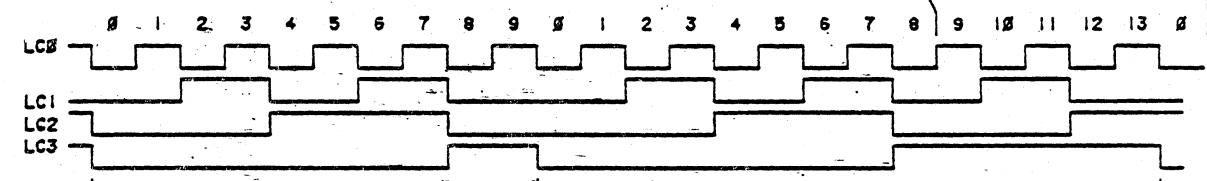
SHT ZONE LTR



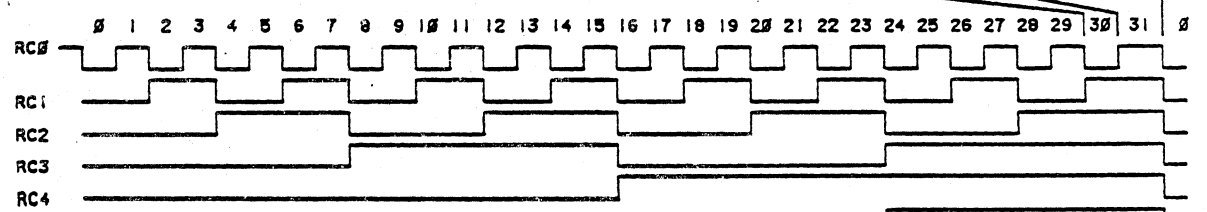
HDRIVE
NOTE:
HDRIVE PULSE WIDTH= 25.00US
HDRIVE STARTS ONE CHARACTER TIME AFTER LAST VIDEO



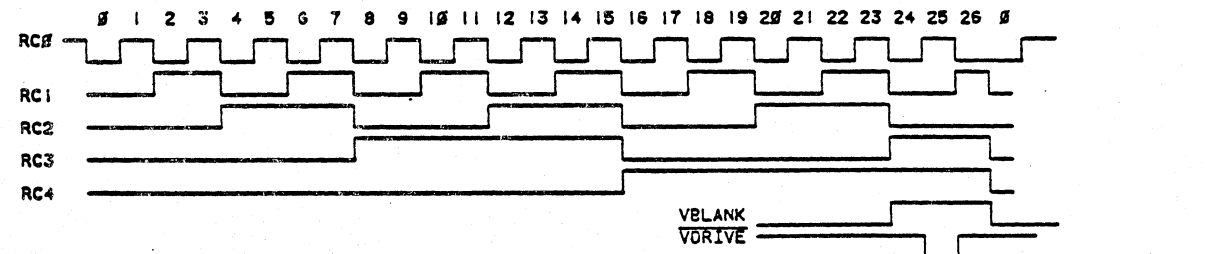
LINE COUNTER +10, PERIOD= 617.28US, FREQ= 1620HZ



ROW COUNTER
50HZ OPERATION + 32.4, PERIOD= 20 MS,
FREQ= 50HZ,



60HZ OPERATION + 27, PERIOD= 16.667MS, FREQ= 60HZ



ADM3A+ TIMING DIAGRAM

LTR C

DWG NO. 131562

FSCM NO. 98439

SIZE C

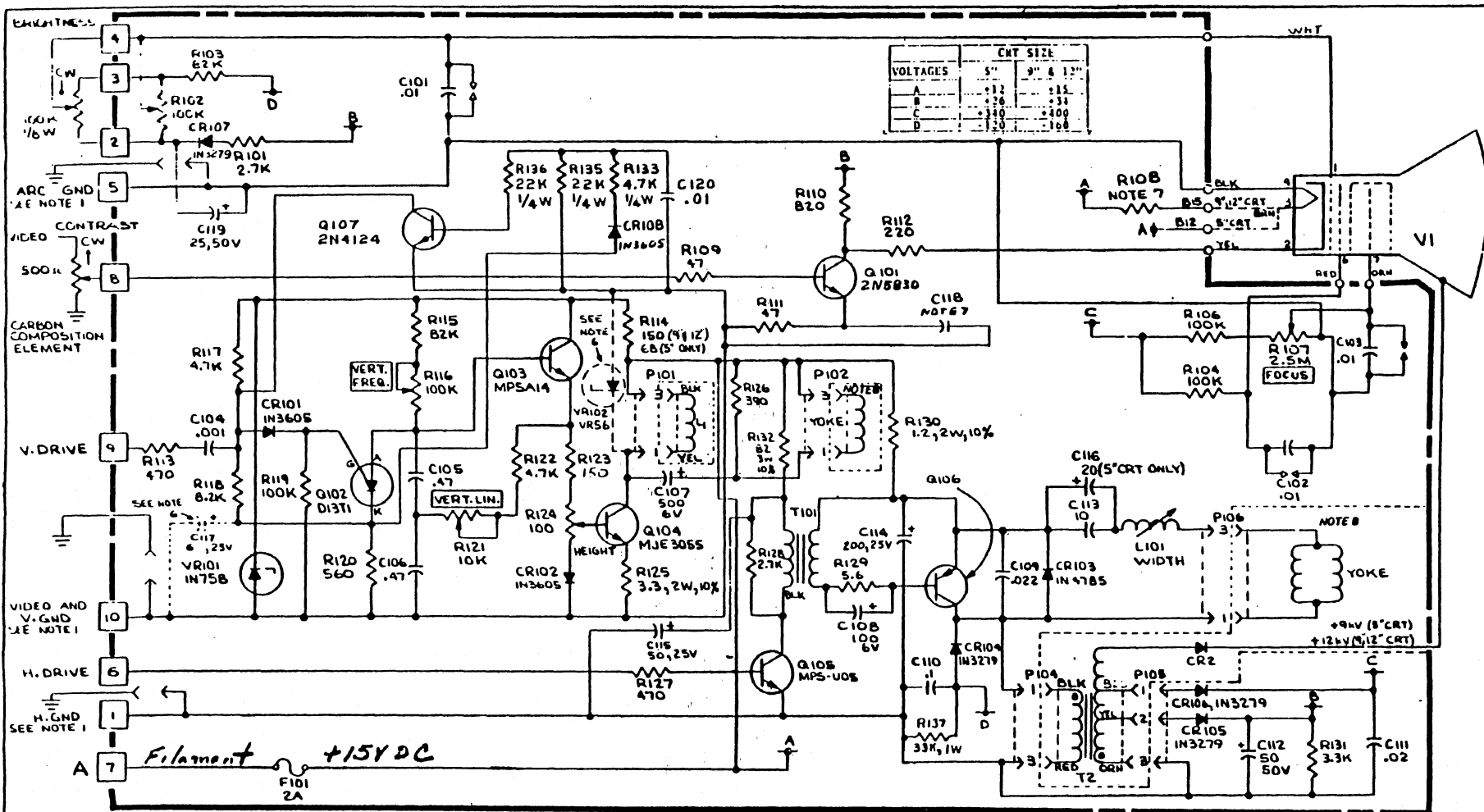
SCALE NONE

SHEET 17-118

PROPRIETARY LITSEAD
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE
DRAWINGS AND CONTAINED INFORMATION ARE UNCLASSIFIED
UNLESS INDICATED OTHERWISE. THIS INFORMATION IS
REPRODUCIBLE IN WHOLE OR IN PART WITHOUT PERMISSION
FROM THE ORIGINAL SOURCE.

D C A B A

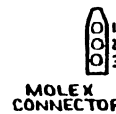
SCHEMATIC, TV9 AND 12 WITH POWER SUPPLY



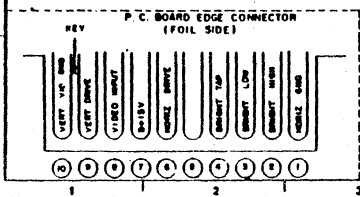
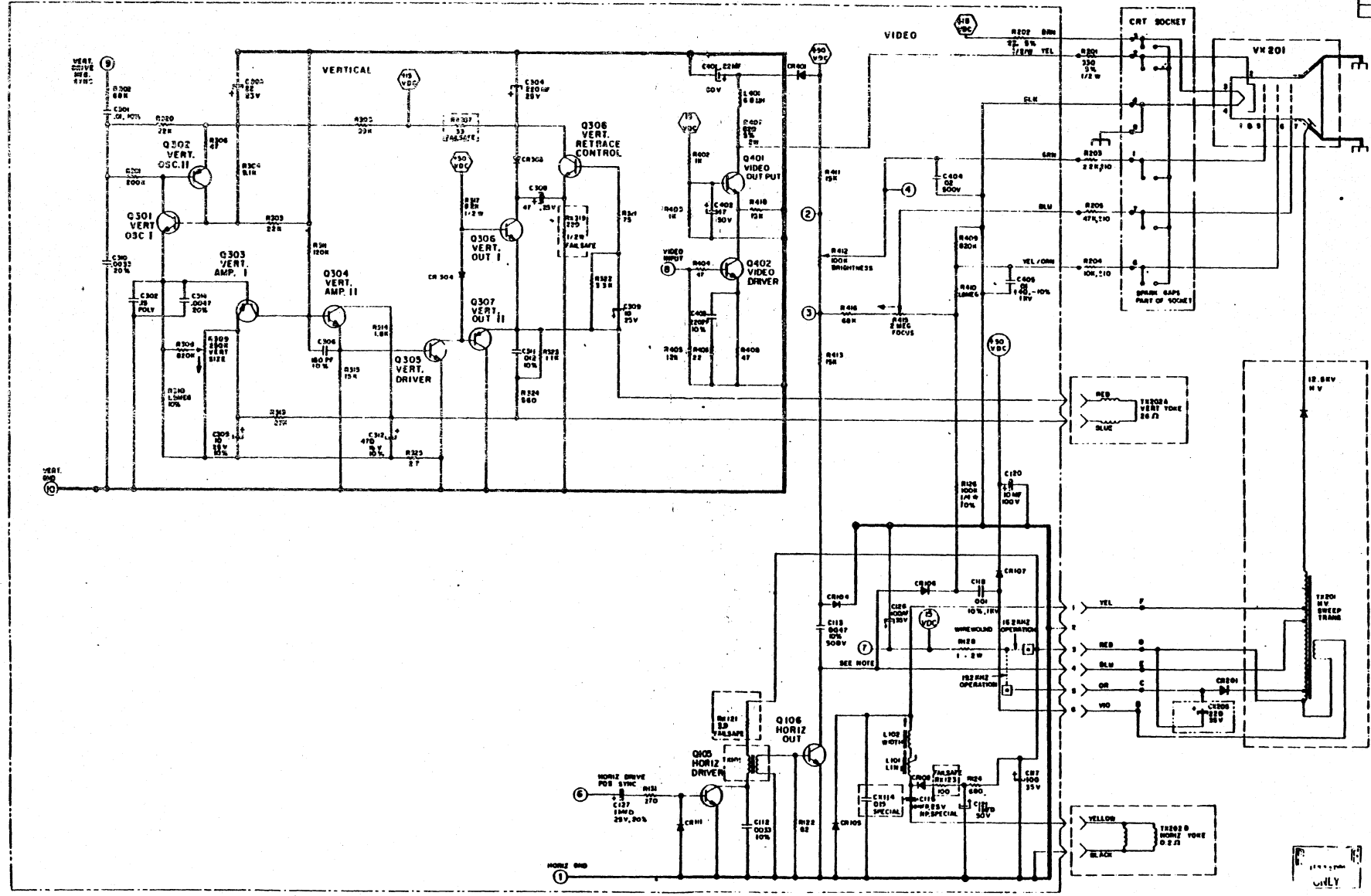
7. FOR PROPER VALUE REFER TO PARTS LIST SECTION 4 OF INSTRUCTION MANUAL.
 B. YOKE LEAD IDENTIFICATIONS: P106-BLUE AND RED LEADS, P102-BROWN AND YELLOW LEADS.

NOTES: UNLESS OTHERWISE SPECIFIED

- SEE SECTION 2.2 OF MANUAL.
- ← ← DENOTES MOLEX PIN CONNECTOR.
- ALL RESISTORS ARE 1/2 W ± 5%.
- ALL CAPACITORS ARE IN UF.
- DENOTES PRINTED CIRCUIT CARD EDGE CONNECTOR.
- C17 MUST BE ADDED AND P12C MUST BE SWAPPED TO 910Ω IF NON-STANDARD VERTICAL CPIPE IS USED. VR102 IS ADDED FOR OVERSCAN IN VERTICAL CONDITION.



FIRST USED ON		TITLE	SCHEMATIC
VERSION A(A TO Z)	SHEET 1 OF 1	SIZE	TV-5,9,12
		DRAWING NO.	1.024-0509
		REV.	H



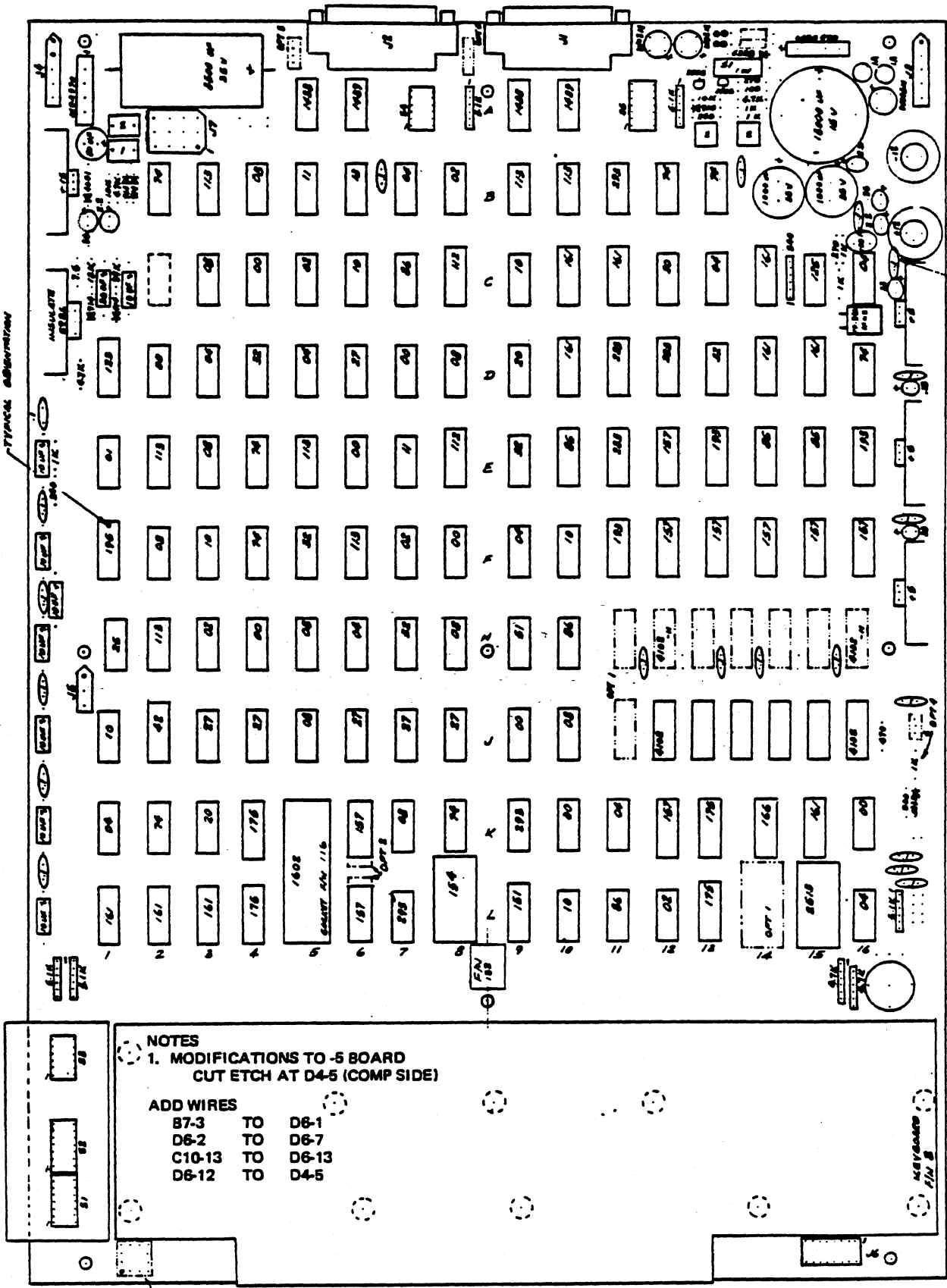
○ = DC VOLTAGE SOURCE
 ○ = DC VOLTAGE APPLIED
 NOTE 1: CUSTOMER SUPPLIED EXTERNAL DC SOURCE ON PIN 7 EDGE CONNECTOR

SHEET 2

SCHEMATIC FOR
 D12 VIDEO DISPLAY
 16.2 KHZ HORIZ. SCAN FREQ

ZENITH
 RADIO CORP.
 CHICAGO 91

123-5498



MOUNT CAP TO PREVENT SHORT
TO HEAT SINK

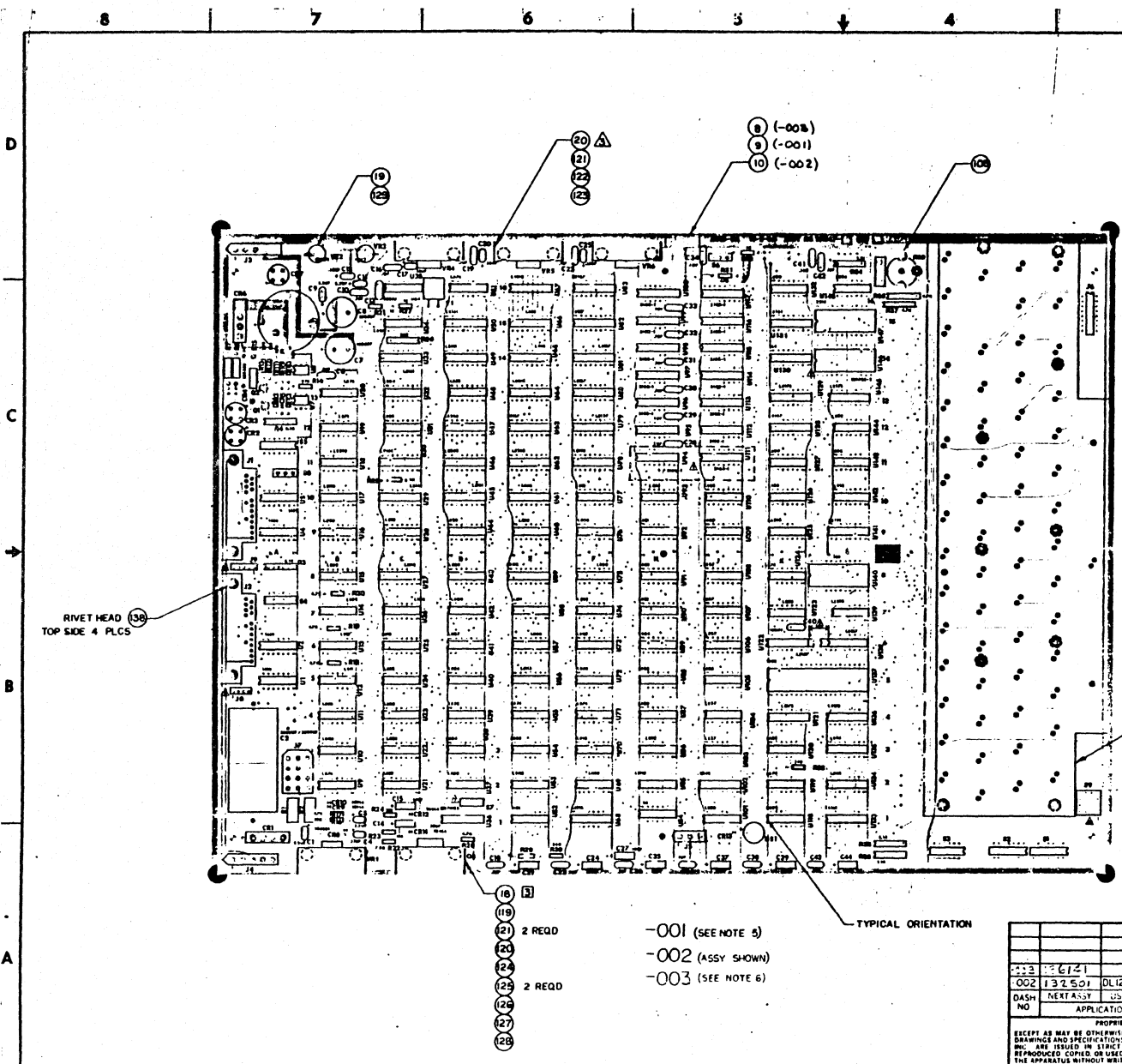
-1 -11 ASSY

NOTES
 1. MODIFICATIONS TO -5 BOARD
 CUT ETCH AT D4-5 (COMP SIDE)

ADD WIRES

B7-3	TO	D6-1
D6-2	TO	D6-7
C10-13	TO	D6-13
D6-12	TO	D4-5

P.C. BOARD ASSEMBLY



REVISIONS					
SHT	ZONE	LTR	DESCRIPTION	DATE	APPROVED
		B	PROD RELEASE PER DCN # 1669	12-2-81	[Signature]
		C	INC DCN # 1835	12-2-81	[Signature]
		D	INC DCN # 2207	12-2-81	[Signature]
		E	INC DCN # 2325	JED 5-4-81	[Signature]
		F	INC DCN # 2336	JED 8-4-81	[Signature]
		G	INC DCN # 2320	JED 5-4-81	[Signature]
		H	INC DCN # 2374	JED 5-4-81	[Signature]
		J	INCORP DCN # 2456	12-2-81	[Signature]
		K	INCORP DCN # 2751, D-2758	12-2-81	[Signature]
		L	INCORP DCN # 2674	12-2-81	[Signature]
		M	INCORP DCN # 2796	12-2-81	[Signature]
		N	INCORP DCN # 2667	12-2-81	[Signature]
		P	INCORP DCN 3087	12-2-81	[Signature]
		R	INCORP DCN 3179	12-2-81	[Signature]
		S	INCORP DCN 3240	12-2-81	[Signature]
		T	INCORP DCN 3157	12-2-81	[Signature]
		U	INCORP DCN 3150	12-2-81	[Signature]

- NOTES: UNLESS OTHERWISE SPECIFIED
- FOR SCHEMATIC REFER TO 131549
 - FOR PRINTED WIRING BOARD REFER TO 131548
 - FOR HEATSINK MTG INSTRUCTIONS REFER TO 131579
 - FOR OPTIONS REFER TO NEXT ASSY 132500 AND CONFIGURATION DWG 132511 CODED ON PWB AS INDICATED BELOW.
 - ▲ LOWER CASE.
 - ▲ ANSWER BACK. (SMD)
 - ▲ NUMERIC KEY PAD. (SMD)
 - ▲ DISPLAY TEST.
 - ▲ EXTENSION PORT CURRENT LOOP.
 - ▲ SPLIT BAUD RATE. (SMD)
 - ▲ 72 COLUMN BEEP DEFEAT. (SMD)
 - REWORK INSTRUCTIONS FOR PWB 131548-002 (131547-001 ASSY).
 - CUT PIN 4 ON U50 (74LS161) AT SEATING PLANE.
 - JUMPER U50, PIN 4 TO PIN 5 WITH BARE 26 AWG WIRE ON COMPONENT SIDE.
 - CUT ETCH ACROSS CR10 (REAR SIDE).
 - JUMPER FROM ANODE OF CR9 TO CATHODE OF CR10.
 - 003 ASSY TO BE THE SAME AS -002 EXCEPT FOR ITEMS 8 THRU 12.

FOR PARTS SEE P/L 131547


- 001 (SEE NOTE 5)
- 002 (ASSY SHOWN)
- 003 (SEE NOTE 6)

UNLESS OTHERWISE SPECIFIED		CONTR NO		LEAR SIEGLER, INC.	
DIM IN INCHES		DR S FLEWERN		DATA PRODUCTS DIVISION	
TOLERANCES:		CHK [Signature]		ANAHEIM, CALIFORNIA 92803	
X ± .1		ENGR: [Signature]		P/C BOARD ASSEMBLY	
XX ± .01		PROJ: [Signature]		ADM 3A	
ANGLES 40°		REL [Signature]		SCALE 1/1	
APPLICATION		APPD		SIZE FSCM NO	
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC. AND ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION		APPD		DWG NO	
				D 98438 131547	
				SHEET 1 OF 1	

REVISIONS

LTR	SHEET	DESCRIPTION	DATE	APPROVED
A		RELEASE PER DCN 1511 T.E.S. 10-24-80	10/30/80	<i>[Signature]</i>
B		INCORP DCN# 1555 DWA 1-19-81	1-29-81 1/30/81	<i>[Signature]</i>
C		INCORP DCN# 1835 JWB 3-23-81	3-30-81	<i>[Signature]</i>
D		INCORP DCN# 2307 JED 5-6-81	5-6-81 5-11-81	<i>[Signature]</i>
E		INCORP DCN# 2325 JED 5-6-81	5-6-81	<i>[Signature]</i>
F		INCORP DCN# 2336 JED 5-6-81	5-6-81	<i>[Signature]</i>
G		INCORP DCN# 2326 JED 5-6-81	5-6-81 5-12-81	<i>[Signature]</i>
H		INCORP DCN# 2374 JED 5-6-81	5-6-81	<i>[Signature]</i>
J		INCORP DCN# 2456 5-26-81 S. FIGUEROA	5-27-81 6-27-81	<i>[Signature]</i>
K		INCORP DCN# 2751, D-2758 ESC 8-18-81	8-24-81	<i>[Signature]</i>
L		INCORP DCN# 2674 ESC 8-18-81	8-24-81	<i>[Signature]</i>
M		INCORP DCN# 2796 ESC 8-18-81	8-24-81	<i>[Signature]</i>
N		INCORP DCN# 2667 ESC 10-1-81	10-1-81 10-5-81	<i>[Signature]</i>
P		INCORP DCN 3087 RM 11-16-81	12-2-81 12-2-81	<i>[Signature]</i>
R		INCORP DCN 3179 RM 11-16-81	12-2-81 12-6-81	<i>[Signature]</i>
S		INCORP DCN 3240 SF 12-2-81	12-2-81	<i>[Signature]</i>
T		INCORP DCN 3157 SF 12-2-81	12-2-81 12-6-81	<i>[Signature]</i>
U		INCORP DCN 3130 SF 12-2-81	12-2-81 12-6-81	<i>[Signature]</i>

-003	136141	DL129450
-002	132501	DL129450
DASH NO.	NEXT ASSY	USED ON
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIM. IN INCHES TOLERANCES X ± .1 .XX ± .03 .XXX ± .010 ANGLES ± 0.5° MACH. FIN. J	DR T.E.S. 9-17-80	 LEAR SIEGLER, INC. ELECTRONIC INSTRUMENTATION DIV. ANAHEIM, CALIF.	P.C. BOARD ASSY ADM-3A	
	CHK S. Figueroa 10/24/80			
	DSGN W. Kelly 10-27-80	SIZE	CODE IDENT	PTV
	ENGR	A	98438	U
	PROJ	SCALE	PL131547	SHEET 1 OF 7
REL D. Hayden 10/30/80	CUSTOMER APPD			

FIND NO.	QTY REQD			STOCK NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REMARKS
	.003	.002	.001				
1			✓		-001	P.C. BOARD ASSY. 24 LINE	
2		✓			-002	" " "	"
3	✓				-003	" " "	"
4	REF	REF	REF		131549	SCHEMATIC	
5	REF	REF	REF		132511	OPTIONS CONTROL DWG	
6							
7							
8	1	0	0		131548-004	PRINTED WIRING BOARD	
9	0	0	1		131548-002	PRINTED WIRING BOARD	
10	0	1	0		131548-003	PRINTED WIRING BOARD	
11	0	1	1		129451-03	KEYBOARD	
12	1	0	0		130143-001	KEYBOARD	
13	1	1	1		129457-03	LEGEND PLATE	
14	2	2	2		129486-03	SPACER, LEGEND PLATE	
15							
16	1	1	1		811003	CRYSTAL, 10.8864MHZ	Y1
17							
18	1	1	1		129474-03	HEAT SINK	FOR Q3
19	2	2	2		820002	" "	FOR VR2, 3
20	4	4	4		129474-09	" "	FOR VR1, 4, 5, 6
21							
22	1	1	1		128348-H04	IC	U35
23	1	1	1		-01		U52
24	1	1	1		-25		U84
25	1	1	1		-159		U140

SIZE
A

FSCM NO.
98438

SH 2
PL 131547

REV
D

FIND NO.	QTY REQD			STOCK NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REMARKS
	.003	.002	.001				
26	1	1	1		128348-166	I.C.	U130
27	2	2	2		-1488		U1, U4
28	2	2	2		-1489		U2, U5
29	1	1	1		-1602		U137
30	1	1	1		-2513		U147
31	12	12	12		-2102A		U95-U100 U112-U117
32	3	3	3		-7805		VR4,5,6
33	1	1	1		-78M12		VR3
34	1	1	1		-7815		VR1
35	1	1	1		-79M12		VR2
36	1	1	1		-123A		U36
37	10	10	10		129467-00	I.C. LS TYPE	U23,37,42,57,75 87,101,109,126,132
38	5	5	5		-02		U15,24,74,86,144
39	9	9	9		-04		U14,32,38,40,76 89,118,127,148
40	10	10	10		-08		U11,22,43,54,69 88,91,105,110,123
41	5	5	5		-10		U25,28,70,77,142
42	2	2	2		-11		U12,58
43	1	1	1		-13		U13
44	3	3	3		-20		U31,44,120
45	6	6	6		-27		U41,103,104,106, 107,108
46	6	6	6		-32		U21,39,48,60,72, 90
47	1	1	1		-42		U102
48	1	1	1		-51		U92
49	8	8	8		-74		U9,19,20,51,55, 71,119,124
50	3	3	3		-85		U61,65,66

SIZE
A
FSCM NO.
98438

SH 3
PL1315A7

REV
U

FIND NO.	QTY RECD			STOCK NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REMARKS
	001	002	003				
51	3	3	3		129467-86	I.C. LS TYPE	U26, 93, 143
52	2	2	2		-112		U27, 59
53	7	7	7		-113		U10, 16, 17, 53, 56 73, 85
54	1	1	1		-125		U34
55	1	1	1		-151		U141
56	9	9	9		-157		U63, 79, 80, 81, 82, 83 122, 128, 138
57	10	10	10		-161		U29, 30, 33, 45, 49, 50 131, 133, 134, 135
58	4	4	4		-175		U121, 129, 136, 145
59	3	3	3		-193		U64, 67, 78
60	1	1	1		-195		U68
61	3	3	3		-283		U46, 47, 62
62	3	3	3		-293		U18, 125, 139
63							
64	2	2	2		808001	BRIDGE	CR1, CR6
65	3	3	3		808008	BRIDGE	CR2, CR3, CR7
66	1	1	1		129498-02	OPTICAL ISOLATOR	U7 (XMTR)
67	1	1	1		129498-01	OPTICAL ISOLATOR	U8 (RCVR)
68	1	1	1		810001	TRANSISTOR	Q2
69	1	1	1		810003	"	Q1
70	1	1	1		810005	" MJE2955	Q3
71	5	5	5		808078	DIODE, IN4148	CR5, 9, 10, 11, 12
72	1	1	1		808004	"	CR8
73	1	1	1		808007	DIODE ZENER 5.1V 5%	CR4
74							
75							

SIZE
A

FSCM NO.
98438

SH 4
PL 131547

REV
U

FIND NO.	QTY REQD			STOCK NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REMARKS
	003	002	001				
76	1	1	1		129468-189	CAP, 18000 UF 15V	C3
77	2	2	2		-108	" 1000 UF 35V	C7, C8
78							
79	8	8	8		129469-106	CAP. 10UF 25V	C15, 21, 24, 27, 35 37, 39, 44
80	1	1	1		-306	30UF 6V	C14
81	1	1	1		-358	3500UF 35V	C2
82	20	20	20		129329-104	.1UF 50V	C6, 10, 16, 18, 19, 22, 23, 26, 28 29, 30, 31, 32, 33, 34, 43, 36, 38 41, 42
83	2	2	2		128518-101	100PF	C13, 40
84	4	4	4		-225	2.2UF 25V	C1, 5, 9, 11
85	5	5	5		-334	.33UF 35V	C4, 12, 17, 20, 25
86							
87	1	1	1		801006	POTENTIOMETER	R39
88							
89	1	1	1		129476-241	RES. MOD. 240Ω	R26
90	2	2	2		-472	" " 4.7K	R37, 38
91	5	5	5		-512	" " 5.1K	R3, 4, 34, 35, 36
92							
93	1	1	1		128533-101	RES. CARB. COMP. 100, 25W5%	R12
94	5	5	5		-102	1K	R21, 25, 27, 29, 32
95	1	1	1		-103	10K	R16
96	1	1	1		-183	18K	R23
97	3	3	3		-241	240	R5, 30, 33
98	1	1	1		-271	270	R13
99	1	1	1		-393	39K	R24
100	2	2	2		-471	470	R11, 31

A

SIZE

98438

FSCM NO.

SH 5

PL131547

HEV

U

FIND NO.	QTY RECD			STOCK NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REMARKS
	001	002	003				
101	5	5	5		128533-47Z	RES. CARB. COMP 4.7K	R17,18,19,20,28
102	1	1	1		-7R5	" " " 7.5	R22
103							
104	1	1	1		80307Z	" " " 51,1W,5%	R15
105	1	1	1		80300Z	RES. WW, 2, 3W, 5%	R1
106	1	1	1		803001	" " " " "	RZ
107							
108	1	1	1		806001	KNOB	FOR R39
109	2	2	2		804006	SWITCH 6 POS	S3,4
110	3	3	3		804007	" 7 POS	S1,2,5
111	1	1	1		809007	WAFERCON 3 CIR KEY1	J5
112	1	1	1		809008	" 5 CIR " 1	J3
113	1	1	1		809009	" 5 CIR " 1#2	J4
114	1	1	1		80901Z	" 12 CIR " 1	J7
115	2	2	2		129478-01	CONN	J1, J2
116	1	1	1		802034	SOCKET 40 PIN	FOR U137
117	3	3	3		802031	" 16 PIN	J6, U94, U111
118	2	2	2		804026	SWITCH	S6,8,
119	1	1	1		839001	INSULATOR	XQ3
120	1	1	1		839044	#4 SHOULDER WASHER, NYLON	
121	20	20	20		821404	SCREW, PAN HD, SLOTTED BRASS, NIC. PL.	
122	4	4	4		823604	LOCKWASHER, STL, CAD, PL.	
123	4	4	4		821625	SCREW PAN HD SLOTTED BRASS NIC. PL.	
124	1	1	1		822401	NUT, HEX 4-40 STL, CAD PL	FOR Q3
125	1	1	1		823404	WASHER, FLAT, CAD PL STL	FOR Q3

SIZE
A

FSCM NO.
98438

SH 2
PL131547

REV
U

FIND NO.	QTY RECD			STOCK NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REMARKS
	003	004	001				
126	1	1	1		823410	LOCKWASHER, STL, CAD. PL. #4	FOR Q3
127	1	1	1		839003	INSULATOR, SCREW (4x 1/32)	" Q3
128	1	1	1		821411	SCREW, 4-40 x 1/2	FOR Q3
129	2	2	2		839012	INSULATOR	FOR VR2,3
130							
131							
132	1	1	1		128533 - 200	RES. CARB. COMP. 20, 1/4W, 5%	R10
133	1	1	1		-561	560	R9
134	1	1	1		-123	12K	R6
135	1	1	1		-913	91K	R14
136	2	2	2		802032	SOCKET 18 PIN	XU122, XU138
137	1	1	1		802033	24 PIN SOCKET	FOR U146
138	4	4	4		824002	RIVET, SIMI-TUBE	
139	4	4	4		129473-3	JACK SOCKETS	
140							
141							
142							
143							
144							
145							
146							
147							
148							
149							
150							

SIZE

FSCM NO. 98438

SH 7

PL131547

U

APPENDIX B

4

3

2

1

CONN PIN ASSIGNMENTS

SWITCH ASSIGNMENTS

SHT			REVISIONS	
ZONE	LTR	DESCRIPTION	DATE	APPROVED


CONN PIN	FUNCTION	SHT	CONN PIN	FUNCTION	SHT
J1 1	FRAME GND		J3 1	9.4 VAC	13D3
MADEM 2	BA	10A1	PWR 2	9.4 VAC	13D3
RS232 3	RCVD DATA	6D4	INPUT 3	31 VAC	13B3
4	CA	12A1	4	GND	13B3
5	CB	12D4	5	31 VAC	13B3
6	CC	12C4			
7	GND		J4 1	20.5 VAC	13B3
8	CF	12B4	2	20.5 VAC	13A3
9	**		PWR 3	FRAME GND	13A3
10			INPUT 4		
11	SA	12B1	5		
12	SB	12A4			
13	**		J5 1		
14	**		2	SPKR	3D1
15	**		3	SPKR	3D1
16	**				
17	CL OUT	10B1	J6 1	ROW C	9C3
18	**		2	COL 3	9B3
19	**		NUMERIC 3	COL 2	9B3
20	CD	12C1	KEYPAD 4	ROW E	9C3
21	**		OUTPUT 5	ROW F	9C4
22	READ BACK EN	7C4	OPTION 6	ROW 9	9C4
23	CL INPUT	10D4	7	ROW 8	9C4
24	CL OUT	10A1	8	ROW 7	9C4
25	CL INPUT	10D4	9	ROW 1	9C4
			10	ROW 2	9C4
J2 1	FRAME GND		11	ROW 3	9C4
EXTEN. 2	BA	10A4	12	ROW 4	9C4
RS232 3	BB	6D3	13	ROW 5	9C4
4	CA	12A2	14	ROW 6	9C4
5	CB	12D3	15	ROW D	9C3
6	CC	12C3	16	COL F	9B3
7	GND				
8	CF	12B3	J7 1	(KEY PIN)	
9	**		2		
10	-12V *		3		
11	SA	12B3	4	VIDEO	8A1
12	SB	12A3	5	VIDEO RET	8A1
13	**		6		
14	**		7		
15	**		8	H DRIVE	7C1
16	**		9	V DRIVE	7D1
17	+12V *		10	GND	13A1
18	**		11	+15V	13B1
19	**		12		
20	CD	12C3			
21	**				
22					
23					
24	EXT CL IN *				
25	EXT CL OUT *				

SWITCH	SECTION	FUNCTION	SHT
S1 7		1800	11B4
6		1200	11B2
5		600	11B2
4		300	11B2
3		150	11C2
2		110	11C4
1		75	11C2
S2 7		AUTO NEWLINE 404	
6		CL	10C3
5		FDX/HDX	6D4
4		19200	11B2
3		9600	11B2
2		4800	11B2
1		2400	11B2
S3 6		BIT 8	10B3
5		PAR INH	10B3
4		STOP BIT	10B3
3		WORD LG	10B3
2		EVEN PAR	10B3
1		UPPER CASE	9A4
S4 6		SPACE	4D4
5		UP CASE DISP	8A4
4		DYS LOCK	10C2
3		DYS CLR SCRN	3D4
2		50/60 HZ	2A4
1		12/24 LINE	3B3
S5 7		CUR MODE	7C2
6		LOCAL	12A2
5		103	12A1
4		202	12B2
3		MODE	12C4
2		ETX	12C4
1		EOT	12C4

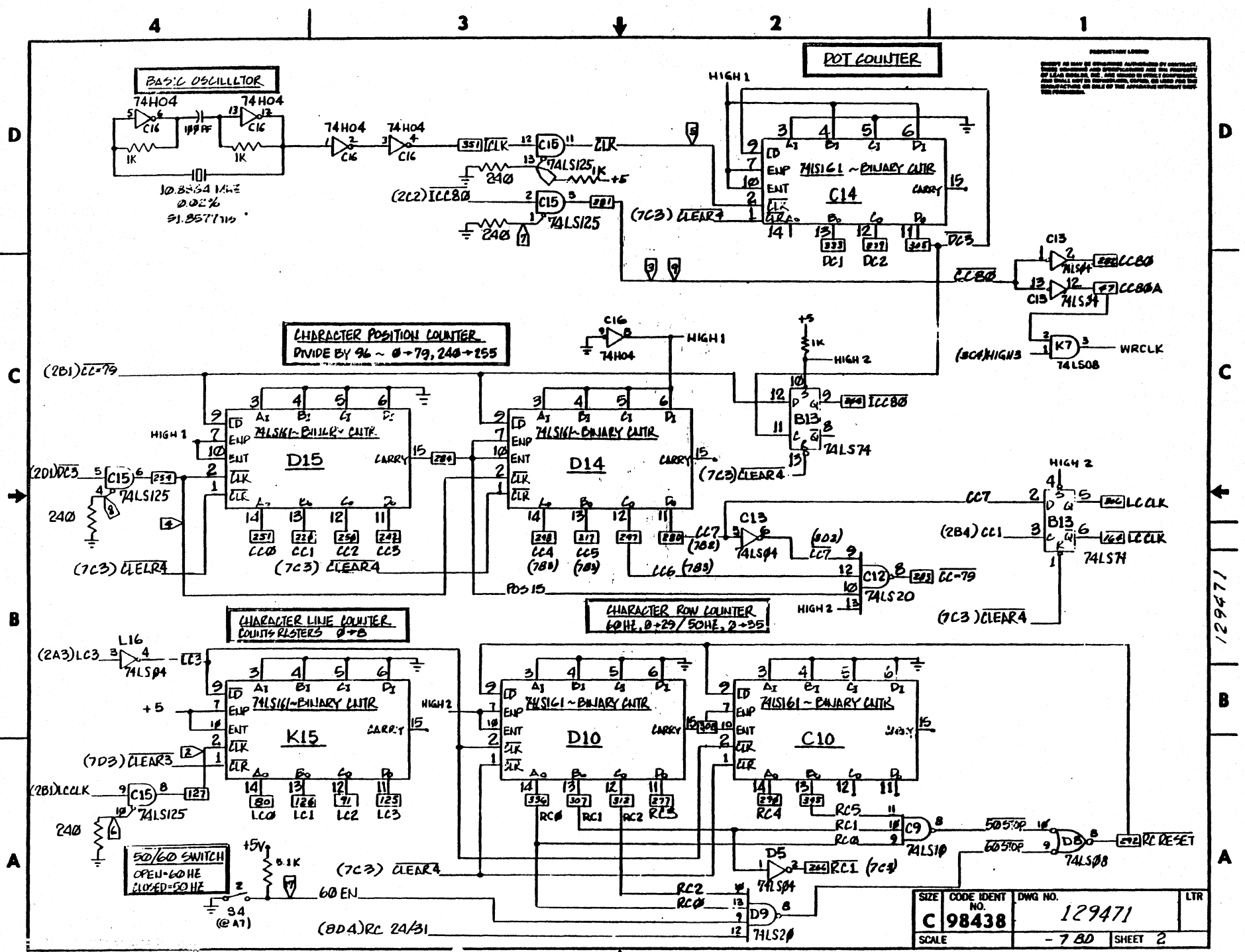
SYMBOLS XXX, X, Y ARE TEST POINTS SHOWN FOR REF ONLY.

* WHEN OPTIONAL EXTENSION PART CURRENT LOOP INSTALLED
** NO SOCKET INSTALLED CONNECTOR

EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DIMENSIONS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC. AND SHALL BE STRICTLY CONFIDENTIAL AND SHALL NOT BE REPRODUCED, COPIED, OR LOANED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT THE WRITTEN PERMISSION.

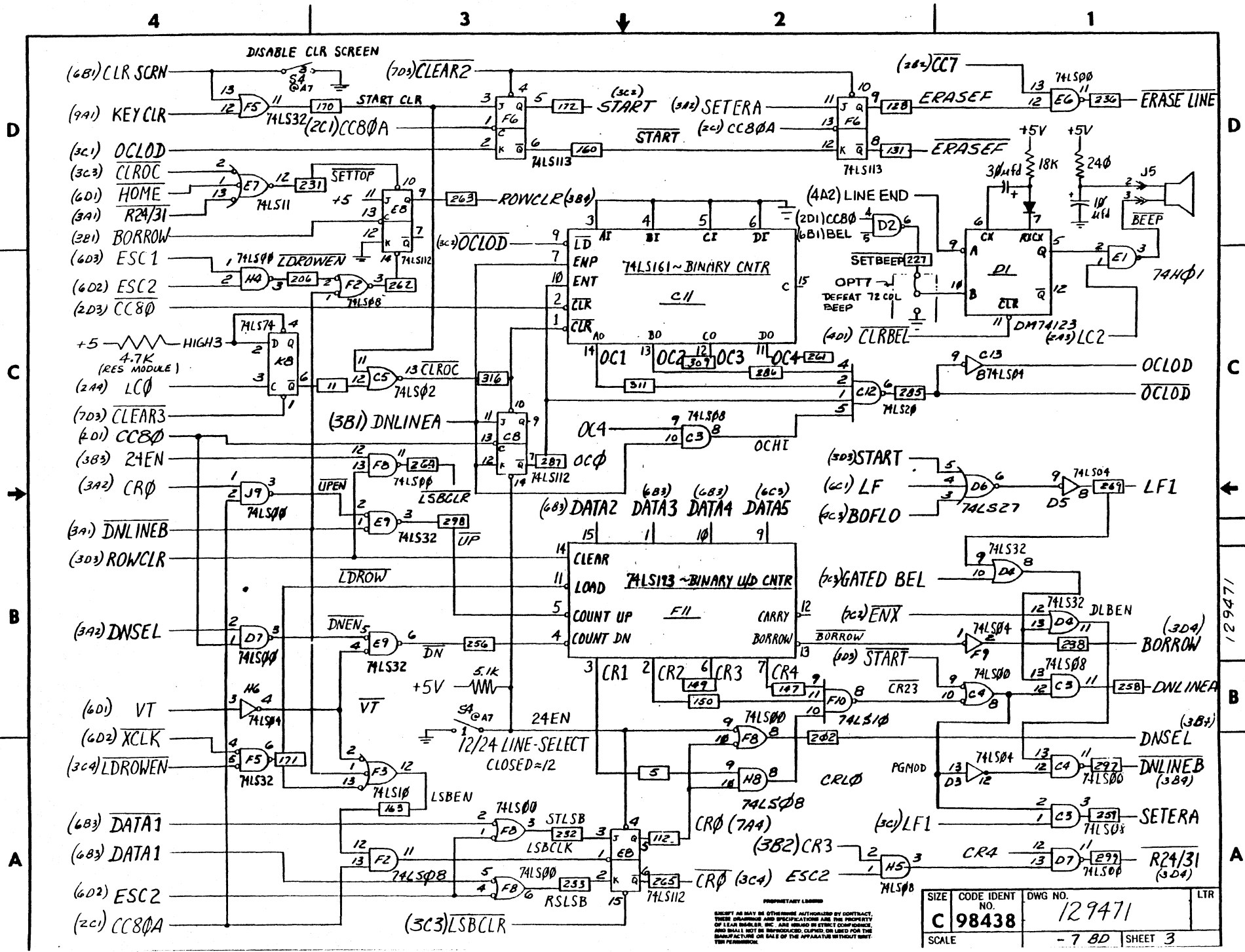
UNLESS OTHERWISE SPECIFIED DIM. IN INCHES TOLERANCES X ± .1 XX ± .03 XXX ± .010 ANGLES ± 0.5° MACH. FIN.			CONTR. NO. DR <i>W. Kelly 2-20-78</i>		 LEAR SIEGLER, INC. ELECTRONIC INSTRUMENTATION DIVISION ANAHEIM, CALIFORNIA 92803
DASH NO.			CHK DSGM ENGR PROJ <i>W. Johnson 2/20/78</i> REL <i>H. Turner 2/20/78</i>		
NEXT ASSY			APPD		SIZE C 98438
USED ON			APPD		CODE IDENT NO. 129471
APPLICATION			SCALE		DWG NO. 129471
					LTR 1 OF 14

129471
B
A



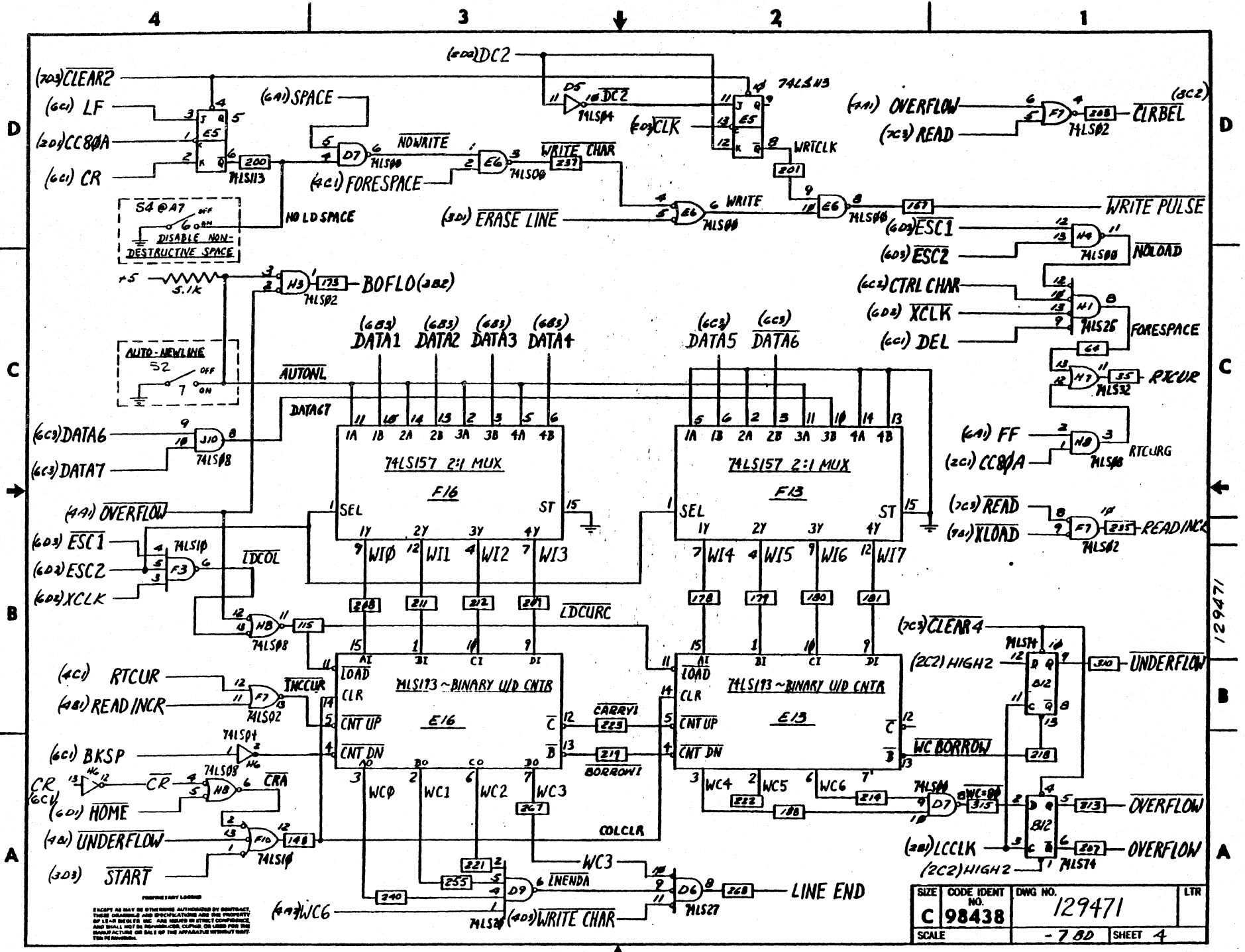
REGISTRATION LABEL
 THESE ARE NOT TO BE REPRODUCED BY CONTRACT
 WITHOUT THE WRITTEN APPROVAL OF THE AUTHORITY
 OF THE GOVERNMENT. THE GOVERNMENT IS NOT
 RESPONSIBLE FOR ANY LOSS OR DAMAGE TO THE
 ORIGINAL OR TO THE REPRODUCTION THEREOF.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE	- 7 80	SHEET 2	



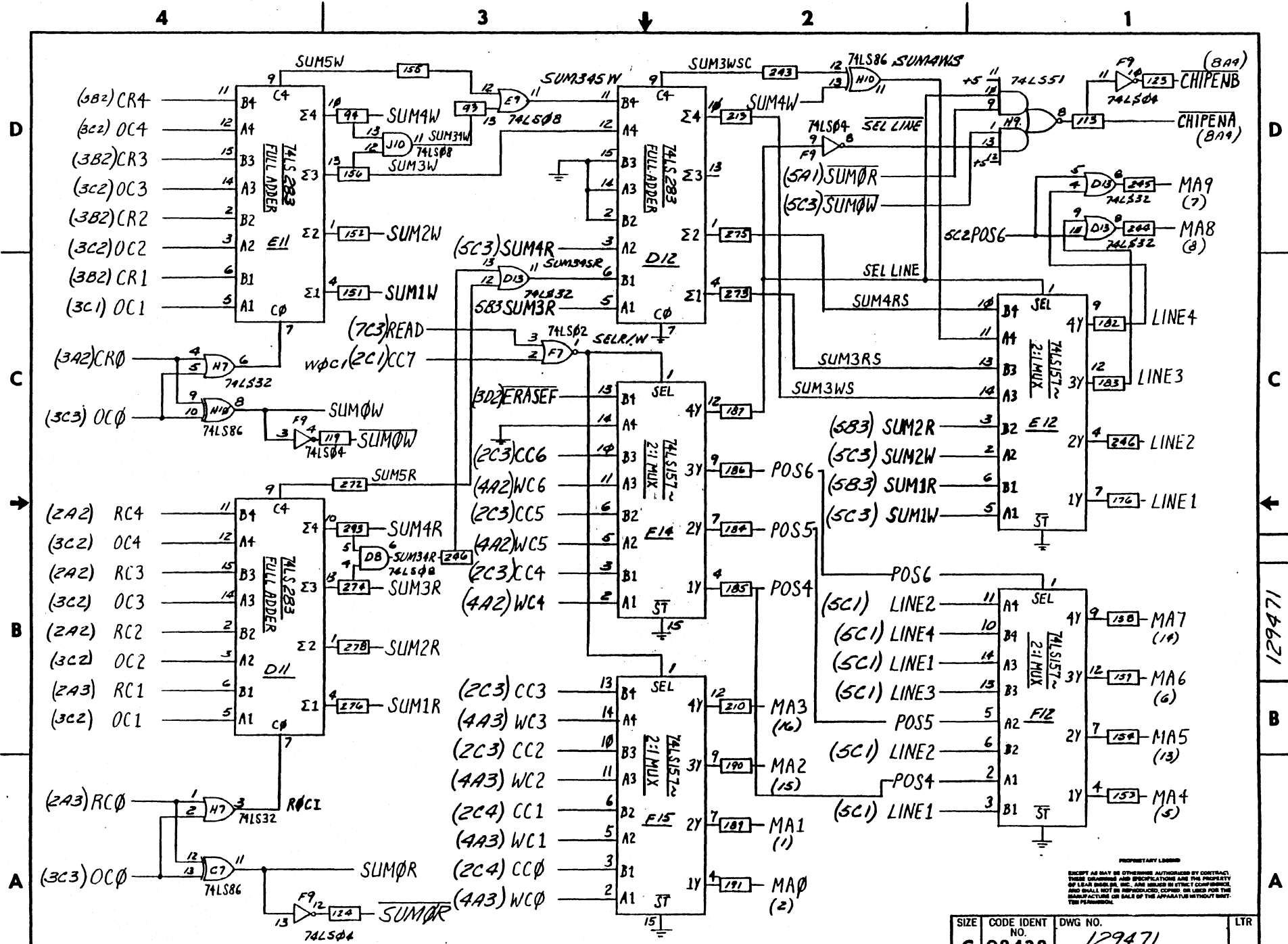
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DIMENSIONS AND SPECIFICATIONS ARE THE PROPERTY OF LEAN ENGINEER, INC. AND SHALL BE KEPT CONFIDENTIAL AND SHALL NOT BE REPRODUCED, COPIED OR USED FOR THE MANUFACTURE OR SALE OF THE APPLICABLE WITHOUT WRITTEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE	- 7 8D	SHEET 3	

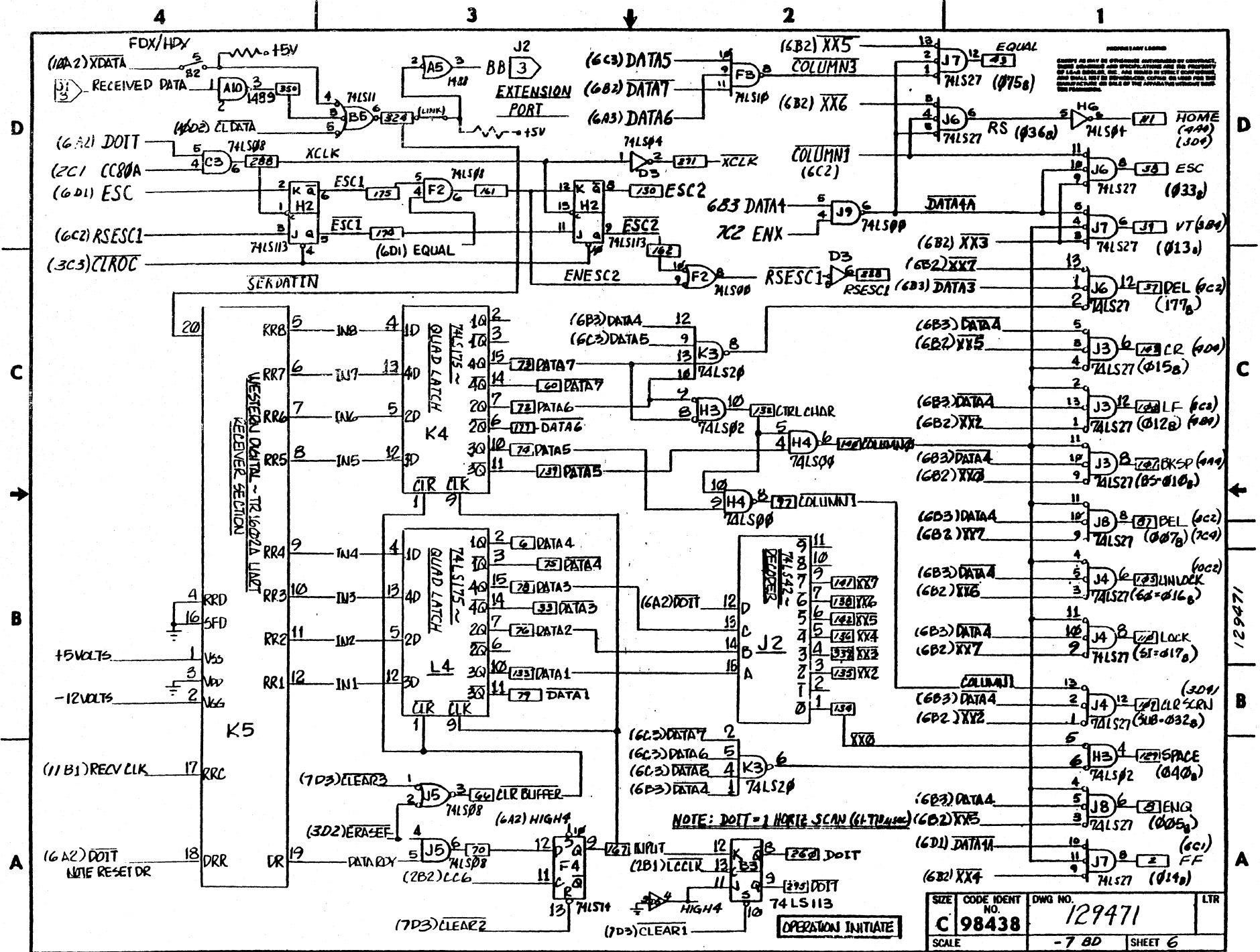


EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT,
 THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY
 OF LAR ELECTRONICS, INC. AND SHALL BE KEPT IN STRICT CONFIDENCE.
 AND SHALL NOT BE REPRODUCED, COPIED, OR LOANED FOR THE
 MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITING
 FROM THIS FIRM.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE	- 7 8 D	SHEET 4	



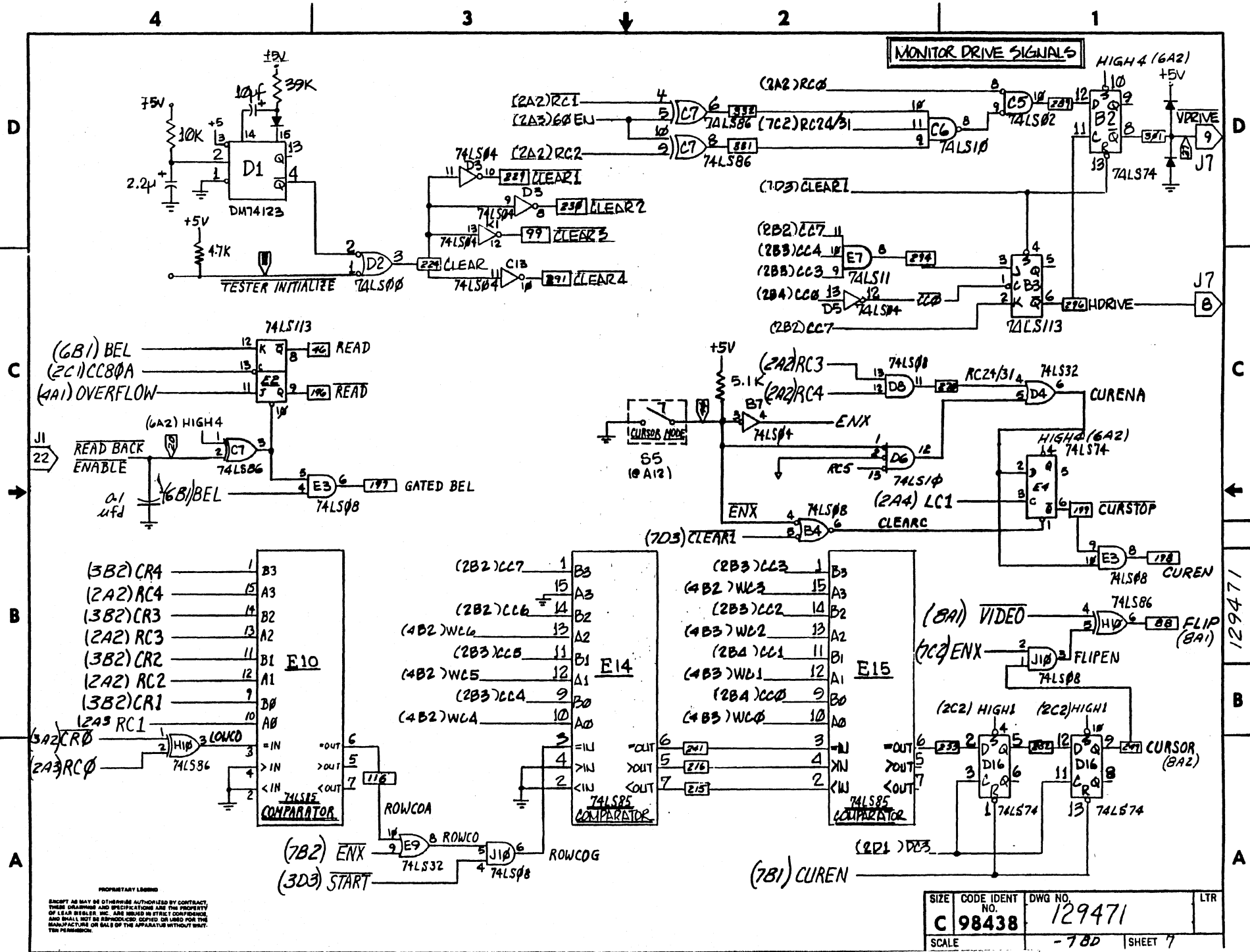
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	



PROPERTY OF WESTERN DIGITAL
 THIS DOCUMENT AND THE INFORMATION CONTAINED HEREIN ARE UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE. IT IS THE PROPERTY OF WESTERN DIGITAL AND IS LOANED TO YOU FOR THE PERFORMANCE OF YOUR DUTY. IT IS TO BE RETURNED TO WESTERN DIGITAL UPON THE COMPLETION OF YOUR ASSIGNMENT.

NOTE: DOIT = 1 HORIZ. SCAN (6170440)

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE	-7 BD	SHEET 6	

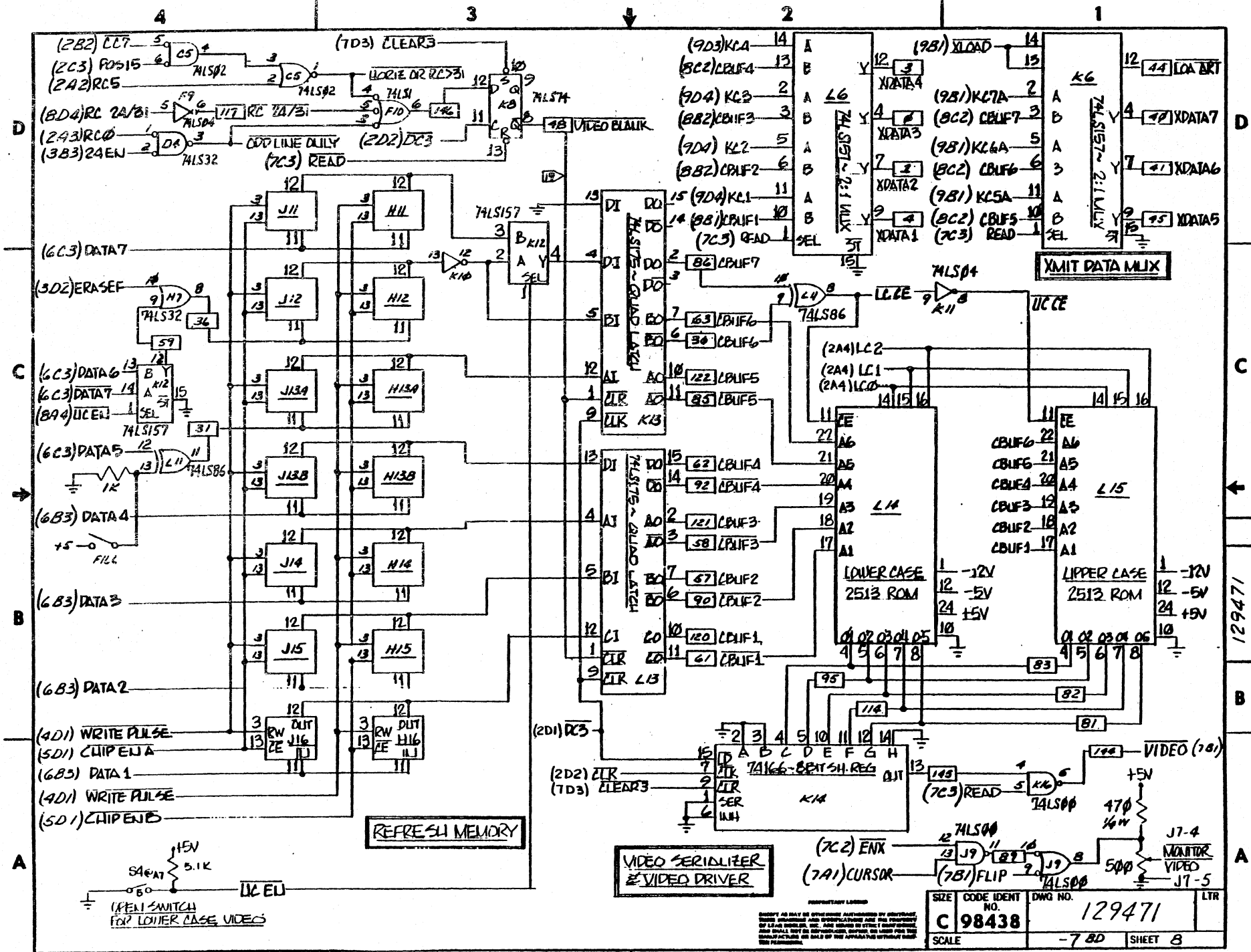


SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE	-7BD		SHEET 7

PROPRIETARY LEGEND
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SEATBELT, INC. AND SHALL BE KEPT IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.

129471

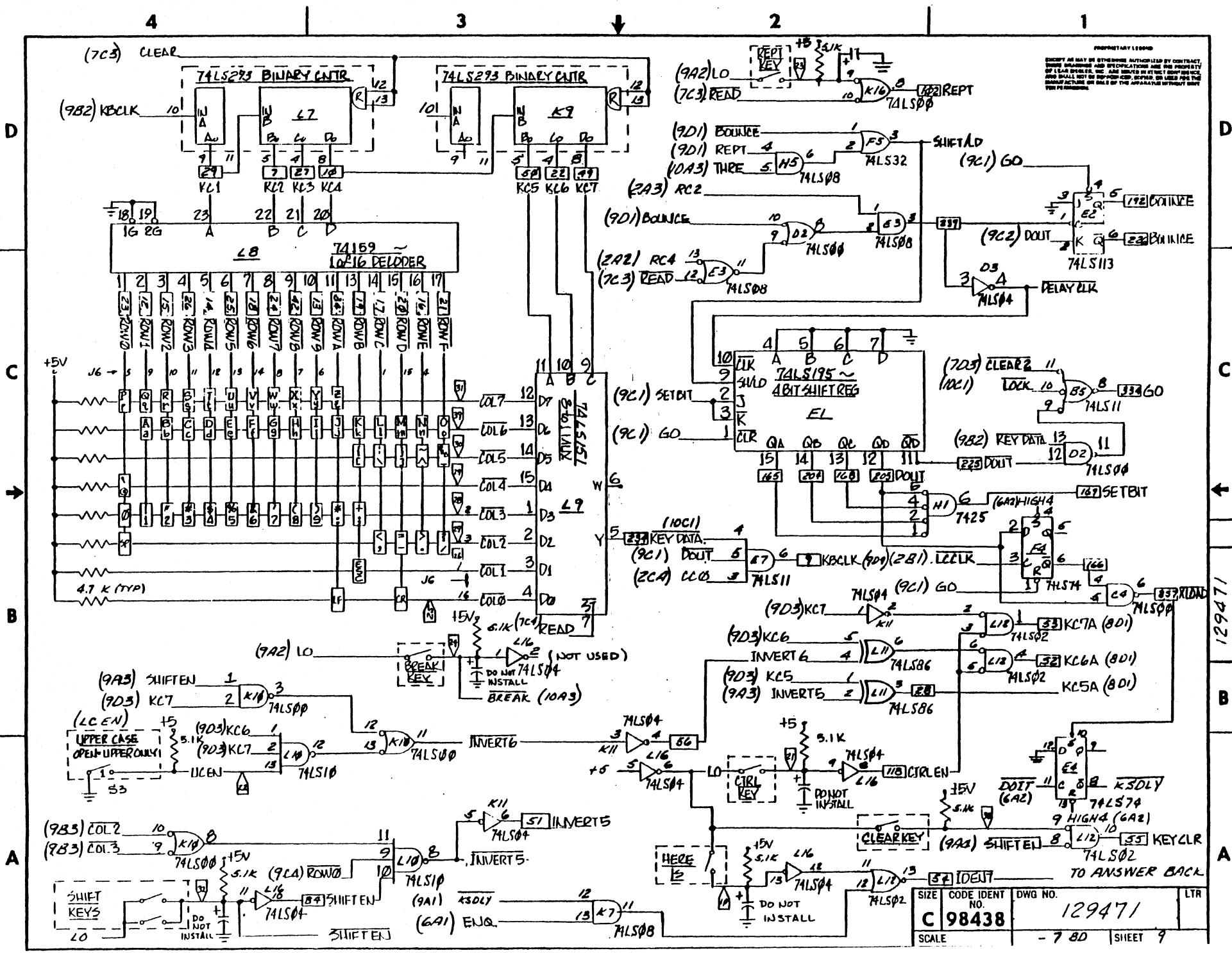
A



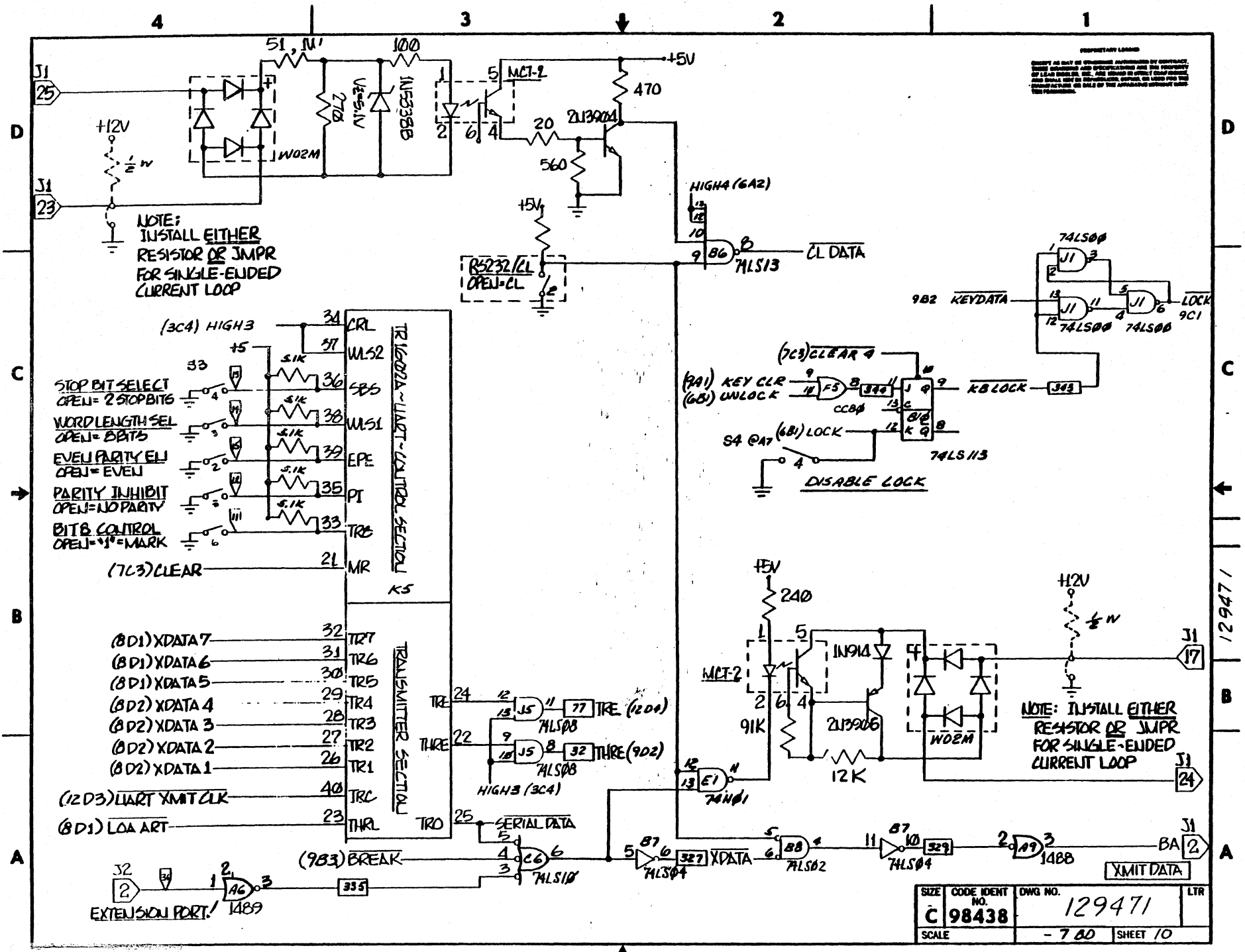
REPRODUCED FROM THE ORIGINAL DRAWING BY THE AUTOMATIC REPRODUCTION SYSTEM OF THE ARMY ELECTRONIC CENTER, FORT MONMOUTH, NEW JERSEY. THIS REPRODUCTION IS UNCLASSIFIED AND IS IN THE PUBLIC DOMAIN. IT IS THE PROPERTY OF THE ARMY ELECTRONIC CENTER AND IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE		-7 80	SHEET 8

PROPERTY 129471
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT
 STATE SPECIFICATIONS AND SPECIFICATIONS ARE THE PROPERTY
 OF LEAD DIVISION, INC. AND SHALL BE RETURNED TO THE
 OFFICE OF ORIGIN UPON REQUEST. REPRODUCTION OF THIS
 DRAWING OR ANY PART THEREOF IS PROHIBITED WITHOUT
 THE WRITTEN PERMISSION OF THE APPROVED AUTHORITY.



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE	- 7 80		SHEET 9

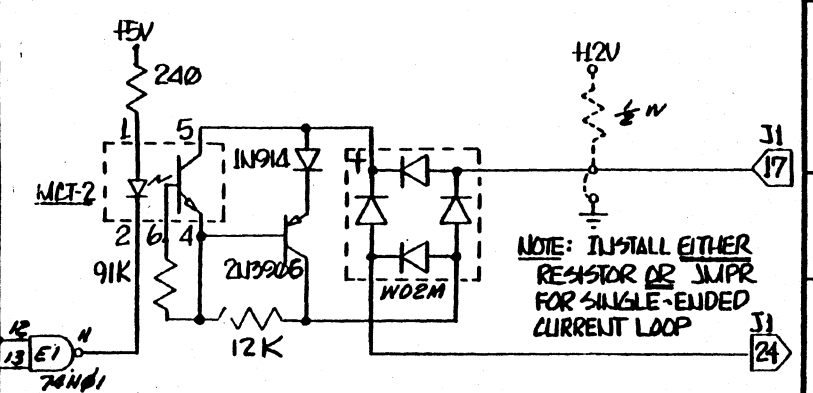
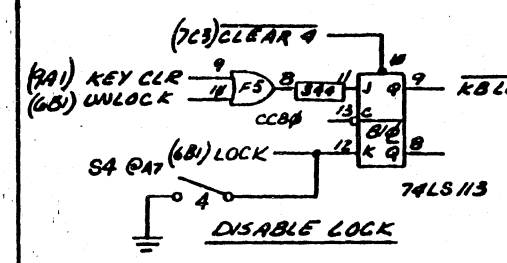
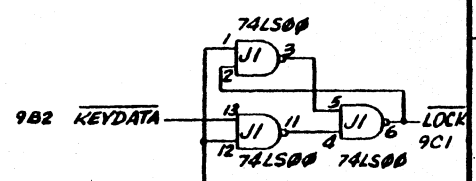
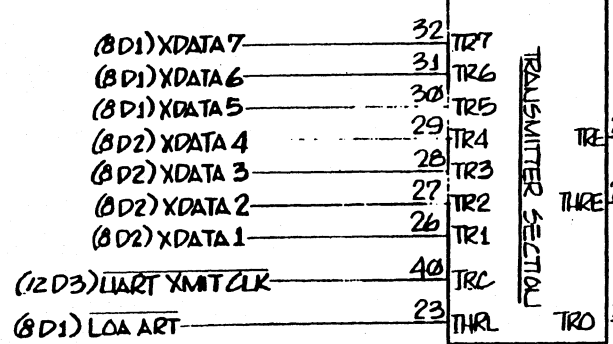
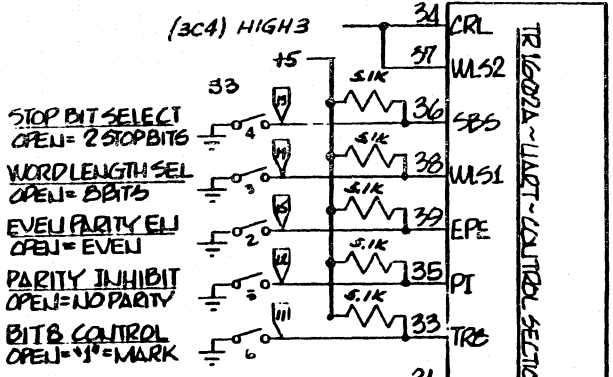


PROPERTY RIGHTS

NOTICE: THIS DOCUMENT IS UNCLASSIFIED BY CONTRACT DATE 08/20/2013. IT IS THE PROPERTY OF LEASER SYSTEMS, INC. AND SHOULD BE RETURNED TO THE CONTRACTOR OR DESTROYED BY THE USER. NO PART OF THIS DOCUMENT IS TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM.

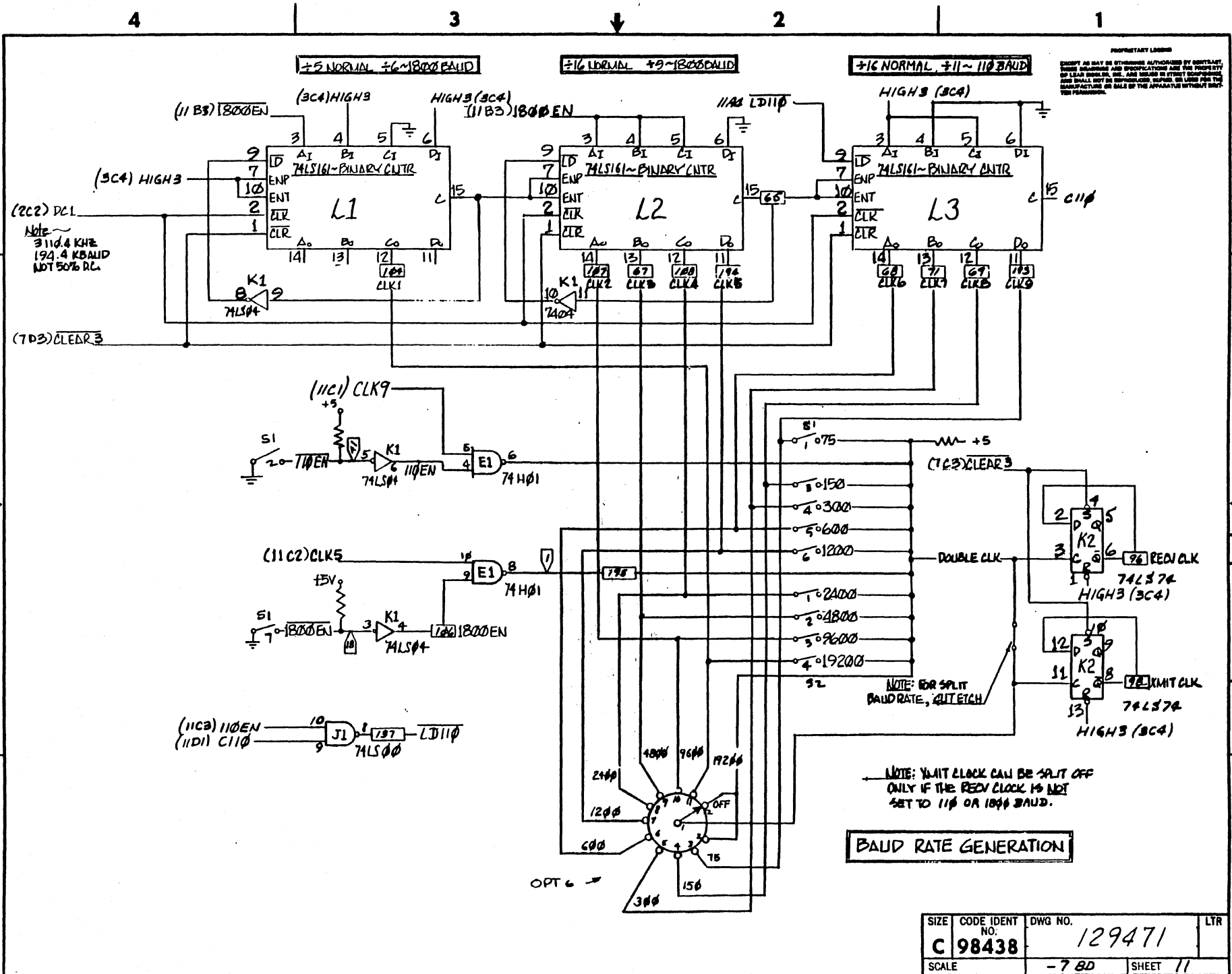
NOTE: INSTALL EITHER RESISTOR OR JMPR FOR SINGLE-ENDED CURRENT LOOP

NOTE: INSTALL EITHER RESISTOR OR JMPR FOR SINGLE-ENDED CURRENT LOOP

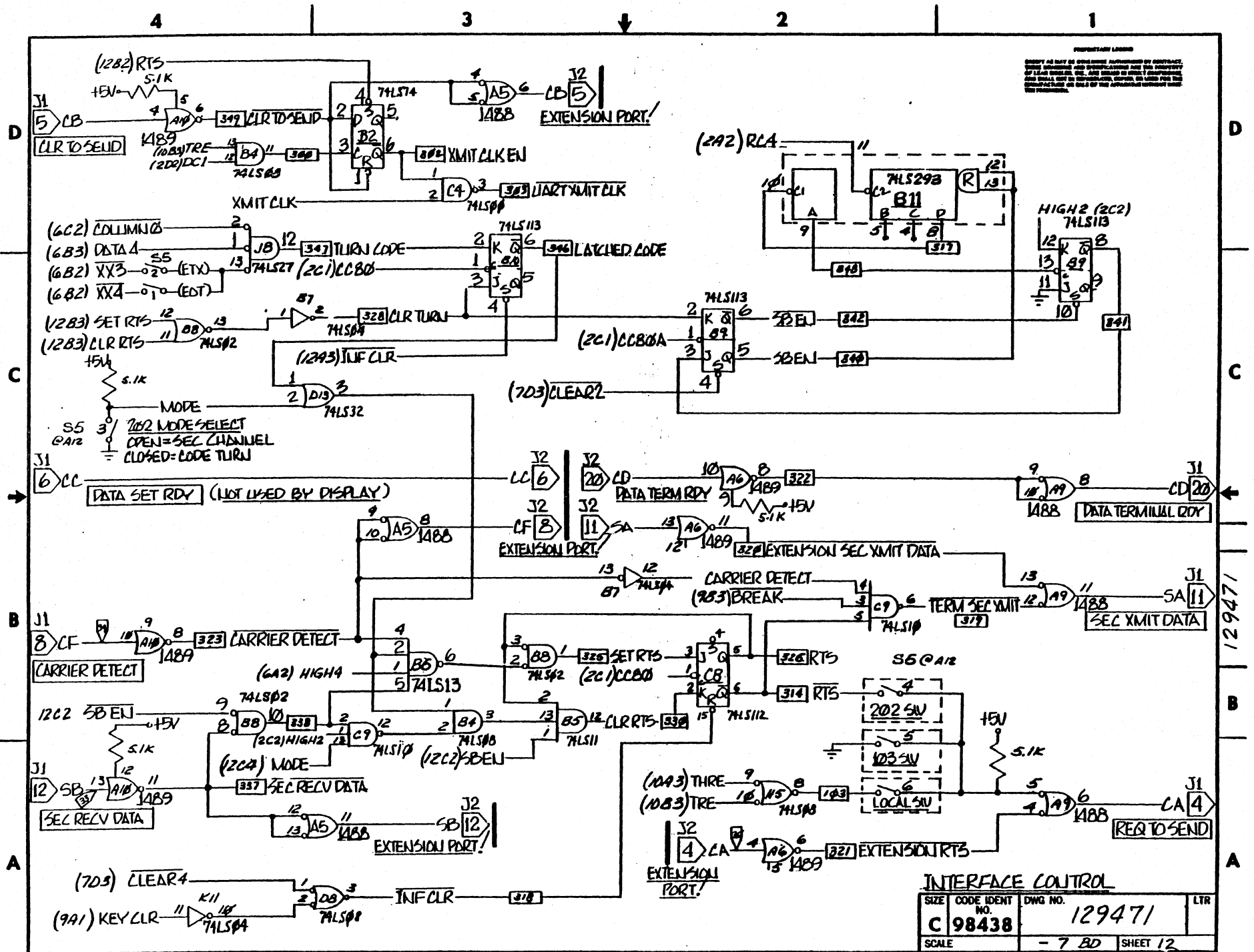


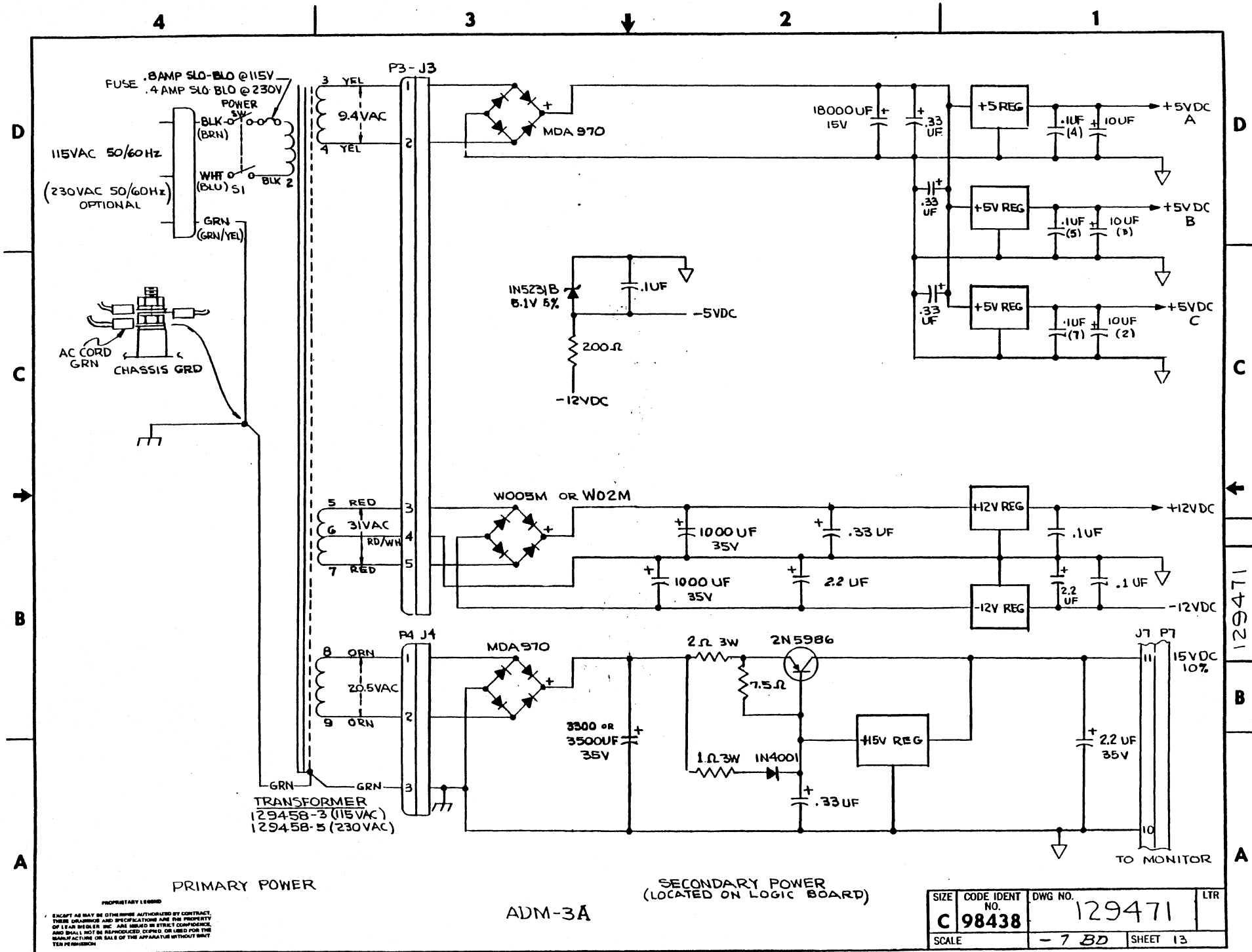
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE	- 7 00	SHEET 10	

PROPRIETARY LOGIC
 REPEAT AS MAY BE OTHERWISE AUTHORIZED BY INSTANTLY
 THESE INVENTIONS AND SPECIFICATIONS ARE THE PROPERTY
 OF LEAS ELECTRONIC, INC. AND SHALL BE KEPT CONFIDENTIAL
 AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE
 MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN
 PERMISSION.



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE		-7 80	SHEET 11





PROPRIETARY LEGEND
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT,
 THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF
 LEAR BENDER INC. AND SHALL BE KEPT IN STRICT CONFIDENCE,
 AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE
 MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN
 PERMISSION

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129471	
SCALE	- 7 BD		SHEET 13

4

3

2

1

CONN PIN ASSIGNMENTS

SWITCH ASSIGNMENTS

REVISIONS

SHT	ZONE	LTR	DESCRIPTION	DATE	APPROVED
		A	RELEASE PER DCN 1511 RES. 10-2A-80	10/24/80 10/30/80	J. Sieglar B. Hyden

CONN PIN	FUNCTION	SHT	CONN PIN	FUNCTION	SHT
J1 1	FRAME GND		J3 1	9.4 VAC	13D3
MODEM 2	BA	10A1	PWR 2	9.4 VAC	13D3
RS232 3	RCVD DATA	6DA	INPUT 3	31 VAC	13B3
4	CA	12A1	4	GND	13B3
5	CB	12D4	5	31 VAC	13B3
CURRENT LOOP 6	CC	12CA			
7	GND		J4 1	20.5 VAC	13B3
8	CF	12B4	2	20.5 VAC	13A3
9	**		PWR 3	FRAME GND	13A3
10			INPUT 4		
11	SA	12B1	5		
12	SB	12A4			
13	**		J5 1		
14	**		2	SPKR	3D1
15	**		3	SPKR	3D1
16	**				
17	CL OUT	10B1	J6 1	ROW C	9C3
18	**		2	COL 3	9B3
19	**		NUMERIC 3	COL 2	9B3
20	CD	12C1	KEYPAD 4	ROW E	9C3
21	**		OUTPUT 5	ROW D	9C4
22	READ BACK EN	7CA	OPTION 6	ROW 9	9C4
23	CL INPUT	10DA	7	ROW 8	9C4
24	CL OUT	10A1	8	ROW 7	9C4
25	CL INPUT	10DA	9	ROW 1	9C4
			10	ROW 2	9C4
J2 1	FRAME GND		11	ROW 3	9C4
EXTEN. 2	BA	10AA	12	ROW 4	9C4
RS232 3	BB	6DB	13	ROW 5	9C4
4	CA	12A2	14	ROW 6	9C4
5	CB	12D3	15	ROW D	9C3
6	CC	12C3	16	COL D	9B3
7	GND				
8	CF	12B3	J7 1	(KEY PAD)	
9	**		2		
10	-12V *		3		
11	SA	12B3	4	VIDEO	8A1
12	SB	12A3	5	VIDEO RET	8A1
13	**		6		
14	**		7		
15	**		8	HDRIVE	7C1
16	**		9	VDRIVE	7D1
17	+12V *		10	GND	13A1
18	**		11	+15V	13B1
19	**		12		
20	CD	12C3			
21	**				
22					
23					
24	EXT CL IN *				
25	EXT CL OUT *				

SWITCH	SECTION	FUNCTION	SHT
S1 7	1800	11B4	
6	1200	11B2	
5	600	11B2	
4	300	11B2	
3	150	11C2	
2	110	11C4	
1	75	11C2	
S2 7	AUTO NEWLINE	4C4	
6	CL	10C3	
5	FDX/HDX	6DA	
4	19200	11B2	
3	9600	11B2	
2	4800	11B2	
1	2400	11B2	
S3 6	BIT B	10B3	
5	PAR INH	10B3	
4	STOP BIT	10B3	
3	WORD LG	10B3	
2	EVEN PAR	10B3	
1	UPPER CASE	9A4	
S4 6	SPACE	4D4	
5	UP CASE DISP	8A4	
4	DIS LOCK	10C2	
3	DIS CLR SCRN	3DA	
2	50/60 HZ	2A4	
1	12/24 LINE	3B3	
S5 7	CUR MODE	7C2	
6	LOCAL	12A2	
5	103	12A1	
4	202	12B2	
3	MODE	12C4	
2	ETX	12C4	
1	EOT	12C4	
S6	FILL "φ"	8C4	
S7	DIS. 72 ND BEEP	3C2	
S8	LOCK/GATE	10C1	

SYMBOLS: [XXX] & [X] ARE TEST POINTS SHOWN FOR REF ONLY.

NOTE: 1. U3 & U6 NOT USED. LAST USED REF. DESIGNATIONS U148, R39, C44, CR13, S9, J9. 2. REF PRINTED WIRING BOARD 13154B

* WHEN OPTIONAL EXTENSION PORT CURRENT LOOP INSTALLED ** NO SOCKET INSTALLED CONNECTOR

NO.	131547	2129450
DASH	NEXT ASSY	USED ON
NO.	APPLICATION	

UNLESS OTHERWISE SPECIFIED DIM. IN INCHES TOLERANCES X ± .1 .XX ± .03 .XXX ± .010 ANGLES ± 0.5° MACH. FIN.
CONTR. NO. DR RES. 10-2A-80
CHK 4/2/80
DSGN 12/80
ENGR 12/80
PROJ. 12/80
REL. 12/80
APPD
APPD

LEAR SIEGLER, INC. ELECTRONIC INSTRUMENTATION DIVISION ANAHEIM, CALIFORNIA 92803			
SCHEMATIC - ADM-3A			
SIZE	CODE IDENT NO.	DWG. NO.	LTR
C	98438	131549	A
SCALE			SHEET 1 OF 14

PROPRIETARY LEGEND EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DIMENSIONS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC. AND SHALL BE KEPT IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITING THE PERMISSION.

D

C

B

A

D

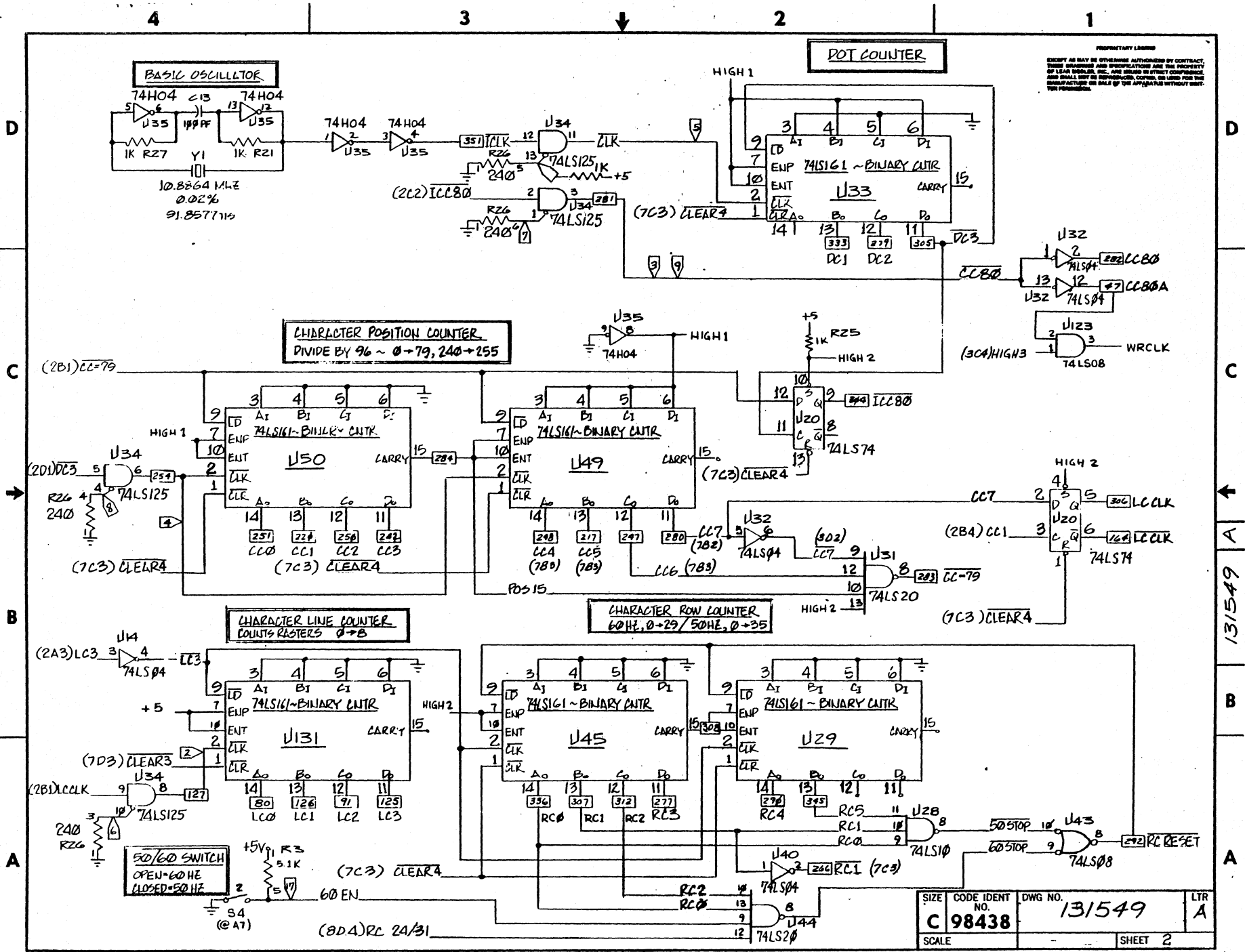
C

A

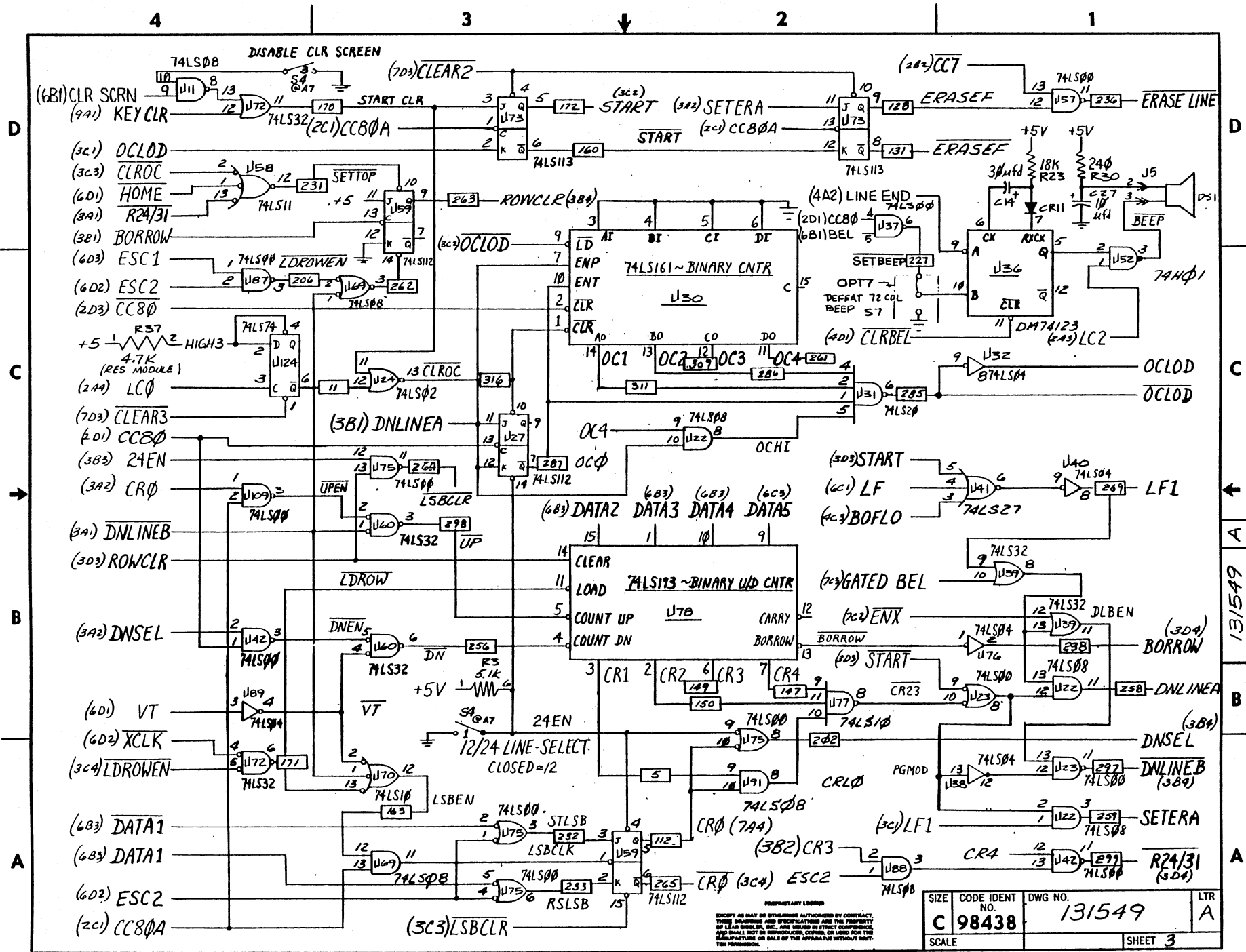
B

A

131549

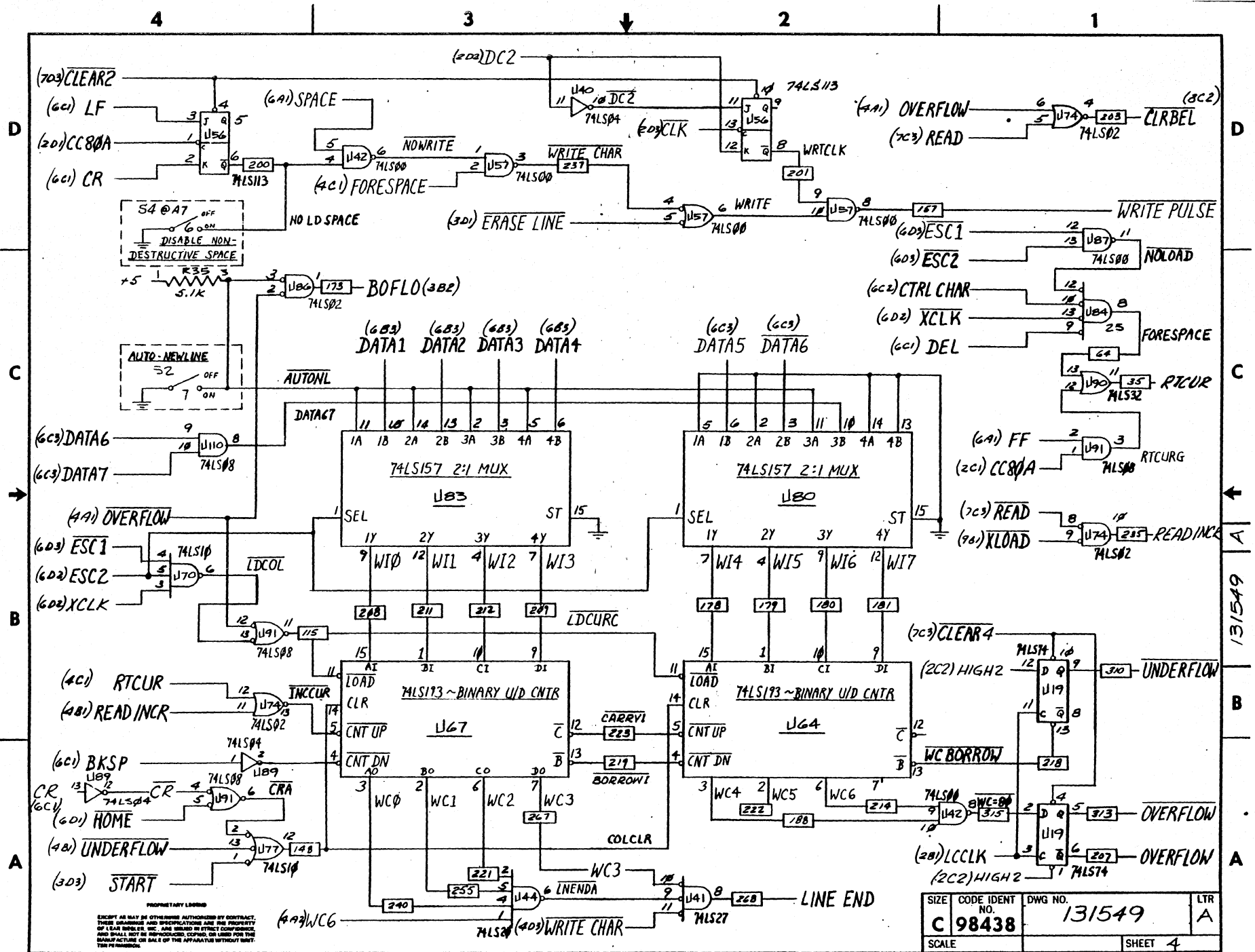


SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	131549	A
SCALE		SHEET 2	



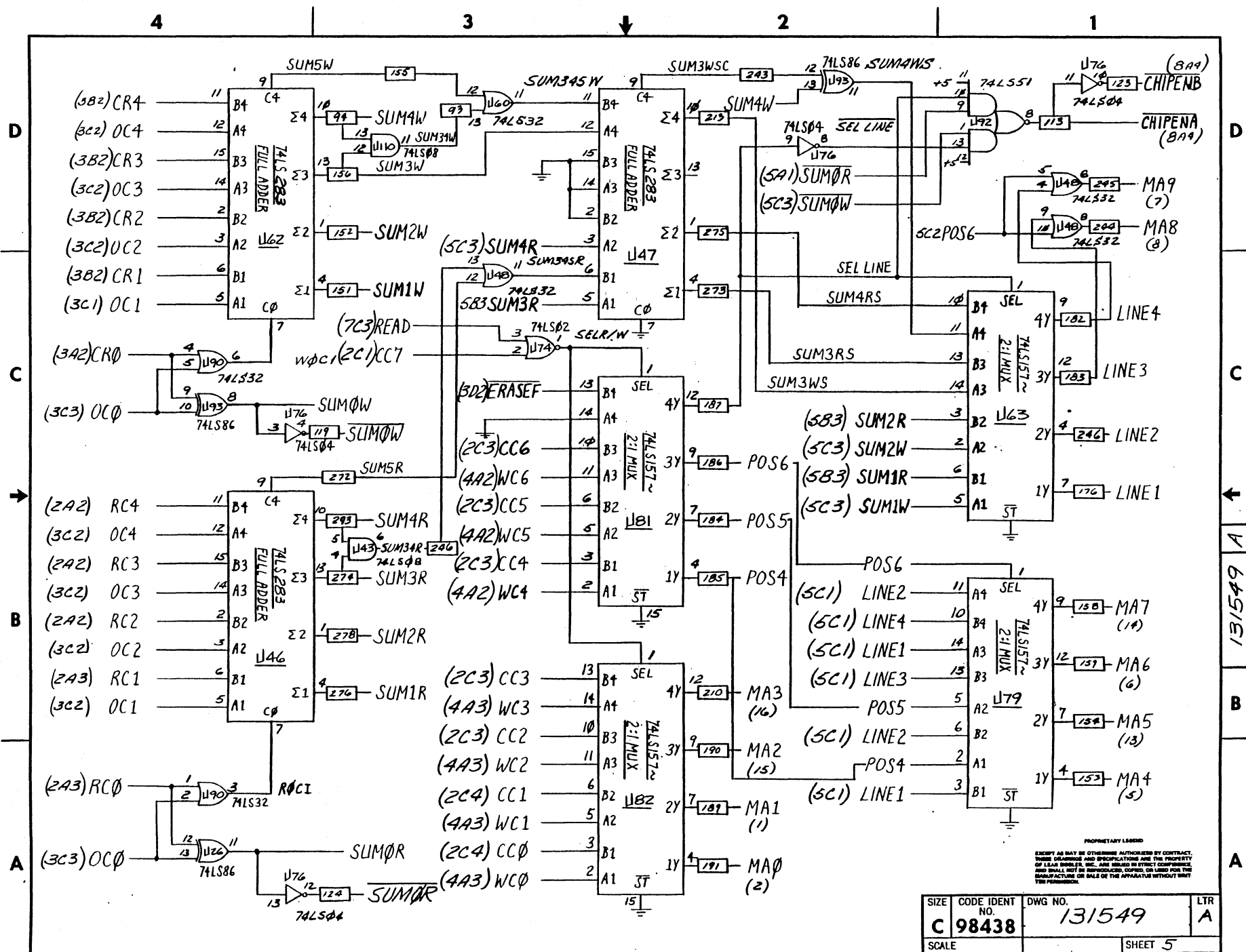
PROPRIETARY LOGIC
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT,
 THIS DRAWING AND SPECIFICATIONS ARE THE PROPERTY
 OF TEXAS INSTRUMENTS, INC. AND SHALL BE RETURNED TO
 THE MANUFACTURER OF THE APPLICABLE LOGIC DEVICE
 UPON REQUEST. THIS DRAWING IS NOT TO BE REPRODUCED,
 COPIED, OR LOANED FOR THE MANUFACTURE OR SALE OF
 THE APPLICABLE LOGIC DEVICE WITHOUT WRITTEN
 PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	131549	A
SCALE	SHEET 3		



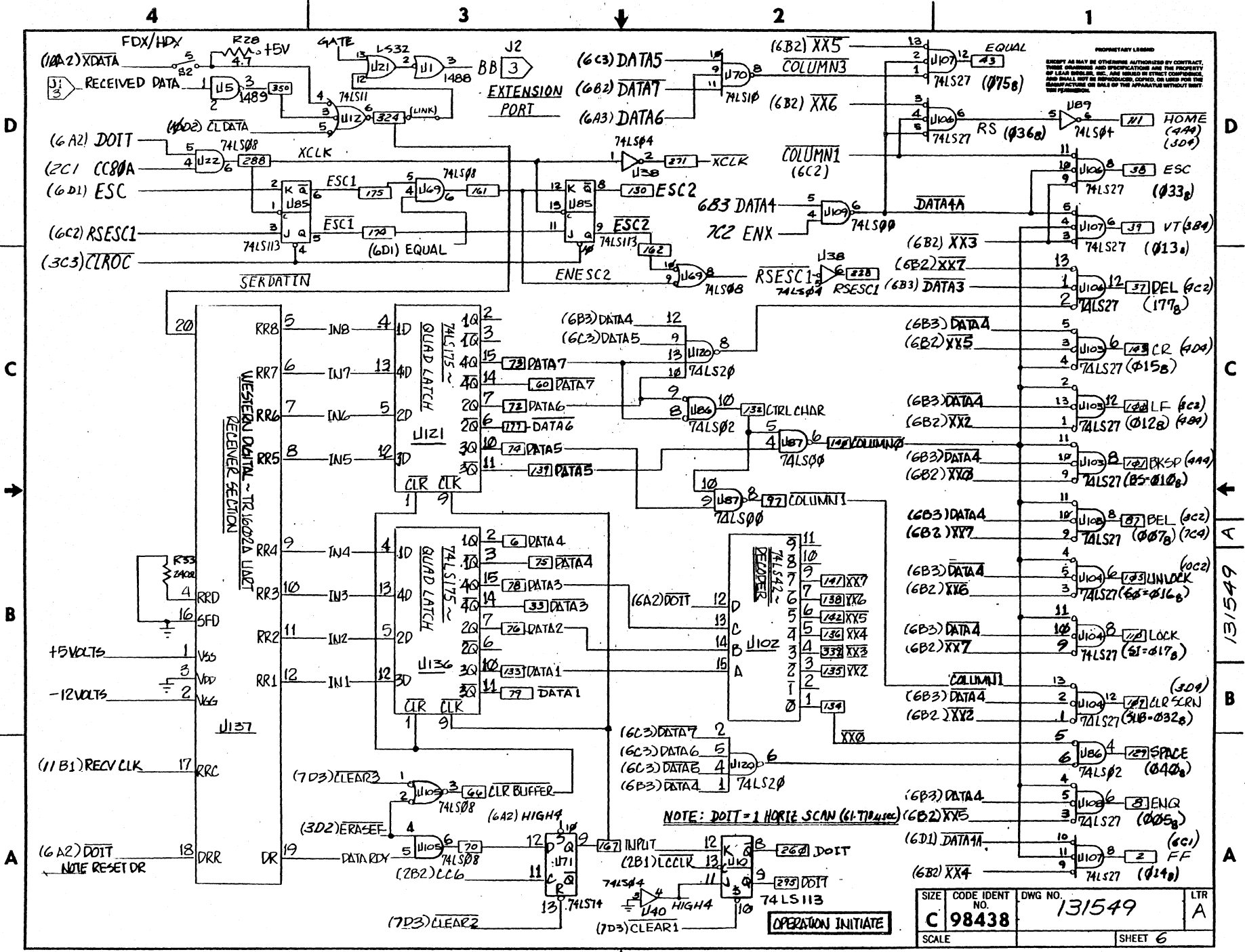
PROPRIETARY LEGEND
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT,
 THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY
 OF LEAR BODIES, INC. AND SHALL BE KEPT IN STRICT CONFIDENCE,
 AND SHALL NOT BE REPRODUCED, COPIED, OR LENT FOR THE
 MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRIT-
 TEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	131549	A
SCALE	SHEET 4		



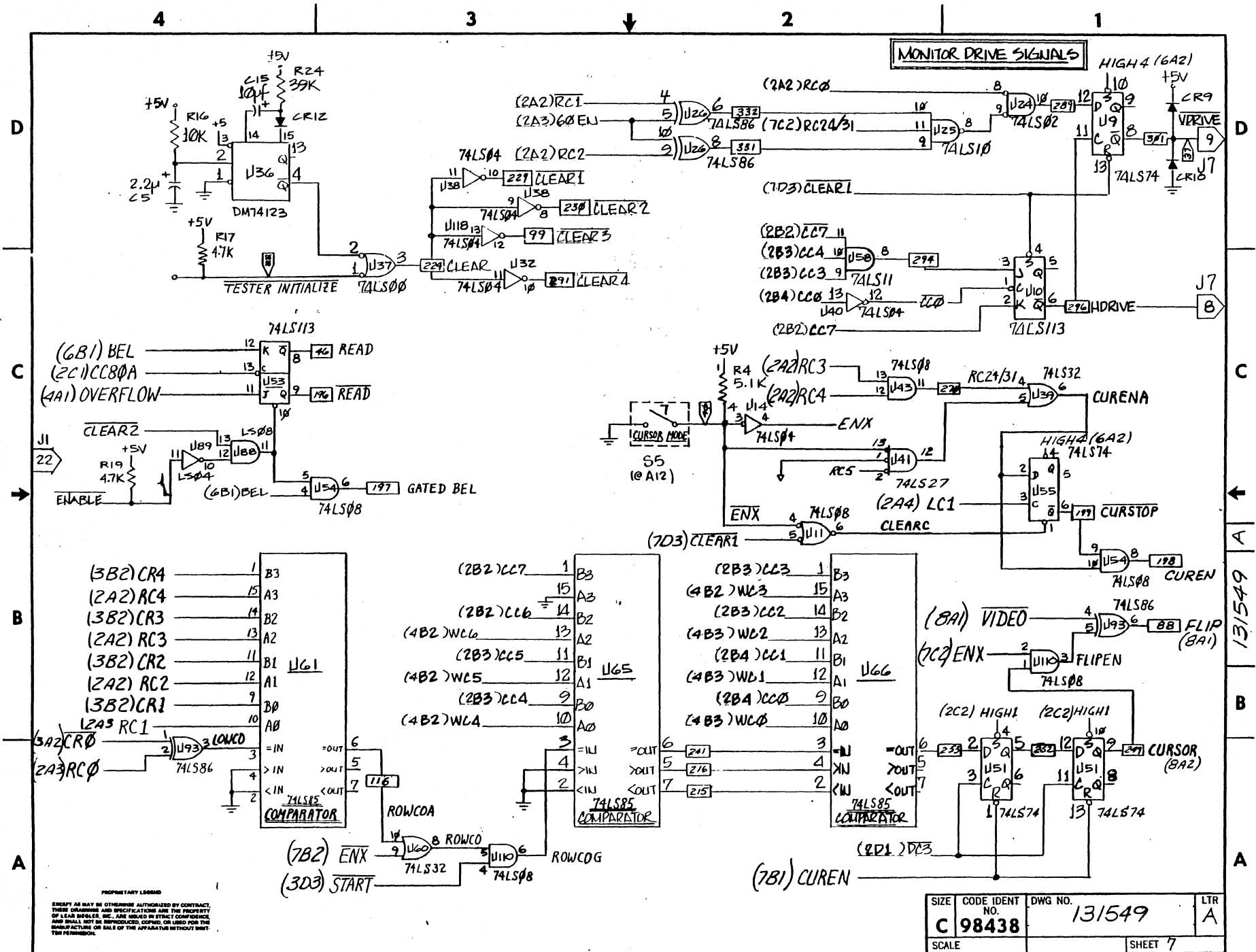
PROPRIETARY LEGEND
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT,
 THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY
 OF LAMAR BROS. INC. AND SHALL BE STRICTLY CONFIDENTIAL
 AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE
 MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN
 PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	131549	A
SCALE	SHEET 5		



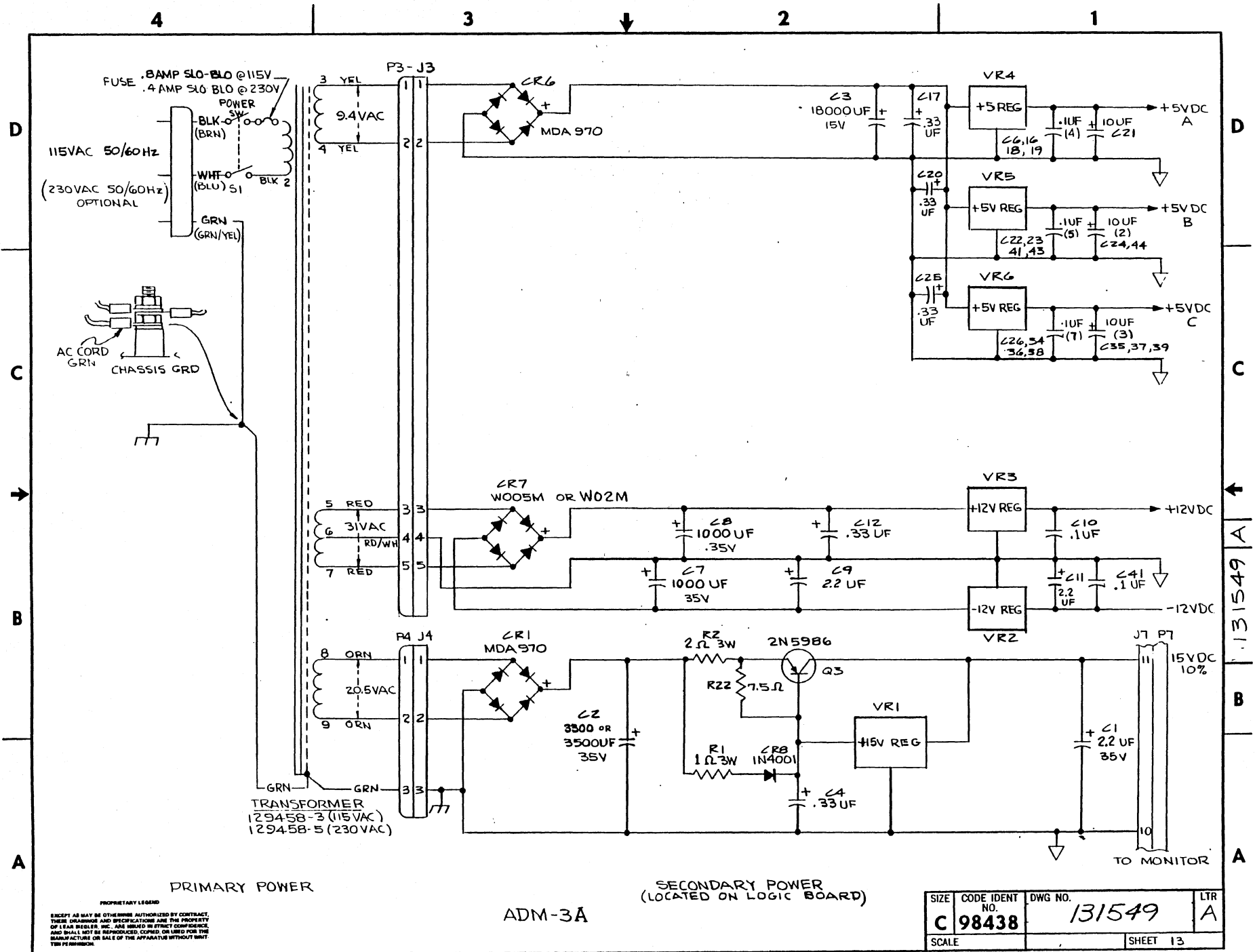
PROPERTY LEGEND
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT,
 THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY
 OF LEAR CORPORATION, INC. AND SHALL BE KEPT IN STRICT CONFIDENCE.
 ANY REPRODUCTION, COPIES, OR USE FOR THE
 MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITING
 THE PROPERTY OF LEAR CORPORATION, INC.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	131549	A
SCALE	SHEET 6		



PROPRIETARY LEGEND
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT,
 THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY
 OF LEAR DELTA, INC. AND SHALL BE KEPT IN STRICT CONFIDENCE
 AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE
 MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRIT-
 TEN PERMISSION.

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	131549	A
SCALE	SHEET 7		

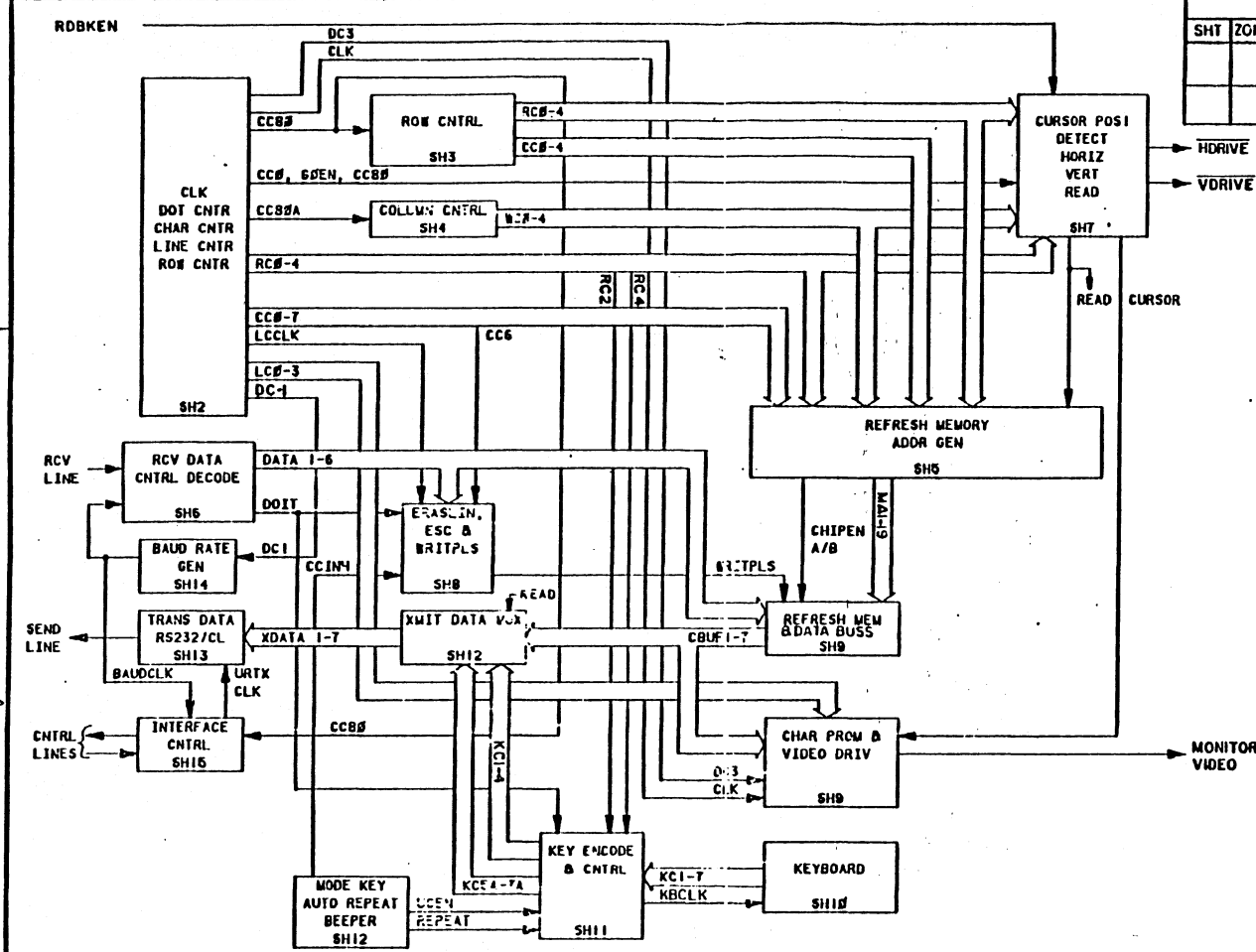


PROPRIETARY LEGEND
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT,
 THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY
 OF LEAR REGLES, INC. AND SHOULD BE KEPT CONFIDENTIAL.
 AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE
 MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN
 PERMISSION.

ADM-3A

SECONDARY POWER
 (LOCATED ON LOGIC BOARD)

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	131549	A
SCALE		SHEET 13	



REVISIONS					
SHT	ZONE	LTR	DESCRIPTION	DATE	APPROVED
		X	RELEASED PER DCN 570		
		A	PILOT RELEASE 755. 2-7-80	2/7/80	
		B	PROD. RELEASE PER DCN 789 AND INCORP OUTSTG DCNS 610 & 628	2/15/80	
		D	INCORP DCN 857	2-10-80	
		C	INCORP DCN #1020	2-17-80	

- NOTES (UNLESS OTHERWISE SPECIFIED):
- FOR PRINTED WIRING BOARD 131661-7, ASSY 131660.
 - [XXXX] DEFINES HEXDECIMAL ADDRESS.
 - CAPACITOR VALUES ARE IN MICROFARADS.
 - RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.
 - PREFIX DEVICE TYPE WITH 74.
EXAMPLE: 74LS161
 - DEVICE DESIGNATION INDICATES LOCATION.
EXAMPLE: 14C
 - DEVICE POWER PINS ARE:
FOR 14 PIN -7 (GND), 14 (+5V)
FOR 16 PIN -8 (GND), 16 (+5V)
FOR 18 PIN -9 (GND), 18 (+5V)
FOR 24 PIN -12 (GND), 24 (+5V)
FOR 1488 ONLY -7(GND), 11(-12), 14(+12).
 - LAST PREFERENCE DESIGNATION USED:
C-49 1CR-13 1J-8 1Q-41
R-45 1S-7 1VR-6 1Y-1.

UNLESS OTHERWISE SPECIFIED. DIM. IN INCHES TOLERANCES: X ± .1 XX ± .03 XXX ± .010 ANGLES ± 0.5°		CONTR NO DR 2/6/80	LEAR SIEGLER, INC. DATA PRODUCTS DIVISION ANAHEIM, CALIFORNIA 92803
DATE: 2/6/80 DRAWN BY: [signature] CHECKED BY: [signature] DESIGNED BY: [signature] ENGR: [signature] PROJ: [signature] REL: [signature]		CHK DSGN ENGR PROJ REL	
PROPRIETARY LEGEND EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC. AND ISSUED IN STRICT CONFIDENCE. NO PART MAY BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.		APPD APPD	SCHEMATIC DIAGRAM ADM 3A + SIZE: FSCM NO 98438 DWS NO 131562 LTR C SCALE: NONE SHEET 1 OF 18

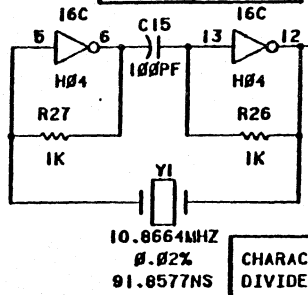
D

C

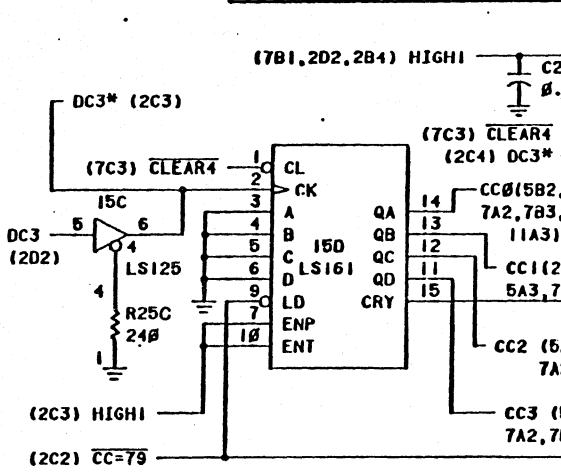
B

A

BASIC OSCILLATOR

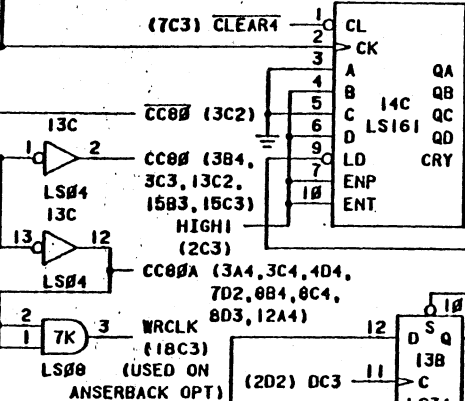


CHARACTER POSITION COUNTER
DIVIDE BY 96 = $\beta \rightarrow 79, 242 \rightarrow 255$



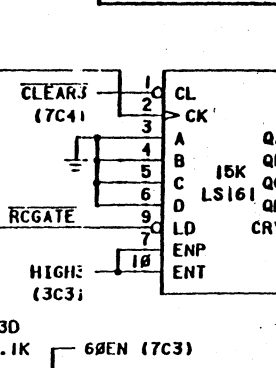
CLK (8C3, 9B1)

DOT COUNTER

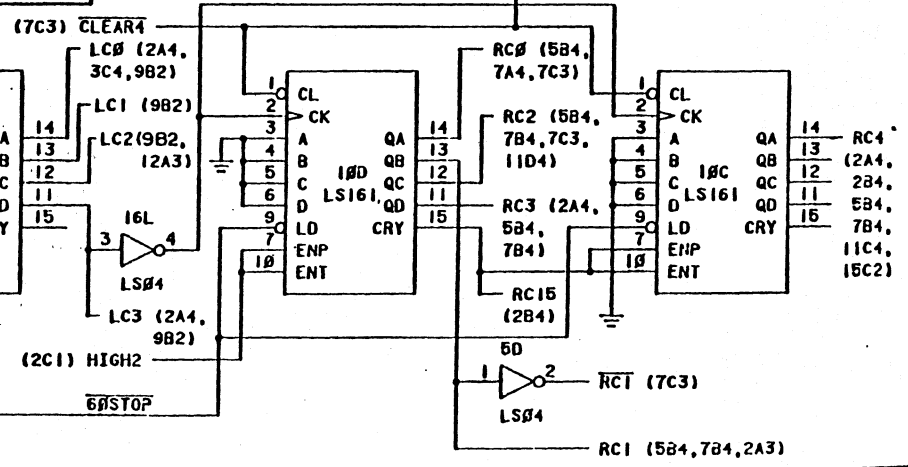


REVISIONS		DATE	APPROVED
SHT	ZCNE LTR		
DESCRIPTION			

CHARACTER LINE COUNTER
COUNTS RASTER $\beta = 9/13$



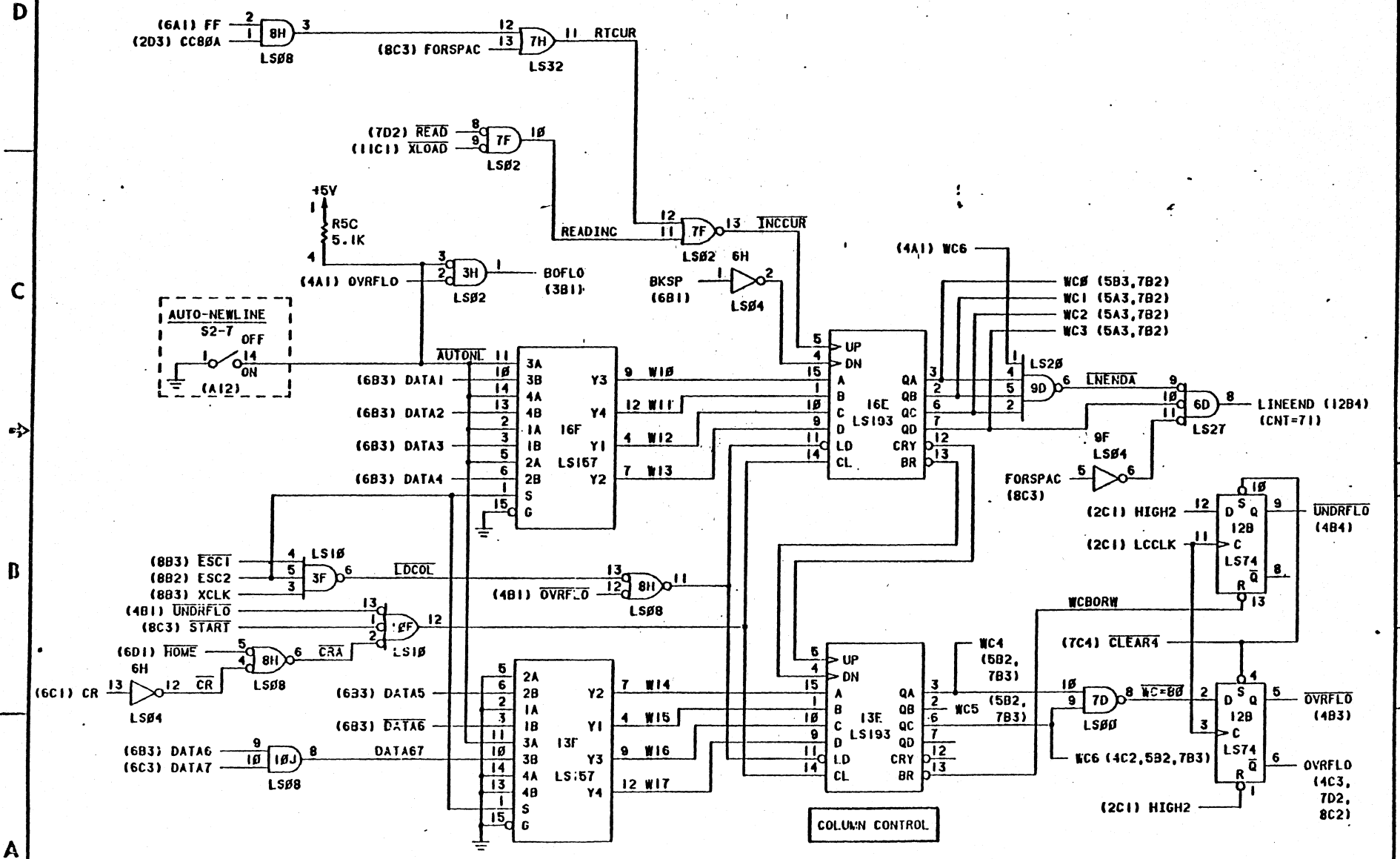
CHARACTER ROW COUNTER
 $60\text{HZ } \beta \rightarrow 26/50\text{HZ } \beta \rightarrow 31.4$



50/60 SWITCH
 OPEN = 60HZ = 1
 CLOSED = 50HZ = 0

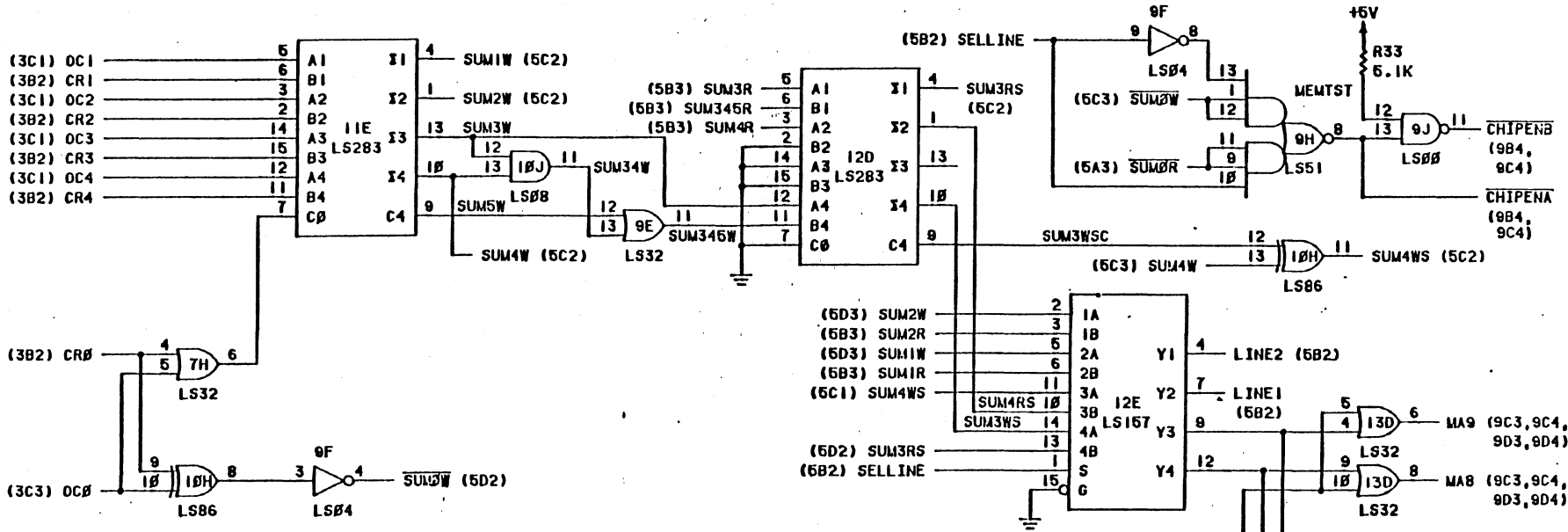
PROPRIETARY LEGEND				SIZE	FSCM NO.	DWG NO.	LTR
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER INC. AND ARE LOANED TO YOUR COMPANY FOR YOUR CONSIDERATION AND SHALL NOT BE REPRODUCED, EITHER WHOLLY OR IN PART, BY ANY MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.				C	99438	131562	C
				SCALE			SHEET 2 of 13

REVISIONS			
SHT	ZONE	LTR	DATE

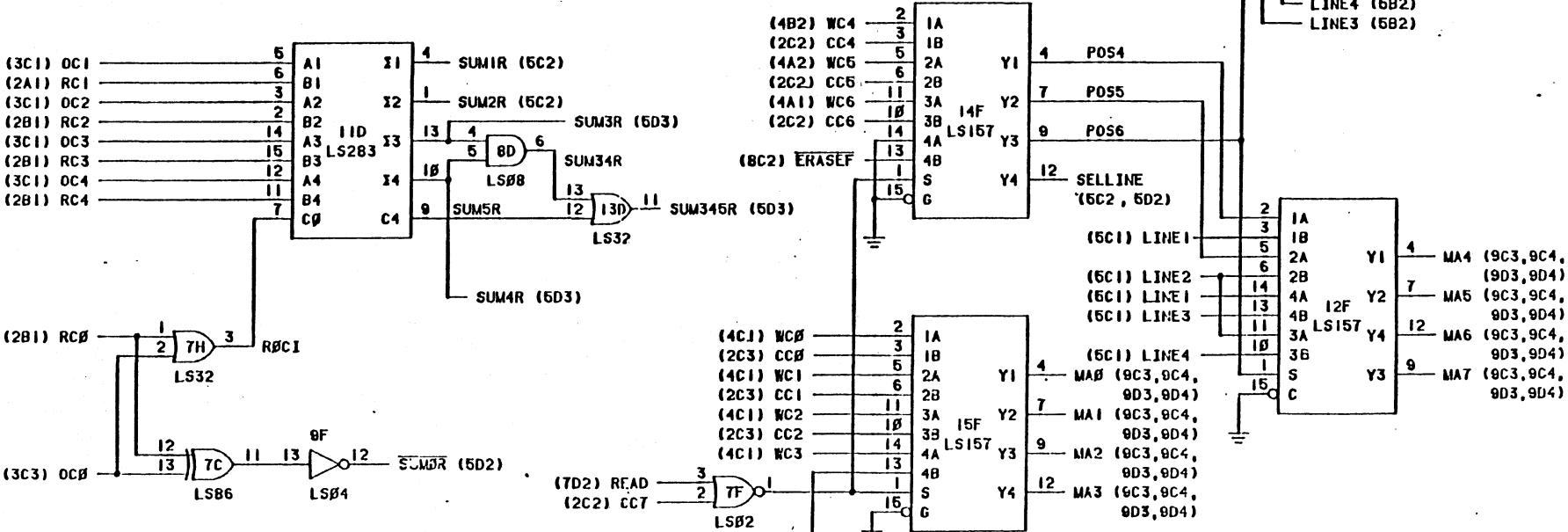


PROPRIETARY LEGEND		SIZE	FSCM NO	DWG NO.	LTR
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC. AND SHALL REMAIN THE PROPERTY OF LEAR SIEGLER, INC. AND SHALL NOT BE REPRODUCED OR USED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF LEAR SIEGLER, INC.		C	S9433	131562	C
SCALE: NONE				SHEET 4 OF 18	

D



C



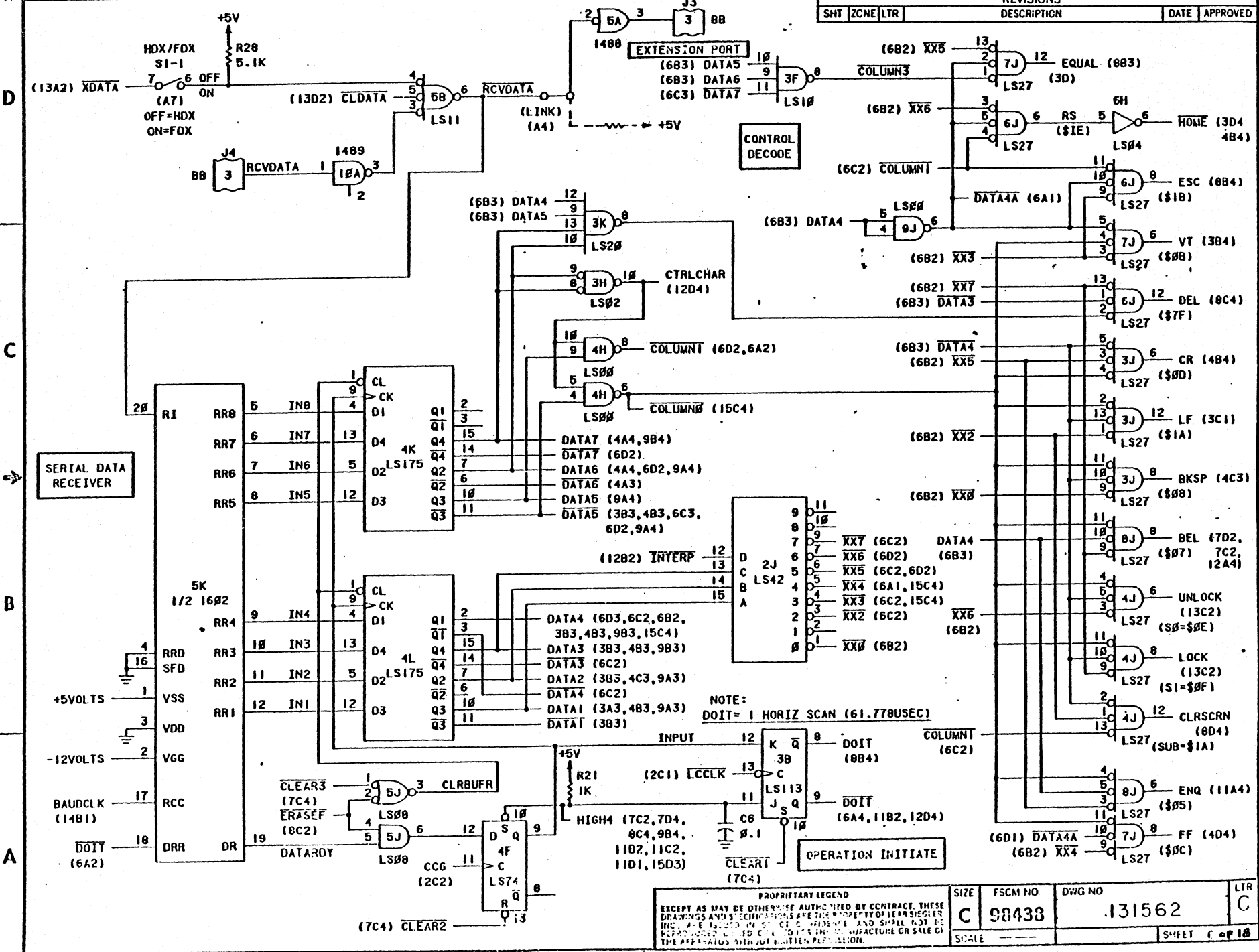
B

REFRESH MEMORY ADDRESS GENERATOR

A

PROPRIETARY LEGEND			SIZE	FSCM NO.	DWG NO.	LTR
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LARSEN ELECTRONICS, INC. AND SHALL BE KEPT IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR DISTRIBUTED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF LARSEN ELECTRONICS, INC.			C	99439	131562	C
			SCALE	NONE		SHEET 5 OF 18

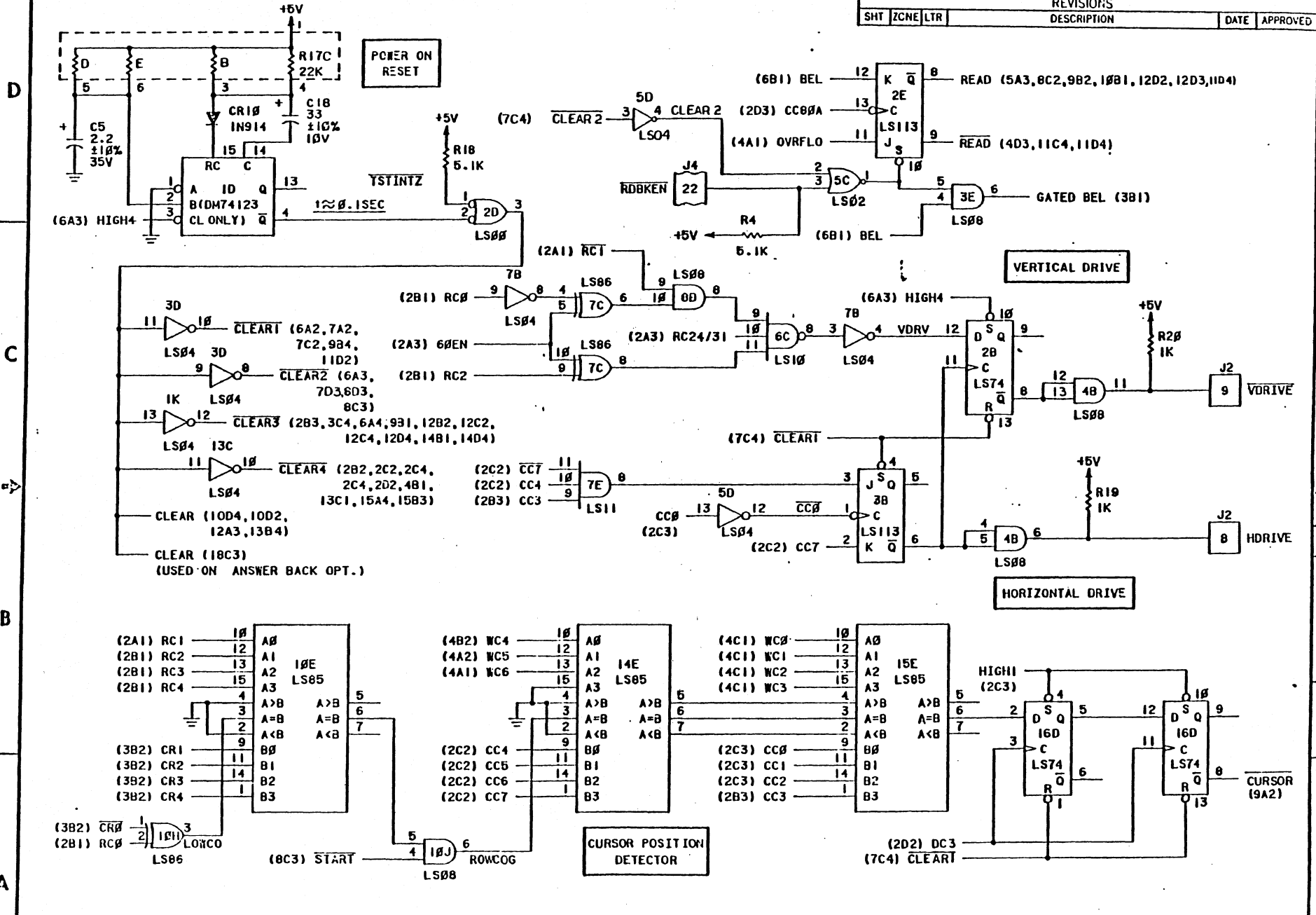
REVISIONS			DATE	APPROVED
SHT	ZCNE	LTR	DESCRIPTION	



SIZE	FSCM NO	DWG NO.	LTR
C	98438	.131562	C
SCALE			SHEET 1 of 18

PROPRIETARY LEGEND
 EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SINGLES INC. AND ARE LOANED TO YOU IN CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, EITHER IN WHOLE OR IN PART, OR THE SALE OF THE APPARATUS THEREOF WITHOUT WRITTEN PERMISSION.

REVISIONS			
SHT	ZCNE	LTR	DESCRIPTION



PROPRIETARY LEGEND			
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAT SIEGLER INC. AND ARE ISSUED UNDER CONTRACT AND SHALL NOT BE REPRODUCED, COPIED, OR IN ANY MANNER DISSEMINATED OR SALE OF THE ALPHA PLUS WITHOUT WRITTEN PERMISSION.			
SIZE	FSCM NO.	DWG NO.	LTR
C	93439	131562	C
SCALE: NONE			SHEET 7 OF 18

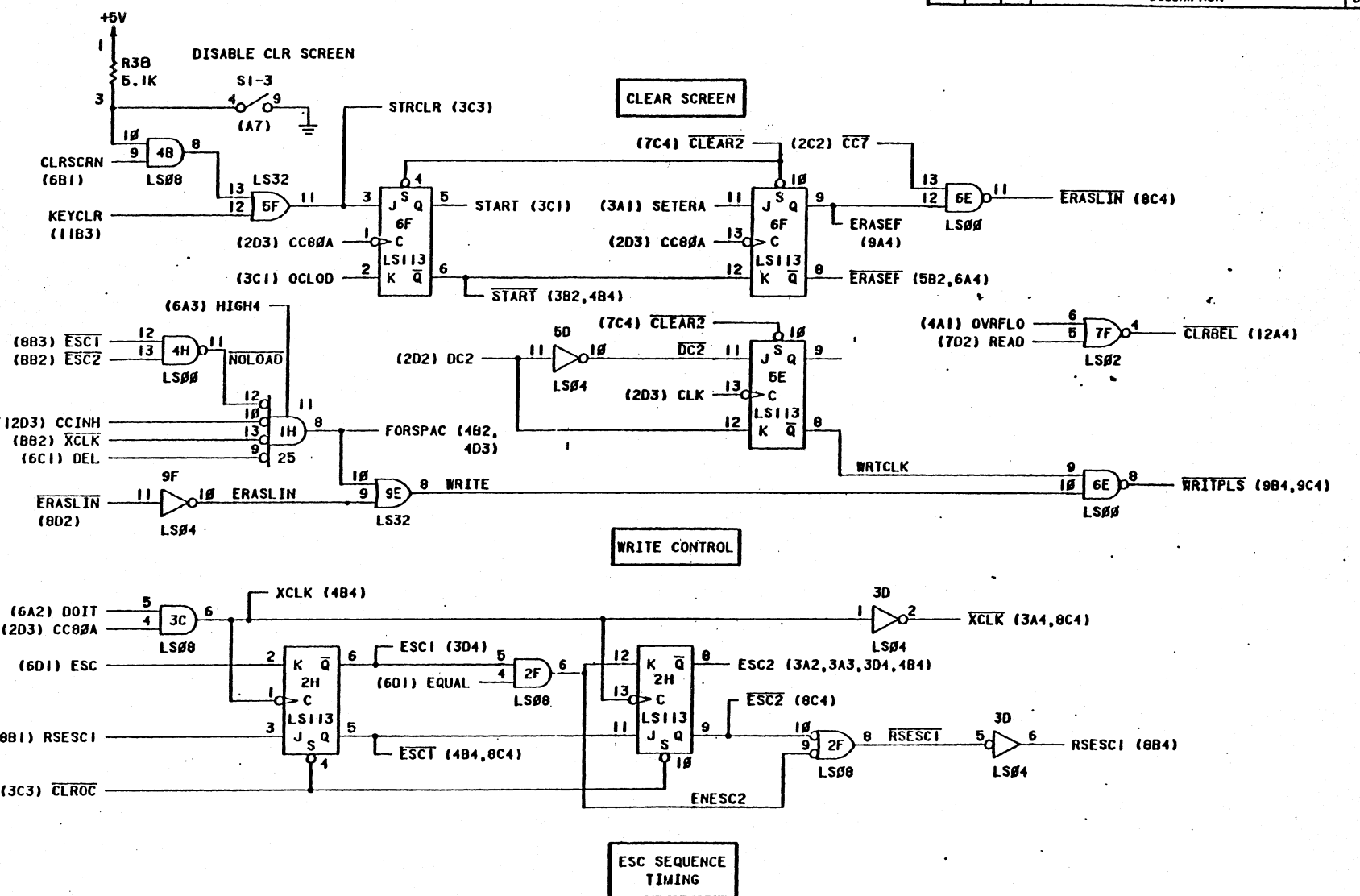
REVISIONS			DATE	APPROVED
SHT	ZONE	LTR	DESCRIPTION	

D

C

B

A



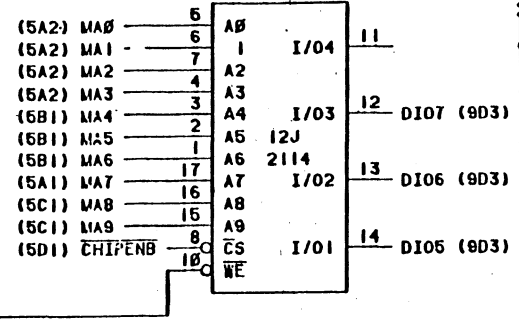
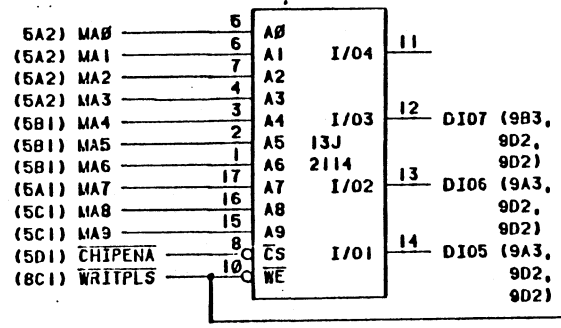
<small> PROPRIETARY LEGEND EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGEL INC. AND SHALL BE KEPT IN CONFIDENTIALITY AND SHALL NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF LEAR SIEGEL INC. </small>				SIZE C	FSCM NO 98439	DWG NO. 131562	LTR C
SCALE NONE			SHEET 6 OF 18				

REVISIONS			DATE	APPROVED
SHT	ZONE	LTR	DESCRIPTION	

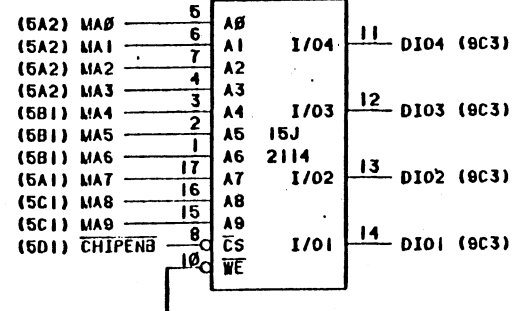
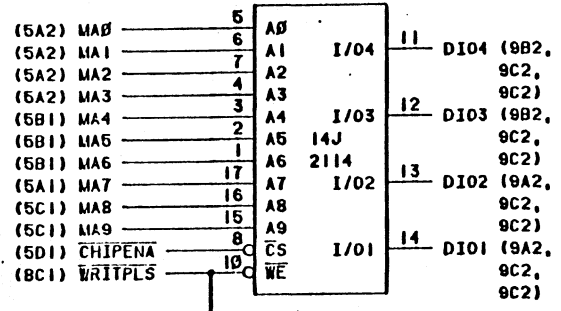
REFRESH MEMORY

+5V
R37
5.1K

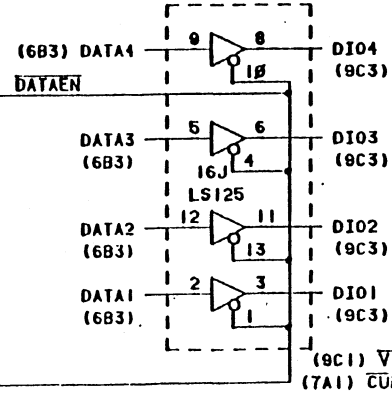
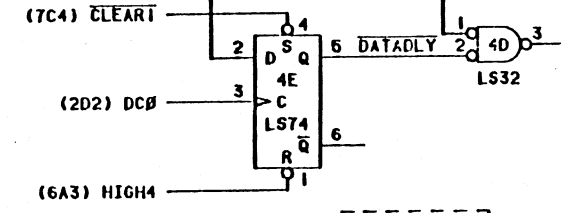
D



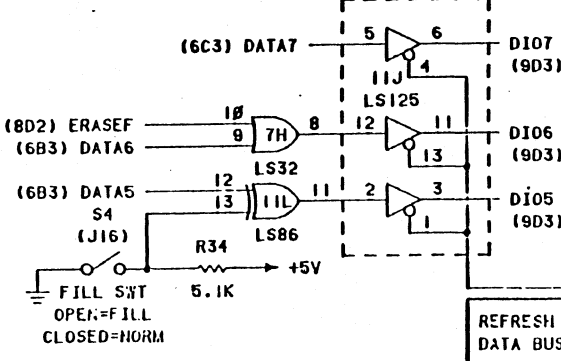
C



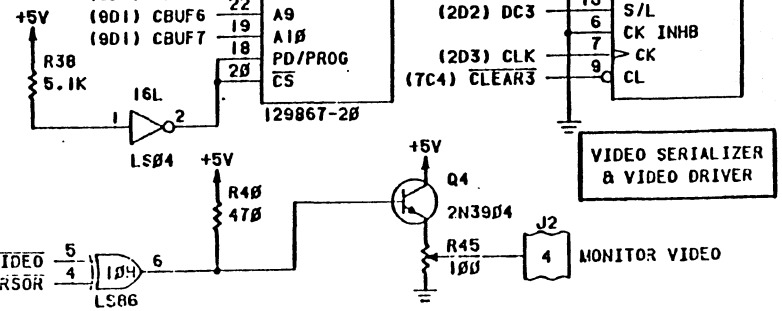
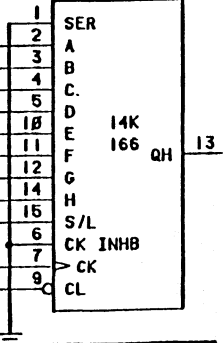
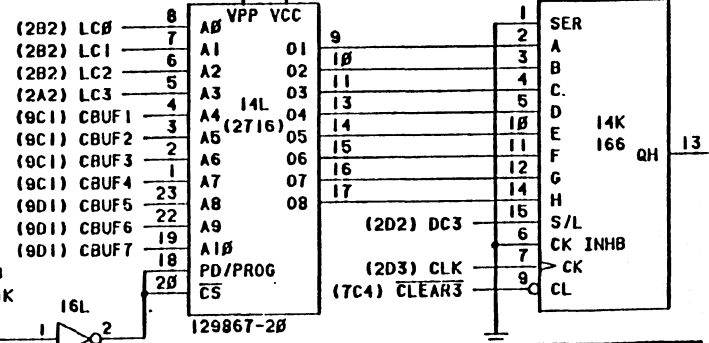
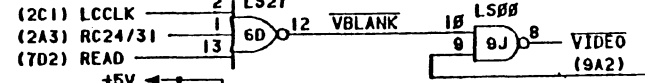
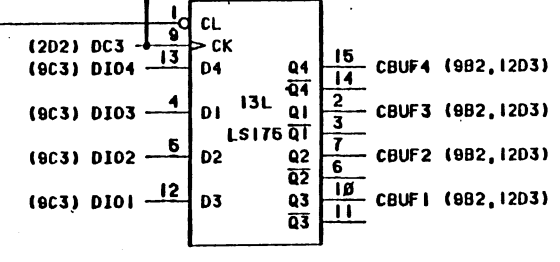
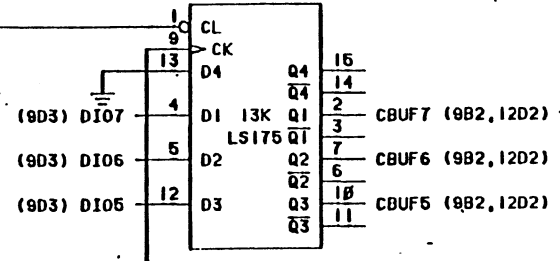
B



A



REFRESH MEMORY DATA BUSS



SIZE	FSCM NO	DWG NO	LTR
C	90433	131562	C
SCALE: NONE			SHEET 9 of 18

PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND CONDITIONS ARE THE PROPERTY OF PERIODIC INC. AND SHALL NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF PERIODIC INC.

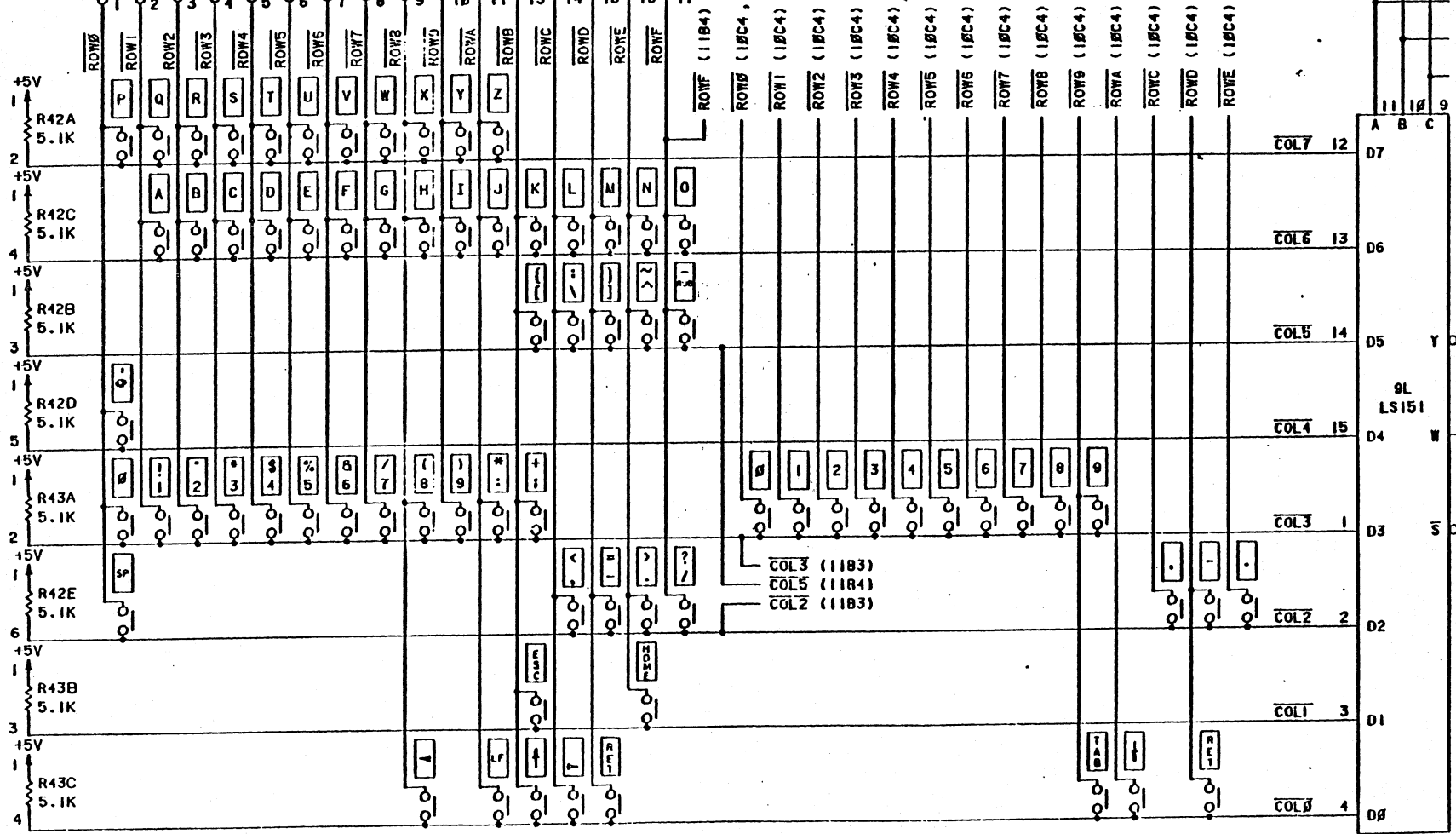
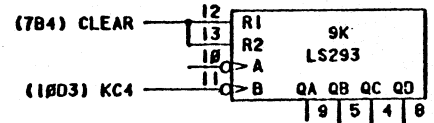
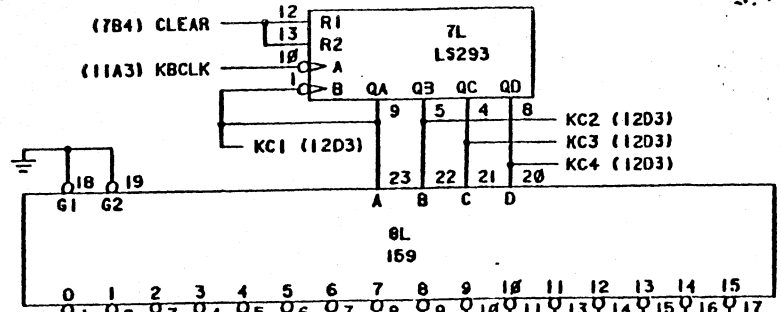
REVISIONS			DATE	APPROVED
SHT	ZONE	LTR	DESCRIPTION	

D

C

B

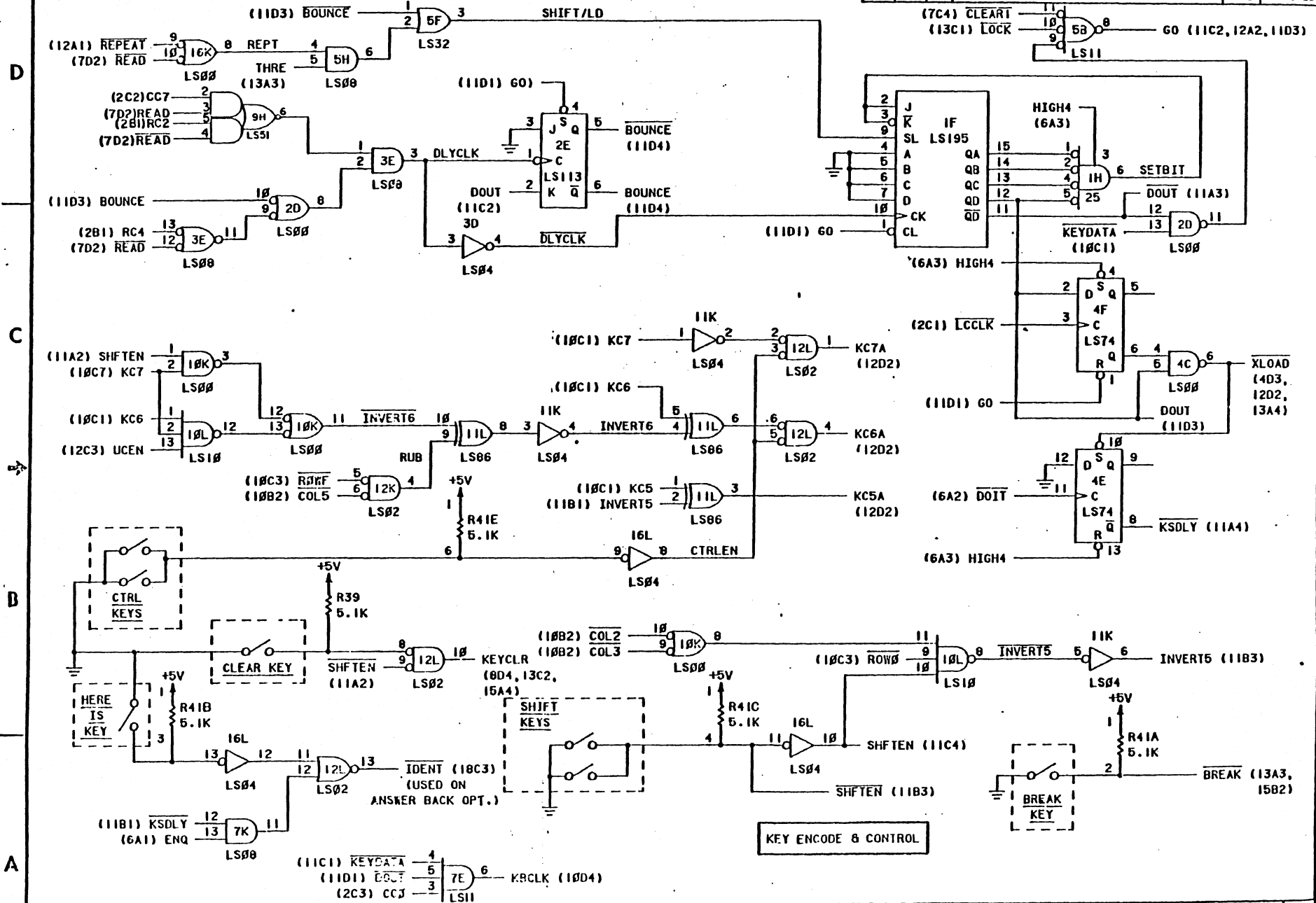
A



KEYBOARD

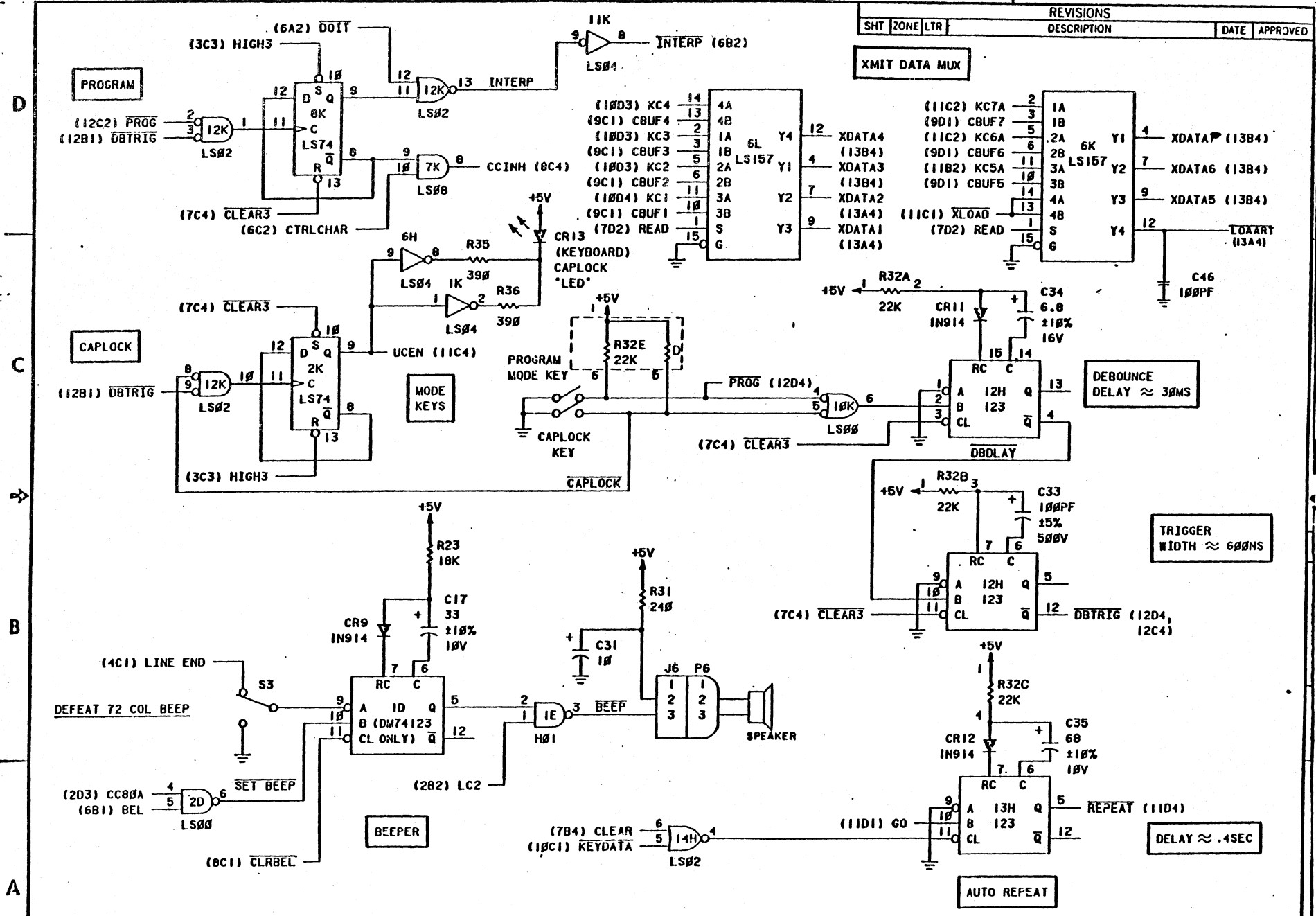
PROPRIETARY LEGEND		SIZE	FSCM NO.	DWG NO.	LTR
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE GRANTINGS AND SPECIFICATIONS ARE THE PROPERTY OF SIEGEL, INC. AND SHALL NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF THE PROPRIETOR.		C	99438	131562	C
SCALE		NONE		SHEET 10 of 18	

REVISIONS				DATE	APPROVED
SHT	ZONE	LTR	DESCRIPTION		
(7C4)			CLEARIT		
(13C1)			LOCK		
			GO (11C2, 12A2, 11D3)		



PROPRIETARY LEGEND EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF SIEGLER INC. AND ARE TO BE USED ONLY FOR THE MANUFACTURE OR SALE OF THE APPLICABLE PRODUCT. OTHER PERMISSIONS			SIZE C	FSCM NO. 98438	DWG NO. 131562	LTR C
SCALE: NONE					SHEET 11 of 18	

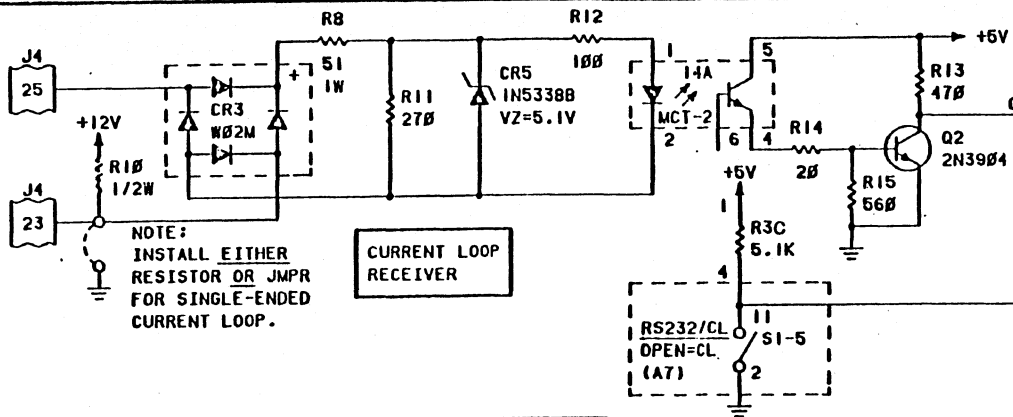
SHT		ZONE		LTR		REVISIONS		DATE	APPROVED
						DESCRIPTION			
						XMIT DATA MUX			



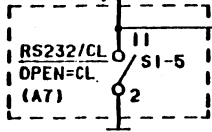
<p>PROPRIETARY LEGEND EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER INC. AND SHALL NOT BE LOANED, REPRODUCED, COPIED, REPRODUCED, OR SALE OF THE APPARATUS WITH OR WITHOUT PERMISSION.</p>				<p>SIZE C</p>	<p>FSCM NO. 98438</p>	<p>DWG NO. 131562</p>	<p>LTR C</p>
				<p>SCALE NONE</p>	<p>SHEET 12 of 18</p>		

REVISIONS			DATE	APPROVED
SHT	ZONE	LTR	DESCRIPTION	

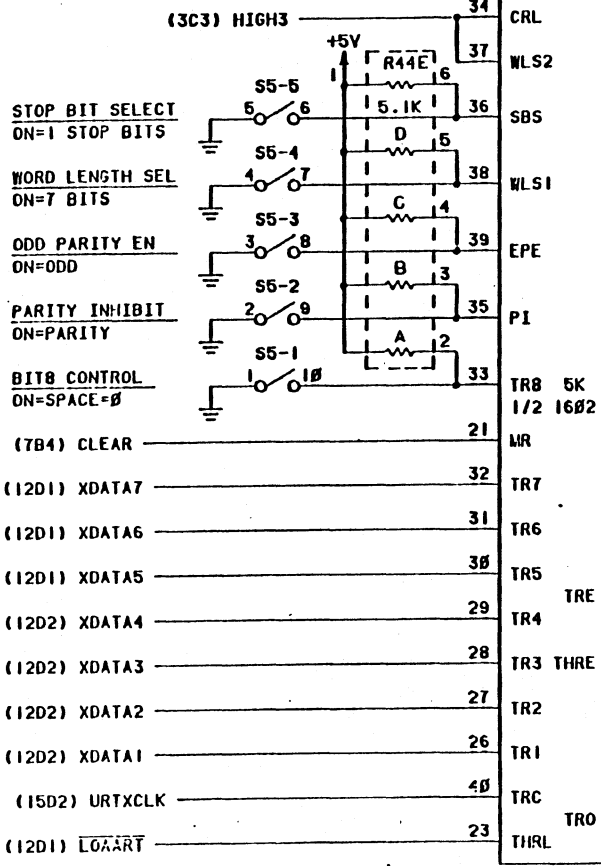
D



CURRENT LOOP RECEIVER

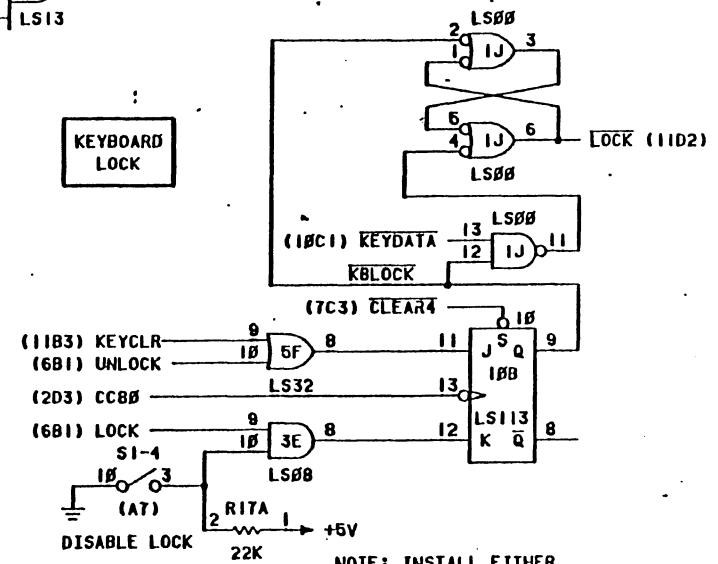


C



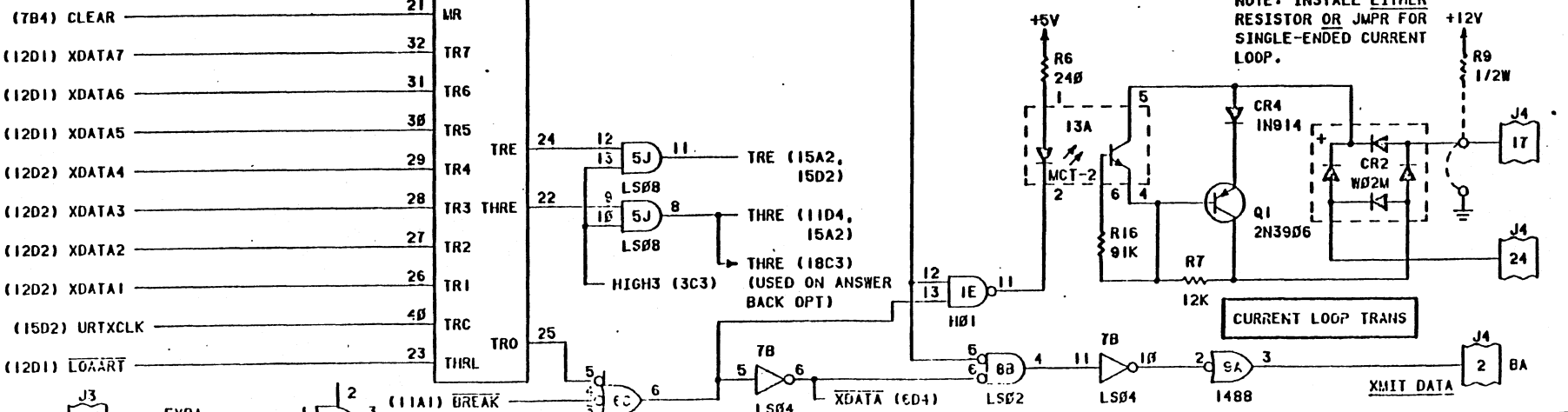
SERIAL DATA TRANSMITTER

B

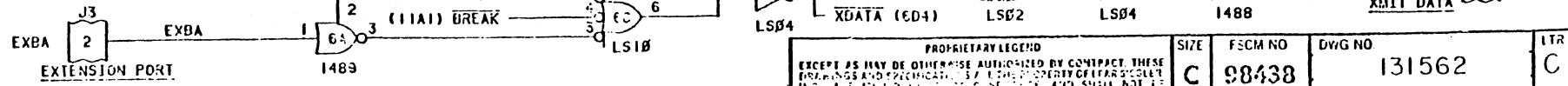


KEYBOARD LOCK

A



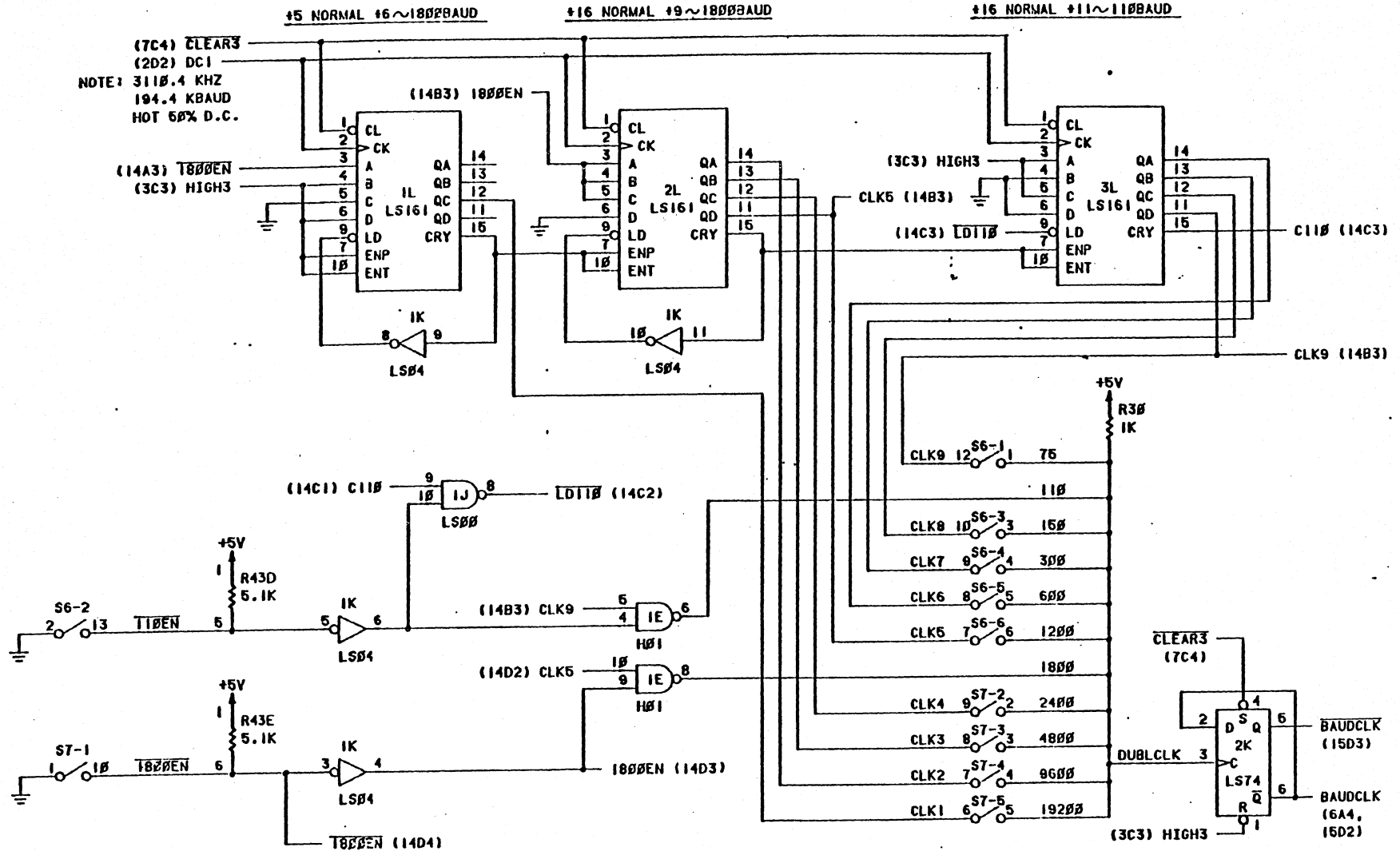
CURRENT LOOP TRANS



EXTENSION PORT

PROPRIETARY LEGEND				SIZE	FSCM NO	DWG NO	LTR
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LARSEN ELECTRONICS, INC. AND SHALL NOT BE REPRODUCED, COPIED, EITHER WHOLLY OR IN PART, OR MANUFACTURED OR SALE OF THE APPARATUS HEREIN WITHOUT PERMISSION.				C	98438	131562	C
				SCALE	NONE		SHEET 13 OF 18

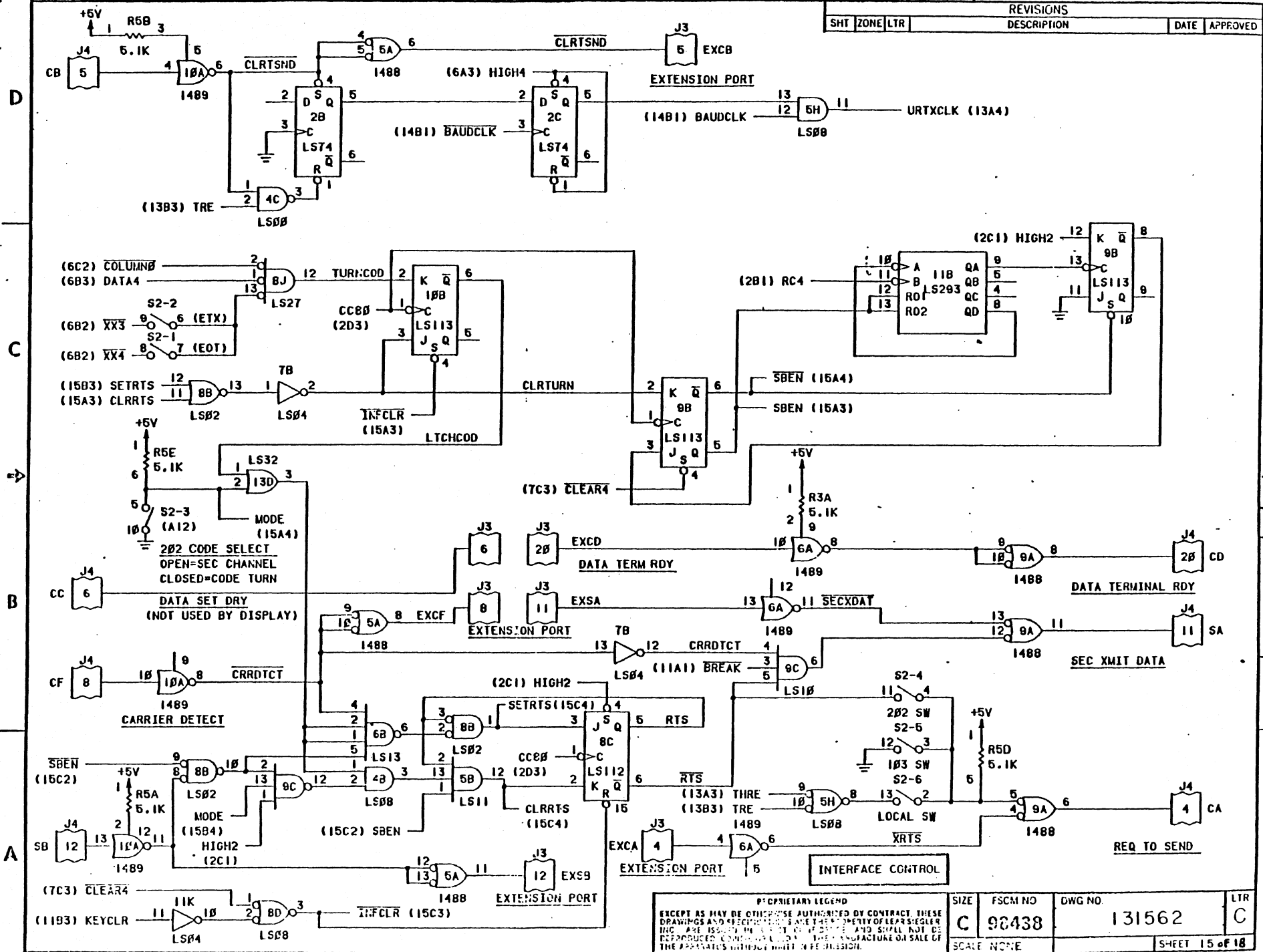
REVISIONS					
SHT	ZONE	LTR	DESCRIPTION	DATE	APPROVED



BAUD RATE GENERATION

PROPRIETARY LEGEND		SIZE	FSCM NO.	DWG NO.	LTR
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER INC. AND ARE LOANED TO YOUR COMPANY. THEY SHALL NOT BE REPRODUCED, COPIED, OR IN ANY MANNER, MANUFACTURE OR SALE OF THE APPROPRIATE PARTS OF ANY OTHER REPRODUCTION.		C	90438	131562	C
SCALE NONE				SHEET 14 of 18	

REVISIONS					
SHT	ZONE	LTR	DESCRIPTION	DATE	APPROVED



PROPRIETARY LEGEND				
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER INC. AND SHALL NOT BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF LEAR SIEGLER INC.				
SIZE	FSCM NO	DWG NO	131562	LTR
C	98438			C
SCALE	NONE			SHEET 15 of 18

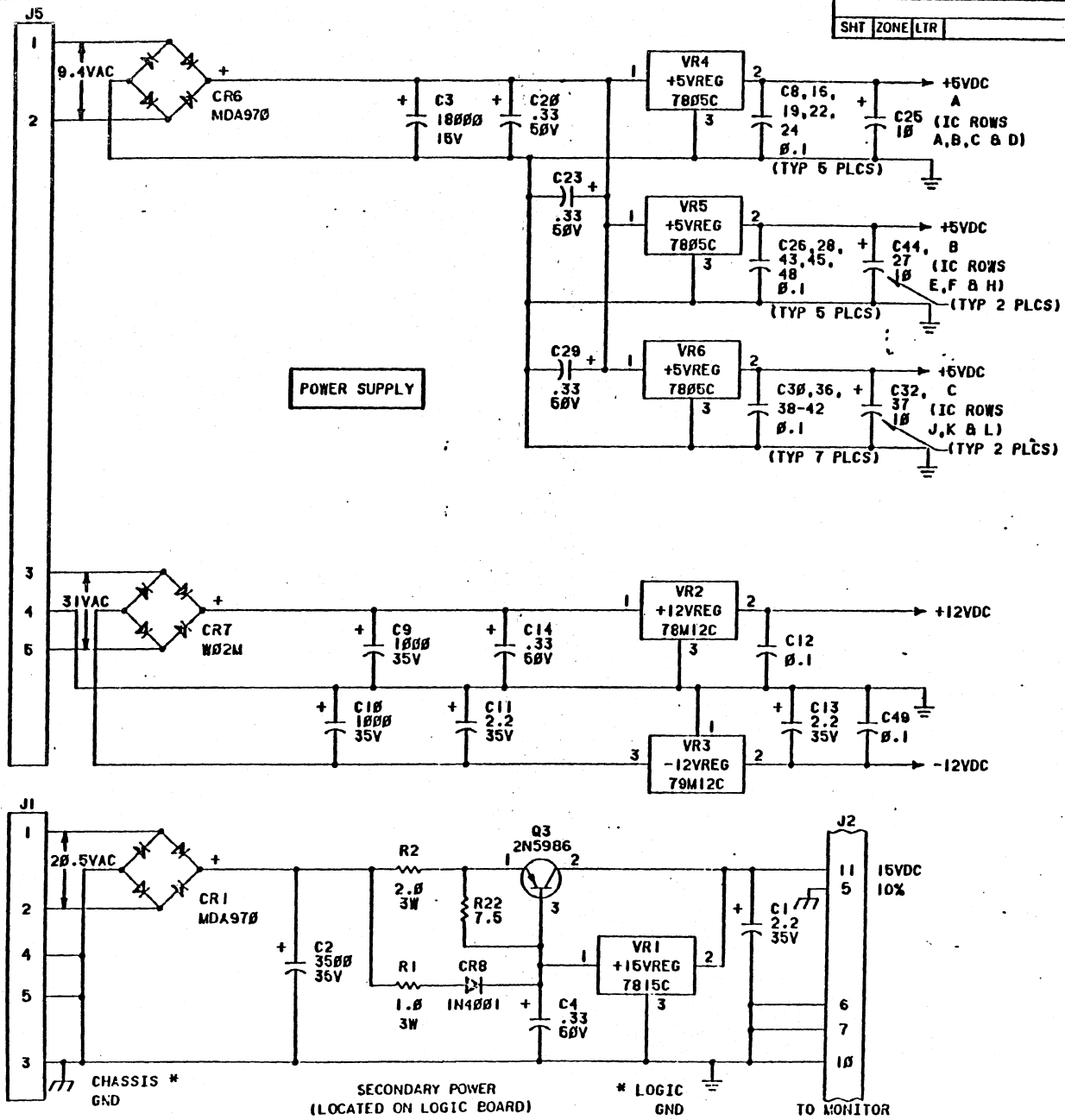
SHT		ZONE	LTR	REVISIONS		DATE	APPROVED
				DESCRIPTION			

D

C

B

A



*NOTE: LOGIC GND AND CHASSIS GND ARE TIED ONLY ONE PLACE ON THE P.C.B.

PROPRIETARY LEGEND				SIZE	FSCM NO.	DWG NO	LTR
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF REP/AS/EGLES, INC. AND ARE LOANED TO YOU FOR YOUR USE ONLY AND SHALL NOT BE REPRODUCED, COPIED, OR IN ANY MANNER MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.				C	93438	131562	C
SCALE: NONE				SHEET 16 OF 18			

CONN PIN ASSIGNMENTS

REVISIONS				DATE	APPROVED
SHT	ZONE	LTR	DESCRIPTION		

SWITCH ASSIGNMENTS

J1 POWER INPUT

PIN NO.	FUNCTION	SHEET
1	2Ø.5VAC	16B4
2	2Ø.5VAC	16B4
3	CHASSIS GND	16A4
4	GND	16A4
5	GND	16A4

J4 MODEM RS 232 B
CURRENT LOOP

PIN NO.	FUNCTION	SHEET
1	FRAME GND	
2	BA	13A1
3	BB	6D4
4	CA	15A1
5	CB	16D4
6	CC	15B4
7	GND	
8	CF	15B4
9	**	
1Ø	NOT USED	
11	SA	15B1
12	SB	15A4
13	**	
14	**	
15	**	
16	**	
17	CL OUT	13B1
18	**	
19	**	
2Ø	CD	15B1
21	**	
22	READ BACK EN	7D2
23	CL INPUT	13D4
24	CL OUT	13A1
25	CL INPUT	13D4

J2 MONITOR

PIN NO.	FUNCTION	SHEET
1	(KEYPIN)	
2		
3		
4	VIDEO	9A1
5	CHASSIS GND	16B2
6	VERT GND	16A2
7	GND	16B2
8	H DRIVE	7B2
9	V DRIVE	7C1
1Ø	HORIZ GND	16A2
11	+15V	16B2
12		

J3 EXTEN RS232

PIN NO.	FUNCTION	SHEET
1	FRAME GND	
2	EX BA	13A4
3	EX BB	6D3
4	EX CA	15A2
5	EX CB	15D2
6	CC	15B3
7	GND	
8	EX CF	15B3
9	**	
1Ø	-12V*	
11	EX SA	15B3
12	EX SB	15A3
13	**	
14	**	
15	**	
16	**	
17	+12V*	
18	**	
19	**	
2Ø	EX CD	15B3
21	**	
22	NOT USED	
23	NOT USED	
24	EXT CL IN*	
25	EXT CL OUT*	

J5 POWER INPUT

PIN NO.	FUNCTION	SHEET
1	9.4VAC	16D3
2	9.4VAC	16D3
3	3IVAC	16B3
4	GND	16B3
5	3IVAC	16B3

J6 SPEAKER

PIN NO.	FUNCTION	SHEET
1	NOT USED	
2	SPEAKER	12A3
3	SPEAKER	12A3

K6

(7D2) READ	O 1	16 O	+5VOLTS	
(11C2) KC7A	O 2	15 O	GND	
(9D1) CBUF7	O 3	14 O	XLOAD	(11C1)
(12D1)XDATA7	O 4	13 O	XLOAD	
(11C2) KC6A	O 5	12 O	XDATA7	(12C1)
(9D1) CBUF6	O 6	11 O	KC5A	(11B2)
(12D1)XDATA6	O 7	1Ø O	CBUF5	(9D1)
GND	O 8	9 O	XDATA5	(12C1)
(11A3) IDENT	O 17	18 O	THRE	(13A3)

ANSWER BACK OPT 2

L6

(2C3) WRCLK	O 17	18 O	CLEAR	(7B4)
(7D2) READ	O 1	16 O	+5VOLTS	
(1ØD3) KC3	O 2	15 O	GND	
(9C1) CBUF3	O 3	14 O	KC4	(1ØD3)
(12D2)XDATA3	O 4	13 O	CBU4	(9C1)
(1ØD3) KC2	O 5	12 O	XDATA4	(12C2)
(9C1) CBUF2	O 6	11 O	KC1	(1ØD4)
(12D2)XDATA2	O 7	1Ø O	CBUF1	(9C1)
GND	O 8	9 O	XDATA1	(12C2)

S1

SEC-TION	FUNCTION	SHEET
1	HDX/FDX	6D4
2	SØ/6ØH2	2A3
3	DIS CLR SCRN	8D4
4	DIS LOCK	13B2
5	RS232/CL	13C3

S6

SEC-TION	FUNCTION	SHEET
1	75	14C2
2	11Ø	14B4
3	15Ø	14B2
4	3ØØ	14B2
5	6ØØ	14B2
6	12ØØ	14B2

S2

SEC-TION	FUNCTION	SHEET
1	EOT	15C4
2	ETX	15C4
3	CODE	15B4
4	2Ø2	15B2
5	1Ø3	15A1
6	LOCAL	15A2
7	AUTO NEW LINE	4C4

S7

SEC-TION	FUNCTION	SHEET
1	18ØØ	14B4
2	24DØ	14B2
3	48ØØ	14B2
4	96ØØ	14B2
5	192ØØ	14A2

S3

FUNCTION	SHEET
DEFEAT 72	12B4
CLO BEEP	

S4

FUNCTION	SHEET
FILL SW	9A4

S5

SEC-TION	FUNCTION	SHEET
1	BIT 8 CONTROL	13B4
2	PARITY INHBIT	13B4
3	ODD PARITY EN	13C4
4	WORD LENGTH	13C4
5	STOP BIT	13C4

*WHEN OPTIONAL EXTENSION PORT CURRENT LOOP INSTALLED
*KNO SOCKET INSTALLED IN CONNECTOR

PROPRIETARY LEGEND		SIZE	FSCM NO.	DWG NO.	LTR
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER INC. AND ARE LOANED TO YOUR OFFICE. YOU AND YOUR EMPLOYEES SHALL NOT BE PERMITTED TO REPRODUCE OR TRANSMIT IN ANY MANNER OR FOR ANY PURPOSE THE APPEARANCE OR CONTENTS OF THESE DRAWINGS.		C	92438	131562	C
SCALE: NONE				SHEET 18 of 18	

APPENDIX C

REVISIONS		SYMBOL	SHEET	DESCRIPTION	APPROVED	DATE															
<p style="margin-left: 20px;"><i>NOTE</i></p> <p style="margin-left: 20px;">1. INSTALL OPTION PACKAGE "A" (SEE SH 3) ON PC. BOARD 129460 IF OPTION 1, 2, 3, OR 5 ARE INDICATED.</p>																					
RECORD OF REVISION STATUS OF EACH SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
		DR				LEAR SIEGLER, INC. ELECTRONIC INSTRUMENTATION DIVISION, ANAHEIM, CALIF.		<p style="font-size: 1.2em; margin: 0;"><i>CONFIGURATION CONTROL -</i></p> <p style="font-size: 1.2em; margin: 0;"><i>ADM-3</i></p>													
		CHK																			
		DSGN																			
		ENGR																			
		PROJ																			
		REL																			
DASH NO.		NEXT ASSY		APP'D		APP'D		CODE IDENT NO	SIZE	REV											
<i>ADM-3</i>								98438	B	<i>129502</i>											
APPLICATION		DO NOT SCALE DRAWING		SCALE				SHEET 1 OF 8		DISTR											

@A6

SPACE	6	ADV
UC DISP	5	1/4 DISP
DISABLE	4	KB LOCK
DISABLE	3	CLEAR SCREEN
50HZ	2	60 HZ
12 LINE	1	24 LINE

@A10

LOCAL	6	OFF
103	5	OFF
202	4	OFF
CODE	3	SEC CHAN
ETX	2	OFF
EOT	1	OFF

KEYBOARD

BIT 0	6	1
PRIORITY	5	INH
STOP 1	4	2
DATA 7	3	8
PAR. ODD	2	EVEN
LC EN	1	UC

AUTO NL	7	OFF
RS 232	6	CL
MDX	5	ADK
19200	4	
9600	3	
4800	2	
2400	1	
1800	7	
1200	6	
600	5	
300	4	
150	3	
110	2	
75	1	

SELECT ONLY ONE

BAUD RATE

CODE IDENT NO.	SIZE	REV
98438	B	129502
SHEET		2

OPTION PACKAGE A

PARTS LIST

PND NO.	QTY REQD			PART NO.	DESCRIPTION	VENDOR	LOCATION/REFS	NOTE
1			✓		FOR 24 LINE			
2		✓			FOR 12 LINE			
3								
4		2	2	CA-18S-10SD	SOCKET	CIRCUIT ASSY	K6, L6	
5		2	3	CA-16S-10SD	"	"	J8, H8(24 LINE) CONN J6	
6		1	1	CA-24S-10SD	"	"	J7	
7								
8		1	1	22-02-2051	CONNECTOR	MOLEX	NEAR CONN J2	A
9		1	1	22-02-2041	"	"	"	A
10								
11								

A. REMOVE TABS

THIS OPTION IS MANDATORY FOR ANY 129460 WHICH WILL CONTAIN OPTIONS 1, 2, 3 OR 5

CODE IDENT NO.	SIZE	129502	REV
98438	B		
			SHEET 3

OPTION 1 LOWER CASE								
PARTS LIST								
PART NO.	QTY	REQD		PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
		1B	1A					
1			✓	1A	LOWER CASE - 12 LINE			
2		✓		1B	LOWER CASE - 24 LINE			
3								
4								
5		1	1	129323-02	CHAR GEN		J7	
6		2	1	128348-4102	RAM		J8, H8(18)	
7								
8								
9								

INSTALL PARTS PER 129460
SEE NOTE 1 ON SHT 1

OPTION 2 ANSWER BACK								
PARTS LIST								
PART NO.	QTY	REQD		PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
		1B	1A					
1			✓	2	ANSWER BACK			
2								
3		1		129489-01	P.C. BOARD ASSY			
4								
5		2		CA-D-18P02-261-C-014	DIP INTERCONNECT	CIRCUIT ASSEMBLY		
6								
7		2		4(.125)-20 x $\frac{5}{16}$ LG	SCREW - PLASTITE, HEX WASH HD, SLOTTED, STL, CAD PL	CONTINENTAL SCREW CO.		
8								
9								

REMOVE 2 157 I.C.'S AT L6 & K6 AND INSTALL ON F/N 3
INSTALL F/N 3 UNDER MAIN P.C. BOARD WITH F/N 7 SCREWS
INTERCONNECT WITH F/N 5 TO L6 & K6 ON MAIN BOARD
SEE NOTE 1 ON SHT 1

CODE IDENT NO.	SIZE	REV
98438	B	129502
SHEET		4

OPTION 3 NUMERIC KEY PAD

PARTS LIST

FIND NO.	QTY REQD			PART NO	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1			✓	3				
2								
3								
4								
5			1		CABLE			
6			1	129490-01	NUMERIC KEY PAD ASSY			
7								
8								
9								

ROUTE CABLE (EIN 5) THRU BOTTOM VENTILATION HOLE
SEE NOTE 1 ON SHT 1

OPTION 4 DISPLAY TEST

PARTS LIST

FIND NO.	QTY REQD			PART NO	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
1			✓	4				
2								
3								
4			1	MSS-104 D	SWITCH	ALCO		
5								
6								
7								
8								
9								

CODE IDENT NO.	SIZE	REV
98438	B	129502

SHEET 5

OPTION 5 EXTENSION PORT CURRENT LOOP

PARTS LIST

PART NO.	QTY REQD			PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
	1	2	3					
1			✓	5	EXT. PORT C.L.			
2								
3								
4		1		129488-01	P.C. BOARD ASSY			
5								
6								
7								
8								
9								

INSTALL IN SOCKETS NEAR J2 CONNECTOR
SEE NOTE 1 ON SMT 1

OPTION 6 SPLIT BAUD RATE

PARTS LIST

PART NO.	QTY REQD			PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
	1	2	3					
1			✓	6	SPLIT BAUD RATE			
2								
3								
4		-						
5		1		CTS 235-1	SWITCH, 12 POS	CTS		
6								
7								
8								
9								

INSTALL SWITCH PER 129460
CUT ETCH AT 76 BAUD SWITCH
(SEE ENGINEERING)

CODE IDENT NO.	SIZE	REV
98438	B	129502
SHEET		6

OPTION 11 230 VOLT AC, EUROPEAN

PARTS LIST

P/N NO	QTY REQD			PART NO	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
			11					
1			✓	11				
2								
3								
4		1		129458-05	TRANSFORMER			
5								
6		1		129455-05	POWER CORD			
7								
8		1		129456-05	NAMEPLATE			
9								

OPTION 12 230 VOLT AC, AUSTRALIAN

PARTS LIST

P/N NO	QTY REQD			PART NO	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE
			12					
1			✓	12				
2								
3								
4		1		129458-05	TRANSFORMER			
5								
6		1		129455-07	POWER CORD			
7								
8		1		129456-05	NAMEPLATE			
9								

CODE IDENT NO.	SIZE	REV
98438	B	129502
SHEET		7

OPTION 21 CABLE										
PARTS LIST										
PMSB NO.	QTY RECD				PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE	
				21						
1				✓	-21					
2										
3										
4			1		129316-11	CABLE				
5										
6										
7										
8										
9										
OPTION										
PARTS LIST										
PMSB NO.	QTY RECD				PART NO.	DESCRIPTION	VENDOR	LOCATION/REF DES	NOTE	
1										
2										
3										
4										
5										
6										
7										
8										
9										
					CODE IDENT NO.	SIZE				REV
					98438	B	129502			
								SHEET	8	

▽
REVISIONS

LTR	SHEET	DESCRIPTION	DATE	APPROVED
A		RELEASED PER DCN 490	1-16-80 11/2/80	RC [Signature] [Signature]

	131551	DL131550
DASH NO.	NEXT ASSY	USED ON
APPLICATION		

UNLESS OTHERWISE SPECIFIED
DIM. IN INCHES
TOLERANCES
X ± .1
XX ± .03
XXX ± .010
ANGLES ± 0.5°
MACH. FIN.

J

DR *[Signature]*
CHK *[Signature]*
DSGN *[Signature]*
ENGR *[Signature]*
PROJ *[Signature]*
REL *[Signature]*
CUSTOMER APPD
[Signature]



LEAR SIEGLER, INC.
ELECTRONIC INSTRUMENTATION DIV.
ANAHEIM, CALIF.

OPTIONS
ADM 3A+

SIZE	CODE IDENT	REV
A	98438	A
SCALE	SHEET 1 OF 4	

131552

QTY. REQD		PARTS LIST			
No.		PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1					
2					
3	1	129489-01	P.C. BOARD ASSY		
4					
5	2	812002	CABLE		
6	2	821403	SCR. 4- ⁵ / ₁₆ PLASTITE		
7					
8					
9					
10					
11					
12					
13					

A. REMOVE 2 74LS157 IN SOCKETS AT K6 & L6.
 INSTALL P.C.B. ASSY, F/N 3, UNDER MAIN P.C.B.
 WITH F/N 6 SCREWS.
 INTERCONNECT WITH F/N 5 CABLES TO K6 & L6.
 RUN DIRECT, DO NOT CROSS.

OPTION 1	SIZE	CODE IDENT	REV
TITLE ANSWER BACK	A	98438	131552 A
SHEET 1 OF 1	SCALE	SHEET	2

QTY REQD		PARTS LIST			
LINE NO.		PART NUMBER	DESCRIPTION	LOCATION/REF DES	NOTES
1					
2					
3	1	129488-01	P.C. BOARD ASSY		B
4					
5					
6	1	809001	CONN (22-02-204)	J7	A
7	1	809002	CONN (22-02-205)	J8	A
8					
9					
10					
11					
12					
13					

A. REMOVE TABS

B. INSTALL P.C.B ASSY IN. J7 & J8 NEAR J2

ACCESSORIES

CABLE, I/O - 129316-11

Form 10-1011a

SIZE	CODE IDENT	REV
A	98438	131552 A
SCALE	SHEET 4	



CONTAINS INDIVIDUAL KEYCAP PART NUMBERS AND THEIR ASSIGNED STATION NUMBERS ON THE KEYBOARD.

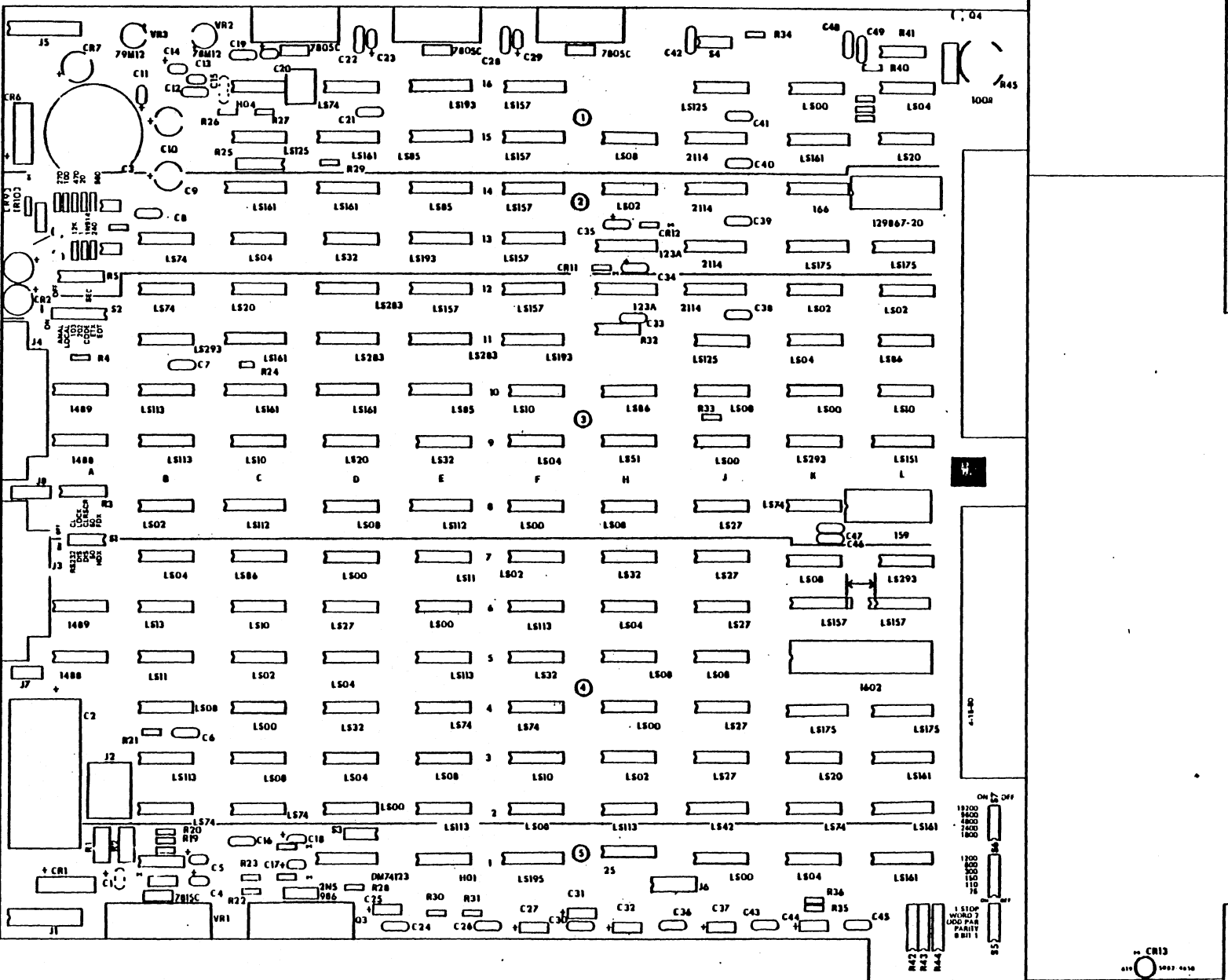
<u>STA NO.</u>	<u>131553</u>	<u>STA NO.</u>	<u>131553</u>
1.2	131663-2	43	131664-135
1.4	131665-4	44	131664-136
1	131664-144	45	131664-137
6	131664-115	46	131664-121
7	131664-117	47	131670-1
8	131664-119	48	131664-1
9	131664-113	49	131664-19
10	131664-114	50	131664-4
11	131669-1	51	131664-6
12	131664-45	52	131664-7
13	131664-46	53	131664-8
14	131664-47	54	131664-10
15	131664-48	55	131664-11
16	131664-49	56	131664-12
17	131664-50	57	131664-57
18	131664-51	58	131664-58
19	131664-52	59	131664-59
20	131664-53	60	131667-7
21	131664-55	61	131664-131
22	131664-59	62	131664-133
23	131664-53	63	131664-134
24	131664-5	64	131665-5
25	131664-138	65	131665-1
26	131664-139	66	131664-26
27	131664-140	67	131664-24
28	131664-143	68	131664-3
29	131668-3	69	131664-22
30	131664-17	70	131664-2
31	131664-23	71	131664-14
32	131664-5	72	131664-13
33	131664-18	73	131664-63
34	131664-20	74	131664-62
35	131664-25	75	131664-64
36	131664-21	76	131665-1
37	131664-3	77	131664-84
38	131664-15	78	131664-142
39	131664-16	79	131664-116
40	131664-56	80	131664-141
41	131664-94	81	131667-9
42	131669-1	82	131666-1
		83	131667-8

NOTE: 1. FOR REPLACEMENT PARTS REFER TO PART NUMBERS FOR INDIVIDUAL KEYCAPS SHOWN.

DRAWING NO. 131553
(Sheet 2 of 2)

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

REV. 001



P.C. Board Ass'y, ADM 3A+; From Engineering Drawing No. 131560 (1 of 2)

NOTES UNLESS OTHERWISE SPECIFIED

1. FOR OPTIONS REFER TO 131552 INDICATED AS FOLLOWS

① ANSWER BACK

② EXTENSION PORT CURRENT LOOP

2. FOR SCHEMATIC REFER TO 131562.

3. FOR PRINTED WIRING BOARD SEE 131561.

④ FOR HEATSINK MTG ASSY INSTRUCTIONS SEE 131579

5. KEYBOARD INSTALLATION INSTRUCTIONS

THE F/N 9 KEYBOARD CONSISTS OF 4 MODULES RETAINED IN POSITION ON PC BOARD WITH SCREWS F/N 134 THE KEYTOPS OF THE MODULES SHOULD BE POSITIONED WITH .035 TO .062 GAP TO THE KEYTOP OF ADJACENT MODULES WHEN INSTALLED. IF DIMENSION EXCEEDS ABOVE CLEAN OFF EXCESS PLASTIC FROM MODULE BASE AND REINSTALL.

6. LED INSTALLATION INSTRUCTIONS SECTION (A-A)

AFTER KEYBOARD IS INSTALLED REMOVE CAP LOCK KEYTOP POSITION LED IN WELL ON KYBD ORIENT LED AS IN SECTION A A WITH FLAT TO REAR OF KYBD REINSTALL KEYTOP DEPRESS KEY ALLOWING LED TO TOUCH KEYTOP LENS. CENTER LED UNDER LENS (IT WILL BE TO THE REAR OF KYBD., NOT IN CENTER OF WELL. SOLDER IN PLACE RELEASE KEY

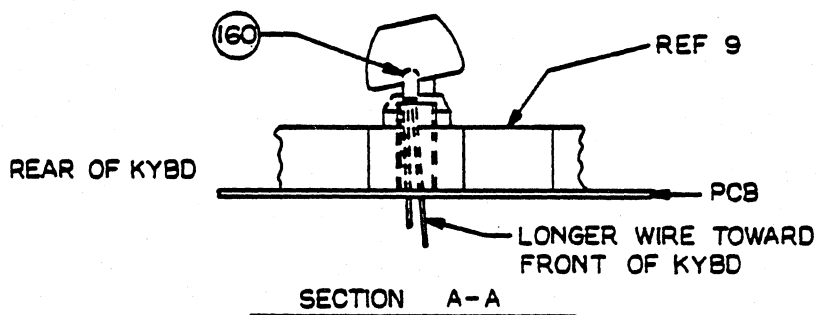
7. MODIFICATION INSTRUCTIONS FOR-9 BD

A. CUT ETCH AT 15L-12 SOLDER SIDE.

B. CUT ETCH BETWEEN 14L-6 AND 15L-12, COMPONENT SIDE.

C. ADD JUMPER WIRE (30 AWG) FROM 15L-12 TO 15L-14, COMPONENT SIDE.

D. ADD JUMPER WIRE (30AWG) FROM 15K-12 TO 14L-6, COMPONENT SIDE.



FOR PARTS SEE P/L 131560

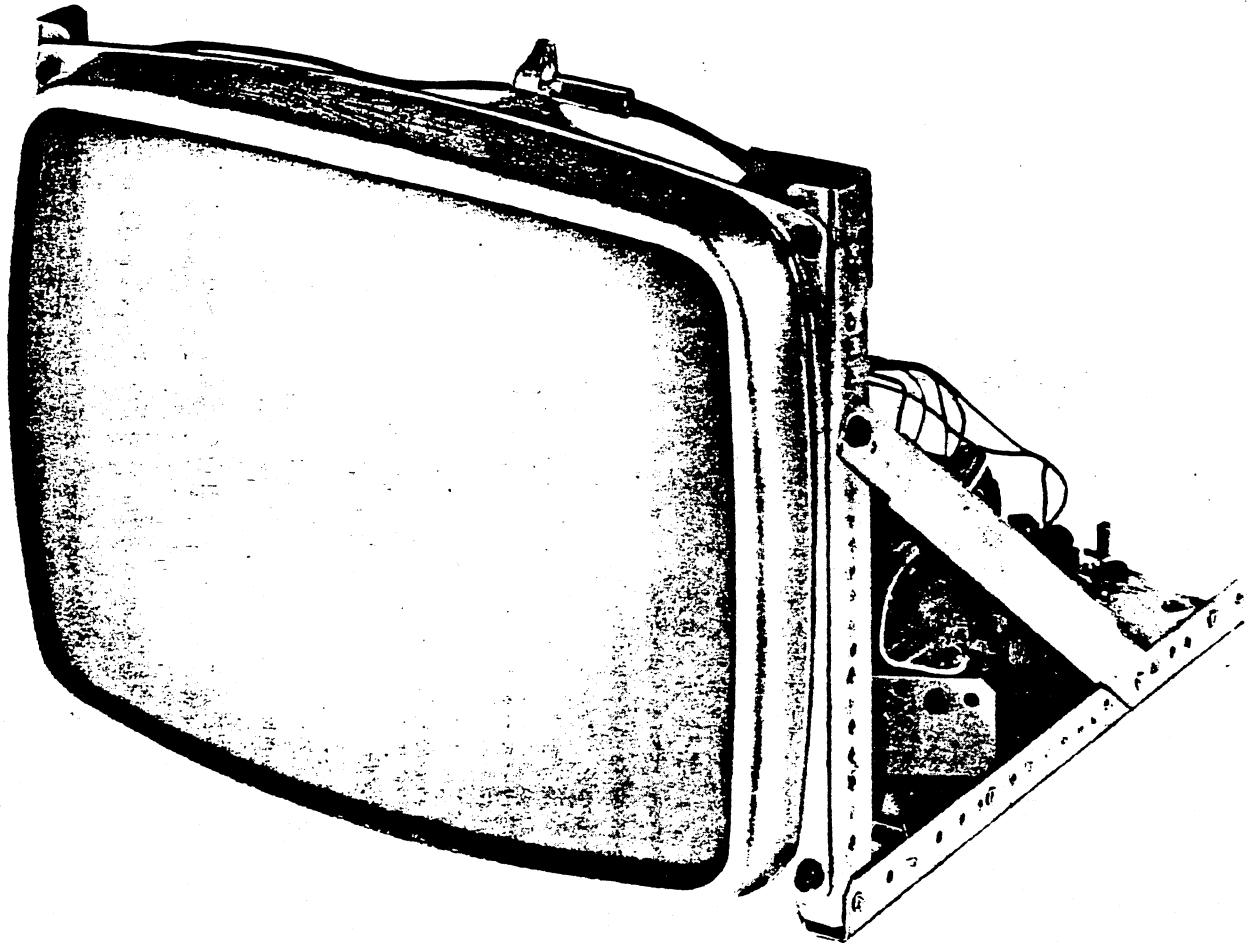
APPENDIX D

DT2

DT2



SERVICE MANUAL



DT2

D12 SERIES DATA DISPLAY TERMINALS

ZENITH RADIO CORPORATION

1000 MILWAUKEE AVENUE, GLENVIEW, ILLINOIS 60025

PRODUCT SAFETY SERVICING GUIDELINES FOR ZENITH DATA DISPLAY TERMINALS

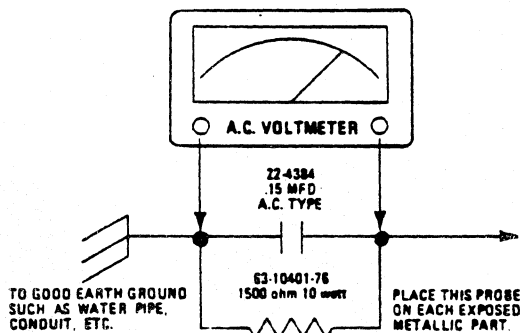
CAUTION: No modification of any circuit should be attempted. Service work should be performed only after you are thoroughly familiar with all of the following safety checks and servicing guidelines. To do otherwise increases the risk of potential hazards and injury to the user.

SAFETY CHECKS

After the original service problem has been corrected, a check should be made of the following:

SUBJECT: FIRE & SHOCK HAZARD

1. Be sure that all components are positioned in such a way to avoid possibility of adjacent component shorts. This is especially important on those chassis which are transported to and from the repair shop.
2. Never release a repair unless all protective devices such as insulators, barriers, covers, shields, strain reliefs, and other hardware have been reinstalled per original design.
3. Soldering must be inspected to uncover possible cold solder joints, frayed leads, damaged insulation, solder splashes or sharp solder points. Be certain to remove all loose foreign material.
4. Check "across-the-line" capacitor (if used) and other components for physical evidence of damage or deterioration and replace if necessary. Follow original layout, lead length and dress.
5. No lead or component should touch a resistor rated at 1 watt or more. Lead tension around protruding metal surfaces must be avoided.
6. All critical components (shaded on the schematic diagram and parts lists) such as: fuses, flameproof resistors, capacitors, etc., must be replaced with exact Zenith types. Do not use replacement components other than those specified or make unrecommended circuit modifications.
7. After re-assembly of the terminal always perform an AC leakage test on all exposed metallic parts of the cabinet and screws to be sure the terminal is safe to operate without danger of electrical shock. **DO NOT USE A LINE ISOLATION TRANSFORMER DURING THIS TEST.** Use an AC voltmeter having 5000 ohms per volt or more sensitivity in the following manner: Connect a 1500 ohm 10 watt resistor (63-10401-76), paralleled by a 0.15 mfd., 150V AC type capacitor (22-4384) between a known good earth ground (water pipe, conduit, etc.) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination 1500 ohm resistor and 0.15 mfd. capacitor. Reverse the AC plug and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 0.75 volts RMS. This corresponds to 0.5 milliamp AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



SUBJECT: IMPLOSION PROTECTION

1. All Zenith picture tubes are equipped with an integral implosion protection system, but care should be taken to avoid damage during installation. Avoid scratching the tube.
2. Use only Zenith replacement tubes.

SUBJECT: X-RADIATION

1. Be sure procedures and instructions to all service personnel cover the subject of X-radiation. The only potential source of X-rays is the picture tube. However, this tube does not emit X-rays when the HV is at the factory-specified level. It is only when the HV is excessive that X-radiation can be generated. The basic precaution which must be exercised is to keep the HV at the factory-recommended level. Refer to the X-ray Precaution Label which is located inside each terminal for the correct high voltage. The proper value is also given in the schematic diagram. Operation at higher voltages may cause a failure of the picture tube or high voltage supply and, also, under certain circumstances, may produce radiation in excess of desirable levels.
2. Only Zenith-specified CRT anode connectors must be used.
3. It is essential that the serviceman has available at all times an accurate high voltage meter. The calibration of this meter should be checked periodically against a reference standard.
4. When the high voltage circuitry is operating properly there is no possibility of an X-radiation problem. Every time a chassis is serviced, the brightness should be run up and down while monitoring the high voltage with a meter to be certain that the high voltage does not exceed the specified value and that it is regulating correctly. We suggest that you and your service organization review test procedures so that voltage regulation is always checked as a standard servicing procedure, and that the reason for this prudent routine be clearly understood by everyone.
5. When trouble shooting and making test measurements in a terminal with a problem of excessive high voltage, do not operate the chassis longer than is necessary to locate the cause of excessive voltage.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.

CAUTION

**NO WORK SHOULD BE ATTEMPTED ON
ANY EXPOSED MONITOR CHASSIS BY
ANYONE NOT FAMILIAR WITH SERVICING
PROCEDURES AND PRECAUTIONS.**

GENERAL INFORMATION

This service manual introduces the Zenith D12 series of Video Displays. The series includes three basic forms: the D12-PF which is complete with power supply and frame, the D12-NF without power supply, the D12-NK in kit form which comes without frame or power supply.

The D12 series incorporate precision CRT's which provide uniformity of display and controlled spot size and geometry. The display may be operated from a standard 15 volt D.C. supply (or optional 12 V.D.C.) or from 120 volts A.C.

Input and output connections for the displays are made through a 10 pin edge connector on the main circuit board. Provision has been made for an optional remote brightness control. Schematic reference numbers are printed on

the circuit board to aid in the location and identification of components for servicing.

Vertical and horizontal linearity is maintained within specifications without the use of linearity controls or adjustable devices. Excellent vertical linearity is assured by the extensive use of current feedback and horizontal linearity is achieved with a fixed saturable reactor.

Vertical and horizontal deflection systems sustain scan even in the absence or interruption of synchronizing signals. Vertical and horizontal synchronization is automatic and stable throughout the entire specified operating frequency range.

SPECIFICATIONS

CATHODE RAY TUBE

12" diagonal measure, 90° deflection, 12.5KV nominal high voltage at 50 μ A. beam current. Available with bonded anti-reflective face plate option. P4 phosphor is standard and other EIA phosphors are available.

NOMINAL DISPLAY AREA

51 sq. in. defined by a rectangle 8 1/2" \times 6" centered on the CRT. (Other display dimensions optional.)

INPUT SIGNALS (TTL LEVEL)

HORIZONTAL

4 to 40 μ sec. duration (positive going standard).

VERTICAL

50 to 2500 μ sec. duration (negative going standard).

VIDEO

1.0V to 2.5V P-P (internal or customer supplied 500 Ω contrast control for higher input levels).

Positive polarity for white characters. (Other polarities are available for horizontal and vertical sync.)

POWER SUPPLY

120V \pm 10% or 240V \pm 10%
(customer strappable) 47 to 63 Hz., or
15V DC at 800 ma. max., or
12V DC at 1100 ma. max.

BRIGHTNESS CONTROL

Internal or Customer supplied 100 K Ω potentiometer (accessible at pins 2, 3 and 4 of edge connector).

INTERCONNECT TO CUSTOMER SYSTEM

Via standard 10-pin edge connector.

VIKING #25V10S/1-2
AMP #225-21031-101
CINCH #250-10-30-170

RESOLUTION

900 vertical lines minimum at center of display and 700 vertical lines at the corners. Pulse rise time less than 20 nanoseconds, for 30V rise at CRT. Bandwidth is within 3db from 10 Hz. to 18 MHz.

GEOMETRY

NOTE: Measurements made with an input of 1.0-2.5V P-P and with the display adjusted to 6" high \times 8 1/2" wide.

VERTICAL

a. Height of display at left side shall be within \pm 2.0 percent of height at right side.

b. Top and bottom pincushion or barrel shall be within \pm 1.25% of the average height.

HORIZONTAL

a. Width of display at top shall be within \pm 2.5% of the width at bottom.
b. Side pincushion or barrel shall be within \pm 1.0% of the average width.

LINEARITY

No character shall vary in width or height by more than \pm 10% of the average width or height of all the characters in a row or column respectively. No specific character shall vary in width or height more than \pm 10% of an adjacent character.

SYNCHRONIZATION

HORIZONTAL

15.75 \pm 0.5KHz.
18.60 \pm 0.5KHz. (Optional)

Horizontal Blanking

9.0 μ sec. min.

Horizontal Phasing Control

11.0 μ sec. nominal range

VERTICAL

47 to 63 Hz.

VERTICAL RETRACE TIME

850 μ sec. max.

STORAGE

55° C. max. with bonded anti-reflective faceplate.
65° C. max. for plain faced CRT's.

ENVIRONMENT

Operating temperature

55° max. (free air temperature of display electronics).

Altitude

40,000 ft. + storage & shipment.
10,000 ft. max. operating.

WEIGHT

11.5 lbs. max. without optional power supply.
13.5 lbs. max. with optional power supply.
9.0 lbs. max. without frame.

THEORY OF OPERATION

POWER SUPPLY

Power Transformer TX201 is designed for use with 120V or 240V A.C. source. The secondary provides power to bridge rectifier (CR501, CR502, CR503 and CR504). The positive output of the bridge rectifier (junction of CR503 and CR504), forms the raw B+ supply ($\sim 20\text{VDC}$).

Voltage regulation is accomplished in the negative leg of the power supply through a feedback network consisting of transistors QX501 and QX502 and their associated circuitry. The emitter voltage of QX501 is maintained by diodes CR505, CR506 and CR507. The base voltage is provided by potentiometer RX506.

If B+ increases, diodes CR505, CR506 and CR507 will draw more current to maintain the emitter voltage of QX501. Additionally, the voltage developed across RX506 will increase, resulting in a higher positive voltage at the base of QX501 which will result in less conduction. This reduces the base current of QX502 since QX501 provides the emitter/base current path for QX502. When QX502 conducts less, the voltage drop across Q502 is increased thus lowering B+.

If B+ decreases, diodes CR505, CR506 and CR507 will reduce conduction to maintain the emitter voltage of QX501. Additionally, the base voltage provided by RX506 will decrease. Less voltage on the base of QX501 will cause it to increase conduction, resulting in a greater emitter/base current flow in QX502. With this condition the voltage drop for Q502 is less and B+ is increased.

HORIZONTAL

The low-level horizontal section, which consists of transistors Q101 and Q102 (and associated circuitry), functions as a variable time delay monostable multivibrator. The input trigger for this circuit is provided by the horizontal drive pulse. The pulse is injected into the base or emitter (for either positive or negative pulse respectively) of Q101 through injection network C101, C111, R101, R110 and CR101. By varying the recovery time of the multivibrator, potentiometer R104 adjusts video information position (with respect to raster scan). Output of the monostable multivibrator, derived at the collector of Q102, is injected through a coupling network consisting of C110 and CR103. The resulting "Lock" signal is rereceived by one side of a precision astable multivibrator at the

emitter of Q103. The astable multivibrator circuit is completed through Q104 and associated circuitry. This circuit will act as a free running oscillator until the "Lock" signal is received from the previous stage. Once locked, an output pulse is formed at the emitter of Q104 which is then D.C. coupled to the base of the horizontal driver transistor, Q105.

Remainder of the horizontal circuit is straightforward. Features to be noted are: Width and Linearity Coils LX102 and LX101 in series with the yoke (TX202). Linearity is fixed and an adjustable coil is provided for width. The linearity coil has a magnetically biased core which makes the inductance of the coil dependent upon its current. Pincushion and geometric corrections are made at the factory by the addition of rubber magnets around the plastic ring of the yoke. D.C. operation of 12 volts is accomplished by the (optional) addition of a boost circuit at the horizontal sweep transformer.

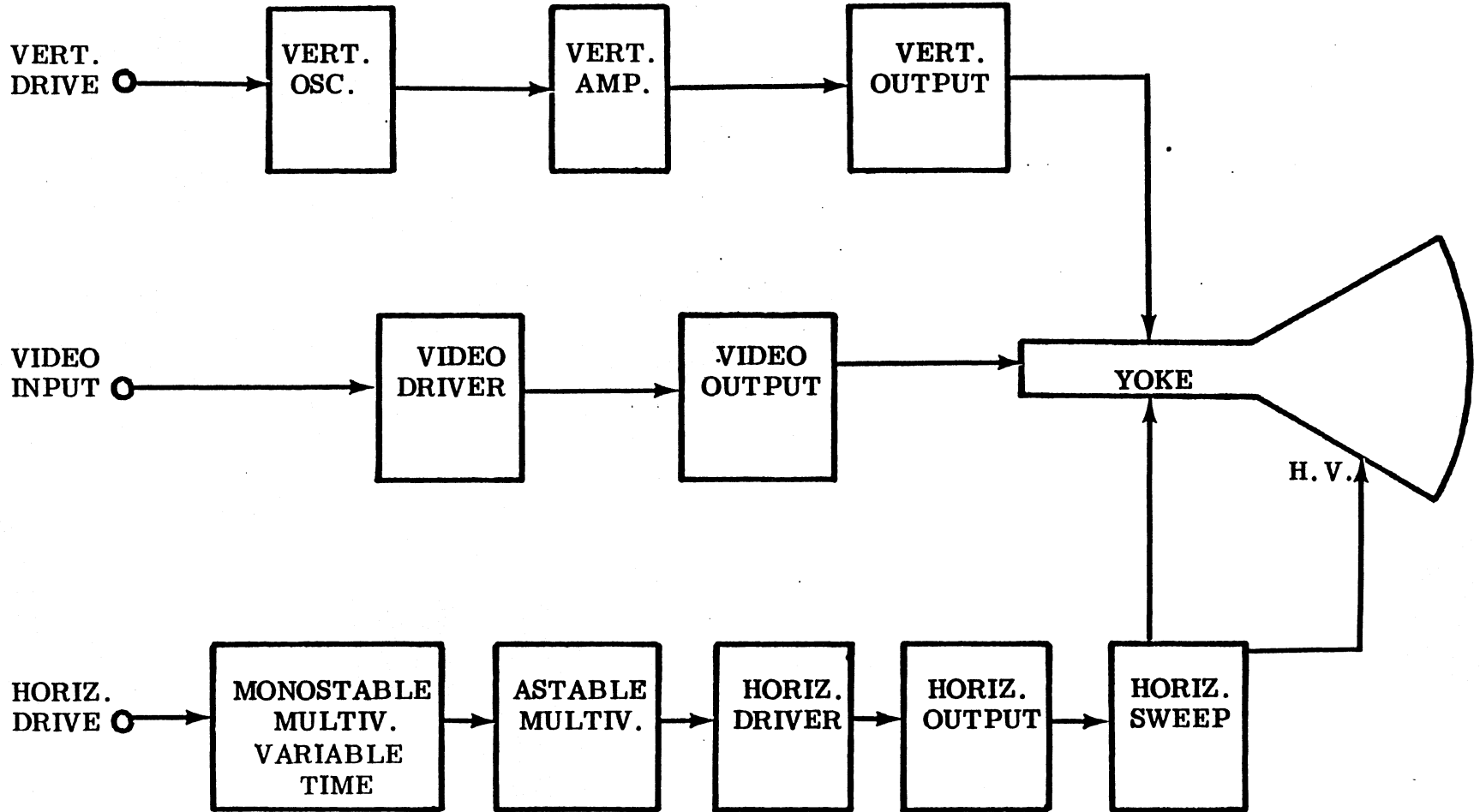
VERTICAL

The vertical circuit includes an oscillator consisting of transistors Q301 and Q302 and associated circuitry. Amplification is provided by transistors Q303 and Q304 with the emitter of Q304 feeding the base of the vertical driver Q305. The vertical output transistors, Q306 and Q307 are wired in the standard push-pull configuration. Transistor Q308 doubles B+ during retrace, maintaining less than 800 μ sec. of retrace time.

VIDEO

The video amplifier circuit consists of transistors Q401 and Q402 and associated circuitry. The circuit comprises a cascode amplifier which is triggered by a positive pulse at pin 8 of the edge connector. Upon receiving the input pulse, conduction is initiated and the collector voltage of Q402 is lowered. Amplification of low frequency voltage gain is fixed by the ratio of R407 and R408. Gain is maintained to 18 MHz by the bandwidth enhancing components R406, C403, and L401. Resistors R402 and R403 provide bias for the amplifier.

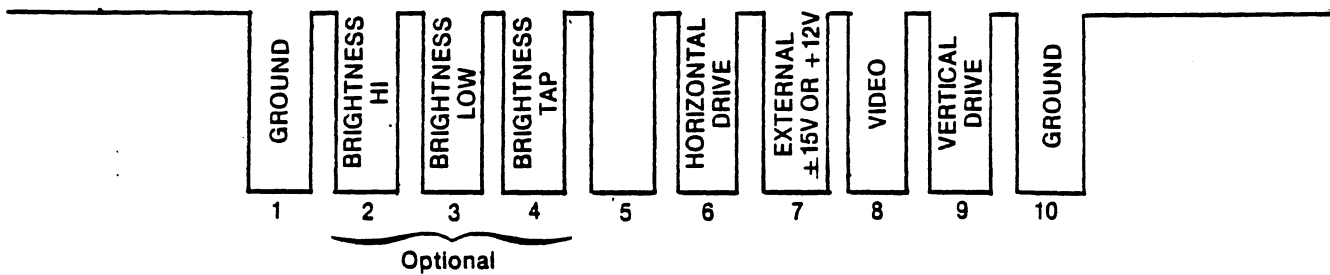
The collector output of Q401 is D.C. coupled to the cathode of the C.R.T. through resistor R201. Raster cut-off is adjusted with the brightness control R114 which is connected to G1 of the C.R.T.



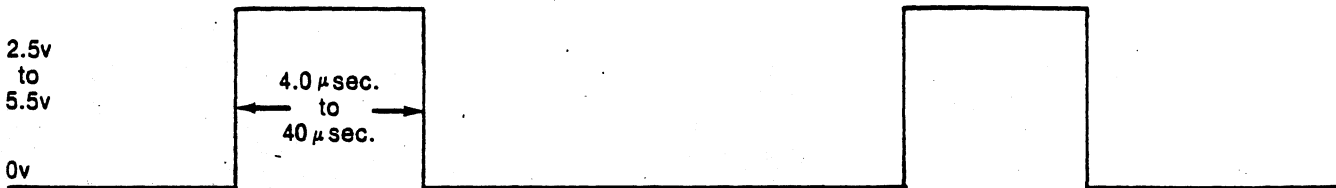
ADJUSTMENT PROCEDURES FOR D12 VIDEO DISPLAY

- External power is applied to the monitor through an AC line cord or a 4 pin molex connector. The unit is wired for 120 VAC 50/60 Hz operation. (240 VAC 50/60 Hz optional)
- INPUT SIGNALS:** Input signals are connected to the display board through a 10 pin edge connector.

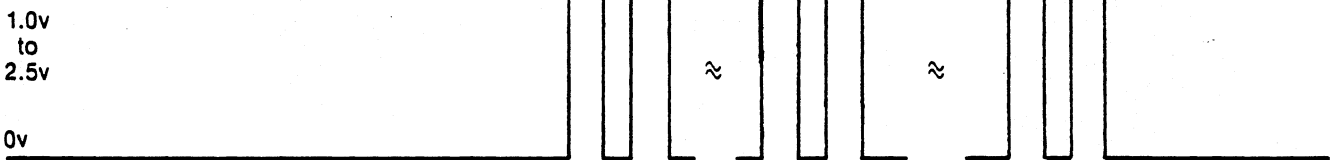
Component Side of Display Board



A. Horizontal drive signal — 15750Hz \pm 500Hz, 18,600Hz \pm 500Hz

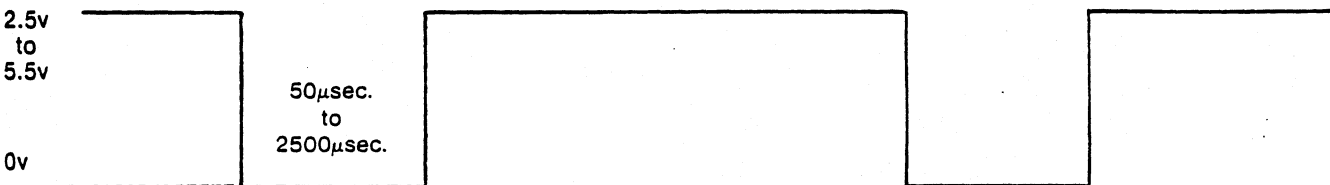


B. Video drive signal

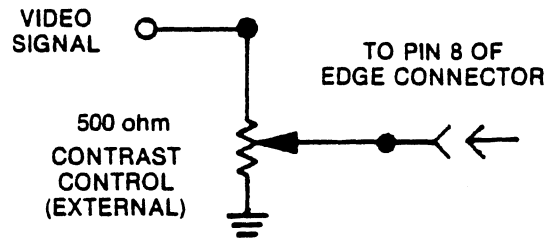


At a horizontal frequency of 15.7KHZ the video drive signal should start 11 microseconds $\pm 5 \mu$ sec. after the leading edge of horizontal sync, and 900 microseconds or greater after the leading edge of vertical sync.

C. Vertical drive signal — 47Hz to 63Hz



Should the video drive level exceed the 2.5 volts specified, an external contrast control must be provided. The video drive signal is connected to the top end of the 500 Ω pot, the bottom end is grounded and the wiper arm connects to the video input of the edge connector as shown.



3. Once power is applied to the display and the input signals connected, adjust the brightness control until the edges of the raster are visible.
4. Depending on the requirements for height and width of the video presentation, the vertical size control and width coil should be adjusted accordingly.
5. The power supply board also has a control to adjust the regulated B+ of the monitor to +15V. Check for proper adjustment.
6. Adjust the phase control to center the video information within the raster. (The contrast control may have to be adjusted to obtain a display of the video information.)
7. Adjust brightness control for visual cutoff of the raster.
8. Adjust external contrast control for desired luminance.
9. Adjust focus control for best possible overall focus.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.

ITEM NUMBER	PART NUMBER	DESCRIPTION	ITEM NUMBER	PART NUMBER	DESCRIPTION
C112	22-2870	0033 MFD CAPACITOR :10% DISC. 500V	R321	63-9921-45	75 OHM RESISTOR :5% FILM 1/4W
C113	22-7440	0047 MFD CAPACITOR :10% DISC. 500V	R322	63-9921-84	3.3K OHM RESISTOR :5% FILM 1/4W
C114	22-7530-07	015 MFD CAPACITOR SPECIAL 400V	R323	63-9921-73	1.1K OHM RESISTOR :5% FILM 1/4W
C116	22-7313	10 MFD CAPACITOR SPECIAL 25V	R324	63-9921-66	560 OHM RESISTOR :5% FILM 1/4W
C117	22-7154-08	100 MFD CAPACITOR :100-10% ELEC. 35V	R325	63-9921-10	2.7 OHM RESISTOR :5% FILM 1/4W
C118	22-3748	001 MFD CAPACITOR :10% DISC. 1KV	R402	63-9921-72	1K OHM RESISTOR :5% FILM 1/4W
C120	22-7712-05	10 MFD CAPACITOR :50-10% ELEC. 100V	R403	63-9921-72	1K OHM RESISTOR :5% FILM 1/4W
C121	22-7153	1 MFD CAPACITOR :100%-10% ELEC 50V	R404	63-9921-40	47 OHM RESISTOR :5% FILM 1/4W
C126	22-7154-09	100 MFD CAPACITOR :100-10% ELEC. 35V	R405	63-9921-90	12K OHM RESISTOR :5% FILM 1/4W
C127	22-7309-02	1 MFD CAPACITOR :±20% ELEC. 25V	R406	63-9921-32	22 OHM RESISTOR :5% FILM 1/4W
CX205	22-7144-09	220 MFD CAPACITOR :100-10% ELEC. 35V	R407	63-10371-70	820 OHM RESISTOR :5% FILM 2W
C301	22-7813-24A	01 MFD CAPACITOR :10% DISC 50V	R408	63-9921-40	47 OHM RESISTOR :5% FILM 1/4W
C302	22-7340	15 MFD CAPACITOR :10% POLYESTER 50V	R409	63-9922-42	820 K OHM RESISTOR :5% FILM 1/4W
C303	22-7152-05	22 MFD CAPACITOR :100%-10% ELEC. 25V	R410	63-9922-44	1 MEG OHM RESISTOR :5% FILM 1/4W
C304	22-7152-09	220 MFD CAPACITOR :100-10% ELEC. 25V	R411	63-9922	15K OHM RESISTOR :5% FILM 1/4W
C305	22-7308-10	10 MFD CAPACITOR ELEC. :10% 25V	R412	63-10013-02	CONTROL 100K OHM BRIGHTNESS
C306	22-7813-02A	150 PFD CAPACITOR :10% DISC. 50V	R413	63-9922	15K OHM RESISTOR :5% FILM 1/4W
C308	22-7152-07	47 MFD CAPACITOR :100-10% ELEC. 25V	R415	63-10012-01	CONTROL 2 MEG OHM FOCUS
C309	22-7152-04	10 MFD CAPACITOR :100-10% ELEC. 25V	R416	63-9922-16	68K OHM RESISTOR :5% FILM 1/4W
C310	22-7814-18A	0033 MFD CAPACITOR :20% DISC. 50V	R418	63-9922	15K OHM RESISTOR :5% FILM 1/4W
C311	22-7813-25A	012 MFD CAPACITOR :10% DISC 50V	L101	20-3808	COIL, RCF LINEARITY
C312	22-7578-07	470 MFD CAPACITOR :10% ELEC. 16V	L102	20-3802-04	COIL, RCF TUNABLE WIDTH
C314	22-7814-20A	0047 MFD CAPACITOR :20% DISC. 50V	L401	20-3807-10C	COIL, RCF 6.8 uH
C401	22-7158-05	22 MFD CAPACITOR :100-10% ELEC. 80V	TX101	95-3136-03	TRANSFORMER HORIZ. DRIVER
C402	22-7153-03	4.7 MFD CAPACITOR :100-10% ELEC. 50V	TX201	95-3457	H. V. SWEEP TRANSFORMER
C403	22-7813-00A	220 PFD CAPACITOR :10% DISC. 50V	TX202	95-3387-02	DEFLECTION YOKE
C404	22-7724	.02 MFD CAPACITOR :00-20% DISC. 500V	CR104	103-295-03A	DIODE
C405	22-3512	.01 MFD CAPACITOR :40-10% DISC. 1KV	CR105	103-284	DIODE
BRX121	63-10550-14	3.3 OHM RESISTOR :5% FAILSAFE 1/4W	CR106	63-267-02-A	DIODE
R122	63-9921-48	82 OHM RESISTOR :5% FILM 1/4W	CR107	103-322-09A	DIODE
BRX123	63-10558-48	100 OHM RESISTOR :5% FAILSAFE 1/4W	CR108	212-76 -02	DIODE
R124	63-9921-88	800 OHM RESISTOR :5% FILM 1/4W	CR111	103-143-04	DIODE
R125			CR201	103-298 -09	DIODE
R126	63-10104-20	100K OHM RESISTOR :10% CARBON COMP. 1/4W	CR301		
R127			CR302		
R128	63-10420-24	1 OHM RESISTOR :5% WIREWOUND 2W	CR303		
R129	63-9921-50	270 OHM RESISTOR :5% 1/4W	CR304	103-142-01	DIODE
R202	63-7718	27 OHM RESISTOR :5% CARBON COMP. 1/2W	CR305	212-74 -02	DIODE
R301	63-9922-27	200 K OHM RESISTOR :5% FILM 1/4W	CR401	103-261-02	DIODE
R302	63-9921-92	8.2K OHM RESISTOR :5% FILM 1/4W	Q105	121-1048	TRANSISTOR HORIZ. DRIVER
R303	63-9922-04	22K OHM RESISTOR :5% FILM 1/4W	Q106	121-1038	TRANSISTOR HORIZ. OUTPUT
R304	63-9921-95	9.1K OHM RESISTOR :5% FILM 1/4W	Q301	121-875	TRANSISTOR VERT. OSC. I
R305	63-9922-10	39K OHM RESISTOR :5% FILM 1/4W	Q302	121-899	TRANSISTOR VERT. OSC. II
R306	63-9921-48	47 OHM RESISTOR :5% FILM 1/4W	Q303	121-899	TRANSISTOR VERT. AMP I
BRX307	63-10559-38	33 OHM RESISTOR :5% FAILSAFE 1/4W	Q304	121-875	TRANSISTOR VERT. AMP. II
R308	63-9922-42	820K OHM RESISTOR :5% FILM 1/4W	Q305	121-872-04	TRANSISTOR VERT. DRIVER
R309	63-10651-13	CONTROL 250K OHM VERT. SIZE 1/4W	Q306	121-1035	TRANSISTOR VERT. OUTPUT I
R310	63-9922-48	1.5 OHM RESISTOR :5% FILM 1/4W	Q307	121-1036	TRANSISTOR VERT. OUTPUT II
R311	63-9922-22	120 K OHM RESISTOR :5% FILM 1/4W	Q308	121-1040	TRANSISTOR VERT. RETRACE CONTROL
R312	63-9922-06	27K OHM RESISTOR :5% FILM 1/4W	Q401	121-1058	TRANSISTOR 121-1034 ALT. VIDEO OUTPUT
R314	63-9921-78	1.8K OHM RESISTOR :5% FILM 1/4W	Q402	121-895	TRANSISTOR VIDEO DRIVER
R315	63-9922	15K OHM RESISTOR :5% FILM 1/4W	VR201	108-648	12" CRT
R317	63-1823	0.2K OHM RESISTOR :5% CARBON COMP. 1/2W			
R318					
BRX315	63-10568-58	220 OHM RESISTOR :5% FAILSAFE 1/2W			
R320	63-9922-04	22K OHM RESISTOR :5% FILM 1/4W			

1 2 3 4

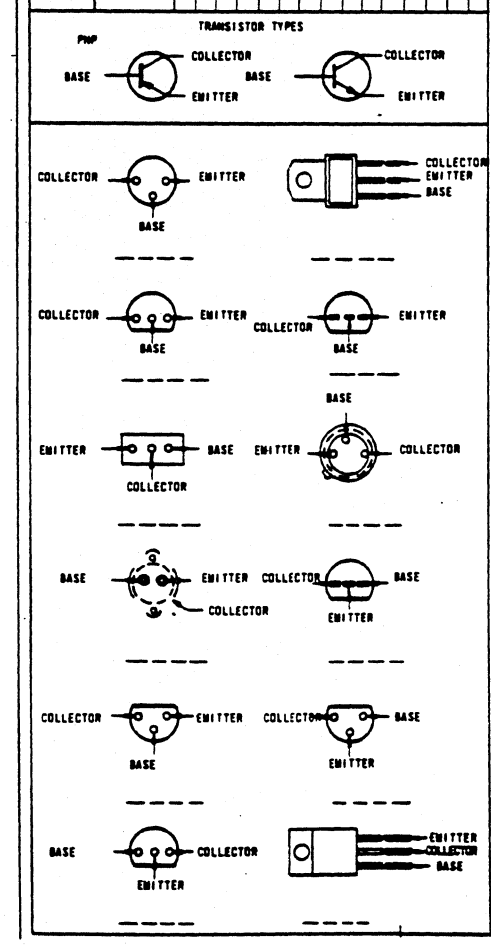
LEGEND FOR
D12 VIDEO DISPLAY 162/19.2KHz HORIZ SCAN FREQ

ZENITH RADIO CORP.
CHICAGO, ILL.

123-5498

BOTTOM VIEWS OF TRANSISTORS

Q NUMBER	PART NUMBER	SKETCHES												
		A	B	C	D	E	F	G	H	I	J	K	L	M
Q105	121-1040	X	X							X	X			
Q106	121-1038													X
Q301	121-875				X								X	
Q302	121-899				X								X	
Q303	121-899				X								X	
Q304	121-875				X								X	
Q305	121-872-04				X	X							X	
Q306	121-1035												X	
Q307	121-1036												X	
Q308	121-1040	X	X		X	X				X	X			
Q401	121-1058	X												
Q402	121-895				X	X								



REVISIONS

DATE: FEB 22, 80

LEGEND FOR
D12 VIDEO DISPLAY 162/19.2KHz HORIZ SCAN FREQ

ZENITH RADIO CORP.
CHICAGO, ILL.

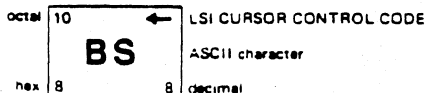
123-5498

APPENDIX E

ASCII CONTROL CODE CHART

BITS B7 B6 B5 B4 B3 B2 B1	0 0 0 0		0 1 0 1		1 0 0 1		1 1 0 1	
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL	20 DLE	40 SP	60 0	100 @	120 P	140 '	160 p
0 0 0 1	1 SOH	21 DC1	41 !	61 1	101 A	121 Q	141 a	161 q
0 0 1 0	2 STX	22 DC2	42 "	62 2	102 B	122 R	142 b	162 r
0 0 1 1	3 ETX	23 DC3	43 #	63 3	103 C	123 S	143 c	163 s
0 1 0 0	4 EOT	24 DC4	44 \$	64 4	104 D	124 T	144 d	164 t
0 1 0 1	5 ENQ	25 NAK	45 %	65 5	105 E	125 U	145 e	165 u
0 1 1 0	6 ACK	26 SYN	46 &	66 6	106 F	126 V	146 f	166 v
0 1 1 1	7 BEL	27 ETB	47 '	67 7	107 G	127 W	147 g	167 w
1 0 0 0	8 BS	28 CAN	48 (68 8	108 H	128 X	148 h	168 x
1 0 0 1	9 HT	29 EM	49)	69 9	109 I	129 Y	149 i	169 y
1 0 1 0	10 LF	30 SUB	50 *	70 :	110 J	130 Z	150 j	170 z
1 0 1 1	11 VT	31 ESC	51 +	71 ;	111 K	131 [151 k	171 {
1 1 0 0	12 FF	32 FS	52 ,	72 <	112 L	132 \ backslash	152 l	172
1 1 0 1	13 CR	33 GS	53 -	73 =	113 M	133]	153 m	173 }
1 1 1 0	14 SO	34 RS	54 .	74 >	114 N	134 ^	154 n	174 ~
1 1 1 1	15 SI	35 US	55 /	75 ?	115 O	135 _	155 o	175 RUBOUT (DEL)

LEGEND



OPERATORS QUICK REFERENCE CHART OF CONTROL AND OPERATORS CODES

CONTROL CODE		HEX CODE	OPERATION
FROM HOST	FROM KEYBOARD		
ETX	CTRL C	03	Secondary channel line turnaround codes for 202 Modem operation (From Host Only)
EOT	CTRL D	04	
ENQ	HERE IS	05	Initiates ID message when Answerback Option is installed
BEL	CTRL G	07	Sounds audible beep in Video Display Unit
BS	CTRL H	08	Backspace
LF	LINE FEED	0A	.Line Feed
VT	CTRL K	0B	Upline
FF	CTRL L	0C	Forward Space
CR	RETURN	0D	Return
SO	CTRL N	0E	With S8 in GT (ON) position, enables gated EXTENSION port and passes CTRL N through the EXTENSION port With S8 in LK (OFF) position, unlocks keyboard (From Host Only)
SI	CTRL O	0F	With S8 in GT (ON) position, disables gated EXTENSION port and passes CTRL O through the EXTENSION port With S8 in LK (OFF) position, locks keyboard
SUB	SHIFT CLEAR	1A	Clears Screen
ESC	ESC =	1B	Initiates load cursor operation
RS	HOME	1E	Homes Cursor

OPERATORS QUICK REFERENCE CHART
OF ABSOLUTE CURSOR POSITIONS

Keys Used: =

ASCII CODES	POSITION		ASCII CODES	POSITION		ASCII CODES	POSITION	
	ROW	COL		ROW	COL		ROW	COL
=	1	1	=		28	=		55
	2	2			29			56
	3	3			30			57
	4	4	> key"/>		31			58
	5	5			32			59
	6	6			33			60
	7	7			34	\ key"/>		61
	8	8			35			62
	9	9			36			63
	10	10			37			64
	11	11			38			65
	12	12			39			66
	13	13			40			67
	14	14			41			68
	15	15			42			69
	16	16			43			70
	17	17			44			71
	18	18			45			72
	19	19			46			73
	20	20			47			74
	21	21			48			75
	22	22			49			76
	23	23			50			77
	24	24			51			78
	25	25			52			79
	26	26			53	=		80
=	27	27	=		54			

INDEX

INDEX

A-B

Absolute Cursor Positioning	1-1
ASCII Characters	1-1,A-1
Auto New Line	1-1

C

Carrier Detect	3-4
Character Format	1-3
Cleaning	2-14
Clear To Send	3-1
Code Turnaround	3-4
Configuration Control	1-8,2-2
Control Characters	1-1
Control Codes	3-4,A-2
Control Logic	1-3

D-E

Data Entry and Overflow	1-8
Display Memory	1-3
Display Monitor	1-3
EOT	2-7,3-4
ETX	2-7,3-4

F-G-H

Full Duplex	2-11,3-1
Gated EXTENSION Port Mode	2-4,3-5
Half Duplex	2-11,3-1

I-J-K

Interfaces:	
EXTENSION Port	2-4
MODEM Port	2-4
Input/Output Channel	1-2
Inspection	2-14
Installation	2-4
Keyboard Operations	3-1,3-3
Keyboard Section	1-2

INDEX (Continued)

L-M-N

Load Cursor Operation	3-4
Numeric Keypad	1-5,1-8

O-P-Q

Options:

Alternate Configuration - Green Phosphor Screen	1-8
Answerback	1-8
Beep Defeat	1-8
Lower Case Characters	1-8
Numeric Keypad	1-8
Output Cable	1-8
Power ON/OFF	2-13
Primary Channel	3-1
Split Baud Rate	1-8
20mA Current Loop on EXTENSION Port	1-8
230VAC	1-8

R-S-T

Refresh Rate	1-1
Remote Load Cursor Operation	3-4
Request To Send	3-1
Safety Requirements	2-1
Secondary Channel	3-4
Site Requirements	2-1
Specifications	1-4

U-V-W-X-Y-Z

Unpacking	2-1
Voltage Selection	2-2
Word Structure	1-1



LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

901 EAST BALL ROAD, ANAHEIM, CALIFORNIA 92805
PHONE: (714) 778-3500 TELEX: 65-5444 TWX: 910-591-1157