# MLSI-DB11-R

## AND MLSI-DB11-RA
## Q-BUS REPEATER ASSEMBLIES

For use with DEC™ LSI-11™ Computers

## INSTRUCTION MANUAL

MDB SYSTEMS, INC.

# MLSI-DB11-R
## AND MLSI-DB11-RA
## Q-BUS REPEATER ASSEMBLIES

For use with DEC™ LSI-11™ Computers

## INSTRUCTION MANUAL

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Price: $10.00

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## Scope of Manual

This technical manual provides instruction and information for installing and utilizing the MDB Systems' MLSI-DB11-R and MLSI-DB11-RA Q-bus Repeater Assemblies. These Bus Repeater Assemblies are to be used with Digital Equipment Corporation (DEC) LSI-11 Q-bus computers.

Since the MLSI-DB11-R and MLSI-DB11-RA differ only in the length of their interconnection cables and installation, and have identical operating characteristics, the general term "Bus Repeater" will be used throughout this instruction manual to represent both bus repeater assemblies. Specific differences between the MLSI-DB11-R and MLSI-DB11-RA will be indicated where appropriate.

## Product Description

The Bus Repeater Assembly consists of two dual-size modules (MLSI-DB11 and MLSI-DBT) and two 10-foot (3.05m) flat ribbon interconnection cables. When the MLSI-DB11-RA is used, the interconnection cables are only 1-foot (30.48 cm) long.

When installed (MLSI-DB11 in main Q-bus and MLSI-DBT in expansion bus), the Repeater receives and re-drives (rejuvinates) all Q-bus signals. Therefore, the Bus Repeater allows the Q-bus to be extended beyond twenty (20) DC bus loads.

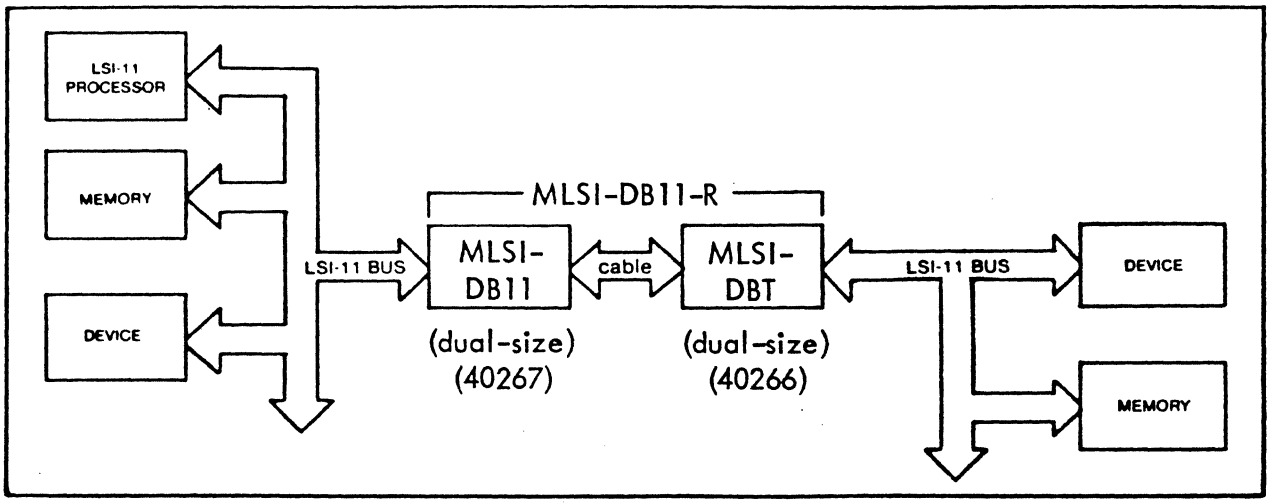
The Bus Repeater appears to the primary CPU segment of the Q-bus as one DC bus load, and drives a new bus segment (expansion bus) capable of handling an additional set of DC bus loads, essentially doubling the total number of module loads that one processor can accommodate. The Repeater is counted as one DC load on each Q-bus segment, and drives an additional nineteen (19) loads on the repeated bus. (The system may then accommodate 40 total DC loads, including the Bus Repeater modules.)

The Bus Repeater is completely compatible with the DEC LSI-11 family and repeats the appropriate Q-bus signals to support 22-bit addressing, 4-level priority interrupt, DMA transfers, and parity, as well as all other Q-bus signals. (Refer to Table 1 for a complete listing of Q-bus signals.)

The Bus Repeater also provides complete 120 ohm termination in the primary CPU Q-bus, and matching 120 ohm impedance for the beginning of the repeated bus in the expansion backplane. Termination for the repeated bus must be accomplished by means of an appropriate terminator module (i.e., MLSI-TEV-003, or equivalent).

Figure 1 on the following page is a block diagram showing the position of the Bus Repeater in a typical repeated bus system.

Figure 1
System Block Diagram




## Physical Description/Specification Summary

This section provides a brief description of the mechanical and electrical specifications of the MDB Bus Repeater Assembly.

1. Mechanical

a. Logic Modules: One (1) dual-size MLSI-DB11 module (p/n 45040267).

One (1) dual-size MLSI-DBT module (p/n 45040266).

b. Interconnection Cables: One (1) 10-foot (3.05m), 60-pin, flat ribbon cable (GPRCSR-60-D, p/n 500-46856-XXX).

One (1) 10-foot, 26-pin, flat ribbon cable (GPRCSR-26-D, p/n 50046852-XXX).

Note: When the MLSI-DB11-RA is used, the interconnection cables are only 1-foot (30.48 cm) long. (Model and part numbers are identical to those listed above.)

c. LED Indicators: One (1) red LED indicator is mounted on the edge of the MLSI-DB11 module. When lighted, indicates Repeater active.

d. Jumpers: Jumper plugs are factory-installed on the MLSI-DB11 module, as follows:

1 F-H and 2 F-H (location 3E).
3 F-H and 4 F-H (location 4E).

No jumper modifications are necessary for operation.

## 2. Electrical

a. Power Required: +5V DC at 3.0 amperes, maximum, from the backplane.

b. Bus Loading: The MLSI-DB11 module places one DC bus load on the primary CPU Q-bus, and the MLSI-DBT module places one DC load on the repeated segment of the Q-bus.

The Repeater drives an additional nineteen (19) DC loads on the repeated bus for system expansion.

c. Cable Loading: The CPU bus segment ends where the MLSI-DB11 module is installed; the repeated bus segment begins at the MLSI-DB11 and appears as 10 feet of cable length.

d. Bus Compatibility: LSI-11/23 bus with 22-bit addressing and 4-level interrupt capability. If any of these signals are dedicated to special wiring on an LSI-11/2, etc., they must be disconnected from the MLSI-DB11 module.

## Installation

To install the Bus Repeater, perform the following steps:

1. Install the MLSI-DB11 module in the last slot of the primary CPU backplane assembly (i.e., slot 8 A-B if an MDB MLSI-BA11-600 Series Chassis is used.)

2. Install the MLSI-DBT module in the first slot of the expansion backplane assembly (i.e., slot 1 A-B if an MDB MLSI-BA11-700 Series Expansion Chassis is used).

3. Connect the 10-foot, 60-pin, flat ribbon interconnection cable between connector P1 of the MLSI-DB11 and connector P1 of the MLSI-DBT modules.

4. Connect the 10-foot, 26-pin, flat ribbon interconnection cable between connector P2 of the MLSI-DB11 and connector P2 of the MLSI-DBT modules.

Note: The 10-foot Repeater interconnection cables must be considered part of the repeated bus length. The drivers and termination are provided on the MLSI-DB11 module, while the MLSI-DBT is primarily a cable connect module.

When using the MLSI-DB11-RA Bus Repeater Assembly, installation is slightly different than that for the MLSI-DB11-R, as explained below.

The purpose and features of the MLSI-DB11-RA are identical to those of the MLSI-DB11-R; however, whereas the MLSI-DB11-R was designed to be used to interconnect two separate backplanes, the MLSI-DB11-RA was designed specifically for use in an MDB MLSI-BA11-1000 Series Chassis Assembly.

The MLSI-BA11-1000 contains two backplanes, joined together, in a single chassis assembly. The MLSI-BA11-1000 provides sixteen (16) quad-size (32 dual) slots. Since the two backplanes contained in the chassis are connected together, a 1-foot cable is all that is needed to pass the Q-bus signals, through the MLSI-DB11-RA, from the top segment of the chassis backplane to the bottom segment. Thus, the shorter cable is supplied with the MLSI-DB11-RA. (The MLSI-DB11-RA Bus Repeater should be used in the MLSI-BA11-1000 if the total number of DC loads in the system exceeds twenty (20) loads.)

To install the MLSI-DB11-RA Bus Repeater Assembly, perform the following steps:

1. Install the MLSI-DB11 module in slot 8 A-B of the MLSI-BA11-1000 chassis backplane assembly.

2. Install the MLSI-DBT module in slot 9 A-B of the MLSI-BA11-1000 chassis backplane assembly.

3. Connect the 1-foot, 60-pin, cable between connector P1 of the MLSI-DB11 and connector P1 of the MLSI-DBT modules.

4. Connect the 1-foot, 26-pin, cable between connector P2 of the MLSI-DB11 and connector P2 of the MLSI-DBT modules.

## General Operation

The Bus Repeater receives and re-drives all Q-bus signals. Most of the signals are bidirectional; that is, they can be driven by the LSI-11 processor and received by a device and, in turn, be re-driven by the device and received by the processor. In fact, the signal direction may change several times for each bus cycle, as shown in Figure 2 on the following page.

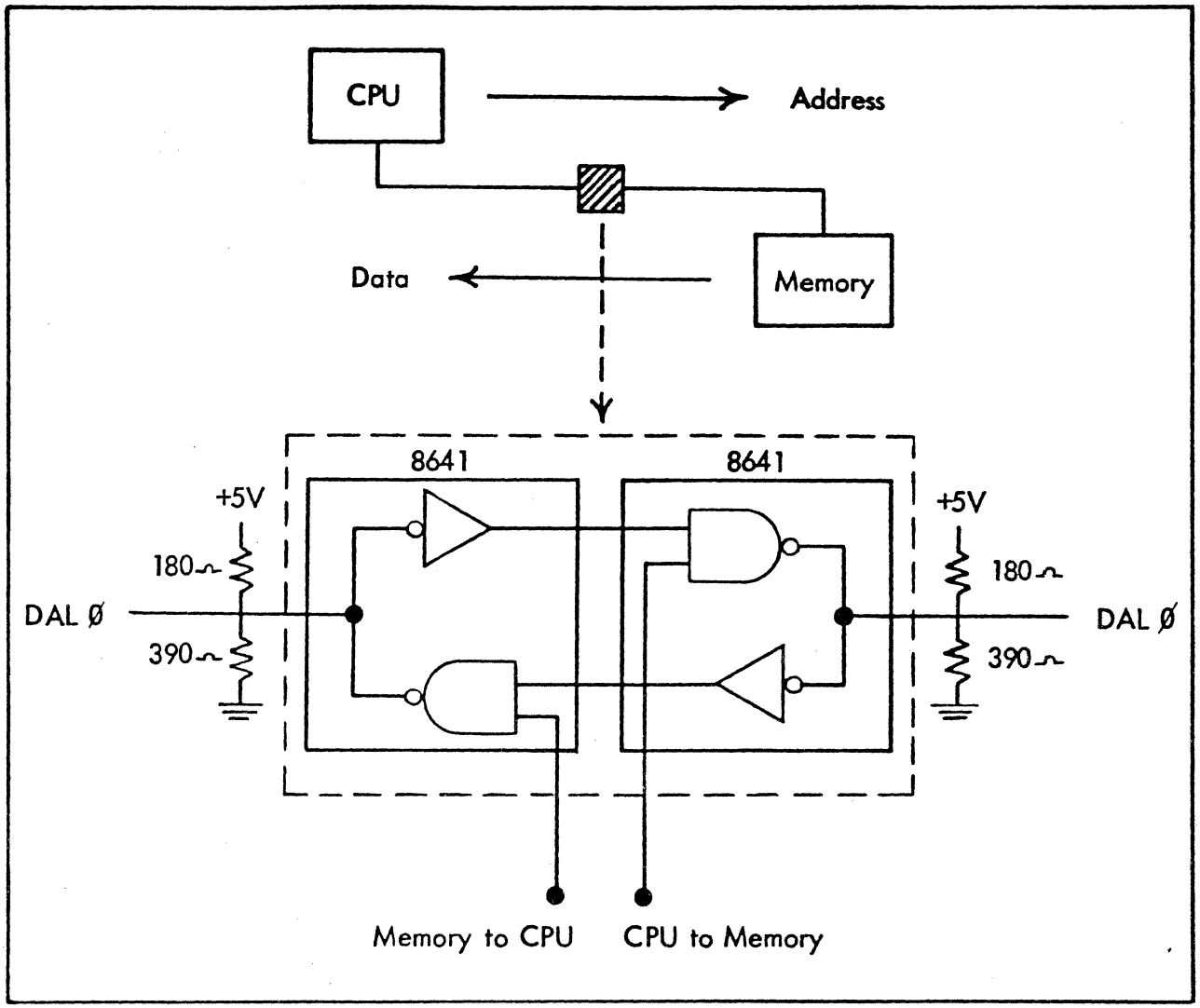
When the processor reads data from a location in memory:

1. The processor drives the DAL signal lines to specify the memory address (CPU to Memory).

2. The memory device receives the DAL signal lines and responds to its address and the proper control signals by driving the DAL signal lines with the data contents of the addressed memory location (Memory to CPU).

3. The processor receives the DAL signal lines as data.

Figure 2
Block Diagram: Bus Repeater Assembly, General Operation



When the Bus Repeater is inserted into the system between the processor and memory (as shown in Figure 2 on the preceding page), it will:

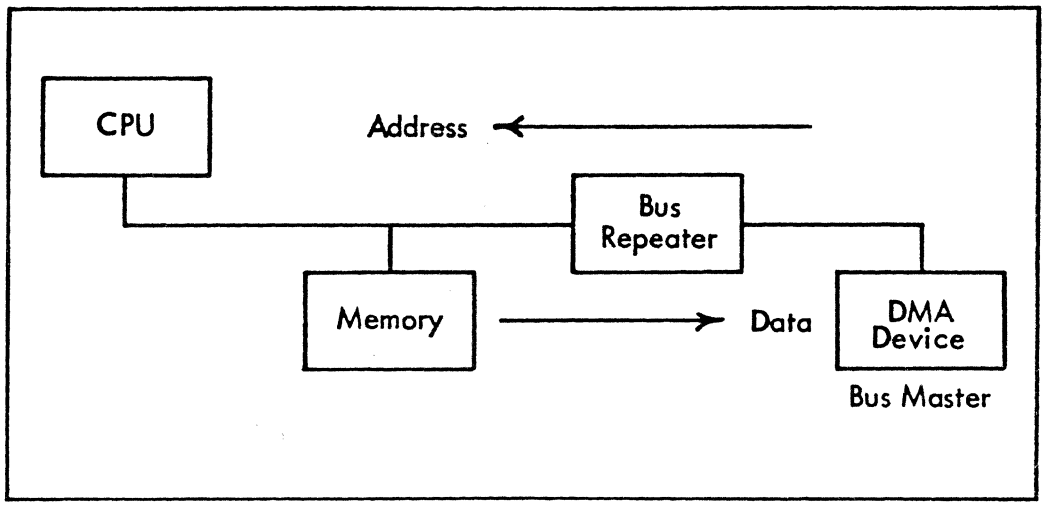
1. Drive the DAL signal lines first in one direction (CPU to Memory), and then in the opposite direction (Memory to CPU).

2. Monitor bus control signals to determine what signals to drive in which direction, during which phase of each cycle.

3. Drive specific control signals associated with each bus cycle in the proper direction (i.e., SYNC, DIN, DOUT, RPLY, etc.).

In addition to memory read cycles, the Q-bus also performs memory write cycles, read-modify-write cycles, interrupt cycles, DMA bus mastership arbitration cycles, and DMA transfer cycles. Each of these cycles has its own unique set of requirements to enable signal flow. For example, when a DMA device is bus master on the repeated bus, the direction of data flow is opposite that of the cycle shown in Figure 2. The illustration below is a block diagram of data flow when a DMA device on the repeated segment of the bus holds bus master status.

Figure 3
Block Diagram: DMA Bus Master on Repeated Bus




The Bus Repeater switches signal flow direction for various signals at precise phase times during cycles to ensure proper timing relationships between Q-bus signals. This is accomplished by an array of logic elements in the Repeater which monitors bus control signals and issues gating commands to several independent receiver and driver structures (see Figure 2).

In this way, the address, data, bus control, interrupt, and DMA control signals are handled so that the CPU is "unaware" that any device has been placed between the

CPU and other devices or memory in the system. In other words, the Bus Repeater is transparent to the hardware and the system software.

Note: Since the Repeater is software transparent, it is non-programmable. Proper initial operation may be verified by running a diagnostic on memory or an I/O device on the main CPU Q-bus, and then moving the same device to the repeated bus and repeating the diagnostic.

## Repeated Q-bus Signals

Table 1 on the following pages lists and defines all Q-bus signals that are repeated by the Bus Repeater Assembly, and provides pin assignments at the backplane for each bus signal.

Table 1
Functional Description of Q-bus Signals

Note: An asterisk (*) denotes a Q-bus pin that is not used on this module assembly.

| Bus Pin | Mnemonic | Description |
|---|---|---|
| AA1 (CA1) | BIRQ5L | Priority Level 5 interrupt request. |
| AB1 (CB1) | BIRQ6L | Priority Level 6 interrupt request. |
| AC1 (CC1) | BDAL16L | Extended address bit 16. |
| AD1 (CD1) | BDAL17L | Extended address bit 17. |
| *AE1 (CE1) | SSPARE | Spare pin. Not assigned. This pin is available for user connection. |
| *AF1 (CF1) | SRUNL | Run light signal. |
| *AH1 (CH1) | SRUNL | Run light signal. |
| AJ1 (CJ1) | GND | Signal ground. |
| *AK1 (CK1) | MSPAREA | Maintenance spare. Normally connected to bus pin AL1 (CL1) on the backplane. |
| *AL1 (CL1) | MSPAREA | Maintenance spare. Normally connected to bus pin AK1 (CK1) on the backplane. |
| AM1 (CM1) | GND | Signal ground. |
| AN1 (CN1) | BDMRL | Direct Memory Access (DMA) Request. Asserted by a device to request control of the bus (bus master). If the processor is not the bus master, and it is not asserting BSYNCL, it grants bus master status to the requesting device by asserting BDMGOL. The requesting device responds by negating BDMRL and asserting BSACKL. |
| AP1 (CP1) | BHALTL | Processor Halt. A device will cause the processor to halt normal program execution by asserting BHALTL. |

Table 1
Functional Description of Q-bus Signals

| Bus Pin | Mnemonic | Description |
|---|---|---|
| AR1 (CR1) | BREFL | Memory Refresh. When BREFL is asserted, the processor will perform as memory refresh that forces all dynamic memory devices to be activated for each BSYNCL/BDINL bus transaction. |
| *AS1 (CS1) | +12B | +12V battery power. |
| AT1 (CT1) | GND | Signal ground. |
| *AU1 (CU1) | PSPARE | Power Spare. Not assigned. This pin is not recommended for use. |
| *AV1 (CV1) | +5B | +5V battery power. |
| AA2 (CA2) | +5V | +5V DC power. |
| *AB2 (CB2) | -12V | -12V DC power. |
| AC2 (CC2) | GND | Signal ground. |
| *AD2 (CD2) | +12V | +12V DC power. |
| AE2 (CE2) | BDOUTL | Data Output. Implies that valid data is available on lines BDAL0L through BDAL15L and, with reference to the bus master device, that an output transfer is in process. The slave device that responds to the BDOUTL signal must assert BRPLYL to complete the data transfer. |
| AF2 (CF2) | BRPLYL | Reply. Asserted in response to BDINL or BDOUTL. The signal indicates that input data is available on the BDAL bus, or that output data has been accepted from the bus. |
| AH2 (CH2) | BDINL | Data Input. When BSYNCL is asserted, BDINL indicates an input transfer from the active bus master. When BSYNCL is not asserted, it implies that an interrupt operation is in process. |
| AJ2 (CJ2) | BSYNCL | Synchronize. Asserted by the bus master device when it has placed an address on lines BDAL0L through BDAL21L. |

Table 1
Functional Description of Q-bus Signals

| Bus Pin | Mnemonic | Description |
|---|---|---|
| AK2 (CK2) | BWTBTL | Write/Byte. Controls the bus cycle in either of two ways, as follows:<br>1. Asserted with leading edge of BSYNCL to indicate that an output sequence will follow (DATO or DATOB).<br>2. Asserted, while BDOUTL is asserted, for byte addressing in a DATOB cycle. |
| AL2 (CL2) | BIRQ4L | Priority Level 4 interrupt request. |
| AM2 (CM2) | BIAKIL | Interrupt Acknowledge. Asserted by the processor in response to BIRQL. Causes the device to put an interrupt vector address on the bus. |
| AN2 (CN2) | BIAKOL | Interrupt Acknowledge Out. Normally asserted to the device having the next-lower priority on the interrupt chain, and appears at BIAKIL input to that device. If the module stores an interrupt request, BIAKOL is negated at the next device. |
| AP2 (CP2) | BBS7L | Bank 7 Select. Indicates that the address on the bus is for the upper 4K bank. When BSYNCL is asserted, BBS7L will remain active until the addressing of the bus cycle is completed. |
| AR2 (CR2) | BDMGIL | DMA Bus Grant Input. |
| AS2 (CS2) | BDMGOL | DMA Bus Grant Output. This processor-generated signal is daisy-chained through all DMA devices on the bus. When asserted, BDGMIL grants bus master status to the DMA device requesting the bus that has the highest priority. If a higher-priority DMA device has no active bus request, BDMGOL passes from that device to the BDMGIL input of the next DMA device. If the higher-priority device has an active bus request, that device inhibits its BDMGOL output. A DMA device requests the bus by asserting BDMRL. |
| AT2 (CT2) | BINITL | Initialize. Generated by the processor during a power-up or reset operation. Clears all devices on the I/O bus. |

Table 1
Functional Description of Q-bus Signals

| Bus Pin | Mnemonic | Description |
|---|---|---|
| AU2 (CU2) | BDAL0L | Bit 0. One of the data/address bus lines used to transfer all address and data information. Bidirectional. |
| AV2 (CV2) | BDAL1L | Bit 1. Data/Address bit. |
| BA1 (DA1) | BDCOKH | DC Power OK. Asserted when the DC voltage level is suitable for reliable system operation. |
| BB1 (DB1) | BPOKH | AC Power OK. Asserted when primary power is within limits assuring reliable system operation. |
| BC1 (DC1) | BDAL18L | Bit 18. One of the extended address bus lines used to transfer address information. |
| BD1 (DD1) | BDAL19L | Extended address bit 19. |
| BE1 (DE1) | BDAL20L | Extended address bit 20. |
| BF1 (DF1) | BDAL21L | Extended address bit 21. |
| *BH1 (DH1) | SSPARE | Special spare. Not assigned. This pin is available for user connection. |
| BJ1 (DJ1) | GND | Signal ground. |
| *BK1 (DK1) | MSPAREB | Maintenance spare. Normally connected to bus pin BL1 (DL1) on the backplane. |
| *BL1 (DL1) | MSPAREB | Maintenance spare. Normally connected to bus pin BK1 (DK1) on the backplane. |
| BM1 (DM1) | GND | Signal ground. |
| BN1 (DN1) | BSACKL | Bus Grant Acknowledge. Asserted by a DMA device in response to the processor's BDMGOL signal, indicating that the device is now the bus master. |
| BP1 (DP1) | BIRQ7L | Priority Level 7 interrupt request. |
| BR1 (DR1) | BEVNTL | External Event Interrupt Request. Using BEVNTL, Line Time Clock interrupts occur every 16-2/3 msec for a 60 Hz line frequency, and every 20 msec for a 50 Hz line frequency. |

Table 1
Functional Description of Q-bus Signals

| Bus Pin | Mnemonic | Description |
|---|---|---|
| *BS1 (DS1) | +12B | +12V battery power. |
| BT1 (DT1) | GND | Signal ground. |
| *BU1 (DU1) | PSPARE | Power spare. Not assigned. This pin is not recommended for use. |
| *BV1 (DV1) | +5V | +5V DC power. |
| BA2 (DA2) | +5V | +5V DC power. |
| *BB2 (DB2) | -12V | -12V DC power. |
| BC2 (DC2) | GND | Signal ground. |
| *BD2 (DD2) | +12V | +12V DC power. |
| BE2 (DE2) | BDAL2L | Bit 2. One of the data/address bus lines used to transfer all address and data information. Bidirectional. |
| BF2 (DF2) | BDAL3L | Bit 3. Data/Address bit. |
| BH2 (DH2) | BDAL4L | Bit 4. Data/Address bit. |
| BJ2 (DJ2) | BDAL5L | Bit 5. Data/Address bit. |
| BK2 (DK2) | BDAL6L | Bit 6. Data/Address bit. |
| BL2 (DL2) | BDAL7L | Bit 7. Data/Address bit. |
| BM2 (DM2) | BDAL8L | Bit 8. Data/Address bit. |
| BN2 (DN2) | BDAL9L | Bit 9. Data/Address bit. |
| BP2 (DP2) | BDAL10L | Bit 10. Data/Address bit. |
| BR2 (DR2) | BDAL11L | Bit 11. Data/Address bit. |
| BS2 (DS2) | BDAL12L | Bit 12. Data/Address bit. |
| BT2 (DT2) | BDAL13L | Bit 13. Data/Address bit. |
| BU2 (DU2) | BDAL14L | Bit 14. Data/Address bit. |
| BV2 (DV2) | BDAL15L | Bit 15. Data/Address bit. |

## Repair

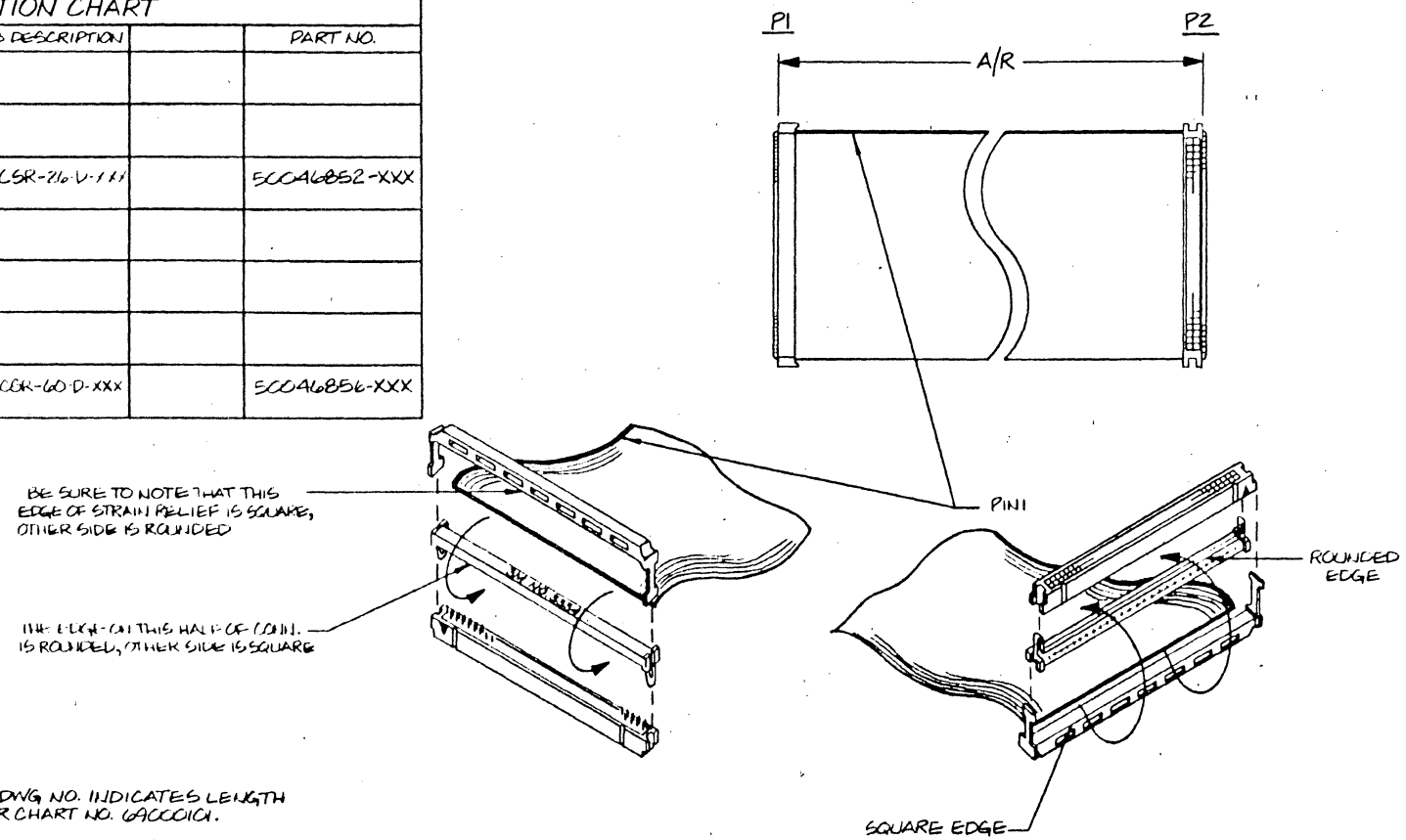
In the event of apparent Bus Repeater malfunction, refer to the assembly drawings and logic diagrams contained in the rear of this manual. Check to be sure that all connectors are secured and that both Repeater modules are seated tightly in their respective backplane assemblies.

Repair the Bus Repeater using appropriate skills, techniques, and materials. If you wish MDB Systems to repair the assembly, contact the Customer Service Department and request a Return Material Authorization (RMA) number. Once return authorization is obtained, pack the Bus Repeater Assembly carefully, along with your best evaluation of trouble symptoms, and ship it, prepaid, to MDB Systems, Inc.

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPROVED |
| | A | ECO NO. 2042 RELEASE TO PRODUCTION | 7-9-82 | PWH |

## TABULATION CHART

| CONNECTOR | CABLE | MDB DESCRIPTION | | PART NO. |
|---|---|---|---|---|
| | | | | |
| | | | | |
| 26 PIN I/O 20083156 | 26 COND. RIBBON (20085006) | GPRCSR-26-D-XXX | | 50046852-XXX |
| | | | | |
| | | | | |
| | | | | |
| 60 PIN I/O 20083155 | 60 COND. RIBBON (20085008) | GPRCSR-60-D-XXX | | 50046856-XXX |




NOTE:

1. THE -XXX OF THE DWG NO. INDICATES LENGTH OF CABLE ASSY PER CHART NO. 6ACCCICI.
2. THE X IN PART NO. I.E. 50046851X INDICATES DIFFERENT CABLE ASSEMBLIES PER TABULATION CHART I.E.: 50046851-XXX REFERS TO A 10 COND. RIBBON CABLE WITH A 10 PIN I/O CONNECTOR ON BOTH ENDS AS PER ILLUSTRATION.

GPRCSR-D = GENERAL PURPOSE REVERSE CONNECTOR STRAIN RELIEF - DOUBLE. DOUBLE MEANING A CONNECTOR AT EACH END



| NEXT ASSY | USED ON |
|---|---|
| APPLICATION | |

PARTS LIST

| QTY REQD | FSCM NO | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL SPECIFICATION |
|---|---|---|---|---|

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO

MATERIAL

FINISH

DO NOT SCALE DRAWING

| APPROVALS | DATE |
|---|---|
| DRAWN J. McNEILLY | 7-9-82 |
| CHECKED L.A.T. JAMES | 7-12-82 |
| ISSUED PWH | 7-12-82 |

MDB SYSTEMS, INC.

GPRCSR-D-ASSEMBLY DWG

| SIZE | FSCM NO | DWG NO | REV |
|---|---|---|---|
| C | 51648 | 50046856X-XXX | A |

SCALE | SHEET 1 OF 1

50046856X-XXX 1 A

| DWG. NO. | SH | REV. |
|---|---|---|
| 10034032 | 1 | A |

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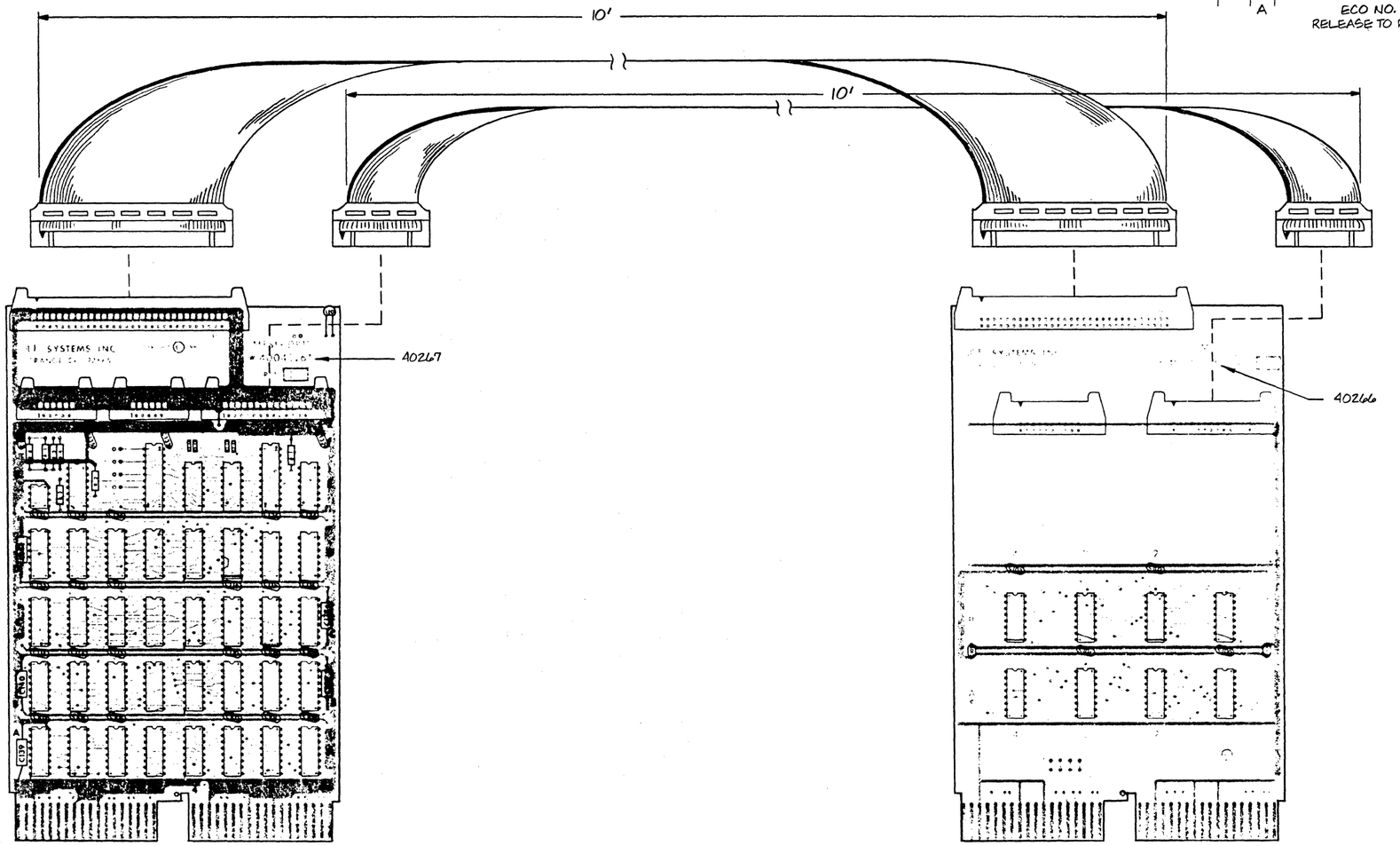
| ZONE | REV. | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| | A | ECO NO. 2039 RELEASE TO PRODUCTION | 7-9-82 | R WE |




NOTES:

1. INSERT 10' CABLES
   - A. 60 PIN FROM P1 (A0267 BD.) TO P1 (A0266 BD.)
   - B. 26 PIN FROM P2 (A0267 BD.) TO P2 (A0266 BD.)
2. INSERT A0267 IN LAST SLOT OF ISI BACKPLANE
3. INSERT A0266 IN FIRST SLOT OF EXPANSION BACKPLANE



| QTY REQD | FSCM NO. | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL SPECIFICATION |
|---|---|---|---|---|

PARTS LIST

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| APPLICATION | |

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MATERIAL

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| CHECKED RAY INBLUM | 7-12-82 |
| ISSUED Rudy | 7-13-82 |

MDB SYSTEMS, INC.

MLSI-DBIIR
BUS REPEATER

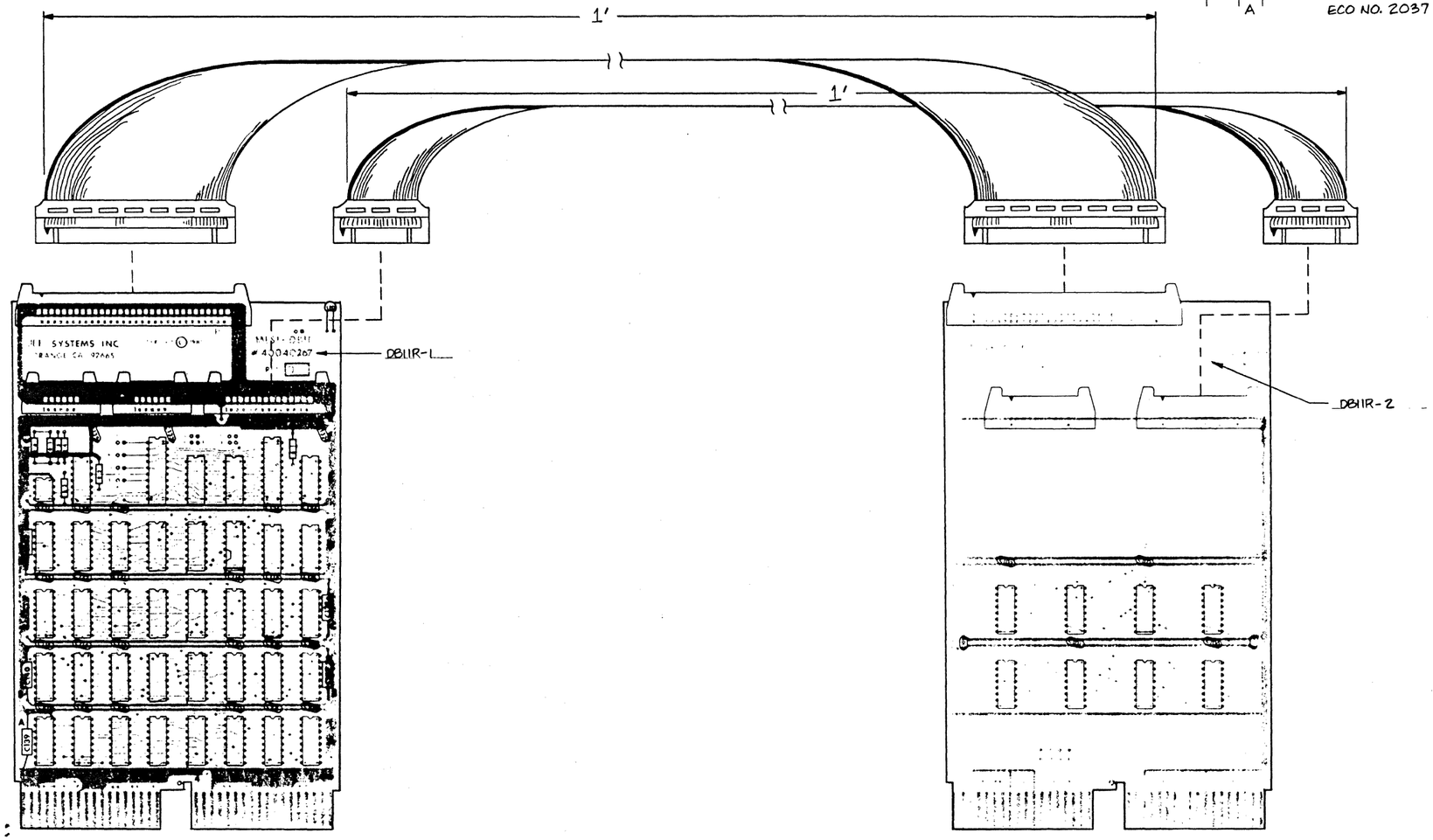
| SIZE | FSCM NO. | DWG. NO. | REV. |
|---|---|---|---|
| D | 51648 | 10034032 | A |

SCALE NTS SHEET 1 OF 1

| DWG. NO. | 10034033 | SH 1 | REV A |
|---|---|---|---|

REVISIONS

| ZONE | REV. | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| | A | ECO NO. 2037 | 7-9-82 | RWd |




NOTES:

1. INSERT 1' CABLES
   - A. 60 PIN FROM P1 (DB11R-1 BD.) TO P1 (DB11R-2 BD.)
   - B. 26 PIN FROM P2 (DB11R-1 BD.) TO P2 (DB11R-2 BD.)
2. INSERT DB11R-1 IN LAST SLOT OF ISI BACKPLANE
3. INSERT DB11R-2 IN FIRST SLOT OF EXPANSION BACKPLANE
4. THIS CONFIGURATION INTENDED FOR USE IN THE BA11-1000 CHASSIS



| QTY REQD | FSCM NO | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION | MATERIAL SPECIFICATION |
|---|---|---|---|---|

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
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.XXX

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

| APPROVALS | DATE |
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| DRAWN J. McNEILLY | 7-9-82 |
| CHECKED KAY INBLUM | 7-12-82 |
| ISSUED RWd | 7-12-82 |

# MDB SYSTEMS, INC.

## MLSI-DB11RA BUS REPEATER

| SIZE | FSCM NO. | DWG. NO. | REV. |
|---|---|---|---|
| D | 51648 | 10034033 | A |

SCALE NTS SHEET 1 OF 1

| DWG. NO. | SH | REV. |
|---|---|---|
| 44040266 | 1 | B |

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| ZONE | REV. | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| | A | ECO NO. 1255 | 9-81 | |
| | B | ECO NO. 1515 | 12-29-81 | |
| | B | RELEASE TO PRODUCTION<br>ECO NO. 1832 | 4-5-82 | |



| NEXT ASSY | USED ON |
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| APPLICATION | |

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

| APPROVALS | DATE |
|---|---|
| DRAWN J. MCNEILLY | 9-81 |
| CHECKED RWJ | 9-81 |
| ISSUED | 9-81 |

| QTY REQD | FSCM NO. | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL SPECIFICATION |
|---|---|---|---|---|

PARTS LIST

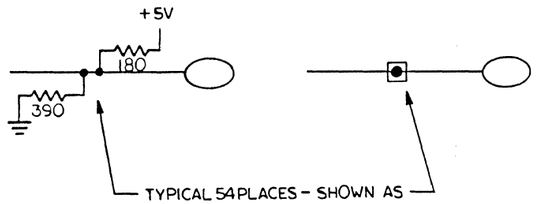
MDB SYSTEMS, INC.

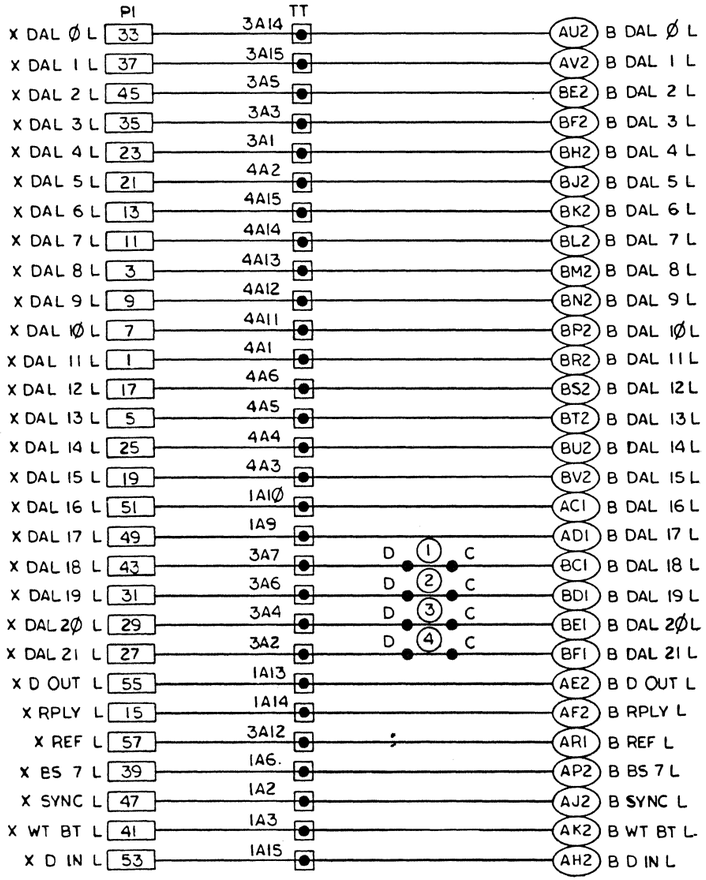
REPEATER TERMINATOR BOARD
MLSI-DB T

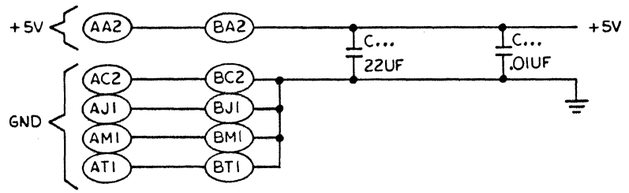
| SIZE | FSCM NO. | DWG. NO. | REV. |
|---|---|---|---|
| D | 51648 | 44040266 | B |

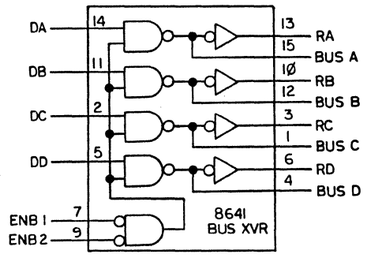
SCALE

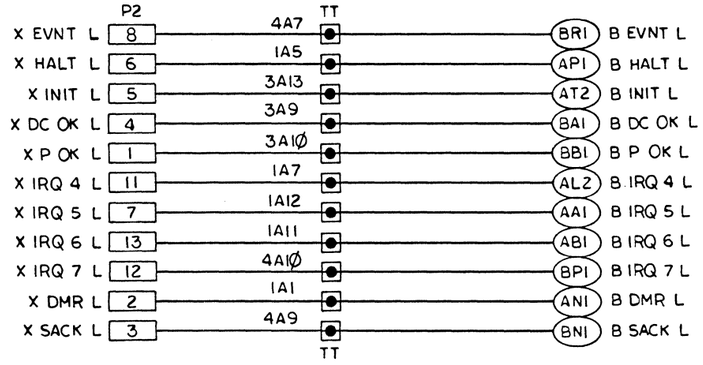
SHEET 1 OF 2

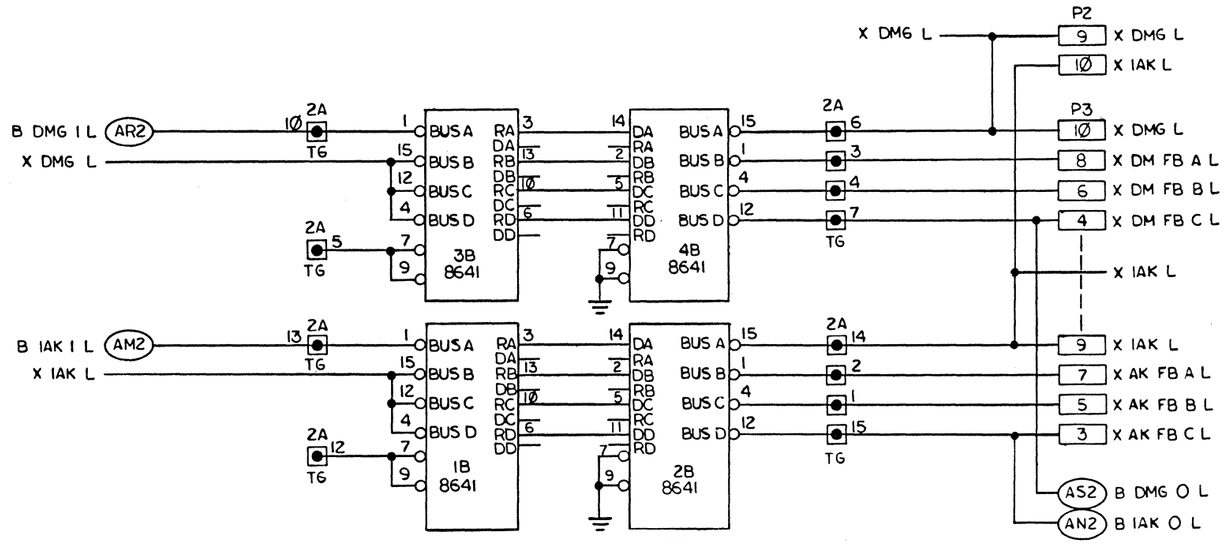


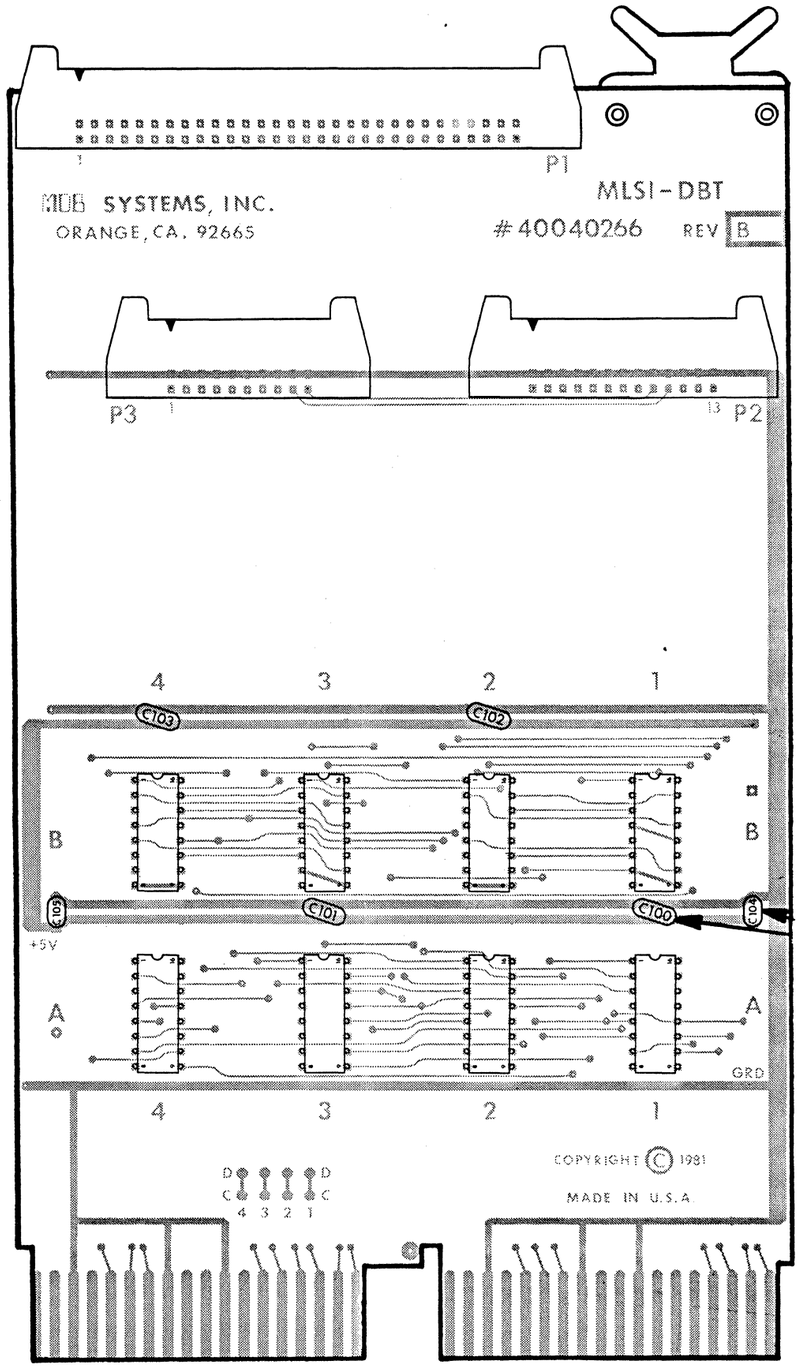




NOTE:

1. THE FOLLOWING IS A DESCRIPTION OF THE I.C.'S BEING USED AND THEIR POWER PIN NUMBERS:
   - A. 8641 - +5V = PIN 16
     GND = PIN 8
   - B. RESISTOR PAKS - +5V = PIN 16
     GND = PIN 8
2. THE FOLLOWING CONNECTOR PINS ARE GROUNDED
   - A. P1 - ALL EVEN PINS 2 THRU 60
   - B. P2 - ALL PINS 14 THRU 26
   - C. P3 - ALL PINS 11 THRU 20



| MDB SYSTEMS, INC. | SIZE | FSCM NO. | DWG. NO. | REV. |
|---|---|---|---|---|
| DRAWN J. MC. | D | 51648 | 44040266 | B |
| ISSUED Ray W Tomlinson | SCALE | | SHEET 2 OF 2 | |

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|---|---|---|---|---|
| MDB SYSTEMS, INC. | SIZE | FSCM NO. 51648 | DWG. NO. 45040266 | REV. B |
| DRAWN | | | | |
| ISSUED | SCALE | | SHEET 1 OF 1 | |

| DWG. NO. 44040267 | SH 1 | REV. D |
|---|---|---|

REVISIONS

| ZONE | REV. | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| | B | ECO NO. 1474 | 12-15-81 | RWS |
| | C | ECO NO. 1788 | 3-29-82 | RWS |
| | C | RELEASE TO PRODUCTION<br>ECO NO. 1831 | 4-5-82 | RWS |
| | D | ECO NO. 1926 | 5-13-82 | RWS |
| | D | RELEASE TO PRODUCTION<br>ECO NO. 2021 | 7-29-82 | RWS |
| | D1 | ECO NO. 2661 | 1-18-84 | |



| QTY REQD | FSCM NO. | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL SPECIFICATION |
|---|---|---|---|---|

PARTS LIST

| | |
|---|---|
| NEXT ASSY | USED ON |
| APPLICATION | |

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

| APPROVALS | DATE |
|---|---|
| DRAWN J. MC. | 12-15-81 |
| CHECKED KAY IMELUM | 3-29-82 |
| ISSUED R W Imhlum | 3-29-82 |

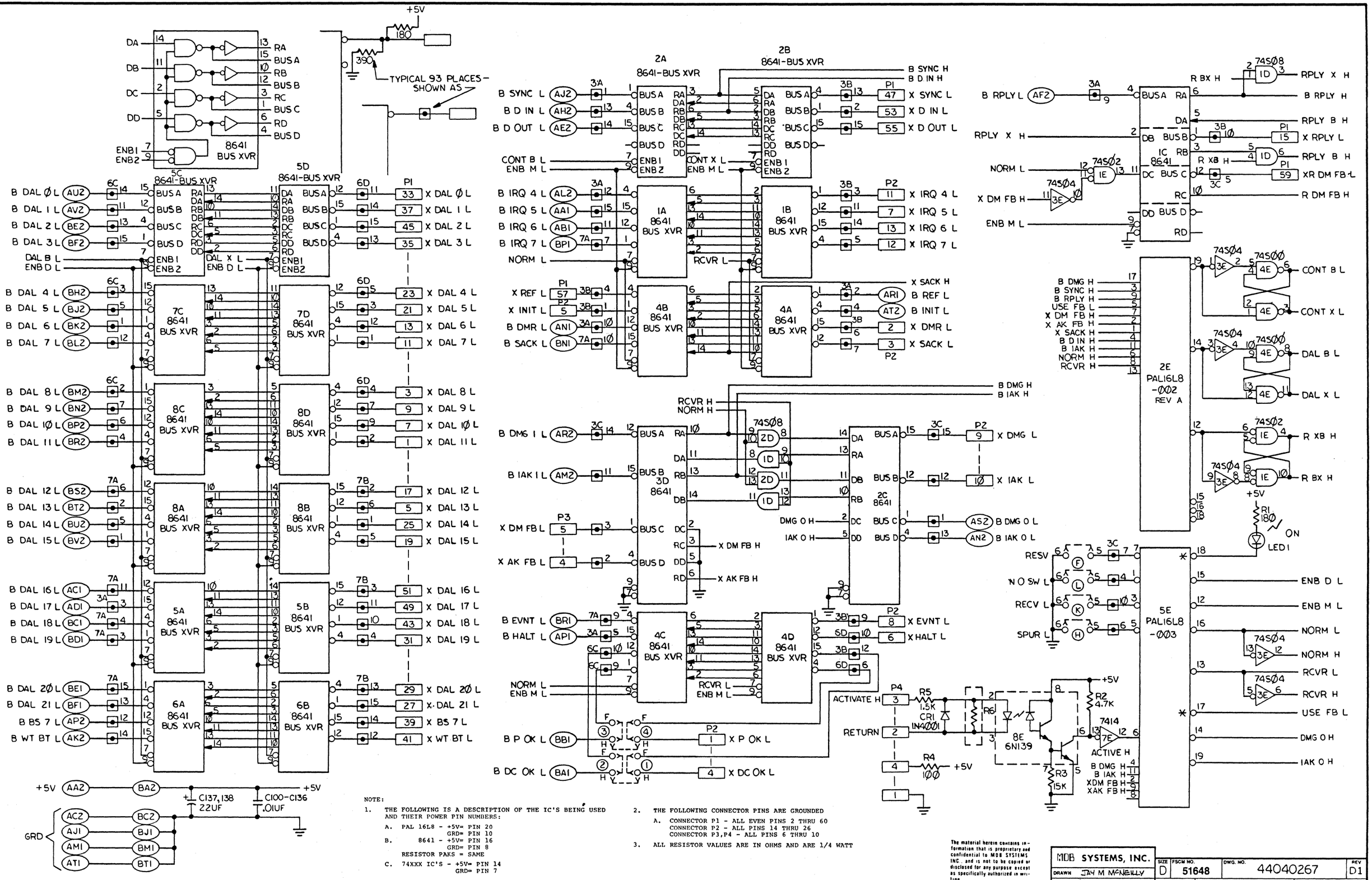
MDB SYSTEMS, INC.

MLSI-DB11

| SIZE | FSCM NO. | DWG. NO. | REV. |
|---|---|---|---|
| D | 51648 | 44040267 | D1 |

SCALE

SHEET 1 OF 2

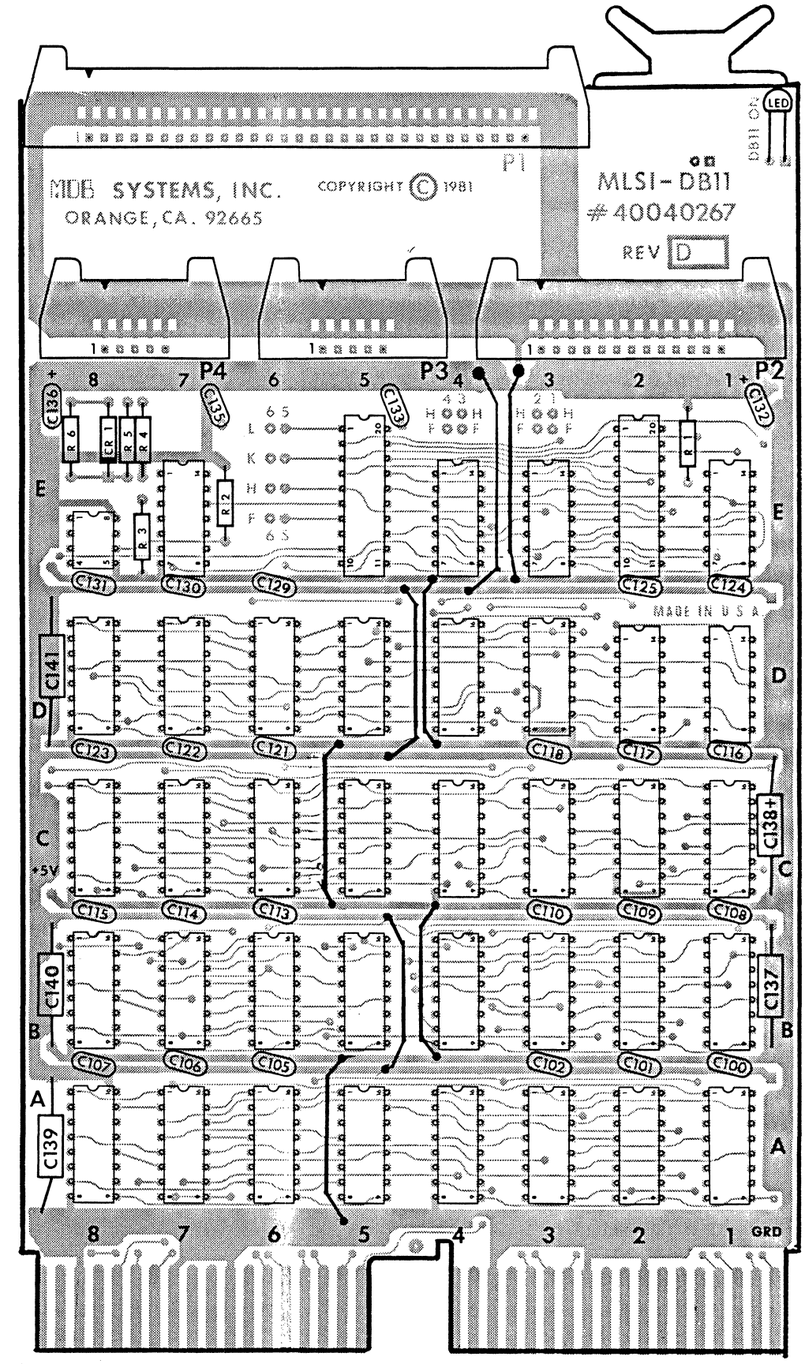



NOTE:

1. THE FOLLOWING IS A DESCRIPTION OF THE IC'S BEING USED AND THEIR POWER PIN NUMBERS:
   - A. PAL 16L8 - +5V= PIN 20, GRD= PIN 10
   - B. 8641 - +5V= PIN 16, GRD= PIN 8; RESISTOR PAKS = SAME
   - C. 74XXX IC'S - +5V= PIN 14, GRD= PIN 7
2. THE FOLLOWING CONNECTOR PINS ARE GROUNDED
   - A. CONNECTOR P1 - ALL EVEN PINS 2 THRU 60; CONNECTOR P2 - ALL PINS 14 THRU 26; CONNECTOR P3,P4 - ALL PINS 6 THRU 10
3. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4 WATT



| | | | | | |
|---|---|---|---|---|---|
| MDB SYSTEMS, INC. | | SIZE D | FSCM NO. 51648 | DWG. NO. 44040267 | REV D1 |
| DRAWN JAY M MCNEILLY | | | | | |
| ISSUED RAY IMBLUM 3-3-82 | SCALE | | | SHEET 2 OF 2 | |




| MDB SYSTEMS, INC. | SIZE | FSCM NO. | DWG. NO. | REV. |
|---|---|---|---|---|
| DRAWN | | 51648 | 45040267 | D |
| ISSUED | SCALE | | SHEET 1 OF 1 | |

**MDB SYSTEMS, INC.**
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TWX: 910-593-1339