REV	EO	DESCRIPTION	DWN	CHKD	APPD	DATE
AX	6114	PROTO RELEASE	[illegible]	[illegible]	[illegible]	1/31/77

PROTOTYPE

CURRENT REV	AX	AX	AX	AX	AX	AX	AX		
SHEET NO.	10	11	12	13	14	15	16	17	18
CURRENT REV.	AX	AX	AX	AX	AX	AX	AX	AX	AX
SHEET NO.	1	2	3	4	5	6	7	8	9

UNINCORPORATED ENGINEERING ORDERS	

	DATE
PREPARED K.Batman	1-27-77
CHECKER [signature]	1-31-77
ENGINEER [signature]	
APPD [signature]	1/28/77
APPD	
APPD	
RECORDS L. Roemer	1/31/77

TITLE

INTERFACE SPECIFICATION
REFLEX MOD II

IDENT CODE 52936

Microdata™
IRVINE, CALIFORNIA

DWG SIZE		REV
A	IS 20013000	AX
	SHEET 1 OF 16	

Form 3-132-1

1.0 MOD II INTERFACE

1.1 General

The MOD II Interface board provides the REFLEX disk drive family with architectural compatibility with the CDC 9762-1 disk drive. This configuration uses eight bus out lines and three tag lines for address and control. The decoded tag lines allow eight possible combinations of tag functions. The tag function is strobed with Tag Gate Out which indicates the Bus In information is valid. This interface also has eight Bus In lines which, when multiplexed, allows up to thirty-two different status bits to the control unit.

1.2 All input and output signals are digital. They are transmitted and received differentially.

1.3 A terminated and balanced transmission system is achieved by using industry standard type 75110 and 75108 or equivalent transmitters and receivers.

1.4 A signal ground strap must be provided from the controller and must be daisy chained to each REFLEX. One-quarter (¼) inch ground braid is recommended.

1.5 REFLEX requires three cables: (1)An A.C. power cable, (2)A data cable, and (3)A signal cable. The total length of the data cable of the signal cable may not exceed 50 feet.

1.6 Ribbon cable with a ground plane is used for the data cable. It has twenty conductors with drain wire and has the following characteristics:

28 AWG, 7 Strand

.005 In. Copper Mesh Ground Plane

65 Ohm Impedance

1.7 Ribbon cable is used for the signal cable. It has the following characteristics:

60 Conductor

100 ± 10% Ohm Impedance

1.8 Data Cable

1.8.1 The data cable consists of lines that are unique to each REFLEX.

1.8.2 I READ/WRITE DATA - A bi-directional line used to transmit write data to the drive or to transmit read data to the control unit. The data is NRZI in both cases.

1.8.3 I WRITE CLOCK - A line used to transmit write clock signal to be syn-

chronized to the NRZI data. Write clock is the Servo PLO re-transmitted to REFLEX. Write clock must be transmitted continuously.

1.8.4 I READ CLOCK - A line used to send the clock that defines the beginning of a data cell. It is in phase sync within 10 µs after read is active. This signal is 7.08 MHZ ± 5%.

1.8.5 I SERVO CLOCK - A line used to send phase locked clock generated from the servo tracks at 7.08 MHZ ± 5%. It is continuously transmitted by REFLEX.

1.8.6 I ADDRESS ACKNOWLEDGED - A line used to signal that the last Tag Decode 000 caused selection of this drive and that the drive shall transmit status and data as required over the interface circuits.

1.8.7 I INTERRUPT MH - A line used to signal the control unit that the contents of the moving head target register is equal to the present sector location.

1.8.8 I INTERRUPT FH - A line used to signal the control unit that the contents of the fixed head target register is equal to the present sector location.

1.8.9 I SEEK END - A line used to signal the control unit that the drive has completed a Seek operation. This condition is satisfied by either a normal On Cylinder condition following a Seek Command or an incomplete Seek Operation resulting from a Seek Operation.

1.8.10 I START - A line from the control unit which allows a controlled power sequence up or sequence down. It also acts as an open cable detector thus preventing a sequence up condition if the line is open.

1.9 Signal Cable

1.9.1 For installations using more than one REFLEX, the signal cables can be daisy chain cabled or star cabled.

1.9.2 Tag Decode 000 (Select) - If the decoded unit address is equal to the unit address switch setting internal to the drive, the drive shall become selected.

1.9.2.1 I Bus Out 7 - Least significant bit of unit address.

1.9.2.2 I Bus Out 6 - Most significant bit of unit address.

1.9.2.3 I Bus In 7 - Least significant bit of drive unit address.

1.9.2.4 I Bus In 6 - Most significant bit of drive unit address.

1.9.2.5 I Bus In 5 - Fixed head configuration.

0= No fixed heads

1= 30 tracks of fixed heads.

1.9.2.6 I Bus In 4 - Reserved for fixed head expansion.

1.9.2.7 I Bus In 3 - Attention: The heads have been unloaded. Attention is reset by the Clear Attention Command.

1.9.2.8 I Bus In 2 and Bus In 1 - Moving head configuration:

01= 2 heads (Bus In 2 least significant bit)

10= 6 heads

11=10 heads

1.9.2.9 I Bus In 0 = Number of moving head tracks.

0= 350 tracks

1= 700 tracks

1.9.3 Tag 001 Error Recovery - This tag decode is used to recover any marginally recorded data from the disk.

1.9.3.1 I Bus Out 3 Offset Reverse - This bit offsets the servo away from the spindle with respect to its normal track follow position. The servo will remain in this position until cleared by an Offset Forward Command, a Restore Command, a Seek Command, a Clear Error Recovery Command, or a Tag 001 with Bus Out 3 inactive.

1.9.3.2 I Bus Out 2 Offset Forward - This bit offsets the servo toward the spindle with respect to its normal track follow position. The servo will remain in this position until cleared by an Offset Reverse Command, a Restore Command, a Seek Command, a Clear Error Recovery Command, or a Tag 001 with Bus Out 2 inactive.

1.9.3.3 I Bus Out 1 Data Strobe Late - This bit will command the data recovery circuitry to strobe the data at a time 8 ns later than normal. This command is cleared by a Restore Command, a Seek Command, a Clear Error Recovery Command or a Tag 001 with Bus Out 1 inactive.

1.9.3.4 I Bus Out 0 Data Strobe Early - This bit will command the data recovery circuitry to strobe the data at a time 8 ns earlier than normal. This command is cleared by a Restore Command, a Seek Command, a Clear Error Recovery Command, or a Tag 001 with Bus Out 0 inactive.

1.9.3.5 I Bus In's are the same as for Tag Decode 000.

A servo offset command will result in a loss of On Cylinder and Seek End for 3 ms maximum. Any attempt to write while offset is active will cause a Fault in the drive.

1.9.4 Tag 010 Diagnostic - When this tag is active, the fault status is available on the Bus In lines for the control unit and the drive will respond to the following commands:

1.9.4.1 I Bus Out 7 Fixed Heads Status - This bit

selects the fixed head status register for monitoring by the control unit.

1.9.4.2 I Bus Out 6 Interrupt Reset Gate - This bit allows the interrupt reset to initiate a fixed head interrupt or a moving head interrupt.

0= Moving Head Interrupt
1= Fixed Head Interrupt

1.9.4.3 I Bus Out 5 Clear RPS Interrupt - This bit shall reset the enable condition and RPS interrupts will be inhibited each revolution.

1.9.4.4 I Bus Out 4 Clear Error Recovery - This bit shall reset the error recovery conditions set by the Tag 001.

1.9.4.5 I Bus Out 3 Clear Fault Status - This bit resets the fault condition and clears the fault isolation register.

1.9.4.6 I Bus Out 2 Clear Check Diagnostic - This bit resets the check diagnostic condition.

1.9.4.7 I Bus Out 1 Clear Attention - This bit resets the attention condition.

1.9.4.8 I Bus Out 0 Restore - This bit returns the heads to cylinder 000. Restore will reset any Seek Error conditions and will set the head address to 000.

1.9.4.9 I Bus In 7 Write Protect Fault - This bit indicates that a write operation was attempted on a Write Protected Unit. This condition is reset by the Clear Fault Status Command.

1.9.4.10 I Bus In 6 Seek Error - This bit indicates that the drive failed to complete a seek in a normal manner, or that an illegal cylinder address was requested by the control unit. This condition is reset by a restore function.

1.9.4.11 I Bus In 5 Head Select Fault - This bit indicates a malfunction has occurred in the head address circuits and the drive is inhibited from writing. A clear check diagnostic command is required to reset this fault.

1.9.4.12 I Bus In 4 Voltage Fault - This bit indicates an unsafe DC voltage condition exists in the drive. All write operations are inhibited and the drive is in a sequenced down state. Power sequencing is required to reset this fault.

1.9.4.13 I Bus In 3 Write and Read Fault - This bit indicates that the write and read gates are active simultaneously. Writing is inhibited during this time. A clear check diagnostic command is used to clear this fault.

1.9.4.14 I Bus In 2 Write or Read Offtrack - This bit

indicates that a Read or Write was attempted when the heads were not on track. A clear check diagnostic and a Restore Command are required to clear this fault.

1.9.4.15 I Bus In 1 Write Fault - This bit indicates write current was absent while Write Gate was active. A clear check diagnostic command resets this fault.

1.9.4.16 I Bus In 0 Illegal Head - This bit indicates the control unit has requested a head address that does not exist.

1.9.5 Tag 011 Head Address Decode - This tag decodes head address bits being sent from the control unit.

1.9.5.1 I Bus Out 7 - Head 1.

1.9.5.2 I Bus Out 6 - Head 2.

1.9.5.3 I But Out 5 - Head 4.

1.9.5.4 I Bus Out 4 - Head 8.

1.9.5.5 I Bus Out 3 - Head 16.

1.9.5.6 I Bus Out 2 - Head 32.

1.9.5.7 I Bus Out 0 - (Fixed Head Select) - This bit loads the head address into the fixed head address register.

1.9.5.8 I Bus In's are the same as for Tag Decode 010.

1.9.6 Tag 100 High Cylinder Address - This tag decode is used to transmit the most significant bits of the desired cylinder address. It must always precede the low cylinder address tag.

1.9.6.1 I Bus Out 7 - Cylinder 256.

1.9.6.2 I Bus Out 6 - Cylinder 512.

1.9.6.3 I Bus In 7 thru I Bus In 2 - Indicates the contents of either the moving or fixed head target registers or the contents of either the moving or fixed head sector counters. Bus In 7 is the least significant bit.

1.9.6.4 I Bus In 1 Data Source.

1= Fixed Head

0= Moving Head

1.9.6.5 I Bus In 0 Register Source.

1= Target Register

0= Sector Counter

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DWG SIZE	SHEET 6 OF 16	REV

1.9.7 Tag 101 Target Register - If this tag decode and Bus Out 0 are active, the desired sector address for rotational positioning sensing is transmitted to the drive. The RPS interrupt will be enabled and each time the contents of the sector counter compare with the contents of the target register, the interrupt line shall become active. This will continue to occur until a clear RPS command is generated by the control unit. The Bus In lines will contain the contents of the target register after the transfer and can be used to echo check the Bus Out and Bus In lines. If Bus Out 0 is inactive, the target register is cleared and the Bus In lines will contain the contents of the sector counter.

1.9.7.1 I Bus Out 7 thru I Bus Out 2 - The desired target address. Bus Out 7 is the least significant bit.

1.9.7.2 I Bus Out 1 Circuit Select.

1= Fixed Head

0= Moving Head

1.9.7.3 I Bus Out 0 Load or Echo.

1= Load Target

1= Echo Sector

1.9.7.4 Bus In's are the same as for Tag Decode 100.

1.9.8 Tag 110 Low Cylinder Address - This tag decode transmits the eight least significant bits of the desired cylinder address. The Seek Command is initiated with this tag decode.

1.9.8.1 I Bus Out 7 = Cylinder 001.

1.9.8.2 I Bus Out 6 = Cylinder 002.

1.9.8.3 I Bus Out 5 = Cylinder 004.

1.9.8.4 I Bus Out 4 = Cylinder 008.

1.9.8.5 I Bus Out 3 = Cylinder 016.

1.9.8.6 I Bus Out 2 = Cylinder 032.

1.9.8.7 I Bus Out 1 = Cylinder 064.

1.9.8.8 I Bus Out 0 = Cylinder 128.

1.9.8.9 I Bus In 7 Check Diagnostic - This bit indicates a detected malfunction within the drive electronics. The control unit should check status further by use of the Diagnostic Tag 010. This condition can be cleared by a Clear Fault Command, Clear Check Diagnos-

tic Command, or by the CE reset switch in the drive. If the check diagnostic condition resulted from a Seek Command, the condition is cleared only by a Restore Command or a Power Sequence.

1.9.8.10 I Bus In 6 Offset Active - This bit indicates the servo is offset in response to an Offset Command.

1.9.8.11 I Bus In 5 Fixed Head Fault - This bit indicates that a fault has occurred in the fixed head electronics.

1.9.8.12 I Bus In 4 Fixed Heads Active - This bit indicates that the fixed heads are selected.

1.9.8.13 I Bus In 3 Unit Ready - This bit indicates that the drive is operational with no fault conditions present.

1.9.8.14 I Bus In 2 On Cylinder - This bit indicates that the drive is capable of reading or writing data or performing a Seek Command. Momentary loss of this condition is to be expected when the carriage has been offset.

1.9.9 I Tag 111 Control Decode - When this tag is decoded, control information is on the bus lines.

1.9.9.1 I Bus Out 3 Read Gate - This command enables the data recovery electronics and causes read data to be sent to the control unit along with read clock. The leading edge of this command initiates the phase lock of the decoding electronics and should occur only over an all zeroes field.

1.9.9.2 I Bus Out 1 Write Gate - This command causes data generated by the control unit to be written on the disk.

1.9.9.3 I Bus In's are the same as for tag decode 110.

1.9.10 I Tag Gate Out - This bit gates the tag decode. It is a pulse for select, head address, high cylinder, low cylinder, target register, diagnostic and read target register. It must be held active for control functions.

1.9.11 I Tag Gate In - This bit indicates that the information on the Bus In lines is valid.

INTERFACE SIGNAL CABLE PINOUT

NOTES:

1. For signals generated by the REFLEX, any term name followed by a (/) is connected to the (-) pin of its line driver.

2. For signals received by the REFLEX, any term name followed by a (/) is connected to the (-) pin of control unit line driver.

	J2, J3
IBUSOUT Ø	4
IBUSOUT Ø/	3
IBUSOUT 1	6
IBUSOUT 1/	5
IBUSOUT 2	8
IBUSOUT 2/	7
IBUSOUT 3	10
IBUSOUT 3/	9
IBUSOUT 4	12
IBUSOUT 4/	11
IBUSOUT 5	14
IBUSOUT 5/	13
IBUSOUT 6	16
IBUSOUT 6/	15
IBUSOUT 7	18
IBUSOUT 7/	17
ITAG Ø	48
ITAG Ø/	47
ITAG 1	52
ITAG 1/	51
ITAG 2	54
ITAG 2/	53
ITAG GATE OUT	46
ITAG GATE OUT/	45
ISELECT HOLD	44
ISELECT HOLD/	43
IBUSIN Ø	20
IBUSIN Ø/	19
IBUSIN 1	22
IBUSIN 1/	21
IBUSIN 2	24
IBUSIN 2/	23
IBUSIN 3	26
IBUSIN 3/	25
IBUSIN 4	28
IBUSIN 4/	27
IBUSIN 5	30
IBUSIN 5/	29
IBUSIN 6	32
IBUSIN 6/	31
IBUSIN 7	34
IBUSIN 7/	33
ITAG GATE IN	2
ITAG GATE IN/	1
IINDEX	36
IINDEX/	35
ISECTOR	50
ISECTOR/	49

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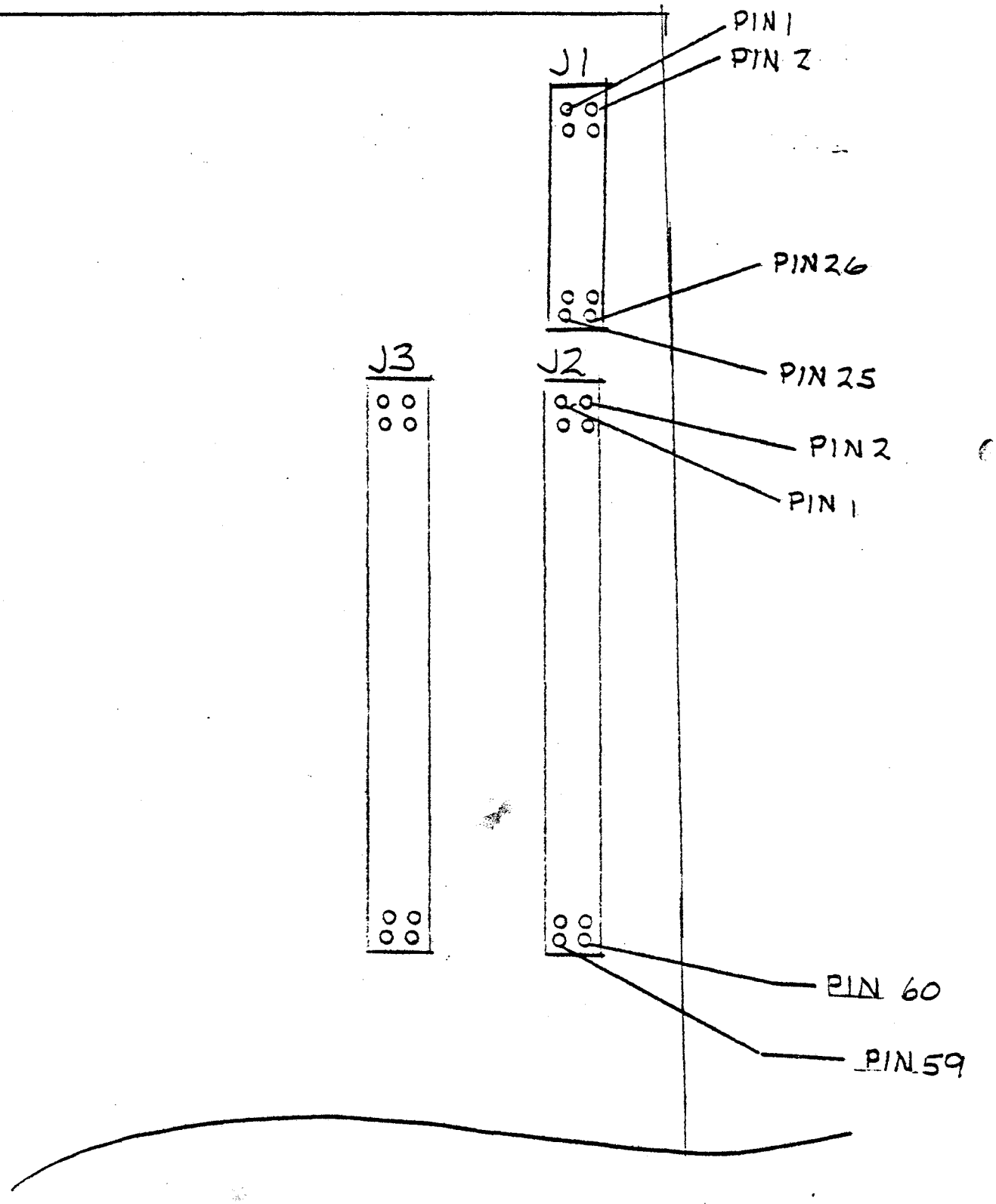
DWG SIZE	SHEET 9 OF 16	REV

INTERFACE DATA CABLE PINOUT

	J1
ISTART	6
ISTART/	5
IADDRESS ACKNOWLEDGED	18
IADDRESS ACKNOWLEDGED/	17
IINTERRUPT MH	22
IINTERRUPT MH/	23
IINTERRUPT FH	26
IINTERRUPT FH/	25
ISEEK END	20
ISEEK END/	19
ISERVO CLOCK	3
ISERVO CLOCK/	2
IREAD CLOCK	8
IREAD CLOCK/	9
IWRITE CLOCK	11
IWRITE CLOCK/	12
IREAD/WRITE DATA	14
IREAD/WRITE DATA/	15

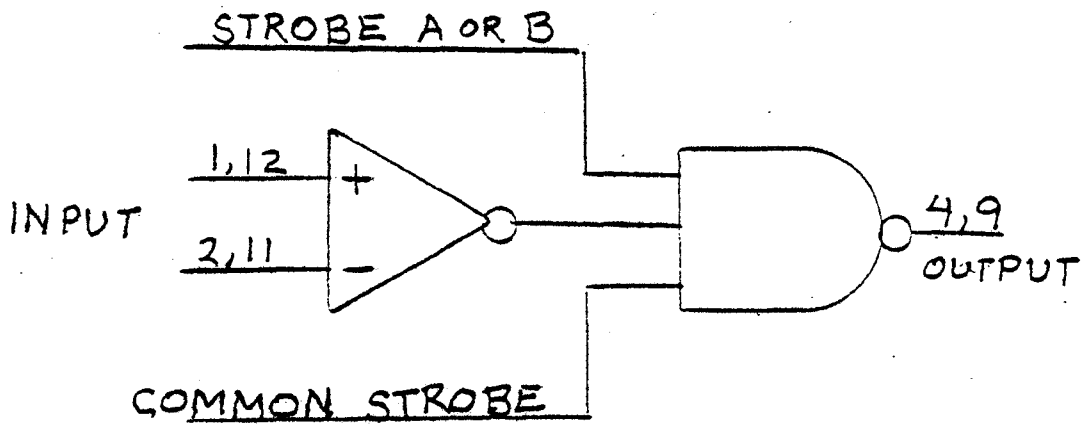


TOP VIEW OF J1 (DATA CABLE)
AND J2/J3 (SIGNAL CABLE)

A	IS 20013000	AX
DWG SIZE	SHEET 11 OF 16	REV

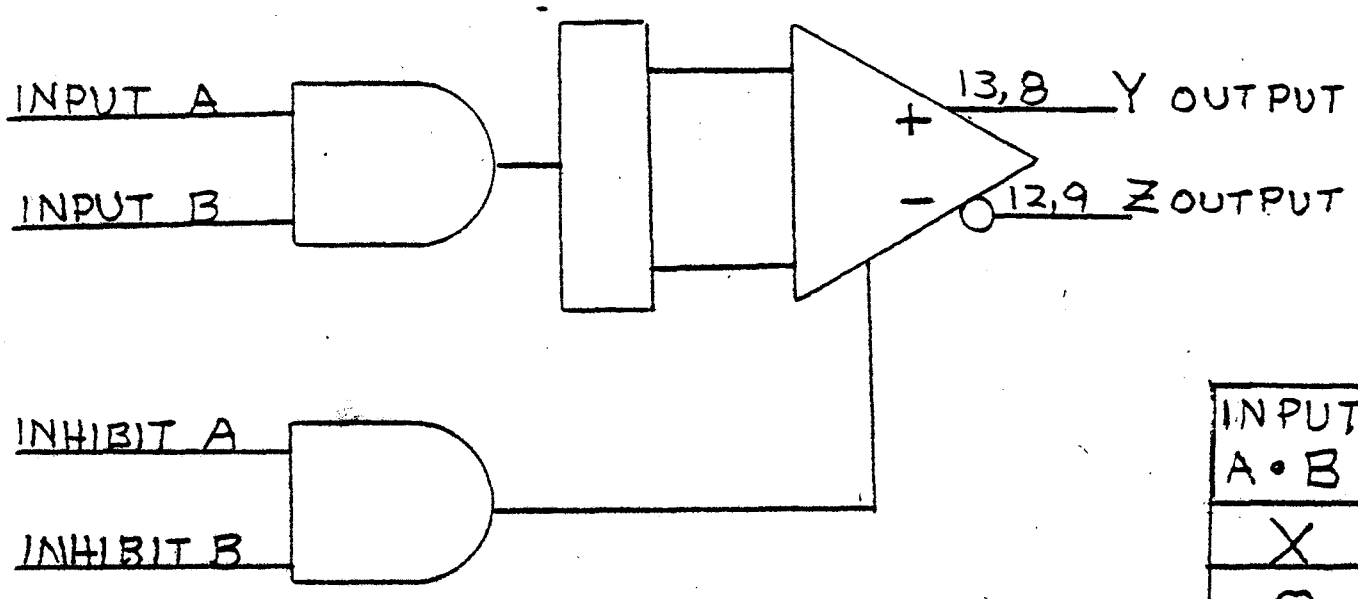
FORM 3-132-2

75107 OR 75108 RECEIVER



INPUT PIN +	INPUT PIN −	STROBE COMMON	STROBE A+B	OUTPUT
X	X	0	X	1
X	X	1	0	1
−	+	1	1	0
+	−	1	1	1
+	+	1	1	X
−	−	1	1	X

75110 DRIVER



INPUT A·B	INHIBIT A·B	OUTPUT Y	OUTPUT Z
X	0	+	+
0	1	−	+
1	1	+	−

A	IS 20013000	AX
DWG SIZE	SHEET 12 OF 16	REV

FORM 3-132-2

BUS OUT								
BUS / TAG	0	1	2	3	4	5	6	7
SELECT 0 0 0							2^1	2^0
ERR REC 0 0 1	EARLY STROBE	LATE STROBE	(+) OFFSET	(−) OFFSET				
DIAG 0 1 0	RESTORE	CLEAR ATTEN-TION	CLEAR CHECK DIAG	CLEAR FAULT STATUS	CLEAR ERROR REC	CLEAR RPS	CLEAR FH INT	SELECT FH STATUS
HD ADDR 0 1 1	SELECT FH		2^5	2^4	2^3	2^2	2^1	2^0
HI CYL 1 0 0							2^9	2^8
TARGET 1 0 1	LOAD TARGET REG	SELECT FH TARGET	2^5	2^4	2^3	2^2	2^1	2^0
LOW CYL 1 1 0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
CONTROL 1 1 1	TRANS-FER SECTOR COUNT	WRITE GATE		READ GATE				

BUS OUT DECODE

A	IS 20013000	AX
DWG SIZE	SHEET 13 OF 16	REV

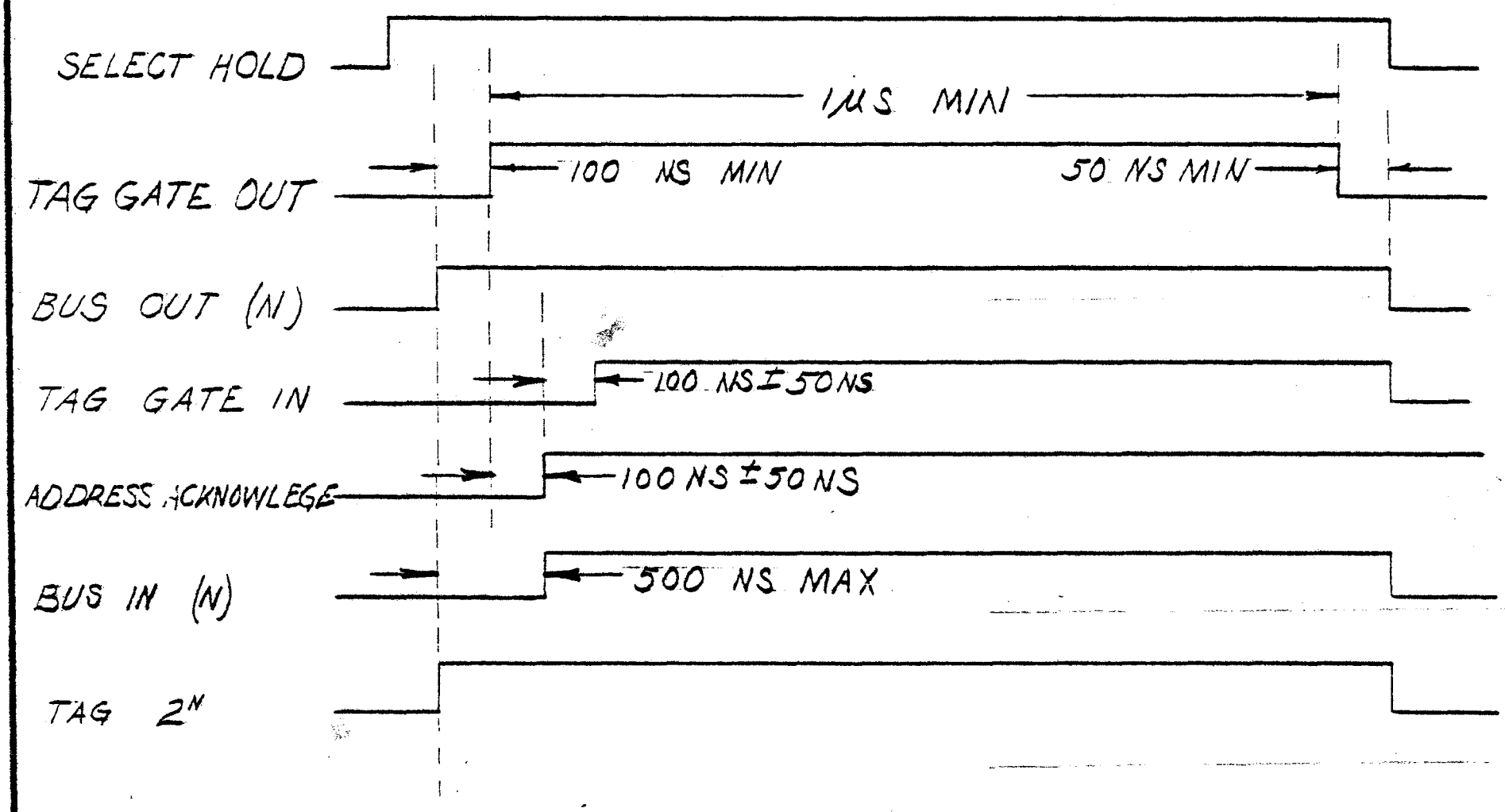
FORM 3-132-2

BUS IN								
BUS / TAG	0	1	2	3	4	5	6	7
SELECT 000	CONFIG 2^4	CONFIG 2^3	CONFIG 2^2	ATTEN-TION	CONFIG 2^1	CONFIG 2^0	ADDR 2^1	ADDR 2^0
ERR REC 001	11	11	11	11	11	11	11	11
DIAG 010	ILL HD	WRITE FAULT	W+R OFF TRK	W/R FAULT	VOLTAGE FAULT	HEAD SELECT FAULT	SEEK ERROR	WRITE PROTECT FAULT
HD ADDR 011	11	11	11	11	11	11	11	11
HI CYL 100	ECHO TARGET REG	ECHO FH REG	2^5	2^4	2^3	2^2	2^1	2^0
TARGET 101	11	11	11	11	11	11	11	11
LOW CYL 110			ON CYL	UNIT READY	FH ACTIVE	FH FAULT	OFFSET ACTIVE	CHECK DIAG
CONTROL 111	11	11	11	11	11	11	11	11

BUS IN DECODE

A	IS 20013000	AX
DWG SIZE	SHEET 14 OF 16	REV

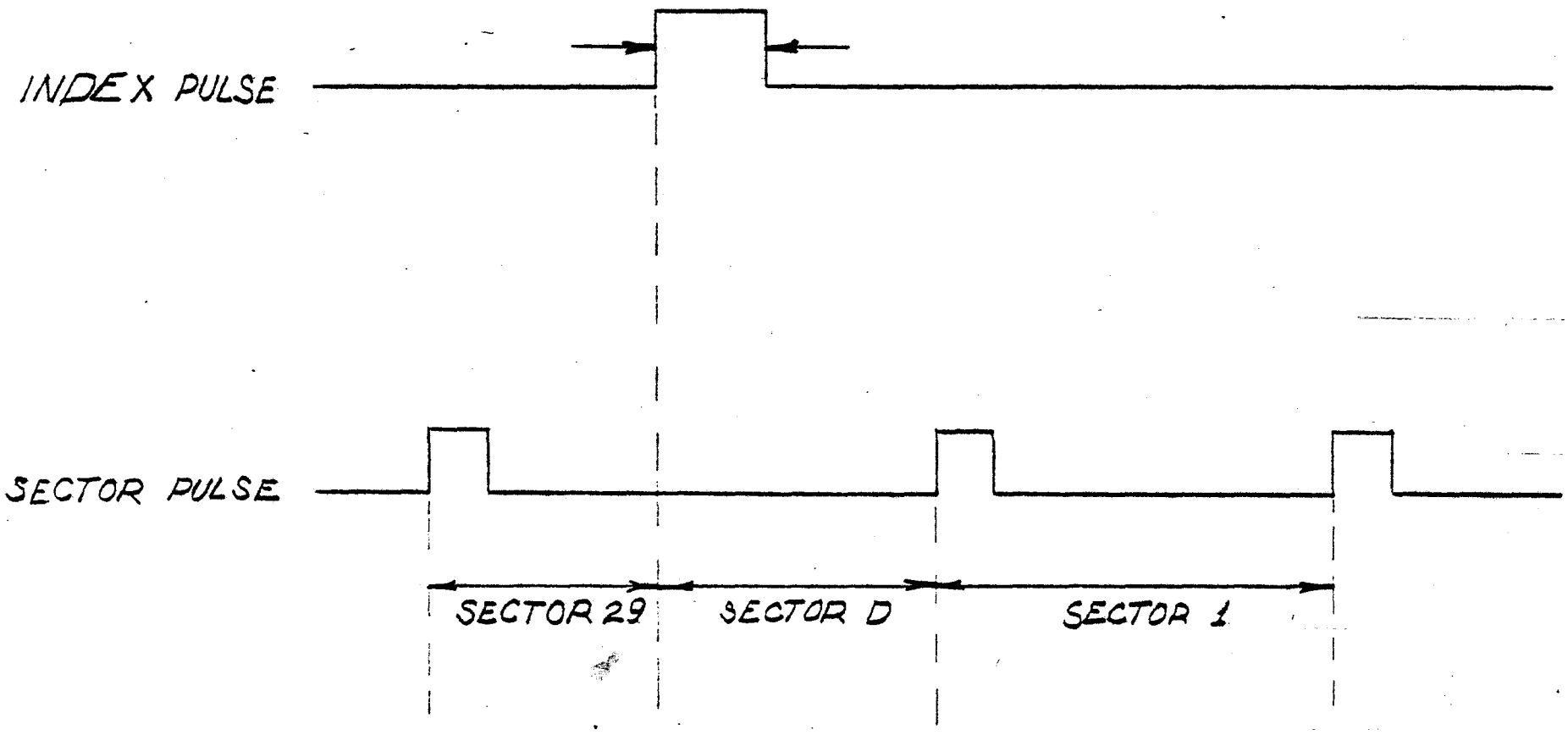
FORM 3-132-2



TIMING AT THE INTERFACE

A	IS 20013000	AX
DWG SIZE	SHEET 15 OF 16	REV

FORM 3-132-2



INDEX AND SECTOR TIMING

A	IS 20013000	A-X'
DWG SIZE	SHEET 16 OF 16	REV

FORM 3-132-2

SUMMARY

FIXED DISC UNIT

SPECIFICATION

Model	1	2	3	9000
Capacity (M Bytes Unformatted)	12.6	38	63.4	12.5
Bit Density	5700	5700	5700	2200
Track Density (Tracks/inch)	300	300	300	200
Tracks/Surface	700	700	700	406
Positioning Time (msec)				
Track to Track	6	6	6	10
Average	30	30	30	35
Full Stroke	55	55	55	70
R P M	3000	3000	3000	2400
Options:				
Fixed Heads 32 Tracks (M Bytes)	.54	.54	.54	No
R P M	No	No	No	1500
	2400	2400	2400	No
	3600	3600	3600	No