

PRODUCT MANUAL MODEL 3180E

130 or 182 MByte 5¼″ Half-Height Winchester Disk Drives



- ESDI or SCSI interface
- Fast 17 msec. avg. access time
- 35,000 hour MTBF
- Proven technology
- Very low power consumption
- Single printed circuit board
- Non-data landing zone and automatic carriage lock
- Rugged thin film media
- Superior shock and vibration and thermal design

MiniScribe's 3130 and 3180 disk drives deliver true full-height performance in a half-height form factor.

The newest generation of personal computers and workstations are featuring smaller footprints, lower profiles and are packed with higher performance. The 3130 and 3180 models are available in either SCSI or ESDI interfaces to meet this need. This new series has been designed to bring the latest technologies to MiniScribe's full product line of data storage solutions.

Formatted storage capacities of the 3130/3180 Series range from 112 MBytes to 160 MBytes and average access times of 17 msec. are achieved. Data integrity is ensured by rugged thin film media.

Because of its extensive product line, MiniScribe is able to bring a variety of proven technology building blocks to the development of new products. The 3130 and 3180 products have benefited from this strength.

Superior shock and vibration and thermal performance are realized by the four-point mounting system and by an enhanced baseplate design.

The series also features efficiencies of low power dissipation. The ESDI models maintain power dissipation of only 15 watts when idle and the SCSI models 17 watts.

The 3130/3180 Series has been designed for automated robotic assembly. MiniScribe's integrated manufacturing experience delivers the highest, most consistent quality. Assembly design has been simplified to include fewer subassemblies. Rapid production ramp-up is facilitated by MiniScribe's "designed-forautomation" principles and by its modular, software-based assembly techniques.

Prior to shipment, MiniScribe drives undergo rigorous burn-in and testing which ensures high standards of reliability and performance.

In addition to the 3130 and 3180 drives, the company produces a complete line of 3½-inch and 5¼-inch Winchester disk drives which begin at 20 MBytes, extend to high capacity/high performance models, and include a variety of standard, intelligent and custom interfaces.



5¹/₄" Half-Height Winchester **Disk Drive Specifications**

					The Broke second	and the second s
		3130E		3180E	3130S	3180S
Capacity Unformatted						
Per Drive (MBytes)		130		182	130	182
Per Track (Bytes)		20,832		20,832	20,832	20,832
Capacity Formatted						
Per Drive (MBytes)		112		157	115	160
Per Track (Bytes)		17,920		17,920	18,432	18,432
Per Sector (Bytes)		512		512	512	512
Sectors Per Track		35		35	36	36
Functional						
Disks		3		4	3	4
Servo Heads		1		1	1	1
R/W Heads		5		7	5	7
		1250		1250	1255	, 1255
Cylinders				and the second second		
Track Density (tpi)		1,193		1,193	1,193	1,193
Recording Density (bpi)	1	19,763		19,763	19,763	19,763
Areal Density (Mbits/sq.in Rotational Speed (RPM)	.)	13.4 3,600		13.4 3,600	13.4 3.600	13.4 3,600
						100.000.000
Interface		ESDI		ESDI	SCSI	SCSI
Data Transfer Rate		10.0 M				
(per second)		10.0 Mb		10.0 Mbits	4.0 MBytes	1 2000 Million - 100 Million
Recording Method		2,7 RLL		2,7 RLL	2,7 RLL	2,7 RLL
Access Time (including	settling)					
Average (msec.)		17		17	17	17
Track-to-track (msec.)		4.0		4.0	4.0	4.0
Maximum (msec.)		35		35	35	35
Latency (average, msec.)		8.33		8.33	8.33	8.33
DC Dower Beguirement	-		2120E	/3180E	212	0S/3180S
DC Power Requirement	.5					
+ 5 VDC ±5%				nps typical		amps typical
+12 VDC ±5%			1.1 amps typical 2.5 amps			amps typical
Max. Starting (10 sec.)			2.5 an	nps	2.5	amps
Power Dissipation						the baseline l
Idle				tts typical		watts typical
Seeking			18 wat	tts typical	20	watts typical
Environmental Limits						
Ambient Temperature				to 122°F		F to 122°F
B L P L L L P				to 50 °C)	and an	°C to 50 °C)
Relative Humidity			8% to			to 80%
Maximum Wet Bulb			78°F (26°C)	785	°F (26 °C)
Error Rates	a. e		Reliat	sility		
Soft Read Errors	1 per 10 ¹⁰ bits		MTBF	Jinty	35 (000 hours
Son nead Enors	transferred		PM		Nor	
Hard Read Errors	1 per 10 ¹² bits		MTTR			ninutes
	transferred			onent Design		
Seek Errors	1 per 10 ⁶ seeks				0 yt	
Shock	14		Physic		1.00)E in
Operational	2 G's, 11 msec.		Height			25 in. 3 mm)
	pulse duration, 1/2 sine wave		Width		5.75	5 in. 5 mm)
Non-Operational	40 G's, 15 msec.		Depth) in.
	pulse duration 1/2		Sopul		0.00	

Weight

(203 mm)

3.2 lbs. (1.45 kg)

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pulse duration, 1/2

sine wave

MINISCRIBE

PRODUCT MANUAL

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MiniScribe Corporation 1861 Lefthand Circle Longmont, Colorado 80501 (303) 651-6000

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PREFACE

This Product Manual, intended for use by engineers, designers, and planners, describes the design characteristics of the MiniScribe 3180E hard disk drives.

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3130/3180: KEY SELLING POINTS

- Half-Height form factor
 - Full-Height replacement
 - "Half-Height" capacity upgrade
- Interface flexibility
 - ESDI or SCSI with common HDA
- Performance
 - 17 msec average access time
 - 10 MBit/sec transfer rate (ESDI)
 - Up to 4 MB/sec (SCSI)
- Proven Design
 - Electronics: 9380
 - Mechanics: 3085
- High Volume capability
 - Proven design
 - Automated assembly
- Highest quality/reliability
 - 35,000 MTBF
 - Simple design: Low "part-count"

1.0 INTRODUCTION

The MiniScribe 3180E Series of disk drives are low cost, high capacity, high performance random access storage devices utilizing 5 1/4" thin film disks as storage media. Each disk surface employs one moveable head to access the data tracks. The 3180E Series features capacity of 182 megabytes (unformatted storage capacity). The 3180E disk drives utilize advanced 3380 Whitney-type head flexures and sliders which allow closer spacing of disks, allowing a higher number of disks in a standard 5 1/4" package.

High performance is achieved by the utilization of a rotary voice coil actuator, microprocessor control, and a closed loop servo positioning system. The closed loop servo system and dedicated servo surface combine to allow state-of-theart recording densities (1100 TPI) in a 5-1/4" package. The read/write heads, disk platters and actuator assembly are housed within a sealed enclosure containing a recirculating and breather filter to supply clean air exceeding Class 100 environment.

High quality mechanical construction with a sophisticated single printed circuit assembly allows for high MTBF (35,000 hours) and maintenance-free operation throughout the life of the drive.

The 3180E utilizes the industry standard ESDI compatible interface with a 10 megabit/second data transfer rate. It also supports hard and soft sectoring along with a range of ESDI standard options such as track offset, spindle motor sequencing, and initiation of drive diagnostics.

Other advantages of ESDI are data separation performed on drive, disk configuration data stored on drive along with a self-contained defect map, data encoded in (NRZ) rather than MFM, insuring higher data integrity over longer cable distances.

The 3180E uses size and shock mountings identical to the industry standard half height 5-1/4" mini-floppy mounting dimensions. It also uses the same DC voltages and connectors.

KEY FEATURES OF THE M9000E SERIES

- o Storage capacity of 156 mb (formatted).
- Identical physical size and mounting as standard 5 1/4"
 Winchester disk drives.
- Power supply requirements compatible with industry standard 5-1/4" fixed disk drives.
- o 18 msec. average access time (including settling).
- o 15 watt standby power requirement.
- o No adjustments necessary.
- o Fail-safe actuator lock at spin down or power failure.

- Dual chassis construction for protection during adverse operating conditions.
- Start up diagnostics.
- o Dedicated shipping zone.
- Single printed circuit board utilizing custom VLSI IC's and SMT.
- Thin film metallic media for higher bit density and resolution plus improved durability.
- o MTTR of less than 30 minutes.
- Hard or soft sectoring permits use with existing ESDI controller.

2.0 PRODUCT SPECIFICATIONS

2.1 MODEL SPECIFICATIONS

2.2

	<u>3180E</u>
Capacity (Unformatted): Number of Heads: Number of Cylinders Bytes per Track: Number of Disks: Type of Disk: Type of Head: Servo Head Transfer rate (Mbits/sec):	182 MB 7 1250 20832 4 sputtered composite 1 10
<pre>*Typical Formatted Capacities: Capacity Formatted: (ESDI) Sector size (bytes): Sectors/Track (1 spare): Number of Cylinders: *See Section 7.3.3 for Fixed Sector.</pre>	157 MB 512 35 1250
*See Section 7.3.3 for Fixed Sector. Recording Characteristics: BPI (Bits per Inch) TPI (Tracks per Inch) FCI (Flux Changes per Inch) Recording Code Rotational Speed Average Latency	20.1K 1135 13.4K 2,7 3600 rpm 8.33 msec
PERFORMANCE SPECIFICATIONS Data Transfer Rate Access Times	10.0 Mbits/second

(incl. settling time)*3.5 msec.Single Track3.5 msec.** Average (of all possible seeks)17 msec. typ1/3 Stroke Seek Time18 msec. maxFull Stroke Seek Time35 msec. maxRezero250 msec. max

Start time (typical) 20 seconds from power on to -Ready Stop time (typical) 15 seconds from power removal

*Not including command transfer overhead

2.3 POWER REQUIREMENTS

DC Voltage Input		
+12 Volts, DC Start Surge: Steady State:	<u>+</u> 5%, 1.1 amps (seeking). Max	during initial 15 sec. typical, 1.9 amps peak kimum ripple allowed is 1% t resistive load.
+5 Volts, DC <u>+</u> 5%, .6 amps typical Maximum ripple allow		equivalent resistive load.
AC Input	None required	
Power Dissipation	IDLE MODE SEEKING MODE	

2.4 PHYSICAL CHARACTERISTICS

Outline Dimensions 1.625 in. (41.3mm) H X 5.75 in. (146mm) W X 8.0 in. (203mm) L Mounting Dimensions See Figure 2-1 Weight 3.2 Pounds

2.5 ENVIRONMENTAL CHARACTERISTICS

Temperature

Operating	50 deg. F (10 deg. C) to 122 deg. F
(stabilized)	(50 deg. C)
Non-operating	-40 deg. F (-40 deg. C) to 140 deg. F
	(60 deg. C)
Thermal Gradient	18 deg. F/hr. (10 deg. C/hr.) max.

Humidity

Oper. and Non-operating8% to 80% (noncondensing)Maximum Wet Bulb78 deg. F (26 deg. C)Altitude (rel. to sea level)Operative-200 to 10,000 feetNon-operative40,000 feet

2.6 RELIABILITY AND MAINTENANCE

MTBF	35,000 POH
MTTR	30 minutes
Preventive Maint.	None
Comp. Design Life	5 years

Data Reliability 1 recoverable error in 10¹⁰ bits read 1 permanent error in 10¹² bits read (not recoverable in 16 reads) 1 seek error in 10⁶ seeks

Media defect criteria (as shipped from MiniScribe)

Maximum Defects* 2 bytes in length Cylinder zero defect free

*A single defect is defined as being less than 2 bytes long. A multiple defect is defined as 2 bytes or longer, or as a track with more than 1 single defect.

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2.7 SHOCK AND VIBRATION

Non-operational Shock	40 G's, 15 ms pulse duration, 1/2 sine wave
Non-operational Vibration	5 to 31 Hz, .01 in. peak to peak, 31 to 300 Hz, 1.0 G peak
Operational Shock	2.0 G's, 11 ms duration, 1/2 sine wave with no error rate degrada- tion. 10.0 G's, 11 ms duration, 1/2 sine wave with no permanent damage or loss of data
Operational Vibration	5 - 22 Hz, .01 in peak to peak, 22 to 300 Hz, .25 G peak acceler- ation

2.8 MAGNETIC FIELD

The externally induced magnetic flux density may not exceed 3 gauss as measured at the top of the drive.

2.9 ACOUSTIC NOISE

IDLE MODE	42	dBa	Sound	Pressure	Level
SEEKING MODE	50	dBa	Sound	Pressure	Level

2.10 SAFETY STANDARDS

The MiniScribe 3180E will comply with the following relevant product safety standards:

UL 478 CSA C22.2 No. 0-M1982 C22.2 No. 154-M1983 IEC/VDE DIN IEC 380 VDE 0806/8.81 FCC SUBPART J OF PART 15 FOR CLASS B COMPUTING DEVICES

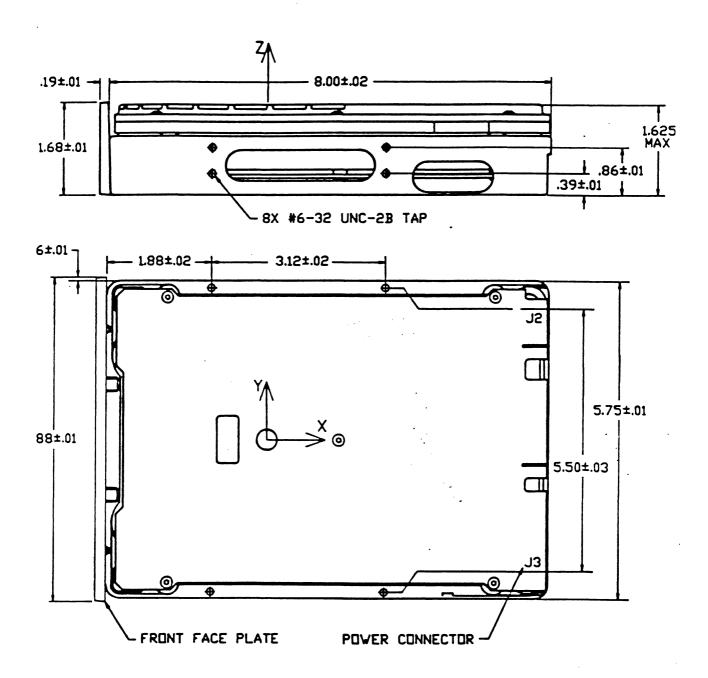
This equipment generates and uses radio frequency energy, and if not installed and used properly, that is, in strict accordance with manufacturer's instructions, may cause interference to radio and television reception. This product has been type-tested in a representative system, and found to comply with the limits for a Class B computing device in accordance with specifications in Subpart 2 of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference in a residential This does not imply that this product installation. guarantees FCC compliance in any given system. It is the responsibility of the installing systems manufacturer to insure system assembly EMC compliance. MiniScribe maintains product compliance regarding FCC requirements and will provide technical assistance in securing system product compliance where appropriate.

If the system equipment does cause interference to radio or television reception (this can be determined by turning the equipment off and on) the user is encouraged to try to correct the interference by using one or more of the following measures:

- Reorient the receiving antenna.
- Relocate the computer with respect to the receiver.
- o Move the computer away from the receiver.

It is recommended that shielded interface cable be used to ensure compliance with FCC emission limits.

Figure 2-1 OUTLINE AND MOUNTING DIMENSIONS



3.0 FUNCTIONAL CHARACTERISTICS

3.1 GENERAL THEORY OF OPERATION

The 3180E disk drive consists of read/write, control and ESDI interface electronics, read/write heads, a servo head, a head positioning actuator, thin film media and a patented air filtration system. These components perform the following functions:

- 1. Interpret and generate control signals
- 2. Position and maintain position over the desired track
- 3. Read and write data
- 4. Provide a contamination-free environment while performing all of the above functions.

3.2 READ/WRITE AND CONTROL ELECTRONICS

All the drive and interface electronics are packaged on a single printed circuit board, using Surface Mount Technology (SMT). Integrated circuits are mounted within the sealed enclosure of the head/disk assembly in close proximity to the read/write heads. Their functions are to provide head selection 0 through 6, read data preamplification, write data circuitry and servo data preamplification.

The microprocessor controlled printed circuit board contains the necessary electronic circuits to perform the following tasks:

- 1. read/writing of data
- 2. index detection
- 3. head positioning
- 4. head selection
- 5. drive selection
- 6. fault detection
- 7. voice coil actuator positioning
- 8. track 0 detection
- 9. recalibrate to track 0 on power-up
- 10. initiate diagnostics on power-up
- 11. track position counter
- 12. speed control for spindle drive motor
- 13. braking for the spindle drive motor
- 14. drive up-to-speed indication
- 15. monitoring for write fault conditions
- 16. controlling internal timings of the drive
- 17. generation of seek complete signals
- 18. data separation

3.3 3180E HEAD POSITIONING SYSTEM

The 3180E Read/Write heads are mounted on an integral rotary actuator assembly which is positioned by a voice coil motor. The voice coil, an integral part of the rotary actuator assembly, lies inside a magnet housing when installed in the drive. Current from the power amplifier, controlled by the servo system, causes a magnetic field in the voice coil which either aids or opposes the field around the permanent magnets. This reaction in turn causes the voice coil to move within the magnetic field. Since the heads are mounted to the voice coil, the voice coil movement is translated directly to the Read/Write heads and achieves positioning over the desired track/cylinder.

Rotary actuator movement is controlled by the servo feed back signal from the servo head. The servo head reads a dedicated surface where servo information is pre-written at the factory. This servo information serves as a control signal for the actuator to provide track-crossing signals during a seek operation, provide track-following signals during "on cylinder" operation and provide timing information such as index (start of a track) and servo clock.

3.4 HEADS AND DISKS

The 3180E employs composite Read/Write heads on Whitneystyle sliders and flexures to provide aerodynamic stability, superior head/disk compliance and a higher signal to noise ratio. Data on each of the data surfaces is read by one Read/Write head, each of which accesses 1250 tracks.

The 3180E employs sputtered thin film media with a 130mm diameter. The carbon overcoating formulation combined with the low load/low mass Whitney-style heads permits highly reliable contact start/stop operation. Thin film media yields high amplitude signals, and very high resolution performance compared to conventional oxide coated media. It also provides a high abrasion-resistant surface, decreasing the potential for damage caused by shipping and handling before installation.

A composite servo head reads servo data encoded at the factory on the dedicated servo disk surface.

3.5 SPINDLE DRIVE MECHANISM

A brushless DC drive motor located inside the spindle/hub assembly rotates the disk pack at 3600 RPM. The disk pack (including spindle, hub, disks, and motor) is dynamically balanced prior to installation to insure low vibration and servo stability.

Dynamic braking is employed to quickly stop the drive motor when power is removed.

3.6 AIR FILTRATION SYSTEM

The disks and Read/Write heads are assembled in an ultraclean air environment (Class 100 or better) and then sealed within the head disk assembly.

Within this sealed HDA a 0.1 micron filter provides constant internal air filtration. In addition, a breather filter provides a clean, equalized pressure between internal air and ambient to the HDA for the life of the drive.

3.7 AUTOMATIC CARRIAGE RETRACT AND LOCKING

If power is removed from the drive during a normal power down or in the event of a power failure, the actuator assembly will automatically retract and be locked in a nondata area located at the innermost portion of the disk. The heads will land on and take off from this area only.

3.8 FINE TRACK SAFETY SYSTEM

The 3180E Series drives utilize a fine track safety system which inhibits write operations if an excessive offtrack condition occurs. This aids in enhancing data reliability under extreme shock and vibration conditions that may exceed specified levels.

4.0 ELECTRICAL INTERFACE

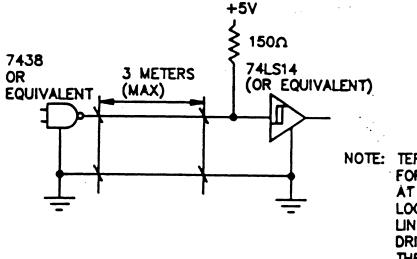
The MiniScribe 3180E is pin and function compatible with the serial mode of the Enhanced Small Device Interface (ESDI) for 5-1/4" Winchester Disk Drives. In the serial mode, interface signals (control, data and status) are transmitted serially via handshaking request/acknowledge signals.

The Enhanced Small Device Interface can be divided into three categories, each of which is physically separated:

- a. Control signals
- b. Data signals
- c. DC power

4.1 CONTROL SIGNAL DRIVERS AND RECEIVERS

All control lines are digital in nature (open collector TLL) and either provide signals to the drive (input) or signals to the host (output). Refer to Figure 4-1 for the control signal driver and receiver equivalent circuit and signal level specifications.



NOTE: TERMINATION RESISTORS FOR LINES ORIGINATING AT THE CONTROLLER ARE LOCATED IN LAST DRIVE. LINES ORIGINATING AT THE DRIVE ARE TERMINATED AT THE CONTROLLER.

The drivers have the following electrical specifications.

True/Active: False/Deactive: 0.0 VDC to 0.4 VDC @ 1 = -48 mA (Max.) 2.5 VDC to 5.25 VDC @ 1 = +250 uA (Open Collector)

Figure 4-1 CONTROL SIGNAL DRIVER AND RECEIVER CIRCUIT

4.2 DATA SIGNAL DRIVERS AND RECEIVERS

The data transfer signals are differential in nature and provide data either to (write) or from (read) the drive. Refer to Figure 4-2 for the data signal driver and receiver equivalent circuit.

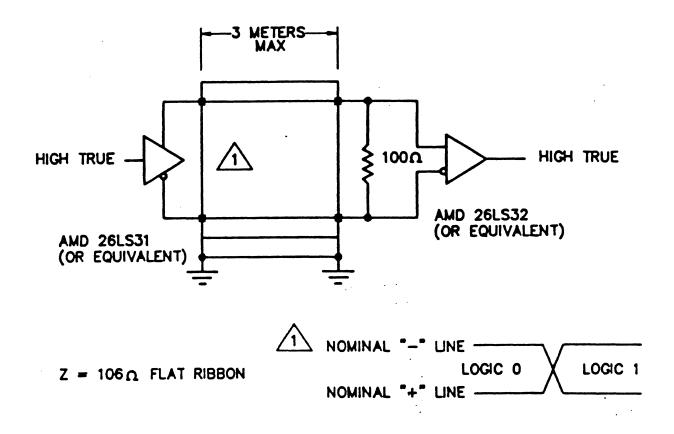


Figure 4-2 DATA SIGNAL DRIVER AND RECEIVER CIRCUIT

5.0 PHYSICAL INTERFACE

The electrical interface between the drive and the host controller is via four connects:

- a. J1 Control Signals (multiplexed)
- b. J2 Data Signals (radial)
- c. J3 DC Power Input
- d. Frame Ground

5.1 J1 CONNECTOR

J1 is a 34-pin board edge connector on the drive printed circuit board. The signals on this connector control the drive and transfer drive status to the host controller. The 34 pins are oriented with even pin numbers on the component side of the PCB. A key slot is provided between pins 4 and 6. See Figure 5-1 for connector dimensions and Section 7.2.2 for orientation and recommended types.

5.2 J2 CONNECTOR

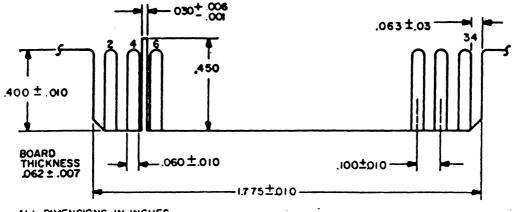
J2 is a 20-pin edge connector on the drive PCB. The signals on this connector contain Read or Write data to be transferred between the drive and host controller. The 20 pins are oriented with even numbered pins 4 and 6. See Figure 5-2 for connector dimensions and Section 7.2.3 for orientation and recommended types.

5.3 J3 CONNECTOR

The DC power connector (J3) is a 4-pin connector. +5V and +12V is supplied to the drive via this connector. J3 pin assignments are shown in Figure 5-3. See Section 7.2.4 for recommended type.

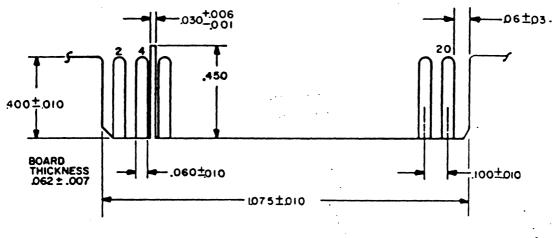
5.4 FRAME GROUND CONNECTOR

A frame ground connection is available through a fasten type connector. It is located on the shock mount frame and is isolated from the printed circuit board. See Section 7.2.5 for recommended types.



ALL DIMENSIONS IN INCHES

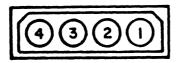
Figure 5-1 J1 CONNECTOR-CONTROL SIGNALS



ALL DIMENSIONS ARE ININCHES

•

Figure 5-2 J2 CONNECTOR-DATA SIGNALS



P3-I = +I2 VOLTS DC P3-2 = +I2 VOLTS GROUND RETURN P3-3 = +5 VOLTS GROUND RETURN P3-4 = +5 VOLTS DC

Figure 5-3 J3 CONNECTOR PIN ASSIGNMENTS

6.0 3180E ESDI-SERIAL MODE INTERFACE IMPLEMENTATION

This section describes the interface lines, hardware, and interface protocols necessary to implement the Serial mode disk version of the ESDI. Pin assignments for connectors J1 and J2 are shown in Tables 6-1 and 6-2.

Table 6-1 J1 CONTROL SIGNAL CONNECTOR PIN ASSIGNMENTS

J1 Co	nnector		
Signal	Ground	<u>Signal Name</u>	Source
2	1	-Head Select 23	Controller
4	3	-Head Select 2²	Controller
6	5	-Write Gate	Controller
8	7	-Configuration/Status Data	Drive
10	9	-Transfer Acknowledge	Drive
12	11	-Attention	Drive
14	13	-Head Select 2º	Controller
16	15	-Sector/AM Found	Drive
18	17	-Head Select 21	Controller
20	19	-Index	Drive
22	21	-Ready	Drive
24	23	-Transfer Request	Controller
26	25	-Drive Select 1	Controller
28	27	-Drive Select 2	Controller
30	29	-Drive Select 3	Controller
32	31	-Read Gate	Controller
34	33	-Command Data	Controller

Table 6-2 J2 DATA SIGNAL CONNECTOR PIN ASSIGNMENTS

J2 (Connector		
Signal	Ground	Signal Name	Source
1	-	-Drive Selected	Drive
2	-	-Sector/AM Found	Drive
3	-	-Command Complete	Drive
4	-	-Address Mark Enable	Controller
5	6	(Reserved)	
7	6	+Write Clock	Controller
8	6	-Write Clock	Controller
9	-	(Reserved)	
10	12	+Read/Reference Clock	Drive
11	12	-Read/Reference Clock	Drive
13	15	+NRZ Write Data	Controller
14	16	-NRZ Write Data	Controller
17	19	+NRZ Read Data	Drive
18	-	-NRZ Read Data	Drive
20	-	-Index	Drive

6.1 CONTROL INPUT LINES

The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are Write Gate, Read Gate, Head Select 2, Head Select 2, Head Select 2, Head Select 2, Transfer Req and Command Data. The signals to do the multiplexing are Drive Select 1, Drive Select 2, and Drive Select 3.

Two removable 150 ohm resistor packs (RP4 and RP17) are used for control input line termination. See Section 7.3.4 for details.

Address Mark Enable is a control input in the radial cable. It is not multiplexed.

6.1.1 DRIVE SELECT

in

in

out

in

in

in

Three Drive Select lines are to be decoded to determine the drive select address. Drive select jumper J15 consists of 3 jumpers which are configured by the user to represent a binary address (1-7). See Figure 7-3 for J15 locations and Table 6-3 for address jumper configurations.

J15 Drive Select ŝ 1 <u>Binary Address</u> 2 Address 0 0 out 0115 out 0 No Select 0 0 in 1 1 out cut 0 2 in 1 0 out out 0 1 3 out in in 1 in out out 1 0 0 4 1 1 0 5 in out in

1

1

Table 6-3 J15 DRIVE SELECT JUMPERS 1,2,3

6.1.2 HEAD SELECT 2°, 2¹, 2², AND 2³

1

1

These four lines allow selection of each individual read/write head in a binary coded sequence. Head Select 2° is the least significant line. Heads are numbered 0 through 6. When all Head Select lines are high (inactive), head 0 will be selected.

0

1

6

7

Addressing more heads than contained in the drive will result in a write fault when attempting to perform a write operation.

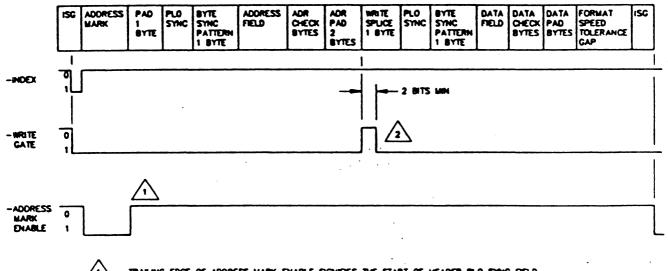
A 150 chm resistor pack allows for line termination.

6.1.3 WRITE GATE

/ <u>2</u>`

The active state of this signal enables write data to be written on the disk.

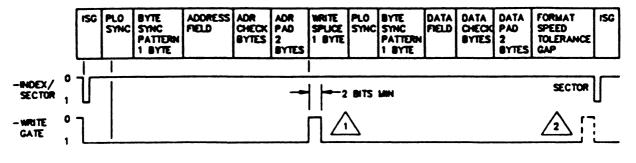
The high-to-low transition of this signal creates a write splice which is immediately followed by the PLO Sync field. See Figures 6-1 and 6-2. When formatting, Write Gate should be deactivated for 2 bit times minimum between the address field and the data field to identify to the drive the beginning of the data PLO Sync field. This line shall be protected from terminator power loss by implementation of an equivalent circuit shown in Figure 6-3.



TRAILING EDGE OF ADDRESS WARK ENABLE SIGNIFIES THE START OF HEADER PLO SYNC FIELD.

TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE.

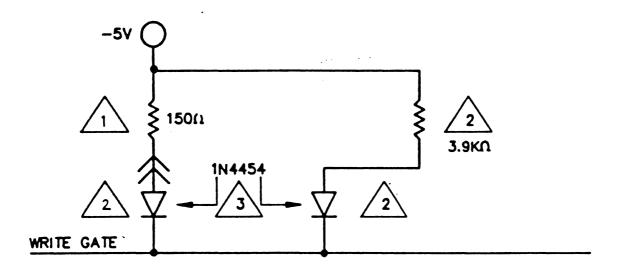
Figure 6-1 SOFT SECTOR ADDRESS MARK, WRITE GATE, PLO SYNC FORMAT TIMING



NOTES:

 $\frac{1}{2}$ transition required only if the disk is read after a format and prior to a data field write update.

Figure 6-2 FIXED SECTOR, WRITE GATE, PLO SYNC FORMAT TIMING



 $\frac{1}{1}$ PART OF THE TERMINATOR RESISTOR PACK IN THR LAST DRIVE OF THE DAISY CHAIN.

> Figure 6-3 WRITE GATE TERMINATION CIRCUIT

6.1.4 READ GATE

The active state of this signal, or low level, enables data to be read from the disk. This signal should become active only during a PLO Sync field and at least the number of bytes defined by the drive prior to the ID or Date Sync Bytes. The PLO Sync field length can be determined by the response to the Request PLO Sync Field Length command. Read Gate must be false when passing over a write splice area.

A 150 ohm resistor pack allows for line termination.

6.1.5 COMMAND DATA

When presenting a command, 16 information bits of serial data, plus parity, will be presented on this line. This data is to be controlled by the handshake protocol with signals Transfer Req and Transfer Ack. Upon receipt of this serial data, the drive will perform the required function as specified by the bit configuration.

Data is transmitted MSB first. See Table 6-4 for the meaning of the various bit combinations. See Figure 6-4 for timing.

No communications should be attempted unless the Command Complete line is true. NOTE: This line must be a logic 0 when not in use.

A 150 ohm resistor pack allows for line termination.

Table 6-4 COMMAND DATA WORD STRUCTURE AND DEFINITION

Mos† Sigr Bit	-	cant										Si	gni		ast ant Bit	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	P
CMD	FUN	ICTIO	N	CMD	MOD	IFI	ER			AL	LΖ	ERO	S			P
CMD	FUN	ICTIO	N			C	MD	PAR	AME	TER						P
BIT	Ρ.	PARI	TY	(000)												

COMMAND DATA WORD STRUCTURE

COMMAND DATA DEFINITION

CMD FUNCTION BIT		ION	CMD FUNCTION DEFINITION	CMD MODIF APPLIC	CMD PARAM APPLIC	STATUS/CONF DATA RTN			
<u>15</u>	14	<u>13</u>	<u>12</u>		<u>(BITS 11-8)</u>	(BITS 11-0)			
0	0	0	0	Seek	No	No Yes			
0	Ò	0	1	Recalibrate	No	No	No		
0	c	1	0	Request Status	Yes	No	Yes		
0	0	1	1	Request Conf.	Yes	No	Yes		
0	1	0	0	Select Hd Group	No	Yes	No		
0	1	0	1	Control	Yes	No	No		
0	1	1	0	Data Strobe Offs.	Yes	No	No		
0	1	1	1	Trk Offset	Yes	No	No		
1	0	0	0	Initiate Diag.	No	Yes	No		
1	0	0	1	Set Bytes per Sec	. No	Yes	No		
1	0	1	0	Reserved					
1	0	1	1	Reserved					
1	1	0	0	Reserved					
1	1	0	1	Reserved					
1	1	1	0	Set Conf.					
1	1	1	1	Reserved					
NOT	ES:	1.	All	unused or not ap	plicable low	ver order bi	ts must be		

NOTES: 1. All unused or not applicable lower order bits must be zero.

2. Any "Reserved" or command function received shall be treated as an invalid.

- 6.1.5.1 COMMAND DATA BITS 15 THROUGH 12 DECODE DEFINITION
 - a. Seek (0000)

This command causes the drive to seek to the cylinder indicated in bits 0 through 11. A Seek command will restore track offset to zero.

b. Recalibrate (0001)

This command causes the actuator to return to cylinder 0000. A Recalibrate command will restore track offset to zero.

c. Request Status (0010)

This command causes the drive to send 16 bits (see Table 6-5) of standard or vendor unique status information to the controller as determined by the command modifier bits. The parity utilized in all status responses shall be odd.

Request Standard Status

When the command modifier bits (11-8) of the Request Status command is 0000, the drive will respond with 16 bits of standard status. Bits 15-12 of this status are defined as state bits which do cause Attention to be asserted. Bits 11-0 of this status are fault or change of status bits that cause Attention to be asserted each time one is set. See Section 6.2.3.2 for response protocol and format of the status response from the drive.

Request Vendor Unique status

When the command modifier bits (11-8) of the Request Status command is 0001 through 1111, the drive responds with vendor unique status. Upon notification that vendor unique status is available, the drive will return one word of unique status as shown in Table 6-6.

Table 6-5 STATUS RESPONSE BITS

Bit		Att
15	Reserved	0
14	1=Removable media not present	0
	0=If not removable	0
13	1=Write protected - removable media	0
	0=If not removable	0
12	1=Write protected - fixed media	0
11	Reserved	0
10	Reserved	0
9	1=Spindle motor stopped by stop command	0
	<pre>1=Spindle motor stopped for other (e.g. power on, reset)</pre>	1
8	1=Power on reset conditions exist (reconf. or	
	restart Spindle motor command may be required)	1
7	1=Command data parity fault	
6	1=Interface fault	1
5	1=Invalid or unimplemented command fault	1
4	1=Seek fault	1
3	1=Write gate with track offset fault	1
2	1=Vendor unique status available	VD
1	1=Write fault*	1
0	1=Removable media changed (has been changed since	
	last status request)	1

*Conditions that can cause write fault are:

- Write current in a head without Write Gate asserted or no a. write current with Write Gate asserted and the drive selected.
- Multiple heads selected, no head selected, or improperly b. selected with Write Gate asserted.
- Simultaneous assertion of Read Gate and Write Gate. c.
- d. DC voltages grossly out of tolerance with Write Gate asserted.
- No write data transitions with Write Gate active. e.
- f. Open or shorted heads.
- Offtrack condition with Write Gate asserted. g.

Table 6-6 VENDOR UNIQUE STATUS WORDS

Word	Description
00	Microprocessor RAM error
01	Microprocessor ROM checksum error
02	Interface chip diagnostic failure
03	Sector counter fault
04	Index pulse not detected or lost
05	Spin speed not within 0.5% tol
06	Loss of fine track during idle mode
07	Reserved
08 08	Time out on +End Decel signal (during seek)
09	Time cut on CYL Pulse (during seek)
0 A	Overshoot (after a seek)
OB	Time out on fine track (after a seek)
00	Track zero signal not detected (after a seek)
OD	Comparator mismatch (after a seek)
0 E	Comparator mismatch (during a seek)
OF	Unexpected interrupt from processor
10	Time out on non-GB pattern (during a rezero)
11	Time out on GB1 pattern (during a rezero)
12	Time out on GB2 pattern (during a rezerc)
13	Seek range error
14	Voltage unsafe
15	Track offset fault
15	Write fault
17	Reserved
18	Time out on +End Decel (during a rezero)
19	Time out on CYL Pulse (during a rezero)
1A	Overshoot (after a rezero)
1B	Time out on fine track (after a rezero)
1C	Track 0 signal not detected (after a rezero)
1D	Comparator mismatch (after a rezero)
1E	Reserved
1F	6301 trap
30	Time out on non-GB pattern (adj)
31	Time out on GB1 pattern (adj)
32	Time out on GB2 pattern (adj)
39	Time out on CYL Pulse (adj)
3E	Cannot adjust servo

d. Request Configuration (0011)

This command causes the drive to send 16 bits (Tables 6-7 and 6-8) of configuration data to the controller. The parity utilized in all configuration responses shall be odd. The specific configuration requested is specified by bits 11-8 of the command as shown in Table 6-9.

Table 6-7 CONFIGURATION RESPONSE BITS

	Most										Le	ast					
	Sig	Significant Signifi										ic	icant				
	Bit										1	Bit					
		14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Р
	Bit																
Posit	ion		F	unct	ion											P	esponse
	15		0	= M	agne	tic	Dis	k D	riv	e						Ō	
	14		F	orma	t Sp	eed	Tol	era	nce	Ga	p R	equ	ire	eđ		0	
	13		Т	rack	Off	set	Opt	ion	Av	ail	abl	e				1	
	12		D	ata	Stro	be C	ffs	et	Opt	ion	Av	ail	ab]	e		0	
	11					l Sp			_							Ō	
	10		Т	rans	fer	Rate	>	10	Mhz							0	
	9		Ţ	rans	fer	Rate	•	5	Mhz		< =	10	M	ΩZ		1	
	8		Т	rans	fer	Rate	<=	5 M	hz							0	
	7		R	emov	able	Car	tri	dqe	Dr	ive						0	
	5			ixed				-								1	
	5		S	pind	le M	lotor	· Co	ntr	ol	Opt	ion	Im	ple	mer	nteð	X	jumper
	4			-		ch T				_			-			0	5 1
	3		R	LL E	ncođ	ed (Not	MF	M)							1	
	2					r So				eđ	(Ad	dre	SS	Mar	(년)	x	jumper
	1					ored									- ,	x	jumper
	ō		R	eser	ved		. –		-							0	J

* Command Complete shall be negated with 15 usec. of a head change if this bit is set to 1.

Table 6-8 CONFIGURATION RESPONSES

1

v

COM MODIFIER BITS CONFIGURATION RESPONSE	
<u>11</u> <u>10</u> <u>9</u> <u>8</u>	
0 0 0 1 Number of cylinders - Fixe	ed (1250)
0 0 1 0 Number of cylinders - Remo 0 0 1 1 Number of Heads	oved Media (0)
0 0 1 1 Number of Heads	
Bits 15-8 Removable driv Bits 7-0 Fixed heads (7)	
0 1 0 0 Min. unformatted bytes per	r track (20832)
0 1 0 1 Min. unformatted bytes per	
sec. only) See Note #2	
0 1 1 0 Number of sectors per trac	ck (hard sector
only)	
Bits 15-8 Reserved (0)	
Bits 7-0 bytes per ISG	(16)
1 0 0 0 Min. bytes per PLO sync fi	
Bits 15-8 Reserved (0)	
Bits 7-0 bytes per PLO s	sync field
required when READ GATE	
1 0 0 1 Number of words of vendor	unique status
available	-
Bits 15-8 Reserved (0)	
Bits 7-0 Number of vendo	or unique status
words (1)	-
1 0 1 0	
through Reserved (0)	
1 1 1 0	
1 1 1 1 Vendor Identification (20))

NOTE:

The number of unformatted bytes per sector as well as the number of sectors per track is dependent on the sector configuration Jumpers J12, J13 and J19 (refer to Section 7.3.3).

Table 6-9 REQUEST CONFIGURATION MODIFIER BITS

COM	Modifier	Bits		Function
11	10	9	<u>8</u>	
Ō	0	0	Û	General Configuration of Drive and format
Ņ,	<u>Ņ</u>	Û	1	Number of cylinders fixed
Û	0	1	Ũ	Number of cylinders, removable
0	Q	1	1	Number of heads
Û	1	Ū	0	Minimum unformatted bytes per track
Ũ	1	0	1	Unformatted byte per sector (hard sector only)
Q	1	1	<u> </u>	Sector per track (hard sector only)
Ũ	1	1	1	Minimum bytes in ISG field
1	0	0	0	Minimum bytes per PLO sync field
1	0	Û	1	Number of words of vendor unique status available
1	1	1	1	Vendor identification

e. Vendor Identification (1111)

Bits 15-8 identify the vendor. The vendor identification code for MiniScribe is 14 hex. (1101)

f. Control (0101)

This command causes the control operations specified by bits 11-8 to be performed as shown in Table 6-10.

The spindle motor control option is available only when the drive is jumper configured for that option. If the drive is not jumper configured for the spindle motor control option and a stop or start spindle command is issued, the drive will respond with invalid command fault. Refer to Figure 7-2 for the location of the spindle motor control option Jumper J7.

Table 6-10 CONTROL COMMAND MODIFIER BITS

COM 11	Modifier <u>10</u>	Bits <u>9</u>	8	Function
0	0	0	0	Reset interface attention and standard status (Bits 0-11)
0	0	0	1	Reserved
0	0	1	0	Stop spindle motor (only when J7 is installed)
0	0	1	1	Start spindle motor
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	x	X	X	Reserved

g. Track Offset (0111)

This optional command causes the drive to perform a track offset in the direction and amount specified by bits 11-8 as shown in Table 6-11. Only one offset in either direction is supported.

When a track offset command is issued, Command Complete will be inactive for approximately 2.5 msec to allow for settling. A track offset command will inhibit any attempted write operations to the drive. If a write is attempted with track offset a write gate with track offset fault will be reported.

Table 6-11 TRACK OFFSET COMMAND MODIFIER BITS

COM	Modifie	er Bits		Function
<u>11</u>	<u>10</u>	<u>9</u>	<u>8</u>	
0	0	0	0	Restore offset to 0
0	0	0	1	Restore offset to 0
0	0	1	0	Positive offset 1
0	0	1	1	Negative offset 1
NOTE	:: ;	Seek an	d Reca	alibrate command restore offsets to zero.

h. Initiate Diagnostics (1000)

This optional command with a command of zero causes the drive to perform internal diagnostics. Command Complete indicates the completion of the diagnostics. Attention with Command Complete indicates that a fault was encountered and status should be requested to determine the proper course of action.

i. Set Unformatted Bytes per Sector (1001)

The set bytes per sector option is available only when the drive is jumper configured for hard sector operation. If the drive is jumper configured for soft sectored operation, an invalid command fault will be reported if a set bytes per sector command is issued. The range of allowed number of unformatted bytes per sector in the command parameter is between 162 and 4095 bytes in one byte increments. If the number of bytes in the command parameter is not within the range of 162 and 4095 bytes, then the drive will respond with an invalid command fault.

6.1.6 TRANSFER REQUEST (TRANSFER REQ)

This line functions as a handshake signal in conjunction with Transfer Ack during command configuration/status transfers. See Figures 6-4 and 6-5 for timing.

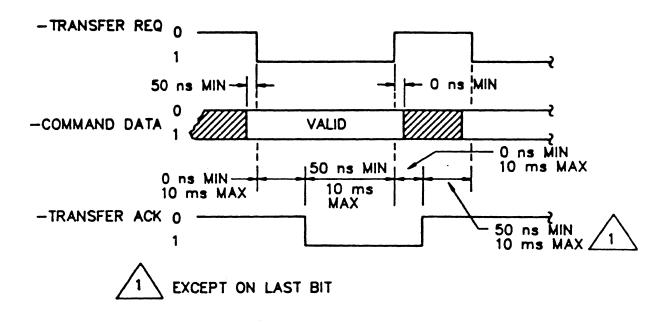


Figure 6-4 ONE BIT TRANSFER TIMING TO DRIVE

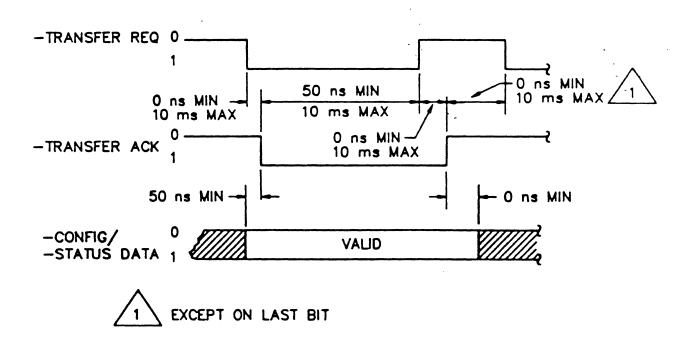


Figure 6-5 ONE BIT TRANSFER TIMING FROM DRIVE

6.1.7 ADDRESS MARK ENABLE (SOFT SECTORED MODE)

This signal, when active with Write Gate, causes an Address Mark to be written. Address Mark Enable shall be active for 24 bit times. See Figure 6-6 for timing.

Address Mark Enable, when active without Write Gate or Read Gate, causes a search for Address Marks. See Figure 6-2.

The trailing edge of Address Mark Enable with Write Gate true indicates the beginning of the PLO sync field.

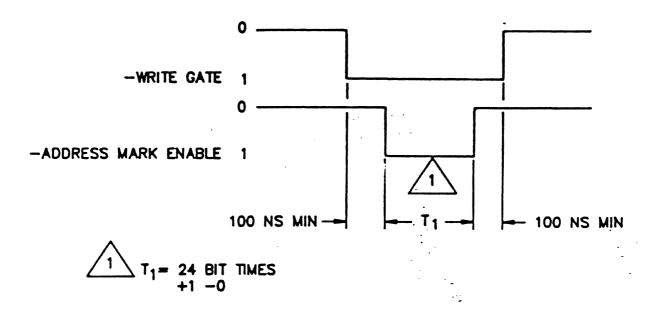


Figure 6-6 WRITE ADDRESS MARK TIMING

6.2 CONTROL OUTPUT LINES

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48 mA at low level or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and collector leakage current is a maximum of 250 uA.

All J1 output lines are enabled by their respective Drive Select decodes.

6.2.1 DRIVE SELECTED

A status line provided at the J2/P2 connector to inform the host system of the selection status of the drive. The Drive Selected line is driven by a TTL open collector driver as shown in Figure 4-1. This signal will go active only when the drive is selected as defined in Section 6.2.2. The Drive Select lines at J1/P1 are activated by the host system.

6.2.2 READY

This signal indicates that the spindle is up to speed. This interface signal when true, together with Command Complete indicates that the drive is ready to read, write or seek. When the line is false, all writing and seeking is inhibited.

6.2.3 CONFIGURATION/STATUS (CONFIG/STATUS) DATA

The drive presents serial data on this line upon request from the controller. See Figure 6-7 for typical operation. This configuration status serial data will be presented to the interface and transferred using the hand-shake protocol with signals Transfer Req and Transfer Ack. See Figure 6-5. Once initiated, 16 bits plus parity will be transmitted MSB first. The parity utilized shall be odd.

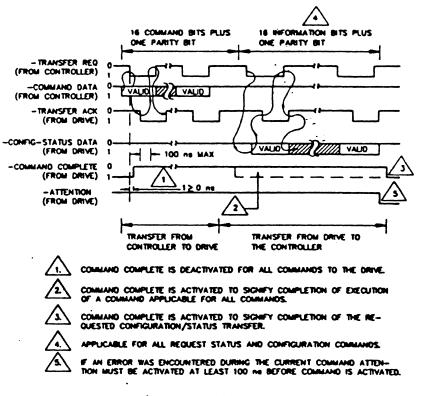


Figure 6-7 TYPICAL SERIAL OPS

6.2.3.1 CONFIGURATION RESPONSE BITS

In response to the Request Configuration command (see Section 6.1.5.1) 16 bits of configuration information is returned to the controller. There shall be no invalid response made to a Request Configuration command. General configuration response flags must be used to verify the validity of the responses.

6.2.3.1.1 GENERAL CONFIGURATION RESPONSE BITS

> If the command modifier bits (11-8) were 0000, the general configuration status information shown in Table 6-7 is returned.

> If other command modifier bits were used, the specific configuration status information shown in Table 6-8 is returned for each configuration command with those modifiers.

> Upon notification that vendor unique status is available, the drive product will return one word of unique status as shown in Table 6-6

6.2.3.2 STATUS RESPONSE BITS

In response to the Request Status command (see Section 6.1.5.1), 16 bits of status information is returned to the controller. Refer to Table 6-5.

Bits 15-12 of the status are defined as state bits which do not cause Attention to be asserted. Bits 11-0 are fault or change of status bits that cause Attention to be asserted.

6.2.4 TRANSFER ACKNOWLEDGE (TRANSFER ACK)

This signal functions as a hand-shake signal along with TRANSFER REQ during COMMAND and CONFIGURATION-STATUS transfers. See Figures 6-5 and 6-6.

6.2.5 ATTENTION

This output is asserted when the drive wants the controller to request its standard status. Generally, this is a result of a fault condition or a change of status. Writing is inhibited when ATTENTION is asserted. ATTENTION is deactivated by the Reset Interface Attention command (see Section 6.1.5.1).

6.2.6 INDEX

This pulse is provided by the drive once each revolution to indicate the beginning of a track. This signal is high and makes the transition to low to indicate INDEX. Only the transition at the leading edge of the pulse is accurately controlled. The period (T) of this signal is the reciprocal of the rotational speed, Figure 6-10. This signal is available on the command cable J1/P1 (gated) and on the data cable J2/P2 (ungated).

6.2.7 SECTOR/ADDRESS MARK FOUND

These two signals are mutually exclusive and therefore share this line. The signal that is used is determined by the NRZ data transfer control implementation. These signals are available on the command data J1/P1 (gated) and on the data cable J2/P2 (ungated).

6.2.7.1 SECTOR (DRIVE HARD SECTORED)

This interface signal indicates the start of a sector. The leading edge of the sector pulses is the only edge that is accurately controlled. The index pulse indicates sector zero. See Figure 6-8.

6.2.7.2 ADDRESS MARK FOUND (CONTROLLER SOFT SECTORED)

> This signal indicates the detection of the end of an address mark. See Figure 6-9 for timing.

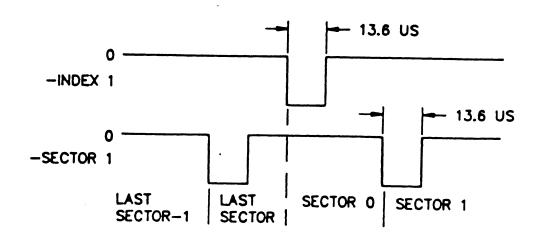


Figure 6-8 SECTOR PULSE TIMING

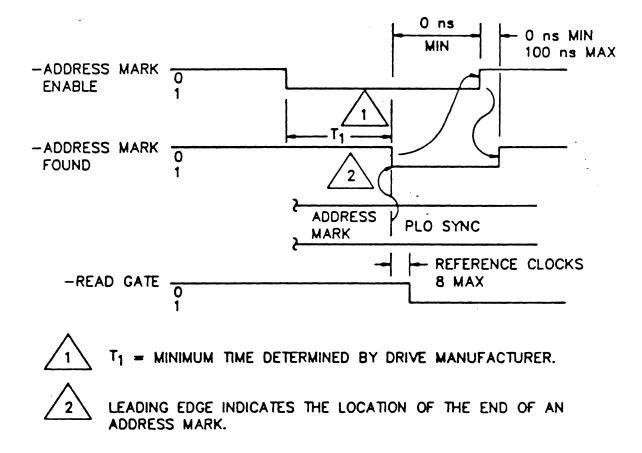


Figure 6-9 READ ADDRESS MARK TIMING

6.2.8 COMMAND COMPLETE

Command Complete is a status line provided at the J2/P2 connector. This is an ungated output from the drive which allows the host to monitor the drive's Command Complete status, during overlapped commands, without selecting the drive. This signal line will go false in the following cases:

- a. A recalibration sequence is initiated (by drive logic) at power on if the Read/Write heads are not over track zero.
- b. Upon receipt of the first Command Data bit, Command Complete will stay false during the entire command sequence.

This signal is driven by an open collector driver as shown in Figure 4-1.

6.3 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Four pair of balanced signals are used for the transfer of data and clock: NRZ Write Data, NRZ Read Data, Write Clock, and Read/Reference Clock. Figure 4-2 illustrates the recommended driver/receiver circuit.

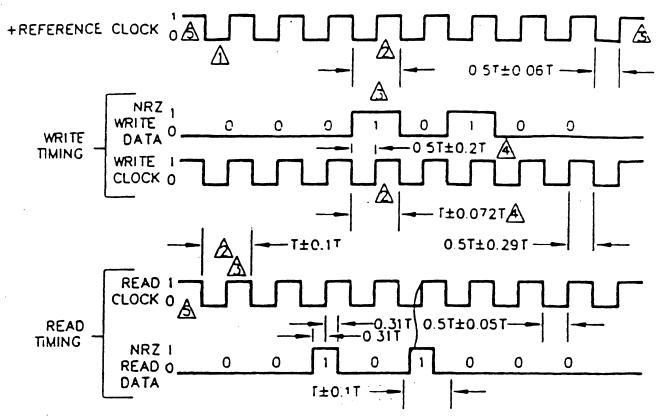
6.3.1 NRZ WRITE DATA

This is a differential pair that defines the data to be written on the track. This data will be clocked by the Write Clock signal. See Figure 6-10 for timing.

6.3.2 NRZ READ DATA

The data recovered by reading previously written information is transmitted to the host system via the differential pair of NRZ Read Data lines. This data is clocked by the Read Clock signal. See Figure 6-10 for timing. These lines will be held at a zero level until PLO sync has been obtained and data is valid.

Figure 6-10 NRZ READ/WRITE DATA TIMINGS



NOTES

- A ALL TIMES IN NS MEASURED AT 1/0 CONNECTOR OF THE DRIVE. T IS THE PERIOD OF THE CLOCK SIGNALS AND IS THE INVERSE OF THE REFERENCE OR READ CLOCK FREQUENCY.
- A SIMILAR PERIOD SYMMETRY SHALL BE IN ±4 NS BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
- ▲ EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES SHALL NOT VARY MORE THAN -5.5% TO +5.0%. PHASE RELATIONSHIP BETWEEN REFERENCE CLOCK AND NRZ WRITE DATA OR WRITE CLOCK IS NOT DEFINED.
- THE WRITE CLOCK MUST BE THE SAME FREQUENCY AS THE DRIVE SUPPLIED REFERENCE CLOCK (I.E. THE WRITE CLOCK IS THE CONTROLLER RECEIVED AND RETRANSMITTED DRIVE REFERENCE CLOCK.)
- A REFERENCE CLOCK IS VALID WHEN READ GATE IS INACTIVE. READ CLOCK IS VALID WHEN READ GATE IS ACTIVE AND PLG SYNCHRONIZATION HAS BEEN ESTABLISHED.

6.3.3 READ/REFERENCE CLOCK

The timing diagram as shown in Figure 6-10 depicts the necessary sequence of events (with associated timing restrictions for proper read/write operation of the drive). The Read/Reference Clock is a glitchless clock with a maximum of two missing clock pulses when switching from reference to read clock.

6.3.4 WRITE CLOCK

Write Clock is provided by the controller. This clock frequency shall be dictated by the Read/-Reference Clock during the write operation. See Figure 6-10 for timing.

Write Clock need not be continuously supplied to the drive. Write Clock should be supplied before beginning a write operation and should last for the duration of the write operation.

6.4 READ, WRITE, AND FORMAT PARAMETERS

6.4.1 GENERAL SUMMARY OF CRITICAL READ-FUNCTION TIMING PARAMETERS

Controller variations of the read timing are allowed if the following drive-dependent parameters are met:

a. Read Initialization Time

A read operation must not be initiated until 8 usec. following a head change.

b. Read-Gate Timing

Read Gate must not be enabled or true during a Write Splice area (Read Gate must be deactivated one bit time minimum before a Write Splice and must be enabled one bit time minimum after a Write Splice area).

c. Read Propagation Delay

Data (read) at the interface is delayed by approximately 6 bit times from the data recorded on the disk media. d. Read Clock Timing

Read Clock and Read Data are valid within the number of PLO sync field bytes specified by the drive configuration after Read Enable and PLO sync field is encountered. The Read/Reference Clock line may contain no transitions for up to 2 Reference Clock periods when switching from a write to a read. The transition period will also be 1/2 of a Reference Clock period minimum with no shortened pulse widths.

6.4.2 GENERAL SUMMARY OF CRITICAL WRITE-FUNCTION PARAMETERS

Controller timing variations in the record-update function are allowed if the following drive-dependent write (and interrelated read) timing parameters are met:

a. Read-to-Write Recovery Time

Assuming head selection is stabilized the time lapse from deactivating Read Gate to activating Write Gate shall be 5 Reference Clock periods minimum.

b. Write Clock-to-Write Gate Timing

Write Clocks must precede Write Gate by a minimum of 2-1/2 Reference Clock periods.

c. Write Driver Plus Data-Encoder Turn-On Write Gate

The Write Driver Plus Data-Encoded Turn-On Time (write splice width) is between 3 and 7 Reference Clock periods.

d. Write-Driver Turn-Off from Write Gate

To account for data-encoding delays, Write Gate must be held on for at least 2 byte times after the last bit of the information to be recorded.

e. Write-to-Read Recovery Time

The time lapse before Read Gate or Address Mark Enable can be activated after deactivating the Write Gate is defined by the "ISG Bytes after Index/Sector" in configuration data response.

f. Head Switching Time

Write Gate may not be activated until 8 usec. after a head change and Command complete is true.

Write Gate must be deactivated at least 1 usec. before a head change.

g. Reference Clocks Valid Time

The Read/Reference Clock lines will contain valid Reference Clocks within two Reference Clock periods after the deactivation of Read Gate. Pulse widths will not be shortened during the after switching from a read to write but clock transitions may not occur for up to 2 Reference Clock periods.

h. Read Clocks Valid Time

The Read/Reference Clock line will contain valid Read clocks within 2 clock periods after PLO synchronization is established. Pulse widths will not be shortened during the Reference Clock to Read Clock transition time, but missing clocks may occur for up to 2 clock periods.

i. Write Propagation Delay

Write Data received at the I/O connector will be delayed by the Write Data Encoder by up to 8 bit times maximum prior to being recorded on the media.

6.4.3 FIXED SECTOR IMPLEMENTATION

6.4.3.1 FORMAT RULES

The Index and Sector pulses are available for use by the controller to indicate the beginning of a track and to define the beginning of a sector. A suggested format for fixed data records is shown in Figure 6-11.

FUED SECTOR "N" IDENTICAL SECTORS

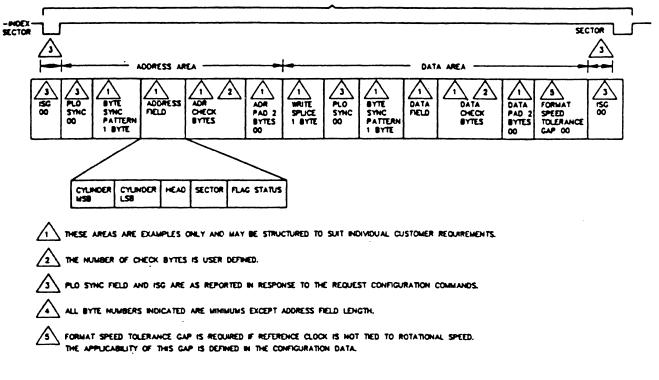


Figure 6-11 FIXED SECTOR FORMAT

6.4.3.2 INTERSECTOR GAP (ISG)

The minimum Intersector Gap size is determined from the configuration data. The Intersector Gap provides separation between each sector. The gap size is chosen to provide for:

- a. Drive required Write-to-Read recovery time (minimum time between deassertion of Write Gate and assertion of Read Gate).
- b. Drive required head switching time.
- c. Control decision making time between sectors.
- d. Variations in detecting Index and Sector.

6.4.3.3 ADDRESS AREA

The address area (Figure 6-11) provides a positive indication of the track and sector locations. The address area is normally read by the controller and the address bytes verified prior to a data

area read or write. The address area is normally only written by the controller during a format function and thereafter only read to provide a positive indication of the sector location and establish the boundaries of the data area. The address area consists of the following bytes.

a. PLO Sync Field

These bytes are required by the drive to allow the drive's read-data phaselocked oscillator to become phase and frequency synchronized with the data bits recorded on the media. The controller must send NRZ 00's during this time.

b. Byte Sync Pattern (1 Byte Minimum)

This byte establishes byte synchronization (i.e. the ability to partition this ensuing serial bit stream into meaningful information groupings such bytes) and indicates to as the controller the beginning of the address field information. It is recommended that the Byte Sync Pattern contain more than a single 1 bit for a greater confidence level of detection.

c. Address Field

These bytes are user-defined and interpreted by the user's controller. A suggested format consists of 5 bytes, which allows 2 bytes to define the head address, 1 byte to define the sector address and 1 byte to define flag status.

d. ADR Check Bytes (Address Field Check Codes)

An appropriate error-detection mechanism is generated by the controller and applied to the address for dataintegrity purposes. These codes are written on the media at format time. Data integrity is maintained by the controller recalculating and verifying the address-field check codes when the address field is read. ADR check bytes are user defined. e. ADR Pad (2 Bytes Minimum) (Address Field Pad)

The address Field Pad bytes must be written by the controller and are required by the drive to ensure proper recording and recovery of the last bits of the address-field check codes. These pad bytes should be 00's.

6.4.3.4 DATA AREA

The Data Area (Figure 6-10) is used to record data fields. The contents of the data fields within the Data Area are specified by the host system. The remaining parts of the Data Area are specified and interpreted by the disk controller to recover the data fields and ensure their integrity. The Data Areas consist of:

a. Write Splice (1 Byte Minimum)

This byte area is required by the drive to allow time for the write drivers to turn on and reach recording amplitude sufficient to ensure data recovery. This byte should be allowed for in the format, and the controller should send 00's during this byte time.

b. PLO Sync Bytes

These bytes are required when reading to allow the drive's phase-locked oscillator to become phase and frequency synchronized with the data bits recorded in the media. The controller must send NRZ 00's during these byte times.

c. Byte Sync Pattern (1 Byte Minimum)

This byte establishes byte synchronization and indicates, to the controller, the beginning of the data field. It is recommended that this byte contain more than a single one bit.

d. Data Field

The data field contains the host system's data files.

e. Data Check Bytes

The Data Check or Error Check Code bytes are generated by the controller and written on the media at the end of the Data Field. Data integrity is maintained by the controller recalculating and verifying the Data Field Check Codes or applying error correction algorithms, if applicable, when the Data Field is read. The Data Check Field is user defined, but should have a correction span of 6 bits or greater.

f. Data Pad (2 Bytes Minimum)

The Data Field Pad bytes must be issued by the controller and is required by the drive to ensure proper recording and recovery of the last bits of the data field check codes. The controller should send 00's during these byte times.

6.4.3.5 FIXED SECTOR, WRITE GATE, PLO SYNC FORMAT TIMING

See Figure 6-2

6.4.4 ADDRESS MARK IMPLEMENTATION (CONTROLLER SOFT SECTORED)

This section is included as an example to give meaning to the definitions given.

6.4.4.1 FORMAT RULES

The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors.

6.4.4.2 SOFT SECTORED FORMAT

The format shown below in Figure 6-12 is similar to the format commonly used for hard sectored disk drives and indicates minimum requirements.

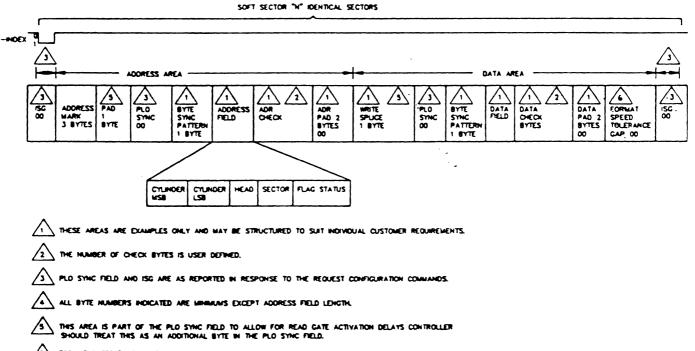
This format is a soft sectored type of sector which means that the beginning of each sector is defined by an ID Address Mark followed by a prewritten identification (ID) field which contains the logical sector address plus cylinder and head information. The ID field is then followed by a user supplied data field.

The definitions of the functional areas shown in the soft sectored format are identical to those described for the hard sectored format. There are some additional fields in this format and they are the Address Mark Field, Address Mark Pad, and ISG.

6.4.4.3 ADDRESS MARK FIELD

The address mark field is a field 3 bytes long and is found before the PLO sync field in and the address area. The contents of this 3 byte field is drive dependent and is written by the drive when so commanded by Write Gate and Address Mark Enable active simultaneously.

Detection of Address Mark indicates the location of the beginning of a sector.



FORMAT SPEED TOLERANCE GAP IS REQUIRED IF REFERENCE CLOCK IS NOT THED TO ROTATIONAL SPEED. THE APPLICABILITY OF THIS GAP IS DEFINED IN THE CONFIGURATION DATA.

Figure 6-12 SOFT SECTORED FORMAT

6.4.4.4 ADDRESS MARK PAD

The Address Mark Pad byte follows the Address Mark field and is to be considered a part of the PLO sync field. Its purpose is to allow for Read Gate activation delays after detecting the Address Mark Found signal.

6.4.4.5 INTERSECTOR GAP (ISG)

The ISG is included in the format to allow for all those items discussed in Section 6.4.3.2.

6.4.4.6 SOFT SECTORED ADDRESS MARK, WRITE GATE, PLO SYNC FORMAT TIMING

> This timing is mainly to support the unique encoding for PLO sync field. The beginning of each PLO sync field must be specified by the controller. The beginning of the header PLO sync field will be specified by the trailing edge of the Address Mark Enable signal when Write Gate is true. See Figure 6-1.

6.5 DEFECT LIST

The 3180 series drives are shipped with a defect list that is written in the ESDI Rev. F recommended format.

The defect list resides on Sector 0 of cylinder 1249 and is repeated on cylinder 1241. This allows for redundancy should an error occur on the maximum cylinder. The Sector 0 or any surface will contain the defects for that surface. The format for the data field portion (see Figure 6-13) of this sector is 256 bytes with 2 bytes of CRC (x16 = 12 = x5= 1):

Defect locations are 5 bytes long and the bytes are defined in Figure 6-13.

The start of the actual defect may be off by up to 7 bits due to the one byte resolution.

The end of the defect list for each surface will be indicated by 5 bytes of ones in the defect location field or the end of the sector. The CRC check bytes should be used if that capability exists but may be ignored if multiple reads are a more desirable approach. CRC seed is zero. (Initialized state)*.

Byte count is the number of Bytes from Index.

*Sync byte will be included in the CRC calculation.

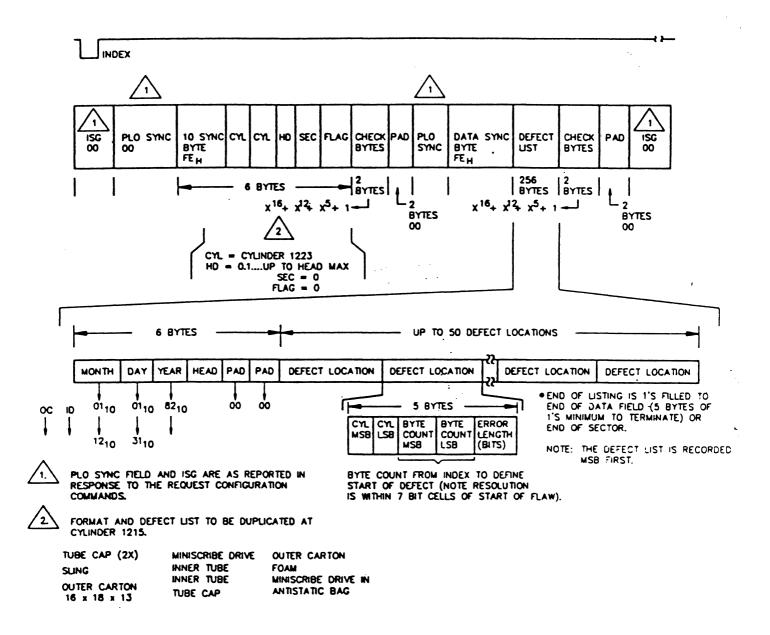


Figure 6-13 DEFECT LIST FORMAT

7.0 INSTALLATION

INTRODUCTION

This installation section is intended for the customer to install the MiniScribe Drive 3180E in minimal time. The section includes explanation of all pertinent jumpers as well as unpacking instructions. It also includes a diagnostic user's guide. This will aid the customer in running diagnostics and explaining any error codes that may occur.

CAUTION/WARNING

THE MINISCRIBE DRIVE IS A PRECISION PRODUCT. DURING HANDLING THE PRODUCT MUST NOT BE DROPPED, JARRED, OR BUMPED, OTHERWISE DAMAGE TO THE HEADS AND DISKS MAY OCCUR. THE STAND ALONE DRIVE IS SENSITIVE TO ELECTRO-STATIC DISCHARGE (ESD). PROPER ESD PRECAUTIONS (PERSONNEL AND EQUIPMENT GROUNDING) ARE REQUIRED PRIOR TO UNPACKING OR HANDLING THE FAILURE TO FOLLOW THESE PRECAUTIONS DRIVE. COULD LEAD TO AN IMMEDIATE CATASTROPHIC DRIVE FAILURE OR A PREMATURE RELIABILITY FAILURE. WHEN THE DRIVE IS REMOVED FROM THE MINISCRIBE SHIPPING CONTAINER AND NOT IMMEDIATELY SECURED WITHIN A CHASSIS THROUGH ITS SHOCK IT MUST BE STORED ON A PADDED, MOUNTS, GROUNDED, ANTISTATIC SURFACE.

FAILURE TO COMPLY WITH THE ABOVE PROCEDURE WILL RENDER NULL AND VOID ALL WARRANTIES.

7.1 UNPACKING AND INSPECTION

7.1.1 SINGLE PACK

Retain the packing materials for reuse. Refer to Figure 7-1 for the following steps.

- STEP 1: Inspect the shipping container for evidence of damage in transit. If damage is evident, notify the carrier immediately.
- STEP 2: Open the outer carton by carefully cutting the tape on the top of the carton.
- STEP 3: Lift the inner carton out of the outer carton and remove the outer end foam cushions.
- STEP 4: Open the inner carton by carefully cutting the tape on the top of the carton.

- STEP 5: Lift the drive from the inner carton and remove the inner end foam cushions and cardboard wrap.
- STEP 6: Place the pair of end cushions, the cardboard wrap, and the inner carton within the outer carton and store for subsequent reuse.
- STEP 7: Inspect the drive for shipping damage, loose screws or components and correct, if possible. If damage is evident without noticeable damage to the shipping cartons, notify MiniScribe immediately for drive disposition.

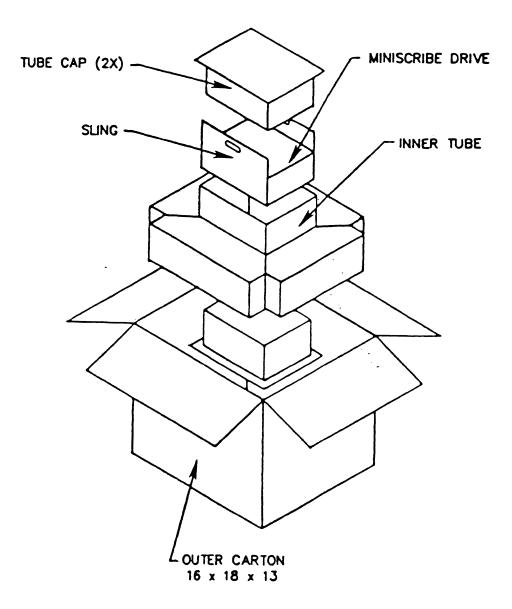


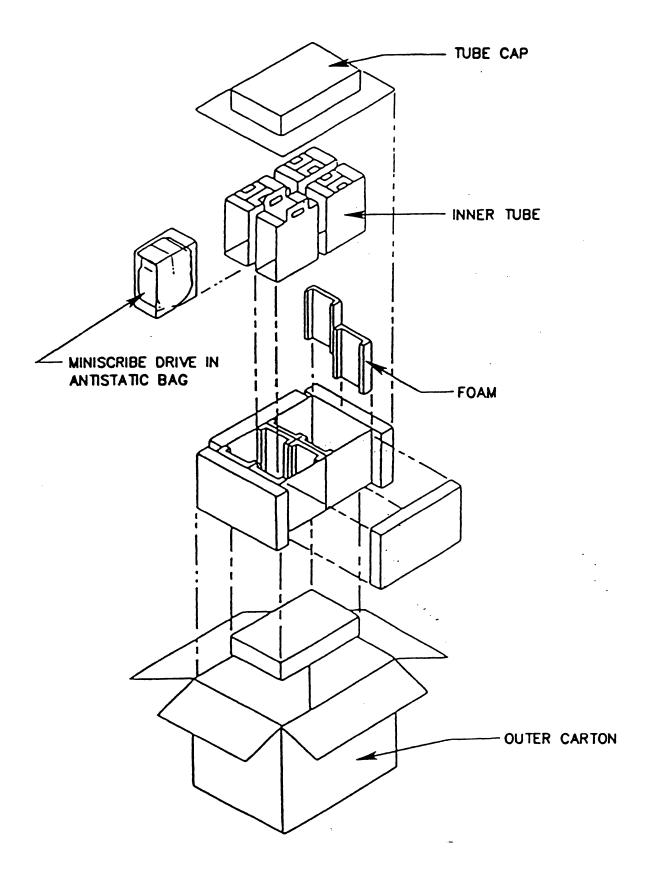
Figure 7-1 SINGLE PACK SHIPPING CONTAINER

7.1.2 MULTIPACK

Retain the packing materials for reuse. Refer to Figure 7-2 for the following steps.

- STEP 1: Inspect the shipping container for evidence of damage in transit. If damage is evident, notify the carrier immediately.
- STEP 2: Remove banding from container and shrink wrap if used.
- STEP 3: Lift off upper cap and outer sleeve surrounding the multipacks.
- STEP 4: Open each multipack carton and remove foam cap to access drives.
- STEP 5: Remove each drive from the carton by the tabs on each cardboard sleeve containing them.
- STEP 6: Take each drive from cardboard sleeve and remove from anti-static bag.
- STEP 7: Place the drive on a protective foam pad and inspect the drive for shipping damage, loose screws or components and correct, if possible. If damage is evident without noticeable damage to the shipping carton, notify MiniScribe immediately for drive disposition.
- STEP 8: Once all the drives have been removed from the shipping carton and the cardboard sleeves have been returned to the slots in the foam, replace foam cap and store for reuse.
- STEP 9: When using a multipack carton for reshipping, it is not to be shipped unless secured to a standard size wood pallet of 40" X 48".

Figure 7-2 MULTIPACK SHIPPING CONTAINER



7.1.3 REPACKING

Should the MiniScribe drive require shipment, repack the drive using the MiniScribe packing materials and follow the steps in Section 7.1.1 or 7.1.2 in reverse order.

NOTICE

THE MINISCRIBE DRIVE WARRANTY IS VOID IF THE DRIVE IS RETURNED TO MINISCRIBE IN OTHER THAN THE STANDARD MINISCRIBE SHIPPING CARTON PACKED IN ACCORDANCE WITH THE ENCLOSED PROCEDURE.

7.2 PHYSICAL INTERFACE

The electrical interface between the MiniScribe 3180E and the host system is accomplished via four connectors: J1, J2. J3 and ground spade connection. The connectors and their recommended mating connectors are described below. Also refer to Section 5.0.

7.2.1 POWER AND INTERFACE CABLES AND CONNECTORS

Figure 7-3 shows locations of the power and interface connectors. Pin assignments for J1, J2 and J3 are listed in Section 6.1.

The interface connection is made through connectors J1 and J2 on the 3180E printed circuit board. The control cable interconnects the controller and J1; the data cable interconnects the controller and J2. See Figure 7-5 for J1 and J2 orientation.

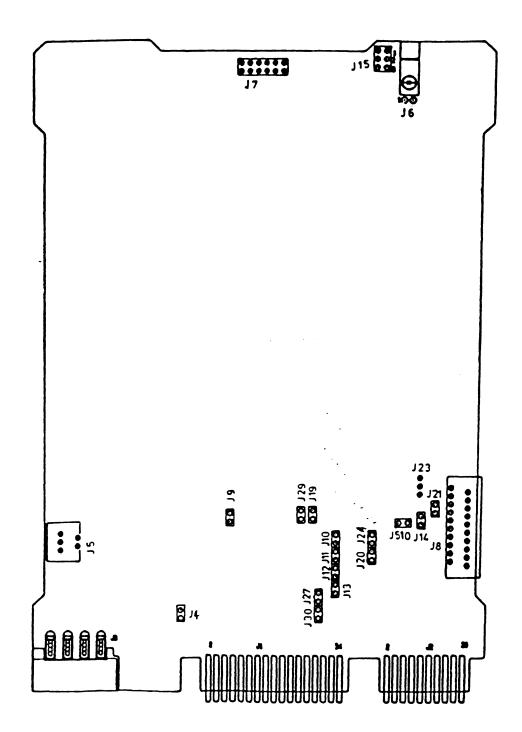
7.2.2 CONTROL SIGNAL CONNECTOR J1

J1 is a 34-pin board edge connector on the drive printed circuit board. The signals on this connector control the drive and transfer drive status to the host controller. A key slot is provided between pins 4 and 6.

Recommended mating connector: AMP ribbon connector 88373-3, or equivalent (key slot between pins 4 and 6).

Recommended cable: 3M Scotchplex 3365/34 or equivalent.

Figure 7-3 OPTION JUMPER, TERMINATOR, AND CONNECTOR LOCATIONS



7-6

7.2.3 DATA TRANSFER CONNECTOR J2

J2 is a 20-pin board connector on the printed circuit board. The signals on this connector contain read or write data. A key slot is provided between pins 4 and 6.

Recommended mating connector: AMP ribbon connector 88373-6 or equivalent.

Recommended cable: 3M Scotchflex 3365-20, or equivalent (keyslot between pins 4 and 6).

7.2.4 DC POWER CONNECTOR - J3

J3 is a 4-pin keyed connector on the printed circuit board. DC power (+5V and +12V) is supplied to the drive via this connector.

Recommended connector: AMP 350543-1 Pins: AMP pin 350078-4

Note:1 Equivalents of the above are permissible Note:2 Suggested wire size: 18 AWG

7.2.5 FRAME GROUND CONNECTOR

The frame ground connector is a fasten-type connection. If wire is used, the hole in the connector will accommodate wire size of 18 AWG max.

Recommended mating connector: AMP pin 61761-2, or equivalent

7.3 3180E DRIVE OPTIONS

7.3.1 DRIVE ADDRESSING AND INTERFACE TERMINATION

Figure 7-3 shows the locations of the three J15 drive address jumpers for drive address selection (drive address 1 through 7) and interface terminators RP4 and RP17 on the printed circuit board. Only one drive address jumper is installed on a 3180E drive, and the drive is addressed as Drive 1 at the factory. See Table 6-1 Drive Addressing. See Table 6-3 for drive address configurations and Section 6.1.1 for more information.

Terminator packs RP4 and RP17 provide proper termination for interface lines. When daisy chaining multiple 3180E drives, the terminators are installed only in the last drive on the daisy chain.

7.3.2 SPINDLE CONTROL OPTION

Refer to Section 6.1.5.1F. Jumper J4 selects the spindle control option. See Figure 7-3 for location.

- When J4 is installed, the 3180E must wait for a start spindle command to start the spindle motor.
- When J4 is NOT installed, the drive automatically starts the spindle motor at power on.

7.3.3 SECTOR CONFIGURATION OPTIONS

The 3180 series can operate in either hard or soft sector modes. Figure 7-3 shows the locations of Jumpers J12, J13, J19.

JUMPER J19 SELECTS HARD OR SOFT SECTORING MODE.

- When J19, J13 and J14 are installed, the drive is configured to operate in soft sectored mode. ADDRESS MARK GENERATION and DETECTION are enabled, and the SECTOR/ADDRESS MARK FOUND interface signal is used to report ADDRESS MARK FOUND.
- When J19 is NOT installed, the drive is configured to operate in the hard sectored mode. The SECTOR/ADDRESS MARK FOUND interface signal is used to transmit sector pulses to the host controller. The number of bytes/sector may be specified using the SET BYTES PER SECTOR command or by selecting a default sector configuration with option Jumpers J12 and J13. Three fixed sectored and one soft sectored format is available as shown in Table 7-1. Also refer to Sections 6.1.5.11, 6.1.7, 6.2.7.

7.3.4 DAISY CHAINING THE MINISCRIBE 3180E DRIVES

Up to seven 3180E drives may be connected to a single host controller/formatter. Control signals at J1 are transmitted via standard, daisy-chain interconnection. Data signals at J2 are transmitted via radially connected data-transfer lines. Figure 7-4 shows connections for a system configuration using multiple 3180E drives.

Note: Interface terminators RP4 and RP17 are installed only in the last physical drive in the control chain. Maximum number of drives = 7.

Table 7-1 SECTOR CONFIGURATION JUMPERS

Sector <u>Configuration</u>	<u>J19</u>	<u>J12</u>	<u>J13</u>	Unformatted Bytes <u>Per Sector</u>	Formatted Bytes <u>Per Sector</u>	Number of <u>Sectors</u>
Soft	on	on	on	Soft sectored	mode	
Fixed	off	on	off	612	512	34
Fixed	off	off	on	578	512	36
Fixed	off	off	off	594	512	35

For all sector configurations, the configuration response given is as follows:

Minimum Bytes per ISG Field16 bytesISG Bytes after Index/sector12 bytesMinimum Bytes per PLO Sync Field14 bytes (12 bytes in 36 sector mode)

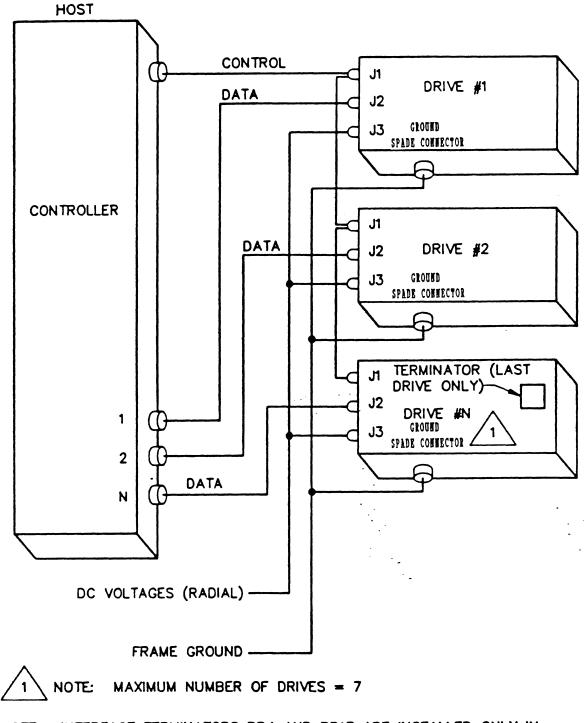
7.4 MOUNTING ORIENTATION

The MiniScribe 3180E uses industry-standard mounting for 5-1/4" Winchester Disk Drives (the same as for 5-1/4" flexible disk drives). See Figure 2-1. The 3180E is designed to be used in applications where the unit may experience shock and vibration at greater levels than larger and heavier disk drives. The drive may be mounted in any attitude.

The 3180E is mounted using 6-32 UNC screws 1/4" maximum penetration. The customer must allow adequate ventilation to the drive to insure reliable operation.

In as much as the drive frame acts as a heat sink to dissipate heat from the unit, the enclosure and mounting structure should be designed to allow natural convection of heat around the HDA and outer frame. If the enclosure is small or if natural convection is restricted, a fan may be required.

Figure 7-4 DAISY CHAINING THE MINISCRIBE 3180E DRIVES



NOTE: INTERFACE TERMINATORS RP4 AND RP17 ARE INSTALLED ONLY IN THE LAST PHYSICAL DRIVE IN THE CONTROL CHAIN. MAXIMUM NUMBER OF DRIVES = 7.

7.5 CABLING

Attach interface cables with connectors P1, P2, P3 and ground connector to J1, J2, J3 and ground spade connector, respectively. (See Figure 7-5). Insure that connectors P1 and P2 have keys installed as indicated in Figures 5-1 and 5-2. If multiple drives are to be interconnected, remove the terminator packs in all but the last drive in the daisy chain. Refer to Figure 7-3 for terminator locations and Figure 7-4 for cable inter-connections for multiple drive systems.

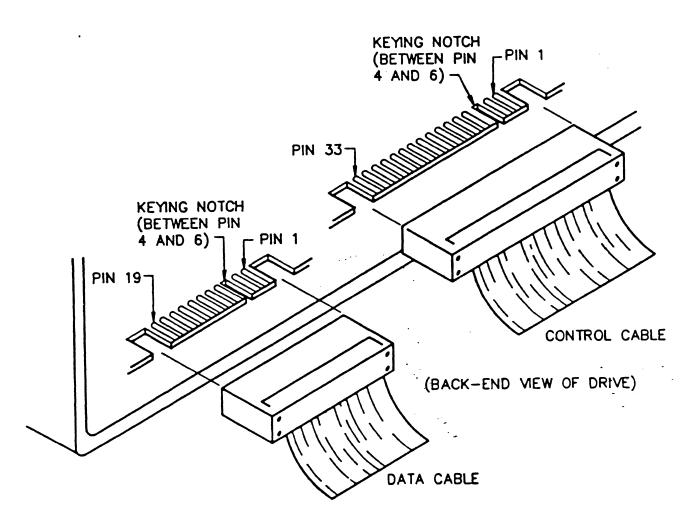


Figure 7-5 CONNECTOR ORIENTATION

7.6 DIAGNOSTICS

7.6.1 DIAGNOSTIC MODE

This section covers the Exercise mode for the MiniScribe 3180E. Error identification and error message definitions are also included.

Error codes are displayed in a "morse-code" type manner. Flashes or bits are interpreted and converted into a hexadecimal error code. "Zeroes" are indicated by a short (1/2 second) flashing mode. "Ones" are indicated by a short (1/2 second) continuous "on" mode. Error codes are separated by a one-second LED "off" time. All error codes and the revision level are 6 bits long. Zero = 1/2 second "flashing" mode One = 1/2 second "continuous" on mode Between Bits = 1/2 second off Between repeat cycles (words) = 1.0 second off "1A" 011010 EXAMPLE: 0 1/2 sec FLASHING 1/2 sec OFF 1/2 sec ON 1 1/2 sec OFF $1 \quad 1/2 \text{ sec ON}$ 1/2 sec OFF 0 1/2 sec FLASHING 1/2 sec OFF 1 1/2 sec ON 1/2 sec OFF 0 1/2 sec FLASHING

1.0 sec OFF

Listed below are the binary to hexadecimal conversion values:

00	000000	10	010000	30	110000
01	000001	11	010001	31	110001
02	000010	12	010010	32	110010
03	000011	13	010011	39	111001
04	000100	14	010100	3E	111110
05	000101	15	010101		
06	000110	16	010110		
07	000111	17	010111		
80	001000	18	011000		
09	001001	19	011001		
0A	001010	1A	011010		
OВ	001011	1B	011011		
0C	001100	1C	011100		
OD	001101	1D	011101		
0E	001110	1E	011110		
OF	001111	1F	011111		

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