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Memorandum M 1547

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Date: 2-1-60

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

July 7, 1952

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SUBJECT: INITIAL DECISIONS ON WWIA BLOCK DIAGRAMS

To: WWIA Planning Group

From: W. A. Hosier

Abstract: Certain preliminary specifications are set forth as a basis for further work on WWIA system.

As a result of discussions held during the week of June 30, it has been agreed to proceed with block diagrams of WWIA on the following basis:

GENERAL:

Since the main purpose of WWIA is to test memory and other components, reliability and conservative design will be emphasized throughout. Also, since time is short and since it is essential that the great majority of circuits be circuits of proven and unquestioned reliability, it will be built as far as possible to begin with out of standard plug-in units or test equipment.

It will probably be desired eventually to interchange certain components - e.g. to try a transistor read amplifier for the memory or a transistor arithmetic element; the mechanical design should be such as to facilitate this.

Marginal checking will be provided. Probably no bus will be used.

MEMORY:

Magnetic core, metallic ribbon type, 32 x 32 = 1024 registers, 17 bits (16 carrying information and one parity check) Selection by 3 superimposed currents of relative magnitude (1/2, 0), (1/2, 0) and (0, -1/2) respectively. Vacuum tube drivers on each of the 3 "coordinates" selected by crystal matrix driver from FF's of Storage Switch.

Allowance should be made for the possibility that "read" and "rewrite" may not require complete

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switching of memory cores, thus making faster completion of these operations possible, but necessitating more complex driving equipment to distinguish between them and "clear and write".

**ARITHMETIC
ELEMENTS:**

A-Register, 17 FF's (1 for parity check), acts as buffer between memory and Accumulator, 16 FF's, a subtractor (This last to give unambiguous zero, and give better balance in number of gate tubes driven by 1 & 0 sides of Accumulator FF's) Other FF registers would probably include a program counter (10 bits), storage switch (10 bits) and control switch (not more than 6 bits).

**CONTROL AND
ORDER CODES:**

The code will not include either multiply or divide, since these orders contribute little or nothing to the testing of other components. Other orders are not entirely decided - first thoughts included:

- (1) The 8 orders ca, ad, su, ts, cp, cr, io, and sp or possibly cp (0), implemented WWI style with TPD and matrix. (Six bits would be available for order coding, though it may not be advisable to use them all).
- (2) The same orders implemented through an operation counter of the Jeffrey-Reed type described in E-462.
- (3) Six orders (presumably, through not necessarily, 6 of the above 8), one for each of the available order digits, implemented by simple gates.
- (4) Orders with interchangeable parts corresponding roughly to the ten alternatives of the first five order digits, combined in suitable ways to get at least the 8 orders mentioned above.

It was proposed to have each member of the group sketch out rough block diagrams of a computer based on one of the four listed order systems - K. Olsen drawing up No. (1), R. Jeffrey (2), W. Hosier (3), and R. Mayer (4). Possibly some test program such as N. Daggett's #697 would be programmed in each system to see how convenient the order code is.

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IN-OUT EQUIPMENT: The input will consist of a photoelectric tape reader; output of paper tape punch and type-writer, along with CRT display.

Signed

W. A. Hosier

W. A. Hosier

Approved

R. R. Everett

R. R. Everett

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