Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND II MEETING OF JULY 18, 1952

To: Whirlwind II Planning Group

From: N. H. Taylor and W. A. Hosier

Date: July 24, 1952

Members Present:

N. Alperin	T. Gates	D. Neville
H. Anderson	A. Guditz	W. Ogden
P. Baltzer	A. Heineck	R. Paul
D. Brown	W. Hosier	W. Papian
R. Callahan	R. Hughes	L. Piecha
J. Crane	J. Jacobs	H. Platt
R. DiNolfo	R. Jeffrey	F. Sandy
D. Eckl	R. Jenney	D. Shansky
M. Epstein	C. Kirk	H. Smead
R. Everett	W. Klein	L. Sutro
R. Farmer	C. LaSpina	N. Taylor
S. Fine	W. Linvill	S. Thompson
J. Forgie	R. Mayer	R. von Buelow
W. Frank	J. McCusker	C. Wieser

N. Taylor explained that the purpose of this meeting was to set forth such decisions and progress as have been made on the unnamed prototype computer, formerly referred to as WWIA, (since christened MTC, for Memory Test Computer). The Laboratory's purpose in constructing this computer was reviewed; since this has already been gone over in more detail in the minutes of the May 16th meeting, it will not be presented here. These minutes will be concerned, rather, with the aspects of the machine which have crystallized into proposals more definite than those mentioned at the earlier meeting or which have been changed since that meeting. Reference is also made to the note of July 7, 1952, "Initial Decisions on WWIA Block Diagrams", M-1547.

Space has already been allocated on the third floor of Whittemore 2 for assembly of the computer under the direction of K. H. Olsen and R. von Buelow; an idea of its anticipated physical size can be had from the skeleton assembly of eight-foot test racks already set up.

As now envisaged, it will actually be a working computer, although it will not have the orders "multiply" and "divide" built in. Carrying out the plan of the July 7th note, it is intended to construct the computer of standard test equipment as far as possible. Except for the magnetic memory, no circuits fundamentally different from those of WWI are likely to appear in the machine at first. However, new circuits now being worked on in other groups will be incorporated into the set-up in the course of time. One reason for starting with standard test equipment in this manner, N. Taylor has emphasized, is to keep the number of circuits of unproven reliability at a minimum. In this way, any difficulty occuring in testing a new circuit, such as the magnetic memory, can more easily be localized and assessed than it could if unpredictable failures were occuring in various circuits throughout the machine.

The block diagram which will probably be the basis for its logical design was originally sketched by R. Mayer. He explained the details of his proposed system, component by component, as follows:

Accumulator

The accumulator will have 16 flip-flops, will be able to shift (or cycle) right, and to subtract. This last, which is logically similar to adding, was chosen in preference to adding for two reasons: it does not give rise to negative ZERO, and the carry gates (which become borrow gates in a subtractor) are on the ZERO rather than the ONE side of the accumulator flip-flops, thus helping to balance the number of gate tubes on the two sides. In order to eliminate as many gate tubes as possible, the accumulator will have a low-speed carry circuit, using about a half-microsecond delay per digit, instead of an instantaneous high-speed carry of the type used in WWI.

A-Register

The A-register acts in general as an intermediary for most transfers taking place in the computer. Read-outs from the memory go first into this register. By reading (subtracting) its complement directly into the accumulator, it adds its content to that of the accumulator; if, on the other hand, it is first complemented and then read out, its content is subtracted from that of the accumulator. The last five digits of the A-register also operate as a subtracting counter when needed - for example, to count the number of shifts in a shift-right operation.

Reading out of the memory or the accumulator into the A-register initiates a "parity count" pulse for each ONE read in; these pulses, in chains of 8 at the most, move down the register toward the right with a delay of a half-microsecond per digit to two parity flip-flops, one of which is connected at the right of AR7, and the other at the right of AR15. These two flip-flops are thus the means of accomplishing a

Parity Count and Check

Let us review the point that the parity check, as installed and proved useful in WWI, consists of an extra digit associated with a word and stored with it in the memory to indicate whether the number of ONE's in the word is odd or even. Each parity flip-flop, initially set to ZERO, will read ONE or ZERO after the last pulse of the chain has reached it, depending on whether the number of ONE's in its half of the A-register was odd or even. After all the pulses from the A-register have arrived, a "parity count" pulse complements one of the parity flip-flops if, and only if, the other flip-flop contains a ONE, thus making the first flip-flop (which amounts to a 17th digit of the A-register) contain ONE or ZERO, depending on whether the total number of ONE's in the 16 digits of the A-register is odd or even. On a ts order, the content of this flip-flop is written into the 17th digit of the storage register containing the word. When this word is later read out of storage, the 17th digit is held aside while a parity count is performed on the other 16, and the result of the count is compared with the segregated 17th digit. If these two agree, the computer proceeds; if not, it stops and sounds an alarm.

This parity check circuit thus serves to detect any single digit which does not come out of the memory the same as it went in. It will of course fail to detect a change of two digits, but such a change is considered to be so improbable as to be negligible.

Memory

Salient features of the memory have been mentioned previously in the reports referred to above. Any significant elaborations or changes from those specifications are described below in the summary of W. N. Papian's remarks.

Program Counter

The program counter is not essentially different from that of WWI; it has 10 digits, can be cleared, and may be read into from the last 10 digits of the A-register on sp and cp orders. It reads out into the storage switch.

Terminal Equipment

Terminal equipment will consist of a photoelectric tape reader input and, as outputs, a typewriter, paper tape punch, and display oscilloscope. The decoders for the horizontal and vertical axes of the oscilloscope, instead of having their own driver flip-flops as in WWI, will be driven through a permanent connection by the A-register and accumulator flip-flops. This means that a pattern representing the operation of these registers can be seen at all times by turning up the scope intensity and may possibly prove useful in checking computer operation.

Interconnections

It was decided not to use a bus, thus dispensing with some of the gate tubes and drivers entailed by a bus. Further, since Burroughs flip-flops come equipped with read-in gates, it was decided to make use of these gates wherever possible, and one suggested way of doing this was to pipe the outputs of certain flip-flops (e. g., those of the A-register) hither and yon directly to the aforesaid gates.

Control

The control system, as set forth in R. Mayer's proposal, is probably the most distinguishing feature of the machine, apart from its memory. 6 digits are available to specify orders; this would, of course, make possible some 64 orders, much more than are either necessary or desirable. Mayer's system, instead of assigning an arbitrary 6-digit number to an order and using this to initiate appropriate command pulses through a switch, makes use of the fact that orders fall naturally into operational categories by virtue of including or not including a certain operation such as "clear accumulator" or "read out of memory", etc. To oversimplify somewhat, each of the 6 available order digits can be used to indicate whether or not a given operation is to be included as an element in an order, and orders are thus built up out of "standard parts" like constructions with a Meccano set. The following partial list of orders will serve to illustrate:

Use Storage:	ca, ad, su, ts	(Read out of storage: ca, ad, su (Read into storage: ts
Do Not Use Storage:	cr, sr, cp, sp, io	(Use shift: cr, sr (Read into Program Counter: sp, cp (Use terminal equipment: io

Closer inspection will show that this description, as remarked above, is an oversimplification. In many cases, a given order digit can represent the inclusion or exclusion of several different component operations, depending on the operations which have preceded it. The following diagram and complete list of orders will serve to clarify the system, particularly when used in conjunction with Mayer's block diagram SB-37330 and traffic schedule drawing SB-37331:

-- Control Digit --

1.	2.	3.	4.	5.	6.
1: Storage	1: In	1: 10 Digits	(Not Used)	1: Clear AC	(Not Used)
		0: 16 Digits			
	0: Out	1: Comp. AR	1. Display	0: Not	
		0: Not	0. Add		
0: No Storage	1: Subprogram	1: cp	1: Alarm	(Not used)	(Not used)
		0: sp	0: Not		
	0: Not	1: In from PETR	1: Out to tape, etc.	1: sr	1: Shift
		0: Not	0: Not	0: cr	0: Not

Equivalent in WWI orders -

100000: ad
100010: ca
100100: qd(V,H)
101000: su
101010: cs
110000: ts
110010: tc
110100: td
110110: tdc

100110: qd (O,H)
101100: qd (V,-H)
101110: qd (O,-H)

000001: cr
000011: sr
000101: cr/qp
000111: sr/qp
001001: qr/cr
001011: qr/sr
010000: sp
010100: rs(&sp)
011000: cp
011100: "ck"

000000 (address ≠0) halt
000000 (address =0) dummy

In the resulting combinations of control digits, certain orders on which one might not place much priority occur more or less gratis as by-products of the control system: for example, qd(V,-H) qd (0,H), tdc, etc. The order listed as "ck" is like a MMI program cp RC (rs), and will stop the computer if AC is negative.

No sign control will be used. There is only one reason why sign control is used in MMI for shift right, and that is to make the roundoff work correctly. The MTC has no roundoff and, therefore, needs no sign control. (Note that the sign digit, being shifted right, will fill up the "evacuated" flip-flops with (+) or (-) ZERO's as it should.) In-out orders are combined with sr or cr to accommodate 6-digit flexowriter tape.

If the 6 control digits come up ZERO and are followed by a non-ZERO address, the computer will try to execute "cycle right" but will halt instead; if, on the other hand, the address in this case is all ZERO's, the computer will simply pass on to the next instruction.

Under the title of Time Pulse Distributor, a flip-flop determines by its ZERO or ONE state whether the computer will embark on a program-timing or operation-timing cycle. At the end of each cycle, either of program-timing or of operation-timing, an "end-carry" pulse goes back through Test Control and, under normal circumstances complements the TPD flip-flop, initiating the alternate cycle. If it is desired to interrupt this course of events, appropriate switches may be opened in Test Control. For test purposes, a single pulse may then be returned by push button, or pulses synchronized with a test oscilloscope sweep may be fed in.

Test Storage

To read a program in initially, either one must have a special read-in order, which automatically issues the necessary sequence of commands, or one must have a read-in program "prewritten" into certain registers of the memory, usually referred to as Test Storage. It is felt that the latter approach will probably be simpler, at least with this machine. Various methods of achieving such "cold storage" have been proposed: one means, of course, is toggle switch storage, generally rejected as involving

too much equipment; the others all make use of the magnetic memory and involve writing ONE's en bloc throughout, say, 40 memory registers, certain digits of which would be prevented by preset mechanical means from actually switching to ONE. The mechanical means of inhibition could be a by-passed driving or sensing winding, a shorted turn, or a separate reset line which goes through selected cores in the negative direction. The reset line system has the advantage of freeing the Test Storage registers for general use once the read-in program has been completed.

W. N. Papian, for the benefit of the uninitiated, sketched a group of proposed features of the MTC memory which might otherwise be available only in scattered references. Metallic ribbon cores will be used: cores wound of 1/8 mil Mo-Permalloy ribbon, 1/8" wide, wrapped about 10 times around a hollow ceramic core of 1/8" outer diameter. These require 200 ma-turns at 20 mv to switch. The decision to use metallic cores rather than the ferrites proposed in the earlier notes is primarily a consequence of the manufacturers' ability to make more uniform metallic cores, thus requiring less time and effort for core testing and development. Secondary reasons are: First, the high current requirement of the ferrite cores (2.5 ampere turns) would necessitate larger driver tubes, such as 715's, instead of 7AD7's, which are adequate for metallic cores. Second, the hysteresis loops of present ferrite cores are not quite as rectangular and do not give quite such good selection ratios as those of the metallic cores. W. Papian estimates that a memory which could be developed in nine months out of metallic cores, starting now, would take eighteen months to develop with ferrites. D. R. Brown's group and Papian's section will, of course, continue to work on ferrites as a high priority undertaking.

A sample batch of 300 metallic cores will be delivered about July 22 for testing. If, as anticipated, these prove satisfactory, an order for the entire 20,000 will be placed for a delivery date of, hopefully, some time in September.

The cores will be driven by vacuum tubes (presumably 7AD7's). The complete switching time of a core under these conditions will be about 10 microseconds, giving a read-write time of about 20 microseconds. However, it has been found

unnecessary to switch the core completely in order to get a satisfactory read pulse. This means that, for the read and re-write cycle, the core need be only partially switched, traversing a smaller hysteresis loop and taking only 12 microseconds or so for the whole cycle. It is planned to drive and sense cores with single-turn windings, such as have been used on the experimental 256-core ferrite array. However, it may not be possible to support cores on interwoven driving wires in the manner of the ferrite array, because of the shape of the hole in the ceramic spool on which cores are wound. This hole, being long and narrow compared with the hole in the ferrite "cheerios", will not permit two straight wires to go through it unless they are nearly parallel. Various proposals have been advanced for packaging and wiring the array, such as, for example, to embed the cores in a plastic sheet with their axes normal to the sheet and possibly to thread all wires, or all wires except z-axis drive and sensing windings, as bundles or cables through stacked arrays of cores.

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