MOTOROLA

MVME050/D2

MVME050 System Controller Module and MVME701/MVME701A I/O Transition Module User's Manual

MICROSYSTEMS

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MOTOROLA

MVME050/D2

OCTOBER 1985

MVME050 SYSTEM CONTROLLER MODULE

AND

MVME701/MVME701A I/O TRANSITION MODULE

USER'S MANUAL

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERICAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE, IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

Second Edition

First Edition November 1984

MICROSYSTEMS

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Microsystems Warranty and Repair for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the MVME050 System Controller Module, MVME701 I/O Transition Module, and MVME701A I/O Transition Module. Throughout this manual these modules are referred to as controller module and I/O module. Typical modules are shown in Figure 1-1.

1.2 FEATURES

The features of the controller module and I/O module include:

- System controller functions:
  - 4-level priority bus arbiter
  - Power up reset/front panel reset
  - System clock and serial clock generators
  - Bus time-out generator
- Eight 28-pin sockets for EPROM/RAM
- Two RS-232C multiprotocol serial ports
- Centronics-type parallel printer port
- Time-of-day clock
- Global interrupter
- User-defined/controlled front panel display
- A32/A24: D8/D16/D32 VMEbus slave interface

1.3 SPECIFICATIONS

The controller module and I/O module specifications are identified in Table 1-1.

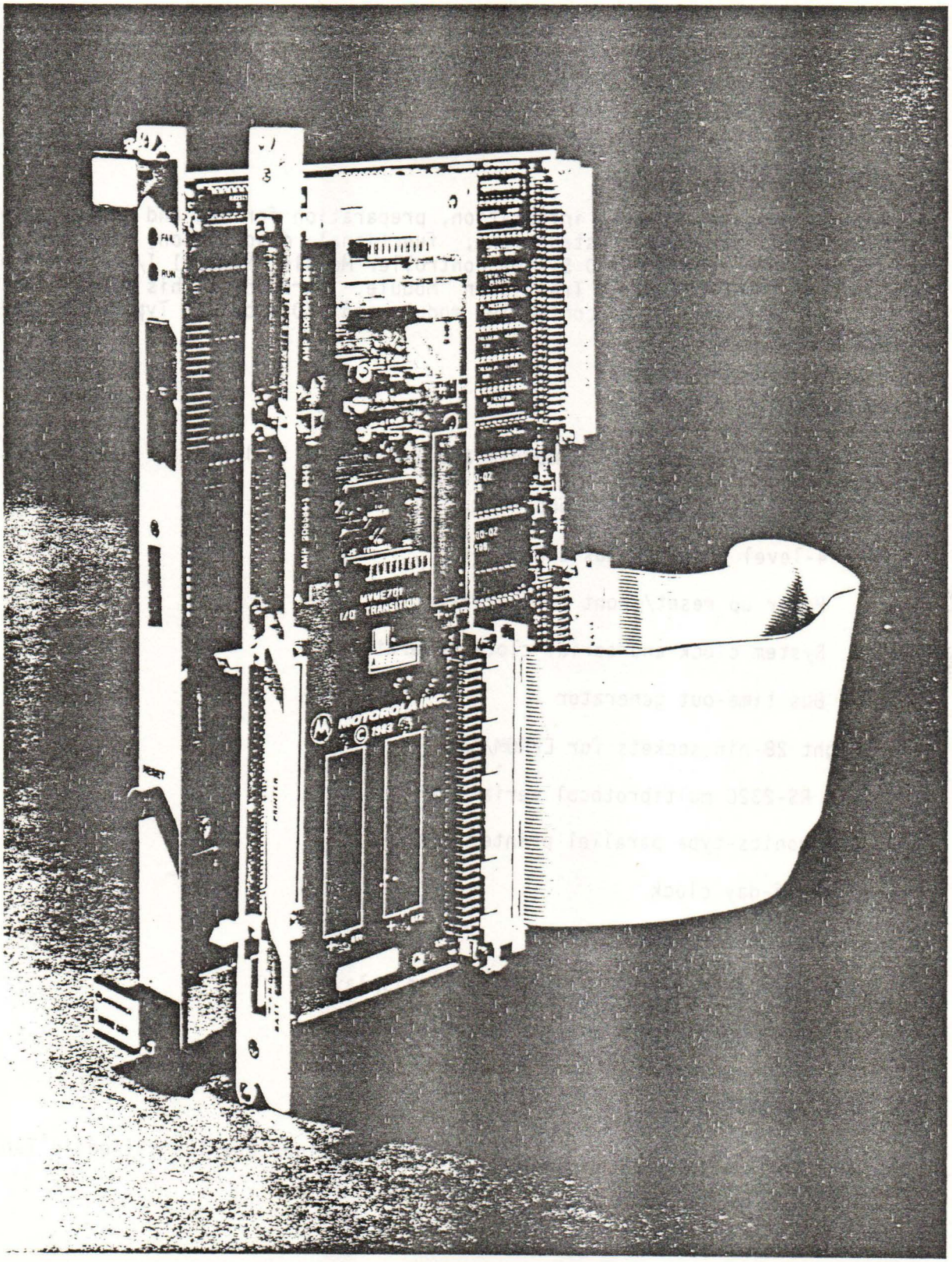


FIGURE 1-1. Typical Controller Module and I/O Module

TABLE 1-1. Controller Module and I/O Module Specifications

CHARACTERISTICS	SPECIFICATIONS			
Performance	Access time		Cycle time	
	Typ	Max	Typ	Max
RAM (J26) ROM (J27) Select Speed				
150 ns	375 ns	400 ns	455 ns	520 ns
250	475	550	555	670
350	575	675	655	785
450	650	700	730	820
Interface (I/O)				
Serial ports, printer, switches, LED	350 ns	400 ns	540 ns	650 ns
VBIM	500 ns	550 ns	580 ns	675 ns
Time-of-day clock	1100 us	1300 us	1180 us	1420 us
Bus arbitration time	Typical 75 ns		Maximum 125 ns	
Temperature				
Operating	0 degrees to 55 degrees C			
Storage	-40 degrees to 85 degrees C			
Relative humidity	5% to 90% (noncondensing)			
Physical characteristics				
Controller module				
Width x height	7.40 in. (188 mm) x 10.28 in. (261 mm)			
Thickness	0.83 in. (21 mm)			
I/O module				
Width x height	4.25 in. (108 mm) x 10.28 in. (261 mm)			
Thickness	0.83 in. (21 mm)			
Power requirements	+5 Vdc @ 3.7 A (typical) 4.4 A (max.)			
	-12 Vdc @ 35 mA (typical) 42 mA (max.)			
	+12 Vdc @ 140 mA (typical) 170 mA (max.)			

1.4 GENERAL DESCRIPTION

The controller module is a combination system controller and debug/diagnostics module for VME systems. The module is designed to offload the system controller functions from computer type modules, also to provide the typical one-per-system type features such as the time-of-day clock, printer/parallel port, and a serial port for downline loading of programs from a host system. The module is capable of holding a system diagnostics and debug monitor for end-use in-system trouble shooting and maintenance. A global interrupter provides the ability to have tightly coupled task/message passing between intelligent modules in multiprocessor systems. The controller module allows extended addressing for supporting the expanded (32 bit) VMEbus. Both 32-bit data and address are supported on EPROM/RAM sockets.

The I/O module is a combination printer interface, terminal and host ports I/O, and battery backup. Terminal and host ports can be configured as modem or terminal through jumper arrangements. The module holds four nickel-cadmium (Ni-cad) batteries that are rechargeable through the charging circuit on the controller module. A 4-pin connector (MVME701); 9-pin connector (MVME701A) is provided for a remote standby battery and remote reset.

1.5 RELATED DOCUMENTATION

The following publication may provide additional helpful information. If not shipped with this product, the manual may be obtained from Motorola Literature Distribution Center, 616 W. 24th Street, Tempe, Arizona 85282; telephone (602) 994-6561.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
VMEbus Specification Manual (Revision C)	MVMEBS

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking, hardware preparation, and installation instructions for the controller module and the I/O module.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment.

2.3 HARDWARE PREPARATION

To select the desired configuration and ensure proper operation of the controller module and the I/O module, certain changes may be made before installation. These changes are made through jumper arrangements on the headers. Figure 2-1 illustrates the location of the headers and connectors on the controller module. Figure 2-2 illustrates the location of the headers and connectors on the MVME701 I/O module. Figure 2-3 illustrates the headers and connectors on the MVME701A I/O module. The modules have been factory tested and are shipped with factory-installed jumper configurations that are also shown in Figures 2-1, 2-2, and 2-3. The modules are operational with the factory-installed jumpers. The controller module is configured to provide all the system controller functions required for a VMEbus system. The I/O module is configured to interface the controller module with a printer, host computer, or terminal. It is necessary to make changes in the jumper arrangements for the following conditions:

Controller module

a. EPROM base address select (J1,J2)

b. EPROM/RAM configuration select (quad 2) (J3)

c. Bus time-out select (J4)

d. Clock damping shorting select (J5,J6)

e. System controller select (J7)

f. EPROM size select (J8)

g. RAM base address select (J9,J10)

h. EPROM/RAM configuration select (quad 1) (J11)

i. Address Modifier (AM1E) enable select (EPROM bank 1); AM16 enable select (EPROM bank 2) (J12)

j. EPROM bank enable select (J13)

k. RAM bank enable select (J14)

l. RAM size select (J15)

m. EPROM/RAM configuration select (quad 1 and 2) (J16,J17,J18,J19)

n. I/O base address select (512 byte boundaries) (J20)

o. Time-of-day clock power select and battery charge (J21)

p. SYSFAIL* or GND select for interrupt source (J22)

q. Internal/external transmit clock serial port 1 select (J23)

r. Internal/external transmit clock serial port 2 select (J24)

s. Display blanking enable select (J25)

t. RAM access time select (J26)

u. EPROM access time select (J27)

v. RESET switch disable select (J28)

w. Printer acknowledge edge select (J29)

I/O Module

a. To terminal (serial port 1) select (J5)

b. To modem (serial port 1) select (J6)

c. DSR select (serial port 1) (J7)

d. DSR select (serial port 2) (J8)

e. To terminal (serial port 2) select (J9)

f. To modem (serial port 2) select (J10)

g. CTS select (serial port 1) (J11)

h. CTS select (serial port 2) (J12)

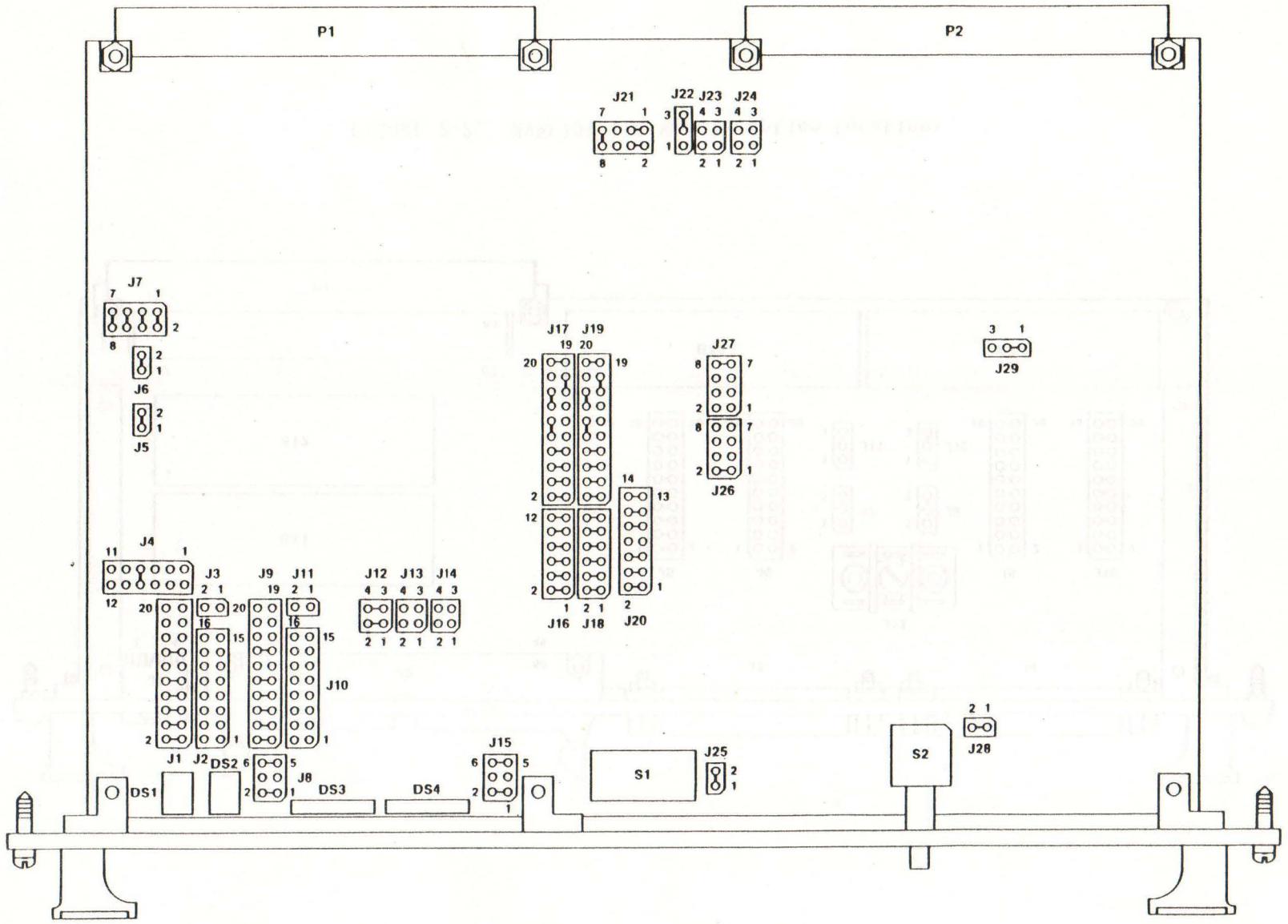


FIGURE 2-1. Controller Module Option Locations

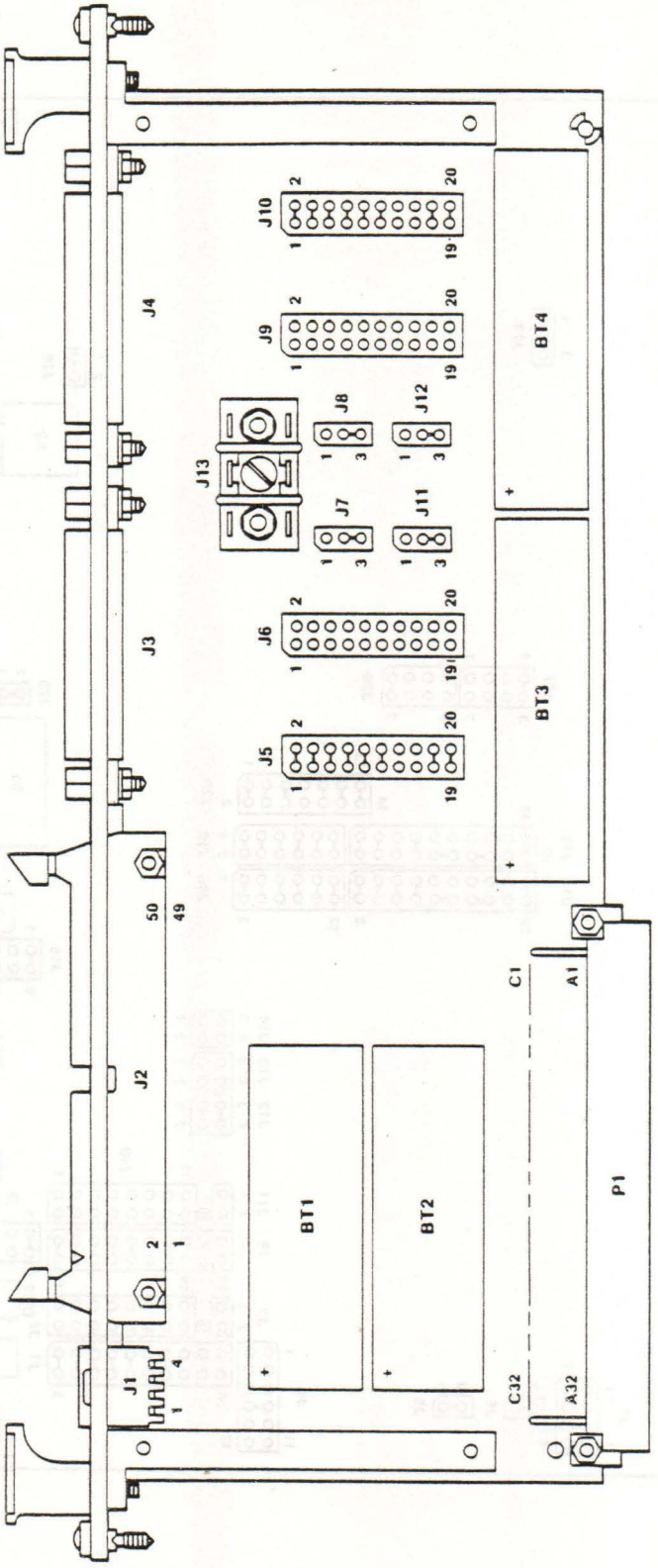


FIGURE 2-2. MVME701 I/O Module Option Locations

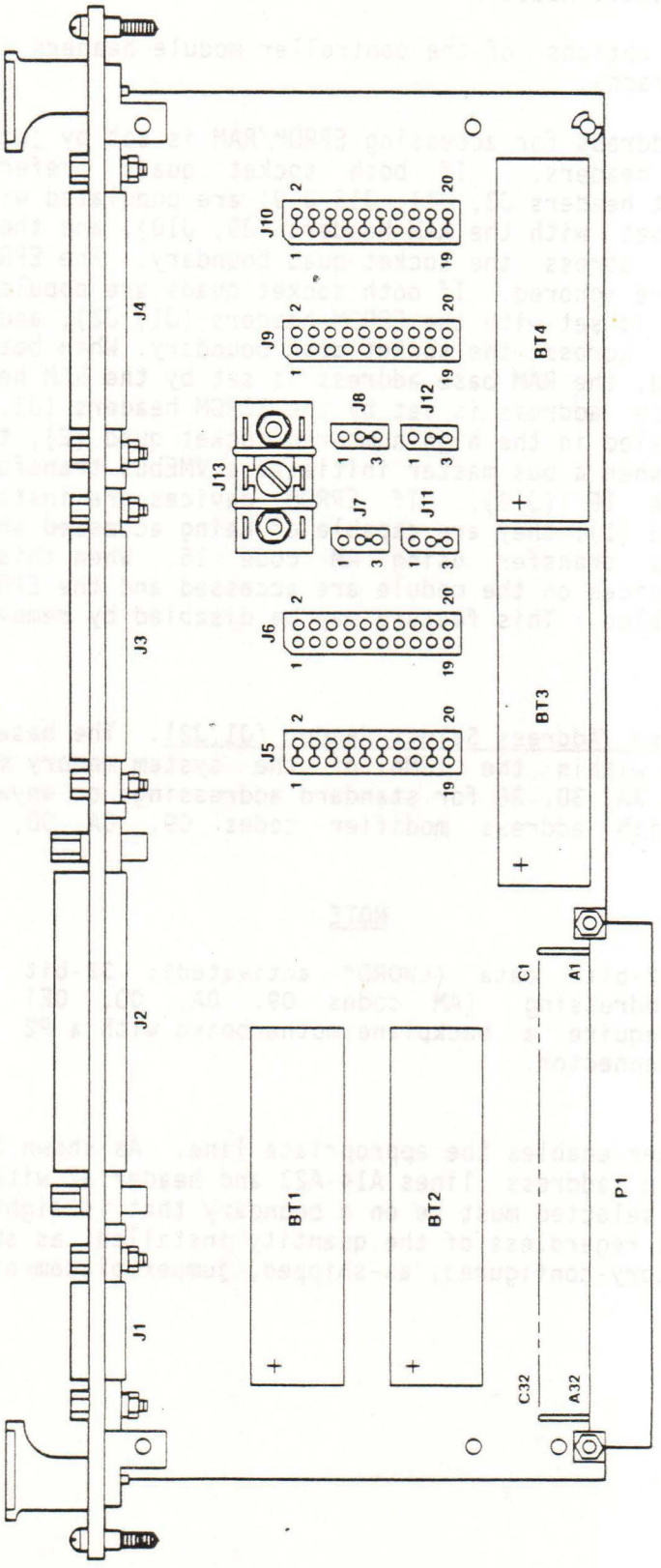


FIGURE 2-3. MVME701A I/O Module Option Locations

2.3.1 Controller Module Headers

The configuration options of the controller module headers are discussed in the following paragraphs.

The VMEbus base address for accessing EPROM/RAM is set by jumper position on the appropriate headers. If both socket quads (refer to EPROM/RAM configuration select headers J3, J11, J16-J19) are populated with RAM, the RAM base address is set with the RAM headers (J9, J10), and the RAM addressing becomes contiguous across the socket quad boundary. The EPROM base address headers (J1, J2) are ignored. If both socket quads are populated with EPROM, the base address is set with the EPROM headers (J1, J2), and the addressing becomes contiguous across the socket quad boundary. When both RAM and EPROM populations are used, the RAM base address is set by the RAM headers (J9, J10) and the EPROM base address is set by the EPROM headers (J1, J2). If EPROM devices are installed in the high numbered socket quad (2), they are capable of being accessed when a bus master initiates a VMEbus transfer using Address Modifier (AM) code 1E (J12). If EPROM devices are installed in the low numbered socket quad (1), they are capable of being accessed when a bus master initiates a VMEbus transfer using AM code 16. When this type of access occurs, no other devices on the module are accessed and the EPROM base address circuitry is disabled. This feature may be disabled by removing the jumpers from J12.

2.3.1.1 EPROM Base Address Select Header (J1,J2). The base address may be selected anywhere within the 16Mb of the system memory map with address modifier codes 39, 3A, 3D, 3E for standard addressing; or anywhere within the 4 gigabyte map with address modifier codes 09, 0A, 0D, 0E for extended addressing.

NOTE

32-bit data (LWORD* activated); 32-bit addressing (AM codes 09, 0A, 0D, 0E) require a backplane motherboard with a P2 connector.

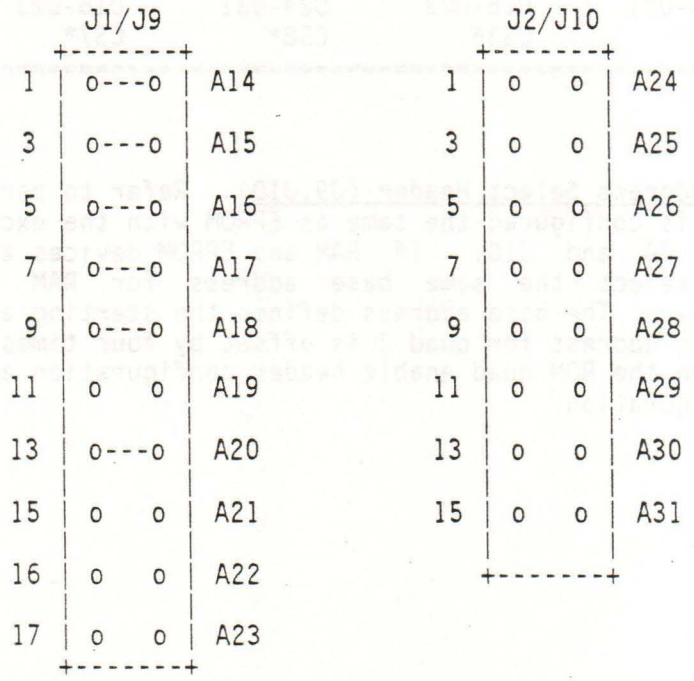
Installing a jumper enables the appropriate line. As shown below, header J1 is associated with address lines A14-A23 and header J2 with lines A24-A31. The base address selected must be on a boundary that is eight times the size of the devices used regardless of the quantity installed, as shown below. See Figure 2-1 for factory-configured, as-shipped, jumper placement.

For each quad used, a four-way split of data must be used. Let's assume the four sections of the quad were numbered as follows:

D0-D7 = 1
D8-D15 = 2
D16-D23 = 3
D24-D31 = 4

As an example, the four-way split would be:

ADDRESS	DATA	SECTION NUMBER
0	01	1
1	02	2
2	03	3
3	04	4
4	05	1
5	06	2
6	07	3
7	08	4



JUMPER IN = ADDRESS LINE LOW

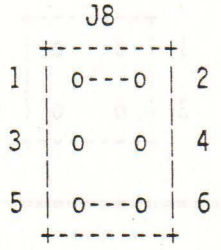
DEFAULT SHOWN = E80000 24-BIT ADDRESS
FFE80000 32-BIT ADDRESS

DEVICE SIZE	BOUNDARY
2K x 8	16K
4K x 8	32K
8K x 8	64K
16K x 8	128K
32K x 8	256K
64K x 8	512K

EPROM QUAD 2 RAM QUAD 1		EPROM QUAD 1 RAM QUAD 2	
XU33 D8-D15 CS2*	XU25 D0-D7 CS1*	XU16 D8-D15 CS6*	XU8 D0-D7 CS5*
XU36 D24-D31 CS4*	XU28 D16-D23 CS3*	XU19 D24-D31 CS8*	XU11 D16-D23 CS7*

2.3.1.2 RAM Base Address Select Header (J9,J10). Refer to paragraph 2.3.1.1. RAM base address is configured the same as EPROM with the exception that the headers used are J9 and J10. If RAM and EPROM devices are mixed in the sockets, do not select the same base address for RAM and EPROM. One overwrites the other. The base address defines the starting address for quad 1, and the starting address for quad 2 is offset by four times the part size. This also depends on the ROM quad enable header configuration and the RAM quad enable header configuration.

2.3.1.3 EPROM Size Select Header (J8). Header J8 allows the user to configure the module to operate with the devices installed in the sockets. Jumpers are positioned according to the table and illustration below. The size of the device (i.e., 2K x 8) determines the position of the jumpers. Devices must all be the same size. The as-shipped configuration is shown below.

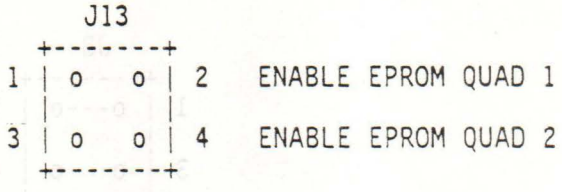


SIZE OF PART	HEADER PINS 1 TO 2	3 TO 4	5 TO 6
2K	X	X	X
4K	O	X	X
8K	X	O	X
16K	O	O	X
32K	X	X	O
64K	O	X	O

X = jumper installed

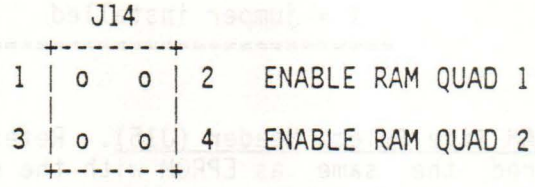
2.3.1.4 RAM Size Select Header (J15). Refer to paragraph 2.3.1.3. RAM size is configured the same as EPROM with the exception that the header is J15. All other information applies.

2.3.1.5 EPROM Quad Enable Select Header (J13). Header J13 allows the user to select quad 1 or quad 2 according to the installation of the EPROM devices. Refer to table below for quad information. To enable quad 1, install a jumper between pins 1 and 2. To enable quad 2, install a jumper between pins 3 and 4. If all EPROM in both quads, install both jumpers.



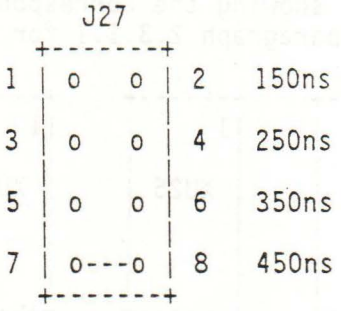
EPROM QUAD 2		EPROM QUAD 1	
XU33	XU25	XU16	XU8
D8-D15	D0-D7	D8-D15	D0-D7
CS2*	CS1*	CS6*	CS5*
XU36	XU28	XU19	XU11
D24-D31	D16-D23	D24-D31	D16-D23
CS4*	CS3*	CS8*	CS7*

2.3.1.6 RAM Quad Enable Select Header (J14). Header J14 allows the user to select quad 1 or quad 2 according to the installation of the RAM devices. Refer to the table below for quad information. To enable quad 1, install a jumper between pins 1 and 2. To enable quad 2, install a jumper between pins 3 and 4. If all RAM in both quads, install both jumpers.



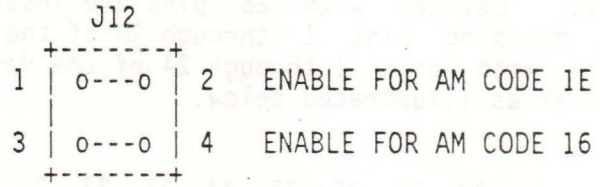
RAM QUAD 1		RAM QUAD 2	
XU33	XU25	XU16	XU8
D8-D15	D0-D7	D8-D15	D0-D7
CS2*	CS1*	CS6*	CS5*
XU36	XU28	XU19	XU11
D24-D31	D16-D23	D24-D31	D16-D23
CS4*	CS3*	CS8*	CS7*

2.3.1.7 EPROM Access Time Select Header (J27). Header J27 is used to select the appropriate delay to compensate for the access times of the EPROM memory devices that are installed in the sockets. The access times of the EPROM devices installed should be compared with the access times in the illustration below. Install a jumper between pins that correspond to the access required by the EPROM device. Default is 450 ns as shown below:



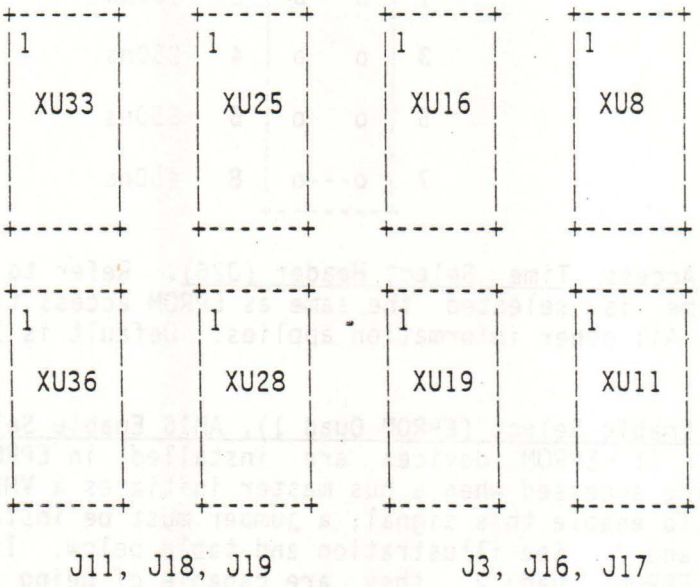
2.3.1.8 RAM Access Time Select Header (J26). Refer to paragraph 2.3.1.7. RAM access time is selected the same as EPROM access time except that the header is J26. All other information applies. Default is 150 ns.

2.3.1.9 AM1E Enable Select (EPROM Quad 1), AM16 Enable Select (EPROM Quad 2) Header (J12). If EPROM devices are installed in EPROM quad 1, they are capable of being accessed when a bus master initiates a VMEbus transfer using AM code 1E. To enable this signal, a jumper must be installed on header J12 between pins 1 and 2. See illustration and table below. If EPROM devices are installed in EPROM quad 2, they are capable of being accessed when a bus master initiates a VMEbus transfer using AM code 16. To enable this signal, a jumper must be installed between pins 3 and 4.

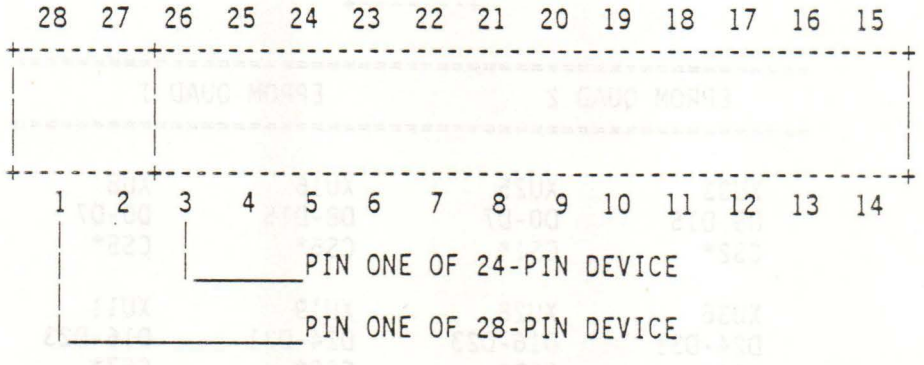


EPROM QUAD 2		EPROM QUAD 1	
XU33	XU25	XU16	XU8
D8-D15	D0-D7	D8-D15	D0-D7
CS2*	CS1*	CS6*	CS5*
XU36	XU28	XU19	XU11
D24-D31	D16-D23	D24-D31	D16-D23
CS4*	CS3*	CS8*	CS7*

2.3.1.10 EPROM/RAM Configuration Select Headers (J3,J11,J16,J17,J18,J19). Eight, 28-pin sockets may be populated by the user with 24-pin or 28-pin RAM or EPROM devices. ROM devices may be used provided the CS line is masked as true low. RAM and EPROM populations may be mixed. RAM's are installed into the sockets starting at RAM quad 1. EPROM's are installed into the sockets starting at EPROM quad 1 (refer to table in paragraph 2.3.1.9). Configuration headers (J3,J11,J16-J19) are provided to configure each socket quad for RAM or EPROM and the type of device (i.e., 2K x 8). The socket layout on the module is illustrated below showing the corresponding headers for configuration of the sockets. Refer to paragraph 2.3.1.1 for four-way split information



Each quad may be individually configured to accept a wide range of industry standard 24-pin and 28-pin RAM and EPROM devices. The user must provide and install the appropriate memory devices to suit the specific application intended. Devices with 28 pins are inserted with pins 1 through 28 of the device matching pins 1 through 28 of the socket. Devices with 24 pins are inserted with pins 1 through 24 of the device matching pins 3 through 26 of the socket as illustrated below.



Associated with each socket quad are three local memory configuration headers. The headers must be configured for each quad that contains memory devices. Each figure shows the as shipped factory configuration. The factory configuration is the same for both quads assuming 8K x 8 EPROMS.

Table 2-1 lists several RAM and EPROM devices that may be installed in the socket quads. The jumpering of pins on the headers for some of the configurations can be performed with the jumpers provided; other configurations may have to be done with wire wrap. Some wire wrap is necessary between pins of different headers.

TABLE 2-1. Allowable EPROM and RAM Memory Devices

PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS
AM2716	Advanced Micro Devices	EPROM	2K x 8	24
AM9716	Advanced Micro Devices	EPROM	2K x 8	24
HM6716	Harris	EPROM	2K x 8	24
HN462716	Hitachi	EPROM	2K x 8	24
I2716	Intel	EPROM	2K x 8	24
MBM2716	Fujitsu	EPROM	2K x 8	24
MCM2716	Motorola	EPROM	2K x 8	24
MK2716	Mostek	EPROM	2K x 8	24
MM2716	National Semiconductor	EPROM	2K x 8	24
MN2716	Panasonic	EPROM	2K x 8	24
MSM2716	OKI Electric Industry	EPROM	2K x 8	24
S4716	American Microsystems Inc.	EPROM	2K x 8	24
SM2716	Siemens	EPROM	2K x 8	24
SY2716	Synertek	EPROM	2K x 8	24
TMS2516	Texas Instruments	EPROM	2K x 8	24
TMM323	Toshiba	EPROM	2K x 8	24
UPD2716	Nippon Electric Company	EPROM	2K x 8	24

TABLE 2-1. Allowable EPROM and RAM Memory Devices (cont'd)

PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS
HN462532	Hitachi	EPROM	4K x 8	24
HN462732	Hitachi	EPROM	4K x 8	24
I2732	Intel	EPROM	4K x 8	24
MBM2732	Fujitsu	EPROM	4K x 8	24
MCM2532	Motorola	EPROM	4K x 8	24
NMC2532	National Semiconductor	EPROM	4K x 8	24
NMC2732	National Semiconductor	EPROM	4K x 8	24
TMM2732	Toshiba	EPROM	4K x 8	24
TMS2532	Texas Instruments	EPROM	4K x 8	24
UPD2732	Nippon Electric Company	EPROM	4K x 8	24
MCM68764	Motorola	EPROM	8K x 8	24
MCM68766	Motorola	EPROM	8K x 8	24
AM2764	Advanced Micro Devices	EPROM	8K x 8	28
HN2764	Hitachi	EPROM	8K x 8	28
MBM482764	Fujitsu	EPROM	8K x 8	28
MK2764	Mostek	EPROM	8K x 8	28
MSM2764	OKI Electric Industry	EPROM	8K x 8	28
NMC2564	National Semiconductor	EPROM	8K x 8	28
TMM2764	Toshiba	EPROM	8K x 8	28
TMS2564	Texas Instruments	EPROM	8K x 8	28
UPD2764	Nippon Electric Company	EPROM	8K x 8	28

TABLE 2-1. Allowable EPROM and RAM Memory Devices (cont'd)

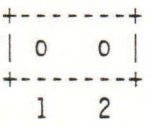
PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS
AM27128	Advanced Micro Devices	EPROM	16K x 8	28
I27128	Intel	EPROM	16K x 8	28
MBM27128	Fujitsu	EPROM	16K x 8	28
TMS27128	Texas Instruments	EPROM	16K x 8	28
AM27256	Advanced Micro Devices	EPROM	32K x 8	28
I27256	Intel	EPROM	32K x 8	28
MK27256	Mostek	EPROM	32K x 8	28
TMS27256	Texas Instruments	EPROM	32K x 8	28
AM27512	Advanced Micro Devices	EPROM	64K x 8	28
I27512	Intel	EPROM	64K x 8	28
AM9218	Advanced Micro Devices	RAM	2K x 8	24
HM6116	Harris	RAM	2K x 8	24
HM6516	Harris	RAM	2K x 8	24
HM6116	Hitachi	RAM	2K x 8	24
MB2128	Fujitsu	RAM	2K x 8	24
MB8418	Fujitsu	RAM	2K x 8	24
MCM4016	Motorola	RAM	2K x 8	24
MCM65116	Motorola	RAM	2K x 8	24
MSM5116	Mitsubishi	RAM	2K x 8	24
MSM2128	OKI Electric Industry	RAM	2K x 8	24
NMC2116	National Semiconductor	RAM	2K x 8	24
SY2128	Synertek	RAM	2K x 8	24

TABLE 2-1. Allowable EPROM and RAM Memory Devices (cont'd)

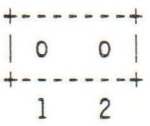
PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS
TC5516	Toshiba	RAM	2K x 8	24
TC5517	Toshiba	RAM	2K x 8	24
TC5518	Toshiba	RAM	2K x 8	24
TMM2016	Toshiba	RAM	2K x 8	24
TMS4016	Texas Instruments	RAM	2K x 8	24
8148	Mostek	RAM	4K x 8	28
HM6264	Hitachi	RAM	8K x 8	28
TC5564	Toshiba	RAM	8K x 8	28
TC5565	Toshiba	RAM	8K x 8	28

Header configuration for 2K x 8 EPROM memory devices is shown below:

J3



J11



J16

+5V	1	o o	2	Q2P1
LA14	3	o o	4	Q2P2
OE*	5	o---o	6	P22XU8
OE*	7	o---o	8	P22XU16
OE*	9	o---o	10	P22XU11
OE*	11	o---o	12	P22XU19

J18

+5V	1	o o	2	Q1P1
LA14	3	o o	4	Q1P2
OE*	5	o---o	6	P22XU25
OE*	7	o---o	8	P22XU33
OE*	9	o---o	10	P22XU28
OE*	11	o---o	12	P22XU36

J17

CS1*	1	o---o	2	P20XU8
CS2*	3	o---o	4	P20XU16
CS3*	5	o---o	6	P20XU11
CS4*	7	o---o	8	P20XU19
LA15	9	o o	10	Q2P26
LA17	11	o -o	12	+5V
LA16	13	o | o	14	Q2P27
Q2P23	15	o- o	16	WE*
LA13	17	o o	18	GND
LA12	19	o---o	20	Q2P21

EPROM QUAD 1

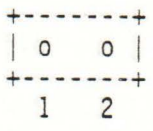
J19

CS1*	1	o---o	2	P20XU25
CS2*	3	o---o	4	P20XU33
CS3*	5	o---o	6	P20XU28
CS4*	7	o---o	8	P20XU36
LA15	9	o o	10	Q1P26
LA17	11	o -o	12	+5V
LA16	13	o | o	14	Q1P27
Q1P23	15	o- o	16	WE*
LA13	17	o o	18	GND
LA12	19	o---o	20	Q1P21

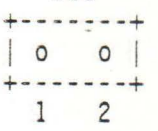
EPROM QUAD 2

Header configuration for 4K x 8 EPROM memory devices (I2732, MBM2732, NMC2732, TMM2732, UPD2732) is shown below:

J3



J11



J16

+5V	1	2	Q2P1	
LA14	3	4	Q2P2	
OE*	5	6	P22XU8	
OE*	7	8	P22XU16	
OE*	9	10	P22XU11	
OE*	11	12	P22XU19	

J18

+5V	1	2	Q1P1	
LA14	3	4	Q1P2	
OE*	5	6	P22XU25	
OE*	7	8	P22XU33	
OE*	9	10	P22XU28	
OE*	11	12	P22XU36	

J17

CS1*	1	2	P20XU8	
CS2*	3	4	P20XU16	
CS3*	5	6	P20XU11	
CS4*	7	8	P20XU19	
LA15	9	10	Q2P26	
LA17	11	12	+5V	
LA16	13	14	Q2P27	
Q2P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q2P21	

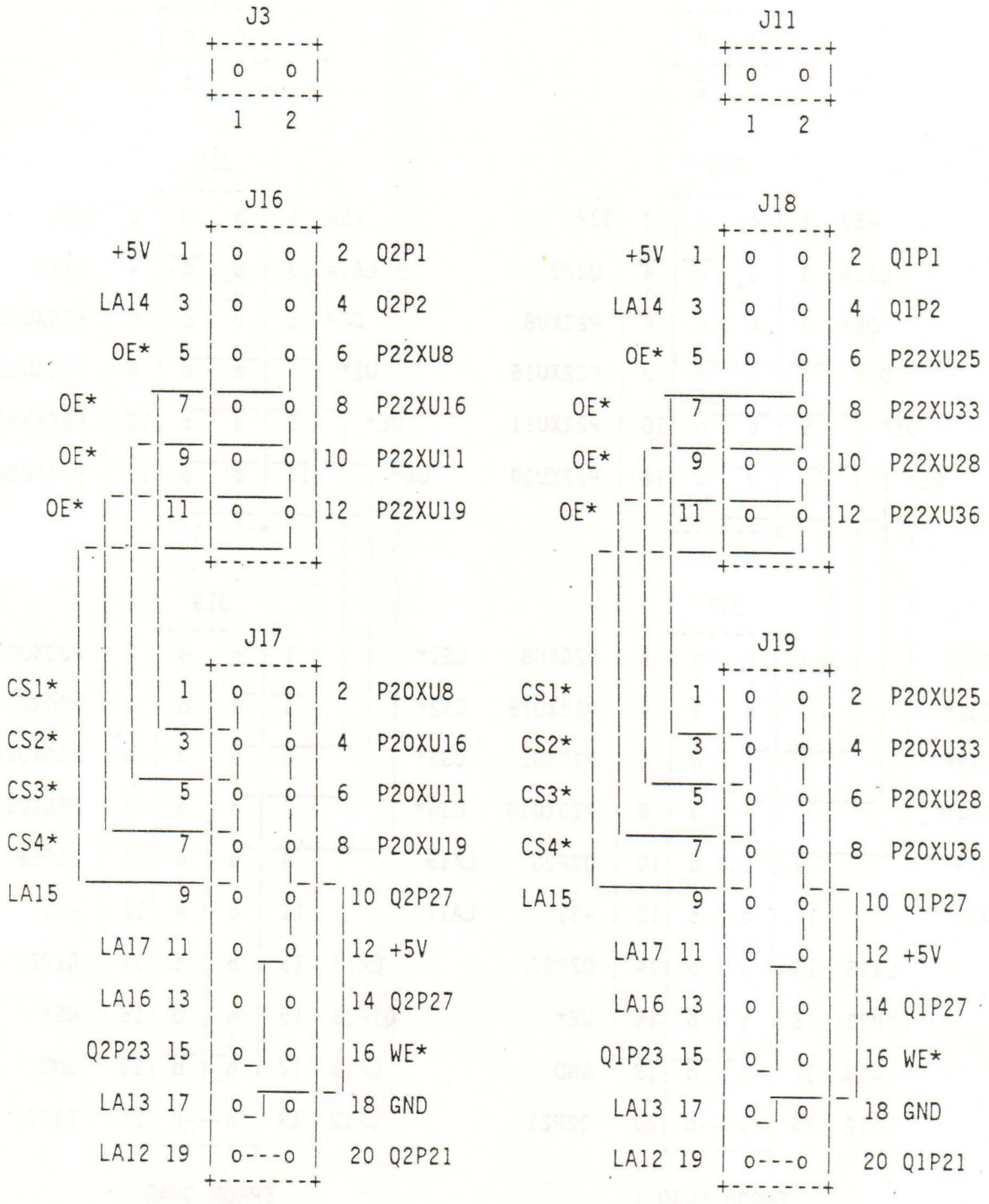
EPROM QUAD 1

J19

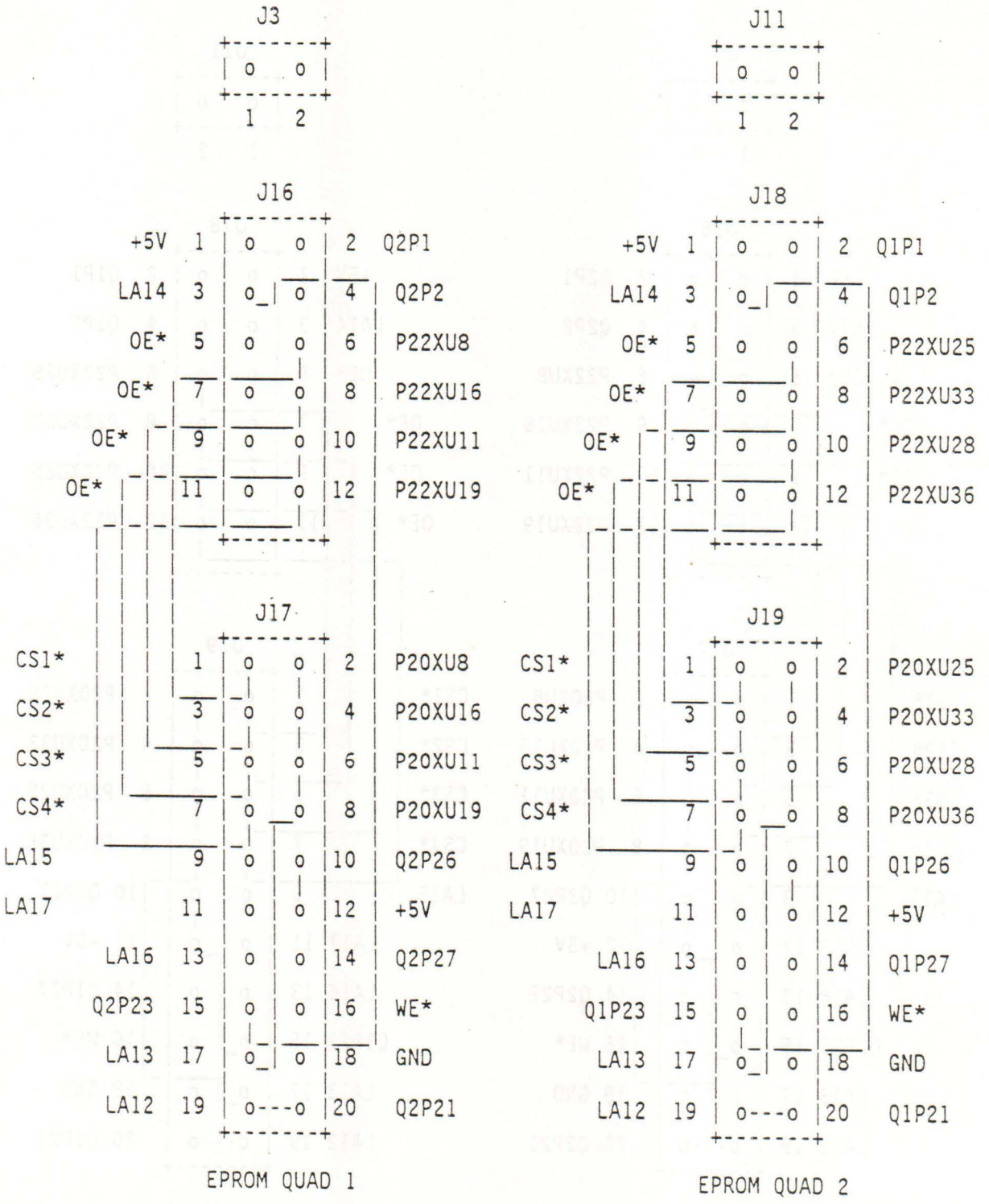
CS1*	1	2	P20XU25	
CS2*	3	4	P20XU33	
CS3*	5	6	P20XU28	
CS4*	7	8	P20XU36	
LA15	9	10	Q1P26	
LA17	11	12	+5V	
LA16	13	14	Q1P27	
Q1P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q1P21	

EPROM QUAD 2

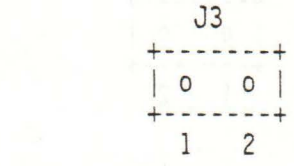
Header configuration for 4K x 8 EPROM memory devices (HN462532, HN462732, MCM2532, NMC2532, TMS2532) is shown below:

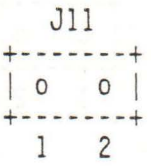


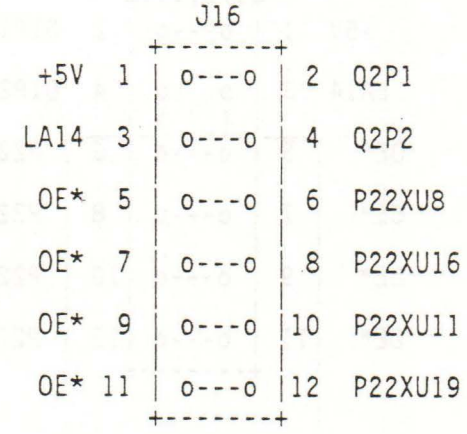
Header configuration for 8K x 8 EPROM memory devices (MCM68764, MCM68766) is shown below:

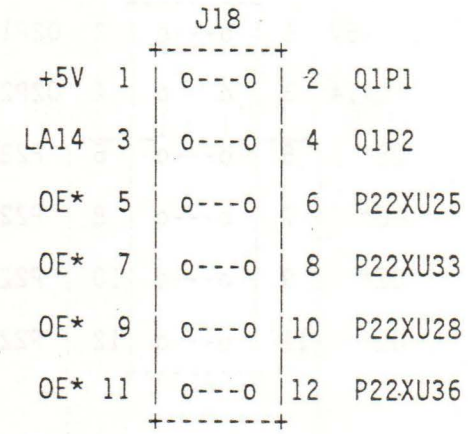


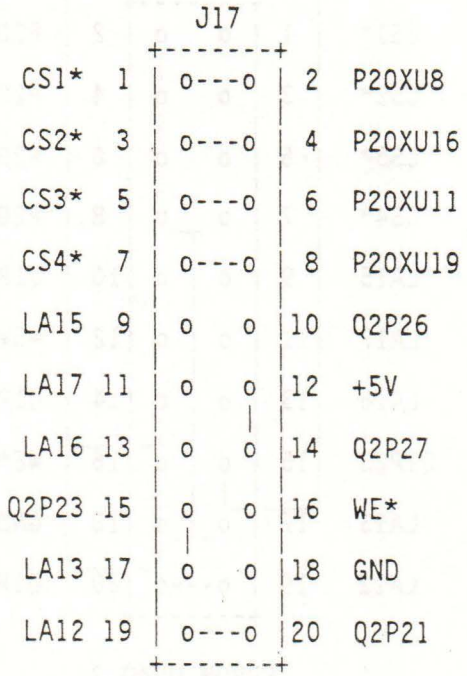
Header configuration for 8K x 8 EPROM memory devices (AM2764, HN2764, I2764, MBM48764, MK2764, MSM2764, TMM2764, UPD2764) is shown below:



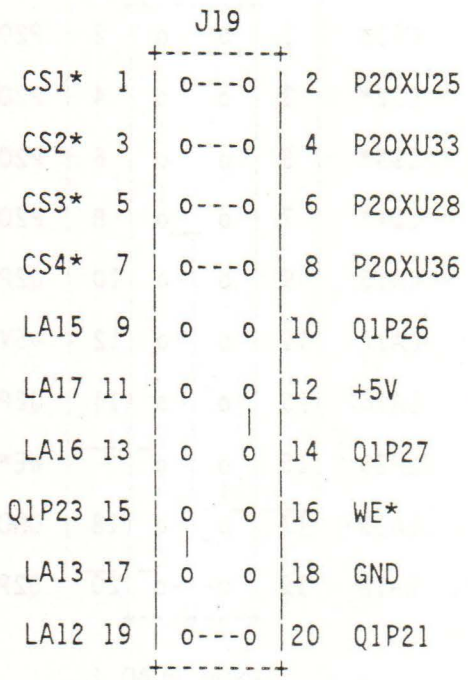






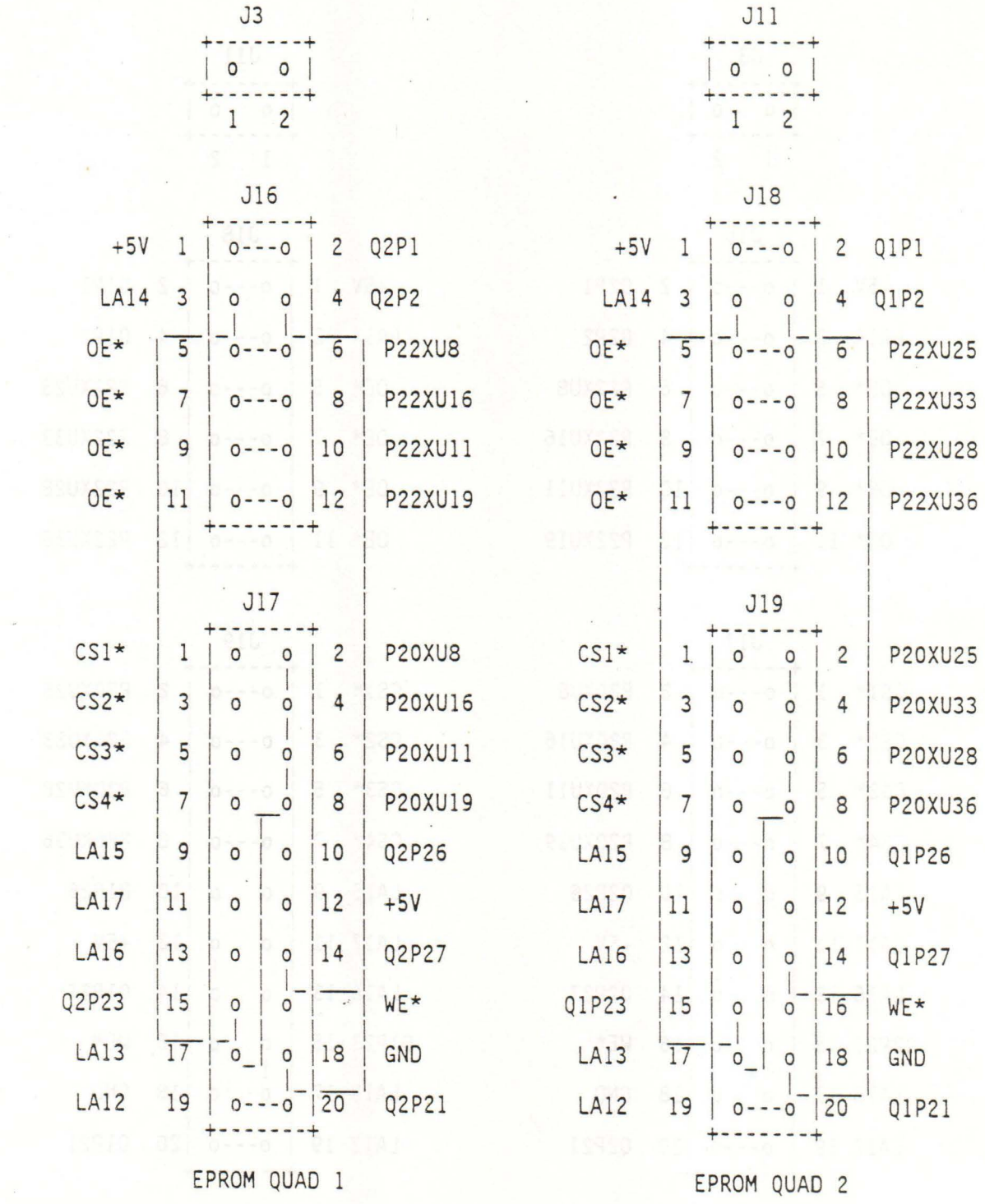


EPROM QUAD 1



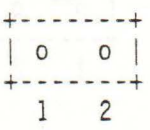
EPROM QUAD 2

Header configuration for 8K x 8 EPROM memory devices (NMC2564, TMS2564) is shown below:

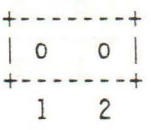


Header configuration for 16K x 8 EPROM memory devices (AM27128, I27128, MBM27128) is shown below:

J3



J11



J16

+5V	1	2	Q2P1	
LA14	3	4	Q2P2	
OE*	5	6	P22XU8	
OE*	7	8	P22XU16	
OE*	9	10	P22XU11	
OE*	11	12	P22XU19	

J18

+5V	1	2	Q1P1	
LA14	3	4	Q1P2	
OE*	5	6	P22XU25	
OE*	7	8	P22XU33	
OE*	9	10	P22XU28	
OE*	11	12	P22XU19	

J17

CS1*	1	2	P20XU8	
CS2*	3	4	P20XU16	
CS3*	5	6	P20XU11	
CS4*	7	8	P20XU19	
LA15	9	10	Q2P26	
LA17	11	12	+5V	
LA16	13	14	Q2P27	
Q2P23	15	16	WE*	
LA13	17	18	GND	
LA12		20	Q2P21	

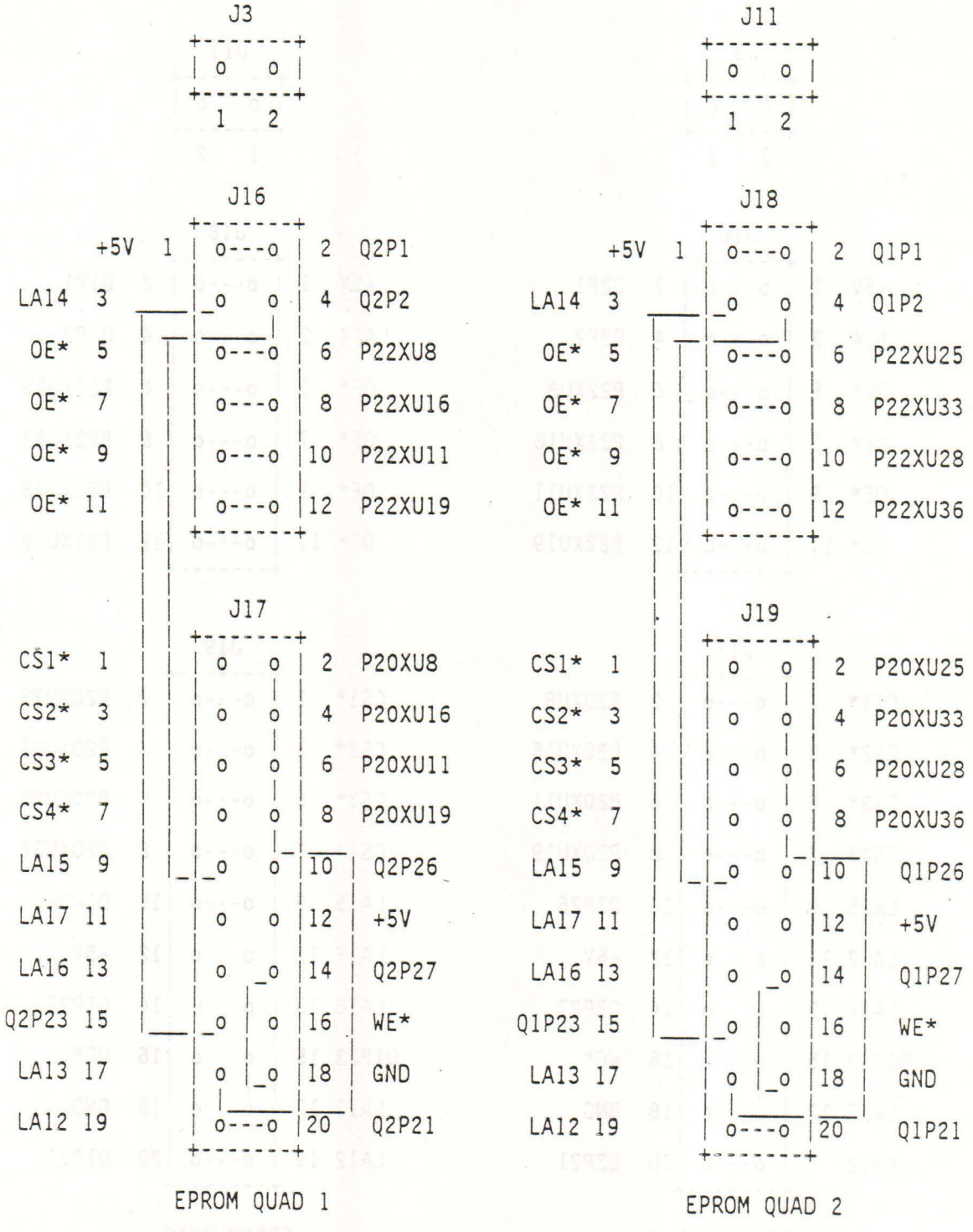
EPROM QUAD 1

J19

CS1*	1	2	P20XU25	
CS2*	3	4	P20XU33	
CS3*	5	6	P20XU28	
CS4*	7	8	P20XU36	
LA15	9	10	Q1P26	
LA17	11	12	+5V	
LA16	13	14	Q1P27	
Q1P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q1P21	

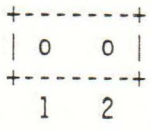
EPROM QUAD 2

Header configuration for 16K x 8 EPROM memory devices (TMS27128) is shown below:

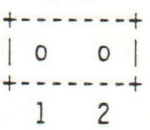


Header configuration for 32K x 8 EPROM memory devices (AM27256, I27256) is shown below:

J3



J11



J16

+5V	1	2	Q2P1	
LA14	3	4	Q2P2	
OE*	5	6	P22XU8	
OE*	7	8	P22XU16	
OE*	9	10	P22XU11	
OE*	11	12	P22XU19	

J18

+5V	1	2	Q1P1	
LA14	3	4	Q1P2	
OE*	5	6	P22XU25	
OE*	7	8	P22XU33	
OE*	9	10	P22XU28	
OE*	11	12	P22XU36	

J17

CS1*	1	2	P20XU8	
CS2*	3	4	P20XU16	
CS3*	5	6	P20XU11	
CS4*	7	8	P20XU19	
LA15	9	10	Q2P26	
LA17	11	12	+5V	
LA16	13	14	Q2P27	
Q2P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q2P21	

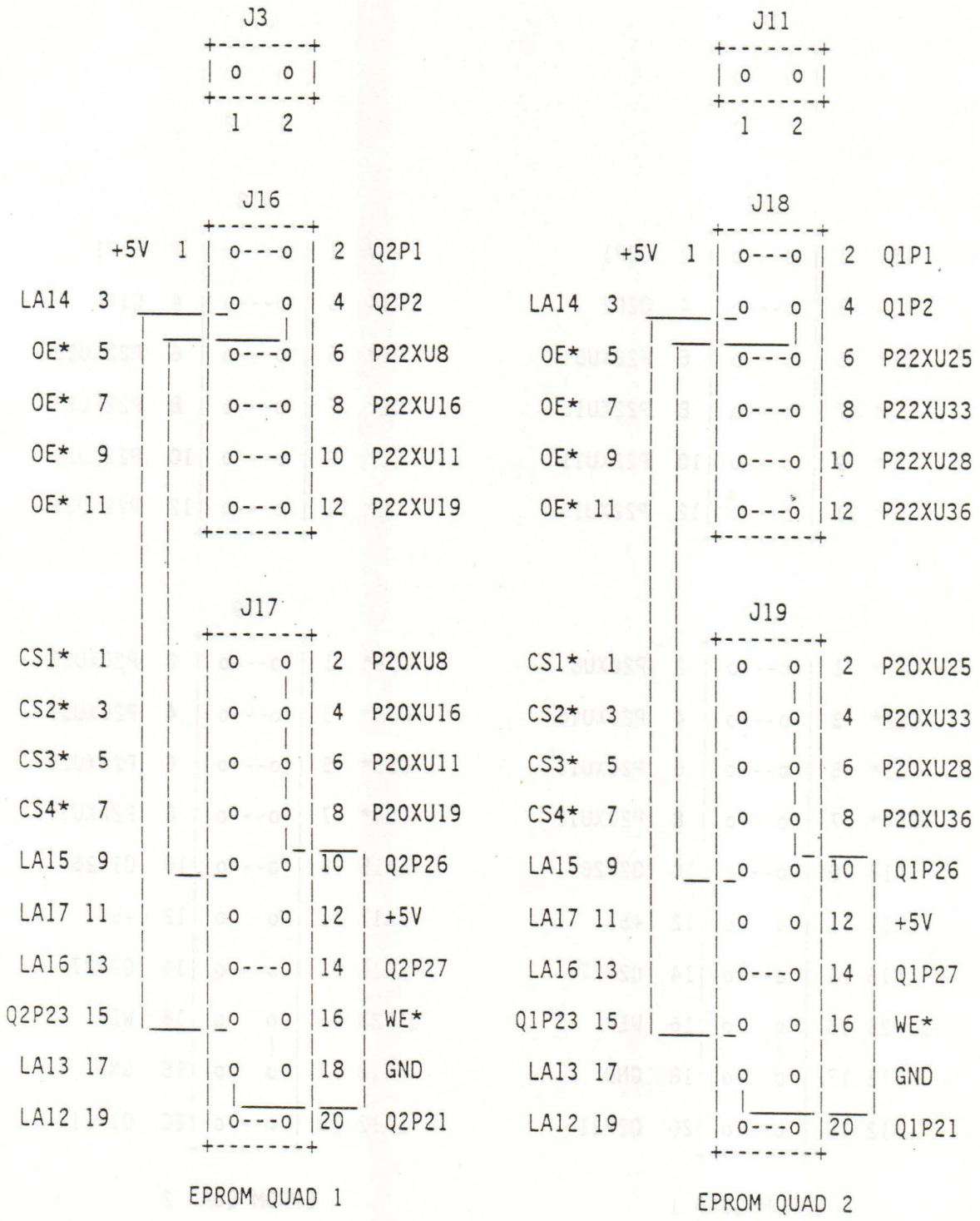
EPROM QUAD 1

J19

CS1*	1	2	P20XU25	
CS2*	3	4	P20XU33	
CS3*	5	6	P20XU28	
CS4*	7	8	P20XU36	
LA15	9	10	Q1P26	
LA17	11	12	+5V	
LA16	13	14	Q1P27	
Q1P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q1P21	

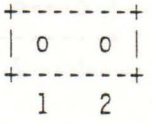
EPROM QUAD 2

Header configuration for 32K x 8 EPROM memory devices (TMS27256) is shown below:

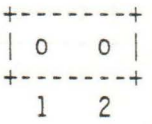


Header configuration for 32K x 8 EPROM memory devices (MK27256) is shown below:

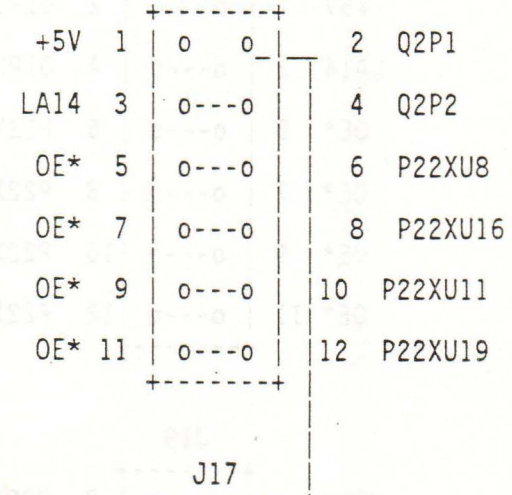
J3



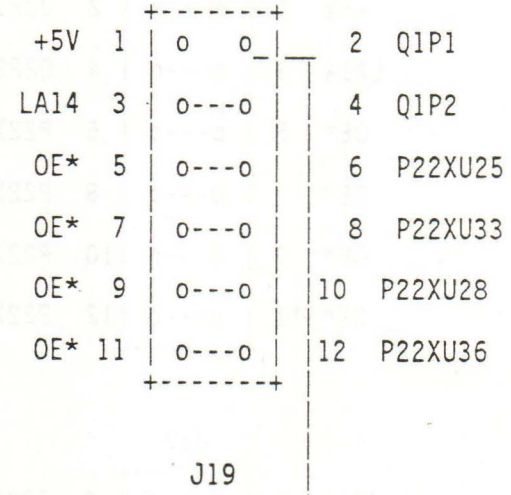
J11



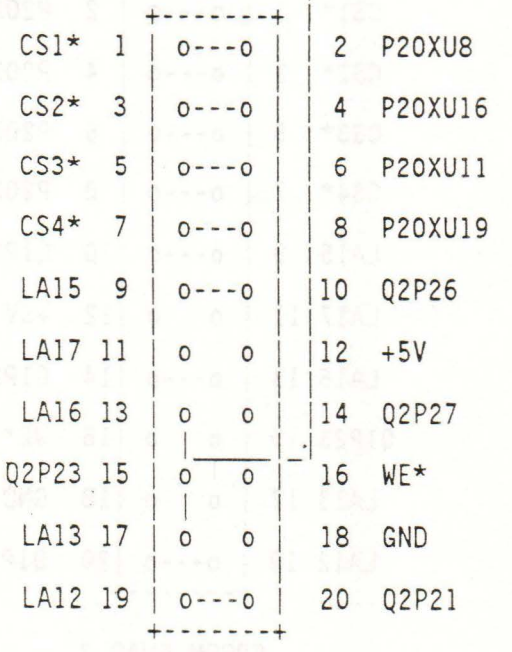
J16



J18

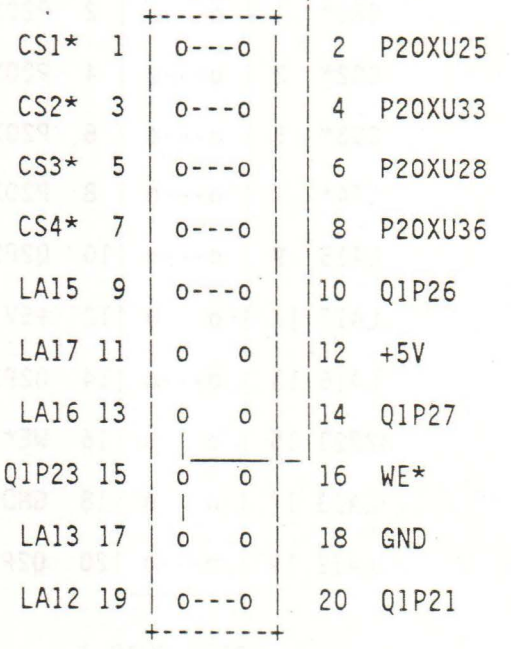


J17



EPROM QUAD 1

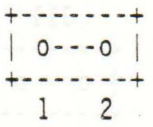
J19



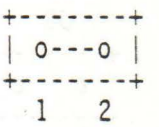
EPROM QUAD 2

Header configuration for 64K x 8 EPROM memory devices is shown below:

J3



J11



J16

+5V	1	2	Q2P1	
LA14	3	4	Q2P2	
OE*	5	6	P22XU8	
OE*	7	8	P22XU16	
OE*	9	10	P22XU11	
OE*	11	12	P22XU19	

J18

+5V	1	2	Q1P1	
LA14	3	4	Q1P2	
OE*	5	6	P22XU25	
OE*	7	8	P22XU33	
OE*	9	10	P22XU28	
OE*	11	12	P22XU36	

J17

CS1*	1	2	P20XU8	
CS2*	3	4	P20XU16	
CS3*	5	6	P20XU11	
CS4*	7	8	P20XU19	
LA15	9	10	Q2P26	
LA17	11	12	+5V	
LA16	13	14	Q2P27	
Q2P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q2P21	

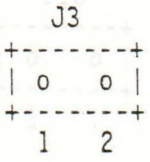
EPROM QUAD 1

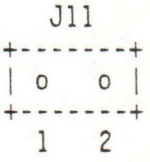
J19

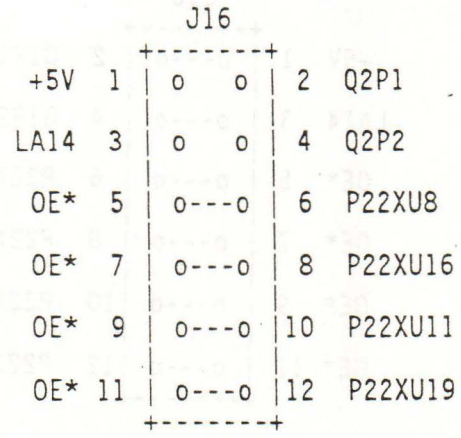
CS1*	1	2	P20XU25	
CS2*	3	4	P20XU33	
CS3*	5	6	P20XU28	
CS4*	7	8	P20XU36	
LA15	9	10	Q1P26	
LA17	11	12	+5V	
LA16	13	14	Q1P27	
Q1P23	15	16	WE*	
LA13	17	18	GND	
LA12	19	20	Q1P21	

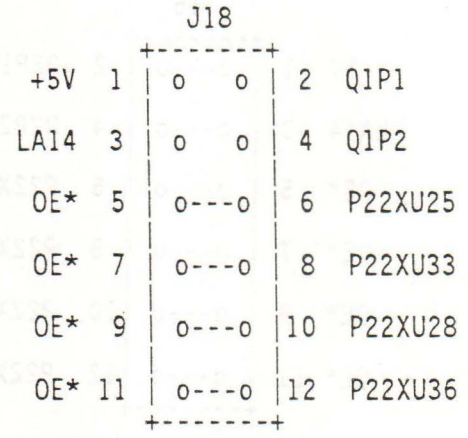
EPROM QUAD 2

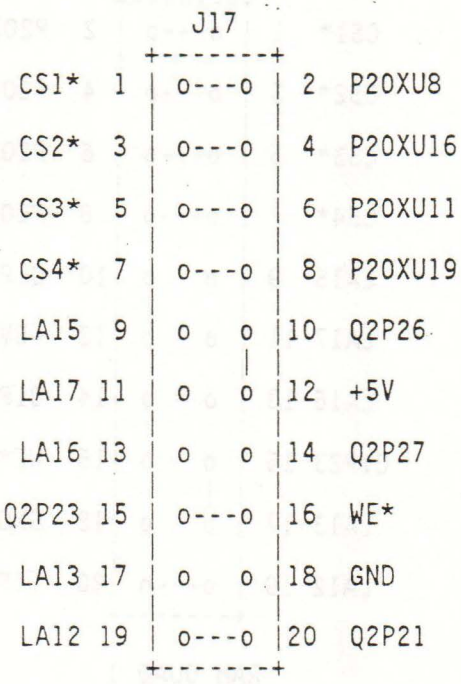
Header configuration for 2K x 8 RAM memory devices is shown below:



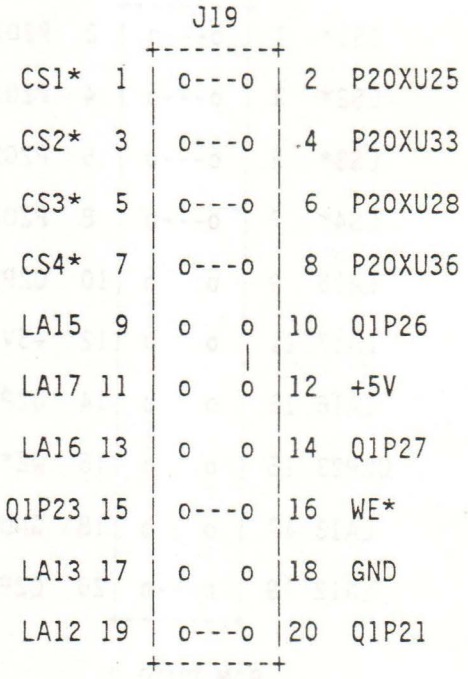






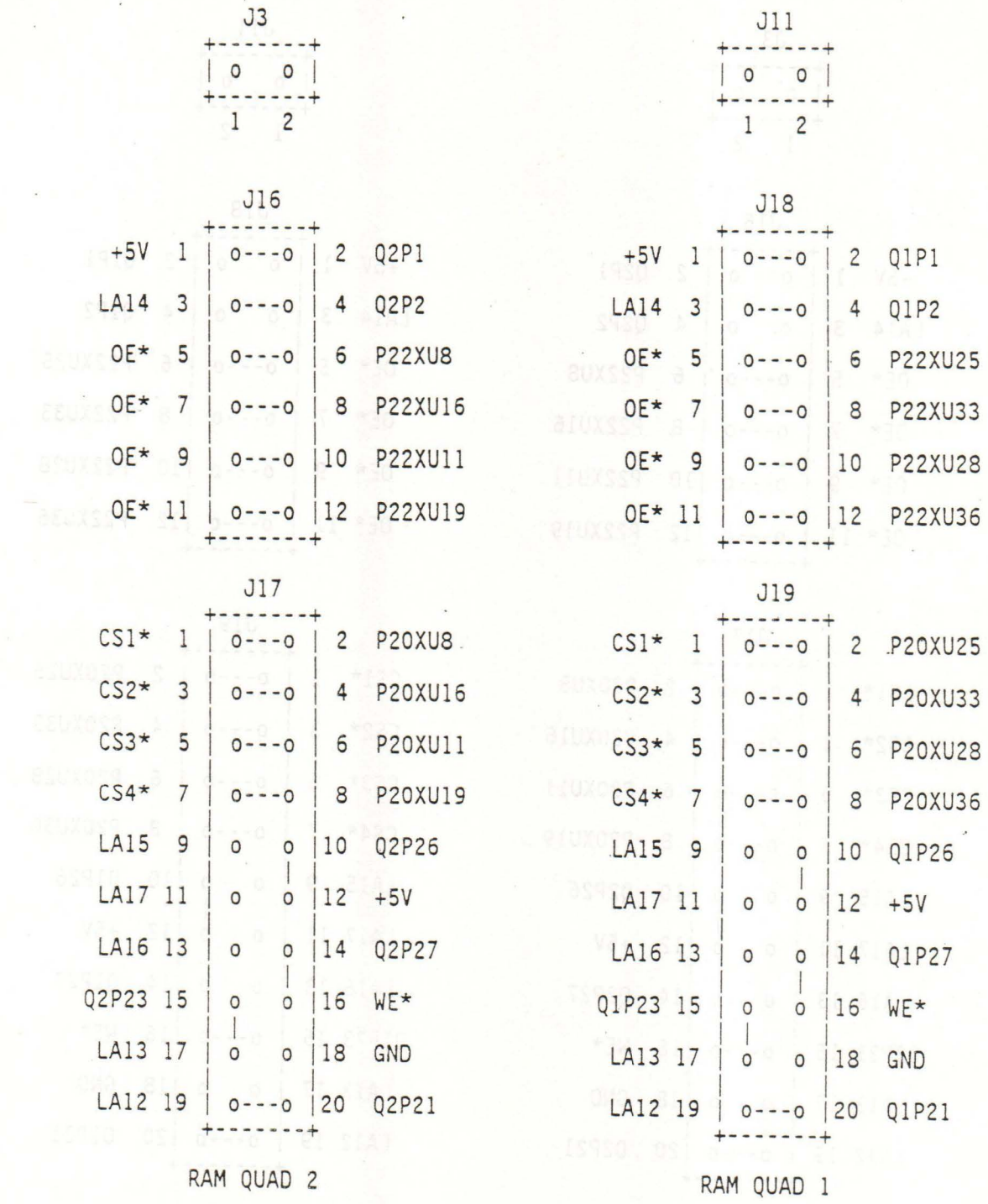


RAM QUAD 2

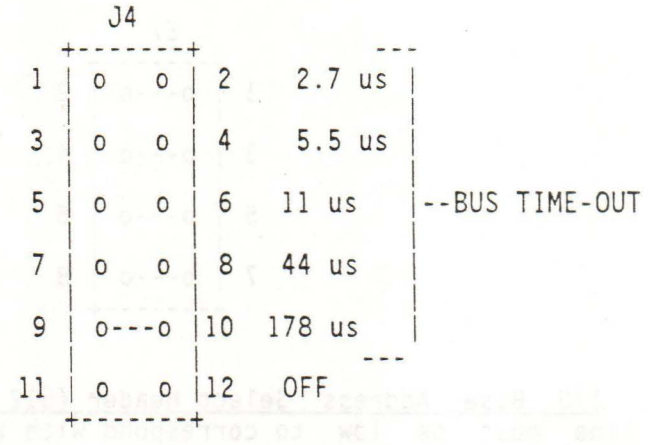


RAM QUAD 1

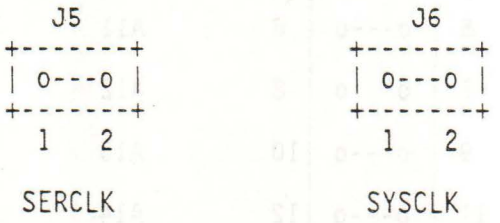
Header configuration for 8K x 8 RAM memory devices is shown below:



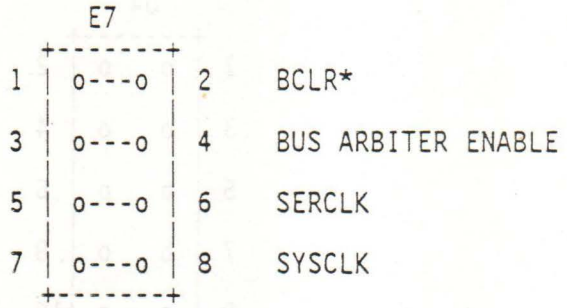
2.3.1.11 Bus Time-Out Select Header (J4). Header J4 allows the user to select the bus time-out time after Data Strobe 0 (DS0) or Data Strobe 1 (DS1) is activated. A time-out activates Bus Error (BERR*). A time-out time in microseconds is selected by positioning a jumper on the desired time. Only one jumper may be installed at a time. If the controller module is not selected as the system controller, the bus time-out should be OFF. A jumper may be installed between pins 11 and 12 to turn the time-out off. Header J4 is illustrated below:



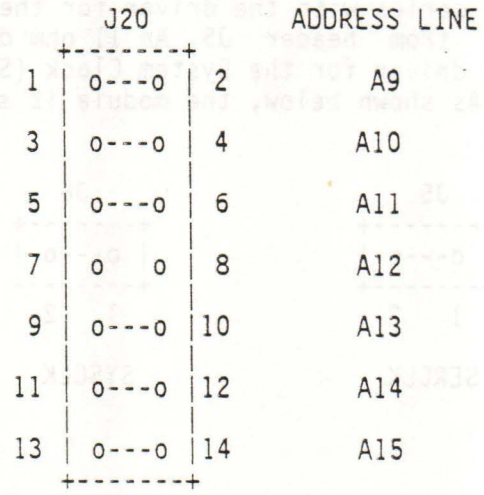
2.3.1.12 Clock Damping Shorting Select Headers (J5,J6). An 11 ohm damping resistor may be placed in series with the driver for the Serial Clock (SERCLK) by removing the jumper from header J5. An 11 ohm damping resistor may be placed in series with the driver for the System Clock (SYSCLK) by removing the jumper from header J6. As shown below, the module is shipped with jumpers on the headers.



2.3.1.13 System Controller Select Header (J7). This module may be selected as the system controller by installing all four jumpers on the header as shown below. If the module is not to be the system controller, all four jumpers must be removed from the header and header J4 pins 11 and 12 jumpered. The module is factory-configured as the system controller. If the bus arbiter is disabled, bus arbitration signals must be configured on the backplane as though the controller was an empty slot as shown in paragraph 2.4.4. The IACK bypass jumper must remain open.



2.3.1.14 I/O Base Address Select Header (512 Byte Boundaries) (J20). The address line must be low to correspond with a jumper installed. As shown below, the base address is FF1000.



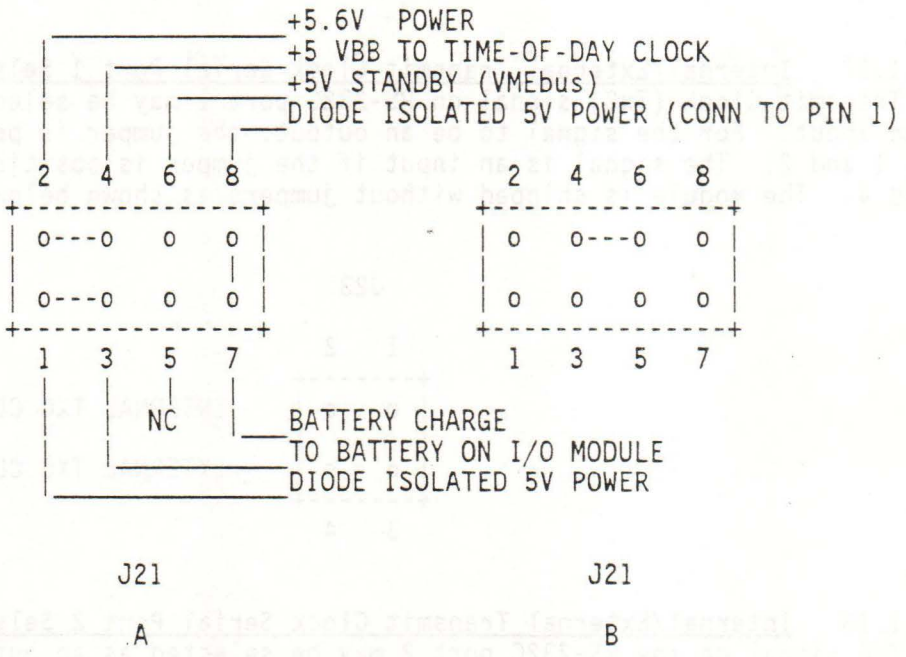
JUMPER IN = ADDRESS LINE LOW

DEFAULT SHOWN = 10XX WITHIN SHORT ADDRESSING RANGE
AM CODES = 2D OR 29

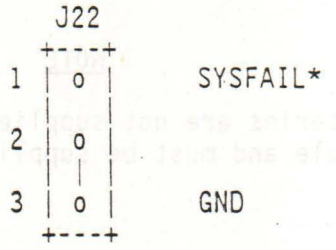
2.3.1.15 Time-of-Day Clock Power Select and Battery Charge Header (J21). Header J21 is used to select the method of powering the time-of-day clock. As shown in illustration A below, the normal configuration powers the time-of-day clock from system power while the system is ON and from the backup batteries while the system is OFF. As shown in illustration A, installing a jumper between pins 7 and 8 allow the backup batteries to be charged while the system is ON. Illustration B shows the jumper position to power the time-of-day clock from the +5V STANDBY on the VMEbus. The charge voltage is limited to 5.6 Vdc and the charge current limited to approximately 60 mA.

NOTE

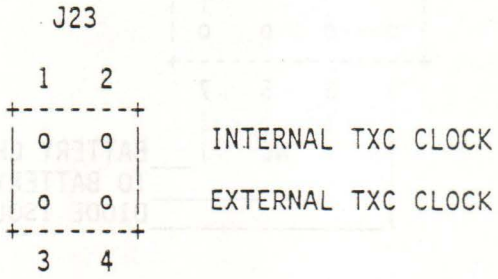
Batteries are not supplied with the I/O module and must be supplied by the user.



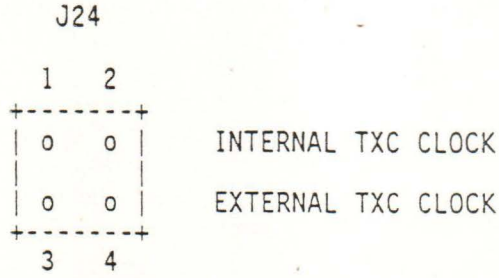
2.3.1.16 System Fail (SYSFAIL*) or GND Select for Interrupt Source Header (J22). Header J22 allows the user to enable the input to the Bus Interrupt Module (BIM) to be held low to provide for one software controlled global interrupt. The user may select the SYSFAIL* line to generate a global system failure interrupt. When the jumper is positioned between pins 1 and 2, the SYSFAIL* line is activated. The BIM interrupt is enabled when the jumper is positioned between pins 2 and 3. As shown below, the module is shipped with the SYSFAIL* line activated.



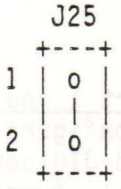
2.3.1.17 Internal/External Transmit Clock Serial Port 1 Select Header (J23). The Transmit Clock (TxC) signal on RS-232C port 1 may be selected as an output or an input. For the signal to be an output, the jumper is positioned between pins 1 and 2. The signal is an input if the jumper is positioned between pins 3 and 4. The module is shipped without jumpers as shown below:



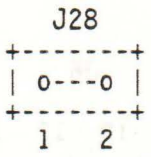
2.3.1.18 Internal/External Transmit Clock Serial Port 2 Select Header (J24). The TxC signal on the RS-232C port 2 may be selected as an output or an input. For the signal to be an output, the jumper is positioned between pins 1 and 2. The signal is an input if the jumper is positioned between pins 3 and 4. The module is shipped without jumpers as shown below:



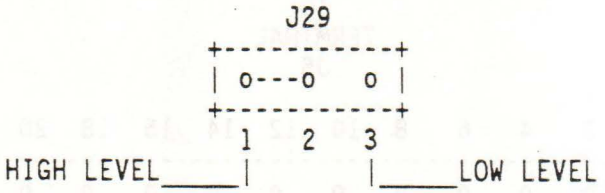
2.3.1.19 Display Blanking Enable Select Header (J25). A two-character Light Emitting Diode (LED) display is provided on the front panel of the controller module for user software applications. Its intended use is for a user-supplied diagnostics program to display status information. The display is updated by writing information to an onboard register. Header J25 works with section 8 of the front panel switch. With the jumper removed from the header, the switch has no effect. With the jumper installed, if the switch is OFF (open), the displays operate normally. If the switch is ON (closed), the displays are blanked (no display). If the display is not blanked by J25 and switch section 8, software may control the blanking by writing to the blanking register -- D3 = 0 = OFF; D3 = 1 = ON. Refer to the I/O memory map for address. Reset turns the display on if blanked by software. As shown below, the module is shipped with the jumper installed.



2.3.1.20 RESET Switch Disable Select Header (J28). The front panel RESET switch on the controller module may be disabled. The switch is disabled when the jumper is removed from the header. As shown below, the module is shipped with the jumper installed.



2.3.1.21 Printer Acknowledge Level Select Header (J29). Header J29 is provided as a means of selecting the high level or low level of the printer acknowledge signal. The module is shipped with the jumper installed between pins 1 and 2 (high level selected). The low level is selected by positioning the jumper between pins 2 and 3.



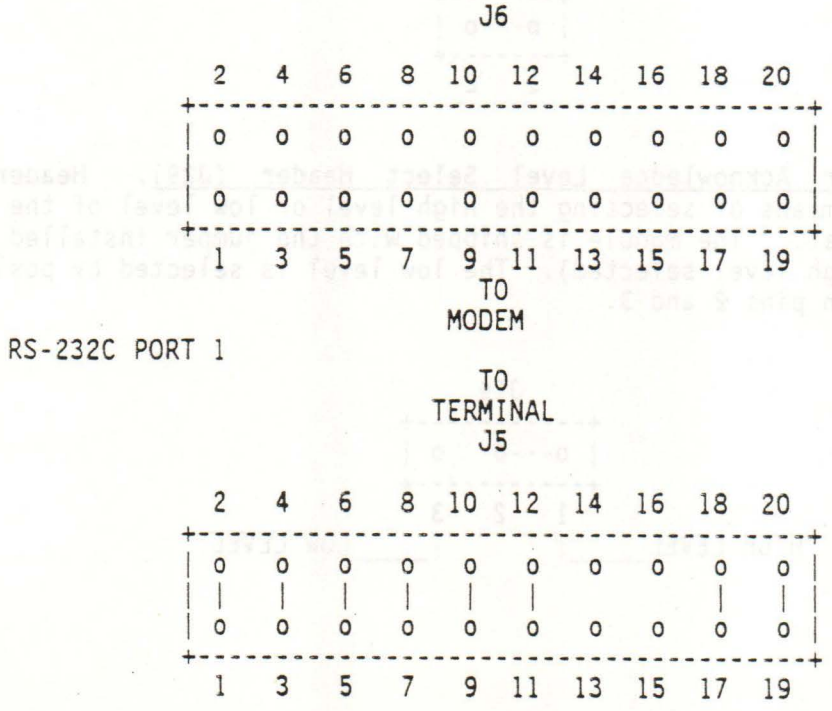
NOTE

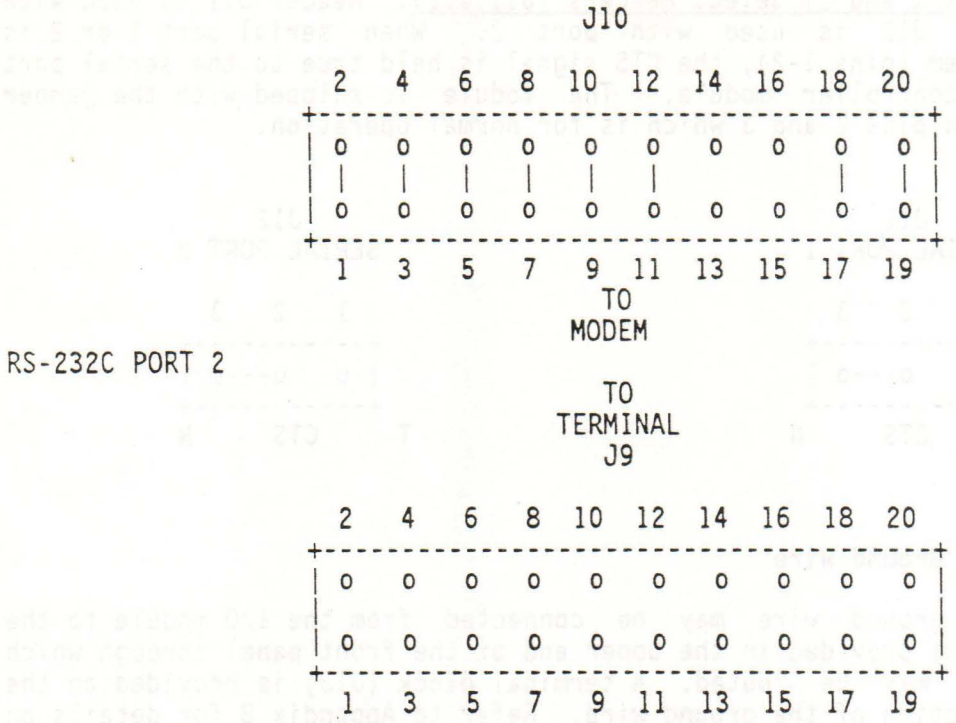
The printer acknowledge flag register latches the acknowledge signal from the printer and must be cleared by reading the printer strobe register. If the printer is still holding the acknowledge signal, the flag does not clear. The correct sequence is: 1. clear acknowledge, 2. check acknowledge flag, 3. if not clear, go back to 1.

2.3.2 I/O Module Headers

The configuration options of the I/O module headers are discussed in the following paragraphs.

2.3.2.1 To Terminal/To Modem (Port 1 and 2) Select Headers (J5,J6,J9,J10). Headers J5 and J6 are used to configure serial port 1 to interface with a terminal or a modem. Headers J9 and J10 perform the same function for serial port 2. To interface with a terminal, jumpers must be installed on pins 1-2, 3-4, ... through 11-12 and 17-18, 19-20 on header J5 for port 1 (J9 for port 2). Similarly, to interface with a modem, install jumpers on pins 1-2, 3-4, ... through 11-12 and 17-18, 19-20 on header J6 for port 1 (J10 for port 2). Jumpers on J5 or J6 and J9 or J10 pins 13-14 and 15-16 should be installed only for synchronous operation. The module is shipped with port 1 configured to terminal and port 2 configured to modem as shown below:





When configured to modem, the DCD signal may be held true to the serial port device on the controller module by repositioning jumpers. Reposition the jumper on port 1 header J6 pins 17-18 to port 1 header J5 pins 17-18. Reposition the jumper on port 2 header J10 pins 17-18 to port 2 header J9 pins 17-18.

2.3.2.2. <u>DSR (Port 1 and 2) Select Headers (J7,J8)</u>. Header J7 is used with port 1. Header J8 is used with port 2. When serial port 1 or 2 is configured to modem (jumper on pins 1-2), the DSR signal is held true to the serial port device on the controller module. The module is shipped with the jumper positioned between pins 2 and 3 which is for normal operation.

2.3.2.3 CTS (Port 1 and 2) Select Headers (J11,J12). Header J11 is used with port 1. Header J12 is used with port 2. When serial port 1 or 2 is configured to modem (pins 1-2), the CTS signal is held true to the serial port device on the controller module. The module is shipped with the jumper positioned between pins 2 and 3 which is for normal operation.

2.3.3 I/O Module Ground Wire

A user-supplied ground wire may be connected from the I/O module to the chassis. A hole is provided in the upper end of the front panel through which the ground wire may be routed. A terminal block (J13) is provided on the module for connection of the ground wire. Refer to Appendix B for details on RS-232C grounding.

2.4 INSTALLATION

The following paragraphs discuss installation of batteries, battery/reset cables interface cable, and installation of the modules into the chassis. Ensure that EPROM and/or RAM memory devices are installed and configured and that all other headers on both modules are configured for desired operation.

2.4.1 Battery Installation

Batteries for time-of-day clock backup operation must be supplied by the user. The batteries are to be installed on the I/O module. Batteries should be nickel-cadmium, 1.2 volt, AA size. Four batteries are required. Be sure to observe polarity when inserting battery leads into the module. Pads on the module are designated BT1, BT2, BT3, and BT4.

An external two-pin battery connection (BATT) is provided on the front panel of the I/O module. The connection is pins 1 and 2 on the MVME701 4-pin or on the MVME701A 9-pin connector. This connection may be used for +5 volt battery power input instead of the batteries installed on the module.

CAUTION

DO NOT USE BOTH BATTERY INSTALLATIONS AT THE SAME TIME AS DAMAGE TO THE MODULE COMPONENTS MAY RESULT.

2.4.2 Interface Cable Installation

The interface cable interconnects the controller module and the I/O module. The cable may be installed on the card cage rails or as follows. To install the interface cable proceed as follows:

a. Lay the controller module on a clean surface with component side up.

b. Lay the I/O module on top of the controller module with component side up and front panels together.

c. Connect the flat ribbon interface cable to connector P2 on the controller module. Be sure to orient pin one of the cable with pin one of the connector.

d. Connect the other end of the interface cable to connector P1 on the I/O module. Be sure to orient pin one of the cable with pin one of the connector.

e. Modules are now ready for installation into a VME chassis or any double-wide VME card cage.

2.4.3 Module Installation

Now that the modules are ready for installation, proceed as follows:

a. Turn all equipment power OFF.

CAUTION

INSERTING/REMOVING MODULES WHILE POWER IS APPLIED COULD RESULT IN DAMAGE TO MODULE COMPONENTS.

b. This installation requires two card slots.

c. Carefully pick up the two-card combination and insert combination into the first double-wide card slot (the controller must be the first module in the string ahead of an Microprocessor (MPU) or Computer (CPU) module).

d. Be sure controller module is seated properly in the connectors on the backplane. Fasten modules in card cage with screws provided.

2.4.4 VMEmodule Chassis Backplane Daisy-Chained Headers

Whenever there are any empty slots between modules in the VMEmodule chassis, jumpers must be installed on the backplane headers at the empty slot locations to continue the bus arbitration signals and the acknowledge signals across the empty slot(s). Refer to paragraph 2.3.1.13 for information on bus grant signals. The table below is a list of backplane pins to be daisy-chained across the empty slot(s).

BACKPLANE PIN NO.			REMARKS		
A21	to	A22	IACKIN*	to	IACKOUT*
B4	to	B5	BG0IN*	to	BG0OUT*
B6	to	B7	BG1IN*	to	BG1OUT*
B8	to	B9	BG2IN*	to	BG2OUT*
B10	to	B11	BG3IN*	to	BG3OUT*

2.4.5 Printer Connection

A Centronics-type printer may be attached to the I/O module through a 50-pin cable (MVME701 only) connected to the PRINTER connector. A printer cable, Motorola part number M68KVMPRTCE, may be used (for the MVME701 only). A standard 36-pin printer cable (obtainable from many sources) is used with the MVME701A connected to the PRINTER connector. Pin one is located at the bottom of the connector with the module installed.

2.4.6 Terminal Connection

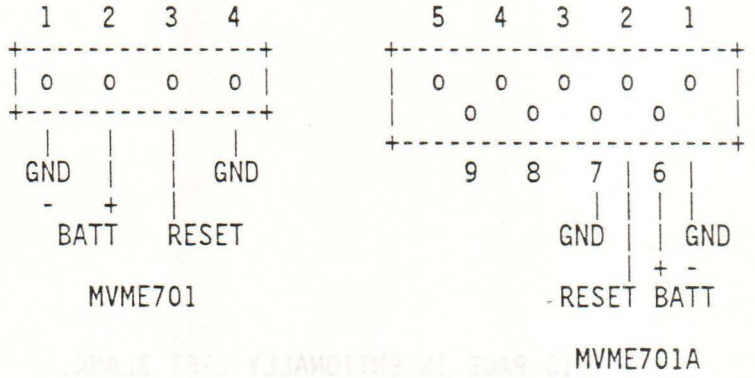
Serial port 1 is factory-configured for terminal operation. A 25-pin RS-232C cable may be connected to SER PORT 1 on the I/O module with the other end connected to a compatible terminal.

2.4.7 Modem or Host Computer Connection

Serial port 2 is factory-configured for modem or host computer operation. 25-pin RS-232C cable may be connected to SER PORT 2 on the I/O module with the other end connected to a compatible host computer or a modem.

2.4.8 Remote Reset Connection

A remote RESET switch may be connected to the 4-pin connector on the MVME701 or the 9-pin connector on the MVME701A. A normally open switch must be used with a two wire cable connected to the connector. See illustration below for connections:



2.4.9 Remote +5V Battery

A part of the 4-pin or 9-pin connector includes two pins that provide a means to power the time-of-day clock from a remote +5V battery. See illustration above for connections.

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CHAPTER 3

OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the necessary information to use the controller module and I/O module in a system configuration.

3.2 CONTROLS AND INDICATORS

The controller module has a RESET switch, an eight section readable switch, a FAIL indicator, a RUN indicator, and a two segment display indicator.

3.2.1 RESET Switch

The reset performed by the RESET switch is a system-level function. The RESET switch may be disabled by removing a jumper from header J28. Depressing the RESET switch activates the reset.

An optional remote reset may be connected to the I/O module (refer to paragraph 2.4.8.).

Depressing the RESET switch enables the RESET signal to generate the System Reset (SYSRESET*), which is sent via the VMEbus, to the other modules in the system.

3.2.2 RUN Indicator

The RUN indicator is lit whenever the System Fail (SYSFAIL*) line is high and the controller module is operational.

3.2.3 FAIL Indicator

The FAIL indicator is lit whenever the controller module detects the SYSFAIL* line low on the VMEbus and the controller module is not operational.

3.2.4 User Status Display

The user status display indicator is provided for user software applications. Its intended use is for a user-supplied diagnostics program to display status information. The display is updated by writing information to an onboard register. The display may be blanked by section 8 of the readable switch or by software (refer to paragraph 2.3.1.19). If blanked by software, a system reset turns the display on. D7-D4 is latched and displayed in the top display. D3-D0 is latched and displayed in the bottom display. Refer to the I/O memory map for address.

3.2.5 User 8-Section Software-Readable Switch

The piano type 8-section switch on the front panel of the controller module is a software readable switch. The user may include the functions of this switch in the software program. Section 8 of this switch may also function as blanking for the user status display. Refer to the I/O memory map for address.

3.3 I/O MEMORY MAP

The I/O memory is shown below:

ADDRESS	FUNCTION
FFXX00 - FFXX3F	MPCC1 64 BYTES ODD BYTES ONLY
FFXX40 - FFXX7F	MPCC2 64 BYTES ODD BYTES ONLY
FFXX80 - FFXX9F	PRINTER 32 BYTES ODD BYTES ONLY
FFXX81	(WRITE D0-D7) PRINTER DATA REGISTER
FFXX81	(READ) - PUTS FF INTO DATA OUT REGISTER
FFXX83	(WRITE D3) PRINTER STROBE REGISTER
FFXX83	(READ) - CLEARS ACKNOWLEDGE FLAG AND PRINTER IRQ
FFXX85	(WRITE) HARDWARE BUFFER CONFLICT
FFXX85	(READ) - PRINTER STATUS D0 = SELECT FROM PRINTER D1 = BUSY FROM PRINTER D2 = FAULT FROM PRINTER D7 = ACKNOWLEDGE FROM PRINTER
FFXX87	(WRITE D3) PRINTER INPUT PRIME
FFXX87	(READ) - NO OPERATION
FFXX89	(WRITE) - NO OPERATION
FFXX89	(READ D7) STATUS OF SYSFAIL* ON VMEbus
FFXX8B	(WRITE D3) BLANKING TO FRONT PANEL (0 = OFF)
FFXX8B	(READ) - NO OPERATION
FFXXA0 - FFXXBF	FRONT PANEL DISPLAY - 32 BYTES ODD ONLY (WRITE ONLY)
FFXXA0 - FFXXBF	FRONT PANEL SWITCH - 32 BYTES ODD ONLY (READ ONLY)
FFXXC0 - FFXXDF	BIM 1 - 32 BYTES ODD ONLY
FFXXE0 - FFXXFF	BIM 2 - 32 BYTES ODD ONLY
FFX100 - FFX17F	TIME-OF-DAY CLOCK - 128 BYTES ODD ONLY

XX = 00---> FE ON 512 BYTE BOUNDARIES

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CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides the overall block diagram level description for the controller module and the I/O module. The general description provides a overview of the modules, followed by a detailed description of each section of the modules. Figure 4-1 shows the block diagram of the controller module. Figure 4-2 shows the block diagram of the I/O module.

4.2 GENERAL DESCRIPTION

In normal operation, the controller module provides all the system controller functions required for a VMEbus system. For time-of-day accesses, the system software reads the time from the time-of-day clock. Two serial ports may be used by the system software for interfacing to terminals, modems, or data links. Hard copy output is available via the Centronics-type printer port. EPROM/RAM sockets may be used as general system memory or to hold debug and/or diagnostics programs and scratch pad RAM.

In many multiprocessor systems, it is desirable for a process executing in one MPU module to interrupt a process being executed by another MPU module. The global interrupter (complete with semaphore) on the controller module provides this global interrupting capability.

4.3 BLOCK DIAGRAM DESCRIPTION OF CONTROLLER MODULE

The block diagram of the controller module is shown in Figure 4-1. The controller operates through the following functional logic blocks.

- Time-of-day clock
- EPROM/RAM sockets
- Serial ports
- Centronics parallel printer port
- Global interrupter
- Battery backup
- Bus arbiter
- System clock generator
- Serial bus clock generator
- Bus time-out generator
- Power up reset
- RESET switch
- VMEbus interface
- User display
- Front panel lights

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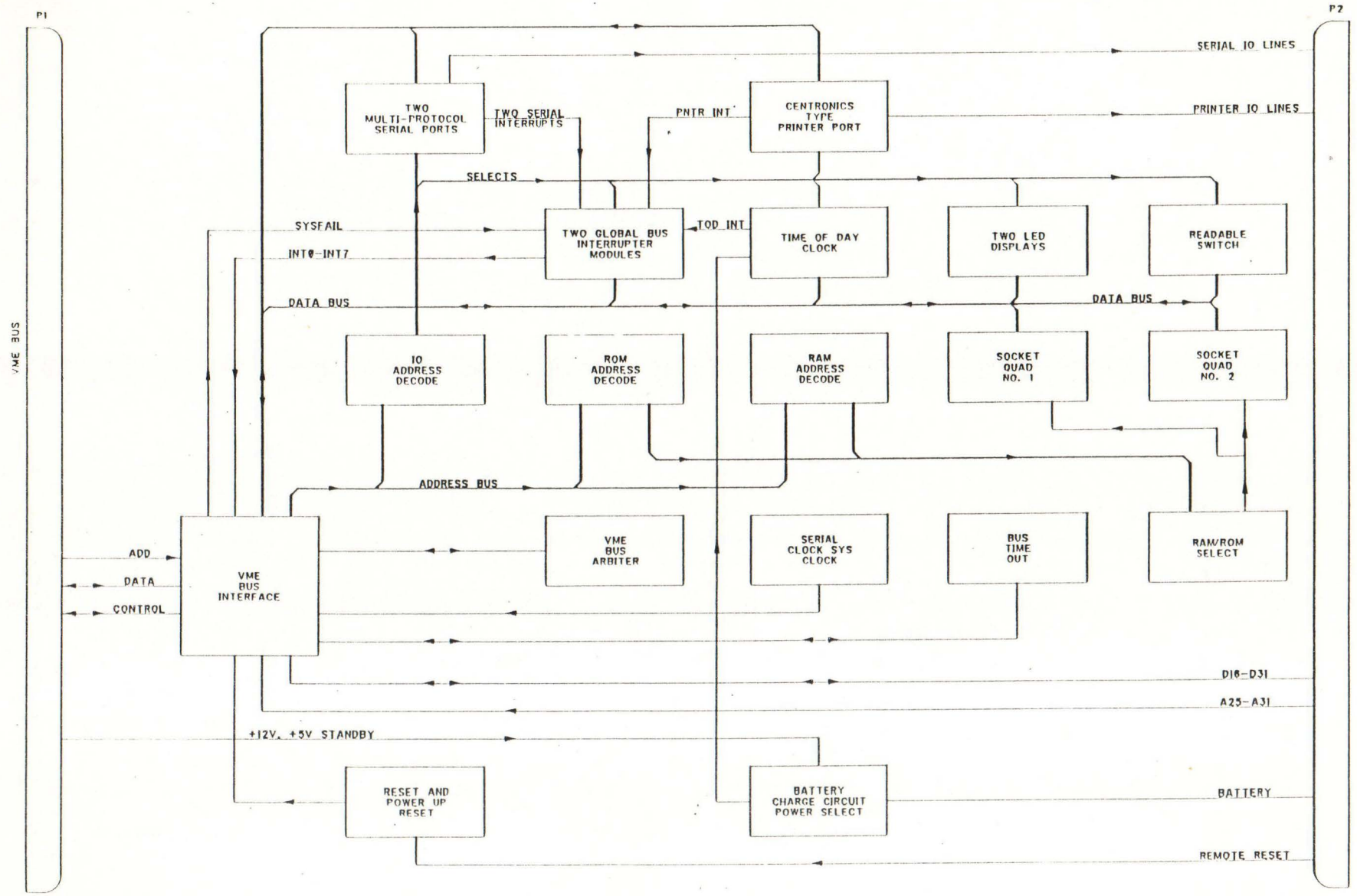


FIGURE 4-1. Controller Module Block Diagram

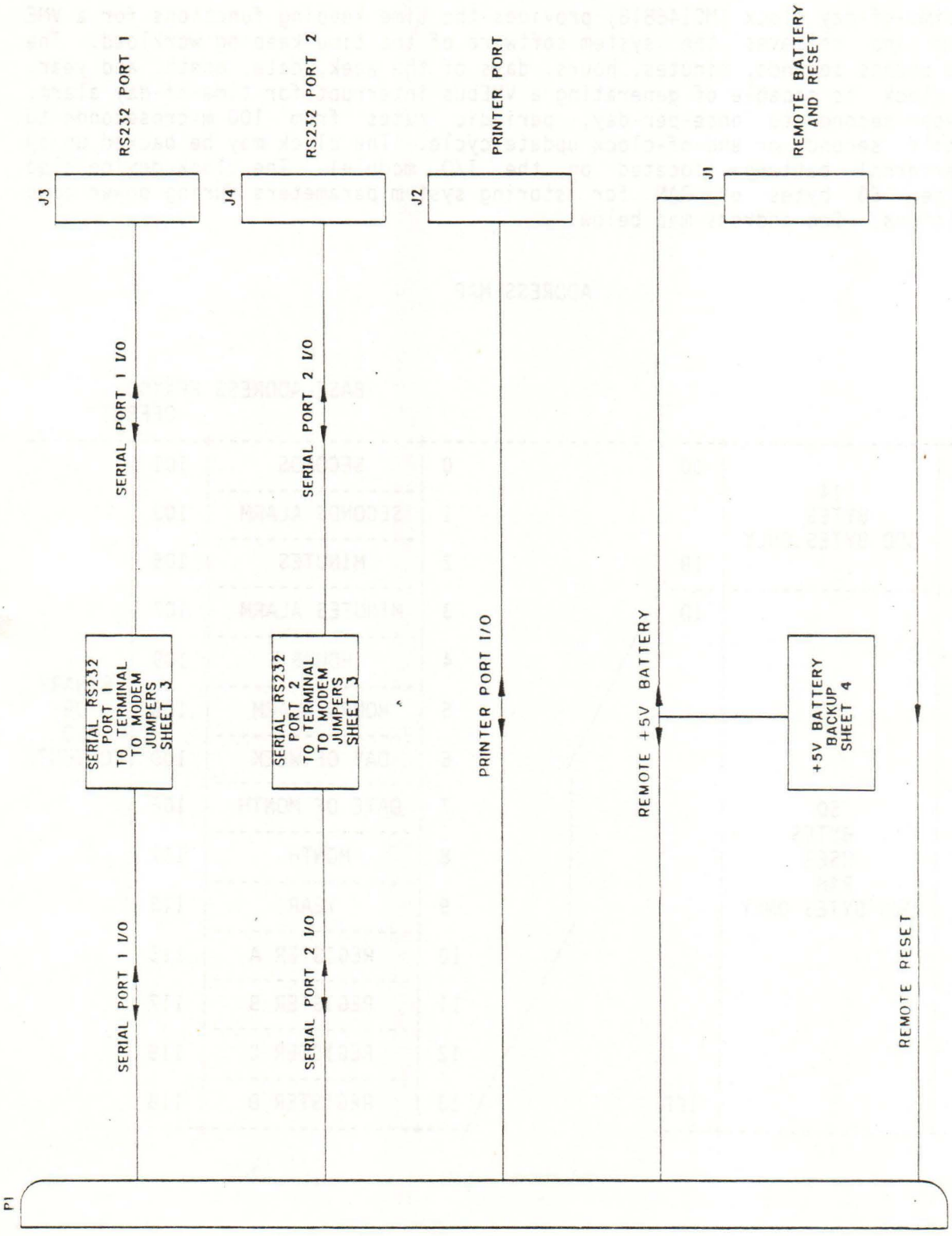
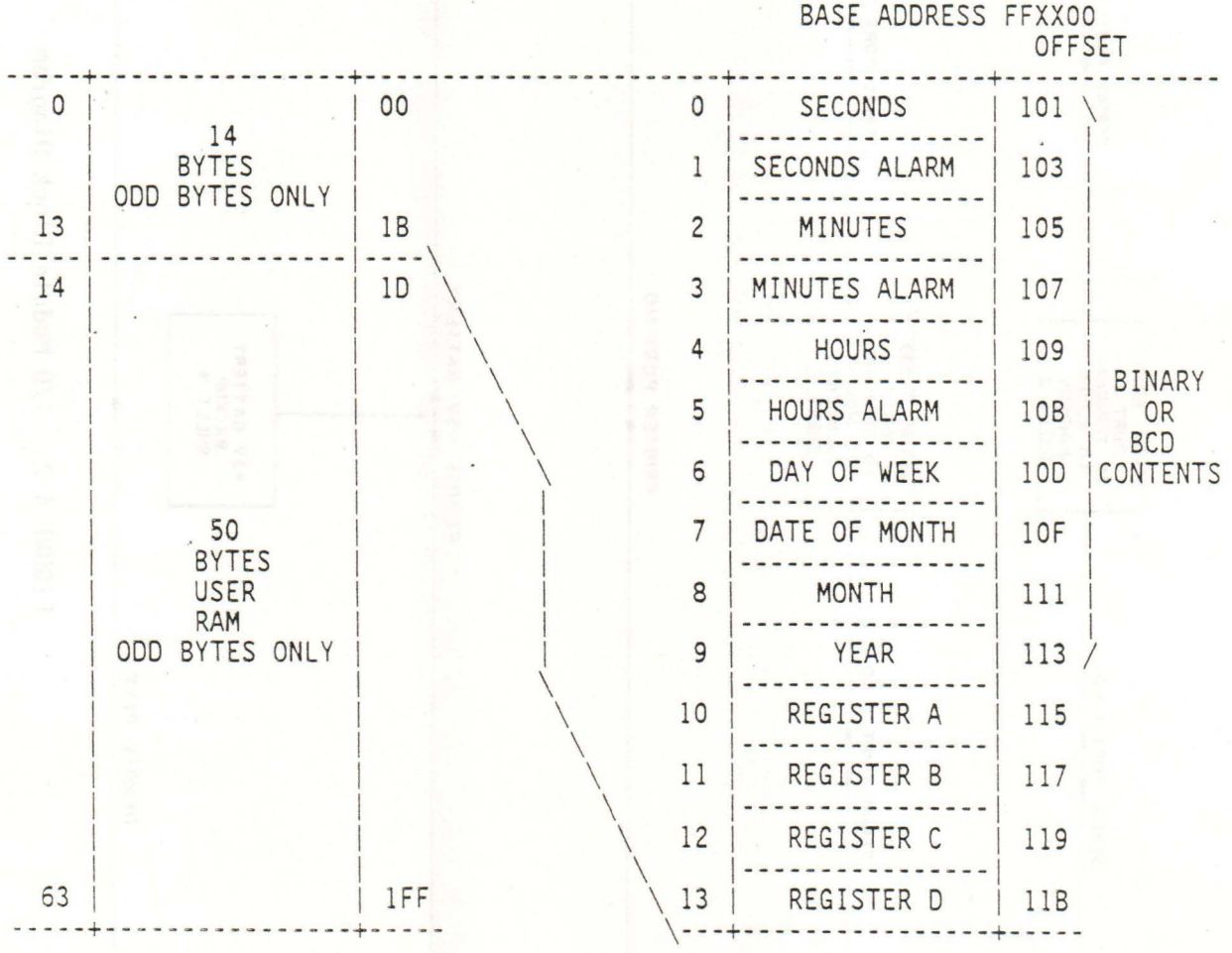


FIGURE 4-2. I/O Module Block Diagram

4.3.1 Time-of-Day Clock

The time-of-day clock (MC146818) provides the time keeping functions for a VME system and relieves the system software of the time keeping workload. The clock counts seconds, minutes, hours, days of the week, date, month, and year. The clock is capable of generating a VMEbus interrupt for time-of-day alarm, once-per-second to once-per-day, periodic rates from 100 microseconds to one-half second, or end-of-clock update cycle. The clock may be backed up by an external battery (located on the I/O module). The clock device also provides 50 bytes of RAM for storing system parameters during power down conditions. See address map below:

ADDRESS MAP



4.3.2 EPROM/RAM Sockets

Eight, 28-pin sockets may be populated by the user with 24-pin or 28-pin RAM, or EPROM devices. RAM and EPROM populations may be mixed. RAM's are loaded into the sockets starting at XU25, XU33, XU28, XU36 (RAM quad 1). EPROM's are loaded into the sockets starting at XU8, XU16, XU11, XU19 (EPROM quad 1). Socket configuration headers are provided to configure each socket quad for RAM or EPROM and the type of device.

The VMEbus base address for accessing EPROM/RAM is set by jumper position on the appropriate headers. If both socket quads are populated with RAM, the RAM base address is set with The RAM header, and the RAM addressing becomes contiguous across the socket quad boundary. The EPROM base address header is ignored. If both socket quads are populated with EPROM, the base address is set with the EPROM headers, and the addressing becomes contiguous across the socket quad boundary. When both RAM and EPROM populations are used, the RAM base address is set by the RAM header and the EPROM base address is set by the ROM/EPROM header. If EPROM devices are installed in EPROM quad 1, they are capable of being accessed when a bus master initiates a VMEbus transfer using Address Modifier (AM) code 1E. If EPROM devices are installed in EPROM quad 2, they are capable of being accessed when a bus master initiates a VMEbus transfer using AM code 16. When this type of access occurs, no other devices on the module are accessed and the EPROM base address circuitry is disabled. This feature may be disabled by removing the jumpers at J12. Refer to paragraph 2.3.1.9.

The EPROM/RAM devices supported by the controller module are listed in Table 2-1. Separate Data Transfer Acknowledge (DTACK*) timing headers are provided for separately timing the accesses from RAM or EPROM. This allows both fast RAM's and slow EPROM devices to be used on the same module without impacting the performance of the faster parts.

4.3.3 Serial Ports

Two independent, Multi-Protocol Communications Controllers (MPCC) (R68560) interface with connector P2 on the controller module and the RS-232C serial ports on the I/O module. The headers normally associated with configuring the serial ports as TO TERMINAL or TO MODEM are incorporated on the I/O module.

Serial ports Interrupt Request (IRQ*) line goes into Bus Interrupter Module (BIM 1) (MC68153). Interrupt (INT0) and INT1 are the BIM control register and BIM vector register as shown below:

Serial port 1	BIM	control register = FFXXC1
	BIM	vector register = FFXXC9
Serial port 2	BIM	control register = FFXXC3
	BIM	vector register = FFXXCB

Interrupts can be enabled to the VMEbus by writing to the BIM control register (refer to the MC68153 Data Sheet).

NOTE

The BIM must be initialized for external vector in control register 0 and 1 because the R68560 supplies the interrupt vector. If the BIM is initialized for internal vector, both devices supply the vector, which causes a buffer conflict.

A sample initialization procedure for asynchronous mode 9600 baud and no interrupts is shown below:

```
00---> RCR    Receiver control register
80---> TCR    Transmitter control register
C0---> SICR   Serial interface control register
1E---> PSR2   Protocol select register 2
8B---> BRDR1  Baud rate divider register 1
00---> BRDR2  Baud rate divider register 2
1D---> CCR    Clock control register
```

Now the MPCC is ready to transmit and receive characters.

The following table lists port 1 and port 2 addresses, reset values and MPCC registers.

HEX ADDRESS PORT 1	HEX ADDRESS PORT 2	RESET VALUE	ASYNCHRONOUS MODE 9600 NO INTERRUPTS	MPCC REGISTER
FFXX01	FFXX41	00		RSR
FFXX03	FFXX43	01	00	RCR
FFXX05	FFXX45			RDR
FFXX07	FFXX47	00		
FFXX09	FFXX49	0F		RIVNR
FFXX0B	FFXX4B	00		RIER
FFXX0D	FFXX4D	00		
FFXX0F	FFXX4F	00		
FFXX11	FFXX51	80		TSR
FFXX13	FFXX53	01	80	TCR
FFXX15	FFXX55			TDR
FFXX17	FFXX57	00		
FFXX19	FFXX59	0F		TIVNR
FFXX1B	FFXX5B	00		TIER
FFXX1D	FFXX5D	00		
FFXX1F	FFXX5F	00		
FFXX21	FFXX61	00		SISR
FFXX23	FFXX63	00	C0	SICR
FFXX25	FFXX65			
FFXX27	FFXX67			
FFXX29	FFXX69	0F		SIVNR
FFXX2B	FFXX6B	00		SIER
FFXX2D	FFXX6D	00		
FFXX2F	FFXX6F	00		
FFXX31	FFXX71	00		PSR1
FFXX33	FFXX73	00	1E	PSR2
FFXX35	FFXX75	00		AR1
FFXX37	FFXX77	00		AR2
FFXX39	FFXX79	01	8B	BRD1
FFXX3B	FFXX7B	00	00	BRD2
FFXX3D	FFXX7D	00	1D	CCR
FFXX3F	FFXX7F	04		ECR

XX = 00---> FE

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the baud rate divider circuit. BRDR1 contains the Least Significant Half (LSH) and BRDR2 contains the Most Significant Half (MSH). With an 8 MHz External Crystal (EXTAL) input, standard bit rates can be selected using a combination of prescaler divider (in the Clock Control Register (CCR)) and baud rate divider values shown in Table 4-1. A system reset resets the MPCC.

TABLE 4-1. Standard Baud Selection

DESIRED BAUD RATE	K VALUE	PRESCALER DIVIDER	BAUD RATE DIVIDER DECIMAL	BAUD RATE DIVIDER HEXADECIMAL MSH	LSH
			ASYNCHRONOUS MODE		
50	2	3	26,667	68	2B
75	2	2	26,667	68	2B
110	2	3	12,121	2F	59
135	2	2	14,815	39	DF
150	2	3	8,889	22	B9
300	2	2	6,667	1A	0B
1200	2	3	1,111	04	57
1800	2	2	1,111	04	57
2400	2	2	883	03	41
3600	2	2	556	02	2C
4800	2	3	278	01	16
7200	2	2	278	01	16
9600	2	3	139	00	8B
19200	2	2	104	00	68
38400	2	2	52	00	34
			ISOCHRONOUS AND SYNCHRONOUS		
50	1	3	53,333	D0	55
75	1	2	53,333	D0	55
100	1	3	24,242	5E	B2
135	1	2	29,630	73	BE
150	1	3	17,778	45	72
300	1	2	13,333	34	15
1200	1	3	2,222	08	AE
1800	1	2	2,222	08	AE
2400	1	2	1,667	06	83
3600	1	2	1,111	04	57
4800	1	3	556	02	2C
7200	1	2	556	02	2C
9600	1	3	278	01	16
19200	1	2	208	00	D0
38400	1	2	104	00	68

PRESCALER DIVIDER: 0 = DIVIDE BY 2
1 = DIVIDE BY 3

K = 1 FOR ISOCHRONOUS AND SYNCHRONOUS
2 FOR ASYNCHRONOUS

4.3.4 Centronics Parallel Printer Port

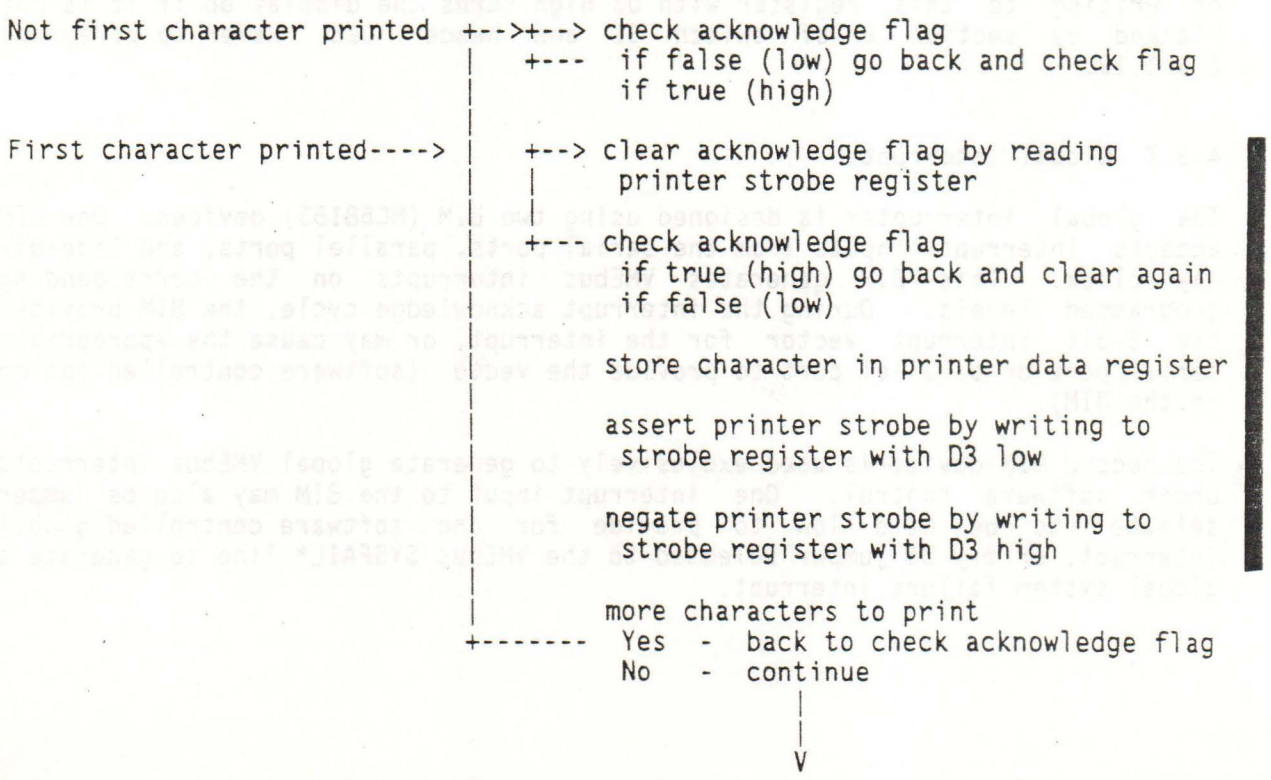
The parallel I/O port is designed to operate with a Centronics printer. The signal lines are buffered and are available at connector P2. The printer port consists of an 8-bit data register, a strobe output, an input prime, output registers, a acknowledge input, and a 4-bit status register.

The printer strobe register and the input prime register are both initialized (set high) by reset. Input prime is an input signal that clears the printer buffer and initializes the logic. Not used on all printers. The printer addresses are listed below:

```
FFXX81    (Write D0-D7) printer data register
FFXX81    (Read) - puts FF into data out register
FFXX83    (Write D3) printer strobe register
FFXX83    (Read) - clears acknowledge flag and printer IRQ
FFXX85    (Write) hardware buffer conflict
FFXX85    (Read) - printer status
             D0 = select from printer
             D1 = busy from printer
             D2 = fault from printer
             D7 = acknowledge from printer
FFXX87    (Write D3) printer input prime
FFXX87    (Read) - no operation

FFXX00   XX = 00-FE on 512 byte boundaries
```

To output a character to a printer:



NOTE

The printer acknowledge flag register latches the acknowledge signal from the printer and must be cleared by reading the printer strobe register. If the printer is still holding the acknowledge signal, the flag does not clear. The correct sequence is: 1. clear acknowledge, 2. check acknowledge flag, 3. if not clear, go back to 1.

The printer acknowledge can be selected to either level thus permitting the use of this interface on Data Products and other printers. Refer to paragraph 2.3.1.21.

4.3.5 SYSFAIL Register

The SYSFAIL* status register (FFXX89) is provided to read the status of the VMEbus SYSFAIL* signal. D7 is low if SYSFAIL* is low. D7 is high if SYSFAIL* is high.

4.3.6 User Display Blanking Register

The display blanking register is a write only register to enable the user display to be blanked (turned off) by writing to FFXX8B with D3 low. A reset or writing to this register with D3 high turns the display on if it is not blanked by section 8 of switch S1 and header J25. Refer to paragraph 2.3.1.19.

4.3.7 Global Interrupter

The global interrupter is designed using two BIM (MC68153) devices. One BIM accepts interrupt inputs from the serial ports, parallel ports, and time-of-day clock. This BIM generates VMEbus interrupts on the corresponding programmed levels. During the interrupt acknowledge cycle, the BIM provides the 8-bit interrupt vector for the interrupt, or may cause the appropriate serial port or parallel port to provide the vecto (software controlled option in the BIM).

The second BIM device is used exclusively to generate global VMEbus interrupts under software control. One interrupt input to the BIM may also be jumper selected to be held low to provide for one software controlled global interrupt, or may be jumper selected to the VMEbus SYSFAIL* line to generate a global system failure interrupt.

The MC68153 register model is shown below:

MC68153 REGISTER MODEL

ADDRESS BIM1	ADDRESS BIM2	FLAG	FLAG AUTO-CLEAR	EXTERNAL/INTERNAL	INTERRUPT ENABLE	INTERRUPT AUTO-CLEAR	INTERRUPT LEVEL			REGISTER NAME	BIM1	BIM2
FFXXC1	FFXXE1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 0	SERIAL PORT 1	SYSFAIL/GND
FFXXC3	FFXXE3	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 1	SERIAL PORT 2	GND
FFXXC5	FFXXE5	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 2	TOD CLOCK	GND
FFXXC7	FFXXE7	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 3	PRINTER	GND
FFXXC9	FFXXE9	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 0	NOT USED	SYSFAIL/IPC
FFXXCB	FFXXEB	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 1	NOT USED	IPC
FFXXCD	FFXXED	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 2	TOD CLOCK	IPC
FFXXCF	FFXXEF	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 3	PRINTER	IPC
		7	6	5	4	3	2	1	0			
		REGISTER BIT										

NOTE

When using the serial port interrupts, the BIM must be initialized for external vector in control register 0 and 1 because the R68560 supplies the interrupt vector. If the BIM is initialized for internal vector , both devices supply the vector, which causes a buffer conflict.

4.3.8 Battery Backup

An external battery may be connected to the controller module through the P2 connector to provide battery backup power for the time-of-day clock. These batteries may be located on the I/O module. Headers are provided for selecting power backup from the external batteries, +5 Vdc standby from the VMEbus, or +5 Vdc from the VMEbus. Jumper selectable battery charging is provided when system power is applied to the controller module.

4.3.9 Bus Arbiter

The bus arbiter arbitrates requests and grants bus mastership on four levels. If the level of the current bus master is lower than the current bus request, the bus arbiter initiates a bus clear.

4.3.10 System Clock Generator

The system clock generator provides the 16 MHz system clock signal on the VMEbus. The 16 MHz clock signal is derived from the 32 MHz oscillator.

4.3.11 Serial Bus Clock Generator

The serial bus clock generator provides the 4 MHz nonsymetrical serial clock for the VMEbus. The signal is derived from the 32 MHz oscillator.

4.3.12 Bus Time-Out Generator

The bus time-out generator monitors VMEbus data transfer activities. If a transfer takes longer than the jumper selected time, the module generates a VMEbus error signal. The time-out starts when either data strobe goes low and clears when both data strobes are high. The time-out is jumper selectable from minimum of 2 to 160 microseconds to OFF.

4.3.13 Power-Up Reset

When system power is turned on, this circuit provides a system reset for 300 to 800 milliseconds minimum. Power down reset is not provided. Power backed up systems require an external power monitor to generate a ACFAIL and power down reset sequence as specified in the VMEbus specification.

4.3.14 RESET Switch

A system RESET switch is located on the front panel of the controller module. Depressing the switch generates a system reset on the VMEbus. The switch may be disabled by removing a jumper. The capability of resetting the system from a remote switch is provided through connector P2 from the I/O module.

4.3.15 VMEbus Interface

The VMEbus interface is slave mode only and supports 8-, 16-, and 32-bit data transfers. It also supports the 24-bit or 32-bit addressing mode. The cycle types supported are shown in Table 4-2.

4.3.16 User Display

A 2 character LED display is provided on the front panel for user software applications. Its intended use is for a user-supplied diagnostics program to display status information. The display is updated by writing information to an onboard register.

4.3.17 Front Panel Indicators

Front panel indicator lights display the overall system status. A red FAIL light illuminates whenever the controller module detects the SYSFAIL* line low on the VMEbus. A green RUN light illuminates when the SYSFAIL* line on the VMEbus is high.

TABLE 4-2. Supported Cycle Types

IACK*	LWORD*	AM CODE	CYCLE TYPE	ACCESSIBLE RESOURCES
X	L	X	32 bit data cycle	EPROM/RAM
L	H	X	Interrupt acknowledge	Interrupter or interrupting serial port (only D0-D7 are used)
H	X	09 0A 0D 0E	Extended addressing (32 bit) access modes	RAM/EPROM sockets - full addressing range
H	X	16 1E	User-defined mode-defined by MVME120 as alternate reset vector fetch	EPROM quad 2 EPROM quad 1
H	H	29 2D	Short I/O access	Serial ports, parallel port, time-of-day clock, global interrupter, user display (only D0-D7 are used)
H	X	39 3A 3D 3E	Standard addressing (24 bit) access mode	RAM/EPROM sockets - A24-A31 address compare is don't care

X = DON'T CARE L = LOW H = HIGH

4.4 BLOCK DIAGRAM DESCRIPTION OF I/O MODULE

The I/O module functions as the transition module for the controller module. The I/O module routes the printer signals, the two serial ports signals, the remote reset signal, and the remote battery power from the controller module to the connectors on the front panel. Only the signals on the two outer rows (A and C) on connector P2 of the controller module are connected to the I/O module. The port 1 and port 2 configuration headers are located on the I/O module. Pads to install the user-supplied batteries for backup of the time-of-day clock are provided.

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CHAPTER 5

SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the interconnection signals, parts list with parts location illustration, and schematic diagram for the controller module and the I/O module.

5.2 INTERCONNECT SIGNALS

The controller module interconnects with the VMEbus through connector P1. Connector P2 interconnects the controller module with the I/O module connector P1 through a cable.

5.2.1 Controller Module Connector P1 Interconnect Signals

Connector P1 is a standard DIN 41612 triple row, 64 pin male connector. All Motorola VMEbus specifications are met by the controller module. Table 5-1 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 5-1. Connector P1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A8	D00-D07	DATA bus (bits 0-7) - eight of 16 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
A9	GND	GROUND
A10	SYSCLK	SYSTEM CLOCK - a 16 MHz input signal used as a timing reference. This signal is provided by the VMEbus system controller.
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - input signal that indicates a data transfer on data bus lines D08-D15.
A13	DS0*	DATA STROBE 0 - input signal that indicates a data transfer on data bus lines D00-D07.
A14	WRITE*	WRITE - input signal that specifies the direction of data transfers.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A15	GND	GROUND
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - this output signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
A17	GND	GROUND
A18	AS*	ADDRESS STROBE - the falling edge of this input signal indicates a valid address is present on the address bus.
A19	GND	GROUND
A20	IACK*	INTERRUPT ACKNOWLEDGE - input signal that indicates a VME interrupt acknowledge cycle. The VME system controller has been interrupted on one of seven levels and is now acknowledging the specific interrupt with a service routine.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - IACKIN* and IACKOUT* form a daisy-chained acknowledge. The standard Motorola VMEbus backplane must have jumpers installed to continue the daisy-chained interrupt acknowledge beyond vacant card slots. This input signal is used when the controller module forms part of the daisy-chained interrupt acknowledge sequence.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - IACKIN* and IACKOUT* form a daisy-chained acknowledge. The standard Motorola VMEbus backplane must have jumpers installed to continue the daisy-chained interrupt acknowledge beyond vacant card slots. This input signal is used when the controller module forms part of the daisy-chained interrupt acknowledge sequence.
A23	AM4	ADDRESS MODIFIER (bit 4) - one of the three-state input lines that provide additional information about the address bus, such as size, cycle type, and/or data transfer bus master identification.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A24	A07	ADDRESS bus (bit 7) - one of 16 three-state input lines that specify an address in the memory map. Only the least significant 16 bits of the 23 associated VMEbus address lines are employed on the controller module.
A25	A06	ADDRESS bus (bit 6) - same as A07 on pin A24.
A26	A05	ADDRESS bus (bit 5) - same as A07 on pin A24.
A27	A04	ADDRESS bus (bit 4) - same as A07 on pin A24.
A28	A03	ADDRESS bus (bit 3) - one of 16 three-state input lines that specify an address in the memory map. During an interrupt acknowledge cycle, address bus lines A01-A03 are used to indicate the interrupt level that is being acknowledged.
A29	A02	ADDRESS bus (bit 2) - same as A03 on pin A28.
A30	A01	ADDRESS bus (bit 1) - same as A03 on pin A28.
A31	-12 VDC	-12 Vdc Power - used by the logic circuits on the controller module.
A32	+5 VDC	+5 Vdc Power - used by the logic circuits on the controller module.
B1	BBSY*	BUS BUSY - This signal is driven low when the controller module is the bus master. This signal is an input to the arbiter to indicate that the bus may be arbitrated.
B2	BCLR*	BUS CLEAR - input signal that causes the release of the mastership in the RBC mode.
B3,B4		Not used.
B5	BGOOUT*	BUS GRANT 0 OUT - bus-grant-in and bus-grant-out form a daisy-chained bus grant. When a bus-grant-in is received at the jumpered level and the MPU is not awaiting bus mastership, the bus-grant-out signal is true on the respective level.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B6		Not used.
B7	BG1OUT*	BUS GRANT 1 OUT - same as BG0OUT on pin B5.
B8		Not used.
B9	BG2OUT*	BUS GRANT 2 OUT - same as BG0OUT on pin B5.
B10		Not used.
B11	BG3OUT*	BUS GRANT 3 OUT - same as BG0OUT on pin B5.
B12-B15	BR0*-BR3*	BUS REQUEST (0-3) - the bus request at the jumpered level is true when the MPU requires bus mastership. When one or more bus request lines is true in the ROR mode, bus mastership is released. When the controller module is the system controller, bus request level three is monitored by the arbiter.
B16-B19	AM0-AM3	ADDRESS MODIFIER (bits 0-3) - same as AM4 on pin A23.
B20	GND	GROUND
B21	SERCLK	SERIAL CLOCK - a high level signal used to clock the serial communication bus.
B22		Not used.
B23	GND	GROUND
B24-B30	IRQ7*-IRQ1*	INTERRUPT REQUEST (7-1) - seven prioritized interrupt request inputs. Jumper enabled, level seven is the highest priority.
B31	+5V STDBY	+5Vdc STANDBY - this line supplies +5 Vdc to devices requiring battery backup.
B32	+5 VDC	+5 Vdc Power - same as +5 VDC on pin A32.
C1-C8	D08-D015	DATA bus (bits 8-15) - eight of 16 three-state bidirectional data lines that provide the data path between VMEbus master and slave.
C9	GND	GROUND

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C10	SYSFAIL*	SYSTEM FAIL - reflects state of FAIL bit in MCR and fail indicator. When enabled in MCR, this bidirectional signal generates an interrupt request.
C11	BERR*	BUS ERROR - an active low output signal that indicates an error has occurred during a data transfer cycle.
C12	SYSRESET*	SYSTEM RESET - the system controller provides this input signal that causes a board level reset on the controller module.
C13	LWORD*	LONGWORD - three-state driven signal to indicate that the current transfer is a 32-bit transfer.
C14	AM5	ADDRESS MODIFIER (bit 5) - same as AM4 on pin A23.
C15	A23	ADDRESS bus (bit 23) - same as A07 on pin A24.
C16	A22	ADDRESS bus (bit 22) - same as A07 on pin A24.
C17	A21	ADDRESS bus (bit 21) - same as A07 on pin A24.
C18	A20	ADDRESS bus (bit 20) - same as A07 on pin A24.
C19	A19	ADDRESS bus (bit 19) - same as A07 on pin A24.
C20	A18	ADDRESS bus (bit 18) - same as A07 on pin A24.
C21	A17	ADDRESS bus (bit 17) - same as A07 on pin A24.
C22	A16	ADDRESS bus (bit 16) - same as A07 on pin A24.
C23	A15	ADDRESS bus (bit 15) - same as A07 on pin A24.
C24	A14	ADDRESS bus (bit 14) - same as A07 on pin A24.
C25	A13	ADDRESS bus (bit 13) - same as A07 on pin A24.
C26	A12	ADDRESS bus (bit 12) - same as A07 on pin A24.
C27	A11	ADDRESS bus (bit 11) - same as A07 on pin A24.
C28	A10	ADDRESS bus (bit 10) - same as A07 on pin A24.
C29	A09	ADDRESS bus (bit 9) - same as A07 on pin A24.

TABLE 5-1. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C30	A08	ADDRESS bus (bit 8) - same as A07 on pin A24.
C31	+12 VDC	+12 Vdc Power - used by the logic circuits on the controller module.
C32	+5 VDC	+5 Vdc Power - same as +5 Vdc on pin A32.

5.2.2 Controller Module Connector P2 Interconnect Signals

Connector P2 is a standard DIN 41612 connector. Table 5-2 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 5-2. Connector P2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1	GND	GROUND
A2	RTS1	REQUEST TO SEND (Port 1) - RTS is supplied by the terminal to the modem when it is required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.
A3	DTR1	DATA TERMINAL READY (Port 1) - a signal from the terminal to the modem indicating that the terminal is ready to send or receive data.
A4	DCD1TT	DATA CARRIER DETECT (Port 1) - furnished by the modem to the terminal to indicate that a valid carrier is being received.
A5	SUP1	PULLUP LINE (Port 1) - an active pullup line activated by jumper arrangement on headers J7 or J11.
A6	RxC1	RECEIVE CLOCK (Port 1) - this line clocks input data from a terminal to a modem.
A7,A8,A9	GND	GROUND
A10	RTS2	REQUEST TO SEND (Port 2) - same as RTS1 on pin A2.

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A11	DTR2	DATA TERMINAL READY (Port 2) - same as DTR1 on pin A3.
A12	DCD2TT	DATA CARRIER DETECT (Port 2) - same as DCD1TT on pin A4.
A13	SUP2	PULLUP LINE (Port 2) - same as SUP1 on pin A5 except headers J8 and J12 apply.
A14	RxC2	RECEIVE CLOCK (Port 2) - same as RxC1 on pin A6.
A15,A16	GND	GROUND
A17-A24	D00-D07	PRINTER DATA (bits 0-7) - output data to the I/O module.
A25	PACK	PRINTER ACKNOWLEDGE - a low level input pulse indicating that the next character may be sent.
A26	PSTB*	PRINTER STROBE - an output pulse used to clock data from the system to the printer. This pulse is active low.
A27	INPRIME	PRINTER INPUT PRIME - an output signal that clears the printer buffer and initializes the logic.
A28	SEL	PRINTER SELECT - input signal indicating that the printer is selected.
A29	BUSY	PRINTER BUSY - an input signal indicating that the printer cannot receive data.
A30	FAULT	PRINTER FAULT - an input signal that indicates a printer fault condition such as paper empty, light detect, or a deselect condition.
A31	BATT	BATTERY - +5 Vdc input to the controller module for battery backup of the time-of-day clock.
A32	REMRES*	REMOTE RESET - an input for as remote switch to reset the system (normally open).
B1	+5 VDC	+5 Vdc Power - used by the logic circuits on the I/O module.
B2	GND	GROUND

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B3		Not used.
B4-B11	A24-A31	VME ADDRESS bus (bits 24-31) - eight three-state input lines that specify an address in the memory map.
B12	GND	GROUND.
B13	+5 VDC	+5 Vdc Power - same as +5 Vdc on pin B1.
B14-B21	D16-D23	VME DATA bus (bits 16-23) - eight three-state bidirectional data lines.
B22	GND	GROUND
B23-B30	D24-D31	VME DATA bus (bits 24-31) - eight three-state bidirectional data lines.
B31	GND	GROUND
B32	+5 VDC	+5 Vdc Power - same as +5 Vdc on pin B1.
C1	TxD1	TRANSMIT DATA (Port 1) - data to be transmitted is furnished on this line to the modem from the terminal.
C2	RxD1	RECEIVE DATA (Port 1) - data that is demodulated from the receive line is presented to the terminal by the modem.
C3	CTS1	CLEAR TO SEND (Port 1) - CTS is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of the message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
C4	DCD1IN	DATA CARRIER DETECT (Port 1) - furnished by the modem to the terminal to indicate that a valid carrier is being received.
C5	DSR1	DATA SET READY (Port 1) - DSR is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
C6,C7	GND	GROUND
C8	TxC1	TRANSMIT CLOCK (Port 1) - this line clocks output data to the modem from the terminal.

TABLE 5-2. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C9	TxD2	TRANSMIT DATA (Port 2) - same as TxD1 on pin C1.
C10	RxD2	RECEIVE DATA (Port 2) - same as RxD1 on pin C2.
C11	CTS2	CLEAR TO SEND (Port 2) - same as CTS1 on pin C3.
C12	DCD2IN	DATA CARRIER DETECT (Port 2) - same as DCD1IN on pin C4.
C13	DSR2	DATA SET READY (Port 2) - same as DSR1 on pin C5.
C14,C154	GND	GROUND
C16	TxC2	TRANSMIT CLOCK (Port 2) - same as TxC1 on pin C8.
C17-C32	GND	GROUND

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5.2.3 I/O Module Connector P1 Interconnect Signals

The signals on connector P1 on the I/O module are the same pin-for-pin as the signals on connector P2 on the controller module. Pins B1 through B32 are not used on the P1 connector. Refer to paragraph 5.2.2 for signal descriptions.

5.2.4 I/O Module Connector J1 Interconnect Signals

Connector J1 on the MVME701 is a 4-pin connector. Connector J1 on the MVME701A is a 9-pin connector. Table 5-3 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 5-3. Connector J1 Interconnect Signals

PIN NUMBER	PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	1	GND	BATTERY GROUND
2	6	BATT	BATTERY - a +5 Vdc battery remote backup connection for time-of-day clock.
3	2	RESET	REMOTE RESET - a remote reset connection for a normally open switch.
4	7	GND	RESET GROUND
	3-5,8,9		Not used.

5.2.5 MVME701 Connector J2 Interconnect Signals

Table 5-4 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 5-4. MVME701 Connector J2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	INPRIME	INPUT PRIME - an input signal that clears the printer buffer and initializes the logic.
2-4	GND	GROUND
5	FAULT	FAULT - an input signal that indicates printer fault condition.
6-8	GND	GROUND
9		Not used
10	GND	GROUND
11		Not used.
12	GND	GROUND
13		Not used.

TABLE 5-4. MVME701 Connector J2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
14	GND	GROUND
15		Not used.
16	GND	GROUND
17		Not used.
18	GND	GROUND
19	BUSY	BUSY - an input signal indicating that the printer cannot receive data.
20	GND	GROUND
21		Not used.
22	GND	GROUND
23	SEL	SELECT - an input signal indicating that the printer is selected.
24	GND	GROUND
25	DATA	DATA (bit 8) - output data to the printer.
26	GND	GROUND
27	DATA	DATA (bit 7) - output data to the printer.
28	GND	GROUND
29	DATA	DATA (bit 6) - output data to the printer.
30	GND	GROUND
31	DATA	DATA (bit 5) - output data to the printer.
32	GND	GROUND
33	DATA	DATA (bit 4) - output data to the printer.
34	GND	GROUND
35	DATA	DATA (bit 3) - output data to the printer.

TABLE 5-4. MVME701 Connector J2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
36	GND	GROUND
37	DATA	DATA (bit 2) - output data to the printer.
38	GND	GROUND
39	DATA	DATA (bit 1) - output data to the printer.
40-42	GND	GROUND
43	PSTB*	PRINTER STROBE - an active low output pulse used to clock data from the system to the printer.
44-46	GND	GROUND
47	PACK*	PRINTER ACKNOWLEDGE - a low level input pulse indicating that the next character may be sent.
48-50	GND	GROUND

5.2.6 MVME701A Connector J2 Interconnect Signals

Table 5-5 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 5-5. MVME701A Connector J2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	PSTB*	PRINTER STROBE - an output pulse used to clock data from the system to the printer. This pulse is active low.
2-9	DATA1-8	DATA (bits 1-8) - output data to the printer.
10	PACK*	PRINTER ACKNOWLEDGE - a low level input pulse indicating the the next character may be sent.
11	BUSY	BUSY - an input signal indicating that the printer cannot receive data.

TABLE 5-5. MVME701A Connector J2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
12		Not used.
13	SEL	SELECT - an input signal indicating that the printer is selected.
14-18		Not used.
19-30	GND	GROUND
31	INPRIME	INPUT PRIME - an output signal that clears the printer buffer and initializes the logic.
32	FAULT	FAULT - an input signal that indicates a printer fault condition such as paper empty, light detect, or a deselect condition.
33-36		Not used.

5.2.7 I/O Module Connectors J3 and J4 Interconnect Signals

Standard RS-232C cables mate with these connectors. Table 5-6 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 5-6. Connectors J3 and J4 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1		Not used.
2	TxD	TRANSMIT DATA - data to be transmitted is furnished on this line to the modem to the terminal.
3	RxD	RECEIVE DATA - data that is demodulated from the receive line is presented to the terminal to the modem.
4	RTS	REQUEST TO SEND - RTS is supplied by the terminal to the modem when it is required to transmit a message. When RTS is off, the modem carrier is off. When RTS is turned on, the modem immediately turns on the carrier.

TABLE 5-6. Connectors J3 and J4 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
5	CTS	CLEAR TO SEND - CTS is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of a message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
6	DSR	DATA SET READY - DSR is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
7	SIG-GND	SIGNAL GROUND - common return for all signals.
8	DCD	DATA CARRIER DETECT - furnished by the modem to the terminal to indicate that a valid carrier is being received.
9-14		Not used.
15	TxC	TRANSMIT CLOCK - this line clocks output data to the modem from the terminal.
16		Not used.
17	RxC	RECEIVE CLOCK - this line clocks input data from a terminal to a modem.
18,19		Not used.
20	DTR	DATA TERMINAL READY - a signal from the terminal to the modem indicating that the terminal is ready to send or receive data.
21-25		Not used.

5.3 PARTS LISTS

Table 5-7 lists the components of the controller module. Table 5-8 lists the components of the I/O module. The parts locations are illustrated in Figures 5-1 and 5-2, respectively. These parts reflect the latest issue of hardware at the time of printing.

TABLE 5-7. Controller Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8292B01	Printed wiring board
CR1,CR2	48NW9607A01	Rectifier, 1N4001
CR3,CR4	48NW9616A03	Diode, 1N4148
C1-C26,C28, C29,C31-C35, C38-C43,C45, C48-C50,C52-C59	21NW9632A03	Capacitor, fixed, ceramic, 0.1 uF @ 50 Vdc
C27,C36	23NW9618A22	Capacitor, electrolytic, 50 uF @ 16 Vdc
C30	23NW9618A43	Capacitor, electrolytic, 6.8 uF @ 35 Vdc
C37	23NW9618A67	Capacitor, electrolytic, 10 uF @ 35 Vdc
C44,C46	21NW9710A01	Capacitor network, SIP, 7/470 pF
C47	20NW9628A04	Capacitor, trimmer, 5.5-18 pF
C51	21NW9629A18	Capacitor, fixed, mica, 56 pF @ 500 Vdc
DL1	01NW9804B35	Digital delay, 100 ns
DS1	48NW9612A49	Indicator, LED, red
DS2	48NW9612A59	Indicator, LED, green
DS3,DS4	72NW9624A03	Display, LED readout
J1,J9,J17, J19	28NW9802B62	Header, double row post, 20-pin
J2,J10	28NW9802B34	Header, double row post, 16-pin
J3,J5,J6, J11,J25,J28	28NW9802D01	Header, double row post, 2-pin

TABLE 5-7. Controller Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
J4,J16,J18, J20	28NW9802C63	Header, double row post, 12-pin
J7,J21,J26,	28NW9802C43	Header, double row post, 8-pin
J8,J15	28NW9802B21	Header, double row post, 6-pin
J12-J14,J23, J24	28NW9802C29	Header, double row post, 4-pin
J18	28NW9802C36	Header, double row post, 14-pin
J22,J29	28NW9802D04	Header, single row post, 3-pin
P1,P2	28NW9802E51	Connector, 96-pin
Q1	48NW9610A22	Transistor, MPS2222
R1	51NW9626A53	Resistor network, SIP, 4/47 ohm
R2	51NW9626A56	Resistor network, SIP, 4/22 ohm
R3,R6	06SW-124A20	Resistor, fixed, film, 62 ohm, 5%, 1/4 W
R4,R14,R34	51NW9626A37	Resistor network, SIP, 9/10k ohm
R5,R30-R32, R33,R36	51NW9626A41	Resistor network, SIP, 9/4.7k ohm
R7		Not used.
R8,R9,R17	06SW-124A65	Resistor, fixed, film, 4.7k ohm, 5%, 1/4 W
R10	51NW9626B55	Resistor network, SIP, 9/4.7k ohm
R11	06SW-124A11	Resistor, fixed, film, 27 ohm, 5%, 1/4 W
R12	06SW-123A35	Resistor, fixed, film, 270 ohm, 5%, 1/4 W
R13	06SW-125A27	Resistor, fixed, carbon, 120 ohm, 5%, 1/2 W
R15	51NW9626B51	Resistor network, SIP, 5/1k ohm
R16,R19,R21	51NW9626B53	Resistor network, SIP, 7/4.7k ohm

TABLE 5-7. Controller Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R18,R22	51NW9626B54	Resistor network, SIP, 7/39k ohm
R20	06SW-124A87	Resistor, fixed, film, 39k ohm, 5%, 1/4 W
R23	06SW-124B50	Resistor, fixed, film, 15 megohm
R25	06SW-124B22	Resistor, fixed, film, 1.0 megohm
R26	06SW-124A25	Resistor, fixed, film, 100 ohm, 5%, 1/4 W
R27	06SW-124A41	Resistor, fixed, film, 470 ohm, 5%, 1/4 W
R28	06SW-124A49	Resistor, fixed, film, 1.0k ohm, 5%, 1/4 W
R29	06SW-124A75	Resistor, fixed, film, 4.7k ohm, 5%, 1/4 W
R35	51NW9626A47	Resistor network, SIP, 7/4.7k ohm
S1	40NW9801B35	Switch, 8-section, DIP, SPST, piano
S2	40NW9801A54	Switch, pushbutton, SPDT, momentary contact
U1,U15	(See NOTE)	I.C. programmed
U2	51NW9615F38	I.C. SN74LS393N
U3,U5,U55, U61	51NW9615J39	I.C. 74F74PC
U4,U7,U81, U87	51NW9615H89	I.C. SN74LS645-1N
U6	51NW9615F79	I.C. SN74S240N
U9,U17,U26,	51NW9615H41	I.C. SN74LS682N
U10	51NW9615E77	I.C. SN74LS27N
U12,U44	51NW9615F02	I.C. SN74LS244N
U13	(See NOTE)	I.C. programmed
U14,U90	51NW9615E95	I.C. SN74LS240N
U18,U27	51NW9615N56	I.C. 74F174PC

TABLE 5-7. Controller Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U20,U29	51NW9615E86	I.C. SN74LS151N
U21,U22,U30	51NW9615E98	I.C. SN74LS373N
U23	51NW9615F85	I.C. SN74S38N
U24	51NW9615D93	I.C. SN74S30N
U32		Not used.
U35,U78,U85	51NW9615C21	I.C. SN74LS04N
U37	51NW9615H83	I.C. SN74LS641-1N
U38	(See NOTE)	I.C. programmed
U39	(See NOTE)	I.C. programmed
U40	(See NOTE)	I.C. programmed
U41,U46	51NW9615L26	I.C. SC34000-02
U43	51NW9615C22	I.C. SN74LS08N
U45	51NW9615E67	I.C. SN74S260N
U47,U79	51NW9615K71	I.C. 74F04PC
U48	51NW9615C56	I.C. SN74S08N
U49,U54,U62	51NW9615N32	I.C. 74F164PC
U50	(See NOTE)	I.C. programmed
U51	51NW9615D32	I.C. SN74S02N
U52,U64	51NW9615D27	I.C. SN74S32N
U53	51NW9615F05	I.C. SN74LS20N
U56,U89	51NW9615E91	I.C. SN74LS00N
U57,U67	51NW9615P40	I.C. R68560P
U58,U60,U68	51NW9615B30	I.C. MC1489AP

TABLE 5-7. Controller Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U59,U69,U70	51NW9615B29	I.C. MC1488P
U65	51NW9615E88	I.C. SN74LS10N
U66,U76	51NW9615C24	I.C. SN74LS32N
U71	51NW9615B56	I.C. MC14528CP
U72	51NW9615D91	I.C. SN74S139N
U73	(See NOTE)	I.C. programmed
U75	51NW9615F41	I.C. SN74LS164N
U77	51NW9615E99	I.C. SN74LS374N
U80,U86	51NW9615H11	I.C. SN74LS645N
U82	51NW9615H35	I.C. MC146818P
U83	51NW9615N44	I.C. SN74LS647NT
U84	51NW9615H54	I.C. SN74LS12N
U88	51NW9615H93	I.C. SN74LS641N
VR1,VR2	48NW9608A31	Diode, zener, 5.6V, 1N5339B
VR3	51NW9615J93	I.C. LM317LZ
Y1	48AW1014B14	Crystal oscillator, 32 MHz
Y2	48AW4206B02	Crystal, 4.194304 MHz, 0.001%
	09NW9811A88	Socket, DIL, right angle (use at DS3,DS4)
	09NW9811A78	Socket, DIL, 20-pin (use at U1,U13,U15,U38,U40, U50,U73)
	09-W4659B14	Socket, DIL, 14-pin (use at U8,U11,U16,U19,U25, U28,U33,U36)
	09NW9811B01	Socket, DIL, 24-pin (use at U39)

TABLE 5-7. Controller Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	09-W4659B14	Socket, SIL, 20-pin (use at U41,U46)
	09-W4659B12	Socket, SIL, 12-pin (use at U82)
	09NW9811A46	Socket, oscillator, 4-pin
	64-W4667B01	Panel, front
	29NW9805B17	Jumper, shorting, insulated (use at J1,J4-J9, J12-J29)

NOTE: When ordering, use number labeled on part

TABLE 5-8. I/O Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8306B01	Printed wiring board MVME701
	84-W8427B01	Printed wiring board MVME701A
J1	28NW9802F85	Connector, right angle, 4-pin MVME701
J1	28NW9802G47	Connector, right angle, 9-pin MVME701A
J2	28NW9802D76	Connector, right angle, 50-pin MVME701
J2	28NW9802G48	Connector, right angle, 36-pin MVME701A
J3,J4	28NW9802D88	Connector, RS-232C, 25-pin MVME701
J3,J4	28NE9802G42	Connector, RS-232C, 25-pin MVME701A
J5,J6,J9, J10	28NW9802B62	Header, double row post, 20-pin
J7,J8,J11, J12	28NW9802D04	Header, single row post, 3-pin

TABLE 5-8. I/O Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
P1	28NW9802E05	Connector, DIN, 64-pin
	64-W4676B01	Panel, front
	29NW9805B17	Jumper, shorting, insulated (use at J5,J7,J8, J10-J12)

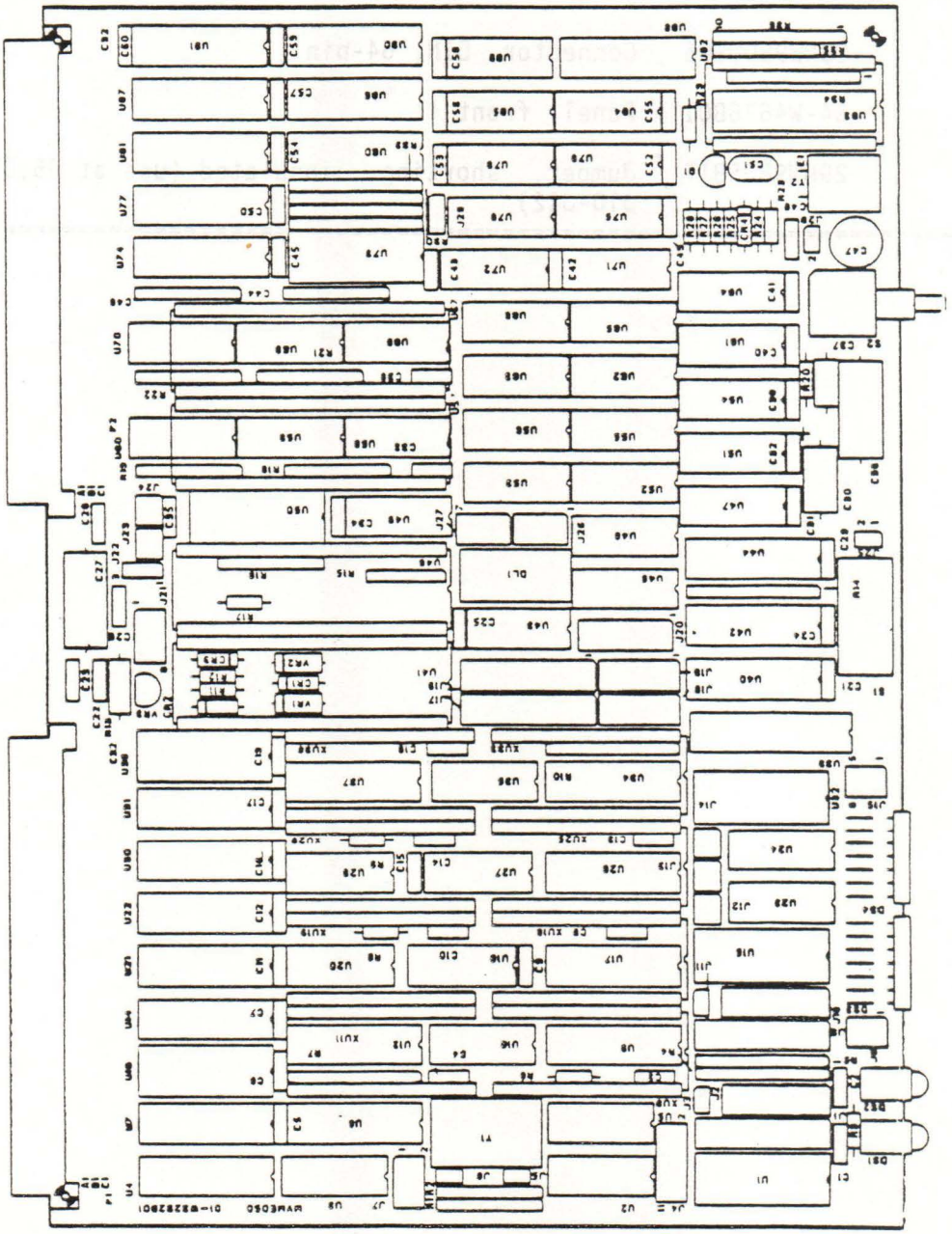

FIGURE 5-1. Controller Module Parts Location

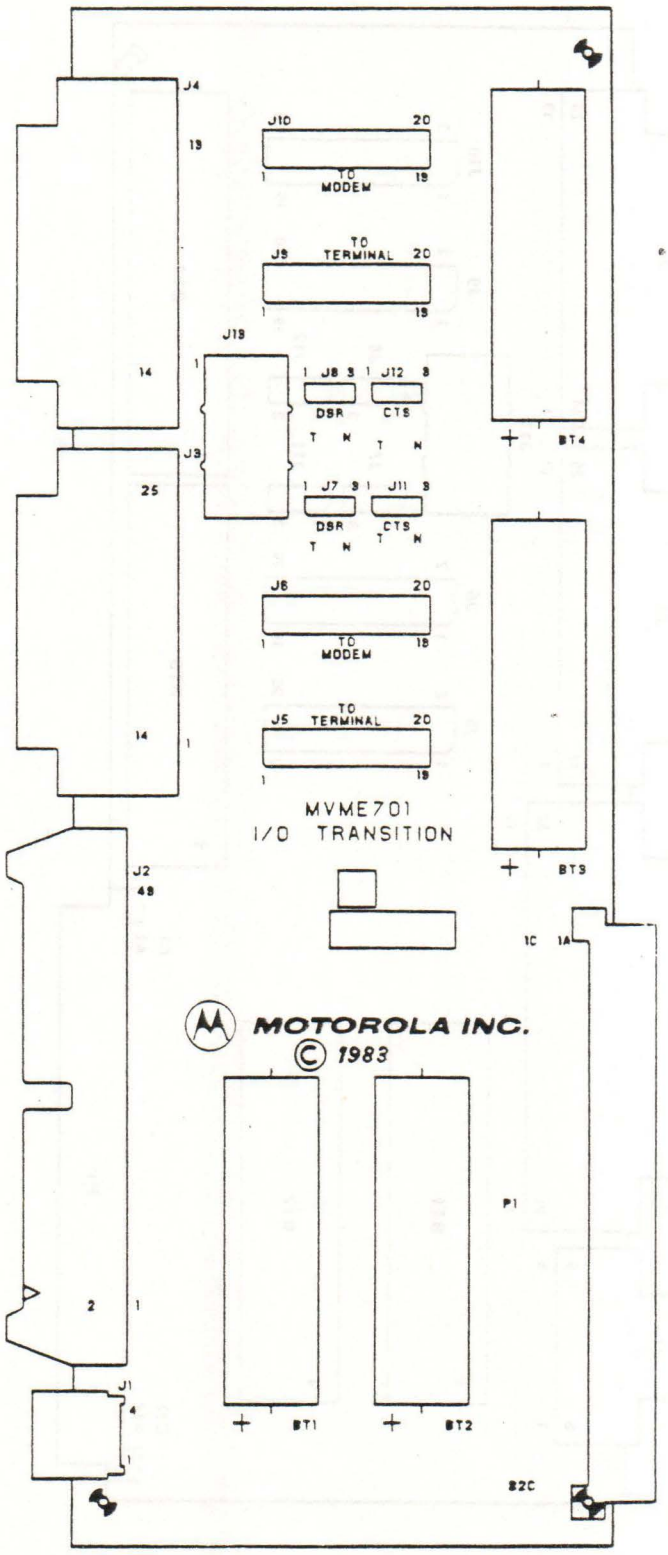

FIGURE 5-2. MVME701 I/O Module Parts Location

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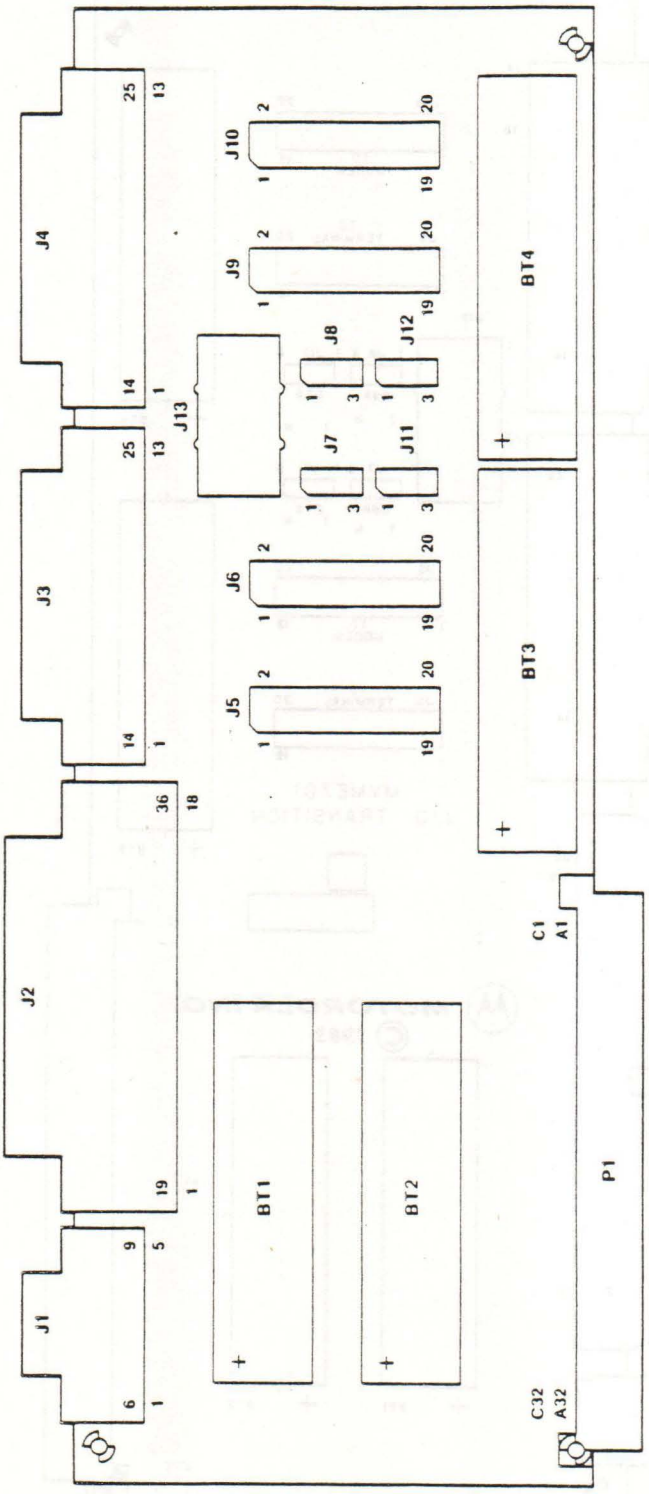

FIGURE 5-3. MVME701A I/O Module Parts Location

5.4 SCHEMATIC DIAGRAMS

Figure 5-4 illustrates the schematic diagram for the controller module. Figure 5-5 illustrates the schematic diagram for the MVME701 I/O module. Figure 5-6 illustrates the schematic diagram for the MVME701A I/O module.

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NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3292B01.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   () DENOTES - ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
4. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING, FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:

SHEET — 8 A6 — ZONE

REFERENCE DESIGNATIONS	
CR4	
U91	
C59	
DL1	
DS4	
J29	
P2	
Q1	
R36	
S2	
XU36	XU1-7,9,10, XU12-15,17,18, XU20-24,26,27, XU29-32,34,35
VR3	
Y2	
HIGHEST NUMBER USED	NOT USED

4 TABLE 1

REF DES	4 TYPE	GND	+5V	SH
DL1	100NS	7	14	11
DS3	TIL311	7	14	15
DS3	TIL311		L	15
DS4	TIL311	7	14	15
DS4	TIL311		L	15
U1	82S153	10	20	5
U2	74LS393	7	14	11
U3	74F74	7	14	11
U4	74LS645-1	10	20	10
U5	74F74	7	14	11
U6	74S240	10	20	11,12
U7	74LS645-1	10	20	10
U9	74LS682	10	20	5
U10	74LS27	7	14	7,10
U12	74LS244	10	20	4,15
U13	PAL16L8	10	20	11
U14	74LS240	10	20	11
U15	82S153	10	20	6
U17	74LS682	10	20	5
U18	74F174	8	16	11
U20	74LS151	8	16	7
U21	74LS373	10	20	4
U22	74LS373	10	20	4
U23	74S30	7	14	14,16
U24	74S30	7	14	7
U26	74LS682	10	20	6
U27	74F174	8	16	11
U29	74LS151	8	16	7
U30	74LS373	10	20	4
U31	74LS373	10	20	4
U32	SPARE			3
U34	74LS682	10	20	6
U35	74LS04	7	14	4,11,12,14
U37	(74LS641-1	10	20	12
U38	TBP28S42	10	20	4
U39	PAL20L8	12	24	7
U40	82S153	10	20	4
U41	MC88153	8	30	12
U41	MC88153	10	21	12
U41	MC88153	20	11	12
U41	MC88153	31	L	12
U42	74LS682	10	20	4
U43	74LS08	7	14	5,7,11
U44	74LS244	10	20	15
U45	74S288	7	14	5,8
U46	MC88153	8	30	12
U46	MC88153	10	21	12
U46	MC88153	20	11	12
U46	MC88153	31	L	12
U47	74S04	7	14	4,5,8
U48	74S08	7	14	4,5,8
U49	74F164	7	14	7
U50	PAL16L8	10	20	11
U51	74S02	7	14	5,8,7,10
U52	74S32	7	14	5,8,7
U53	74LS27	7	14	13,14
U54	74F164	7	14	13
U55	74F74	7	14	12
U56	74LS00	7	14	7,10
U57	R68560	9	24	13

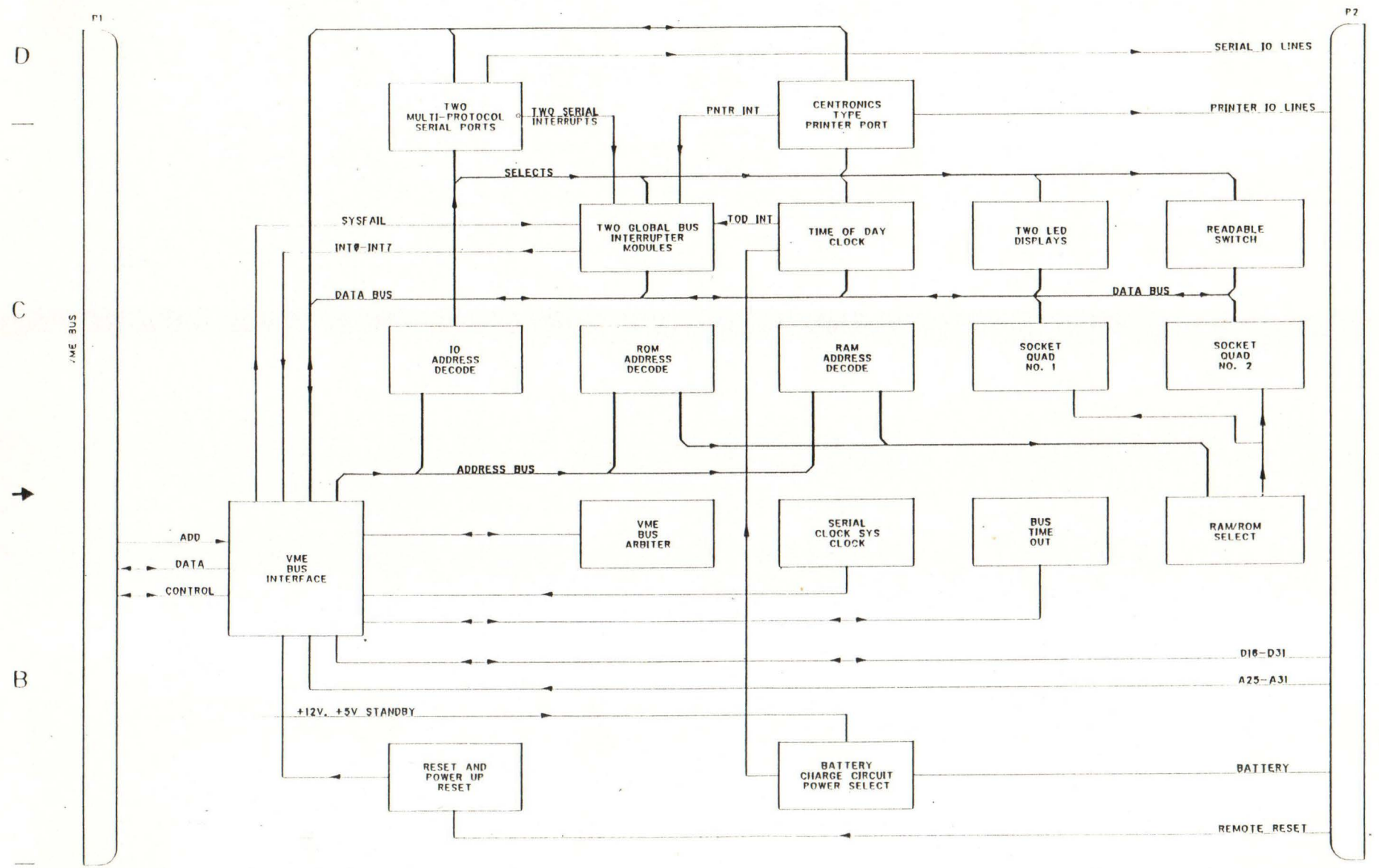
4 TABLE 1 CONT.

REF DES	4 TYPE	GND	+5V	+12V	-12V	+5VBB	SH
U57	R68560	35					13
U58	MC1489A	7	14				13
U59	MC1488	7		14	1		13
U60	MC1489A	7	14				13,14
U61	74F74	7	14				13
U62	74F164	7	14				4
U63	74LS00	7	14				12
U64	74S32	7	14				4,10
U65	74LS10	7	14				10
U66	74LS32	7	14				4,7,14
U67	R68560	9	24				14
U67	R68560	35					14
U68	MC1489A	7	14				14
U69	MC1488	7		14	1		14
U70	MC1488	7		14	1		13,14
U71	MC14528B	8	16				3,13
U72	74S139	8	16				12,15
U73	82S153	10	20				15
U74	74LS373	10	20				4
U75	74LS164	7	14				16
U76	74LS32	7	14				12,15
U77	74LS374	10	20				15
U78	74LS04	7	14				11,16
U79	74LS04	7	14				4,10,15
U80	74LS645	10	20				10
U81	74LS645-1	10	20				10
U82	MC14818	12				24	16
U83	74LS647	12	24				16
U84	74LS12	7	14				16
U85	74LS04	7	14				7,13,16
U86	74LS645	10	20				10
U87	74LS645-1	10	20				10
U88	74LS641	10	20				16
U89	74LS00	7	14				15,16
U90	74LS240	10	20				4,15
U91	SPARE						9
XU8	SOCKET						9
XU11	SOCKET						9
XU16	SOCKET						9
XU19	SOCKET						9
XU25	SOCKET						8
XU28	SOCKET						8
XU33	SOCKET						8
XU36	SOCKET						8
Y1	KIII4A	7	14				11

JUMPER TABLE

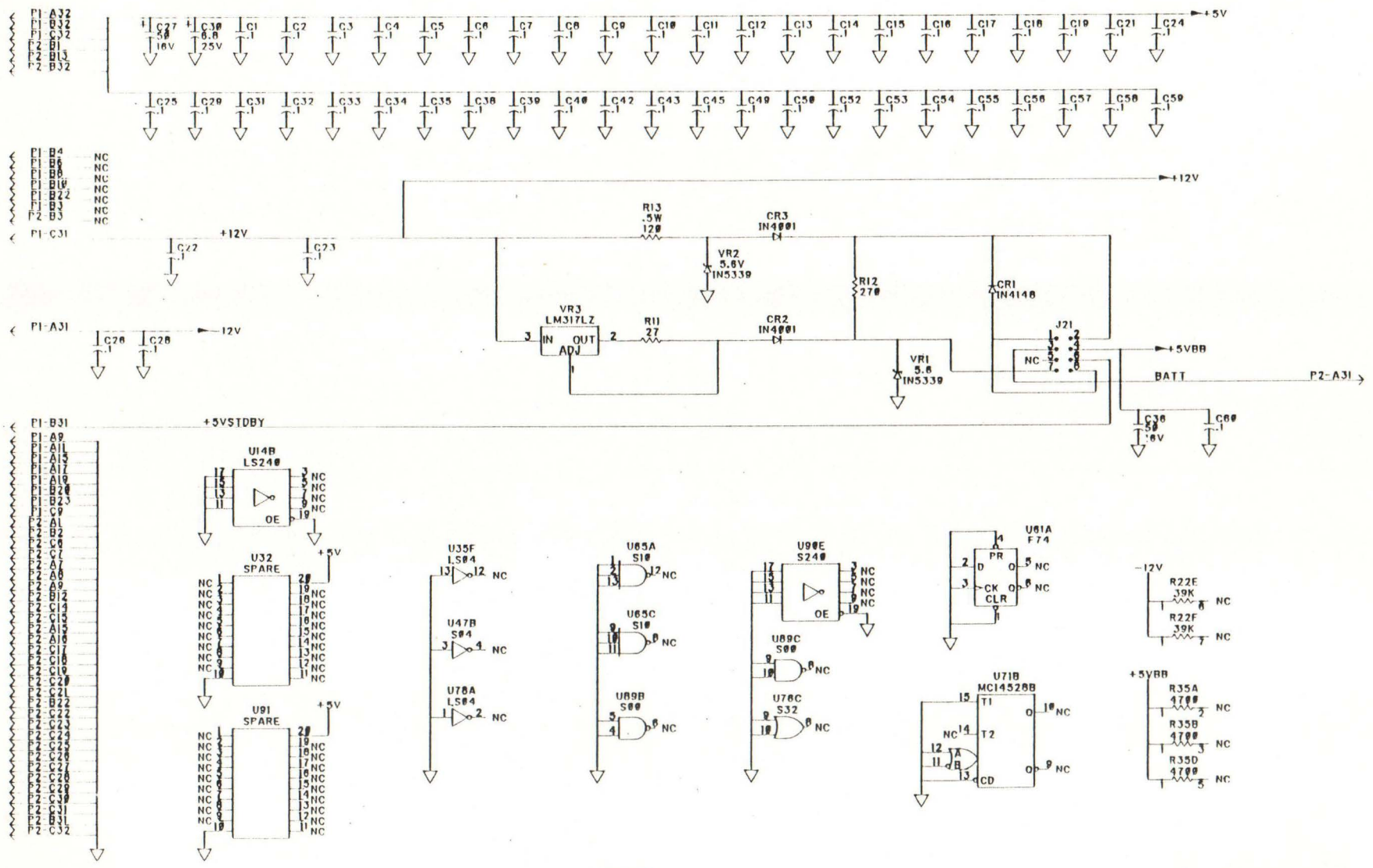
REF DES	LOCATION
J 1	(1-2)(3-4)(5-6)(7-8)(9-10)(13-14)
J 4	(9-10)
J 5	(1-2)
J 6	(1-2)
J 7	(1-2)(3-4)(5-6)(7-8)
J 8	(1-2)(5-6)
J 9	(1-2)(3-4)(5-6)(7-8)(9-10)(13-14)
J 12	(1-2)(3-4)
J 14	(1-2)(3-4)
J 15	(1-2)(5-6)
J 16	(1-2)(3-4)(5-6)(7-8)(9-10)(11-12)
J 17	(1-2)(3-4)(5-6)(7-8)(10-12)(14-16)(15-17)(19-20)
J 18	(1-2)(3-4)(5-6)(7-8)(9-10)(11-12)
J 19	(1-2)(3-4)(5-6)(7-8)(10-12)(14-16)(15-17)(19-20)
J 20	(1-2)(3-4)(5-6)(9-10)(11-12)(13-14)
J 21	(1-3)(2-4)(7-8)
J 22	(2-3)
J 25	(1-2)
J 26	(1-2)
J 27	(7-8)
J 28	(1-2)
J 29	(1-2)

FIGURE 5-4. Controller Module Schematic Diagram



63DW32128 REV B SH 2 OF 16

FIGURE 5-4. Controller Module Schematic Diagram



NOT USED

63DW3292B REV B SH 3 OF 16 97/98

FIGURE 5-4. Controller Module Schematic Diagram

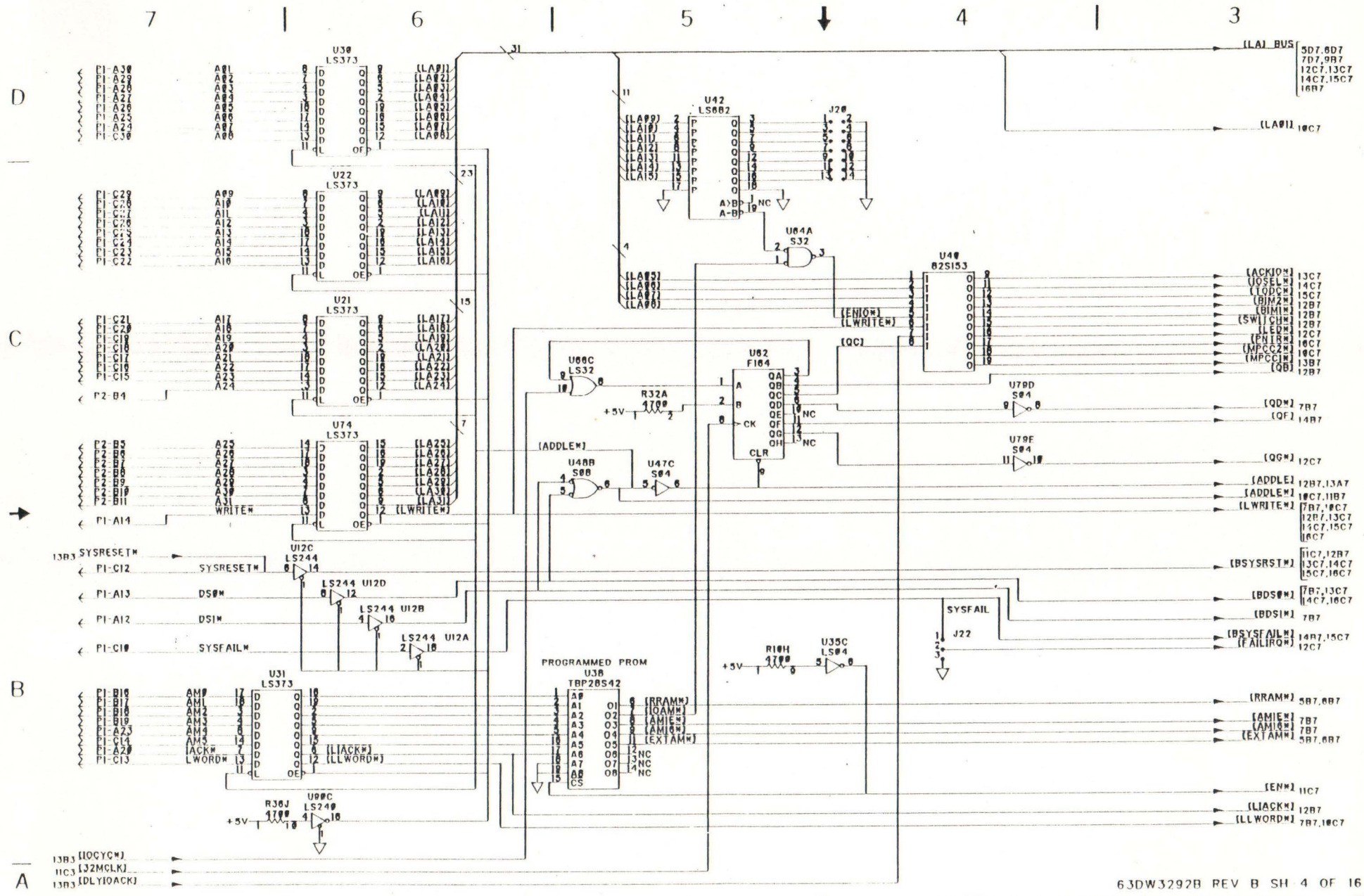


FIGURE 5-4. Controller Module Schematic Diagram

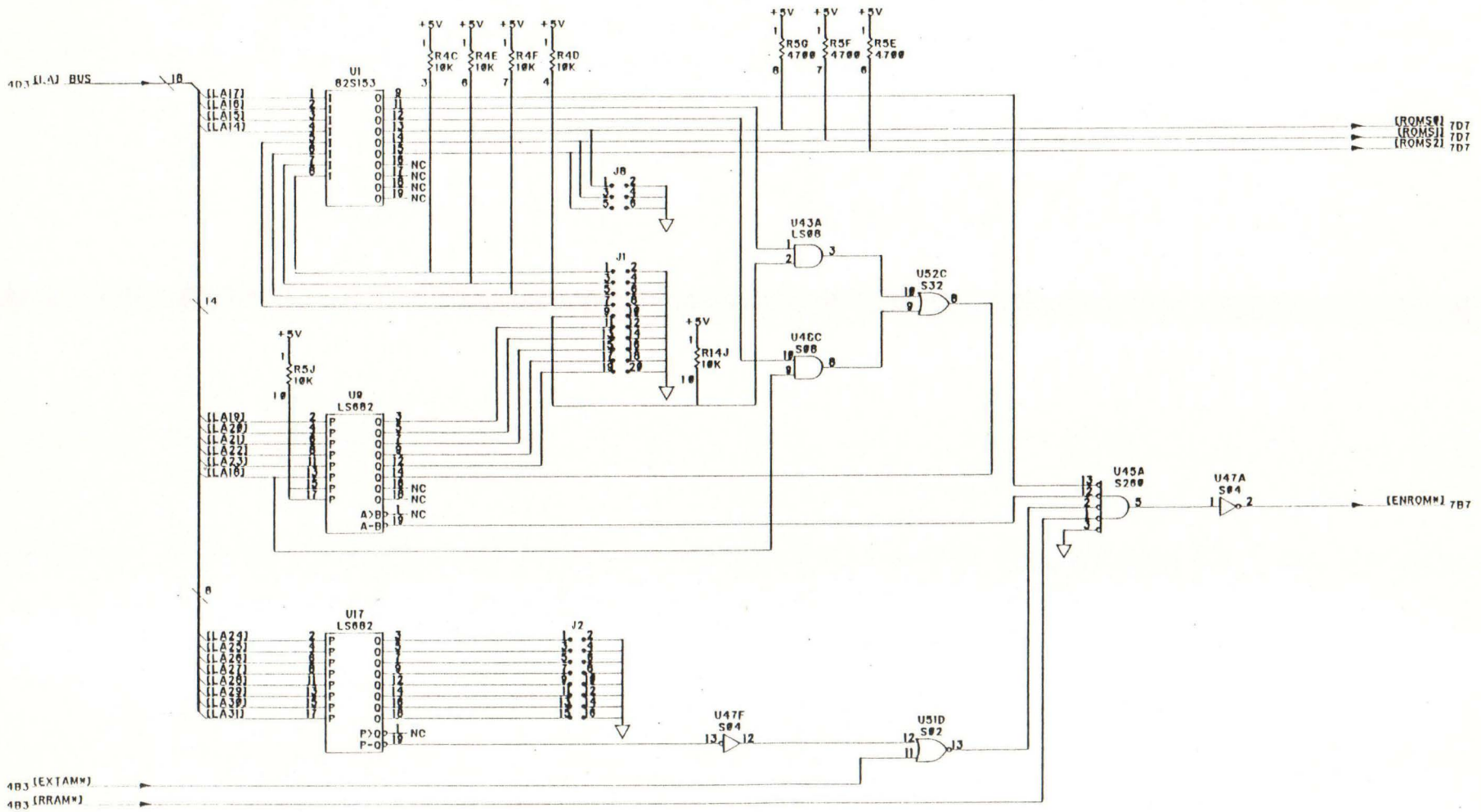
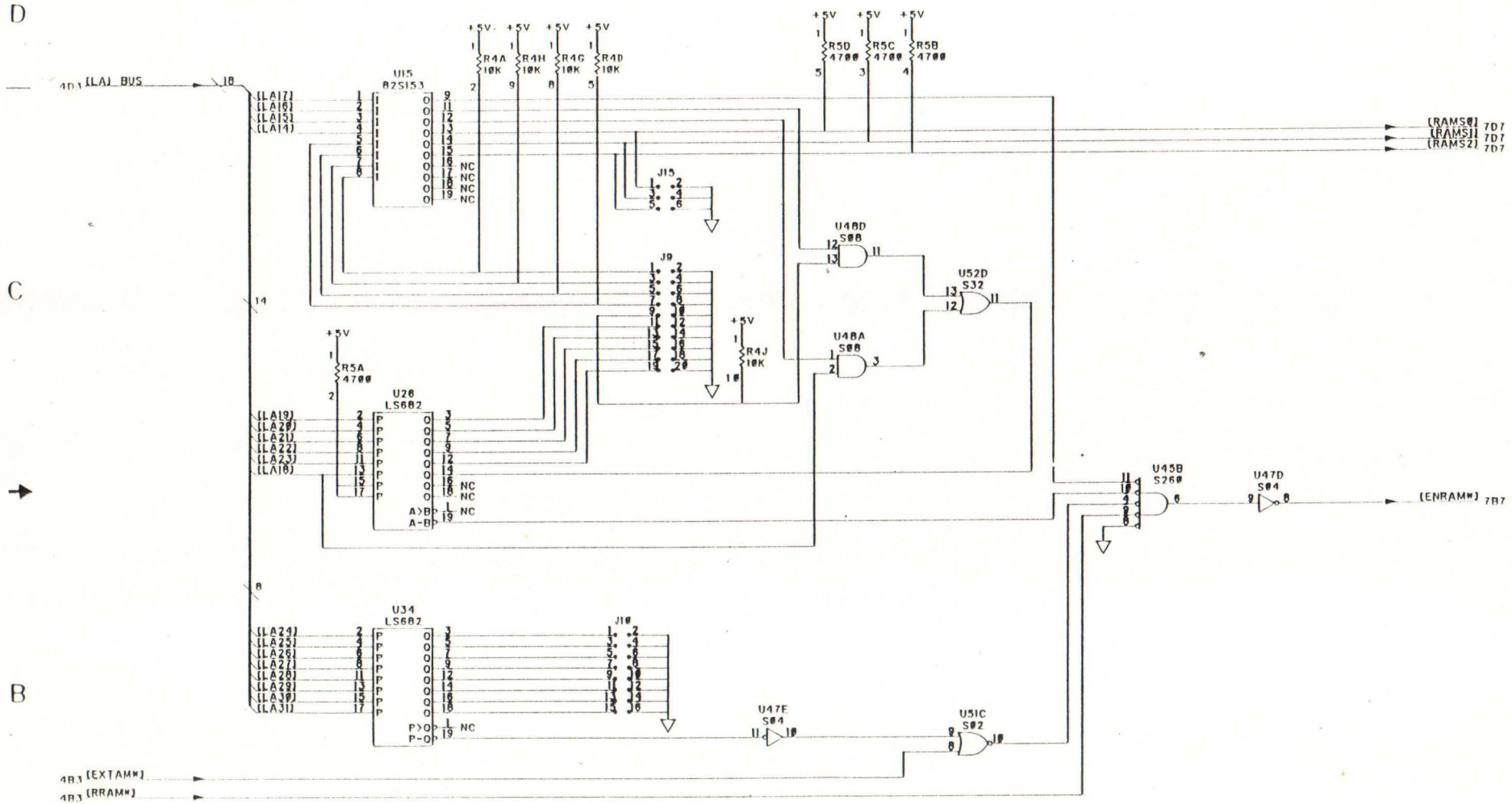
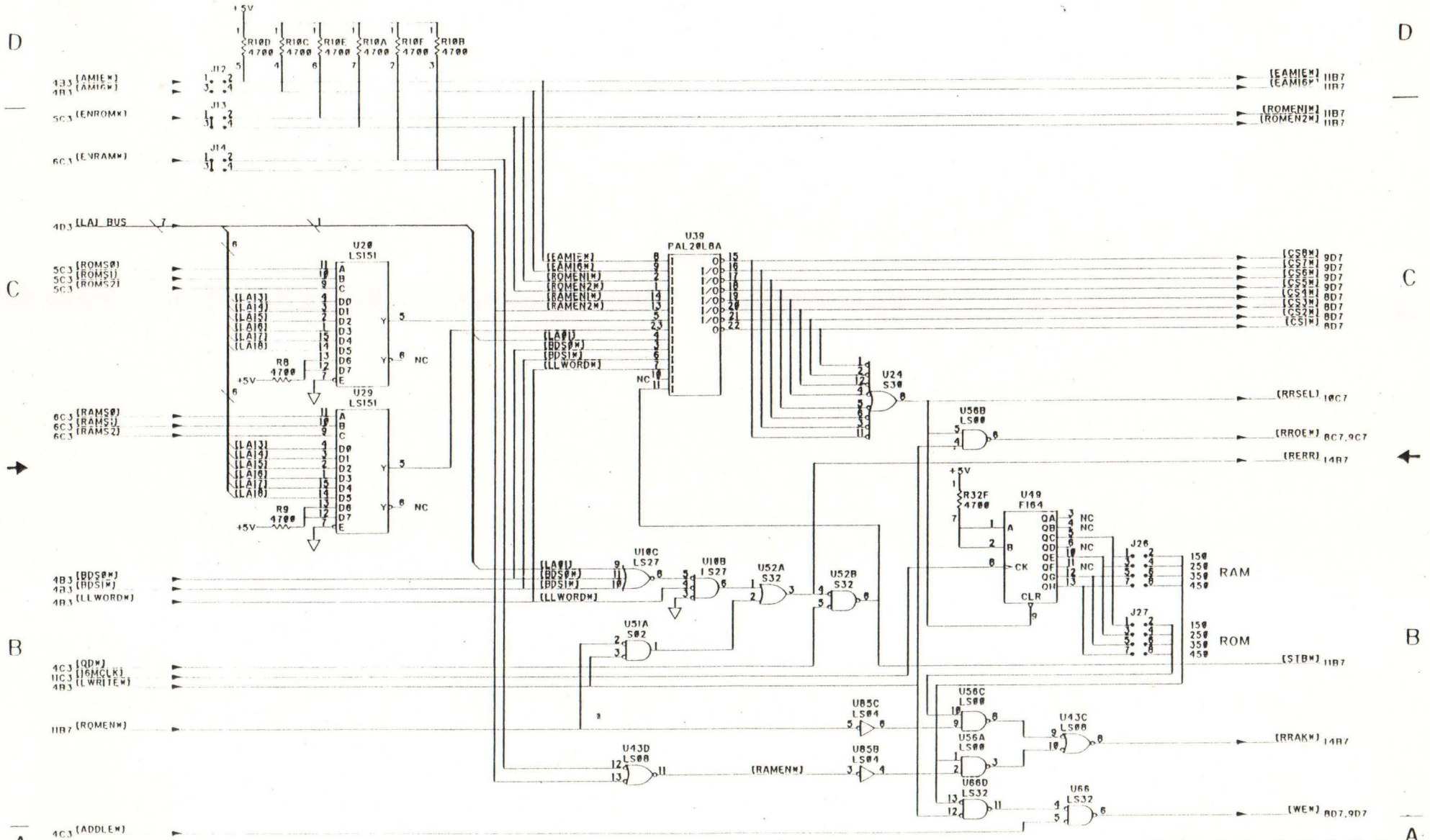


FIGURE 5-4. Controller Module Schematic Diagram



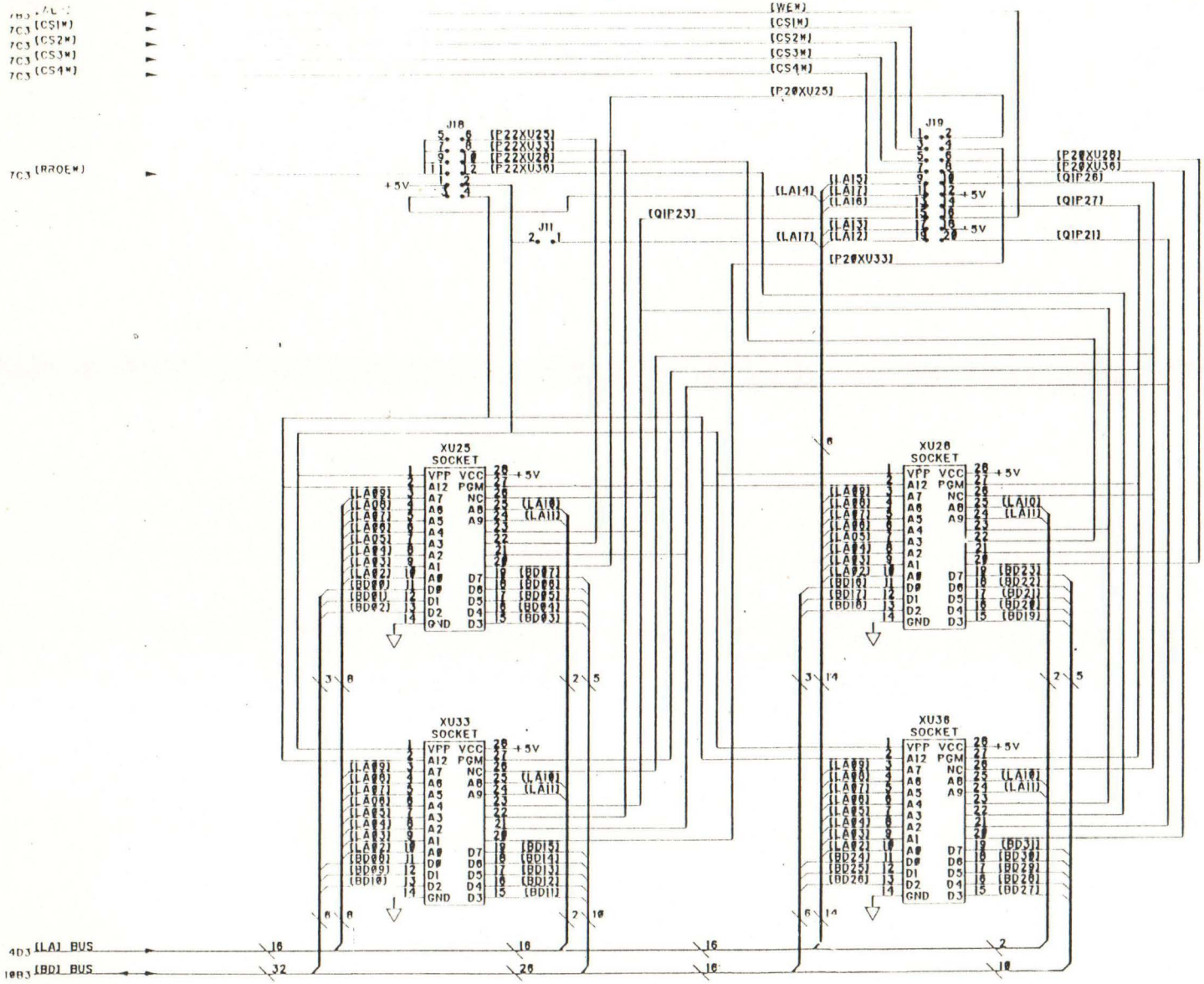
63DW3292B REV B SH 6 OF 16

FIGURE 5-4. Controller Module Schematic Diagram



63DW3292B REV B SH 7 OF 16

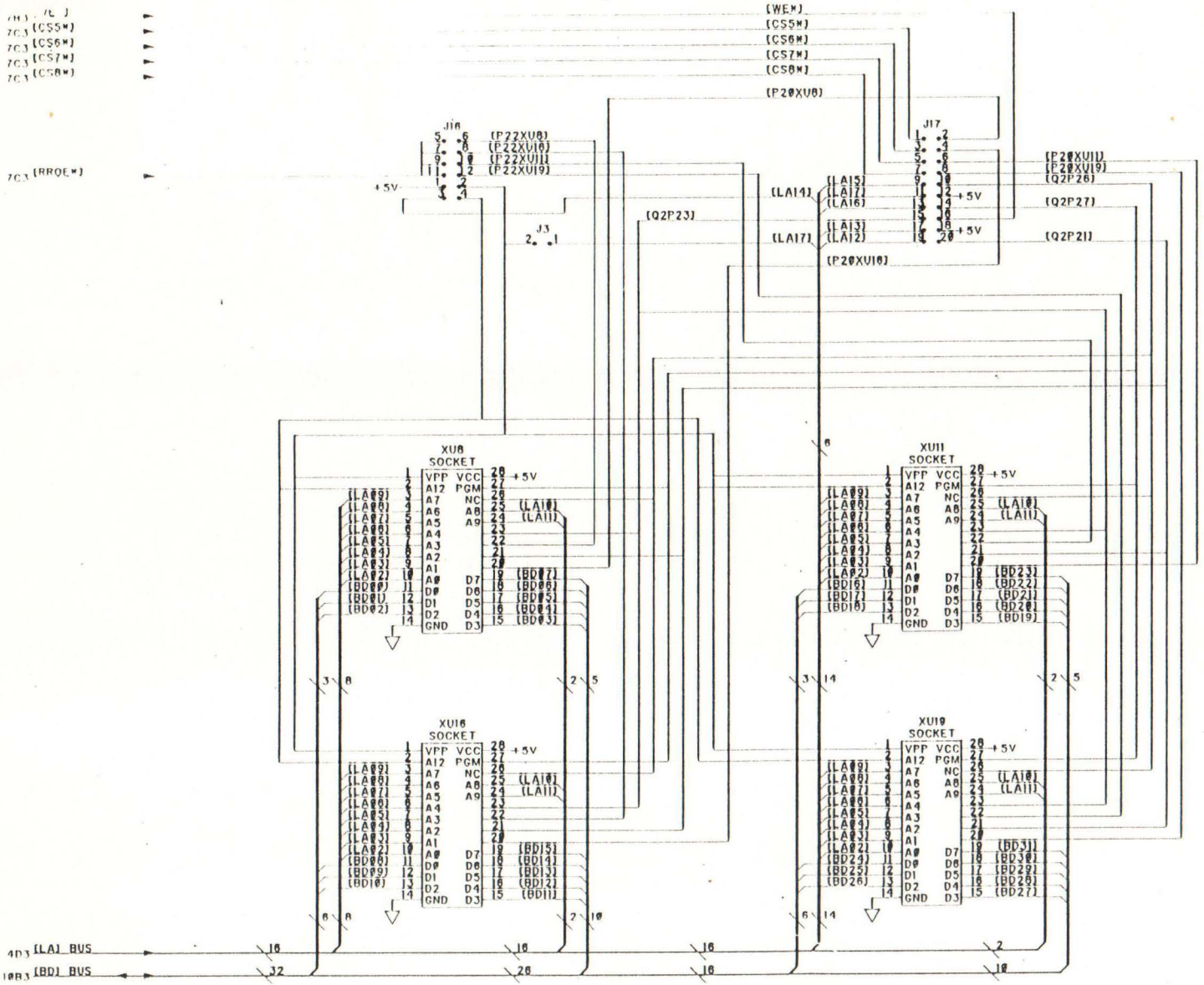
FIGURE 5-4. Controller Module Schematic Diagram



RAM/ROM SOCKET QUAD 1

63DW3292B REV B SH 8 OF 16

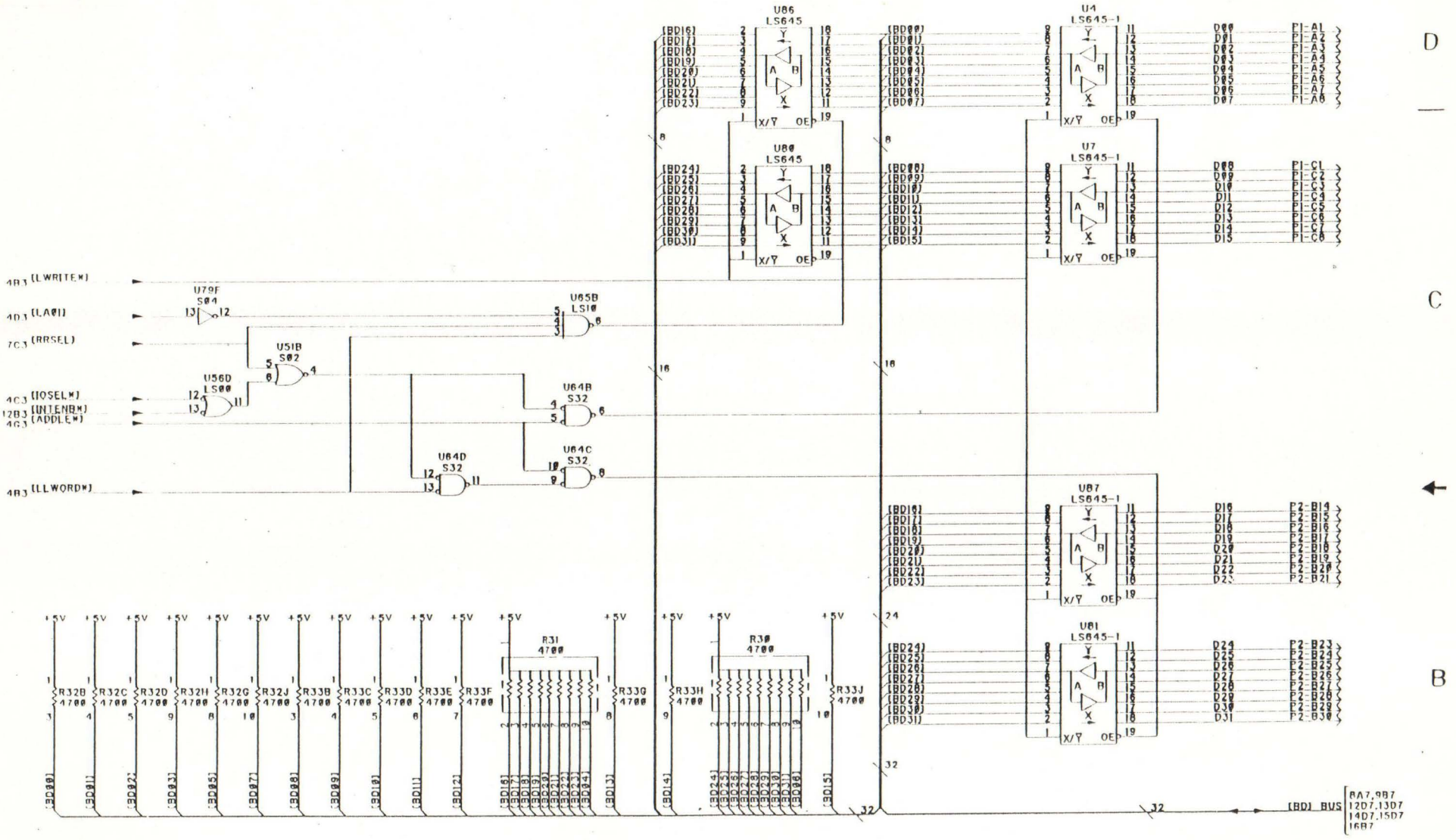
FIGURE 5 4. Controller Module Schematic Diagram



RAM/ROM SOCKET QUAD 2

63DW3292B REV B SH 9 OF 16

FIGURE 5-4. Controller Module Schematic Diagram



DATA BUS BUFFERS AND CONTROL LOGIC

63DW3292B REV B SH 10 OF 16

FIGURE 5-4. Controller Module Schematic Diagram

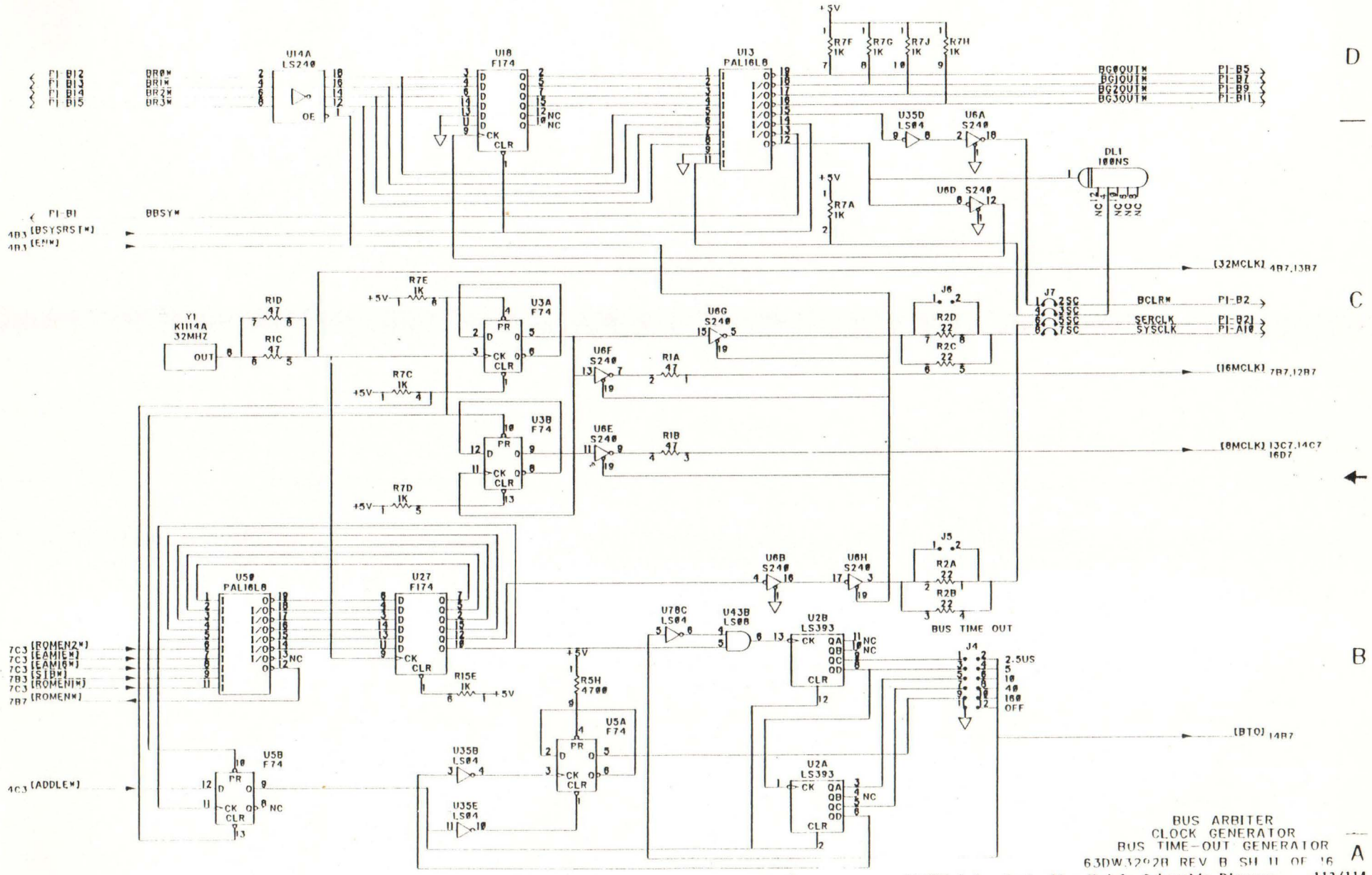


FIGURE 5-4. Controller Module Schematic Diagram

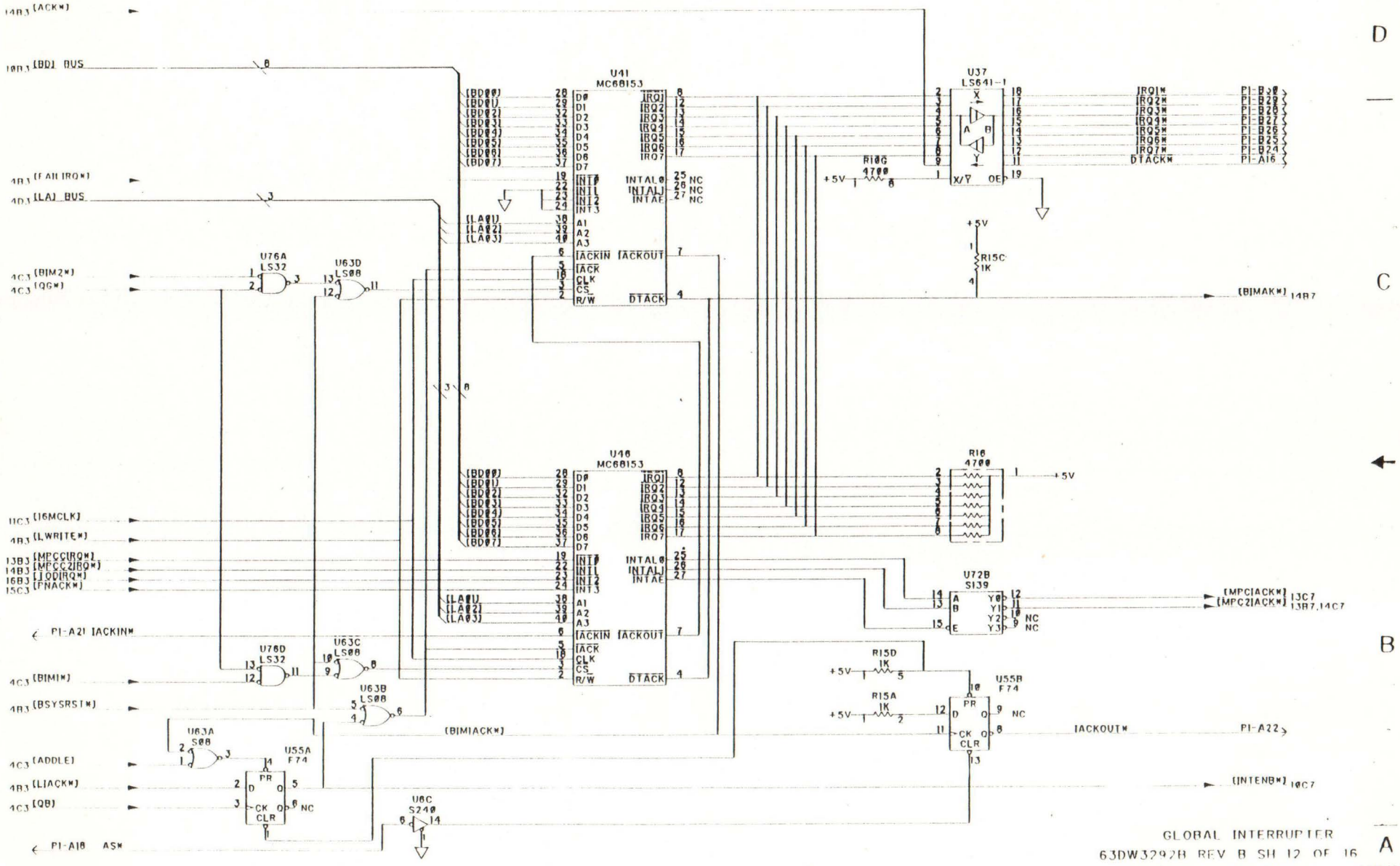


FIGURE 5-4. Controller Module Schematic Diagram

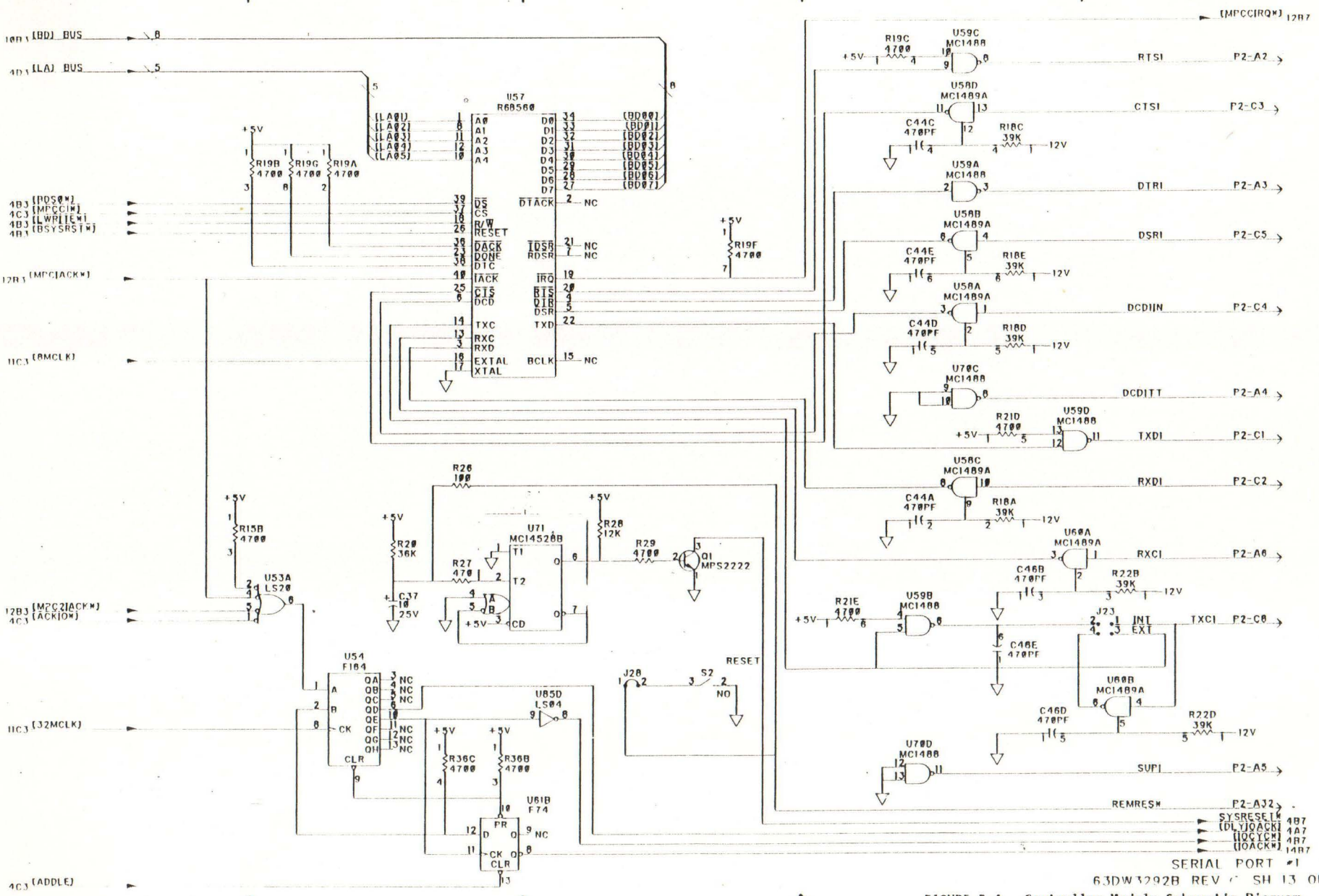
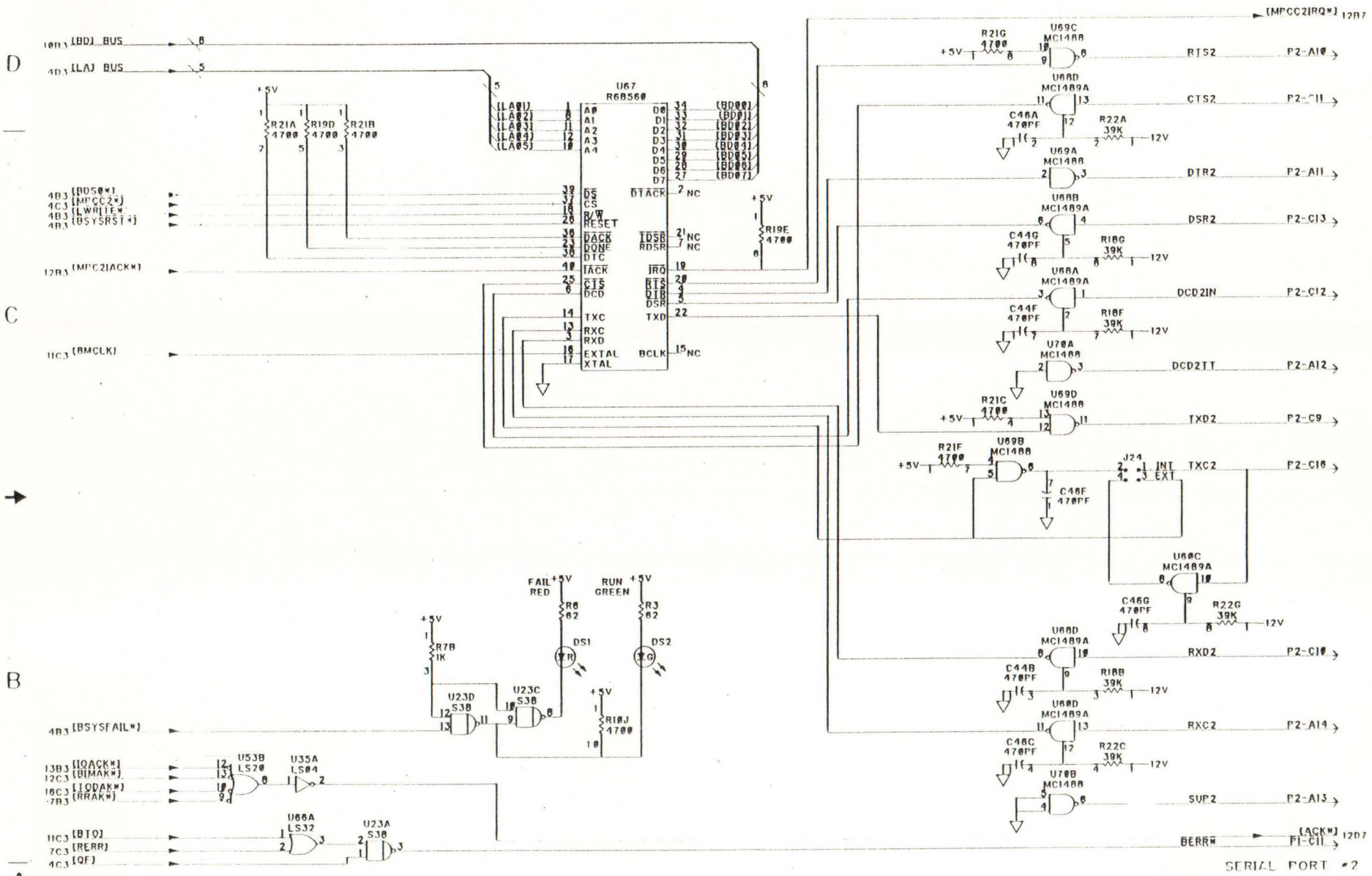
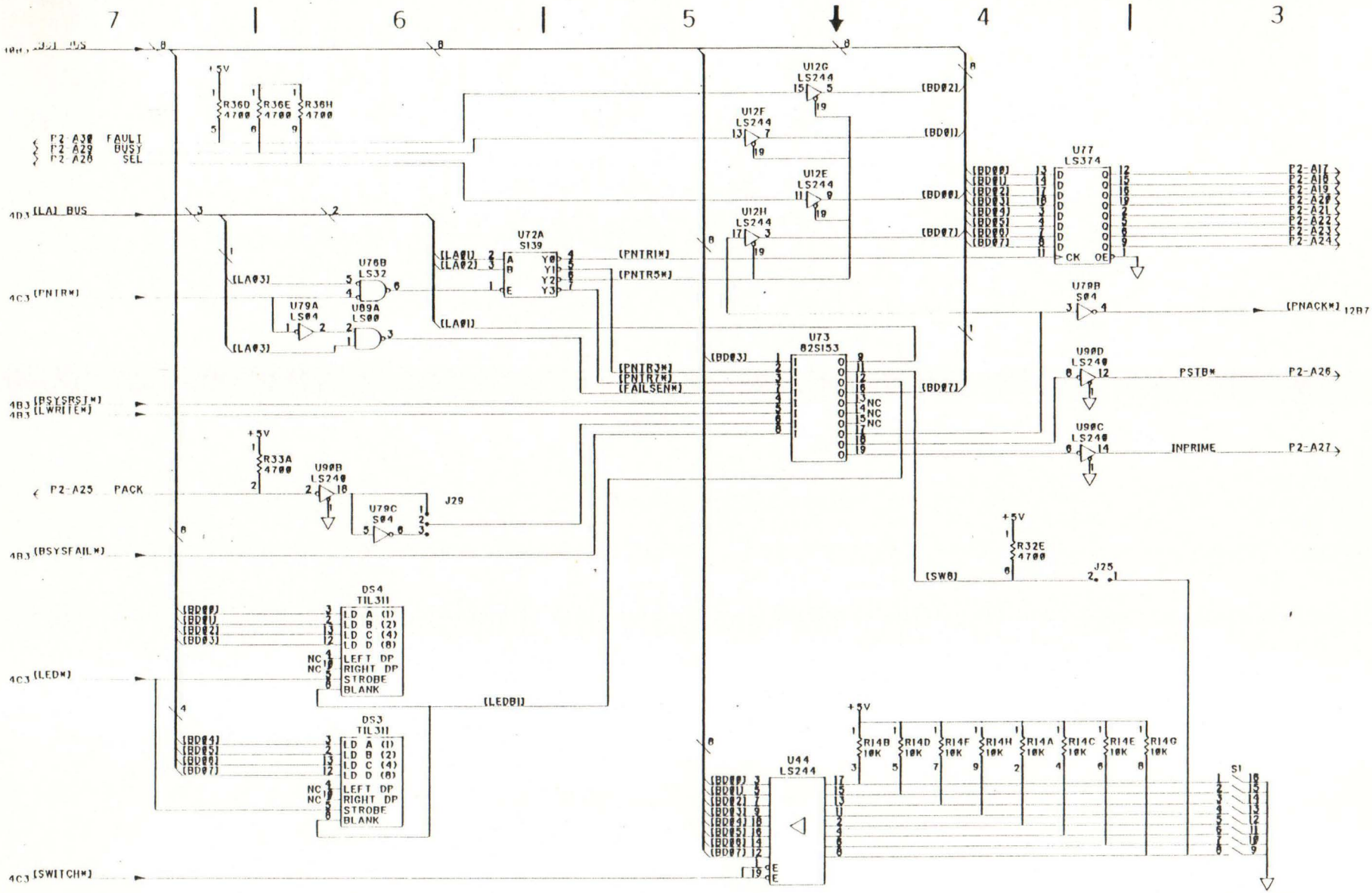


FIGURE 5-4. Controller Module Schematic Diagram



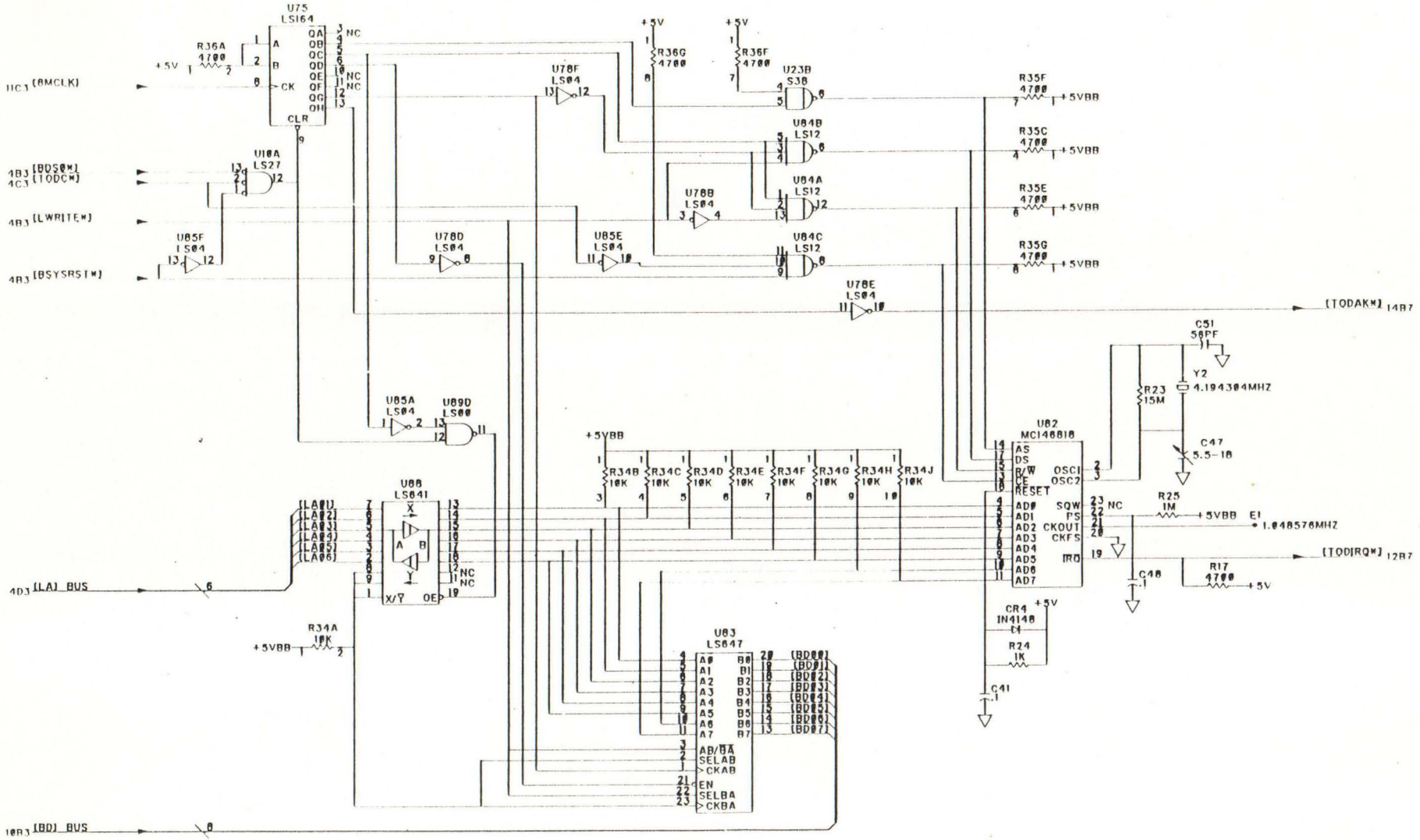
SERIAL PORT #2
63DW3292B REV B SH 14 OF 16

FIGURE 5-4. Controller Module Schematic Diagram



PRINTER PORT
63DW3292B REV B SH 15 OF 16

FIGURE 5-4. Controller Module Schematic Diagram



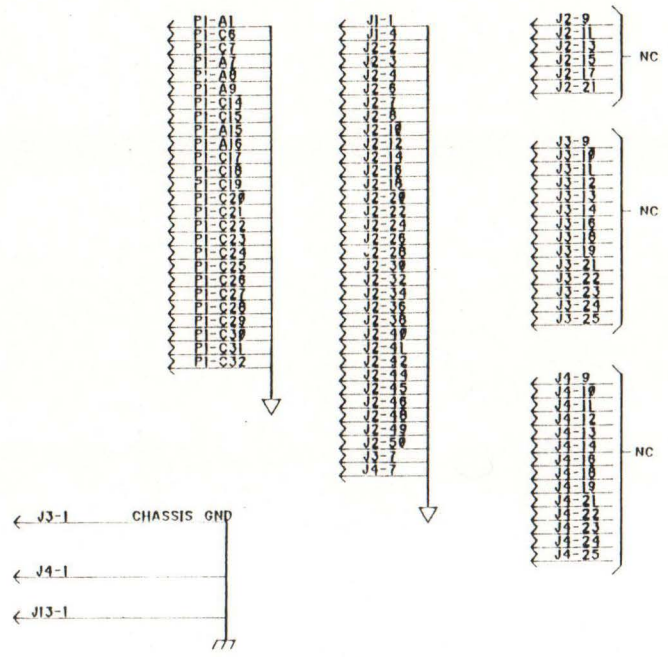
T.O.D. CLOCK
63CW3292B REV B SH 16 OF 16

FIGURE 5-4. Controller Module Schematic Diagram

NOTES:

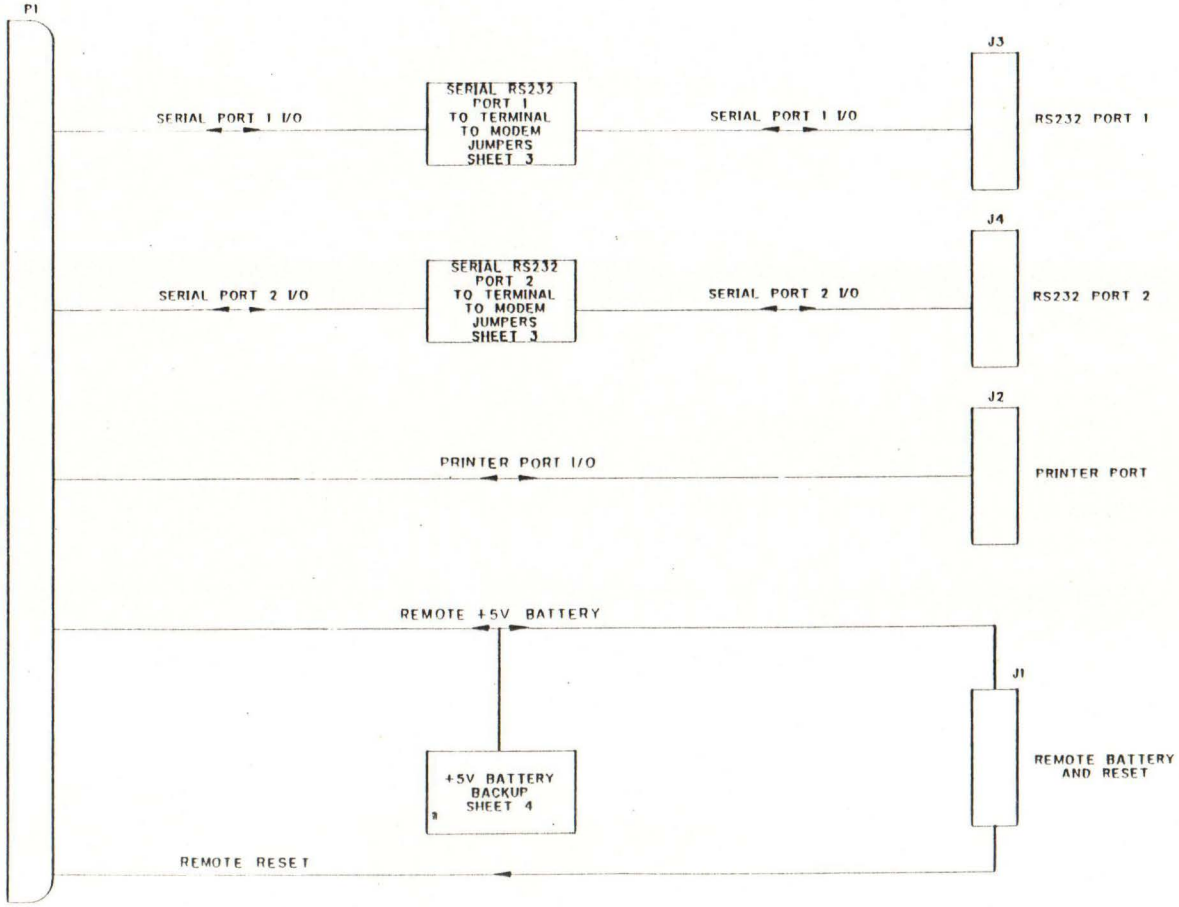
1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL @1 W3306B@1.
2. UNLESS OTHERWISE SPECIFIED: ALL VOLTAGES ARE DC.
3. SPECIAL SYMBOL USAGE: * DENOTES ACTIVE LOW SIGNAL.
4. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.

/5\ USERS OPTION, PARTS NOT INSTALLED.



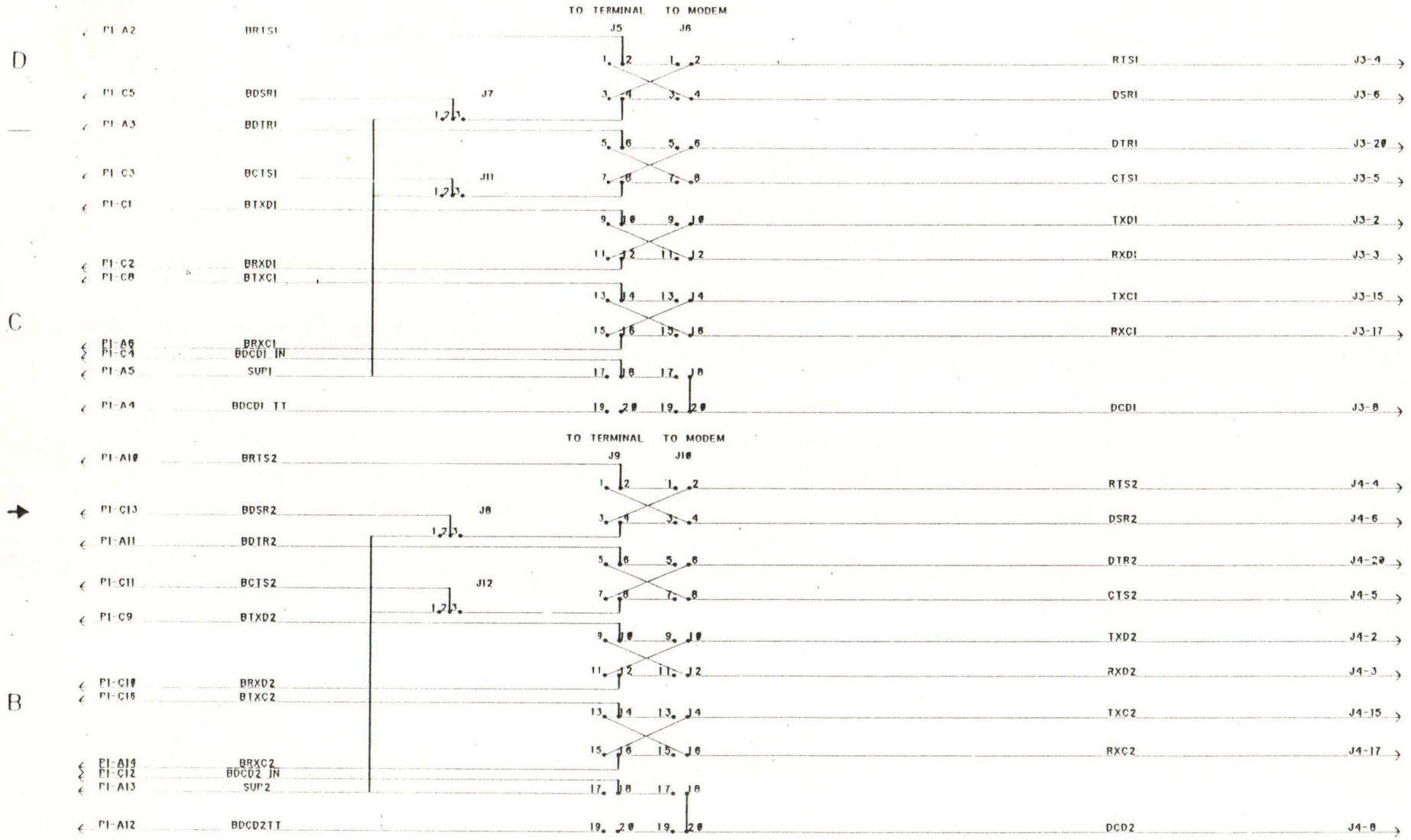
NOT USED

REFERENCE DESIGNATIONS	
P1	
J13	
BT4	
HIGHEST NUMBER USED	NOT USED



VME701 BLOCK DIAGRAM

FIGURE 5-5. MVME701 I/O Module Schematic Diagram


7
6
5
4
3
D
C
B
A
TO TERMINAL
TO MODEM
J5
J6
P1-A2
BRTS1
RTS1
J3-4
P1-C5
BDSR1
J7
DSR1
J3-6
P1-A3
BDTR1
DTR1
J3-20
P1-C3
BCTS1
J11
CTS1
J3-5
P1-C1
BTXD1
TXD1
J3-2
P1-C2
BRXD1
RXD1
J3-3
P1-C8
BTXC1
TXC1
J3-15
P1-A6
BRXC1
RXC1
J3-17
P1-C4
BDCD1 IN
P1-A5
SUP1
P1-A4
BDCD1 TT
DCD1
J3-8
TO TERMINAL
TO MODEM
J9
J10
P1-A10
BRTS2
RTS2
J4-4
P1-C13
BDSR2
J8
DSR2
J4-6
P1-A11
BDTR2
DTR2
J4-20
P1-C11
BCTS2
J12
CTS2
J4-5
P1-C9
BTXD2
TXD2
J4-2
P1-C10
BRXD2
RXD2
J4-3
P1-C16
BTXC2
TXC2
J4-15
P1-A14
BRXC2
RXC2
J4-17
P1-C12
BDCD2 IN
P1-A13
SUP2
P1-A12
BDCD2TT
DCD2
J4-8

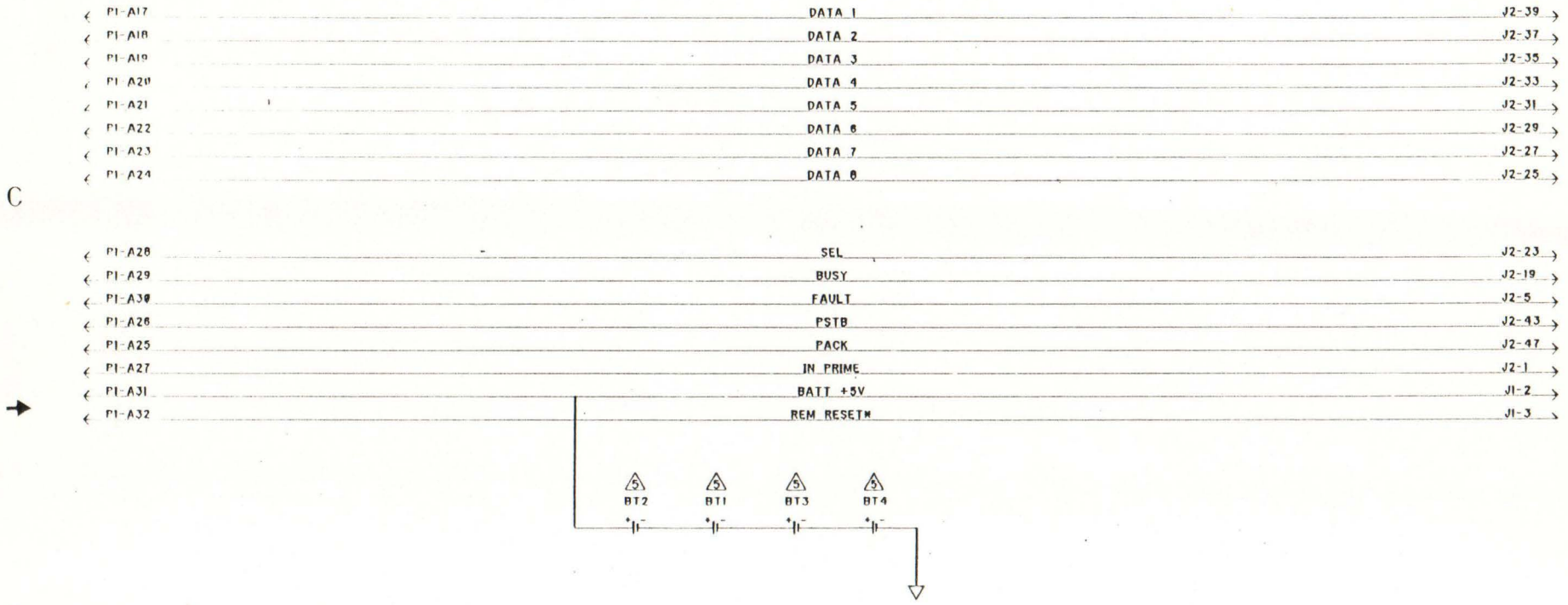
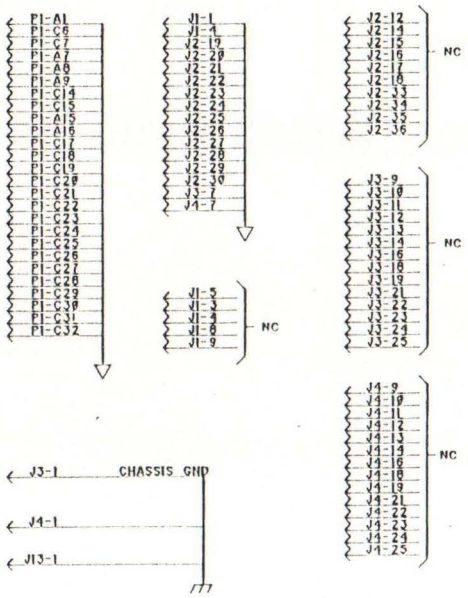


FIGURE 5-5. MVME701 I/O Module Schematic Diagram

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL @ W3427B01.
2. UNLESS OTHERWISE SPECIFIED:
   ALL VOLTAGES ARE DC.
3. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
4. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.

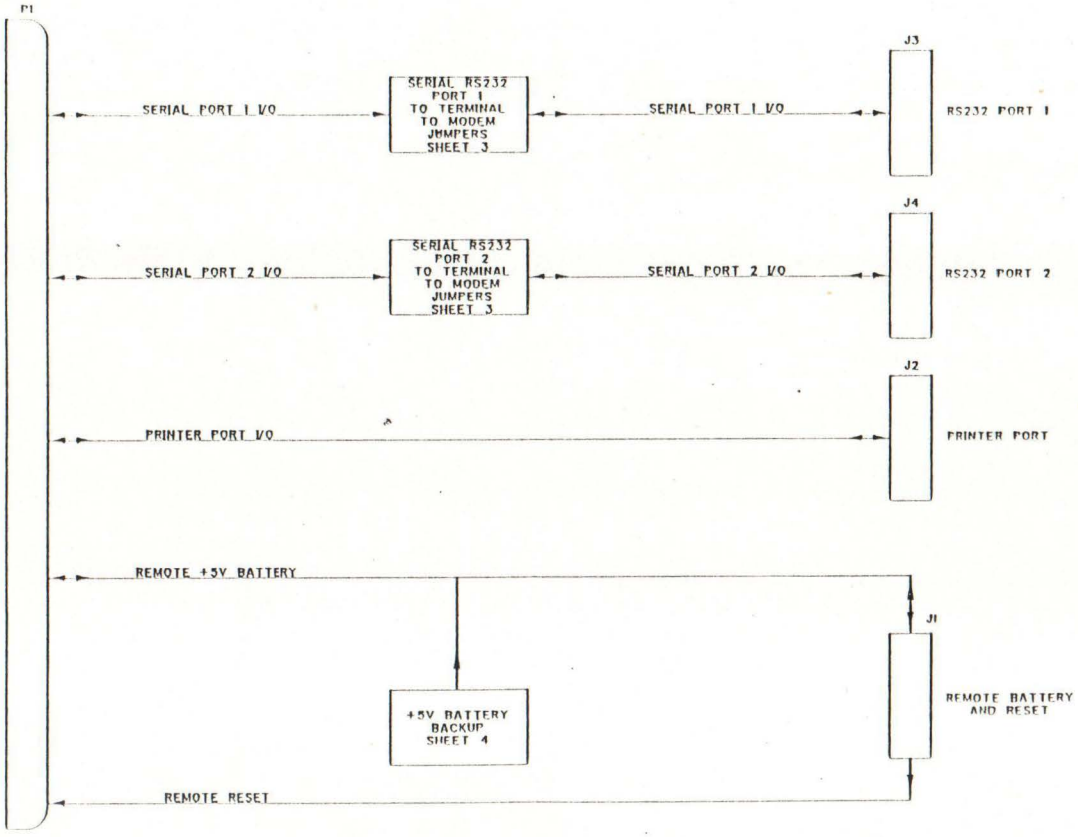
⚠ USERS OPTION, PARTS NOT INSTALLED.



P1	
J13	
BT4	
HIGHEST NUMBER USED	NOT USED
REFERENCE	DESIGNATIONS

63DW3427B REV A. SH 1 OF 4

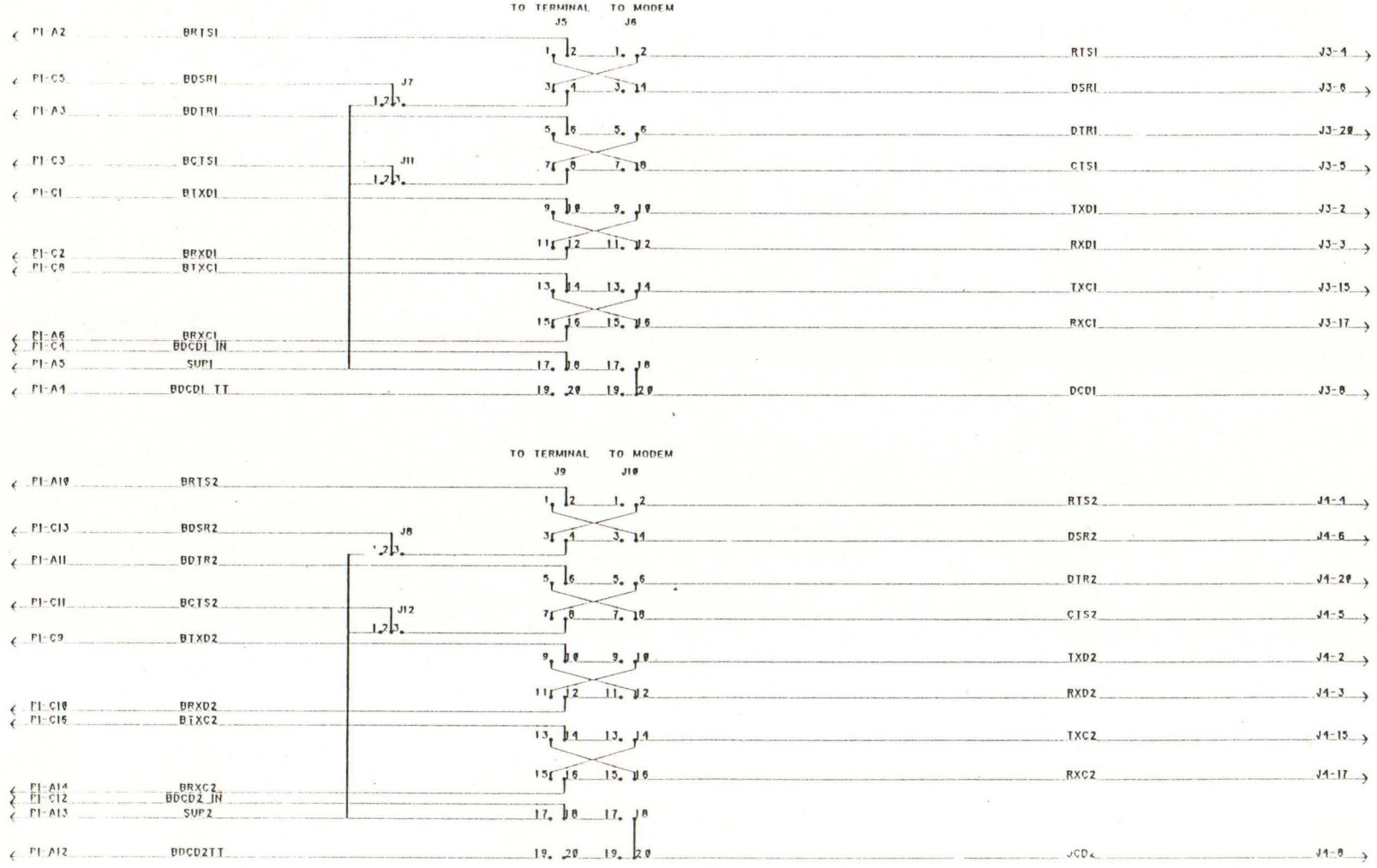
FIGURE 5-6. MVME701A I/O Module Schematic Diagram



VME701A BLOCK DIAGRAM

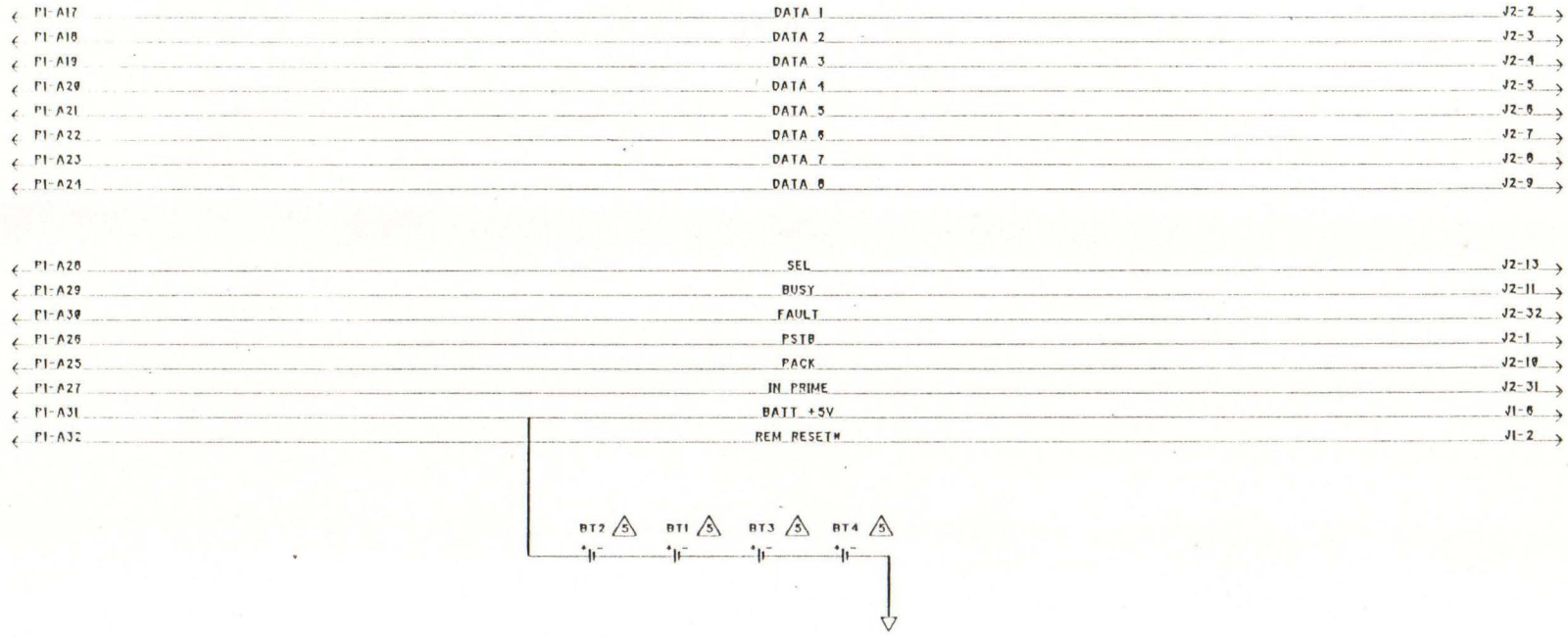
63DW3427B REV A SH 2 OF 4

FIGURE 5-6. MVME701A I/O Module Schematic Diagram



SERIAL PORTS
63DW3427B REV A SH 3 OF 4

FIGURE 5-6. MVME701A I/O Module Schematic Diagram



PRINTER PORT AND
BATTERY BACKUP
63DW3427B REV A SH 4 OF 4

FIGURE 5-6. MVME701A I/O Module Schematic Diagram

APPENDIX A

TIME-OF-DAY CLOCK COMPENSATION

The time-of-day clock function is controlled by crystal Y2. This is a 4.194304 MHz, 0.001% device specified over the temperature range of 0-70 degrees C. Assuming the crystal parameters of CO and CL are met by the particular circuit configuration, this time base provides the time-of-day clock with an inherent accuracy of +/- 5.26 minutes per year. While these parameters can be exactly matched for any selected module, matching many modules would require different values of tuning capacitance to compensate for varying circuit capacitance. Module capacitance, because of the crystal holder, MC146818 socket, etc., would possibly cause the frequency of Y2 to change beyond its tolerance, thus affecting long term clock accuracy.

An obvious method of performing this tuning would be through the use of an onboard trimmer capacitor. While this would be a method tuning, it could also introduce variation because of temperature, life degradation, and shock, as well as ease of accessibility.

A better method of time base adjustment would be to adjust any clock inaccuracies through a software compensation method. An example of this would be to allow the module to run in the final environment and determine how fast or how slow the clock device (MC146818) is actually running over a known period of time. A software update could then be made periodically to add or subtract the proper amount of seconds. The MC146818 alarm function might be used to generate a daily interrupt, with the corresponding interrupt service routine performing the adjustment.

Located next to the reset switch on the controller module, a trimmer capacitor (C47) is provided to adjust the frequency of the time-of-day clock, instead of the method listed above.

The time-of-day clock should be adjusted periodically to maintain its accuracy. For this procedure it is assumed the clock is powered from the VMEbus power supply. To adjust the time-of-day clock, proceed as follows:

a. Turn all equipment power OFF.

CAUTION

REMOVING/INSERTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

b. Remove the controller module from the chassis.

c. Install controller module on a VME compatible extender card and install in chassis.

d. Connect a frequency counter to pin 21 of the MC146818 device located at the lower front corner of the module.

e. Turn equipment power ON.

f. Adjust capacitor C47 until frequency reading is 1.048576 MHz.

g. Turn equipment power OFF, remove counter, remove extender card, install controller module in chassis, and turn equipment power ON, if desired.

This completes the adjustment of the time-of-day clock.

APPENDIX B

RS-232C INTERCONNECTIONS

The RS-232C standard is the most widely used interface between terminals and computers or modems, and yet it is not fully understood. This is because all the lines are not clearly defined, and many users do not see the need to conform for their applications. A system should easily connect to any other. Many times designers think only of their own equipment, but the state-of-the-art is computer-to-computer or computer-to-modem operation.

The RS-232C standard was originally developed by the Bell System to connect terminals via modems. Therefore, a number of handshaking lines were included. In many applications these are not needed, but since they permit diagnosis of problems, they are included in many applications.

Table 1 lists the standard RS-232C interconnections. To interpret this information correctly it is necessary to know that RS-232C is intended to connect a terminal to a modem. When computers are connected to computers without modems, one of them must be configured as a terminal and the other as a modem. Because computers are normally configured to work with terminals, they are said to be configured as a modem. Also, the signal levels must be between +3 and +15 volts for a high level, and between -3 and -15 volts for a low level. Any attempt to connect units in parallel may result in out of range voltages and is not allowed by the RS-232C specification.

TABLE 1. RS-232C Interconnections

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1		Not used.
2	TxD	TRANSMIT DATA - Data to be transmitted is furnished on this line to the modem from the terminal.
3	RxD	RECEIVE DATA - Data that is demodulated from the receive line is presented to the terminal by the modem.
4	RTS	REQUEST TO SEND - RTS is supplied by the terminal to the modem when required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.

TABLE 1. RS-232C Interconnections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
5	CTS	CLEAR TO SEND - Clear to send is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of a message. When using a modem, CTS follows the off-to-on transition of RTS after a time delay.
6	DSR	DATA SET READY - Data set ready is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
7	SIG-GND	SIGNAL GROUND - Common return line for all signals at the modem interface.
8	DCD	DATA CARRIER DETECT - Sent by the modem to the terminal to indicate that a valid carrier is being received.
9-14		Not used.
15	TxC	TRANSMIT CLOCK - This line clocks output data to the modem from the terminal.
16		Not used.
17	RxC	RECEIVE CLOCK - This line clocks input data from a terminal to a modem.
18,19		Not used.
20	DTR	DATA TERMINAL READY - A signal from the terminal to the modem indicating that the terminal is ready to send or receive data.
21		Not used.
22	RI	RING INDICATOR - RI is sent by the modem to the terminal. This line indicates to the terminal that an incoming call is present. The terminal causes the modem to answer the phone by carrying DTR true while RI is active.
23		Not used.
24	TxC	TRANSMIT CLOCK - Same as TxC on pin 15.

TABLE 1. RS-232C Interconnections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
25	BSY	BUSY - A positive EIA signal applied to this pin causes the modem to go off-hook and make the associated phone busy.

NOTES: 1. High level = +3 to +15 volts. Low level = -3 to -15 volts.

2. RS-232C is intended to connect a terminal to a modem. When computers are connected to computers without modems, one of the computers must be configured as a modem and the other as a terminal.

There are several levels of conformance that are appropriate for typical RS-232C interconnections. The bare minimum requirement is the two data lines and a ground . The full version of RS-232C requires 12 lines and accommodates automatic dialing, automatic answering, and synchronous transmission. A middle-of-the-road approach is illustrated in Figure 1.

One set of handshaking signals frequently implemented are RTS and CTS. CTS is used in many systems to inhibit transmission until the signal is high. In the modem application, RTS is turned around and returned as CTS after 150 microseconds. RTS is programmable in some systems to work with the older type 202 modem (half duplex). CTS is used in some systems to provide flow control to avoid buffer overflow. This is not possible if modems are used. It is usually necessary to make CTS high by connecting it to RTS or to some source of +12 volts such as the resistors shown in Figure 1. It is also frequently jumpered to an MC1488 gate that has its inputs grounded (the gate is provided for this purpose). Another signal used in many systems is DCD. The original purpose of this signal was to tell the system that the carrier tone from the distant modem was being received. This signal is frequently used by the software to display a message like CARRIER NOT PRESENT to help the user to diagnose failure to communicate. Obviously, if the system is designed properly to use this signal, and it is not connected to a modem, the signal must be provided by a pullup resistor or gate as described before (see Figure 1). Many modems expect a DTR high signal and issue a DSR. These signals are used by software to help prompt the operator for possible causes of trouble. The DTR signal is used sometimes to disconnect the phone circuit in preparation for another automatic call. It is necessary to provide these signals to talk to all possible modems (see Figure 1). As shown, Figure 1 is a good minimum configuration that almost always works. If the CTS and DCD signals are not received from the modem, the jumpers can be moved to provide the needed signal, artificially. Figure 2 shows a way that an RS-232C connector can be wired to enable a computer to connect to a basic terminal

with only three wires. This is based on the fact that most terminals have a DTR signal that is ON, and that can be used to pullup the CTS, DCD, and DSR signals. Two of these connectors wired back-to-back can be used. It must be realized that all the handshaking has been bypassed and possible diagnostic messages do not occur. Also the Tx and Rx lines may have to be crossed since Tx from a terminal is outgoing but the Tx line on a modem is an incoming signal.

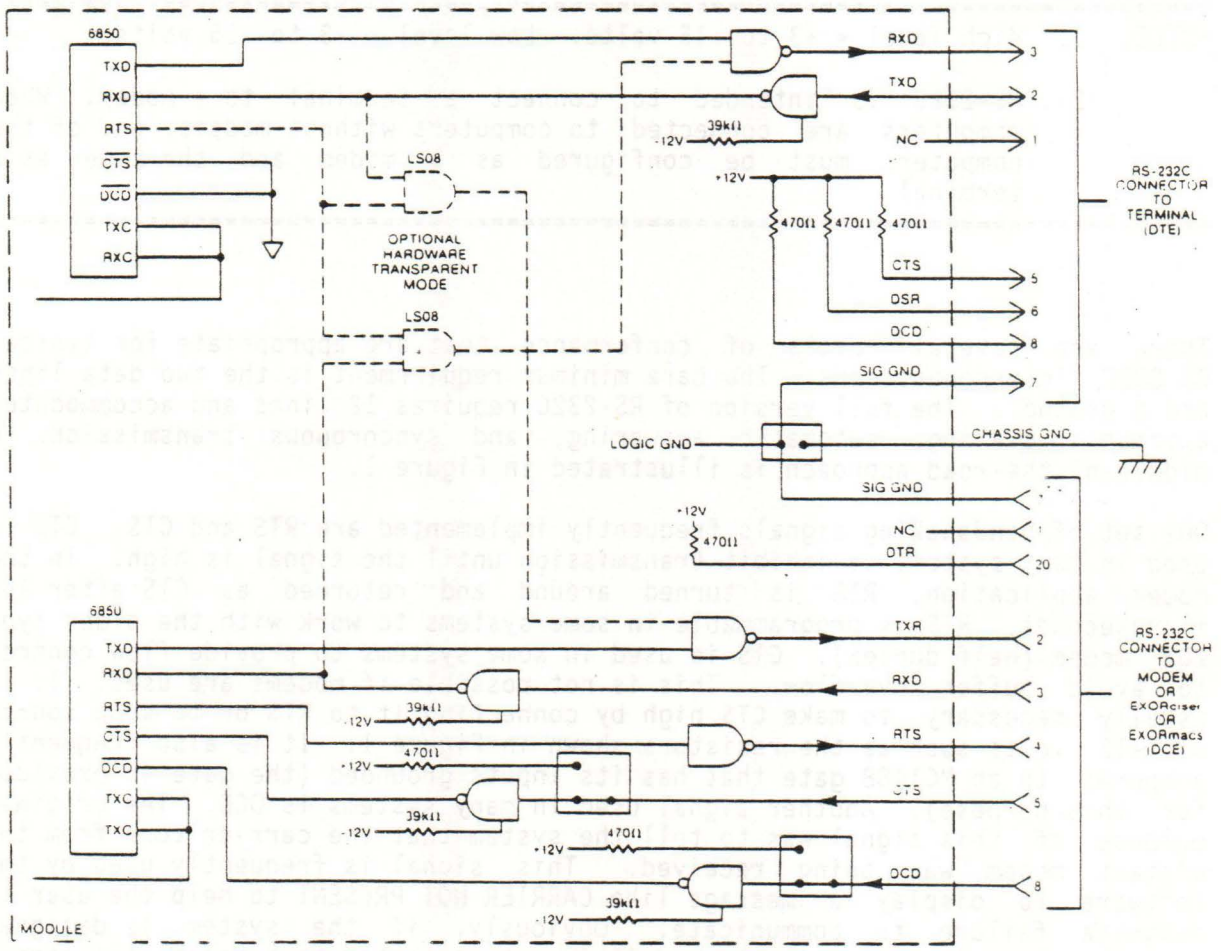


FIGURE 1. Middle-of-the-Road RS-232C Configuration

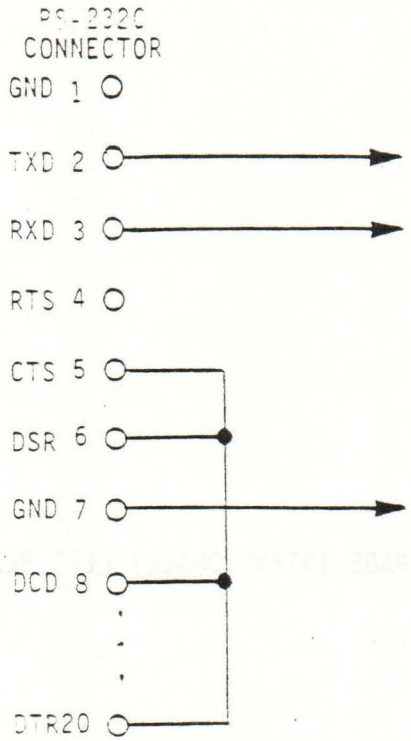


FIGURE 2. Minimum RS-232C Connection

Another subject that needs to be considered is the use of ground pins. There are two pins labeled GND. Pin 7 is the SIGNAL GROUND and must be connected to the distant device to complete the circuit. Pin 1 is the CHASSIS GROUND, but it must be used with care. The chassis is connected to the power ground through the green wire in the power cord and must be connected to the chassis to be in compliance with the electrical code. The problem is that when units are connected to different electrical outlets, there may be several volts difference in ground potential. If pin 1 of the devices are interconnected with a cable, several amperes of current could result. This not only may be dangerous for the small wires in a typical cable, but could result in electrical noise that could cause errors. That is the reason that Figure 1 shows no connection for pin 1. Normally, pin 7 should only be connected to the CHASSIS GROUND at one point, and if several terminals are used with one computer, the logical place for that point is at the computer. The terminals should not have a connection between the logic ground return and the chassis.

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APPENDIX C

PROGRAMMABLE ARRAY LOGIC

Programmable Array Logic (PAL) source code for the various devices on MVME050 is listed in the following pages. In the upper left corner of each page is the PAL number (PAL16L8B), the device reference designation (U108), and the schematic sheet number (SHEET 6). The pages are arranged in sheet number order.

AM PROM

TBP28S42 U38 SHEET 4

INPUTS			OUTPUTS		
PIN	PROM FUNCTION	SIGNAL	PIN	PROM FUNCTION	SIGNAL
1	A0	AM0	6	Q1	RRAM*
2	A1	AM1	7	Q2	IOAM*
3	A2	AM2	8	Q3	AM1E*
4	A3	AM3	9	Q4	AM16*
5	A4	AM4	11	Q5	EXTAM*
16	A5	AM5	12	Q6	NC
17	A6	LIACK*	13	Q7	NC
18	A7	GND	14	Q8	NC
19	A8	GND			
15	CS*	LOW			

The output RRAM* is used to qualify the EPROM or RAM address decoding on sheet 5 and 6 of the schematic.

The signal RRAM* will go true if:

LIACK* is HI (false) and an address modifier code of 09, 0A, 0D, 0E, 39, 3A, 3D, 3E is true.

The outout IOAM* is used to qualify the IO address decoding on sheet 4 of the schematic.

The signal IOAM* will go true if

LIACK* is HI (false) and an address modifer code of 29, or 2D is true.

The output AM1E* is used to enable EPROM quad one when a VME 120 board puts out the address modifier code of 1E during its reset vector fetch

The signal AM1E* will go true if:

LIACK* is HI (false) and an address modifer code of 1E is true

The output AM16* is used to enable EPROM quad two when a VME 120 board puts out the address modifier code of 16 during its reset vector fetch.

The signal AM16* will go true if:

LIACK* is HI (false) and an address modifer code of 16 is true.

The output EXTAM* is used to enable the address decoding circuit for the address lines A24 through A31. If this signal is false, these address lines are "dont cared".

The signal EXTAM* will go true if:

LIACK* is HI (false) and an address modifer code of 0A, 0B, 0D, 0E is true.

```
PALIOD   51AW4644B02        D093
82S153
U40 SHEET 4 VME 050     5 MAR 83

NOTE: a / in the pin definition means LOW true signal

LA05 LA06 LA07 LA08 /ENIO /WRITE DIOACK GC /ACKIO GND                  PIN
/IOSEL /TODSEL /BIM2 /BIM1 /SWITCH /LED /PNTR /MPCC2 /MPCC1 VCC        Definition

NOTE: a / in the output equations means FALSE
      a * in the output equations means AND
      a + in the output equations means OR

IF (VCC) MPCC1 =        /LA06*/LA07*/LA08*ENIO* WRITE*GC   ;READ
               +        /LA06*/LA07*/LA08*ENIO*/WRITE*/DIOACK*GC ;WRITE

IF (VCC) MPCC2 =        LA06*/LA07*/LA08*ENIO* WRITE*GC   ;READ
               +        LA06*/LA07*/LA08*ENIO*/WRITE*/DIOACK*GC ;WRITE

IF (VCC) PNTR  = /LA05*/LA06*LA07*/LA08*ENIO* WRITE*GC   ;READ
               + /LA05*/LA06*LA07*/LA08*ENIO*/WRITE*/DIOACK*GC ;WRITE

IF (VCC) LED   =
               + LA05*/LA06*LA07*/LA08*ENIO*/WRITE*/DIOACK*GC ;WRITE

IF (VCC) SWITCH =  LA05*/LA06*LA07*/LA08*ENIO* WRITE*GC   ;READ

IF (VCC) BIM1  = /LA05*LA06*LA07*/LA08*ENIO*GC   ;READ
               + /LA05*LA06*LA07*/LA08*ENIO*GC ;WRITE

IF (VCC) BIM2  =  LA05*LA06*LA07*/LA08*ENIO*GC   ;READ
               +  LA05*LA06*LA07*/LA08*ENIO*GC ;WRITE

IF (VCC) TODSEL = /LA07*LA08*ENIO*GC   ;READ OR WRITE

IF (VCC) IOSEL  =        /LA06*/LA07*/LA08*ENIO*GC   ;MPCC1
                +         LA06*/LA07*/LA08*ENIO*GC   ;MPCC2
                + /LA05*/LA06*LA07*/LA08*ENIO*GC     ;PNTR
                +  LA05*/LA06*LA07*/LA08*ENIO*GC     ;LED
                +  LA05*/LA06*LA07*/LA08*ENIO*GC     ;SWITCH
                + /LA05* LA06*LA07*/LA08*ENIO*GC     ;BIM1
                +  LA05*LA06*LA07*/LA08*ENIO*GC      ;BIM2
                +             /LA07*LA08*ENIO*GC     ;TODSEL
                +   LA05*LA06*LA07*/LA08*ENIO*GC     ;REDUNDANT

IF (VCC) ACKIO =         /LA06*/LA07*/LA08*ENIO*WRITE*GC          ;READ MPCC1
               +         /LA06*/LA07*/LA08*ENIO*/WRITE*DIOACK*GC  ;WRITE
               +          LA06*/LA07*/LA08*ENIO*WRITE*GC          ;READ MPCC2
               +          LA06*/LA07*/LA08*ENIO*/WRITE*DIOACK*GC  ;WRITE
               +  /LA05*/LA06*LA07*/LA08*ENIO*WRITE*GC            ;READ PNTR
               +  /LA05*/LA06*LA07*/LA08*ENIO*/WRITE*DIOACK*GC    ;WRITE
               +   LA05*/LA06*LA07*/LA08*ENIO*/WRITE*DIOACK*GC    ;WRITE LED
               +   LA05*/LA06*LA07*/LA08*ENIO*WRITE*GC           ;READ SWITCH
               +   /ACKIO*GC   , feedback term to hold ACKIO
                               , true until GC goes away
```

This is the I/O decoder for all the enables of the I/O functions.

Output Signal	Address	Function
MPCC1	FFXX00	Chip enable for first serial port (MPCC)
MPCC2	FFXX40	Chip enable for second serial port (MPCC)
PNTR	FFXX80	Chip enable for printer port
LED	FFXXA0	Chip enable for user display (write only)
SWITCH	FFXXA0	Chip enable for user readable switch (read only)
BIM1	FFXXC0	Chip enable for first BIM (no dtack on even bytes)
BIM1	FFXXE0	Chip enable for second BIM (no dtack on even bytes)
TODSEL	FFX100	Chip enable for time of day clock (no dtack on even bytes)

The output IOSEL (low true) turns on the data bus buffers and will go true if any I/O is selected

The output ACKIO (low true) starts the DTACK timing only for the I/O devices which cant generate a dtack. NOTE the BIMs and the time-of-day circuit generate their own dtack signal.

```
ADDRESS COMPARITOR    VME-050   51AW4644B01          97D3
82S153
U1 & U15 SHEETS 5 & 6      15 MAR 84

The following list of signals is the pin definition for this PAL.  The
first signal is for pin 1 and the next is for pin 2 etc.

The / before a signal means low true signal

LA1 LA16 LA15 LA14 J4 J3 J2 J1 /OUTEQ GND
/LSIZE5 SIZE5 SZ0 SZ1 SZ2 NC16 NC17 NC18 NC19 VCC

The following list is the output equations for each output in human
readable form.  The last listing lists the fuse numbers for programming
a part.

The / before a signal means FALSE.
The + means OR

IF (VCC) OUTEQ
         = 1 LOW TRUE                                                    AND T
                                                    * S2   */S1   * S0    00
+                                                   * S2   */S1   */S0    01
+  LA17                    * J4                     */S2   * S1   * S0    02
+ /LA17                    */J4                     */S2   * S1   * S0    03
+  LA17* LA16              * J4   * J3              */S2   * S1   */S0    04
+ /LA17* LA16              */J4   * J3              */S2   * S1   */S0    05
+  LA17*/LA16              * J4   */J3              */S2   * S1   */S0    06
+ /LA17*/LA16              */J4   */J3              */S2   * S1   */S0    07
+  LA17* LA16* LA15        * J4   * J3   * J2       */S2   */S1   * S0    08
+  LA17* LA16*/LA15        * J4   * J3   */J2       */S2   */S1   * S0    09
+  LA17*/LA16* LA15        * J4   */J3   * J2       */S2   */S1   * S0    10
+  LA17*/LA16*/LA15        * J4   */J3   */J2       */S2   */S1   * S0    11
+ /LA17* LA16* LA15        */J4   * J3   * J2       */S2   */S1   * S0    12
+ /LA17* LA16*/LA15        */J4   * J3   */J2       */S2   */S1   * S0    13
+ /LA17*/LA16* LA15        */J4   */J3   * J2       */S2   */S1   * S0    14
+ /LA17*/LA16*/LA15        */J4   */J3   */J2       */S2   */S1   * S0    15
+  LA17* LA16* LA15* LA14* J4   * J3   * J2   * J1   */S2   */S1   */S0    16
+  LA17* LA16* LA15*/LA14* J4   * J3   * J2   */J1   */S2   */S1   */S0    17
+  LA17* LA16*/LA15* LA14* J4   * J3   */J2   * J1   */S2   */S1   */S0    18
+  LA17* LA16*/LA15*/LA14* J4   * J3   */J2   */J1   */S2   */S1   */S0    19
+  LA17*/LA16* LA15* LA14* J4   */J3   * J2   * J1   */S2   */S1   */S0    20
+  LA17*/LA16* LA15*/LA14* J4   */J3   * J2   */J1   */S2   */S1   */S0    21
+  LA17*/LA16*/LA15* LA14* J4   */J3   */J2   * J1   */S2   */S1   */S0    22
+  LA17*/LA16*/LA15*/LA14* J4   */J3   */J2   */J1   */S2   */S1   */S0    23
+ /LA17* LA16* LA15* LA14*/J4   * J3   * J2   * J1   */S2   */S1   */S0    24
+ /LA17* LA16* LA15*/LA14*/J4   * J3   * J2   */J1   */S2   */S1   */S0    25
+ /LA17* LA16*/LA15* LA14*/J4   * J3   */J2   * J1   */S2   */S1   */S0    26
+ /LA17* LA16*/LA15*/LA14*/J4   * J3   */J2   */J1   */S2   */S1   */S0    27
+ /LA17*/LA16* LA15* LA14*/J4   */J3   * J2   * J1   */S2   */S1   */S0    28
+ /LA17*/LA16* LA15*/LA14*/J4   */J3   * J2   */J1   */S2   */S1   */S0    29
+ /LA17*/LA16*/LA15* LA14*/J4   */J3   */J2   * J1   */S2   */S1   */S0    30
+ /LA17*/LA16*/LA15*/LA14*/J4   */J3   */J2   */J1   */S2   */S1   */S0    31
```

```
IF (VCC) SIZE5 = S2 */S1 *S0
     HIGH TRUE

IF (VCC) LSIZE5 = S2 */S1 *S0
       LOW TRUE
```

This PAL is a programmable comparitor simular to the function of the 74LS682 s execpt that the three size inputs are used to determine how many of the address lines and jumpers to compare. If the size is zero, (all three size inputs low) the logic level of all of the address lines LA17 through LA14 must match the jumper levels J4 through J1 for the output OUTEQ to go true (low). There are sixteen possible combinations that the match may occur for size zero. If the size is set to one, the address line LA14 and the jumper J4 are dont cared so there are eight possible combinations that may match and assert the output OUTEQ. For size two, the address lines LA14 and LA15 and jumpers J1 and J2 are dont cared, and four possible combinations for a match. Size three will have address lines LA14, LA15, LA16 and jumpers J1, J2, J3 dont cared, and two possible combinations for a match. Size four has all the address lines and all the jumper inputs dont cared and the signal OUTEQ is held true. Size five also has the signal OUTEQ held true and the signal SIZE5 will be true (high) and the signal LSIZE5 will also be true (low).

```
PAL20L8
U39 VME-050   51AW4697B03   FB8C
RAM / ROM CHIP SELECT PAL FOR VME-050  SHEET 7  01 JUNE 84

/ROMEN2 /ROMEN1 /BDS0 LA01 ROMA /BDS1 /LLWORD /AM1E /AM16 NC /STB GND
/RAMEN2 /RAMEN1 /CS8 /CS7 /CS6 /CS5 /CS4 /CS3 /CS2 /CS1 RAMA VCC

IF (VCC) CS1 = STB*ROMEN2*ROMA*LA01*BDS0*/LLWORD ; D0 - D7
   + STB*ROMEN2*ROMA*LLWORD
   + STB*RAMEN1*/RAMA*LA01*BDS0*/LLWORD
   + STB*RAMEN1*/RAMA*LLWORD
   + STB*AM16*/ROMA*LA01*BDS0*/LLWORD
   + STB*AM16*/ROMA*LLWORD

IF (VCC) CS2 = STB*ROMEN2*ROMA*LA01*BDS1*/LLWORD ; D8 - D15
   + STB*ROMEN2*ROMA*LLWORD
   + STB*RAMEN1*/RAMA*LA01*BDS1*/LLWORD
   + STB*RAMEN1*/RAMA*LLWORD
   + STB*AM16*/ROMA*LA01*BDS1*/LLWORD
   + STB*AM16*/ROMA*LLWORD

IF (VCC) CS3 = STB*ROMEN2*ROMA*/LA01*BDS0*/LLWORD ; D16 - D23
   + STB*ROMEN2*ROMA*LLWORD
   + STB*RAMEN1*/RAMA*/LA01*BDS0*/LLWORD
   + STB*RAMEN1*/RAMA*LLWORD
   + STB*AM16*/ROMA*/LA01*BDS0*/LLWORD
   + STB*AM16*/ROMA*LLWORD

IF (VCC) CS4 = STB*ROMEN2*ROMA*/LA01*BDS1*/LLWORD ; D24 - D31
   + STB*ROMEN2*ROMA*LLWORD
   + STB*RAMEN1*/RAMA*/LA01*BDS1*/LLWORD
   + STB*RAMEN1*/RAMA*LLWORD
   + STB*AM16*/ROMA*/LA01*BDS1*/LLWORD
   + STB*AM16*/ROMA*LLWORD

IF (VCC) CS5 = STB*ROMEN1*/ROMA*LA01*BDS0*/LLWORD ; D0 - D7
   + STB*ROMEN1*/ROMA*LLWORD
   + STB*RAMEN2*RAMA*LA01*BDS0*/LLWORD
   + STB*RAMEN2*RAMA*LLWORD
   + STB*AM1E*/ROMA*LA01*BDS0*/LLWORD
   + STB*AM1E*/ROMA*LLWORD

IF (VCC) CS6 = STB*ROMEN1*/ROMA*LA01*BDS1*/LLWORD ; D8 - D15
   + STB*ROMEN1*/ROMA*LLWORD
   + STB*RAMEN2*RAMA*LA01*BDS1*/LLWORD
   + STB*RAMEN2*RAMA*LLWORD
   + STB*AM1E*/ROMA*LA01*BDS1*/LLWORD
   + STB*AM1E*/ROMA*LLWORD

IF (VCC) CS7 = STB*ROMEN1*/ROMA*/LA01*BDS0*/LLWORD ; D16 - D23
   + STB*ROMEN1*/ROMA*LLWORD
   + STB*RAMEN2*RAMA*/LA01*BDS0*/LLWORD
   + STB*RAMEN2*RAMA*LLWORD
   + STB*AM1E*/ROMA*/LA01*BDS0*/LLWORD
   + STB*AM1E*/ROMA*LLWORD
```

```
IF (VCC) CS8 = STB*ROMEN1*/ROMA*/LA01*BDS1*/LLWORD ; D24 - D31
   + STB*ROMEN1*/ROMA*LLWORD
   + STB*RAMEN2*RAMA*/LA01*BDS1*/LLWORD
   + STB*RAMEN2*RAMA*LLWORD
   + STB*AM1E*/ROMA*/LA01*BDS1*/LLWORD
   + STB*AM1E*/ROMA*LLWORD
```

****

ROM QUAD 2 ROM QUAD 1

RAM QUAD 1 RAM QUAD 2

XU33	XU25	XU16	XU8
D8-D15	D0-D7	D8-D15	D0-D7
CS2*	CS1*	CS6*	CS5*
XU36	XU28	XU19	XU11
D24-D31	D16-D23	D24-D31	D16-D23
CS4*	CS3*	CS8*	CS7*

****

The / means low true in the pin definitions

In the output equations

The * means AND

The / means FALSE

The + means OR

```
PAL16L8
U13 VME 050  51AW4281B12   46EE
FOUR LEVEL VME BUS ARBITOR  SHEET 11     5 MAR 84

PSBR0 PSBR1 PSBR2 PSBR3 NSBR0 NSBR1 NSBR2 NSBR3 LOW GND
/DGP /GP /BBSY /RESET /CLR /BG3OUT /BG2OUT /BG1OUT /BG0OUT VCC

IF (DGP) BG3OUT = PSBR3

IF (DGP) BG2OUT = /PSBR3*PSBR2

IF (DGP) BG1OUT = /PSBR3*/PSBR2*PSBR1

IF (DGP) BG0OUT = /PSBR3*/PSBR2*/PSBR1*PSBR0

IF (VCC) CLR = RESET
             + NSBR3*/PSBR3*BBSY
             + /PSBR3*NSBR2*/PSBR2*BBSY
             + /PSBR3*/PSBR2*NSBR1*/PSBR1*BBSY
             + /PSBR3*/PSBR2*/PSBR1*NSBR0*/PSBR0*BBSY


IF (VCC) GP =  /RESET*/BBSY*NSBR3
           +  /RESET*/BBSY*NSBR2
           +  /RESET*/BBSY*NSBR1
           +  /RESET*/BBSY*NSBR0

DESCRIPTION   VME 050 FOUR LEVEL BUS ARBITOR PAL

   The BUS GRANT OUT'S  are priortised so that grant 3 has the hightest
   priotity   BG3OUT* will be asserted if PSBR3 is true and DLYGNTPND* is
   true   BG2OUT* will be asserted if PSBR2 is true and PSBR3 is false and
   DLYGNTPND* is true   BG1OUT* will be asserted if PSBR1 is true and PSBR2
   is false and PSBR3 is false and DLYGNTPND* is true   BG0OUT will be asserted
   if PSBR0 is true and PSBR1 is false and PSBR2 is false and PSBR3 is false
   and DLYGNTPND* is true

  BUSCLR* will be asserted if BSYSRST* is asserted or if the next state of
  BR3 (NSBR3) is true and the present state of BR3 (PSBR3) is false and
  BBSY* is true ( this means the bus is still busy by the current bus master).
  likewise for the other levels

  Grant pending ( GNTPEND* ) is asserted when BSYSRST* is false and BBSY*
  is false and there is a bus request pending.   note normally BBSY*
  will be the last signal of this term to cause the output to true.

*****************************************************************

The / means low true in the pin definitions

In the output equasions

     The * means AND

     The / means FALSE
```

```
PAL16L8
U50   SHEET 11 VME 050  15 AUG 84      51AW4804B03     86E8
NEW SERIAL CLOCK & TIMEOUT CLOCK GENERATOR .

/PSA /PSB /PSC /PSD /PSE /ROM2 /A1E /A16 /STB GND
/ROM1 /ROMOE /NC13 /NSE /SC /NSD /NSC /NSB /NSA VCC

IF (VCC) NSE = PSE*/PSC
             + PSE*/PSB*/PSA
             + PSE*/PSD*PSB
             + PSE*PSB*/PSA
             + PSE*PSD*/PSB
             + /PSE*PSD*PSC*PSB*PSA

IF (VCC) NSD = PSD*/PSC
             + PSD*PSB*/PSA
             + PSD*/PSB
             + /PSD*PSC*PSB*PSA

IF (VCC) NSC = /PSC*PSB*PSA
             + PSC*PSB*/PSA
             + PSC*/PSB*/PSA
             + /PSE*PSC*/PSB
             + PSD*PSC*/PSB

IF (VCC) NSB = /PSC*/PSB*PSA
             + PSB*/PSA
             + /PSE*PSC*/PSB*PSA
             + PSD*PSC*/PSB*PSA

IF (VCC) NSA = /PSA

IF (VCC) SC  = /PSE*/PSD*PSC*PSB*/PSA
             + /PSE*PSD*/PSC*PSB*/PSA
             + PSE*/PSD*/PSC*/PSB*PSA
             + PSE*/PSD*PSC*/PSB*PSA

IF (VCC) ROMOE = ROM1*STB
               + ROM2*STB
               + A1E*STB
               + A16*STB

DESCRIPTION  SERIAL CLOCK PAL FOR VME 050     6-1-3-1 SEQUENCE
```

The above output equations form a state machine that follows the state table below. The inputs to the PAL are the present state of which the next state outputs will be derived. The states follow a binary counting scheme from count hex 0 to count hex 15. The present state of QE is used for the bus time-out circuit.

PRESENT STATE					NEXT STATE					OUTPUTS	
QE	QD	QC	QB	QA	QE	QD	QC	QB	QA	SC	Also the PS of QE is used as an output to the timeout circuit
0	0	0	0	0	0	0	0	0	1	0	
0	0	0	0	1	0	0	0	1	0	0	
0	0	0	1	0	0	0	0	1	1	0	
0	0	0	1	1	0	0	1	0	0	0	
0	0	1	0	0	0	0	1	0	1	0	
0	0	1	0	1	0	0	1	1	0	0	
0	0	1	1	0	0	0	1	1	1	1	
0	0	1	1	1	0	1	0	0	0	0	
0	1	0	0	0	0	1	0	0	1	0	
0	1	0	0	1	0	1	0	1	0	0	
0	1	0	1	0	0	1	0	1	1	1	
0	1	0	1	1	0	1	1	0	0	0	
0	1	1	0	0	0	1	1	0	1	0	
0	1	1	0	1	0	1	1	1	0	0	
0	1	1	1	0	0	1	1	1	1	0	
0	1	1	1	1	1	0	0	0	0	0	
1	0	0	0	0	1	0	0	0	1	0	
1	0	0	0	1	1	0	0	1	0	1	
1	0	0	1	0	1	0	0	1	1	0	
1	0	0	1	1	1	0	1	0	0	0	
1	0	1	0	0	1	0	1	0	1	0	
1	0	1	0	1	0	0	0	0	0	1	
1	0	1	1	0	1	0	1	1	1	0	The following 10 states
1	0	1	1	1	1	1	0	0	0	0	are legal states but not
1	1	0	0	0	1	1	0	0	1	0	used. The circuit will go
1	1	0	0	1	1	1	0	1	0	0	to the normal counting
1	1	0	1	0	1	1	0	1	1	0	within 10 clocks.
1	1	0	1	1	1	1	1	0	0	0	
1	1	1	0	0	1	1	1	0	1	0	
1	1	1	0	1	1	1	1	1	0	0	
1	1	1	1	0	1	1	1	1	1	0	
1	1	1	1	1	0	0	0	0	0	0	

****

The / means low true in the pin definitions

In the output equations

The * means AND

The / means FALSE

The + means AND

```
PRINTER
82S153                19 MAR 83
U 73 VME050     51AW4644B03    D050

The following list of signals is the pin definition for this PAL. The
first signal is for pin 1 and the next is for pin 2 etc.

The / before a signal means low true signal.

BD03 /PNTR3 /PNTR7 /RESET /WRITE /PACK /FAILSN /SFAIL A01 GND
/SW8 /LEDBI  FFLED FFPS FFIP BD07 PNTACK PSTB /INPRIM VCC

The following list is the output equations for each output in human
readable form. The last listing lists the fuse numbers for programming
a part.

The / before a signal means FALSE.
The + means OR
The * means AND


IF (VCC) FFLED  = FFLED RESET WRITE
       hi true
                + /A01 FFLED  RESET

                + FFLED  FAILSN  RESET

                + A01 /BD03 /WRITE /FAILSN


IF (VCC)  LEDBI = A01 LEDBI  RESET /WRITE /FAILSN
        hi true
                + /SW8

                + FFLED  RESET  WRITE

                + /A01 FFLED  RESET

                + FFLED  RESET  FAILSN

The above terms make a D type flip-flop.


IF (/A01 WRITE /FAILSN)  BD07 = SFAIL
                       HI TRUE

These are the terms to read the status of SYSFAIL* on the VMEbus.


IF (VCC) /PNTACK= /PNTACK /ACK
        LOW TRUE
                + /PNTR3 WRITE

                + /RESET

The above terms make a set-reset type flip-flop.
```

```
IF (VCC) /FFPS =  /FFPS  PNTR3
      LOW TRUE
                + /FFPS WRITE
                + /RESET
                +  BD03 /PNTR3 /WRITE

IF (VCC) /PSTB  = /PSTB /PNTR3 /WRITE
                + /FFPS WRITE
                + /RESET
                + /FFPS PNTR3
```

The above terms make a D type flip-flop with the D input tied high.

```
IF (VCC) /FFIP  = /FFIP PNTR7
      LOW TRUE
                + /FFIP WRITE
                + /RESET
                +  BD03 /PNTR7 /WRITE

IF (VCC) /INP   = /INP /PNTR7 /WRITE
     LOW TRUE
                + /FFIP WRITE
                + /RESET
                + /FFIP PNTR7
```

The above terms make a D type flip-flop.

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MOTOROLA

Rockwell

R68560, R68561 MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC)

PRELIMINARY

DESCRIPTION

The R68560, R68561 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 68008/68000 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, two channel DMA interface and three separate interrupt vector numbers optimize MPCC performance to take full advantage of the 68008/68000 processing capabilities and asynchronous bus structure.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYNC) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 22 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC68440/MC68450 DMA Controllers. Three prioritized interrupt vector numbers separately support receiver, transmitter and modem interface operation.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

The 48-pin R68561 supports word-length (16-bit) operation when connected to the 68000 16-bit asynchronous bus, as well as byte-length (8-bit) operation when connected to the 68008 8-bit bus. The 40-pin R68560 supports byte-length operation on the 68008 bus.

FEATURES

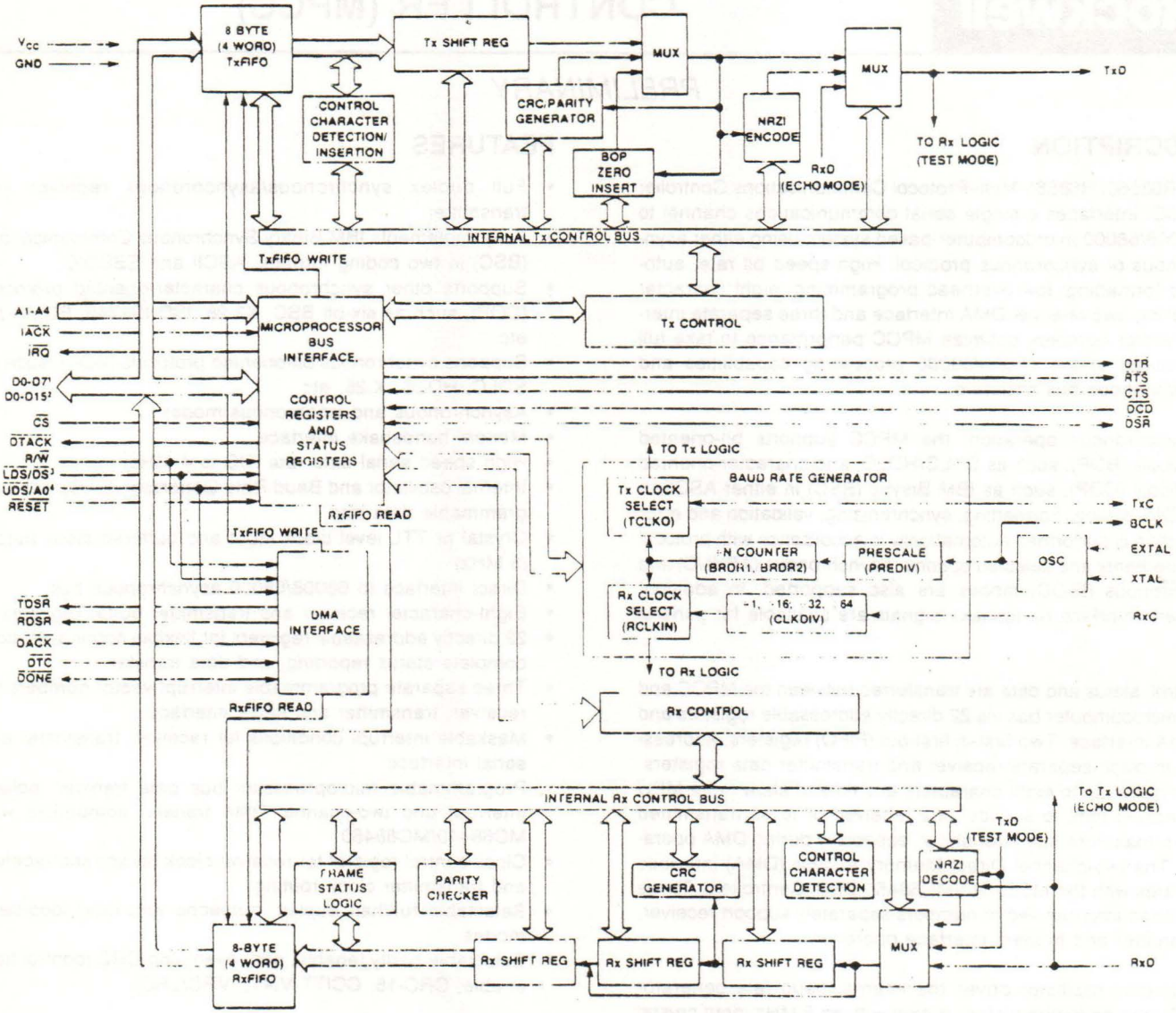
- Full duplex synchronous/asynchronous receiver and transmitter
- Fully implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, X3.28, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit-oriented protocols (BOP), such as SDLC, HDLC, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and Baud Rate Generator (BRG) with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 68008/68000 asynchronous bus
- Eight-character receiver and transmitter buffer registers
- 22 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Three separate programmable interrupt vector numbers for receiver, transmitter and serial interface
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer: polled, interrupt and two-channel DMA transfer compatible with MC68440/MC68450
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41,, VRC/LRC)

ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R6856 _ _	4 MHz	0°C to 70°C

Package: C = Ceramic, P = Plastic

Number of pins: 0 = 40, 1 = 48



NOTES:
1. R68560 ONLY.
2. R68561 ONLY.
3. UDS ON R68561 A0 ON R68560
4. LDS ON R68561 DS ON R68560

Figure 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a write is active low and a read active high.

Note: The R68561 interface is described for word mode operation only and the R68560 interface is described for byte mode operation only.

A1 – A4—Address Lines. A1 – A4 are active high inputs used in conjunction with the $\overline{CS}$ input to access the internal registers. The address map for these registers is shown in Table 1.

D0 – D15—Data Lines. The bidirectional data lines transfer data between the MPCC and the MPU, memory or other peripheral device. D0 – D15 are used when connected to the 16-bit 68000 bus and operating in the MPCC word mode. D0 – D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the MPCC byte mode. The data bus is three-stated when $\overline{CS}$ is inactive. (See exceptions in DMA mode.)

$\overline{CS}$—Chip Select. $\overline{CS}$ low selects the MPCC for programmed transfers with the host. The MPCC is desclected when the $\overline{CS}$ input is inactive in non-DMA mode. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

R/$\overline{W}$—Read/Write. R/$\overline{W}$ controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

$\overline{DTACK}$—Data Transfer Acknowledge. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MPCC after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. DTACK is driven high after assertion prior to being tri-stated. A holding resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{DS}$—Data Strobe (R68560). During a write (R/$\overline{W}$ low), the $\overline{DS}$ positive transition latches data on data bus lines D0 – D7 into the MPCC. During a read (R/$\overline{W}$ high), $\overline{DS}$ low enables data from the MPCC to data bus lines D0 – D7.

$\overline{LDS}$—Lower Data Strobe (R68561). During a write (R/$\overline{W}$ low), the positive transition latches data on the data bus lines D0 – D7 (and on D8 – D15 if UDS is low) into the MPCC. During a read (R/$\overline{W}$ high), $\overline{LDS}$ low enables data from the MPCC to D0 – D7 (and to D8 – D15 if $\overline{UDS}$ is low).

A0—Address Line A0 (R68560). When interfacing to an 8-bit data bus system such as the 68008, address line A0 is used to access an internal register. A0 = 0 defines an even register and A0 = 1 defines an odd register. See Table 1b.

$\overline{UDS}$—Upper Data Strobe (R68561). When interfacing to a 16-bit data bus system such as the 68000, a low on control bus signal $\overline{UDS}$ enables access to the upper data byte on D8 – D15. A high on $\overline{UDS}$ disables access to D8 – D15. Data is latched and enabled in conjunction with $\overline{LDS}$.

$\overline{IRQ}$—Interrupt Request. The active low $\overline{IRQ}$ output requests interrupt service by the MPU. $\overline{IRQ}$ is driven high after assertion prior to being tri-stated.

$\overline{IACK}$—Interrupt Acknowledge. The active low $\overline{IACK}$ input indicates that the current bus cycle is an interrupt acknowledge cycle. When $\overline{IACK}$ is asserted the MPCC places an interrupt vector on the lower byte (D0 – D7) of the data bus.

$\overline{TDSR}$—Transmitter Data Service Request. When Transmitter DMA mode is active, the low $\overline{TDSR}$ output requests DMA service.

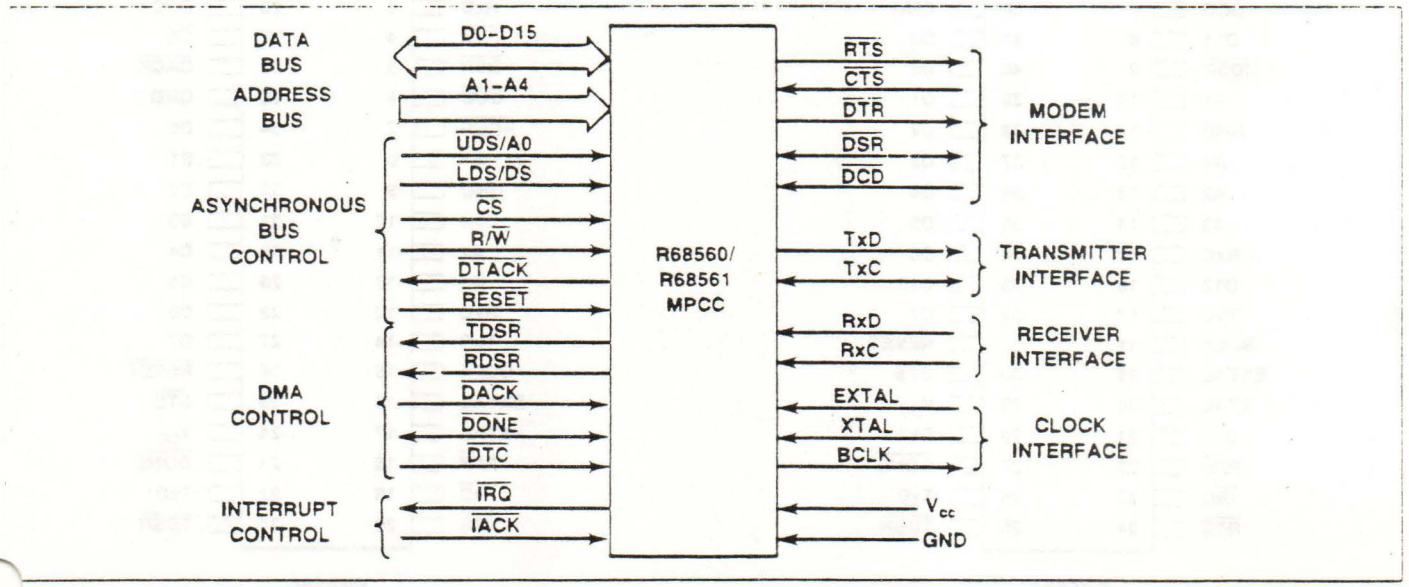


Figure 2. MPCC Input and Output Signals

$\overline{\text{RDSR}}$—Receiver Data Service Request. When receiver DMA mode is active, the low $\overline{\text{RDSR}}$ output requests DMA service.

$\overline{\text{DACK}}$—DMA Acknowledge. The $\overline{\text{DACK}}$ low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

$\overline{\text{DTC}}$—Data Transfer Complete. The $\overline{\text{DTC}}$ low input indicates that a DMA data transfer is complete. $\overline{\text{DTC}}$ in response to a $\overline{\text{RDSR}}$ indicates that the data has been successfully stored in memory. $\overline{\text{DTC}}$ in response to a $\overline{\text{TDSR}}$ indicates that the data is present on the data bus for strobing into the MPCC. $\overline{\text{DTC}}$ is used in conjunction with R/$\overline{\text{W}}$ to increment the TxFIFO or RxFIFO pointer.

$\overline{\text{DONE}}$—Done. $\overline{\text{DONE}}$ is a bidirectional active low signal. The $\overline{\text{DONE}}$ signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or asserted by the MPCC when the status byte following the last character of a frame (block) is being transferred in response to a $\overline{\text{RDSR}}$. The $\overline{\text{DONE}}$ signal asserted by the DMAC in response to a $\overline{\text{TDSR}}$ will be stored to track with the data byte (lower byte for word transfer) through the TxFIFO.

$\overline{\text{RESET}}$—Reset. $\overline{\text{RESET}}$ is an active low, high impedance input that initializes all MPCC functions. $\overline{\text{RESET}}$ must be asserted for at least 500 ns to initialize the MPCC.

$\overline{\text{DTR}}$—Data Terminal Ready. The $\overline{\text{DTR}}$ active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR).

$\overline{\text{RTS}}$—Request to Send. The $\overline{\text{RTS}}$ active low output is general purpose in nature, and is controlled by the RTSLVL bit in the SICR.

$\overline{\text{CTS}}$—Clear to Send. The $\overline{\text{CTS}}$ active low input positive transition and level are reported in the CTST and CTSLVL bits in the Serial Interface Status Register (SISR), respectively.

$\overline{\text{DSR}}$—Data Set Ready. The $\overline{\text{DSR}}$ active low input negative transition and level are reported in the DSRT and DSRLVL bits in the SISR, respectively. $\overline{\text{DSR}}$ is also an output for RSYN.

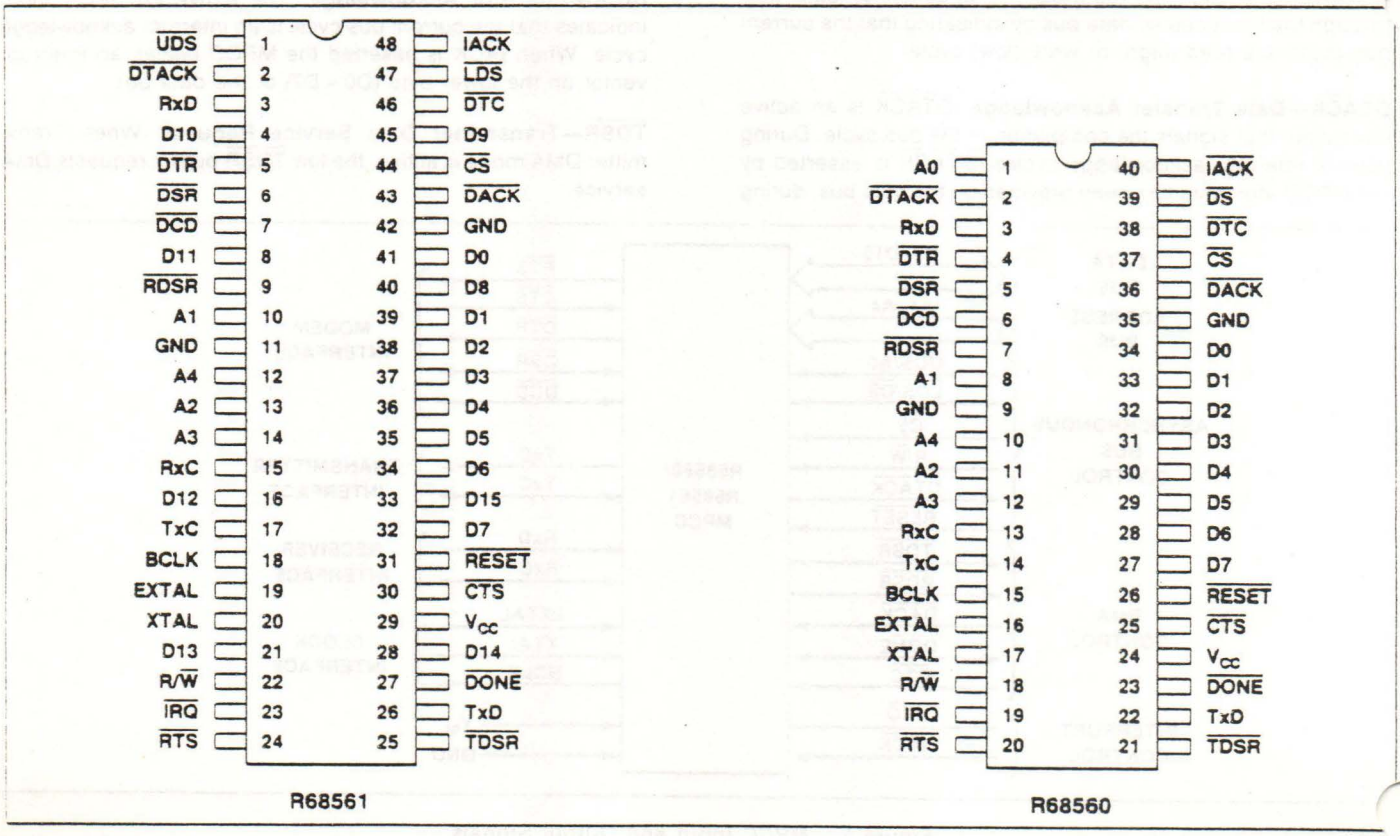
$\overline{\text{DCD}}$—Data Carrier Detect. The $\overline{\text{DCD}}$ active low input positive transition and level are reported in the DCDT and DCDLVL bits in the the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of TxC.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the negative going edge of RxC.

TxC—Transmitter Clock. TxC can be programmed to be an input or an output. When TxC is selected to be an input, the transmitter clock must be provided externally. When TxC is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator. The low-to-high transition of the clock signal nominally indicates the center of a serial data present on the TxD output.

RxC—Receiver Clock. RxC provides the MPCC receiver with received data timing information. . .



Pin Configuration

EXTAL—Crystal/External Clock Input.
XTAL Crystal Return. EXTAL and XTAL connect an 8 MHz external crystal to the MPCC internal oscillator. The pin EXTAL may also be used as a TTL level input to supply a DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

Vcc—Power. 5V ± 5%.

GND—Ground. Ground (V_{SS}).

MPCC REGISTERS

Twenty-two registers control and monitor the MPCC operation. The registers and their addresses are identified in Table 1a (R68561 operation in word mode) and in Table 1b (R68560 operation in byte mode). When the R68561 is operated in the word mode, two registers are read or written at a time starting at an even boundary. When the R68560 is operated in the byte mode, each register is explicitly addressed based on A0.

Table 2 summarizes the MPCC register bit assignments and their access. A read from an unassigned location results in a read from a "null register." A null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.

Table 1a. R68561 Accessible Registers (Word Mode)

Register(s)		R/W	Addr (Hex.)	Address Lines A4 A3 A2 A1
15 8	7 0			
Receiver Control Register (RCR)	Receiver Status Register (RSR)	R/W	00	0 0 0 0
Receiver Data Register (RDR)—16 bits[1]		R	02	0 0 0 1
Receiver Interrupt Enable Register (RIER)	Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0 0 1 0
Transmitter Control Register (TCR)	Transmitter Status Register (TSR)	R/W	08	0 1 0 0
Transmitter Data Register (TDR)—16 bits[2]		W	0A	0 1 0 1
Transmitter Interrupt Enable Register (TIER)	Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0 1 1 0
Serial Interface Control Register (SICR)	Serial Interface Status Register (SISR)	R/W	10	1 0 0 0
Reserved[3]	Reserved[3]	R/W	12	1 0 0 1
Serial Interrupt Enable Register (SIER)	Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1 0 1 0
Protocol Select Register 2 (PSR2)	Protocol Select Register (PSR1)	R/W	18	1 1 0 0
Address Register 2 (AR2)	Address Register 1 (AR1)	R/W	1A	1 1 0 1
Band Rate Divider Register 2 (BRDR2)	Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1 1 1 0
Error Control Register (ECR)	Clock Control Register (CCR)	R/W	1E	1 1 1 1

Notes:
1. Accessible register of the four word RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first word.
2. Accessible register of the four word TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first word.
3. Reserved registers may contain random bit values.

Table 1b. R68560 Accessible Registers (Byte Mode)

Register(s)	R/W	Addr (Hex.)	Address Lines A4	A3	A2	A1	A0
7 0							
Receiver Status Register (RSR)	R/W	00	0	0	0	0	0
Receiver Control Register (RCR)	R/W	01	0	0	0	0	1
Receiver Data Register (RDR)—8 bits[1]	R	02	0	0	0	1	0
Reserved[3]		03	0	0	0	1	1
Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0	0	1	0	0
Receiver Interrupt Enable Register (RIER)	R/W	05	0	0	1	0	1
Transmitter Status Register (TSR)	R/W	08	0	1	0	0	0
Transmitter Control Register (TCR)	R/W	09	0	1	0	0	1
Transmitter Data Register (TDR)[2]—8 bits	W	0A	0	1	0	1	0
Reserved[3]		0B	0	1	0	1	1
Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0	1	1	0	0
Transmitter Interrupt Enable Register (TIER)	R/W	0D	0	1	1	0	1
Serial Interface Status Register (SISR)	R/W	10	1	0	0	0	0
Serial Interface Control Register (SICR)	R/W	11	1	0	0	0	1
Reserved[3]		12	1	0	0	1	0
Reserved[3]		13	1	0	0	1	1
Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1	0	1	0	0
Serial Interrupt Enable Register (SIER)	R/W	15	1	0	1	0	1
Protocol Select Register 1 (PSR1)	R/W	18	1	1	0	0	0
Protocol Select Register 2 (PSR2)	R/W	19	1	1	0	0	1
Address Register 1 (AR1)	R/W	1A	1	1	0	1	0
Address Register 2 (AR2)	R/W	1B	1	1	0	1	1
Band Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0	0
Baud Rate Divider Register 2 (BRDR2)	R/W	1D	1	1	1	0	1
Clock Control Register (CCR)	R/W	1E	1	1	1	1	0
Error Control Register (ECR)	R/W	1F	1	1	1	1	1

Notes:

1. Accessible register of the eight byte RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first byte.
2. Accessible register of the eight byte TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first byte.
3. Reserved registers may contain random bit values.

Table 2. MPCC Register Bit Assignments

R/W Access	Bit Number 7	6	5	4	3	2	1	0	Reset[1] Value	
R/W	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
R/W	0	RDSREN	DONEEN	RSYNEN	STRSYN	2ADCMP	RABTEN	RRES	01	Receiver Control Register (RCR)
R	RECEIVED DATA (RxFIFO)[2]								— —	Receiver Data Register (RDR)
R/W	RECEIVER INTERRUPT VECTOR NUMBER (RIVN)								0F	Receiver Interrupt Vector Number Register (RIVNR)
R/W	RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0	00	Receiver Interrupt Enable Register (RIER)
R/W	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
R/W	TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
W	TRANSMITTED DATA (TxFIFO)[2]								— —	Transmitter Data Register (TDR)
R/W	TRANSMITTER INTERRUPT VECTOR NUMBER (TIVN)								0F	Transmitter Interrupt Vector Number Register (TIVNR)
R/W	TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	0	00	Transmitter Interrupt Enable Register (TIER)
R/W	CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
R/W	RTSLVL	DTRLVL	0	0	0	ECHO	TEST	NRZI	00	Serial Interface Control Register (SICR)
12	RANDOM BIT VALUES									(reserved)
13	RANDOM BIT VALUES									(reserved)
R/W	SERIAL INTERRUPT VECTOR NUMBER (SIVN)								0F	Serial Interrupt Vector Number Register (SIVNR)
R/W	CTS IE	DSR IE	DCD IE	0	0	0	0	0	00	Serial Interrupt Enable Register (SIER)
R/W	0	0	0	0	0	0	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
R/W	WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL			00	Protocol Select Register 2 (PSR2)
		SB2	SB1	CL2	CL1	PS3	PS2	PS1		
R/W	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
R/W	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
R/W	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
R/W	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
R/W	0	0	0	PSCDIV	TCLKO	RCLKIN	CLK SEL		00	Clock Control Register (CCR)
							CK2	CK1		
R/W	PAREN	ODDPAR	0	0	CTLCRC	CRCPRE	CRC SEL		04	Error Control Register (ECR)
							CR2	CR1		

Notes:
1. RESET = Register contents upon power up or $\overline{\text{RESET}}$.
2. 16-bits for R68561 (word mode); 8-bits for R68560 (byte mode).

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

Reset Value = $00

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by $\overline{\text{RESET}}$. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the first byte or word in the RxFIFO) must be read prior to resetting the corresponding status bit in the RSR. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR
7 **RDA —Receiver Data Available.** (RSR only).
0 The RxFIFO is empty (i.e., no received data is available).
1 Received data is available in the RxFIFO and can be read via the RDR.

RSR
6 **EOF —End of Frame.**
0 No end of frame or block detected.
1 End of frame or block detected (BOP and BSC).

RSR
5 **RHW —Receive Half Word.** (Frame Status only)*
0 The last word of the frame contains data on the upper half (D8 – D15) and frame status on the lower half (D0 – D7) of the data bus.
1 The lower half of the data bus (D0 – D7) contains the frame status but the upper half (D8 – D15) is blank or invalid.

RSR
4 **C/PERR —CRC/Parity Error.**
0 No CRC or parity error detected.
1 CRC error detected (BOP, BSC), Parity error detected (ASYNC, ISOC and COP).

RSR
3 **FRERR —Frame Error.**
0 No frame error detected.
1 Short Frame or a closing FLAG detected off boundary (BOP), Frame error (ASYNC, ISOC) or receiver overrun.

RSR
2 **ROVRN —Receiver Overrun.**
0 No receiver overrun detected.
1 Receiver overrun detected. Indicates that receiver data was attempted to be transferred into the RxFIFO when it was full, resulting in loss of received data. The data that is already in RxFIFO are not affected and may be read by the processor.

RSR
1 **RA/B —Receiver Abort/Break.**
0 Normal Operation.
1 ABORT detected after an opening flag (BOP), ENQ detected in a block of text data (BSC), or BREAK detected (ASYNC).

RSR
0 **RIDLE —Receiver Idle.** (RSR only).
0 Receiver not idle.
1 15 or more consecutive "1's" have been received and the receiver is in an inactive idle state.

***Frame Status (RSR)**

7	6	5	4	3	2	1	0
0	EOF	RHW	C/PERR	FRERR	ROVRN	RA/B	0

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the RxFIFO following the last data byte of each block. The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE. But, in addition to the RSR contents, the frame status byte has a RHW status in bit 5 which indicates either an even or odd boundary (applicable to word mode only).

If the MPCC is in word mode and the last data byte was on an even byte boundary (i.e., there was an even number of bytes in the message), a blank byte will be loaded into the RxFIFO prior to loading the frame status byte in order to force the "frame status" byte and the next frame to be on an even boundary. When RHW = 0, the last word of the frame contains data on the upper half and status on the lower half of the data bus. If RHW = 1, the lower half of the bus contains status but the upper half is a blank or invalid byte.

In the byte mode, the status byte will always immediately follow the last data byte of the block/frame (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the RxFIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

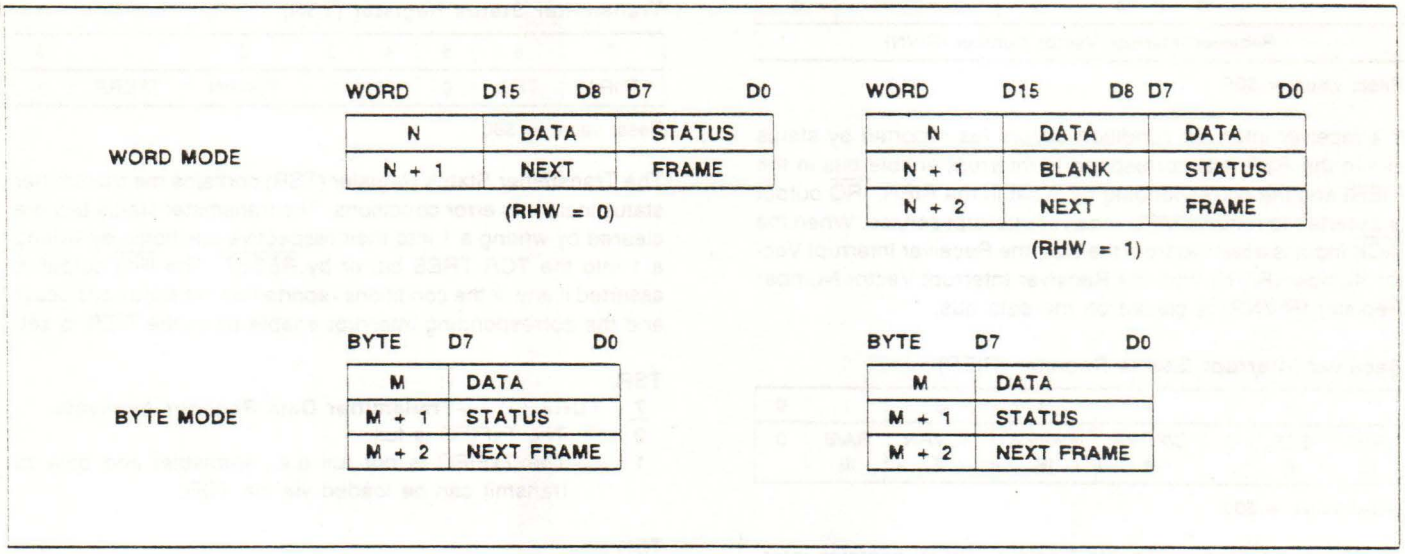


Figure 3. BSC/BOP Block/Frame Status Location

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
—	RDSREN	DONEEN	RSYNEN	STRSYN	2ADCMP	RABEN	RRES

Reset value = $01

The Receiver Control Register (RCR) selects receiver control options.

RCR 7 —**Not used.**

RCR 6 **RDSREN —Receiver Data Service Request Enable.**
- 0 Disable receiver DMA mode.
- 1 Enable receiver DMA mode.

RCR 5 **DONEEN —$\overline{\text{DONE}}$ Output Enable.**
- 0 Disable $\overline{\text{DONE}}$ output.
- 1 Enable $\overline{\text{DONE}}$ output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR 4 **RSYNEN —RSYNEN Output Enable.** Selects the DSR signal input or the RSYN SYNC signal output on the $\overline{\text{DSR}}$ pin.
- 0 Input DSR on $\overline{\text{DSR}}$.
- 1 Output RSYN on $\overline{\text{DSR}}$.

RCR 3 **STRSYN —Strip SYN Character (COP only).**
- 0 Do not strip SYN character.
- 1 Strip SYN character.

RCR 2 **2ADCMP —One/Two Address Compare (BOP only).**
- 0 Compare one address byte with the contents of AR1.
- 1 Compare two address bytes with the contents of AR1 and AR2.

RCR 1 **RABTEN —Receiver Abort Enable (BOP only).**
- 0 Do not abort frame upon error detection.
- 1 Abort frame upon RxFIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame.

RCR 0 **RRES —Receiver Reset Command.**
- 0 Enable normal receiver operation.
- 1 Reset receiver. Resets the receiver section including the RxFIFO and the RSR (but not the RCR). RRES is set by $\overline{\text{RESET}}$ or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. RRES requires clearing after $\overline{\text{RESET}}$.

Receiver Data Register (RDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1			LSB		MSB			Byte 0			LSB	

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0			LSB	

The receiver has an 8-byte (or 4-word) First In First Out (FIFO) register file (RxFIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the RxFIFO via the RDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. When the RxFIFO has a data byte/word ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Vector Number Register (RIVNR)

7	6	5	4	3	2	1	0
Receiver Interrupt Vector Number (RIVN)							

Reset value = $0F

If a receiver interrupt condition occurs (as reported by status bits in the RSR that correspond to interrupt enable bits in the RIER) and the corresponding bit is set in the RIER, $\overline{IRQ}$ output is asserted to request MPU receiver interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Receiver Interrupt Vector Number (RIVN) from the Receiver Interrupt Vector Number Register (RIVNR) is placed on the data bus.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0

Reset value = $00

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the $\overline{IRQ}$ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER
7 RDA IE —Receiver Data Available Interrupt Enable.
0 Disable RDA Interrupt.
1 Enable RDA Interrupt.

RIER
6 EOF IE —End of Frame Interrupt Enable.
0 Disable EOF Interrupt.
1 Enable EOF Interrupt.

RIER
5 —Not used.

RIER
4 C/PERR IE —CRC/Parity Error Interrupt Enable.
0 Disable C/PERR Interrupt.
1 Enable C/PERR Interrupt.

RIER
3 FRERR IE —Frame Error Interrupt Enable.
0 Disable FRERR Interrupt.
1 Enable FRERR Interrupt.

RIER
2 ROVRN IE —Receiver Overrun Interrupt Enable.
0 Disable ROVRN Interrupt.
1 Enable ROVRN Interrupt.

RIER
1 RA/B IE —Receiver Abort/Break Interrupt Enable.
0 Disable RA/B Interrupt.
1 Enable RA/B Interrupt.

RIER
0 —Not used.

TRANSMITTER REGISTERS

Transmitter Status Register (TSR)

7	6	5	4	3	2	1	0
TDRA	TFC	0	0	0	TUNRN	TFERR	0

Reset value = $80

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by $\overline{RESET}$. The $\overline{IRQ}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR
7 TDRA —Transmitter Data Register Available.
0 The TxFIFO is full.
1 The TxFIFO is not full (i.e., available) and data to transmit can be loaded via the TDR.

TSR
6 TFC —Transmitted Frame Complete. (BOP, BSC and COP only).
0 Frame not complete.
1 Closing FLAG or ABORT character has been transmitted (BOP), Trailing PAD has been transmitted (BSC), or the last character of a frame or block as defined by TLAST (TCR bit 3) has been transmitted (COP).

TSR
5-3 —Not used.

TSR
2 TUNRN —Transmitter Underrun (BOP, BSC and COP only). A transmitter underrun occurs when the transmitter runs out of data during a transmission. For BOP, the underrun condition is treated as an abort. For BSC and COP, SYN characters are transmitted until more data is available in the TxFIFO.
0 No transmitter underrun occurred.
1 Transmitter underrun occurred.

TSR
1 TFERR —Transmit Frame Error (BOP only).
0 No frame error has occurred.
1 No control field was present (short frame).

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES

Reset value = $01

The Transmitter Control Register (TCR) selects transmitter control function.

TCR
7 TEN —Transmitter Enable.
0 Disable transmitter. TxD output is idled. The TxFIFO may be loaded while the transmitter is disabled.
1 Enable transmitter.

TCR

6 TDSREN —**Transmitter Data Service Request Enable.**

0 Disable transmitter DMA mode.

1 Enable transmitter DMA mode.

TCR

5 TICS —**Transmitter Idle Character Select.** Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).

0 Mark Idle (TxD output is held high).

1 Content of AR2 (BSC and COP), BREAK condition (ASYNC and ISOC), or FLAG character (BOP).

TCR

4 THW —**Transmit Half Word.** (R68561, word mode only). This bit is used when the frame or block ends on an odd boundary in conjunction with the TLAST bit and indicates that the last word in the TxFIFO contains valid data in the upper byte only. This bit must always be 0 in byte mode (R68560).

0 Transmit full word (16 bits) from the TxFIFO.

1 Transmit upper byte (8 bits) from the TxFIFO.

TCR

3 TLAST —**Transmit Last Character** (BOP, BSC and COP only).

0 The next character is not the last character in a frame or block.

1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the TxFIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by $\overline{\text{DONE}}$ from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR

2 TSYN —**Transmit SYN** (BSC and COP only).

0 Do not transmit SYN characters.

1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR

1 TABT —**Transmit ABORT** (BOP only).

0 Enable normal transmitter operation.

1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the TxFIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the TxFIFO.

TCR

0 TRES —**Transmitter Reset Command.**

0 Enable normal transmitter operation.

1 Reset transmitter. Clears the transmitter section including the TxFIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by $\overline{\text{RESET}}$ or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. TRES requires clearing after $\overline{\text{RESET}}$.

Transmit Data Register (TDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1				LSB	MSB			Byte 0				LSB

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0				LSB

The transmitter has an 8-byte (or 4-word) FIFO register file (TxFIFO). Data to be transmitted is transferred from the bus into the TxFIFO via the TDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. The TDRA status bit in the TSR is set to 1 when the TxFIFO is ready to accept another data word/byte.

Transmitter Interrupt Vector Number Register (TIVNR)

7	6	5	4	3	2	1	0
Transmitter Interrupt Vector Number (TIVN)							

Reset value = $0F

If a transmitter interrupt condition occurs (as reported by status bits in the TSR that correspond to interrupt enable bits in the TIER) and the corresponding bit in the TIER is set, the $\overline{\text{IRQ}}$ output is asserted to request MPU transmitter interrupt service. When the $\overline{\text{IACK}}$ input is asserted from the bus, the Transmitter Interrupt Vector Number (TIVN) from the Transmitter Interrupt Vector Number Register (TIVNR) is placed on the data bus.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	—

Reset value = $00

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the $\overline{\text{IRQ}}$ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER

7 TDRA IE —**Transmitter Data Register (TDR) Available Interrupt Enable.**

0 Disable TDRA Interrupt.

1 Enable TDRA Interrupt.

TIER

6 TFC IE —Transmit Frame Complete (TFC) Interrupt Enable.

0 Disable TFC Interrupt.
1 Enable TFC Interrupt.

TIER

5-3 —Not used.

TIER

2 TUNRN IE —Transmitter Underrun (TUNRN) Interrupt Enable.

0 Disable TUNRN Interrupt.
1 Enable TUNRN Interrupt.

TIER

1 TFERR IE —Transmit Frame Error (TFERR) Interrupt Enable.

0 Disable TFERR Interrupt.
1 Enable TFERR Interrupt.

TIER

0 —Not used.

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0

Reset value = $00

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTST, DSRT and DCDT) are cleared by writing a 1 into their respective positions, or by $\overline{\text{RESET}}$. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR

7 CTST —Clear to Send Transition Status.

1 $\overline{\text{CTS}}$ has transitioned positive (from active to inactive). (TRES must be zero).
0 $\overline{\text{CTS}}$ has not transitioned positive.

SISR

6 DSRT —Data Set Ready Transition Status.

1 $\overline{\text{DSR}}$ has transitioned negative (from inactive to active).
0 $\overline{\text{DSR}}$ has not transitioned negative.

SISR

5 DCDT —Data Carrier Detect Transition Status.

1 $\overline{\text{DCD}}$ has transitioned positive (from active to inactive).
0 $\overline{\text{DCD}}$ has not transitioned positive.

SISR

4 CTSLVL —Clear to Send Level.

0 $\overline{\text{CTS}}$ input level is negated (high).
1 $\overline{\text{CTS}}$ input level is asserted (low).

SISR

3 DSRLVL —Data Set Ready Level.

0 $\overline{\text{DSR}}$ input level is negated (high).
1 $\overline{\text{DSR}}$ input level is asserted (low).

SISR

2 DCDLVL —Data Carrier Detect Level.

0 $\overline{\text{DCD}}$ input level is negated (high).
1 $\overline{\text{DCD}}$ input level is asserted (low).

SISR

1-0 —Not used.

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	0	0	0	ECHO	TEST	NRZI

Reset value = $00

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR

7 RTSLVL —Request to Send Level.

0 Negate $\overline{\text{RTS}}$ output (high).
1 Assert $\overline{\text{RTS}}$ output (low).

NOTE

In BOP, BSC, or COP, when the RTSLVL bit is cleared in the middle of data transmission, the $\overline{\text{RTS}}$ output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the $\overline{\text{RTS}}$ output is negated when the TxFIFO is empty. If the transmitter is idling when the RTSLVL bit is reset, the $\overline{\text{RTS}}$ output is negated within two bit times.

SICR

6 DTRLVL —Data Terminal Ready Level.

0 Negate $\overline{\text{DTR}}$ output (high).
1 Assert $\overline{\text{DTR}}$ output (low).

SICR

5-3 —Not used. These bits are initialized to 0 by $\overline{\text{RESET}}$ and must not be set to 1.

SICR

2 ECHO —Echo Mode Enable.

0 Disable Echo mode (enable normal operation).
1 Enable Echo mode. Received data (RxD) is routed back through the transmitter to TxD. The contents of the TxFIFO is undisturbed. This mode may be used for remote test purposes.

SICR

1 TEST —Self-test Enable.

0 Disable self-test (enable normal operation).
1 Enable self-test. The transmitted data (TxD) and clock (TxC) are routed back through to the receiver through RxD and RxC, respectively ($\overline{\text{DCD}}$ and $\overline{\text{CTS}}$ are ignored). This "loopback" self-test may be used for all protocols. RxC is external regardless of the state of CCR bit 2. CCR bit 3 may be a 0 or a 1.

SICR

0 NRZI —**NRZI Data Format Select.** Selects the transmit and receive data format to be NRZ or NRZI.

0 Select NRZ data format. NRZ coding—high = 1 and low = 0.

1 Select NRZI data format. The serial data remains in the same state to send a binary 1 and switches to the opposite state to send a binary 0. A 1 bit delay is added to the TxD output to allow for encoding.

Serial Interrupt Vector Number Register (SIVNR)

7	6	5	4	3	2	1	0
Serial Interrupt Vector Number (SIVN)							

Reset value = $0F

If a serial interface interrupt condition occurs (as reported by status bits in the SISR that correspond to interrupt enable bits in the SIER) and the corresponding bit in the SIER is set, the $\overline{IRQ}$ output is asserted to request MPU serial interface interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Serial Interrupt Vector Number (SIVN) from the Serial Interrupt Vector Number Register (SIVNR) is placed on the data bus.

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	0	0	0	0	0

Reset value = $00

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the $\overline{IRQ}$ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER

7 **CTS IE —Clear to Send (CTS) Interrupt Enable.**

0 Disable CTS Interrupt.

1 Enable CTS Interrupt.

SIER

6 **DSR IE —Data Set Ready (DSR) Interrupt Enable.**

0 Disable DSR Interrupt.

1 Enable DSR Interrupt.

SIER

5 **DCD IE —Data Carrier Detect (DCD) Interrupt Enable.**

0 Disable DCD Interrupt.

1 Enable DCD Interrupt.

SIER

4-0 **—Not used.**

GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES in the TCR and RRES in the RCR should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTLEX	ADDEX

Reset value = $00

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1

7-2 **—Not used.**

PSR1

1 **CTLEX —Control Field Extend (BOP only).**

0 Select 8-bit control field.

1 Select 16-bit control field.

PSR1

0 **ADDEX —Address Extend (BOP only).**

0 Disable address extension. All eight bits of the address byte are utilized for addressing.

1 Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL		
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Reset value = $00

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2

7 **WD/BYT —Data Bus Word/Byte Mode.**

0 Select byte mode. Selects the number of data bits to be transferred from the RxFIFO and the registers to the data bus and to be transferred from the data bus to the TxFIFO and the registers. The MPCC is initialized by $\overline{RESET}$ to the byte mode.

1 Select word mode. For operation with the 16-bit bus, select the word mode by sending $80 on D7 – D0 to address $19 prior to transferring subsequent data between the MPCC and the data bus.

PSR2

6-5 **STOP BIT SEL —Number of Stop Bits Select.** Selects the number of stop bits transmitted at the end of the data bins in ASYNC and ISOC modes.

6 SB2	5 SB1	No. of Stop Bits ASYNC	No. of Stop Bits ISOC
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2

4-3 CHAR LEN SEL —**Character Length Select.** Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.

4 CL2	3 CL1	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2

2-0 PROTOCOL SEL —**Protocol Select.** Selects protocol and defines the protocol dependent control bits.

2 PS3	1 PS2	0 PS1	Protocol
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYNC
1	1	1	ISOC

Address Register 1 (AR1)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Reset value = $00

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP SYN							

Reset value = $00

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of the address registers are used for address matching depending on the 2 ADCMP selection in the RCR. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	2ADCMP	AR1	AR2
BOP (Primary)	X	X	X
BOP (Secondary)	0	Address	X
	1	Address	Address
BSC EBCDIC	X	Leading PAD	SYN
BSC ASCII	X	Leading PAD	SYN
COP	X	Leading PAD	SYN
*X = Not used			

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Reset value = $01

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

Reset value = $00

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH). With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{(\text{Prescaler Divider})\ (\text{Baud Rate})\ (K)}$$

where: K = 1 for isochronous or synchronous
2 for asynchronous

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
0	0	0	PSCDIV	TCLKO	RCLKIN	CLK SEL	
						CK2	CK1

Reset value = $00

The CCR selects various clock options.

CCR
7-5 —**Not used.**

CCR
4 **PSCDIV** —**Prescaler Divider.** The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.

0 Divide by 2.
1 Divide by 3.

CCR
3 **TCLKO** —**Transmitter Clock Output Select.**
0 Select TxC to be an input.
1 Select TxC to be an output.

Table 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bit Rate)	Prescaler Divider		Baud Rate Divider					
			Asynchronous			Isochronous and Synchronous		
				Hexadecimal Value			Hexadecimal Value	
	Decimal Value	PSCDIV (0 to 1)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	8C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

CCR

2 **RCLKIN** —**Receiver Clock Internal Select** (ASYNC only).

0 Select External RxC.

1 Select Internal RxC.

CCR

1-0 **CLK DIV** —**External Receiver Clock Divider.** Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider
0	0	1 (ISOC)
0	1	16
1	0	32
1	1	64

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CRCCTL	CRCPRE	CRCSEL	
						CR2	CR1

Reset value = $04

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR

7 **PAREN** —**Parity Enable.** (ASYNC, ISOC and COP only).

0 Disable parity generation/checking.

1 Enable parity generation/checking.

ECR

6 **ODDPAR** —**Odd/Even Parity Select** (Effective only when PAREN = 1).

0 Generate/check even parity.

1 Generate/check odd parity.

ECR

5-4 —**Not used.**

ECR

3 **CFCRC** —**Control Field CRC Enable.**

0 Disable control field CRC. Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR

2 **CRCPRE** —**CRC Generator Preset Select.**

0 Preset CRC Generator to 0.

1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder.

ECR

1-0 **CRCSEL** —**CRC Polynomial Select.** Selects one of the RC polynominals.

1 CR2	0 CR1	Polynominal
0	0	$x^{16} + x^{12} + x^5 + 1$ (CCITT V.41)
0	1	$x^{16} + x^{15} + x^2 + 1$ (CRC-16)
1	0	$x^8 + 1$ (VRC/LRC)*
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals:

	R68561	R68560
Address Lines	A1–A4	A0–A4
Data Lines	D0--D15	D0–D7
Read/Write	R/$\overline{W}$	R/$\overline{W}$
Data Transfer Acknowledge	$\overline{DTACK}$	$\overline{DTACK}$
Chip Select	$\overline{CS}$	$\overline{CS}$
Data Strobes	$\overline{UDS}$ and $\overline{LDS}$	$\overline{DS}$

Figures 10 and 11 show typical interface connections.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the MPCC for access to the internal registers and other operations. When $\overline{CS}$ is asserted, the data I/O buffer acts as an output driver during a read operation and as an input buffer during a write operation. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

When the R68561 is connected to the 16-bit bus for operation in the word mode (WD/BYT = 1 in the PSR2), address lines A1–A4 select the internal register(s) (the 8-bit control/status registers are accesed two at a time and the 16-bit data registers are accessed on even address boundaries). When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), 16 bits of register data are placed on the data bus when the data strobes ($\overline{LDS}$ and $\overline{UDS}$) are asserted. $\overline{LDS}$ strobes the eight data bits from the even numbered registers to the lower data bus lines (D0–D7) and $\overline{UDS}$ strobes the eight data bits from the odd numbered registers to the upper data bus lines (D8–D15). The MPCC asserts Data Transfer Acknowledge ($\overline{DTACK}$ prior to placing data on the data bus. Conversely, when the MPCC is selected ($\overline{CS}$ low) during a write (R/$\overline{W}$ low) $\overline{LDS}$ and $\overline{UDS}$ strobe data from the D0 – D7 and D8–D15 data bus lines into the addressed even and odd numbered registers, respectively, and the MPCC asserts $\overline{DTACK}$. $\overline{DTACK}$ is negated when $\overline{CS}$ is negated. Figures 12 and 13 show the read and write timing relationships.

When the R68560 is connected to the 8-bit bus for operation in the byte mode (WD/BYT = 0 in the PSR2), address lines A0–A4 select one internal 8-bit register. When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), eight bits of register data are placed on data bus lines D0–D7 when the data strobe ($\overline{DS}$) is asserted. When the MPCC is selected ($\overline{CS}$ low) for a write (R/$\overline{W}$ low), $\overline{DS}$ strobes data from the D0–D7 data lines into the selected register.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers up to 2 Mbytes per second when used with the MC68440 or MC68450 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which requires a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input ($\overline{DACK}$) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/$\overline{W}$ input to distinguish between the Transmitter Data Service Request ($\overline{TDSR}$ acknowledge and the Receiver Data Service Request ($\overline{RDSR}$) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the RxFIFO, Receiver Data Service Request ($\overline{RDSR}$) is asserted for one receiver clock period to initiate the MPCC to memory DMA transfer. The next $\overline{RDSR}$ cycle may be initiated as soon as the current $\overline{RDSR}$ cycle is completed (i.e., a full sequence of $\overline{DACK}$, $\overline{DS}$, and $\overline{DTC}$).

In response to $\overline{RDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to write, asserts the memory address, address strobe, and DMA acknowledge. The MPCC outputs data from the RxFIFO to the data bus and the DMAC asserts the data strobes. The memory latches the data and asserts $\overline{DTACK}$ to complete the data transfer. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data transfer is complete. Figure 13 shows the timing relationships for the receiver DMA mode.

$\overline{RDSR}$ is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when $\overline{RESET}$ is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the TxFIFO is available, Transmitter Data Service Request ($\overline{TDSR}$) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. The next $\overline{TDSR}$ cycle may be initiated as soon as the current $\overline{TDSR}$ cycle is completed.

In the transmitter DMA mode, the TxFIFO is implicitly addressed. That is, when the transfer is from memory to the TxFIFO, only the memory is addressed. In response to $\overline{TDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to read, asserts the memory address, the address strobe, the data strobes and DMA acknowledge. The memory places data on the data bus and asserts $\overline{DTACK}$. Data is valid at this time and will remain valid until the data strobes are negated. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data is available. The MPCC loads the data into the TxFIFO on the negation (rising edge) of $\overline{DS}$ and the transfer is complete. A timing diagram for the transmitter DMA Mode is shown in Figure 15.

$\overline{TDSR}$ is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when $\overline{RESET}$ is asserted.

$\overline{DONE}$ Signal

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts $\overline{DONE}$ which sets the TLAST bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode, $\overline{DONE}$ is asserted by the MPCC when the last character of the frame/block is being transferred from the RxFIFO to the data bus if the DONEEN bit is set to a 1 in the RCR.

INTERRUPTS

If an interrupt generating status occurs and the interrupt is enabled, the MPCC asserts the $\overline{IRQ}$ output. Upon receiving $\overline{IACK}$ for the pending interrupt request, the MPCC places an interrupt vector on D0–D7 data bus and asserts $\overline{DTACK}$.

The MPCC has three vector registers: Receiver Interrupt Vector Number Register (RIVNR), Transmitter Interrupt Vector Number Register (TIVNR), and Serial Interrupt Vector Number Register (SIVNR). The receiver interrupt has higher priority over the transmitter interrupt, and the transmitter interrupt has priority over the serial interface interrupt. For example, if a pending interrupt request has been generated simultaneously by the receiver and the transmitter, the Receiver Interrupt Vector Number (RIVN) is placed on D0–D7 when acknowledged by the MPU. Upon completion of the first interrupt request cycle (which clears the receiver interrupt), $\overline{IRQ}$ will remain low to start the transmitter interrupt cycle. $\overline{IRQ}$ is negated by clearing all bits set in a status register that could have caused the interrupt.

A timing diagram for the interrupt acknowledge sequence is shown in Figure 15.

SERIAL INTERFACE

The MPCC is a high speed, high performance device supporting the more popular bit and character oriented data protocols. The lower speed asynchronous (ASYNC) and isochronous (ISOCH) modes are also supported. An on-chip clock oscillator and baud rate generator provide an output data clock at a frequency of DC to 4 MHz. The clock can also be used in the ASYNC mode to provide a receive clock for the incoming data. The serial interface consists of the following signals:

$\overline{RTS}$ (Request to Send) Output

The $\overline{RTS}$ output to the DCE is controlled by the RTSLVL bit in the SICR in conjunction with the state of the transmitter section. When the RTSLVL bit is set to 1, the $\overline{RTS}$ output is asserted. When the RTSLVL bit is reset to 0, the $\overline{RTS}$ output remains asserted until the TxFIFO becomes empty or the end of the message (or frame), complete with CRC code if any, has been transmitted. $\overline{RTS}$ also is negated when the RTSLVL bit is reset during transmitter idle, or when the $\overline{RESET}$ input is asserted.

$\overline{CTS}$ (Clear to Send) Input

The $\overline{CTS}$ input signal is normally generated by the DCE to indicate whether or not the data set is ready to transmit data. The CTST bit in the SISR reflects the transition status of the $\overline{CTS}$ input while the CTSLVL bit in the SISR reflects the current level. A positive transition on the $\overline{CTS}$ pin asserts $\overline{IRQ}$ if the CTS IE bit in the SIER is set. The $\overline{CTS}$ input in an inactive state disables the start of transmission.

$\overline{DCD}$ (Data Carrier Detect) Input

The $\overline{DCD}$ input signal is normally generated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The DCDT bit in the SISR reports the transition status of the $\overline{DCD}$ input while the DCDLVL bit in the SISR contains the current level. A positive transition on the $\overline{DCD}$ pin asserts the $\overline{IRQ}$ output if the DCD IE bit in the SIER is set. A negated $\overline{DCD}$ input disables the start of the receiver.

$\overline{DSR}$ (Data Set Ready) Input/RSYN Output

The DSRT input from the DCE indicates the status of the local set. The DSRT bit in the SISR contains the transition status of the $\overline{DSR}$ input while the DSRLVL bit in the SISR reports the current level. A negative transition on the $\overline{DSR}$ pin asserts the $\overline{IRQ}$ output if the DSR IE bit in the SIER is set.

When the RSYN bit in the RCR is set to 1, the frame synchronization signal (RSYN) in the receiver is output on the $\overline{DSR}$ pin. In this mode, $\overline{DSR}$ output low indicates detection of SYN in BSC or COP, or an address match in BOP

$\overline{DTR}$ (Data Terminal Ready) Output

The $\overline{DTR}$ output is general purpose in nature and can be used to control switching of the DCE. The $\overline{DTR}$ output is controlled by the DTRLVL bit in the SICR.

TxC (Transmitter Clock) Input/Output

The transmitter clock (TxC) may be programmed to be input or an output. When the TCLKO control bit in the CCR is set to a 1, the TxC pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the TCLKO control bit is reset, TxC is an input and the transmitter shift timing must be provided externally. The TxD output changes state on the negative-going edge of the transmitter clock. In the asynchronous mode when TCLKO = 0 in the CCR, the TxC input frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in NRZ or NRZI (zero complement) data format as selected by the NRZI control bit in the SICR.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the RxC.

RxD (Received Data) Input

The serial data received by the MPCC can be coded in NRZ or NRZI data format. The MPCC will decode the received data in accordance with the NRZI control bit setting in the SICR.

Serial Interface Timing

The timing for the serial interface clock and data lines is shown in Figure 18. The MPCC supports high speed synchronous operation. As shown, the TxD output changes with the negative-going edge of TxC and the received data on RxD is latched on the negative edge of RxC. This assures high speed two-way operation between two MPCCs connected as shown in Figure 17.

For low speed operation between the MPCC and a modem or RS-232C Data Communications Equipment (DCE), an inverter can be used in the TxC output lines as shown in Figure 17. RS-232 and RS-423 (covering serial data interface up to 100K baud) require that data be centered ±25% about the negative-going edge of the RxC. This criteria is met for frequencies up to 1.25 MHz using the inverter. Use of the inverter also allows MPCC to MPCC operation up to 2.17 MHz.

SERIAL COMMUNICATION MODES AND PROTOCOLS

ASYNCHRONOUS AND ISOCHRONOUS MODES

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (LSB) first. The data line is normally held high (MARK) between frames, however, a BREAK (minimum of one frame length for which the line is held low) is used for control purposes. Figure 4 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (ASYNC) mode, data received on RxD occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on RxC. When RCLKIN in the CCR is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchronization. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the RxFIFO and set appropriate status bits in the RSR when the character with an error reaches the last RxFIFO register where it is ready to be transferred onto the data bus via the RDR.

Isochronous Receive

In the isochronous (ISOC) mode, a 1 times clock on RxC is required with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data tansmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character.

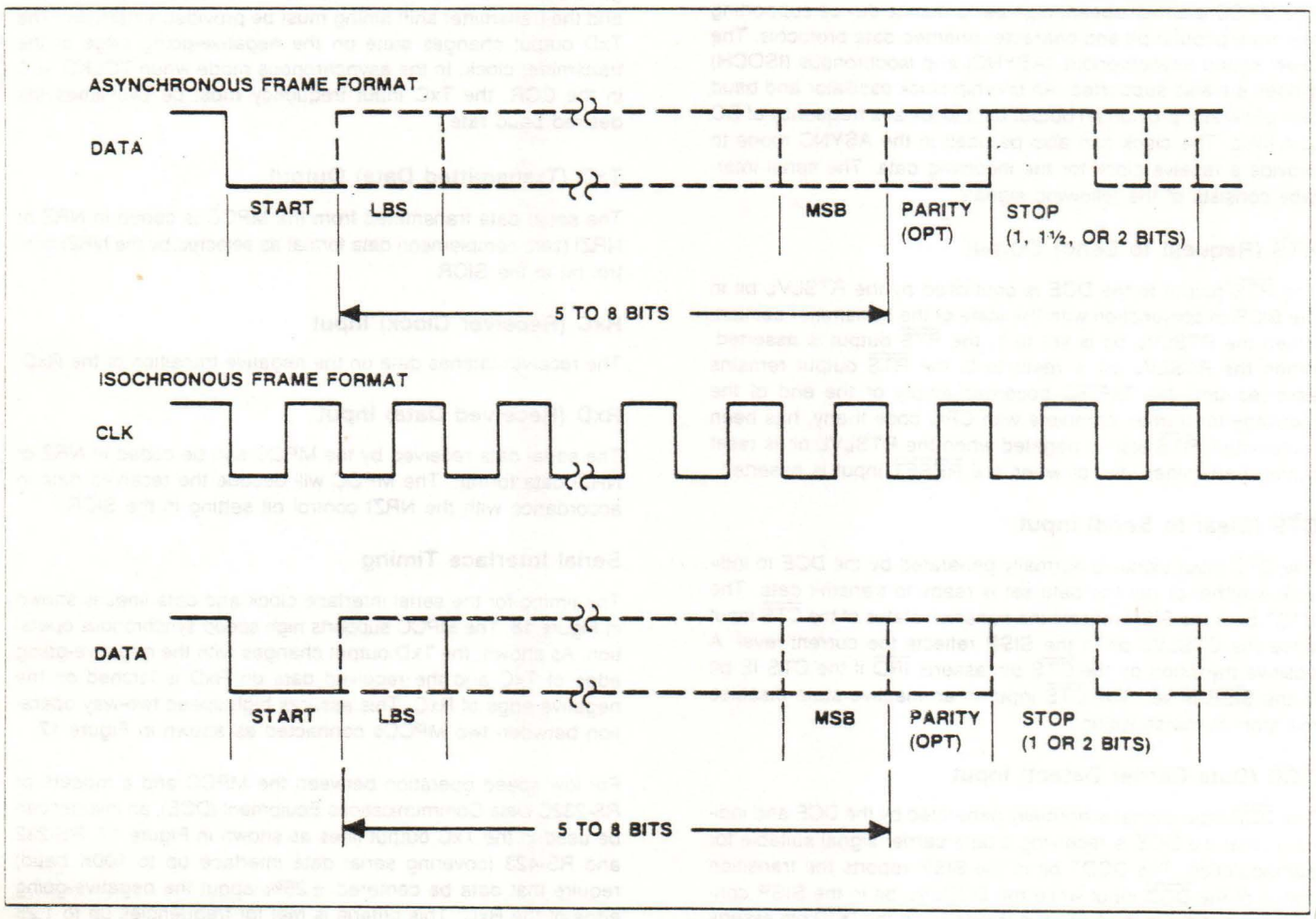


Figure 4. Asynchronous and Isochronous Frame Format

SYNCHRONOUS MODES

In synchronous modes, a one-times clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 5).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. Up to two bytes of the address field may be automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made. The control field of one or two bytes is transparent to the MPCC and sent directly to the host without interpretation.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1s, and the 1s complement of the resulting remainder is transmitted. (See X.25 Recommendation.)

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

The end of the frame is determined by the detection of the closing Flag special character which is the same is the opening Flag.

With the control options offered by the MPCC, commonly used bit oriented protocols such as SDLC, HDLC and X.25 standards can be supported. Figure 6 compares the requirements of these options.

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a Flag. The receiver also continues to search for additional Flag, or Abort, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the Flag detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "01111101111110."

Character assembly and CRC accumulation are stopped when a closing Flag or Abort is detected. The CRC accumulation includes all the characters between the opening Flag and the closing Flag. The contents of the CRC register are checked at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the Flag are not passed on to the RxFIFO.

If the Flag is a closing flag, checks for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an Abort (seven 1s) is detected, the remaining frame is discarded and the RA/B bit is set in the RSR. When a link idle (15 or more consecutive 1s) is detected, the RIDLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of up to two bytes. If there is no address match, the receiver (secondary station) ignores the remainder of the frame by searching for the Flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110

Figure 5. Bit Oriented Protocol (BOP) Frame Format

IBM SDLS FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

ADCCP/HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

Figure 6. Implemented Bit Oriented Protocols

For the control field, one or two bytes are assembled and passed on to the RxFIFO depending on the state of the extended control field bit.

If the CFCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the TxFIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading Flag is automatically sent prior to transmitting data from the TxFIFO. The TDRA bit is set to 1 in the TSR as long as TxFIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an Abort (11111111) is transmitted followed by continuous Flags or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the $\overline{\text{DONE}}$ signal from the DMAC.

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an Abort character followed by the remainder of the current frame data in the TxFIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1s, and a 0 is inserted in the data stream each time this condition occurs (excluding Flag and Abort characters).

CRC accumulation begins with the first non-Flag character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTLCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control field. The final Frame Check Sequence is calculated over the balance of the frame.

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 7. The MPCC can process both transparent and nontransparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 4.

Table 4. BSC Control Sequences—Inclusion in CRC Accumulation

ASCII			EBCDIC		
Command	**Byte 1**	**Byte 2**	**Command**	**Byte 1**	**Byte 2**
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

Note: *Programmable

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

LEADING PAD 1 BYTE (AR1)	SYN 1 BYTE (AR2)	SYN 1 BYTE (AR2)	BODY	BCC	TRAILING PAD 11111111

Figure 7. BSC Block Format

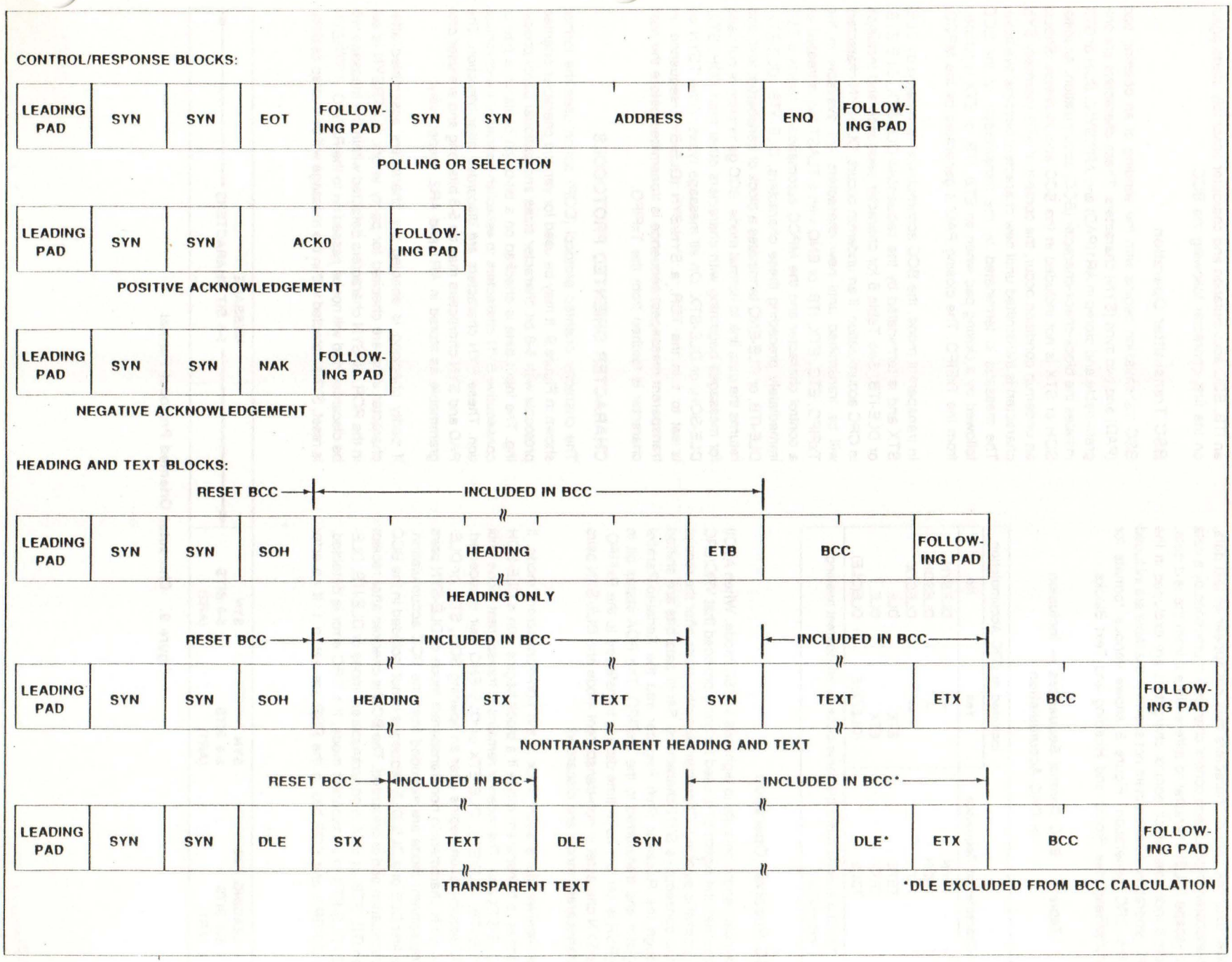


Figure 8. BSC Message Format Examples

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 5 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 8 shows various formats for Control/Response Blocks and Heading and Text Blocks.

Table 5. BSC Control Sequences — Inclusion in CRC Accumulation

Character of Sequence	Included in CRC Accumulation	
	Yes	No
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

*If not preceded within the same block by transparent heading information.

BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided that VRC/LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the RxFIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the RxFIFO. The SYN character in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation and is discarded. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available. The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the TxFIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 5 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the TxFIFO, ETC, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters, DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the TxFIFO.

CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 9. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the RxFIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.

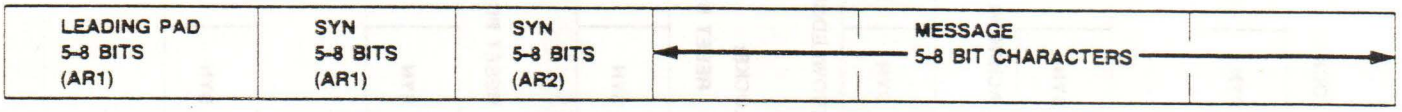
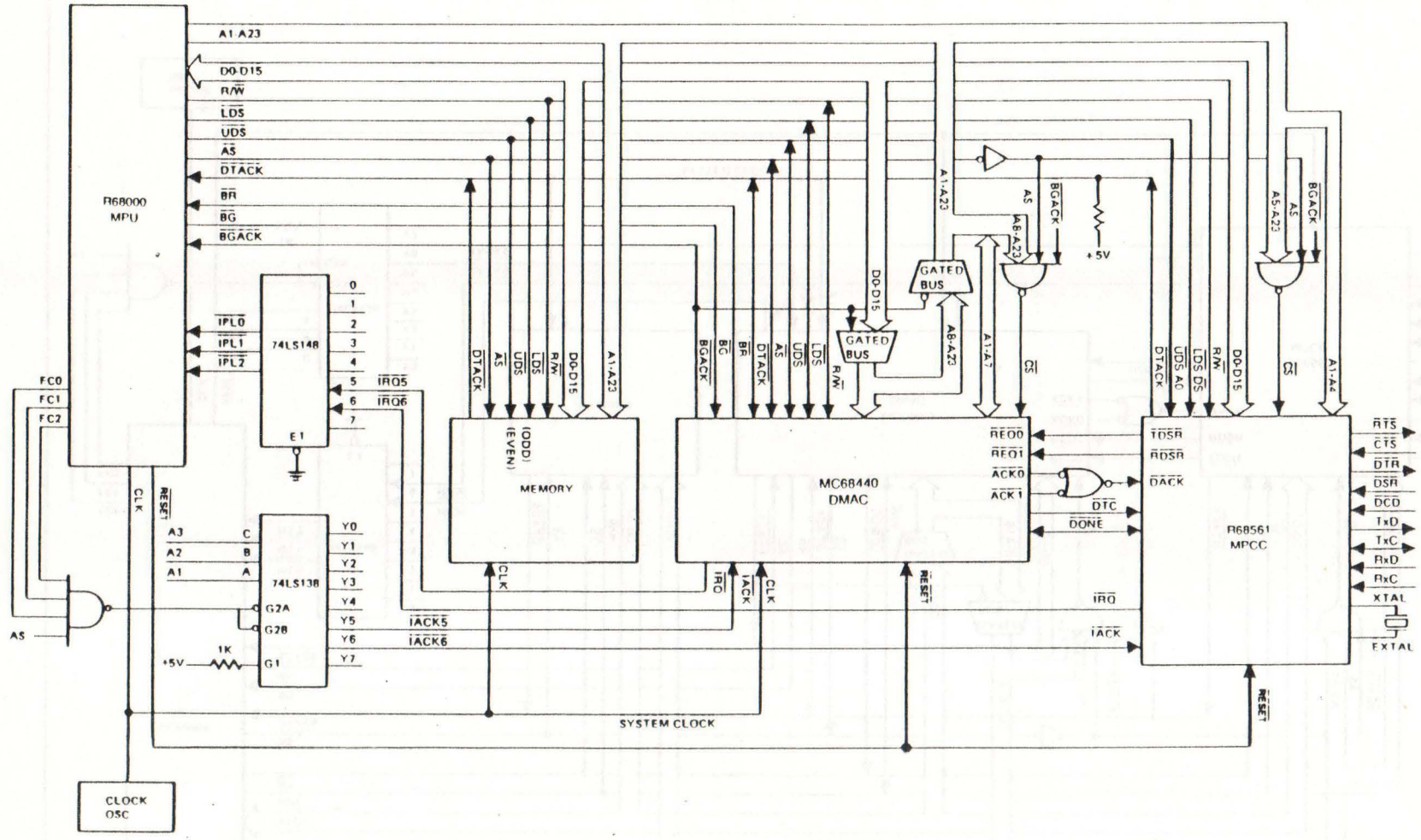


Figure 9. Character Oriented Protocol Format



NOTE: $\overline{UDS}$ MAY BE TIED LOW (GROUND).

Figure 10. Typical Interface to 68000-Based System

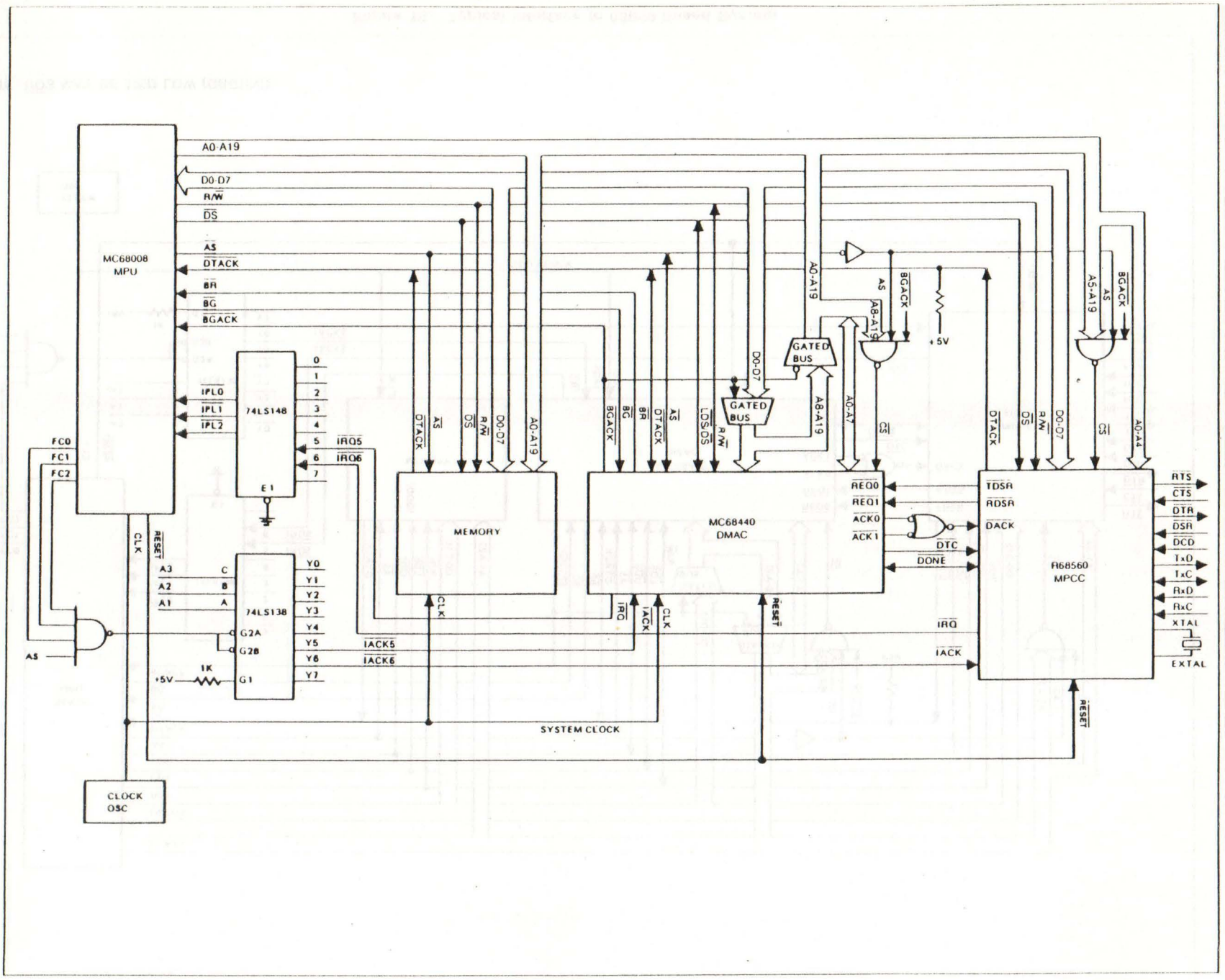
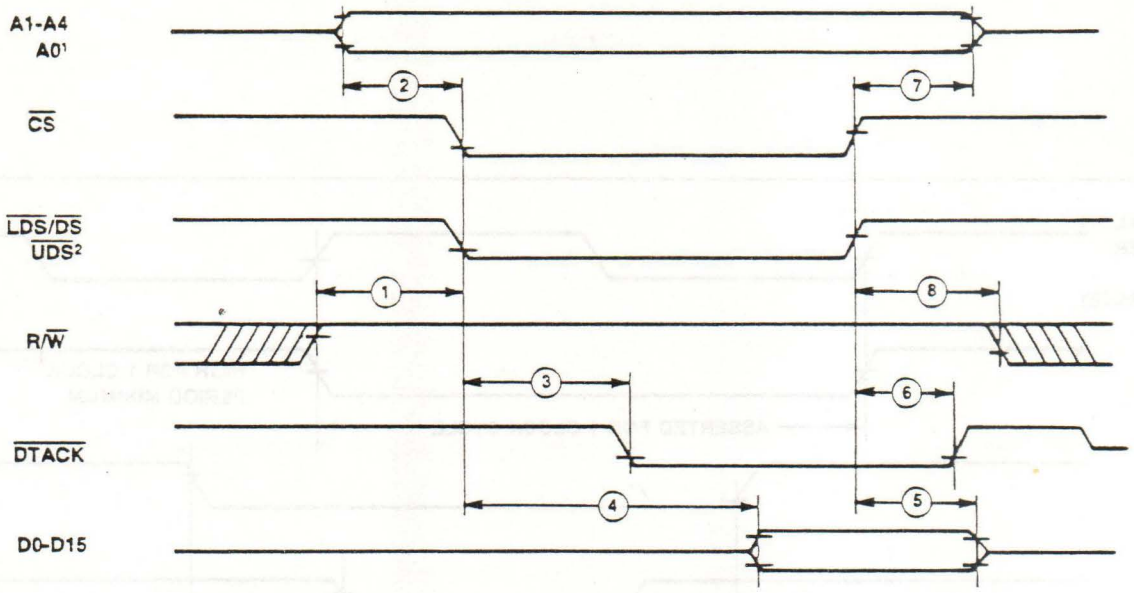
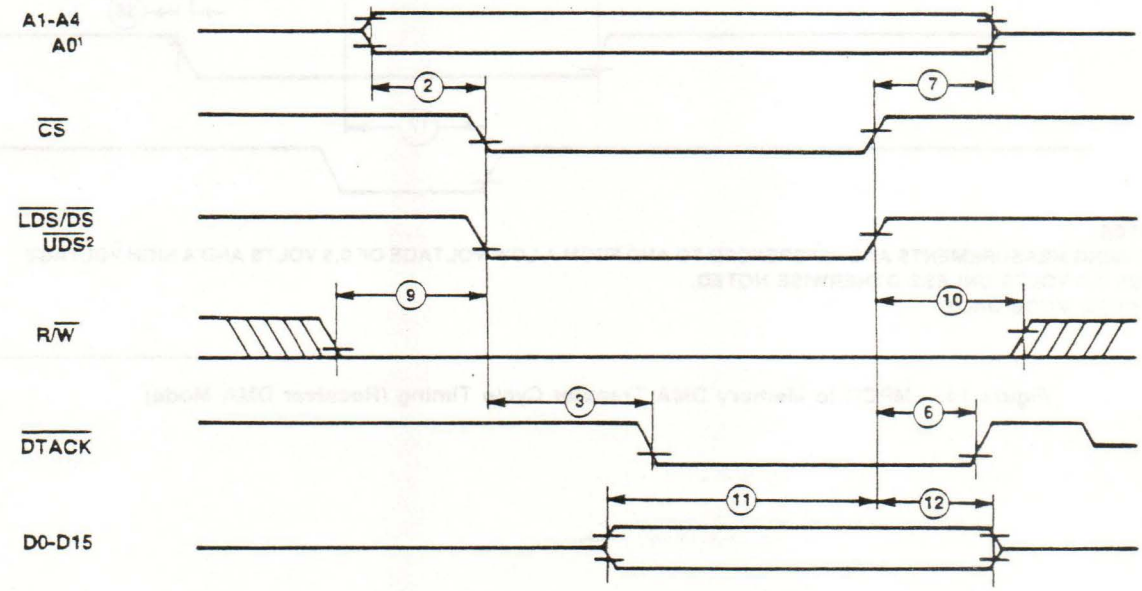


Figure 11. Typical Interface to 68008-Based System



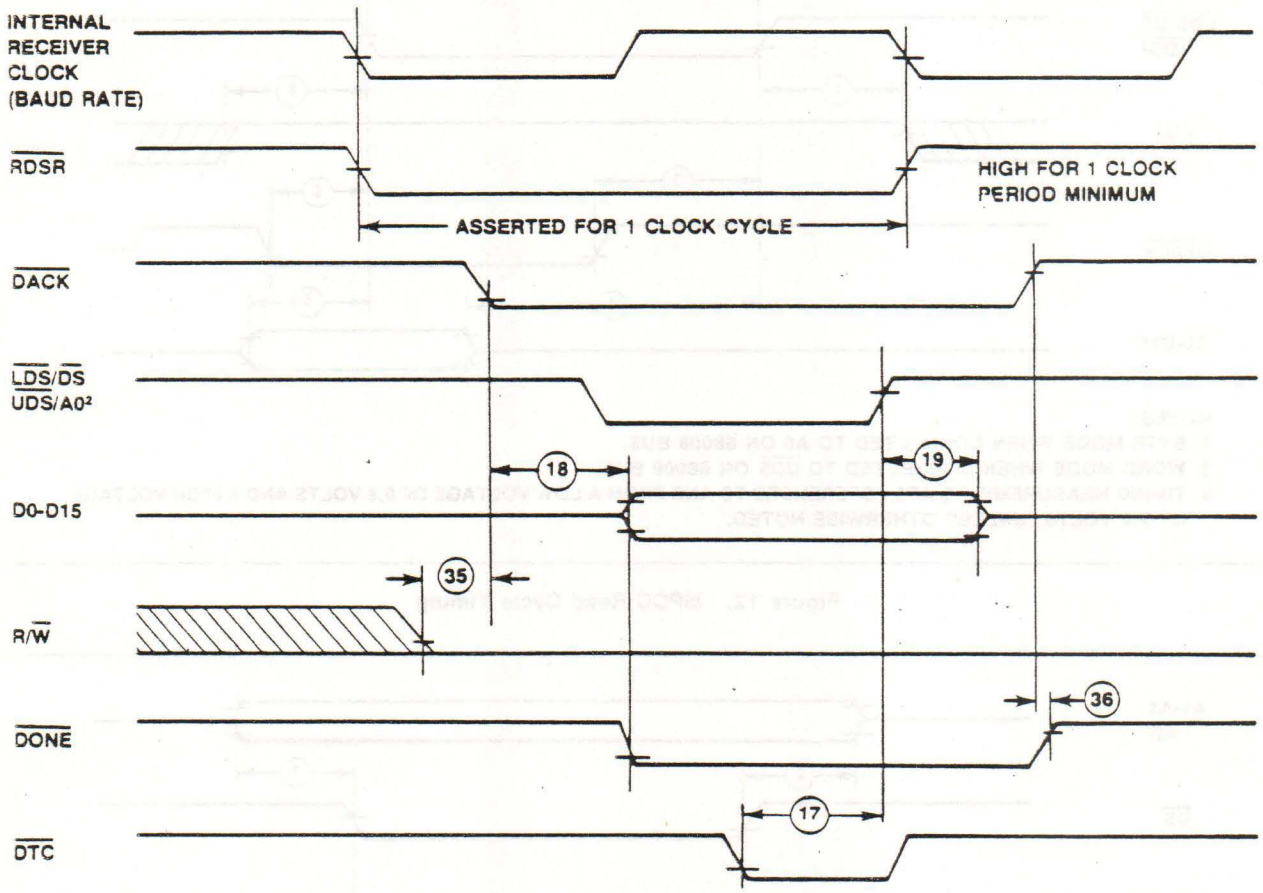
NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO UDS ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 12. MPCC Read Cycle Timing



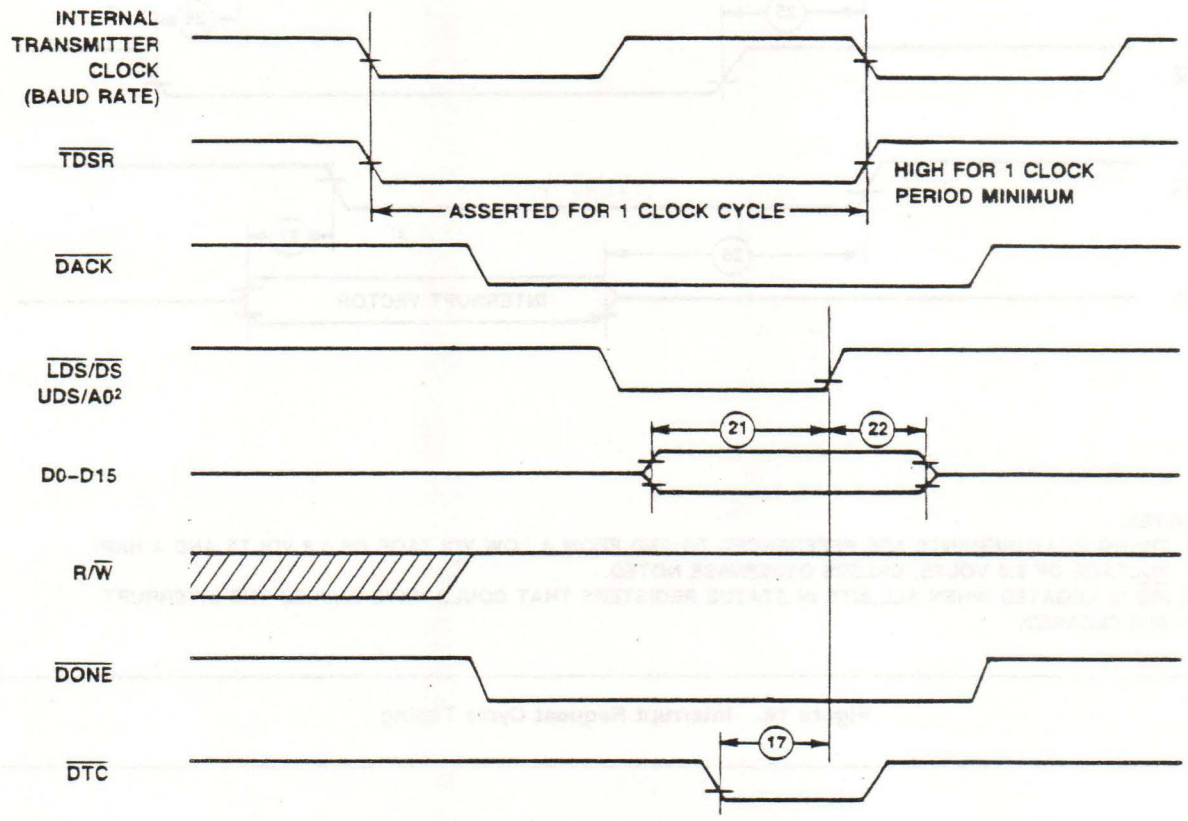
NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO UDS ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 13. MPCC Write Cycle Timing



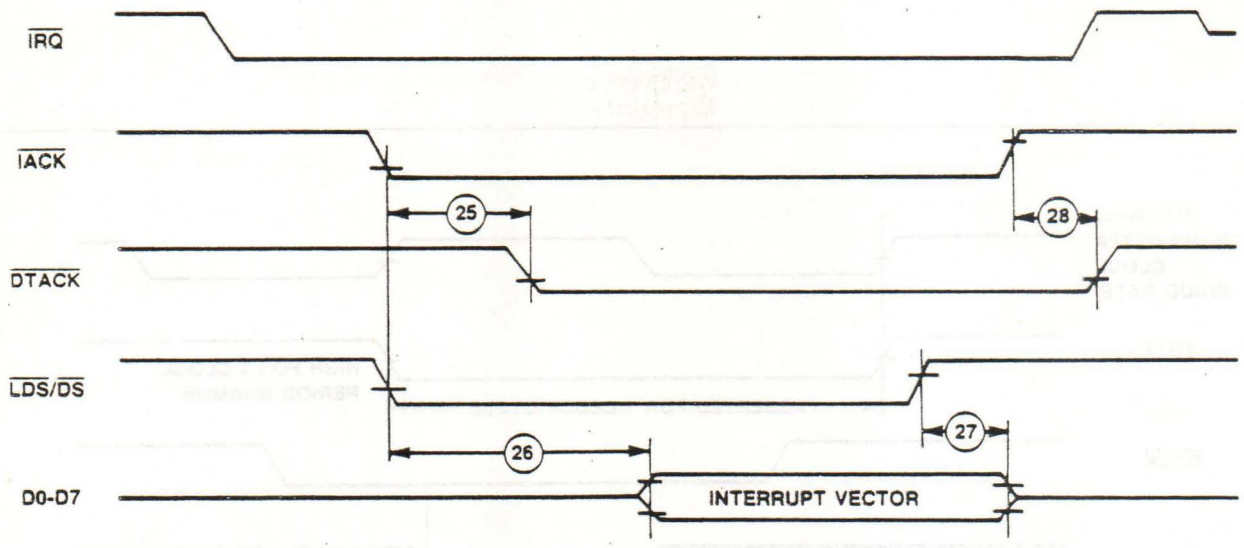
NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.

Figure 14. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.

Figure 15. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. IRQ IS NEGATED WHEN ALL BITS IN STATUS REGISTERS THAT COULD HAVE CAUSED THE INTERRUPT ARE CLEARED.

Figure 16. Interrupt Request Cycle Timing

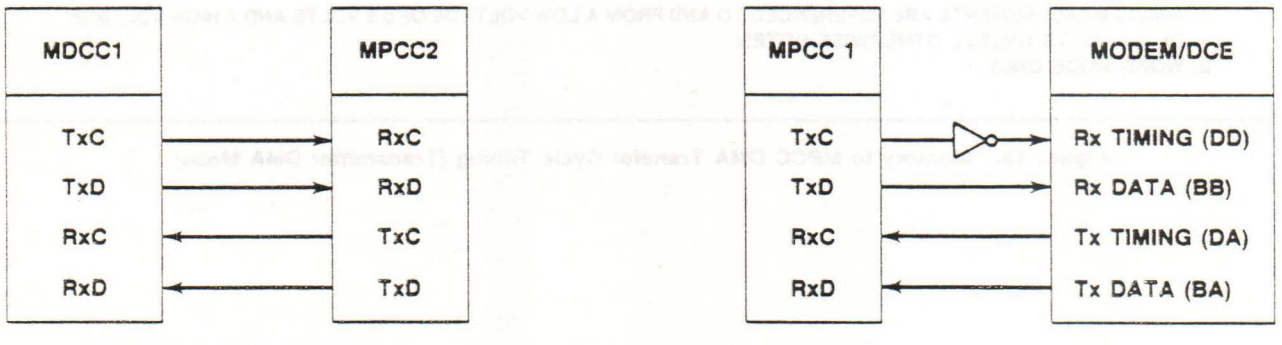


Figure 17. Serial Interface

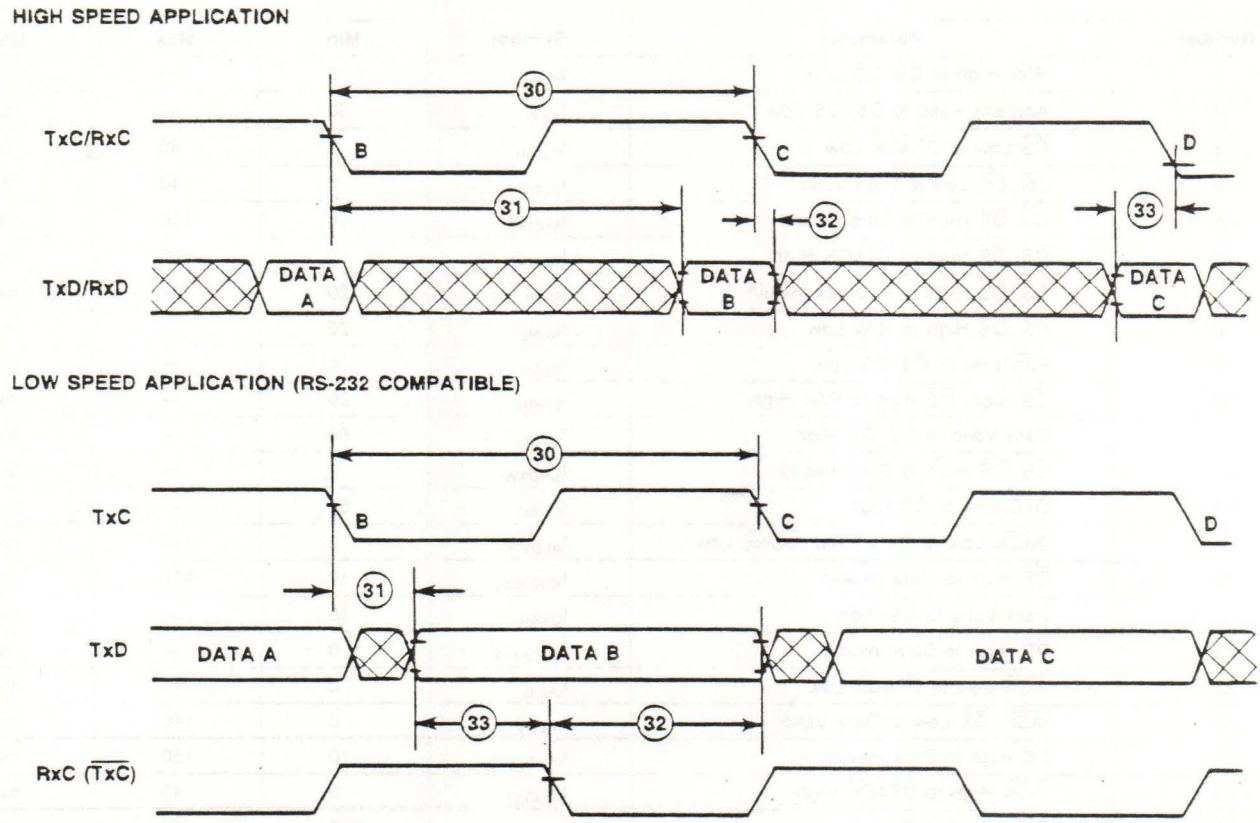
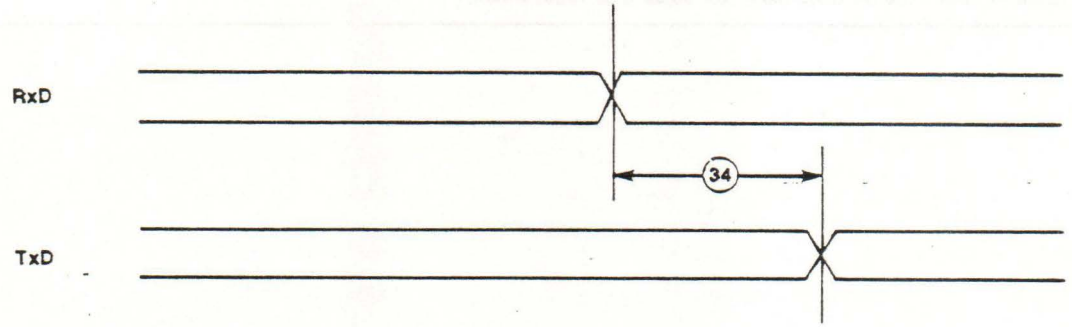


Figure 18. Serial Interface Timing



NOTE:
TIMING MEASUREMENTSS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 19. Serial Interface Echo Mode Timing

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Number	Parameter	Symbol	Min	Max	Unit
1	R/$\overline{W}$ High to $\overline{CS}$, $\overline{DS}$ Low	t_{RHSL}	0	—	ns
2	Address Valid to CS, $\overline{DS}$ Low	t_{AVSL}	30	—	ns
3[1]	$\overline{CS}$ Low to $\overline{DTACK}$ Low	t_{CLDAL}	0	60	ns
4[1]	$\overline{CS}$, $\overline{DS}$ Low to Data Valid	t_{SLDV}	0	140	ns
5	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDXR}	10	150	ns
6	$\overline{CS}$, $\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAT}	0	40	ns
7	$\overline{CS}$, $\overline{DS}$ High to Address Invalid	t_{SHAI}	20	—	ns
8	$\overline{CS}$, $\overline{DS}$ High to R/$\overline{W}$ Low	t_{SHRL}	20	—	ns
9	R/$\overline{W}$ Low to $\overline{CS}$, $\overline{DS}$ Low	t_{RLSL}	0	—	ns
10	$\overline{CS}$ High, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	20	—	ns
11	Data Valid to $\overline{CS}$, $\overline{DS}$ High	t_{DVSH}	60	—	ns
12	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDXW}	0	—	ns
17	$\overline{DTC}$ Low to $\overline{DS}$ High	t_{CLSH}	60	—	ns
18	$\overline{DACK}$ Low to Data Valid, $\overline{DONE}$ Low	t_{ALDV}	0	140	ns
19	$\overline{DS}$ High to Data Invalid	t_{SHDXDR}	10	150	ns
21	Data Valid to $\overline{DS}$ High	t_{DVSH}	60	—	ns
22	$\overline{DS}$ High to Data Invalid	t_{SHDXDW}	0	—	ns
25	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{IALAL}	0	40	ns
26	$\overline{IACK}$, $\overline{DS}$ Low to Data Valid	t_{IALDV}	0	140	ns
27	$\overline{DS}$ High to Data Invalid	t_{ISHDI}	10	150	ns
28	$\overline{IACK}$ High to $\overline{DTACK}$ High	t_{IAHDAT}	0	40	ns
30	RxC and TxC Period	t_{CP}	248	—	ns
31	TxC Low to TxD Delay	t_{TCLTD}	0	200	ns
32	RxC Low to RxD Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to RxC Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to TxD Delay (Echo Mode)	t_{RDTD}	—	200	ns
35	R/$\overline{W}$ Low to $\overline{DTACK}$ Low (Setup)	t_{RLAL}	0	—	ns
36	$\overline{DACK}$ High to $\overline{DONE}$ High	t_{AHDH}	0	—	ns

Note:

1. For read cycle timing, the MPCC asserts $\overline{DTACK}$ within the MPU S4 clock low setup time requirement and establishes valid data (Data In) within the MPU S6 clock low setup time requirement.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		68	

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V ±5%
Operating Temperature	0°C to 70°C

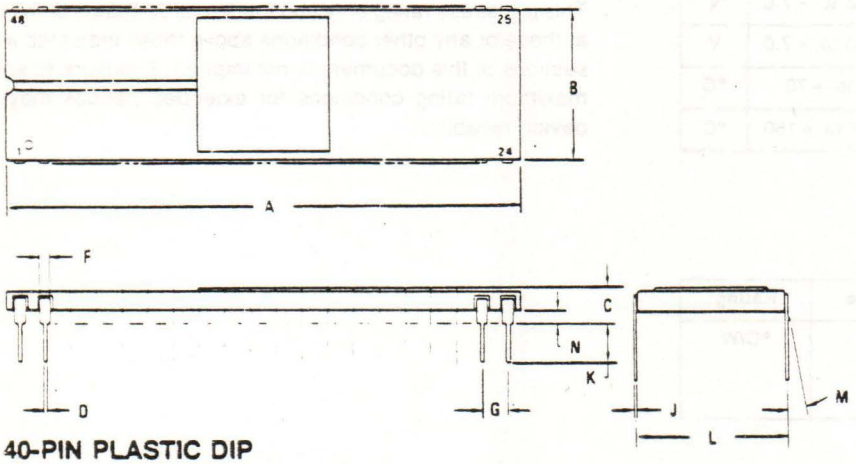
DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage All Inputs	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage All Inputs	V_{IL}	−0.3	+0.8	V	
Input Leakage Current (V_{IN} = 0 to 5.25V) R/$\overline{W}$, $\overline{RESET}$, $\overline{CS}$	I_{IN}	—	10.0	μA	V_{IN} = 0 to 5.25V V_{CC} = 0
Three-State (Off State) Input Current (V_{IN} = 0.4 to 2.4) $\overline{IRQ}$, $\overline{DTACK}$, D0-D15	T_{TSI}	—	10.0	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.0V
Output High Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$, D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = −400μA C_{LOAD} = 130 pF
BCLK	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = 0 C_{LOAD} = 30 pF
Output Low Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$ D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC, BCLK,	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA
$\overline{DONE}$					V_{CC} = 4.75V I_{LOAD} = 8.8 mA
Internal Power Dissipation	P_{INT}	—	1	W	T_A = 25°C
Input Capacitance	C_{IN}	—	13	pF	V_{IN} = 0V T_A = 25°C f = 1 MHz

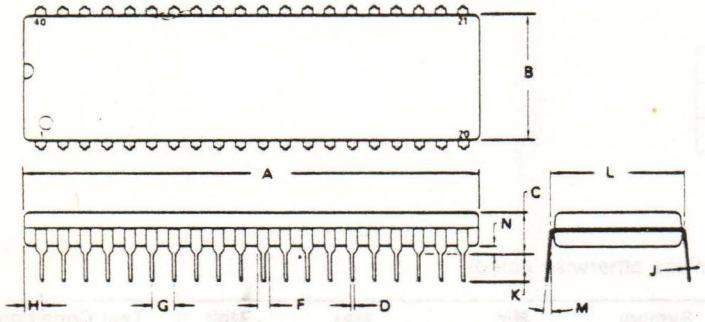
PACKAGE DIMENSIONS

48-PIN CERAMIC DIP



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.606

40-PIN PLASTIC DIP



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

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