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MVME202/D1

MVME202/222-1/222-2
512KB/1MB/2MB
Dynamic Memory Module
User's Manual

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MVME202/222-1/222-2

512KB/1MB/2MB DYNAMIC MEMORY MODULE

USER'S MANUAL

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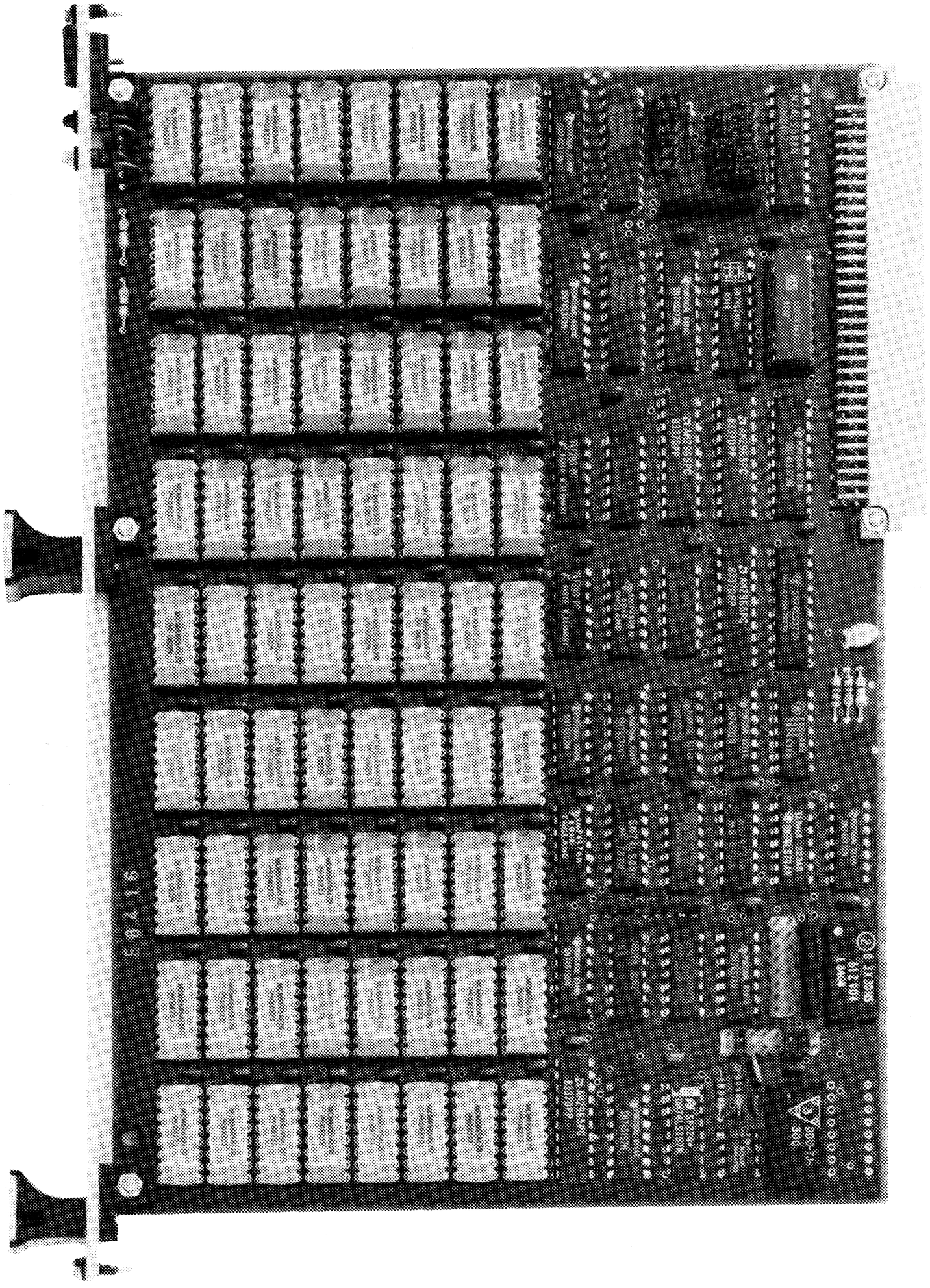
Figure 1.1: The MVME202 Dynamic Memory Module



CHAPTER 1

GENERAL INFORMATION

1.1. INTRODUCTION

This manual provides general information, functional description, installation instructions, operating instructions and maintenance information for the MVME202, MVME222-1 and MVME222-2 Dynamic Memory modules.

Figure 1.1 shows the MVME202 module.

1.2. SPECIFICATIONS

The specifications of the MVME202, MVME222-1 and MVME222-2 Dynamic Memory modules are given in the following table.

Table 1.1: MVME202/222 Specifications

CHARACTERISTIC	SPECIFICATION
Memory Capacity	MVME202: 512K bytes (524288 bytes) MVME222-1: 1M bytes (1048576 bytes) MVME222-2: 2M bytes (2097152 bytes)
VMEbus Interface	Option A24:D16 slave interface, supporting 8-bit and 16-bit read, write and read-modify-write data transfers. Address modifier codes factory-programmed or user-selectable.
Access Times	Write access time (AS* to DTACK*): 70 ns (typ) Read access time (AS* to DTACK*): 320 ns (typ)
Error Detection	Byte parity generation and checking.
Memory Refresh	Local asynchronous refresh controller independent of VMEbus signals.
Indicators	LEDs on the front panel for parity error and board selection.
System Requirements	The following system modules are required to operate the MVME202/222 Dynamic Memory module: - a VME microprocessor module with an option A24:D16 VMEbus master interface - a VMEbus backplane - a VME card cage - a power supply unit

Table 1.1: MVME202/222 Specifications (continued)

CHARACTERISTIC	SPECIFICATION
Mechan. Dimensions	Double height VME board with front panel Board size: 233 mm * 160 mm Front panel size: 262 mm * 20 mm
Connectors	One 96 pole DIN 41612 connector for VMEbus
Power Requirements	+ 5 V DC, 1.4 A (typ), 1.9 A (max)
Environmental Conditions	Operating temperature: 0 to 70 C Storage temperature: -40 to 100 C Operating humidity: 0% to 90% non condensing

1.3. REFERENCE MANUALS

The following manuals may be used for further information about the VMEbus, and the VME system configuration:

- MVMEBS VMEbus Specification Manual
- MVMECNFG1 VMEmodules Hardware and Software Configuration Manual

1.4. MANUAL TERMINOLOGY

1.4.1. Address and Data Formats

Throughout this manual, unless otherwise noted, all address and data values are given in hexadecimal format.

1.4.2. Electrical Signal Levels

A signal line is always assumed to be in one of two levels, or in transition between these levels. Whenever the term "high" is used, it refers to a high TTL voltage level (> +2.0 V). The term "low" refers to a low TTL voltage level (< +0.8 V).

There are two possible transitions which can appear on a signal line, and these will be referred to as "edges". A "rising edge" is defined as the time period during which a signal line makes its transition from a low level to a high level. The "falling edge" is defined as the time period during which a signal line makes its transition from a high level to a low level.

A signal is defined as "active low" if the function associated with the signal line is valid or initiated by either a low level or a falling edge on the signal line. The mnemonics of active low signals are marked with the suffix "*".

A signal is defined as "active high" if the function associated with the signal line is valid or initiated by either a high level or a rising edge on the signal line.

1.4.3. Logic Signal States

The terms "assert" and "negate" describe the logic state of a signal without indicating the associated voltage level.

An active low signal is asserted when its voltage level is low, it is negated when its voltage level is high.

An active high signal is asserted when its voltage level is high, it is negated when its voltage level is low.

For signals which are driven by three-state or open-collector outputs, the term "release" describes the high impedance state of the corresponding driver. Typically these signal lines are driven to a high voltage level by pull-up resistors when all drivers on the line are turned off.

CHAPTER 2

FUNCTIONAL DESCRIPTION

2.1. INTRODUCTION

For the following description, the MVME202/222 module is regarded as consisting of functional blocks, as shown in Figure 2.1.

2.2. HARDWARE OVERVIEW

The MVME202/222 Dynamic RAM module consists of the memory array, the VMEbus slave interface, a byte parity generator/checker, and refresh, timing and control logic.

The memory array of the MVME202 module has a size of 524288 bytes, organized in four banks of eighteen 64 Kbit RAM devices.

The memory array of the MVME222-1 module has a size of 1048576 bytes, organized in two banks of eighteen 256 Kbit RAM devices.

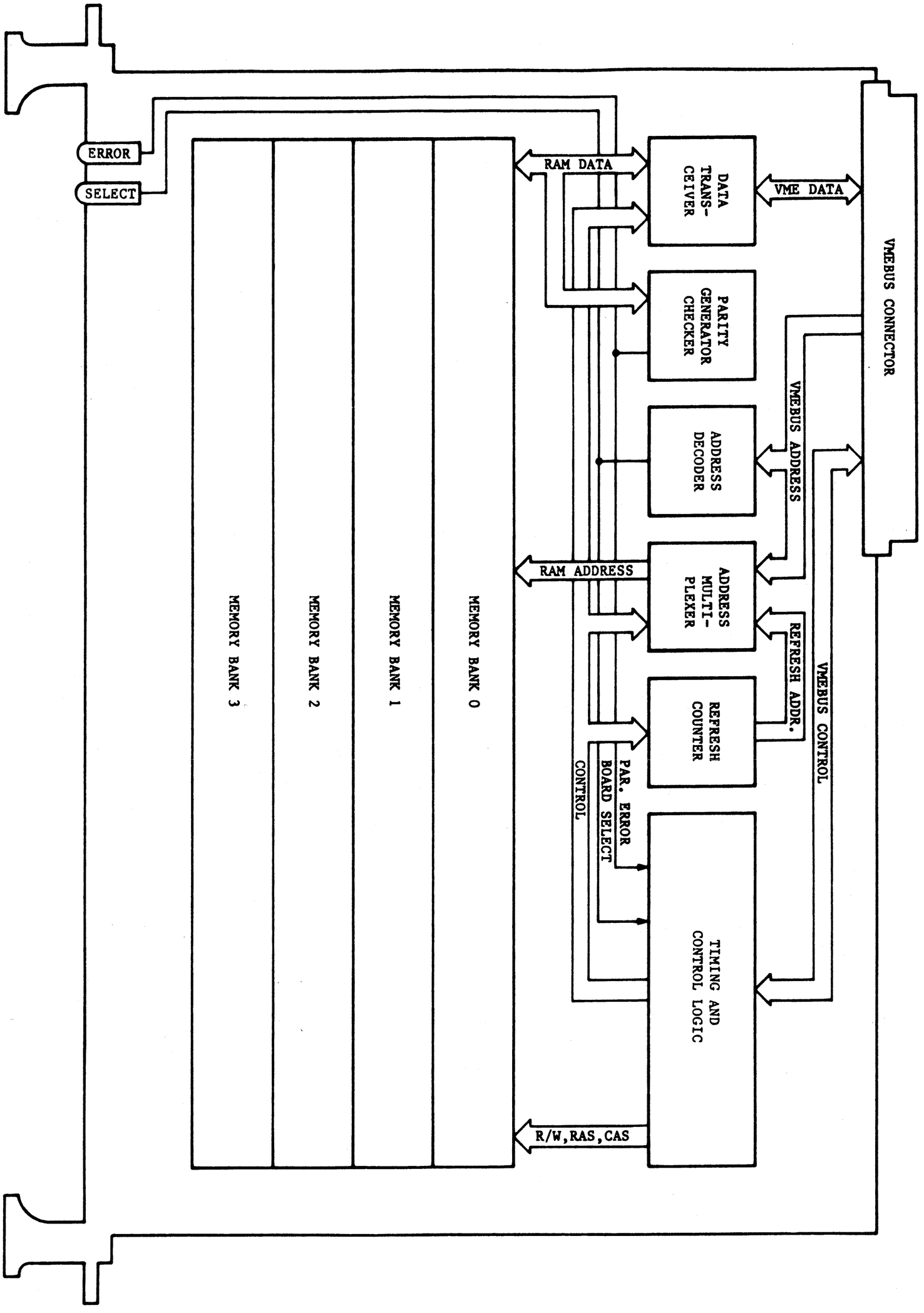
The memory array of the MVME222-2 module has a size of 2097152 bytes, organized in four banks of eighteen 256 Kbit RAM devices.

The VMEbus interface provides an option A24:D16 slave interface and supports 8-bit (byte) and 16-bit (word) read, write and read-modify-write data transfers. The interface consists of the address decoder, the data transceivers, and data transfer control logic. A board selection is indicated by the green SELECT diode on the front panel, which is lit for the duration of a data transfer cycle on the module. A detailed description and timing diagrams of the VMEbus interface are given in Paragraph 2.6.

When data is written into RAM, a parity bit is generated for each byte and stored along with the data. When data is read from RAM, the parity of each byte and the parity bit are checked. Depending on the result of the parity check, either a data transfer acknowledge or a bus error signal is returned to the VMEbus master. If a parity error is detected, the red ERROR diode on the front panel is turned on. It remains lit until the completion of the next successful read or write access.

To ensure data retention in the memory, a refresh controller performs a RAS-only refresh cycle in the dynamic RAM devices every 15.6 microseconds on ascending row addresses. Memory refresh is independent of VMEbus signals. Control logic arbitrates between memory refresh and data transfer cycles and generates the local control and timing signals totally irrespective of the VMEbus data transfer handshake.

Figure 2.1: MVME202/222 Block Diagram



2.3. ADDRESS DECODER

The VMEbus address lines A01-A23 are routed on the MVME202/222 modules to the board selector, the memory bank selector, and the row/column address inputs at the memory chips. The distribution of the address lines is dependant on the memory module capacity (512KB, 1MB or 2MB) and addressing mode (continuous or interleaving).

Continuous addressing is the standard mode of operation where one memory module contains all sequential address locations from its base address upwards throughout its total capacity.

Interleaving is a method of addressing a pair of memory modules so that one module contains all even, the other module all odd word address locations. This method improves the speed of writing data into sequential addresses, as the access to the second module may already be started while the first module is still busy with storing the previously transferred data locally.

With the MVME202/222 Dynamic Memory modules interleaving can be selected as a jumper option. The benefit in data throughput depends mainly on the speed of the VMEbus master and may be significant for fast DMA controllers.

The following table illustrates where the VMEbus address lines are routed on the MVME202/222 modules for the different memory capacities and addressing modes.

Table 2.1: Address Decoding Scheme

MODULE	ADDRESSING	BOARD SELECT	BANK SELECT	MATRIX ADDRESS
MVME202	continuous	A19-A23	A01,A18	A02-A17
MVME222-1	continuous	A20-A23	A01	A02-A19
MVME222-2	continuous	A21-A23	A01,A20	A02-A19
MVME202	interleaving	A01,A20-A23	A18,A19	A02-A17
MVME222-1	interleaving	A01,A21-A23	A20	A02-A19
MVME222-2	interleaving	A01,A22,A23	A20,A21	A02-A19

In addition to the address lines, the MVME202/222 modules decode the VMEbus address modifier lines for detecting a board selection. The address modifier decoder is a bipolar PROM at designation U5 which may be programmed by the user to respond to any desired address modifier codes. A detailed description of how to configure addressing mode, base address and address modifier codes will be given in Chapter 4.

The MVME202/222 modules are shipped with the PROM programmed for the standard address modifier codes shown in Table 2.2.

Table 2.2: Factory Programmed Address Modifier Codes

AM CODE	FUNCTION
39	Standard Non-Privileged Data Access
3A	Standard Non-Privileged Program Access
3D	Standard Supervisory Data Access
3E	Standard Supervisory Program Access

2.4. WRITE OPERATION

The sequence of a write operation on the MVME202/222 Dynamic Memory modules is as follows:

When the board is selected, the bank select signals, the RAM row/column addresses, the data and the data strobes are latched. The data transfer acknowledge signal is then asserted on the VMEbus. This allows the VMEbus master to terminate the current cycle and to begin the next operation while the MVME202/222 module performs all further data storage functions locally.

The parity logic generates a parity bit for each byte received from the VMEbus. Depending on the state of the data strobe signals, either the lower byte (D00-D07), or the upper byte (D08-D15), or both are written along with their parity bits into the addressed memory location.

If a memory refresh is currently in progress when the module is accessed from the VMEbus, the write access is made pending on the module and the local data storage will not be started until the refresh cycle is terminated. However, this has no effect on the access time, i.e. the data transfer acknowledge signal will not be delayed.

2.5. READ OPERATION

The sequence of a read operation on the MVME202/222 Dynamic Memory modules is as follows:

When the board is selected, the bank select signals, the RAM row/column addresses and the data strobes are latched. Both data bytes are then read along with their parity bits from the addressed memory word location and asserted on the VMEbus.

The parity logic checks the parity of each byte and its corresponding parity bit. Depending on the result of this check either the data transfer acknowledge or the bus error signal is asserted on the VMEbus. A parity error is also indicated by the red ERROR diode on the front panel.

If a memory refresh is currently in progress when the module is accessed from the VMEbus, the local data fetch will not be started until the refresh cycle is terminated. In this case, the data transfer acknowledge or the bus error signal will be delayed by the necessary amount of time.

2.6. VMEBUS INTERFACE

The VMEbus interface provides the data path between the MVME202/222 memory and the VMEbus backplane. The interface complies with all requirements for the signal driver/receiver characteristics and bus operation protocols, as specified in the VMEbus Specification Rev.B.

The following paragraphs give detailed specifications of all VMEbus signals and operations supported by the MVME202/222 module.

2.6.1. VMEbus Signals

All VMEbus signals are available at the upper rear connector P1. Table 2.3 identifies all these signals by mnemonics, pin numbers at P1, and functional descriptions. The locations of the VMEbus signals at connector P1 are shown in Table 2.4.

Table 2.3: VMEbus Signal Description

SIGNAL	PIN NO.	SIGNAL DESCRIPTION
A01..A07 A08..A23	A30..A24 C30..C15	ADDRESS BUS 23 address input lines that specify a memory word location.
AM0 AM1 AM2 AM3 AM4 AM5	B16 B17 B18 B19 A23 C14	ADDRESS MODIFIERS Six address modifier input signals that provide additional address information.
D00..D07 D08..D15	A1..A8 C1..C8	DATA BUS 16 bidirectional three-state data lines for byte and word transfers.
LWORD*	C13	LONG WORD An active low input signal that indicates a 32-bit data transfer.
WRITE*	A14	WRITE An active low input signal that specifies the direction of a data transfer: A high level indicates a read operation, a low level indicates a write operation.

Table 2.3: VMEbus Signal Description (continued)

SIGNAL	PIN NO.	SIGNAL DESCRIPTION
SYSRESET*	C12	SYSTEM RESET An active low input signal that resets the control logic on the module.
GND	A9, A11, A15, A17, A19, B20, B23, C9	GROUND
+5V	A32, B32, C32	+ 5 VOLTS POWER
BR0*	(B12)	BUS REQUEST LEVEL 0
BR1*	(B13)	BUS REQUEST LEVEL 1
BR2*	(B14)	BUS REQUEST LEVEL 2
BR3*	(B15)	BUS REQUEST LEVEL 3
BBSY*	(B1)	BUS BUSY
BCLR*	(B2)	BUS CLEAR
IRQ1*	(B30)	INTERRUPT REQUEST LEVEL 1
IRQ2*	(B29)	INTERRUPT REQUEST LEVEL 2
IRQ3*	(B28)	INTERRUPT REQUEST LEVEL 3
IRQ4*	(B27)	INTERRUPT REQUEST LEVEL 4
IRQ5*	(B26)	INTERRUPT REQUEST LEVEL 5
IRQ6*	(B25)	INTERRUPT REQUEST LEVEL 6
IRQ7*	(B24)	INTERRUPT REQUEST LEVEL 7
ACFAIL*	(B3)	AC POWER FAILURE
SYSFAIL*	(C10)	SYSTEM FAILURE
SYSCLK	(A10)	SYSTEM CLOCK
SERCLK	(B21)	VMSBUS CLOCK
SERDAT	(B22)	VMSBUS DATA
+5VSTB	(B31)	+ 5 VOLTS STAND BY POWER
+12V	(C31)	+ 12 VOLTS POWER
-12V	(A31)	- 12 VOLTS POWER
		These signals are not connected with the module.

Table 2.4: Connector P1 Signal Locations

PIN NO.	ROW A SIGNALS	ROW B SIGNALS	ROW C SIGNALS	PIN NO.
1	D00	(BBSY*)	D08	1
2	D01	(BCLR*)	D09	2
3	D02	(ACFAIL*)	D10	3
4	D03	BG0IN*	D11	4
5	D04	BG0OUT*	D12	5
6	D05	BG1IN*	D13	6
7	D06	BG1OUT*	D14	7
8	D07	BG2IN*	D15	8
9	GND	BG2OUT*	GND	9
10	(SYSCLK)	BG3IN*	(SYSFAIL*)	10
11	GND	BG3OUT*	BERR*	11
12	DS1*	(BR0*)	SYSRESET*	12
13	DS0*	(BR1*)	LWORD*	13
14	WRITE*	(BR2*)	AM5	14
15	GND	(BR3*)	A23	15
16	DTACK*	AM0	A22	16
17	GND	AM1	A21	17
18	AS*	AM2	A20	18
19	GND	AM3	A19	19
20	IACK*	GND	A18	20
21	IACKIN*	(SERCLK)	A17	21
22	IACKOUT*	(SERDAT)	A16	22
23	AM4	GND	A15	23
24	A07	(IRQ7*)	A14	24
25	A06	(IRQ6*)	A13	25
26	A05	(IRQ5*)	A12	26
27	A04	(IRQ4*)	A11	27
28	A03	(IRQ3*)	A10	28
29	A02	(IRQ2*)	A09	29
30	A01	(IRQ1*)	A08	30
31	(-12V)	(5V STBY)	(+12V)	31
32	+5V	+5V	+5V	32

Note: Signals in parentheses are not used by the MVME202/222

2.6.2. Timing Specifications

This paragraph provides detailed VMEbus timing specifications of the MVME202/222 Dynamic Memory modules for read and write operations.

The tabulated maximum and minimum times are guaranteed over the recommended operating conditions, as specified in Table 1.1. Whenever possible, typical times for operation at 25 C temperature and 5.00 V supply voltage are given.

The diagrams specify the timings that are supplied by the MVME202/222 modules for interactions with other modules on the VMEbus. No timing requirements for these modules are given, but it is assumed that they comply with the requirements of the VMEbus Specification Rev.B.

Figure 2.2: Read Cycle

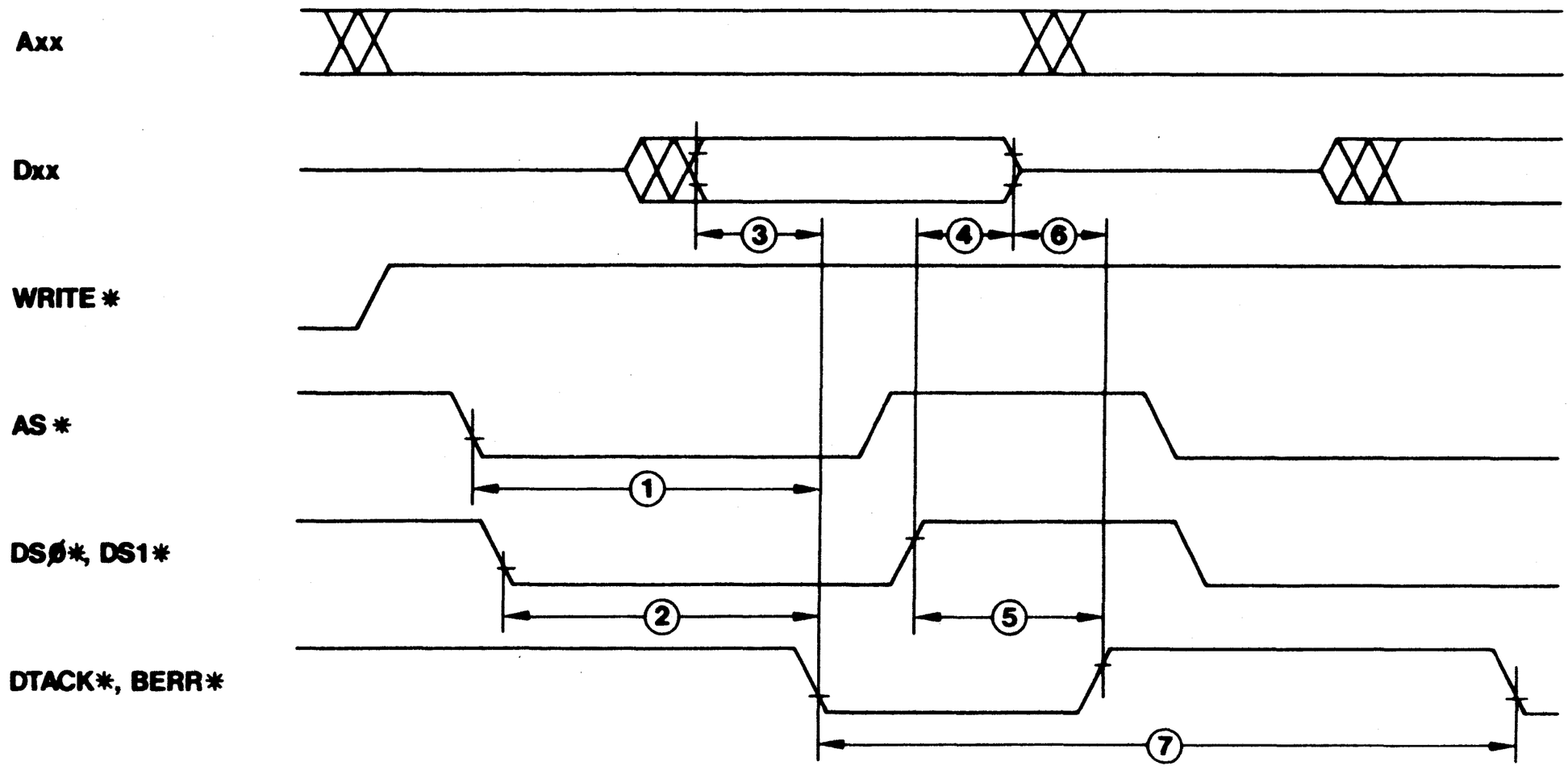


Table 2.5: Read Cycle Timing

NO.	PARAMETER	NOTES	MIN	TYP	MAX	UNIT
1	AS* low to DTACK*/BERR* low	1,4		320	830	ns
2	DS0*/DS1* low to DTACK*/BERR* low	2,4		290	800	ns
3	Data valid to DTACK* low		35	55		ns
4	DS0*/DS1* high to Data invalid		10	20		ns
5	DS0*/DS1* high to DTACK*/BERR* high			25	35	ns
6	Data high imp. to DTACK*/BERR* high		0	5		ns
7	DTACK* low to DTACK* low	3,4		370	880	ns

Note 1: Provided that the VMEbus master drives DS0*/DS1* low less than 30 ns after driving AS* low.

Note 2: Provided that the VMEbus master drives DS0*/DS1* low more than 30 ns after driving AS* low.

Note 3: Provided that the VMEbus master drives AS* low less than 50 ns and DS0*/DS1* low less than 80 ns after receiving DTACK* low.

Note 4: The maximum time can result if a refresh cycle has just started when the board is selected.

Figure 2.3: Write Cycle

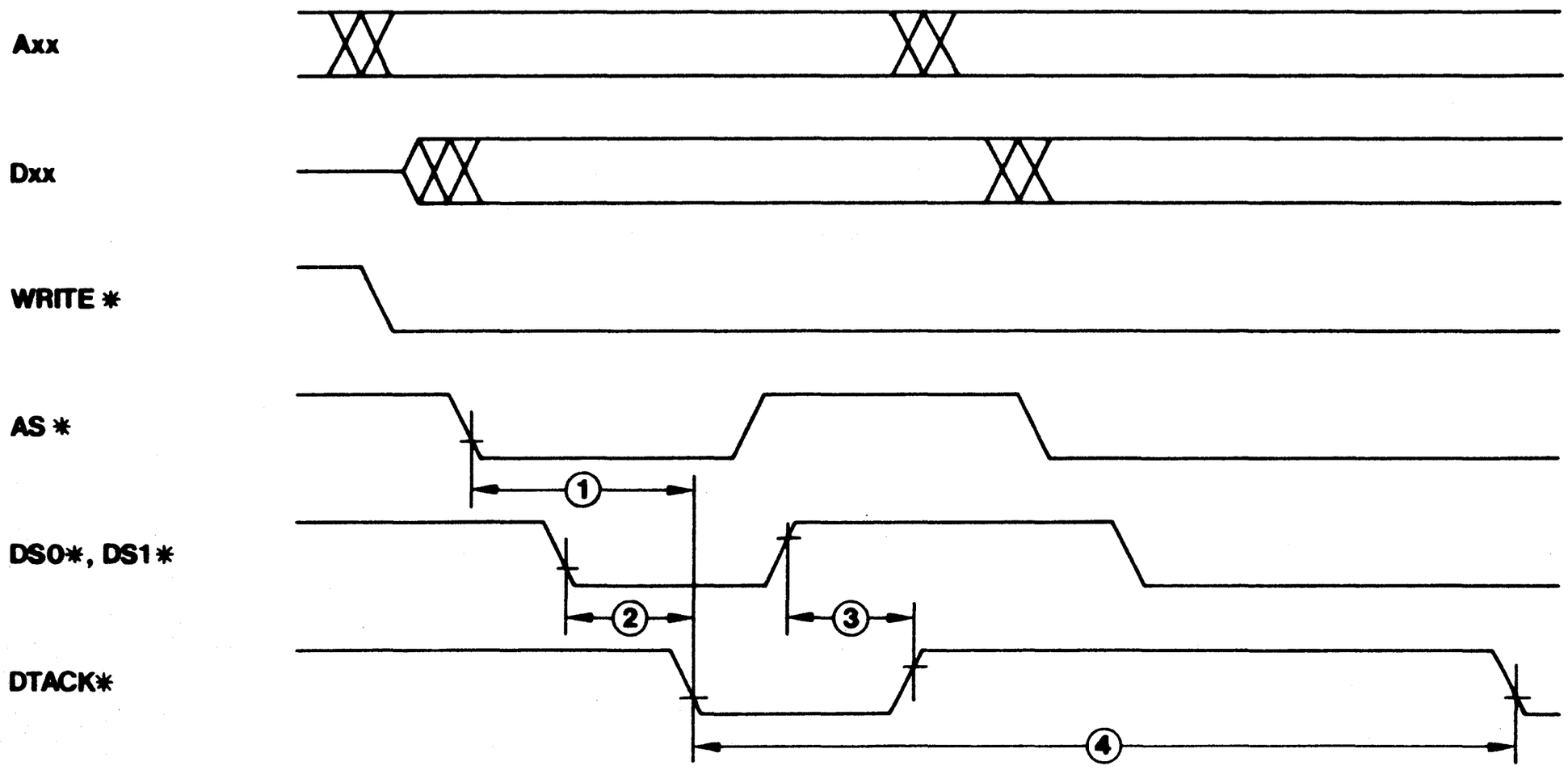


Table 2.6: Write Cycle Timing

NO.	PARAMETER	NOTES	MIN	TYP	MAX	UNIT
1	AS* low to DTACK* low	1,4		70	815	ns
2	DS0*/DS1* low to DTACK* low	2,4		35	780	ns
3	DS0*/DS1* high to DTACK* high			25	35	ns
4	DTACK* low to DTACK* low	3,4		390	865	ns

Note 1: Provided that the VMEbus master drives DS0*/DS1* low less than 35 ns after driving AS* low.

Note 2: Provided that the VMEbus master drives DS0*/DS1* low more than 35 ns after driving AS* low.

Note 3: Provided that the VMEbus master drives AS* low less than 320 ns and DS0*/DS1* low less than 355 ns after receiving DTACK* low.

Note 4: The maximum time can result if a refresh cycle has just started when the board is selected.

CHAPTER 3

INSTALLATION INSTRUCTIONS

3.1. INTRODUCTION

This chapter provides the user of the MVME202/222 Dynamic Memory module with the unpacking, inspection, hardware preparation and installation procedures.

3.2. UNPACKING INSTRUCTIONS

IF THE SHIPPING CARTON IS DAMAGED UPON RECEIPT, REQUEST THAT CARRIER'S AGENT BE PRESENT DURING UNPACKING AND INSPECTION OF THE MODULE.

Unpack the MVME202/222 Dynamic Memory module from its shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing or reshipping the module.

AVOID TOUCHING AREAS OF MOS CIRCUITRY. STATIC DISCHARGE CAN DAMAGE INTEGRATED CIRCUITS.

3.3. INSPECTION

The module should be inspected upon receipt for broken, damaged or missing parts and for physical damage to the printed circuit board.

3.4. MODULE PREPARATION

This paragraph describes the hardware preparation of the MVME202/222 module prior to system installation. The module is shipped with factory-installed jumpers ready for use in a VME system. However, the jumper areas which determine the VMEbus base address and the interleaving mode must be configured according to the actual system requirements. Also, if the module shall respond to address modifier codes other than the factory-programmed codes listed in Table 2.2, the user has to program a new address modifier PROM.

Figure 3.1 illustrates the locations of the jumper areas and the address modifier PROM on the MVME202/222 module. Jumper area K1 determines the module base address on the VMEbus, jumper area K2 specifies the memory module capacity and selects the interleaving mode. K3 is a test connector, K4 configures the local timing for various dynamic RAM devices. K3 and K4 are reserved for Motorola Manufacturing and Field Service purposes and are not available to the user.

3.4.1. Base Address Selection

Jumper Area K1 determines the base address of the MVME202/222 module in the 16MB VMEbus address map. Each of the VMEbus address lines A01 and A19-A23 is represented by one row of four pins on K1 and may be chosen to be low (jumper on right position), high (jumper on left position), or not used (jumper on mid position) for selecting the board.

The address lines which are used for the board selection are dependant on the module capacity (512KB, 1MB or 2MB) and the addressing mode (continuous or interleaving).

Continuously addressed modules contain all sequential even and odd word address locations. Address line A01 is not used for the board selection. The base address may be any address boundary which corresponds to the memory module capacity.

Interleaving addressed modules are used in pairs with one module containing all even, the other module containing all odd word address locations. The first module is selected when A01 is low, the second when A01 is high. The base addresses of both modules must be equal and may be any address boundary which corresponds to the total capacity of the memory module pair.

Figure 3.2 illustrates the configuration of K1 for each module capacity and addressing mode option. The jumper positions on not used address lines are prescribed and shown as bold-faced connections. The jumpers on the address lines which are used for the board selection may be placed on the "high" (left) or "low" (right) position and are shown as outlined connections.

Original configuration:
MVME202: 512KB continuous, base address $200000
MVME222-1: 1MB continuous, base address $200000
MVME222-2: 2MB continuous, base address $200000

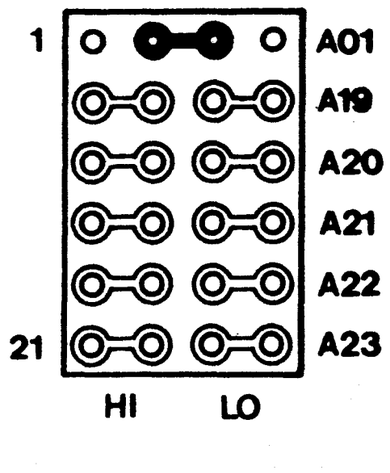
3.4.2. Memory Capacity and Addressing Mode

The jumper area K2 configures the memory bank select lines for the various module capacities (512KB, 1MB or 2MB) and for the addressing mode (continuous or interleaving). Figure 3.3 illustrates the jumper positions on K2 for all selectable options.

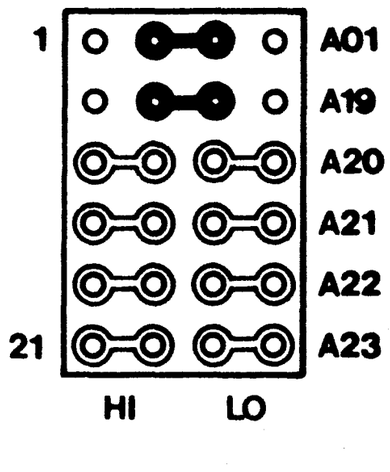
Original configuration:
MVME202: 512KB, continuous addressing
MVME222-1: 1MB, continuous addressing
MVME222-2: 2MB, continuous addressing

Figure 3.2: Jumper Area K1

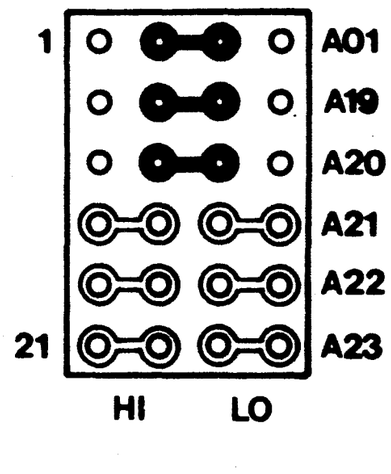
MVME202
512KB continuous



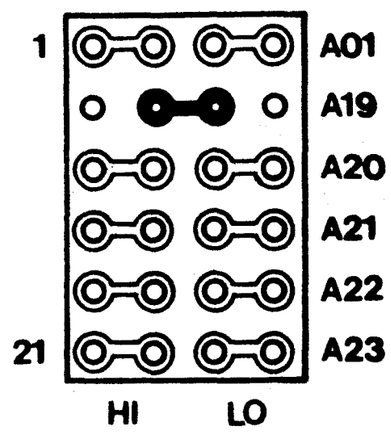
MVME222-1
1MB continuous



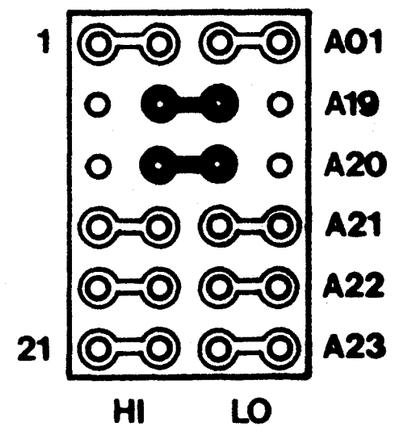
MVME222-2
2MB continuous



MVME202
512KB interleaving



MVME222-1
1MB interleaving



MVME222-2
2MB interleaving

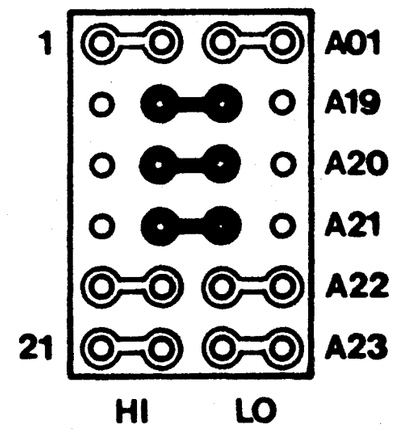
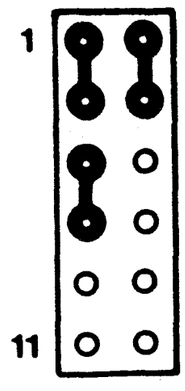
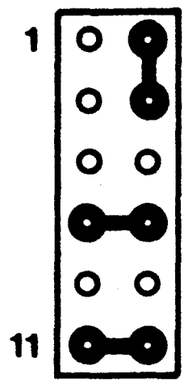


Figure 3.3: Jumper Area K2

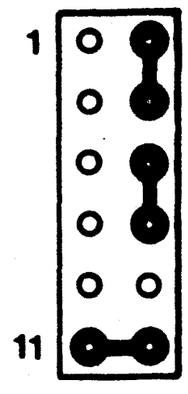
MVME202
512KB continuous



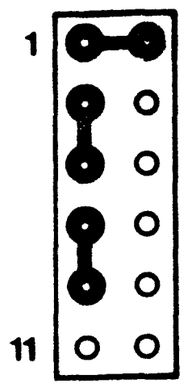
MVME222-1
1MB continuous



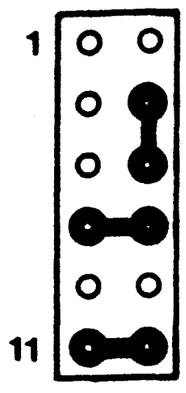
MVME222-2
2MB continuous



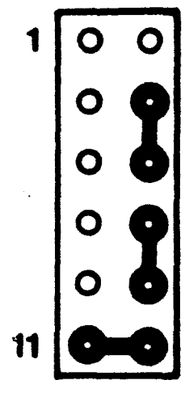
MVME202
512KB interleaving



MVME222-1
1MB interleaving



MVME222-2
2MB interleaving



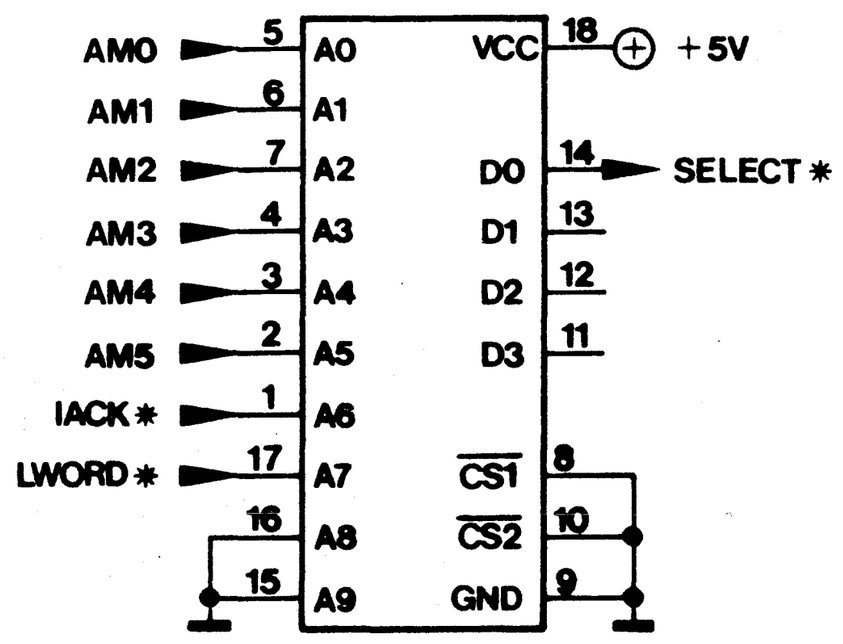
3.4.3. Address Modifier Decoder

The address modifier decoder is a bipolar PROM at designation U5 on the MVME202/222 module. This PROM is programmed in the factory to respond to the address modifier codes for standard supervisory and non-privileged program and data access (39, 3A, 3D, 3E). However, the user may select any other subset of valid address modifier codes and program the decoder PROM accordingly. Valid address modifier codes for the MVME202/222 modules are the codes 10-1F, 39, 3A, 3D and 3E.

In addition to decoding the address modifiers, the PROM is used for disabling a board selection during interrupt acknowledge and longword transfer cycles.

Figure 3.4 illustrates the connections of the address modifier decoder PROM. The signals AM0-AM5 are fed to the PROM address inputs A0-A5, IACK* and LWORD* are fed to A6 and A7. The inputs A8 and A9 are not used and are connected to ground. The PROM data output D0 is used for the board selection.

Figure 3.4: Address Modifier Decoder PROM



The PROM may be an Advanced Micro Devices Am27S33A or any electrically and physically compatible bipolar PROM, organized in 1024 x 4 bits, with a maximum address access time of 35 ns.

Table 3.1 may be used for specifying the PROM contents. Each address modifier code (00-3F) is represented by a corresponding PROM address. All PROM locations belonging to address modifier codes to which the module shall respond must be programmed with the data "0". All other PROM locations must be programmed with the data "F". For unused and invalid locations "F" is already entered in the table.

Table 3.1: Address Modifier Decoder PROM Specification

AM CODE	FUNCTION	ADDRESS	DATA
XX	Not Used	100-3FF	F
3F	Standard Supervisory Ascending Access	0FF	F
3E	Standard Supervisory Program Access	0FE	.
3D	Standard Supervisory Data Access	0FD	.
3C	Reserved	0FC	F
3B	Standard Non-Privileged Ascending Access	0FB	F
3A	Standard Non-Privileged Program Access	0FA	.
39	Standard Non-Privileged Data Access	0F9	.
2E-38	Reserved	0EE-0F8	F
2D	Short Supervisory I/O Access	0ED	F
2A-2C	Reserved	0EA-0EC	F
29	Short Non-Privileged I/O Access	0E9	F
20-28	Reserved	0E0-0E8	F
1F	User Defined	0DF	.
1E	User Defined	0DE	.
1D	User Defined	0DD	.
1C	User Defined	0DC	.
1B	User Defined	0DB	.
1A	User Defined	0DA	.
19	User Defined	0D9	.
18	User Defined	0D8	.
17	User Defined	0D7	.
16	User Defined	0D6	.
15	User Defined	0D5	.
14	User Defined	0D4	.
13	User Defined	0D3	.
12	User Defined	0D2	.
11	User Defined	0D1	.
10	User Defined	0D0	.
0F	Extended Supervisory Ascending Access	0CF	F
0E	Extended Supervisory Program Access	0CE	F
0D	Extended Supervisory Data Access	0CD	F
0C	Reserved	0CC	F
0B	Extended Non-Privileged Ascending Access	0CB	F
0A	Extended Non-Privileged Program Access	0CA	F
09	Extended Non-Privileged Data Access	0C9	F
00-08	Reserved	0C0-0C8	F
XX	Interrupt Acknowledge	080-0BF	F
XX	Longword Transfer	040-07F	F
XX	Invalid	000-03F	F

Note: Data "F" disables, data "0" enables the MVME202/222 module for the corresponding address modifier code.

3.5. MODULE INSTALLATION

When the MVME202/222 Dynamic Memory module has been configured as desired by the user, it is ready to be installed in a VME chassis as follows:

a. Turn all equipment power off.

b. Insert the MVME202/222 module in any VMEbus card slot.

c. Secure the module in place with two screws on the front panel.

d. Turn the equipment power on.

PRIOR TO INSERTING OR REMOVING MODULES INTO OR FROM THE VME CHASSIS, ENSURE THAT POWER IS TURNED OFF TO AVOID DAMAGE TO THE COMPONENTS.

CHAPTER 4

OPERATING INSTRUCTIONS

4.1. INTRODUCTION

This chapter describes the function of the front panel LEDs, explains the possible reasons for parity errors, and gives initialization instructions for the MVME202/222 module.

4.2. FRONT PANEL INDICATORS

The green SELECT diode indicates a board selection. Note that the LED is turned on only for the duration of a data transfer cycle. Therefore sporadic accesses to the MVME202/222 module will not be visible.

The red ERROR diode indicates that a parity error has been detected during a read cycle. The LED remains lit until the completion of the next successful read or write cycle on the module. The ERROR diode is also cleared by a system reset.

4.3. PARITY ERRORS

On the MVME202/222 Dynamic Memory module parity errors may occur for the following reasons:

a. Charge alterations in the memory cells caused by alpha particles.

This problem is common for all dynamic memories. The MVME202/222 modules, however, are populated with modern RAM devices which offer an optimum in insensitivity to alpha particles.

b. Reading bytes without previously writing the whole word.

When reading a single (upper or lower) data byte from the MVME202/222, the module transmits the whole data word containing the addressed byte, and also performs the parity check on both bytes.

c. Unexpected read cycles on not initialized locations.

Note that the MC68000, and probably other microprocessors too, perform extra read cycles when executing certain instructions in memory. Such instructions are CLR, MOVE from SR, MOVEM and Scc.

4.4. PARITY INITIALIZATION

For the previously described reasons it is good practice to initialize all parity bits on the MVME202/222 modules prior to executing programs on them. This can be done by writing some data into all dynamic RAM locations during the initialization phase of the operating system.

The following example is such an initialization routine in MC68000 assembler language:

```
START     EQU       $200000              dynamic RAM start address
SIZE      EQU       $200000              dynamic RAM size = 2MB

          MOVEM.L   D0-D7/A0-A1,-(A7)    save registers on stack
          CLR.L     D0                   clear all data registers
          CLR.L     D1
          CLR.L     D2
          CLR.L     D3
          CLR.L     D4
          CLR.L     D5
          CLR.L     D6
          CLR.L     D7
          MOVEA.L   #START,A0            load RAM start address into A0
          LEA.L     SIZE(A0),A1          load RAM end address in A1

LOOP      MOVEM.L   D0-D7,(A0)+          write zeros into all RAM locations
          CMPA.L    A0,A1
          BNE.S     LOOP

          MOVEM.L   (A7)+,D0-D7/A0-A1    restore registers

          END
```

Note that the CLR instruction must not be used for initializing dynamic RAM as CLR reads a memory destination before it writes to it.

CHAPTER 5

MAINTENANCE INFORMATION

5.1. INTRODUCTION

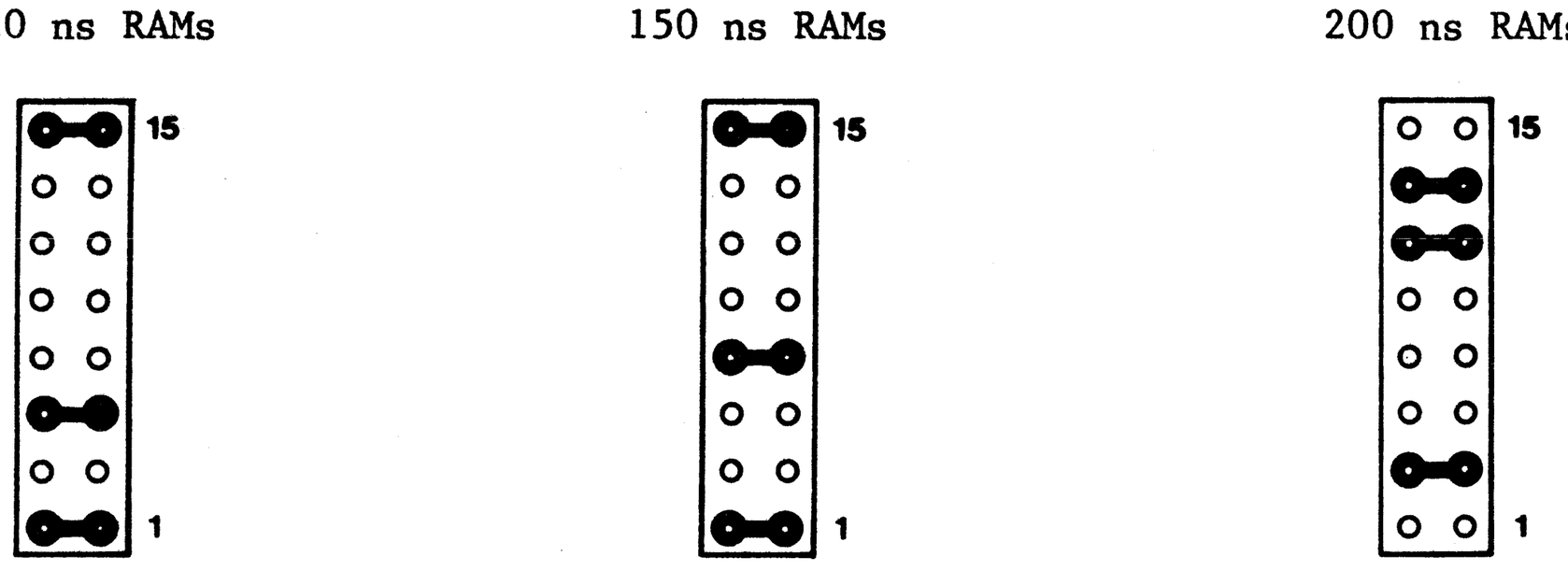
This chapter provides access time configuration instruction, test connector description, parts list, and assembly drawing for the MVME202/222 Dynamic Memory module.

5.2. ACCESS TIME CONFIGURATION

The MVME202/222 module is populated in the factory with dynamic RAM devices of 150 ns access time. The module design however provides for upgrade to 120 ns or downgrade to 200 ns RAM devives. The jumper area K4 configures the control logic timing for the various access times.

Figure 5.1 illustrates the jumper positions on K4 for all selectable options.

Figure 5.1: Jumper Area K4

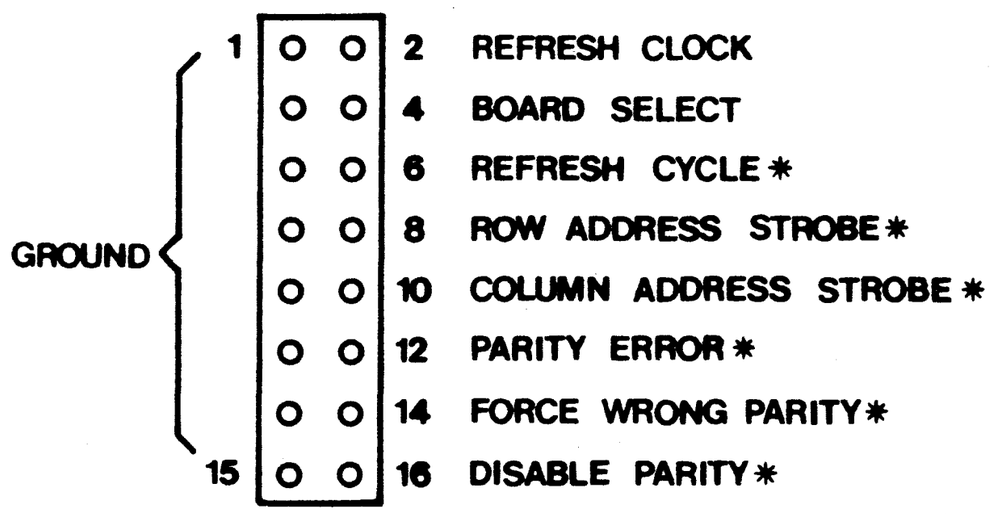


5.3. TEST CONNECTOR

K3 is a test connector for Motorola Manufacturing and Field Service purposes. The connector provides test pins for several control signals (refresh clock, board select, refresh cycle, row and column address strobes, parity error). The parity generator can be forced to generate wrong parity bits by placing a jumper on pins 13 and 14. Parity generation and checking can be disabled by placing a jumper on pins 15 and 16.

Figure 5.2 illustrates the signal locations at K3.

Figure 5.2: Test Connector K3



5.4. PARTS LIST

Table 5.1 reflects the latest issue of hardware for the MVME202/222 modules at the time of printing. All parts are identified by quantity, designation on the board, Motorola part number, and a short part description. The part locations are shown in Figure 5.3.

Table 5.1: MVME202/222 Parts List

QU	DESIGNATION	PART NUMBER	DESCRIPTION
1	C2	21NG9604A01	270 pF, 50 V Ceramic Capacitor
82	C3-C84	21NW9702A09	0.1 uF, 50 V Ceramic Cap. (MVME202)
50	C3-C52	21NW9702A09	0.1 uF, 50 V Ceramic Cap. (MVME222-1)
82	C3-C84	21NW9702A09	0.1 uF, 50 V Ceramic Cap. (MVME222-2)
1	C1	23NW9618A74	47 uF, 10 V Electrolytic Capacitor
1	DL1	01NW9804C32	3*30 ns Triple Delay Line
1	DL2	01NG9804A01	300 ns Delay Line, 10 Taps
3	K1,K2	28NW9802C63	Header Double Row 2*6 Pins
2	K3,K4	28NW9802B34	Header Double Row 2*8 Pins
1	LD1	48NW9612A34	Light Emitting Diode Red
1	LD2	48NW9612A38	Light Emitting Diode Green
1	P1	28-G9802M03	DIN 41612 C 96 Male Connector
2	R7,R8	29NW9805B98	0 ohm Dummy Resistor
1	R3	06SW-124A09	22 ohm, 0.25 W, 5% Carbon Resistor
1	R4	06SW-124A17	47 ohm, 0.25 W, 5% Carbon Resistor
2	R1,R2	06SW-124A73	10 kohm, 0.25 W, 5% Carbon Resistor
1	R5	06SW-124A79	18 kohm, 0.25 W, 5% Carbon Resistor
1	R6	06SW-124A81	22 kohm, 0.25 W, 5% Carbon Resistor
2	RP1,RP2	51NW9626A69	7*1 kohm, 5% SIL Resistor Network
1	U5	51-G5021M01	AM27S33APC 1024*4 PROM (programmed)
4	U11,U12,U18, U39	51NG9615A04	AM2965PC Octal DRAM Driver TS
1	U16	51NW9615B65	MC1455P Timing Circuit
2	U24,U25	51NW9615G47	MC3482B Octal Latch TS
72	U40-U111	51NG9615A01	MCM6665B-15 64K DRAM (MVME202)
36	U40-U75	51NG9615A06	MCM6256-15 256K DRAM (MVME222-1)
72	U40-U111	51NG9615A06	MCM6256-15 256K DRAM (MVME222-2)

Table 5.1: MVME202/222 Parts List (continued)

QU	DESIGNATION	PART NUMBER	DESCRIPTION
1	U14	51NG9615A05	SN74AS74N Dual D-Flip-Flop
2	U34,U35	51NW9615E35	SN74AS280N Parity Generator/Checker
1	U22	51NW9615C21	SN74LS04N Hex Inverter
1	U29	51NW9615C22	SN74LS08N Quad 2-Input AND Gate
1	U9	51NW9615C25	SN74LS74AN Dual D-Flip-Flop
2	U6,U7	51NW9615E98	SN74LS373N Octal D-Latch TS
1	U1	51NW9615G12	SN74LS375N Quad Latch
1	U26	51NW9615F83	SN74LS393N Dual 4-Bit Binary Counter
1	U23	51NG9615A07	SN74LS399N Quad 2 to 1 Multiplexer
1	U4	51NW9615N77	SN74LS688N 8-Bit Comparator
1	U19	51NW9615C94	SN74S00N Quad 2-Input NAND Gate
1	U36	51NW9615D32	SN74S02N Quad 2-Input NOR Gate
1	U27	51NW9615C56	SN74S08N Quad 2-Input AND Gate
1	U21	51NW9615E27	SN74S10N Triple 3-Input NAND Gate
1	U30	51NW9615D92	SN74S20N Dual 4-Input NAND Gate
2	U13,U20	51NW9615D27	SN74S32N Quad 2-Input OR Gate
1	U8	51NW9615F85	SN74S38N Quad 2-Input NAND Driver
4	U3,U15,U28, U37	51NW9615C95	SN74S74N Dual D-Flip-Flop
1	U2	51NW9615A03	SN74S132N Quad 2-Input ST NAND Gate
1	U31	51NW9615C99	SN74S157N Quad 2 to 1 Multiplexer
1	U38	51NW9615J90	SN74S158N Quad 2 to 1 Multiplexer
1	U10	51NW9615F79	SN74S240N Octal Inv. Bus Driver TS
1	U17	51NW9615F65	SN74S241N Octal Bus Driver TS
2	U32,U33	51NW9615G56	SN74S373N Octal D-Latch TS
72	at U40-U111	09NW9811A04	16-Pin DIL IC Socket (MVME202)
36	at U40-U75	09NW9811A04	16-Pin DIL IC Socket (MVME222-1)
72	at U40-U111	09NW9811A04	16-Pin DIL IC Socket (MVME222-2)
1	at U5	09NW9811A09	18-Pin DIL IC Socket
5	at P1, Front Panel	03SW993D210	DIN 84 M 2.5*10 Flat Head Screw
5	at P1, Front Panel	02SW990D001	DIN 934 M 2.5 Hexagonal Nut
12		29NW9805B17	Jumper Shorting Insulated
1		84-G8025M01	MVME202/222 Printed Circuit Board
1		64-G4154M01	MVME202 Front Panel (MVME202)
1		64-G4155M01	MVME222 Front Panel (MVME222-1)
1		64-G4155M01	MVME222 Front Panel (MVME222-2)

5.5. ASSEMBLY DRAWING

Figure 5.3 is the assembly drawing of the MVME202/222 Dynamic Memory module.

Figure 5.3: MVME202/222 Assembly Drawing