134-190342-0

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

806-120404-0

MAGNETIC TAPE CONTROL UNIT

STC ADAPTER

CIRCUIT DIAGRAM

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER
MAGNETIC TAPE CONTROL UNIT
CIRCUIT DIAGRAM

134-190342-0

NEC

SHT 1/2

QUIP

DC—405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190342-0

Diagram Number	Diagram Name	Description
134 - 190343	INTRODUCTORY REMARKS OF Circuit Diagram	
134 - 190344 - 001	BACK BOARD Cable Connection diagram.	
134 - 190344 - 002	STC ADAPTER	

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER MAGNETIC TAPE CONTROL UNIT CIRCUIT DIAGRAMS

134-190342-0

NEC

SHT 2/2

QUIP

DC-405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190343-0

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	

1. Constitution

The circuit diagram collection of this MTA911 magnetic tape processing units consists of diagrams as follows .

(1) Example of magnetic tape processing unit circuit diagram indicates a reading method of a circuit diagram.

(2) Connection diagram of magnetic tape processing unit cable.

(3) Logic circuit diagram of magnetic tape processing unit.

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	57.4.19

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

NEC SHT 1/23

QUIP

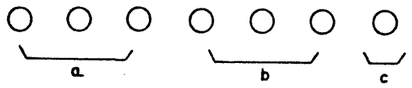
REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	

2. Reading of Logic Circuit Diagram

2.1 Attachment of logical tags

Logical tags of signals between PKGs

The logical tag is expressed with 7 alphanumeric characters and indicates a connection relation between PKGs.



a : displays a function block which sends out signals or displays an interface between devices

b : A functional display of a signal

c : A display of polarity of a signal

The details of the C part

True signal	1: 3. 5. 7. 9. B. D. F. H. J. L. N P. R. T. V X. Z
Complement signal	0. 2. 4 6. 8. A. C. E. G. I. K. M 0. Q. S. U. W. Y

2.2 Attachemnt of the name of a special signal.

XNU : Displays that a signal is not inputted to an input terminal and displays that no signal is emitted to any output terminal.

XOOO : Always displays a logical value "0".

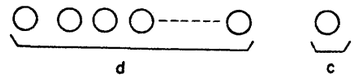
X100 : 00 is displayed with numerical characters and displays a logical value "1".

XGOO : Displays a power source terminal ground.

XP05 : Displays a positive votage (+5V) of the power source terminal.

2.3 Attachment of connector tags

A connector tag displays the connection relation among PKGs by means of optional numerical characters and together with this, it displays the function and a polarity of a signal.



d : Displays the function of a signal

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

NEC SHT 2/23

EQUIP

DC—405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

2.4. Package position of PKG

1) When MTA160P is connected.

IF2
IF1 G9QYS PKG
FCT
DCT
GCW
PEG
NRG
RDL
ECT
GRF
DSB
PLS
PLS
PLS

2) When MTA110P is connected.

FMT
IF2
IF1 G9QYS PKG

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

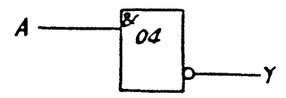
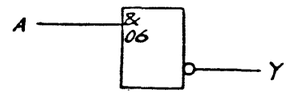
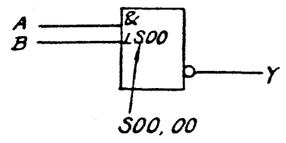
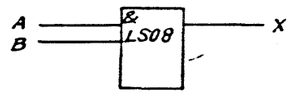
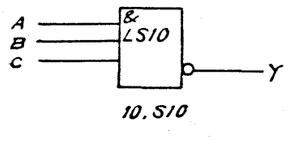
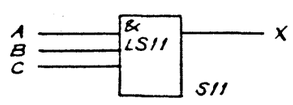
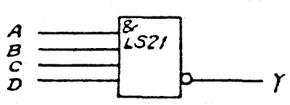
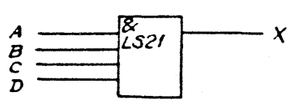
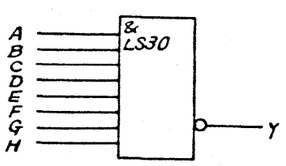
STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

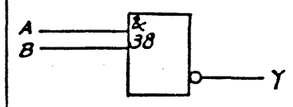
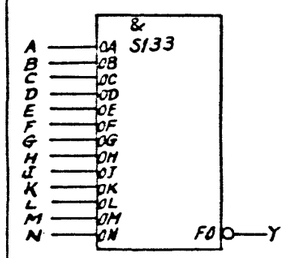
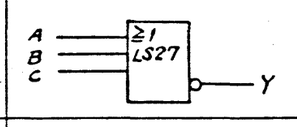
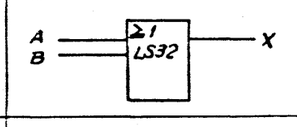
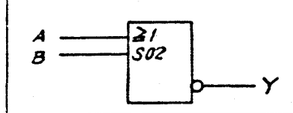
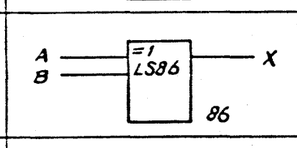
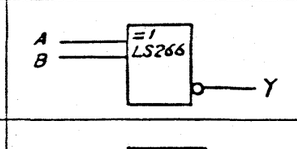
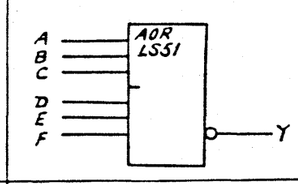
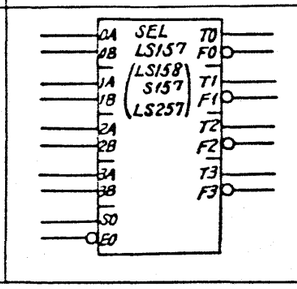
134-190343-0

NEC

EQUIP

2.5 List of used ICs

Type Logic	Name IC	Symbol	Function
&	LS04 04 H04 S04		HEX INVERTER $\overline{Y} = A$
	06		HEX INVERTER BUFFER (O/C) $Y = \overline{A}$
	LS00 00 S00		QUAD 2-NAND GATE $\overline{Y} = A \cdot B$
	LS08 08 S08		QUAD 2-AND GATE $X = A \cdot B$
	LS10 10 S10		TRIPLE 3-NAND GATE $\overline{Y} = A \cdot B \cdot C$
	LS11 S11		TRIPLE 3-AND GATE $X = A \cdot B \cdot C$
	LS20		DUAL 4-NAND GATE $\overline{Y} = A \cdot B \cdot C \cdot D$
	LS21		DUAL 4-AND GATE $X = A \cdot B \cdot C \cdot D$
	LS30		SINGLE 8-NAND GATE $\overline{Y} = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$

Type Logic	Name IC	Symbol	Function
&	38		QUAD 2-NAND BUFFER (O/C) $\overline{Y} = A \cdot B$
	S133		13-INPUT NAND GATE $\overline{Y} = A \cdot B \cdot \cdots \cdot M \cdot N$
≧1	LS27		TRIPLE 3-NOR GATE $\overline{Y} = A + B + C$
	LS32		QUAD 2-OR GATE $X = A + B$
	S02		QUAD 2-NOR GATE $\overline{Y} = A + B$
=1	LS86 86		QUAD EXCLUSIVE OR GATE $X = A \oplus B$
	LS266		QUAD 2-EXCLUSIVE NOR GATE $\overline{Y} = A \oplus B$
AOR	LS51 51 S51		DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE $\overline{Y} = A \cdot B \cdot C + D \cdot E \cdot F$ Or. $\overline{Y} = B \cdot C + E \cdot F$
SEL	LS157 S157 LS257 LS158		 1 Fnis in case of LS158. 2 LS257 is the 3-state output.

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

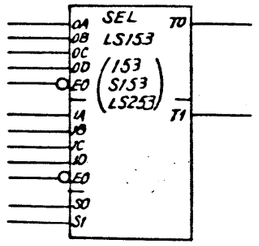
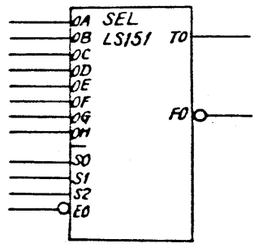
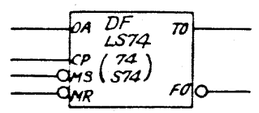
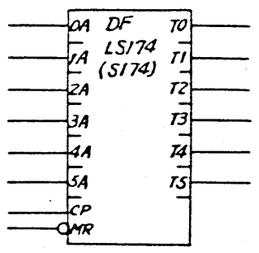
NEC

SHT 4/23

DC—405
JIS A3 (297×420)

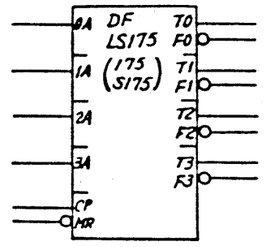
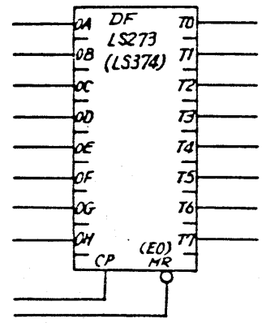
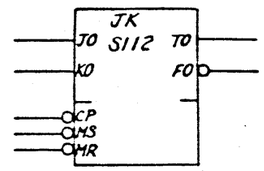
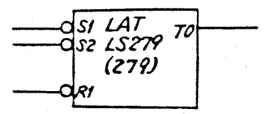
Nippon Electric Co.,Ltd.

134-190343-0

Type Logic	Name IC	Symbol	Function
SEL	LS153 153 S153 LS253		DUAL 4-INPUT MULTIPLEXER LS253 3-
	LS151		8-INPUT MULTIPLEXER
DF	LS74 74 S74		DUAL D-TYPE FLIP-FLOP
	LS174 S174		HEX D-TYPE FLIP-FLOP

0A	CP	MS	MR	T0	F0
X	X	1	0	0	1
X	X	0	1	1	0
0	↑	1	1	0	1
1	↑	1	1	1	0
X	0	1	1	HOLD	$\overline{T0}$
X	1	1	1	HOLD	$\overline{T0}$
X	X	0	0	1	1

nA	CP	MR	Tn
X	X	0	0
0	↑	1	0
1	↑	1	1
X	0	1	HOLD
X	1	1	HOLD

Type Logic	Name IC	Symbol	Function
DF	LS175 175 S175		QUAD D-TYPE FLIP-FLOP
	LS273 LS374		OCTAL D-TYPE FLIP-FLOP LS374は3-ステート出力(E0)
JK	S112		DUAL J-K EDGE TRIGGERED FLIP-FLOP
LAT	LS279 279		QUAD S-R LATCH

On	CP	MR(E0)	Tn
X	X	0	0
		1	3-State
0	↑	1	0
1	↑	1	1
X	0	1	HOLD
X	1	1	HOLD

MS	MR	CP	J0	K0	T0	F0
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	↓	0	0	Q_0	$\overline{Q_0}$
1	1	↓	1	0	1	0
1	1	↓	0	1	0	1
1	1	↓	1	1	TOG	GLE
1	1	1	X	X	Q_0	$\overline{Q_0}$

S1 - S2	R1	T0
0	0	1
0	1	1
1	0	0
1	1	HOLD

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 吉木		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

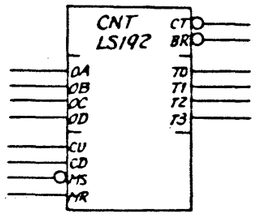
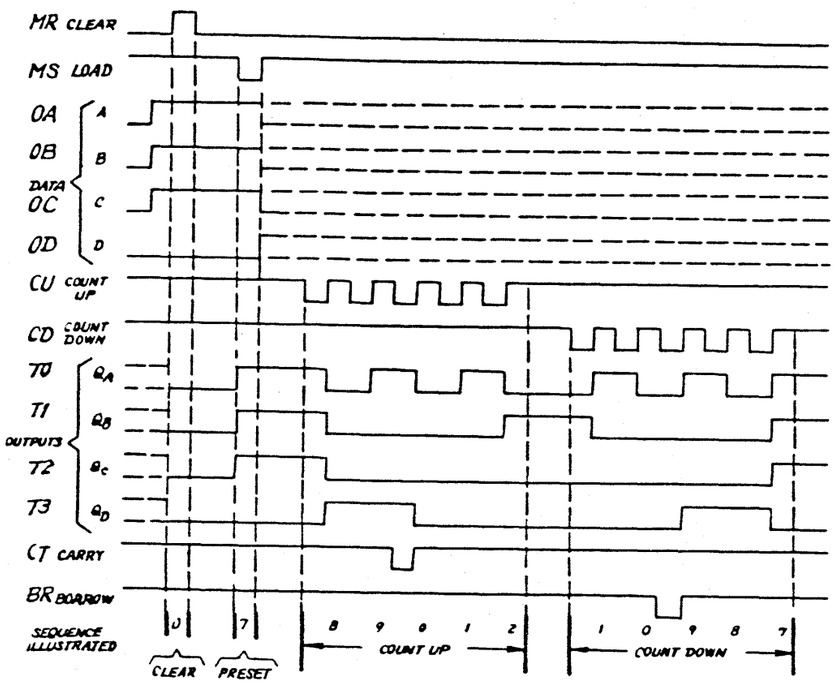
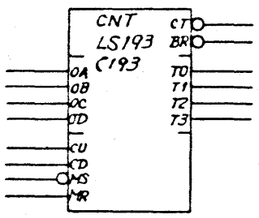
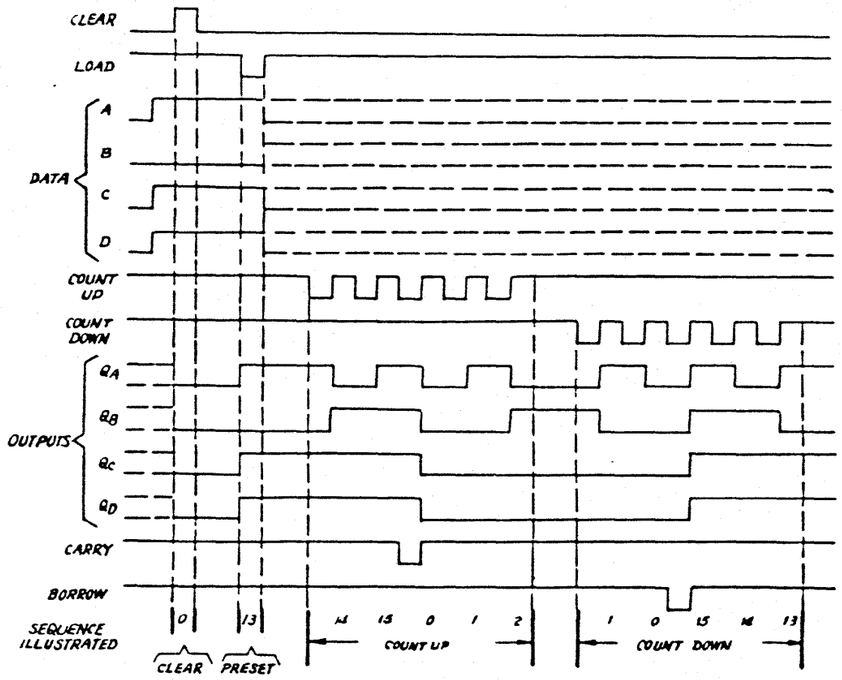
134-190343-0

NEC SHT 5/23

DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190343-0

Type Logic	Name IC	Symbol	Function
CNT	LS192		UP/DOWN BCD COUNTER 
	LS193 193		UP/DOWN BINARY COUNTER 

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

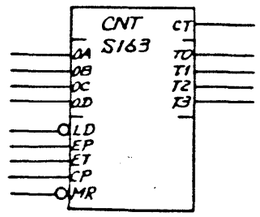
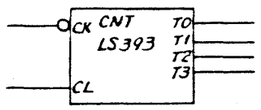
134-190343-0

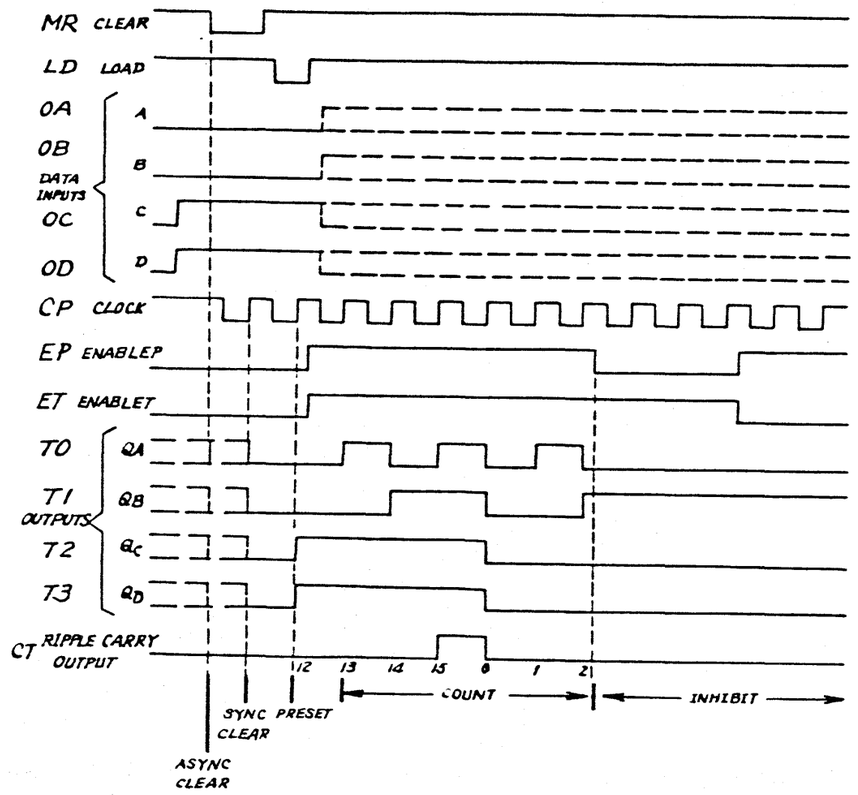
NEC

SHT 6/23

Nippon Electric Co.,Ltd.

DC-405
JIS A3 (297×420)

Type Logic	Name IC	Symbol	Function
CNT	S163		SYNCHRONOUS 4-BIT COUNTERS
	LS393 393		DUAL 4-BIT BINARY COUNTER



COUNT	T0	T1	T2	T3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 日本		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

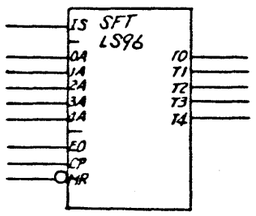
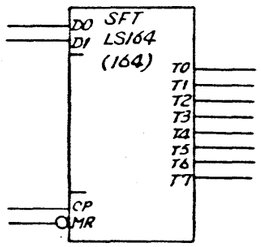
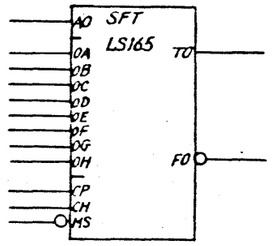
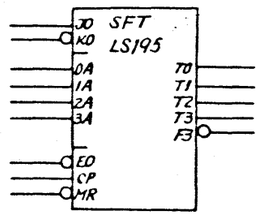
NEC

SHT 7/23

DC—405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190343-0

Type Logic	Name IC	Symbol	Function
SFT	LS96		5-BIT SHIFT REGISTER
	LS164 164		8-BIT SHIFT REGISTER SERIAL IN/PARALLEL OUT
	LS165		PARALLEL LOAD 8 BIT SHIFT REGISTER
	LS195		4-BIT SHIFT REGISTER

5-BIT SHIFT REGISTER

MR	E0	0A	1A	2A	3A	4A	CP	IS	T0	T1	T2	T3	T4
0	0	X	X	X	X	X	X	X	0	0	0	0	0
0	X	0	0	0	0	0	X	X	0	0	0	0	0
1	1	1	1	1	1	1	X	X	1	1	1	1	1
1	1	0	0	0	0	0	L	X	0A0	1A0	2A0	3A0	4A0
1	1	1	0	1	0	1	L	X	1	1A0	1	3A0	1
1	0	X	X	X	X	X	L	X	0A0	1A0	2A0	3A0	4A0
1	0	X	X	X	X	X	↑	1	1	0An	1A0	2An	3An
1	0	X	X	X	X	X	↑	0	0	0An	1An	2An	3An

8-BIT SHIFT REGISTER SERIAL IN/PARALLEL OUT

MR	CP	D0	D1	T0	T1	T2	T3	T4	T5	T6	T7
0	X	X	X	0	0	0	0	0	0	0	0
1	1	X	X	T0₀	T1₀	T2₀	T3₀	T4₀	T5₀	T6₀	T7₀
1	↑	1	1	1	T0n	T1n	T2n	T3n	T4n	T5n	T6n
1	↑	0	X	0	T0n	T1n	T2n	T3n	T4n	T5n	T6n
1	↑	X	0	0	T0n	T1n	T2n	T3n	T4n	T5n	T6n

PARALLEL LOAD 8 BIT SHIFT REGISTER

MS	CH	CP	A0	0A------0H	INTERNAL QA	INTERNAL QB	TO	FO
0	X	X	X	a-------h	a	b	h	$\bar{h}$
1	0	0	X	X	Q_{A0}	Q_{B0}	Q_{H0}	$\bar{Q}_{H0}$
1	0	↑	1	X	1	Q_{An}	Q_{Gn}	$\bar{Q}_{Gn}$
1	0	↑	0	X	0	Q_{An}	Q_{Gn}	$\bar{Q}_{Gn}$
1	1	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}	$\bar{Q}_{Gn}$

4-BIT SHIFT REGISTER

MR	E0	CP	J0	K0	0A	1A	2A	3A	T0	T1	T2	T3	F3
0	X	X	X	X	X	X	X	X	0	0	0	0	1
1	0	↑	X	X	a	b	c	d	a	b	c	d	$\bar{d}$
1	1	0	X	X	X	X	X	X	T0₀	T1₀	T2₀	T3₀	$\overline{T3_0}$
1	1	↑	0	1	X	X	X	X	T0₀	T0₀	T1₀	T2₀	$\overline{T2_0}$
1	1	↑	0	0	X	X	X	X	0	T0n	T1n	T2n	$\overline{T2n}$
1	1	↑	1	1	X	X	X	X	1	T0n	T1n	T2n	$\overline{T2n}$
1	1	↑	1	0	X	X	X	X	$\overline{T0n}$	T0n	T1n	T2n	$\overline{T2n}$

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER
INTRODUCTORY
REMARKS OF
CIRCUIT DIAGRAM

134-190343-0

NEC

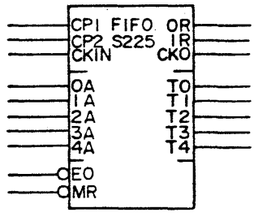
SHT 8/23

134-190343-0

重名

DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

Logic Type	IC Name	Symbol
FIFO	S225	

Description

FIFO BUFFER MEMORY

This circuit is an open-ended high speed buffer memory consisting of 16 words X 5 bits.

The function of each terminal is shown as follows :

Logic Pin Number	Function
0A~4A	5-bit parallel input data.
CP1 CP2	This is a signal to load a parallel data. A data is stored at the inside of a memory array by means of the leading edge of this signal.
CKIN	A signal which is used when a data is read out of the inside of a memory; and the deta is read from the array by means of the trailing edge(arise) of this signal.
EO	A signal to control an output data. When "0", a permissible state is made to enable an output.
MR	Clears FIFO.
T0~T4	A 5 bit parallel output data.
IR	A signal indicating that a write of data is feasible into FIFO. This signal checks the state of the last word of a memory within FIFO and when data is written in all of 16 words, this signal becomes "0".
OR	A signal indicating a state wherein a data can be read out of FIFO. The signal is turned "1" when a data is written in the initial word of the memory within FIFO. But at this time, CP1 and CP2 shall be "1." Accordingly, when the initial word is empty, this signal is "0".

Logic pin Number	Function
CKO	Unload clock output. When CP1 and CP2 are "1" and data is written in the last word, a pulse is output from CKO.

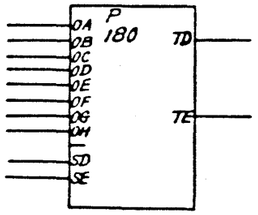
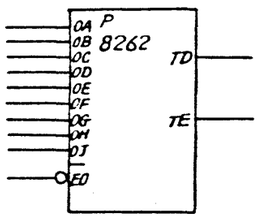
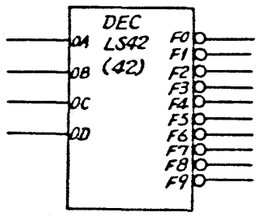
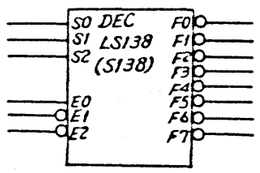
REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

STC-ADAPTER
INTRODUCTORY
REMARKS OF
CIRCUIT DIAGRAM

134-190343-0

NEC

Type Logic	NumberIC	Symbol	Function
P	180		8-BIT PARITY GENERATOR/CHECKER
	8262		9-BIT PARITY GENERATER/CHECKER
DEC	LS42 42		1-OF-10 DECODER
	LS138 S138		3-OF-8 DECODER

8-BIT PARITY GENERATOR/CHECKER

0A ~ 0H	SE	SD	TE	TD
The number of "1" input is even.	1	0	1	0
The number of "1" input is odd.	1	0	0	1
The number of "1" input is even.	0	1	0	1
The number of "1" input is odd.	0	1	1	0
X	1	1	0	0
X	0	0	1	1

9-BIT PARITY GENERATER/CHECKER

0A ~ 0J	E0	TD	TE
The number of "1" input is even.	0	0	1
The number of "1" input is odd.	0	1	0
X	1	0	0

1-OF-10 DECODER

0A	0B	0C	0D	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

3-OF-8 DECODER

E0	E1,E2	S0	S1	S2	F0	F1	F2	F3	F4	F5	F6	F7
X	1	X	X	X	1	1	1	1	1	1	1	1
0	X	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口 音木		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

NEC

SHT 10/23

DC—405
JIS A3 (297×420)

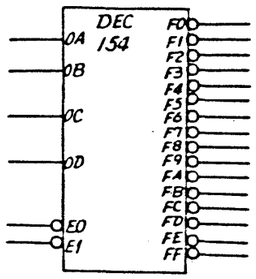
Nippon Electric Co.,Ltd.

0-134-190343-0

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

Type Logic	Name IC	Symbol	Function

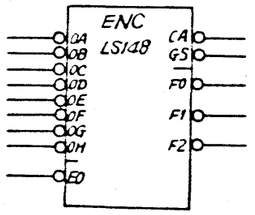
DEC 154



1-OF-16 DECODER

E0	E1	0A	0B	0C	0D	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

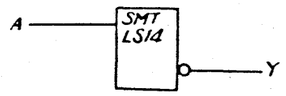
ENC LS148



8-LINE TO 3-LINE OCTAL PRIORITY ENCODER

E0	0A	0B	0C	0D	0E	0F	0G	0H	F0	F1	F2	GS	C0
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	X	X	X	X	X	X	X	0	0	0	0	0	1
0	X	X	X	X	X	X	0	1	0	0	1	0	1
0	X	X	X	X	X	0	1	1	0	1	0	0	1
0	X	X	X	X	0	1	1	1	0	1	1	0	1
0	X	X	X	0	1	1	1	1	1	0	0	0	1
0	X	X	0	1	1	1	1	1	1	0	1	0	1
0	X	0	1	1	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1

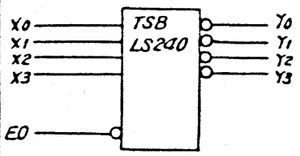
SMT LS14



HEX SCHMIT TRIGGER

$\overline{Y} = A$

TSB LS240



OCTAL BUFFERS/LINE DRIVERS/ UNE RECIVER (3-STATE)

X_n	E_0	Y_n
Y_n	0	$\overline{X_n}$
X	1	3 STATE

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

STC-ADAPTER
INTRODUCTORY
REMARKS OF
CIRCUIT DIAGRAM

134-190343-0

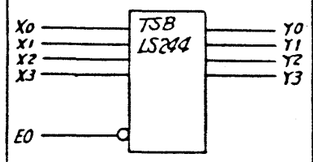
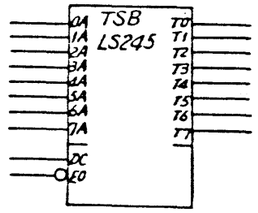
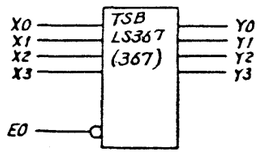
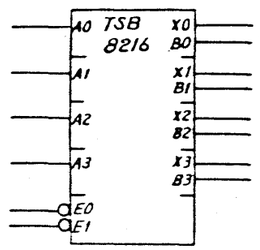
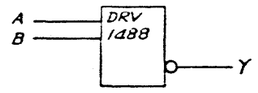
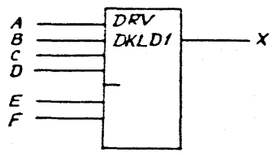
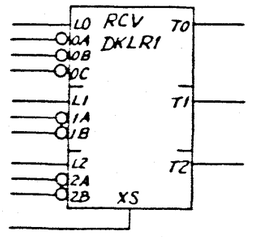
NEC

SHT 11/23

装置名

DC—405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

Type Logic	Name IC	Symbol	Function
TSB	LS244		OCTAL BUFFERS/LINE DRIVER/LINE RECEIVER (3-STATE) Xn | EO | Yn. Xn | 0 | Xn X | 1 | 3 STATE
	LS245		OCTAL BUFFERS TRANCEIVERS (3-STATE) EO | DC | OPERATION 0 | 0 | nA ← Tn 0 | 1 | nA → Tn 1 | X | 3 STATE
	LS367 367		HEX BUFFERS 3-STATE 4 BITS & 2 BITS Xn | EO | Yn Xn | 0 | Xn X | 1 | 3
	8216		4 BIT TRANCEIVER (3-STATE) EO | E1 | OPERATION 0 | 0 | A → X 1 | 0 | X → B 0 | 1 | 3 STATE 1 | 1 | 3 STATE
DRV	1488		QUAD LINE DRIVER $\overline{Y} = A \cdot B$
	DKLD1 (B263)		DUAL LINE DRIVER $X = A \cdot B \cdot C \cdot D + E \cdot F$
RCV	DKLR1 (B261)		TRIPLE LINE RECEIVER $T0 = XS(L0.0A + 0B \cdot 0C)$

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 晋本		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

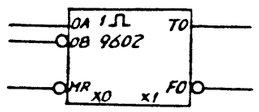
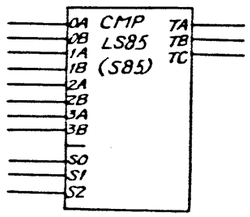
NEC

SHT 12/23

134-190343-0

DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

Type Logic	Name IC	Symbol	Function
1 ⎍	9602		DUAL RETRIGGERABLE ONE SHOT
CMP	LS85 S85		4 BIT MAGNITUDE COMPARATOR

OA	OB	MR	TO	FO
0	↓	1	⎍	⎍
↑	1	1	⎍	⎍
X	X	0	0	1

0A 0B	1A 1B	2A 2B	3A 3B	S0	S2	S1	TA	TC	TB
0A>0B	X	X	X	X	X	X	1	0	0
0A<0B	X	X	X	X	X	X	0	1	0
0A=0B	1A>1B	X	X	X	X	X	1	0	0
0A=0B	1A<1B	X	X	X	X	X	0	1	0
0A=0B	1A=1B	2A>2B	X	X	X	X	1	0	0
0A=0B	1A=1B	2A<2B	X	X	X	X	0	1	0
0A=0B	1A=1B	2A=2B	3A>3B	X	X	X	1	0	0
0A=0B	1A=1B	2A=2B	3A<3B	X	X	X	0	1	0
0A=0B	1A=1B	2A=2B	3A=3B	1	0	0	1	0	0
0A=0B	1A=1B	2A=2B	3A=3B	0	1	0	0	1	0
0A=0B	1A=1B	2A=2B	3A=3B	0	0	1	0	0	1
0A=0B	1A=1B	2A=2B	3A=3B	X	X	1	0	0	1
0A=0B	1A=1B	2A=2B	3A=3B	1	1	0	0	0	0
0A=0B	1A=1B	2A=2B	3A=3B	0	0	0	1	1	0

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

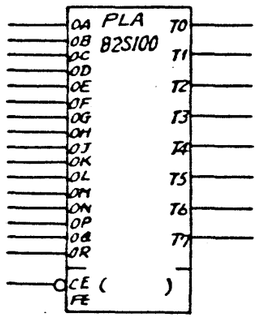
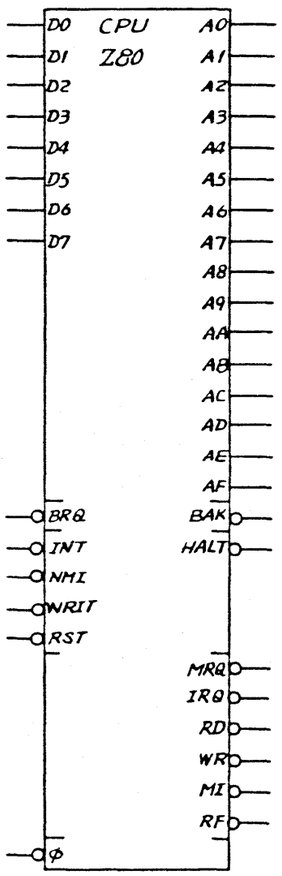
NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER
INTRODUCTORY
REMARKS OF
CIRCUIT DIAGRAM

134-190343-0

NEC SHT 13/23

Type Logic	Name IC	Symbol	Function
PLA	82S100		FIELD PROGRAMABLE LOGIC ARRAY. 1 This is a logic array of AND-OR gate having a 16 bit input-and a 8 bit output, and is constitueut of programs. The operation is shown according to each truth table.
CPU	D780C-1		8·BIT CPU

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 哲夫		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

NEC

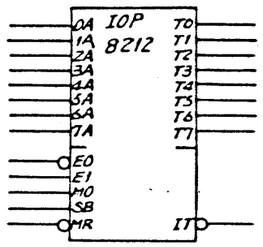
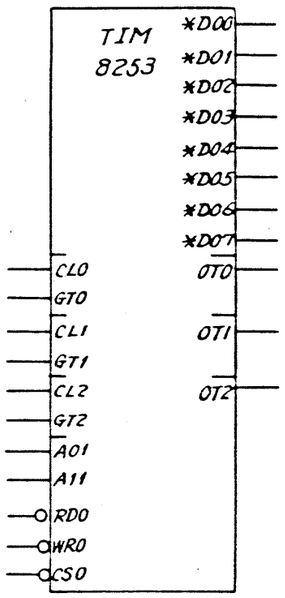
SHT 14/23

134-190343-0

装置名

DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

Type Logic	Name IC	Symbol	Function
IOP	8212		8-BIT I/O PORT
TIM	8253		PROGRAMMABLE INTERVAL TIMER

MR	SB	M0	E0·E1	State of T0~T7
X	X	0	0	High impedance
1	X	1	0	Output(=data.latch)
1	0	0	1	Output(=data.latch)
0	X	1	0	Output(="0" rest)
0	0	0	1	Output(="0" rest)
X	1	0	1	Output(=data input)
X	X	1	1	Output(=data input)

MR	E0·E1	SB	*SR	IT
0	0	X	1	1
0	1	X	1	0
1	1	X	1	0
1	↘	0	1	1
1	0	0	HOLD	HOLD
1	0	1	HOLD	HOLD
1	0	↘	0	0

* SR : Internal SR flip flop (Q)

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

NEC

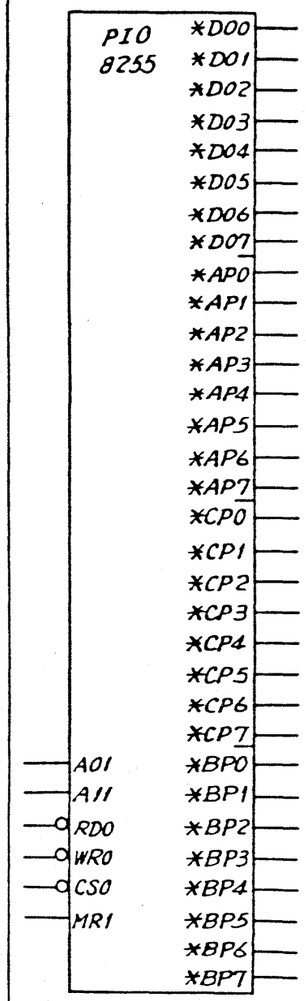
SHT 15/23

134-190343-0

置名

DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

Type Logic	Name IC	Symbol	Function
PIO	8255		PROGRAMMABLE I/O PORT

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

STC-ADAPTER
INTRODUCTORY
REMARKS OF
CIRCUIT DIAGRAM

134-190343-0

NEC

SHT 16/23

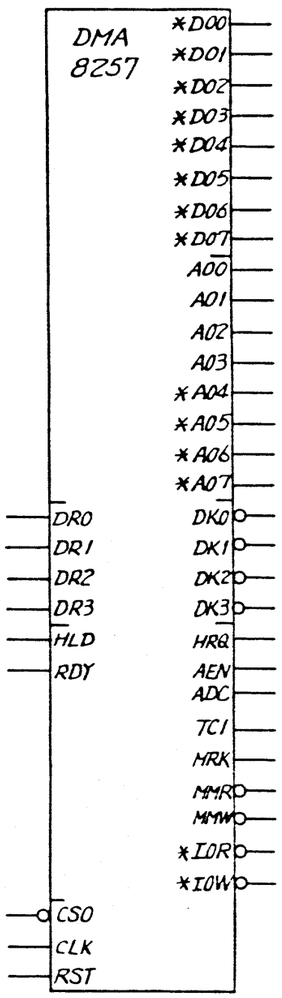
134-190343-0

署名

DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190343-0

Type Logic	Name IC	Symbol	Function
DMA	8257		PROGRAMMABLE DMA CONTROLLER

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

STC-ADAPTER
INTRODUCTORY
REMARKS OF
CIRCUIT DIAGRAM

134-190343-0

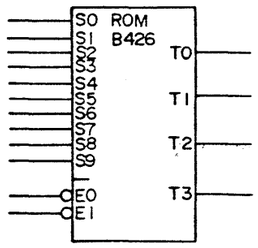
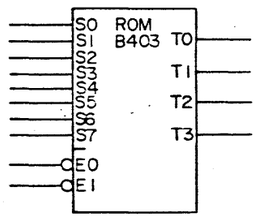
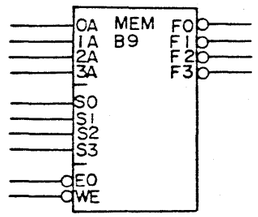
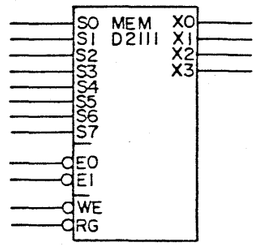
NEC

SHT 17/23

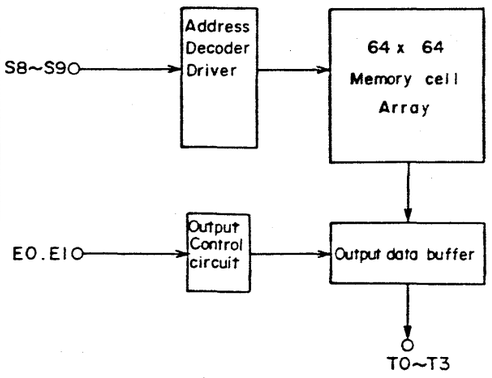
DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

Logic Type	IC Name	Symbol	Function
ROM	B426		1024W X 4B PROM (3-STATE)
	B403		256W X 4B PROM
MEM	89		16W X 4B RAM
	D2111		256W X 4B STATIC MOS RAM

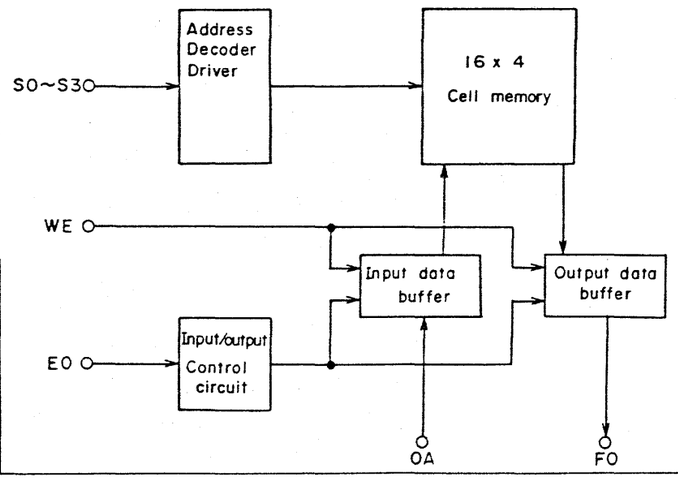
E0	E1	T0 ~ T3
0	0	Volues selected from the values stored in this circuit by means of S0~S9.
1	0	Being placed in a 3 state condition.
0	1	
1	1	



E0	E1	T0 ~ T3
0	0	Content of address selected by means of S0 ~ S7
1	0	Non selection : 1
0	1	
1	1	

Block diagram is same as that of B426

E	WE	A	Operation	Output T
0	0	0	Write	1
0	0	1	Write	0
0	1	X	Read	Correction of selected address content
1	0	X	Non selection	Non decision
1	1	X		1



EO	EI	RG	Chip	Output state
0	0	0	Selec-tion	Data output
0	0	1		High impedance
Other than the above-mentioned			Non selection	

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

NEC

SHT 18/23

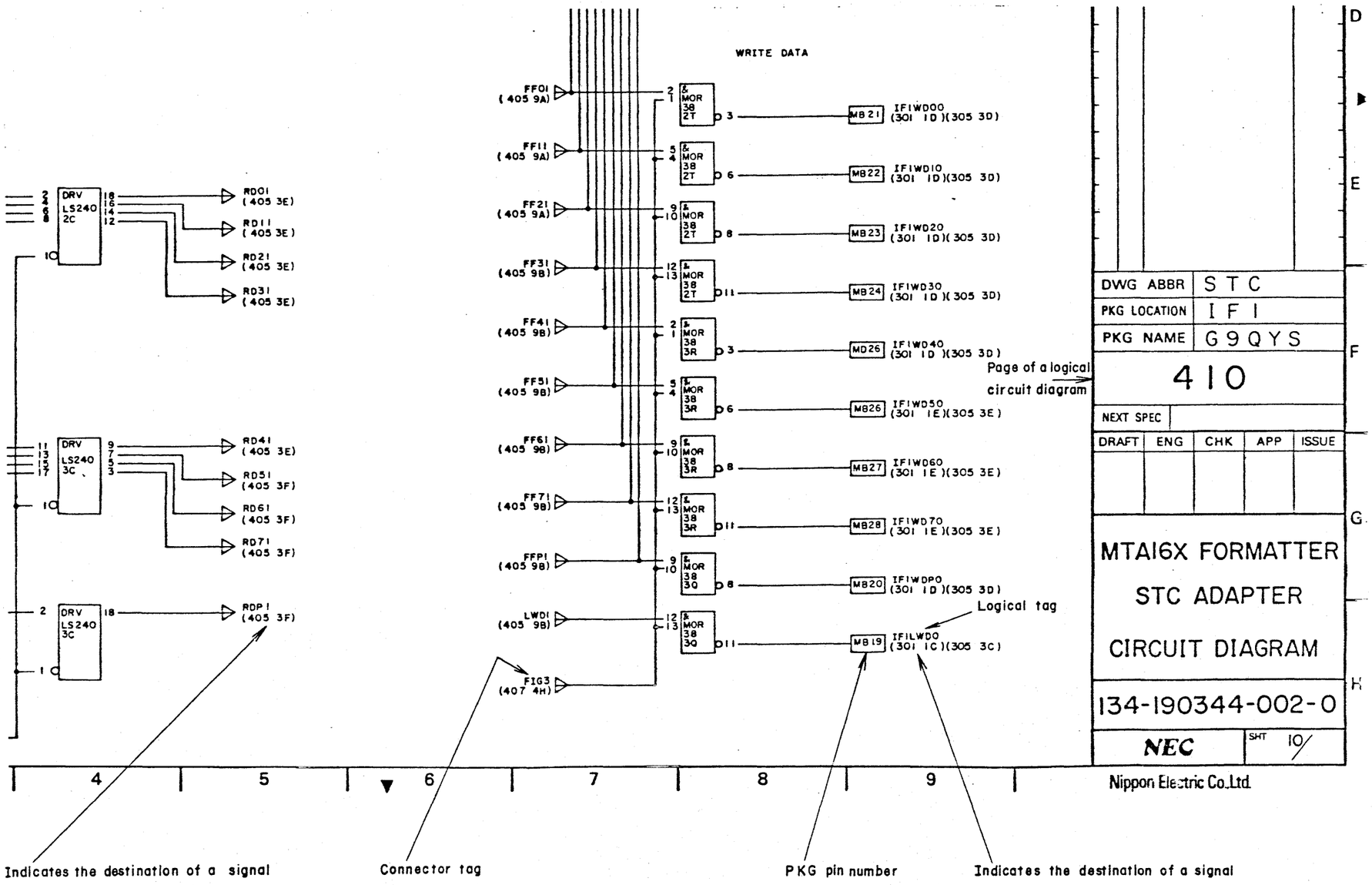
QUIP

DC-405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190343-0

Legend of Logical Circuit Diagram



DWG ABBR	STC
PKG LOCATION	IF1
PKG NAME	G9QYS
	410
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE

MTAI6X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

NEC SHT 10/

Nippon Electric Co.,Ltd.

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER INTRODUCTORY REMARKS OF CIRCUIT DIAGRAM

134-190343-0

NEC SHT 19/23

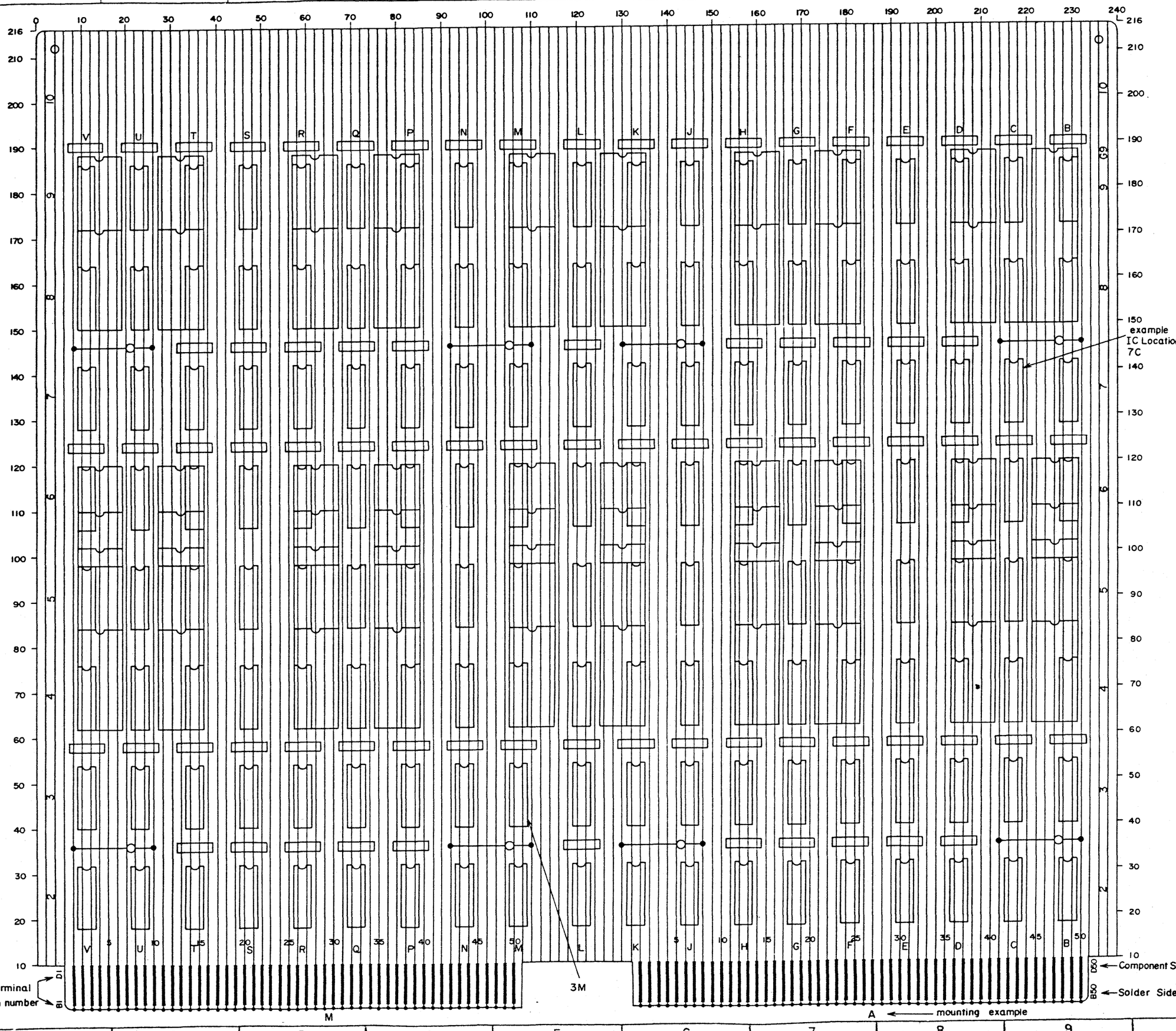
EQUIP

DC—405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190343-0

REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.2.20	—



DWG ABBR	
PKG LOCATION	
PKG NAME	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
山本			井	

STC-ADAPTER

INTRODUCTORY REMARKS

OF CIRCUIT DIAGRAM

134-190343-0

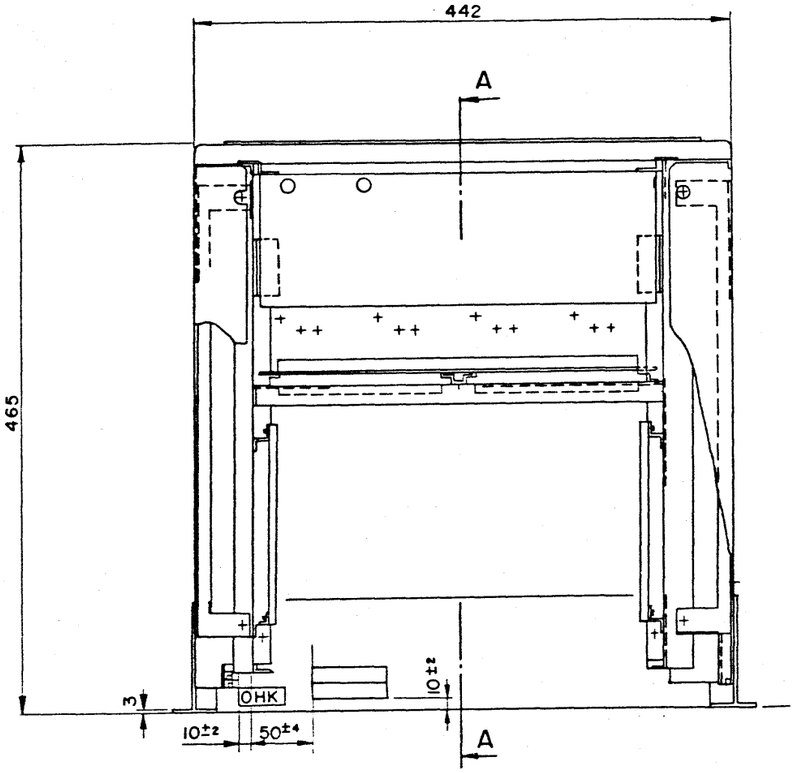
NEC | SHT 20/23

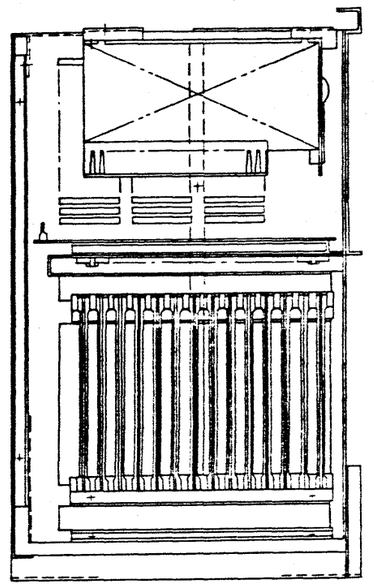
Nippon Electric Co.,Ltd

DB-4135
A2 (420x594)

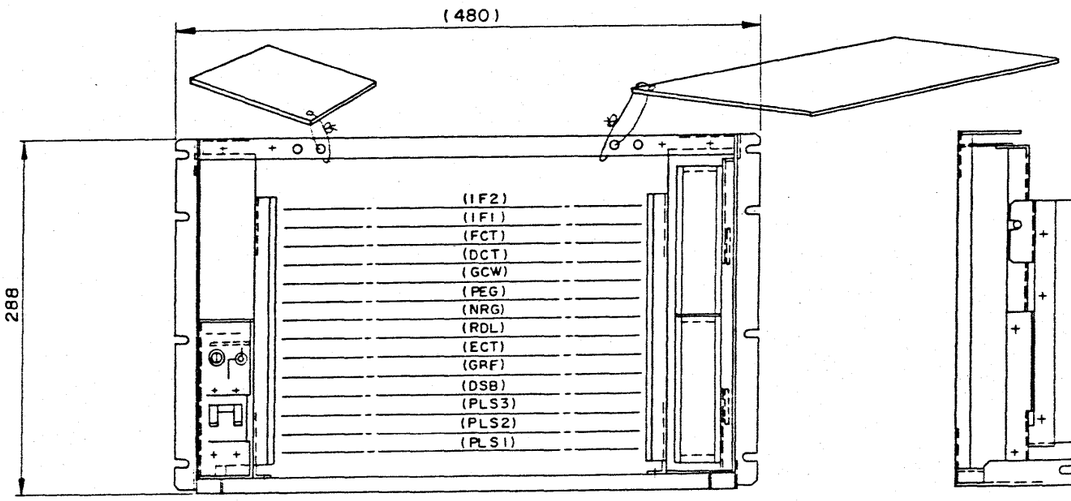
134-190343-0

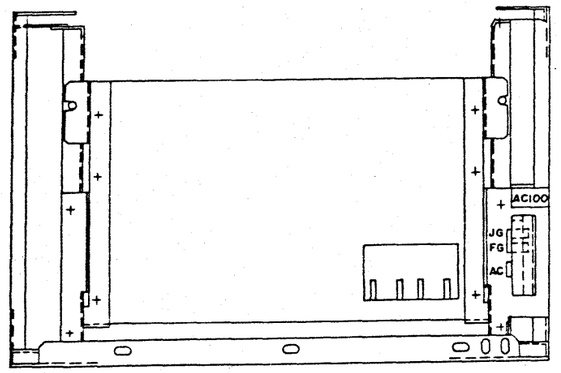
REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——





SECTION A - A





REAR VIEW

STRUCTURE DIAGRAM (MTA160P CONNECTION

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC-ADAPTER
INTRODUCTORY REMARKS
OF CIRCUIT DIAGRAM

134-190343-0

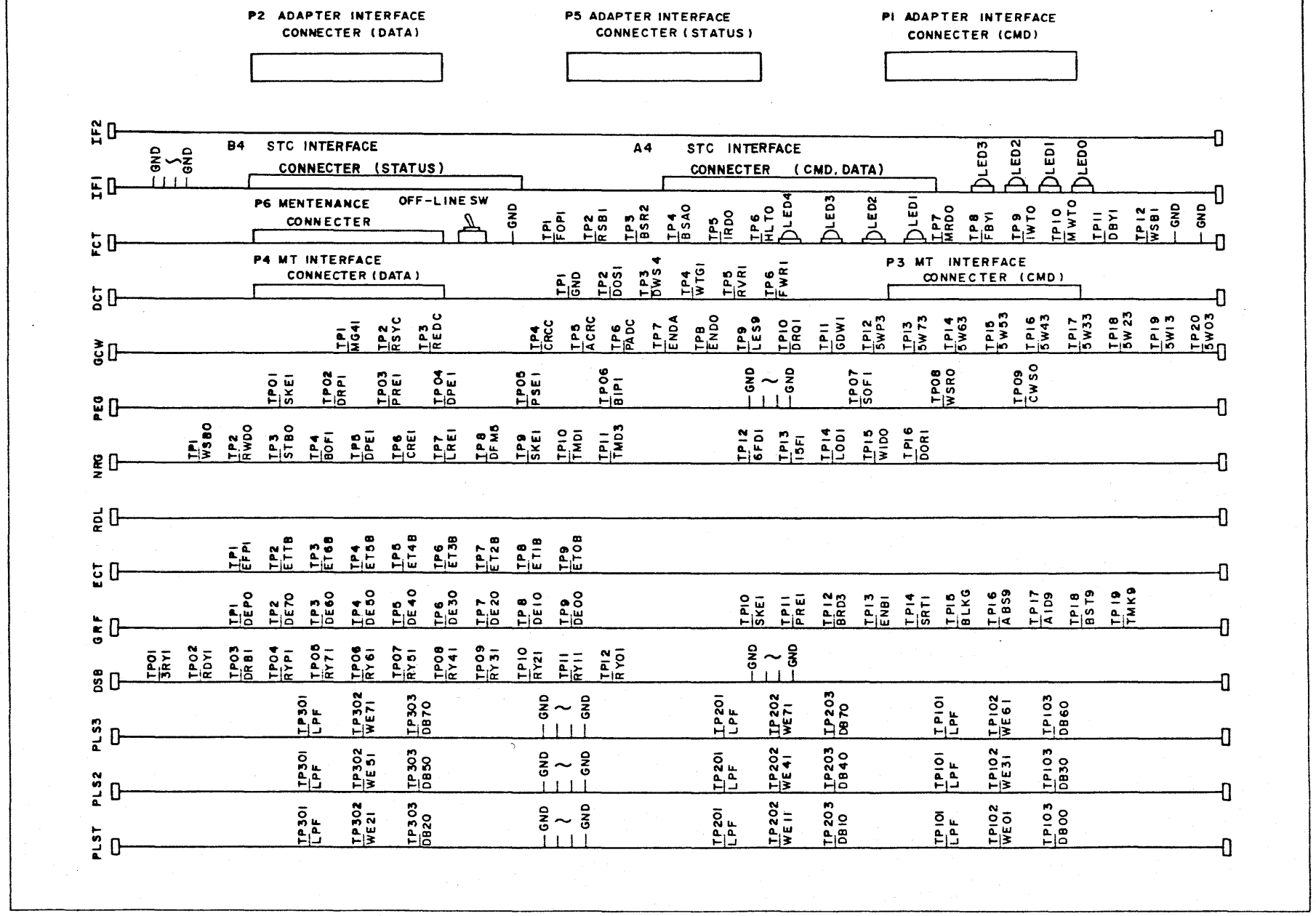
NEC SHT 21/23

EQUIP

DC-405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	—



DWG ABBR	
PKG LOCATION	
PKG NAME	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
山口			今村	

STC-ADAPTER
INTRODUCTORY REMARKS
OF CIRCUIT DIAGRAM

134-190343-0

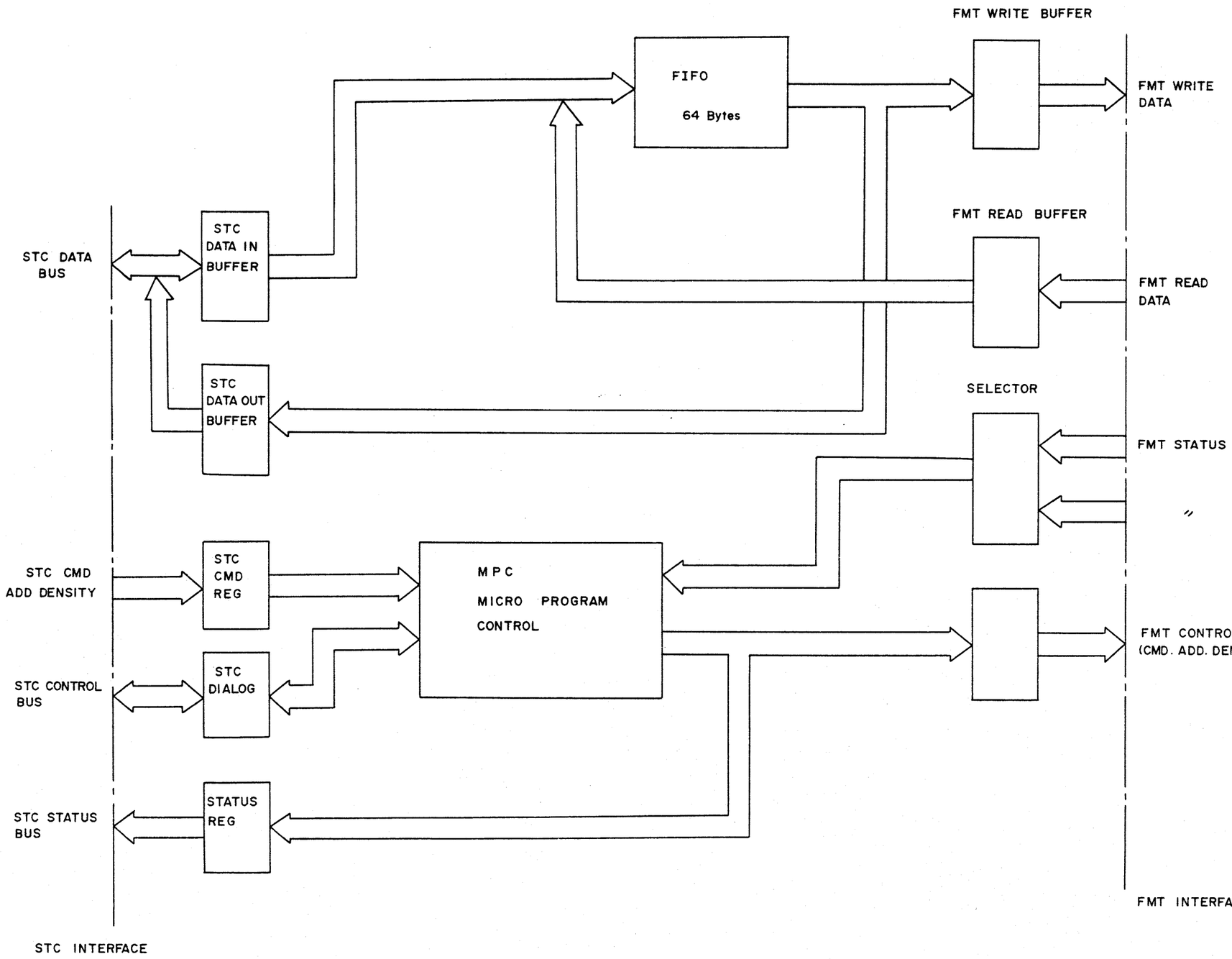
NEC SHT 22/23

Nippon Electric Co.Ltd.

EQUIP

DB-4136
JIS A2 (420×594)

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——



STCA BLOCK DIAGRAM

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木			

STC-ADAPTER
INTRODUCTORY REMARKS
OF CIRCUIT DIAGRAM

134-190343-0

NEC

SHT 23/23

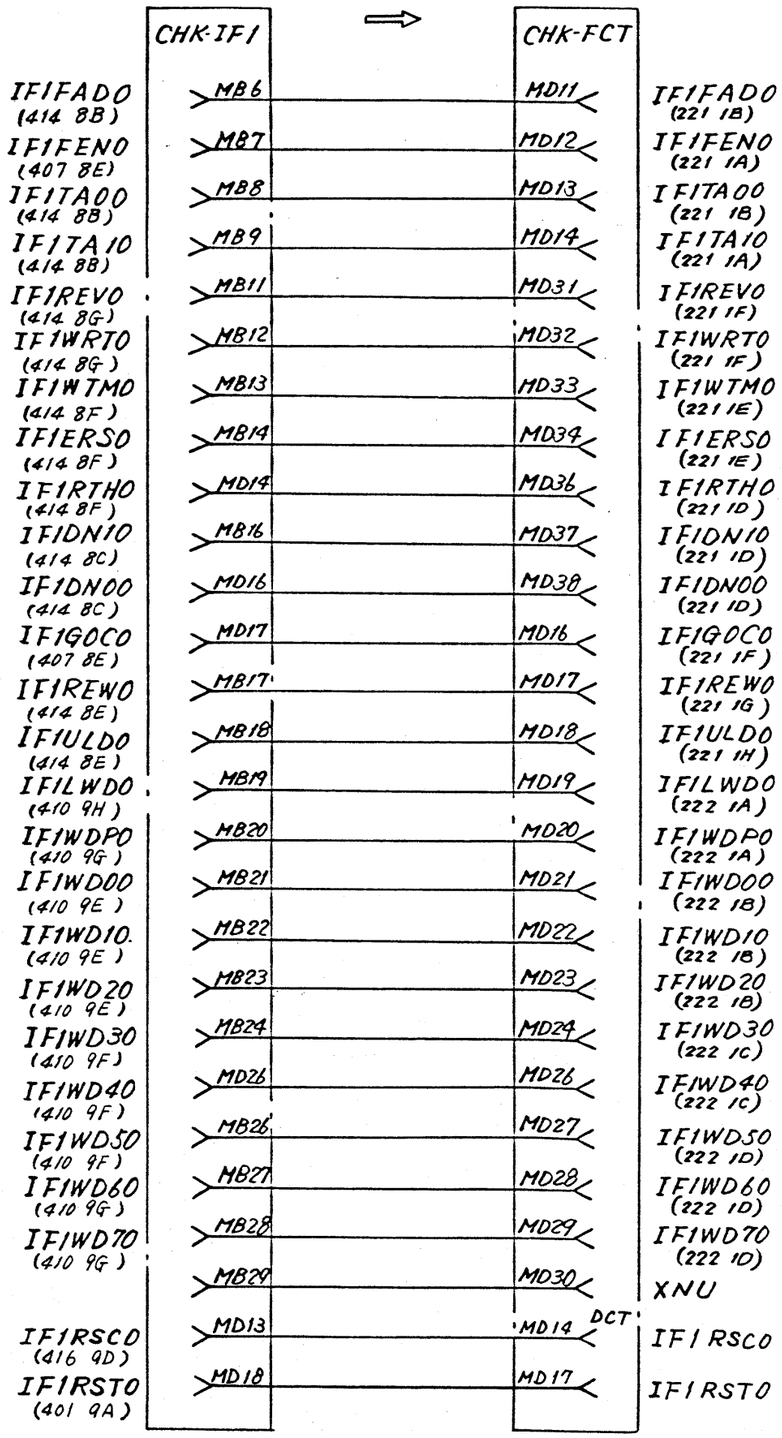
QUIP

DC-405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190344-001-0

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982. 2. 20	
2	0	1982. 11. 22 SC-414076	



301

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 音木		今村	

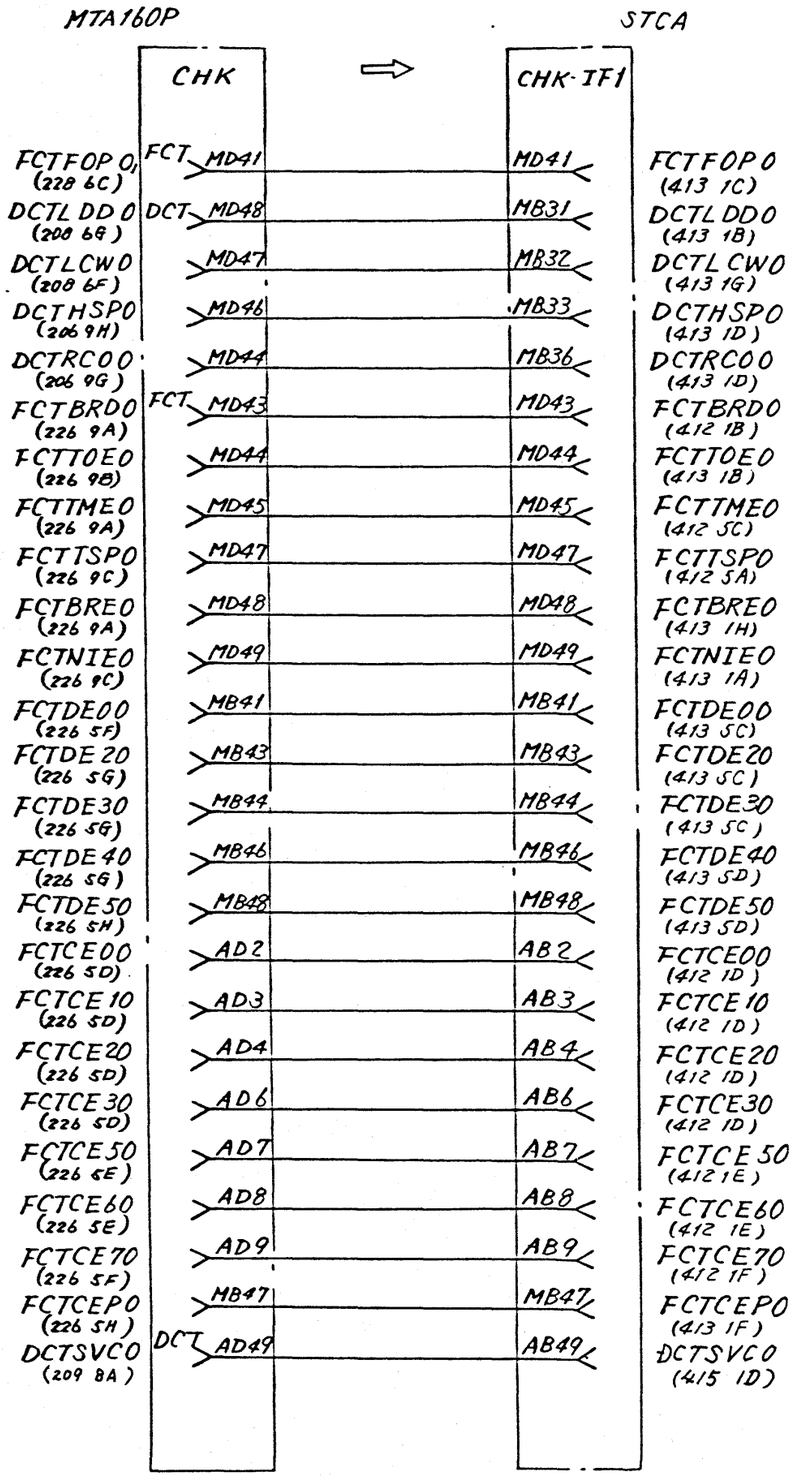
STC ADAPTER CONNECTION DIAGRAM OF BACK BOARD

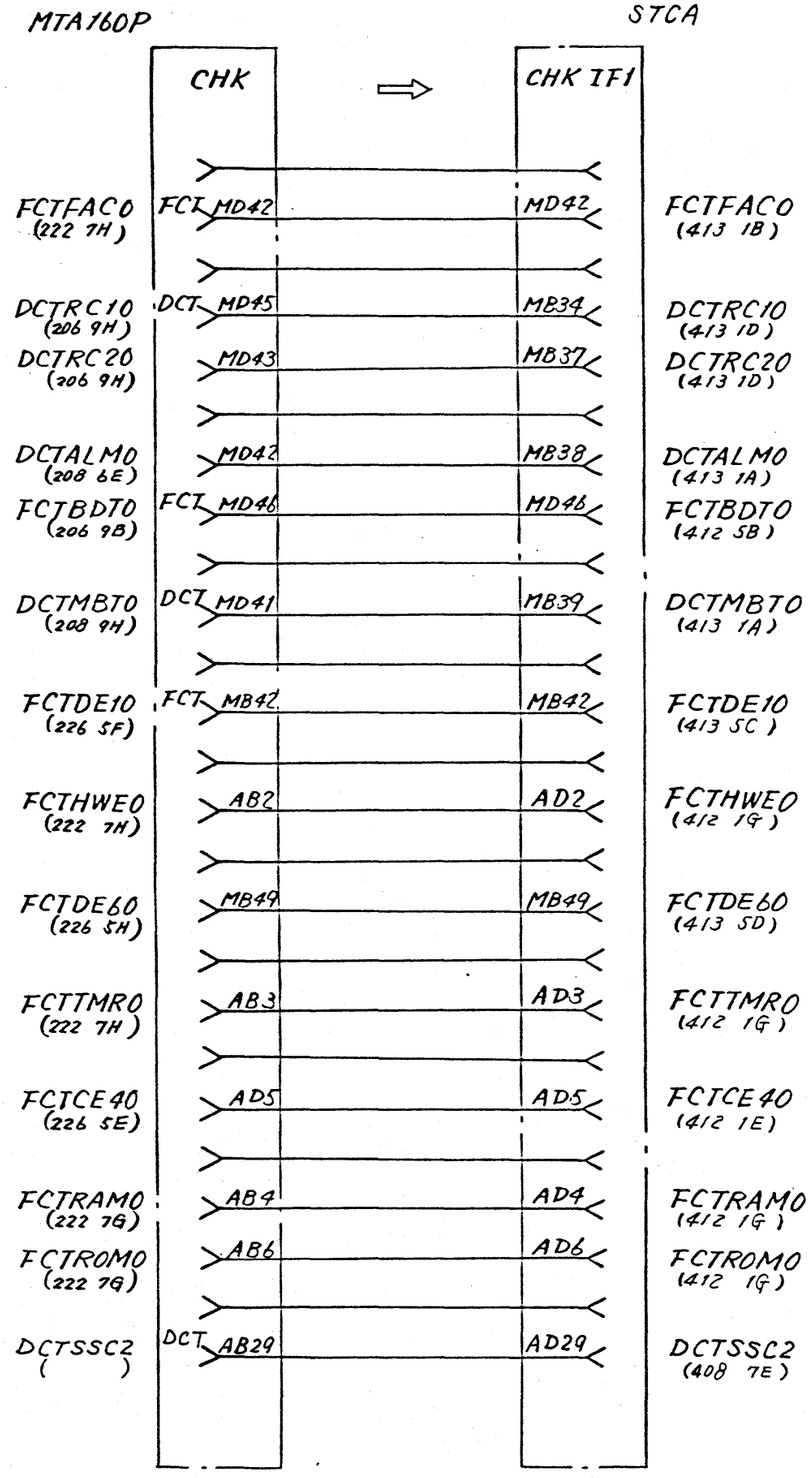
134-190344-001-0

NEC SHT 1/6

署名

134-190344-001-0





REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——
2	0	1982.11.22	山口

302

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC ADAPTER CONNECTION DIAGRAM OF BACK BOARD

134-190344-001-0

NEC

SHT 2/6

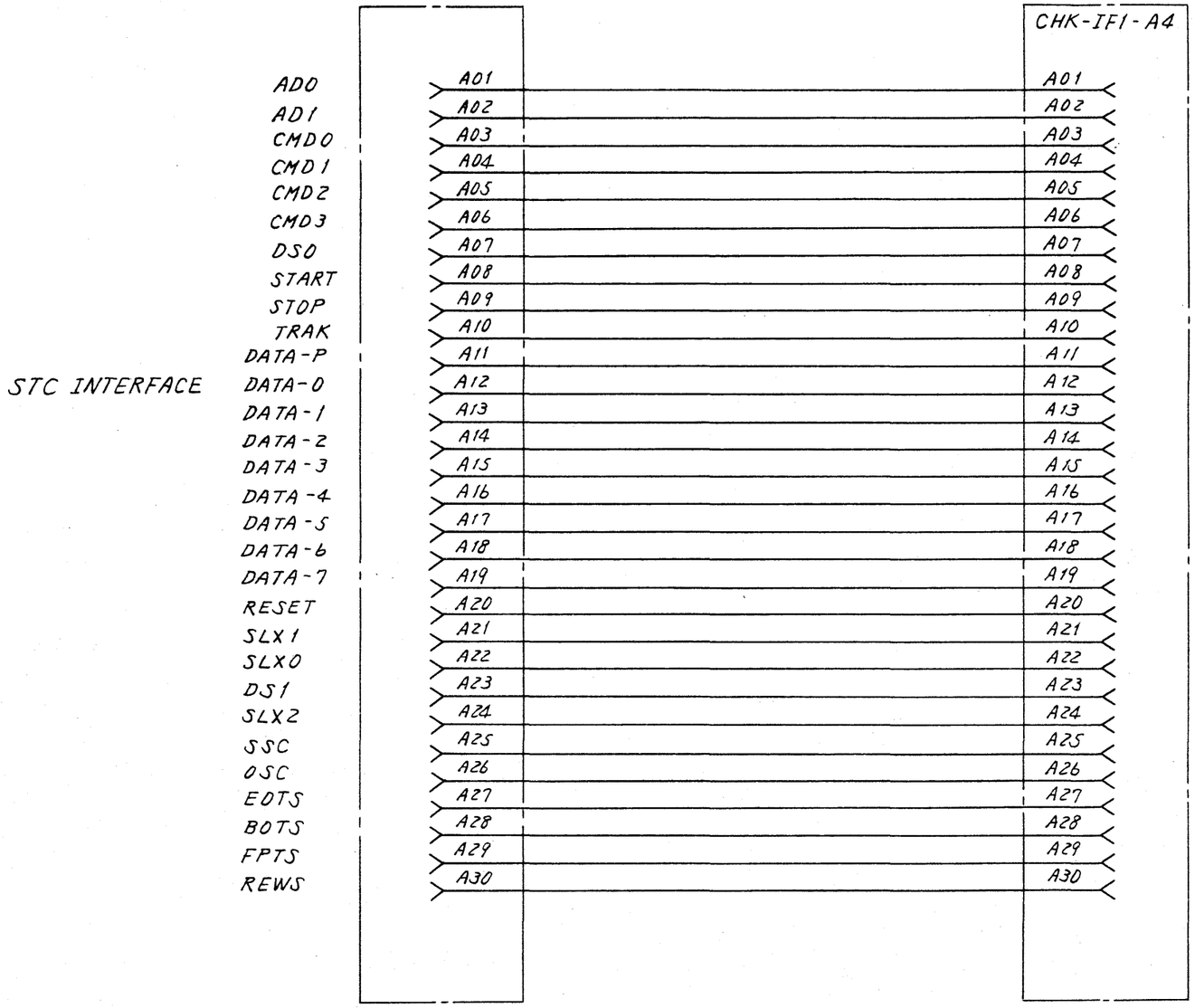
置名

DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190344-001-0

STC-INTERFACE (CMD DATA)



ADO	(401 1B)	
AD1	(401 1B)	
CMD 0	(401 1E)	
CMD 1	(401 1D)	
CMD 2	(401 1D)	
CMD 3	(401 1D)	
DS 0	(401 1E)	
START	(401 1F)	
STOP	(407 1B)	
TRAK	(407 1A)	
DATAP	(405 1E)	
DATA 0	(405 1A)	
DATA 1	(405 1B)	
DATA 2	(405 1B)	
DATA 3	(405 1B)	
DATA 4	(405 1C)	
DATA 5	(405 1D)	
DATA 6	(405 1D)	
DATA 7	(405 1E)	
RESET	(401 1A)	
SLX1	(407 1E)	
SLX0	(407 1E)	
DS 1	(401 1F)	
SLX2	(407 1F)	
SSC	(408 8F)	
OSC	(415 8D)	
EOTS	(408 9H)	
BOTS	(408 9G)	
FPRT	(408 9H)	
REWS	(407 8F)	

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——
2	0	1982.11.22	山口

303

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC ADAPTER CONNECTION DIAGRAM OF CABLE

134-190344-001-0

NEC

SHT 3/6

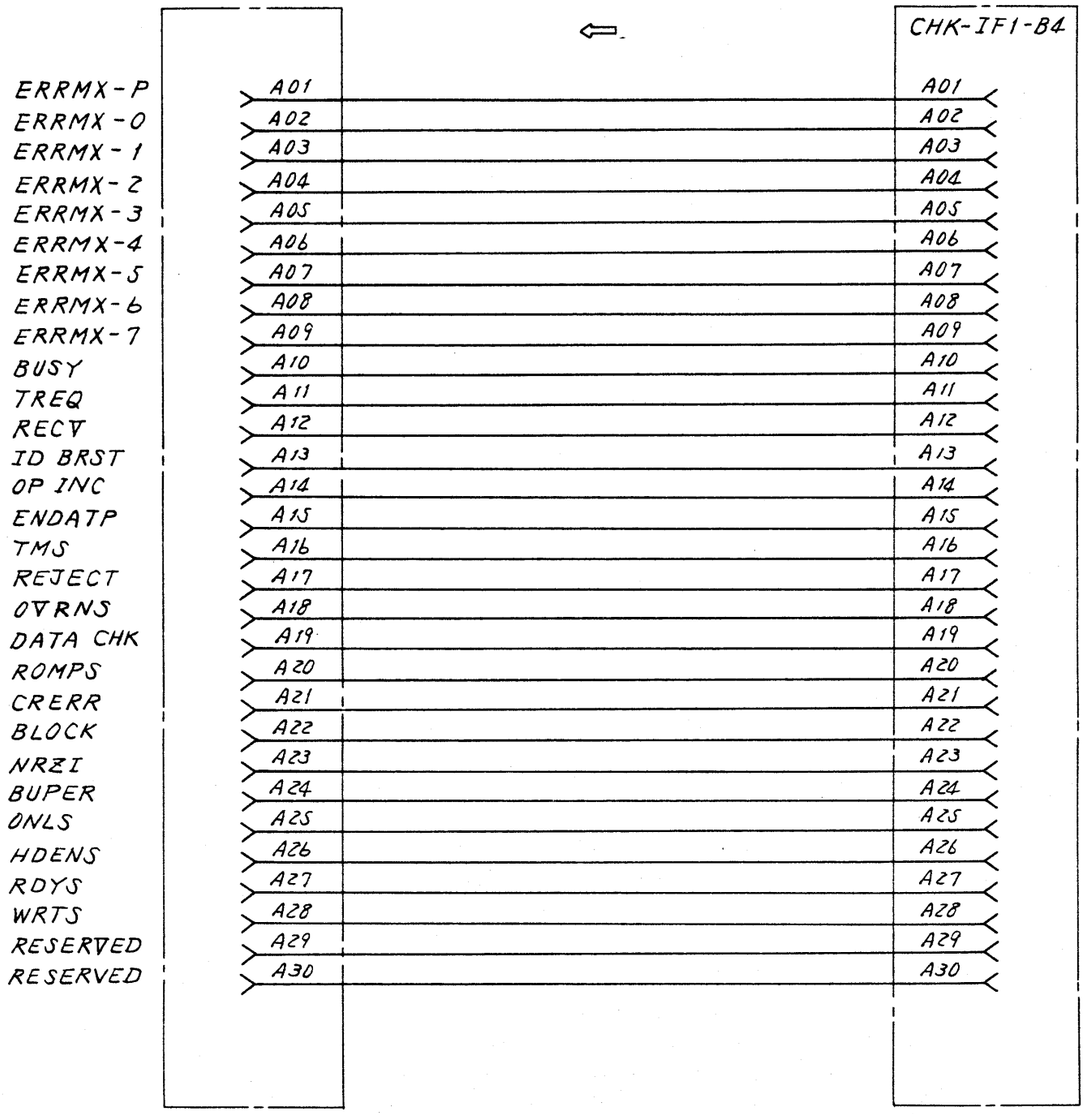
QUIP

DC—405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190344-001-0

STC-INTERFACE (STATUS)



ERMXP	(410 7A)	
ERMX0	(409 9A)	
ERMX1	(409 9B)	
ERMX2	(409 9C)	
ERMX3	(409 9D)	
ERMX4	(409 9E)	
ERMX5	(409 9F)	
ERMX6	(409 9G)	
ERMX7	(409 9H)	
BUSY	(407 8A)	
TREQ	(407 8C)	
RECV	(407 8D)	
ID BRST	(408 8C)	
OP INC	(407 8C)	
ENDATP	(407 8B)	
TMS	(407 8F)	
RJCT	(408 8D)	
OVRNS	(407 8C)	
DTCHK	(408 8D)	
ROMPS	(408 8C)	
CRERR	(408 8B)	
BLOCK	(407 8D)	
NRZI	(408 8B)	
BUPER	(407 8B)	
ONLS	(408 9F)	
HDS	(408 9G)	
RDYS	(408 9F)	
WRTS	(407 8G)	

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——
2	0	1982.11.22	山口

304

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC ADAPTER CONNECTION DIAGRAM OF CABLE

134-190344-001-0

NEC

SHT 4/6

QUIP

DC—405E
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190344-001-0

MTA110 CHK-P1 ⇐ STCA CHK IF1

FORMATTER ADDR	1	MB06	IF1FAD0 (414 8B)
FORMATTER ENABLE	2	MB07	IF1FEN0 (407 8E)
MTU ADDRESS 0	3	MB08	IF1TA00 (414 8B)
MTU ADDRESS 1	4	MB09	IF1TA10 (414 8B)
REVERSE/FORWARD	5	MB11	IF1REV0 (414 8G)
WRITE/READ	6	MB12	IF1WRT0 (414 8G)
WRITE TAPE MARK	7	MB13	IF1WTM0 (414 8F)
ERASE	8	MB14	IF1ERS0 (414 8F)
READ THRE SHOLD	9	MD14	IF1RTH0 (414 8F)
DESITYSELECT1	10	MB16	IF1DN10 (414 8C)
DENSITYSELECT0	11	MD16	IF1DN00 (414 8C)
COMMAND STROBE	12	MD17	IF1GOC0 (407 8E)
REWIND	13	MB17	IF1REW0 (414 8E)
UNLOAD	14	MB18	IF1ULD0 (414 8E)
LAST DATA	15	MB19	IF1LWD0 (410 9H)
WRITE DATA P	16	MB20	IF1WDP0 (410 9G)
WRITE DATA 0	17	MB21	IF1WD00 (410 9E)
WRITE DATA 1	18	MB22	IF1WD10 (410 9E)
WRITE DATA 2	19	MB23	IF1WD20 (410 9E)
WRITE DATA 3	20	MB24	IF1WD30 (410 9F)
WRITE DATA 4	21	MD26	IF1WD40 (410 9F)
WRITE DATA 5	22	MB26	IF1WD50 (410 9F)
WRITE DATA 6	23	MB27	IF1WD60 (410 9G)
WRITE DATA 7	24	MB28	IF1WD70 (410 9G)
NOT USED	25	MB29	
NOT USED	26	MD04	IF17TR0 (414 8D)
XNU	27	MD11	XNU
GND	28~50		XG00

STCA CHK IF1 ⇐ MTA110 CHK-P2

DCTFPT0 (412 5E)	AD30	1	FILE PROTECT
DCTDS10 (413 1E)	AD32	2	DENSITY STATUS1
DCTONL0 (412 5D)	AD33	3	ONLINE
DCTRDY0 (412 5D)	AD34	4	READY
DCTRWD0 (413 1G)	AD36	5	REWINDING
DCTBOT0 (412 5E)	AD37	6	BEGINNING OF TAPE
DCTEOT0 (412 5F)	AD38	7	END OF TAPE
FCTFBY0 (412 1C)	AB28	8	FORMATTER BUSY
FCTDBY0 (412 1B)	AB29	9	DATA BUSY
FCTTMD0 (412 1B)	AB30	10	TAPE MARK DETECT
FCTHER0 (412 1B)	AB31	11	HARD ERROR
FCTDER0 (412 1A)	AB32	12	DATA ERROR
FCTDSR0 (412 1A)	AB33	13	DENSITY ERROR
FCTCRJ0 (412 1A)	AB34	14	COMMAND REJECT
FCTRSB0 (407 1D)	AB36	15	READ STROBE
FCTWSB0 (407 1C)	AB37	16	WRITE STROBE
FCTRDP0 (410 1H)	AB38	17	READ DATA P
FCTRD00 (410 1E)	AB39	18	READ DATA 0
FCTRD10 (410 1E)	AB41	19	READ DATA 1
FCTRD20 (410 1E)	AB42	20	READ DATA 2
FCTRD30 (410 1F)	AB43	21	READ DATA 3
FCTRD40 (410 1G)	AB44	22	READ DATA 4
FCTRD50 (410 1G)	AD45	23	READ DATA 5
FCTRD60 (410 1G)	AB46	24	READ DATA 6
FCTRD70 (410 1G)	AB47	25	READ DATA 7
DCTDS00 (413 1E)	AD31	26	7 TRACK
DCTDST0 (413 1E)	AB22	27	GND
XG00		28~50	GND

置名

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——
2	0	1982.11.22	山口

305

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC ADAPTER CONNECTION DIAGRAM OF CABLE

134-190344-001-0

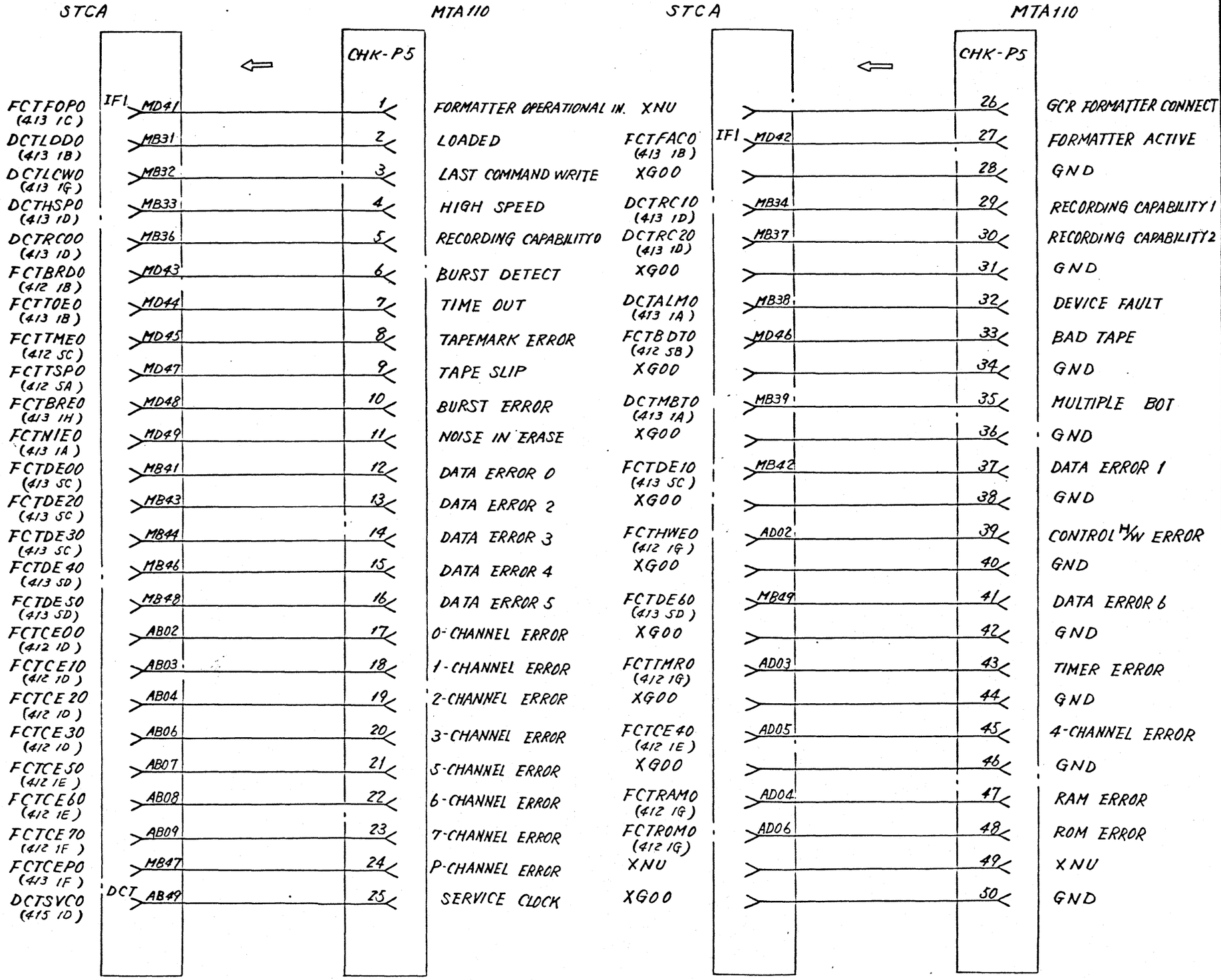
NEC SHT 5/6

DC-405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190344-001-0

REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.2.20	——
2	0	1982.11.22	山口



306

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

STC ADAPTER CONNECTION DIAGRAM OF CABLE

134-190344-001-0

NEC

SHT 6/6

承認名

DC—405
JIS A3 (297×420)

Nippon Electric Co.,Ltd.

134-190344-002-0

REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.11.20.	
2	0	1982.11.22 SC-414076 写替え	
3	0	1983.2.1 SC-414150	

RESET (303 5C) A4A20 RESET — SMT ST LS14 8S 1 — ZTM MC20 2

ADO (303 5A) A4A01 ADO 2° — SMT ST LS14 8S 3 — ZTM MC21 2

AD1 (303 5A) A4A02 AD1 2' — SMT ST LS14 8S 5 — ZTM MC21 3

(FADO) — SMT ST LS14 8S 9 — ZTM MC21 6

SIG3 (407 3H) → & LGD LS08 2B (12, 13 → 11)

& LGA LS04 5J (1 → 2)

X111 (8C) RESET NMI → OA DF TO, CP DFK LS74, MS, MR 8G, FO 6 → NMIO (402 4C)

RSYO (415 2B)(407 6E)

MD18 IFIRSTO (301 1E)

RNMO (7G)

CNT CTD, CNE BRD, LS193 BT: OA IA 2A 3A → TO 7, T1 6, T2 2, T3 3 → TA13 (414 5A), TA03 (414 5A), FAD3 (414 5A)

X111 (8C) → 5, 4; X000 → 11, 14; 9, 10, 1

CM31 (416 6A)
CM21 (416 6A)
CM11 (416 6A)
CM01 (416 6B)

CMD3 (303 5B) A4A06 — SMT ST LS14 8U 1 — ZTM MC21 7
CMD2 (303 5B) A4A05 — SMT ST LS14 8U 3 — ZTM MC21 5
CMD1 (303 5B) A4A04 — SMT ST LS14 8S 11 — ZTM MC20 3
CMD0 (303 5A) A4A03 — SMT ST LS14 8U 5 — ZTM MC21 4
DS0 (303 5B) A4A07 — SMT ST LS14 8U 9 — ZTM MC20 4
DS1 (303 5C) A4A23 — SMT ST LS14 8U 11 — ZTM MC20 7
XNU — SMT ST LS14 8S 13 — ZTM MC20 5
START (303 5B) A4A08 START — SMT ST LS14 8U 13 — ZTM MC20 6

SMT ST LS14 8U 2 → 3 OA, 4 OB, 7 OC, 8 OD, 13 OE, 14 OF, 17 OG, 18 OH; CP 11, MR 1; DF DFN LS273 8V: TO 2, T1 5, T2 6, T3 9, T4 12, T5 15, T6 16, T7 19

CM31 (411 5A)
CM21 (411 5A)
CM11 (411 5A)
CM01 (411 5A)
DS01 (411 5A)
DS11 (411 5B)
XCC1 (411 5B)

TP 7 → ABY1 (411 5B)(407 6A)

& LGA LS04 5J 3 → 4 → ABY0 (2H)

SRT3 (416 6B)

ABY INT

X111 (8C) → & LGA LS04 2L 5 → 6 → OA DF TO, CP DFK LS74, MS, MR 8G, FO → 12, 11, 10, 13; TO 9 → INT1 (411 1D); FO 8 → INT0 (402 5C)

& LGA LS00 2J 2, 1 → 3 → 5, 4 & LGA LS00 2J → 6

SABO (415 4H) → 5
RAB2 (415 4E) → 2
RAF0 (415 6A) → 1

& LGD LS08 4M 2, 1 → 3

RINO (415 4H) → 5
POR2 (415 6A) → 4
& LGD LS08 4M → 6 → RNMO (7B) (416 6D)

ABY0 (6E) → 1
SIG3 (407 3H) → 2
& LSD LS08 2B → 3

X111 (4B)(4F)(7A)(403 6B)(404 5C)(416 6C) → ZTM MC16 2

X112 (405 6G)(406 1B)(406 2F)(406 3H)(406 5D) → ZTM MC12 2

EQUIP

DWG ABBR	STC
PKG LOCATION	IFI
PKG NAME	G9QYS
	401
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER STC ADAPTER CIRCUIT DIAGRAM

134-190344-002-0

NEC — SHT 1/18

Nippon Electric Co.Ltd.

DB-413E
JIS A2 (420×594)

134-190344-002-0

REV	COMP	DESCRIPTION(SC)	APP
1	0	1981.11.20.	
2	0	1982.11.22	
3	0	1982.12.1	

DWG ABBR	STC
PKG LOCATION	IF1
PKG NAME	G9QYS
	402
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

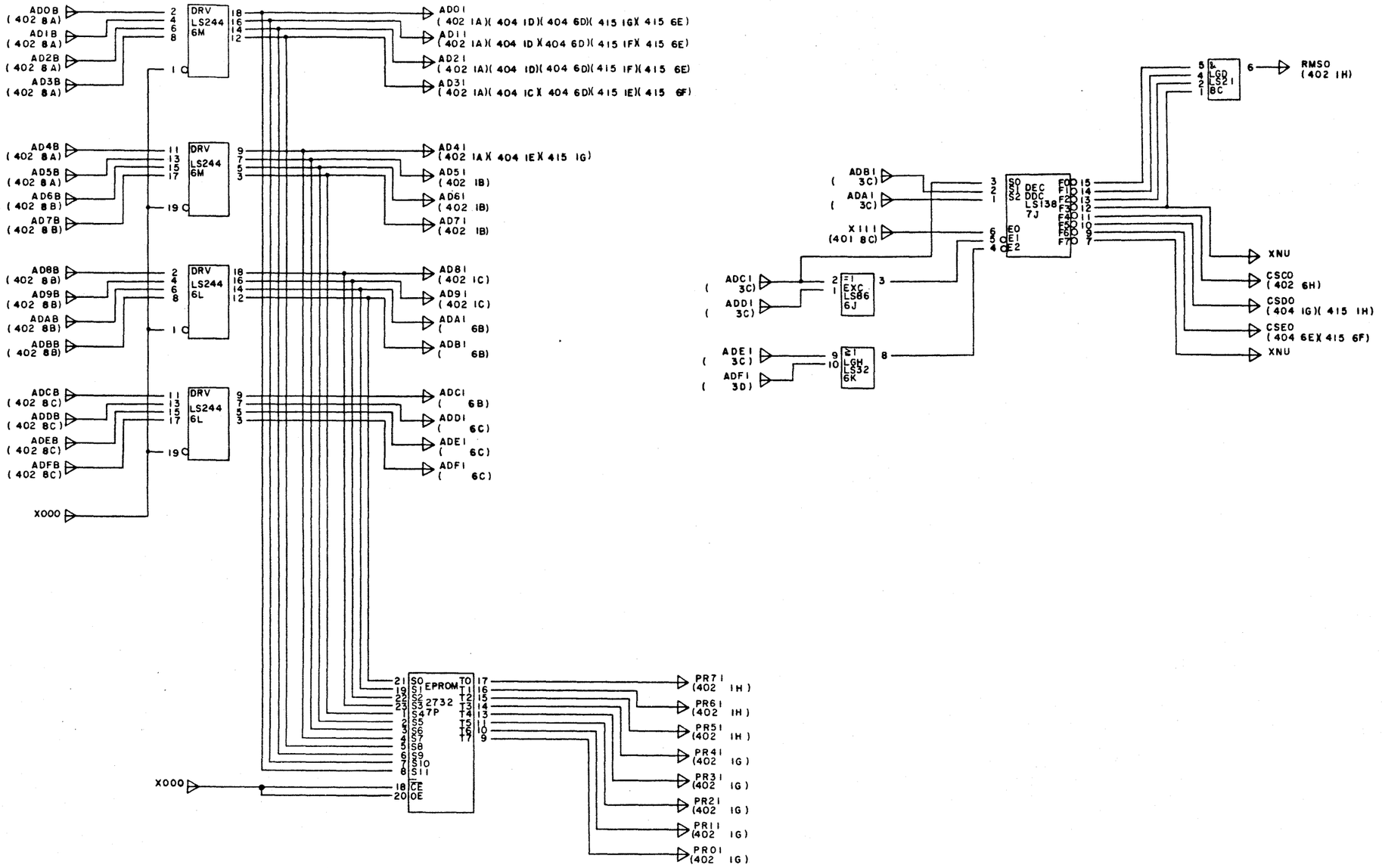
NEC SHT 2/

Nippon Electric Co.Ltd.

EQUIP

DB 413E
JIS A2 (420×594)

134-190344-002-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	1981.11.20	
2	0	1982.11.22	
3	0	198	

DWG ABBR	S T C
PKG LOCATION	I F I
PKG NAME	G 9 Q Y S

403

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山[illegible]口		今村	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

NEC

SHT 3/

Nippon Electric Co.Ltd.

EQUIP

DB-413E
JIS A2 (420×594)

134-190344-002-0

REDO (402 8D)
IRQO (402 8D)
MRQO (402 8C)
WRTO (402 8D)
XOOO
LGH LS32 4P
DRV LS244 4N
XNU
MRDO (6E)(402 6G)(402 1H)(1G)
MWTO (402 1B)(402 6G)(415 1H)(415 5F)

EXT REGISTER READ

AD3I (403 3A)
AD2I (403 3A)
AD1I (403 3A)
AD0I (403 3A)
AD4I (403 3B)
LGA LS04 2L
DEC DDC LS138 8R
EX00 (411 3B)
EX10 (411 3D)
EX20 (411 3F)
EX30 (411 3G)
EX40 (411 6D)
EX50 (411 6B)
EX60 (413 6E)
EX70 (411 6F)
DEC DDC LS138 8Q
XNU
EX90 (411 6G)
RAB4 (416 6E)
XNU
XNU
XNU
RSCO (416 6D)
XNU
CSDO (403 9B)
MRDO (5B)
LGH LS32 4L
CDRO (402 1E)

STATUS READ

X1II (401 8C)
AD3I (403 3A)
AD2I (403 3A)
AD1I (403 3A)
AD0I (403 3A)
DEC DDC LS138 2M
SR00 (412 3F)
SR10 (412 7C)
SR20 (413 3C)
SR30 (412 7F)
SR40 (413 3H)
SR50 (413 6E)
SR60 (413 3F)
SR70 (412 3C)
CSEO (403 9C)
MRDO (5B)
LGH LS32 4L
CERO (402 1F)
X000
ZSW 4W **1
TF16I (413 1F)
XNU
XNU
XNU
SW5I (411 5G)
SW6I (411 5G)
SW7I (411 5G)
SW8I (411 5G)
R T2M MC14 RN206

REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.11.20.	
2	0	1982.11.22	
3	0	1985	

DWG ABBR	STC
PKG LOCATION	IF1
PKG NAME	G9QYS
	404
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

NEC SHT 4/

Nippon Electric Co.Ltd.

EQUIP

D8-413E
JIS A2 (420×594)

134-190344-002-0

REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.11.20.	——
2	0	1982.11.22	
3	0	1982.[illegible]	

DATA0 (303 5B) A4A12 — ZTM MC19 4
DATA1 (303 5B) A4A13 — ZTM MC19 5
DATA2 (303 5C) A4A14 — ZTM MC19 2
DATA3 (303 5C) A4A15 — ZTM MC19 6
DATA4 (303 5C) A4A16 — ZTM MC19 7
DATA5 (303 5C) A4A17 — ZTM MC18 2
DATA6 (303 5C) A4A18 — ZTM MC18 3
DATA7 (303 5C) A4A19 — ZTM MC18 4
DATAP (303 5B) A4A11 — ZTM MC19 3

DRV LS240 4H
DRV LS240 4H
DRV LS240 3K
& LGA LS04 4G

DWT1 (414 6H)
STP3 (406 5H)
FLD3 (406 9G)
X000
RDO1 (410 5E)
RD11 (410 5E)
RD21 (410 5E)
RD31 (410 5F)
RD41 (410 5G)
RD51 (410 5G)
RD61 (410 5G)
RD71 (410 5G)
RDP1 (410 5H)

FF01 (9A) — & MOK 38 3Q
FF11 (9A) — & MOK 38 3P
FF21 (9A) — & MOK 38 3P
FF31 (9A) — & MOK 38 3P
FF41 (9B) — & MOK 38 3P
FF51 (9B) — & MOK 38 3N
FF61 (9B) — & MOK 38 3N
FF71 (9B) — & MOK 38 3N
RDP3 (410 8B) — & MOK 38 3N
DRD1 (414 6G)

X000
RSTO (415 6B)

ODFIFO 2D S225 3D 3H 4D
ODFIFO 2D S225 3D 3J 4D
ODFIFO 2D S225 3D 3L 4D
ODFIFO 2D S225 3D 3M 4D
ODFIFO 2D S225 3D 3D 4D
ODFIFO 2D S225 3D 3E 4D
ODFIFO 2D S225 3D 3F 4D
ODFIFO 2D S225 3D 3G 4D

FF01 (IF)(410 7D)
FF11 (IF)(410 7E)
FF21 (IF)(410 7E)
FF31 (IG)(410 7F)
FF41 (IG)(410 7F)
FF51 (IG)(410 7F)
FF61 (IG)(410 7G)
FF71 (IH)(410 7G)
FFP1 (410 7G)
LWD1 (410 6H)

FUD2 (406 9H)

& LGD LS08 4F — INRDY1 (406 1A)
& LGA LS04 4G — INRDY0 (5F)
& LGD LS08 4F — OUTRY1 (406 1B)
& LGA LS04 4G — OUTRY0 (5E)

BUS PARITY ERR

=1 EXC LS86 6J
DF DFK LS74 4D — BPY1 (411 1E)(407 6B)
FLD3 (406 9G)

OVERRUN
OUTRY0 (9D)
WSB1 (407 4D)
DF DFK LS74 4D
&I LGH LS32 4L — OVRN1 (407 6C)(411 1E)

STP2 (406 5H)
INRDY0 (6D)
& LGD LS08 4F

UNDERRUN
RSTO (415 6B)
RSB1 (4073D)
DF DFK LS74 4E

FLD3 (406 9G)
RST1 (415 6B)
CK CN LS393 4C — TO T1 T2 T3
FUD2 (406 9H)
CK CN LS393 4C — TO T1 T2 T3
A3 B3 A2 B2 A1 B1 A0 B0 CMP LCC LS85 4B — TA TB TC — FER0 (411 1E)
X112 (401 8D)

EVN1 (410 9C)
FUD3 (406 9G)
RSTO (415 6B)
DF DFK LS74 4E — FPY1 (411 1E)

EQUIP

DWG ABBR: STC
PKG LOCATION: IFI
PKG NAME: G9QYS

405

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山内		今村	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

NEC — SHT 5/

Nippon Electric Co.,Ltd.

DB 413E
JIS A2 (420×594)

134-190344-002-0

REV	COMP	DESCRIPTION (SC)	APP
1	0	1981. 11. 20.	
2	0	1982.11.22	
3	0	1983. 2. 1	

DWG ABBR	STC
PKG LOCATION	IFI
PKG NAME	G9QYS

406

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	田 吉 山 本		今 村	

MTAI6X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

NEC

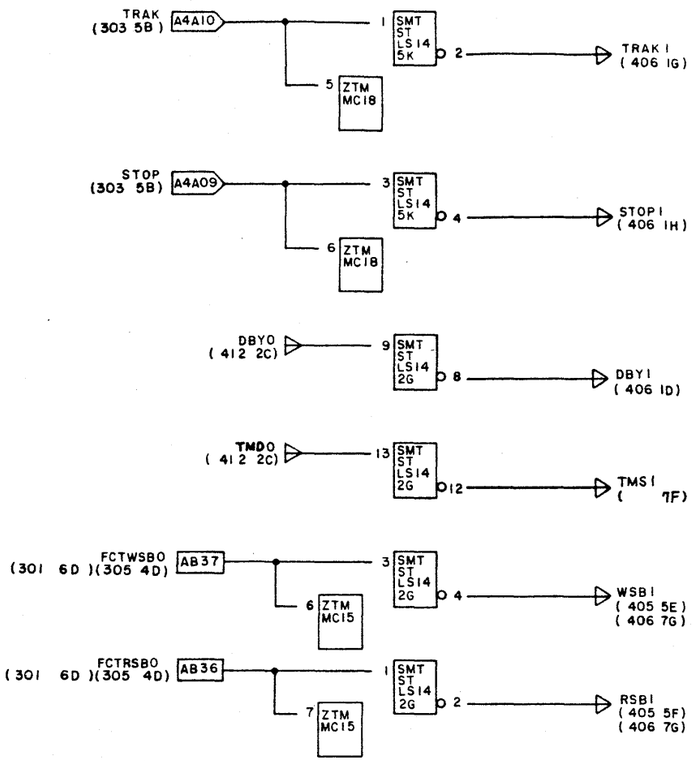
SHT 6/

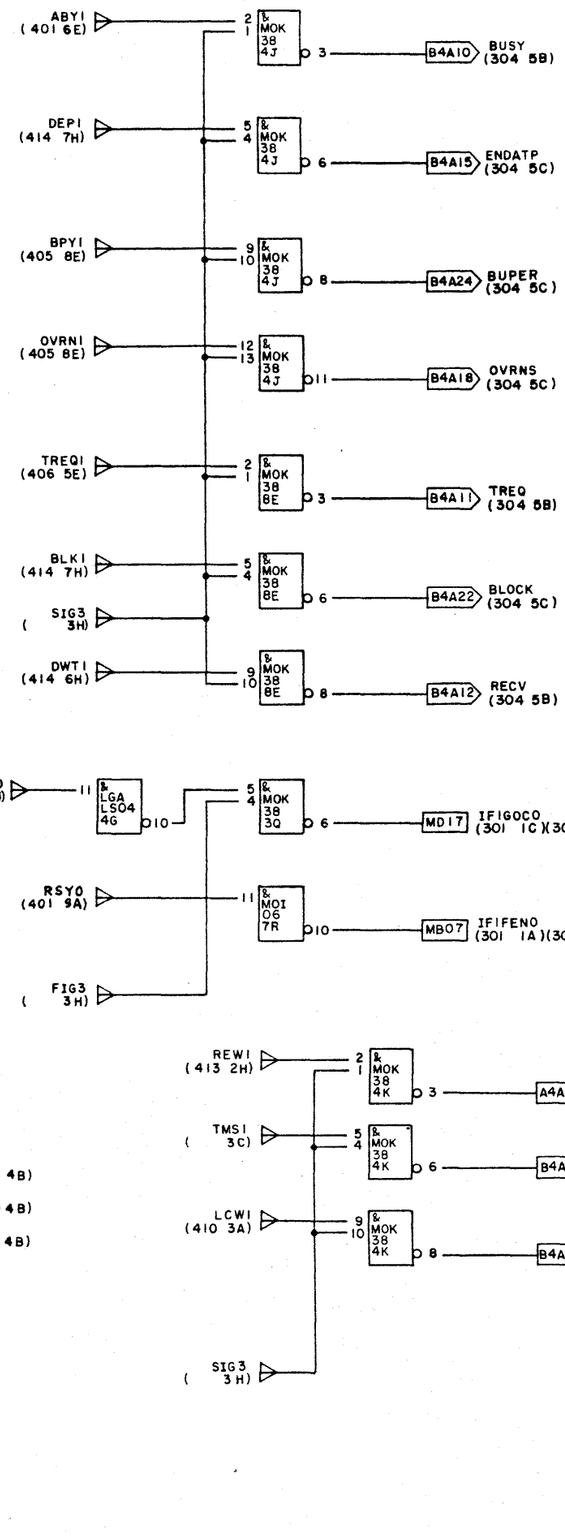
Nippon Electric Co.Ltd.

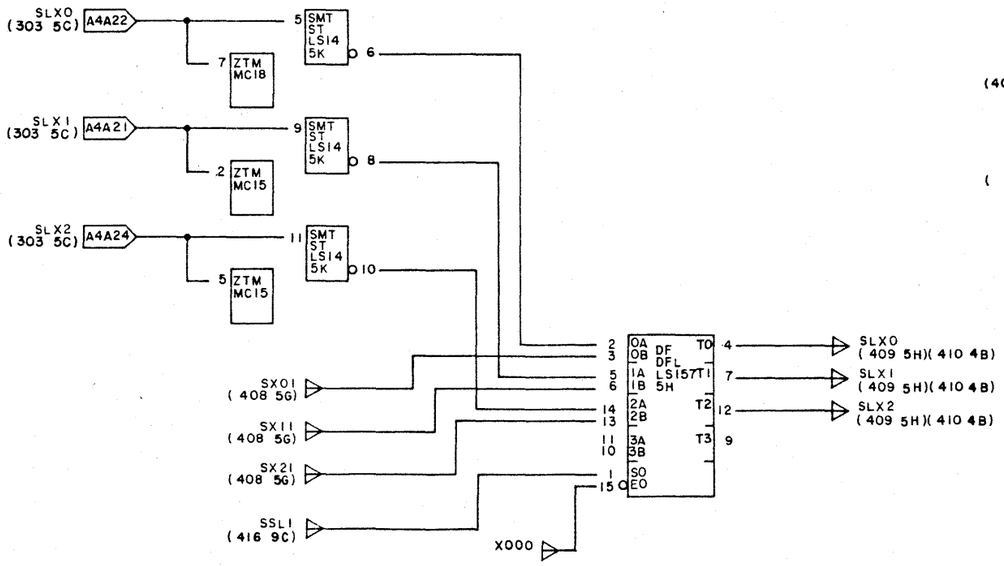
EQUIP

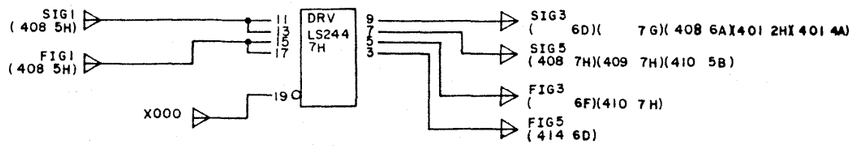
DB-413E
JIS A2 (420×594)

134-190344-002-0









REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.11.20.	——
2	0	1982.11.22	山口
3	0	1982.[illegible]	

DWG ABBR	STC
PKG LOCATION	IFI
PKG NAME	G9QYS
407	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山口 木		介村	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

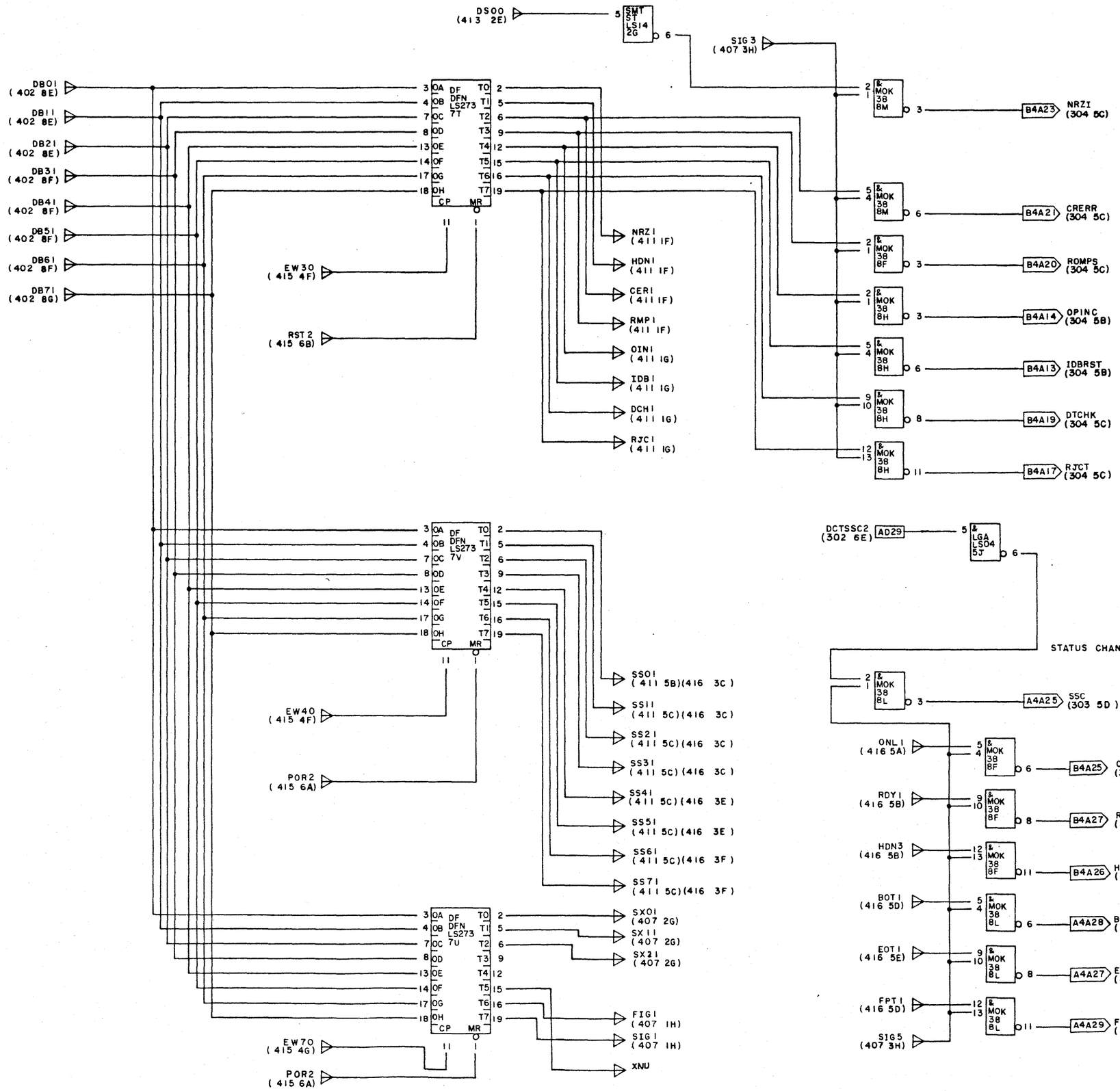
134-190344-002-0

NEC SHT 7/

EQUIP

DB-413E
JIS A2 (420×594)

Nippon Electric Co.,Ltd.



REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.11.20.	——
2	0	1982.11.22	
3	0	198 . 1	

DWG ABBR	S T C
PKG LOCATION	I F I
PKG NAME	G 9 Q Y S
408	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山崎 口木		今村	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

NEC SHT 8/

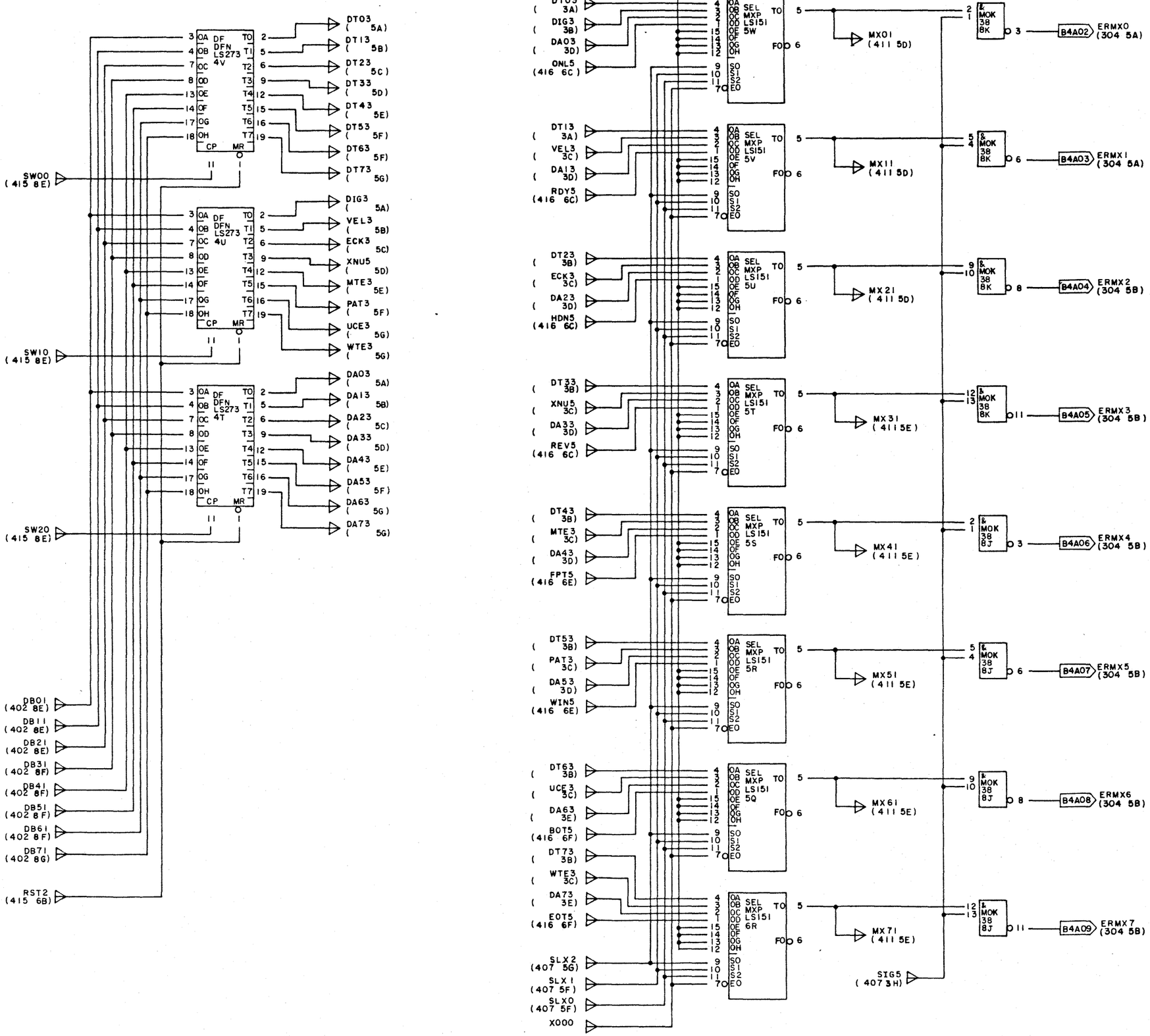
Nippon Electric Co.Ltd.

134-190344-002-0

EQUIP

DB-413E
JIS A2 (420×594)

134-190344-002-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.11.20.	——
2	0	1982.11.22	
3	0	198[illegible]	

DWG ABBR	STC
PKG LOCATION	IFI
PKG NAME	G9QYS

409

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	[illegible] 日本		今村	

MTA16X FORMATTER STC ADAPTER CIRCUIT DIAGRAM

134-190344-002-0

NEC

SHT 9/

EQUIP

DB-413E
JIS A2 (420×594)

Nippon Electric Co.,Ltd.

134-190344-002-0

STATUS

LCW0 (413 2G) → SMT ST LS14 7K
LCW1 (407 7G)
DB01 (402 8E)
DB11 (402 8E)
DB21 (402 8E)
DB31 (402 8F)
DB41 (402 8F)
DB51 (402 8F)
DB61 (402 8F)
DB71 (402 8G)
SW40 (415 8F)
RST2 (415 6B)
DFN LS273 4R
DTP
CRC
TACH
XNU
BRE1
XNU
XNU
X000
SLX2 (407 5G)
SLX1 (407 5F)
SLX0 (407 5F)
X000
SEL MXP LS151 4Q
MXP1 (413 5E)
SIG5 (407 3H)
&MOK 38 8M
B4A01 ERMXP (304 5A)

LED DISPLAY

EW60 (415 4G)
POR2 (415 6A)
DFN LS175 7S
&MOI 06 7R
LED0
LED1
LED2
LED3
ZRD ZRD **1
ZRD ZRD **2
ZRD ZRD **3
ZRD ZRD **4

READ DATA

FCTRD00 (301 6D)(305 4D) AB39
FCTRD10 (301 6D)(305 4D) AB41
FCTRD20 (301 6D)(305 4D) AB42
FCTRD30 (301 6E)(305 4D) AB43
FCTRD40 (301 6E)(305 4E) AB44
FCTRD50 (301 6E)(305 4E) AD45
FCTRD60 (301 6E)(305 4E) AB46
FCTRD70 (301 6E)(305 4E) AB47
FCTRDP0 (301 6D)(305 4D) AB38
DRV LS240 2C
DRV LS240 3C
DRV LS240 3C
ZTM MC11
ZTM MC12
DRDI (414 6G)
&LGA LS04 6C
RD01 (405 3E)
RD11 (405 3E)
RD21 (405 3E)
RD31 (405 3E)
RD41 (405 3E)
RD51 (405 3F)
RD61 (405 3F)
RD71 (405 3F)
RDP1 (405 3F)

X000
P PAC 82S62 3S
TD
TE
RDP3 (405 1H)
=1 EXC LS86 6J
EVN1 (405 5H)

WRITE DATA

FF01 (405 9A)
FF11 (405 9A)
FF21 (405 9A)
FF31 (405 9B)
FF41 (405 9B)
FF51 (405 9B)
FF61 (405 9B)
FF71 (405 9B)
FFP1 (405 9B)
&MOK 38 2T
&MOK 38 3R
&MOK 38 3Q
MB21 IF1WD00 (301 1D)(305 3D)
MB22 IF1WD10 (301 1D)(305 3D)
MB23 IF1WD20 (301 1D)(305 3D)
MB24 IF1WD30 (301 1D)(305 3D)
MD26 IF1WD40 (301 1D)(305 3D)
MB26 IF1WD50 (301 1E)(305 3E)
MB27 IF1WD60 (301 1E)(305 3E)
MB28 IF1WD70 (301 1E)(305 3E)
MB20 IF1WDP0 (301 1D)(305 3D)
LWD1 (405 9C)
LST1 (414 5H)
F1G3 (407 3H)
&1 LGM LS32 5E
MB19 IF1LWD0 (301 1C)(305 3C)

REV	COMP	DESCRIPTION(SC)	APP
1	0	1981.11.20	
2	0	1982.11.22	
3	0	198[illegible]	

DWG ABBR	STC
PKG LOCATION	IF1
PKG NAME	G9QYS
	410
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山口 山本		斗 斗	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

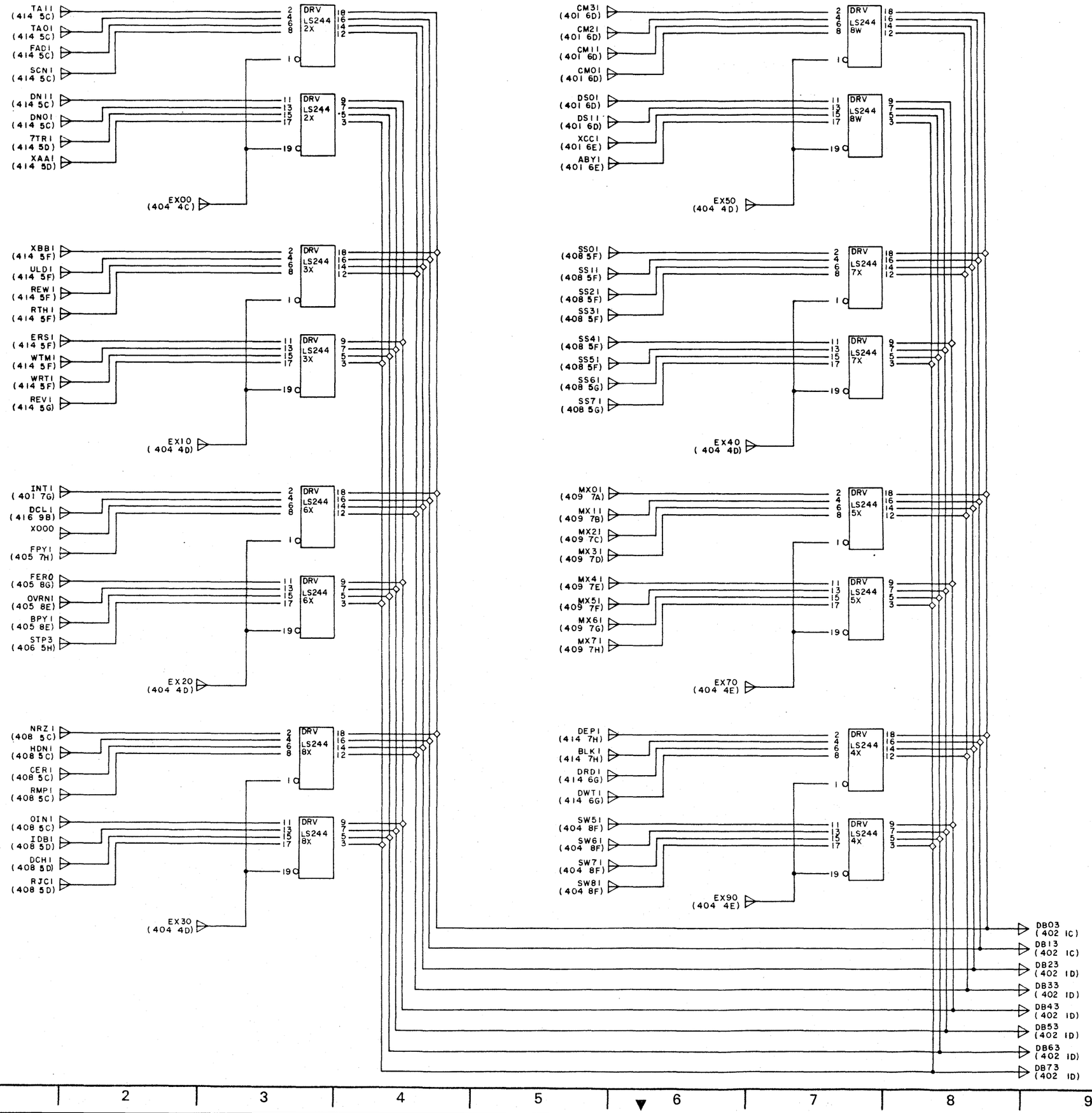
NEC SHT 10/

Nippon Electric Co.,Ltd.

EQUIP

DB-413E
JIS A2 (420×594)

134-190344-002-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	1981 11. 20.	
2	0	1982.11.22	
3	0	983	

DWG ABBR	S T C
PKG LOCATION	I F I
PKG NAME	G 9 Q Y S

411

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山本		今村	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

NEC

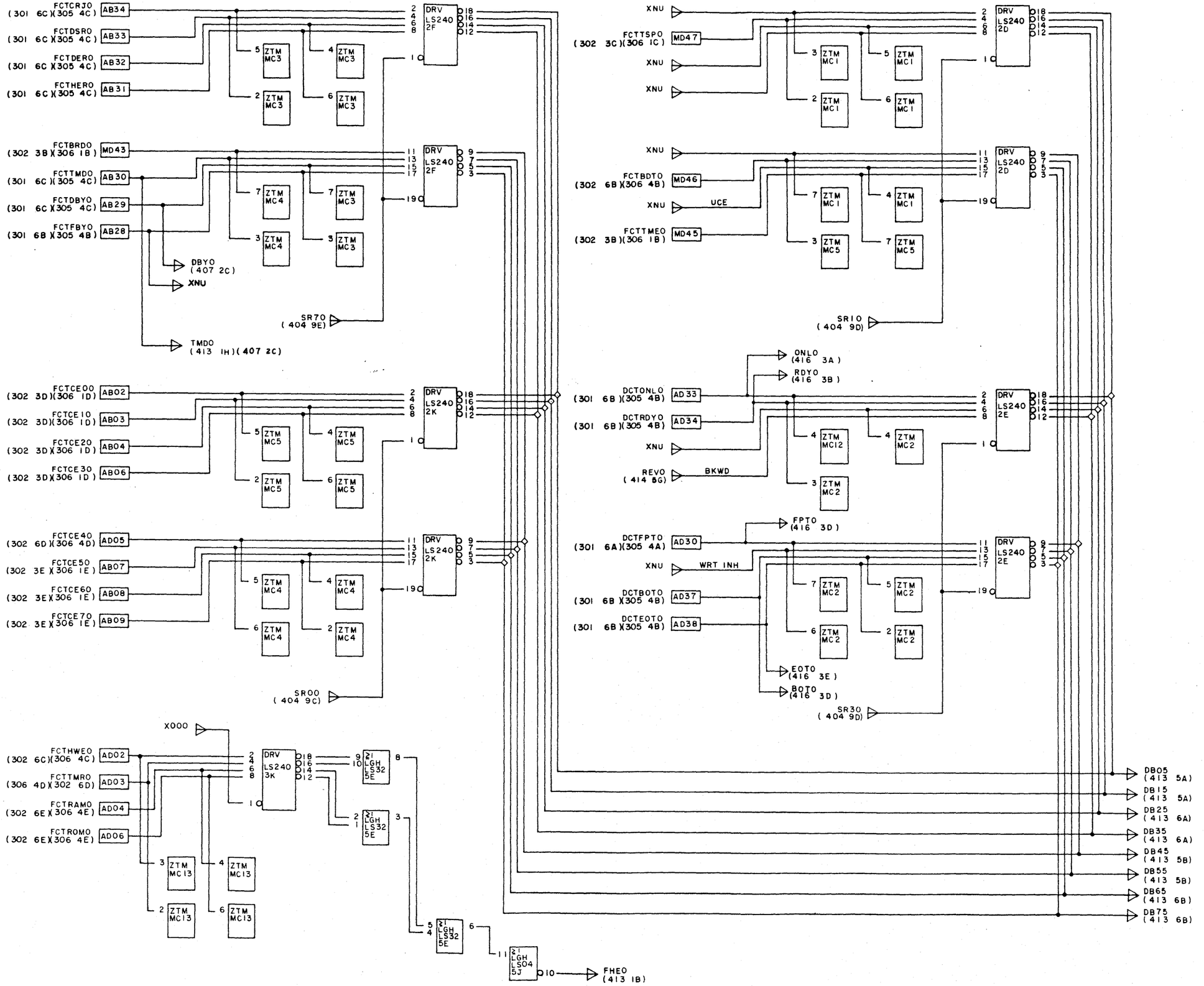
SHT 11/

Nippon Electric Co.,Ltd.

EQUIP

DB 413E
JIS A2 (420 × 594)

134-190344-002-0



EQUIP

REV	COMP	DESCRIPTION (SC)	APP
1	0	1981. 11. 20	——
2	0	1982. 11. 22	
3	0	19-	

DWG ABBR	STC
PKG LOCATION	IFI
PKG NAME	G9QYS
	412
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山本		今村	

MTA16X FORMATTER STC ADAPTER CIRCUIT DIAGRAM

134-190344-002-0

NEC SHT 12/

DB 413E
JIS A2 (420×594)

Nippon Electric Co.,Ltd.

134-190344-002-0

REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.11.20.	
2	0	1982.11.22	
3	0	198-	

DCTALMO (302 6B)(306 4B) MB38
DCTMBTO (302 6C)(306 4C) MB39
FCTN1EO (302 3C)(306 1C) MD49
FCTTOEO (302 3B)(306 1B) MD44
DRV LS240 2Q
ZTM MC9
DB05 (412 9G)
DB15 (412 9G)
DB25 (412 9G)
DB35 (412 9G)
DB05 (402 1E)
DB15 (402 1E)
DB25 (402 1E)
DB35 (402 1F)

FHE0 (412 5H)
DCTLDDO (302 3A)(306 1A) MB31
FCTFACO (302 6A)(306 4A) MD42
FCTFOPO (302 3A)(306 1A) MD41
DRV LS240 2Q
ZTM MC8
DB45 (412 9G)
DB55 (412 9G)
DB65 (412 9H)
DB75 (412 9H)
DB45 (402 1F)
DB55 (402 1F)
DB65 (402 1F)
DB75 (402 1F)
SR20 (404 9D)

FCTDE00 (302 3C)(306 1C) MB41
FCTDE10 (302 6C)(306 4C) MB42
FCTDE20 (302 3C)(306 1C) MB43
FCTDE30 (302 3C)(306 1C) MB44
DRV LS240 2P
ZTM MC7
ZTM MC8

DCTRC20 (302 6B)(306 4B) MB37
DCTRC10 (302 6B)(306 4B) MB34
DCTRC00 (302 3B)(306 1B) MB36
DCTHSPO (302 3B)(306 1B) MB33
DRV LS240 2R
ZTM MC10
DS10 (416 3B)
DS00 (416 3B)(408 5A)
DCTDS10 (301 6A)(305 4A) AD32
DCTDS00 (301 6A)(305 4E) AD31
DCTDSTO (305 4E) AB22
TF16! (404 8E)
TF110 : CONECT
ZTM MC9

FCTDE40 (302 3D)(306 1D) MB46
FCTDE50 (302 3D)(306 1D) MB48
FCTDE60 (302 6D)(306 4D) MB49
MXP1 (410 5A)
&
LGA LS04 2L
DRV LS240 2P
ZTM MC7
SR50 (404 9D)

FCTCEPO (302 3E)(306 1E) MB47
XNU
XNU
DCTLCWO (302 3B)(306 1B) MB32
LCWO (410 1A)
DRV LS240 2N
ZTM MC7
ZTM MC6
SR60 (404 9D)

EX60 (404 4D)
PROM PARA
X000
0A 0B 0C 0D 0E 0F 0G 0H ZSW ZSW 6U **2
TO TI T2 T3 T4 T5 T6 T7
DRV LS244 6V
RM0 DB03 (402 1C)
RM1 DB13 (402 1C)
RM2 DB23 (402 1D)
RM3 DB33 (402 1D)
RM4 DB43 (402 1D)
RM5 DB53 (402 1D)
RM6 DB63 (402 1D)
RM7 DB73 (402 1D)
R T2M MC14 RN206
R T2M MC17 RN206

XNU
DCTRWDO (301 6B)(305 4B) AD36
FCTBREO (302 3C)(306 1C) MD48
TMDO (412 2C)
SMT ST LS14 7K
REW1 (407 7F)
SR40 (404 9D)

EQUIP

DWG ABBR	STC
PKG LOCATION	IFI
PKG NAME	G9QYS

413

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山水		今村	

MTAI6X FORMATTER STC ADAPTER CIRCUIT DIAGRAM

134-190344-002-0

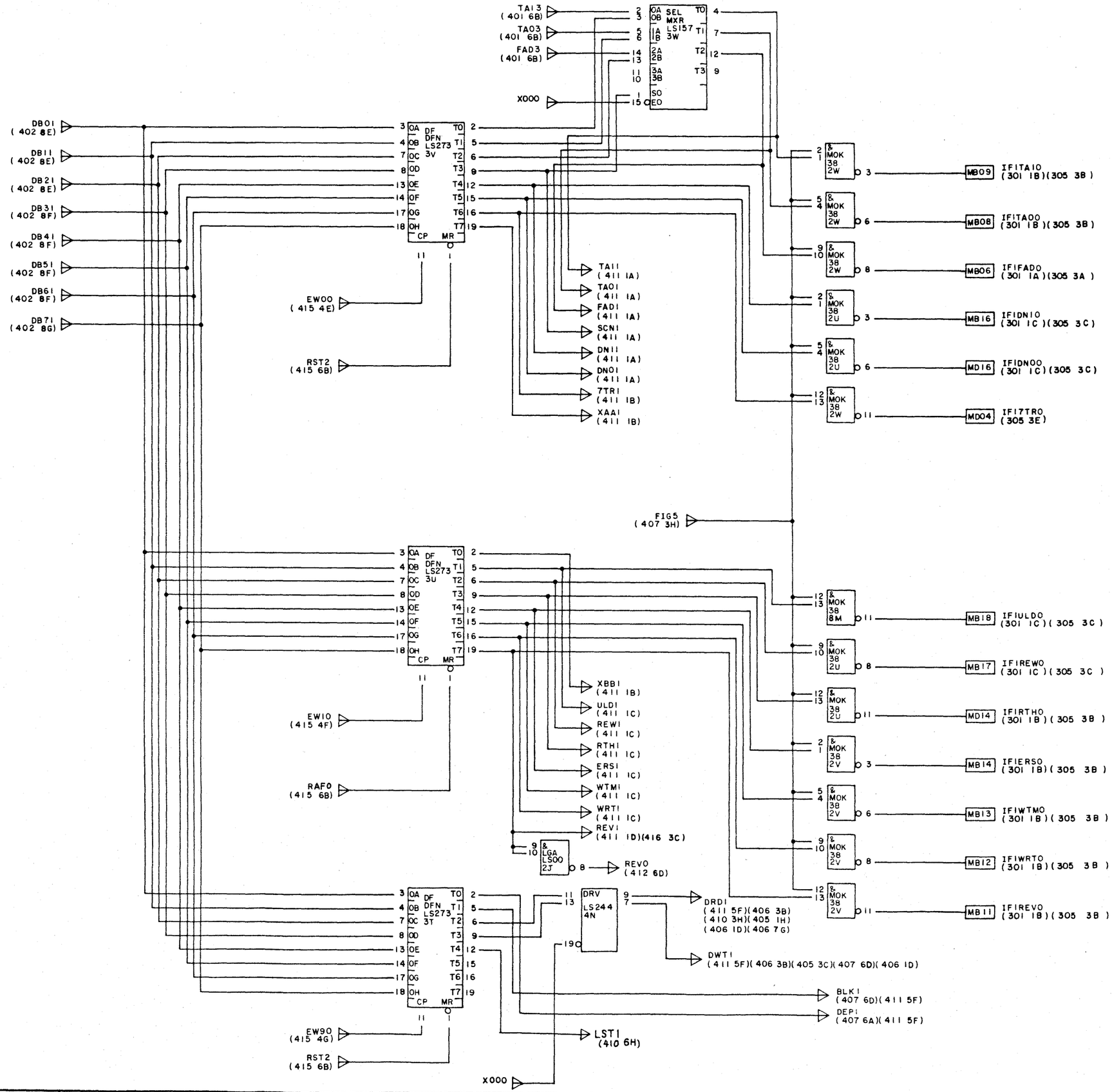
NEC SHT 13/

Nippon Electric Co.Ltd.

DB 413E
JIS A2 (420×594)

134-190344-002-0

REV	COMP	DESCRIPTION (SC)	APP
1	0	1981.11.20.	
2	0	1982.11.22	
3	0	1983	



DWG ABBR	STC
PKG LOCATION	IF1
PKG NAME	G9QYS
	414
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER STC ADAPTER CIRCUIT DIAGRAM

134-190344-002-0

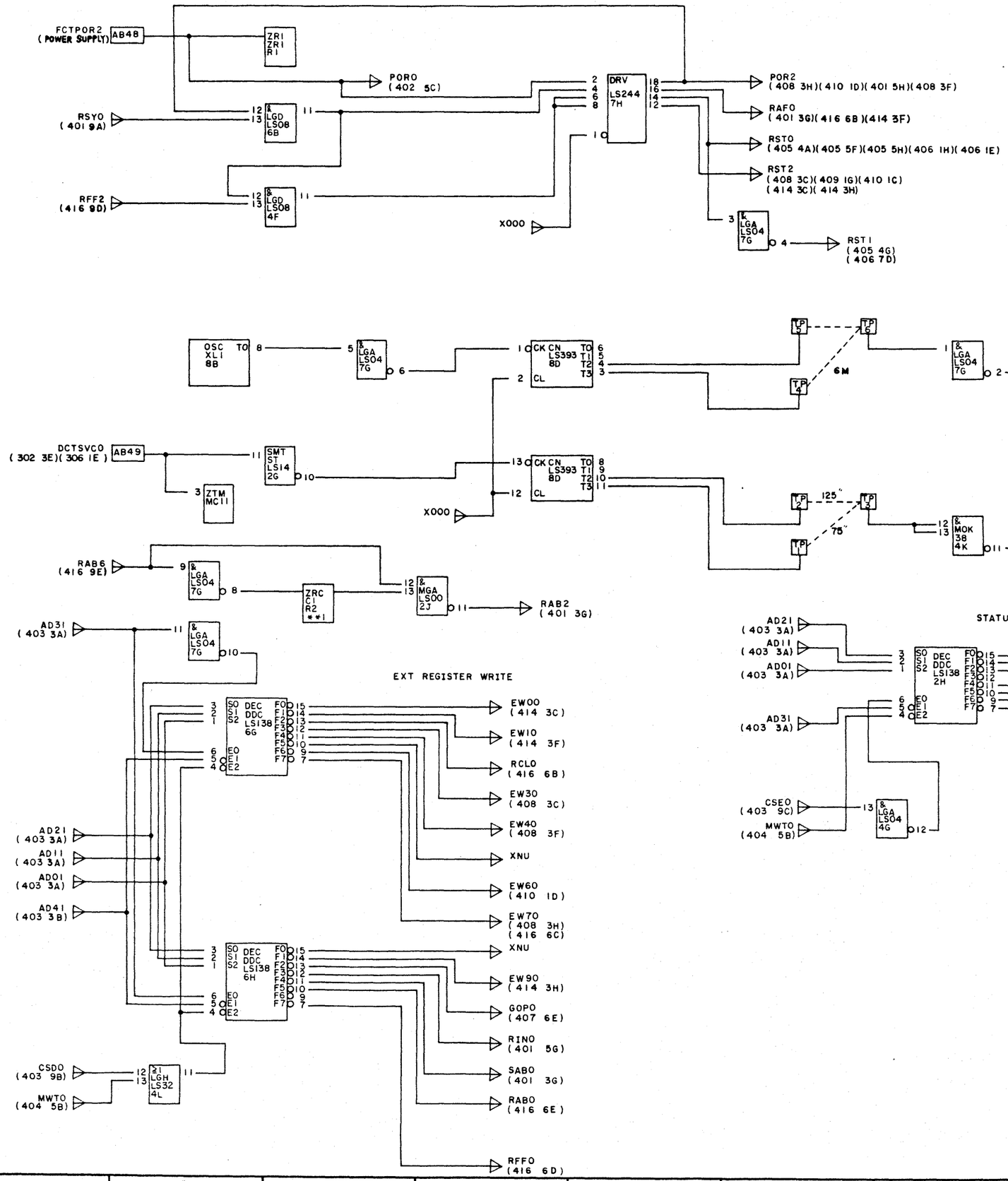
NEC SHT 14/

Nippon Electric Co.,Ltd.

EQUIP

DB 413E
JIS A2 (420×594)

134-190344-002-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	1981.11.20.	——
2	0	1982.11.22	
3	0	19[illegible]	

DWG ABBR	STC
PKG LOCATION	IFI
PKG NAME	G9QYS

415

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	[illegible]		[illegible]	

MTA16X FORMATTER STC ADAPTER CIRCUIT DIAGRAM

134-190344-002-0

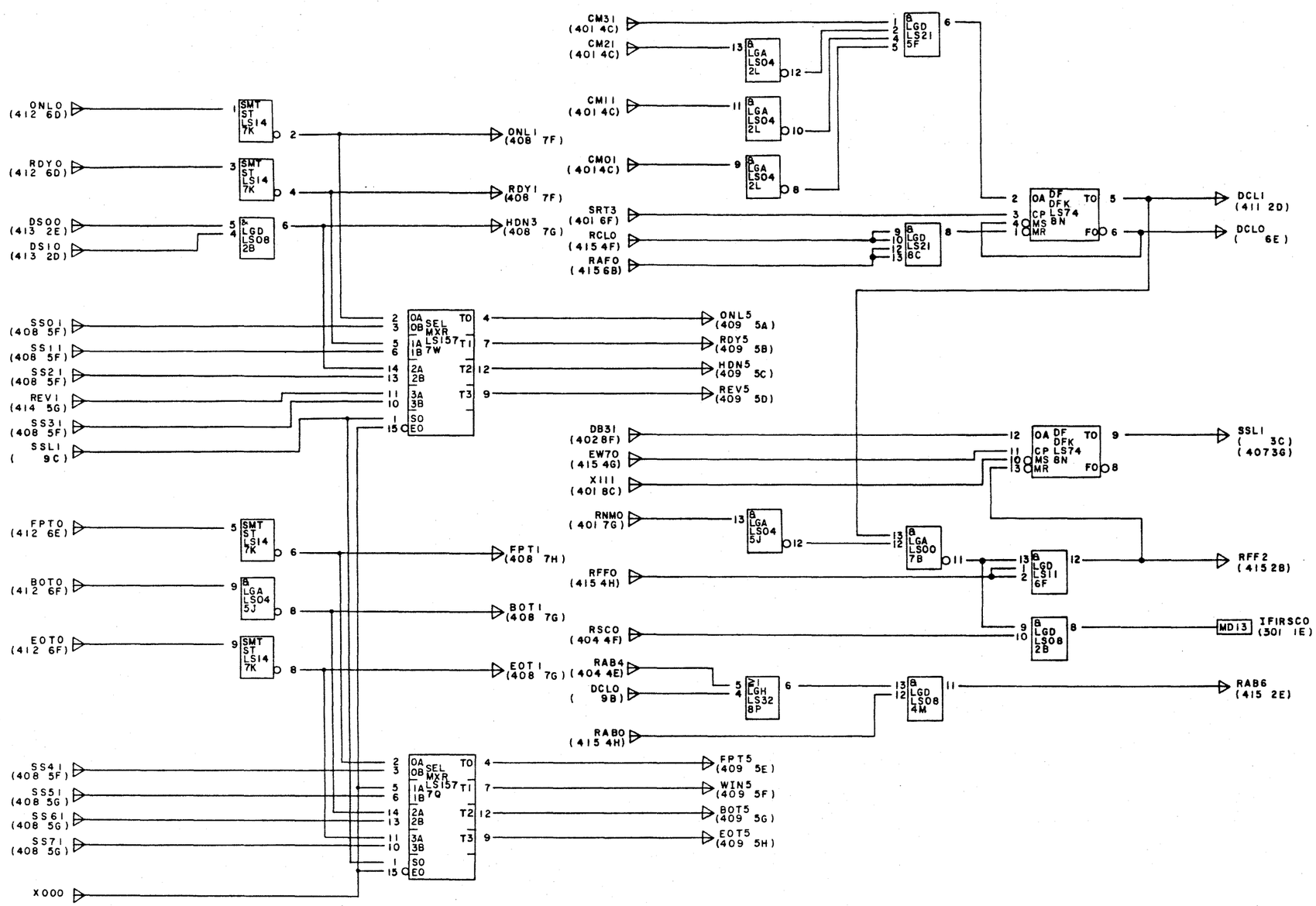
NEC SHT 15/

Nippon Electric Co.,Ltd.

EQUIP

DB 413E
JIS A2 (420×594)

134-190344-002-0



REV	COMP	DESCRIPTION(SC)	APP
1	0	1981.11.20	
2	0	1982.11.22	
3	0		

DWG ABBR	S T C
PKG LOCATION	I F I
PKG NAME	G 9 Q Y S

416

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

MTA16X FORMATTER
STC ADAPTER
CIRCUIT DIAGRAM

134-190344-002-0

NEC

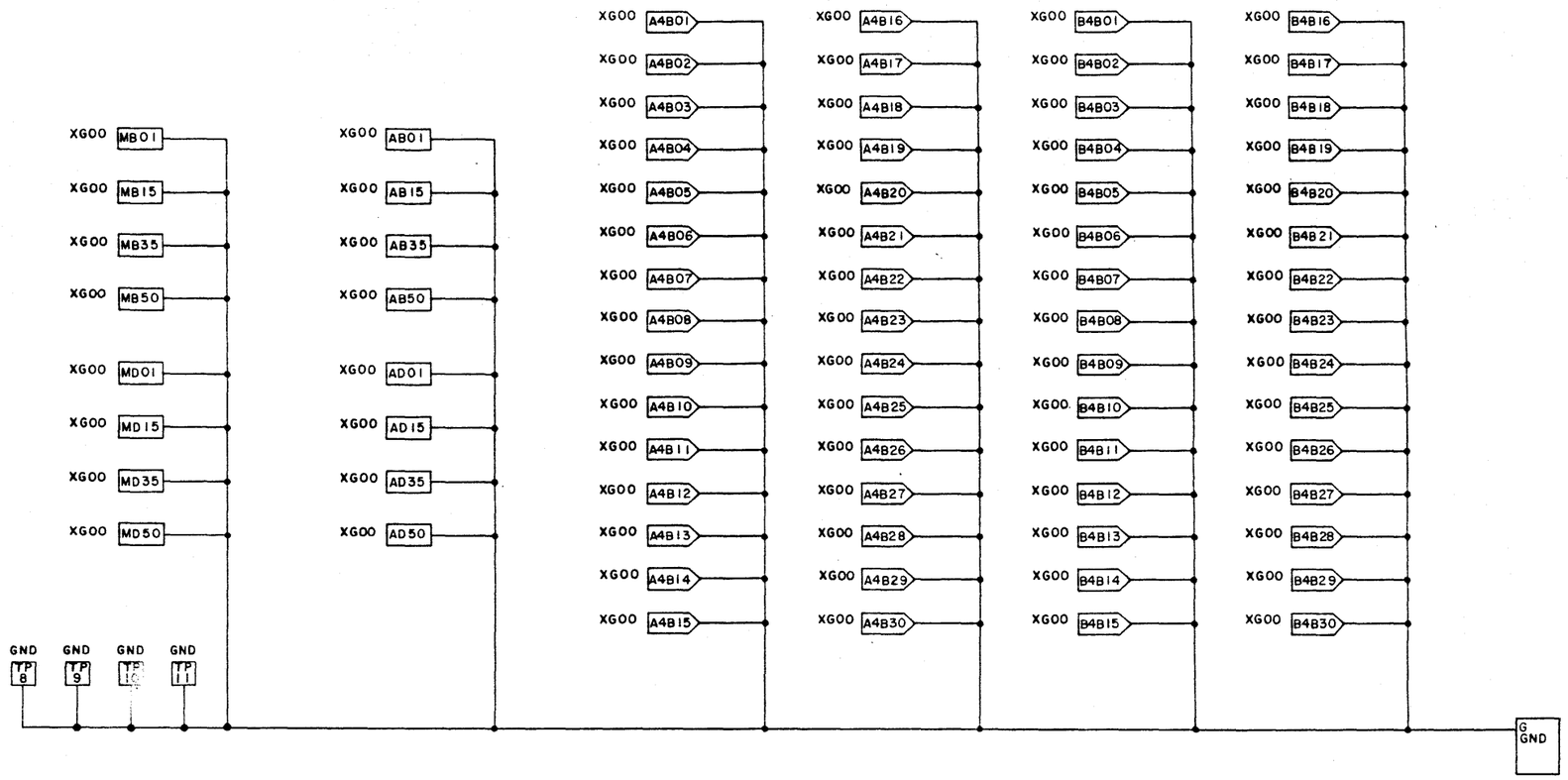
SHT 16/

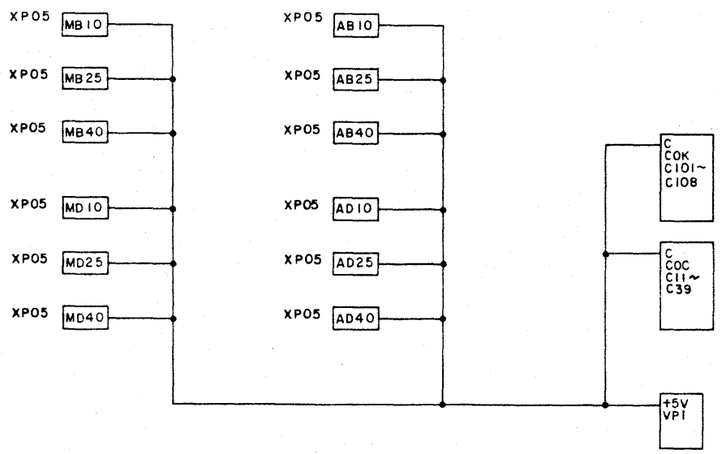
EQUIP

DB-413E
JIS A2 (420×594)

Nippon Electric Co.,Ltd.

134-190344-002-0





REV	COMP	DESCRIPTION(SC)	APP
1	0	1981.11.20	——
2	0	1982.11.22	
3	0	198	

DWG ABBR	STC
PKG LOCATION	IF1
PKG NAME	G9QYS

417

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口		今村	

MTA16X FORMATTER STC ADAPTER CIRCUIT DIAGRAM

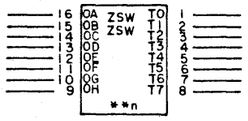
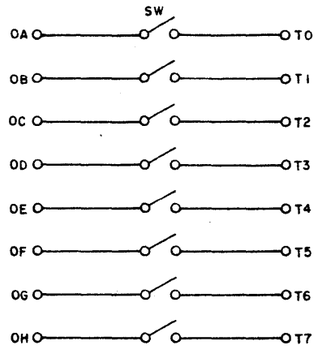
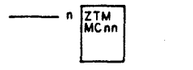
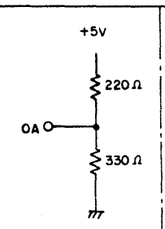
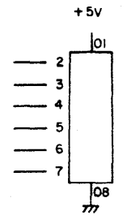
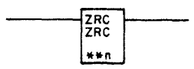
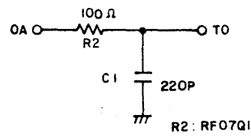
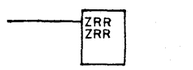
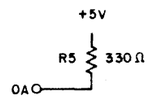
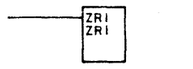
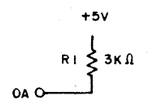
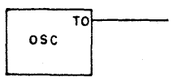
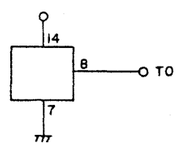
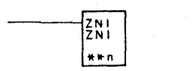
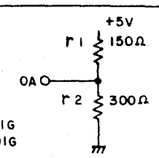
134-190344-002-0

NEC SHT 17

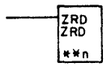
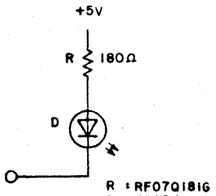
Nippon Electric Co.Ltd.

EQUIP

DB-413E
JIS A2 (420×594)

SYMBOL	DETAILED DIAGRAM
	
 nn : 1~13, 15, 16 18~21	  12D-8Z-220/330
	 R2 : RF07Q101G
	 R5 : RF07Q331G
	 R1 : RF07Q302G
	
	 Γ1--- RF07Q151G Γ2--- RF07Q301G

**n	Γ1	Γ2
**1	R8	R9
**2	R6	R7
**3	R3	R4

SYMBOL	DETAILED DIAGRAM
	 R : RF07Q181G D : SR104D

**n	D	R
1	D1	R13
2	D2	R12
3	D3	R11
4	D4	R10

REV	COMP	DESCRIPTION(SC)	APP
1	0	1981. 11. 20	——
2	0	1982. 11. 22	山口
3	0	[illegible]	

DWG ABBR	STC
PKG LOCATION	IF1
PKG NAME	G9QYS

418

NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE
	山口 青木		今村	

MTA16X FORMATTER STC ADAPTER CIRCUIT DIAGRAM

134-190344-002-0

NEC

SHT 18/18

Nippon Electric Co.Ltd.

134-190344-002-0

EQUIP

DB 413E
JIS A2 (420×594)