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I. SCOPE

This document describes the interface requirements for the PRIAM DISKOS 3350, 6650, 15450, 1070, 3450, and 7050 Winchester disc drives. For specific drive characteristics see Table 1; for additional product detail, reference the applicable product specifications.

II. APPLICABLE DOCUMENTS

Product Specification 3350, 6650, and 15450

Product Specification 3450 and 7050

Product Specification 1070

TABLE 1 - PRIAM DISKOS PRODUCT CHARACTERISTICS

MODEL	DISC DIAMETER (IN)	NO. OF DATA HEADS	NO. OF SERVO HEADS	DATA TRANSFER RATE (MB/SEC)	BYTES PER TRACK	BYTES PER CYLINDER	CYLINDER PER DRIVE	S BYTES PER DRIVE
3350	14	3	1	1.04	20,160	60,480	561	33,929, 280
6650	14	3	1	1.04	20,160	60,480	1121	67,677,012
15450	14	7	1	1.04	20,160	140,868	1121	157,913,028
3450	8	5	1	0.81	13,440	67,200	525	35,280,0 00
7050	8	5	1	0.81	13,440	67,200	1049	70,492,800
1070	8	4	None *	0.90	15,151	60,604	190	11,514,760

* Stepper Motor Controlled Positioner

III. GENERAL DESCRIPTION

PRIAM offers a basic 8-bit bidirectional bus control interface designed to be readily connected to popular 8-bit and 16-bit microprocessors. Across this interface all spindle motor and head positioning controls are passed.

Read and Write Data is passed via synchronous serial-bit NRZ signal lines. The interface provides INDEX, SECTOR MARK, READ/REFERENCE CLOCK, and WRITE CLOCK signals.

Up to four drives may be daisy chained along a single 50 conductor flat ribbon cable. Power is provided via a separate connector. Control switches and a Remote Panel Connector are provided on the PCB.

Each of these interface areas is discussed in detail in this specification for all DISKOS disc drive products.

A. Physical Interface

All drive signal connections are made via a single 50-pin ribbon cable connector. A second 50-pin connector is available for daisy chaining to another drive or for a terminator for the last drive in the string. Up to four drives may be daisy chained.

A separate connector for DC power is provided. However, if the optional power supply is installed, then its output is connected to this DC power connector and AC power must be supplied to the optional power supply.

Mini-dip type switches are provided on the PCB to select drive address, sector length, write protect functions and write clock control.

A dip socket output for remote write protect control and drive status is also provided on the PCB.

1. Interface Connectors

The interface connectors are 50-pin ribbon cable connectors and provide for interface cable and terminator connections. The pins are numbered 1 through 50. A recommended mating connector is Spectra-Strip 802-050-004 or Scotchflex 3425-0000. The lines are described at the drive end in Table 2.

TABLE 2 - Interface Connectors

<u>Pin</u>	Signal		Line Type
1	Ground		Ground
2	+ DBUS 0		Bi-Dir/Single
3	+ DBUS 1		Bi-Dir/Single
4	+ DBUS 2		Bi-Dir/Single
5	+ DBUS 3		Bi-Dir/Single
6	+ DBUS 4		
7	+ DBUS 5		Bi-Dir/Single
8	+ DBUS 6		Bi-Dir/Single
9	+ DBUS 7		Bi-Dir/Single
10			Bi-Dir/Single
	Ground		Ground
11	- READ GATE		Received/Single
12	Ground		GND
13	- RESET		Received/Single
14	Ground		GND
15	- WRITE GATE		Received/Single
16	Ground		GND
17	- RD		Received/Single
18	- WR		Received/Single
19	+ AD 1		Received/Single
20	+ AD 0		Received/Single
21	Ground		GND
22	- DRIVE SELECT 1		Received/Single
23	- DRIVE SELECT 2		Received/Single
24	- DRIVE SELECT 3		Received/Single
25	- DRIVE SELECT 4		Received/Single
26	Ground		Ground
27	Ground		Ground
28	+ 5 VOLTS DC (TERMINATOR	POWER)	Diode or'd/Single
29	- HEAD SELECT 4		Received/Single
30	- HEAD SELECT 2		Received/Single
31	- HEAD SELECT 1		Received/Single
32	Ground		GND
33	- INDEX		Transmitted/Single
34	Ground		GND
35	- READY		Transmitted/Single
36	Ground		GND
37	- SECTOR MARK		Transmitted/Single
38	Ground		GND
39	+ WRITE DATA		Received/DIFF
40	- WRITE DATA		Received/DIFF
41	Ground		GND
42	+ WRITE CLOCK		Received or
			Transmitted/DIFF
43	- WRITE CLOCK		Received or
			Transmitted/DIFF
44	Ground		GND
45	+ READ/REFERENCE	CLOCK	Received or
			Transmitted/DIFF
46	- READ/REFERENCE	CLOCK	Received or
			Transmitted/DIFF
47	Ground		GND
48	+ READ DATA		Transmitted/DIFF
49	- READ DATA		Transmitted/DIFF
50	Ground		GND

2. DC Power Connector

This connector is used to supply DC power to the drive which mates to the optional power supply. It is a 6-pin AMP MATE-N-LOK Connector, and the recommended mating connector is an AMP 1-480270-0 socket using AMP 60619-1 pins.

DC POWER CONNECTOR

PIN	VOLTAGE
1	GND
2	-5 VDC
3	+5 VDC
4	GND
5	-12 VDC
6	+24 VDC

3. AC Power Connector

This is a 3-pin connector used to supply AC power to the drive when the optional power supply is used. The mating connector is Belden 5PH-386 or equivalent.

AC POWER CONNECTOR

PIN	VOLTAGE
L	110 or 220 VAC (HOT)
Е	FRAME GROUND
N	110 or 220 VAC (COMMON)

4. Remote panel Connector (3350, 6650 & 15450 only)

This is an 8 pin DIP socket connector; it provides limited remote sensing and control as described below.

REMOTE PANEL CONNECTOR

PIN		VOLTAGE
1	_	WRITE PROTECT (CONTROL)
2		FAULT RESET (CONTROL)
3	-	READY (STATUS)
4		GROUND
5	-	BZY (STATUS)
6	-	FAULT (STATUS)
7		RESERVED
8	+	5VDC

5. Switches

The following switch functions are provided on the drive PCB: (See tables 14 and 15 for more detailed controls).

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Select Drive Address 1 (A11 Drives) Select Drive Address 2 (A11 Drives) Select Drive Address 3 (A11 Drives) Select Drive Address 4 (A11 Drives) Sector/track, Sector length - Bit 1,16 (3450, 7050, 3350, 6650, 15450) Sector/track, Sector length - Bit 2,32 (3450, 7050, 3350, 6650, 15450) Sector/track, Sector length - Bit 4,64 (3450, 7050, 3350, 6650, 15450) Sector/track, Sector length - Bit 8,128 (3450, 7050, 3350, 6650, 15450) Sector/track, Sector length - Bit 16,256 (3450, 7050, 3350, 6650, 15450) Sector/track, Sector length - Bit 32,512 (3450, 7050, 3350, 6650, 15450) Sector/track, Sector length - Bit 32,512 (3450, 7050, 3350, 6650, 15450) Sector/track, Sector length - Bit 64,1024 (3450, 7050, 3350, 6650, 15450) Sector/track, Sector length - Bit 64,1024 (3450, 7050, 3350, 6650, 15450) Write Clock Transmit (3450, 7050, 3350, 6650, 15450) Write Protect (3450, 7050, 3350, 6650, 15450) Write Clock Phase (3450, 7050, 3350, 6650, 15450) Skip Defect Write (3450, 7050, 3350, 6650, 15450) Sectors/track, Sector Length - Bit 1 (1070 only) Sectors/track, Sector Length - Bit 2 (1070 only)
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Write Protect Head 1 (1070 only)
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Write Protect Head 2 (1070 only)
Write Protect Head 3 (1070 only)

6. Ground Strap

A braided #14 ground strap connected to the drive chassis, the controller chassis, and DC ground common connection, preferably in close proximity to the interface cable DC ground connection is recommended. (See Figures 1, 2 and 3.)

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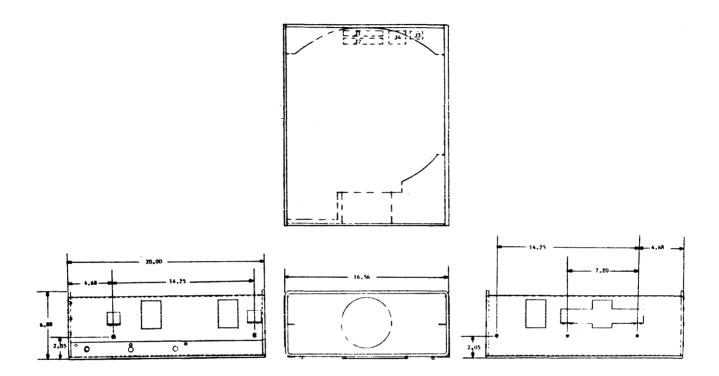


Figure 1 - DISKOS 3350, 6650, and 15450 Disc Drives

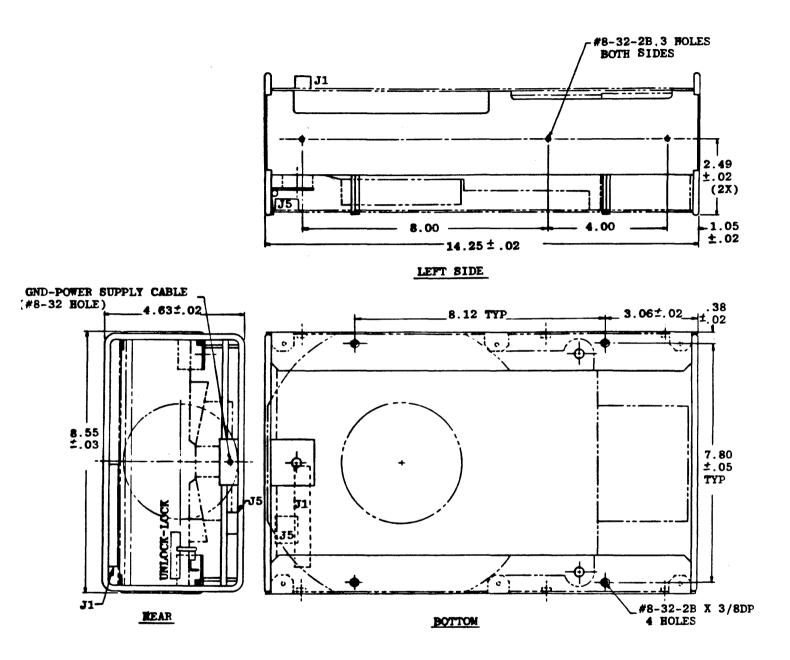


Figure 2 - DISKOS 3450 and 7050 Disc Drives

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and a second second

Figure 3 - DISKOS 1070 DISC DRIVE

NOTES:

1. For rack-mounting, MOUNTING HOLES (six places) are used.

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2. Use of a cooling fan is recommended to assure highest reliability.

B. Interface Signals

Following is an electrical description of each interface signal.

1. +DBUS 0-7

A high active 8-bit wide bus is used to transfer commands and status (carriage control and interface) between drive and controller. These lines connect directly to an 8304B (or 8286) bus transceiver as shown in Figure 4. DC Characteristics are shown in Table 3.

If long cables are used, these lines should be terminated at each end.

2. + ADO-1

A high active 2-bit wide address bus, whose function is to select one of three registers in which data is stored or from which it is read. These lines connect directly to a 74LS244 Schmitt-Triggered Receiver enabled by DRIVE SELECTED as shown in Figure 5. The DC Characteristics are shown in Table 4.

If long cables are used, these lines should be terminated at the drive end. PRIAM provides an optional terminator.

3. – RD

This low active signal is used to gate the contents of the selected register (decode of AD1,AD0) onto the DBUS. This line is connected to a 74LS244 as shown in Figure 5. Also, the DC characteristics are listed in Table 4.

Long cables should be terminated at the drive end. PRIAM provides an optional terminator (Figure 7).

4. - WR

This low active signal is used to gate the contents of the DBUS into the selected register. This line is connected to a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4.

Long cables should be terminated at the drive end. PRIAM provides an optional terminator (Figure 5).

5. - RESET

This low active signal resets the drive logic. If the drive is sequenced down when RESET occurs it will remain sequenced down. If the drive is sequenced up, it will remain up and the carriage will RESTORE to Cylinder Zero. This line is connected to a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4.

Long cables should be terminated at the drive (Figure 5).

6. - DRIVE SELECT 1-4

These low active signals enable drive response. No reading, writing, register selection, or command response will occur unless the drive is selected. These single-ended receiver lines are shown in Figure 6. Long cables should be terminated (Figure 6). DC Characteristics are shown in Table 5.

7. -HEAD SELECT 1-2

These low active signals are used to select the desired head for reading or writing. The head selection decoding is shown in Table 16. These lines are connected to a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4.

Long cable connections should be terminated (Figure 5).

8. -READY

This low active signal from the drive indicates that it is up to speed and ready to read, write or seek. It is driven by a 75462 open collector driver as shown in Figure 7. DC characteristics are shown in Table 6.

9. - INDEX

This low active signal occurs once per revolution and indicates the beginning of a track. It is driven by a 75462 open collector driver as shown in Figure 7 and has the DC characteristics listed in Table 6. This line must be terminated at the controller.

10. - SECTOR MARK

This low active signal indicates the beginning of a sector. It is driven by a 75462 open collector driver as shown in Figure 7 and has the DC characteristics listed in Table 6. This line must be terminated at the controller.

11. -WRITE GATE

This low active signal enables the writing of data by the selected head. This signal is received by a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4. Long cable connections should be terminated at the drive (Figure 5).

12. -READ GATE

This low active signal initiates synchronization of the drive's phase lock loop for data separation. READ GATE must be enabled during a gap. This signal is received by a 74LS244 as shown in Figure 5 and its DC characteristics are listed in Table 4. Long cable connections should be terminated at the drive (Figure 5).

13. +, - WRITE DATA

WRITE DATA is an NRZ serial data signal synchronous with WRITE CLOCK. It is received by a RS422 type differential line receiver section as shown in Figure 8.

14. +, - WRITE CLOCK

This signal is switch selectable and may be either a square wave signal from the controller which is phase locked to the WRITE DATA. Or, if the switch is set in the other position, WRITE CLOCK is a square wave signal from the drive to the controller to provide clocking and synchronization for WRITE DATA. The controller should be designed so that WRITE DATA is stable at the drive connector during the positive transition of WRITE CLOCK. It is received by a RS422 type differential line receiver as shown in Table 7 and Figure 8. These lines should be terminated. If long cables are used, cable delays must be considered.

15. +, - READ/REFERENCE CLOCK

This square wave signal provides clocking and synchronization for reading and writing data. It is derived from either the servo clock or the VFO synchronized to the READ DATA signal. It is driven by an RS442 type differential line driver as shown in Figure 8 and its DC characteristics are listed in Table 8.

16. +, - READ DATA

This serial NRZ signal is used to transmit data from the drive to the controller. This output is valid 9 microseconds after READ GATE is enabled. It is driven by a RS422 type differential line driver as shown in Figure 8 and its DC characteristics are listed in Table 8.

TABLE 3 - DBUS DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
v _{ol}	Output Low Level		0.5	v	I _{OI.} = 32 MA
VOL	Output High Level	2.4	0.9	v	$I_{OH} = -5 MA$
IOFF	Output Off Current		-0.2	mA	$V_{OFF} = 0.45 V$
			+0.2	mA	$V_{OFF} = 5.25 V$
VIL	Input Low Level		0.9	v	
VIH	Input High Level	2.0		v	1

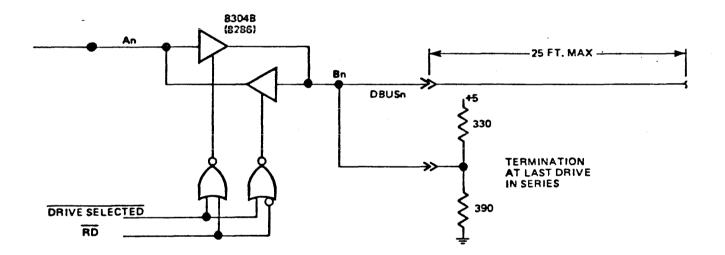


Figure 4 - DBUS Transceiver

TABLE 4 - Single End Line Receiver Gated by Drive Select DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
VIH	Input High Level	2		v	
V _{IL} I _{IH}	Input Low Level High Level Input		0.8	V	
I _{IL}	Current Low Level Input		0.02	mA	$V_{I} = 2.7V$
TD	Current		-0.2	mA	$V_{I} = 0.4V$

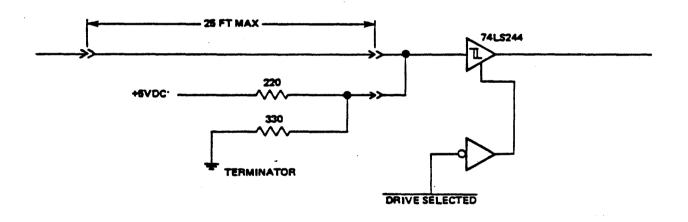


Figure 5 - Single End Line Receiver Gated By Drive Select

Symbol	Parameter	Min	Max	<u>Units</u>	Test Conditions
V _{T+}	Positive-going				
1+	threshold	1.4	1.9	V	:
v _{r-}	Negative-going				
-	threshold	0.5	1	V	
IIH	High level input				
	current		.020	mA	$V_{I} = 2.7V$
IIL	Low level input current		-0.400	mA	$v_{I} = 0.4v$

TABLE 5 - Single End Line Receiver DC Characterisitcs

Long cable connections should be terminated at the drive.

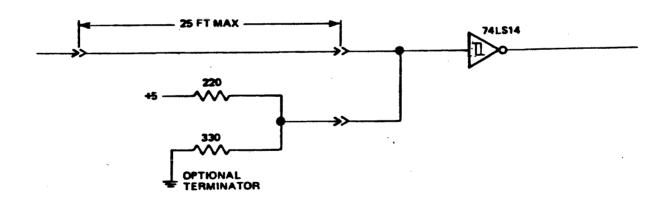


Figure 6 - Single End Line Receiver

TABLE 6 - Single End Line Driver DC Characteristics

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Symbol	Parameter	Min	Max	Units	Test Conditions
T	Wich land outside				
I _{OH}	High level output current		0.10	mA	
IOL	Low level output current	300		mA	
VOL	Low level output				
	voltage		0.8	V	$I_{OL} = 300 \text{mA}$

This line must be terminated at the controller.

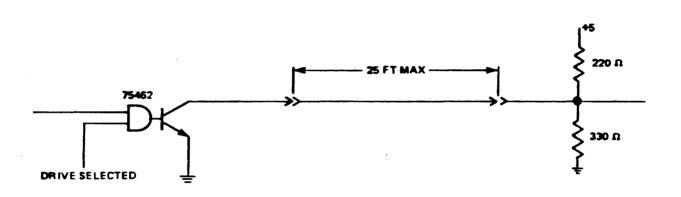


Figure 7 - Single End Line Driver

TABLE 7 - Differential Line Receiver DC Characteristics

Symbol	Parameter	Min	Max	<u>Units</u>	Test Conditions
v _{TH}	Differential input				
VICR	high-threshold Common-mode input	+15 to	0.2	V	
·ICK	range	-15		v	
I _{I(REC)}	Receiver input				
	current		2.3	mA	

TABLE 8 - Differential Line Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V _{OH}	High level output voltage	2.5		v	$I_{OH} = -20 mA$
VOL	Low level output voltage		0.32	v	$I_{OL} = 20 mA$
IOZ	Off-state (non- selected) output				
	current		<u>+</u> 0.02	mA	
loh	High-level output current		-20	mA	
IOL	Low-level output		20	mA	
IOS	Short circuit output current	-30	-150	mÂ	

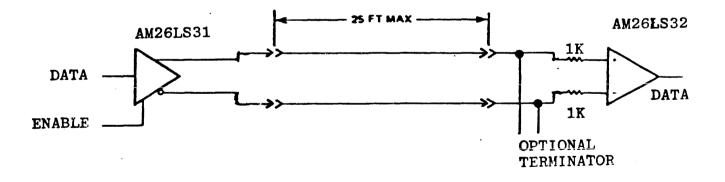


Figure 8 - Differential Line Drivers & Receivers

The DC characteristics are listed in Table 7 and 8. The last drive in a string should be terminated with P/N 200028.

C. Address and Command Control

1. Address, status and command registers

All cylinder addresses, status information and commands are transferred over a three-state bidirectional DBUS 0 through 7 lines. These eight lines present an open circuit (tri-state) to the controller's bus until activated by DRIVE SELECT. An active DRIVE SELECT combined with RD (Read) sets the DBUS into the transmit mode while DRIVE SELECT combined with an active WR (Write) sets the DBUS into the receive mode. The information to control the drive resides in six accessible 8-bit registers.

- a. <u>Control Command Register</u> which receives and stores commands from the controller;
- <u>Target Address Register Upper Byte</u> which receives the eight most significant bits of the desired cylinder address;
- c. <u>Target Address Register Lower Byte</u> which receives the eight least significant bits of the desired cylinder address;
- d. <u>Status Register</u> which contains pertinent information about present operation;
- e. <u>Current Address Register Upper Byte</u> which contains the eight most significant bits of the current cylinder address;
- f. <u>Current Address Register Lower Byte</u> which contains the eight least significant bits of the current cylinder address.

2. Accessing of the registers is accomplished by a combination of active levels on DRIVE SELECT, RD, or WR, and register address lines Al and AO, as shown in Table 9. The Command and Target Address Registers can only receive information and the Status and Current Address Registers can only transmit information.

TABLE 9 - Register Selection

A1	A0	WR	RD	Selected Register
0	0	1	0	Status Register
0	0	0	1	Command Register
0	1	1	0	Current Address-Upper Byte
0	1	0	1	Target Address-Upper Byte
1	0	1	0	Current Address-Lower Byte
1	0	0	1	Target Address-Lower Byte

3. Control Commands

Seven Control Commands are used. All are single byte commands and are listed in Table 10.

TABLE 10 - Command Summary

BITS								
Command	7	6	5	<u>4</u>	3	2	1	0
SEQUENCE UP	0	0	0	0	0	0	0	1
SEQUENCE DOWN	õ	õ	Õ	õ	Õ	Õ	1	ō
RESTORE	Õ	Õ	Õ	Õ	Õ	Õ	1	1
SEEK	Ō	0	Ō	0	0	1	0	0
FAULT RESET	0	0	0	0	0	1	0	1
READ DRIVE ID	0	0	0	1	0	0	0	0
READ BYTES PER								
SECTOR	0	0	0	1	0	0	0	1

a. SEQUENCE UP

The SEQUENCE UP Command causes the disc drive spindle motor to power up. The rotational speed of the disc is monitored, and after the drive is up to speed, a position signal calibration is performed (except for the 1070) and the heads are positioned to cylinder zero. The drive will present BUSY status while the SEQUENCE UP is in process. CYLINDER ZERO, SEEK COMPLETE and READY status is set at the successful completion of this command. WRITE PROTECT and DRIVE FAULT are set if the SEQUENCE UP was unsuccessful. The drive will also sequence up as described with a RESTORE command.

b. SEQUENCE DOWN

The SEQUENCE DOWN command causes the heads to be positioned to the landing zone and the spindle motor is braked to a stop. WRITE PROTECT status will be set at the completion of this command.

c. RESTORE

The RESTORE command causes the drive carriage to be repositioned to cylinder zero. The drive RESTORES automatically on SEQUENCE UP, or when a SEEK FAULT is detected. Upon failure of the RESTORE command, the heads will be positioned to the landing zone area and DRIVE FAULT status will be set. If the drive is not sequenced up, the restore command will result in the drive sequencing up and drive carriage positioned to cylinder zero.

d. SEEK

The SEEK command uses the contents of the Target Address Registers for desired cylinder address information. Upon receipt of this command, the drive will go NOT READY and BUSY while moving the carriage to the desired cylinder. When this is complete, the drive will again become READY and SEEK COMPLETE status will be posted. Upon failure of the SEEK command, the drive will RESTORE to cylinder zero and present READY, CYLINDER ZERO and SEEK FAULT status.

e. FAULT RESET

The FAULT RESET command clears both fault condition flip-flops (SEEK FAULT and DRIVE FAULT).

f. READ ID

This command sets the Drive ID code in the Current Address Register. READY status will be reset to the not ready state. In order to bring the drive to the READY state a SEQUENCE UP or RESTORE command must be executed. Thus, the Current Address Register contains the valid current cylinder address if the drive is READY and last requested parameter information if not READY. The drive ID assignment is shown in Table 11.

TABLE 11 - Drive ID Assignment

ID Code (HEX)	Drive Designation
00	Invalid
01	DISKOS 3350-01 or -10 (20, 160 bytes/track)
02	DISKOS 3350-01 (19,960 bytes/track)
03	DISKOS 3450 (12,960 bytes/track)
04	DISKOS 3450 (13,440 bytes/track)
05	DISKOS 7050 (13,440 bytes/track)
06	DISKOS 6650
07	DISKOS 15450
08-0F	Reserved
10	Reserved
11	DISKOS 1070-1
12	CD8005
13	CD8010
14	Reserved
15	DISKOS 1070-2
16-1F	Reserved
20-FF	Reserved

g. READ BYTES PER SECTOR

This command reports the bytes per sector selected by the switches mounted on the drive. The sector size is reported in the Current Address Registers.

Upon the receipt of this command the drive will become not READY and remain in the not READY state until a Sequence Up or Restore command is received and executed.

See Tables 14 and 15 for the various sector size selection available on each drive.

4. Current and Target Address Register Bit Definitions

Table 12 is a definition of the various bits in the Current Address Registers and Target Address Register.

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TABLE 12 - Address Register Bit Definition

Data Bus Bit	<u>7</u>	<u>6</u>	<u>5</u>	<u>4</u>	<u>3</u>	2	<u>1</u>	<u>0</u>			
Current Address Reg. Upper Byte	0	0	0	0	0	c ₁₀	Cg	с ₈			
Current Address Reg. Lower Byte	C7	С ₆	C ₅	C4	C3	C ₂	C_1	с _о			
Target Address Reg. Upper Byte	0	0	0	0	0	с ₁₀	Cg	Cg			
Target Address Reg. Lower Byte	с ₇	c ₆	С₅	C4	C3	с ₂	c ₁	c ₀			
where for cylinder addre	ess										
	c ₁₀	Cg	C8	с ₇	c ₆	C ₅	C4	Сз	c ₂	c_1	c ₀
Cylinder 000	0	0	0	0	0	0	0	0	0	0	0
Cylinder 001 : :	0	0	0	0	0	0	0	0	0	0	1
Cylinder 1123	1	0	0	0	1	1	0	0	0	1	1
and for sector length address											
Sector Length 000	0	0	0	0	0	0	• 0	0	0	0	0
Sector Length 001 : :	0	0	0	0	0	0	0	0	0	0	1
Sector Length 1,316	1	0	1	0	1	0	1	0	0	0	0

5. The following is a definition of the various bits of the Status Register.

TABLE 13 - Status Register Bit Definition

<u>Bit</u>	Name	Description
0	READY	The drive is up to speed, servo system is locked onto a servo track, and the unit is in a state to read, write, or seek.
1	SEEK COMPLETE	This bit is set when seek operation is completed. This status is invalid while BUSY is active.
2	SEEK FAULT	A fault was detected during a seek operation. This status is invalid while BUSY is active.
3	CYLINDER ZERO	Access arm is set to Cylinder 0. This status is invalid while BUSY is active.
4	BUSY	Drive is in process of executing a command.
5	DRIVE FAULT	A fault was detected during a write operation or a drive unsafe condition was detected.
6	WRITE PROTECT	The head selected is write protected. Write protection is set by switches in the drive or when the drive is not sequenced up.
7	COMMAND REJECT	Control or Register Load command received while drive is not ready, or improper command received. This status is invalid while BUSY is active.

D. Serial Data Transfer

Several individual signal lines provide timing and status information to facilitate the serial data transfer between the drive and controller. These signals are:

1. INDEX

A pulse that occurs whenever the servo track index mark is encountered to indicate the beginning of a track. The timing is discussed in the timing section.

2. READY

This signal indicates that the selected drive is ready to read, write, or seek. When this line is false, WRITE, READ and SEEK commands should not be initiated by the controller. However, READY will go false whenever a SEEK command is initiated.

READY will be true when the drive is at speed, the carriage is positioned on the cylinder expected and no fault condition exists.

3. SECTOR MARK

Sector Mark is a pulse that occurs at the beginning of each sector. Sector size is selectable by setting mini-dip switches on the drive.

a. For the DISKOS 1070 drive, two mini-dip switches are provided to select sector length (or sectors per track) as shown in Table 14.

TABLE 14 - DISKOS 1070 Sector Length

SW RSW-1	SW RSW-2	Sector Length
On	On	3450 Bytes (44 Sectors/Track)
Off	On	680 Bytes (22 Sectors/Track)
On	Off	1360 Bytes (11 Sectors/Track)

b. For the DISKOS 3450, 7050, 3350, 6650 and 15450 drives, 8 position mini-dip switches are provided to select sector length or bytes per sector depending upon switch position 8 setting as shown in Table 15.

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TABLE 15 - DISKOS 3450, 7050, 3350, 6650 & 15450 Sector Length

Sector Sw Position	Position 8 Closed Bytes/Sector *	Position 8 Open Sectors/Track **
1 Closed	16	1
2 Closed 3 Closed	32 64	2 4
4 Closed	128	8
5 Closed 6 Closed	256 512	16 32
7 Closed	1,024	64
1-7 Open	2,048	128

* to calculate sectors per track with position 8 closed

use:	Sectors/Track	=	Bytes/Track - 36
			Bytes/Sector

** to calculate bytes per sector with position 8 open

use:	Bytes/Sector =	=	Bytes/Track - 36
			Sectors/Track

4. Head Select 1, Head Select 2 and Head Select 4.

These low active signals are gated by drive select and are used to select the head as defined in Table 16.

TABLE 16 - Head Selection

Head	Head	Head	Selected Head	l		
Sel	Sel	Sel	3350		7050	
	_2	_4	6650	1070	3450	15450
High	High	High	Zero	Zero	Zero	Zero
Low	High	High	One	One	One	One
High	Lo	High	Two	Two	Two	Two
Low	Low	High	Zero*	Three	Three	Three
High	High	Low	Zero*	Zero*	Four	Four
Low	High	Low	One*	One*	Zero*	Five
High	Low	Low	Two*	Two*	Zero*	Six
Low	Low	Low	Zero*	Three*	Zero*	Zero*

* Selected by default because of head select range/heads available.

5. WRITE GATE

WRITE GATE enables data to be written on the disc when in the active state. READY must be valid before signaling WRITE GATE. An attempt to write between INDEX and the first SECTOR MARK will result in a DRIVE FAULT because the prerecorded skip defect information is write protected. DRIVE FAULT will be set if any of the following error conditions occur during writing.

TABLE 17 - Drive Fault Conditions

- 1 WRITE GATE without write current at the head
- 2 Write current at the head without WRITE GATE
- 3 WRITE GATE without READY *
- 4 More than one head selected
- 5 No transitions during write *
- 6 WRITE GATE with WRITE PROTECT *
- 7 Spindle Speed Error *
- 8 RESET while drive Sequenced Up *
- 9 Off-Track condition when track following (READY) *
- 10 Failure to Restore *
- 11 Software Error (Watch-dog timer time out). *

* all drives except the 1070

6. WRITE CLOCK

Provides clocking and synchronization for WRITE DATA. WRITE CLOCK is generated by the controller by echoing the REFERENCE CLOCK signal back to the drive through a similar delay path. Thus, it is at the same frequency and with a phase delay similiar to WRITE DATA. The timing of these signals is shown in the timing section.

7. WRITE DATA

Provides the data to be stored on the track. The required format is NRZ (non-return to zero). READ/REFERENCE CLOCK (received from the drive) is used by the controller to clock WRITE DATA on the positive edge. READ/REFERENCE CLOCK is retransmitted back to the drive as WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe WRITE DATA into the drive's encoder circuitry. Detailed timing diagrams are shown in the timing section.

8. READ GATE

This signal must be enabled in a gap area (all 0's recorded) and at least 9 microseconds before the sync byte. READ GATE enables the VFO clock to synchronize with the information from the read head. Raising READ GATE during a data record may cause the VFO to spuriously lock in incorrect phase relationship for correct decoding of recorded information.

Six microseconds after the leading edge of READ GATE the READ CLOCK is selected for the READ/REFERENCE CLOCK signals.

9. READ/REFERENCE CLOCK

Provides clocking and synchronization for reading and writing data. When READ GATE is not active this signal is the REFERENCE CLOCK which is derived from the servo track information.

Six microseconds after the leading edge of READ GATE, READ/REFERENCE CLOCK is switched to the VFO clock which is phase locked to READ DATA. A change in the READ/REFERENCE CLOCK phase will occur when it is switched between the servo and VFO clocks.

10. READ DATA

Data from the drive are in serial bits NRZ (non-return to zero) form and are synchronized with READ/REFERENCE CLOCK after a six microsecond delay from the leading edge of READ GATE. READ DATA may not be valid for the first 9 microseconds after READ GATE is enabled.

E. Timing

In the following section, timing requirements are discussed.

•

1. REGISTER TIMING

Register load timing is shown in Figure 9 and the AC characteristics are listed in Table 18.

TABLE 18 - Register Load AC Characteristics

Symbol	Parameter	Min	Max	Units
t _{AW}	Address stable before WR	60		ns
tWA	Address hold time for WR	30		ns
^t ww	WR pulse width	100		ns
t _{DW}	Data set up time for WR	60		ns
t _{WD}	Data hold time for WR	30		ns
t _{RV}	Recovery time between WR	200		ns

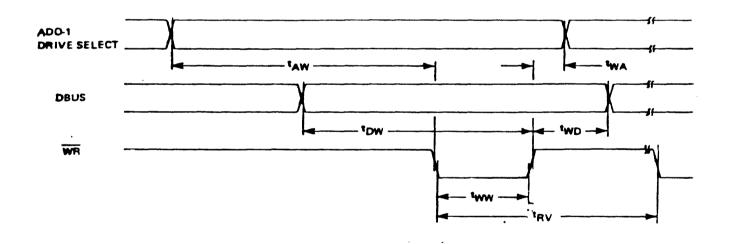
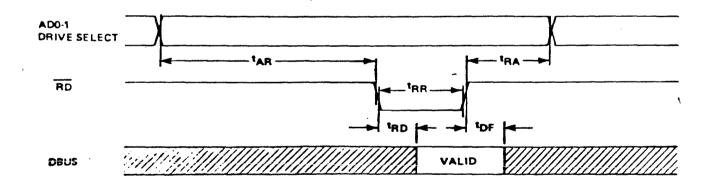


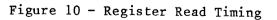
Figure 9 - Register Load Timing

Register read timing is shown in Figure 10 and the AC characteristics are listed in Table 19.

Symbol	Parameter	Min	Max	Units
t _{AR}	Address stable before RD	60		ns
^t RA	Address hold time for RD	30		ns
t _{RR}	RD pulse width	100		ns
t _{RD}	Data delay from RD		60	ns
tDF	RD to data floating	10	40	ns

TABLE 19 - Register Read AC Characteristics





2. RESET TIMING

RESET timing is shown in Figure 11 and the AC characteristics are listed in Table 20.

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TABLE 20 - Reset AC Characteristics

Symbol	Parameter	Min	Max	Units
t _{RST}	Reset pulse width	100		ms
t _{SR}	DRIVE SELECT to RESET	0		ns

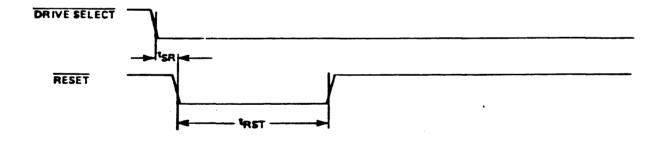


Figure 11 - Reset Pulse Width Timing

3. INDEX SECTOR MARK TIMING

INDEX and SECTOR MARK timings are shown in Figure 12 and their AC characteristics are listed in Table 21.

TABLE 21 - Index and Sector Mark AC Characteristics

Symbol	Parameter		Timing		Units
		3350	3450 &	1070	
		6650 &	7050		
		15450			
t	INDEX Pulse Width	1 00, 10	0 / 0 - 05	1 0 . 2	
t _{IW}		1.92+.19	2.48+.25	1.9+.3	us
t _{IR}	INDEX Period	19.35+.5	16.67 <u>+</u> .4	16.67 <u>+</u> .4	ms
t _{SW}	SECTOR MARK Pulse Width	960 <u>+</u> 140	1240+160	960 <u>+</u> 140	ns
t _{IS}	INDEX to First SECTOR	30.7 <u>+</u> 4.7	44.6 <u>+</u> 1.4	187 <u>+</u> 8 us	
^t sr*	Sector Width	*	*	*	
t BYTE	Byte Period	960 <u>+</u> 144	1240 <u>+</u> 184	1112 <u>+</u> 80	ns

* t_{SR} = (Sector size in bytes) X t_{BYTE} ns) + 10%

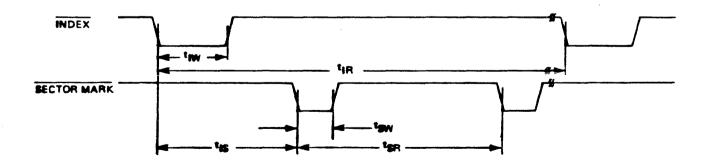


Figure 12 - INDEX and SECTOR MARK Timing

4. WRITE DATA AND CLOCK TIMING

WRITE DATA and WRITE CLOCK timing relationship is shown in Figure 13 and their AC characteristics are listed in Table 22.

TABLE 22 - Write Data and Write Clock AC Characteristics

Symbol	Parameter		Timing		Units
		3350	3450 &	1070	
		6650 &	7050		
		15450			
^t CLK	WRITE CLOCK period	120+18	155+23	139+11	ns
tWH	WRITE CLOCK				
	high pulse width	60+9	77.5+12.5	69.5+5.5	ns
t _{WL}	WRITE CLOCK low pulse width	60 <u>+</u> 9	77.5 <u>+</u> 12.5	69.5 <u>+</u> 5.5	ns
t _{BIT}	WRITE DATA bit period	120 <u>+</u> 18	155 <u>+</u> 23	139 <u>+</u> 11	ns
^t DC	WRITE DATA setup time	20*	20*		ns min
^t CD	WRITE DATA hold time	20*	20*		ns min

* 60 ns is typical

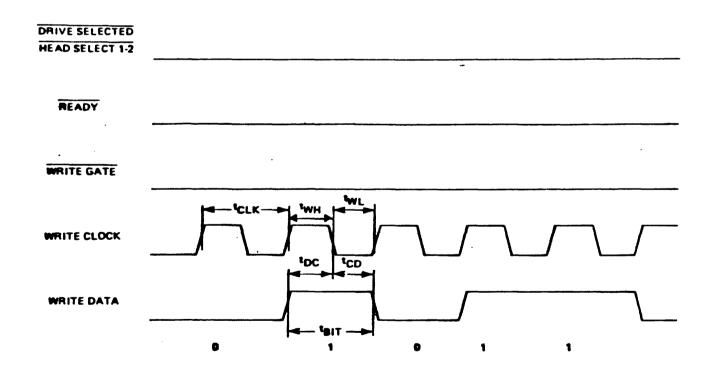


Figure 13 - WRITE DATA and WRITE CLOCK Timing

5. READ DATA AND READ CLOCK TIMING

READ DATA and READ CLOCK timing relationship is shown in Figure 14 and their AC characteristics are listed in Table 23.

TABLE 23 - Read Data and Read Clock AC Characteristics

Symbol	Parameter		Timing		Units
		3350	3450 &	1070	
		6650 &	7050		
		15450			
t _{CLK}	READ CLOCK period	120+18	155+23	139+11	ns
t _{WH}	READ CLOCK	120-10	100-20	10,111	110
W11	high pulse width	60+9	77.5+12	69.5+5.5	ns
t _{WL}	READ CLOCK low pulse width	60+9	77.5+12	69.5+5.5	ns
t _{BIT}	READ DATA bit period	120 <u>+</u> 18	155+23	139 <u>+</u> 11	ns
t _{DC}	READ DATA setup time	40*	40*		ns min
t _{CD}	READ DATA hold time	40*	40*		ns min
t _{BYTE} B	yte period	960 <u>+</u> 144	1240 <u>+</u> 184	1112 <u>+</u> 80	ns
* 60 ns	is typical				

DRIVE SELECT

HEAD SELECT 1-2-4

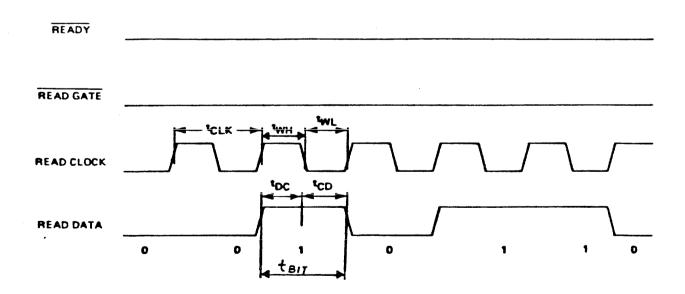


Figure 14 - READ DATA and READ CLOCK Timing

6. RECORD WRITING

Figure 15 shows timing requirements for writing full sectors (ID and data fields) and also for writing sector data fields only. Their AC characteristics are listed in Tables 24 and 25.

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TABLE 24 - Record Writing Control AC Characteristics for DISKOS 1070

Symbol [missing]	Parameter	Min	<u>Typ</u>	Max	Units
t _{SH}	DRIVE SELECTED to HEAD				
bii	SELECTED			500	ns
t _{SR}	DRIVE SELECTED to READY			150	ns
^t SG	SECTOR MARK TO WRITE GATE	-1	0	1	us
t _{IDG}	ID gap timing	20			us
t _{IDF}	ID fill	1			us
t _{DG}	Data gap (no Write to				
	read transitions	8			us
^t DF	Data fill	1			us
t _{HW}	Head Select to WRITE GATE	100			ns

TABLE 25 - Record Writing Control AC Characteristics for DISKOS 3450, 7050, 3350, 6650 & 15450

Symbol	Parameter	Timing		Units
		3350	3450 &	
		6650 &	7050	
		15450		
t _{SH}	DRIVE SELECTED to HEAD			
Ull	SELECTED	20	20	us min
t _{SR}	DRIVE SELECTED to READY	100	100	ns min
t _{SG}	SECTOR MARK TO WRITE GATE	0+1	0+1	us
t _{IDG}	ID gap timing	23	23	Bytes min
t _{IDF}	ID fill	2	2	Bytes min
tDG	Data gap (no Write to			-
	read transitions	11	11	Bytes min
t _{DF}	Data fill	2	2	Bytes min
t _{HW}	Head Select to WRITE GATE	100	100	ns
tBYTE	Time for 1 byte	960 <u>+</u> 144	1240 <u>+</u> 184	ns

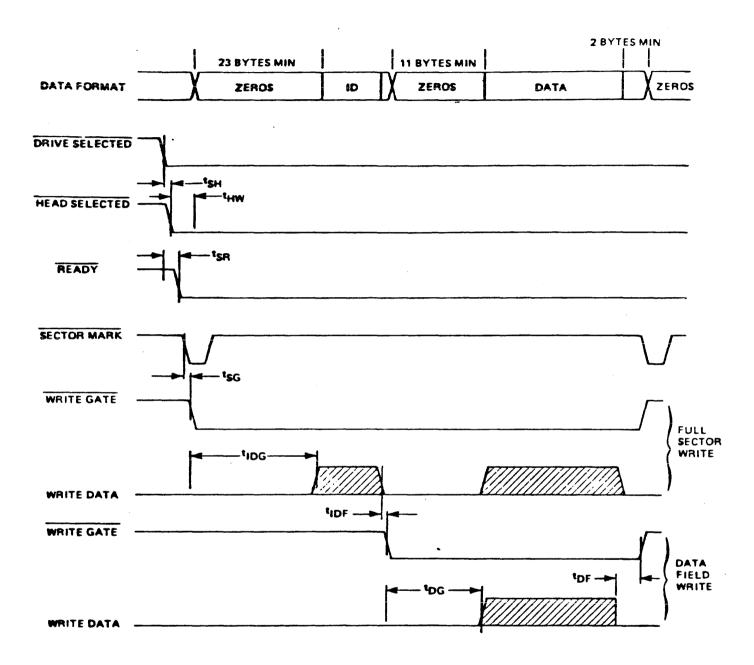


Figure 15 - Record Writing Timing

7. RECORD READING

Figure 16 shows timing requirements for reading ID and data fields and for reading data fields only. Their AC characteristics are listed in Tables 26 and 27.

TABLE 26 - Record Reading Control AC Characteristics for DISKOS 1070

Symbol	Parameter	Min	Max	Units
t _{SH}	DRIVE SELECTED to HEAD			
	SELECTED	20		us
t _{SR}	DRIVE SELECTED to READY	100		ns
t _{RDLW}	READ GATE DELAY for gaps			
	allowing WRITE to READ			
	transitions	10		us
t _{RD} LR	READ GATE DELAY for gaps			
	limited to READ to READ			
	or READ to WRITE	-		
	transitions	1		us
tsyn	READ PLO SYNCHRONIZATION			
	(Data not valid for this		_	
	period)		8	us
^t HR	HEAD SELECT to READ GATE	10		uS

TABLE 27 - Record Reading Control AC Characteristics for DISKOS 3450, 7050, 3350, 6650 & 15450

Symbol	Parameter	Min	Max	Units
t _{SH}	DRIVE SELECTED to HEAD			
	SELECTED	20		us
^t SR	DRIVE SELECTED to READY	100		ns
t _{RDLW}	READ GATE DELAY for gaps			
	allowing WRITE to READ			
	transitions	13		us
t _{RDLR}	READ GATE DELAY for gaps			
	limited to READ to READ			
	or READ to WRITE			
	transitions	1.9		us
tsyn	READ PLO SYNCHRONIZATION			
	(Data not valid for this			
	period)		9	us
t _{HR}	HEAD SELECT to READ GATE	25		us

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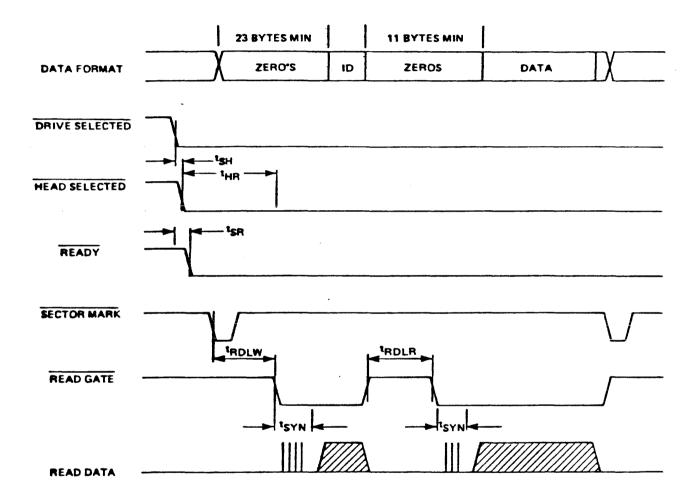


Figure 16 - Record Reading Timing

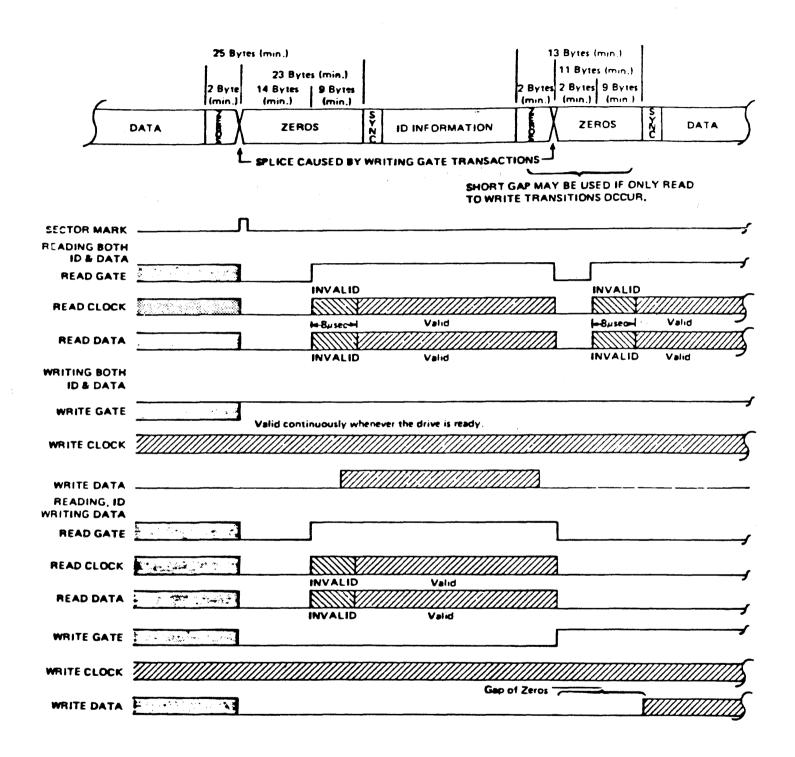


Figure 17 - READ & WRITE Transitions During Gaps