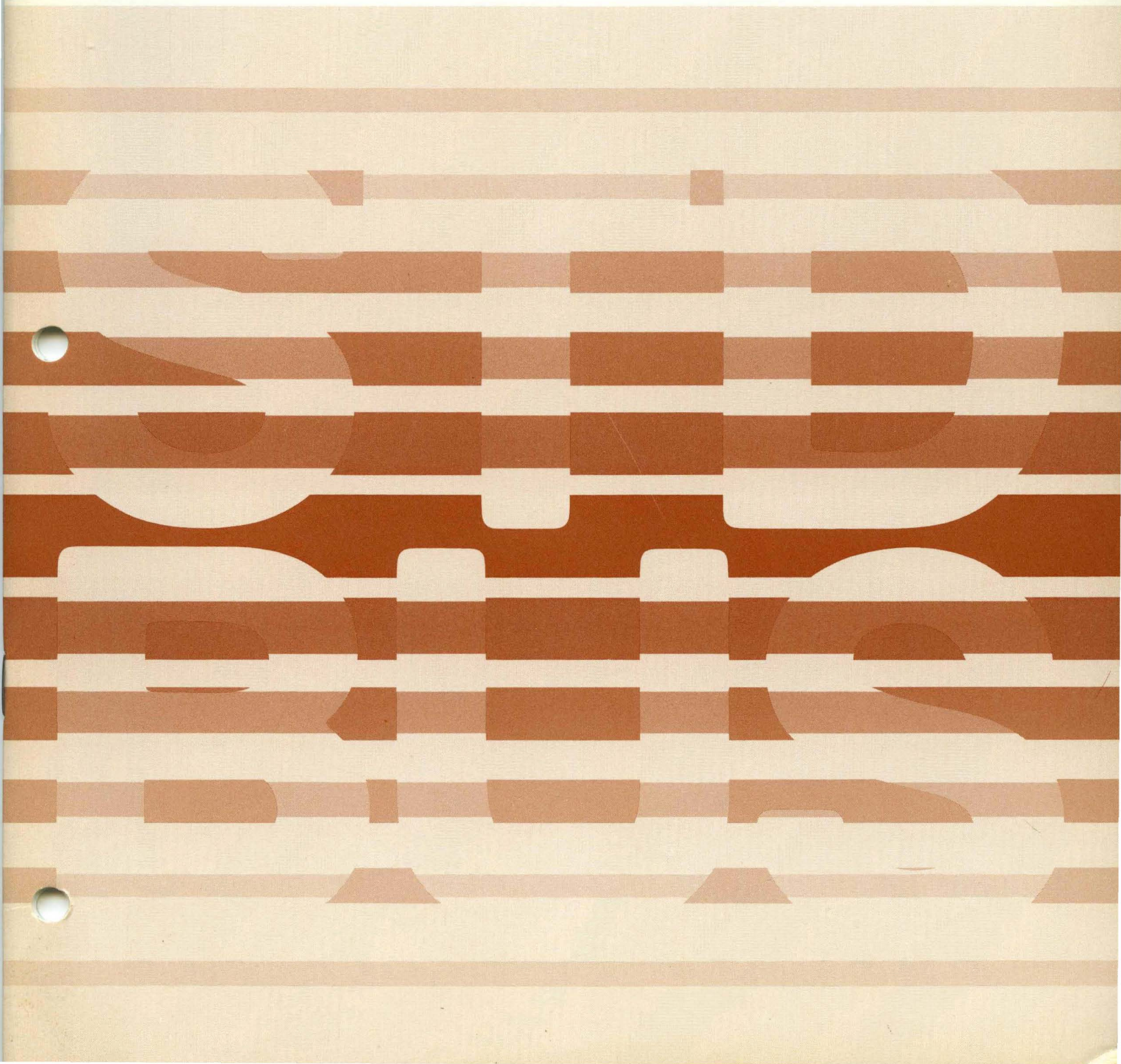
PRO-LOG
CORPORATION

STD 7000

7507
I/O Rack Interface Card

USER'S MANUAL



7507
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PRELIMINARY

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9/81

7507 I/O MODULE MOUNTING RACK INTERFACE CARD USER'S MANUAL

TABLE OF CONTENTS

1. PRODUCT DATA SHEET - 7507 I/O MODULE MOUNTING RACK INTERFACE CARD

A. PRODUCT OVERVIEW

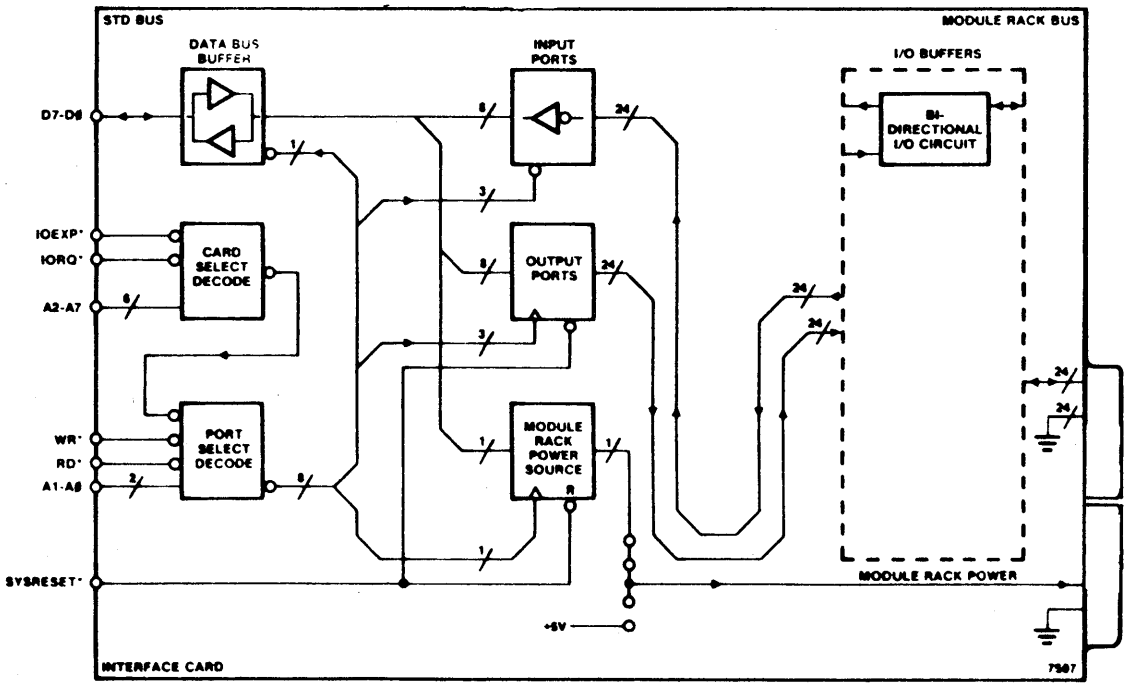
The 7507 provides an interface between the STD BUS and the Industry Standard I/O Module Mounting Rack (OPTO-22 Corp. or equivalent). This interface card can control up to 24 AC or DC input or output modules in any combination and position on the I/O Module Mounting Rack. The I/O Module Mounting Rack may be separated from the 7507 by up to ten feet (3.05m) of 50 conductor ribbon cable.

The 7507 is also useful as a general purpose TTL interface card. Three 8-bit read/write ports control 24 bidirectional signal lines. In addition, an output port-controlled power source rated at +4.75V at 500mA is provided. An LED assembly, visible from the card edge moditors the state of the power source and the three signal lines. Connection to the 7507 is supplied through a 50-pin card edge connector. Adjacent grounds are provided for each signal line for use in ribbon cable or discrete wire cable assemblies.

B. PRODUCT FEATURES

- Up to 24 I/O Modules per 7507
- Any Type of Module can be Controlled in any Combination and Position
- Standard I/O Module Bus allows use of Industry Standard Industrial I/O Module Mounting Racks.
- Low Pass Input Filters for Noisy Industrial Environments
- Single +5V Operation
- Socketed ICs

C. BLOCK DIAGRAM



2. FUNCTIONAL DESCRIPTION

The 7507 uses the Industry Standard I/O Module Bus to communicate with the I/O Module Mounting Rack. The bus consists of 24 bidirectional data lines alternated with 24 ground lines, a switched +4.75/500mA power lead and a ground power lead. These signals are routed over up to ten feet (3.05M) of 50 conductor flat cable.

Each bidirectional data line controls one I/O module on the I/O Module Mounting Rack. Since the I/O module may be an input or an output device, each signal line must perform as an input or an output. This signal line characteristic is achieved by the circuit shown in the Bidirectional I/O Circuit diagram. (Section 2)

The output circuit capability is supplied through an output port register, an open-collector inverting driver, and a pull-up resistor. There are no programming constraints in the output mode; active high data is written to the output port causing an output module on the I/O Module Rack to conduct.

Input circuit capability is provided through an inverting input port buffer and a low-pass RC filter. The low-pass filter, combined with the Schmitt-trigger characteristic of the input port buffer, removes noise-induced voltage spikes from the input signal. The active condition of any input module (high voltage present), appears as active-high data in the input port. There is one programming constraint in the input mode: active-high data cannot be written to the output port bit that is to be used as an input port bit. This constraint is required to disable the open-collector output drive for that bit. Note: On system power up the SYSRESET* signal clears the output port and puts the output drivers in the disabled state. Thus programming overhead is not required to select the input mode of operation.

The power needed to operate the I/O Module Mounting Rack is supplied by an output port-controlled power source capable of providing 500mA. To disable all input and output modules in the I/O Module Mounting Rack, this power source should be switched off by setting the I/O Module Rack power disable bit. This is useful when performing a test on the 7507. If the I/O Module Rack is disabled, the 7507 may be tested by writing a value to an output port and then reading the value back for verification. A time delay is required before reading the value back to allow for the operation of the input filter. Check the Switching Characteristics table for the correct time delay value.

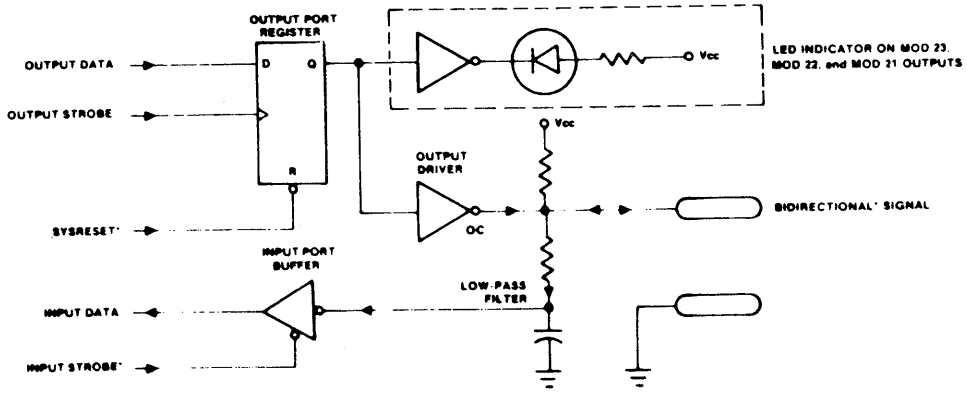
To output power directly from the Vcc of the STD system to the I/O Module Mounting Rack, it is possible to bypass the output port-controlled +4.7V power source by moving the wire jumper from location SA to location SB (see Component Placement diagram). Remove this jumper to disable the I/O Module Mounting Rack supply completely. The state of the I/O Module Mounting Rack current supply is indicated by the bottom LED (on→Vcc = +4.7V, off→Vcc = +0V) See the Component Placement diagram for LED placement information. (Section 7)

GENERAL PURPOSE INTERFACE

The 7507 is useful as a general purpose TTL interface card. The ground-signal-ground of the I/O connectors allows minimum crosstalk between signal lines for flat cable or twisted pair discrete wire cable assemblies for interconnection between systems in electrically noisy environments.

Three LED's are provided for use as general purpose status indicators. These indicators may be accessed by writing the output port bits for module 23 (mod 23*), module 22 (mod 22*), and module 21 (mod 21*) (on = active-high output register data). See the Component Placement diagram for LED placement information. (Section 7)

The bidirectional signal lines at the card edge connector are active-low on both input and output. The signals are terminated with a 1K pull-up resistor.

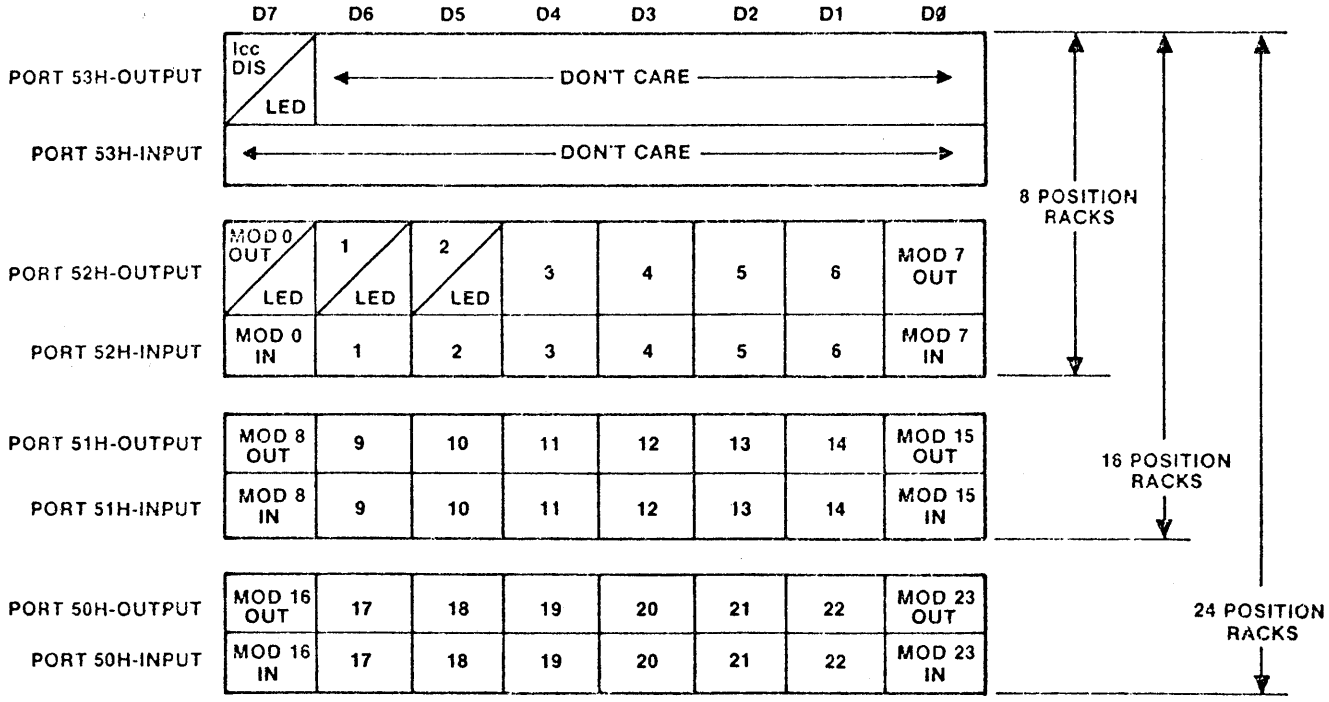


Typical Bidirectional I/O Circuit

3. MAPPING

The 24 bidirectional signals are accessed as three 8-bit input/output ports. Note: The 24 position I/O Module Mounting Rack uses all three ports. The 16 position I/O Module Mounting Rack uses two ports. The 8 position rack requires a single input/output port. See the Port Mapping diagram for port assignments for all three configurations. The I/O Module Mounting Rack power supply uses the same 1-bit output-only port for all three I/O Module Rack configurations. With the exception of these differences, the three I/O configurations program identically.

The I/O ports of the 7507 are selected by a decoded combination of address lines A7 through A0. The 7507 is shipped with the port assignments shown in the Port Mappping diagram. The user may change the port address assignments by changing jumper wires SW, SX, and SY. Refer to the Component Placement diagram for the position of SW, SX, and SY. (Section 7)



Port Mapping

4. ADDRESS DECODER OPERATION

Refer to the schematic, Document #105391

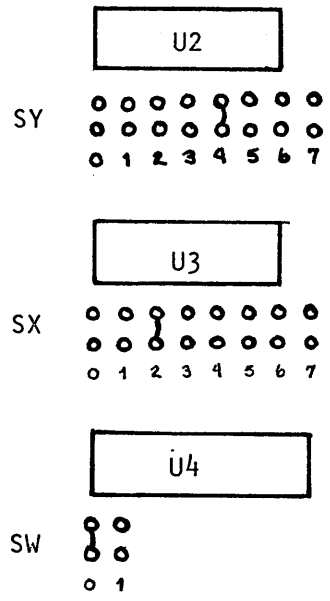
The 7507 uses four cascaded 74LS42 decoders (U2, U3, U5 and U6) to decode address lines A0-A7. These decoders are enabled only when IORQ* is active. The WR* signal is used to gate the select strobes from U5 that control the output ports. The RD* signal is used to gate the select strobes from U6 that control the input ports.

CHANGING THE 7507's PORT ADDRESS

Refer to the assembly diagram, Document #104392

Locate decoders U2 and U3 (74LS42) adjacent to the STD BUS edge connector. Each decoder device has a dual row of pads which form decoder output select matrices. Make one (and only one) connection to each of the matrices adjacent to U2 and U3.

The decoder jumper pad numbering figure shows the numbering of the pads adjacent to the decoder chips on the 7507. Also shown are the jumpers (at X2 and Y4) which produce hexadecimal port addresses 50, 51, 52 and 53, the selections made when the card is shipped.



DECODER JUMPER PAD NUMBERING

The 7507 may respond to the alternate I/O address condition which is determined by the state of IOEXP* signal. The 7507 can respond to an I/O address when the IOEXP* is low when jumper SW is in the number "0" position (the position as shipped). The card will respond to an I/O address when the IOEXP* is high when jumper SW is in the number "1" position. The IOEXP* is normally held low by the CPU card.

The I/O address mapping and jumper selection table for 4 addresses per card shows where to place jumper straps to obtain any four sequential port addresses in the hexadecimal range 00-FF. Using the lowest of the 2-digit hexadecimal addresses desired, find the most significant hexadecimal address digit along this vertical axis, and the least significant hex digit on the horizontal axis. For example, port addresses 50, 51, 52, and 53 are obtained by connecting jumpers at X2 and Y4.

The only restriction that applies in address selection for the 7507 is the lower of the four port addresses (50 as shipped) must occur only at every fourth possible address. For example, the sequence 51, 52, 53 and 54 is not allowed by the decoder.

The pad matrices adjacent to U2, U3, and U4 are on 0.10 inch (0.25cm) centers. The jumper wires may be conveniently replaced by wirewrap post if frequent address selection changes are anticipated.

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION X & Y
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	X0 Y0				X0 Y1				X0 Y2				X0 Y3				X AND Y
1	X0 Y4				X0 Y5				X0 Y6				X0 Y7				
2	X1 Y0				X1 Y1				X1 Y2				X1 Y3				
3	X1 Y4				X1 Y5				X1 Y6				X1 Y7				
4	X2 Y0				X2 Y1				X2 Y2				X2 Y3				
5	X2 Y4				X2 Y5				X2 Y6				X2 Y7				
6	X3 Y0				X3 Y1				X3 Y2				X3 Y3				
7	X3 Y4				X3 Y5				X3 Y6				X3 Y7				
8	X4 Y0				X4 Y1				X4 Y2				X4 Y3				
9	X4 Y4				X4 Y5				X4 Y6				X4 Y7				
A	X5 Y0				X5 Y1				X5 Y2				X5 Y3				
B	X5 Y4				X5 Y5				X5 Y6				X5 Y7				
C	X6 Y0				X6 Y1				X6 Y2				X6 Y3				
D	X6 Y4				X6 Y5				X6 Y6				X6 Y7				
E	X7 Y0				X7 Y1				X7 Y2				X7 Y3				
F	X7 Y4				X7 Y5				X7 Y6				X7 Y7				

I/O Address Mapping And Jumper Selection Table For 4 Addresses Per Card

5. 7507 CARD ENVIRONMENTAL SPECIFICATIONS

RECOMMENDED OPERATING LIMITS				ABSOLUTE NON-OPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	0	25	55	-40	75	°C
Humidity ①	0		95	0	95	%RH
Shock	← Not Specified →					
Vibration	← Not Specified →					
EMI	← Not Specified →					
ESD	← Not Specified →					

① Non-condensing relative humidity

6. ELECTRICAL SPECIFICATIONS

7507 I/O Module Mounting Rack Interface Card Electrical Specifications

MNEM.	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	Volt
T_A	Free air temp.	0	25	55	-40	75	°C

User Interface Electrical Characteristics Over Recommended Operating Limits

MNEM.	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{OL}	Low level interface voltage (at 10mA current level)			.80	Volt
I_{OL}	Low level interface current (at 0.70V level)			20	mA
V_{OH}	High level interface voltage	4.75		5.25	Volt
I_{OH}	High level interface current (at 2.0V)	-3.0			mA
V_{EXT}	Supply voltage output to module rack	4.45	4.70	4.95	Volt
I_{EXT}	Supply current output to module rack			500	mA

STD BUS Electrical Characteristics Over Recommended Operating Limits

MNEM.	PARAMETER	MIN.	TYP.	MAX.	UNIT
Icc	Interface supply current*		750	1000	mA
	STD BUS input load		(See STD BUS Pin List)		
	STD BUS output drive		(See STD BUS Pin List)		

*Includes 500mA load to external I/O Module Mounting Rack

Switching Characteristics Over Recommended Operating Limits

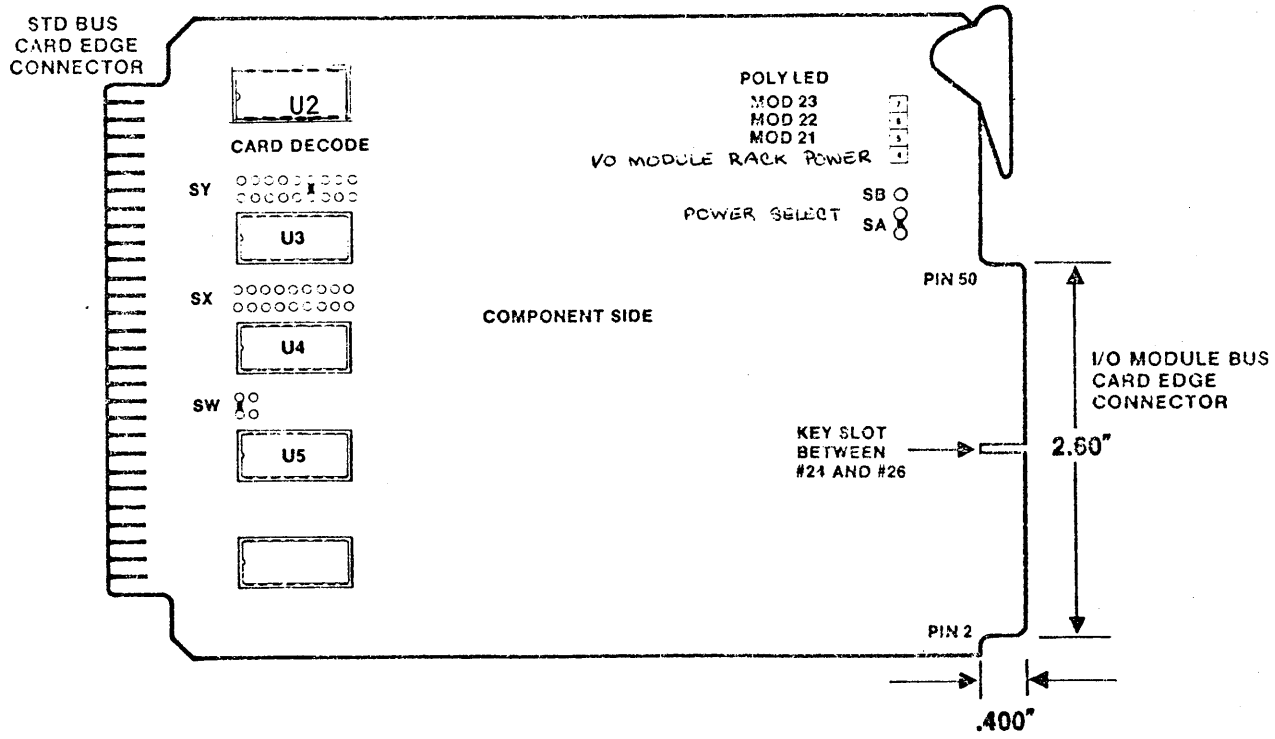
MNEM.	PARAMETER	FROM	TO	MIN.	TYP.	MAX.	UNIT
T_{PHL}	PROPAGATION TIME	STD DATA BUS	USER IFC			25	NSEC.
T_{PLH}	"	"	"			75	NSEC.
T_{PHL}	PROPAGATION TIME	USER IFC	STD DATA BUS	3	6	15	µSEC.
T_{PLH}	"	"	"	3	6	15	µSEC.

7. MECHANICAL

Refer to the Component Placement diagram for component placement information. The 7507 meets all STD BUS general mechanical specifications. The 7507 requires one card slot in a standard STD BUS card rack. The input connector clearance requirements vary according to the specific connector used. A 50-pin flat cable connector requires clearances of 0.250" on the component and circuit side of the board.

Recommended flat cable card edge connectors include 3-M part number 3415-0001 or equivalent. This may be used with a polarizing key 3-M part 3439-0000 or equivalent to avoid incorrect cable hook-up. A complete cable assembly may be obtained from Pro-Log as RC50-6.

For discrete wire cable assemblies, a PC board edge connector with solder tail connections may be used in conjunction with a cable hood assembly to provide reliable, strain-relieved termination. The recommended 50-pin card edge connector is a Viking part number 3VH25/1JN5. This connector is used with a Viking Hood part number 036-0097-002 or equivalent. These components may be obtained from Pro-Log as CS50.



Component Placement

STD 7507 EDGE CONNECTOR PIN LIST								
PIN NUMBER					PIN NUMBER			
OUTPUT (LSTTL DRIVE)							OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)								INPUT (LSTTL LOADS)
MNEMONIC								MNEMONIC
+5 VOLTS	VCC		2		1		VCC	+5 VOLTS
GROUND	GND		4		3		GND	GROUND
-5V			6		5			-5V
D7	1	55	8		7	55	1	D3
D6	1	55	10		9	55	1	D2
D5	1	56	12		11	55	1	D1
D4	1	55	14		13	56	1	D0
A15			16		15		1	A7
A14			18		17		1	A6
A13			20		19		1	A5
A12			22		21		1	A4
A11			24		23		1	A3
A10			26		25		2	A2
A9			28		27		2	A1
A8			30		29		2	A0
RD*	1		32		31		1	WR*
MEMRQ*			34		33		1	IORQ*
MEMEX*			36		35		1	IOEXP*
MCSYNC*			38		37			REFRESH*
STATUS 0*			40		39			STATUS 1*
BUSRQ*			42		41			BUSAK*
INTRQ*			44		43			INTAK*
NMIRQ*			46		45			WAITRQ*
PBRESET*			48		47		1	SYSRESET*
CNTRL*			50		49			CLOCK*
PC1	IN		52		51	OUT		PC0
AUX GND			54		53			AUX GND
AUX -V			56		55			AUX -V

*Designates Active Low Level Logic

Edge Connector Pin List

7507 USER INTERFACE EDGE CONNECTOR PIN LIST								
PIN NUMBER					PIN NUMBER			
OUTPUT (LSTTL DRIVE)							OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)								INPUT (LSTTL LOADS)
MNEMONIC								MNEMONIC
GROUND			2		1	50	13	MOD 0
"			4		3	50	13	" 1
"			6		5	50	13	" 2
"			8		7	50	13	" 3
"			10		9	50	13	" 4
"			12		11	50	13	" 5
"			14		13	50	13	" 6
"			16		15	50	13	" 7
"			18		17	50	13	" 8
"			20		19	50	13	" 9
"			22		21	50	13	" 10
"			24		23	50	13	" 11
"			26		25	50	13	" 12
"			28		27	50	13	" 13
"			30		29	50	13	" 14
"			32		31	50	13	" 15
"			34		33	50	13	" 16
"			36		35	50	13	" 17
"			38		37	50	13	" 18
"			40		39	50	13	" 19
"			42		41	50	13	" 20
"			44		43	50	13	" 21
"			46		45	50	13	" 22
"			48		47	50	13	" 23
"			50		49	500mA		MODULE RACK POWER

User Interface Pin List

8. 7507 OPERATING SUBROUTINE MODULES

This section provides flow diagrams and subroutines to operate your 7507 card. These may be used intact, or used as models to construct subroutines for a specific application.

The subroutines are written in 8080-family assembly code and will execute on 8080, 8085, and Z80 processors. The memory addresses selected are compatible with Pro-Log's 7801 (8085A) and 7803 (Z80) processor cards. The 7507 port addresses used are the address jumper selections made when the 7507 is shipped.

To use these subroutines in systems other than those described above, the memory and/or I/O port addresses may require change for compatibility.

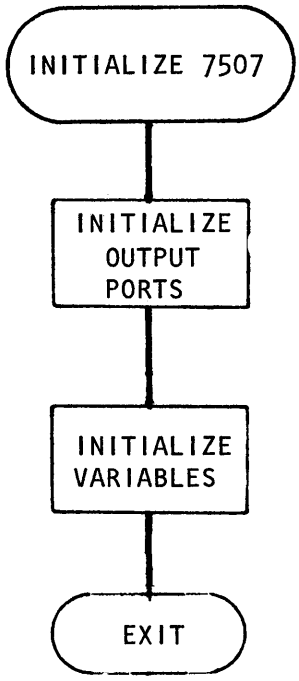
The flow diagrams presented can be easily translated into the assembly code used by any microprocessor since they show the steps required to achieve 7507 operation without reference to a particular microprocessor.

The following subroutines are provided for use with the 7507.

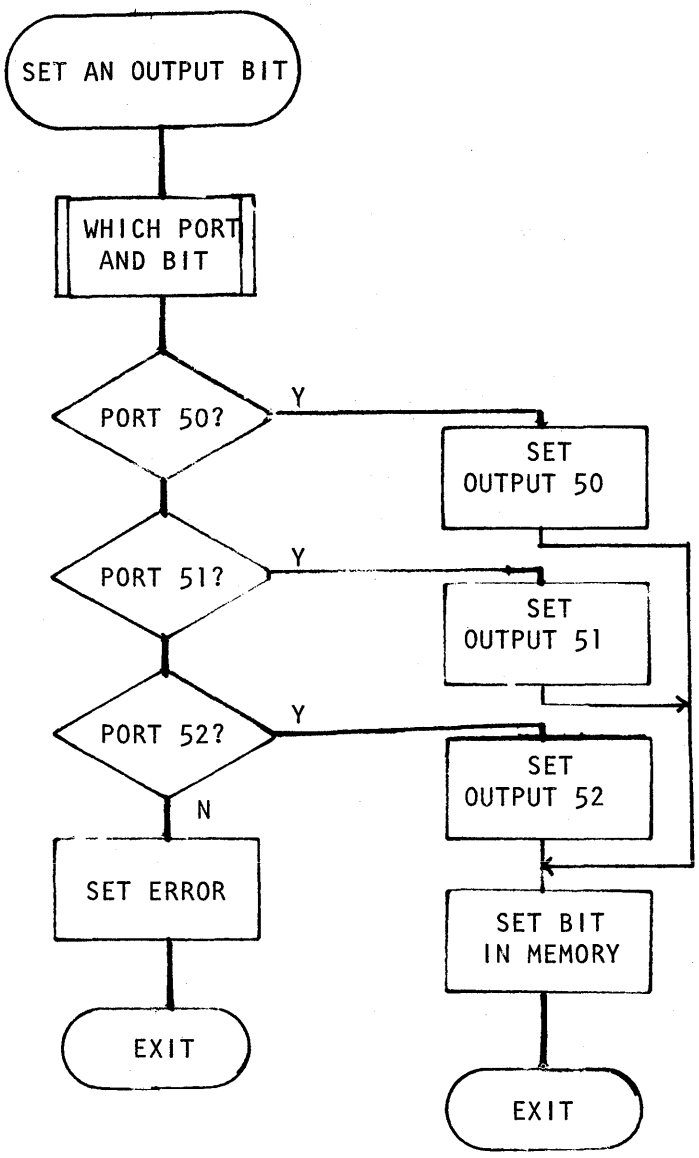
NAME AND DESCRIPTION	REGISTERS CHANGED	FLOW DIAGRAM	PROGRAM
(7507) This subroutine sets all outputs to a predefined state. It also initializes all variables used by the other subroutines.	A H L	Page 14	Page 18
(SET A BIT) This routine accepts a hex value in the accumulator which corresponds to the I/O module to be turned on. If the I/O module number is out of range, the carry flag will be set.	A B H L	Page 15	Page 19
(CLEAR A BIT) This routine accepts a hex value in the accumulator which corresponds to the I/O module to be turned off. If the I/O module number is out of range, the carry flag will be set.	A B H L	Page 16	Page 20

continued

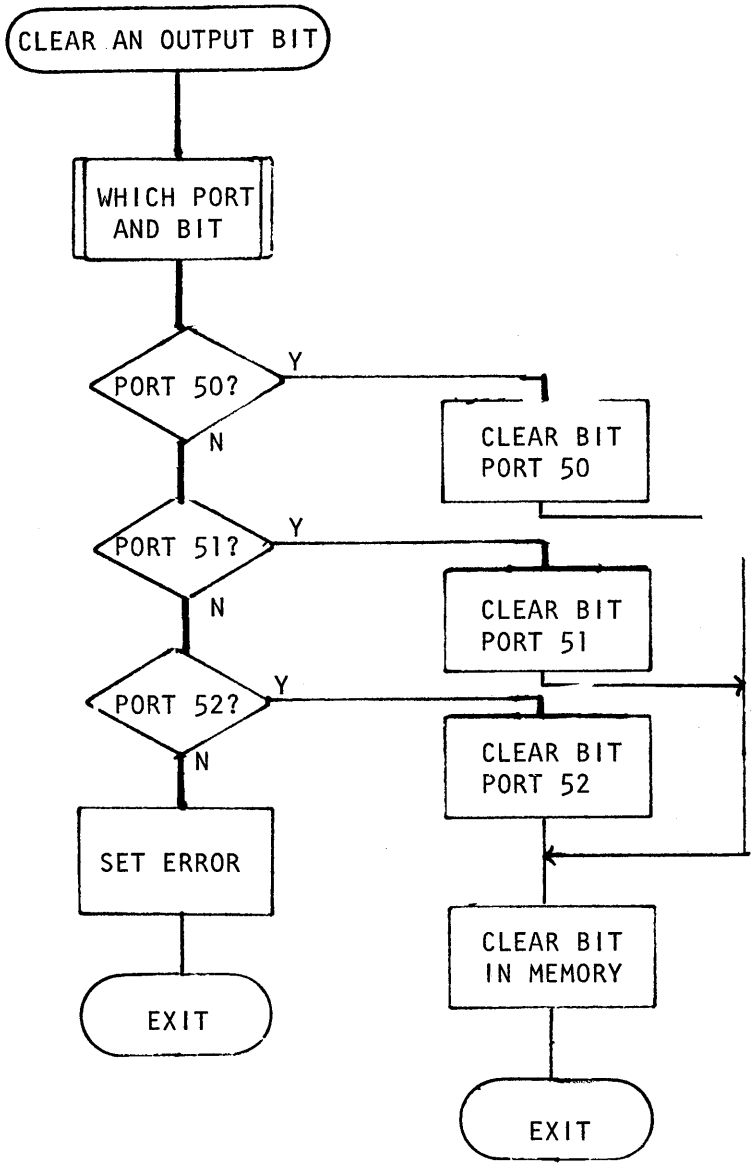
NAME AND DESCRIPTION	REGISTERS CHANGED	FLOW DIAGRAM	PROGRAM
(BIT CHANGED?) This routine accepts a hex value in the accumulator which corresponds to the I/O module to be tested. If the I/O module number is out of range, the carry flag will be set. It returns with P=0 if there were no changes and P=1 if the addressed module did change since the last test. The Z flag = 0 if the bit is set and Z=1 if the input port is clear	A B H L C D F	Page 17	Page 21



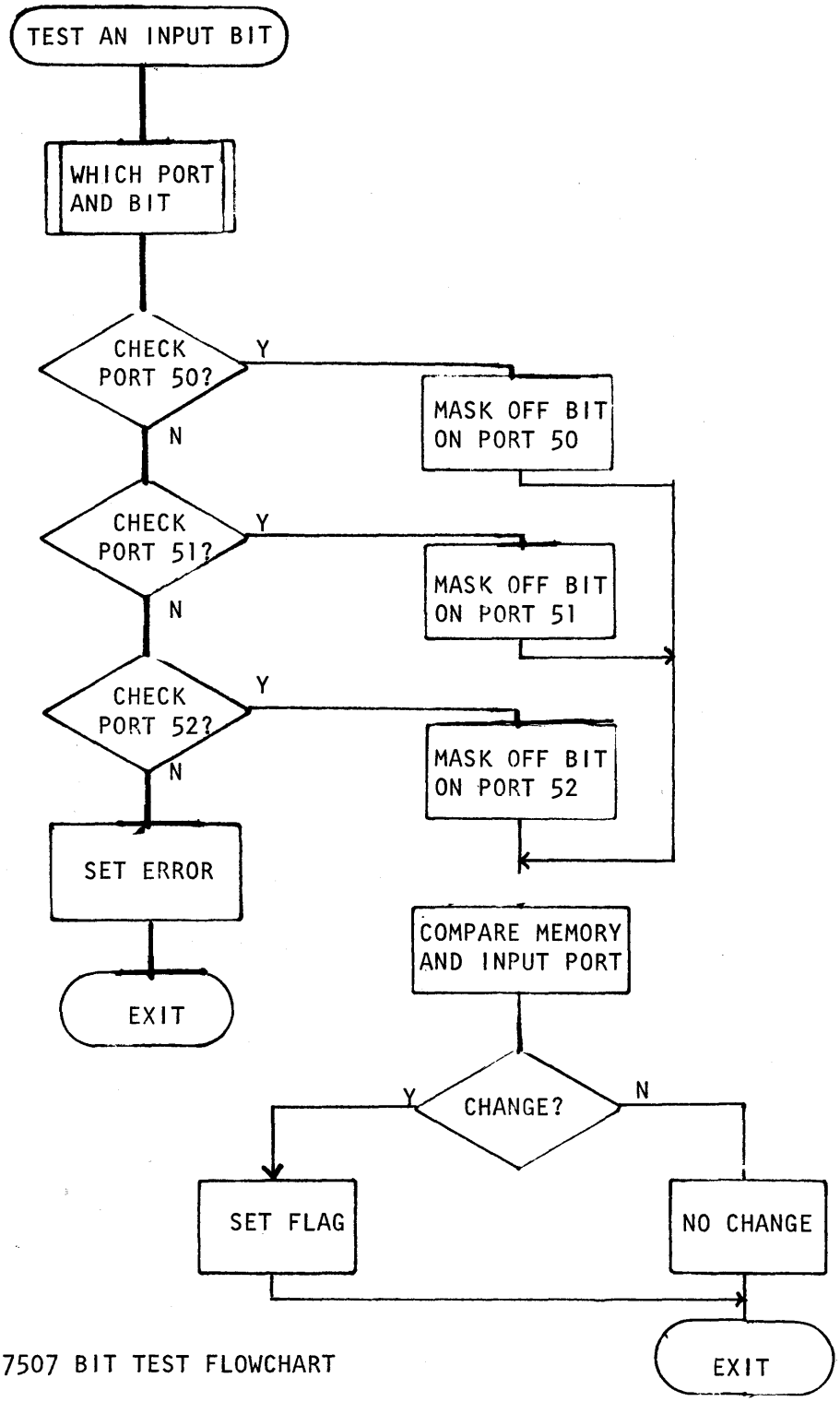
7507 INITIALIZATION FLOWCHART



7507 BIT SET FLOWCHART



7507 BIT CLEAR FLOWCHART



7507 BIT TEST FLOWCHART

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PROGRAM ASSEMBLY FORM

TITLE

DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
	00	21	(7507)	LDPI	HL	INITIALIZE PROGRAM
	1			-	XX	
	2			-	RAM PAGE	
	3	3E		LDAI		SET PORT 50
	4				XX	
	5	D3		OPA		
	6	50		-	50	
	7	3E		LDAI		SET PORT 51
	8			-	XX	
	9	D3		OPA		
	A	51		-	51	
	B	3E		LDAI		SET PORT 52
	C			-	XX	
	D	D3		OPA		
	E	52		-	52	
	OF	DB		IPA		SET MEMORY TO I/O PORT STATUS
	10	50		-	50	
	1	77		STAN	(HL)	
	2	23		ICP	(HL)	
	3	DB		IPA		
	4	51		-	51	
	5	77		STAN	(HL)	
	6	23		ICP	(HL)	
	7	DB		IPA		
	8	52		-	52	
	9	77		STAN	(HL)	
	A	C9		RTS		
	B					
	C					
	D					
	E					
	1F					

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	20	4F	(WHICH LINE?)	LDC	A	SAVE A CONVERT NUMBER IN ACCUMULATOR TO BIT POSITION
	1	3E		LDAI		BIT → A
	2	C1		-	01	PUT 01 IN A AND B BIT → B
	3	47		LDB	A	
	4	CC		ICC		
	5	CD	LOOP	DCC		DECREMENT #
	6	C8		RTS	Z 1	← A = BIT B = PORT 01 FIRST BIT
	7	CC		NOP		02 SECOND PORT
	8	CD		NOP		03 THIRD PORT
	9	07		RLC		← ROTATE TO NEXT BIT POSITION
	A	D2		JP	CD	IF CARRY IS SET INCREMENT PORT REG
	B			-	LOOP	
	C			-		
	D	C4		ICB		
	E	C3		JP		
	2F			-	LOOP	
	30			-		
	1	3E	CHANGE?	LDAI		LOAD A WITH 00 FOR NO CHANGE
	2	00		-	00	LOAD A WITH 80 FOR CHANGE (SIGN BIT)
	3	CA		JP	Z 1	
	4			-	NO CHANGE	
	5			-		
	6	3E		LDAI		
	7	80		-	80	
	8	C1	NO CHANGE	PLP	BC	← PUT Z FLAG IN B
	9	B1		ORA	B	OR Z FLAG WITH SIGN FLAG
	A	4F		LDB	A	
	B	C5		PSP	BC	PUT NEW FLAG STATUS IN FLAG REG
	C	F1		PLP	AF	
	D	C9		RTS		← RETURN Z=0 BIT SET Z=1 BIT CLEAR
	E					P=0 NO CHANGE P=1 CHANGE
	3F					

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PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / DATE / COMMENTS
	40	3E		LDAI		
	1			-	XX	
	2	CD	(SET A BIT)	JS		CALCULATE PORT AND BIT — SET A BIT
	3			-	(WHICH LINE?)	
	4			-		
	5	21		LDPI	HL	SET POINTER
	6			-	XX	
	7			-	RAM PAGE	
	8	05		DCB		JUMP TO PROPER I/O ROUTINE FOR EACH PORT
	9	CA		JP	Z1	
	A			-	PORT 50	
	B			-		
	C	23		ICP	HL	
	D	05		DCB		
	E	CA		JP	Z1	
	4F			-	PORT 51	
	50			-		
	1	23		ICP	HL	
	2	05		DCB		
	3	CA		JP	Z1	
	4	6B		-	PORT 52	
	5	13		-		
	6	00		NOP		
	7	37		STC		
	8	C9		RTS		← RETURN WITH CARRY SET FOR INVALID #.
	9	47	PORT 50	LDB	A	← SAVE A (BIT)
	A	DB		IPA		SET BIT IN OUTPUT LATCH
	B	50		-	50	
	C	B0		ORA	B	
	D	D3		OPA		
	E	50		-	50	
	5F	C3		JP		

100061 2 77

	60			-	UPDATE M	
	1			-		
	2	47	PORT 51	LDB	A	← SAVE A (BIT)
	3	DB		IPA		SET BIT IN OUTPUT LATCH
	4	51		-	51	
	5	B0		ORA	B	
	6	D3		OPA		
	7	51		-	51	
	8	C3		JP		
	9			-	UPDATE M	
	A					
	B	47	PORT 52	LDB	A	← SAVE A (BIT)
	C	DB		IPA		SET BIT IN OUTPUT LATCH
	D	52		-	52	
	E	B0		ORA	B	
	6F	D3		OPA		
	70	52		-	52	
	1	7E	UPDATE M	LDA	M(HL)	SET BIT IN MEMORY
	2	B0		ORA	B	
	3	77		STAN	(HL)	
	4	C9		RTS		
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	7F					

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HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS
	80	3E		LDAI		
	1			-	XX	
	2	CD	(CLEAR A BIT)	JS		CALCULATE PORT AND BIT CLEAR A BIT
	3			-	(WHICH LINE?)	
	4			-		
	5	21		LDPI	HL	SET POINTER
	6			-	XX	
	7			-	RAM PAGE	
	8	05		DCB		GO TO PROPER I/O ROUTINE
	9	CA		JP	Z1	
	A			-	PORT 50*	
	B			-		
	C	23		ICP	HL	
	D	05		DCB		
	E	CA		JP	Z1	
	8F			-	PORT 51*	
	90	13		-		
	1	23		ICP	HL	
	2	05		DCP		
	3	CA		JP	Z1	
	4			-	PORT 52*	
	5			-		
	6	00		NOP		
	7	37		STC		←RETURN WITH CARRY = 1 IF INVALID #
	8	C9		RTS		
	9	2F	PORT 50*	CMA		PUT BIT MASK IN B
	A	47		LDB	A	
	B	DB		IPA		CLEAR BIT
	C	50		-	50	
	D	A0		ANA	B	
	E	03		OPA		
	9F	50		-	50	

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	A0	C3		JP		
	1			-	UPDATE MEM	
	2			-		
	3	2F	PORT 51*	CMA		PUT BIT MASK IN B
	4	47		LDB	A	
	5	DB		IPA		CLEAR BIT
	6	51		-	51	
	7	A0		ANA	B	
	8	D3		OPA		
	9	51		-	51	
	A	C3		JP		
	B			-	UPDATE MEM	
	C			-		
	D	2F	PORT 52*	CMA		PUT BIT MASK IN B
	E	47		LDB	A	
	AF	DB		IPA		CLEAR BIT
	B0	52		-	52	
	1	A0		ANA	B	
	2	DB		OPA		
	3	52		-	52	
	4	7E	UPDATE MEM	LDA	M(HL)	CLEAR BIT IN MEMORY
	5	A0		ANA	B	
	6	77		STAN	(HL)	
	7	C9		RTS		
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	BF					

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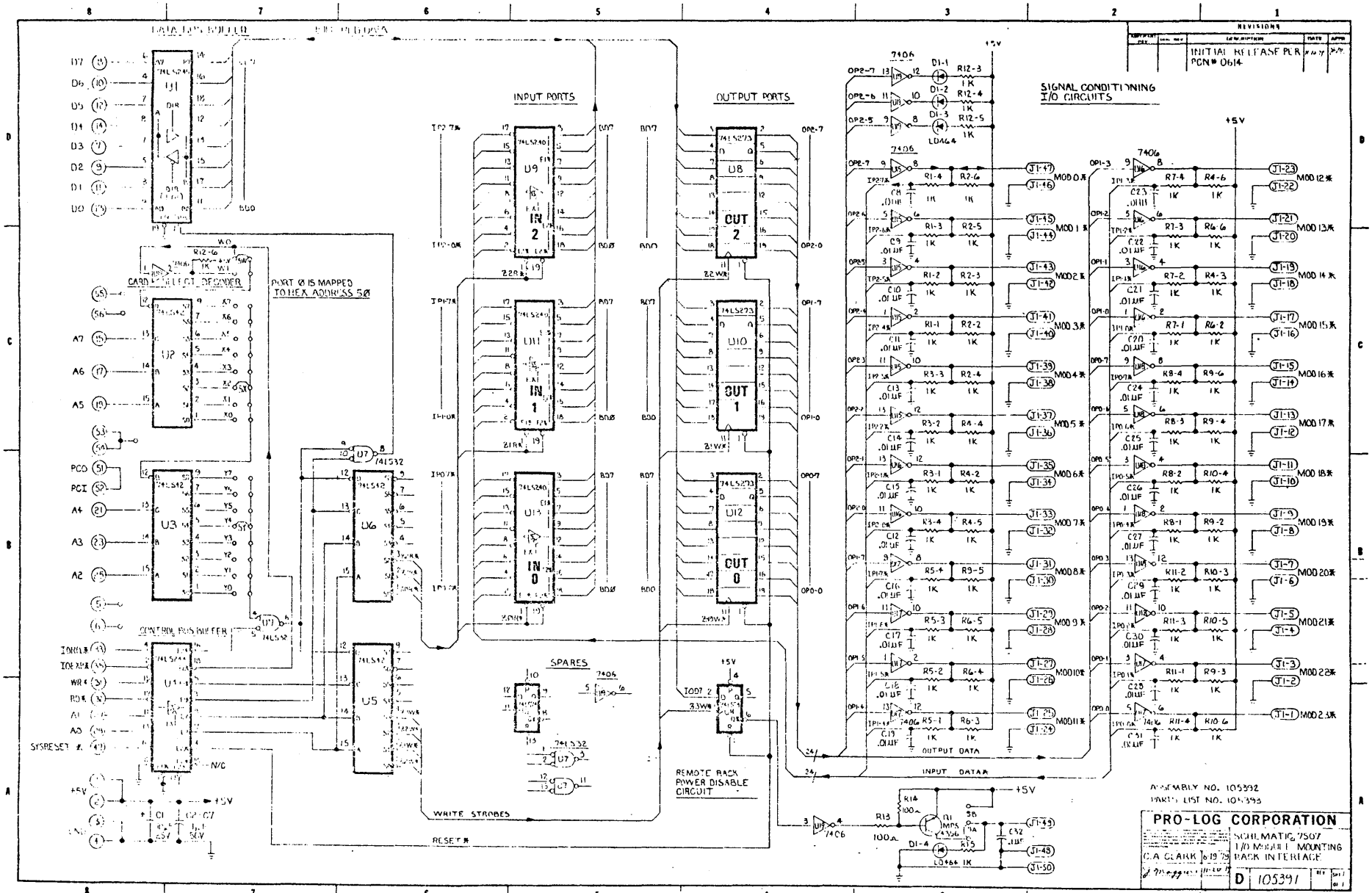
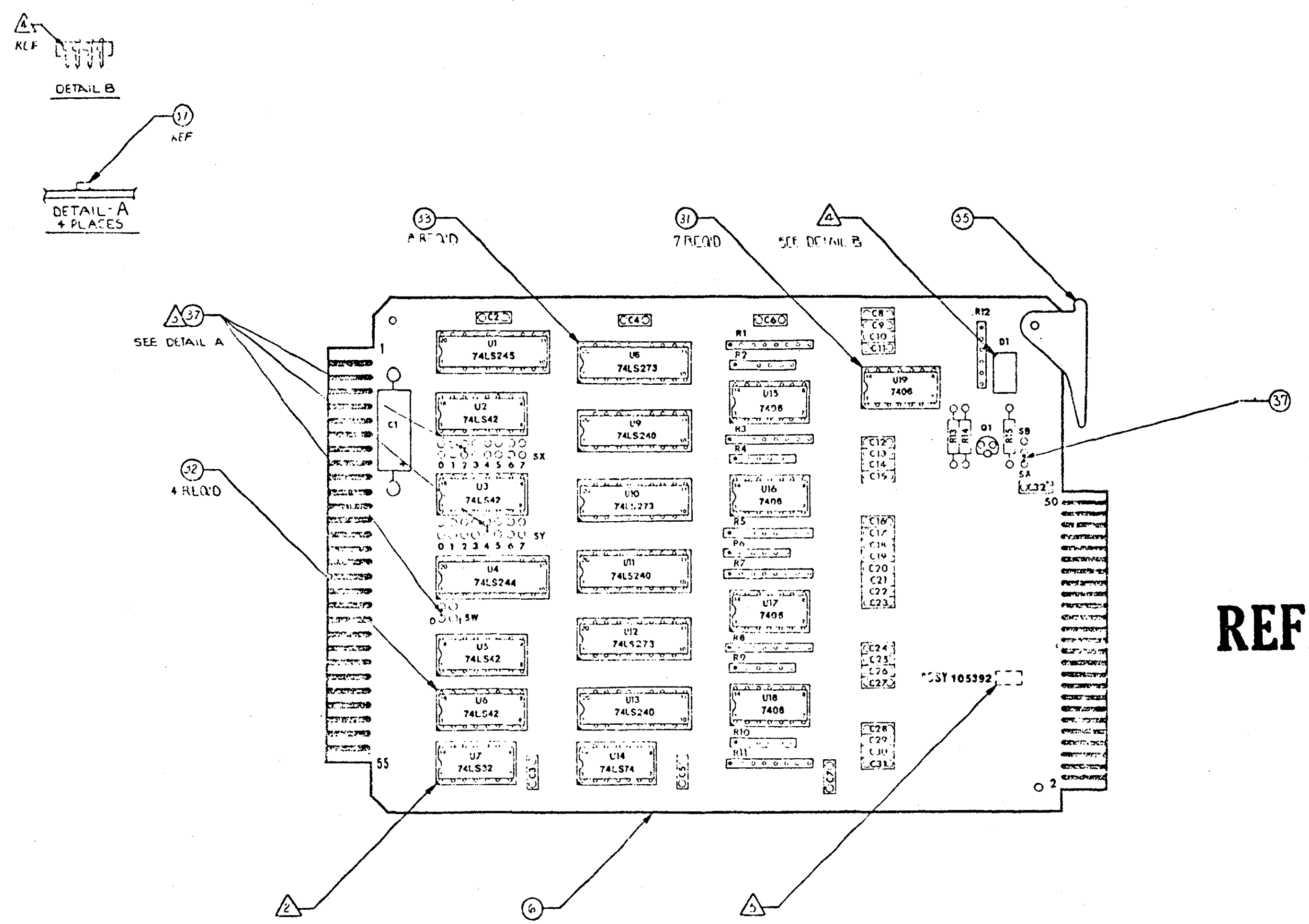
HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS / DATE
	C0	3E		LDAI		
	1			-	XX	
	2	CD	(BIT CHANGED?)	JS		CALCULATE PORT AND BIT — INPUT STATUS OF A BIT AND SEE IF IT HAS CHANGE
	3			-	(WHICH LINE?)	
	4			-		
	5	21		LDPI	HL	SET POINTER
	6			-	XX	
	7			-	RAM PAGE	
	8	C5		DCB		GO TO PROPER PORT ROUTINE
	9	CA		JP	Z1	
	A			-	PT50	
	B			-		
	C	23		ICP	HL	
	D	05		DCB		
	E	CA		JP	Z1	
	CF	E0		-	PT51	
	D0	13		-		
	1	23		ICP	HL	
	2	05		DCB		
	3	CA		JP	Z1	
	4			-	PT52	
	5			-		
	6	00		NOP		
	7	37		STC		
	8	C9		RTS		
	9	00	PT50	NOP		PUT BIT MASK IN B
	A	47		LDB	A	
	B	DB		IPA		INPUT DATA
	C	50		-	50	
	D	C3		JP		
	E			-	CMEM	
	DF			-		

	E0	00	PT51	NOP		PUT BIT MASK IN B
	1	47		LDB		
	2	DB		IPA		INPUT DATA
	3	51		-	51	
	4	C3		JP		
	5			-	CMEM	
	6			-		
	7	00	PT52	NOP		PUT BIT MASK IN B
	8	47		LDB	A	
	9	DB		IPA		INPUT DATA
	A	52		-	52	
	B	A0	CMEM	ANA	B	←MASK UNWANTED BITS (NEW)
	C	4F		LDC	A	←SAVE NEW DATA IN C
	D	F5		PSP	AF	←SAVE FLAG
	E	7E		LDA	M(HL)	←LOAD OLD DATA
	EF	A0		ANA	B	←MASK UNWANTED BITS
	F0	57		LDD	A	←SAVE OLD DATA IN D
	1	F1		PLP	AF	SET FLAG
	2	F5		PSP	AF	
	3	CC		JS	Z1	PUT NEW DATA IN MEMORY
	4			-	UPDATE MEM	CLEAR BIT IF CLEAR
	5			-		
	6	F1		PLP	AF	SET FLAGS
	7	F5		PSP	AF	
	8	C4		JS	Z0	SET BIT IF SET
	9			-	UPDATE MEM	
	A			-		
	B	7A		LDA	D	OLD ⊕ NEW = CHANGES Z1 = NO CHANGES Z0 = CHANGE
	C	A9		XRA	C	
	D	33		JP	UN	GO SET FLAGS PRIOR TO RETURN
	E			-	CHANGE ?	
	FF			-		


INPUT PORTS
OUTPUT PORTS
SIGNAL CONDITIONING
I/O CIRCUITS
PORT Ø IS MAPPED
TO HEX ADDRESS 5Ø
CARD SELECT DECODER
CONTROL BUS BUFFER
SPARES
REMOTE RACK
POWER DISABLE
CIRCUIT
WRITE STROBES
RESET*
OUTPUT DATA
INPUT DATA
INITIAL RELEASE PER
PGN# 0614
ASSEMBLY NO. 105392
PARTS LIST NO. 105393
PRO-LOG CORPORATION
SCHEMATIC, 7507
I/O MODULE MOUNTING
RACK INTERFACE
D 105391

REV	ECN NO.	DESCRIPTION	DATE	APPR
		INITIAL RELEASE PER PCN # 0114		
A		REVISED PER PCN 0114		



REFERENCE ONLY

5. IDENTIFY WITH ASSEMBLY REV LETTER.
4. INDICATES CATHODE PIN OF LED.
3. PORT 0 IS JUMPED TO ADDRESS 50.
2. INDICATES PIN 1 OF SOCKETS. (TYP)
1. FOR ASSEMBLY PROCEDURES SEE AS1004.

NOTES: UNLESS OTHERWISE SPECIFIED.

SCHEMATIC NO. 105391
PARTS LIST NO. 105393

ITEM	DESCRIPTION	REF DESIGNATION
20	MPS4356	Q1
19		
18	1K, CF, 1/4W, 5%	R15
17	100Ω, CF, 1/4W, 5%	R13, 14
16		
15	1K, 4 RES, 5%	R1, 3, 5, 7, 8, 11
14	1K NETWORK	R2, 4, 6, 9, 10, 12
13		
12	LD464	D1
11		
10	.01 µF, 50V	C8 - C31
9	.1 µF, 50V	C2 - C7, C32
8	10 µF, 25V	C1

PRO-LOG CORPORATION

ASSEMBLY 7507 I/O MODULE MOUNTING RACK INTERFACE

D 105392 REV A

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USER'S MANUAL

PRO-LOG
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