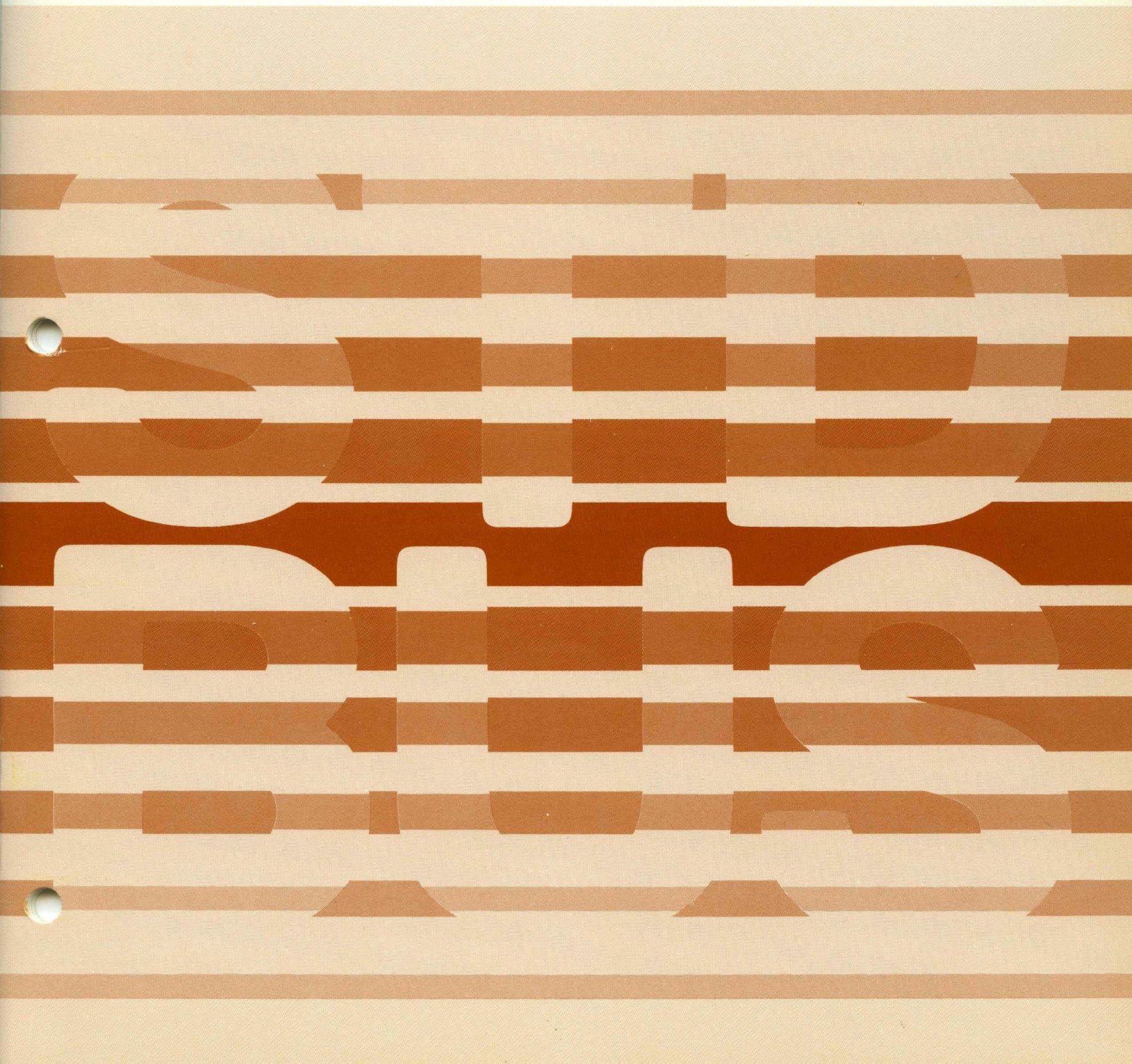
PRO-LOG
CORPORATION

STD 7000

7701
16K Static Ram
Memory Card

USER'S MANUAL



7701
16K Static Ram Memory Card
USER'S MANUAL

PRELIMINARY

PRO-LOG CORPORATION

10/81

7701 16K STATIC RAM MEMORY CARD USER'S MANUAL

TABLE OF CONTENTS

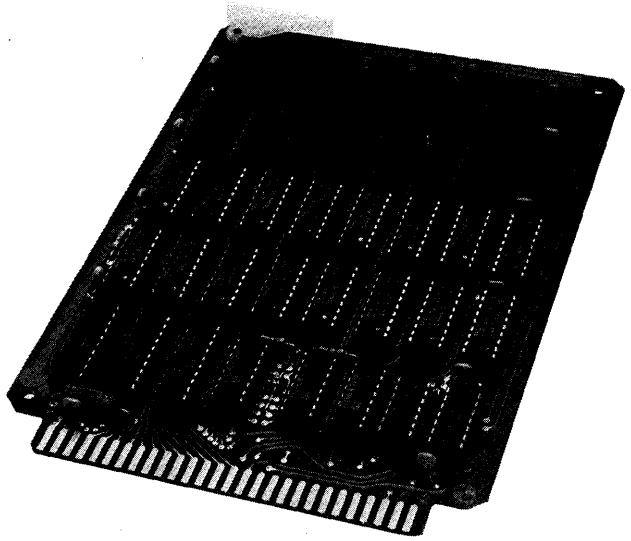
7000 STD BUS

7701 MEMORY CARD

16K BYTE STATIC RAM MEMORY CARD

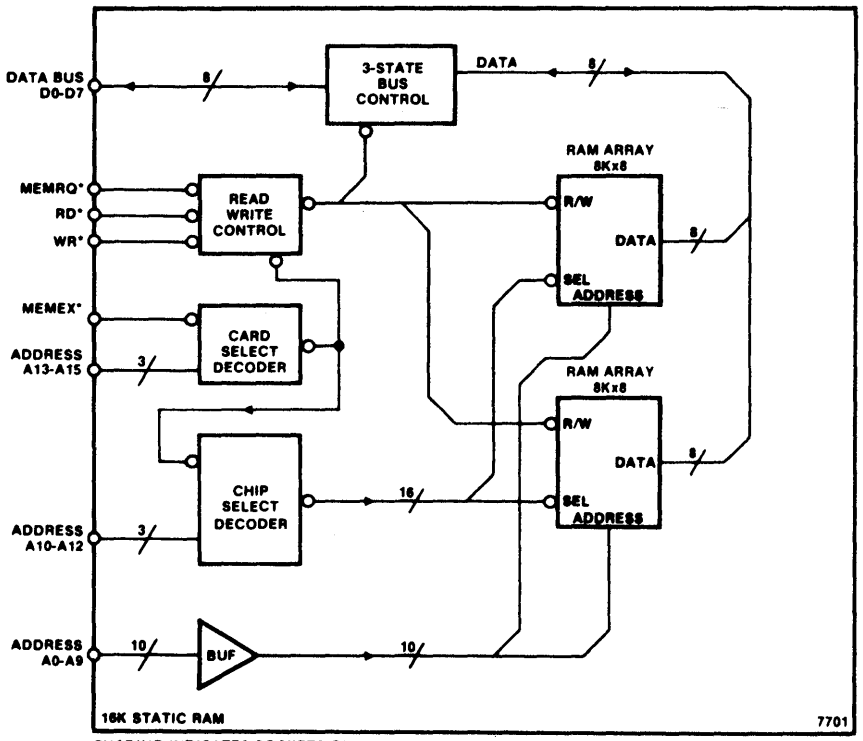
This card provides sockets for up to 16,384 bytes of Read-Write or PROM Memory. The card uses 2114 type RAMs or equivalent and has sockets for 16 pairs of RAMs. Alternately the card will accept 3625 type PROMs or equivalent. PROMs and RAMs can not be mixed on the same card.

The 7701 decodes 16 address lines, and can be mapped into either 8K or 16K bytes of consecutive address space. An on-card jumper system allows users to establish which 16K segment of a 64K microprocessor memory each 7701 occupies.



FEATURES

- **Sockets for 16K bytes of 2114L RAMs or 3625 PROMs**
- **User selectable card address**
- **All STD BUS lines buffered**
- **Minimal logic bus loading**
- **All IC's socketed**
- **Single +5V operation**
- **Use Pro-Log D1004, 1Kx8 memories (two 2114L's)**



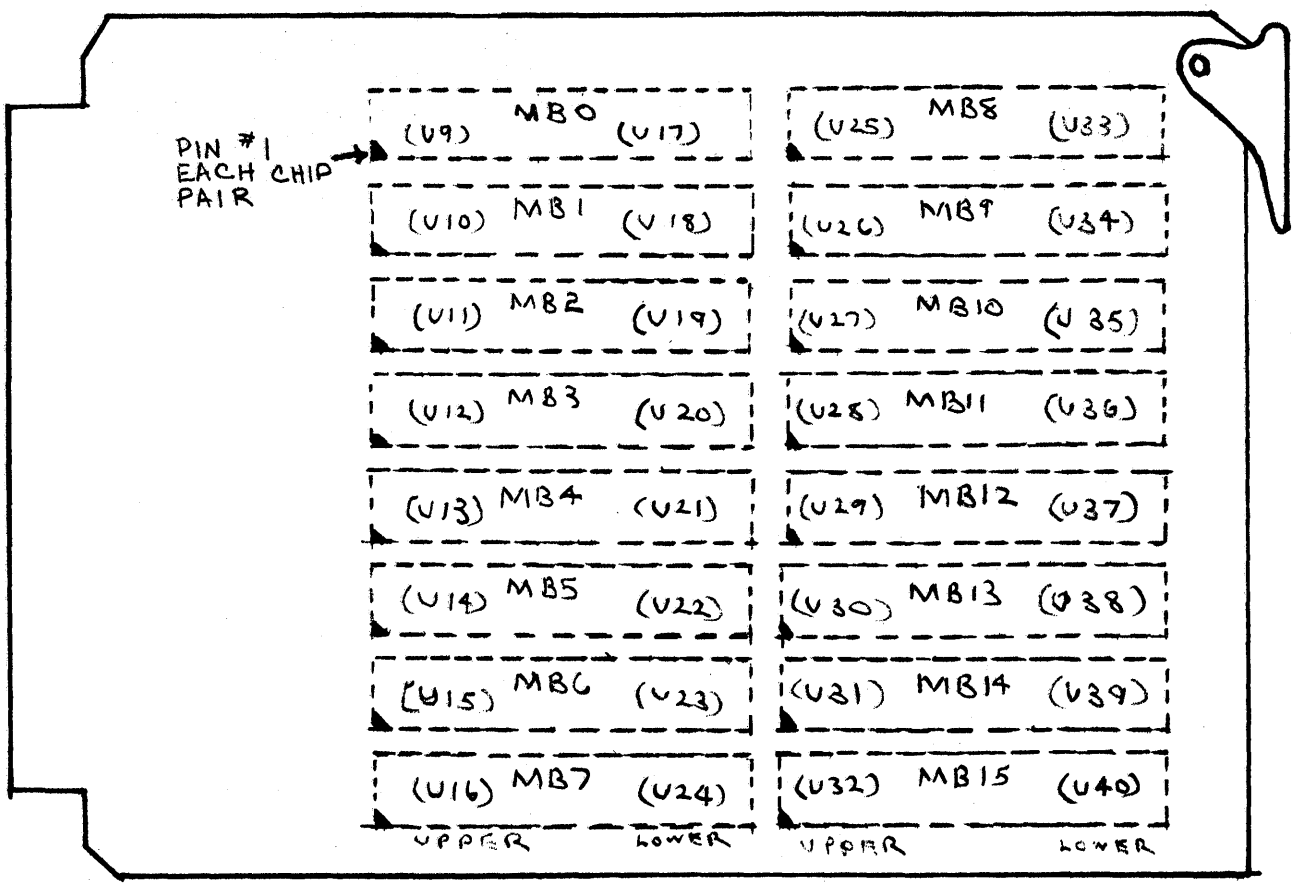
SHADING INDICATES SOCKETS ONLY

*INDICATES ACTIVE LOW LOGIC

2. FUNCTIONAL DESCRIPTION

The 7701 is organized to accept 16 pair (32 sockets) 2114L 1024 x 4-bit statis RAMs. Although the card may be populated with less than the full complement of 2114L chips, the data bus drivers are enabled anytime a valid address is present even if memory chips are not plugged in. The card address range is chosen to prevent bus contention with other system memory elements including processor on-card memory, other memory cards, and memory mapped I/O. Each pair of the 2114L's add 1K 8-bit bytes of RAM, which are designated memory blocks 0 -15 (MB0 - MB15).

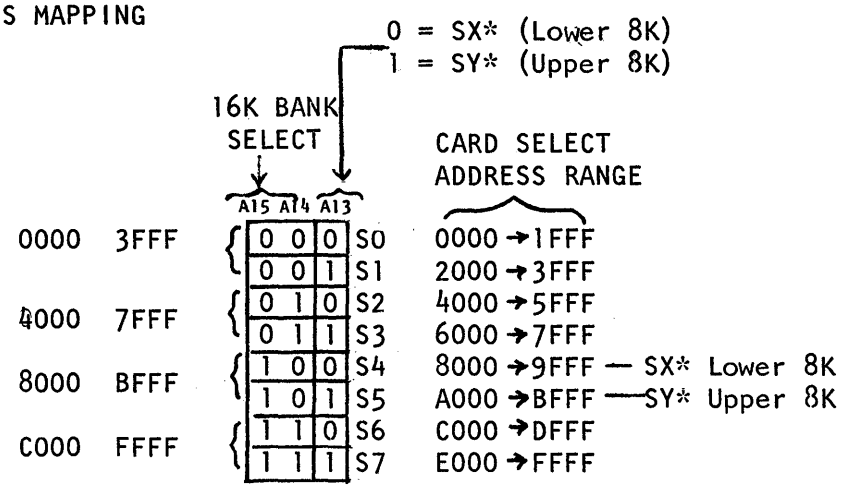
Each memory block consists of 2 each (1024 x 4) 2114L RAMs. (Reference Assembly Diagram 102687)



PROM OPTION

The card is designed to accept type 3625 PROMs in place of 2114 RAMs with an increase in card power consumption. PROMs and RAMs may not be mixed on the same card. If this option is exercised be sure to cut traces and ground pin 10 of all chips.

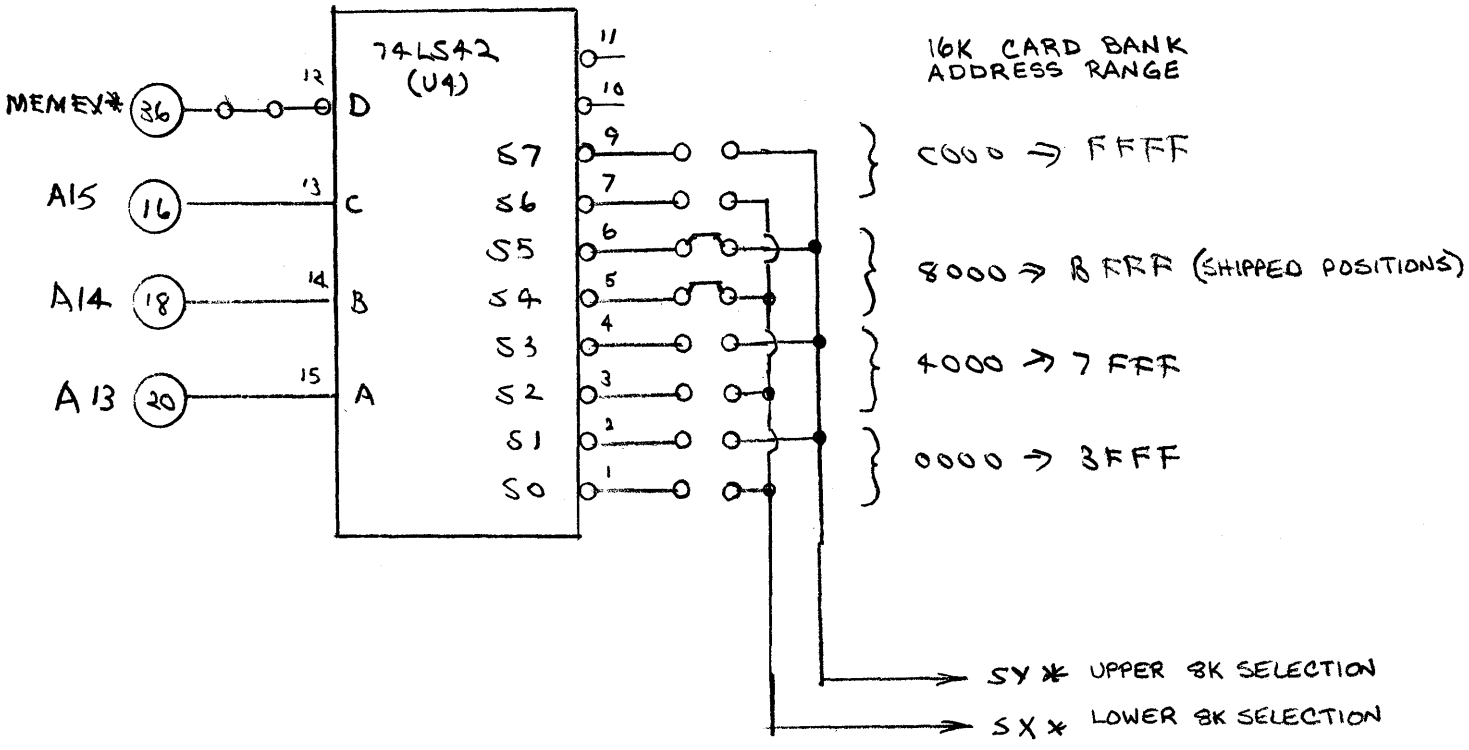
3. CARD ADDRESS MAPPING



CARD SELECT DECODING 74LS42 (U4)

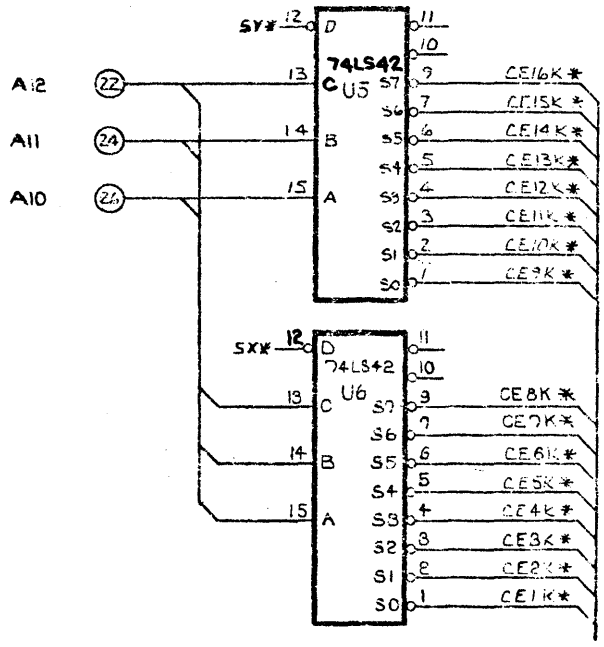
The upper three (A15, A14, A13) address lines are decoded by an 74LS42 (U4) for card address selection. A15 and A14 are decoded to select one of the four 16 banks. Address line A13 is decoded for selection of the lower 8K (SX*) and the upper 8K (SY*) of the 16K bank.

CARD SELECT DECODER



The next lower three address lines (A12, A11, A10) are decoded by two each 74LS42, U5 and U6. U5 is strobed by SX* line and selects the lower 8 address banks. U6 is strobed by SY* line and selects the upper 8 address banks, U5 and U6 are designated Chip Select Decoders on the schematic diagram.

CHIP SELECT DECODERS



Each chip enable line goes to pin 8 (CE*) of a pair of 2114L chips, (1K block) The lower ten address lines are used for direct addressing of the 1K chip pairs, and are buffered by U3 and U7.

FROM CARD SELECT DECODER
SX* LOWER 8K

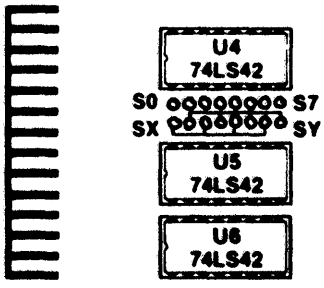
(U6) CHIP ENABLE	CHIP SET UPPER	CHIP SET LOWER	BLOCK	SHIPPED ADDRESS RANGE
CE1K*	U9	U17	MB0	8000 - 83FF
CE2K*	U10	U18	MB1	8400 - 87FF
CE3K*	U11	U19	MB2	8800 - 8BFF
CE4K*	U12	U20	MB3	8C00 - 8FFF
CE5K*	U13	U21	MB4	9000 - 93FF
CE6K*	U14	U22	MB5	9400 - 97FF
CE7K*	U15	U23	MB6	9800 - 9BFF
CE8K	U16	U24	MB7	9C00 - 9FFF

FROM CARD SELECT DECODER
SY* LOWER 8K

(U5) CHIP ENABLE	CHIP SET UPPER	CHIP SET LOWER	BLOCK	
CE9K*	U25	U33	MB8	A000 - A3FF
CE10K*	U26	U34	MB9	A400 - A7FF
CE11*	U27	U35	MB10	A800 - ABFF
CE12K*	U28	U36	MB11	AC00 - AFFF
CE13K*	U29	U37	MB12	B000 - B3FF
CE14K*	U30	U38	MB13	B400 - B7FF
CE15K*	U31	U39	MB14	B800 - BBFF
CE16K*	U32	U40	MB15	BC00 - BFFF

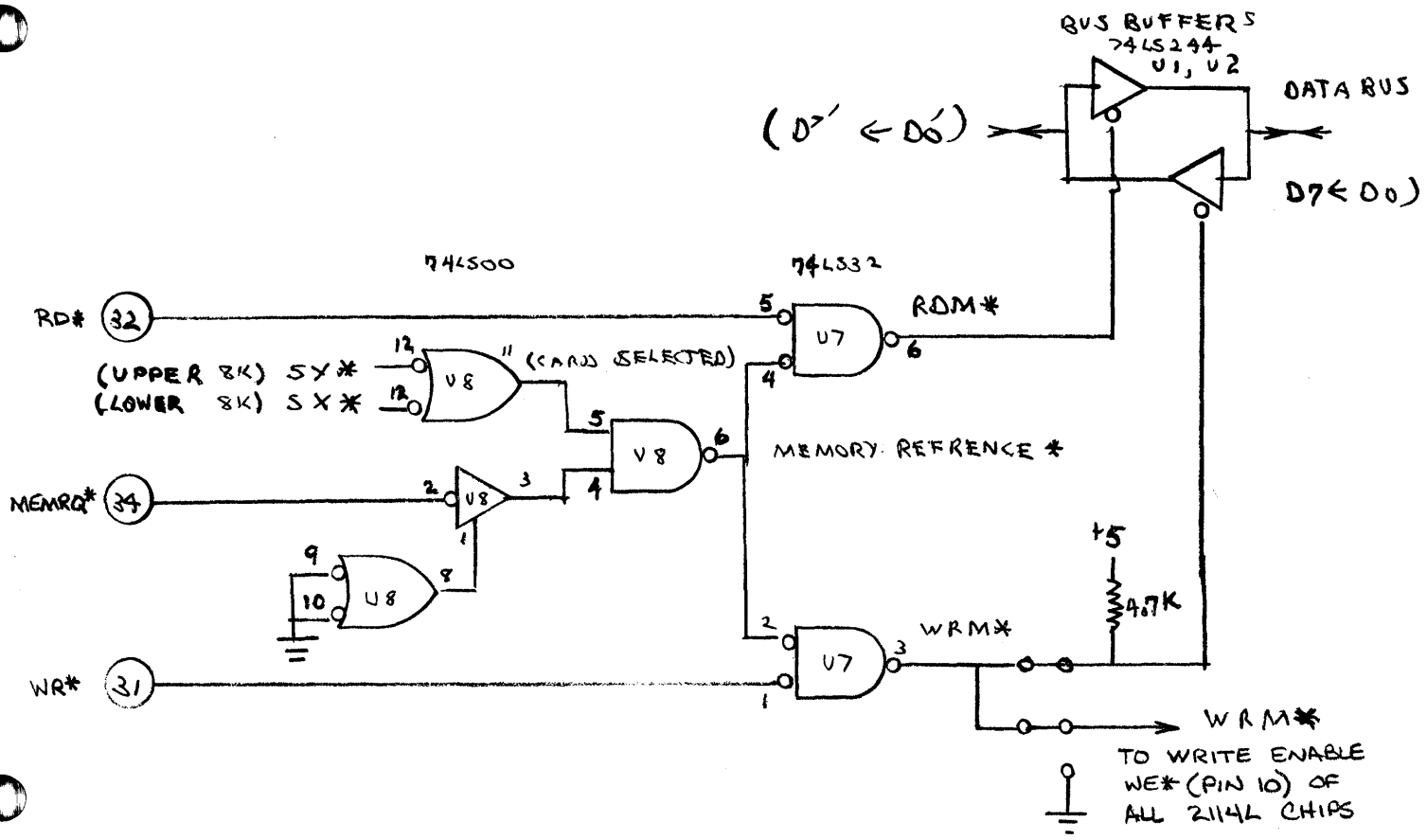
PAGE ↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	JUMPER SELECT TO X Y
0X		MB0				MB1				MB2				MB3			S0 TO SY
1X		MB4				MB5				MB6				MB7			
2X		MB8				MB9				MB10				MB11			S1 TO SX
3X		MB12				MB13				MB14				MB15			
4X		MB0				MB1				MB2				MB3			S2 TO SY
5X		MB4				MB5				MB6				MB7			
6X		MB8				MB9				MB10				MB11			S3 TO SX
7X		MB12				MB13				MB14				MB15			
8X		MB0				MB1				MB2				MB3			S4 TO SY
9X		MB4				MB5				MB6				MB7			
AX		MB8				MB9				MB10				MB11			S5 TO SX
BX		MB12				MB13				MB14				MB15			
CX		MB0				MB1				MB2				MB3			S6 TO SY
DX		MB4				MB5				MB6				MB7			
EX		MB8				MB9				MB10				MB11			S7 TO SX
FX		MB12				MB13				MB14				MB15			

MEMORY ADDRESS MAP & JUMPER SELECTION TABLE FOR 1K MEMORY BLOCK



Card Address Selection

4. READ, WRITE, AND BUS CONTROL



The write strobe to the 2114L chips and the read/write control signals for BUS BUFFER directional control is the implementation of the following Boolean Logic:

$$RDM^* = \overline{[(SX + SY) \cdot MERQ \cdot READ]}$$

$$WRM^* = \overline{[(SX + SY) \cdot MERQ \cdot WRITE]}$$

If Intel Mask ROM 3625 is to be used, it is necessary to cut the two traces of the WRM* line and ground pin 10 of all memory sockets. Pads are provided for this option. (PROMs and RAMs may not be mixed on the same card).

NOTE: The Card's data bus drivers (74LS244) U1 and U2 are enabled anytime a valid address is present even if memory chips are not plugged in. The card address range is chosen to prevent bus contention with other system memory elements including processor on-card memory, other memory cards, and memory mapped I/O.

5. ELECTRICAL SPECIFICATIONS

Vcc = +5V ±5%

Icc = 2.08A maximum (1.6A typical) with RAM

Power = 8.0 watts (typical)**

Sockets fully loaded (65mA per RAM maximum)

Address, Data, and Control Busses meet all STD BUS general electrical specifications except: A10, A11, A12 - These address bus inputs present 2 LSTTL loads maximum each.

STD/7701 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE) LSTTL	INPUT (LOADING) LSTTL	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE) LSTTL	INPUT (LOADING) LSTTL	MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	2		22	21		1	A4
A11	2		24	23		1	A3
A10	2		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*	1		34	33			IORQ*
MEMEX*	1		36	35			IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

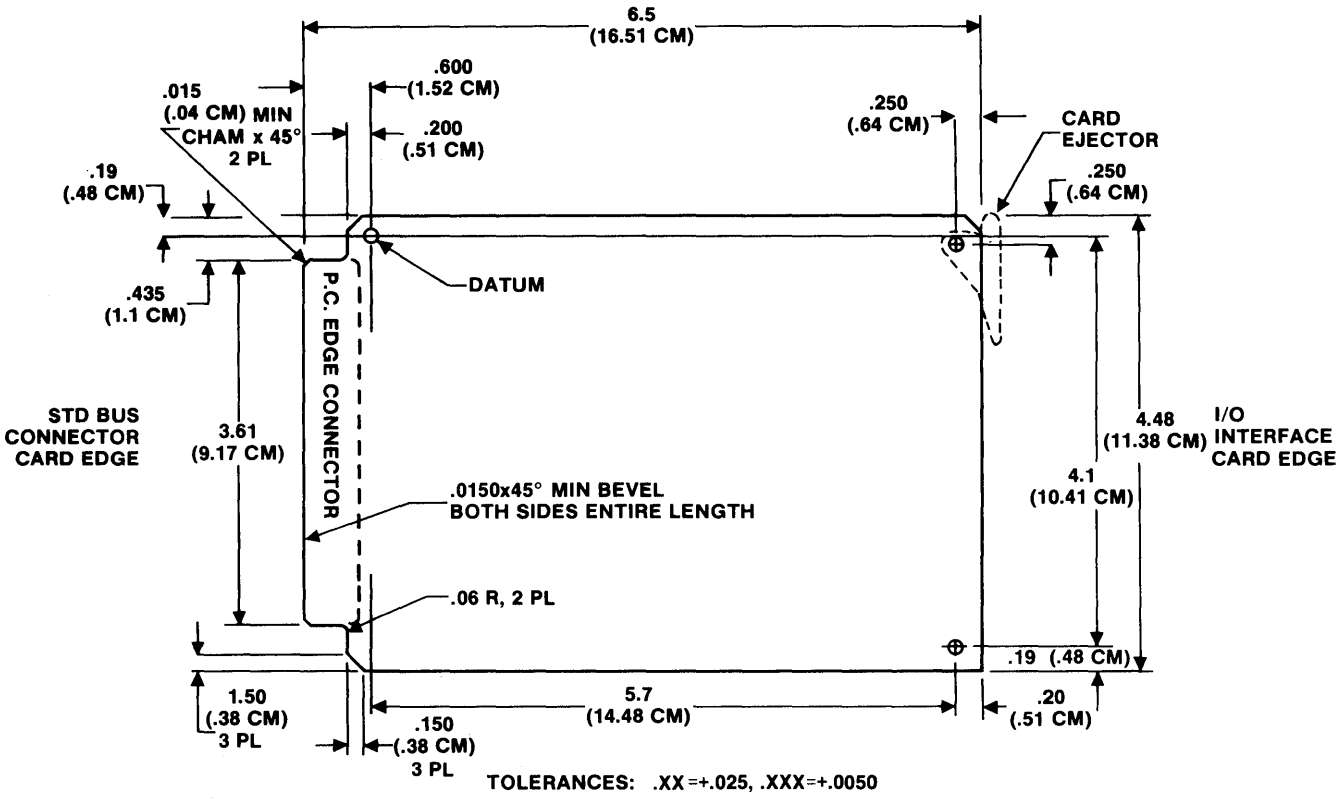
*Designates Active Low Level Logic

Edge Connector Pin List

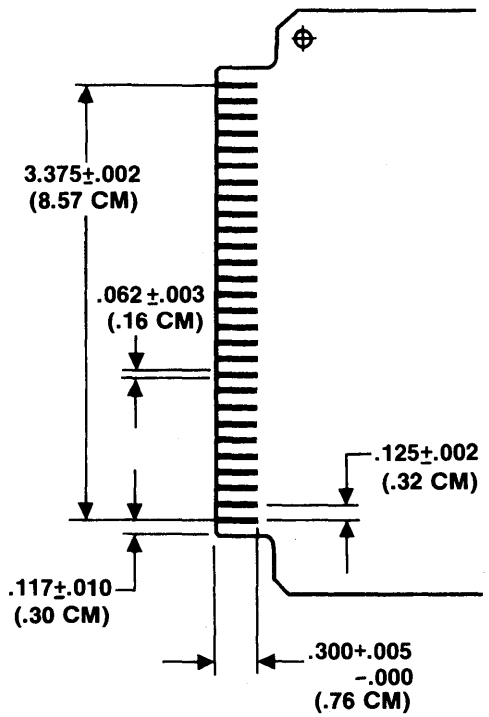
** See Appendix A, Thermal Considerations

6. MECHANICAL SPECIFICATIONS

The Series 7000 cards conform to the STD BUS standards, with the following additional requirements, including those shown.

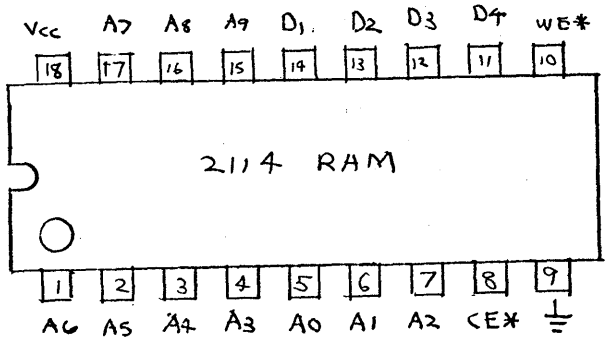


Series 7000 STD BUS Standard Card Outline

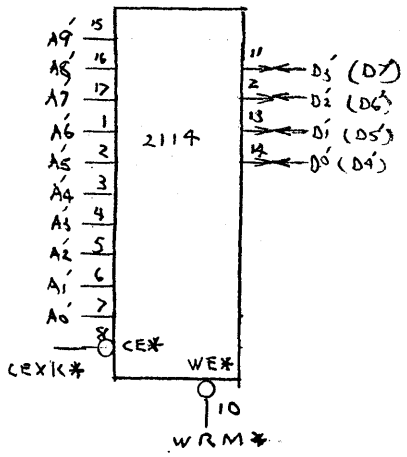


Series 7000 STD BUS Edge Card Finger Specifications

7. 2114 1024 x 4 BIT STATIC RAM DESCRIPTION

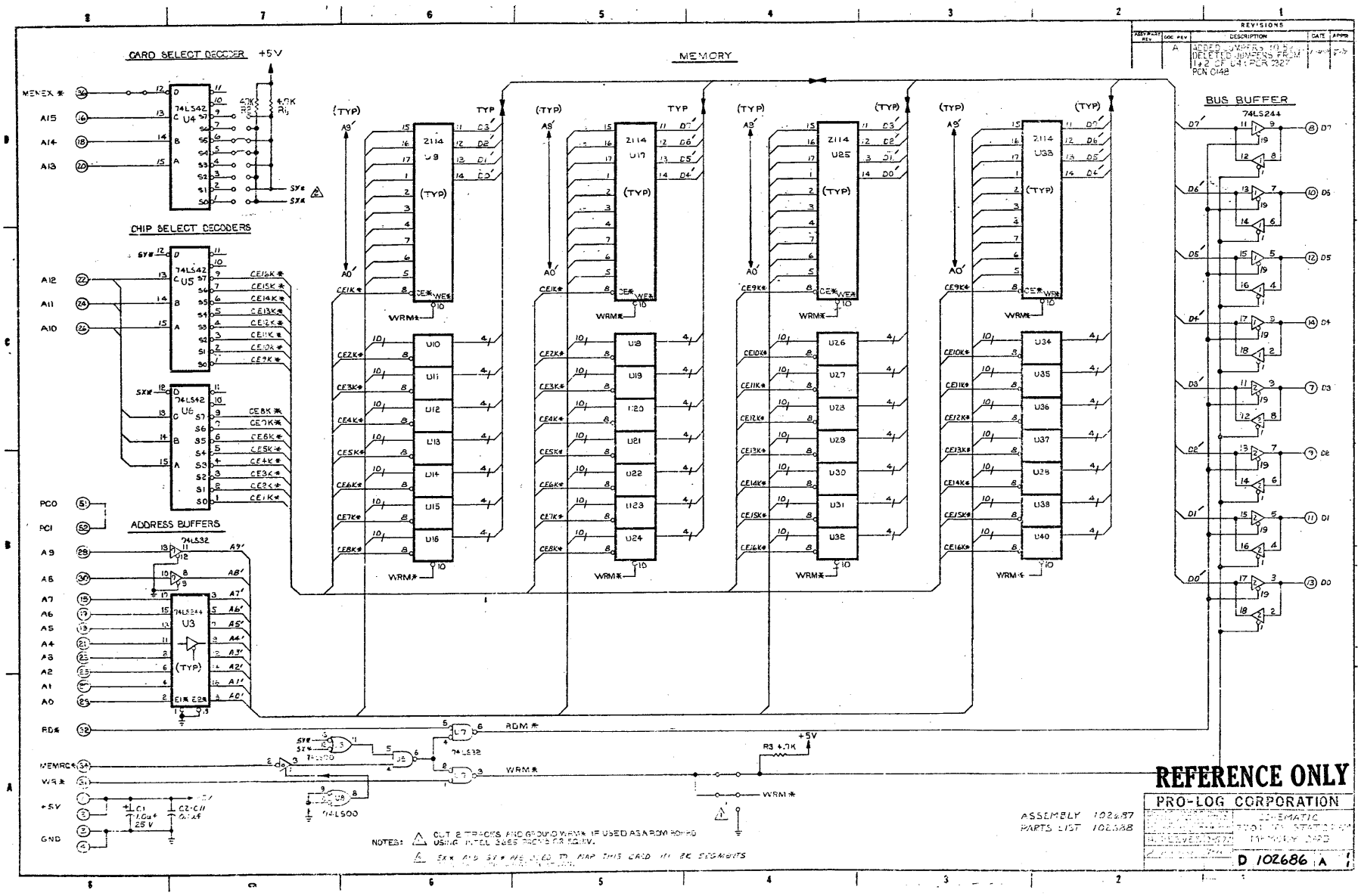


PIN CONFIGURATION

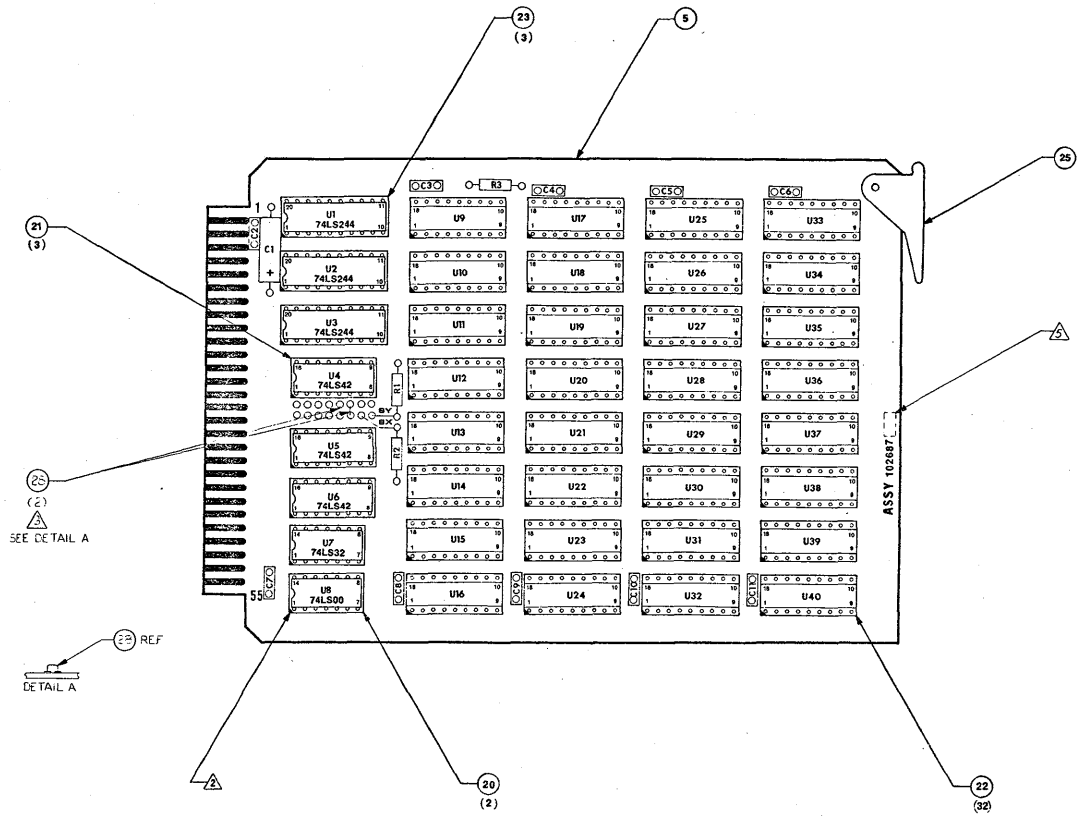


LOGIC DIAGRAM

2114 RAM PIN NAMES	ACTIVE STATE
A0 - A9 Address Inputs	High
D0 - D3 Data Input/Output	High
CE* Chip Enable	Low
WE* Write Enable	High Read/Low Write
Vcc Power (+5V)	-
⏚ Ground	-


CARD SELECT DECODER
+5V
MEMEX *
A15
A14
A13
74LS42
U4
SX*
SX*
CHIP SELECT DECODERS
A12
A11
A10
74LS42
U5
CE15K*
CE14K*
CE13K*
CE12K*
CE11K*
CE10K*
CE9K*
74LS42
U6
CE8K*
CE7K*
CE6K*
CE5K*
CE4K*
CE3K*
CE2K*
CE1K*
PCO
PCI
ADDRESS BUFFERS
74LS32
74LS244
U3
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
RD*
MEMRC*
WR*
+5V
GND
C1
1.0μF
25 V
C2-C11
0.1μF
74LS00
74LS32
RDM*
WRM*
R3 4.7K
+5V
WRM*
MEMORY
(TYP)
TYP
Z114
U9
U17
U25
U33
A9'
A0'
CE1K*
CE9K*
WE*
WRM*
U10
U11
U12
U13
U14
U15
U16
U18
U19
U20
U21
U22
U23
U24
U26
U27
U28
U29
U30
U31
U32
U34
U35
U36
U37
U38
U39
U40
CE2K*
CE3K*
CE4K*
CE5K*
CE6K*
CE7K*
CE8K*
CE10K*
CE11K*
CE12K*
CE13K*
CE14K*
CE15K*
CE16K*
BUS BUFFER
74LS244
D7'
D6'
D5'
D4'
D3'
D2'
D1'
D0'
D7
D6
D5
D4
D3
D2
D1
D0
REVISIONS
DESCRIPTION
DATE
APPR
ADDED JUMPERS TO E4
DELETED JUMPERS FROM
1 & 2 OF U4 PER 322
PCN 0148
NOTES:
CUT 2 TRACES AND GROUND W.E.N.* IF USED AS A ROM BOARD
USING INTEL 3665 PROMS OR EQUIV.
EX* AND SX* ARE USED TO MAP THIS CARD IN 8K SEGMENTS
ASSEMBLY 102687
PARTS LIST 102588
REFERENCE ONLY
PRO-LOG CORPORATION
SCHEMATIC
MEMORY CARD
D 102686 A 1

REVISIONS				
ASSY PART REV	DOC REV	DESCRIPTION	DATE	APPR
		[illegible]	[illegible]	[illegible]
	B	REVISED PER PCN 0383	[illegible]	[illegible]
	C	REVISED PER PCN 871.	[illegible]	[illegible]



REFERENCE ONLY

ITEM	DESCRIPTION	REF. DESIGNATION
10	47K, 1/4W, 5% CC	R1 - R2 E3
9		
8	0.1 uF 50V	C2 - C11
7	2.2 uF 25V	C1

PRO-LOG CORPORATION

ASSEMBLY 7701
16K STATIC RAM
MEMORY CARD

C.A. CLARK 7-5-77

D 102687 REV C SHT 1 OF 1

SCHEMATIC NO. 102686
PART S LIST NO. 102688

△5 IDENTIFY WITH ASSEMBLY REV LETTER USING RUBBER STAMP.

4. REF. DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND MAY NOT APPEAR ON ACTUAL PART.

△3 MAPPED AT 8000-9FFF. AND MAPPED AT A000-BFFF.

△2 INDICATES PIN NO. 1 OF SOCKETS (TYP).

1 FOR ASSY PROCEDURES SEE AS 1004.

NOTES: UNLESS OTHERWISE SPECIFIED.

10. SERIES 7000 MEMORY CARD TIMING

Series 7000 cards are designed to communicate over the STD BUS backplane in any combination without user timing considerations. The following information is provided to accommodate the use of pin compatible memory chip variations which can be used in the Series 7000 memory cards.

Figure 10-1 shows the functional blocks of the 7700 Memory cards. The delays contributed by these blocks are added to the memory chip delays and access times to determine the AC characteristics of the card. The table in Figure 10-2 gives maximum propagation delays for the memory card. For exact delays use the IC manufacturer's data sheets and the appropriate schematics.

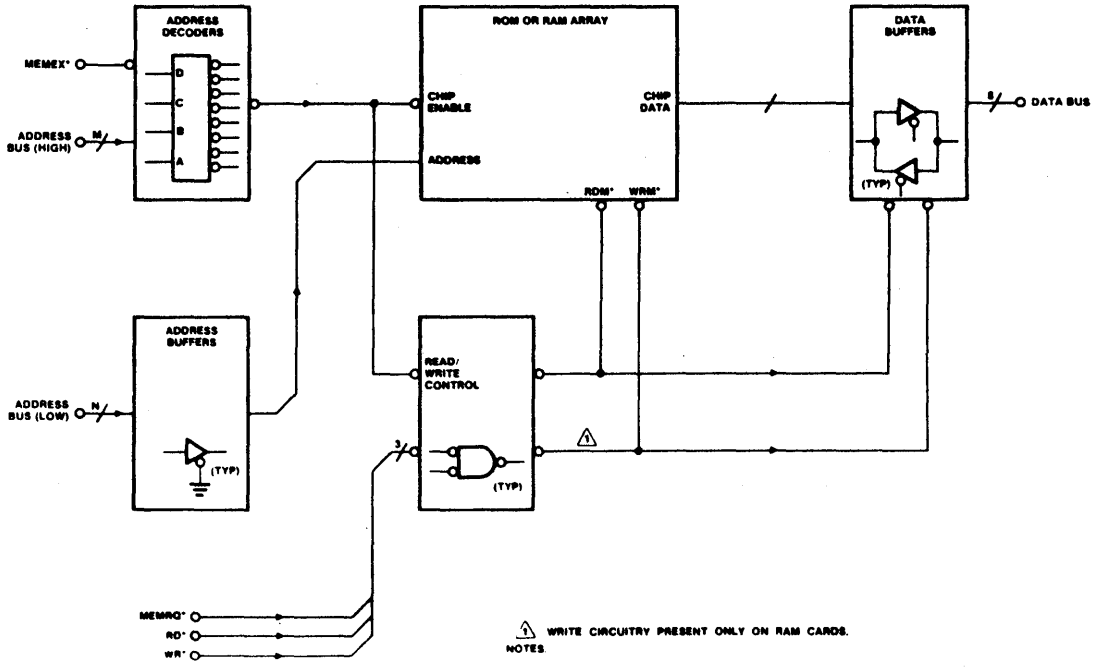


Figure 10-1 Memory Card Functional Blocks

CIRCUIT	PROPAGATION DELAY			LOAD CONDITIONS	
	FROM	TO	T_{PD} MAX	CL	RL
ADDRESS DECODERS	ADDRESS BUS OR MEMEX*	MEMORY CHIP ENABLE OR READ/WRITE ENABLE	75 ns	15 pF	—
ADDRESS BUFFERS	ADDRESS BUS	MEMORY CHIP ADDRESS	35 ns	160 pF	—
DATA BUFFERS	MEMORY CHIP DATA (OUT)	DATA BUS	20 ns	45 pF	4.7KΩ
	DATA BUS	MEMORY CHIP DATA (IN)	25 ns	80 pF	—
	READ WRITE CONTROL	VALID OUTPUT ENABLE	30 ns	100 pF	4.7KΩ
READ WRITE CONTROL	DECODER OUTPUT RD*, WR*, OR MEMRQ*	RDM* OR WRM* (RAMs ONLY)	70 ns		

Figure 10-2 Generalized Maximum Delays For Memory Cards

For example, the 2114 RAM chip's specified Data Read access time from an address change (A0-A9) is 450ns. In the 7701 this increased by the address buffers (35ns) and data buffers (20ns) to 505ns. In this case the decoding of A10-A15 and the Data Bus buffer control are presumed to occur during the RAM data access time.

APPENDIX A

PLAN #133 - THERMAL APPLICATION NOTE FOR MICROPROCESSOR SYSTEMS USING STD/SERIES 7000 CARDS

TABLE OF CONTENTS

ILLUSTRATIONS

TABLES

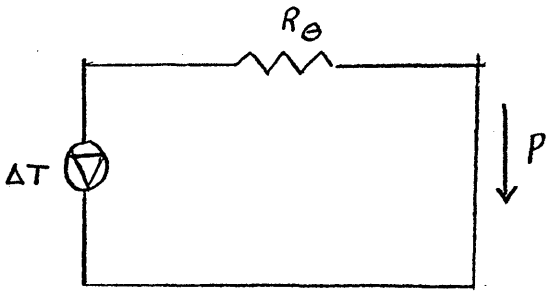
THERMAL APPLICATION NOTE FOR MICROPROCESSOR SYSTEMS USING STD/SERIES 7000 CARDS

SECTION 1 - INTRODUCTION

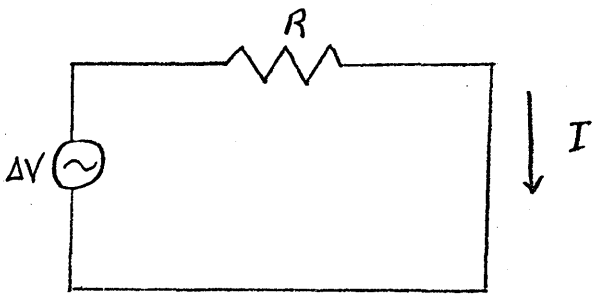
The failure rate of many electrical components is an exponential function of junction temperature. Temperature rise from ambient to junction temperature depends on many factors such as power density i.e. watts/inch^3, air velocity over the high dissipating components, thermal resistance (junction-to-case) and dissipation of the component, and the thermal characteristics of the cabinet which houses the system.

This application note is intended to aid the user in estimating and solving his thermal problems. Sample analyses of two Series 7000 Systems are included, as well as suggestions for minimizing thermal effects.

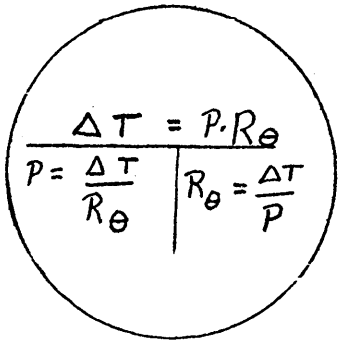
Heat flow is analogous to current flow in an electrical circuit. The electrical and thermal equivalent are presented in Figure 1.



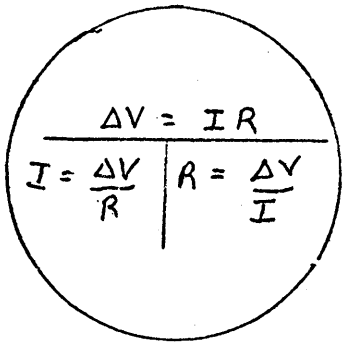
THERMAL CIRCUIT



ELECTRICAL CIRCUIT



THERMAL EQUATIONS



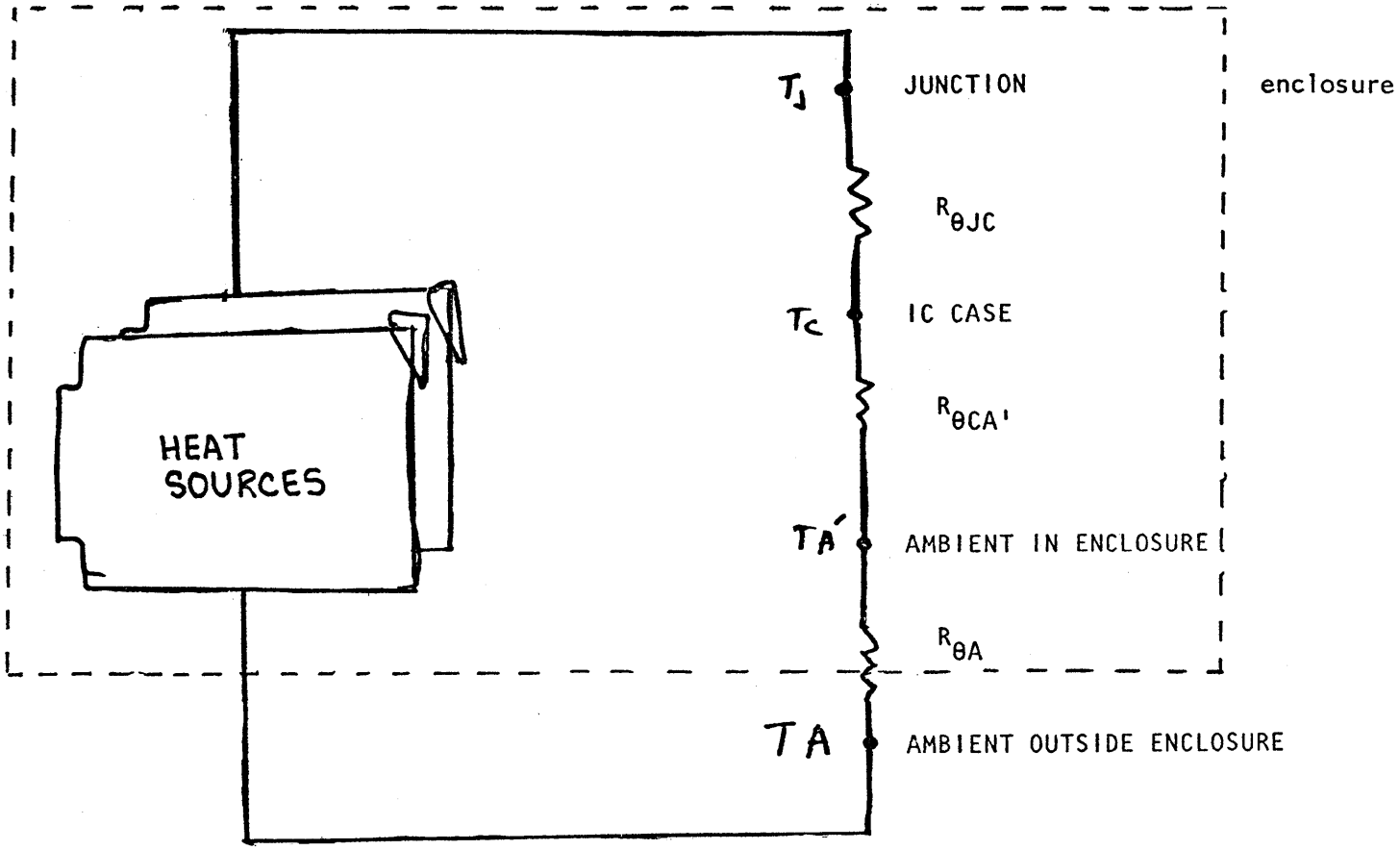
ELECTRICAL EQUATIONS

THERMAL		
SYMBOL	NAME	UNITS
P	POWER (HEAT FLOW)	WATTS
T	TEMPERATURE DIFFERENCE	°C
R_θ	THERMAL RESISTANCE	°C/W

ELECTRICAL		
SYMBOL	NAME	UNITS
I	CURRENT	AMPS
V	VOLTAGE DIFF.	VOLTS
R	ELECTRICAL RESISTANCE	OHMS

FIGURE 1 - THERMAL AND ELI

Figure 2 shows STD cards as heat sources in an enclosed digital system. The heat generated by a card is the sum of numerous heat sources: the heat generated by ICs plus any singular components. Most heat is generated in the different junctions within the IC. An average thermal resistance between any junction and the case is assumed. Heat flow from an IC with a junction temperature T_J encounters the junction-to-case thermal resistance $R_{\theta JC}$ and raises the case temperature to T_C. From the IC case, the heat flows through $R_{\theta CA'}$ to the ambient air in the enclosure, and finally through $R_{\theta A}$ to give T_A the ambient temperature outside the enclosure



T_J - IC junction temperature
T_C - IC case temperature
$T_{A'}$ - Ambient temperature in enclosure
T_A - Ambient temperature outside enclosure
$R_{\theta JC}$ - Thermal resistance, junction-to-case
$R_{\theta CA'}$ - Thermal resistance, junction-to-ambient in enclosure
$R_{\theta A}$ - Thermal resistance, ambient in enclosure to ambient outside enclosure

FIGURE 2 - HEAT FLOW IN ENCLOSED DIGITAL SYSTEM

When many heat sources are involved, the thermal circuit becomes quite complex. The use of analysis with assumptions, approximations, and experimental techniques is necessary to understand the problems and find practical solutions.

SECTION 2 - THERMAL CONSIDERATIONS FOR STD SYSTEMS

Pro-Log Series 7000 logic cards are designed with components rated at +70°C or higher. We recommend a maximum ambient free-air temperature of +55°C for this system. This provides for a +30°C temperature rise over normal room temperature.

Card placement and card rack orientation are important considerations in configuring a system. Distribution of power throughout the card rack can contribute to optimizing system performance and lifetime. Even power distribution can be achieved by spacing high power-dissipating cards between cards of lower power.

In an STD/Series 7000 system a sequence of six cards such as 7803 CPU, 7702 ROM, 7602 I/O, 7701 RAM, 7502 I/O, 7604 I/O is a good example of even power distribution. This sequence was used in Example 2. Nominal power dissipation for these and other Series 7000 cards is listed in Table 1.

Further temperature reduction can be achieved by leaving a card slot empty adjacent to the component side of a high power dissipating card, or by providing forced air cooling to improve air circulation in the card rack.

This application note includes sample calculations for two system situations. Example 1 is for three fully loaded 7701 RAM cards on 1/2" and 1" centers. Example 2 is for six cards sequenced as listed above, for 1/2" centers and again for 1" spacing on component side of 7701 RAM card. (See Configuring a Typical System)

To determine whether a particular card's temperature parameters will be exceeded, the user can calculate the maximum acceptable ambient temperature with the method outlined below.

1. Measure the case temperature (T_C) of the hottest device or devices on the card(s) in question. This can be accomplished by placing a thermocouple probe imbedded in silicone grease in the sockets under selected IC's. Typically this T_C will result in the worst case junction temperature (T_J).
2. Use the data in Table 2 to determine the maximum acceptable device junction temperature (T_J). This table shows different failure acceleration factors for different temperatures (T_J).
3. Use Table 3 to find the approximate thermal resistance junction-to-case for the device or devices being considered. For more accurate calculations use the $R_{\theta JC}$ from the specific device manufacturer.
4. Using the manufacturer's data sheets, determine the maximum power the device dissipates.
5. Calculate the maximum T_A' acceptable. See sample calculations.
6. If the card cage is enclosed, measure the exhaust temperature ($T_{A'}$) after the temperature has stabilized. If this temperature is much above T_A, subtract T_A from $T_{A'}$ and lower the acceptable $T_{A'}$ calculated for the system by this amount.

CARD NO.	CARD NAME	NOMINAL POWER WATTS
7504	TRIAC	16.75W (maximum)
7502	RELAY	1.50
7506, 7503	OPTO ISOLATED INPUT	2.90
7601	TTL I/O	1.50
7602	TTL IN	1.10
7603	TTL I/O	1.75
7604	TTL I/O	2.30
7701	RAM	8.00
7702	CPUROM	1.00
7801	CPU 8085	5.00
7802	CPU 6800	6.30
7803	CPU Z80	6.00

TABLE 1 - TYPICAL POWER DISSIPATIONS FOR SERIES 7000 CARDS

EXAMPLE 1 - SAMPLE CALCULATIONS 7701 MEMORY CARD

	Calculations for 7701 Memory Card with 16K/2114L's convection/cooling	
Equations, Assumptions and Constants	1/2" Spacing ④	1" Spacing ④
Absolute $T_J = 125^oC$ Desired Maximum $T_J = 115^oC$ Hottest IC for 7101 RAM card is 2114L in center of card ① $R_{\theta JC} = 45^oC/watt$ Pmax(2114L) = 0.37 W	$T_A = 23.2^oC$ $T_C = 93.2^oC$ (measured)	$T_A = 23.2^oC$ $T_C = 65.2^oC$ (measured)
$T_J = T_C + R_{\theta JC} \cdot (Pmax)$	$T_J \leq 93.2^oC + (45^oC/W)(.37W)$ $T_J \leq 93.2^oC + 17^oC = 110.2^oC$	$T_J = 65.2^oC + (45^oC/W)\ .37W$ $T_J = 65.2^oC + 17^oC = 82.2^oC$
$\Delta T = T_J$ maximum desired - T_J calculated	$\Delta T = 115^oC - 110.2^oC = 4.8^oC$	$\Delta T = 115^oC - 82.2^oC = 32.8$
Maximum $T_A' = T_A$ measured $+\Delta T$	Maximum $T_A' = 23.2^oC + 4.8^oC = 28^oC$	Maximum $T_A' = 23.2^oC + 32.8^oC = 56^oC$

① The data taken was on the center card of 3 adjacent memory cards.

② Abreviations: T_A = Temperature ambient, T_J = Temperature junction, T_C = Temperature case, $R_{\theta JC}$ = Thermal resistance junction to case, P = Power

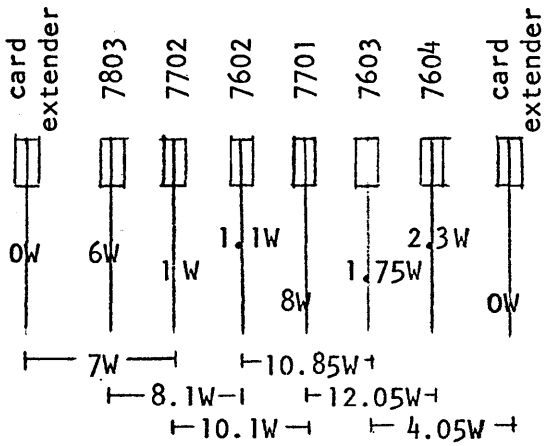
③ The data was taken on cards mounted in a Pro-Log card cage with 3/8" rubber feet

④ Data was taken on the center card of 3 memory cards on the indicated spacing

SECTION 3 - CONFIGURING A TYPICAL SYSTEM

The three card spacing arrangements below show three possible system configurations to distribute power dissipation and heat. The first two correspond to the calculations in example 2 which follows. An improvement of 6°C in the calculated $T_{A'}$ was attained by the addition of a space near the component side of the 7701 RAM card. The third configured system may not be optimal. The additional space may give better result if it is also on the component side of the RAM card. This depends on the power dissipated on the card adjacent to the circuit side of the RAM card and other system characteristics.

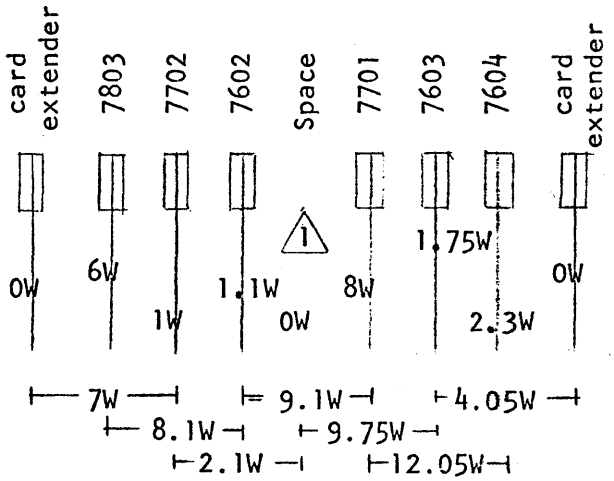
First attempt for power distribution Example 2 (See sample calculation $T_{A'}$ = 52°C)



All cards on 1/2" centers.

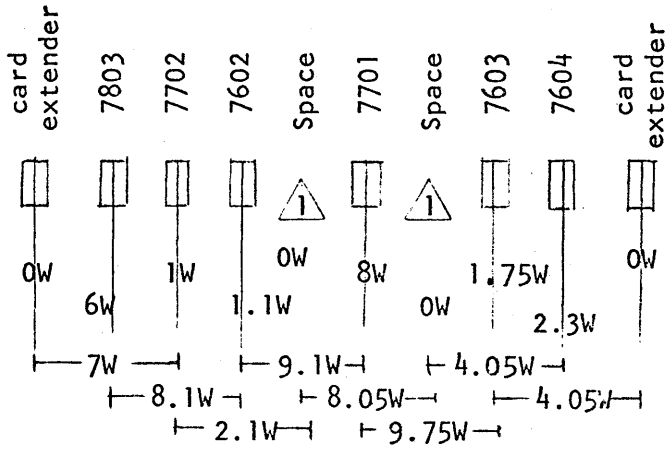
Power distribution in groups of 3 card slots

Second attempt for power distribution (See example 2 sample calculation $T_{A'}$=56°C)



As above except 1" spacing on component side of 7701 RAM card.

Third attempt for power distribution (no sample calculations included in text)



As above except 1" space on both sides of 7701 RAM card

1 Primary consideration should be given to the space provided on the component side for the high power dissipating card.

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EXAMPLE 2 - CALCULATION STD/7000 MIXED CARD SYSTEM

Equations, Assumptions and Constants	7701 Memory Card with 16K/2114L's convection cooling	
	1/2" spacing	1" spacing component side 7701 only
Absolute $T_J = 125^oC$ Desired maximum $T_J = 115^oC$ Hottest IC for 7701 RAM card is 2114L in center of card $R_{\theta JC} = 45^oC/watt$ Pmax (2114L) = 0.37W TA = 24^oC	$T_A = 24.8^oC$ $T_C = 70.8^oC$ (measured)	T_A of 24.8^oC $T_C = 64.8^oC$ (measured)
$T_J = T_C + R_{\theta JC} \cdot$ (Pmax)	$T_J = 70.8^oC + (45^oC/W)(0.37W)$ $T_J = 70.8^oC + 17^oC = 87.8^oC$	T_J $64.8^oC + (45^oC/W)(0.37W)$ T_J $64.8^oC + 17^oC = 81.8^oC$
$\Delta T = T_J$ maximum desired - T_J Calculated	$\Delta T = 115^oC - 87.8^oC = 27.2^oC$	$\Delta T = 115^oC - 81.8^oC = 33.2^oC$
T_A' maximum - T_A measured + ΔT	Maximum $T_A' = 24.8^oC + 27.2^oC$ T_A' max = 52^oC	Max $T_A' = 24.8^oC + 33.2^oC = 58^oC$ T_A' max. = 58^oC

NOTE: These calculations are for the first two of three examples of configuring a system for even power (heat distribution). See figure

The data taken on cards mounted in a Pro-Log CR16A card cage with 3/8" rubber feet.

SECTION 4 - FAILURE RATE ACCELERATION DUE TO T_J

Table 2 indicates the relative failure rate as a function of junction temperature based on the assumption that the Arrhenius relationship is valid and that the average activation energy is 0.6eV. $T_J = 55^oC$ is used as the reference temperature. It should be noted that different device manufacturers' assumptions may vary from those upon which the acceleration factors in Table 1 are based.

Additional design margin is recommended if T_J is above 105^oC. Also, a more thorough analysis should be done if the designer's system causes T_J to exceed 105^oC for any length of time.

TABLE 2 - FAILURE RATE AS A FUNCTION OF T_J

RECOMMENDATIONS	T_J	ACCELERATION FACTORS	
		Relative to 55^oC	Incremental
Good Operating Range	55^oC	1.00	1.8
	65^oC	1.87	1.87
	75^oC	3.39	1.75
	85^oC	5.92	1.70
	95^oC	10.04	1.65
Acceptable for Intermittant Operation	105^oC	16.56	1.61
	115^oC	26.62	
Not Recommended	125^oC	41.78	1.57

Example: The MTBF (mean time to failure) for a device with $T_J = 55^oC$ will on the average be 3.39 times longer than the MTBF for the same device with $T_J = 75^oC$.

SECTION 5 - THERMAL RESISTANCE OF ICs

Typical thermal resistance values of standard plastic integrated circuit packages are shown in Table 3. The values shown do not imply any guarantee, but represent the latest and best available data. Steady-state thermal conditions are assumed in the resistance measurements. Also, the following definitions apply:

Table 3 Conditions and Definitions

$R_{\theta JC}$ - Thermal resistance from junction to case using freon as a heat sink. This parameter offers good reapeatability and a high degree (±5%) of correlation.

$R_{\theta JA}$ - Thermal resistance from junction to still air (25°C ambient) with package in a specified socket. This parameter is highly dependent on test conditions which are difficult to reproduce accurately.

PACKAGE DESCRIPTION	°C/WATT (1)		SOCKET USED FOR $R_{\theta JA}$ MEASUREMENT	POWER (mW)
	$R_{\theta JC}$ ±5%	$R_{\theta JA}$ ±15%		
8-Pin Plastic DIP	52	95	Augat	300
14- or 16-Pin Plastic DIP	45	90	Augat	300
24-Pin Plastic DIP	35	65	Barnes	500
14- or 16-Pin Ceramic DIP	20	70	Augat	300
24 lead Ceramic, Kovar Lid	15	50		
14 or 16 lead with glass seal	27	95		
24 lead ceramic with glass seal	12	50		
14- or 16-pin Ceramic Flat Pak (alloy mounted)	45	160	Barnes Carrier/ Contactor	500
14-Pin Ceramic Flat Pak (glass mounted)	70	190	Mech-Pak Carrier	300
8- or 10-Pin Plug-In (alloy mounted)	40	120	Barnes	400
8- or 10-Pin Plug-In (glass mounted)	90	170	Barnes	700

TABLE 3 - THERMAL RESISTANCE OF TYPICAL IC PACKAGES

(1) For more accurate calculations use values given by the device manufacturer

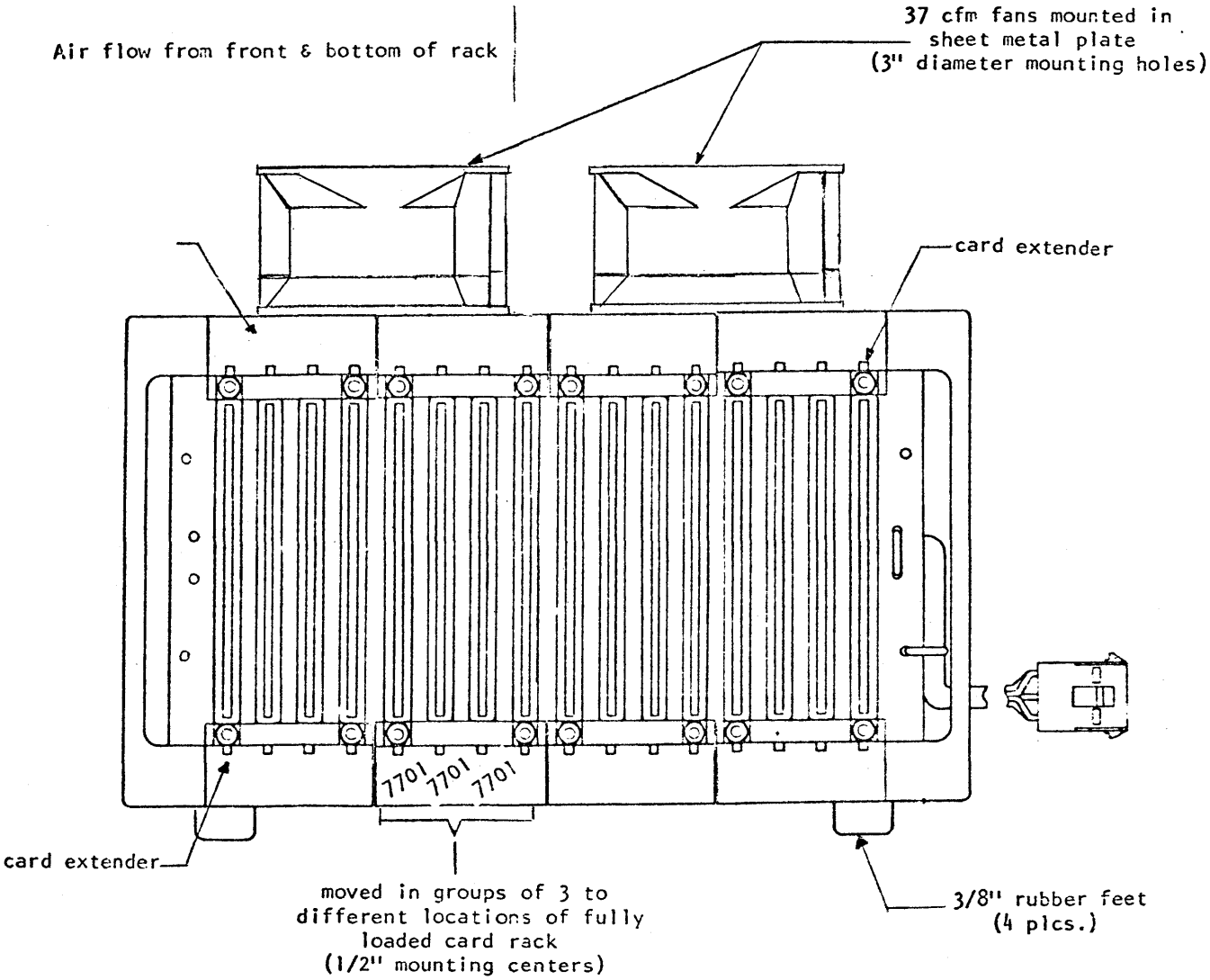
SECTION 6 - FORCED AIR COOLING

The card cage configuration shown below was used to evaluate the effects of forced-air cooling. A 37 cfm (no head) fan was mounted over each 8-slot section of the card cage. The temperature was then monitored at different locations on the center card of the three adjacent 7701 RAM cards.

It was found that for this forced-air cooling configuration, the hottest IC on the card was at the top center of the memory chip array. The case temperature (T_C) of the hottest 2114Ls was, in every instance, within 20°C of ambient (T_A).

Note that, without forced-air cooling, the hot spot on the card was at the center of the memory chip array rather than at the top of the card.

For design of systems using forced-air, refer to fan manufacturer literature such as "How to Select the Optimum Fan for Your Application" by Pamotor Corp., 770 Airport Blvd., Burlingame, Ca., 94010.



SECTION 7 - CONCLUSION

If power dissipation is evenly distributed throughout an STD/Series 7000 system, convection cooling is often sufficient to maintain the ambient in the enclosure at an acceptable level. However this should never be assumed. Rather the designer should assess his particular system's thermal requirements.

It should be noted that the desired ambient may also be limited by components other than ICs. For example, the temperature limitations of special components, such as batteries, may add additional temperature constraints to the system.

By applying the principles presented in this application note, the designer can determine the thermal profile of his system and optimize its life expectancy.

USER'S MANUAL

2411 Garden Road
Monterey, California 93940
Telephone: (408) 372-4593
TWX: 910-360-7082

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