

MODEL 70/752 VIDEO DATA TERMINAL

Maintenance Manual

# REVISION INSTRUCTIONS AND MANUAL HISTORY 

EQUIPMENT: 70/752 Video Data Terminal
PUBLICATION NO. 70-01-752-1
PURPOSE: Adds Theory and Parts location information for the RCA High Voltage Power Supply (2166024) to 70/752 Reissue, dated 080169.

NOTE: This revision reflects ERL 25 only; ERL 21 thru 24 are not included.

REVISION INSTRUCTIONS: Delete and add pages as shown on the following table. File this page in front of page iii.

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| Title page, ii, A85 ADD |  |
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## MANUAL HISTORY

| REV. <br> NO. | REV. <br> TVPE | DATE <br> ISSUED | CONTROL <br> DOC. NO. | ERL |
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| 1st Ptg. | - | 100167 | 2149850 | 2 |
| 2nd Ptg. | R | 080169 | 2149850 | 20 |
| Rev.1 | 1 | 032770 | 2149850 | 25 |
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## REVISION INSTRUCTIONS AND MANUAL HISTORY

EQUIPMENT: 70/752 Video Data Terminal PUBLICATION NO. 70-01-752-2
PURPOSE: Incorporates a new Keyboard Drive Train Adjustment procedure.

REVISION INSTRUCTIONS: Delete and add pages as shown on the following table. File this page in front of page iiA.

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| $4-20$ | iiB, 4-20, 4-20A, 4-20B |  |
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MANUAL HISTORY


## REVISION INSTRUCTIONS AND MANUAL HISTORY

## EQUIPMENT: 70/752 Video Data Terminal

PUBLICATION NO. 70-01-752-3
PURPOSE: This revision incorporates all outstanding 70/752 TIPs (except PM and recommended spares) to appropriate sections of the maintenance manual for the Model 70/752 Video Data Terminal.

Also included in this revision are important cautions pertaining to the new High Voltage Power Supply (2166024-503). The cautions contain mandatory instructions relating to power supply adjustments when components of the supply are replaced.

REVISION INSTRUCTIONS: Delete and add pages as shown on the following table. File this page in front of page iiB.

| DELETE | ADD |
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| 1-15, 1-16, 4-7, 4-8, 4-15, 4-16, 4-19, thru 4-208, 4-31 thru 4-36, 4-43, 4-44, 5-29 thru 5-34. <br> 70/752 TIPs \#3.1, \#4.2, \#5, \#6, \#7, \#8, \#13, \#14, \#15, \#17 | $\begin{aligned} & \text { iiC, } 1-15,1-16,4-7,4-8,4-14 A, 4-14 B, 4-15 / 4-16 \text {, } \\ & 4-19,4-20,4-20 A, 4-20 B, 4-31,4-32,4-32 A, 4-32 B \text {, } \\ & 4-33,4-34,4-35,4-36,4-36 A / 4-36 B, 4-43,4-44, \\ & 4-45,4-46,5-29 \text { thru } 5-35 \end{aligned}$ |

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## MANUAL HISTORY

| REV. NO. | *REV. <br> TYPE | DATE ISSUED | CONTROL DOC. NO. | ERL |
| :---: | :---: | :---: | :---: | :---: |
| 1st Ptg | - | 100167 | 2149850 | 2 |
| 2nd Ptg | R | 080169 | 2149850 | 20 |
| Rev 1. | I | 032770 | 2149850 | 25 |
| Rev 2 | 1 | 072770 | 2149850 | 25 |
| Rev 3 | 1 | 030571 | 2149850 | 25 |


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iiC

PUBLICATION NO. 70-01-752-4
PURPOSE: This revision adds a CAUTION to the Deflection Yoke replacement procedure to ensure that the associated Deflection Amplifier is modified (when necessary) to increase the horizontal gain to produce the correct screen raster.

Also included in this revision are CAUTIONS and revised resistor values to the Deflection Amplifier IPB.

REVISION INSTRUCTIONS: Delete and add pages as shown on the following table. File this page in front of page iic.

| DELETE | ADD |
| :---: | :---: |
| $4-13,4-14$, A19, A20, A43, A44 | iiD, 4-13, 4-14, A19, A20, A43, A44 |

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| 1st Ptg. | - | 10/67 | 2149850 | 2 |
| 2nd Ptg. | R | 08/69 | 2149850 | 20 |
| Rev 1 | 1 | 03/70 | 2149850 | 25 |
| Rev 2 | 1 | 07/70 | 2149850 | 25 |
| Rev 3 | 1 | 03/71 | 2149850 | 25 |
| Rev 4 | 1 | 06/71 | 2149850 | 25 |



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## REVISION INSTRUCTIONS AND MANUAL HISTORY

EQUIPMENT: Model 70/752 Video Data Terminal PUBLICATION NO. 70-01-752-5<br>PURPOSE: This revision contains an entirely new lllustrated Parts Breakdown for the mechanical keyboard used in the Video Data Terminal. Numerous parts and assemblies not previously identified are added, along with associated part numbers. Vendor part numbers are listed wherever RCA numbers are not available.

This revision also corrects stock numbers in the Viewer plug-in boards.

REVISION INSTRUCTIONS: Delete and add pages as shown on the following table. File this page in front of page iiD.

| DELETE | ADD |
| :---: | :---: |
| Pages A1 through A8, A15, A16, A19, A20, A33, A34, A41, <br> A42, A47, and A48. | Pages iiE, A1 through A8U/A8V, A15, A16, A19, A20, A33, <br> A34, A41, A42, A47, and A48. |

NOTE: Revised pages are marked with the Rev. No. in the upper unbound corner. Revised areas are marked with a vertical bar.

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| :---: | :---: | :---: | :---: | :---: |
| 1st Ptg | - | 10/67 | 2149850 | 2 |
| 2nd Ptg | R | 08/69 | 2149850 | 20 |
| R1 | 1 | 03/70 | 2149850 | 25 |
| R2 | 1 | 07/70 | 2149850 | 25 |
| R3 | 1 | 03/71 | 2149850 | 25 |
| R4 | 1 | 06/71 | 2149850 | 25 |
| R5 | 1 | 08/71 | 2149850 | 30 |


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REVISION INSTRUCTIONS: Delete and add pages as shown on the following table. File this page in front of page iiE.

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| $5-29$ thru 5-36 |  |

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| 1st Ptg. | - | $10 / 67$ | 2149850 | 2 |
| 2nd Ptg. | R | $08 / 69$ | 2149850 | 20 |
| Rev 1 | 1 | $03 / 70$ | 2149850 | 25 |
| Rev 2. | I | $07 / 70$ | 2149850 | 25 |
| Rev 3 | I | $03 / 71$ | 2149850 | 25 |
| Rev 4 | I | $06 / 71$ | 2149850 | 25 |
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| Page 4-36A/4-36B. |  |
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| R4 | 1 | $06 / 71$ | 2149850 | 25 |
| R5 | 1 | $08 / 71$ | 2149850 | 30 |
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## REVISION INSTRUCTIONS AND MANUAL HISTORY

| EQUIPMENT: | Model $70 / 752$ Video Data Terminal PUBLICATION NO. 70-01-752-8 |
| :--- | :--- | :--- |
| PURPOSE: | Provides information for the incorporation of the Data Set Cable, Special Feature 5766. Adds installation <br> requirements for the Flexible Character Array, Special Feature $5734-01$. |

REVISION INSTRUCTIONS: Delete and add pages as shown on the following table. File this page in front of page iiG.

| DELETE | ADD |
| :---: | :---: |
| Pages 1-21, 1-22, 3-73, and 3-74 | Pages iiH, 1-21, 1-22, 3-73, and 3-74 |

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| Rev 1 | 1 | $03 / 70$ | 2149850 | 25 |
| Rev 2 | 1 | $07 / 70$ | 2149850 | 25 |
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| Rev 7 | 1 | $04 / 72$ | 2149850 | 33 |
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## UNIVAC SERIES 70

REVISION INSTRUCTIONS AND MANUAL HISTORY

EQUIPMENT: Model 70/752 Video Data Terminal
PUBLICATION NO. 70-01-752-UR9

PURPOSE: This revision contains the following:

1. Corrects contents pages to reflect changes made by previous revisions.
2. Adds new delay line parts breakdown to Appendix B, Pages B15 and B16.

REVISION INSTRUCTIONS: Delete and add pages as shown in the below table. File this page in front of page iiH.

| DELETE | ADD |
| :---: | :---: |
| RCA Title Page, Pages iii thru xi, Aii | UNIVAC Title Page, Pages iil, iii thru xiii, Ai thru Aiv, <br> B15, B16 |

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| REV. <br> NO. | *REV. <br> TYPE | DATE <br> ISSUED | CONTROL <br> DOC.NO. | ERL |
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| 1st Ptg | - | $10 / 67$ | 2149850 | 2 |
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| R1 | I | $3 / 70$ | 2149850 | 25 |
| R2 | I | $7 / 70$ | 2149850 | 25 |
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## UNIVAC SERIES 70

REVISION INSTRUCTIONS AND MANUAL HISTORY

## EQUIPMENT: Model 70/752 Video Data Termina

PUBLICATION NO.

PURPOSE: This interim revision changes the 70/752 Maintenance Manual as follows:

1. Adds two callouts to Figure $2 B$ to identify the left-hand and right-hand key lever spring on the Keyboard Assembly.
2. Adds cross references between early and late models of Keyboard Assembly.

REVISION INSTRUCTIONS: Delete and add pages as shown in the below table. File this page in front of page iil.

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| Rev 1 | I | $3 / 70$ | 2149850 | 25 |
| Rev 2 | I | $7 / 70$ | 2149850 | 25 |
| Rev 3 | I | $3 / 71$ | 2149850 | 25 |
| Rev 4 | I | $6 / 71$ | 2149850 | 25 |
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# SECTION ONE <br> INTRODUCTION 

### 1.1 GENERAL

The Model 70/752 Video Data Terminal is a completely self-contained, input/output device which permits an operator at a remote station to interchange information with a central computer facility via standard telephone lines. The Video Data Terminal (VDT) consists of two major assemblies, the Viewer and the Control Panel. The Viewer contains the display tube, display memory, character generator, input/output logic, data set interface, power supply, and the circuitry required for video and for read, write, and erase operations. The Control Panel contains the keyboard and controls to operate the VDT. The central computer may be ar RCA Spectra $70 / 35,45,46,55$, or 60 processor.

### 1.1.1 SYSTEM CONFIGURATION (Refer To Figure 1-1.)

A 70/752 VDT may be linked to one of the processors by one multiplexor trunk connected to a 70/720-21 Asynchronous Data Set (ADS) Buffer housed in a 70/668 Communications Controller-Multichannel (CCM). The VDT may also be remotely located from the processor. In this case, the VDT is connected to a communications link consisting of an AT \& T 202C or 202D Data Set or equivalent, a voice-grade communications channel, and another 202C or 202D Data Set, or equivalent. The data set on the processor site is then connected to the 70/720-21 ADs Buffer.


Figure 1-1. System Configuration

In either installation the VDT operates in a half duplex mode at a transmission rate up to 120 characters per second.

Up to 8 VDTs may be connected to a $70 / 755$ Video Data Switch (VDS) which may be connected to the 70/720-21 Buffer or to a communications link.

### 1.2 FUNCTIONAL DESCRIPTION

The 70/752 VDT provides a means of communicating with a central computer facility and gives the operator a means of entering data in and retrieving data from the central computer.

The terminal contains a 12 -inch rectangular cathode-ray tube that can simultaneously display a maximum of 1,080 characters in 20 lines of 54 characters per line, and a 4-row keyboard to generate data characters and control codes.

A maximum character set of 64 different characters can be displayed. The VDT uses the USA Standard Code for Information Interchange (USASCII) as shown in Table 1-1.

Inquiries and transactions are composed on the keyboard, verified on the display screen, and if necessary corrected before transmission to the processor. The response from the processor overwrites the inquiry, or if desired it may be displayed along with the inquiry or with format headings. If a teletypewriter is attached, the displayed message may be printed out as hard copy. Data may be entered, changed, erased, inserted, or shifted at the keyboard. A moving cursor (displayed as an underline) gives a continuous indication to the operator of the position in which the next character will be entered or received, or from which the character will be transmitted.

## Data Entry

The operator enters data up to 20 characters per second by using the Control Panel, which contains the keyboard and control switches. The operator can select 64 different alphanumerics to generate a 20 line message, each line consisting of 54 characters for a total character count per page of 1080 characters. The composed message is displayed on the viewer screen, enabling the operator to edit the message before transmission to the Basic Processing Unit (BPU).

## Character Generation

The characters displayed are generated from the keyboard, stored in display memory, and by means of a character generator that converts the digital code to analog voltages generate character video at the monoscope tube. The character video is applied to the viewer CRT. The CRT deflection system provides a vertical sweep rate of 1.67 microseconds or a full page of display, refreshed at a 60 Hz rate. The horizontal sweep rate of 1280 Hz gives a 20 line display array with 54 characters per line, or a total page count of 1080 characters. This coincides with the maximum storage capacity of the VDT Delay Line Memory (1080 characters plus 200 character times reserved for retrace time).

Table 1-1. ASCII Codes

| ASCII Code | Displayed Character | $\begin{aligned} & \text { ASCII } \\ & \text { Code } \end{aligned}$ | Displayed Character |
| :---: | :---: | :---: | :---: |
| $\mathrm{b}^{7} \quad \mathrm{~b}^{1}$ |  |  |  |
| 0100000 | . (space) | 1000101 | E |
| 0100001 | $\div$ (divide) | 1000110 | F |
| 0100010 | " | 1000111 | G |
| 0100011 | \# | 1001000 | H |
| 0100100 | \$ | 1001001 | I |
| 0100101 | \% | 1001010 | J |
| 0100110 | \& | 1001011 | K |
| 0100111 |  | 1001100 | L |
| 0101000 | ( | 1001101 | M |
| 0101001 | ) | 1001110 | N |
| 0101010 | * | 1001111 | O |
| 0101011 | + | 1010000 | P |
| 0101100 | , | 1010001 | Q |
| 0101101 | - | 1010010 | R |
| 0101110 | - (period) | 1010011 | S |
| 0101111 | 1 | 1010100 | T |
| 0110000 | 0 | 1010101 | U |
| 0110001 | 1 | 1010110 | V |
| 0110010 | 2 | 1010111 | W |
| 0110011 |  | 1011000 | X |
| 0110100 | 4 | 1011001 | Y |
| 0110101 | 5 | 1011010 | Z |
| 0110110 | 6 | 1011011 | [ |
| 0110111 | 7 | 1011100 | Not Displayed |
| 0111000 | 8 | 1011101 |  |
| 0111001 | 9 | 1011110 | $\times$ (multiply) |
| 0111010 | : | 0000000 | NUL (Not Displayed) |
| 0111011 | < | 0000010 | STX (Not Displayed) |
| 0111100 | < | 0000011 | 」(ETX) |
| 0111101 | $=$ | 0000100 | EOT (Not Displayed, used in Station Select) |
| 0111111 | $?$ | 0001101 | << (return) |
| 1000000 | A | 0001110 | SO (Not Displayed) |
| 1000001 | A | 0001111 | SI (Not Displayed) |
| 1000010 | B | 1100001 | Reserved for TSC |
| 1000011 | C | thru | (Feature 5707) Not |
| 1000100 | D | 1111010 | Displayed |

*NOTE: All characters are generated with even parity and checked for even parity.

The internal bit rate of the $70 / 752$ VDT is 768,000 bits per second or 76,800 characters per second. However, for external transmission, the bit rate is reduced to 1200 bits per second to match the processing speed of the Telephone Line Data Sets.

When the printer option is installed, the VDT operator may select messages or segments of messages to be printed out.

When the Data Format option is installed, the VDT operator may request a standard format from the computer which is displayed on the viewer screen at approximately one-half the intensity of the variable data entered by the operator.

## Editing of Composed Message

The message data may be changed, erased, or new data may be inserted in existing words or lines allowing any type of corrections to be made before the data is transmitted. A moveable mark (or cursor), displayed as an underscore, gives the operator a continous indication of the position in which the next character will be entered in the message format. The entire message is stored in the Delay Line Memory and is constantly refreshed on the viewer screen at a 60 Hz rate. When the entire message has been composed, the operator must enter an end-oftext symbol before the transmit mode will function.

## Messaqe Transmission

The message is transmitted at the option of the VDT operator, who may send the entire message or a selected segment of the message. The message is transmitted in ASCII Code to the central computer facility and the reply message is displayed on the VDT viewer screen and stored in the VDT Memory so it can be constantly refreshed on the screen until the operator initiates an erase operation.

### 1.3 CHARACTERISTICS

The operational and physical characteristics are shown in Table 1-2.

Table 1-2. Characteristics

| OPERATING CHARACTERISTICS |  |
| :--- | :--- |
| Power Requirements and Protection <br> Requirements | 115 volts $48-52 \mathrm{~Hz}$ or $58-62 \mathrm{~Hz}$ <br> at 15 amps |
| Receiving and Transmitting Bit Rate <br> (maximum) : | 1200 baud (bits per second) |
| Transmitted and Received Data Format: | 10 -bit serial; 1 start bit, <br> 8 data bits, and 1 stop bit |
| Processed Data Format: | 8 -bit parallel: 7 data bits and <br> 1 parity bit |
| Displayed Characters: |  |

Table 1-2. Characteristics (cont'd.)

| OPERATING CHARACTERISTICS - (Cont'd.) |  |
| :--- | :--- |
| Display Format: | 1080 characters in 20 lines <br> of 54 characters |
| Maximum Typing Speed: |  |
| Parity Errors: | 20 characters per second <br> Displayed as a white block <br> equivalent to one character <br> space in the wrong character <br> position |
| Logic Levels: |  |
| Transmitted and Received: | $1=-3 \mathrm{v}$ to $-25 \mathrm{v} ; 0=+3 \mathrm{v}$ to +25 v |
| Internally Processed: | $1=+4.5 \mathrm{v} ; 0=0 \mathrm{v}$ |


| CABLING LIMITATIONS |  |
| :---: | :---: |
| Control Panel to Viewer: | Standard length 1 foot, optional lengths available 5, 10, 15 , or 20 feet |
| Data-Phone Data Set to Viewer: | 50 feet |
| Viewer to 70/720 Buffer: | 50 feet |
| Viewer to Teletype <br> Model 198420 Data Coupler: | 50 feet |
| ENVIRONMENT | OPERATING STORAGE |
| Temperature | $45^{\circ}$ to $110^{\circ} \mathrm{F} \quad 50^{\circ}$ to $110^{\circ} \mathrm{F}$ |
| Humidity: | 20 to 65 percent 0 to 80 percent |

## KEYBOARD

Weight: 30 pounds
Height: 3.75 inches
Width: 16.9 inches
Depth: 7.75 inches

Table 1-2. Characteristics (cont'd.)

|  | VIEWER |
| :--- | :--- |
| Weight: 100 pounds |  |
| Height: 14.5 inches |  |
| Width: 16.9 inches |  |
| Depth: 20.5 inches |  |

## DATA-PHONE DATA SET OPTIONS

```
1. Line classification of }1200\mathrm{ baud (bits/second)
2. Voltage interface
3. Two wire input/output line
*4. Amplitude and/or delay equalization
*5. Squelch and/or demodulation
*6. 600 ohm or 900 ohm line termination
*7. 0 db, -3 db, -6 db, or -9 db data transmit levels
```

NOTE: Those options marked with an * are installed at the decision of the telephone company installation technician.
8. The CY control lead is not used to reverse communications.

### 1.4 MAJOR ASSEMBLIES AND SUBASSEMBLIES (Refer To Figure 1-2.)

The 70/752 Video Data Terminal consists of two major assemblies, the Control Panel Assembly and the Viewer Assembly.

### 1.4.1 CONTROL PANEL

The Control Panel consists of the Keyboard and the Matrix Switch Assembly and contains all the VDT operator controls used to compose, edit, and transmit a message to the central computer facility.


Figure 1-2. Major Assemblies

## Matrix Switch Controls

The Matrix Switch Assembly consists of a series of indicator-type switches that the VDT operator uses to select the mode of operation, and to activate the Standard Features, such as Data Insert and Message Segment Address, and control the mark. When Special Features, such as Print and Format Data are installed, the optional control switches are also installed on the Matrix Switch Assembly. Other matrix switches permit the operator to erase either a character, line, or the full viewer screen. The POWER switch for the 115 volt 60 cycle input to the VIT power supplies is also located at the top of the Matrix Switch Assembly.

## Keyboard

The Keyboard is a modified electric typewriter 4-row keyboard. The keys, when pressed, control a series of coding microswitches which produce the standard ASCII digital code for each character. The digital code output enters the Viewer through a short cable, which may be replaced with a longer cable when the Keyboard is installed at a different location than the Viewer.

### 1.4.2 VIEWER

The Viewer Assembly is housed in a cabinet which may be adjacent to the Control Panel Assembly or, when the keyboard extension is used, the Viewer may be mounted up to 20 feet away from the Control Panel Assembly.

The Viewer contains the Logic Nest, consisting of printed circuit cards A1 through A6, the Delay Line Memory A7, the Character Generation section which consists of the Selection Amplifier A8, the Character Generator Monoscope A10, the Video Pre-amplifier A10A1, and voltage divider A1OA2. Also contained in the Viewer are the Deflection Amplifier A9, the Video System which consists of the Video Amplifier A12, the 12-inch Display Tube, the Tickler Amplifier A11, and the Dynamic Focus Circuit Board A20. The High Voltage Power Supply A13, and the Low Voltage Power Supply A14, are also contained in the VDT cabinet (Table 1-3).

The Selection Amplifier A8 and the Deflection Amplifier A9, are mounted with all their adjustments available to the VDT operator inside a door located on the VDT front panel, to the left side of the display tube (operator's right). Access to the Logic Nest printed circuit cards (A1 through A6) is available by removing the Viewer Cabinet rear cover.

When the cabinet main cover is removed, all other subassemblies (except the monoscope box assembly) are accessable for trouble-shooting or replacement. The monoscope box components are accessable by removing the ends of the box and detaching the monoscope box from the Viewer Chassis.

## Logic Nest (A1 through A6)

The Logic Nest consists of a card cage located at the rear of the Viewer Cabinet which contains six, four-layer printed circuit cards. The six logic cards contain all the timing and logic control circuits for the entire Viewer Assembly. Each of the logic cards has an 80 pin connector and each card can mount up to 48 dual in-line integrated circuit packages plus a number of discrete components. Up to 30 test points to internal connections on the logic module are available.

Table 1-3. Assembly Locations

| UNIT | DRAWING NO. | TITLE |
| :---: | :---: | :---: |
| 70/752 | 2134548 | Installation Drawing-70/752 Video Data Terminal |
| 70/752 SYSTEM | 2165479 | Schematic-70/752 Video Data Terminal |
| A1 | 2144559 | Detailed Logic Diagram-I/O No. 1 Logic |
| A2 | 2144560 | Detailed Logic Diagram-I/O No. 2 Logic |
| A3 | 2144558 | Detailed Iogic Diagram-Register Logic |
| A4 | 2144557 | Detailed Logic Diagram-Mark Logic |
| A5 | 2144556 | Detailed Logic Diagram-Timing Logic |
| A6 | 2144509 | Schematic/Logic-Printer Terminator and Oscillator |
| A7 | 2039ACE23 | Schematic-Delay Line (Mfg. by L.F.E) |
|  | 5000-105S | Schematic-Delay Line (Mfg. by Digital Devices) |
|  | 2144547 | Schematic-Control Panel 70/752-10 |
| A8 | 2110687-501 | Selection Amplifier |
| A9 | 2110686-501 | Deflection Amplifier |
| A10 | 2110691-501 | Monoscope Assembly |
| A11 | 2110689-501 | Tickler Driver |
| A12 | 2110588-501 | Video Driver |
| A13 | 100423 | Schematic-High Voltage Power Supply (Mfg. by Astro Metrics) |
|  | KV-3214 | Schematic-High Voltage Power Supply (Mfg. by ITT, RCA HVPS Sub-assy.) |
| A14 | 2165472 | Schematic-Low Voltage Power Supply |
|  | 2110683-501 | Low Voltage Power Supply |
| A 20 | 2144178-501 | Dynamic Focus Board |
| A21 | 2165856-501 | Keyboard Filter |
| OPTION | 2144565 | Detailed Logic Diagram-Station Select (Replaces A2) |
| OPTION | 2144567 | Detailed Logic Diagram-Data Format (Replaces A4) |
| OPTION | 2144570 | Detailed Logic Diagram-Printer Adapter (Replaces A6) |
| OPTION | 2144570 | Detailed Logic Diagram - Flexible Character Array (Replace A5) |

Table 1-4 lists the name of each printed circuit card in the logic Nest and gives a brief description of the logic function performed by each card.

Table 1-4. PC Unit Functions

| UNIT | FUNCTION |
| :---: | :--- |
| Printer Terminator and Master <br> Oscillator, A6 | Contains the 6.144 MHz Crystal <br> Oscillator that controls logic <br> timing generating the Master <br> Clock frequency of 3.072 MHz. |
| Timing Card, A5 | Contains several timing circuits <br> that divide down the 3.072 MHz <br> Master Clock frequency to generate <br> all the timing pulses used in <br> the VDT. |
| Register Card, A3 Mark Logic Board, A4 | Contains all logic controlling <br> the movement of the Mark and <br> controls the Data Insert function. |
| Input/Output cards, A1 and A2 | Contains the Delay Line Register, <br> the Display Register, and assoc- <br> iated control logic. |
| These two cards contain three <br> Buffer Registers and the assoc- <br> iated control logic for all <br> remote transmission and reception <br> operations. |  |

## Delay Line Memory, A7

The Delay Line Memory is mounted at the left side of the Viewer Chassis by a hinge which permits access to the Selection Amplifier (A8) and the Deflection Amplifier (A9). The Delay Line is mounted in a box approximately one-inch thick, 13 inches wide and 16 inches long. Detailed data on the Delay Line is given in Section Three of this manual.

## Character Generator

The Character Generator Section consists of the Selection Amplifier (A8), the Monoscope Tube (A10), the Voltage Divider (A10A2), and the Video Preamplifier (A1OA1). The selection amplifier adjustments are available to the VDT operator on the Viewer front panel. The monoscope (A10) and its subassemblies (A1OA1 and A1OA2) are all mounted in a box which provides shielding from magnetic fields.

## Video Section, A11, 12, and 20

The Video Section consists of the Video Driver (A12), the Tickler Driver (A11), and the Dynamic Focus Card (A20). The Video Driver is mounted to the CRT Yoke and the tube neck shield. The Tickler Driver circuit board is mounted on the sloping back of the CRT shield. The Dynamic Focus board is mounted inside of the CRT neck shield at the rear of the viewer chassis.

## Deflection Section, A9

Both the Horizontal and Vertical Deflection amplifiers are contained on the Deflection amplifier card A9 which is mounted beside the Character Selection amplifier card A8. All adjustments are accessable on the viewer front panel. The Deflection Amplifier has large heat sinks to disapate the heat from the Deflection Amplifier output stages.

Low Voltage Power Supply, A14
The Low Voltage Power Supply (A14), is mounted to the Viewer Chassis at the upper right front corner (as viewed from the rear). The power supply adjustments are accessable by opening a hinged door located on the outside Viewer case. The adjustments are mounted on a printed circuit regulator board which is plugged into the connector on the door. The power supply outputs connect to the viewer cabling at a terminal board.

## High Voltage Power Supply, A13

The High Voltage Power Supply is mounted on the bottom of the viewer chassis at the right front corner (as viewed from the rear). The unit is approximately four-inches long.

### 1.5 MODES OF OPERATION

The 70/752 VDT has three modes of operation: Write, Transmit, and Receive. The normal mode sequence in operations is to Write, Transmit, Receive, and then return to Write mode.

### 1.5.1 WRITE MODE

The Write Mode is entered by three means:

1. Upon completion of the power-on procedure.
2. By the operator pressing the WRITE switch on the operator's control panel.
3. By the normal cycling of the VDT through the Transmit/Receive cycle and automatically returning to the Write mode.

When the VDT is in the Write mode, the operator has complete control of the unit. By using the keyboard and the control panel switches, the VDT operator can compose a message (which will appear on the viewer screen), make corrections to the message by either erasing old data, replacing characters, or inserting missing characters.

By use of the proper control switch, the operator can erase individual characters, a complete line, or the entire screen. All editing of the message can be accomplished by the operator and the message proofed prior to transmission of the message to the central computer facility.

The moveable mark (or cursor) is positioned on the Viewer Screen by the operator to indicate the position in which the next character will be entered or deleted from the message.

The ADVANCE control steps the mark to the right until the end of the line is reached, then to the beginning of the next line of the raster. The RETURN control moves the mark to the beginning of the next line. The BACKSPACE control moves the mark within one line only and will not move the mark back the preceeding line.

### 1.5.2 TRANSMIT MODE

Pressing the Transmit switch disables all local controls and enables the circuitry to the Data Set unit, which converts the VDT output to FM signals for phone-line transmission to the central computers Data Set unit. Initiation of the Transmit mode requires that an End-of-Text (ETX) character ( $ل$ ) has been entered at the end of the composed message. After the transmission of last message character (ETX), the VDT senses the End-of-Text character and automatically places the VDT in the Receive mode. The transmitted message remains on the Viewer Screen unless the operator manually returns the VDT to the Write mode by pressing the Write switch.

## Note

Manual intervention immediately after transmission may interrupt a returning message from the central computer.

When the original message must be changed after it has been transmitted, the operator can place the VDT in the Write mode, make the necessary corrections, return to the Transmit mode, and retransmit the corrected message to the central computer complex.

### 1.5.3 RECEIVE MODE

The Receive mode is inhibited until the VDT has transmitted a message to the central computer. Then the VDT automatically enters the Receive mode. During normal reception, the incoming message characters replace the existing message characters on the Viewer Screen, one at a time, until the incoming message is complete. The remainder of the Viewer Screen is then automatically erased, leaving only the received message from the central computer. When the original VDT message is transmitted using the Message Segment Address (MSA) feature, the original message will remain on the Viewer Screen and the computer's response will be displayed immediately following the ETX character of the original message. This allows the VDT operator to observe the original querry and the computer response simultaneously.

### 1.6 CONTROLS AND INDICATORS

The controls and indicators available to the VDT operator at the operator's position are shown in Figure 1-3. Figure 1-4 shows adjustments for maintenance personnel, which are located on the electrical adjustment panel located on the Viewer Front Panel on the left side of the Viewer Screen (operator's right).

Table 1-5 lists the keyboard keys and the matrix control switches located on the Control Panel Assembly. The control designator, front panel title, and the function of each control are listed in the tables. Table 1-6 lists the maintenance controls.

### 1.7 FEATURES

The features available on the $70 / 752$ VDT may be grouped into two classifications, Standard and Special. The Standard Features are those that are normally supplied with the unit. The Special Features are available as options that the user may select to satisfy a special need.

### 1.7.1 STANDARD FEATURES

## Data Insert

Data Insert is a Standard Feature of the $70 / 752$ VDT that permits the operator to insert additional characters into the displayed message. The VDT must be in the Write mode and the operator must press the DATA INSERT switch to enable the insert logic. Pressing the DATA INSERT switch again, extinguishes the switch indicator lamp and places the VDT in the normal Write mode.

When the DATA INSERT switch is activated (light on), a character entered from the keyboard will be entered at the mark (cursor) position and all subsequent characters, including the character previously over the mark, will be shifted one character later in the Delay Line Memory. This moves all the characters following the newly inserted character one space to the right on the Display. Characters at the end of a line are advanced to the beginning of the next line, except RETURN and ETX characters. These two characters, if needed, must be reinserted at the desired position in the message after the Data Insert operation is completed. When an affected memory location contains a NUL character, the NUL or blank space is over-written by characters being entered (or shifted). Characters at the end of the last line of the displayed page are dropped from the VDT memory.

## Nofe

When the VDT is provided with the Data Format Special Feature 5710, the Data Insert Feature is not available.


Figure 1-3. Controls and Indicators

## Message Seqment Address (MSA)

The Message Segment Address (MSA) feature is controlled by the MSA switch, located on the Control Panel. The operator must press (to light) the MSA switch to enable the MSA logic.

The Message Segment Address feature permits the VDT operator to display both the originally composed message, which is transmitted to the central computer, and the computer's response to the message. The MSA feature also allows the VDT operator to transmit a segment of the composed message by entering an ETX character at the end of that segment which is to be transmitted and then positioning the cursor at the beginning of the segment to be transmitted.


Figure 1-4. Maintenance Controls

Table 1-5. Controls and Indicators

| CONTROL PANEL MATRIX SWITCHES |  |  |
| :---: | :---: | :---: |
| CONTROL DESIGNATOR | TITLE | FUNCTION |
| A 2 S 1 | POWER | Applies and removes all power to the |
| A 2 S 4 | WRITE | Positions the cursor to beginning of frame, permits data to be entered and displayed, and is lighted in the Write mode. When the Data Format Feature is used, the cursor will be moved to the first position available for data entry. When the MSA feature is enabled, the cursor is not moved. |
| A 2 S 3 | PRINT | Causes the displayed message to be reproduced at the printer, is lighted during printing operation, and is enabled only in the Write mode. |
| A2S 2 | XMT | Causes the displayed message to be transmitted, is lighted in the Transmit mode, and is enabled only in the Write mode. |
| A 2 S 7 | DATA INSERT | Permits insertion of a new character or characters, causes all characters at and to the right of the cursor to be shifted one position to the right with each new character entry, and is lighted when the data insert operation is enabled. |
| A 2 S 5 | MSA | Causes transmit and print operations to begin at the cursor location and end at the location of the " ل", and is lighted when the MSA feature is enabled. |
| A2S6 | FORMAT DATA | Erases characters in variable data display fields when enabled by the master erase key. |
| A2S10 | CHAR | Erases the character in the position indicated by the cursor when enabled by the master erase key. |
| A2S9 | L INE | Erases all characters in the line at and to the right of the position indicated by the cursor and moves the cursor to the beginning of the next line when enabled by the master erase key. When using the data format, only variable data is erased. |

Table 1-5. Controls and Indicators (Cont'd.)

| CONTROL PANEL MATRIX SWITCHES - (CONT'D.) |  |  |
| :---: | :---: | :---: |
| CONTROL DESIGNATOR | TITLE | FUNCTION |
| A2S8 | SCREEN | Erases the entire displayed message and returns the cursor to beginning of the page when enabled by the master erase key. |
| A2S13 | (Backspace) | Moves cursor one position to left. If held down, this will repeat at about ten times per second, five times per second if the Data Format Feature 5710 is provided. |
| A2S12 | (Advance) | Moves cursor one position to right. If held down, this will repeat at about ten times per second, five times per second if the Data Format Feature 5710 is provided. |
| A2S11 | (Return) | Repositions cursor to first character of next line. This control must be pressed each time it is desired that the cursor move to the next line. |



Table 1-5. Controls and Indicators (Cont'd.)

| KEYBOARD KEYS - (Cont'd.) |  |  |
| :--- | :--- | :--- |
| CONTROL <br> DESIGNATOR | TITLE | FUNCTION |
|  | Space Bar |  |
| Standard. <br> Character <br> Keys | Inserts small dot and one-character space <br> into the displayed message for the space <br> between words. <br> Produce the characters of the displayed <br> message. |  |


| OPERATOR'S ADJUSTMENT PANEL CONTROLS AND INDICATORS |  |  |
| :---: | :---: | :---: |
| R73 | P ICTURE | Corrects double-image display of characters. |
| R72 | BRIGHTNESS | Controls the intensity of displayed message. |
| R74 | FOCUS | Controls the sharpness of displayed message. |
| CB1 | Circuit <br> Breaker | Provides circuit breaker control for <br> line input power. (Located on rear panel.) |

Table 1-6. Maintenance Controls

| HORIZONTAL SELECTION AMPLIFIER |  |  |
| :--- | :--- | :--- |
| R57 | HORIZ SCAN | Controls the amplitude of the horizontal <br> sweep ramp that is applied to the hori- <br> zontal selection amplifier to scan the <br> character stencil in the monoscope tube. |
| R73 | HORIZ CENT | Controls the monoscope horizontal centering <br> at the leading edge of the selected char- <br> acter cut-out. |
| HORIZ GAIN | Controls the gain of operational amplifier <br> Zo2 in the horizontal selection amplifier. |  |
| HORIZ SKEW | Controls the amount of cross talk current <br> applied to the monoscope horizontal de- <br> flection plates to correct physical skEW <br> in the monoscope tube deflection plates. |  |

Table 1-6. Maintenance Controls (Cont'd.)

| VERTICAL SELECTION AMPLIFIER |  |  |
| :---: | :---: | :---: |
| CONTROL DESIGNATOR | TITLE | FUNCTION |
| R14 | VERT GAIN | Controls the gain of operational amplifier ZO1 in the vertical selection amplifier. |
| R15 | VERT CENT | Controls the monoscope vertical centering. |
| R22 | VERT SKEW | Controls the amount of cross talk current applied to the monoscope vertical deflection. |
| R43 | VERT SCAN | Controls the amplitude of the tickler scan on the monoscope character stencil. |
| R102 | ASTIG. | Applies 0 to +75 vdc to XVI-9 astigmatism grid of monoscope tube. |


| DEFLECTION AMPLIFIER |  |  |
| :--- | :--- | :--- |
| R56 | VERT CENT | Controls the viewer display tube vertical <br> centering. |
| R38 | HORIZ CENT | Controls horizontal centering of viewer <br> display tube. |
| R4 | HERT GAIN | Controls gain of vertical sweep to <br> viewer CRT deflection yoke. |
| Controls gain of horizontal sweep to |  |  |
| viewer CRT deflection yoke. |  |  |

When the message has been transmitted, the mark will remain at the ETX character of the message segment transmitted and the central computer response will be displayed immediately following ETX, leaving the original message in place rather than replacing the original message. When the Printer Adapter Special Feature 5711 is provided with the VDT, the printed message will be only the message segment enclosed by the mark and the ETX character. All NUL characters are converted by the print feature to spaces for $T$ eletypewriter readout.

### 1.7.2 SPECIAL FEATURES

## Keyboard Extension, Special Feature 5713

The Keyboard Extension Feature is a cable, up to 20 feet in length, which connects the Control Panel to the Viewer Assembly. The use of the extension option permits the Viewer to be installed in alternate positions for maximum shielding or shelf installation of the Viewer Assembly.

## Data Format, Special Feature 5710

When the VDT operator desires to use the Data Format Feature, he must type a coded message to request a Standard Message Format from the central computer.

The Standard Message Format, which is a partial message consisting of columns and headings, will appear on the viewer screen at approximately one-half the intensity of the normal message characters. The VDT operator can then enter variable data in the format blanks. The logic is so arranged to modify the mark (or cursor) operation so that the mark cannot appear under any format character; therefore, the operator cannot modify the format except to completely erase the entire viewer screen. When DATA FORMAT has been selected, the write control logic will position the mark under the first available character position within the first variable data field. When one line of the format variable data has been entered, the return control logic will cause the mark to move to the first available position on the next line.

Variable data may be entered in any or all of the variable data fields and then transmitted to the central computer. Variable data entries may be erased by pressing the DATA FORMAT switch, located on the Control Panel. Only the variable data will be erased, leaving the Standard Data Format on the viewer screen. The LINE erase switch, when pressed, will also erase only the variable data leaving the format. The SCREEN erase switch when pressed, erases the entire screen of all variable data and the format.

## Note

When the Data Format Special Feature is installed in the VDT by installation of the alternate mark logic board A4, the Data Insert Standard Feature is removed due to changes in the logic. The speed of the repetitive mark operation is modified to repeat at five times per second rather than the normal ten times per second.

## Printer Adapter, Special Feature 5711

The Printer Adapter Special Feature allows connection of a Model 33 or 35 Teletype to the VDT which enables the VDT operator to retain a hard copy of all messages displayed, transmitted, or received on the VDT viewer screen. The printer adapter may be enabled only when the VDT is in the Write mode. Pressing the PRINT switch, located on the Control Panel will cause the Write mode switch indicator to extinguish and will light the PRINT switch indicator. The message will be printed on the Teletype at the rate of 10 characters per second following the same 20 line presentation of the viewer screen. The VDT automatically sends a Carriage Return and Line Feed to the teletype at the end of each line. All NUL characters (all zeros) stored in the VDT memory are converted by the Print feature and sent to the teletype as spaces. An ETX terminates the print operation and the VDT Print indicator is extinguished and the Write indicator is lit, returning the VDT to the Write mode.

When the MSA switch is pressed and the Print function is activated, the Print operation begins at the mark location and the selected message segment is printed, terminating the ETX character. When the Data Format option has been used in composing the message, the format data will also be printed.

When the printer adapter feature is installed, the teletype (Model 33 or 35) must be connected to the VDT with a Data Coupler (198420). The teletypewriter is connected to the VDT by a cable that is furnished with the print feature. When the print feature is installed, the printer oscillator card A6 is replaced by the alternate A6 card.

## Station Select, Special Feature 5707

The Station Select Special Feature provides a means of using one multistation communication line to link several VDT's (up to 26 ) to a common central computer. This requires a separate Data Set for each VDT as well as a Data Set at the $70 / 720$ Buffer, located at the central computer facility. The System is controlled by the central computer by use of a "Polling" sequence. Each station Data Set is assigned a different Transmit Start Code (TSC); additional logic decoded by a recognition diode matrix in each station Data Set allows the Data Set to respond to the "polling" with a "no traffic" (EOT) signal when no message is ready to transmit (in the Transmit mode), the polling sequence is interrupted and the central computer accepts the stations message, sends a response to the station, and continues the polling sequence.

The maximum number of VDT's that can be installed on one communication line, using the Station Select Feature, is 26. Due to practical limitations, however, at installations with heavy traffic loads the number of VDT's sharing one communication line may be held to a maximum of five to prevent the operators from having to wait more than one and one-half minutes before receiving a reply from the central computer. When the Station Select Feature is installed the I/O card A2 is replaced by the alternate A2 card.

## Video Data Switch (70/755)

The Video Data Switch (VDS) serves a function similar to that of the Station Select Special Feature in that it permits a maximum of eight VDT's to be connected to one point-to-point private line telephone circuit. The Video Data Switch differs from the Station Select Special Feature in that it permits a maximum of eight VDT's to be connected to one point-to-point private line telephone
circuit. The Video Data Switch differs from the Station Select Special Feature in that only one Data Set is needed for the VDS; the Station Select needs one Data Set for each VDT connected to the line.

The VDS cabinet is approximately the size of the VDT unit and may be mounted on a table or other convenient.support. When remote data transmission is not required, the VDS is connected by cable directly to the BPU Buffer eliminating the two Data Sets used on the phone line for remote transmission.

The VDS services each VDT in an established sequence. When a VDT is in the Transmit mode and there is a message ready to transmit, the VDS establishes a connection to the central computer, or processor, and transmits the message. The processor prepares and transmits a response back through the VDS to the VDT. The VDS then continues the scanning sequence of the remaining VDT's.

The processor must issue a new READ command within 45 milliseconds of the termination of its response to each VDT to ensure reception of the next VDT's inquiry.

VDS Delay Timer
The VDS is equipped with a timer to limit the time allotted for the BPU to reply to a VDT message. The timer may be manually set to provide either a 15 or 30 second delay interval, or can be disabled. When used the timer is started upon completion of a VDT transmission to the processor and is reset by the processor's response to the VDT. When the response delay exceeds the selected time interval, the timer expires, the VDT is disconnected, the VDS scan advances to the next VDT , and the timer is reset.

## Flexible Character Array, Special Feature 5734-01

The Flexible Character Array Special Feature provides a means of changing the Viewer display format from a standard array of 20 lines of 54 characters each, to several alternate arrays. The recommended configuration is a 14 line raster of 81 characters per line. The changes in Viewer array are accomplished by means of jumpers that change the sweep timing. Changing the array requires realignment of the viewer.

## Data Set Cable, Special Feature 5766

The Data Set Cable Special Feature is intended for use on installations where electrical noise radiation originating from other equipment is nearby.

Special Feature 5766 incorporates a twisted pair cable to minimize noise pickup and is available by MI 2100383 with dash numbers designating available lengths (e.g. -5, -25, -50, -100). The Cable Assembly Drawing Number and Installation Drawing Number are 2166844-501 and 2134548, respectively.

# SECTION TWO <br> INSTALLATION 

## GENERAL

Refer to the Systems Installation Manual (70-01-SIM) for installation procedures for the Model 70/752 Video Data Terminal.

## SECTION THREE

## THEORY

### 3.1 GENERAL

The Video Data Terminal (VDT) functions as an information interchange unit between the operator and a central computer. The central computer may be located at the same location as the VDT or, the computer can be at a remote facility and data can be transmitted over telephone lines by using two Model 202 C/D Data Set units manufactured by Bell (or equivalent). The Data Sets convert the serial ASCII code (American Standard Code for Information Interchange) data to FM signals for transmission over telephone lines.

The VDT contains a Delay Line Memory which has a capacity of 12,800 bits (1080 characters at 10 bits per character plus 200 character spaces for flyback time). The characters are processed internally at a rate of 768,000 bits per second. External transmission and reception rate is at 1200 bits per second (baud). The operator input rate can be up to 20 characters per second.

### 3.2 INTERFACE

### 3.2.1 LOCAL CONNECTION

When the VDT is connected to a computer at the same location, the VDT output is connected directly into the 70/720 Buffer at the 70/668 Communications Controller, and no Data Set units are needed. Some rewiring is necessary for local operation. Refer to the Installation manual for details.

### 3.2.2 REMOTE CONNECTION

When the VDT is connected to a remote computer facility, the VDT output data must be converted from d.c. logic levels to equivalent FM signals for transmission via telephone communication lines. This requires a Model 202C or 202D Data Set (furnished by American Telephone and Telegraph Bell System) at each end of the telephone line. The Data Set at the central computer facility is then connected to the processor via the Communications Controller.

### 3.3 FUNCTIONAL DESCRIPTION (Refer To Figure 3-ו.)

The VDT operator manually composes a message on the Keyboard, and when necessary can correct the message before it is transmitted to the central computer facility. When the message is ready, the operator can transmit the message to the central computer. The central computer processes the incoming message and then sends a response message which is displayed on the Viewer screen.


Figure 3-1. VDT Simplified Block Diagram

### 3.3.1 KEYBOARD ENTRY

Data is entered from the Keyboard in the form of a seven bit ASCII digital code. The code for each selected character is applied to the Display Register entry logic. The Display Register (DR) is enabled after each character has been selected to allow a parallel transfer from the Keyboard microswitches into the DR. The DR output is then serially shifted through the Delay Line Memory. From Memory, the data is shifted into the Delay Line Register. The Delay Line Register then parallel transfers the character bits into the Display Register. The Display Register applies the character bits to the Selection Amplifier. The Selection Amplifier converts the digital code to gross positioning voltages for the monoscope tube. The monoscope generates character video which is displayed on the Viewer display tube.

### 3.3.2 MESSAGE TRANSMISSION

Message transmission is initiated by an automatically generated Start-of-Text (STX) character. The STX character indicates to the Central Processor the start of a new message. Following the STX character, each VDT message character is transmitted serially beginning with the lowest order bit ( $b_{1}$ ). Refer to the external character format in Figure 3-2. When all of the message characters have been transmitted, the ETX (End-of-Text), 」, character is transmitted. This notifies the processor that the message is complete and that the VDT is awaiting the processor's answer.


CHARACTER FORMAT IN DELAY LINE MEMORY


CHARACTER FORMAT FOR TRANSMIT AND RECEIVE OPERATIONS

Figure 3-2. Character Format

The central computer's Data Set reconverts the FM signals from the VDT Data Set to d.c. logic levels and applies the message characters to the 70/720 Asynchronous Data Set Buffer. The 70/720 Buffer then transfers the characters to the central computer via the $70 / 668$ Multichannel Communications Controller.

### 3.3.3 MESSAGE RECEPTION

When the BPU has processed the message, it begins its response with an STX character, transmits the response message, and ends the message with an ETX character. The ETX character notifies the VDT that the response is complete. The VDT then automatically returns to the Write mode.

### 3.3.4 VDT SYNCHRONIZATION

To keep the Delay Line Memory and the system timing in synchronization, two sync bits are generated at the start of each page ( 60 times per second). The Master Clock is stopped and a new count is started at the beginning of each page. This eliminates any problem that might be encountered due to the Delay Line length varying with temperature.

WAIT, START and HOLD Flip-Flops
The WAIT, START, and HOLD flip-flops control the timing synchronization;

1. For the initial power up sequence.
2. For timing resync each page time ( 60 Hz or once each 16.7 milliseconds).
3. To generate new sync pulses after a Screen Erase and Master Clear operation.

## Sync Pulse Generation (Refer to Figure 3-3.)

Note that the Line Counter advances during character count 55. Therefore, all functions occurring during horizontal and vertical flyback times are considered as being at the beginning of the following line. That is, timing resync occurs during L1, which starts at character count 56 at the end of the last line.


Figure 3-3. Sync Pulse Generation and Timing

At the end of the last line of each page during retrace time, the WAIT, START, HOLD flip-flops stop the Character and Bit Counters, hold the Master Clock, and generate two new sync pulses. Note that the Line Counter was advanced to L1 by character count 55 after the last displayed line of the page. The WAIT flip-flop is set at character count 59 after last line. When the WAIT flip-flop is set, CHARACTER COUNTER TRIGGER (CHCT) is inhibited, holding the Character Counter at count 59.

The START flip-flop is then set by the next " 1 " bit from the Delay Line. This "1" bit represents the first sync bit. The HOLD flip-flop is then set during BTIA and disables the output of the 3.072 MHz Master Clock. The counters now are locked at count 59, L1, Bit Time BT1A•BT1B (the second 651 nanoseconds of BT1A).

The WAIT flip-flop is then reset. The HOLD flip-flop remains set for up to 14.3 microseconds, then is reset by the second sync pulse from the Delay Line which starts the timing sequence by releasing the Master Clock and the Bit, Character, and Line Counters. From the leading edge of the second sync bit to the start of character 1 of line 1 is a dead time of 70 microseconds (Figure 3-4) to complete the flyback time.


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Figure 3-4. Sync Pulses and Video

The START flip-flop does not reset until character count 63 (IOBP) which is after the timing resync sequence is completed.

## Sync Pulse Generation During the Power Up Sequence

During the power up sequence, it is necessary to generate the two sync pulses since the Delay Line Memory will not retain any information during power off periods. During the power up sequence, relay $K 1$, located at the rear of the VDT, is deenergized until the operator presses the WRITE switch. When relay K1 is deenergized, pin 8 of the relay is connected to ground. This generates SCREEN ERASE AND MASTER CLEAR (SEMC). SEMC resets the HOLD and WAIT flip-flops and sets the START flip-flop.

Since the HOLD and WAIT flip-flops are reset by SEMC, the Bit, Character, and Line Counters are running. When the counters reach L1, character count 59, Bit Time BT1B, the Start Up Bit gate ( $56 \mathrm{~B} 5 \mathrm{~A}-\mathrm{B}$ ) generates START UP BIT (SUB). SUB sets the Delay Line Stretch (DLS) flip-flop (Gate 58C1B) of the DLR input


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Figure 3-5. Master Oscillator, Block Diagram
circuit (Dwg. 2144558 Sheet 2). The DLS flip-flop sets the DLRIN flip-flop which enters a "1" bit into the Delay Line Register (Figure 3-3).

The DLRIN flip-flop output also is applied to AND gate 68B1A. START is ANDED with the 1 output of DLRIN to activate the BREAKOUT GATE (BOG). The BOG signal is applied directly to the Delay Line Memory input as the first sync pulse. At the same time, the same "1" bit from DLRIN is shifting through the DLR to generate the second sync pulse 14.3 microseconds later. The result will be two sync pulses in the Delay Line spaced 14.3 microseconds apart.

When the VDT is in the Write mode and the operator presses the SCREEN ERASE with MASTER ERASE held down, the SEMC signal will cause all the data stored in the Delay Line Memory to be erased, including the two sync pulses. The sync pulse generation cycle is then automatically repeated to generate two new sync pulses for the Delay Line.

### 3.4 LOGIC DESCRIPTION (Refer to Figures 3-5 and 3-6.)

The VDT logic circuits (Figure 3-6) are on the six printed circuit boards (Al through A6) in the Logic Nets. Each board has a specific set of logic functions controlling a specific portion of the VDT. Table $3-1$ lists the main mnemonics gen-
erated in the VDT logic. The following detailed logic description follows the order of generation of timing signals from the 6.144 MHz crystal through the countdown circuits to the 60 Hz output used for vertical resync. This includes the generation of the master clock frequency, the timing clocks used to shift the registers, the tickler frequency used in character generation and presentation, the Bit Counter, Character Counter, Line Counter, the 19.2 KHz Drive Enable, the Horizontal and Vertical Sync pulses, the mode control logic, the mark control logic and transmit/receive logic.

### 3.4.1 PRINTER TERMINATOR AND OSCILLATOR, A6 (Refer To Dwg. 2144509.)

The master oscillator card (Figure 3-5) contains a 6.144 MHz crystal controlled oscillator, an amplifier with an output clipper network, a differential switch, an emitter follower with an output clamp, spike suppression logic, and a triggered flip-flop.


The function of the oscillator circuit is to produce a Master Clock frequency that is used to generate all the other timing pulses in the VDT logic. The sinusoidal output of the colpits oscillator is amplified, clipped, and applied to a differential amplifier to produce a 6.144 MHz square wave. The clamped output of the emitter follower triggers the Master Oscillator flip-flop $Z 01$ thru the spike suppression logic.

## Note

The Printer Terminator and Oscillator Adapter P/C board is replaced when the Printer Special Feature is installed by a Printer Adapter P/C board, No. 2144570.

## Spike Suppression Loqic

The spike suppression circuit consists of flip-flop Z03 and gate Z02. The function of the circuit is to prevent the oscillator emitter follower output from setting the master oscillator flip-flop during resync time. During the timing resync sequence, the HOLD-OP signal is applied to both the $Z 01$ and $Z 03$ flip-flops to stop the master clock. When the HOLD signal terminates, the oscillator again is able to set the master oscillator flip-flop (zO1) and the 3.072 MHz clock frequency is again applied to the Timing card A5.

### 3.4.2 TIMING LOGIC, A5 (Refer To Dwg. 2144556 Sheet 1.)

The Timing Logic card receives the 3.072 MHz Master Clock frequency from the A6 card and generates all the countdown pulses required for the logic timing of the VDT.

## Timing Requirements

The VDT timing requires the following frequencies generated on card A5:

1. 1.536 MHz used to generate the tickler frequency.
2. 768 KHz used to generate the TBA and TBB timing clocks.
3. 76.8 Khz character count (10 bits per character).
4. 19.2 KHz used for $\mathrm{H} . \mathrm{V}$. DRIVE ENABLE.
5. 1200 Hz used for line time (Horizontal Sync).
6. 60 Hz used for page time (Vertical Resync).

In addition to the basic frequencies required, the Timing logic card generates the START, WAIT, and HOLD signals. With the standard timing board, this timing sequence controls presentation of 1080 characters presented on a 20 line raster with 54 characters per line displayed. An additional 10 character-times per line are required for flyback time during horizontal retrace between lines. This makes the total time per line 833 microseconds. Each character bit requires 1.302 microseconds. Each character (10 bits) requires 13.02 microseconds.

Each line of 54 characters requires 703 microseconds. The total viewer screen page is refreshed at a 60 Hz rate to prevent flicker due to the short image persistance time of the viewer display tube.

## Functional Parts of A5 (Refer to Figure 3-5.)

The Timing Logic card contains the following functional parts: two frequency dividers, a TIPS flip-flop, a two-phase pulse former, a Bit Counter, a Character Counter, a Line Counter, and the asynchronous delay line control timing. The resulting outputs are the two clocks, TBA and TBB, A and B bit times, character counts at character times $1,2,55,58$, and 63 , and line counts used in establishing horizontal and vertical sync.

Tickler Frequency Generation (Refer to Dwg. 2144556.)
The input Master Clock frequency to A5 (from A6) is applied to Frequency Divider flip-flop 56C8B. This flip-flop divides the 3.072 Master Clock frequency to 1.536 MHz for use as the Tickler frequency. Both outputs of the Frequency Divider flip-flop are applied to separate AND circuits, which also receive the two outputs of the TIPS flip-flop, 56C8A. The TIPS flip-flop is triggered by the VERTICAL SYNC signal (VSYNC-N). VSYNC occurs at the end of each page scan of the Viewer tube. The AND circuits are arranged so that the OR circuit 56B8A output to the Tickler Driver will apply opposite phases of the Tickler frequency on alternate screen scans. This produces a better character presentation on the screen by double scanning the Monoscope stencil to completely cover the character cutout.

## Two Phase Pulse Former (Refer to Figure 3-7.)

The function of the two-phase pulse former is to generate two timing clocks, TBA and TBB, which provide the basic timing for the VDT timing. The two-phase pulse former consists of five transistors and a 100 nanosecond delay line. The circuit input is a 768 KHz square wave from the Frequency Divider flip-flop, 56C7A, through two amplifiers 56D6A and 56D5A.

## TBA and TBB Generation (Refer to Figure 3-7.)

The positive $(+4.5 v)$ half cycle of the square wave causes input transistor Q3 to invert the input and Q2 applies a ground level to one end of the circuit's 100 nanosecond delay line. At the same time, Q1 is turned off. The positive change in Q1 collector level applies an input signal to the ungrounded end of the delay line. The delay line reflection 200 nanoseconds later causes the collector of Q1 to drop to zero. During the 200 nanosecond period that the collector of Q1 is positive, output transistor Q4 is turned on. The 200 nanosecond timing clock (TBA) is generated and amplified by 56D6B and applied to amplifier 56C6A. The output of 56C6A (TBA) is available at TP7 and is routed to several other logic circuits.

When the 768 KHz input square wave goes negative, transistor Q1 conducts to ground one end of the delay line.

$\tau T-\varepsilon$

## Note

The opposite end of the delay line is now grounded compared to the TBA generation half cycle.

At the same time, transistor $Q 2$ is turned off, and the rising level of the $Q 2$ collector applies a signal to the ungrounded end of the delay line. 200 nanoseconds later the delay line reflection turns off transistor Q2. During the 200 nanosecond period, output transistor $Q 5$ generates a 200 nanosecond timing clock which is amplified by 56D5B. The output of 56D5B (TBB) is applied to a fan-out of several amplifiers and is available at TP3. The amplifiers apply the TBB signal to several other logic circuits, including the BIT COUNTER flipflop (BBCNT), 56C3A.

The result of the TBA and TBB generation circuits produces two 200 nanosecond clock pulses spaced 651 nanoseconds apart and occurring at the leading and trailing edge of the positive half cycle of the 768 KHz square wave. This produces two clocks during each bit period of 1.302 microseconds.

Bit Time Counter, BCNT1-BCNT5 (Refer to Dwg. 2144556 Sheet 1.)
The Bit Time Counter located on the A5 board is a five stage ring counter with a reset on the first two stages. The counter states are shown in Figure 3-8.

Initial conditions are set into the counter by clearing the first two stages. The counter is shifted by the TBA-N pulses from amplifier 56D6B. TBA-N shifts the state of the lower numbered stages to the higher number stages. The Bit Counter utilizes a walking grey code, shown in Figure 3-8, to decode the ten bit counts, BT1A through BT10A.

| COUNT | BCNT1 | BCNT2 | BCNT3 | BCNT4 | BCNT5 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 0 | 0 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 | 0 |
| 4 | 1 | 1 | 1 | 0 | 0 |
| 5 | 1 | 1 | 1 | 1 | 0 |
| 6 | 1 | 1 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 |
| 8 | 0 | 0 | 1 | 1 | 1 |
| 9 | 0 | 0 | 0 | 1 | 1 |
| 10 | 0 | 0 | 0 | 1 |  |

NOTE: These outputs may be seen at the "1" or "0" sides of the BCNT flip-flops.

Figure 3-8. Walking Grey Code Counter


- ChP: Character pulse - every character at bpia
- DRS: DISPlAY REGISTER STROBE-EVERY CHARACTER AT BTIA AND BTIOB
- MSG: MONOSCOPE SWEEP GATE-EVERY ChARACTER at bTIA AND bTZA
- CHCT: CHARACTER COUNTER TRIGGER-EVERY CHARACTER BT4A

Figure 3.9. Bit Counter Timing

The Bit Counter is a self-correcting type in that on initial start-up the states of the counter are not determinable but after a few counts the reset will correct the count. For example, when the BCNT4 and BCNT5 flip-flops contain the "01" count, the BCNT1 and BCNT2 flip-flops are reset. In one case the count could be "00101". The next counts then would be 00010 and 10001; then the first two stages would again be reset to provide the counter state of 00001 . The counter would then proceed to count as shown in Figure 3-8.

## Bit Time Decoding

The "A" bit times (BT1A-BT1OA) are formed by ANDing the BIT COUNTER flip-flop outputs to decode the desired counts.

The output of the "B" BIT COUNT flip-flop is applied to AND logic along with the outputs of the Bit Counter to produce the bit times BT1B thru BT1OB. The "B" BIT COUNT flip-flop (BBCNT) is triggered by the second timing clock, TBB-N, which occurs 651 nanoseconds later than TBA. The "B! bit times trail the "A" bit times by 651 nanoseconds, as shown in Figure 3-9. Note that many of the bit times are not decoded.

## Character Counter, CHC1-CHC6 (Refer to Dwg. 2144556 Sheet 2.)

The Character Counter, located on the A5 board, is a standard six stage binary counter with 64 counts. Each count corresponds to one of the 64 character positions on one line of the viewer 20 line raster. The Character Counter is triggered by CHARACTER COUNT TRIGGER, CHCT (56B7A-SH3), which occurs once each character time. The Character Counter outputs in conunction with the Line counter outputs generate the following signals (Figure 3-10):

```
BOL = Beginning-of-Line
EOL = End-of-Line
BOP = Beginning-of-Page
    IOBP = I/O Beginning-of-Page
    COEOP = Center-or-end-of-page
    EOP = End-of-Page
    V SYNC = Vertical SYNC
    H SYNC = Horizontal SYNC
```

For example, the logic decodes character count 55, and this count is ANDed with $B T 10 B$ to produce the END-OF-LINE (EOL) pulse, which triggers the Line Counter.


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Figure 3-10. Character Counter Timing

Line Counter, LC1-LC5 (Refer to Dwg. 2144556 Sht. 2.)
The Line Counter, located on card A5, is a five stage counter that generates the 20 line count (Figure 3-11). The counter is a decrementing type counter with selective reset in the second and third stages. Two outputs are generated by the Line Counter. LOOP occurs after line 10 and line 20 and is used to generate CENTER OR END-OF-PAGE (COEOP). Ll is generated after the last line and is used to generate END-OF-PAGE (EOP) and BEGINNING-OF-PAGE (BOP). L1 is also used to generate VERTICAL SYNC (VSYNC), which is sent to the Deflection Amplifier to provide vertical retrace.


Figure 3-11. Line Counter Timing

### 3.4.3 DELAY LINE MEMORY, A7

The Delay Line Memory unit used in the $70 / 752$ VDT is manufactured by two vendors. The first type is manufactured by Laboratory for Electronics, Inc. (Figure 3-12.) The second type is the unit manufactured by Digital Devices, Inc. (Figure 3-13.) The theory of operation of each type is covered in the following paragraphs.

## Laboratory For Electronics Delay Line Memory

The Delay Line is a magnetostrictive type with a delay time of $16,703 \pm 27$ microseconds. This storage time provides storage of one complete page of information ( 1080 characters, each 13.02 microseconds in duration, plus 200 character times utilized as flyback time, for a total of 1280 character times). Since each character contains ten bits of data of 1.302 microseconds duration each, the Delay Line can contain 12,800 data bits in addition to a start character (sync bits), and several NUL (all zero) characters.

The data inserted into the Delay Line is in the return-to-zero format; that is, a "1" bit is applied to the delay line as a positive pulse while a "0" bit requires no pulse at all. The total length of the Delay Line varies with temperature and affects the total Delay Line storage time. The variance in the delay time makes it necessary to resync the timing at the end of each displayed page. This resync cycle is controlled by the WAIT-HOLD-START logic, which is explained in paragraph 3.3.4.

The magnetostrictive Delay Line consists of a metal wire, about 160 feet long. The input transducer, on one end of the delay wire, launches a torsional wave into the wire. This wave propagates in the wire with a velocity of about 100 microseconds per foot. At the other end of the wire, the output transducer translates the torsional wave into an electric signal. With an output current of about 30 milliamps, the output voltage will be about two millivolts. Because of the small output signal an amplifier is provided. The amplifier output signal is reshaped in the detector and will then resemble the input signal. The driver provides the current to the Delay Line input transducer.

## Circuit Description (Refer to Figure 3-12.)

The electrical portion of the Delay Line Memory is divided into three parts: the driver, the amplifier, and the detector.

The input signal turns on $Q 1$ enabling current flow through the input transducer. This current is limited by R3, a resistor inside the Delay Line. When Q1 turns off, the storage energy in the transducer is absorbed through CR2 by R3. If no input signal is connected, CR1 limits the negative base-emitter voltage of Q1.

The output amplifier consists of three stages (Q3, Q4, and Q5) providing a voltage gain of about 76 db . An emitter follower $Q 2$ is provided to make the delay line output termination less dependent on the input impedance of the amplifier. The gain of the amplifier is, in part, determined by the signal developed in the ratio of collectors to emitter resistors of $Q 3, Q 4$, and 85. To provide a gain control, the emitter resistor (R15) of $Q 5$ is variable and can change the gain by about 6 db . Emitter follower $Q 6$ isolates the detector from the amplifier and provides the signal for the test point. A test point at the amplifier output allows observation of the signal-to-noise ratio and the signal amplitude.



The detector consists basically of a tunnel diode (CR3) and a transistor (Q7) with a bias network (CR4, R23, R26, C15). A signal of 1.5 volts at the emitter of $Q 6$ will cause a current of about one milliamp to flow into the tunnel diode through R22. Any increase in input signal will now drive the tunnel diode into the negative resistance region. The voltage across the tunnel diode will increase and most of the signal current will flow into the base of $Q 7$. This transistor will turn on and its collector voltage will drop to about 0.25 volts. $Q 8$ will turn off and the output voltage will rise to 4.5 volts. When the input signal returns to zero, $Q 7$ will turn off and the collector current of $Q 7$ will now flow into the base of Q8. The output voltage will then be about 0.25 volts.

A bias of 0.4 volts provided by the network shifts the tunnel diode's characteristic curve. The load line of the combined tunnel diode-base/emitter (of Q7) characteristic will cross the base/emitter characteristic before it crosses the portion of the tunnel diode characteristic after the valley point voltage. This causes most of the tunnel diode current to flow into the base of 07 after the input current exceeds the peak point current. In a like manner, as the signal voltage is removed, the tunnel diode retraces over the current peak and the voltage falls, allowing insufficient bias for Q 7 .

## Digital Devices Delay Line Memory

The second Delay Line Memory is similar to the first type and utilizes the same voltage levels. The two units are considered interchangeable and no rewiring is necessary when replacing one type with the other.

Circuit Description (Refer to Figure 3-13.)
The electrical portion of the Delay Line Memory is divided into four parts: the input driver, the amplifier, the quantizer, and the output one shot.

The INPUT signal is applied through logic gates 21 A and $\mathrm{Z1B}$ (an inverter) to a push-pull output stage (Q11 and 12). The push-pull output drives the delay line input transducer which launches a torsional wave into the delay line wire.

The delay line output transducer is connected to the output amplifier. The output amplifier consists of a six stage amplifier (Q1 through Q6). Amplitude adjustment is made by adjusting potentiometer R11. The amplifier output is available at test point TP1.

The output of the six stage amplifier is applied to the quantizer consisting of Q7 and CR1. The quantized output signal turns on Q8. The one shot (Q9 and 10) is triggered and the one shot output is available at test point TP2. The one shot output is applied to the Delay Line Memory OUTPUT through logic gate zlc.

### 3.4.4 REGISTER LOGIC CARD, A3 (Refer To Figure 3-14.)

## Delay Line Register, DLR (Refer to Dwg. 2144558 Sht. 2.)

The DLR is an eleven stage shift register, the contents of which are parallel transferred to the Display Register (DR). The function of the DLR is to act as the input register for the Delay Line Memory, A7. During normal recirculation of stored data, the Delay Line Memory output is amplified, shaped, stretched, and applied to the input stage of the DLR. After being parallel shifted into the DR, the character bits are again serially shifted back into the Delay Line Memory.

## Display Reqister, DR (Refer to Dwg. 2144558 Sht. 2.)

The DR functions as a storage buffer between the DLR and the Selection Amplifier, A8. This allows storage of each character for one full character time (13.02 microseconds) in the DR while the next character's bits are being serially shifted out of the delay line and into the DLR, and the previous character's bits are being shifted back into the delay line for recirculation. During this storage time, the character bits stored in the DR are applied to the Selection Amplifier, A8, and $D / A$ converters which convert the $X$ and $Y$ deflection bits into equivalent gross positioning voltages for selection of the proper character on the monoscope character stencil.

The Display Register also has a set of input AND gates connected to the set terminal of the seven flip-flops (DR1 through DR7), which are used to enter the seven character bits from the keyboard microswitches during keyboard entry.

## Delay Line Reqister Entry Circuit (Refer to Dwq. 2144558 Sht. 2.)

The delay line entry circuit, located on card A3, consists of an inverter-amplifier 58C1A, the DELAY LINE STRETCH (DLS) flip-flop, and the DELAY LINE REGISTER INPUT flip-flop (DLRIN) (Figure 3-3).

The DLR entry circuit receives the 225 nanosecond output of the keyboard filter one shot, which is the amplified Delay Line Memory output DLOUT-P. The DELAY LINE STRETCH flip-flop (DLS) stretches the one shot signal and applies it to the DELAY LINE REGISTER INPUT flip-flop (DLRIN). The TBB clock pulse controls the shifting of the data into the DLR.

## Keyboard Parity Generator (Refer to Dwg. 2144558 Sht. 1.)

The PARITY GENERATOR flip-flop (KBP) monitors the output of the Display Register stage CR1. When a character has been entered into the DR from the keyboard microswitches, the character bits are serially shifted to the Delay Line Memory input circuits through gate 58C6B. During the transfer of the character bits, the output of the KEYBOARD PARITY GENERATOR flip-flop is ANDed with BT8B-P. When the number of "l's" counted by the KBP flip-flop is an odd number, the AND circuit enters an additional "1" bit into the delay line input circuit to make the total character "1" bit count an even number.

## Keyboard Parity Checker (Refer to Dwg. 2144558.)

When the character bits exit the delay line and enter the DLR, the parity count (number of "1" bits) is monitored by the DISPLAY PARITY CHECK flip-flop, DPC (58A8A). When the DPC flip-flop parity count ("1's") is an even number, the character in the DR is displayed. When the parity count ("1's") detected by the DPC is an odd number, the logic causes a bright square block to be displayed in place of the faulty character.

## Normal Recirculation of Stored Data

Figure 3-14 shows the normal recirculation path of data stored in the Delay Line Memory. Stored character bits are shifted serially into the Delay Line Register from the Delay Line Memory, through a 225 nanosecond one shot pulse shaper, located in the keyboard filter (A21), and through the DLR input circuit, located on card A3.


TBB serial shifts the DLR every 1.302 microseconds; therefore the bit rate is 768,000 bits per second. When a character is shifted into the DLR, the least significant bit is the first to shift from the delay line into DLRMN (Mark Now) flip-flop. The first bit per character is shifted in at BT1B. At BT10B the complete ten bit character is in the DLR. The least significant ASCII character bit is in DLR1 and the most significant bit is in DLR7. The parity bit is in DLRP, and the mark bit is in DLRMN. The format bit will be set to "1" in DLRF only for a format character.

## Parallel Shift of Data From DLR to DR

The parallel shift is enabled by DLR ENABLE (DLREN) from 58C8B. The DLREN signal is present at time BT1A•BT1OB, during the second 651 nanoseconds of BT10B. During this gating period the DLR contents are enabled through AND gates to set the character bits into the Display Register where they are held for one character period, or 13.02 microseconds. The serial shift of the DLR is continuous; the character shifts out of the DLR into the delay line input for memory recirculation. The next character from the delay line is similarly shifted into the DLR.

Delay Line Memory Entry Circuit (Refer to Dwg. 2144558 Sht. 1.)
The delay line entry circuit consists of an OR gate (58B6A and B) through which data is routed from six sources and stored in the Delay Line Memory, A7
(Figure 3-15).

## DTDLM Generation

To standardize the input signal to the delay line memory, all input signals are routed from the delay line entry OR circuit to the AND circuit 58B6C, where the input signal is ANDED with the 768 KHz square wave and the output of the 130 nanosecond delay line (DL1). The AND circuit generates a standardized pulse 521 nanoseconds wide and delayed 130 nanoseconds from the leading edge of the TBA pulse. This standardized pulse is DISPLAY TO DELAY LINE MEMORY (DTDLM-P), which is the "1" bit entered into the Delay Line Memory for each "1" bit of data to be stored.

## Normal Recirculation

The normal recirculation path from the Delay Line Register (DLR) output stage is routed to the $O R$ circuit (through other gating logic) to pin 4 of 58B6B. During normal recirculation, all data displayed is recirculated at a 60 Hz rate to constantly refresh the viewer screen phosphor.

## Keyboard Entry

When the operator selects a new character at the VDT Keyboard, the character bits are entered into the Display Register, and serially shifted from the DR output stage (DR1-P) through gating logic to the OR circuit input at 58B6B pin 2.


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Figure 3-15. Delay Line Entry, Block Diagram

## Remote Data Entry

When data is being received from the Basic Processor Unit, whether it is remotely located or at the local installation, the received data is routed from the InputOutput Registers (in units A1 and A2) through gating logic by the BUFFER TO DISPLAY signal (BTD) and applied to the OR circuit at 58B6B pin 1.

## Note

The received data is shifted into the I/O registers at the 1200 bit rate of the Data Set and shifted out of the $I / O$ registers at the 768 KHz rate of the delay line.

SYNC Pulse Entry
The SYNC pulse from the Breakout Gate (BOG) circuit is applied to the delay line entry OR circuit at 58B6A pin 5. This enters the breakout gate signal into the delay line to form the first SYNC pulse stored in the Delay Line Memory during RE-SYNC time at the beginning of each page display time (before the start of a new page entry at line 1).

Format or Mark Insert (FOMI)
The initial entry of the mark (or cursor) is routed from the mark logic to the OR gate at 58B6A pin 4.

When the Format Special Feature is installed in the $70 / 752$ VDT, the operator can request a Standard Format from the BPU. The Format bit is entered in a Format Data character through gating logic to the delay line entry OR circuit at 58B6A pin 4.

## Keyboard Parity Entry

When a new character is entered from the Keyboard and the parity generator generates a "1" to make the character parity count even, the parity bit is entered into the Delay Line Memory at 58B6B pin 5.

### 3.4.5 MARK LOGIC, A4 (Refer to Dwg. 2133557.)

The mark logic board contains the logic that controls the movement of the mark (or cursor) in the Delay Line Memory and the position of the mark on the Viewer screen. The A4 board also controls the Data Insert Feature logic (one of the standard features).

Some of the operations controlled by the mark movement are:

1. Transmission of data
2. Reception of data
3. Erase operations
4. Printing sequences
5. Keyboard input
6. Manual mark movements initiated by the operator such as:
a. Mark advance
b. Backspace
c. Line advance

## Mark Position Sensing

To enter characters in the Delay Line Memory at the proper position the position of the mark must be sensed when it is in the Delay Line Register (DLR). This ensures correct placement of characters, allows the mark to be advanced or backspaced, and additional characters to be inserted or erased.

The position of the mark is sensed in the DLR at the Register Input flip-flop DLRIN, the Mark Now flip-flop (DLRMN), and at the output end of the register at flip-flop DLRME, the Mark Early flip-flop (Dwg. 2144558 Sht. 2.).

## Backspace Operation

During the backspace operation, when the character having the mark enters the Delay Line Register and the mark bit is positioned in the DLRMN (Mark Now) flipflop, the mark bit is sensed in the Mark Now flip-flop DLRMN. The Mark Early flip-flop (DLRME) is set and the DLRMN flip-flop is cleared.

## Note


#### Abstract

The backspace command depends upon DLRMN Steering (DLRIN levels) to set the MKFF at BT1OB. The output of the MKFF in this case enables the gate BKS-N and at the next TBA, the BKS-N signal resets the DLRMN flip-flop and sets the DLRME flip-flop, effectively moving the mark back one character time on the viewer screen. This means the mark bit now enters and exits the Delay Line Memory one character time earlier than it did previous to the backspace operation being initiated. This means the mark will appear on the Viewer screen one character time sooner than it had previously.


## Mark Advance Operation

To advance the mark, it must be sensed in the Mark Early flip-flop. Note that this flip-flop is at the output end of the DLR and therefore the character containing the mark bit has already been serially shifted out of the DLR (with the exception of the mark bit). The Mark Early (DLRME) flip-flop can be cleared and the Mark Now flip-flop (DLRMN) can be set. The mark bit will now enter and exit Delay Line Memory one character time later than it did before the advance operation was initiated. This means the mark will appear on the Viewer screen one character time later, or effectively will be advanced one character on the display.

Mark Control Cycle Counter (Refer to Dwa. 2144557 Sht. 2.)

## Note

To eliminate the effects of the command switch contact bounce, the outputs of all mark control panel matrix switches and Keyboard Strobe are ORed to produce the MARK CONTROL (MK CONT) signal. The MARK CONTROL signal is used to activate the Mark Control Cycle Counter.

The function of tine Mark Control Cycle Counter is to delay keyboard entry and mark control actions for $\Omega$ to 16 milliseconds to bypass the contact bounce interval, and to cause advance and backspace functions to repeat at a rate of 9 times per second.

When a mark conmand has been entered, the mark control and COEOP, (Center-or-End-of-Page) signals will advance the counter to a count of one, (CC1 Set=001). The next center-or-end-of-rpage pulse will advance the counter to a count of two (CC2 Set=010). Note that the advance to count two may take from a minimum of 8.3 milliseconds to a maximum of 16.6 milliseconds from the time the mark command was entered. The count of two (010) enables the steering gates of the MKFF to sample the mark bit of eacl character as it is shifted through the DLR. When the mark is det.ected at DLRMN (for backspace) or DLRME (for other functions), the MKFF is set to move the mark. The mark is detected at DLRMN to activate data entry or erase functions.

## Keyboard Entry

Normally, the Delay Line Register Enable signal (DLREN) transfers successive characters from the DLR to the DR, where each is held for one character time. When a character is typed, KBS activates the mark control logic. Detection of the mark in DLRMN blocks DLREN and activates the Keyboard Enable signal (KBEN). KBEN transfers the keyboard character into the DR and sets the Keyboard Entry (KBE) flip-flop. KBE enables the DATA INSERT AND KEYBOARD ENTRY (DIKE) signal (which blocks DLRME and enables DR1 into the delay line input circuit) and activates the DISPLAY REGISTER TRIGGER (DRT) pulses, which shift the character through the DR1. At the end of the character time, KBE is cleared and data flow returns to normal. A character may be entered into a blank position in the displayed page or it may replace a character previously stored.

## Data Insert

If a character is to be inserted into a series of characters already stored (for example, to change INERT or INSERT), the Data Insert switch is turned on and the new character typed into the position occupied by the character which should follow it (for example, position the mark under $E$ and type S). The keyboard entry is done normally but, with the DI switch on, KBE sets the DATA INSERT DISPLAY (DIDF) flip-flop.

DIDF maintains the DIKE and DRT functions after KBE is cleared. While the character in the DR is shifted to the delay line, the character in the DLR is shifted into the DR (Figure 3-16.) As long as DIDF remains set, the previously stored characters are delayed one character time before being returned to the delay line. At the end of each line, the End-of-Line flip-flop (EOLF) blocks DIKE and DRT to hold the last character on the line until the beginning of the next line. DIDF is cleared at the end of any line in which the last character is non-graphic (NUL or control code) or at the end of page.

## Erase Functions

The operator may select a Matrix Switch to enable logic to erase either an individual character, a complete line (or last part of the Line), or the entire page presentation on the viewer screen. When a single character is erased, the logic will move the mark to the next character. When all or part of a line is erased, the mark is automatically advanced to the beginning of the next line. When the entire screen is erased, the mark returns to zero or the beginning of the first line of the displayed page.

Table 3-1. Glossary of Mnemonics

| MNEMONIC | DESCRIPTION | DRAWING NO. | SHEET |
| :---: | :---: | :---: | :---: |
| 19.2 KHz | H. V. ENABLE | 56 | 2 |
| A1-1P | BUFFER REGISTER NUMBER 1 (B1) | 59 | 2 |
| A2 (1P) | BUFFER REGISTER NUMBER 2 (B2) | 59 | 2 |
| ADVSW | ADVANCE SWITCH |  |  |
| ASK | ADVANCE OR STROBE KEYBOARD | 57 | 2 |
| AT (1P) | TR REGISTER FULL | 59 | 2 |
| ATA | TR REGISTER FULL (PRINTER) | 70 | 1 |
| B11-B18 | BUFFER 1 REGISTER | 59 | 1 |
| B21-B28 | BUFFER 2 REGISTER | 59 | 1 |
| B2T | BUFFER 2 TRIGGER CONTROL | 59 | 2 |
| BBCNT | "B" BIT COUNT |  |  |
| BCNT1-BCNT5 | BIT COUNTER | 56 | 1 |
| B11N | BUFFER 1 INPUT | 59 | 2 |
| BKS | BACKSPACE | 57 | 1 |
| BKSPL | BACKSPACE LOOKOUT | 67 | 1 |
| BOL | BEGINNING OF LINE | 56 | 2 |
| BOG | BREAKOUT GATE (1ST SYNC BIT) | 58 | 2 |
| BOP | BEGINNING OF PAGE | 56 | 2 |
| BTD | BUFFER TO DISPLAY | 59 | 2 |
| BTDS | BUFFER TO DISPLAY SET | 59 | 2 |
| BT1A-BT10A | BIT TIME 1A-10A | 56 | 1 |
| BT1B-BT10B | BIT TIME 1B-10B |  |  |
| B2T | BUFFER 2 TRIGGER CONTROL | 59 | 2 |
| CA2 | CLEAR A2 | 60 | 2 |
| CC1, 2, 4 | CYCLE COUNTER | 57 | 2 |
| CCC | CLEAR CYCLE COUNTER | 67 | 1 |

Table 3-1. Glossary of Mnemonics (Cont'd)

| MNEMONIC | DESCRIPTION | DRAWING NO. | SHEET |
| :---: | :---: | :---: | :---: |
| CFMC | CLEAR FORMAT MODE CONTROL | 59 | 1 |
| CHC1-CHC6 | CHARACTER COUNTER (1-6) |  |  |
| CH1 | CHARACTER COUNT 1 | 56 | 2 |
| CH5 5 | CHARACTER COUNT 55 | 56 | 2 |
| CHARACTER UNBLANK |  | 58 | 2 |
| CHCT | CHARACTER COUNTER TRIGGER | 56 | 3 |
| C HOLD | CLEAR HOLD | 56 | 3 |
| CL | CLEAR | 60 | 1 |
| CNT1-CNT10 | PRINT TIMING COUNTS | 70 | 2 |
| COEOP | CENTER OR END OF PAGE | 56 | 2 |
| COG | CARRY OVER GATE | 57 | 1 |
| CR | CARRIAGE RETURN | 57 | 1 |
| CRCD | CARRIAGE RETURN CODE DETECT | 58 | 1 |
| CRDR | CARRIAGE RETURN IN DR | 58 | 1 |
| CRET | CARRIAGE RETURN OR END TEXT | 58 | 1 |
| CRLE | CARRIAGE RETURN OR LINE ERASE | 57 | 1 |
| CRRCV | CARRIAGE RETURN RECEIVED | 59 | 1 |
| CRSW | CARRIAGE RETURN SWITCH | 57 | 1 |
| C SYNC | CLEAR SYNC F.F. (STARTING I.O. COUNTER) | 60 | 2 |
| CTS | CLEAR TO SEND (FROM DATA SET) |  |  |
| CTS-D | CLEAR TO SEND DIRECT (TO PROCESSOR) | 60 | 2 |
| DATA | PRINTER OUTPUT | 70 | 2 |
| DIDF | DATA INSERT DISPLAY F.F. | 57 | 2 |
| DIKE | DATA INSERT OR KEYBOARD ENTRY | 57 | 2 |
| DISW | DATA INSERT SWITCH |  |  |

Table 3-1. Glossary of Mnemonics (Cont'd)

| MNEMONIC | DESCRIPTION | DRAWING NO. | SHEET |
| :---: | :---: | :---: | :---: |
| DLMIN | DELAY LINE MEMORY INTO DLR |  |  |
| DLR1-DLR7 | DELAY LINE REGISTER | 58 | 2 |
| DLREN | DELAY LINE REGISTER ENABLE | 57 | 1 |
| DLRF | DELAY LINE REGISTER FORMAT BIT | 58 | 2 |
| DLRIN | DLR IN FF | 58 | 2 |
| DLRME | DELAY LINE REGISTER MARK EARLY | 58 | 2 |
| DLRMN | DELAY LINE REGISTER MARK NOW |  |  |
| DLRP | DELAY LINE REGISTER PARITY | 58 | 2 |
| DLS | DELAY LINE STRETCH F.F. | 58 | 2 |
| DPC | DISPLAY PARITY CHECK | 58 | 1 |
| DR1-DR7 | DISPLAY REGISTER | 58 | 2 |
| DRF | DISPLAY REGISTER FORMAT | 58 | 2 |
| DRM | DISPLAY REGISTER MARK F.F. | 58 | 2 |
| DRPE | DISPLAY REGISTER PARITY ERROR | 58 | 2 |
| DRR | DISPLAY REGISTER RESET | 58 | 2 |
| DRT | DISPLAY REGISTER TRIGGER | 58 | 1 |
| DSR | DATA SET READY |  |  |
| DTB | DISPLAY-TO-BUFFER CONTROL | 59 | 2 |
| DTDLM | DISPLAY TO DELAY LINE MEMORY | 58 | 1 |
| DTR | DATA TERMINAL READY | 60 | 2 |
| EAR | ERASE AFTER RECEIVE | 57 | 2 |
| ELF1 | ERASE LINE AND FLYBACK INHIBIT | 57 | 1 |
| EOL | END OF LINE | 56 | 2 |
| EOLF | END OF LINE F.F. | 57 | 2 |
| EOP | END OF PAGE | 56 | 2 |
| EOT | END OF TEXT | 65 | 2 |

Table 3-1. Glossary of Mnemonics (Cont'd)

| MNEMONIC | DESCRIPTION | DRAWING NO. | SHEET |
| :---: | :---: | :---: | :---: |
| EP59 | END OF PAGE, CHAR 59 | 56 | 3 |
| ETX | END OF TEXT | 65 | 1 |
| ETXDR | END OF TEXT IN DISPLAY REGISTER | 58 | 1 |
| FBI | FORMAT BIT INSERT | 67 | 2 |
| FBMS | FORMAT BIT MARK STORE | 67 | 3 |
| FIG | FORMAT INSERT GATE | 67 | 3 |
| FMI | FLYBACK MARK INHIBIT | 67 | 2 |
| FMRF | FORMAT MARK REMEMBER F.F. | 67 | 3 |
| FOMI | FORMAT OR MARK INSERT | 67 | 3 |
| GC-N | GRAPHIC CHARACTER GATE |  |  |
| HOLD | STOPS BASIC TIMING | 56 | 3 |
| H SYNC | HORIZONTAL SYNC | 56 | 2 |
| IOBP | I/O BEGINNING OF PAGE | 56 | 2 |
| IFM | INHIBIT FORMAT |  |  |
| IOCNT 575 | I/O COUNT 575 | 59 | 2 |
| IOCO-IOC9 | I/O COUNTER | 59 | 1 |
| IOM3D | IOM 3 DELAYED | 65 | 2 |
| IOMC1-IOMC4 | I/O MODE COUNTER | 60 | 1 |
| IOMO | WRITE MODE |  |  |
| IOMO- IOM15 | INPUT OUTPUT MODE (0-15) | 60 | 1 |
| IOMOCL | IOMO CLEAR | 60 | 1 |
| KBE | KEYBOARD ENTRY F.F. | 57 | 2 |
| KBEN | KEYBOARD ENABLE | 57 | 1 |
| KBEND | KEYBOARD ENTRY DELAYED' | 57 | 2 |
| KBP | KEYBOARD PARITY GENERATOR | 58 | 1 |
| KBS | KEYBOARD STROBE | 58 | 2 |

Table 3-1. Glossary of Mnemonics (Cont'd)

| MNEMONIC | DESCRIPTION | DRAWING NO. | SHEET |
| :---: | :---: | :---: | :---: |
| LC1-LC5 | LINE COUNTER (1-5) | 56 | 2 |
| LE | LINE ERASE | 67 | 1 |
| LEFF | LINE ERASE F.F. |  |  |
| LEG | LINE ERASE GATE | 57 | 2 |
| LESW | LINE ERASE SWITCH | 57 | 1 |
| LFCR | LINE FEED CARRIAGE RETURN | 70 | 1 |
| LOOP | CENTER OF PAGE LINE OR END OF PAGE LINE | 56 | 2 |
| MAG | MARK ADVANCE GATE | 57 | 1 |
| MCL | MASTER CLEAR |  |  |
| MEL | MARK END OF LINE | 57 | 1 |
| MESS | MARK EARLY SET STROBE | 57 | 2 |
| MIG | MARK INHIBIT GATE | 57 | 1 |
| MK | MARK F.F. | 57 | 1 |
| MK CONT | MARK CONTROL | 57 | 1 |
| MK/EOL | MARK/END OF LINE | 70 | 1 |
| MSG | MONOSCOPE SWEEP GATE | 56 | 3 |
| NIFTO | NULL INHIBIT TO FORMAT DATA | 67 |  |
| NONSEL | NON SELECTED | 65 | 2 |
| NULL | NULL CHARACTER DECODED | 59 | 1 |
| PCR | PRINT CARRIAGE RETURN | 70 | 1 |
| PLEOT | PRINT LOAD EOT | 65 | 1 |
| PLF | PRINT LINE FEED | 70 | 1 |
| PRT | PRINT MODE | 70 | 1 |
| PRXMT | PRINT/TRANSMIT | 65 | 2 |
| PS1-PS4 | PRINT PULSE COUNTER | 70 | 2 |

Table 3-1. Glossary of Mnemonics (Cont'd)

| MNEMONIC | DESCRIPTION | DRAWING NO. | SHEET |
| :---: | :---: | :---: | :---: |
| RAH | RECEIVE AFTER HOLD | 67 | 1 |
| RBNF | RECEIVE BUFFER NOT FULL | 59 | 1 |
| RCV | RECEIVE | 60 | 1 |
| RCV DATA | RECEIVE DATA | 60 | 1 |
| RCVR | RECEIVE START BIT FROM DATA SET | 60 | 2 |
| RCVT | RECEIVE (I/O MODE ENABLES RECEIVE OF DATA) | 60 | 1 |
| RNC | REQUEST NEXT CHARACTER | 70 | 2 |
| RS | REQUEST TO SEND (TO DATA SET) | 59 | 2 |
| RS-D | REQUEST TO SEND DIRECT (FROM PROCESSOR) |  |  |
| SA1 | SET AI F.F. (INDICATES BUFFER 1 FULL) | 70 | 2 |
| SA2 | SET A2 F.F. (INDICATES BUFFER 2 FULL) |  |  |
| SB16 | SET B16 (B1 REG BIT 6) | 70 | 2 |
| SB1T | SET BUFFER 1 TRIGGER F/F | 70 | 1 |
| SCNT1-SCNT4 | PRINTER STROBE COUNTER | 70 | 2 |
| SCOR | STORE CHARACTER OR RECEIVE | 57 | 1 |
| SEMC | SCREEN ERASE OR MASTER CLEAR | 57 | 1 |
| SEMS | SCREEN ERASE MARK STORE | 58 | 1 |
| SETMN | SET MARK NOW | 57 | 2 |
| SFMC | SET FORMAT MODE CONTROL | 59 | 1 |
| SLSHR | SLOW SHIFT RECEIVE | 59 | 2 |
| SLSHX | SLOW SHIFT TRANSMIT | 59 | 2 |
| SLST | SLOW SHIFT START (PRINTER) | 70 | 2 |
| START | TIMING CONTROL F.F. | 56 | 3 |
| STX | START OF TEXT | 60 | 2 |

Table 3-1. Glossary of Mnemonics (Cont'd)

| MNEMONIC | DESCRIPTION | DRAWING NO. | SHEET |
| :---: | :---: | :---: | :---: |
| SUB | START UP BIT | 56 | 3 |
| SYNC | SYNC. F.F. - (IO COUNTER CONTROL) | 59 | 2 |
| TBA | TIMING CLOCK A | 56 | 1 |
| TBB | TIMING CLOCK B | 56 | 1 |
| T DATA | TRANSMITTED DATA | 60 | 2 |
| TIOMC | TRIGGER I/O MODE COUNTER | 60 | 2 |
| TRO-TR8 | TRANSMIT/RECEIVE REGISTER | 60 | 2 |
| TRIN | TRANSMIT/RECEIVE REGISTER INPUT | 60 | 2 |
| TRT | TRANSMIT/RECEIVE TRIGGER CONTROL | 59 | 2 |
| V SYNC | VERTICAL SYNC | 56 | 2 |
| WAIT | TIMING CONTROL F.F. | 56 | 3 |
| WFDE | WRITE MODE-FORMAT DATA ERASE |  |  |
| WRL | WRITE LAMP | 60 | 1 |
| WRSW | WRITE SWITCH |  |  |
| XBNF | TRANSMIT BUFFER NOT FULL | 59 | 1 |
| XMT, XMTF, XMTR, XMTRC | TRANSMIT MODES | 60 | 2 |
| XMTSW | TRANSMIT SWITCH | 60 | 2 |
| ZIM | ZERO INDEX MARK |  |  |
| ZIM10 | ZIM MODE 10 | 70 | 1 |
| ZIM11 | ZIM MODE 11 | 70 | 1 |
| ZMD | ZERO MARK DELAY | 67 | 3 |
| ZMKS | ZERO MARK STORE F.F. | 67 | 3 |



Figure 3-16. Data Insert Data Flow

### 3.5 CHARACTER GENERATOR (Refer to Figure 3-17.)

The Character Generator's function is to convert the selected character digital data into video for display on the Viewer screen. This is done by converting the digital bits from the Display Register into equivalent analog deflection voltages which are applied to the Monoscope tube (A10) as gross deflection voltages to select the correct character on the Monoscope stencil (Figure 3-18).

The Monoscope beam then scans the stencil cutout for the selected character and generates a series of video pulses equivalent to the character which is then applied to the Viewer CRT control grid. The Monoscope and the Viewer CRT Tickler scan frequencies are synchronous so that the selected character appears on the Viewer screen instantaneously as it is produced in the Monoscope tube.

### 3.5.1 SELECTION AMPLIFIER, A8

The Character Selection Amplifier card is located behind the Viewer front panel with all circuit adjustments available to the operator on the adjustment panel located at the left side of the Viewer panel (operator's right). The Selection Amplifier circuit consists of two digital-to-analog (D/A) converters, (one for $X$ deflection bits and one for $Y$ deflection bits,) a two channel deflection amplifier circuit and a horizontal sweep ramp generator. The function of the Selection Amplifier is to convert the selected character digital data bits (X and Y) from the Display Register into gross positioning deflection voltages which are applied to the deflection plates of the Monoscope tube to select the correct character cutout on the Monoscope stencil.


## HORIZONTAL SELECTION CODE - $b^{3} b^{2} b^{1}$ <br> VERTICAL SELECTION CODE - $b^{7} b^{5} b^{4}$

(

The gross positioning voltages position the Monoscope beam at the left side of the stencil character cutout for the selected character. The beam then scans the character cutout both horizontally and vertically to produce the equivalent series of video pulses on the Monoscope plate or target.

Digital-TO-Analog Converters (DACON, or D/A)
The $X$ and $Y$ channels of the Selection Amplifier $D / A$ converters are similar, therefore only the $X$ or horizontal channel is explained in detail (Figure 3-19). The input to the $X$ channel of the $D / A$ converter is a three-bit binary code from the Display Register which represents the horizontal position of the selected character on the Monoscope character stencil.

## D/A Selection Switches

The binary coded bits determine how many of the selection switches on the $D / A$ constant current ladder network will be turned off or on to subtract or add current to the current summing bus (Figure 3-19). The selected current on the summing bus is applied to the input of integrated circuit zO .

## Note

The binary input permits selection of eight discrete current levels that can be injected into the current summing bus which permits horizontal gross positioning on the complete Monoscope character stencil to select one of 64 characters.

## Differential Operational Amplifier

The high-gain operational amplifier consists of $202, \mathrm{Q} 18,19,22$, and 23 (Figure 3-19). The summed current injected into the input of differential amplifier $Z 02$ is converted into a proportional voltage difference at the output of 202. The $z 02$ output is applied to a differential pair of transistors (Q18 and Q19). The differential pair push-pull output is applied to a pair of emitter followers (Q22 and Q23) which apply the opposite phased deflection voltages to the Monoscope horizontal deflection plates.

## Operational Amplifier Feedback Circuits

The operational amplifier negative feedback circuit components are selected to ensure that the voltage of the current summing bus remains at zero or ground potential by draining away the exact amount of current injected at the circuit input. This ensures that the voltage output of the differential amplifier will always stabilize at a specific voltage level for a specific current input to give accurate gross positioning voltages for the Monoscope.

The secondary feedback circuit function is to maintain equal and opposite voltage amplitudes at the operational amplifier output emitter followers Q22 and Q23. The circuit consists of transistors $Q 20$ and 21 and resistors R98, R99, and R100.


## Note

When a selection switch transistor is turned on by a digital "1", the transistor subtracts the current which its precision current source would normally supply to the current summing bus. When the D/A binary data bit is "O", the switch transistor is turned off (binary 000) and the maximum current is injected into the summing bus. This enables full conduction of transistor Q19 of the differential pair. Conversely, a binary 111 code will enable full conduction of Q18.

## Skew Compensation Circuit

Both the horizontal and vertical channels of the Selection Amplifier have a current pick-off potentiometer connected to the current summing bus to furnish a small skew compensation current to the opposite channels Monoscope deflection plates. This permits an electrical skew adjustment to compensate for any physical rotational misalignment between the Monoscope deflection plates and the character stencil in both the horizontal and vertical plane by altering the deflection plates electrostatic fields.

The vertical D/A converter and amplification channel function identically to the horizontal channel, except that the horizontal channel has an additional circuit to generate the horizontal sweep ramp needed to horizontally scan the individual selected stencil character cutout, while the vertical channel has an additional vertical sweep circuit for vertical tickler scan of the stencil.

## Horizontal Sweep Circuit

The function of the horizontal sweep ramp circuit is to generate a ramp that can be added to the horizontal gross positioning voltage which will cause the monoscope beam to horizontally scan the selected character on the monoscope stencil while the vertical tickler frequency is causing the beam to also scan the stencil vertically at the 1.5 MHz rate. The combined scans generate the character video pulses on the Monoscope target or plate. The ramp generator circuit consists of transistors Q12, 13, and 14 and a linear charging circuit consisting of capacitor C15, resistor R53 and associated components. During circuit operation, the two microsecond MONOSCOPE SWEEP GATE (MSG), which is generated on the Video Driver (A12) is applied to the base of transistor Q12. The pulse causes transistor Q12 to conduct and dissipate the charge on capacitor C15. After the MSG pulse expires, capacitor $C 15$ begins to charge at a linear rate. The resultant linear ramp output is applied to the HORIZ SCAN potentiometer, R57. The wiper of R57 applies the horizontal sweep ramp to the current summing bus of $Z 02$ where it is added to the horizontal gross positioning voltage for the selected character. This results in the generation of the horizontal scan for scanning the selected character on the Monoscope character stencil. The horizontal scan duration is 10.4 microseconds, which gives a linear time base for the Vertical Tickler scan of 1.5 MHz .

## Vertical Sweep Generation Circuit (Refer to Figure 3-20.)

The output of the vertical channel of the Selection Amplifier differs from the horizontal channel by the addition of a vertical sweep generator circuit. The

circuit consists of a potentiometer, two transistors, and an output transformer, T1, containing three windings.

## Tickler Input

The 1.5 MHz Tickler frequency sine wave input is capacitively coupled to the VERTICAL SCAN potentiometer R43. The potentiometer furnishes base drive to transistor Q10, which is connected to one end of the Tickler winding of transformer T1. The opposite end of the Tickler winding is connected to transistor Q11. Adjustment of VERTICAL SCAN potentiometer R43 controls the amplitude of the Tickler scan on the Monoscope character stencil.

The Tickler scan frequency is superimposed on the gross positioning voltage produced by the vertical Selection Amplifier (A8) and applied to the second T1 winding. The resultant voltage output is induced into the third $T 1$ winding and applied to the Monoscope vertical deflection plates.

Voltage Regulator Circuits (Refer to Dwg. 2165479 Sht. 2.)
Several precision voltage regulators required for proper operation of the horizontal and vertical Selection Amplifiers are located on unit A8.

Zener Requlated Voltages (Refer to Fiqure 3-21.)
The $+5.6,-5.6$, and -9.1 vdc power supplies are generated by zener diodes which regulate a portion of a higher voltage supplied by the Low Voltage Power Supply (L.V.P.S.), A14. The zener diodes (CR32, 31, and 34) are reverse-biased through resistors R104, 103, and R110, respectively, to generate the $+5.6,-5.6$ and -9.1 vdc supplies needed by the integrated circuits in the Selection Amplifiers.


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Figure 3-21. Selection Amplifier Voltage Regulator, Simplified Schematic

## -9.1 vdc Isolation Circuit (Refer to Figure 3-21.)

The -9.1 vdc supply has an additional isolation circuit consisting of transistors Q24, 25, and 26. Transistors Q24 and 26 form a differential pair and Q25 is the output stage, which also provides negative feedback to the differential pair. The additional isolation circuit is required to ensure sufficient stability for use as a reference in the +50 volt regulation circuit.

## $\pm 50$ Volt Requlation Circuit (Refer to Figure 3-21.)

The +50 volt precision-regulated power supply is used as a constant current source for the ladder networks in both the horizontal and vertical selection amplifier D/A converters. The +50 volts is also used in the horizontal sweep generator circuit.

The +50 volt regulation circuit consists of differential amplifiers $Z 03$, and $Q 27$ and 28, a Darlington emitter follower output stage, and a negative feedback loop consisting of diodes CR33 and 35 and resistors R107 and 108.

The -9.1 vdc supply is used as an input reference level to differential amplifier Z03. The output of $z 03$ drives a second differential amplifier consisting of Q27 and 28. Transistor Q28 drives the Darlington emitter follower (Q29 and 30) which is connected to the +75 volts supplied by the LVPS. The regulated +50 volt output is taken off the emitter of Q30. Regulation is accomplished by negative feedback through diodes CR23 and 35, and resistors R107 and 108. As the external load varies, the negative feedback to the input of differential amplifier ZO3 causes the circuit to compensate for load variations and maintains a constant +50 volt output, thus maintaining a constant current source for the D/A converter ladder networks, regardless of the number of selection switches being energized by the X and Y binary data bits from the Display Register.

### 3.5.2 MONOSCOPE ASSEMBLY, A1O (Refer to Figure 3-22.)

The Monoscope tube is an electrostatic deflection cathode-ray tube which contains an electron gun, a pair of horizontal deflection plates, a pair of vertical deflection plates, a character stencil, an accelerator anode, and the target, or plate, of the tube (Figure 3-22).

The gross positioning voltages from the horizontal and vertical Selection Amplifiers are applied to the respective deflection plates in the Monoscope tube. The selected character gross positioning voltages cause the electron beam to be positioned on the character stencil at the left side of the selected character cutout. The beam is then moved horizontally by the 11 microsecond horizontal sweep ramp and is simultaneously scanned vertically by the 1.5 MHz Tickler frequency to cover the selected character stencil cutout.

The resultant variation in the voltage level of the plate or target electrode of the Monoscope tube is the character video pulses which are applied through the Video Preamplifier (A1OA) to the control grid of the Viewer CRT and generate the character on the Viewer screen. In order to give a better character presentation on the Viewer screen, the phase of the 1.5 MHz Tickler frequency is reversed $180^{\circ}$ on each alternate scan of the stencil to ensure complete coverage of the selected character cutout (Figure 3-18.)


Figure 3-22. Monoscope

Voltage Divider Network, A10A2 (Refer to Dwg. 2165479, Sheet 2.)
Voltage Divider (A10A2) divides down the -1.8 kv potential from the High Voltage Power Supply (A13) for use on the control elements in the Monoscope CRT.

The following adjustment potentiometers are mounted on the voltage divider:

1. INTENSITY (R1) controls Monoscope control grid XV1-2.
2. FOCUS (R4) controls Monoscope focus grid XV1-5.

## Video Preamplifier, A10A1 (Refer to Dwg. 2165479 Sht. 2.)

The function of the Video Amplifier is to amplify the video microvolt pulses from the Monoscope signal plate (or target) to a millivolt level for application to the Video Driver (A12) located in the display circuits section of the VDT. The circuit consists of a series of four high-frequency capacitive coupled amplification stages (Q1 through Q4), and an output emitter follower driver stage. There are no gain adjustments on the Video Preamplifier.

### 3.6 VIDEO DISPLAY CIRCUITS SECTION (Refer to Figure 3-23.)

The display circuits section consists of a Video Driver (A12), a Deflection Amplifier (A9), a Tickler Coil Driver (A11), and a Dynamic Focus Network (A20). These units provide the video, deflection, tickler scan, and dynamic focus correction for the Viewer cathode-ray tube. A block diagram of the video Section is shown in Figure 3-23.


Figure 3-23. Video Circuits, Block Diagram

### 3.6.1 VIDEO DRIVER, A12 (Refer to Dwg. 2165479, Sheet 2.)

The function of the Video Driver (Figure 3-24) is to amplify the video from the Video Preamplifier (A1OA1) and apply it to the Viewer CRT control grid (XV1-2). Additional circuit inputs from the resistor logic (A3) control brightness and parity error. A mark video input, from the Tickler Coil Driver (All) supplies the mark video.

A separate circuit provides amplification of the MONOSCOPE SWEEP GATE (MSG) from the Timing Logic (A5) for use in the Video Driver (A12) and also the Selection Amplifier (A8). The zener power supply furnished a +55 volt reference for use on the CRT brightness and focus controls.

## Character Video Input

The selected character video from the Video Preamplifier (A1OA1) is applied to a differential amplifier (Q1 and Q2) and capacitively coupled from emitter follower Q3 to drive a second differential amplifier (Q5 and Q8). The input to the second differential amplifier is quantized by clamps CR2 and CR3.

## Character Unblank

The CHARACTER UNBLANK signal from the register logic is applied through transistors Q4 and Q6 to control the collector of Q8. During character blanking, emmitter follower Q6 conducts and inhibits the video output of Q8. When the characters are not blanked (character unblank mode), the amplified video is applied through forward biased diode CR5 to emitter follower Q11 and to a second transistor NOR configuration (Q9 and Q10).


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Figure 3-24. Video Driver, Simplified Schematic

## Index Mark and Parity Blank

Transistor Q10 controls the application of the mark video from the Tickler Driver while $Q 9$ controls the parity error signal from the register logic. When a parity error occurs, $Q 9$ will cause the video level to increase to a full-brightness level, which forces the display of a white character block that blocks presentation of the faulty character video. The output of Q11 is applied to a complementary pair (Q14 and Q15) which may be blanked by the application of the MONOSCOPE SWEEP GATE (MSG).

Monoscope Sweep Gate (MSG)
The MONOSCOPE SWEEP GATE from the timing logic is applied to a dual amplifier circuit consisting of Q7, Q12, and Q13. The output of Q13 is used in A8 in the Monoscope Character Selection Amplifier. The output of Q12 is applied to the input of the complementary pair Q14 and Q15. During repositioning of the Monoscope electron beam (when a new character is slected), MSG forces amplifier Q14 into cut-off to prevent spurious video signals, which are generated during repositioning, from being displayed.

## CRT Drive Network

The composite video signal developed across resistor R 39 by the complementary pair (Q14 and Q15) is applied as the base drive to Q18. The collector of Q18 controls the current supplied to $Q 17$ which generates the video signal that is directly coupled to the Viewer CRT control grid XV1-2.

## Viewer CRT Brightness Control

The format brightness gate from the register logic is applied to a circuit consisting of Q16 and Q19, potentiometer R43, and zener CR1O. The function of the circuit is to cause all format characters to be displayed at a brightness level approximately one-half that of the variable data. The zener, CR10, generates a +55 volt reference level for the format brightness circuit and also is applied to the Viewer CRT INTENSITY and FOCUS controls available to the operator on the Viewer front panel.

When a format brightness gate is applied to the base of $Q 16$, the transistor is cut-off allowing $Q 19$ to conduct and shunt a portion of the current available to the CRT drive network. The result is a format character of less intensity than the variable data. The brightness of the format characters may be set by adjusting R53 FORMAT BRIGHTNESS ADJUST.

### 3.6.2 DEFLECTION AMPLIFIER, A9 (Refer to Dwg. 2165479, Sheet 3.)

The Deflection Amplifier is a dual channel unit containing both the horizontal and vertical Deflection Amplifiers. The unit is mounted behind the Viewer front panel on the left side (operator's right), and all adjustment potentiometers are available to the operator at the adjustment panel on the front of the Viewer.

The two amplifier channels are similar with the exception that the horizontal amplifier has an additional protection circuit fused to disable the High Voltage Power Supply (A14).

## Vertical Deflection Amplifier (Refer to Figure 3-25.)

The positive Vertical Sync pulse from the timing logic is applied to the base of transistor Ql4, driving the transistor into full conduction and cutting off Ql6. This allows capacitor C8 to charge linearly from a constant current source provided by Ql5 and the VERT GAIN potentiometer R38. The resulting ramp is applied to a pair of emitter followers (Ql7 and Ql8). The output of Ql8 is a zero to +8 volt ramp which is applied to the output amplifiers, Q21 through Q26, and to the voltage sensing circuit.

## Voltage Sensing Circuit

Transistor Q19 senses the voltage level of the vertical sweep ramp generated by Q18. When a logic failure occurs during vertical sync time, the ramp will increase above +8 volts. When a +9 volt level is reached, transistor $Q 19$ has enough current drive to force Q20 into conduction. This clamps the Q18 output ramp to ground potential until the logic failure is removed. The clamping action of Q20 prevents an excessive ramp signal from causing extreme current conduction through the vertical deflection coil and the output transistor Q26.

## Output Amplifier Circuit

The zero to +8 volt ramp from Q18 is first mixed with the horizontal sweep through R57, and then amplified by transistors Q21 through Q26. Q25 and Q26 act as a class AB push-pull amplifier. Zero crossing distortion is avoided by the bias provided by CR20 and CR21. The resulting current waveform through the vertical winding is a stairstep ramp varying from +1 ampere to -1 ampere.

## Note

+1 ampere deflects the Viewer CRT beam to the top of the screen raster. During the 20 line scan, the current level decreases in a stairstep fashion to -1 ampere at the bottom of the page (last line).

## Vertical Centering

The vertical centering potentiometer R56 (labeled VERT CTR) adjusts the bias voltage applied to the output differential amplifier (Q25 and Q26), enabling the operator to shift the reference point of the output current waveform about the zero volt index to center the Viewer raster vertically on the CRT screen.

## Retrace Flyback

At tne end of page time (end of last line of the display raster), the vertical sync pulse from the timing logic goes negative, cutting off transistor Q14 and forcing Q16 into conduction to provide a current shunt to immediately discharge capacitor C8. The ramp output of $Q 18$ is dropped to ground level and the current through the vertical deflection coil is driven to +1 ampere and deflects the Viewer CRT beam to the top of the display raster.


## Horizontal Deflection Amplifier

The horizontal deflection amplifier channel of A9 is similar to the vertical channel, however, the sweep speed is 1200 Hz compared to the 60 Hz frequency of the vertical channel.

The horizontal sync pulse from the timing logic is applied to input transistor Q1, which conducts to place a ground level on the base of Q3. This allows the constant current source consisting of the HORIZ GAIN potentiometer, R4, and transistor Q2 to drive the emitter follower pair (Q4 and Q5). The voltage sensing circuit (Q6 and Q7) functions to protect from any overvoltage condition in a manner identical to the voltage sensing circuit in the vertical channel. The output amplifiers, Q8 through Q13 function identical to the vertical channel output amplifiers and drive the horizontal deflection coil.

A second output is applied to the linear amplifier in Dynamic Focus (A20) to generate the Viewer CRT focus compensating voltage. The HORIZ CENT potentiometer controls the bias on the output differential amplifiers (Q12 and Q13) and centers the display raster horizontally.

Sweep Loss Protection Circuit
A 1.2 KHz output is tapped off through CR12 and applied to the High Voltage Power Supply (A13) as safety interlock to prevent damage to the Viewer CRT phosphor when a failure occurs in the horizontal sweep.

## Nofe

Loss of the horizontal sweep would cause the electron beam to sweep at the slow vertical rate of 60 Hz in the same area of the CRT tube face and could burn the phosphor coating.

The l.2 KHz sweep loss is applied to a voltage doubler circuit (CRIl andCR12 and associated components) and then applied to a transistor switch in the HVPS (Al3). The voltage holds the transistor base negative, cutting off the switch. When sweep failure occurs, the switch conducts, grounding the protection network. This causes all of the HVPS outputs to decrease to zero volts which turns off the Viewer CRT electron beam, preventing damage to the tube's phosphor coating.

### 3.6.3 DYNAMIC FOCUS NETWORK, A2O (Refer to Dwg. 2165479, Sheet 3.)

The function of the Dynamic Focus Circuit is to provide horizontal beam sweep compensation necessary to maintain correct focus of the CRT throughout the full horizontal sweep. The voltage potential on the focus grid must be varied to compensate for the varying focal length of the scanning beam to the flat face of the CRT.

## Dynamic Focusing

The horizontal sweep ramp voltage generated in the Deflection Amplifier (A9) is symetrical about a zero volt reference level, and is applied to linear amplifier Ql through back-to-back diodes CR1 and CR2 (Figure 3-26).


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Figure 3-26. Dynamic Focus, Simplified Schematic

The resultant collector output of $Q 1$ is a symetrical triangular waveform of 75 volts. The corrective signal is applied through capacitor C3 to the focus grid of the Viewer CRT (XVI-6). The triangular compensating signal alters the focus grid potential at both extremes of the horizontal sweep to provide dynamic focusing.

### 3.6.4 TICKLER DRIVER, All (Refer to Dwg. 2165479, Sheet 1.)

The input to the Tickler Driver is a $4.9 \mathrm{v}, \mathrm{l} .5 \mathrm{MHz}$ square wave generated on A5, the Timing Logic card (Figure 3-27).

The Tickler Driver generates three output signals:

1. The Mark Video (to Video Driver, Al2)
2. The Vertical Scan Input (to Selection Amplifier, A8)
3. Tickler Frequency Drive (to Viewer CRT Tickler Coil)

The 1.5 MHz Tickler Frequency input is applied to the base of transistor Ql which drives Q2. The output of $Q 2$ is clamped by CRl and amplified by transistors Q3 and Q4. The 10 volt square wave output of Q4 is applied to a double pi low pass eliptical filter which eliminates low frequency distortion. The filter output is a 1.5 MHz sine wave which is amplified by Q5 and Q6. The emitter output of Q6 (a four volt sine wave) is applied to the Selection Amplifier (A8) as the vertical scan input for use by the Monoscope tube.

## Mark Unblank Circuit

The 1.5 MHz sinusoidal output of $Q 6$ is also capacitively coupled to the mark unblank circuit, consisting of inverter Q7 and gate transistors $Q 8$ and $Q 9$. When the mark unblank signal from the register logic is applied, gate $Q 9$ is cut off, enabling gate Q8. The resulting peak detected mark video is applied through CR4 to the Video Driver (A2).

## Viewer CRT Tickler Circuit

The 1.5 MHz output of Q 6 is applied to a third circuit which generates the Tickler drive for the CRT Tickler coil.


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## Constant Amplitude and Phase Adjust

The phase adjust circuit permits phasing the Viewer CRT Tickler to sync with the vertical sweep of the Monoscope tube. The 1.5 MHz sine wave is capacitively coupled to the base of transistor QlO.

The PHASE COARSE ADJ potentiometer, R26, is also connected to the base of Qlo.

## Nofe

The PHASE COARSE ADJ. (R26) is connected in series with the PICTURE potentiometer, R73, located in the Deflection Amplifier (A9).

## Tickler Phase Balance Adjust

The Tickler Phase Balance Adjust is necessary to compensate for the phase lag between the 1.53 MHz tickler sine wave applied to the Viewer CRT tickler coil and the amplified video applied to the Viewer CRT control grid. Phase differences of more or less than 180 degrees will cause portions of the displayed character to be written at slightly different vertical locations on adjacent page times, making the horizontal portions of the character appear double on the viewer screen. The operator can correct this condition by adjusting the PICTURE potentiometer, R73, located at the left side of the viewer panel (operator's right).

## Note

The PICTURE potentiometer, R73 is physically located on the Deflection Amplifier (A9); however, it is connected in series with the Tickler Driver PHASE COARSE ADJ, R26, located on All (Figure 3-27).

The emitter of $Q 10$ is connected to the GAIN ADJ potentiometer, R31, which controls the height of the characters displayed on the Viewer CRT.

## High Gain Feedback Amplifier

Transistors Q13 through Q17 comprise a high gain amplifier which is coupled through diodes CR5 and CR6 to a push-pull stage (Q18 and Ql9).

The Tickler signal is then capacitively coupled to Q20, the coil driver, which applies the 1.5 MHz Tickler signal to the Viewer CRT Tickler (Minor) deflection coil. The CRT Tickler coil is shunted by capacitor C24 to cause the coil to resonate at the Tickler frequency to minimize the drive power required. When the Tickler output for the Viewer CRT is synchronized with the Tickler used in the Monoscope tube, the character displayed on the Viewer will duplicate instantaneously the character scanned on the Monoscope character stencil.

## Phase Laq-Neqative Feedback Network

The phase-lag network (resistors $R 63$ through 66) provides negative feedback to amplifier Q13. The feedback provides stability for the amplitude adjusted 1.5 MHz sine wave and also minimizes phase/wave distortion due to temperature variations and circuit component aging.

### 3.7 INPUT/OUTPUT CIRCUITS (Refer To Figure 3-28.)

In order to understand the I/O logic explanation in the following paragraphs it is necessary to know the definitions and functions of the mnemonics listed in Table 3-2.

### 3.7.1 INPUT/OUTPUT CONTROL LOGIC

The input-output mode counter sequence is shown in Figure 3-29 and Figure 3-30. The signals necessary for the $I / O$ logic to cause the mode counter to advance sequentially through the states (zero through 15) are given both for the basic $70 / 752$ VDT and for the printer adapter option (when installed).

The Input/Output control logic is contained on two logic boards, I/O1 and I/O2. (Refer to logic diagrams 2144559 and 2144560. ) The logic controls the transfer of data from and to the central computer and also controls the operating mode of the Video Data Terminal. The mode controlling circuit is the I/O Mode Counter. The I/O Mode Counter consists of four triggerable flip-flops and the required decoding gates. The four flip-flops, IOMC1 through IOMC4, control the transmission and reception of data by decoding counter states IOMO through IOM15. The IOM counter may be reset to zero at any time by pressing the WRITE switch. When the IOM count of zero (IOMO) is decoded, the Video Data Terminal is in the Write mode. In this mode the I/O logic is inactive and the manual controls are enabled. The IOM counter is advanced when the conditions required for advance are satisfied, on the trailing edge of BT 9 A .

## IOMO

When the XMT (Transmit) switch is pressed, gate $60 \mathrm{D} 5 \mathrm{~A}-1$ is enabled at the next BT7A if there is an ETX character in the Display Register (ETXDR). The output of this gate (TRIOMC3 or IOMC3ADV) will trigger the IOMC3 flip-flop producing count IOM4. The counts IOM1, IOM2, and IOM3 are used only when the Station Select special feature is installed. (Refer to Figure 3-30.)

IOM4 and IOM5
The counts IOM4 and IOM5 are not used in the basic Video Data Terminal, and the next two BT9A pulses from 60A8C-2 (TIOMC) advance the IOM Counter to IOM6.

IOM6
The count IOM6 is used to ensure that transmission will start at the beginning of the message. This mode count will last until BT9A of the 58th character of the last line (at the end-of-page pulse). The purpose of this delay time is to provide a fixed reference point for start of transmission. The EOP pulse will generate the TIOMC (TRIGGER IO MODE COUNTER) pulse to advance to IOM7.


Table 3-2. Input/Output Mnemonics

| MNEMONIC | DEFINITION | FUNCTION |
| :---: | :---: | :---: |
| IOM | INPUT OUTPUT MODE COUNTER | CONTROLS SEQUENCE OF TRANSMIT AND RECEIVE MODES |
| TIOMC | TRIGGER IO MODE COUNTER SEE 60A8C-2 | ADVANCES THE IOM COUNTER |
| STX | START OF TEXT | SHIFTS INTO TR REGISTER TO START XMIT OR RECEIVE. |
| TRT | TR TRIGGER CONTROL |  |
| AT (OP ) | TR REGISTER CONTENT INDICATOR $\mathrm{F} / \mathrm{F}$ | INDICATES TR REGISTER IS EMPTY |
| XMTF ( P ) | TRANSMIT MODES |  |
| XMT | TRANSMIT |  |
| IOBP | I/O BEGINNING OF PAGE |  |
| EOP | END OF PAGE | ADVANCES IOM COUNTER TO IOM9 |
| Z IM | ZERO INDEX MARK | PLACES INDEX MARK AT START OF <br> FIRST LINE AND ERASES ANY OTHER <br> INDEX MARKS ON PAGE. |
| B1 | B1 BUFFER REGISTER |  |
| B2 | B2 BUFFER REGISTER |  |
| TR | TRANSMIT REGISTER |  |
| ETX | END OF TEXT | WHEN DETECTED, GENERATES TIOMC TO ADVANCE IOM COUNTER |
| IOMC575 | IOM COUNT 575 | PRODUCES TIOMC TO ADVANCE IOM TO IOM11 AND IOM12 |
| RCVDATA | RECEIVE DATA | SIGNAL FROM DATA SET ENABLED BY IOM12 |
| A1 (OP) | A1 FLIP FLOP OUTPUT | INDICATES B1 REGISTER IS EMPTY |
| A2 (OP) | A2 FLIP FLOP OUTPUT | INDICATES B2 REGISTER IS EMPTY |
| EAR | ERASE-AFTER-RECEIVE | CLEARS DELAY LINE REGISTER, <br> ADVANCES IOM COUNTER TO 000, <br> AND TRANSFERS VDT TO WRITE MODE. |

Table 3.2. Input/Output Mnemonics (Cont'd)

| MNEMONIC | DEFINITION | FUNCTION |
| :---: | :---: | :---: |
| SYNC | SYNC SIGNAL | CLEARS IOM COUNTER |
| TRO | TR REGISTER OUTPUT ZERO | MAINTAINS STOP SIGNAL AT DATA SET INPUT |
| CTS | CLEAR TO SEND (FROM DATA SET) | CLEARS TRO, ENABLES IO COUNTER TO GENERATE SLOW SHIFT PULSES SLSHX |
| SLSHX | SLOW SHIFT XMIT PULSES | USED TO SHIFT I/O REGISTERS AT 1200 BAUD DATA SET RATE DURING TRANSMIT |
| SLSHR | SLOW SHIFT RECEIVE PULSES | OCCUR IN MIDDLE OF BIT TIMES TO SAMPLE AND SHIFT RECEIVED DATA INTO TR REGISTER |
| DLRME | LAST STAGE OF DELAY <br> LINE REGISTER <br> (MARK EARLY F/F) | ENABLED BY DTB SIGNAL TO ENTER DATA INTO B1 BUFFER REGISTER |
| DTB | DISPLAY-TO-BUFFER F/F | ENABLED BY DTB SIGNAL TO ENTER DATA INTO B1 BUFFER REGISTER |
| BP1B | BIT PULSE 1B | BASIC TIMING PULSE 1B USED TO RESET DTB $F / F$ |
| XBNF | XMIT BUFFER NOT FULL | ENABLES DTB TO SHIFT IN DATA |
| ADV | ADVANCE | ADVANCES INDEX MARK ONE CHARACTER |
| ASK | ADVANCE OR STROBE KEYBOARD |  |
| KBS | KEYBOARD STROBE | GENERATED DURING KEYBOARD ENTRY OF DISPLAYED CHARACTERS, ADVANCES MARK ONE CHARACTER |
| MAG | MARK ADVANCE GATE | GENERATES ASK LEVEL TO RESET <br> DLRME F/F AND SET DLRMN TO <br> ADVANCE INDEX MARK ONE CHARACTER |
| DL RMN | FIRST STAGE OF DELAY <br> LINE (MARK NOW F/F) | SET DURING MARK ADVANCE OPERATION TO ADVANCE MARK ONE CHARACTER |
| B1T | B1 TRIGGER F/F | CONTROLS SHIFT PULSES TO B1 BUFFER REGISTER |
| B2T | B2 TRIGGER F/F | CONTROLS SHIFT PULSES TO B2 BUFFER REGISTER |

Table 3.2. Input/Output Mnemonics (Cont'd)

| MNEMONIC | DEFINITION | FUNCTION |
| :---: | :---: | :---: |
| TRT | TR TRIGGER F/F | CONTROLS SHIFT PULSES TO TR REGISTER |
| RCVT | RECEIVE MODES | ENABLES SENSING OF RECEIVED DATA AT INPUT TO TR REGISTER |
| RCV ( P ) | RECEIVE |  |
| BTD | BUFFER-TO-DISPLAY CONTROL | CAUSES CHARACTER IN B2 TO BE STORED IN DELAY LINE RATHER THAN CHARACTER IN DLR. ALSO ADVANCES MARK |
| RBNF | RCV BUFFERS NOT FULL | DURING RECEIVE MODE INDICATES <br> B1 AND B2 REGISTERS NOT FULL. |
| RCV DATA TO TR IN | REC. DATA TO TR INPUT |  |
| TBB | FAST SHIFT PULSES | USED TO SHIFT FROM AND TO DISPLAY DELAY LINE MEMORY AND TO FAST SHIFT I/O REGISTERS |
| B1IN | BUFFER 1 INPUT | DATA INPUT SIGNAL TO B1 BUFFER |
| IOCNT 575 | I/O COUNTER TIME 575 | INHIBITS INPUT DATA BY INHIBITING RCVT LEVEL |
| EOP | END OF PAGE | USED TO ADVANCE I/O COUNTER IOMO OR WRITE MODE |
| XMTR | TRANSMIT MODE |  |
| RBNF | RECEIVE BUFFER NOT FULL |  |
| TR8 (TRIN) | TRANSMIT/RECEIVE <br> REGISTER INPUT |  |
| STOP | STOP BIT $=$ "1" | WHEN IN TR REGISTER SIGNALS STOP TO DATA SET |
| BP2A | BIT PULSE 2A | SETS DTB F/F AT IOM9 IF XBNF AND MARK IS SENSED IN DLRMF FLIP FLOP |
| CRRCV | CARRIAGE RETURN RECEIVED | ADVANCES MARK TO BEGINNING OF NEXT LINE |
| SO | FORMAT ON | USED AS FORMAT CONTROL SIGNAL (NOT STORED) |

Table 3.2. Input/Output Mnemonics (Cont'd)

| MNEMONIC | DEFINITION | FUNCTION |
| :---: | :---: | :---: |
| SI | FORMAT OFF | USED AS FORMAT CONTROL SIGNAL (NOT STORED) |
| SFMC | SET FORMAT MODE CONTROL | USED TO SET A2 F/F |
| CFMC | CLEAR FORMAT MODE CONTROL | USED TO CLEAR A2 F/F |
| EOT | END OF TEXT | ADVANCES I/O COUNTER THROUGH RECEIVE SEQUENCE |
| PRT | PRINT MODE FLIP-FLOP |  |
| IRIOMC3 | IOMC 3 TRIGGER |  |
| IOMC3ADV |  |  |
| PCR | PRINTER CARRIAGE RETURN |  |
| PLF | FEED LINE RETURN |  |
| SAl | SET Al F/F | INDICATES BUFFER AI FULL |
| RNC | REQUEST NEXT CHARACTER | CLEARS Al F/F |
| CAl | CLEAR Al F/F |  |
| SA2 | SET A2 F/F | INDICATES BUFFER A2 FULL |
| XMTSW | XMT SWITCH PRESSED | USED IN LOGIC TO ADVANCE I/O COUNTER TO MODE 4 |
| ETX DR | END OF TEXT ENTERED IN DR |  |
| PRT | PRINT SWITCH OFF | USED IN LOGIC TO ADVANCE I/O COUNTER TO MODE 5 |
| EOP | END OF PAGE | USED IN LOG IC TO ADVANCE I/O COUNTER TO MODE 7 |
| IOBP | I/O BEGINNING OF PAGE | USED IN LOGIC TO ADVANCE I/O COUNTER TO MODE 8 |
| IOCNT 575 | I/O COUNT 575 | USED IN LOGIC TO ADVANCE I/O COUNTER TO MODE 12 |
| ZM | ZERO THE MARK | USED IN LOGIC TO ENSURE ONLY ONE MARK EXISTS ON PAGE |
| RS | REQUEST TO SEND (LEVEL) | MAINTAINS CARRIER FROM DATA SET TO CCM FOR 8 MILLISECONDS |

Table 3.2. Input/Output Mnemonics (Cont'd)

| MNEMONIC | DESCRIPTION | FUNCTION |
| :---: | :---: | :---: |
| FON |  |  |
| SFMC |  |  |
| F OFF | FORMAT OFF |  |
| B TDS CRRV |  |  |
| RNC | REQUEST NEXT CHARACTER |  |
| RD | RSD REG TO SEND FROM DATA SET |  |
| OC | STATION IDENTIFIER | ENABLES LOGIC TO IDENTIFY CENTRAL COMPUTER STATION CALL |
| TR TD | TR DATA TO DATA SET |  |
| DL | DELAY LINE |  |
| CR | CARRIAGE RETURN |  |
| LF |  |  |
| DLM | DELAY LINE MEMORY |  |
| FMCFF | FORMAT MODE CONTROL F/F | SET WHEN FORMAT BIT IS CONTAINED IN RECEIVED MESSAGE |
| FBI | FORMAT BIT INSERT GATE |  |
| FMRF | FORMAT MARK REMEMBER F/F |  |
| FIG | FORMAT MARK INSERT GATE |  |
| MESS | MARK EARLY SET STROBE |  |



Figure 3-29. IOM Sequencing For Basic Unit And With Printer Adapter


Figure 3-30. IOM Sequencing For Station Selector And With Printer Adapter

During IOM7, the STX character is shifted into the TR (Transmit/Receive register). The STX character is formed by combining BT3A and BT9A in gate 60B5D-2 to produce the character code 10000010. This signal is enabled by IOM7 and is shifted into the TR by TBB which is enabled by TRT (TRIGGER TR REGISTER). The TRT signal is produced by the TRT flip-flop when it is set by AT-OP (TR REGISTER EMPTY) and XMTF-P. This occurs at BT2A of character 59. The next BT3A places a "1" into the TR Register. Since TRT and TBB are shifting the TR Register, BT9A will put the eighth bit into the TR Register. At BT1OA the TRT flip-flop is reset and will be inhibited from being set again by the setting of the AT flip-flop. The AT flip-flop is set at BT3A of the 60th character. The IOM7 period is terminated after the XMT switch is released and the IOBP (IO BEGINNING OF PAGE) pulse occurs.

IOM8

IOM8 allows the STX character to be transmitted to the data set and the zero index mark function (ZIM) in the register logic is enabled for one page time. The EOP pulse advances the IOM counter to IOM9.

IOM9
IOM9 is the basic Transmit mode. Characters are transferred from the Delay Line Register under control of the mark to the B1 and B2 Buffer Registers and to the TR Register. The characters are then transferred to the data set under control of the IO timing which will be discussed later. Transferring the ETX character to B1 generates the TIOMC signal to advance the IOM Counter.

## IOM10

IOM1O enables the ZIM operation again and the remaining characters in the $\mathrm{B} 1, \mathrm{~B} 2$, and TR Registers are transmitted. When the registers are empty, indicated by A1-OP, A2-OP, and AT-OP, gate 60C8A-2 will generate the TIOMC signal to advance the IOM Counter at IOCNT575.

## IOM11

IOM11 maintains the REQUEST-TO-SEND (RS) level. ZIM is also enabled to ensure that the ZIM operation lasts at least one page time. This is accomplished by allowing the IO Counter to count for an additional 640 counts (one I/O character time). At count 575, gate 60C7B-2 produces the TIOMC signal and advances the IOM Counter to IOM12.

IOM1 2
The IOM12 mode enables the RCVDATA signal to be generated from the data bit pulses from the data set. The IOM12 mode lasts until the STX character is detected in the TR Register by gate $60 B 6 C-2$, generating the IOMC signal and advancing the counter to count IOM13.

IOM13

IOM13 is the basic Receive mode. The data is still enabled by RCVT-P and is shifted under control of IO timing into the $T R$, to the B1, to the B2 Registers, and to the delay line under control of the mark logic. When the ETX character is detected in the TR Register, the TIOMC signal is again generated to advance the counter to IOM14.

IOM14
This period allows the characters contained in registers $T R, B 1$, and $B 2$ to be shifted into the Delay Line Memory. When the A1-OP and A2-OP signals occur, indicating that the buffer registers are empty, the TIOMC signal advances the IOM Counter.

## IOM15

The IOM15 period enables the erase operation to erase the remainder of the page. This is accomplished by generating the EAR (ERASE AFTER RECEIVE) signal. This signal will hold the Delay Line Register cleared until the EOP pulse advances the IOM Counter to count.0000. This will transfer operations back to the write mode and enable the operator to compose another message.

### 3.7.2 INPUT/OUTPUT TIMING CONTROL

The I/O timing is a function of the basic Video Data Terminal timing. (Refer to logic diagram 2144559.) Each transmitted or received character consists of 10 bits; 1 start bit, 7 data bits, 1 parity bit, and 1 stop bit. The transmission and reception rate is 1200 bits per second, or 833 microseconds per input/output bit. This period is regulated by the IO Counter consisting of flip-flops IOCO through IOC9. Flip-flops IOCO through IOC5 count from $76,8 \mathrm{KHz}$ (triggered by BT1A) and repeat every 833 microseconds. Flip-flops IOC6 through IOC9 count the number of input/output bit times until the counter is cleared by the SYNC signal. A timing diagram of the counting states of the 10 Counter is shown in Figure 3-31. The SYNC flip-flop (59A7B-2) controls the IO Counter operation. When the SYNC flip-flop is set, the IO Counter is cleared and triggering is inhibited by gate 59A8A-1.

Initially TRO (60D4A-2) is in the set state maintaining the STOP level to the data set. When a character is ready to be transmitted, gate 60B3A-2 clears TRO to initiate the START bit. This requires that the CTS (CLEAR TO SEND) signal from the data set is high, that there is a character in the TR Register (AT-1P), and that transmission of the previous character, if any, has been completed (SYNC-1P). Clearing TRO permits gate 59B6C-2 to clear the SYNC flip-flop and to enable the IO Counter. The IO Counter generates the SLOW-SHIFT PULSES (SLSHX) from gate $59 \mathrm{C} 7 \mathrm{C}-2$ to shift successive bits of the character into TRO. The SLSHX pulses also shift "1's" into TR (60A6A-2) so that the ninth shift pulse shifts the STOP bit into TRO. IOCNT640(59B7A-2) sets the SYNC flip-flop after the tenth bit.

A SLOW SHIFT PULSE is generated every 833 microseconds as shown in Figure 3-31. When transmitting, SLSHX pulses occur at the end of each I/O bit time as they supply successive bits to the data set. When receiving, SLSHR pulses occur in the middle of each bit time to sample the received data and shift successive bits into the TR Register. The first character shifted out of the TR Register is the


STX character. The output of DLRME, the last stage of the Delay Line Register, is enabled through gate 59D3B-2 by the DTB (DISPLAY TO BUFFER) signal and applied to the B1 Buffer Register. The CTB signal is produced by setting the DTB flip-flop when any output register is empty during IOM9 and the mark occurs. This will allow the code for one character to be transferred to the B1 Register. If the $B 2$ or $T R$ Registers are still empty, the DTB flip-flop, although reset by BP1B, may be set again until two more characters have been shifted to the Bl Register, placing the first character transferred in the $T R$ Register. At this time the XBNF (XMT BUFFER NOT FULL) signal will not be present and the DTB flip-flop will remain reset.

Three character codes are now contained in the buffer registers. These three characters were selected by the mark, previously placed in the first character, first line position by the zero index mark operation. The DTB signal is maintained for one half bit time after each character is shifted out of the DLR. It will perform the same function as the ADV (ADVANCE) or KBS (KEYBOARD STROBE) signals and will advance the mark one character. The mark is sensed in DLR1 by gate 57C4B-1 which sets the MK (MARK) flip-flop during the DTB signal. The MK flipflop and MAG (mark advance gate) generate the ASK level (57B7C-2) which will reset the DLRME flip-flop and will set the DLRMN flip-flop moving the mark to the next character position. This sequence of operations is repeated each time a character code is shifted into the buffer registers.

### 3.7.3 INPUT/OUTPUT BUFFER CONTROL

The Buffer Registers B1, B2 and TR (refer to logic diagrams 2144559 and 2144560) are monitored by the A1, A2 and AT flip-flops, respectively. These flip-flops indicate whether the registers are full (contain a character) or empty. During the XMT operations if B1 and B2 Registers are full and the TR Register is empty, the $B 1 T$ and $B 2 T$ flip-flops will be set to allow the registers to be shifted. The TRT flip-flop will also be set to allow the TR Register to be shifted to accept the character from the B2 Register. The logic is formed so that when a register is empty, the previous registers are shifted. For example, if B2 is empty and $T R$ is full, only registers $B 1$ and $B 2$ will be shifted; if only $B 1$ is empty, the A2-1P and AT-1P signals will inhibit setting the B2T and TRT flip-flops so that the B2 and TR Registers will not be shifted.

The above operations will continue until the WRITE switch is pressed or until the ETX character is transferred to B1. At the time the ETX character is transferred, the IOM Counter is advanced to IOM1O and the remaining characters in the B1, B2, and TR Registers are transmitted. When IOM9 is completed, the DTB flipflop may not be set; this prevents further transfers from the Dealy Line Register. When all buffer registers are empty, the IOM Counter will be advanced to IOM11. The IOM11 period allows the mark to be reset to the beginning of the page and maintains the REQUEST TO SEND (RS) level to the data set to ensure transmission of the last character. At the end of this period the IOM Counter is advanced to IOM12 to enable the Receive mode. The RCVT signal, generated by IOM12 and IOM13, enables the received data to be sensed at the input of the TR Register and enables the SLSHR pulses to shift the data into the TR Register. When the STX character is detected in the TR Register, the IOM Counter is advanced to IOM13, which is the basic Receive mode.

The IOM13 level enables the RCV level so that BTD (BUFFER TO DISPLAY) flip-flop may be set. Since the RCV-P signal is not generated in IOM12 by gate 60B7D-1 enabling the BTD flip-flop to be set, the STX character is not shifted to the Delay Line Memory. The BTD signal enables the B1T and RBNF (Receive mode and A1 or A2 buffers not full) signals. Therefore, while a character is being presented to the input of TR Register (RCVDATA to TRIN) the SLSHR-N pulses from the Io Counter will set the TRT flip-flop. The TRT flip-flop is reset between each character time by BT10A. The TR Register is full when the AT flip-flop is set by IOCNT575 and BT9A. The character is then shifted out of the TR Register by TRT and TBB (fast shift pulses) to the B1 Register as the B11N (BUFFER 1 INPUT) signal. When the character is in the B1 buffer, the B1T flip-flop is set. Since the $B 2$ buffer is not full, the absence of the B2T level enables the character to be shifted to the B2 buffer and the B2T flip-flop is set.

## Shift Pulse Control

The content of B 1 is shifted by the leading edge of TBB when the B1 TRIGGER CONTROL (B1T) is set. B1T is set by BT2A in any XMTR mode if B1 or B2 or TR is empty (XBNF-XMT Buffer Not Full). During RCV, B1T is set if B1 or B2 is empty or if the character in $B 2$ is being transferred to the Delay Line (RBNF-RCV Buffer Not Full). B1T is always cleared by BT10A. This applies 8 shift pulses to B1 during every character time unless B1 contains a character which cannot be transferred to B2.

The content of $B 2$ is shifted by $T B B$ when $B 2 T$ is set. $B 2 T$ is always cleared by BT10A and is set by BT2A if B2 is empty or if the BUFFER-TO-DISPLAY transfer (BTD) is initiated or, in XMTR modes, if TR is empty. This applies 8 shift pulses per character time unless $B 2$ contains a character which cannot be transferred to the display or to TR.

The content of $T R$ is shifted by TBB when TRT is set. TRT is always cleared by BT1OA, and in any XMTF mode, is set by BT2A if TR is empty. This enables the fast shift of 8 pulses per character time. When a character has been transferred into TR, the slow shift output control is enabled as described in paragraph 3.7.2. Each SLSHX pulse shifts TR1 into TRO, forces a "1" on the input of TR8 (TRIN), and sets TRT. Since SLSHX occurs at BT9A, only one shift pulse occurs each time TRT is set. At the ninth SLSHX (IOCNT575), the STOP bit is in TRO and TR is, by definition, empty. The next BT2A will set TRT and, if $B 2$ is full, TR will be refilled immediately.

In any RCVT mode, the slow shift input is enabled by receipt of a START bit (the first zero bit of a character). Each SLSHR pulse sets TRT to shift successive data bits from the processor into TR. At the ninth SLSHR (IOCNT543), TR contains the complete 8-bit character and IOCNT 575 sets the TR Full indicator (AT). If $B 1$ or $B 2$ are empty, $B T 2 A$ will set $T R T$ to transfer $T R$ to $B 1$ and $B T 8 B$ will clear AT.

## Data Transfer

The DISPLAY-TO-BUFFER control (DTB) is set at BT2A in IOM9 if the buffer is not full (XBNF) and if the DLR contains the character with the mark. (Note that the mark is in flip-flop DLRF at BT2A. DTB gates the DLR output (ME) into B1 and also activates the mark advance. DTB is cleared by BT1B. Since the mark is advanced each time, DTB will be set again to transfer successive characters until the buffer is full. The BUFFER-TO-DISPLAY control (BTD) is set at BT1B in IOM13
or IOM14 if B2 is full and if the DLR contains the mark. BTD causes the character from B2 instead of the DLR to be stored in the Delay Line Memory. BTD also activates the mark advance so that all characters in the buffer can be stored. Recognition of a Return character in B2 (CRRCV) modifies the mark advance.

## Buffer Control

The status of Bl (full or empty) is indicated by flip-flop A1. Initially, A1 is cleared by IOMO. A1 is set when buffer B1 is filled and cleared when B1 is emptied. During XMTR, when a character is being transferred from the DLR to B1 (DTB), BT7A sets A1. When the character in B1 is transferred to B2, BT7A clears A1 unless another character is being transferred during the same character time from DLR to B1 (B1T and not DTB). Since NULL characters are not to be transmitted to the processor, $A 1$ is cleared by BT10A when a NULL is recognized in B1. In RCV, BT7A sets A1 when a received character is being transferred from TR to B1 (B1T and not AT).

B2 status is indicated by A2. Initially, A2 is set by IOMO. This simulates B2 full to enable shifting the STX code into TR during IOM7. A2 is cleared at the end of IOM7 (CA2) to prepare for normal operation. BT5A sets A2 if B1 is full (A1) and clears A2 if B1 is empty and the character in B2 is being transferred to TR or to the display (B2T and not A1). Since SO (Format On) and SI (Format Off) codes are used with the Format feature for control only, and are not to be stored in the delay line, A2 is cleared by the control signal (SFMC or CFMC) generated at BT1OA when either code is recognized in B2.
$T R$ status is indicated at AT. AT is cleared initially during IOMO. During XMTF, BT3A sets AT if $B 2$ is full (A2). BT4A clears AT after the last bit of the character has been transmitted (IOCNT575). During RCV, BT9A sets AT after the complete character has been received (IOCNT575). BT8B clears AT when the character is transferred to B1 (B1T).

### 3.8 SPECIAL FEATURES

The following paragraphs describe Special Features available for installation in the $70 / 752$ VDT. All of the Special Features are compatible with three exceptions. When the Data Format Special Feature is installed, the Standard Data Insert Feature is removed due to changes in the logic. When the Local Operation Feature is installed, the Station Select Feature cannot be installed. When the Flexible Array Special Feature is installed, the Printer Adapter cannot be installed.

### 3.8.1 STATION SELECT, SF 5707

The Station Select Special Feature (logic diagram 2144665) enables reception of a message from the Central Processor only when the correct Station Identifier is sent to the Video Data Terminal to receive it. This process is used when a number of Video Data Terminals are to communicate with the Central Processor via a common line.

When there is no message to transmit, the Video Data Terminal is in the Write mode or IOMO (Figure 3-30), the RCVT level is enabled, and the AT flip-flop is cleared. The receive sequence consists of an EOT character and the Station Identifier. The receipt of the EOT character advances the IO mode counter to IOM1. If the next character is not the correct Station Identifier the IO Mode Counter is reset to IOMO. If the character following EOT is the correct identifier, the IO MOde

Counter is advanced to IOM2. During IOM2, the EOT character code is shifted into the TR Register and transmitted to the Processor. When transmission of the EOT character is complete, the IO Mode Counter is advanced to IOM3. The IOM3 mode maintains the RS level to the Data Set for an additional 8 milliseconds and then resets the IO Mode Counter to IOMO.

When there is a message ready for transmission and the XMT switch has been pressed, the IO Mode Counter is advanced to IOM4. When the EOT character is received from the Processor IOM5 is enabled. The IOM5 mode is used to detect the correct Station Identifier and advance the IO Mode Counter to IOM6. If the letter received is not the correct Station Identifier, the IO Mode Counter is returned to IOM4. The modes IOM6 through IOM15 are the same as those of the basic Video Data Terminal.

### 3.8.2 PRINTER ADAPTER, SF 5711

All basic operations are the same as in the basic or Station Selector Special Feature equipped models. (Refer to logic diagram 2144570.)

The Printer uses IOMC3 and IOMC4 as a two-bit counter to generate the four modes necessary for its operation. When the Print flip-flop (PRT) is set, the IOMC3 trigger (TRIOMC3) is isolated from IOMC3ADV and is controlled only by the Printer logic. With the Station Select Feature, IOMC1 and IOMC2 are used as an independent two-bit counter (if PRT is set) for the automatic recognition and response function as described for IOMO through IOM3.

IOM Advance control is inactive when PRT is set except for the gates used in automatic operation of the Station Select Feature.

The data interface with the Printer is through the B1 buffer register. Characters are transferred to the B1 buffer from the DLR under DTB control upon request of the Printer logic. The Printer Carriage Return (PCR) and Line Feed (PLF) character codes are shifted into the Bl buffer as controlled by the Printer logic. The B2 buffer register is not used in the Print mode. The TR Register is used only for the automatic functions of the Station Selector Feature. The transfer of data within the unit is essentially the same as in the basic unit; IOM9A is activated by PRT and IOM8; and XBNF (TRANSMIT BUFFERS NOT FULL) depends only upon the status of B1. Buffer Control flip-flop A1 is set by the Printer logic (SA1) to permit PCR and PLF to be generated before any display characters are printed. A1 is cleared by RNC to request the next display character, and set again by DTB. Buffer control flip-flop A2 is set by PRT, indicating that $B 2$ is always full (for the benefit of XBNF). Since AT must be used by the Station Select function, the AT input to XBNF (ATA) is held high by PRT.

NULL recognition in B1 is used by PRT to set B16 (space code) instead of clearing A1 so that the printed copy will be the same as the display.

When the Printer Feature is not used, the Printer logic is replaced by jumpers to interconnect the necessary lines (such as IOM9 to IOM9A and $+4.5 v$ to RNC).

### 3.8.3 DATA FORMAT, SF 5710

Each character stored in the DLM includes as one of its bits a format bit. This identifies the character as a format character when the bit is logical "1" or set, and as a variable character when the bit is cleared, "0".

When the Format option is installed, control of format is accomplished by the computer (logic diagram 2144567). As a message is received, Format ON/OFF is decoded in the IO logic and the results forwarded to the mark and control logic. When the received message contains a format, the Format Mode Control flip-flop (FMCFF) is set. It is used to enable received data format bit sensing logic, Format Bit Insert gate (FBI).

FMRF is used when a Control Panel command (advance, for example) was attempted, generating MESS. If MESS occurred with a format bit present in the character, DLRF inhibits setting the mark now flip-flop, signal SETMN. When MESS is generated in the presence of a format character, FMRF is set, enabling the format insert gate FIG. BT108-P is ANDed with the FMRF and the format bit DLRF-1N which tells us when a non-format character is in the DLR. Also present is flyback inhibit FMI to prevent mark entry during the flyback time. Thus, the new mark will be written in the first character position after a format character when an ADVANCE is received.

### 3.8.4 LOCAL OPERATION AND KEYBOARD EXTENSION

The addition of the Logal Operation and Keyboard Extension Special Feature produces no change in logic operations. When the Local Operation feature is installed, the Station Selector Feature may not be incorporated.

### 3.8.5 FLEXIBLE CHARACTER ARRAY, SF 5734.01

The function of the Flexible Character Array Feature is to permit the display format to be changed from the standard array of 20 lines each having 54 characters to the desired array. This is done by installation of jumpers on the alternate A5 Timing Board. Table 3-3 lists the jumpers necessary for connectors P1 and P2 to obtain the various alternate array formats. Figure 3-32 shows a block diagram of the Flexible Display Array Logic.

> Note
> Changing the number of lines and characters per line requires readjustment of the Deflection Amplifier (A9) to obtain the proper horizontal sweep length for the selected array format.

When the Flexible Character Array Feature is to be installed in a V.D.T having a RCA High Voltage Power Supply, a new High Voltage Driver Board (A1), Drawing No. 2150231-502 must be used in this power supply. Failure to install this board will result in damage to the power supply.

To operate the Flexible Character Array (SF 5734-01) and the Printer Adapter (SF 5711) when both are installed in the same V.D.T. requires the addition of
the Timing Mod Kit \#2112926.

## Variable Array Limit

The number of variable arrays is limited by the total bit storage of the Delay Line Memory, which is 12,800 bits. The maximum number of lines that can be displayed is 32 lines with 30 displayed characters per line for a total of 960 displayed characters. When maximum line length is desired, a raster of 14 lines with 81 displayed characters per line is available. Other arrays within these two extremes are determined by the formula:

NO. OF LINES = 1280
(Whole lines only)
CHARACTERS PER LINE +10


Table 3-3. Flexible Array Jumpers

| FLEXIBLE ARRAY FORMATS |  | CONNECTOR P-1 PIN NUIMERS |  |  |  |  |  |  |  |  |  |  | CONNECTOR P-2 PIN NUMBERS |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CHARACTERS <br> PER LINE | LINES PER PAGE | 1 | 2 | 9 | 10 | 13 | 14 | 15 |  | 16 | 17 | 18 | 1 | : | 3 | 4 | \& | 9 | 10 | 11 | 12 | 13 | 14 | 18 |
| 30 | 32 | 0 | 1 | 1 | 1 | 0 | 1 | 1. |  | 0 | 3 | 0 | 0 | + | 1 | - | 1 | 0 | 1 | 1 | 1 | () | 0 | 0 |
| 31 | 31 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  | + | 0 | 0 | 0 | + | 1 | - | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 32 | 29 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  | + | 0 | 0 | - | + | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 33 | 26 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |  | 1 | 0 | 0 | 1 | + | 1 | - | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 34 | 29 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  | + | 0 | 0 | - | + | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 35 | 27 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  | 1 | 0 | 0 | 1 | + | 1 | - | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 36 | 26 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |  | 1 | 0 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 37 | 27 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 0 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 38 | 25 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  | 1 | 0 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 1 | J. | 0 | 1 | 0 |
| 39 | 20 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 0 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 40 | 25 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  | + | - | 0 | + | + | 1 | - | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 41 | 25 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | + | - | 0 | + | + | 1 | - | 1 | 0 | 0 | 0 | $1)$ | 1 | 1 | 0 |
| 42 | 22 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |  | 1 | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 43 | 24 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 0 | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 44 | 22 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |  | 1 | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 45 | 22 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |  | 1 | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 46 | 22 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |  | 1 | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 47 | 22 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 48 | 22 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 49 | 21 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |  | + | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 50 | 20 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |  | 0 | 1 | 0 | 0 | + | 1 | - | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 51 | 21 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  | + | 1 | 0 | - | + | 1 | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 52 | 20 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  | 0 | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 53 | 20 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |  | 0 | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 54 | 20 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  | 0 | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 55 | 19 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  | + | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 56 | 19 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |  | + | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 57 | 19 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  | + | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 58 | 18 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |  | 1 | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 59 | 18 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  | 1 | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 60 | 18 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | , | 1 | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

Table 3-3. Flexible Array Jumpers (Cont'd)

| FL, FXIBLE ARRAY FORMATS |  | CONNECTOR P-1 PIN NUMBERS |  |  |  |  |  |  |  |  |  | CONNECTOR P-2 PIN NUMBERS |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CHARACTERS PER LINE | LJifs ffi: PAGE | 1 | 2 | 9 | 10 | 13 | 14 | 15 | 16 | 17 | 18 | 1 | 2 | 3 | 4 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 18 |
| $\bigcirc 1$ | 18 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | + | 1 | - | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| ↔ 2 | 17 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | + | + | - | + | + | 1 | - | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 03 | 17 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | + | + | - | + | + | 1 | - | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 64 | 17 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | + | + | - | + | + | 1 | - | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| br | 17 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | + | + | - | + | + | 1 | - | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 6e) | 16 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | + | 1 | - | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 127 | 16 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | $+$ | 1 | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 68 | 16 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 69 | 10 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 70 | 16 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 71 | 15 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | + | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 72 | 15 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | + | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 73 | 15 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | + | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 74 | 15 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | + | 0 | 1 | 0 | $+$ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 75 | 15 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | $+$ | 0 | 1 | 0 | $+$ | 1 | - | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 76 | . 14 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 77 | 14 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| . 78 | 14 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | $+$ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 79 | 14 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 80 | 14 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 81 | 14 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | + | 1 | - | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |


| Viewer Screen Raster Area: | $8.5 \times 3.8$ inches |
| :---: | :---: |
| Number of Lines: | 14 |
| Displayed Characters per line: | 81 |
| Character Height: | . 120 inch |
| Character Width: | . 085 inch |
| Vertical Spacing (Center-to-Center): | . 280 inch |
| Horizontal Spacing (Center-to-Center) : | . 105 inch |

When the recommended configuration of 14 lines with 81 displayed characters is used, the following spacing and character dimensions are obtained:

## General Purpose Timing Board (Refer to Dwg. 2146306.)

The General Purpose Timing board replaces the Standard Timing board in the Logic Nest. The basic timing functions, such as the generation of timing bits and the WAIT, HOLD, START logic, are the same as in the original A5 timing card logic, therefore only the new and altered circuits are described.

Adjustable Character Counter (06C3A and 06C4A-3)
The Adjustable Character Counter is contained in two integrated circuit modules (Z41 and Z45). Eighteen terminals are connected to P1 and P2 to permit selection of the desired number of displayed characters per line on the Viewer Screen, as shown in Table 3-3. The Character Counter outputs are applied to the octal decoders to generate the selected character counts.

## Note

When a different number of characters per line is selected, the character size must be changed by readjustment of the Tickler Coil Driver, A11.

Octal Decoders (06B3A-3 and 06B5A-3)

The octal decoders (Z38 and Z42) decode the character counts needed by the horizontal and vertical SYNC logic and the variable Horizontal Retrace Counter.

## Note

Certain signal names have been retained from the standard A5 timing card but now have a different meaning. For example, the original term CH54 designated the 54 th or last character displayed per line. The term CH54 now means the "last character displayed on each line."

The Character Counter enables the two octal decoder modules, one at a time to generate the selected character count. The two octal modules alternately decode until the total character count selected in obtained.

Horizontal and Vertical Sync Flip-Flop (06B6A-3)

The H.V. SYNC flip-flop (Z47) and associated logic generate the H SYNC and V SYNC as well as the IOBP signals. The flip-flop is enabled by character 56 from the octal decoder and is reset by character 64.

Selectable Horizontal Retrace Counter (06C7A-3)
The function of the Variable Horizontal Retrace Counter (234) is to maintain a constant vertical retrace time to prevent the High Voltage Power Supply's sweep loss protection circuit from being activated and turning off the high voltage to the Viewer CRT. When a different character array is selected, the total horizontal retrace time must be divided equally among the selected number of lines so that the remaining vertical retrace time will always be the same regardless of the number of lines displayed. This is accomplished by installing the appropriate jumpers at Connector P1 as shown in Table 3-3.

## Retrace Counter Steering Flip-Flop (06C6A-3 and 06C6B-3)

The steering flip-flops and associated gating logic are used to steer the retrace counter by use of CH62, from the octal decoder and bit times BT4, 5, and 7 .

Adjustable Line Counter (06C3A-2)
The Line Counter is contained on one integrated circuit pack (Z35) and has four terminals connected to P1 to permit selection of the desired line count by means of external jumpering as shown in Table 3-3. The external jumpers are connected to either +4.5 vdc or ground as shown in the table for the desired number of lines on the viewer display tube. The Line Counter outputs are applied to logic which generates the following signals:

## IOM

SEMC
LI-P
EOP-P

High Voltage Sync Module (06B3A-2)
The High Voltage Sync module ( Z 46 ) generates the $19.2 \mathrm{KHz} \mathrm{H} . \mathrm{V}$. ENABLE signal used as the drive frequency in the High Voltage Power Supply (Unit A13).

Jumpers Required
In all cases, regardless of the flexible array format selected, the following pins of connectors P1 and P2 on card A5 (DLD 2146306) are to be jumpered as shown below:

CONNECTOR P1

PINS

CONNECTOR P2
PINS 6-17 7-16

11-12


#### Abstract

To change the flexible array, select the format desired in the left-hand column of Table 3-3, and install jumpers as shown for the various connectors pins. In Table 3-3 all pins designated by a "zero" (0) shall be connected to signal ground (Pin 1 of P 1 and Pin 18 of P 2 ). All pins designated by a "one" (1) shall be connected to +4.5 vdc ( Pin 2 of P 1 and Pin 3 of P 2 ).


End of Page Trigger Flip-Flops (06B48 and 06B49)
When an odd number of lines are to be displayed, the outputs of the End of Page Trigger flip-flops are used as an input to the Line Counter (06c3A-2) to generate the odd line count. The output pins in Table 3-3 are designated by a plus sign $(+)$ (Pin 2 of $P 2$ ) or minus sign (-) (Pin 4 of $P 2$ ) to show which output of the flip-flops are to be jumpered to P1 when an odd line format is selected.

## Nofe

When the Flexible Array Special Feature is installed, the Printer Adapter Feature may not be installed.

### 3.9 KEYBOARD OPERATION (Refer to Figure 3-33.)

### 3.9.1 GENERAL

The Keyboard is a IBM Selectric Typewriter keyboard modified to produce a seven bit digital code for each of the 64 characters. There are 45 coded key interposers for the alpha, numerical, and upper case characters on the Keyboard. Each key interposer is designed with a specific number of arms to engage only those bail rods needed to generate the seven bit digital ASCII code for the individual character. There are seven bail rods which act as a selecting mechanism to activate only those latch interposers needed to generate a specific selected character's ASCII code. The seven latch interposers activate the seven microswitch link rods that in turn activate the seven microswitches. The coded output of the microswitches is applied to the Display Register for generation of the selected character.

The following paragraphs describe one cycle of operation of the Keyboard from the time the VDT operator presses a key until the Keyboard generates the selected character's ASCII code, completes its full cycle and returns to the ready state. Figure 3-34 shows one cycle of keyboard speration.

### 3.9.2 CHARACTER SELECTION

When the operator presses the key, the key lever's downward movement causes the key pawl to depress the selected character's key interposer downward. The selected interposer activates the compensator interlock by displacing the steel balls
in the compensator tube. The key interposer latch spring engages the end of the key interposer holding the interposer in position to be engaged by the filter shaft cam lobe.


70/752-0200

Figure 3-33. Keyboard Operation

### 3.9.3 LATCH BAIL ROD

At the same time the latch spring engages, the interposer depresses the latch bail rod. The latch bail rod trips the clutch latch pawl from the latch keeper arm, permitting the spring-loaded slide arm to pull the cycle clutch arm from the clutch cam releasing the clutch. The clutch arm engages the filter shaft lobe. Releasing the clutch springs enables the clutch to wind up the inner clutch spring, thus engaging the clutch to the drive motor shaft and begins cycling the filter shaft.


[^6]2017:2-002

Figure 3-34. One Cycle of Keyboard Operation Flow Chart

### 3.9.4 FILTER SHAFT. FUNCTIONS

The filter shaft has three functions:

1. To drive the key interposer and associated bail rods and latch interposers.
2. To drive the storage bar actuating arms.
3. To drive the clutch cycling arm and associated latch pawl linkage.

Each function is described in sequential order.

## Bail Rod Selection

When the filter shaft begins to turn, one of the shaft cam lobes engages the depressed key interposer end lug, and drives the interposer forward. The key interpower arms push the selected bail rods forward. The selected bail rods push their associated latch interposers forward.

Latch Interposer Function
The forward movement of the selected latch interposers pulls their microswitch link rods forward and releases the tension on their selected microswitches, allowing the selected microswitches to open.

## Note

The seven microswitches are energized by +4.5 vdc that is connected to the normally closed (NC) contact of the switches. The switch outputs are taken off the common (C) terminal. Normally closed in this system is defined as that terminal which is normally closed by the pressure of the link rod in the quiescent (unstored) state.

## Storage Bar Action

When the latch interposers have pulled the selected link rods forward to generate the ASCII code for the selected character, the filter shaft lobe engages the two storage actuating arms. The actuating arms lift up the storage bar. The storage bar clamps all seven of the microswitch actuating link rods between the urethane edge of the bar and the nylon storage block. This holds the selected link rods in the stored position for a period of 25 to 28 milliseconds.

## Note

The first segment of the storage time is approximately 28 milliseconds, during which time the storage bar is actually holding the link rods. The remaining storage time of 38 to 42 milliseconds varies due to the delay in the complete cycle of the mechanical parts advancing and returning to their normal (unstored) position.

During storage time the selected key interposer disengages the compensator ball interlock and begins to return to its normal position. At this point in time the VDT operator may select the next character key even though there is a character being held in storage. This permits faster typing speeds than would be possible on a standard typewriter.

## Keyboard Strobe

During the storage time, the keyboard entry logic of the Display Register is enabled to allow a parallel transfer of the selected character's seven bit digital code from the keyboard microswitches into the DR Register.

The filter shaft cam disengages the two storage actuating arms and the storage bar return springs lower the storage bar, releasing the link rods. The selected link rods are then pulled back by the link rod return springs and each rod closes its associated microswitch completing the storage cycle.

## Note

The output of the seven microswitches will be all "ones" in the normal or unstored state (+4.5 vdc = "1").

## Clutch Cycling Arm and Associated Linkage

During the storage cycle the clutch cycling arm has been returned sufficiently by the filter shaft cam to permit the clutch latch pawl to overtravel and clear the keeper arm and allow the pawl spring to depress the pawl into position to engage the keeper arm. As the clutch arm is released by the cam, the latch pawl strikes the end of the keeper bar.

At this time the clutch spring engages the clutch housing cam and causes the clutch to release the filter shaft (by unwinding the inner clutch spring).

## Anti-Backlash Cam Action

When the filter shaft clutch disengages, the forward inertia of the clutch housing allows the leaf spring to engage the backlash cam, holding the clutch in the released position. This completes one cycle of operation of the keyboard mechartism during the selection of one character.

### 3.9.5 SELECTOR COMPENSATOR TUBE FUNCTION

The function of the Selector Compensator Tube is to allow only one key interposer to be depressed at a time, thus acting as an interlock to prevent a second character from being selected simultaneously with the first character.

The Compensator Tube is located at the rear of the keyboard and is directly below the key interposer compensator arms. When a character is selected and the key interposer is depressed, the interposer compensator arm is forced between two of the steel balls in the compensator tube as shown in Figure 3-34.

A. SIMULTANEOUS KEYLEVER DEPRESSION BLOCKED
B. SECOND KEYLEVER DEPRESSION BLOCKED

Figure 3-35. Compensator Tube Interlock


#### Abstract

Note

In the normal state with no key interposer depressed, there is only enough space between the steel balls to allow one key interposer arm to be depressed.


When an interposer compensator arm is depressed between the steel balls, all of the balls are offset enough to prevent any other interposer from being forceably depressed as shown in Figure 3-35.

Note that the second key interposer arm is blocked by the top of one of the offset steel balls. When the key interposer completes its selection cycle, and the filter shaft cam releases the interposer, the interposer compensator arm is raised out of the compensator tube by the interposer return spring. The steel balls are immediately returned to their normal position. The second key may be immediately selected, permitting faster typing speeds.

## SECTION FOUR MAINTENANCE

### 4.1 GENERAL

This section contains the procedures for parts replacement for major components, mechanical and electrical adjustments, lubrication, and procedures for trouble shooting and isolating malfunctions.

### 4.2 PREVENTIVE MAINTENANCE

Refer to the latest Spectra 70 TIP for preventive maintenance schedules and procedures for the Model 70/752 Video Data Terminal.

### 4.3 OPERATIONAL CHECKS

1. Remove the data set connector, apply pnwer and let the unit warm up for five minutes; press the WRITE switch, then press the MASTER ERASE and SCREEN switch.
2. Press each key and ensure it does not repeat when it is held down. If pressing the key does produce repeat characters, refer to the keyboard adjustment procedures.
3. Press and hold the $\rightarrow$ (advance) switch until the mark advances to the next line; ensure that it moves one character space at a time and will advance one space when the switch is pressed once.
4. Press and hold the $\leftarrow$ (backspace) switch until the mark stops moving at the beginning of a line. Move the mark several spaces to the right and ensure that the mark will backspace one space when the switch is pressed once.
5. Press and hold the $\&$ (return) switch until the mark is moved from the last line to the first line; ensure that it will move one line when the switch is pressed once.
6. Press the MASTER ERASE key and the SCREEN switch; all characters will disappear and the mark will move to the beginning of the page.
7. Type the alphabet and two sets of numbers. Backspace the mark under the "1" of the second set of numbers and press the $\ll$ (return) key. The second set of numbers will be erased, the return character will be entered, and the mark will move to the next line.
 with the ADVANCE switch and the M key fill the balance of the first line with the letter $M$, place an $M$ and $\ll$ characters in the third through ninth lines, place alternately M's and spaces six times in the tenth line, place an $M$ in the first position of the eleventh through nineteenth lines, and fill the last line with several M's and sets of numbers.
8. Press and hold the $\rightarrow$ (ADVANCE) switch and check that it returns to the beginning of the next line as it passes a return character and not when it passes the position the return switch was pressed.
9. Check the display for the following qualities:
a. BRIGHTNESS adjustment
b. FOCUS adjustment
c. PICTURE (phase) adjustment
d. The distance from the center of the top line to the center of the bottom line is approximately 5.5 inches.
e. The length of the top and bottom lines is approximately 8.0 inches.
f. The distance from the ends of the lines to the tube frame is approximately equal (both horizontally and vertically).

## Nofe

If the above checks indicate need for adjustment refer to paragraph 4.7.1 Deflection Amplifier Adjustments.
g. Check that all characters are completely formed and there are no extraneous spots around the characters.

## Note

If the display of the characters is not normal refer to paragraph 4.7.5, Character Generator Alignment.
11. Press the XMT switch; it will light. The WRITE light will go out, and the mark will move to the third character position in the first line. This indicates that the display-to-buffer transfer, buffer control, and automatic mark control functions are operative. (Note: Data set cable removed.)
12. Press the WRITE switch; move the mark under the second character with the ADVANCE switch.
13. Press the MASTER ERASE key and CHAR switch; check that the second character has been erased, and the mark has moved to the third character position.
14. Press the MASTER ERASE key and LINE switch; check that the remainder of the line has been erased and the mark has moved to the beginning of the next line.
15. Press the MASTER ERASE key and SCREEN switch; check that the remainder of the screen has been erased and the mark has moved to the beginning of the page.
16. Type "DATA•INSERT•TEST•<< DATA•INSERT." (it will appear as two lines.) Press the WRITE switch and move the mark under the space between INSERT and TEST.
17. Press the DATA INSERT switch; it will light. Type "ED." Check that the display is "DATA•INSERTED.TEST• < DATA•INSERT." (Note: ED added.)
18. Press the Space Bar enough times until the word TEST has moved to the next line. Check that the $\ll$ (carriage return) character has not moved to the second line.
19. Press the DATA INSERT switch; it will go out.
20. Press the MSA switch; it will light. Press the return switch and enter the」 (ETX) character.
21. Press the WRITE switch and move the mark under the "I" of the first line.
22. Press the XMT switch; it will light, the WRITE light will go out, and the mark will move under the S .
23. Press the WRITE switch and then press the MASTER ERASE key and SCREEN switch.
24. If the Video Data Terminal does not have the Printer Adapter Special Feature, skip steps 25, 26, and 27; if it does, type the message "PRINTER • AD APTER • T EST $\cdot \lll \lll E N D T E S T \ll "$.
25. Press the PRIN switch; it will light and the following message will be printed.

PRINTER AD APTER T EST
END TEST (paper moves up one line)
26. Check the printed message for quality printing and ensure that all characters typed were printed.
27. Press the LF button on the printer to advance the paper.
28. If the Video Data Terminal does not have the Data Format Special Feature, skip steps 29 through 30; if it does, request a standard message format.
29. Type some characters and ensure that the variable data characters are noticeably brighter than the data format characters.
30. Press and hold the $\rightarrow$ (ADVANCE) switch and ensure that the mark advances from data field to data field.
31. Press the $\downarrow$ (RETURN) switch and ensure that the mark moves to the first character position of the next variable data following that line.

### 4.4 KEYBOARD LUBRICATION

All lubrication must be performed from the following procedures.

## CAUTION

> Overlubrication of the $70 / 752$ Keyboard mechanism will cause m-llfunctions in the unit; therefore, it is mandatory that all Field Personnel use only those lubricants specified in this manual and follow the lubrication procedure given. Excessive lubrication will cause the mechanical adjustments to give improper operation, and will lead to overadjustment which will result in excessive wear to the mechanisms.

1. Remove the Keyboard from the Control Panel baseplate (by removing four mounting screws) and vacuum all foreign matter from the unit and baseplate.
2. Lubricate ONLY those points shown in Figures 4-1 through 4-4. Each point referenced in the illustrations specifies the type of lubricant that must be us:d.

CAUTION

Do NOT use an alternate grease, since lower melting point grease will migrate and spin-off, causing malfunctions in the keyboard.
a. At all points designated by the letter " $A$ " in Figures $4-1$ through 4-3 use light oil (No. 28 oil - 932694).
b. At all points designated by the letter "B" in Figures $4-1$ and 4-2 use IBM Lubrisant No. 23, IBM part number 1280442,(RCA - 954163).

## Note

When lubricating the filter shaft (Figure 4-2, item F$)$, lightly lubricate the entire lerigth of the shaft lobes.
c. Figure 4-4 shows the clutch lubrication point designated by the letter "C". Lightly grease with Molube-Alloy No. 2 medium (RCA-954165). Apply grease into slot by the spring tang (Figure 4-4, item 1) until grease appears at the end of the collar by the gear hub (Figure 4-4, item 2). DO NOT apply grease to the oilite bearing.
3. Clean the contacts of switches $S 8$ and Sl0, Figure 4-5, located on the lower Keyboard frame, with bond paper saturated in alcohol, by drawing the paper between the closed switch contacts.


Figure 4-1. Cycle Clutch Linkage Lubrication
(A) (RCA 932694)
(B) (IBM 1280442)


Figure 4-2. Filter Shaft And Return Delay Arm Lubrication

(A) (RCA 932694)

Figure 4-3. Drive Motor Lubrication


Figure 4-4. Clutch Lubrication

figure 4-5. $\quad$ S8 and S10 Switch Confact Cleaning

### 4.5 PARTS REMOVAL AND REPLACEMENT PROCEDURES


#### Abstract

Note

When ordering replacement parts it is mandatory that the model number, serial number, and Equipment Revision Level (ERL) be included to ensure receiving the correct replacement part.


The major components of the Video Data Terminal may be removed and replaced using the following procedures. Unless otherwise specified, replacement procedures are assumed to be in the reverse order of removal and are not described.

Assemblies that have been removed should be adequately protected to prevent damage to parts or misalignment of electronic adjustments. When an assembly has been replaced, perform all applicable alignment and adjustment procedures found in Section Four.

Refer to Appendix A for the identification and location of assemblies and components.

### 4.5.1 VIEWER ASSEMBLY ACCESS

## CAUTION

Prior to any parts removal or replacement the Video Data Terminal shall be disconnected from its power source and the data input/output connector P16 removed.

To gain access to the major components in the Viewer, remove the rear panel and the housing as follows:

1. Remove the six screws on the rear panel and tilt the panel backwards, allowing the fan assembly in the upper left hand cover to clear the housing.
2. When the fan assembly is clear, lift the rear panel free of the housing. Disconnect the cable from the fan assembly.
3. Remove the two screws in the lower corners that secure the housing to the connector mounting bracket and the Low Voltage Power Supply.
4. Slide the housing to the rear, taking care to clear the components on the Tickler Driver component board, until the housing is free.

## Module Boards, A1 through A6

Each module board may be removed from the nest assembly by pulling firmly to the rear to disconnect the boards from the appropriate connector (J1 through J6).

## Delay Line, A7

The Delay Line is located on the hinged panel at the left side of the Viewer (looking from the rear).

1. Remove the four screws on the front and rear brackets securing the Delay Line panel.
2. Swing the brackets clear and carefully lower the Delay Line panel.
3. Disconnect $J 7$ and remove the screws securing the hinge to the basic assembly.

## Selection Amplifier, A8

With the Delay Line lowered, remove the Selection Amplifier by pulling. firmly upward to disconnect the Component Board from J801 and J802.

## Deflection Amplifier, A9

The Deflection Amplifier may be removed as follows:

1. Lower the Delay Line.
2. Open the front Control Panel and remove the three knobs on the BRIGHTNESS, PICTURE, and FOCUS controls.
3. Remove the Deflection Amplifier by pulling firmly upward to disconnect the component board from J901 and J902.

## Monoscope, A10

The Monoscope Tube (V1) and the Monoscope Preamplifier (A10A1) may be removed by using the following procedures:

1. Remove the four screws and the monoscope housing cover located at the rear of the Viewer.

## WARNING

Before proceeding, connect a grounding probe clip lead to the viewer baseplate and carefully ground all exposed terminals and anode leads.
2. Mark and remove the two slide-tab connections from the rear of the preamplifier assembly. These leads can be identified by their connection to the feedthrough capacitors C1 and C2 located near the end of the monoscope housing.

## CAUTION

During reinstallation to prevent shorting the power supply ensure that the slide-tabs do not short to the ground terminal, (tab openings should face left).
3. Remove the braided ground lead from the ground screw terminal E1 inside the monoscope housing.
4. Slide the top of the 0 -ring retainer off the end of the monoscope tube.
5. Disconnect component board connector J12 from the Video Driver Board, A12. Mark and remove the coaxial lead terminals 16 and 18 of Video Driver Board connector, J12. Removal will require the use of an AMP "B" 810992-1 extraction tool.
6. Grasp the end of the monoscope tube firmly and disconnect by pulling carefully to the rear of Viewer, while feeding the coaxial lead through the housing grommet.
7. Upon replacement ensure proper alignment of the monoscope tube base with the socket keyway in the monoscope assembly.

## Monoscope Preamplifier Assembly, A10A1

The Monoscope Preamplifier Assembly may be removed after removal of the monoscope tube using the procedure listed above (with preamplifier attached), in the following manner:

1. Remove the anode clip connector from the side of the monoscope tube.
2. Roll or slip the O-ring past the preamplifier assembly support tabs located near the base end of the monoscope tube.
3. Carefully disconnect the board mounted anode clip from the opposite end of the monoscope tube.

## Tickler Driver Module Assembly, All

The Tickler Driver may be removed by using the following procedures:

1. Remove the four screws, one with ground lead attached, from $Q 20$ transistor heat sink assembly.
2. Remove the mounting screw from the upper left corner of the module as viewed from the rear of the viewer.
3. Grasp the module firmly and withdraw it towards the front of the viewer while disconnecting the module connector, J11.
4. Prior to replacement of this module, clean the thermal compound from the bottom of the Q20 heat sink and the mating surface of the Viewer CRT cover with a clean, soft, lint-free cloth.
5. Apply a thin film of Thermal Compound, RCA Part 2187263, to the heatsink mating surface prior to assembly on the viewer.

## Video Driver, A12

The Video Driver may be removed as follows:

1. Disconnect J12 from the video driver component board.
2. Remove four screws in the CR10 diode heatsink in the lower right hand corner of the board.
3. Remove the three screws securing the component board to the rear shield cover.
4. Remove the nut securing the terminal and wire to the lower left hand corner of the board.
5. Prior to replacement of this module, clean the thermal compound from the bottom of the CR1O heatsink and the mating surface on the Viewer CRT cover with a clean, soft, lint-free cloth.
6. Apply a thin film of thermal compound, RCA Part 2187263, to the heatsink mating surface prior to assembly on the Viewer.

High Voltage Power Supply Assembly, A13
The High Voltage Power Supply may be removed by using the following procedures:

1. Remove the six screws from the perforated safety cover and withdraw cover.

## WARNING

Before proceeding, connect a grounding probe clip lead to the viewer baseplate and carefully ground all exposed terminals and anode leads. In the absence of a ground probe, a clip lead from the viewer baseplate to the metal shaft of an insulated handle screwdriver can be used.
2. Mark and remove the 6.3 vac filament leads from terminals E3 and E4. Terminals E3 and E4 are the top-most ceramic stand-off terminals on the right wall of the power supply housing. On later production models. E3 and E4 are on the left wall of the Power Supply Housing.
3. Mark and remove the high voltage leads from terminals $E 1$ and $E 2$. Terminals $E 1$ and $E 2$ are the lower-most long ceramic terminals on the right wall of the power supply housing.
4. Mark and remove the harness wiring from the outboard or nearest side of TB1. Mark and remove the ground lead screw to the left of TB1 which also serves to secure the Power Supply to the baseplate. Slip the grommet and the wiring harness out of the slot and bend clear.
5. Remove the remaining securing screw located to the right of TB1.
6. Carefully withdraw the Power Supply from the left side of the Viewer, ensuring not to damage or pull leads loosened in steps 2, 3, and 4.
7. During replacement, ensure that the securing tab of the power supply base is inserted properly into the slot provided in the center web of the Viewer.
8. Care should be exercised when tightening the filament and high voltage leads on the ceramic stand-off terminals.

Low Voltage Power Supply Assembly, A14 and Requlator Assembly A14A1
The low voltage power supply and the regulator assembly may be removed as follows:

1. Remove the four screws on the power supply cover door and lower the door to expose the interior of the power supply and the door-mounted regulator.

## WARNING

Before proceeding, disconnect the ac plug, connect a grounding probe clip lead to the viewer baseplate and carefully ground all exposed terminals and anode leads. In the absence of a ground probe, a clip lead from the viewer baseplate to the metal shaft on an insulated handle screwdriver can be used.
2. The Regulator Assembly, A14A1, may be removed at this point. Remove the two mounting screws and withdraw the regulator assembly while disengaging connector J1.
3. Remove the filament leads from the High Voltage Power Supply in accordance with steps 1 and 2 of the Low Voltage Power Supply procedure in paragraph 4.5.1.
4. Remove the ring lug from screw terminal E7 located on the power supply housing adjacent to the J11 and J12 component board connectors.
5. Mark and remove the harness wiring from the outboard of TB5 on the bottom of the Power Supply Assembly.
6. Mark and remove the harness wiring from C2 (E2), C4 (E4), and C8 (E5).
7. Remove the two power supply securing screws from the bottom of the assembly and one securing screw at the rear of the Viewer center web partition.
8. Ensure that the Video Data Terminal power cord, blower fan supply cord, and the wiring loosened above is free. Carefully withdraw the Low Voltage power Supply Assembly from the left side of the Viewer.

## Dynamic Focus, A20

The dynamic focus component board may be removed as follows:

1. Disconnect J12 from the video driver component board.
2. Remove the two screws securing the rear shield cover to the basic shield assembly.
3. Remove the three screws securing the component board to the rear shield cover.
4. Lift the rear shield cover free of the basic shield assembly, giving access to the CRT base.
5. For ease of work, disconnect the CRT base socket.
6. Remove the two screws securing the dynamic focus somponent board to the basic shield assembly.
7. Disconnect the component board from J20 by pulling firmly upward.
8. Remove the screw securing the stand-off terminal to the upper edge of the board.

## Keyboard Filter, A21

The Keyboard Filter may be removed as follows:

1. Lower the Delay Line.
2. Disconnect J2101 and J2102.
3. Remove the four screws securing the Keyboard Filter component board to the Nest Assembly.

## Cathode Ray Tube

The Cathode Ray Tube may be removed by using the following procedure:

## WARNING

Cathode Ray Tubes are dangerous to handle. Refer servicing to qualified service personnel. The Cathode Ray Tube in this unit employs integral implosion protection.

1. Remove the two screws from the rear of the CRT housing. Disconnect the video driver connector, J12, and carefully slide the housing back until the forward end tab is clear. Tilt the housing cover to the right side of the Viewer while maintaining slack in the ground lead from the Video Driver. Prop the housing cover clear of the CRT neck area.
2. Mark the yoke and housing tab immediately above, with a fine pencil line. Loosen the yoke clamp screw.
3. Remove the anode clip lead from the left side of the CRT.
4. Remove the socket connection from the base of the CRT.
5. Lower the Delay Line A7, using the Delay Line replacement procedure in previous paragraph. Remove Selection and Deflection Amplifiers, A8 and A9, using procedures contained in the previous paragraphs.
6. Remove the screw from the access door on the bottom front of the Viewer and hinge door down. Remove the three bezel mounting screws which secure the bezel to the baseplate.
7. Remove the six screws from the forward end of the CRT housing. Two screws are located on each side and the top of the CRT housing.
8. Slide the bezel and CRT assembly forward while guiding the tube neck and base through the deflection yoke. Lay the bezel and CRT face down on a padded area.
9. Unhook the grounding braid tension spring from the CRT retaining clamp. Unhook the retaining clamp spring and remove the clamp from the four holding clips.
10. Lift the tube up and tilt to feed the tube neck and base through the grounding braid.
11. After replacement, refer to the deflection amplifier adjustment procedure and the deflection yoke alignment procedure.

## Deflection Yoke

## CAUTION

> Before replacing the deflection yoke, check the serial number of the associated deflection amplifier in the VDT. For deflection amplifiers serial numbers 0135 and below, the following resistors must be replaced with the values indicated on Page A43 before the amplifier is used. Replace resistor R8 with IPB Figure 12 , Item 27 . Replace resistors R5 and R39 with IPB Figure 12 , Item 32 .

The deflection yoke may be removed by using the following procedure.

1. Remove the CRT and bezel assembly by utilizing the procedures contained in the previous paragraph.
2. Mark and remove terminals 14,15 and 16 of the J11 connector for the tickler driver module and terminals $3,5,16$ and 18 of the $J 901$ connector for the deflection amplifier module. Removal will require the use of an AMP "B" 810992-1 extraction tool.
3. Carefully remove the deflection yoke from the Viewer while guiding the wiring loosened in Step 2.

### 4.5.2 INTEGRATED CIRCUIT PACKAGE REPLACEMENT

When replacing an ICP, the primary consideration is that extreme care be taken so that no damage is done to the printed board, etched lines, pads or other components. Excessive heat or mechanical abuse will cause pads to lift and lines to break. During the removal process, all possible precautions to avoid damage to the board must be taken, even at the sacrifice of the ICP itself.

## Tools Required



## CAUTION

Two of the IC packages (RCA Dwgs. 2187271 and 2187272) have the index notch reversed from that of the standard IC packages. To avoid confusion, use the color coded dot rather than the index notch to determine the location of Pin No. 1. When the ICP is held in a vertical position with the color code dot at the bottom, Pin No. 1 will be at the upper left corner of the package. Refer to Figure 4-5A.


Figure 4-5A. IC Pin Identification

From experience, it has been found that the $37 \frac{1}{2}$ watt Ungar iron with a $3 / 64$ " PL340 Tiplet point provides the right amount of heat and can do a very neat job. It is extremely important to keep the tip freshly tinned and free from slag. Retinning the iron and wiping it clean for each soldering operation is a good practice.

## CAUTION

Do not use the large diameter single core resin solder. It is extremely hard to control the flux flow when working on small joints with this type of solder. A solder such as Ersin Multicore, with a diameter of 0.032 inches, should be used.

When soldering or resoldering a connection, do not work the sharp tip of the iron into the hole or eyelet around the leads. This will result in physical damage to the board itself. As much of the flat of the tip as possible should be placed on top of the eyelet and intimate contact maintained so that optimum heat transfer results. This will cause the solder to flow rapidly and prevent heat damage to surrounding areas.

## Removal Procedure

1. Using the needle nose cutters, carefully clip the 14 leads close to the flat pack body. Try to leave $1 / 32^{\prime \prime}$ to $1 / 1^{\prime \prime}$ of the lead on the board. This will leave enough lead on the flat pack to provide contacts for testing (engineering analysis on returned defective parts) and will also leave enough lead on the board to allow easy removal (see step 2).

## CAUTION

The flat pack body may be stuck to the board with flux which was not completely removed during the manufacturing wash cycle. If this is encountered, use extreme care not to lift the printed circuits that run under the ICP. Tweezers can be used to lift the ICP slightly while flowing chlorothene under the ICP to dissolve the flux.

After all 14 leads are cut, remove the flat pack and return according to the procedure in TIP General-4.
2. Bend the portion of the leads remaining on the board up to a position perpendicular to the board.
3. Mount the board in the Tronic Card Holder in a vertical position such that both sides of the board are accessible. For right handers the component side (front) should face to the right and the back side to the left.
4. Cock the Soldapullt and place it over the ICP lead (on the back side) to be removed. Heat the connection on the component side holding the flat of the Tiplet point as flat as possible against the joint. As soon as the solder is molten, trigger the Soldapullt. In most cases, the operation will have to be repeated by reversing the iron and Soldapullt application from side to side until the ICP lead is free to be removed from the back side with the tweezers. Do not use force in removing the lead if it is still being held by solder. Grip the protruding end lightly with the tweezers. Apply the iron tip to the opposite side of the board; when the solder is molten the lead will slip out easily.

CAUTION

> Do Not use the tip of the iron as a pry or as a reamer since this will cause mechanical damage. Do not use excessive pressure with the iron tip to transfer heat.
5. The best transfer of heat requires a clean tip. Frequently, add a little solder to the iron tip in order to aid heat transfer and to add flux to the joint. Wipe the iron tip on a solder sponge after removal of solder from each terminal to avoid transporting a globule of solder to the next terminal to be removed. Do not file the tiplet as it has a special iron-clad copper tip.

## Nofe

Occasionally, the Soldapullt will become sluggish and fail to withdraw solder properly. Disassemble the unit (see instructions accompanying the Soldapullt), clean the cylinder wall and the "O" ring on the plunger. Apply a film of light oil to the cyl. inder, wiping it around the cylinder wall.
6. Repeat step 4 until all 14 leads are removed.
7. Check each lead hole to make certain all solder has been removed. If necessary, reheat and remove any remaining solder using the Soldapullt. Clean the holes and surrounding area with Chlorothene applied with a brush. Use the dispenser for convenience in handling the Chlorothene. Wipe with a clean rag. The holes should now be free from all foreign matter and ready to accept the leads from the new flat pack. Use the jewelers loupe for this inspection.

## Installation Procedure

At this point, it is assumed that the defective flat pack has been removed from the circuit board and that the board is in a condition suitable to accept the new flat pack. The same general soldering rules for removing flat packs should be followed for installation of flat packs.

1. Replacement ICP flat packs will have preformed and precut leads. Mount the new flat pack on the board making sure that it is correctly oriented. The appropriate data sheet will show the correct orientation.

## CAUTION

Ensure that none of the leads are shorting to each other. If any of the leads require additional forming, use tweezers.

Hold the flat pack in place from the component side of the board and bend all leads on the other side in a direction away from the flat pack proper at an angle approximately 30 degrees with the back side of the board to hold the ICP in place.
2. Mount the board in the Tronic Card holder, component side towards the left.
3. Solder each lead in turn in the top four-terminal row first. Apply heat to the printed circuit pad and lead on the back side of the board and feed solder to printed circuit pad on the component side of the board. The solder will flow freely towards the iron and secure the connection at both the front and back. Apply only the minimum amount of heat and solder necessary to make secure connections. Trim away the excess lead lengths in the row just completed. Next, solder the three-terminal row and cut away the excess lead lengths as before. Repeat the procedure for the other leads to be soldered.
4. Remove the resin from the area using cholorothene and the acid brush.

## Alternate Method

1. Plug iron into vanvac and set at 120 vac.

## Nofe

Do not change setting.
2. Place CKT board on styrofoam pad, component side up.
3. Using small diagonals, carefully clip the 14 leads close to the board.

## Note

Leave $1 / 32^{\prime \prime}$ to a $1 / 16^{\prime \prime}$ of the lead on the board.

## CAUTION

In the following step, exercise extreme caution to prevent damage to the $P / C$ board pad.
4. After all 14 leads have been cut, remove the IC Body, carefully lift pack from the board with fingers, without damaging pad or components.
5. Remove one lead at a time by applying solder iron to the related circuit pad. Apply just enough heat to remove lead with tweezers.
6. Pick up braid, dip in kester flux and position braid across 7 pads. Position iron and with light motion pull braid across 7 pads. Repeat for 2nd row. Remove and residual solder in the mounting holes by heating pad and inserting piece of bus wire through the hole. Clean with bristle brush and alcohol.

### 4.5.3 CONTROL PANEL ASSEMBLY

To provide access to the major components in the Control Panel Assembly, remove the cover as follows:

1. Disconnect the Control Panel connector P15 from the Viewer and move the Control Panel to a clear work area.
2. Place the Control Panel Assembly upside down on a padded surface and remove the six cover-retaining screws from the baseplate.
3. Return the Control Panel Assembly and cover to an upright position and remove the cover.

## Keyboard

The Keyboard is removed using the following procedure:

1. While maintaining the Control Panel in an upright position, remove the four screws from beneath the baseplate of the unit.

## CAUTION

Ensure that the wiring harness between the Keyboard and the left side of the baseplate is not restricted by the cabling tab.
2. The tab can be bent to an upright position to facilitate removal and replacement.
3. Raise the Keyboard slightly and withdraw to the left while observing the drive motor and fan clearance through the motor shield.
4. When clear of the baseplate, lay the Keyboard upside down on a soft pad.
5. Mark and remove the wiring harness from the front side of terminal board TB1.

## Switch Matrix Subassembly

With the cover and Keyboard removed from the Control Panel, the switch matrix subassembly may be removed in the following manner:

1. Mark and remove the wiring harness from the rear side of terminal board TB1.
2. Remove the two screws which secure connector J15 to the baseplate. These screws, one male and one female, also serve to polarize the connection, therefore a note of their locations should be made prior to disassembly.
3. Remove the four mounting screws from beneath the baseplate which secures the switch matrix subassembly and lift the unit and its harness free of the baseplate.

## Switch Matrix Alignment

1. When a switch button pops out of the matrix switch, it is usually caused by warping of the center tab on the lens cap. To correct this problem, hold the lens cap and use a screwdriver to pry the center tab back. Hold the tab back in this position with one hand, and with the other, bring a heated soldering iron in close proximity of the center tab. (Be sure not to touch the plastic cap with the iron.) Apply only enough heat to the tab to form it into the outward position. Reinstall the lens cap when it has cooled down.
2. Remove the mounting plates which hold the matrix switch assembly.
3. Loosen the 5 nuts which are secured with Loctite Grade E (932672) on the shafts of the matrix switch assembly. This will allow the switches to operate freely. When all switches are operating, finger tighten the 5 nuts and apply Loctite Grade E.
4. Before putting on mounting brackets, slide a flat washer on the bolt behind the bracket. This will ensure that the bracket does not tighten down against the screws of the matrix switch, causing the switches to stick again.

## CAUTION

During reassembly ensure that the wire harness is not pinched or can later be abraded by any mechanical assembly.

### 4.6 KEYBOARD ALIGNMENT AND ADJUSTMENTS

The only mechanical adjustments to be made in the field are indicated by the word (FIELD) following the title.

The word (FACTORY) following the title denotes adjustments that are normally made at the factory. When field personnel must replace major components, the appropriate factory adjustments must be made.

## CAUTION

> The following procedures indicated as FACTORY adjustments and alignments shall NOT be performed unless replacement of components is necessary. When required, these procedures must be performed with extreme care to ensure that all keyboard alignments are made according to the procedures in the correct sequence.

### 4.6.1 KEYBOARD DRIVE TRAIN ADJUSTMENT (Field)

1. Turn off the Video Data Terminals power.
2. Remove the Control Panel housing as outlined in paragraph 4.5.3.
3. Loosen the $6 / 32$ inch nut on the drive motor's upper mounting screw, located on the inside of the right hand Keyboard end frame (Figure 4-5B).
4. Press on the motor field to engage the drive motor's spur gear fully with the urethane clutch gear.
5. Obtain the special clutch gear gauge (part no. 1144869, stock no. 954361) designed specifically for adjusting the clutch and drive motor gear clearance.
6. Place the wire's feeler arm in the clutch gear as shown in Figure 4-5B and slowly rotate the motor fan blade, allowing the wire to engage the motor's spur gear; move the motor's loose mount back.
7. When the feeler guage passes through the gear's point of tangency, ensure that a slight friction is felt.

## CAUTION

Excess pressure on the motor will cause the wire to be imbedded in the soft urethane clutch gear and result in improper adjustment. A slight feel of friction will result in an approximate clearance of .009, which ensures optimum performance.
8. When the correct clearance is obtained, tighten the $6 / 32$ nut on the motor's upper mounting screw.

(View A)


Figure 4-5 B. Drive Gear Adjustment
9. Recheck the clearance by rotating the wire gauge through the point of tangency and ensure that only a slight friction is felt.

## Note

Proper friction will be just enough to hold the 8 -inch wire from rotating under its own weight.
10. Remove the wire gauge.
11. Place the Control Panel POWER switch to $O N$ and check for proper Keyboard operation.
12. Place POWER switch to OFF.
13. Replace the Control Panel housing.

### 4.6.2 BAIL ROD ALIGNMENT AND ADJUSTMENT (Factory)

1. Release two screws on left-hand side of Keyboard holding the bail plate (Figure 4-6, item 1).
2. Move the bail plate forward or to the rear so that one bail rod (Figure 4-6, item 2) is parallel to key interposer lugs (Figure 4-6, item 3).
3. Tighten the two screws on the bail plate.
4. Release two screws (Figure 4-7, item 1) on latch interposer guide comb (Figure 4-7, item 2), permitting no. 1 and 7 latch interposers to clear respective bail rods approximately . 005 inch (Figure 4-7, item 4).
5. Tighten the two screws on the guide comb.
6. Bend the guide comb tabs (Figure 4-7, item 3) (Nos. 2 through 6) for a clear-
ance of approximately . 005 inches between latch interposer nos. 2 through 6 and their respective bail rods.
7. Raise or lower the bail plate (Figure 4-6, item l) by loosening the two screws called out in step l, so that the latch bail rod (Figure 4-6, item 4) is parallel to the key interposer (Figure 4-6, item 3).
8. Tighten the two screws.
9. Recheck adjustment in Step 2 .


Figure 4-6. Bail Rod Alignment And Adjustment


Figure 4-7. Latch Interposers

### 4.6.3 FILTER SHAFT ALIGNMENT (Factory)

1. Press the "-" key and rotate the filter shaft (Figure 4-8, item l) until the filter shaft vane (Figure 4-8, item 2) touches the end of the "-" key interposer (Figure 4-8, item 3).
2. Manually release the latch spring under the "-" key interposer (Figure 4-9, item 1).
3. Press the "1" key. The end of the "1" key interposer will raise, just touching the forward edge of the filter shaft vane.
4. Manually release the latch spring under the "1" key interposer.
5. If the key interposers do not align with the filter shaft as described above, move the bearing block (Figure 4-8, item 4) forward or to the rear to correct alignment.

6. Press the "1" key.
7. Press and hold down lightly the "-" key.
8. Rotate the filter shaft (Figure 4-8, item l). The filter shaft vane (Figure $4-8$, item 2) should clear the "-" key interposer by approximately . 015 inches, but should never touch (Figure 4-8, item 5).
9. Repeat the above steps, using the "-" in Step 1 and the " 1 " in Steps 2 and 3 .
10. If the filter shaft clearance is incorrect, raise or lower either the lefthand or right-hand bearing block to obtain the correct clearance.

### 4.6.5 FILTER SHAFT ADJUSTMENT WITH CLUTCH MOUNTED (Factory)

1. Check the clearance between end of clutch and the right-hand bearing assembly (Figure 4-4, item 3) for approximately . 015 inches.
2. If the clearance is incorrect, perform the following steps.
3. Position the filter shaft vane as indicated in Figure 4-9. The filter shaft vane should be positioned at start of radius (Figure 4-9, item 2) of clutch arm assembly.
4. Loosen the two set screws (Figure 4-9, item 5) retaining the backlash cam on the clutch housing, and move the cam off the clutch housing.
5. Loosen the two set screws on the clutch housing.
6. Position the filter shaft for the correct clearance between the clutch housing and bearing block, as in step 1.
7. Tighten the two set screws on the clutch housing (Figure 4-9, item 6).
8. Readjust the backlash cam by performing the Backlash Cam Adjustment procedure in paragraph 4.6.6.


Figure 4-9. Filter Shaft Adjustment With Clutch Mounted

### 4.6.6 BACKLASH CAM ADJUSTMENT (Field)

1. Position the filter shaft as indicated in step 3 of paragraph 4.6.5.
2. Check the distance from the end of the leaf spring to the edge of the cam lobe (as shown in Figure 4-9 item 3). If the cam jaw area is approximately .10 inch, check that the two cam set screws (Figure 4-9 item 5) are tight, loctite has been applied and proceed to step 5. If the cam jaw area is not .10 high perform adjustment given in steps 3 and 4.
3. Loosen two set screws (Figure 4-9 item 5) and adjust cam jaw area to an approximate . 01 inch before the leaf spring latches (Figure 4-9 item 3).
4. Tighten two set screws (Figure 4-9 item 5) on the cam and loctite.
5. Loosen the two leaf spring mounting screws (Figure 4-10 item 2) and adjust the leaf spring to the lower edge of the cam for an approximate .020 inch bite as shown in Figure 4-10 item 1.
6. Tighten the two leaf spring mounting screws (Figure 4-10 item 2) and recheck for . 020 bite.
7. Cycle the clutch $360^{\circ}$ and check that both cam jaw areas are approximately . 10 inch when the filter shaft vanes are positioned at the start of the radius of the clutch arm assembly as shown in Figure 4-9 item 3. If the cam jaw areas are not equal repeat steps 1 through 4 to obtain approximately equal cam jaw areas.
8. Recheck the . 020 bite adjustment and repeat steps 5 and 6 if necessary.


Figure 4-10. Backlash Cam Adjustment

### 4.6.7 INTERPOSER LATCH SPRING ADJUSTMENT (Factory)

1. Remove the bail-up stop (Figure 4-6, item 5) on the support bracket.
2. Press the " H " key.
3. Using a . 020 inch feeler gauge (Figure 4-ll, item l), lift the "H" key interposer (Figure 4-11, item 3) to the top of the guide comb.
4. Loosen three screws (Figure 4-1l, item 4) on the right-hand section of the latch springs (also referenced in Figure 4-6, item 5.)
5. Raise or lower this spring section under the "H" key interposer to establish a . 020 inch clearance (Figure 4-11, item 2.)
6. Tighten the three screws (Figure 4-11, item 4.)

## Note

No other adjustment will be made on the remaining latch springs until adjustment procedures are completed on the latch pawl and keeper.


Figure 4-11. Interposer Latch Spring Adjustment

### 4.6.8 KEEPER ARM AND LATCH PAWL OVERTRAVEL ADUUSTMENY (Field)

1. Rotate the filter shaft to estajish full travel of the latch pawl (Figure 4-12, item 1)。
2. At this point of travel, loosen the two sorows (Eigure 4-12, item 2) mounting keeper bracket (Figure $4-12$, item 3). on frame.
3. Move the keeper brafiet to obtain an oventrovci (Figure 4-12, item 4 ) of approximatelytharif inches between the atch miv) and lseeper arm (Figure 4-12, item 50. 3
4. Rotate thD filtex ahaft 300 to cueck bath filtex shact vanes. This overtravel. is ieghtred fof the pawt to latet agetmat the keaper arm.



### 4.6.9 LATCH PAWL CLEARANCE (Field)

1. Hold slide arm assembly (Figure 4-13, item 1) to prevent excessive movement of the latch pawl (Figure 4-13, item 2).
2. Press the "H" key.
3. Check the vertical clearance (Figure 4-13, item 3) between latch pawl (Figure 4-13, item 2) and keeper arm (Figure 4-13, item 4) for a . $008 \pm .002$ inch clearance.
4. If this clearance is incorrect, loosen the two screws (Figure 4-13, item 5) mounting the keeper arm, and adjust the keeper arm for correct clearance.
5. Recheck the adjustment.

### 4.6.10 COMPLETION OF INTERPOSER LATCH SPRING ADJUSTMENT (Factory)

1. Press the "-" key.
2. Release the two right-hand screws on the latch spring.
3. Adjust the latch spring under the key interposer to maintain the clearance obtained in Step 3 of paragraph 4.6.9.
4. Tighten the extreme right-hand screw.
5. Press the "K" key.
6. Repeat Step 3.
7. Tighten the remaining screw.
8. Loosen the three screws on the left-hand latch spring.
9. Press the "G" key.
10. Repeat Step 3.
11. Tighten the right screw.
12. Press the "1" key.
13. Repeat Step 3.
14. Tighten left screw.
15. Press the "D" key.
16. Repeat Step 3.
17. Tighten the middle screw.
18. Check and tighten all screws mounting the switch bracket assembly upon completion of the adjustment.


Figure 4-13. Latch Pawl Clearance


Figure 4-14. Storage: Bar Adjusting Screws and Microswitches

## CAUTION

Do not readjust the pawl latch on the above adjustment.

### 4.6.11 CLEVIS ROD ADJUSTMENT (Facfory)

1. Place a . 013 inch feeler gauge between the end of latch interposer No. 1 (Figure 4-15, item 2) and its guide comb (Figure 4-15, item 3).
2. Connect an ohmmeter to common (C) and normally close (NC) terminals of microswitch No. 1 (Figure 4-14.)


Figure 4-15. Clevis Rod Adjustment

```
3. Loosen the 5/32" jam nut on link rod No. 1 (Figure 4-15, Item 4).
4. Using miniature grooved pliers (stock No. 954164) adjust the link rod
        (Figure 4-15, Item 5) until the ohmmeter indicates switch contacts open,
    (ohmmeter measures open circuit).
5. Grip the link rod and tighten the jam nut.
6. Recheck the adjustment by moving the link rod slowly forward and then allow
    the latch interposer (Figure 4-15, Item 2) to return slowly against a . O13
    inch feeler gauge and its respective guide comb (Figure 4-15, Item 3). The
    ohmmeter should still indicate switch contacts open.
7. Again move the link rod forward to its full travel.
8. Release the link rod, allowing the latch spring to return the link rod.
9. The ohmmeter should indicate microswitch closing. (Ohmmeter measures
    closed circuit.)
10. Repeat the above procedure for link rods No. 2 through No. 7.
```

4.6.12 SWITCH STORAGE TIME ADJUSTMENT (Field)

## CAUTION

Prior to making any adjustments to the storage bar and microswitches, ensure that the storage bar, (Figure 4-15, Item 6), the nylon block (Figure 4-15, Item 7), and the link rods (Figure 4-15, Item 5) are thoroughly cleaned of any trace of lubricants or dirt that could interfere with the free movement of the storage bar and the clamping action upon the microswitch link rods during storage time.

1. Loosen the two screws (Figure 4-15, Item 8; also referenced in Figure 4-14, Item 1) mounting the nylon storage block.
2. Loosen the jam nuts Figure 4-15, Item 9; also referenced in Figure 4-14, Item 3, and adjust the two screws (Figure 4-15, Item 10) until a . 030 inch clearance is maintained between the switch link rod (Figure 4-15, Item 5) No. 1 and No. 7 and the storage bar (Item 6).
3. Tighten the two screws (Figure 4-15, Item 8).
4. Plug the keyboard into the viewer assembly.
5. Connect an oscilloscope to the common (C) terminal of microswitch No. 1 (Figure 4-14).
6. Turn on the keyboard.


Figure 4-16. Bail-up Stop Adjustment
7. By pressing the "A" key; check the oscilloscope for +4.5 volt pulses. Tighten the two adjustment screws down on the bottom flange of the switch bracket until the pulse is approximately 38 to 48 milliseconds wide. Lock the jam nuts.
8. Perform the above procedure on microswitch No. 7.

## CAUTION

Proper storage should result in near equal clearance between the switch link rods and the storage bar. When the correct storage adjustment has been completed, tighten the two screws on the switch plate and the two jam nuts on the adjustment screw.
9. Check pulse time on switches 2 through 6 .

### 4.6.13 REINSTALLATION OF BAIL-UP STOP (Field)

1. Replace the bail-up stop (Figure 4-6, Item 5) removed in paragraph 4.6.7.
2. Adjust the bail-up stop to clear the latch bail rod so that it will pull the latch pawl (Figure 4-16, Item 1) down to accept a bite of $1 / 2$ to $3 / 4$ of the thickness of the keeper arm (Figure 4-16, Item 2).
3. Tighten the two mounting screws on the bail-up stop (Figure 4-6, Item 5).

### 4.7 ELECTRICAL ADJUSTMENTS

## Note

Card Extender (stock no. 938256) can be used to facilitate electrical adjustments and troubleshooting.

The following electrical and electro-mechanical adjustments are to be made as directed by the preventive maintenance procedures, when required after replacement, or as a maintenance operation.

### 4.7.1 DEFLECTION AMPLIFIER ADJUSTMENTS (Refer to Figure 4-16A.)

The seven adjustment controls for the Deflection Amplifier (A9) are located in the front of the Viewer behind the door at the right of the display tube.


Figure 4-16A. Maintenance Controls

1. If characters can be displayed proceed to Step 2; if not, align the Character Generator section as outlined in Paragraph 4.7.5.
2. Type the top line full with 54 characters and adjust the length of the line to $7-7 / 8$ inches using a flat, flexible ruler and the HORIZ GAIN control R4.
3. Type a character and the return character ( $\ll$ ) in each of the 20 lines and adjust the displayed page height to 6 inches using the VERT GAIN control R39.
4. Type the last line full of characters. Using the HORIZ CENTER and VERT CENTER (R22 and R56 respectively) center the displayed message and readjust the horizontal and vertical gain if necessary.
5. Recheck the vertical and horizontal size of the displayed message and readjust the horizontal and vertical gain if necessary.
6. Adjust the FOCUS, BRIGHT, and PICTURE controls for the best presentation of all characters.

### 4.7.2 VIDEO DRIVER, A12

The only adjustment on the Video Driver circuit board is the FORMAT data brightness control R53. This adjustment control is varied until the desired contrast between format data and variable data is reached. It will have no effect on the brightness of information that is NOT format data and will decrease the brightness of the format data. Note that when the BRIGHTNESS control R72 is set too high, there will be no contrast between the format data and the variable data, and the format brightness control R53 will be ineffective.

### 4.7.3 TICKLER DRIVER ADJUSTMENTS, All

The Tickler Driver adjustment controls are located on the Tickler Driver which is mounted above the CRT. The Tickler Driver adjustment procedure may cause the overvoltage protection circuit in the Low Voltage Power Supply to lock in.

1. Turn the power off and on to generate a parity error block.
2. Adjust the tickler GAIN control, R31 (the adjustment to the left when looking at the front of the Viewer) to obtain a parity error block 0.2 inches high.
3. On the Maintenance Panel, center the PICTURE control at mid-range, then adjust the tickler board COARSE PHASE control, (the adjustment to the right when looking at the front of the Viewer), R26, to obtain the best formed $E$, H, or - characters.

### 4.7.4 ELECTRICAL ADJUSTMENTS USING LINE MASK (REFER TO DRAWING 932817)

When the 20 line array is being used on the viewer screen, the line mask can be used to simplify the adjustments for line length, character, or parity error block size.

## Note

When using a new line mask, it may be necessary to trim the outside clear acetate border so that the blue area of the mask fits the bezel opening on the viewer screen.

## Line Length Adjustment

The viewing area of the mask is 5.6 inches by $7 / 8$ inches. One line of 54 characters can be adjusted horizontally to center in the $7 / 8$ inch cutout of the mask.

## Nofe

> Maintenance personnel should first establish the height of the 20 line raster by adjusting the VERTICAL SCAN potentiometer R14. The height of characters or parity blocks can then be established by adjusting the TICKLER SCAN control R31. Do NOT attempt to adjust character size by readjusting the VERTICAL SCAN potentiometer, R14, since this will change the vertical height of the 20 line raster which has already been set.

## Parity Error Block Check

The parity block height of 0.2 inch can be checked by measuring ten percent ( $10 \%$ ) above and below either line 10 or line 11.

## Vertical Scan Adjustment

When adjusting the height of the letter $M$ for the 0.14 inch measurement, adjust the VERTICAL SCAN adjust R43 until the letter M fills the dark area of line 10 or line 11.

### 4.7.5 HIGH VOLTAGE POWER SUPPLY, A13 (Factory)

The following adjustment procedure requires a high voltage probe and dc voltmeter.

WARNING
Use extreme caution when making the following measurements and adjustments as damage to the power supply and severe electrical shock may occur. Use a non-conductive tool when making this adjustment.

## CAUTION

Before the RCA DW-297 High Voltgae Probe is used with a WV-38A multimeter to measure the CRT anode voltage, ensure that the resistor has been installed in the probe handle. The resistor must be installed to extend the range of the meter to 25 kV ( 250 V range X 100 ). The probe stock number is 937524 and the resistor stock number is 937515.

1. Center the FOCUS control R12 at mid-range and adjust potentiometer $R 4$ at the front of the power supply using a non-conductive tool to obtain +12 kV at the high voltage anode lead on the CRT. Do not adjust over +12 kV .
2. Connect the meter to the high voltage lead going to the monoscope chassis and adjust trimpot R5 for -1.8 kV .
3. Measure +400 volts at TB1-7 in the High Voltage Power Supply to ensure proper operation of the High Voltage Power Supply.

### 4.7.6 CHARACTER GENERATOR ALIGNMENT

The controls to align the character generator section are located on the Selection Amplifier ( 9 controls) to the right of the display tube on the front of the Viewer assembly ( 2 monoscope controls) and, accessible through the lower door in the bottom of the front of the Viewer with your palms up. It will also be helpful to refer to the illustration of the character stencil, Figure 3-18.

1. Type the characters $G$ @ $G$ and adjust the @ symbol to the center with HORIZ GAIN control, R14 and HORIZ CENT control R15.
2. Adjust the VERT SKEW control R22, to place the @ on exactly the same line as the $G$ characters.
3. Type the characters \# l \# and adjust the [ symbol to the center with the HORIZ skew control, R82.
4. Adjust the VERT GAIN control R14 and VERT CENT control R15 to place the [ exactly on the same line as the \# sign (centered).
5. Turn the POWER switch on and off to generate a parity error. The parity error block should be 0.2 inches high; if not, refer to Paragraph 4.7.3.
6. Ensure that the horizontal lines are $7 / 8$ inches long; if not, refer to Paragraph 4.7.1.
7. Type an M next to one of the parity errors and adjust the VERT SCAN control R43 to obtain an $M$ of 0.14 inches high.
8. Move the mark under the $M$ and adjust the HORIZ SCAN control, R57, so that the mark extends approximately 10 percent on either side of the M .
9. Adjust the focus control of the monoscope $R 4$ (the one to the right), the intensity control of the monoscope R1, and the ASTIG control R102 to obtain the best formed characters.

### 4.7.7 DEFLECTION YOKE ALIGNMENT

1. Remove the covers from the viewer as outlined in Paragraph 4.5.1.
2. Set the POWER switch to "ON". Fill the top line of the viewer screen with the letter "T". Measure from the top of the first and last character to the bezel opening. Unequal measurements indicate the need for alignment of the deflection yoke. Proceed to step 3.
3. Set the POWER switch to "OFF" and remove the two screws from the rear of the CRT housing. Disconnect the video driver connector J12 and carefully slide the housing back until the forward end tab is clear. Tilt the housing cover to the right side of the Viewer while maintaining slack in the ground lead from the video board. Prop the housing cover clear of the CRT neck area.
4. Mark the yoke and housing tab immediately above with a fine pencil line. Loosen the yoke clamp screw and rotate the yoke slightly in the direction necessary to correct tilt observed in step 3. The yoke should be fitted firmly against the flare of the CRT.
5. While maintaining this position retighten the yoke clamp screw carefully.
6. Replace the housing cover and screws. Reconnect J12 to the Video Driver and repeat step 2.

### 4.7.8 INTERLOCK ADJUSTMENT

1. Remove the rear panel as outlined in Paragraph 4.5.1.
2. Turn interlock adjustment until Video Data Terminal can only be turned on when cover is in place.

### 4.7A TESTING

### 4.7A.1 BACK-TO-BACK TESTING

The $70 / 752$ VDT's can be tested back-to-back. The method that is used depends on whether the $70 / 752$ is a regular type or one with special features. Testing each of these VDT's is described in the following paragraphs.

## Local Operation

When a regular $70 / 752$ (Data Set Operation) is connected to a $70 / 752$ with the special feature (for Local Operation no Data Set) built in, a normal cable can be utilized. With this hookup, both of the 70/752's will always have their Write lights on. This is because the cable pin 13 acts as an "OR" function connecting both Write lights together.

## Normal (Remote) Operation

Testing regular type 70/752's (Data Set Operation) back-to-back is enabled by using a special cable, which is a modified normal cable. The normal cable is modified by reworking one of the connectors as follows:

```
Swap wires on pins 2 and 3. TD & RD
Swap wires on pins }6\mathrm{ and 20. DTR & DSR
Move wire from pin 4 to 15. RS - Blank
Move wire from pin 5 to 15. CTS - Blank
Add wire from pin 4 to 5. RS - CTS
Move wire from pin 13 to 14. WLT - Blank
```

When all connections are complete, tag or mark the connector to indicate that it has been modified. Except for the case described in "Local Operation" above, this special cable will allow testing 70/752's with all special features except Station Select. The paragraph below described how to test VDT's with this
feature.

## Off-Line Testing

$70 / 752$ VDT's with Station Select can be tested off-line by incorporating a few jumpers in conjunction with the modified special cable. The jumpers are used on the I/O No. 2 (A2) board to bypass the station select function. Place one jumper from $Z 25$ pin 10 to $Z 33$ pin 6 , and another from $Z 37$ pin 12 to $Z 11$ pin 4. Instali the modified cable as in previous VDT tests. The entire board can now be checked out, with the exception of the station select gates. If the VDT's work back-to-back, the problem will probably be with one of these gates. This solution can be verified by putting the VDT back on line for a few minutes in order to check out the station select gates. In the event the units do not work back-to-back after the above procedure, there will be no need to put the VDT on-line, as the problem is probably something other than the station select gates.

### 4.7A.2 TESTING PREAMPLIFIER 2100692-501

This test procedure simulates the engineering test procedure used to test the VDT preamplifier.

## Test Equipment Required

The following test equipment is required.

## Note

This test equipment shall be stocked at Region and District levels.

Oscilloscope, Tektronix 545 or equivalent with 1 X probe Signal Generator, H.P. 651A or equivalent Attenuator, Kay $30-0 \mathrm{db}$ or equivalent Power Supply, Harrison Lab, or equivalent Resistor, 100 ohms, $5 \%$, $\frac{1}{2} \mathrm{~W}$ Resistor, $1 \mathrm{kohm}, 5 \%$, $\frac{1}{2} \mathrm{~W}$ Test Jig (Copper Shielded)

## Preliminary Procedure

1. Connect the test equipment as shown in Figure 4-16B.

CAUTION

The +25 volt supply must be turned OFF when connecting or disconnecting the unit under test.
2. Turn ON the signal generator and adjust the 1.5 MHz signal for a 7.0 millivolt output as displayed on trace $A$ of the Oscilloscope. (Set attenuator at 23 db.$)$
3. Before connecting the power supply to the preamp turn it $O N$ and adjust the power supply output voltage to 25 volts ( $\pm 5 \%$ ).
4. Turn OFF the power supply and connect it to the unit under test as shown in Figure 4-16B.

## Test Procedure

1. Turn ON the +25 volt power supply and verify that the output is +5 volts.
2. On Oscilloscope trace $B$ the 1.5 MHz output signal shall be not less than 0.5 volts and shall not exceed 1.25 volts peak-to-peak.
3. Visually monitor the output signal on trace $B$ for a period of 1 minute. Verify that the amplitude of the output signal did NOT increase more than 10 percent.
4. With input to the unit under test open, a noise level of 70 millivolts peak-to-peak should be measured at the output on trace $B$ of the Oscilloscope.
5. Should the unit fail to meet the above parameters use standard troubleshooting techniques to isolate the faulty component.
6. Turn off all test equipment.
7. Disconnect test unit.


The following procedure is recommended for depot use only.

To use delay line 2188422-2, manufactured by Andersen Laboratories, Inc. in the '70/752 VDT, the following adjustments must be performed for proper operation. Once the 2188422-2 delay line has been adjusted using the following instructions, it should be re-marked as 2187310-3.

This procedure consists of two parts: Paragraph 4.7B. 2 Detector Threshold Balance and Paragraph 4.7B.3 Amplifier Gain Adjustment. The detector Threshold Balance adjustment must always be done first.

NOTE
Both PC boards (No. 1 and No. 2) must be adjusted using this procedure, first No. 1 and then No. 2. Complete both the Detector Threshold Balance and the Amplifier Gain Adjustments on PC board No. 1, and then repeat the procedure for PC board No. 2.

### 4.7B.1 TEST EQUIPMENT REQUIRED

Following is a list of the test equipment necessary for the adjustment procedure for converting delay line 2188422-2 to delay line 2187310-3.

1. Oscilloscope, Tektronix 545 or equivalent.
2. Oscilloscope Preamp, Tektronix 1 A1 or equivalent.
3. Probe X1, Tektronix P6028 or equivalent.
4. Probe X 10 , Tektronix P6006 or equivalent.
5. Pattern Generator, Data Pulse 202 or equivalent.
6. Plug-in Output unit, Data Pulse P901 or equivalent.
7. DC Power Supply +25 volts $\pm 2.5 \%$.
8. DC Power Supply -15 volts $\pm 2.5 \%$.
9. DC Power Supply +4 volts $\pm 2.5 \%$.
10. Crystal controlled frequency source $768 \mathrm{KHz} \pm 0.005 \%$.
4.7B.2 DETECTOR THRESHOLD BALANCE
11. Connect the delay line and test equipment as shown in Figure 4-16C. Enter a continuous ONES pattern into the delay line.


Figure 4-16C. Test Setup
2. On the PC board being adjusted (Figure 4-16D), place the X1 probe on Analog Data signal at junction of R4, R7, and C7, place the X10 probe on the Unclocked Data signal at the junction of R17, R20, and Z1-12. Refer to schematic diagram 5000-149-S.


Figure 4-16D. Test Points
3. While observing Unclocked Data, reduce signal gain by turning R4 (GAIN ADJ) clockwise until Unclocked Data just starts to flicker.
4. If data is only flickering on the high side (Figure 4-16E), turn detector balance potentiometer R14 clockwise to obtain as close to a symmetrical pulse train as possible. If data is flickering on the low side, turn R14 counterclockwise to obtain symmetry.


Figure 4-16E. High Side Flickering
5. Reduce gain again by turning R4 clockwise until flickering condition occurs. To obtain symmetry, it may be necessary to further adjust detector potentiometer R14 if flickering condition only occurs on either the high or low side.
6. Adjust gain potentiometer R4 and detector R14 alternately until equal flickering occurs on both high and low side of Unclocked Data simultaneously (Figure 4-16F).


Figure 4-16F. Correct Flickering
7. This completes the Detector Threshold Balance adjustments. Proceed with the Amplifier Gain adjustments for the same PC board.
4.7B.3 AMPLIFIER GAIN ADJUSTMENT

NOTE

> The Detector Threshold Balance adjustment must be performed before proceeding with the Amplifier Gain adjustment.

1. Connect the delay line and test equipment as shown in Figure 4-16C.
2. Enter a single ONE data pattern into the delay line.
3. Observe the Analog Data signal at the junction of R4, R7, and C7; observe the Unclocked Data signal at the junction of R17, R20, and Z1-12.
4. Adjust the Analog Amplitude, using GAIN ADJ R4, so that the Unclocked Data just begins to flicker.
5. Note the amplitude of Z to C , or the third lobe of the Analog signal (Figure 4-16G).
6. Adjust the gain of $R 4$ so that the $Z$ to $C$ amplitude noted in step 5 is doubled.
7. This completes the Amplifier Gain adjustment on the PC board being adjusted. Remember that both PC boards must be adjusted, first No. 1 and then No. 2.


Figure 4-16G. Analog Signal

### 4.8 TROUBLESHOOTING

A list of possible Video Data terminal troubles are given in Table 4-1 and 4.2. Along with these troubles are listed the possible causes and the corrective action needed to clear the problem. Figures 4-17 through 4-24 contain test point locations for all the logic boards. Figure 4-25 contains waveforms of the Video Data Terminal to be used for more detailed troubleshooting.

## Note

When troubleshooting the 70/752 VDT, always verify that the Keyboard is functioning properly and that the proper characters ASCII codes are being generated at the Keyboard before attempting to troubleshoot the Viewer unit electronics. Refer to Table 4-1 for Keyboard mechanical problems which can effect the electrical output of the Keyboard.

Table 4-1. Keyboard Mechanical Troubleshooting

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :--- | :--- | :--- |
| ExCessive motor <br> gear noise | Incorrect Drive_ <br> Train adjustment <br> Continuous <br> Operation <br> (erractic cycling) | Perform Drive-Train adjustment <br> procedure (paragraph 4.6.1) |
| 1. Maladjustment |  |  |
| of Latch Pawl |  |  |
| travel. |  |  |$\quad$| 1. Perform Keeper Arm and Latch Pawl |
| :--- |
| overtravel adjustment |
| (paragraph 4.6.8.) |

Table 4-1. Keyboard Mechanical Troubleshooting (Cont'd)


Table 4-2. Viewer Troubleshooting

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :---: | :---: | :---: |
| NOTE: | When one clear sym low-voltage power on the regulator b <br> 1. Lower the door <br> 2. Check pin 16 for <br> 3. Check pin 11 fo <br> 4. Check pin 14 fo <br> 5. Check pin 9 for | tom is not indicated, check the upply for correct voltages ard connector as follows: $\begin{aligned} & \text { f the low-voltage power supply } \\ & +75 \pm 2 \text { volts } \\ & +25 \pm 2.5 \text { volts } \\ & +4.5 \pm 0.75 \text { volts } \\ & -15 \pm 1.25 \text { volts } \end{aligned}$ |
| 1. Fan and keyboard motor do not operate. | 1. Relay Kl not energized. <br> 2. Keyboard Connectors disconnected. | 1. Close circuit breaker. Check that rear panel is secure. Verify that interlock switch is adjusted properly. (Refer to paragraph 4.7.8) <br> 2. Connect cable. |

Table 4-2. Viewer Troubleshooting (Cont'd)

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :---: | :---: | :---: |
| 2. WRITE switchindicator not lighted after being pressed. <br> 3. No mark in upper left corner is visible. | 1. Circuit breaker in rear not closed or interlock switch not closed. <br> 2. Lamp burned out. <br> Faulty deflection amplifier module, keyboard filter module, logic board, video driver module , tickler driver module, highvoltage power supply or Delay Line. | 1. Replace -4.5 volt fuse (F1) <br> 2. Replace lamp. <br> Depress SCREEN erase switch and master erase key simultaneously. If mark is displayed in middle of screen, replace deflection amplifier module A9. If mark is still not visible check the following points: <br> 1. Check module A21 pin 31 for logic pulses (waveform 1) at output of delay line. If pulses are missing depress SCREEN erase switch and master erase key simultaneously many times. If pulses are still missing, check input of delay line for logic pulses at J7-05. If pulses are present, replace the delay line. If logic pulses are still missing, replace logic boards A6, A5, A4, A3, A2 and A1 in sequence, one at a time. <br> 2. Check video driver module at A12E1 for pulses nominally at $+45 v$. If $+45 v$ pulses are missing, check module A12 connector pin 6 for approximately +2.5 v pulses. If the $+45 v$ pulses are missing and $+2.5 v$ pulses are present, replace video driver module A12. If the $+2.5 v$ pulses are missing, replace tickler driver module A11. <br> 3. Check TB1-7 of the high-voltage power supply for $+400 \mathrm{v} \pm 10 \%$. If the $+400 \mathrm{v} \pm 10 \%$ is present the highvoltage power supply is operating properly. If the $+400 \mathrm{v} \pm 10 \%$ is missing proceed to the following steps. |

Table 4-2. Viewer Troubleshooting (Cont'd)

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :---: | :---: | :---: |
| 3. (Continued) |  | 4. Check TB1-2 of the high-voltage power supply for -1 V to -2 V . If a positive voltage is present replace the deflection amplifier module, A9. <br> 5. Remove 12KV lead from CRT highvoltage button and verify that a nominal 12 KV is present. (Use highvoltage probe.) <br> 6. Check TB1-1 of the high-voltage power supply for a 19.2 KHz square wave. <br> 7. If items (3) or (5) are not present and items (4) and (6) are present, replace the high-voltage power supply. <br> 8. After verifying the above remove the CRT shield rear cover and verify that the CRT is warm. If the CRT is not warm, disconnect socket from CRT and check pins 1 and 12 of CRT for an open filament. Check pins 1 and 12 of connector for open filament transformer winding. |
| 4. Mark immovable | Function switches partially depressed. <br> Faulty logic board. | Release switches by pressing. If switches still partially depressed, replace matrix switch assembly in keyboard, or repair as required. <br> Replace module A4, A3, A2, and A1 in sequence, one at a time. |
| 5. Many marks displayed. | 1. Function <br> Switches partially depressed. <br> 2. Faulty logic board. | 1. Release switches by pressing. If switches still partially depressed, replace matrix switch assembly in keyboard, or repair as required. <br> 2. Replace module A4 or A5 or both. |
| 6. Erratic mark behavior. | Faulty logic board. | Replace module A4, A5, or A3, or all three. |

Table 4-2. Viewer Troubleshooting (Cont'd)

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :---: | :---: | :---: |
| 7. No character displayed. <br> 8. Incorrect character displayed. | Faulty logic board, highvoltage power supply, selertion amplifier module, or monoscope. <br> Keyboard malfunction. Misadjustment of selection amplifier, or faulty logic board. | 1. Verify that monoscope is plugged into connector. <br> 2. Check module A21, pin 31 and verify character code is present (refer to tavle 1-1). If character is not present, replace module A3 or A4 or both. <br> 3. Check module A12, pin 7 for character unblank (CU) signal. This signal will be high for character presence when typed in by the keyboard. If the unblank signal is missing replace module A3. <br> 4. If unblank signal is present, remove cover from monoscope housing (rear of viewer) and touch preamplifier input with finger to verify video output chain. Noise will be displayed in the number of character blocks that characters were entered. If noise is not displayed, replace the video preamplifier, A1OA1 or video driver module, A12. <br> 5. If noise is present but no characters are displayed, check E1 of high-voltage power supply for -1.8 Kv . If voltage is missing perform REMEDY items (3) through (7) Of SYMPTOM 3. <br> 6. If -1.8 Kv is present, replace selection amplifier module A8 or module A3 or both. <br> 7. Check that the filament of the monoscope is functioning. <br> 1. Replace keyboard. <br> 2. Check selection amplifier adjustment (refer to paragraph 4.7). <br> 3. Replace selection amplifier module A8. |

Table 4-2. Viewer Troubleshooting (Cont'd)


Table 4-2. Viewer Troubleshooting (Cont'd)

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :---: | :---: | :---: |
| c. Printer will not operate when print switch is pressed. | Faulty logic board. | Replace module A1, A2, or A6 or all three. |
| d. Cannot transmit or receive after being polled. | Faulty logic board. | Replace module A1 or A2 or both. |
| 14. Poor focus | Improper focus adjustment. Faulty dynamic focus module, high-voltage power supply, or CRT. | Adjust FOCUS (refer to paragraph 5.2.3. If focus cannot be adjusted replace module A20 or highvoltage power supply or both. If focus still cannot be adjusted replace the GRT. |
| 15. Character out of phase (double image). | ```PICTURE control or tickler driver module misadjusted.``` | Adjust PICTURE control on front panel. If unable to adjust perform the tickler driver adjustment (refer to paragraph 4.7.3. If still unable to adjust, replace module A11. |
| 16. No horizontal or vertical scan. | Faulty deflection amplifier module. | Replace module A9. |
| 17. Mark is bright and character is illegible. | Improper monoscope adjustment. | Adjust R1 or R4 or both on monoscope assembly voltage divider A1OA2. |
| 18. Characters shift on Viewer Screen | 1. Faulty High Voltage Power Supply | 1. Turn the INTENSITY control counterclockwise until characters on screen are dim. Quickly turn INTENSITY fully clockwise. When character shift is observed replace the High Voltage Power Supply (Unit A13). |
|  | 2. Faulty Selection Amplifier | 2. When no character shift is observed replace Selection Amplifier (Unit A8). |
| 19. Center bar on character E is dim and center bar of A is bright. | Faulty Driver output stage on Video Driver. | Replace Q17 on Video Driver (A12). |

Table 4-2. Viewer Troubleshooting (Cont'd.)

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :--- | :--- | :--- |
| 20. Noisy keyboard |  |  |
| microswitch |  |  |
| outputs. | 1. Vibration of |  |
| bail rods |  |  |
| due to exces- | Perform bail rod adjustment procedure <br> and all subsequent adjustments. <br> sive clear- <br> ance between <br> bail rods and | Noise outside of the sampling period <br> can be disregarded. <br> Replace faulty microswitch. |
|  | key interpo- <br> sers (check <br> with pencil <br> eraser). |  |
|  | 2. Faulty |  |
| microswitch. |  |  |

## Nofe

It is suggested that at sites with several $70 / 752$ VDT units, two separate maintenance logs be kept for both the Viewer Assembly and the Keyboards. The assemblies should be listed by serial numbers so that when keyboards are moved from one viewer to another as replacements the maintenance history of each assembly can be monitored for frequency of repetition of particular problems.


1/0 No. 1 Logic Board (A1) Test Points


70/752•0826

Figure 4-19. I/O No. 2 Logic Board With Station Selector Special Feature (A2) Test Points



70/752-0828

Figure 4-21. Mark And Data Insert Logic Board (A4) Test Points


Figure 4-22. Timing Logic Board (A5) Test Points


70/752-0830

Figure 4-23. Printer Terminator and Oscillafor Logic Board (A6) Test Points


LOCATION:
CH.A - A5,TP-3. 5
СН. B - АЗ, TP-26
SCALE:
HOR. - 1 usec/cm VERT. - CH.A $5 \mathrm{~V} / \mathrm{cm}$ CH: $\mathrm{B} \quad 10 \mathrm{~V} / \mathrm{cm}$
SYNC:
internal

LOCATION:
CH.A- A5,TP-3,5
CH.B - A3,TP-32
SCALE:
HOR. - 2 usec $/ \mathrm{cm}$
VERT. - $5 \mathrm{~V} / \mathrm{cm}$
SYNC:
INTERNAL

LOCATION:
CH.A - A3, TP-22
CH. B - A5, TP-3, 5
SCALE:
HOR. - 2 usec $/ \mathrm{cm}$
VERT. - $5 \mathrm{~V} / \mathrm{cm}$
SYNC:
AI2,PIN 6 CONNECTOR

LOCATION:
CH.A - All, Q13 baSE
CH.B - A11, Q15 BASE SCALE;

HOR: - 0.5 usec $/ \mathrm{cm}$
VERT. - CH.A $0.5 \mathrm{~V} / \mathrm{cm}$ CH.B $2 \mathrm{~V} / \mathrm{cm}$

SYNC.
INTERNAL

TBB(N) CH.A

RZ PULSE CH.B
4


CH.A


DPC(1P) CH.A TBB(N) CH.B



Figure 4-25. Troubleshooting Waveforms (Sheet 1 of 3)

SCALE:

HOR . -0.5 usec cm
VERT. - CH.A 5 V cm CH. B $50 \mathrm{~V} / \mathrm{cm}$

SYNC.
INTERNAL

### 1.53 MHz TICKLER <br> 1.53 MHz TICKLER

 COIL DRIVECH.A

LOCATION:
CH.A - All, Q4 BASE
CH.B - All, Q6 BASE
SCALE;
HOR. - 0.5 usec cm
VERT. - CH.A 10 V cm
CH. B 2 V cm
SYNC:
INTERNAL

INPUT TO TICKLER

TICKLER VERTICAL SCAN

LOCATION:
CH.A - A11, Q8 COLLECTOR
CH.B - A11, Q9 BASE
SCALE:
HOR. - 5 usec $^{\prime} \mathrm{cm}$
VERT. - $2 V^{\prime} \mathrm{cm}$
SYNC:
INTERNAL

LOCATION:
A21-31 (BOTH WAVEFORMS)
UPPER - WITH CHARACTER "A""
LOWER - WITHOUT CHARACTER
SCALE:
HOR. - 10 usec cm
VERT. - IV cm
SYNC:
INTERNAL


DLMIN (P)


SYNC BITS
INDEX MARK

Figure 4-25. Troubleshooting Waveforms (Sheet 2 of 3)

## LOCATION:

A12, PIN 6 CONNECTOR
SCALE:
HOR. - 10 usec/cm
VERT. - $0.2 \mathrm{~V} / \mathrm{cm}$
SYNC:
A9, R68

## LOCATION:

A12, PIN 16 CONNECTOR
SCALE:
HOR. - 10 usec $/ \mathrm{cm}$
VERT. - $0.2 \mathrm{~V} / \mathrm{cm}$
SYNC:
A9, R68

LOCATION:
A12-E1
SCALE:
HOR. - 5 usec/cm
VERT. - $20 \mathrm{~V} / \mathrm{cm}$
SYNC:
A9, R68
USE DELAY AND MULTIPLIER


INDEX MARK FROM VIDEO DRIVER


VIDEO TO CRT

Figure 4-25. Troubleshooting Waveforms (Sheet 3 of 3)

### 4.8.1 DELAY LINE TROUBLESHOOTING

The following troubleshooting procedure is applicable to the delay line manufactured by Laboratory for Electronics schematic, Dwg. No. 2039ACE23. When the alternate delay line, manufactured by Digital Devices (Dwg. No. 5000-105s) is used the following procedure may be used as a guide.

## Standard Conditions for Troubleshooting



## CAUTION

The output termination (resistor and capacitor R4 and C3) are mounted on the P.C. board. Because the output termination can vary from line to line, always have the terminating components remain with the delay line. Remove these components from the P.C. board and tape them to the Delay Line if the P.C. board must be replaced.

The Delay Line is mounted under the large stainless steel cover and is not to be disassembled. If the delay line is found to be defective, the complete delay line assembly must be returned for repair. The black and grey wires are the input wires and the black and red wires are the output wires.

## CAUTION

The green wire is connected to the case. Up to and including Serial No. 28039 the green wire was black. When there is no green wire, find the ground wire with the resistance meter.

All systems with a serial no. below 28070 will have the input terminating resistor and capacitor (R3, C1) mounted on the P.C. Board. All other units have these components mounted inside the Delay Line.

## CAUTION

If the signal at the test point is the opposite polarity of that in Figure 4-26 reverse the input or output leads (not both) connected to the delay line section.


Figure 4-26. Delay Line Input Wav eform

The anode of $C R 2$ must swing between ground and +25 vdc . If the anode is at steady ground level and the cathode of CR2 is at +25 vdc , it indicates that the irgut cransdicer coil is open. Remove the wires from the P.C. board and measure the: 1 esistance of the input transducers. It should be 11 ohms for delay lines l:p to serial no. 28070 or 700 ohms to 2 K ohms for delay lines with serial numbers ? 8070 and higher.

The cutu. voltaje of the delay line can be measured with the oscilloscope and should be between 1 and 2 millivolts. If no signal is found, measure the resistance of the output transducer, which should be about 45 ohms. If an open transduce is found, the complete delay line assembly should be returned for repair.

Delay I, ine vlectronics
Make sure the sitandard Test Conditions given in previous paragraph are set up.

## CAUTION

In case the P.C. board is damaged, it can ir replaced with another board. Hlowever, terainating trimming resistors and capacitors inust br: removed from the old board and must remain with the delay line and ke mounted on the new board. If possible, replace the delay system (delay line with electrunics) as a complete unit.

## Driver

The input signal will cause the base of $Q 1$ to swing from negative 0.5 v to positive $0.8 v$ and the collector of $Q 1$ from positive $25 v$ to $0 v$. If the input transducer is disconnected or defective, the collector will be at $0 v$. To test the driver, substitute a 1 K ohm resistor in place of the input transducer at the P.C. board.

The fall time of the negative going edge should be 50 nanoseconds or less. The rise time of the positive going edge should be 100 nanoseconds or less.

## Amplifier

The amplitude of the signal at the test point must be approximately +4 measured from baseline to peak.

The signal to noise ratio must be 3 to 1 or greater. The noise is defined as every signal outside the main lobe area and measured from the baseline to the maximum positive noise peak. (Refer to Figure 4-27.)


Figure 4-27. , Delay Line Test Point Waveform
If no signal is present, proceed with the following:

1. Short the input terminals with a clip lead and measure the voltage according to the following table. All readings should indicate within $\mathbf{I}^{10 \%}$.

C = Collector; $\mathrm{B}=$ Base; $\mathrm{E}=$ Emitter

|  | $C$ | $B$ | E |
| :--- | :---: | :---: | :---: |
| Q2 | 24 | 0 | $*$ |
| Q3 | 14 | $*$ | -1 |
| Q4 | 14 | $*$ | -1 |
| Q5 | 14 | $*$ | -1 |
| Q6 | 24 | 14 | 13.5 |

* These values can vary from negative 0.3 volts to negative 0.6 volts.

2. Remove the clip lead and measure the signal at the collectors of Q3, Q4, and Q5. The gain per stage should be about 17. If the gain of one of the stages is much less than 17, check the decoupling capacitors (C5, and C6, C7 and C8, or C10 and C11) for that stage.

Detector
With a signal at the test point and no output signal, the Detector must be at fault. The same AC signal as at the test point must be present at the junction of R22 and C14.

During no-signal periods, the signal baseline level should be 0.35 volts at the anode and cathode of Tunnel Diode CR3.

During the input pulse, the level must rise to about 0.8 volts at the anode of CR3.

If this signal is much smaller, CR3 is probably shorted. If this signal is much larger, Q7 is defective.

With a base-emitter short in Q7, the baseline at the Tunnel Diode Anode will be less than 0.35 volts and the high level will be lower also. The collector of Q7 should swing from +1.5 volts to +0.1 volts. If there is no output at Pin 9, either Q8 is defective, or a short external to the delay system exists.

Gain Adjustment
The only adjustment provided is the Gain Control located under the cover, closest to Pin 18 on the connector.

The Gain Control, R15, must be adjusted while watching the output signal at Pin 9. With the scope on positive internal triggering, the gain potentiometer must be rotated until the widths of all output pulses fall within a range of from 450 nanoseconds to 700 nanoseconds, measured at the $50 \%$ amplitude points. Recheck the test point signal level to ensure that the signal level is at least +3 volts.

## SECTION FIVE POWER

### 5.1 LOW VOLTAGE POWER SUPPLY (Refer To Figure 5-1.)

The Low Voltage Power Supply (L.V.P.S.) specifications are listed in Table 5-1.
Table 5-1. LVPS Specifications

| NORMAL OUTPUT VOLTAGE | MAXIMUM CURRENT | ADJUSTABLE TO |  | REMARK |
| :---: | :---: | :---: | :---: | :---: |
|  |  | MIN. | MAX. |  |
| +75 vdc | 0.35 amps | +73v | +77v |  |
| +25 vdc | 3 amperes | +22.5a | +27.5a |  |
| +4.5 vdc | 2.5 amps | +3.75a | +5.25a | OVER VOLT protection should be set to limit max. to 5.0 v . |
| -15 vdc | 2.5 amps | $-13.75 a$ | -16.25a |  |
| 6.3 vac | 0.6 amps | - | - | For monoscope, insulated for 2.5 K volts. |
| 6.3 vac | 0.6 amps | - | - |  |

### 5.1.1 INPUT POWER REQUIREMENTS

The input power required must be single phase, 48 to 62 Hz . The input transformer primary has seven taps which permit the use of the following ac voltages; $115,190,200,210,220,230$, or 240 vac.

## CAUTION

Before applying input power, check the connection of the transformer input voltage to ensure that the proper primary tap has been connected to the a.c. system voltage on TB 5 terminal 6, (the output side, pin 1 of relay K1).

The input power is applied through interlock S1 to the Control Panel Power Switch. The power switch output controls relay K1 which applies power to the VDT System.

### 5.1.2 INPUT TRANSFORMER

The L.V.P.S. circuit consists of an input Transformer T1 which contains six secondary windings. Two windings generate 6.3 vac. The first winding supplies power to the Viewer CRT filament, while the second winding supplies 6.3 vac to the monoscope tube filament.

### 5.1.3 CONTROLS AND INDICATORS

The Low Voltage Power Supply circuit breaker, CB1, is located on the rear panel of the $70 / 752$ Viewer Assembly. An indicating rod extends through the rear panel. When an overload occurs, the circuit breaker may be reset (after the cause of the overload has been removed) by pressing the indicator rod when the tripping element has cooled.

### 5.1.4 DC RECTIFIERS

The remaining four secondary windings are connected to four full wave bridge rectifiers which generate the following d.c. voltages: $+75,+25,+4.5$ and -15 vdc. Each of the rectifiers generate a dc output approximately 1.1 times the desired dc voltage output, to compensate for the voltage drop in the $R C$ filter on the rectifier output.

### 5.1.5 SERIES VOLTAGE REGULATION

The Low Voltage Power Supply contains four series voltage regulators. Since all four regulators are similar, only the +4.5 volt regulator is explained. The circuit consists of a series regulator Q5, a differential amplifier Q11 and Q12, and a triple Darlington amplifier consisting of 96,9 and 10 . In addition to the basic series regulator components, the +4.5 volt circuit contains an overvoltage protection circuit consisting of a silicon controlled rectifier, CR17, a reference zener CR5, and three amplifiers Q17, 18 and 19.

## Series Requlator

The filtered output from the rectifier is applied through fuse $F 1$ to the emitter of the regulator $Q 5$. The emitter output of $Q 5$ is connected to the output filter capacitors (C6, 7, and 11) and to the sensing divider for the differential amplifier.

## Differential Amplifier

One input to the differential amplifier is connected to ground as a reference level and the other input is connected to the wiper of potentiometer R36 in the sensing divider.

> Note
> The reference level in the other three regulators are referenced to a zener voltage generated by CR2.

The output of the differential amplifier is applied to a triple Darlington amplifier ( $Q 6,9$, and 10) which controls the base drive of the series regulator, Q5.


## Circuit Operation

When a load is placed on the output, the current drain through the series regulator tends to decrease the output voltage level. This lower voltage level is sensed by the differential amplifier and is amplified and applied to the Darlington amplifier. The triple stage Darlington produces sufficient base drive to increase conduction of the series regulator $Q 5$. The increased conduction supplies sufficient current to the load and the output voltage rises to the level controlled by the adjustable level of the sensing potentiometer R36. When the load on the output decreases, the output voltage rises and the error is amplified and applied to the series regulator base to decrease conduction and lower the output voltage to the correct level.

## Overvoltage Protection Circuit

The function of the overvoltage protection circuit is to prevent any excessive overvoltage condition from damaging components such as integrated circuits which are connected to the +4.5 volt supply output. The circuit consists of silicon controlled rectifier CR17, a reference zener CR5, a potentiometer R55, and a three stage amplifier consisting of $Q 17,18$, and 19.

## Circuit Operation

When an overvoltage condition occurs, the increase in voltage is sensed and amplified by transistor Q19 and applied to the two stage Darlington amplifier (Q17 and 18). When the overvoltage is sufficient to cause the output of 017 to reach the firing voltage of the silicon controlled rectifier (SCR), CR17 fires (crowbars) and shorts the +4.5 volt output directly to ground. This causes sufficient current drain to blow the input fuse F1 within seven seconds.

The SCR will remain fired until the supply has been turned off. After clearing the cause of the overvoltage, the supply can be turned on and the SCR will remain off unless another overvoltage causes it to fire.

### 5.1.6 ADJUSTMENTS

## Note

The Low Voltage Power Supply adjustments and test points are located on the regulator circuit board and are accessible when the side plate is lowered.

## Preliminary

Connect a digital voltmeter to the ground (-) terminal and terminal E2 (+).

## Plus 75 Volt Adjustment

1. Apply power to unit.
2. Adjust the +75 VOLT ADJUST potentiometer, R12, until the voltmeter indicates +75 volts.
```
1. Remove digital voltmeter lead from terminal E2 and reconnect to terminal E3.
2. Adjust the +25 vOLT ADJUST potentiometer R25 until the voltmeter indicates
    +25 volts.
3. Turn off input power.
Plus 4.5 Volt Overvoltage Adjustment
1. Remove the digital voltmeter lead from terminal E3 and reconnect it to ter-
    minal E4.
2. On fuseholder XF1 connect terminals 1 and 2 together with a short jumper.
3. Turn on input power to unit.
4. Turn OVER-VOLTAGE ADJUST potentiometer R55 fully clockwise.
5. Adjust +4.5 vOLT ADJUST potentiometer until the voltmeter indicates +5 volts.
```


## CAUTION

```
Prepare to turn off unit input power immediately
after the crowbar circuit fires. Read the next
step carefully before performing.
```

6. While monitoring the digital voltmeter, slowly turn the OVER-VOLTAGE ADJUST potentiometer R55 counterclockwise until the SCR fires as indicated by a sudden decrease in the voltmeter indication to approximately 2 volts. Immediately turn off the input power to avoid damage to the unfused circuit.
7. Turn +4.5 VOLT ADJUST potentiometer R36 fully counterclockwise.
8. Remove the jumper wire from fuseholder XF1 terminals.
9. Turn on input power.

## CAUTION

In the following step do NOT allow the +4.5 volt output level to exceed +5.0 volts since this will activate the overvoltage (crowbar) circuit and blow the fuse.
10. SLOWLY adjust the +4.5 VOLT ADJUST potentiometer until the voltmeter indicates +4.5 volts.

1. Connect the negative lead of voltmeter to terminal $E 5$ and the positive lead of voltmeter to ground.
2. Adjust -15 VOLT ADJUST potentiometer $R 48$ until the voltmeter indicates 15 volts at the -15 volt circuit output.
3. Turn off unit input power and remove the voltmeter leads.
4. Replace the side plate.

### 5.2 HIGH VOLTAGE POWER SUPPLY, ASTRO-METRIX MODEL AMC-M-227

### 5.2.1 GENERAL

The High Voltage Power Supply Model AMC-M-227 has been issued in five different versions (Figures 5-2 and 5-3). Table 5-2 lists the variations of the power supply.

Table 5-2. Astro-Metrix Power Supply Revisions

| AMC-M-227 <br> REVISION LEVEL | ELECTRONIC MODIFICATION |
| :---: | :---: |
| REV A | The original revision "A" supplies have been recalled for modifications. |
| REV B | In the "B" version, capacitors C6 and C7 values were changed to . 002 uf at 6 kv rating. |
| REV C | Zener diodes CR1 and CR2 were removed and a tap was added to Transfermer T1. CR3 was also removed. |
| REV C-SC | The C-SC (short circuit protection) version had the following changes: R23 changed to 5 ohm 5W; R2 (on H.V. Rectifier No. 600749) changed to 1.5 Meg .2 W ; CR12 added across base emitter of $Q 16$ (on H.V. Regulator No. 600752). |
| REV D | Removed capacitor C2 (. $002 \mathrm{uf}, 6 \mathrm{kv}$ ) from 6 kv post E1. Changed value of $C 7$ on assembly no. 600749 to .005 uf at 3 kv rating. Q9 and Q11 drive transistors were changed to RCA part. Colored wire was used in all REV D supplies. |

## Note

Best estimates indicate that all original Revision "A" versions have been recalled for modifications up to the Revision "D" version. Some "B" versions may still be in use. The "C" and "C-SC" versions are similar with the exception of the Short Circuit protection which has been added to the Revision "C-SC" version. The Revision "D" version is electrically similar to the Revision "C-SC" version.

### 5.2.2 THEORY OF OPERATION

The AMC-M-227 Power Supply Block Diagram shown in Figure 5-4 is valid for all five versions except as noted in the following description. The inputs required for the supply are shown in Table 5-3. The Power Supply generates the outputs shown in Table 5-4.

Table 5-3. Input Requirements

| TB1 TERMINAL | INPUT |
| :---: | :--- |
| 5 | +25 VDC |
| 3 | -15 VDC |
| 1 | 19.2 KHz Square Wave <br> (H.V. ENABLE from Unit A5) |
| 2 | SWEEP FAIL (From Unit A9) <br> Focus Input (From front |
| 4 | panel adjust) 0-400 V. <br> Common |

Table 5-4. Power Supply Outputs

| OUTPUT | TERMINAL |
| :--- | :--- |
| +400 vdc | TB1-7 |
| +12 Kv | On H.V. Lead Cap |
| -1.8 Kv | On Post E1 |
| FOCUS OUTPUT <br> $(1.5-1.95 \mathrm{Kv})$ | On Post E2 |

## WARNING

E3 and E4 are tie points for the 6.3vac supplied to the monoscope filament, and are at a potential of -1.8 Kvdc .


Figure 5-2. Astro-Metrix HVPS Schematic (Rev. C, CSC, D)



## Circuit Safety Features

The High Voltage Power Supply is interlocked to the VDT system in two ways to prevent damage to the Viewer CRT phosphor:

1. When a clock failure occurs in A5.
2. When there is a loss of Horizontal Sweep from the Deflection Amplifier, A9.

When either failure occurs, the High Voltage Power Supply outputs are turned off.

## Inverter Switch Drive Frequency (Refer to Fiqure 5-4)

The 19.2 KHz square wave (H.V. ENABLE) from the A5 timing card is used as the drive frequency for the inverter switch transistors Q2 and Q13. The inverters generate opposite phased square waves to drive the push-pull drivers, Q9 and Q11, connected to the transformer's primary. Note that loss of the $19.2 \mathrm{KHz} \mathrm{H} . \mathrm{V}$. ENABLE square wave from the timing card A5 will automatically cause the H.V.P.S. outputs to drop to zero volts.

## Sweep Fail Circuit

The input to the sweep fail transistor, Q14, is a negative level. developed in the Deflection Amplifier's Horizontal Sweep Circuit (A9), which holds the base of Q14 cut-off during normal operation. When a horizontal sweep failure occurs, the negative level is no longer generated, and a positive level (through R2) is applied to the base of Q14 turning on the transistor and shorting the output of Q2. This inhibits the $19.2 \mathrm{KHz} \mathrm{H} . \mathrm{V}$. ENABLE from being applied to the Transformer T1, thus cutting off all outputs of the H.V.P.S. unit.

## +400 V Requlation Circuit

The +400 v secondary winding of Transformer $T 1$ (pins 6 and 8 ) is connected to a full wave bridge rectifier consisting of CR7, 8, 9, and 10. The +400 v output of the rectifier is connected to TB1, terminal 7, and is also applied to the +400 volt regulator Error Amplifier consisting of transistors Q1 and Q15. The Error Amplifier is referenced to a temperature compensated zener (CR1) through the +400 ADJ potentiometer R4. The output of the +400 volt Error Amplifier (at Q7) is applied to the cathode of a pair of diodes (CR5 and 6), and each of the diode anodes is connected to the base of one of the transformer primary driver transistors to control the gain of the drivers by furnishing a dc level, which controls the amplitude of the square wave current pulses applied to the primary winding and thus controls the resulting +400 volt dc output.

## +12 Kv Requlation

The Transformer $T 1$ is designed so that there is a good coupling efficiency between the +400 secondary winding and the high voltage winding for the +12 kv (and the -1.8 kv ). Any change in loading of the 12 kv output affects the +400 volt supply output and is corrected for by the +400 volt regulator circuit.

## +12 Kv Rectifier-Filter

The high voltage secondary winding (T1 terminals 1 and 3) produces a peak-to-peak voltage of 3 kv which is applied to a voltage quadrupler to generate the +12 kv output. The +12 kv is applied through a capacitive input filter and an R-C output filter, to the output terminal, pin 3 of the High Voltage Rectifier Assembly, and to the high voltage lead cap.

## Focus Output Circuit

The focus output level is generated by a voltage divider which is connected to the output of the first voltage doubler of the 12 kv voltage quadrupler. Adjustment of the FOCUS OUTPUT potentiometer will vary the output (at terminal E2) from 1.5 kv to 1.95 kv . Note that the focus input from the front panel adjust is connected to the lower end of the divider. This gives the VDT operator a vernier control that can vary the focus output from zero to +400 volts. A clamp, diode CR1, located on Terminal Board TB1 prevents the focus input from rising above +400 volts.
-1800 Volt Rectifier Circuit
The transformer high voltage secondary winding is tapped for a -2100 volt output (terminals 1 and 2). The -2100 volt tap (T1-2) is connected to the -1800 v halfwave rectifier, CR5, located on the High Voltage Rectifier Assembly No. 600749. 'l'he rectified voltage is applied to a capacitive input pi filter and the resulting -1800 volt level is applied to output terminal E1.

## -1800 Volt Requlation

The -1800 volt regulation circuit consists of an error amplifier (Q3 and Q16), connected to the same reference zener (CR1) used by the +400 v error amplifier. A divider consisting of R 3 through R6 located at the -1800 v output applies a feedback sample to the error amplifier input at the base of $Q 3$. The -1800 volt $A D J$. potentiometer (R5) also connects the base of $Q 3$ to ground and provides an adjustment of the amount of feedback to Q3. The error amplifier output is applied through $Q 5$ to the ground return pass element $Q 8$. Variations in the -1800 output voltage are sensed on the feedback line and the error amplifier controls the conduction of the pass element so that the voltage of the collector of $Q 8$ will vary from -150 v to -300 v and maintain a constant -1800 volt output at terminal post E1.

## Note

Diode CR12, located across the emitter base terminals of the error amplifier Q16, functions as short circuit protection for the pass element Q8.

### 5.2.3 INSTALLATION

## CAUTION

> Use extreme caution during handling to ensure that the components and circuit boards are not damaged and that wiring is properly routed. The -1800 volt and focus output leads must be routed to clear the High Voltage Board by at least the distance between terminals E1 and E2.

During installation, ensure that the chassis mounting hardware is tightened securely to make a good ground connection to the VDT chassis.

## Adjustments (Factory)

Normally all adjustments shall be made at the factory. Adjustments should be made by field personnel only when replacement of critical components, such as the reference zener, causes a large enough change in the output levels that system performance will be affected.

## CAUTION

When performing the +400 v and 12 kv adjustment, do NOT short the wiper of R4. Use a non-conductive tool when making the adjustment because the screw driver slot is connected to the wiper of the potentiometer.
+400 v and +12 kv Adjustment

## CAUTION

> Note that the adjustment of the +400 volt supply also effects the 12 kv output. Do NOT overadjust the +12 kv output. During adjustment, monitor both voltage levels simultaneously to ensure against any overvoltage condition.

While monitoring the +400 and 12 kv outputs, adjust R4, +400 ADJ located on the High Voltage Regulator Board to obtain a +400 volt output at TB1 pin 7 .

Focus Adjust (Factory)

1. Set front panel FOCUS potentiometer R74 at the center of its range.
2. Adjust FOCUS potentiometer R12, located on the High Voltage Rectifier Board
to obtain optimum focus of characters on Viewer screen. (Nominal voltage
at output terminal post $E 2$ should be approximately +1750 volts.)
3. Turn front panel FOCUS potentiometer R74 fully counter clockwise. The voltage at E2 should decrease.
4. Turn front panel FOCUS potentiometer fully clockwise. The voltage level at E2 should increase.

## Note

This will give the VDT operator a vernier adjustment of the Focus voltage at the front panel.
5. Adjust the front panel FOCUS potentiometer (R74) for the best presentation on the viewer screen.
6. Note that the voltage monitored at Terminal E2 is near mid-range (between 1.5 kv and 1.95 kv$)$.

## -1800 Volt Adjustment (Factory)

1. Monitor the -1800 volt output at Terminal E1.
2. Adjust the multiturn trimpot $\mathrm{R} 5,-1800 \mathrm{~V} A D J$, located on the High Voltage Regulator board to obtain -1800 volts at Terminal E1.

### 5.2.4 MAINTENANCE

## CAUTION

Do not use a cleaning device that may damage the power supply components.

1. Dust and other foreign matter shall be removed from the H.V.P.S. by lightly blowing with an air hose.
2. Check the supply wire routing and the condition of the insulated High Voltage leads.

Table 5-5. HVPS Troubleshooting Chart

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :--- | :--- | :--- |
| No voltage at any of the | 1)Shorted primary driver <br> H.V.P.S. outputs and <br> excessive current being <br> drawn from +25 volt <br> power supply (greater <br> than 1.0 amp). | primary input circuit. |$\quad$| transistors (Q9 and |
| :--- |
|  |

Table 5-5. HVPS Troubleshooting Chart (cont'd.)

| MALFUNCTION | POSSIBLE CAUSE | CORRECTIVE ACTION |
| :---: | :---: | :---: |
| All H.V.P.S. outputs low or zero. | 1) Sweep fail negative level missing or positive. <br> 2) +25 V or -15 V input voltages low or zero. <br> 3) Loss of H.V. ENABLE (19.2 KHz Drive Frequency). | 1) Check sweep fail output at Deflection Amplifier (Unit 9). <br> 2) Check Low Voltage Power Supply (Unit A14). <br> 3) Check Timing Card, A5, H.V. ENABLE output. |
| No load regulation on all outputs | 1) Check three causes above. <br> 2) +400 volt regulator loop problem. | 1) Perform appropriate Corrective Action above. <br> 2) Check +400 V regulator loop with Oscilloscope for proper signal flow and voltage levels in the following sequence: <br> a. Error Amp (Q1 \& Q15) <br> b. Amplifiers $(Q 4,6,7)$ <br> c. Switch control diodes (CR5 and 6) <br> d. Inverter Switches (Q9 and 11) <br> e. Reference Zener CR1 <br> f. +400 volt rectifier and filter components (CR7-10, and C1) |
| No regulation of - 1800 volt output only (other outputs normal) | 1) Ground pass element (Q8) failure. | 1) Check - 1800 volt regulator circuit with oscilloscope in following sequence: <br> a. Error amp (Q3 and Q16) <br> b. Short circuit protection diode (CR12) <br> C. Amplifier (Q5) <br> d. Ground Return Pass Element <br> e. Check -1800 volt Rectifier (CR4) and associated filter (C6 and C7). |

### 5.3 HIGH VOLTAGE POWER SUPPLY, ITT/IPD KV3214

### 5.3.1 GENERAL

This sub-section provides information on the function, installation and operation, theory and maintenance, of a Multi-Output High Voltage Power Supply. A complete parts list is included in Appendix B. Maintenance and troubleshooting is described in sufficient detail to enable a service technician to calibrate and perform routine maintenance on the equipment and in case of failure to make an intellignet appraisal and evaluation of the possible source of malfunction, and to take appropriate correction measures in the shortest possible time.

## Description

The ITT/IPD KV3214 Multi-Output High Voltage Power Supply is a completely solid state device designed to provide accelerating potential for a character monoscope and display CRT, first anode and cathode bias, and second anode and focus voltage.

## Physical Specifications

3.98" High
5.75" Wide
8.44" Long

Electrical Specifications - (Refer to Table 5-6)
Table 5-6. Electrical Specifications (ITT HVPS)

| INPUT POWER |  |  |
| :---: | :---: | :---: |
| Voltage <br> dc ( $\pm 2 \%)$   Peak to Peak <br> Ripple (mv) Maximum   <br> +25 100   <br> -15 100   <br> +75 100   | 0.8 |  |

INPUT SIGNAL

Signal Waveform: Square wave, symmetrical within 0.5\%.
Frequency: $19.2 \mathrm{KHz} \pm 0.3 \%$.
Amplitude: $+2.7 v$ minimum amplitude wj.th a driving source capable of delivering at least 1.Oma.

Sweep Failure: With $+0.7 v$ minimum all outputs will collapse to $0 v \pm 5 \%$ of nominal voltage.

Focus Input: +55 to +400 v with a minimum input resistance of 100 Kohms .

```
Output Signals - (Refer to Table 5-7 )
```

Table 5-7. Output Signals (ITT HVPS)

| MONOSCOPE ACCELERATING POTENTIAL |
| :---: |
| Voltage: -1800 volts nominal, adjustable to within $1 \%$ of nominal. Current: $1 \mathrm{ma} \pm 20 \%$ at a voltage of 1800 v (no transient loading). Regulation, Ripple and Drift: The sum of regulation, ripple and 30 day drift is less than $\pm 0.4 \%$. |
| FIRST ANODE AND CATHODE BIAS |
| Voltage: +400v $\pm 5 \%$ <br> Current: 1.0ma $\pm 10 \%$ <br> Regulation and Ripple: The sum of regulation and ripple is less than $\pm 1.5 \%$. |


| SECOND ANODE |
| :---: |
| Voltage: $+12 \mathrm{kv} \pm 5 \%$ <br> Current: 10 to 40 ua average including regulation plus leakage. <br> Regulation, Ripple and Drift: The sum of regulation ripple and 10 hour drift is less than $0.625 \%$ (applies over the temperature range $21^{\circ} \mathrm{C}$ to $38^{\circ} \mathrm{C}$ ). |
| FOCUS |
| Voltage: $+1750 v$ nominal, adjustable over a range of $\pm 250 \mathrm{v}$ from nominal (adjustment range should be measured with focus input set at $+175 v$ ) <br> Current: Will not accommodate loading other than leakage. |

```
Environmental - (Refer to Table 5-8)
```

Table 5-8. Environmental Specifications (ITT HVSP)

| ALTITUDE |
| :---: |
| Operating - Sea level to 7,500 feet. |
| Non Operating - Sea level to 12,000 feet. |

Table 5-8. Environmental Specifications (ITT HVSP) (cont'd.)

| AMBIENT TEMPERATURE |
| :---: |
| Operating - $+5^{\circ} \mathrm{C}$ to $55^{\circ} \mathrm{C}$ <br> Non Operating - $-18^{\circ} \mathrm{C}$ to $+65^{\circ} \mathrm{C}$ |
| VIBRATION |
| Operating - 5-35.5cps @ .060" DA <br> Non Operating - 35.5 - $300 \mathrm{cps} @ 1.56 \mathrm{Gs}$ |
| SHOCK |
| 1 G for $11 \pm 1$ millisecond |

### 5.3.2 INSPECTION

After unpacking the unit from its shipping carton, inspect for damage. Remove the perforated cover and inspect the unit in accordance with the following procedure:

1. Visually inspect transformer pies and circuit boards for damage.
2. Inspect to see that transistor heat sinks are in place and not touching each other.
3. Inspect all screw terminals for loose or missing screws. If a screw is missing be sure it is not in the internal part of the unit before applying power.

### 5.3.3 OPERATION (Refer To Figure 5-5.)

## Signal Input

The 19.2 KHz square wave HV ENABLE input from unit A5 is amplifier by $Q 7$ and emitter follower coupled by $Q 8$ to the driver transformer T1. The driver transformer provides a push-pull signal to the output transformer $T 2$. The secondaries of the output transformer, in conjunction with the rectifiers, provides the dc voltage for the $+400,-1800$, and +12 kv regulators.

## 12 Kv Supply

The 12 kv is obtained from a half wave voltage quadrupler consisting of C 10 , C 11 , C12, C13 and CR7, CR8, CR9, CR10. The base voltage of Q21 is established by the zener CR2 and is compared against the base voltage of 820 . The base voltage of $Q 20$ is obtained from a divider R38, R39, R41 and R42 with Q19 providing the



impedance matching. R41 is a screwdriver adjustment which determines the percentage of voltage division that appears at $Q 20$ and thereby determines the total voltage across the divider.

The voltage difference between the two bases of $Q 20$ and $Q 21$ appears as an amplified error signal at the collector of Q20. The amplified error signal is dc coupled to the base of the emitter follower 86 . The emitter of $Q 6$ controls the collector voltage of $Q 8$ and $Q 9$ and thereby controls the voltage to the primary of the driver transformer thus controlling the dc output to correct any difference in voltage between the two bases of Q20 and Q21.

## -1800v Supply

The differential stage in the -1800 volt supply consists of $Q 16$ and Q17 and compares the grounded base of $Q 16$ to a tapped down voltage referred to +18 v supplied by zeners CR1 and CR2. Q18 provides the high impedance coupling between the voltage divider R29, R30, R32 and R36 and the base of Q17.

The amplified error signal from the differential comparator is further amplified by Q15. The collector of $Q 15$ can algebraically add up to +400 v to the -1800 in the right direction to correct any difference in voltage between the two bases of the differential comparator. CR5 protects $Q 15$ from over voltage by clamping its collector to +400 v .

## +400v Supply

The error signal from the differential comparator $Q 3$ and $Q 5$ is applied to the base of the series regulator Q4, causing it to change its collector emitter resistance in accordance with its emitter base voltage. $Q 1$ and $Q 2$ are being used as zener diodes and cause a greater change to appear at the base of 05 than will appear at the base of $Q 3$ which is connected to the voltage divider R4 and R5.

## Sweep Fail

The collector Q10 is connected to the collector of $Q 7$ and is virtually out of the circuit as long as a negative voltage on its base created by the sweep signal is present. In the absence of the sweep signal the base of Q10 is pulled positive by R17, turning it on and clamping the collector of $Q 7$ to ground and blocking the input signal, thus causing all output voltage to collapse.

## Focus Control

A voltage divider consisting of resistors R49, R50, R52, and R51 connected between the 6 kv point of the 12 kv output and the focus input provides a focus output at the arm of $R 50$ variable from $+1500 v$ to +2000 v with a focus input of +1750 . The low side of $R 52$ is clamped to 400 v as a safety feature should the focus input become disconnected.

### 5.3.4 ADJUSTMENTS

There are two adjustments in the unit, one for the +12 kv and one for the -1800 v . They should be adjusted only when the unit is operating correctly and all voltages have the proper loads. Since the 12 kv controls the input to the step up transformer it should be adjusted first. Figure $5-6$ shows proper connections and loads for bench testing the supply.

### 5.3.5 TROUBLESHOOTING

The following paragraphs contain general information to methods of localizing troubles. The detection and repair of defective circuits can be facilitated by making voltage and resistance measurements or signal tracing with an oscilloscope, with the aid of the schematics.

If the unit fails to operate, first check for proper connections of power supply voltages and input signal. With an oscilloscope check for signal at the collector of Q7; it should be 23 v PP squarewave. Next check for signal at emitters of Q11, Q12, Q13 and Q14. Should one or more of these transistors be damaged, check first for signs of arcing or corona. After replacing transistors check for arcing again in a completely dark room with the unit operating.

If the -1800 v fails to regulate, first check the calibration of the +12 kv . Next check calibration of $-1800 v$; then check voltage at collector of Q15. This voltage should be between 75 v and 350 v with normal load and proper calibration.

### 5.3.6 OPERATIONAL CHECKS

## Test Equipment Needed



1. Connect Power Supply as shown in Figure 5-6.
2. Apply power to unit under test and allow five minutes warm up.
3. Adjustment of each output
a. Adjust R 41 for $+12 \mathrm{kv} \pm 5 \%$ on electro static voltmeter model ESH.
b. Adjust R 32 for $-360 \mathrm{v} \mathrm{I}_{1 \%}$ on differential voltmeter. (Note: 360 v at 450 K tap equals 1800 v @ output).
c. Observe voltage on VOM reads $400 \mathrm{v} \pm 5 \%$.
4. Load Regulation

## Note

Voltage dividers on the outputs as shown on Figure 1 are minimum loads.
a. Short out 900 meg section of voltage divider connected across 12 kv and observe change of 12 kv , -1800 and 400 v .
b. Short out 240 K section of voltage divider across +400 v and observe that 400 v stays within $5 \%$ of 400 v .
c. Connect 417 meg resistor across -1800 v output and observe that the reading on differential voltmeter can be adjusted back to within $\mathbf{I}_{1 \%}$ of 360 v .
5. Ripple
a. Connect Tektronix 453 scope probe ac coupled directly across $+400 v$ output read PP ripple on scope.
b. Connect . Oluf capacitor across 1800v. Connect probe of scope (dc coupled) to ground side of capacitor. Disconnect capacitor from ground and read PP ripple on scope.
c. Connect 500pf capacitor across output of 12 kv . Connect probe of scope (dc coupled) to ground side of capacitor. Disconnect capacitor from ground and read PP ripple on scope.
6. Sweep Fail
a. Remove ground wire from TB 1-2 and observe all outputs collapse to within $5 \%$ of 0 volts.
7. Focus Output
a. Connect VOM to TB 1-8 and adjust pot for +175 v .
b. Connect electrostatic voltmeter ESD to focus output E2. Adjust R50 through its full range. Excursion should cover 1500v-2000v.


The power supply theory originally on pages 5-29 thru 5-36 has been deleted and the 2166024-503 supply theory is now covered in the power supply manual 70-01-SPS.

## SECTION SIX TOOLS AND TEST EQUIPMENT

### 6.1 GENERAL

Due to servicing philosophies and the nature of the Model $70 / 752$, two sets of test equipment are required; one for Field Maintenance and one for the Maintenance Center. The Field Maintanance test equipment will consist of portable test equipment (Table 6-1). The Maintenance Center test and repair equipment will consist of standard test equipment (Table 6-2).

### 6.2 TEST EQUIPMENT CALIBRATION FREQUENCY

The test equipment used should be regularly calibrated to assure the accuracy of measurements. The oscilloscope used, should be calibrated every 6 months or every 500 operating hours. This frequency of calibration will assure sweep frequency measurements within $\pm 3$ percent and voltage calibration accuracies of $\pm 3$ percent on the Tektronix types 531,535 , or 561 A and $\pm_{1}$ percent on the Tektronix type 435 oscilloscope.

The multimeter should also be calibrated every 6 months to assure accuracies within $\pm_{3}$ percent of full scale DC voltages and currents, $\pm 3$ percent of exact resistance measurement readings.

The oscilloscope probes are to be calibrated each time they are used with the Voltage Calibrator on the front of the oscilloscope.

TABLE 6-1. FIELD MAINTENANCE RECOMMENDED TEST EQUIPMENT AND TOOLS

```
Oscilloscope Tektronix Type 453; includes two foot 10x probes (2254-091)
High Voltage Probe, RCA, WG-297 and Resistor WG-211A
Multimeter or VOM, RCA, WV-38A (2428-042)
Extraction Tool, AMP, B810992-1
Nut driver - 1/4 inch
Nut driver - 3/16 inch
Screw driver - 6 inches
Needle nose pliers
Water pump pliers - 3 inches (Channel Locks)
Open end wrench - 5/16 inch
Open end wrench - 5/32 inch
Long tweezer - 6 inches
Feeler gauge set - .008, .013, .020, . 025
```

TABLE 6-2. MAINTENANCE CENTER RECOMMENDED TEST EQUIPMENT AND TOOLS

| EQU IPMENT/TOOL | MODEL |
| :---: | :---: |
| Oscilloscope <br> Scope Cart <br> Test Probes (2) <br> High Voltage Probe <br> Multimeter or VOM <br> Extraction Tool <br> Nut driver - $1 / 4$ inch <br> Nut driver - 3/16 inch <br> Screw driver - 6 inches <br> Needle nose pliers <br> Water pump pliers - 3 inches (Channel Locks) <br> Open end wrench - 5/16 inch <br> Open end wrench - 5/32 inch <br> Long tweezer - 6 inches <br> Feeler gauge set - . 008, .013, .020, . 025 | Tektronix Type 453 <br> Atlantis Model A <br> Tektronix Type P6006, <br> PT\#010-0160-00, BNC connector <br> RCA, WG-297 and Resistor WG-211A <br> RCA, WV-38A <br> AMP, B 810992-1 |

## APPENDIX A

## ILLUSTRATED PARTS BREAKDOWN

## ILLUSTRATIONS

1. $70 / 752$ Video Data Terminal ..... Aii
2. Control Panel Assembly ..... A2
2 A. Control Panel Chassis ..... A4
2 B. Keyboard Assy ..... A6
2 C. Clutch and Filter Shaft Assy; Anti-Backlash Spring ..... A8
2D. Slide and Keeper Assy ..... A8A
2 E. Key Lever and Key Interposer Assy ..... A8B
2 F. Bail Rod Assy ..... A8F
2 G. Latch Interposers and Link Assy ..... A8I
2 H. Storage Bar and Microswitch Assy ..... A8J
2 I. Key Lever Hardware and Leaf Switches ..... A8L
2 J. Selector Compensator Interlock ..... A80
2 K. Shift Mechanism ..... A8P
2 L. Space Bar Assy ..... A8S
2 M. Keycaps (Buttons) for Standard Keyboard ..... A8T
3. 70/752 Video Data Terminal Data Set Cable Assembly ..... A9
4. 70/752 Video Data Terminal Viewer Assembly ..... A10
5. Input/Output No. 1 Logic Module Assembly ..... A22
6. Input/Output No. 2 Logic Module Assembly ..... A24
7. Register Logic Module Assembly ..... A26
8. Mark Logic Module Assembly ..... A28
9. Timing Logic Module Assembly ..... A30
10. Oscillator and Printer Terminator Module Assembly ..... A32
11. Selection Amplifier Module Assembly ..... A34
12. Deflection Amplifier Module Assembly ..... A40
13. Monoscope Assembly ..... A46
14. Monoscope Pre Amplifier Assembly ..... A48
15. Tickler Driver Module Assembly ..... A50
16. Video Driver Module Assembly ..... A56
17. Low Voltage Power Supply Assembly ..... A60
18. Low Voltage Power Supply Regulator Assembly ..... A68
19. Dynamic Focus Module Assembly ..... A74
20. Keyboard Filter Module Assembly ..... A76
21. Station Selection Module Assembly ..... A78
22. Mark Format Module Assembly ..... A80
23. Printer Adapter Module Assembly ..... A82
24. Keyboard Extension Cable Assembly SF 5713 ..... A85
25. RCA High Voltage Power Supply, A13 ..... A86
26. A1 Module Assy., High Voltage Driver ..... A88
27. A2 Module Assy., -1.8 Kv Regulator ..... A90
28. A3 Module Assy., 12 Kv Reg/Sync Converter ..... A92
29. A4 Module Assy., High Voltage Focus ..... A94

## ILLUSTRATIONS (Contd)

30. A5 Module Assy., Transformer Interface ..... A95
31. A6 Module Assy., Low Voltage Interface ..... A96
32. A7 Module Assy., High Voltage Multiplier ..... A97
TABLE
33. Interposing Coding ..... A8E


Figure 1. 70/752 Video Dafa Terminal



Figure 2. Control Panel Assy



Figure 2A. Control Panel Chassis



P405


Figure 2B. Keyboard Assembly



Figure 2C. Clutch and Filter Shaft Assy; Anti-Backlash Spring

| $\begin{gathered} \text { FIG. \& } \\ \text { INDEX } \\ \text { NUMBER } \end{gathered}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $2 C-$ -1 -2 -3 -4 -5 -6 -7 -8 -9 -10 -11 -12 -13 | CLUTCH AND FILTER SHAFT ASSY; ANTI-B/ACKLASH SPRING <br> - . . CLUTCH AND FILTER SHAFT ASSY <br> - SHAFT, FILTER <br> - STOP (ANTI-BACKLASH CAM) <br> . SCREW, SET NO. 4 (.112) $-40 \times .09$ LG <br> - CLUTCH AND GEAR ASSY <br> - . INPUT HUB ASSY (GEAR) <br> - SCREW, THD FORMING ( $2-56 \times .38 \mathrm{LG})$ (ERL 30) <br> - SPRING, ANTI-BACKLASH (ERL 30) <br> - SPACER BLOCK, SPRING (ERL 30) <br> - BEARING ASSY, RIGHT <br> - SPACER, FILTER SHAFT <br> - WASHER, SPRING <br> - BEARING ASSY, LEFT | $\begin{aligned} & 2149839-501 \\ & 2144109-2 \\ & 2144167-1 \\ & 886254-2 \\ & 2188016-501 \\ & 2188016-502 \\ & 2187254-602 \\ & 2166966-1 \\ & 2166967-1 \\ & 2187566-1 \\ & 2144110-1 \\ & 2187565-4 \\ & 2187566-2 \end{aligned}$ | $\begin{aligned} & 303501 \\ & 301178 \\ & 310022 \\ & 310023 \\ & 308487 \\ & 310765 \\ & 303483 \\ & 303484 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 4 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 2 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |



Figure 2D. Slide and Keeper Assy

| $\begin{array}{\|c\|} \text { FIG. \& } \\ \text { INDEX } \\ \text { NUMBER } \end{array}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | Qty. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{r} 2 D- \\ -1 \\ -2 \\ -3 \\ -4 \\ -5 \\ -6 \\ -6 \\ -7 \\ -8 \\ -9 \\ -10 \\ -11 \\ -12 \\ -12 \\ -13 \\ -14 \end{array}$ | SLIDE AND KEEPER ASSY <br> - . . BRACKET, KEEPER <br> - . . SCREW, BRACKET <br> . . . SPRING, RESTORING <br> . . . SCREW, KEEPER MTG <br> - . KEEPER ASSY <br> . . . Slide assy, Clutch release <br> - . . SPRING, PAWL LINK <br> - . Shaft, CYCLE LATCH <br> . . . RETAINER <br> . . . ARM ASSY <br> - . . LATCH ASSY <br> . . . . ARM, Clutch <br> . . . RING, RETAINING <br> . . . SCREW, SHOULDER | $\begin{aligned} & \text { IBM1134976 } \\ & \text { IBM1164579 } \\ & 2.187321-15 \\ & \text { IBM341216 } \\ & \text { IBM1134887 } \\ & 2144112-501 \\ & 2187321-14 \\ & \text { IBM1123688 } \\ & 93605-103 \\ & 2134596-501 \\ & 2187321-13 \\ & 2144535-1 \\ & 93605-102 \\ & 2144538-1 \end{aligned}$ | $\begin{aligned} & 301926 \\ & 311924 \\ & 301927 \\ & 78651 \\ & 303478 \\ & 301929 \\ & 303478 \\ & 251736 \\ & 301907 \end{aligned}$ | $\begin{aligned} & 1 \\ & 2 \\ & 1 \\ & 4 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |



\begin{tabular}{|c|c|c|c|c|c|}
\hline FIG. \& INDEX NUMBER \& DESCRIPTION \& DRAWING OR PART NUMBER \& RCA STOCK NUMBER \& QTY. \& NOTES \\
\hline \begin{tabular}{c}
\(2 \mathrm{E}-\) \\
-1 \\
-2 \\
-3 \\
-4 \\
-5 \\
-6 \\
-7 \\
-8 \\
-9 \\
-10 \\
-11 \\
\hline
\end{tabular} \& \begin{tabular}{l}
KEY LEVER AND KEY INTERPOSER ASSY \\
. . . SUPPORT, FULCRUM \\
- . . ROD, KEY lever fulcrum \\
. . . SPRING, LatCH INTERPOSER \\
. . . PLATE, INTERPOSER SPRING \\
- . . SCREW, LATCH SPRING \\
- . . WASHER, FLAT \\
. . . WASHER, LOCK \\
- . . RETAINER, FULCRUM (KEY LEVER) \\
- . . SPRING, PAWL KEY LEVER* \\
- . . Spring, 1 AND 2 ROW INTERPOSER RETAINING \\
-. . SpRING, 3 AND 4 ROW INTERPOSER RETAINING \\
. . . INTERPOSER, SELECT (INTERLACE) STOCK (UNCODED) INTERPOSER SHOWN IN ILLUSTRATION) \\
NOTE: REFER TO TABLE 1 FOR CODING OF EACH INTERPOSER. \\
- . . plate assy \\
- . . KEY lever, backspace \\
. . . KEY LEVER, CARRIAGE RETURN \\
- . . ROD, FULCRUM (INTERPOSER) \\
. . . RETAINER, FULCRUM (INTERPOSER) \\
. . . GUIDE, INTERPOSER \\
- . . KEY LEVER, SHORT PAWL (ROW 4) \\
. . . KEY LEVER, SHORT PAWL (ROW 3) \\
- . . KEY LEVER, SHORT PAWL (ROW 2) \\
. . . KEY LEVER, SHORT PAWL (ROW 1) \\
. . . SPRING, KEY LEVER \\
- . . KEY LEVER, MASTER ERASE \\
. . . KEy lever, space bar (SEe fig 2L) \\
*On later models of the Keyboard Assembly, these were replaced with Spring, Key levers. (Figure 2B, Index No. 32 and 33)
\end{tabular} \& \begin{tabular}{l}
IBM1134988 \\
IBM1132166 \\
IBM1124430 \\
IBM1124433 \\
2187254-2 \\
82278-103 \\
93620-105 \\
IBM264641 \\
2187321-20 \\
IBM1141266 \\
2187321-17 \\
2144139-1 \\
IBM1134987 \\
IBM1123963 \\
IBM1092125 \\
IBM1141381 \\
IBM1123950 \\
IBM1123940 \\
IBM1123948 \\
IBM1123947 \\
IBM150735 \\
2144140-1
\end{tabular} \& \[
\begin{aligned}
\& 302616 \\
\& 308487 \\
\& 302656 \\
\& 301924 \\
\& 301925 \\
\& 301180 \\
\& \\
\& \hline 302655 \\
\& 301181 \\
\& \\
\& 308698 \\
\& 308328 \\
\& 301789 \\
\& 301181
\end{aligned}
\] \& 1
1
1
2
1
6

1
45
26
20
45

1
1
1
1
1
2
1
10
10
11
12
5
1 \& <br>
\hline
\end{tabular}



70/752.0413

Table 1. Interposer Coding
NOTE: Code replacement interposer by removing required lugs. Lugs removed, coded as $Z E R O S=$ no bail bar movement. Lugs left on, coded as ONES = bail bar movement. When the SHIFT key is pressed, bail 5 moves, but the output of microswitch 5 is ZERO due to the activation of the SHIFT switch AlS8.

| BAIL BAR AND LUGNUMBERS |  |  |  |  |  |  |  |  | BAIL BAR AND LUG NUMBERS |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL | 7 | 6 | 5 | 4 | 3 | 2 | 1 |  | SYMBOL | 7 | 6 | 5 | 4 | 3 | 2 | 1 |  |
| (SPACE) | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  | A | 1 | 0 | 0 | 0 | 0 | 0 | 1 |  |
| $\div$ | 0 | 1 | 1 | 0 | 0 | 0 | 1 |  | B | 1 | 0 | 0 | 0 | 0 | 1 | 0 |  |
| " | 0 | 1 | 1 | 0 | 0 |  | 0 |  | C | 1 | 0 | 0 | 0 | 0 | 1 | 1 |  |
| \# | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  | D | 1 | 0 | 0 | 0 | 1 | 0 | 0 |  |
| \$ | 0 | 1 | 1 | 0 | 1 | 0 | 0 |  | E | 1 | 0 | 0 | 0 | 1 | 0 | 1 |  |
| \% | 0 | 1 | 1 | 0 | 1 | 0 | 1 | SHIFT | F | 1 | 0 | 0 | 0 | 1 | 1 | 0 |  |
| \& | 0 | 1 | 1 | 0 | 1 | 1 | 0 | KEY | G | 1 | 0 | 0 | 0 | 1 | 1 | 1 |  |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | PRESSED | H | 1 | 0 | 0 | 1 | 0 | 0 | 0 |  |
| $($ | 0 | 1 | 1 | 1 | 0 | 0 | 0 |  | I | 1 | 0 | 0 | 1 | 0 | 0 | 1 |  |
| ) | 0 | 1 | 1 | 1 | 0 | 0 | 1 |  | J | 1 | 0 | 0 | 1 | 0 | 1 | 0 |  |
| * | 0 | 1 | 1 | 1 | 0 |  | 0 |  | K | 1 | 0 | 0 | 1 | 0 | 1 | 1 |  |
| + | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  | L | 1 | 0 | 0 | 1 | 1 | 0 | 0 |  |
| , | 0 | 1 | 0 | 1 | 1 | 0 | 0 |  | M | 1 | 0 | 0 | 1 | 1 | 0 | 1 |  |
| - | 0 | 1 | 0 | 1 | 1 | 0 | 1 |  | N | 1 | 0 | 0 | 1 | 1 | 1 | 0 |  |
| - | 0 | 1 | 0 | 1 | 1 | 1 | 0 |  | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |  |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  | P | 1 | 0 | 1 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  | $Q$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |  | R | 1 | 0 | 1 | 0 | 0 | 1 | 0 |  |
| 2 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |  | S | 1 | 0 | 1 | 0 | 0 | 1 | 1 |  |
| 3 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  | T | 1 | 0 | 1 | 0 | 1 | 0 | 0 |  |
| 4 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |  | U | 1 | 0 | 1 | 0 | 1 | 0 | 1 |  |
| 5 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  | V | 1 | 0 | 1 | 0 | 1 | 1 | 0 |  |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |  | W | 1 | 0 | 1 | 0 | 1 | 1 | 1 |  |
| 7 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |  | X | 1 | 0 | 1 | 1 | 0 | 0 | 0 |  |
| 8 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |  | Y | 1 | 0 | 1 | 1 | 0 | 0 | 1 |  |
| 9 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |  | Z | 1 | 0 | 1 | 1 | 0 | 1 | 0 |  |
| : | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  | [ | 1 | 0 | 0 | 1 | 0 |  | 17 | SHIFT |
| ; | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  | ] | 1 | 0 | 0 | 1 | 1 | 0 | 1 | KEY |
| $<$ | 0 | 1 | 0 | 1 | 1 | 0 | 0 |  | X | 1 | 0 | 1 | 1 | 0 | 0 | 0 | PRESSED |
| $=$ | 0 | 1 | 0 | 1 | 1 | 0 | 1 | SHIFT | 」 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |  |
| $>$ | 0 | 1 | 0 | 1 | 1 |  | 0 | KEY | $\ll$ | 0 | 0 | 0 | 1 | 1 | 0 | 1 |  |
| ? | 0 | 1 | 0 | 1 | 1 | 1 |  | PRESSED |  |  |  |  |  |  |  |  |  |
| @ | 1 | 0 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |



Figure 2F. Bail Rod Assy



Figure 2G. Latch Interposers and Link Assy

| $\begin{array}{\|l\|} \text { FIG. \& } \\ \text { INDEX } \\ \text { NUMBER } \end{array}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $2 G-$ -1 -2 -3 -4 -5 -6 -7 -8 -9 -10 -11 -12 -13 -14 | LATCH INTERPOSERS AND LINK ASSY <br> . . . BRACKET, INTERPOSER MTG (GUIDE COMB) <br> - . . SPRING, LATCH <br> - . . INTERPOSER, LATCH (NO. 7) <br> . . . CLEVIS, PIN <br> . . . . BUSHING, CLEVIS (NYLON) <br> . . . NUT, HEX (NO. 2-64) <br> . . . LINK, LATCH (CLEVIS ROD) <br> - . . INTERPOSER, LATCH (NO. 6) <br> - . INTERPOSER, LATCH (NO. 5) <br> . . . INTERPOSER, LATCH (NO. 4) <br> - . . INTERPOSER, LATCH (NO. 3) <br> - . INTERPOSER, LATCH (NO. 2) <br> -. . INTERPOSER. LATCH (NO. 1) <br> . . . SCREW | $\begin{aligned} & \text { IBM1141382 } \\ & 2187393-1 \\ & 2187321-5 \\ & 2187321-8 \\ & 2173676-1 \\ & 2187574-1 \\ & 2144116-1 \\ & 1141379(\text { IBM \#1) } \\ & 1141378(\text { IBM \#3) } \\ & 1141377(\text { IBM \#7) } \\ & 1141376(\text { IBM \#4) } \\ & 1141375(\text { IBM \#6) } \\ & 1141374(\text { IBM \#5) } \\ & \text { IBM1164576 } \end{aligned}$ | $\begin{aligned} & 301916 \\ & 305643 \\ & 301930 \\ & 301908 \\ & 301920 \\ & 305847 \\ & 305846 \\ & 305845 \\ & 305844 \\ & 305843 \\ & 305842 \end{aligned}$ | $\begin{aligned} & 1 \\ & 7 \\ & 1 \\ & 7 \\ & 7 \\ & 7 \\ & 7 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |



Figure 2H. Storage Bar and Microswitch Assy

R5

| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 2H- <br> - 1 <br> - 2 <br> - 3 <br> - 4 <br> - 5 <br> - 6 <br> - 7 <br> - 8 <br> - 9 <br> -10 <br> -11 <br> $-12$ <br> -13 <br> -14 <br> -15 <br> -16 <br> -17 <br> -18 <br> $-19$ | ```STORAGE BAR AND MICROSWITCH ASSY . . . SHAFT, SPACER (11.29 LG) . . . GUIDE, RETURN DELAY (RH) . . . SPRING, TORSION (RH) . . . RING, RETAINING . . . ARM, RETURN DELAY NOTE: WHEN EITHER THE PLATE ASSEMBLY (STORAGE BAR), ITEM 6 OR THE GUIDE (STORAGE BLOCK), ITEM }7\mathrm{ SHOW SUFFICIENT WEAR TO WARRANT REPLACEMENT, BOTH PARTS SHOULD BE REPLACED AT THE SAME TIME TO ENSURE PROPER OPERATION. . . . PLATE ASSY (STORAGE BAR) . . GUIDE (STORAGE BLOCK) . . NUT, PLATE . . SWITCH ASSY, MICRO (STORAGE) S1 THRU S7 . . SCREW, MTG (6-32 x 0.5 LG) . . . BRACKET, SWITCH ASSY MTG (KEYBOARD SN 1001-2000) - BRACKET, SWITCH ASSY MTG (KEYBOARD SN 2001 AND UP) . SCREW, THD FORMING (2-56 x 0.25 LG) . NUT, HEX (NO. 6-32) . SCREW, ADJ (NO. 6-32 x 1.0 LG) - SCREW, PLATE MTG - SPRING, TORSION (LH) - GUIDE, RETURN DELAY (LH) . SCREW (NO. 2-56 x 0.25 LG) . SCREW, PAN HD (NO. 6-32 x 0.50 LG)``` | $\begin{aligned} & 2144539-1 \\ & 2173685-2 \\ & 2144168-1 \\ & 93605-106 \\ & 2173684-1 \end{aligned}$ $\begin{aligned} & 2173686-501 \\ & 2144542-1 \\ & 2173687-1 \\ & 2144111-501 \\ & 990386-113 \\ & \\ & 2144541-1 \\ & 2144541-2 \\ & 2187254-601 \\ & 57435-104 \\ & 990386-121 \\ & 2187254-2 \\ & 2144168-2 \\ & 2173685-1 \\ & 2187254-601 \\ & 990386-113 \end{aligned}$ | 301182 <br> 301910 <br> 252983 <br> 304893 <br> 307620 <br> 308187 <br> 307546 <br> 308487 <br> 103891 <br> 301911 <br> 308487 | $\begin{array}{r} 1 \\ 1 \\ 1 \\ 1 \\ 4 \\ 2 \\ \\ \\ \\ \\ \\ \\ \\ \\ 1 \\ 1 \\ 1 \\ 1 \\ 7 \\ 2 \\ \hline 1 \\ 1 \\ 1 \\ 1 \end{array}$ |  |



Figure 21. Key Lever Hardware and Leaf Switches


Figure 2J. Selector Compensator Interlock

| $\begin{aligned} & \text { FIG. \& } \\ & \text { INDEX } \\ & \text { NUMBER } \end{aligned}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{r} 2 \mathrm{~J}- \\ -1 \\ -2 \\ -3 \\ -4 \\ -5 \\ -6 \\ -7 \\ -8 \\ -9 \\ -10 \end{array}$ | SELECTOR COMPENSATOR INTERLOCK <br> . . . PLUNGER <br> . . . BALL, COMPENSATOR <br> - . . SCREW, SET <br> . . . TUBE, COMPENSATOR <br> - . . SCREW, FLAT HD <br> . . . SUPPORT, FULCRUM <br> - . . SPACER, COMPENSATOR <br> - . . Plate assy <br> . . . NUT <br> . . . SCREW | IBM1124682 <br> IBM1141860 <br> IBM1134988 <br> IBM1134987 <br> IBM38214 <br> IBM1164583 | $\begin{aligned} & 307950 \\ & 302642 \end{aligned}$ | $\begin{array}{r} 2 \\ 48 \\ 2 \\ 1 \\ 4 \\ 1 \\ 4 \\ 1 \\ 4 \\ 4 \end{array}$ |  |



Figure 2K. Shift Mechanism



Figure 2L. Space Bar Assy

| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 2L- $\begin{aligned} & -1 \\ & -\quad 2 \\ & -3 \\ & -4 \\ & -5 \\ & -6 \\ & -7 \\ & -8 \\ & -9 \\ & -10 \\ & -11 \\ & -11 \\ & -12 \\ & -13 \end{aligned}$ |  | I BM1 269422 <br> 2144539-1 <br> 2144140-1 <br> 2187798-1 <br> IBM38051 <br> IBM11 23987 <br> IBM150735 <br> IBM1164467 <br> IBM1164366 <br> IBM1164579 <br> IBM1164425 <br> IBM1164427 <br> IBM1134899 | $\begin{aligned} & 301182 \\ & 301181 \\ & 301789 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 2 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 2 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |  |



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Figure 2M. Keycaps (Buttons) for Standard Keyboard

| $\begin{aligned} & \text { FIG. \& } \\ & \text { INDEX } \\ & \text { NUMBER } \end{aligned}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 2M- | KEYCAPS (BUTTONS) FOR STANDARD KEYBOARD |  |  |  |  |
| - 1 | $\mathbb{\square}$ (CAP, KEY MASTER ERASE) | 2144151-1 |  | 1 |  |
| - 2 | $\div / 1$ | IBM1197152 |  | 1 |  |
| - 3 | "/2 |  |  | 1 |  |
| - 4 | \#/3 | IBM1124898 |  | 1 |  |
| - 5 | \$/4 | IBM1 124899 |  | 1 |  |
| - 6 | \%/5 | IBM1124900 |  | 1 |  |
| - 7 | \&/6 | IBM1133318 |  | 1 |  |
| - 8 | 1/7 | IBM1133909 |  | 1 |  |
| - 9 | (/8 | I BM1 133071 |  | 1 |  |
| -10 | )/9 |  |  | 1 |  |
| -11 | 0 |  |  | 1 |  |
| -12 | */: | IBM1179891 |  | 1 |  |
| -13 | = $/-$ | IBM1197153 |  | 1 |  |
| -14 | BACK SPACE | IBM1124450 |  | 1 |  |
| -15 | $Q$ | IBM1133274 |  | 1 |  |
| -16 | W | I BM1 124957 |  | 1 |  |
| -17 | E | IBM1133329 |  | 1 |  |
| -18 | R | IBM1124959 |  | 1 |  |
| -19 | T | IBM1133278 |  | 1 |  |
| -20 | Y | I BM1 124961 |  | 1 |  |
| -21 | U | IBM1124962 |  | 1 |  |
| -22 | I | IBM1124963 |  | 1 |  |
| -23 | 0 | İBM1 158126 |  | 1 |  |
| -24 | @/P | IBM1179893 |  | 1 |  |
| -25 | - | IBM1197154 |  | 1 |  |
| -26 | LOCK | IBM1132266 |  | 1 |  |
| -27 | A | IBM1133285 |  | 1 |  |
| -28 | S | IBM1127612 |  | 1 |  |
| -29 | D | IBM1127613 |  | 1 |  |
| -30 | F | IBM1127614 |  | 1 |  |
| -31 | G | IBM1133337 |  | 1 |  |
| -32 | H | IBM1127616 |  | 1 |  |
| -33 | J | IBM1133291 |  | 1 |  |
| -34 | [/K | IBM1179895 |  | 1 |  |
| -35 | L | IBM1133293 |  | 1 |  |
| -36 | +/; |  |  | 1 |  |
| -37 | $\ll$ (CAP, KEY CONTROL) | 2144131-2 |  | 1 |  |
| -38 | SHIFT (CAP, KEY SHIFT, LH) | IBM1132259 |  | 1 |  |
| -39 | Z | IBM1133296 |  | 1 |  |
| -40 | X | IBM1133342 |  | 1 |  |
| -41 | c | IBM1133298 |  | 1 |  |
| -42 | V | IBM1133343 |  | 1 |  |
| -43 | B | IBM1127665 |  | 1 |  |
| -44 | $\mathrm{X} / \mathrm{N}$ | IBM1197573 |  | 1 |  |
| -45 | ]/M | IBM1133841 |  | 1 |  |
| -46 | <1, | IBM1179899 |  | 1 |  |
| -47 | $\geqslant 1$ | IBM1179900 |  | 1 |  |
| -48 | ?// | IBM1127670 |  | 1 |  |
| -49 | SHIFT (CAP, KEY SHIFT, RH) | IBM1132252 |  | 1 |  |
| -50 | KEYCAP (BUTTON), SPACE BAR (GRAY) BLANK KEYCAPS (BUTTONS) | IBM1 269422 |  | 1 |  |
|  | ROW 1 | IBM1133801 |  | 1 |  |
|  | ROW 2 | IBM1133802 |  | 1 |  |
|  | ROW 3 | IBM1133803 |  | 1 |  |
|  | ROW 4 | IBM1133804 |  | 1 |  |
|  | BACK SPACE | I BM1133811 |  | 1 |  |
|  | LOCK | IBM1133810 |  | 1 |  |
|  | SHIFT (RH) | IBM1127930 |  | 1 |  |
|  | SHIFT (LH) | IBM1127936 |  | 1 |  |
|  | SPECIAL KEYCAPS (BUTTONS) FOR EXPORT UNITS $£ / 1$ (BRITISH POUND) | 2187321-21 |  | 1 |  |
|  | - \% K | 2187321-22 |  | 1 |  |
|  | 1/M | 2187321-23 |  | 1 |  |
|  | -/N | 2187321-24 |  | 1 |  |
|  |  | $\begin{array}{r} 2187321-26 \\ 2187321-27 \\ \hline \end{array}$ |  | 1 |  |


| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 3- <br> - 1 <br> - 2 <br> - $\begin{array}{r} -3 \\ -\quad 4 \end{array}$ | CABLE ASSY, DATA SET FOR NHA <br> - CONNECTOR, ELECT PLUG <br> - SHELL, ELECT CONNECTOR <br> ATTACHING PARTS <br> - LOCK ASSY, MALE $\qquad$ <br> - SHELL, ELECT CONNECTOR <br> - CABLE, 50 FEET | $\begin{aligned} & 2112702-502 \\ & 2187568-1 \\ & 2187568-3 \\ & 2187568-5 \\ & \\ & 2187568-7 \\ & 2187678-1 \end{aligned}$ | 253001 | $\begin{gathered} \text { REF } \\ 2 \\ 1 \\ 1 \\ 1 \\ 1 \\ \text { AR } \end{gathered}$ |  |



Figure 3. 70/752 Video Data Terminal Data Set Cable Assembly


Figure 4. 70/752 Video Dafa Terminal Viewer Assembly (Sheet 1 of 7)



Figure 4. 70/752 Video Dafa Terminal Viewer Assembly (Sheet 2 of 7)


Figure 4. 70/752 Video Data Terminal Viewer Assembly (Sheet 3 of 7)


Figure 4. 70/752 Video Dafa Terminal Viewer Assembly (Sheef 4 of 7 )

R5

| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-22 | - CONNECTOR, ELECT RECEPTACLE (DATA SUB SET) ATTACHING PARTS <br> - SCREW, FEMALE LOCK | $2187568-2$ $2187568-6$ |  | 1 2 |  |
| -23 | - JACK, TEST POINT (BLUE) | 746282-7 |  | 1 |  |
| -24 | - JACK, TEST POINT (RED) | 746282-1 |  | 1 |  |
| -25 | - BRACKET, CONNECTOR MTG ATTACHING PARTS | 2144510-501 |  | 1 |  |
|  | . SCREW, THREAD FORMING (NO. 8-32 x 0.25 LG ) | 2187254-202 |  | 5 |  |
| -26 | - MODULE ASSY, SELECTION AMPLIFIER (SEE FIGURE 11) | 2110687-501 | 266992 | 1 |  |
| -27 | - MODULE ASSY, DEFLECTION AMPLIFIER (SEE FIGURE 12) <br> ATTACHING PARTS | 2110686-501 |  | 1 |  |
|  | - SCREW, THREAD FORMING (NO. 6-32 x 0.25 LG) | 2187254-101 |  | 2 |  |
| -28 | - CONNECTOR, ELECT RECEPTACLE ATTACHING PARTS | 2187548-1 | 267691 | 10 |  |
|  | . SCREW, THREAD FORMING (NO. 6-32 $\times 0.25 \mathrm{LG}$ ) | 2187254-101 |  | 18 |  |
|  | . SCREW, FLAT HD (NO. $4-40 \times 0.31 \mathrm{LG}$ ) (USED WITH J2O) | 990064-107 |  | 2 |  |
|  | . WASHER, FLAT (NO. 4) | 82278-103 |  | 2 |  |
|  | - WASHER, LOCK (NO. 4) | 93618-105 |  | 2 |  |
|  | . NUT, HEX (NO. 4-40) | 57435-103 |  | 2 |  |
| -29 | - MODULE ASSY, TICKLER DRIVER (SEE FIGURE 15) ATTACHING PARTS | 2110689-501 | 301963 | 1 |  |
|  | - SCREW, THREAD FORMING (NO. 4-40 $\times 0.75$ LG) | 2187254-5 |  | 1 |  |
|  | . SCREW, PAN HD (NO. 6-32 x 0.31 LG ) | 990106-107 |  | 1 |  |
|  | - WASHER, LOCK (NO. 6) | 93618-107 |  | 1 |  |
|  | - WASHER, FLAT (NO. 6) | 82273-104 |  | 1 |  |
| -30 | - MODULE ASSY, VIDEO DRIVER (SEE FIGURE 16) ATTACHING PARTS | 2110688-501 | 266989 | 1 |  |
|  | . SCREW, THREAD FORMING (NO. 4-40 x 0.75 LG) | 2187254-5 |  | 4 |  |
|  | . SCREW, PAN HD (NO. 6-32 x 0.31 LG ) | 990106-107 |  | 3 |  |
|  | - WASHER, LOCK (NO. 6) | 93618-107 |  | 3 |  |
|  | - WASHER, FLAT (NO. 6) | 82273-104 |  | 3 |  |
| -31 | - POWER SUPPLY, HIGH VOLTAGE (SEE APPENDIX B FOR VENDOR PARTS BREAKDOWN) ATTACHING PARTS | 2187577-1 |  | 1 |  |
| -32 | - SCREW, THREAD FORMING (NO. $8-32 \times 0.25$ LG) | $2187254-201$ |  | $2$ |  |
|  | - WASHER, EXT TOOTH LOCK (NO. 8) | $93610-109$ |  | $2$ |  |
| -33 | - POWER SUPPLY ASSY, LOW VOLTAGE, 60 Hz (SEE FIGURE 17) | 2110683-501 | 266999 | 1 | A, E |
|  | . POWER SUPPLY ASSY, LOW VOLTAGE, 50 Hz (SEE FIGURE 17) | 2110683-502 |  | 1 | B-D |
|  | - SCREW, THREAD FORMING (NO. 6-32 x 0.25 LG ) | 2187254-101 |  | 1 |  |
|  | . SCREW, THREAD FORMING (NO. 6-32 x 0.75 LG) | 2187254-105 |  | 1 |  |
|  | - STRAP, WIRE RETAINING | 2183004-41 |  | $1$ |  |
|  | - WASHER, EXT TOOTH LOCK (NO. 6) | 93610-107 |  | $2$ |  |
| -34 | - MODULE ASSY, DYNAMIC FOCUS (SEE FIGURE 19) | 2144178-501 | 267826 | 1 |  |
|  | - POWER SUPPLY, HIGH VOLTAGE | 2166024-503 | 306493 | 1 |  |


$131 / 52 \cdot 9102$

Figure 4. 70/752 Video Dafa Terminal Viewer Assembly (Sheet 5 of 7)


Figure 4. 70/752 Video Dafa Terminal Viewer Assembly (Sheet 6 of 7)


4305-104-7

Figure 4. Video Data Terminal Viewer Assembly (Sheet 7 of 7 )

| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QtY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $4-$ | ATTACHING PARTS <br> . SCREW, PAN HD (NO. 6-32 x 0.31 LG ) <br> - WASHER, LOCK (NO. 6) <br> - WASHER, FLAT (NO. 6) | $\begin{aligned} & 990106-107 \\ & 93618-107 \\ & 82278-104 \end{aligned}$ | 211587 | 2 2 2 |  |
| -35 | . MODULE ASSY., KEYBOARD FILTER (SEE FIGURE 20) ATTACHING PARTS <br> - SCREW, PAN HD (NO. 6-32 x 0.31 LG$)$ <br> . WASHER, LOCK (NO. 6) <br> - WASHER, FLAT (NO. 6) | $\begin{aligned} & 2165856-501 \\ & \\ & 990106-107 \\ & 93618-107 \\ & 82278-104 \end{aligned}$ | 301053 | 1 4 4 4 |  |
| -36 | . SCREW, THREAD FORMING (NO. 10-32 x 0.37 LG) <br> - WASHER, EXT TOOTH LOCK (NO. 10) | $\begin{aligned} & 2187254-302 \\ & 93610-112 \end{aligned}$ |  | 2 |  |
| -37 | . WASHER, EXT TOOTH LOCK (NO. 10) <br> - COVER, DUST | $\begin{aligned} & 93618-112 \\ & 2144500-2 \end{aligned}$ | 97178 | 2 1 |  |
|  | . SCREW, THREAD FORMING (NO. 4-40 x 0.25 LG) | 2187254-1 | 308486 | 10 |  |
| -38 | - REtainer, CABLE | 2144195-1 |  | 1 |  |
| -39 | - CLAMP, LOOP <br> ATTACHING PARTS <br> . SCREW, THREAD FORMING (NO. 6-32 x 0.25 LG ) $\qquad$ | $8811154-6$ $2187254-101$ |  | 1 |  |
| -40 | - CABLE ASSY., KEYBOARD | 2144194-501 | 308484 | 1 |  |
| -41 | - MONOSCOPE ASSY. (SEE FIGURE 13) ATTACHING PARTS | 2110691-501 |  | 1 |  |
|  | . SCREW, PAN HD (NO. 6-32 x 0.31 LG ) | 990106-107 |  | 3 |  |
|  | . WASHER, EXT TOOTH LOCK (NO. 6) <br> SCREW, FLAT HD (NO $6-32 \times 0.37 \mathrm{LG})$ | 93610-107 8924639-109 |  | 3 1 |  |
|  | . SCREW, FLAT HD (NO. 6-32 x 0.37 LG) ---*_-- | 8924639-109 |  | $1$ |  |
| -42 -43 | - COVER, SHIELD REAR - COVER, SHIELD FRONT | $\begin{aligned} & 2144552-501 \\ & 2144551-501 \end{aligned}$ |  | 1 |  |
| -43 | - COVER, SHIELD FRONT <br> ATTACHING PARTS <br> - SCREW, THREAD FORMING (NO. 4-40 x 0.25 LG ) $\qquad$ | $2144551-501$ $2187254-1$ | 308486 | 1 4 |  |
| -44 | - BRACKET, FRONT | 2144129-1 |  | $1$ |  |
| -45 | - BRACKET, REAR <br> ATTACHING PARTS | $2144130-1$ |  | $1$ |  |
|  | - SCREW, THREAD FORMING (NO. 6-32 x 0.25 LG) SCREW, SHOULDER | $\begin{aligned} & 2187254-101 \\ & 1021856-7 \end{aligned}$ |  | 4 |  |
|  | - WASHER | 2187515-4 |  | 2 |  |
| -46 | - GROMMET | 57421-1 | 73155 | 2 |  |
| -47 | - GROMMET | 57421-30 | 52266 | 1 |  |
| -48 | - YOKE, DEFLECTION | 2187326-1 | 267000 | 1 |  |
|  | CAUTION <br> Before replacing the deflection yoke, check the serial number of the associated deflection amplifier in the VDT. For deflection amplifiers serial numbers 0135 and below, the following resistors must be replaced with the values indicated on Page A43 before the amplifier is used. Replace resistor R8 with IPB Figure 12. Item 27. Replace resistors R5 and R39 with IPB Figure 12, Item 32. |  |  |  |  |
| -49 | - TUBE, CATHODE RAY | 2187325-1 | 266995 | 1 |  |
| -50 | - SOCKET, CATHODE RAY TUBE | 2187562-1 |  | 1 |  |
| -51 | - WIRE, CRT MOUNT | 2144549-1 |  | 1 |  |
| -52 | - CLIP, CRT MOUNT | 2144550-1 |  | 4 |  |
| -53 | - CUSHION, CRT MOUNT | 2144573-1 |  | 4 |  |
| -54 | - SPRING, CRT RETAINING | 2144122-1 | 267673 | 1 |  |
| -55 <br> -56 | - SPRING, GROUND STRAP <br> . STRAP, CRT GROUND | $\begin{aligned} & 2144124-1 \\ & 2144507-501 \\ & \hline \end{aligned}$ |  | 1 |  |




4305-105

Figure 5. Input/Output No. 1 Logic Module Assembly



Figure 6. Input/Output No. 2 Logic Module Assembly



4305-107

Figure 7. Regisfer Logic Module Assembly



Figure 8. Mark Logic Module Assembly

| $\begin{aligned} & \text { FIG. \& } \\ & \text { INDEX } \\ & \text { NUMBER } \end{aligned}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QtY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 8- <br> $-1$ <br> - 2 <br> $-3$ <br> - 4 <br> - 5 <br> - 6 <br> $-7$ <br> - 8 <br> $-9$ <br> $-10$ <br> $-11$ <br> -12 <br> $-13$ <br> $-14$ | MODULE ASSY, MARK LOGIC <br> (SEE FIGURE 4 FOR NHA) <br> - CAPACITOR, FIXED, ELECTROLYTIC, 20 UF, $-10 \%,+150 \%, 6$ VDCW <br> - CAPACITOR, FIXED, CERAMIC DIELECTRIC, 1 UF $+80 \%$, $-20 \%$, 50 VDCW <br> - TRANSISTOR, 2N4074 <br> - PAD, TRANSISTOR MTG <br> - RESISTOR, FIXED FILM, 200 OHMS, $2 \% 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FILM, 4.3K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FILM, 51 OHMS, $2 \%, 1 / 2 W$ <br> - RESISTOR, FIXED FILM, 1.8 K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - INTEGRATED CIRCUIT, LOGIC GATE QUAD TWO <br> - INTEGRATED CIRCUIT, BUFFER <br> - INTEGRATED CIRCUIT, LOGIC GATE DUAL FOUR <br> - INTEGRATED CIRCUIT, LOGIC GATE EXPANDER, DIODE <br> - INTEGRATED CIRCUIT, DUAL FLIP-FLOP <br> - INTEGRATED CIRCUIT, DUAL FLIP-FLOP <br> - PRINTED CIRCUIT BOARD | $\begin{aligned} & 2110697-501 \\ & 2187355-1 \\ & 2187391-2 \\ & 2187335-1 \\ & 2180896-1 \\ & 2187363-32 \\ & 2187363-64 \\ & 2187363-18 \\ & 2187363-55 \\ & 2187270-1 \\ & 2187269-1 \\ & 2187267-1 \\ & 2187272-1 \\ & 2187268-1 \\ & 2187268-2 \\ & 2165471-4 \end{aligned}$ | $\begin{aligned} & 266985 \\ & 266780 \\ & 267728 \\ & \\ & 267789 \\ & 270825 \\ & 261530 \\ & 269518 \\ & 269504 \\ & 269513 \\ & 266776 \\ & 266775 \\ & 266773 \\ & 266778 \\ & 266774 \\ & 302085 \end{aligned}$ | $\begin{array}{r} \text { REF } \\ \\ 1 \\ 3 \\ \\ 2 \\ 2 \\ 2 \\ 7 \\ 2 \\ 2 \\ 2 \\ 14 \\ 1 \\ 17 \\ 2 \\ \\ \hline \end{array}$ |  |



Figure 9. Timing Logic Module Assembly



4305-110

Figure 10. Oscillator and Printer Terminator Module Assembly



Figure 11. Selection Amplifier Module Assembly (Sheet 1 of 3)

| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 11- <br> - 1 <br> - 2 <br> $-3$ <br> - 4 <br> - 5 <br> - 6 <br> $-7$ <br> $-8$ <br> $-9$ <br> $-10$ <br> $-11$ <br> $-12$ <br> -13 <br> -14 <br> -15 <br> -16 <br> $-17$ <br> $-18$ <br> -19 <br> $-20$ <br> -21 <br> -22 <br> -23 <br> -24 <br> - 25 <br> $-26$ | MODULE ASSY, SELECTION AMPLIFIER <br> (SEE FIGURE 4 FOR NHA) <br> - DIODE, 1N914 <br> - DIODE, 1N270 <br> - DIODE, 1N752 <br> - DIODE, 1N937A <br> - CAPACITOR, FIXED, CERAMIC DIELECTRIC, <br> 0.1 UF, $+80 \%$, $-20 \%$, 50 VDCW <br> - CAPACITOR, FIXED, MICA DIELECTRIC, 270 PF, PLUS MINUS 2\%, 500 VDCW <br> CAPACITOR, FIXED MICA DIELECTRIC, 10PF, $2 \%, 500$ VDCW <br> - CAPACITOR, FIXED, MICA DIELECTRIC 5PF, PLUS MINUS $2 \%, 500$ VDCW <br> - CAPACITOR, FIXED, CERAMIC DIELECTRIC, 05 UF $+80 \%$, - 20\%, 200 VDCW <br> . CAPACITOR, FIXED, MICA DIELECTRIC 1.000 PF PLUS MINUS $2 \%, 500$ VDCW <br> CAPACITOR, FIXED ELECTROLYTIC, 20 UF, $-10 \%$, $+150 \%$, 50 VDCW <br> - CAPACITUR, FIXED ELECTROLYTIC, 10 UF $-10 \%$, $+150 \%$, 100 VDCW <br> - TRANSISTOR, 2N708, SILICON HIGH FREQ <br> - TRANSISTOR, 2N2102 <br> - TRANSISTOR, MM3906 <br> - TRANSISTOR, MM3904 <br> - TRANSISTOR, (TYPE 2N2476) <br> - HEAT SINK (USED WITH Q10 AND Q11) <br> - TRANSISTOR, 2 N 3638 <br> - TRANSISTOR, 2N4074 <br> - PAD, TRANSISTOR MTG <br> - RESISTOR, FIXED PRECISION WW, 5OK OHMS, <br> - RESISTOR, FIXED FILM, 3.9 K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FILM, 2.7K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FIIM, 5.6K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FILM, 10 K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED PRECISION WW, 100,07K OHMS, $0.25 \%, 0.125 \mathrm{~W}$ | $2110687-501$ $2187382-1$ $2187383-1$ $2187526-1$ $2187525-1$ $2187391-2$ $2187356-35$ $2187356-5$ $2187356-1$ $2187391-3$ $2187356-496$ $2187355-3$ $2187355-5$ $\cdot$ $2187536-1$ $2187331-1$ $2187343-1$ $2187342-1$ $2187340-1$ $2184113-4$ $2187334-1$ $2187335-1$ $2180896-1$ $2187595-1$ $2187363-63$ $2187363-59$ $2187363-67$ $2187363-73$ $2187595-2$ | 301976 <br> 229936 <br> 224882 <br> 267746 <br> 267728 <br>  <br> 22794 <br> 266781 <br>  <br> 219436 <br>  <br> 267729 <br> 219660 <br>  <br> 266782 <br> 266781 <br> 227000 <br> 230214 <br> 207410 <br> 307409 <br> 267792 <br> 233969 <br> 267789 <br> 270825 <br> 267716 <br> 260610 <br> 269515 <br> 269519 <br> 261462 <br> 267717 | REF 34 2 2 1 20 2 2 2 4 4 6 1 3 3 1 6 12 4 3 3 2 1 1 30 2 6 10 6 3 2 |  |



Figure 11. Selection Amplifier Module Assembly (Sheet 2 of 3)



Figure 11. Selection Amplifier Module Assembly (Sheet 3 of 3)



Figure 12. Deflection Amplifier Module Assembly (Sheet I of 2)



Figure 12. Deflection Amplifier Module Assembly (Sheet 2 of 2)




Figure 13. Monoscope Assembly

| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 13. | MONOSCOPE ASSY (SEE FIG. 4 FOR NHA) | 2110691-501 | REF | REF |  |
| -1 | . KNOB A.SSY | 2144131-501 | 267799 | 2 |  |
| -2 | . cover | 2144532-501 |  | 1 |  |
| -3 | . cover ATTACHING PARTS | 2144532-2 |  | 1 |  |
| -4 | . SCREW, THD FORM ( $4-40 \times 25 \mathrm{LG}$ ) | 2187254-1 |  | 8 |  |
| -5 | . SCREW, PAN HD (NO. 6-32 x 0.38 LG ) | 990106-109 |  | 4 |  |
|  | - Washer, flat (no. 6) | 82278-104 |  | 4 |  |
|  | - WA.sher, LOCK (NO. 6) | 93618-106 |  | 4 |  |
| -6 | . Grommet | 2187570-1 |  | 2 |  |
| -7 | - CAPACITOR, FIXED, CERAMIC FEED-THRU, 1500PF $\pm 20 \% 500$ VDCW | 2187582-1 | 57404 | 2 |  |
|  | . WASHER, EXT TOOTH (NO. 12) | 93611-114 |  | 2 |  |
| -8 | . GROMMET | 2187570-2 |  | 3 |  |
| -9 | . housing | 2165428-501 |  | 1 |  |
| -10 | - deleted |  |  |  |  |
| -11 | - Deleted |  |  |  |  |
| -12 | - TERMINAL bOARD ASSY. PREAMPLIFIER (SEE FIGURE 14) | 2110692-501 | 267824 | 1 |  |
| -13 | - o-Ring | 2187636-1 | 275379 | 1 |  |
| -14 | - O-RING | 2187636-2 | 304921 | 1 |  |
| -15 | - CAPACITOR, FIXED, CERAMIC DIELECTRIC, 1 UF, $+80 \%-20 \%$, 50 VDCW | 2187391-2 | 267728 | 2 |  |
| -16 | - SCREW, PAN HD ( $6-32 \mathrm{X}, 50 \mathrm{LG}$ ) | 990106-113 |  | 1 |  |
|  | . SPA ER | 2187755-1 |  | 1 |  |
|  | - WASGER, Lock (ino. 6) | 93618-107 |  | 1 |  |
|  | - WASher, flat (no. 6) | 82278-104 |  | 1 |  |
|  | . NUT (NO. 6-32) | 57435-104 |  | 1 |  |
| -17 | - CAthode ray tube, monoscope | 2187511-1 | 266997 | 1 |  |
| -18 | . SOCKET, ELECTRON TUBE | 2187559-1 | 9952 | 1 |  |
| -19 | - terminal board assy, voltage divider attaching parts | 2110693-501 | 267825 | 1 |  |
| -20 | - SPACER | 2185307-105 |  | 2 |  |
| -21 | - SCREW, PAN HD ( $4-40 \times 62 \mathrm{LG}$ ) | 990104-115 |  | 2 |  |
| -22 | - SCREW, PAN HD ( $4-40 \times 38 \mathrm{LG}$ ) | 990104-109 |  | 2 |  |
|  | - WASher, flat (no. 4) | 82278-103 |  | 2 |  |
|  | - WASHER, LOCK (NO. 4) | 93618-105 |  | 2 |  |
| -23 | . . CAPACITOR, FIXED, DISC CERAMIC 5,000PF $\pm 20 \% 3,000 \mathrm{VDCW}$ | 2187583-1 | 232716 | 1 |  |
| -24 | . . CAPACITOR, FIXED, CERAMIC DIELECTRIC, . 1 UF, $+80 \%-20 \% 200$ VDCW | 2187391-4 | 267730 | 1 |  |
| -25 | . . RESISTOR, VARIABLE COMP, 50 K OHMS, $20 \%$, 0.5 W | 2187514-109 | 267679 | 1 |  |
| -26 | . . RESISTOR, FIXED FILM, 27 k OHMS, $2 \%$, 1 w | 2187363-683 | 267772 | 1 |  |
| -27 | - . RESISTOR, FIXED FILM, 120 K OHMS, $2 \%$, 1W | 2187363-699 | 267773 | 1 |  |
| -28 | . . RESISTOR, VARIABLE COMP, 250 K OHMS, $20 \%$ +. 5W | 2187514-110 | 267680 | 1 |  |
| -29 | . . RESISTOR, FIXED FILM, 560 K OHMS, $2 \%$, 1W | 2187363-715 | 267774 |  |  |
| -30 -31 | - . SPACER <br> . . PRINTED CIRCUIT board | $\begin{aligned} & 2184521-16 \\ & 2165469-1 \end{aligned}$ |  | 4 1 |  |
|  | . . inductor (Li) | 2187531-20 | 267714 | 1 |  |



Figure 14. Monoscope Preamplifier Assembly

\begin{tabular}{|c|c|c|c|c|c|}
\hline \[
\left|\begin{array}{c}
\text { FIG. \& } \\
\text { INDEX } \\
\text { NUMBER }
\end{array}\right|
\] \& DESCRIPTION \& DRAWING OR PART NUMBER \& RCA STOCK NUMBER \& QTY. \& NOTES \\
\hline \begin{tabular}{l}
14 - \\
\(-1\) \\
\(-2\) \\
\(-3\) \\
\(-4\) \\
\(-5\) \\
\(-6\) \\
\(-7\) \\
- 8 \\
\(-9\) \\
\(-10\) \\
-11 \\
\(-12\) \\
-13 \\
\(-14\) \\
-15 \\
\(-16\) \\
\(-17\) \\
\(-18\) \\
\(-19\) \\
- 20 \\
- 21 \\
\(-22\)
\end{tabular} \& \begin{tabular}{l}
TERMINAL BOARD ASSY, PREAMPLIFIER \\
(SEE FIGURE 13 FOR NHA) \\
. CAPACITOR, FIXFD, CERAMTC, . \(22 \mathrm{UF}, \pm 20 \%\), 25 VDCW \\
- CAPACITOR, FIXED, SOLID TANIALUM, 2.2 UF, \(\pm 20 \%, 20 \mathrm{VDCW}\) \\
- CAPACITOR, FIXED, CERAMIC DIELECIRIC, .01 UF, \(+80 \%,-20 \%\), 50 VDCW \\
CAPACITOR, FIXED CERAMIC DIELECTRIC, 1000pF \(\pm 10 \%, 1000 \mathrm{VDCW}\) \\
- CAPACITOR, FIXED, MICA DIELECTRIC, 390 PF \(\pm 2 \%, 500\) VDCW \\
- TRANSISTOR \\
- PAD, TRANSISTOR MTG \\
- RESISTOR, FIXED FILM, 100 OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 4.7K OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 2.7K OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED, COMP, 10 OHMS, \(5 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 150 OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 1K OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 220 OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 1.2 K OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 330 OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 5.1K OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- RESISTOR, FIXED FILM, 10.OK OHMS, \(2 \%, 1 / 4 \mathrm{~W}\) \\
- SIGNAL CONNECTOR, BUTTON \\
- LUG TERMINAL \\
- CABLE, COAXIAL \\
- CLIP \\
- PRINTED CIRCUIT BOARD
\end{tabular} \& \[
\begin{aligned}
\& 2110692-501 \\
\& 2187546-1 \\
\& 2187392-1 \\
\& 2187391-5 \\
\& 2187362-3 \\
\& \\
\& 2187356-39 \\
\& 2187379-1 \\
\& 2180896-21 \\
\& 2182165-208 \\
\& 2182165-248 \\
\& 2182165-242 \\
\& 2182068-1 \\
\& 2182165-212 \\
\& 2182165-232 \\
\& 2182165-216 \\
\& 2182165-234 \\
\& 2182165-220 \\
\& 2182165-249 \\
\& 2182165-256 \\
\& 2181460-2 \\
\& 2187604-1 \\
\& 2187641-1 \\
\& 2144176-1 \\
\& 2165409-1
\end{aligned}
\] \& 267824
267731
230028
224570
105778
218992
267797
267722
267695
267700
267699
267787
267696
239949
239949
239950
267698
267701
267702
267952 \& \(R E F\)
6
6
8
6

5
4
5
5
4
4
4
4
4
4
1
1
2
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1 \& <br>
\hline
\end{tabular}



Figure 15. Tickler Driver Module Assembly (Sheet 1 of 2)



Figure 15. Tickler Driver Module Assembly (Sheet 2 of 2)




4305-116-1

Figure 16. Video Driver Module Assembly (Sheet 1 of 2)



Figure 16. Video Driver Module Assembly (Sheet 2 of 2 )



4305-117-1

Figure 17. Low Voltage Power Supply Assembly (Sheet 1 of 3)



Figure 17. Low Voltage Power Supply Assembly (Sheet 2 of 3)

| $\begin{aligned} & \text { FIG. \& } \\ & \text { INDEX } \\ & \text { NUMBER } \end{aligned}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 17 l | - DISK, INSULATOR <br> - LUG, TERMINAL <br> . WASHER, FLAT (NO. 10) <br> - WASHER, LOCK (NO. 10) <br> - RESISTOR, POWER WW, . 43 OHMS, 5\%, $2 W$ <br> . RESISTOR, FIXED WW, 2 OHMS, 5\%, 12W <br> - TERMINAL STRIP <br> ATTACHING PARTS <br> . SCREW, FLAT HD. (NO. 4-40 x 0.25 LG) <br> - WASHER, LOCK (NO. 4) <br> - NUT, (4-40) | 2185811-20 |  | 16 |  |
|  |  | 2183287-2 |  | 16 |  |
|  |  | 82278-106 |  | 16 |  |
|  |  | 93618-112 |  | 16 |  |
|  |  | 2187533-1 | 267711 | 6 |  |
|  |  | 2187534-1 | 267723 | 2 |  |
|  |  | 99158-9 |  | 4 |  |
|  |  | 8924635-105 |  | 8 |  |
|  |  | 93618-105 |  | 8 |  |
|  |  | 57435-103 |  | 8 |  |
| -21 | - GROMMET | 1008816-1 |  | AR |  |
| -22 | - SCREW, PAN HD. (4-40 x 0.50 LG ) | 990104-113 |  | 1 |  |
|  | - NUT (4-40) | 57435-103 |  | 1 |  |
| -23 | . SWITCH, INTERLȮCK ATTACHING PARTS | 2187581-1 | 267721 | 1 |  |
|  | . SCREW, PAN HD. (NO. $6.32 \times 0.25 \mathrm{LG}$ ) | 990106-105 |  | 2 |  |
|  | . WASHER, FLAT (NO. 6) | 82278-104 |  | 2 |  |
|  | . WASHER, LOCK (NO. 6) | 93618-107 |  | 2 |  |
| -24 | - CIRCUIT BREAKER | 2187584-1 | 267719 | 1 | A |
|  | - CIRCUIT BREAKER | 2187584-2 | 301360 | 1 | B |
| -25 | - RELAY, POWER | 2187369-1 | 267724 | 1 | A |
|  | - RELAY, POWER ATTACHING PARTS | 2187369-2 | 304084 | 1 | B |
|  | - NUT, (6-32) | 57435-104 |  | 1 |  |
|  | - WASHER, FLAT (NO, 6) | 82278-104 |  | 1 |  |
|  | . WASHER, LOCK (NO. 6) | 93618-107 |  | 1 |  |
| -26 | - CAPACITOR, FIXED, PAPER DIELECTRIC, 0.1 UF, $\pm 10 \%, 600$ VDCW | 2187637-1 |  | 1 |  |
| -27 | - CAPACITOR, FIXED, CERAMIC DIELECTRIC, . 1 UF, $+80 \%$, $-20 \%, 200$ VDCW | 2187391-4 | 267730 | 1 |  |
| $\begin{array}{r}-28 \\ \hline\end{array}$ | - CAPACITOR, FIXED, .CERAMIC DIELECTRIC, . 1 UF, $+80 \%$, $-20 \%$, 50 VDCW | 2187391-2 | 267728 | 3 |  |
| -29 | . SCREW, PAN HD. (NO. 10-32 x 0.5 LG ) | 990140-113 |  | 3 |  |
|  | . WASHER, EXT TOOTH LOCK (NO. 10) | 93610-112 |  | 3 |  |
|  | - LUG, RING | 8902750-6 |  | 6 |  |
| $-30$ | - GROUND STRAP <br> ATTACHING PARTS | 2144177-501 |  | 1 |  |
| -31 | . SCREW, PAN HD. ( $1 / 4-20 \times 0.75 \mathrm{LG}$ ) | 990139-117 |  | 1 |  |
|  | - WASHER, LOCK (NO. 1/4) | 93618-116 |  | 1 |  |
|  | - WASHER, EXT TOOTH (NO. 1/4) | 93610-116 |  | 2 |  |
|  | - NUT (1/4-20) | 57435-108 |  | 2 |  |
| -32 | - NUT (10-32) | $57435-106$ $82278-106$ |  | 1 |  |
|  | - WASHER, FLAT (NO. 10) <br> . WASHER, LOCK (NO. 10) | 82278-106 |  | 1 |  |
|  | - WASHER, EXT TOOTH (NO. 10) | 93610-112 |  | 1 |  |
| -33 | - BRACKET, CAPACITOR ATTACHING PARTS | 2144521-1 |  | 1 |  |
| -34 | . SCREW, PAN HD. (NO. $10-32 \times 0.5 \mathrm{LG}$ ) <br> . WASHER, EXT TOOTH LOCK (NO. 10) | $\begin{aligned} & 990140-113 \\ & 93610-112 \end{aligned}$ |  | $5$ |  |
|  | ---*-- |  |  |  |  |



4305-117-3

Figure 17. Low Volfage Power Supply Assembly (Sheet 3 of 3)




Figure 18. Low Voltage Power Supply Regulator Assembly (Sheef 1 of 2)



Figure 18. Low Voltage Power Supply Regulator Assembly (Sheet 2 of 2)




Figure 19. Dynamic Focus Module Assembly



4305-120

Figure 20. Keyboard Filter Module Assembly



Figure 21. Station Selection Module Assembly

| $\begin{array}{\|l\|} \text { FIG. \& } \\ \text { INDEX } \\ \text { NUMBER } \end{array}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $-7$ <br> - 8 <br> - 9 <br> $-10$ <br> -11 <br> -12 <br> -13 <br> -14 <br> -15 <br> $-16$ <br> -17 <br> $-18$ <br> $-19$ <br> -20 <br> - 21 | 70/752 STATION SELECTION MODULE SF5707 <br> (SEE FIGURE 1 FOR GENERAL ASSY) <br> MODULE ASSY, 70/752 STATION SELECTION <br> - DIODE, 1N914 <br> - DIODE, 1 N 958 B <br> - CAPACITOR, FIXED, ELECTROLYTIC, 20 UF $-20 \%$, $+150 \%, 6$ VDCW <br> - CAPACITOR, FIXED CERAMIC DIELECTRIC, <br> 0.1 UF, -20 , $+80 \%, 50$ VDCW <br> - CAPACITOR, FIXED ELECTROLYTIC, 20 UF, -20 , $+150 \%$, 50 VDCW <br> - TRANSISTOR, <br> - TRANSISTOR, 2N4074 <br> - PAD, TRANSISTOR MTG <br> . RESISTOR, FIXED FILM, 3.6K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FILM, 180K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FILM, 1.5 K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FILM, 620 OHMS, $2 \%, 2 W$ <br> - RESISTOR, FIXED FILM, 120 OHMS, $2 \%, 1 / 2 W$ <br> - RESISTOR, FIXED FILM, 2.4K OHMS, $2 \%, 1 \mathrm{~W}$ <br> - INTEGRATED CIRCUIT, QUAD TWO LOGIC GATE <br> - INTEGRATED CIRCUIT, DIODE LOGIC GATE EXPANDER <br> - INTEGRATED CIRCUIT, DUAL FOUR LOGIC GATE <br> - INTEGRATED CIRCUIT, BUFFER <br> - INTEGRATED CIRCUIT, SINGLE FLIP-FLOP <br> - INTEGRATED CIRCUIT, DUAL FLIP-FLOP <br> - TERMINAL BOARD, STATION SELECT MODULE <br> . . PHOTOMASTER, VT51 <br> - RESISTOR, FIXED FILM, 200 OHMS, $2 \%, 1 / 2 W$ | MI2100306 2187382-1 $2187354-1$ $2187355-1$ $2187391-2$ $2187355-3$ $2187333-1$ $2187335-1$ $2180896-1$ $2187363-62$ $2187363-103$ $2187363-53$ $2187363-1044$ $2187363-27$ $2187363-658$ $2187270-1$ $2187272-1$ $2187267-1$ $2187269-1$ $2187271-1$ $2187268-1$ $2165471-8$ 2144566 $2187363-32$ | 229936 <br> 267744 <br> 266780 <br> 267728 <br> 266782 <br> 267788 <br> 267789 <br> 270825 <br> 269895 <br> 122117 <br> 269511 <br> 267782 <br> 262016 <br> 258745 <br> 266776 <br> 266778 <br> 266773 <br> 266775 <br> 266777 <br> 266774 <br> 261530 | REF 1 14 2 1 1 3 2 2 2 4 3 2 2 2 2 2 9 3 23 4 4 5 1 1 1 |  |



Figure 22. Mark Format Module Assembly

| $\begin{array}{\|c} \text { FIG. \& } \\ \text { INDEX } \\ \text { NUMBER } \end{array}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QtY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $-10$ $-11$ $-12$ $-13$ $-14$ | 70/752 MARK FORMAT MODULF SF5710 <br> (SEE FIGURE 1 FOR GENERAL ASSY) <br> - LENS, SWITCH CAP <br> MODULE ASSY, 70/752 DATA FORMAT <br> - INTEGRATED CIRCUIT, DUAL FLIP-FLOP <br> - CAPACITOR, FIXED ELECTROLYTIC, 20 UF $-20 \%$, $+150 \%$, 6 VDCW <br> - CAPACITOR, FIXED CERAMIC DIELECTRIC, 0.1 UF - 20\%, +80\% 50 VDCW <br> - TRANSISTOR, 2N4074 <br> . PAD, TRANSISTOR MTG <br> - RESISTOR, FIXED FILM, 200 OHMS $2 \%, 1 / 2 W$ <br> - RESISTOR, FIXED FILM, 4.3K OHMS 2\%, 1/2W <br> - RESISTOR, FIXED FILM, 1.8 K OHMS $2 \%, 1 / 2 \mathrm{~W}$ <br> - RESISTOR, FIXED FILM, 51 OHMS $2 \%, 1 / 2 W$ <br> - INTEGRATED CIRCUIT, DUAL FLIP-FLOP <br> - INTEGRATED CIRCUIT, QUOD TWO LOGIC GATE <br> - INTEGRATED CIRCUIT, DUAL FOUR LOGIC GATE <br> - INTEGRATED CIRCUIT, DIODE LOGIC GATE EXPANDER <br> - INTEGRATED CIRCUIT, BUFFER <br> - TERMINAL BOARD, MARK FORMAT MODULE <br> . . . PHOTOMASTER, VT41 | MI2100309 <br> 2187376-3 <br> 2112705-501 <br> 2187268-2 <br> 2187355-1 <br> 2187391-2 <br> 2187335-1 <br> 2180896-1 <br> 2187363-32 <br> 2187363-64 <br> 2187363-55 <br> 2187363-18 <br> 2187268-1 <br> 2187270-1 <br> 2187267-1 <br> 2187272-1 <br> 2187269-1 <br> 2165471-7 <br> 2144569 | 301555 301660 302085 266780 267728 267789 270825 261530 269518 269513 269504 266774 266776 266773 266778 266775 | REF 1 1 1 1 3 1 2 8 2 2 2 4 19 20 3 1 1 1 |  |



Figure 23. Prinfer Adapter Module Assembly


\begin{tabular}{|c|c|c|c|c|c|}
\hline $$
\left\lvert\, \begin{gathered}
\text { FIG. \& } \\
\text { INDEX } \\
\text { NUMBER }
\end{gathered}\right.
$$ \& DESCRIPTION \& DRAWING OR PART NUMBER \& RCA STOCK NUMBER \& QtY. \& NOTES <br>
\hline $23-18$
-19
-20
-21
-22
-23
-24
-25
-26
-27
-28
-29
-30
-31
-32
-33
-34
-35
-36

-37
-38
-39

-40 \& | - . RESISTOR, FIXED FILM, 51 OHMS, $2 \%, 1 / 2 W$ |
| :--- |
| - RESISTOR, FIXED FILM, 4.3 K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ |
| - RESISTOR, FIXED FILM, 1 K OHMS, $2 \%, 1 / 2 \mathrm{~W}$ |
| - RESISTOR, FIXED FILM, 620 OHMS, $2 \%, 1 / 2 W$ |
| - RESISTOR, FIXED FILM, 160 OHMS, $2 \%, 1 / 2 W$ |
| - RESISTOR, FIXED FILM, 510 OHMS, $2 \%, 1 / 2 W$ |
| - RESISTOR, FIXED FILM, 680 OHMS, 2\%, 1W |
| . RESISTOR, FIXED FILM, 2K OHMS, 2\%, 1W |
| - RESISTOR, FIXED FILM, 910 OHMS, 2\%, 1W |
| - RESISTOR, FIXED FILM, 47 OHMS, $2 \%, 1 / 2 W$ |
| - RESISTOR, FIXED FILM, 390 OHMS, $2 \%, 2 W$ |
| - RESISTOR, FIXED FILM, 390 OHMS, 2\%, 1/2W |
| . RESISTOR, FIXED FILM, 620 OHMS, 2\%, 2W |
| - RESISTOR, FIXED FILM, 120 OHMS, $2 \%, 1 / 2 W$ |
| - RESISTOR, FIXED FILM, 2.4K OHMS, 2\%, 1W |
| - CRYSTAL, QUARTZ |
| - INTEGRATED CIRCUIT, BUFFER |
| - INTEGRATED CIRCUIT, SINGLE FLIP-FLOP |
| - INTEGRATED CIRCUIT, DIODE LOGIC GATE EXPANDER |
| - INTEGRATED CIRCUIT, DUAL FLIP-FLOP |
| - INTEGRATED CIRCUIT, DUAL FOUR LOGIC GATE |
| - INTEGRATED CIRCUIT, QUAD TWO LOGIC GATE |
| - TERMINAL BOARD, PRINTER MODULE |
| - . PHOTOMASTER, VT61 | \& \[

$$
\begin{aligned}
& 2187363-18 \\
& 2187363-64 \\
& 2187363-49 \\
& 2187363-44 \\
& 2187363-30 \\
& 2187363-42 \\
& 2187363-645 \\
& 2187363-656 \\
& 2187363-48 \\
& 2187363-17 \\
& \text { RL } 42 A D 391 G \\
& 2187363-39 \\
& 2187363-1044 \\
& 2187363-27 \\
& 2187363-658 \\
& 2187553-1 \\
& 2187269-1 \\
& 2187271-1 \\
& 2187272-1 \\
& 2187268-1 \\
& 2187267-1 \\
& 2187270-1 \\
& 2165471-6 \\
& 2144571
\end{aligned}
$$

\] \& \[

$$
\begin{aligned}
& 269504 \\
& 269518 \\
& 269509 \\
& 258560 \\
& 269505 \\
& 261590 \\
& 264811 \\
& 267766 \\
& 262025 \\
& 267753 \\
& \\
& 261455 \\
& 267782 \\
& 262016 \\
& 258745 \\
& 267709 \\
& 266775 \\
& 266777 \\
& 266778 \\
& \\
& 266774 \\
& 266773 \\
& 266776
\end{aligned}
$$

\] \& \[

$$
\begin{aligned}
& 1 \\
& 1 \\
& 3 \\
& 1 \\
& 1 \\
& 3 \\
& 1 \\
& 1 \\
& 1 \\
& 1 \\
& 1 \\
& 1 \\
& 3 \\
& 1 \\
& 1 \\
& 1 \\
& 1 \\
& 2 \\
& 2
\end{aligned}
$$
\] \& <br>

\hline
\end{tabular}

| FIG. 8 INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | Qiy. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 24- $\begin{array}{rl} -1 \\ - & 2 \\ -4 \\ -3 \\ -4 & 4 \\ - & 5 \\ - & 6 \end{array}$ | CABLE ASSY, 5 FOOT KEYBOARD EXTENSION <br> (SEE FIGURE 1 FOR GENERAL ASSY) <br> CABLE ASSY, 10 FOOT KEYBOARD EXTENSION <br> (SEE FIGURE 1 FOR GENERAL ASSY) <br> CABLE ASSY, 15 FOOT KEYBOARD EXTENSION <br> (SEE FIGURE 1 FOR GENERAL ASSY) <br> CABLE ASSY, 20 FOOT KEYBOARD EXTENSION <br> - insulator, elect socket <br> - insulator, elect pin <br> - hood, elect connector <br> . GUIDE, PIN <br> - Guide, socket <br> - CABLE, KEYBOARD EXTENSION | $2112704-501$ $2112704-502$ $2112704-503$ $2112704-504$ $218512-1$ $2187512-2$ $2187512-9$ $218512-8$ $2187512-7$ $2187374-1$ | $\begin{aligned} & 267690 \\ & 228243 \\ & 228244 \end{aligned}$ | $\begin{gathered} \mathrm{REF} \\ \mathrm{REF} \\ \mathrm{REF} \\ \mathrm{REF} \\ 1 \\ 1 \\ 2 \\ 2 \\ 2 \\ 2 \\ 1 \end{gathered}$ |  |



## R-1



Figure 25. RCA High Voltage Power Supply, A13

| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | Qty. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 25- |  | $2166024-503$ 2166110 |  | REF REF |  |
| -1 | - A1 MODULE ASSY., HIGH VOLTAGE DRIVER | 2166051-502 |  | 1 |  |
| -2 | . A2 MODULE ASSY., -1.8 KV REGULATOR ATTACHING PARTS CONTACT | 2166049-501 2187548-2 |  | 1 1 |  |
| -3 | - A3 MODULE ASSY., 12KV REG/SYNC CONVERTER | 2166092-502 |  | 1 |  |
| -4 | . A4 module assy., high voltage focus ATTACHING PARTS <br> NUT, HEX (NO. 6-32) <br> WASHER, EXT. TOOTH (NO. 6) $\qquad$ | $\begin{aligned} & 2166094-501 \\ & 57435-54 \\ & 93610-57 \end{aligned}$ |  | $1$ |  |
| -5 | - A5 MODULE ASSY., TRANSFORMER INTERFACE ATTACHING PARTS <br> LUG, TERMINAL (NO. 4) <br> NUT, HEX (NO. 4-40) <br> WASHER, EXT. TOOTH (NO. 4) | $\begin{aligned} & 2166107-503 \\ & 8982998-12 \\ & 57435-53 \\ & 93610-55 \end{aligned}$ |  | $\begin{aligned} & 1 \\ & 2 \\ & 3 \\ & 3 \end{aligned}$ |  |
| -6 | - A6 MODULE ASSY., LOW VOLTAGE Interface ATTACHING PARTS NUT, HEX (NO. 6-32) SCREW, THD CUT (NO. 6-32 x. 31 LG) STRAP, RETAINING-CABLE WASHER, EXT TOOTH (NO. 6) | $\begin{aligned} & 2166102-503 \\ & 57435-54 \\ & 1402672-134 \\ & 2183004-301 \\ & 93610-57 \end{aligned}$ |  | $\begin{aligned} & 1 \\ & 2 \\ & 2 \\ & 2 \\ & 2 \end{aligned}$ |  |
| -7 | - A7 MODULE ASSY., HIGH VOLTAGE MULTIPLIER | 2166109-501 |  | 1 |  |
| -8,-9 | - C1, C2 CAPACITOR FIXED . 05 uf, 3 KV ATtACHING PARTS <br> LUG, TERMINAL (NO. 8) <br> NUT, HEX (NO. 8-32) <br> WASHER, EXT. TOOTH (NO. 8) $\qquad$ | $\begin{aligned} & 2187832-1 \\ & 8982998-15 \\ & 57435-55 \\ & 93610-59 \end{aligned}$ |  | $\begin{aligned} & 2 \\ & 2 \\ & 4 \\ & 4 \end{aligned}$ |  |
| -10 | - CHASSIS <br> ATTACHING PARTS <br> LABEL - DANGER HIGH VOLTAGE ---*--- | $2166057-501$ $2184092-5$ |  | 1 1 |  |
| $\left\lvert\, \begin{gathered} -11 \text { thru } \\ -14 \end{gathered}\right.$ | - XA1,2,3,4 CONNECTOR, RECEPTACLE ATTACHING PARTS | 218548-1 |  | 4 |  |
|  | SCREW, FL HD (NO. 6-32 x . 50 LG ) | 8924639-113 |  | 8 |  |
|  | NUT, SPRING -U TYPE (NO. 6-32) | 990303-64 |  | 8 |  |
| -15 | - xa6 connector receptacle | 2187548-1 |  | 1 |  |
| -16 | - COVER ATTACHING PARTS | 2166064-1 |  | 1 |  |
|  | SCREW, THD CUT (NO. 4-40 x . 31 LG) ---*--- | 1402672-114 |  | 4 |  |
| -17 | . E1 SCREW, THD FORM (NO. 4-40 x . 38 LG) ATTACHING PARTS | 2187254-2 |  | 1 |  |
|  | WASHER, EXT. TOOTH (NO. 4) $\qquad$ | 93610-55 |  | 1 |  |
| -18 | - E. 3 STRAP, GROUNDING | 2166081-1 |  | 1 |  |
| -19 | - KNOB | 2166076-501 |  | $1$ |  |
| -20 | - R1 RESISTOR, FIXED <br> 22 K OHMS, $+2 \%, 2 \mathrm{~W}$ <br> ATTACHING PARTS | 2187363-1081 |  | $1$ |  |
|  | LUG, TERMINAL (NO. 8) ---*--- | 8982998-15 |  | 2 |  |
| -21 | . T1 TRANSFORMER -6V At'taching parts | 2166250-2 |  | 1 |  |
|  | CABLE, H.V. AWG NO. 24 | 2010706-206 |  | AR |  |
|  | DECAL, (WARNING) | 2166226-1 |  | 1 |  |
|  | NUT, HEX (10-32) | 57435-56 |  | $1$ |  |
|  | SPACER, HEX (10-32 x 1.00 LG) TERMINAL <br> WASHER EXT. TOOTH (NO, 10) | $\begin{aligned} & 82207-11 \\ & 2187864-1 \\ & 93610-62 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1 \\ & 1 \\ & 2 \\ & \hline \end{aligned}$ |  |



THERMAL COMPOUND BOTH SIDES OF MICA INSULATOR

[^7]figure 26. AI Module Assy., High Voltage Driver

|  |  | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |

R-1


70/752•D210

Figure 27. A2 Module Assy., -1.8 Kv Regulator

|  |  | DRAWING OR PART NUMBER | RCA STOCK NUMBER | Qry. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |



70/752-0208

Figure 28. A3 Module Assy., 12 Kv Reg/Sync Converter


| $\left\lvert\, \begin{aligned} & \text { FIG. \& } \\ & \text { INDEX } \\ & \text { NUMBER } \end{aligned}\right.$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 29- | MODULE ASSY., HIGH VOLTAGE FOCUS <br> (ASSEMBLY A4 OF RCA H.V.P.S. 2166024) <br> SChEMATIC <br> - CR1 DIODE, 1N3563 <br> - CR2, CR3 DIODE, 1 N992B <br> - COATING, CONFORMAL <br> - E1 SCREW (NO. 6-32 x.375) <br> - NUT (NO. 6) <br> - R1 RESISTOR, FIXED 12MEG OHMS $\pm 5 \% 1 \mathrm{~W}$ <br> - R2 RESISTOR, VARIABLE 5MEG OHMS $\pm 20 \%$ 2W <br> - WASHER, FLAT <br> - WASHER, LOCK <br> - NUT, (.375-32) <br> - R3 RESISTOR, FIXED 8.7MEG OHMS $\pm 5 \%$ 1W <br> - R4 thru R6 RESISTOR, FIXED 220 K OHMS $\pm 20 \%$ 2W <br> - PRINTED CIRCUIT BOARD | $\begin{aligned} & 2166094-501 \\ & 2166110 \\ & 2187822-1 \\ & 2187881-1 \\ & 2188335 \\ & 990106-59 \\ & 57435-54 \\ & 2187838-2 \\ & 2187836-1 \\ & 82278-125 \\ & 93610-122 \\ & 59149-106 \\ & 2187838-1 \\ & 2187363-1105 \\ & 2166095-1 \end{aligned}$ |  | REF REF 1 2 $A / R$ 1 1 1 1 1 1 1 1 1 1 1 |  |



70/752.0209

Figure 29. A4 Module Assy,, High Voltage Focus

| FIG. \& INDEX NUMBER | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | Qty. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 30- | MODULE ASSY., TRANSFORMER INTERFACE <br> (ASSEMBLY A5 OF RCA H.V.P.S. 2166024) <br> SCHEMATIC <br> CR2 DIODE <br> - E1 thru E3 SCREW (4-40 x.375) ATTACHING PARTS <br> NUT (NO. 4) <br> - PRINTED CIRCUIT BOARD | $\begin{aligned} & 2166107-503 \\ & 2166110 \\ & 2187824-1 \\ & 990104-59 \\ & \\ & 57435-53 \\ & 2166108-1 \end{aligned}$ |  | $\begin{gathered} \text { REF } \\ \text { REF } \\ 1 \\ 3 \\ 3 \\ 1 \end{gathered}$ |  |



Figure 30. A5 Module Assy., Transformer Inferface

R-1

|  <br> INDEX <br> NUMBER | DESCRIPTION | DRAWING OR <br> PART NUMBER | RCA STOCK <br> NUMBER | QTY. |
| :--- | :--- | :--- | :--- | :--- | NOTES



10/732.0212

Figure 31. A6 Module Assy., Low Volfage Inferface

\begin{tabular}{|c|c|c|c|c|c|}
\hline FIG. \& INDEX NUMBER \& DESCRIPTION \& DRAWING OR PART NUMBER \& RCA STOCK NUMBER \& Qty. \& NOTES \\
\hline 32- \& \begin{tabular}{l}
```
MODULE ASSY., HIGH VOLTAGE MULTIPLIER
(ASSEMBLY A7 OF RCA H.V.P.S. 2166024)
SCHEMATIC
- C1, C2 CAPACITOR, FIXED
.01 uf GMV, 3KV
. C3 thru C9 CAPACITOR, FIXED
.002 uf GMV, 6KV
. CR1 thru CR9 DIODE
- R1 RESISTOR, FIXED
2. 2MEG OHMS + 5%, 2W
- R2 RESISTOR, FIXED
1000MEG OHMS }\pm15%,6
ATTACHING PARTS
CABLE, HIGH VOLTAGE
AWG NO. 24
COATING, CONFORMAL
CONTACT
LEAD, ELECT, ANODE
LUG, TERMINAL (NO. 4 MINIATURE)
LUG, TERMINAL
STRAP, RETAINING, CABLE
- COMPONENT BOARD
``` \\
REPAIR OF THIS MODULE IS NOT RECOMMENDED, HOWEVER WHEN RERAIRS ARE MADE THE CONFORMAL COATING MUST BE REPLACED TO PREVENT ARCING.
\end{tabular} \& \(2166109-501\)
2166110
\(2187847-1\)
\(2187847-2\)
\(2187824-1\)
\(99126-239\)
\(2187840-1\)
\(2010706-206\)
\(2188335-1\)
\(2187548-2\)
\(2166255-1\)
\(8982998-3\)
\(8982998-12\)
\(2183004-301\)
\(2166187-501\) \& \& REF
REF
2
2
7
9
1
1

AR
AR
3
1
1
1
1 \& <br>
\hline
\end{tabular}


$70 / 752.0206$
Figure 32. A7 Module Assy., High Voltage Multiplier

## APPENDIX B

VENDOR PARTS INFORMATION

AMC-M-227 HIGH VOLTAGE POWER SUPPLY
HIGH VOLTAGE POWER SUPPLY - 100425 Rev. D

| ITEM | QUAN | PART NO. | $\begin{gathered} \text { REF } \\ \text { DESIG } \end{gathered}$ | DESCRIPTION | $\begin{aligned} & \text { VENDOR } \\ & \text { OR } \\ & \text { SPEC. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 600773 |  | Base | AMC |
| 2 | 1 | 600749 | Al | High Voltage Rectifier | AMC |
| 3 | 1 | 600752 | A2 | High Voltage Regulator | AMC |
| 4 | 1 | 600777-301 |  | Panel Side Left | AMC |
| 5 | 1 | MS8-140 | MS | Marker Strip | Cinch Jones |
| 6 | 1 | 600774 | Tl | Transformer Assy | AMC |
| 7 | 1 | 600777-302 |  | Panel Side Right | AMC |
| 8 | 1 | 2643 |  | Insulated Stand-Off $\frac{1}{2}$ " | H. H. Smith |
| 9 | 4 | 2603 |  | Insulated Stand-Off 1" | H. H. Smith |
| 10 | 2 | 7118 |  | Screws-Binding Hd 6-32 x $\frac{1}{2}$ long |  |
| 11 | 17 | 6155 |  | Washers-Flat \#6. . 38 dia. lge. dia. | C. |
| 12 | 16 | 7356 |  | Washers-External Lock \#6 | C. |
| 13 | 17 | 6091 |  | Screws-Sheet Metal \#6 $\frac{1}{4}$ " long | C. |
| 14 | 5" |  |  | Grommet Strip |  |
| 15 | A/R |  |  | RTV 108 (Epoxy) | G.E. |
| 16 | 8 | 6042 |  | Hex Nuts, \#6 (Small Pattern) | C. |
| 17 | 4 | 7153 |  | Screw Binding Hd 6-32 x 3/8 | C. |
| 18 | 2 | 7152 |  | Screw Binding Hd 6-32 x l/4 | C. |
| 19 | 1 | RC20GF395J | R1 | Resistor 3.9Meg $\frac{1}{2} \mathrm{~W}$ 10\% | Mil-R-ll |
| 20 | 1 | 30GA-Sl0 | Cl | Capacitor . Oluf 3KV | Sprague |
| 21 | 1 | 600776 |  | Wiring Harness | AMC |
| 22 | Ref | 100423 |  | Schematic | AMC |
| 23 | 1 | 600778 |  | Insulator-Mylar | AMC |
| 24 | 3 | C8094-632-4 |  | Tinnermin Speed Nuts |  |
| 25 | 3 | 1416-6 |  | Solder Lug | Smith |
| 26 | 1 | 700046 |  | Insulator Regulator Board |  |
| 27 | 1 | 600990 | Ref | Wiring Harness Layout | AMC |
| 28 | 1 | 2602 |  | Insulated Stand Off (Ceramic) 3/4" | Smith |
| 29 | 1 |  |  | Nylon Screw 6/32 x 3/8 |  |
| 30 | 4 |  |  | 6/32 Reduced dia. flat washer |  |
| 31 | 2" |  |  | \#8GA Black Vinyl Sleeving |  |
| 32 | 2 | 8573C |  | Spade Bolt 6-32 | Walsco |
| 33 | 2 | 600779 |  | Heat Dissipator | AMC |
| 34 | 2 | MS 20470-A3-4 |  | Rivet for spade bolt 3/32 dia. $x^{\frac{1}{4}}$ "L |  |
| 35 |  | $\begin{aligned} & \text { 2N5 } 294 \text { or } \\ & \text { TIP } 14 \end{aligned}$ | Q9 | Transistor | $\begin{aligned} & \text { RCA or } \\ & \text { T.I. } \end{aligned}$ |
| 36 | X | $\begin{aligned} & \text { 2N5 } 294 \text { or } \\ & \text { TIP } 14 \end{aligned}$ | Q11 | Transistor | $\begin{aligned} & \text { RCA or } \\ & \text { T.I. } \end{aligned}$ |

ASTRO-METRIX CORP. - PARTS LIST
AMC-M-227 HIGH VOLTAGE POWER SUPPLY
HIGH VOLTAGE REGULATOR - 600752 Rev. D

| ITEM | QUAN. | PART NO. | $\begin{gathered} \text { REF } \\ \text { DESIG } \end{gathered}$ | DESCRIPTION | VENDOR <br> OR <br> SPEC. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 600754 |  | Circuit Board | AMC |
| 2 |  | 100423 | Ref | Schematic |  |
| 3 | 1 | IN914B | CR12 | Diode, 100ma (Fast Recovery) |  |
| 4 | 1 | WMF6P1 | C1 | Capacitor 0.1uf 600V | CDE |
| 5 | 1 | WMFID47 | C2 | Capacitor . 0047uf 100V | CDE |
| 6 | 1 | C280AE/A220K | C3 | Capacitor . 22 250V $\pm 10 \%$ | Amperex |
|  |  | WMF1P22 | C3 | Capacitor . 22 100V $\pm 10 \%$ | CDE |
| 7 | 1 | C426AR/G1 | C4 | Capacitor 1mf 40V | Amperex |
|  |  | TE1200 | C4 | Capacitor luf 25V | Sprague |
| 8 | 1 | C280AE/A100K | C5 | Capacitor 1mf 250V $\pm 10 \%$ | Amperex |
|  |  | WMFIPI | C5 | Capacitor 0.1uf 100V $\pm 10 \%$ | CDE |
| 9 | 2 | C280AE/A22K | C6 | Capacitor . $022 \mathrm{mf} 250 \mathrm{~V} \pm 10 \%$ | Amperex |
|  |  | WMF1S22 | C6 | Capacitor . 022 uf 100V | CDE |
| 10 | x | C280AE/A 2 2K | C7 | Capacitor . $022 \mathrm{mf} 250 \mathrm{~V} \pm 10 \%$ | Amperex |
|  |  | WMF1S22 | C7 | Capacitor . $022 \mathrm{mf} \mathrm{100V} \pm 10 \%$ | CDE |
| 11 | 1 | 1 N823 | CR1 | Diode, Zener T.C. |  |
| 12 | 4 | 5110 (10D05) | CR2 | Diode 50V 1 Amp | AMC |
| 13 | X | 5110 (10D05) | CR3 | Diode 50V 1 Amp | AMC |
| 14 | 1 | 1N751 | CR4 | Diode, Zener |  |
| 15 | X | 5110 (10D05) | CR5 | Diode 50V 1 Amp | AMC |
| 16 | X | 5110 (10D05) | CR6 | Diode 50V 1 Amp | AMC |
| 17 | 5 | 1 N 2071 -A | CR7 | Diode 500V 1 Amp | Mallory |
|  |  | 5210 (10D5) | CR7 | Diode 500V 1 Amp | AMC |
| 18 | X | 1N2071-A | CR8 | Diode 500V 1 Amp | Mallory |
|  |  | 5210 (10D5) | CR8 | Diode 500V 1 Amp | AMC |
| 19 | x | 1N2071-A | CR9 | Diode 500V 1 Amp | Mallory |
|  |  | 5210 (10D5) | CR9 | Diode 500V 1 Amp | AMC |
| 20 | x | 1 N 2071 -A | CR10 | Diode 500V 1 Amp | Mallory |
|  |  | 5210 (10D5) | CR10 | Diode 500V 1 Amp | AMC |
| 21 | X | 1 N 2071 -A | CR11 | Diode 500V 1 Amp | Mallory |
|  |  | 5210 (10D5) | CR11 | Diode 500V 1 Amp | AMC |
| 22 | 6 | 2N3565 | Q1 | Transistors | Fair |
| 23 | 2 | 2N3646 | Q2 | Transistors | Fair |
| 24 | x | 2N3565 | Q3 | Transistors | Fair |
| 25 | x | 2N3565 | Q4 | Transistors | Fair |
| 26 | X | 2N3565 | 85 | Transistor | Fair |
| 27 | 5 | 2N3567 | 86 | Transistor | Fair |
| 28 | X | 2N3567 | Q7 | Transistor | Fair |
| 29 | 1 | 40327 | Q8 | Transistor | RCA |
| 30 | 1 | TO-5 PAD |  | TO-5 Transistor Pad (Nylon) |  |
| 31 | X | 2N3567 | Q10 | Transistor | Fair |
| 32 |  |  |  | Deleted |  |
| 33 | x | 2N3567 | Q12 | Transistor | Fair |
| 34 | x | 2N3646 | Q13 | Transistor | Fair |
| 35 | X | 2N3567 | 814 | Transistor | Fair |
| 36 | X | 2N3565 | 215 | Transistor | Fair |
| 37 | X | 2N3565 | Q16 | Transistor | Fair |



AMC-M-227 HIGH VOLTAGE POWER SUPPLY
HIGH VOLTAGE REGULATOR - 600752 Rev. D (Cont'd.)

| ITEM | QUAN. | PART NO. | $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | VENDOR <br> OR <br> SPEC. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 38 | 2 | RN7 0C1504F | R1 | Resistor 1.5M 1\% | Mil-R-10509 |
| 39 | 2 | RC20GF103J | R2 | Resistor 10K 1/2W | Mil-R-11 |
| 40 | 1 | RN60C4222F | R3 | Resistor 42.2K 1\% | Mil-R-10509 |
| 41 | 1 | MTC-14L1 | R4 | Resistor (Pot) 10K | Mallory |
| 42 | 1 | 3007P-1-502 | R5 | Resistor (Pot) 5K | Bourns |
| 43 | 1 | RN60C1822F | R6 | Resistor 18.2K 1\% $\frac{1}{2} \mathrm{~W}$ | Mil-R-10509 |
| 44 | 1 | RC20GF225J | R7 | Resistor 2.2M $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 45 | 1 | RC20GF473J | R8 | Resistor 47K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 46 | 1 | RC20GF754J | R9 | Resistor $750 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 47 | 1 | RL20S122G | R10 | Resistor 1. $2 \mathrm{~K} 2 \% \frac{1}{2} \mathrm{~W}$ | Mil-R-22684 |
| 48 | 3 | RC20GF474J | R11 | Resistor 470K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 49 | 1 | RL20S823G | R12 | Resistor 82K 2\% $\frac{1}{2} \mathrm{~W}$ | Mil-R-22684 |
| 50 | 1 | RC20GF223J | R13 | Resistor $22 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 51 | X | RC20GF474J | R14 | Resistor 470K $\frac{1}{2} \mathrm{~W}$ | Mil- R-11 |
| 52 | 2 | RC20GF104J | R15 | Resistor 100K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 53 | X | RC20GF103J | R16 | Resistor 10K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 54 | X | RC20GF103J | R17 | Resistor 10K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 55 | x | RC20GF103J | R18 | Resistor $10 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 56 | 1 | RC20GF220J | R19 | Resistor 22 Ohm $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 57 | 1 | RC20GF682J | R20 | Resistor $6.8 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 58 | 2 | RC42GF511J | R21 | Resistor 510 Ohm 2W | Mil-R-11 |
| 59 | 2 | RC20GF153J | R22 | Resistor $15 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 60 | 1 | PW5 | R23 | Resistor 5 Ohm 5W (Axial) | IRC |
| 61 | 2 | RC20GF471J | R24 | Resistor 470 Ohm $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 62 | X | RC20GF153J | R25 | Resistor $15 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 63 | X | RC42GF511J | R26 | Resistor 510 Ohm 2W | Mil-R-11 |
| 64 | x | RC20GF103J | R27 | Resistor $10 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 65 | x | RN70C1504F | R28 | Resistor 1.5M 1\% | Mil-R-10509 |
| 66 | 1 | RC20GF472J | R29 | Resistor 4.7K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 67 | x | RC20GF103J | R30 | Resistor 10K $\frac{1}{2} \mathrm{~W} 5 \%$ | Mil-R-11 |
| 68 | 3 | RC20GF222J | R31 | Resistor $2.2 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 69 | X | RC20GF471J | R32 | Resistor 470 Ohm $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 70 | 1 | RC20GF272J | R33 | Resistor 2.7K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 71 | x | RC20GF222J | R34 | Resistor $2.2 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 72 | X | RC20GF222J | R35 | Resistor $2.2 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 73 | X | RC20GF104J | R36 | Resistor 100K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 74 | x | RC20GF103J | R37 | Resistor $10 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ | Mil-R-11 |
| 75 | x | RC20GF474J | R38 | Resistor 470K $\frac{1}{2} \mathrm{~W}$ | Mil-R-11 |



ASTRO-METRIX H.V. REGULATOR

AMC-M-227 HIGH VOLTAGE POWER SUPPLY
CIRCUIT BOARD ASSY HIGH VOLTAGE RECTIFIER - 600749 Rev. D

| ITEM | QUAN. | PART NO. | $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | VENDOR <br> OR <br> SPEC. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 600751 |  | Circuit Board | AMC |
| 2 |  | 100423 | Ref | Schematic | AMC |
| 3 | 1 | BS-41162SB |  | Spade Lug | Hollingsworth |
| 4 | 5 | DD60-202 | C1 | Capacitor . O02uf 6KV | CENT |
| 5 | X | DD60-202 | C2 | Capacitor . O02uf 6KV | CENT |
| 6 | X | DD60-202 | C3 | Capacitor . O02uf 6KV | CENT |
| 7 | X | DD60-202 | C4 | Capacitor . O02uf 6KV | CENT |
| 8 |  |  | C5 | Deleted |  |
| 9 | X | DD60-202 | C6 | Capacitor . 002uf 6KV | CENT |
| 10 | 1 | DD30-502 | C7 | Capacitor . O05uf 3KV | CENT |
| 11 |  |  | C8 | Deleted |  |
| 12 | 1 | C280AE/A10K | C9 | Capacitor . 01 250V | AMPEREX |
|  |  | WMF1S1 |  | Capacitor . Oluf 100V | CDE |
| 13 | 4 | US111HFP | CR1 | Diode 8KV, 1.2MA | INT |
| 14 | X | US111HFP | CR2 | Diode 8KV, 1.2MA | INT |
| 15 | X | US111HFP | CR3 | Diode 8KV, 1.2MA | INT |
| 16 | 1 | 5AM6 | CR4 | Diode 6KV, 5MA | ASI |
| 17 | X | US111HFP | CR5 | Diode 8KV, 1.2MA | INT |
| 18 | 2 In . | 1/8 HT105 |  | Shrink Tubing 3/8" (1/8 A/S) |  |
| 19 | 3 In . | 1/16 HT105 |  | Shrink Tubing 5/32" (1/16 A/S) |  |
| 20 | A/R |  |  | HV Paint |  |
| 21 | 42 In . |  |  | HV Insulated Wire Red Rulin |  |
| 22 | 1 | 8637 |  | Crt. Anode Connector \& Lead | GC |
| 23 |  |  | R1 | Delete |  |
| 24 | 1 | RC4 2GF155J | R2 | Resistor 1.5Meg 2W $\pm 10 \%$ | Mil-R-11 |
| 25 | 4 | RN70C1504F | R3 | Resistor 1.5M 1\% | Mil-R-11 |
| 26 | X | RN70C1504F | R4 | Resistor 1.5M 1\% | Mil-R-11 |
| 27 | x | RN70C1504F | R5 | Resistor 1.5M 1\% | Mil-R-11 |
| 28 | X | RN70C1504F | R6 | Resistor 1.5M 1\% | Mil-R-11 |
| 29 | 5 | RC42GF565J | R7 | Resistor 5.6M 2W $\pm 5 \%$ | Mil-R-11 |
| 30 | X | RC42GF565J | R8 | Resistor $5.6 \mathrm{M} \mathrm{2W} \pm 5 \%$ | Mil-R-11 |
| 31 | X | RC4 2GF565J | R9 | Resistor 5.6M 2W $\pm 5 \%$ | Mil-R-11 |
| 32 | X | RC42GF565J | R10 | Resistor $5.6 \mathrm{M} \mathrm{2W} \pm 5 \%$ | Mil-R-11 |
| 33 | X | RC42GF565J | R11 | Resistor 5.6M 2W | Mil-R-11 |
| 34 | 1 | PTA755L | R12 | Resistor (Pot) 7.5M 1W | Mallory |
| 35 | 2 | RC42GF435J | R13 | Resistor 4.3M 2W $\pm 5 \%$ | Mil-R-11 |
| 36 | X | RC42GF435J | R14 | Resistor 4.3M 2W $\pm 5 \%$ | Mil-R-11 |
| 37 | 1 | RC32GF104J | R15 | Resistor 100K 1W | Mil-R-11 |
| 38 | 1 | 7153 |  | Screw 6/32 3 /8" Long S.C.P. | G.C. |
| 39 | 1 | 1416-6 |  | Solder Lug \#6 Int. Tooth | Smith |
| 40 | 1 | 2603 |  | Ceramic Standoff $1^{\prime \prime}$ Long 6/32 thd. | Smith |
| 41 42 | 2 1 | 5703 |  | Solder Lug \#6 Hole Nylon Screw 6/32×3/8L. | G.C. |



70/752-0201

ASTRO-METRIX H.V. RECTIFIER

HVPS - ITT

| ITEM | REF DESIG | PART NO. | DESCRIPTION | VENDOR |
| :---: | :---: | :---: | :---: | :---: |
| 1 | R2 | RN70C4993F | Res. 499K lW l\% | IRC |
| 2 | R3 | RC20GFl05K | Res. 1 Meg, $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 3 | R4 | RN65C3013F | Res. 301K, $\frac{1}{2} \mathrm{~W}$ 1\% | IRC |
| 4 | R5 | RN65Cl002F | Res. $10 \mathrm{~K}, \frac{1}{2} \mathrm{~W}$ 1\% | IRC |
| 5 | R6 | RC20GFl01K | Res. 100 Ohm $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 6 | R7 | RC20GF224K | Res. 220K, $\frac{1}{2} \mathrm{~W}$ 10\% | IRC |
| 7 | R8 | RC20GF684K | Res. 680K, $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 8 | R9 | RC20GF102K | Res. $1 \mathrm{~K}, \frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 9 | RlO | RC20GFl01K | Res. 100 Ohm, $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 10 | R11 | RC20GF222K | Res. $2.2 \mathrm{~K}, \frac{1}{2} \mathrm{~W} 10 \%$ | Ohmite |
| 11 | R12 | RC20GFl01K | Res. loo Ohm, $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 12 | R13 | RC20GFl02K | Res. $1 \mathrm{~K}, \frac{1}{2} \mathrm{~W} 10 \%$ | Ohmite |
| 13 | R14 | RC20GF223K | Res. $22 \mathrm{~K}, \frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 14 | R15 | RC20GF101K | Res. 100 Ohm, $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 15 | R16 | RC20GF470K | Res. 47 Ohm $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 16 | R17 | RC20GFl03K | Res. 10K $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 17 | R18 |  | Res. 1 Ohm $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 18 | R19 |  | Res. 1 Ohm $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 19 | R20 |  | Res. 1 Ohm $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 20 | R21 |  | Res. 1 Ohm $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 21 | R22 | RC2OGFl02K | Res. $1 \mathrm{~K} \frac{1}{2} \mathrm{~W} 10 \%$ | Ohmite |
| 22 | R23 | R3 2GFl05K | Res. 1 Meg , 1W, 10\% | Ohmite |
| 23 | R24 |  | Res. l00K $\frac{1}{2} \mathrm{~W} \mathrm{10} \mathrm{\%}$ |  |
| 24 | R25 | R20GFl5 2K | Res. 1.5K $\frac{1}{2} \mathrm{~W} \mathrm{10} \mathrm{\%}$ | Ohmite |
| 25 | R26 | RC20GF153K | Res. $15 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 26 | R27 | RC20GFl02K | Res. $1 \mathrm{~K} \frac{1}{2} \mathrm{~W} 10 \%$ | Ohmite |
| 27 | R28 | RC20GFl53K | Res. 15K $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 28 | R29 | RC32GFl05K | Res. 10 Meg , 2W 1\% | Dale |
| 29 | R30 | RC32GFl05K | Res. 10 Meg , $2 \mathrm{~W} 1 \%$ | Dale |
| 30 | R31 | RC20GF104K | Res. l00K $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 31 | - R32 | 62PR50K | Pot 50K-Hellitrim. | Bourns |
| 32 | R33 | RC20GFl01K | Res. 100 Ohm $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 33 | R34 | RC20GF75 2K | Res. 7.5K $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 34 | R35 | RC20GF563K | Res. $56 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 35 | R36 | RN65E1823F | Res. 182K $\frac{1}{2} \mathrm{~W}$ 1\% | IRC |
| 36 | R37 |  | Res. 470K $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 37 | R38 | RC32GF105K | Res. $100 \mathrm{Meg}, 2 \mathrm{~W} 5 \%$ | IRC |
| 38 | R39 | RC32GF105K | Res. 100 Meg , 2W 5\% | IRC |
| 39 | R41 | 62PR100K | Pot, l00K-Hellitrim | Bourns |
| 40 | R42 | Type RN65 | Res. $100 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ l\% | IRC |
| 41 | R43 | RC20GF104K | Res. 100K $\frac{1}{2} \mathrm{~W}$ 15\% | Ohmite |
| 42 | R44 | RC20GFl 01 K | Res. 100 Ohm $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 43 | R45 | RC20GF223K | Res. $22 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 44 | R46 | RC20GF473K | Res. $47 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 45 | R47 | RC2OGFl02K | Res. 1K $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 46 | R48 | RC20GFl02K | Res. $1 \mathrm{~K} \frac{1}{2} \mathrm{~W} 10 \%$ | Ohmite |
| 47 | R49 | RC3 2GF105K | Res. 100 Meg , 2W 5\% | IRC |
| 48 | R50 | Type HVC | Pot $20 \mathrm{Meg}-30 \%$ (Focus) | CTS |
| 49 | R51 |  | Res. $10 \mathrm{Meg}, 2 \mathrm{~W} \pm 10 \%$ |  |
| 50 | R5 2 |  | Res. $22 \mathrm{Meg}, 2 \mathrm{~W} \pm 10 \%$ |  |

PARTS LIST
HVPS - ITT

| ITEM | REF DESIG | PART NO. | DESCRIPTION | VENDOR |
| :---: | :---: | :---: | :---: | :---: |
| 51 | R54 | RC20GF332K | Res. 3.3K $\frac{1}{2} \mathrm{~W} 10 \%$ | Ohmite |
| 52 | R55 | RC20GF103K | Res. $10 \mathrm{~K} \frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 53 | R56 | RC20GFl03K | Res. 10K $\frac{1}{2} \mathrm{~W}$ 10\% | Ohmite |
| 54 | C2 | WMFlSl | Cap. $01 \mathrm{Mf} \mathrm{l00V}$ | Cornell-Dubilier |
| 55 | C3 | WMF6S68 | Cap . 068 Mf , 600V | Cornell-Dubilier |
| 56 | C4 | WMF6S68 | Cap . 068 Mf , 600V | Cornell-Dubilier |
| 57 | C5 | TE1307 | Cap 50 Mf , 50V | Sprague |
| 58 | C6 | WMF-1S33 | Cap . 033 Mf , l00V | Cornell-Dubilier |
| 59 | C7 | WMF6S68 | Cap . 068 Mf , 600V | Cornell-Dubilier |
| 60 | Cl4 | WMFlD33 | Cap . 0033 Mf , l00V | Cornell-Dubilier |
| 61 | Cl7 | 30GASl0 | Cap . 01 Mf , 3KV | Sprague |
| 62 | C20 | Type C K6R8C35K | Cap 6.8 Mf, 35V | Kemet |
| 63 | C23 | TE1211 | Cap 100 Mf , 25V | Sprague |
| 64 | C25 | DM19-47L | Cap. 470pf | Elmenco |
| 65 | CR1 | 1 N936 | Diode | Intl. Rect. |
| 66 | CR2 | 1 N936 | Diode | Intl. Rect. |
| 67 | CR3 | 1N4004 | Diode | Motorola |
| 68 | CR4 | RCl00 | Diode | E.D.I. |
| 69 | CR5 | 1N4004 | Diode | Motorola |
| 70 | Q1 | 2N3638 | Transistor | Fairchild |
| 71 | Q2 | 2N3638 | Transistor | Fairchild |
| 72 | Q3 | 2N3242A | Transistor | RCA |
| 73 | Q4 | 2N3440 | Transistor | RCA |
| 74 | Q5 | 2N3242A | Transistor | RCA |
| 75 | Q6 | 2N3053 | Transistor | RCA |
| 76 | Q7 | 2N3053 | Transistor | RCA |
| 77 | Q8 | 2N3053 | Transistor | RCA |
| 78 | Q9 | 2N3053 | Transistor | RCA |
| 79 | Q10 | 2N4074 | Transistor | RCA |
| 80 | Q11 | 2N3053 | Transistor | RCA |

PARTS LIST
DELAY LINE MEMORY - DIGITAL DEVICES, INC.

| ITEM | QUAN | REF DESIG | DESCRIPTION | VENDOR PART NO. |
| :---: | :---: | :---: | :---: | :---: |
| 1 |  |  |  |  |
| 2 |  |  |  |  |
| 3 |  | 5000-105 S | Schematic |  |
| 4 |  |  |  |  |
| 5 |  | 5000-105 L | Layout |  |
| 6 |  |  |  |  |
| 7 |  | 5000-105 | Circuit Board |  |
| 8 |  |  |  |  |
| 9 |  |  |  |  |
| 10 |  |  |  |  |
| 11 |  |  |  |  |
| 12 | 5 | R1, 34, 42 | 1 K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 13 | 1 | R2 | 1.8 K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 14 | 2 | R3, 24 | 1. 2 K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 15 | 1 | R4 | 2.2K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 16 | 2 | R5,19 | 1.5K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 17 | 3 | R6,10,21 | 2.7K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 18 | 3 | R7, 31,33 | 330 Ohms Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 19 | 1 | R8 | 180 Ohms Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 20 | 1 | R9 | 560 Ohms Resistor $\frac{1}{2} \mathrm{~W}$ 5\% |  |
| 21 | 1 | R12 | 8. 2 K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 22 | 3 | R13, 25, 26 | 3.3K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 23 | 2 | R14,17 | 200 Ohms Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 24 | 1 | R15 | 4.7 K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 25 | 2 | R16, 22 | 470 Ohms Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 26 | 3 | Rl8, 23, 28 | 6.8K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 27 | 1 | R27 | 12 K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 28 | 1 | R29 | lOK Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 29 | 1 | R30 | 820 Ohms Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 30 | 1 | R32 | 39 Ohms Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 31 | 1 | R35 | 18K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 32 | 4 | R36, 38, 39, 43, 44,51 | 510 Ohms Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 33 | 1 | R37 | 9.1K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 34 | 3 | R40,45,46 | 27K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 35 | 1 | R41 | 3.3K Resistor $\frac{1}{4} \mathrm{~W} \pm 5 \%$ |  |
| 36 |  |  |  |  |
| 37 |  |  |  |  |
| 38 39 | 4 | R47, 48, 49,50 | lK Resistor $\frac{1}{2} \mathrm{~W} \pm 5 \%$ |  |
| 40 |  |  |  |  |
| 41 |  |  |  |  |
| 42 | 1 | R11 | 5K Potentiometer | Beckman 62 PR 5K |
| 43 | 1 | R20 | 470 Ohms Sensitor TM 1/8 | Texas Inst. |
| 44 |  | C1, C2, C3 | 15uf Cap. 20V | Sprague 150D156x0020B2 |
| 45 | 18 | C4-6,10-16, 24-28 | 2.2uf Capacitor 35V | Sprague 150D225 X9035B2 |
| 46 | 4 | C7,8,9,17 | O.luf Capacitor 35V | Sprague 150D104X9035A2 |
| 47 | 1 | Cl 8 | 150pf Capacitor | Centralab DD-151 |
| 48 | 1 | C19 | 200pf Capacitor | Elmenco DM-15-201J |
| 49 | 2 | C20, 23 | luf Capacitor 35V | Sprague 150D105 X9035A2 |
| 50 51 | 2 | C21, 22 | 47pf Capacitor | Centralab DD-470 |

DELAY LINE MEMORY - DIGITAL DEVICES, INC. (CONT'D.)

| ITEM | QUAN | REF DESIG | DESCRIPTION | VENDOR PART NO. |
| :---: | :---: | :---: | :---: | :---: |
| 52 |  |  |  |  |
| 53 |  |  |  |  |
| 54 |  |  |  |  |
| 55 |  |  |  |  |
| 56 | 1 | CRI | 1 N914 Diode |  |
| 57 |  |  |  |  |
| 58 |  |  |  |  |
| 59 |  |  |  |  |
| 60 | 11 | Q1-6, 8-12 | 2N3646 Transistor |  |
| 61 | 1 | Q7 | 2N979 Transistor |  |
| 62 |  |  |  |  |
| 63 | 12 |  | Transistor Pad | Milton Ross 10194 |
| 64 | AR |  | Wire, Elect. Insul, \#24AWG |  |
| 65 | 1 | Z1 | SN7400N Microcircuit | Texas Inst. |

## PARTS LIST

DELAY LINE MEMORY, LFE

| ITEM | REF DESIG | PART NO. | DESCRIPTION | VENDOR |
| :---: | :---: | :---: | :---: | :---: |
| 1 |  | 2039ACMO1 | Mag Line Assembly |  |
| 2 |  | 2100ACM7 2-1 | Spacer |  |
| 3 |  | 2039ACM21 | P.C. Board Assembly |  |
| 4 |  | 2039ACE | Art Work P.C. Board |  |
| 5 |  | 2039ACE04 | P.C. Board |  |
| 6 | MICRODOT |  | Eyelet |  |
| 7 |  |  | Teflon Tubing Extruded \#18 |  |
| 8 |  |  | Solid Cu Wire Tinned \#22 AWG |  |
| 9 | R1 |  | Res. Carbon 820 Ohms $5 \% \frac{1}{4} \mathrm{~W}$ |  |
| 10 | R2 |  | Res. Carbon 27.0K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 11 | R5 |  | Res. Carbon 56.0K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 12 | R6 |  | Res. Carbon 2.2 K Ohms $5 \% \frac{1}{4} \mathrm{~W}$ |  |
| 13 | R7 |  | Res. Carbon 82 Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 14 | R8 |  | Res. Carbon 3.3K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 15 | R9 |  | Res. Carbon l0.0K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 16 | Rlo |  | Res. Carbon 2.2K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 17 | Rll |  | Res. Carbon 82 Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 18 | R12 |  | Res. Carbon 3.3K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 19 | R13 |  | Res. Carbon l0.0K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 20 | R14 |  | Res. Carbon 2. 2 K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 21 | R15 | 3067P | Res. Variable 100 Ohms (Trimpot) | Bourns |
| 22 | R16 |  | Res. Carbon 82 Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 23 | R17 |  | Res. Carbon 3.3K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 24 | R18 |  | Res. Carbon 100 Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 25 | R19 |  | Res. Carbon 6.8K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 26 | R20 |  | Res. Carbon 100 Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 27 | R21 |  | Res. Carbon lk Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 28 | R22 |  | Res. Carbon 1.5K Ohms |  |
| 29 | R23 |  | Res. Carbon 47 Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 30 | R24 |  | Res. Carbon 47 Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 31 | R25 |  | Res. Carbon 6.8K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 32 | R26 |  | Res. Carbon 12 K Ohms $5 \% \frac{1}{4} \mathrm{~W}$ |  |
| 33 | R27 |  | Res. Carbon 6.8K Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 34 | R28 |  | Res. Carbon l. OK Ohms 5\% $\frac{1}{4} \mathrm{~W}$ |  |
| 35 | C2 | 30 D 805 G 050 BBO | Cap. 8uf 50V | Sprague |
| 36 | C4 |  | Cap. . Oluf 50V (C/D cap) |  |
| 37 | C5 |  | Cap. . 01 uf 50V (C/D cap) |  |
| 38 | C6 | 30D256H050CCO | Cap. 25uf 50V | Sprague: |
| 39 | C7 |  | Cap. . Oluf 50V (C/D cap) |  |
| 40 | C8 | 30D805G050BBO | Cap. 8uf 50V | Sprague |
| 41 | C9 |  | Cap. . Oluf 50V (C/D Cap) |  |
| 42 | Cl0 |  | Cap. . Oluf 50V (C/D Cap) |  |
| 43 | Cll | 30D805G050BB0 | Cap. 8uf 50V | Sprague |
| 44 | C12 | 30D256G050CC0 | Cap. 25uf 50V | Sprague |
| 45 | C13 |  | Cap. . Oluf 50V (C/D Cap) |  |
| 46 | Cl 4 |  | Cap. . Oluf 50V (C/D Cap) |  |
| 47 | Cl5 |  | Cap. . Oluf 50V (C/D Cap) |  |
| 48 | Cl6 |  | Cap. . Oluf 50V (C/D Cap) |  |
| 49 50 | Cl7 | 30D805G050BB0 | Cap. Buf 50V | Sprague |
| 50 | Cl8 |  | Cap. . Ol uf 50V (C/D Cap) |  |

PARTS LIST
DELAY LINE MEMORY, LFE

| ITEM | REF DESIG | PART NO. | DESCRIPTION | VENDOR |
| :---: | :---: | :---: | :---: | :---: |
| 51 | Cl9 |  | Cap. . Oluf 50V (C/D Cap) |  |
| 52 | CR1 | 1N914 | Diode | T.I. |
| 53 | CR2 | 1 N914 | Diode | T.I. |
| 54 | CR3 | $\begin{aligned} & \text { 1N3712/TD712/ } \\ & \text { BD712 } \end{aligned}$ | Diode | G.E. |
| 55 | CR4 | 1N270 | Diode | Transitron |
| 56 | CR5 | 1 N914 | Diode | T.I. |
| 57 | Ll | 934042 | Choke 100 uH | Miller |
| 58 | Q1 | 2N3903 | Transistor | Motorola |
| 59 | Q2 | 2N3903 | Transistor | Motorola |
| 60 | Q3 | 2N3903 | Transistor | Motorola |
| 61 | Q4 | 2N3903 | Transistor | Motorola |
| 62 | Q5 | 2N3903 | Transistor | Motorola |
| 63 | Q6 | 2N3903 | Transistor | Motorola |
| 64 | Q7 | 2N706 | Transistor | G.E. |
| 65 | Q8 | 2N706 | Transistor | G.E. |
| 66 |  |  | Lockwasher Int Tooth St Stl \#2 |  |
| 67 |  |  | Nut Hex St Stl \#2-56 |  |
| 68 |  | 2013ACM22 | Cover | Americ Al. Co: |
| 69 |  |  | Lockmaster Int Tooth St Stl \#2 |  |
| 70 |  |  | Nut Hex St Stl \#2-56 |  |
| 71 |  | 2039ACM | Case Outline |  |
| 73 |  | 2039ACM04 | Acceptance Test Data Sht |  |
| 74 |  | 2039ACM03 | Quality Conformance Test Procedure |  |
| 75 |  | 2039ACM05 | Qualification Test Proc. |  |
| 76 |  | 2039ACE 23 | Schematic |  |





| $\begin{array}{\|l\|} \text { FIG. \& } \\ \text { INDEX } \\ \text { NUMBER } \end{array}$ | DESCRIPTION | DRAWING OR PART NUMBER | RCA STOCK NUMBER | QTY. | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{r} 2 I- \\ -1 \\ -2 \\ -3 \\ -4 \\ -5 \\ -6 \\ -7 \\ -8 \\ -9 \\ -10 \\ -11 \\ -12 \\ -13 \\ -14 \\ -15 \\ -16 \\ -17 \\ -18 \\ -19 \\ -20 \\ -21 \\ -22 \\ -23 \\ -24 \\ -25 \\ -26 \\ -27 \\ -28 \end{array}$ | KEY LEVER HARDWARE AND LEAF SWITCHES <br> . . . COMB, KEY LEVER GUIDE <br> - . . SCREW, GUIDE COMB <br> - . . STOP, KEY LEVER <br> . . . SUPPORT, GUIDE COMB <br> - . SCREW <br> - . . SCREW <br> - . GUIDE, INTERPOSER <br> - . . SCREW, INTERPOSER <br> - . . BRACKET, LEAF SWITCH MTG <br> . . . WASHER, FLAT (NO. 6) <br> - . WASHER, LOCK (NO. 6) <br> . . . SCREW (6-32 x 0.38 LG) <br> . . WASHER, FLAT (NO. 8) <br> - . WASHER, LOCK (NO. 8) <br> . . . SCREW (8-32 x 0.75 LG$)$ <br> - . SWITCH, LEVER 2PDT (S8) <br> - . . SWITCH, LEVER 2PST (S10) <br> . . . SCREW (4-40 x 0.75 LG$)$ <br> . . . SPRING, KEY LEVER, LH <br> - . . COMB, KEY LEVER, LH <br> - . . SPRING, KEY LEVER, RH <br> - . COMB, KEY LEVER, RH <br> - . . GUARD, KEY LEVER <br> - . . SCREW <br> - . . bail, REPEAT <br> - . . BRACKET, SPACE BAR SUPPORT <br> - . . PLATE, KEY LEVER SPRING <br> - . . SCREW, SPRING MTG | IBM1123968 <br> IBM1164576 <br> IBM1133633 <br> IBM1141929 <br> IBM1124411 <br> IBM1141381 <br> IBM116457S <br> 2144152-1 <br> 82278-104 <br> 93620-107 <br> 990386-109 <br> 82278-105 <br> 93620-109 <br> 990388-117 <br> 2187668-2 <br> 2187668-1 <br> 990384-117 <br> IBM1133654 <br> IBM1133683 <br> IBM1133647 <br> IBM1133682 <br> IBM1141226 <br> IBM1164863 <br> IBM1164467 <br> IBM150735 <br> IBM1133679 <br> IBM1164579 | $\begin{aligned} & 115352 \\ & 301297 \\ & 301296 \end{aligned}$ | $\begin{aligned} & 2 \\ & 1 \\ & 1 \\ & 2 \\ & 2 \\ & 1 \\ & 4 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 2 \\ & 2 \\ & 2 \\ & 2 \\ & 1 \\ & 1 \\ & 4 \\ & 1 \end{aligned}$ |  |


[^0]:    $\cdot 1$ = INTERIM REVISION
    F = FORMAL REVISION
    R = REISSUE

[^1]:    -1 = INTERIM REVISION
    $F=$ FORMAL REVISION
    $R=$ REISSUE

[^2]:    -1 = INTERIM REVISION
    F = FORMAL REVISION
    R = REISSUE

[^3]:    -1 = INTERIM REVISION
    $F=$ FORMAL REVISION
    $R=$ REISSUE

[^4]:    * $1=$ INTERIM REVISION UR = UNIVAC REVISION $F=$ FORMAL REVISION
    $R=$ REISSUE

[^5]:    $1=$ INTERIM REVISION UR = UNIVAC REVISION
    $F=$ FORMAL REVISION
    R = REISSUE

[^6]:    * At this print the Keyboard is ready for next key selention by reiator.

[^7]:    70/752-D211

