IIST Seminar

Magnetic Recording Channels

with

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and

Dr. Nersi Nazari, GEC Plessey

Institute for Information Storage Technology
Santa Clara University
May 28, 1996

MAGNETIC RECORDING CHANNELS
an IIST Course

Magnetic Recording Channel Front-Ends

Klaas B. Klaassen, Ph.D.
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and

Digital Read/Write Channels for Magnetic Recording

Nersi Nazari, Ph.D.
GEC Plessey

May 28, 1996
Santa Clara University

Magnetic Recording Channel Front-Ends

Considerations and Design

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KbeeK96

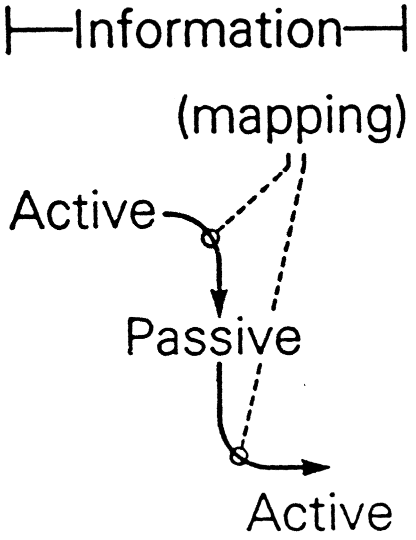
Contents

INFORMATION THEORETICAL CONCEPTS

Recording Channel ⇛ **Information Channel**

⋆ CHANNEL: Physical means for transmitting or storing information.

INFORMATION needs a PHYSICAL CARRIER



- <u>Active Information:</u>

  Grafted onto energetic carrier (power)

- <u>Passive Information:</u>

  Non-energetic carrier (ordered state of matter)

ACTIVE INFORMATION ≡ SIGNAL

PASSIVE INFORMATION ≡ PATTERN

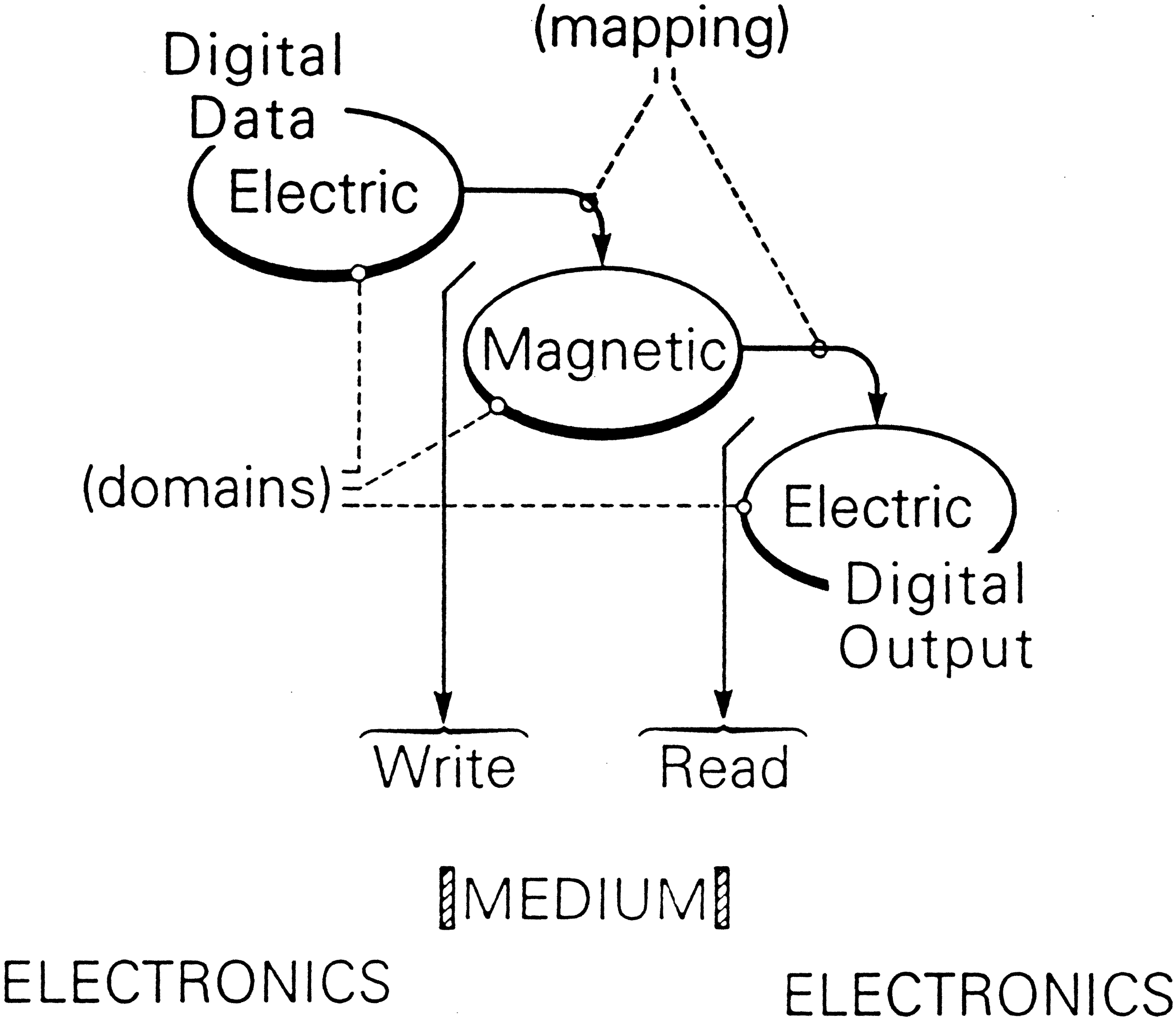
UTILIZATION

Active Information

- Easily transmitted
  (as electromagnetic power)
- Dissipates away
  (eventually drowns in thermal noise)
- Ideal for communication between systems

Passive Information

- Not readily transmitted
  (shipping of matter)
- Little long-term decay
- Ideal for information storage



(mapping)
Digital Data
Electric
Magnetic
(domains)
Electric
Digital Output
Write
Read
MEDIUM
ELECTRONICS
ELECTRONICS

Physical Channel

Active Information is contained in:

☐ **Signals**

- Energetic physical carriers of desired information
- Waveforms we want to see

These are always accompanied by:

☐ ***Noise*** (Internal, fundamental)

- Unpredictable, random perturbations
- Generated in channel hardware
- Theoretically inescapable
- Thermal noise, shot noise, etc.

☐ ***Interference***

- Undesirable garbage signals
- Avoidable
- Environment generated
- Electromagnetic interference, cross-talk, etc.

☐ ***Distortion***

- (trace) average of difference between waveforms we get and those we want
- Linear distortion: channel frequency response not adequate
- Non-linear distortion: channel dynamic range not adequate

Basic Contributors

☐ Magnetic Medium

- Transition
- DC-erase
- Track edge

Noise

- Overwrite
- Adjacent track
- Texture

Interference

Intersymbol *Distortion*

☐ Head

- Coil/sensor resistance
- Eddy current damping
- Barkhausen

Noise

- Tribo-electric
- Thermal asperity
- Conductive contact

Interference

MR head asymmetry *Distortion*

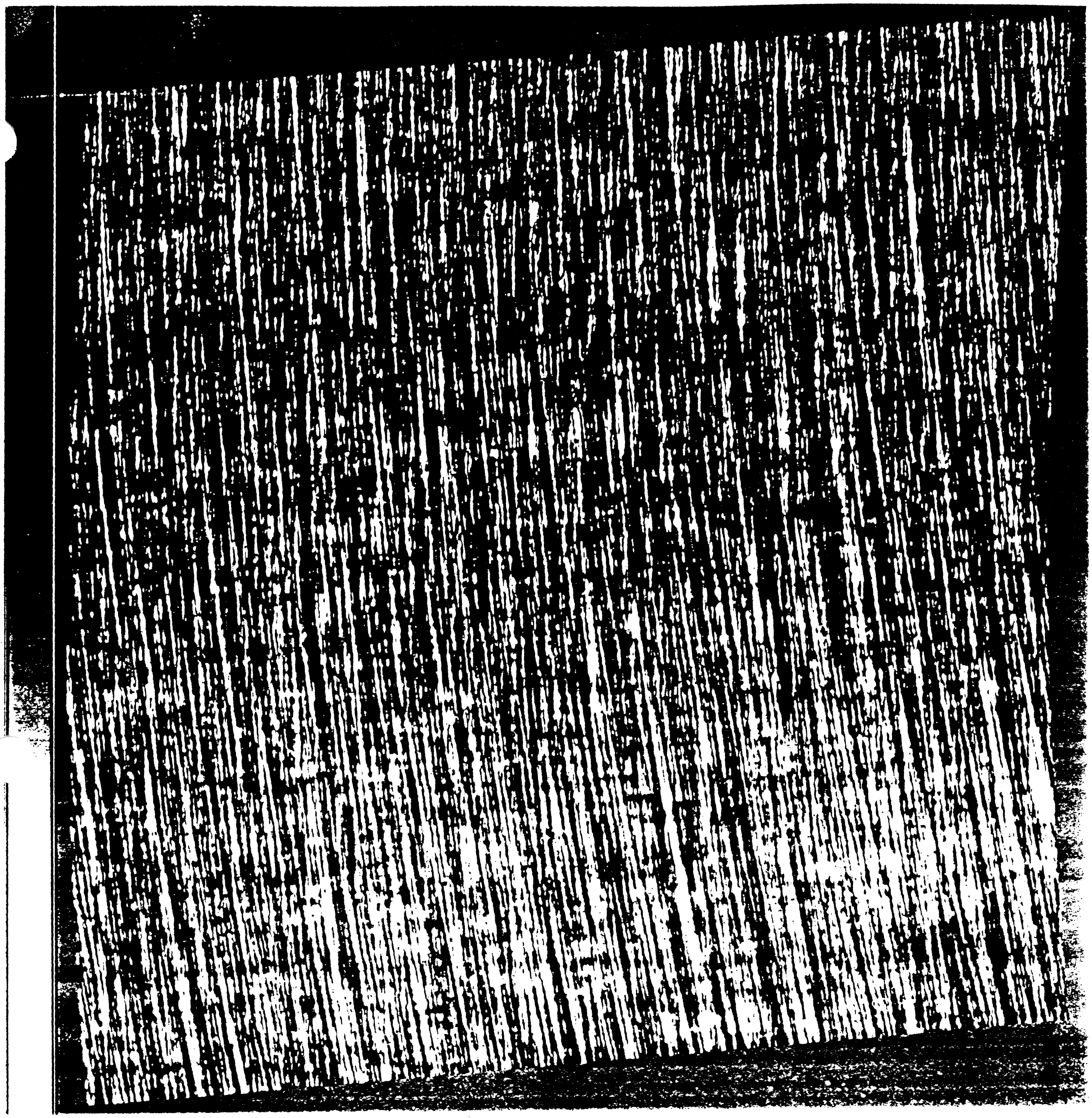
☐ Electronics

- Thermal
- Shot

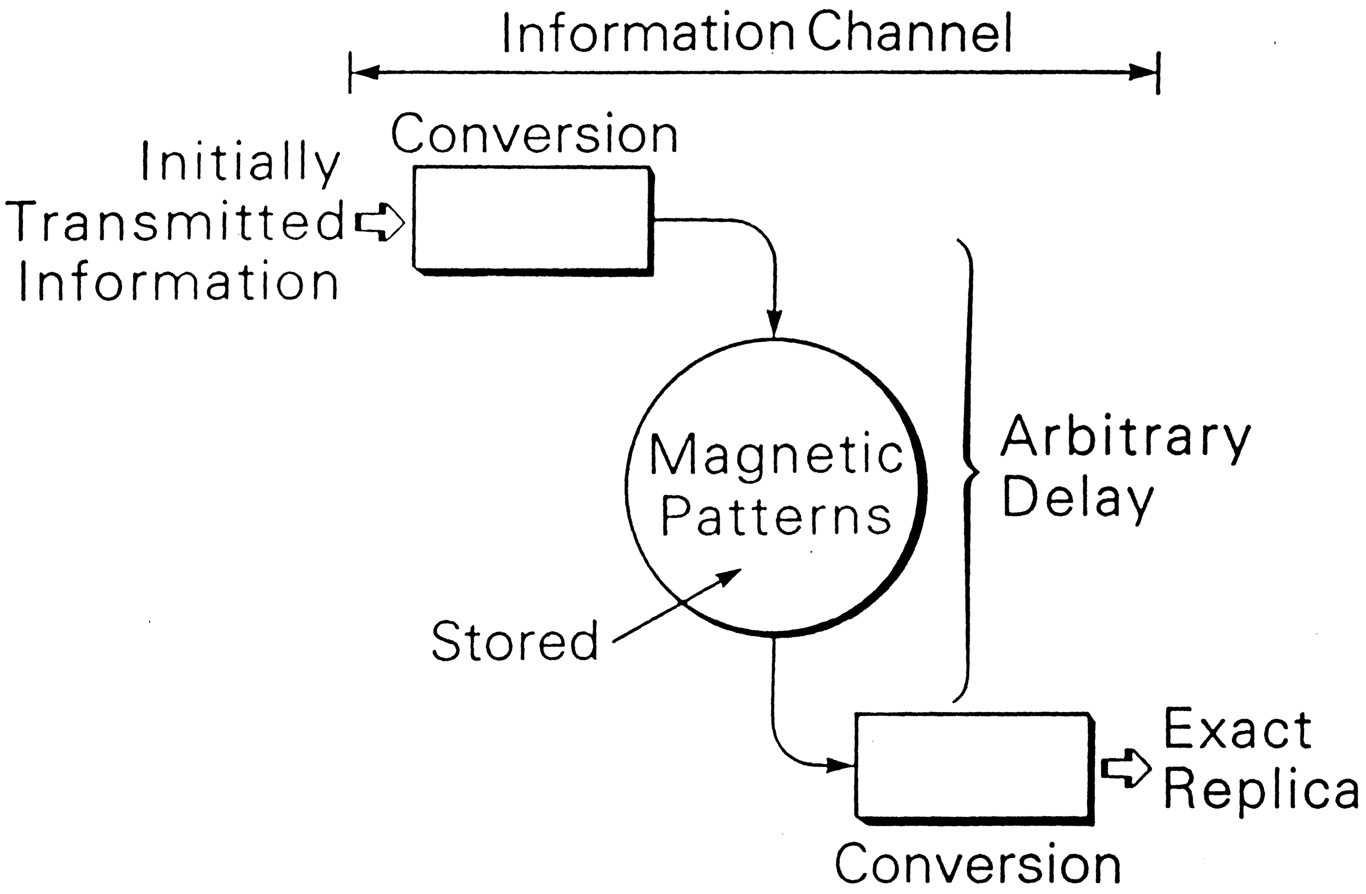
Noise

Electro-magnetic *Interference*

TA dynamics *Distortion*



MR signal resolved texture map.


Information Channel
Conversion
Initially Transmitted Information
Magnetic Patterns
Stored
Arbitrary Delay
Exact Replica
Conversion

WHY ENCODING-PROCESSING ?

At write-read process (mapping) we lose some information

This is due to:

- Noise Contamination
- Interference Injection
- Signal Distortion
  - linear
  - non-linear

This can be counteracted by:

- Encoding
- Signal Processing

Channel Front-End

☐ Definition

The components ahead of the channel data module form the ***channel front-end***

☐ Front-End Components

- — Read/Write transducer
- — Transducer-electronics interconnect
- — Flex cable (input)
- — Electronics module
- — Flex cable (output)
- — Disk enclosure connector
- — Traces on drive electronics card

☐ Two Signal Paths

The front-end comprises two data signal paths:

- ★ Read path
- ★ Write path

Front-End is a System

☐ The components of a front-end form a ***system***

☐ The mutual matching of these components becomes important for ***high data rates***

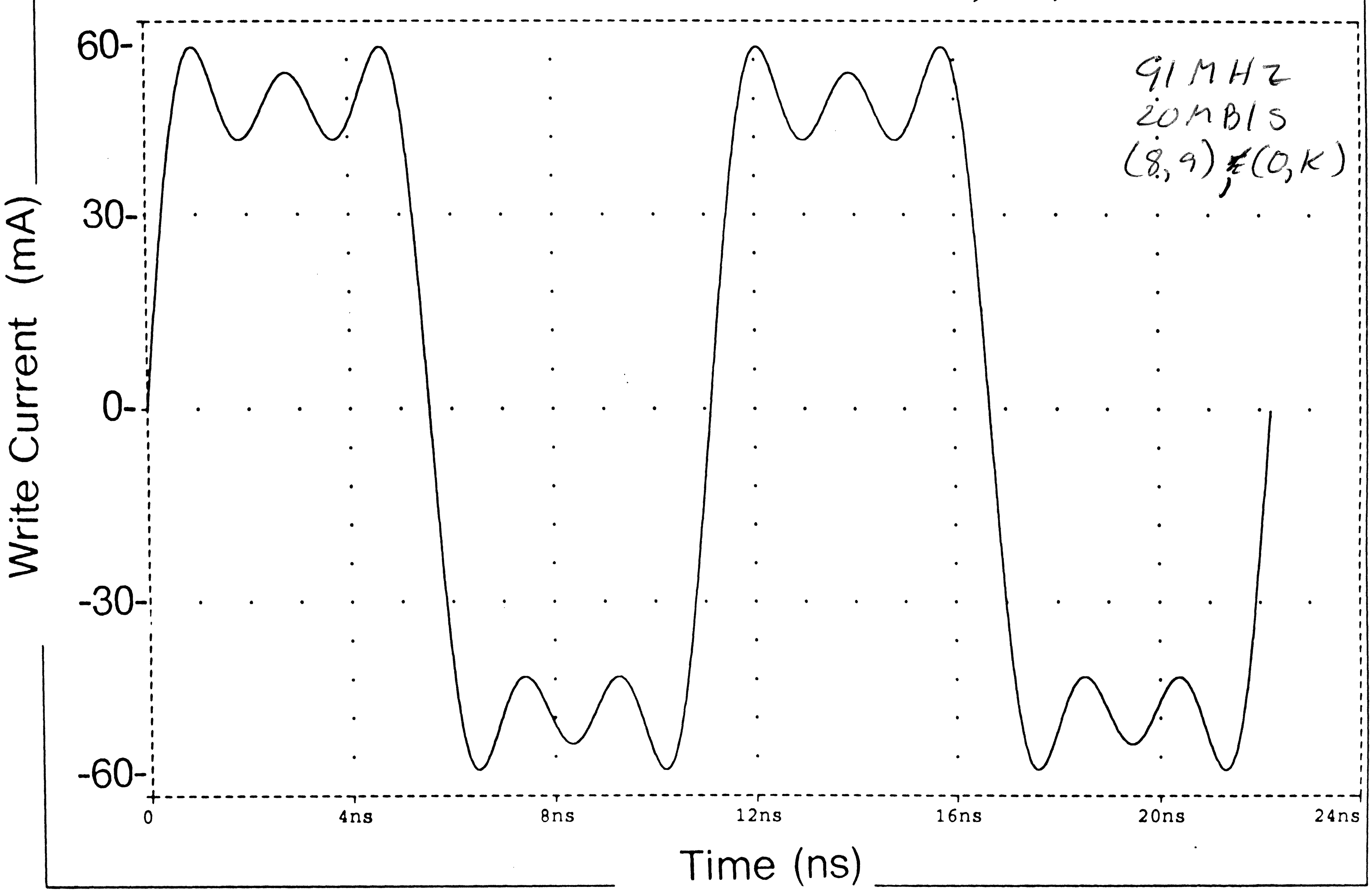
☐ This system approach is needed because the physical dimensions and the signal frequency content in the front-end necessitates the design of a component in the context of its ***environment***

☐ A good understanding of ***Recording Physics*** is important to arrive at the design specifications of the front-end components

including 1st, 3rd, 5th harmonics
Date/Time run: 02/23/95 13:05:25

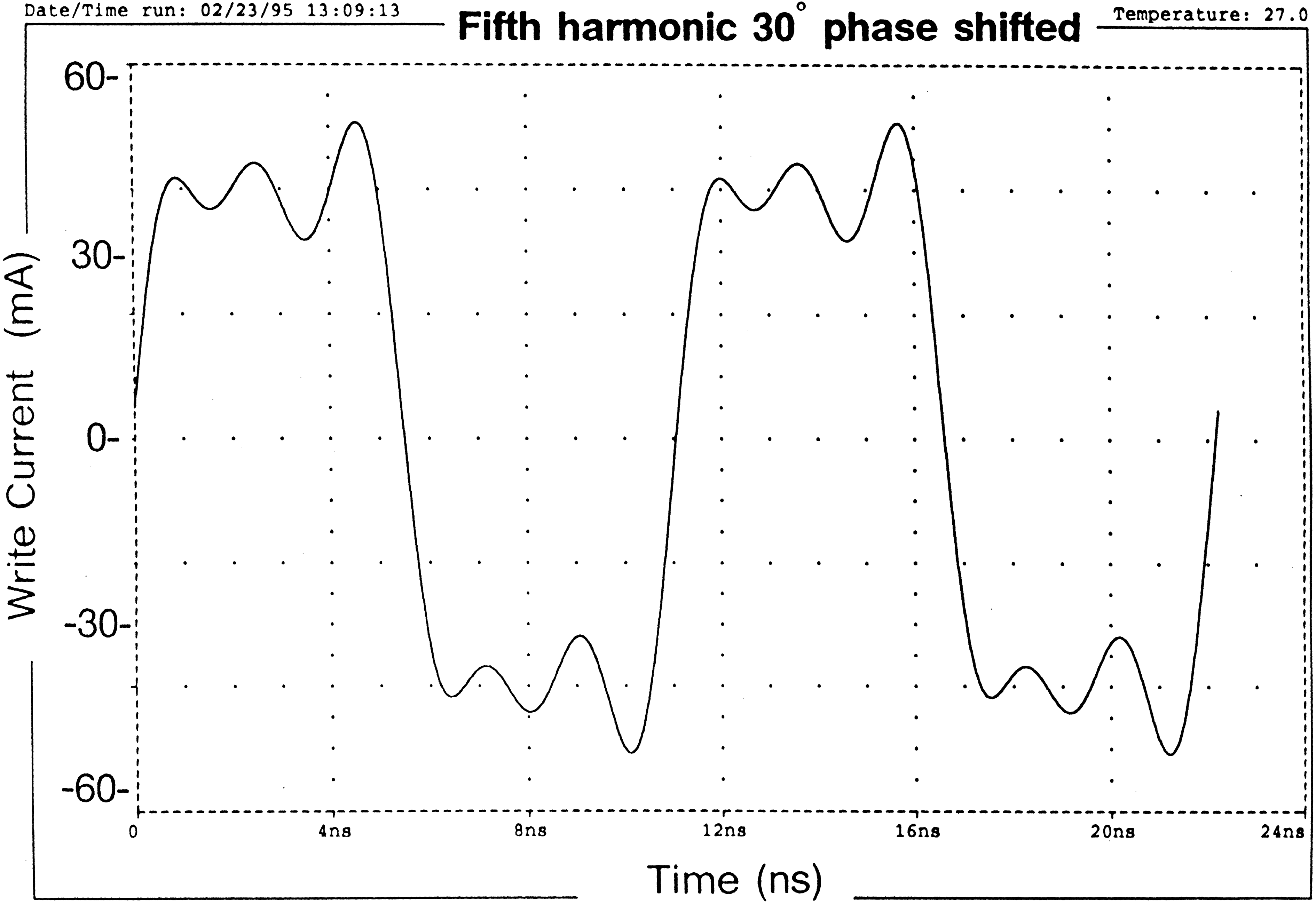
First three harmonics: 1st, 3rd, 5th

Temperature: 27.0



91 MHz
20MB/S
(8,9)~~≠~~,(0,K)

30 deg phase shift in 5th harmonic
Date/Time run: 02/23/95 13:09:13



=> write needs much more BW than read channel.

Electronics Role in Information Conversion

- Signal Conditioning
  (Gain, filtering, TA suppression...)

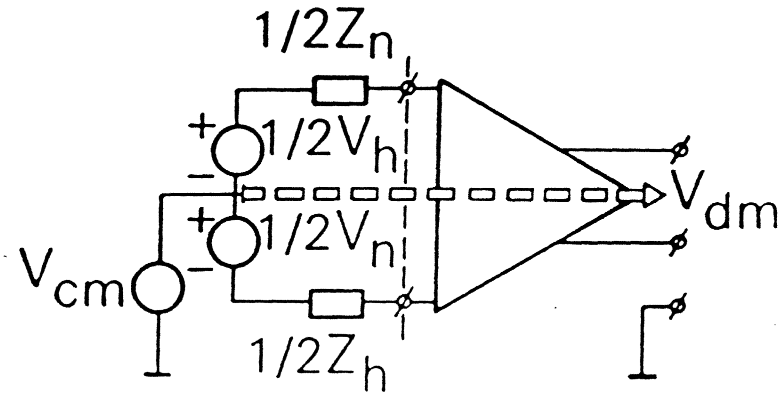
thermal asperity

- Transducer-Electronics Interface
  (Impedance, biasing...)
- Interference Rejection
  (CMRR, PSRR...)

Interference Rejection

☐ *Input Interference Pick-up*

- Capacitively coupled into head
- Couples equally into both head leads
- "Common-mode" type of interference voltage V_{cm}
- Head signal is "differential-mode" type signal voltage V_h



Single-Ended Input Amplifier

(No CM interference rejection)

Differential Input Amplifier

(Rejects CM interference)

Measure of amount of rejection:

$$\textit{Common-Mode Rejection Ratio}\ \frac{V_{cm}}{V_h}\Big|_{\text{same } V_{dm}}$$

$$A_{dm} = \frac{V_{dm}}{V_h}$$

$$CMRR = \frac{A_{dm}}{A_{cm}}$$

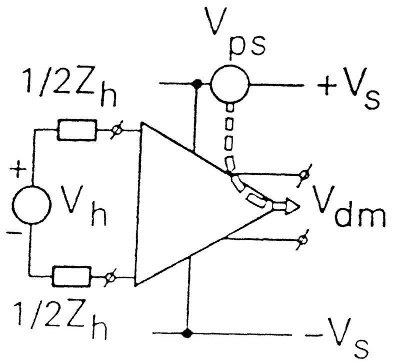
$$A_{cm} = \frac{V_{dm}}{V_{cm}}$$

Interference Rejection

- Cause: Any left/right input impedance imbalance causes CMRR to be finite (> 60 dB) ~1k rejection
- Parasitic capacitances cause high-frequency CMRR roll-off of 6 dB/oct Goes to pot @ high freq's.

□ ***Power Supply Interference***

- Feedthrough of power supply interference to signal output
- Decouple power supply lines at side of module



Measure of amount of rejection:

$$\textit{Power Supply Suppression}\ \frac{V_{ps}}{V_{dm}} = \frac{1}{A_{ps}}$$

Most often "referred to input" (similar to CMRR)

$$\textit{Power Supply Rejection Ratio}\ \frac{V_{ps}}{V_h}\Big|_{\text{same } V_{dm}}$$

$$A_{dm} = \frac{V_{dm}}{V_h}$$

$$PSRR = \frac{A_{dm}}{A_{ps}}$$

$$A_{ps} = \frac{V_{dm}}{V_{ps}}$$

Interference Rejection

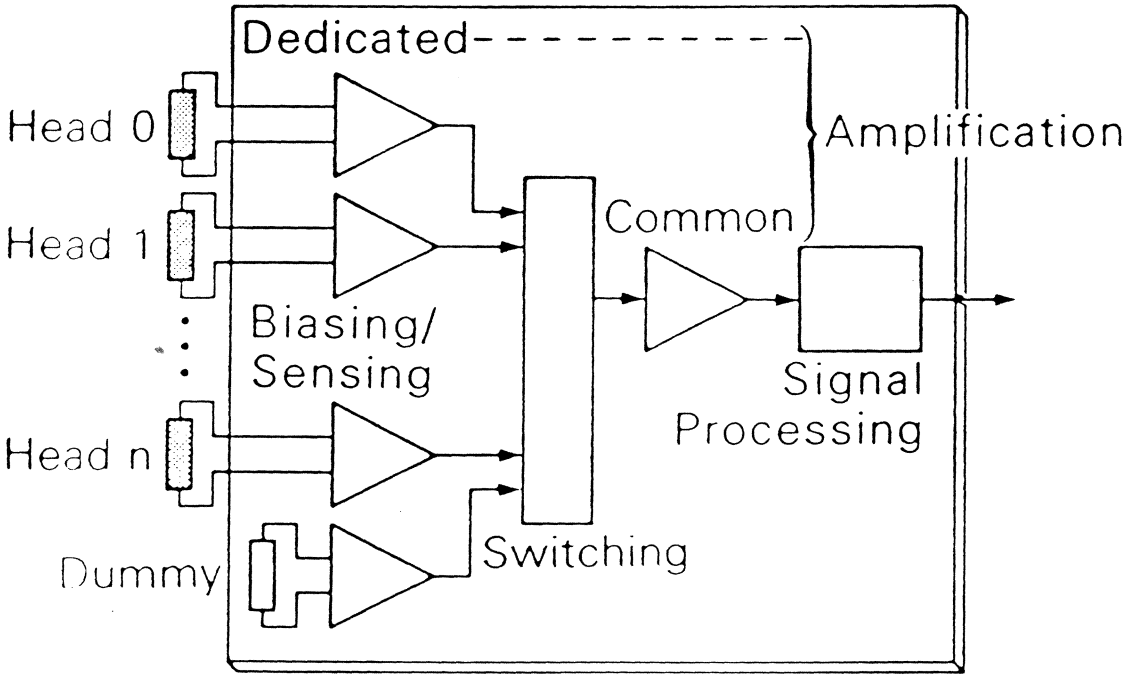
- Cause: Finite impedance of (vertical) amplifier branches connected between the two supply lines. Supply voltage affects branch current and feeds through into signal output. single ended
- PSRR is usually worse in SE amplifiers
- High frequency roll-off 6dB/oct

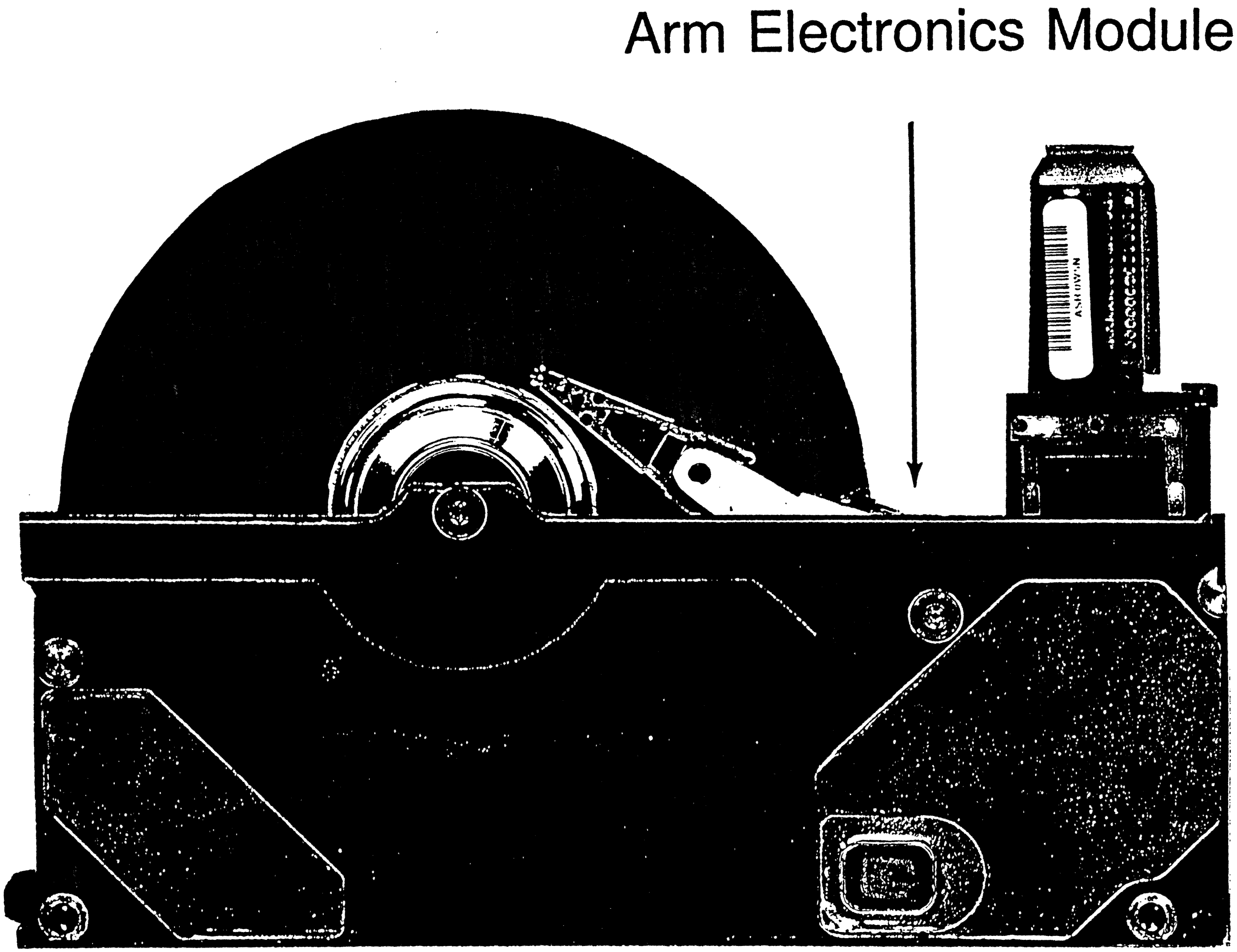
Front-End Electronics

Nomenclature:

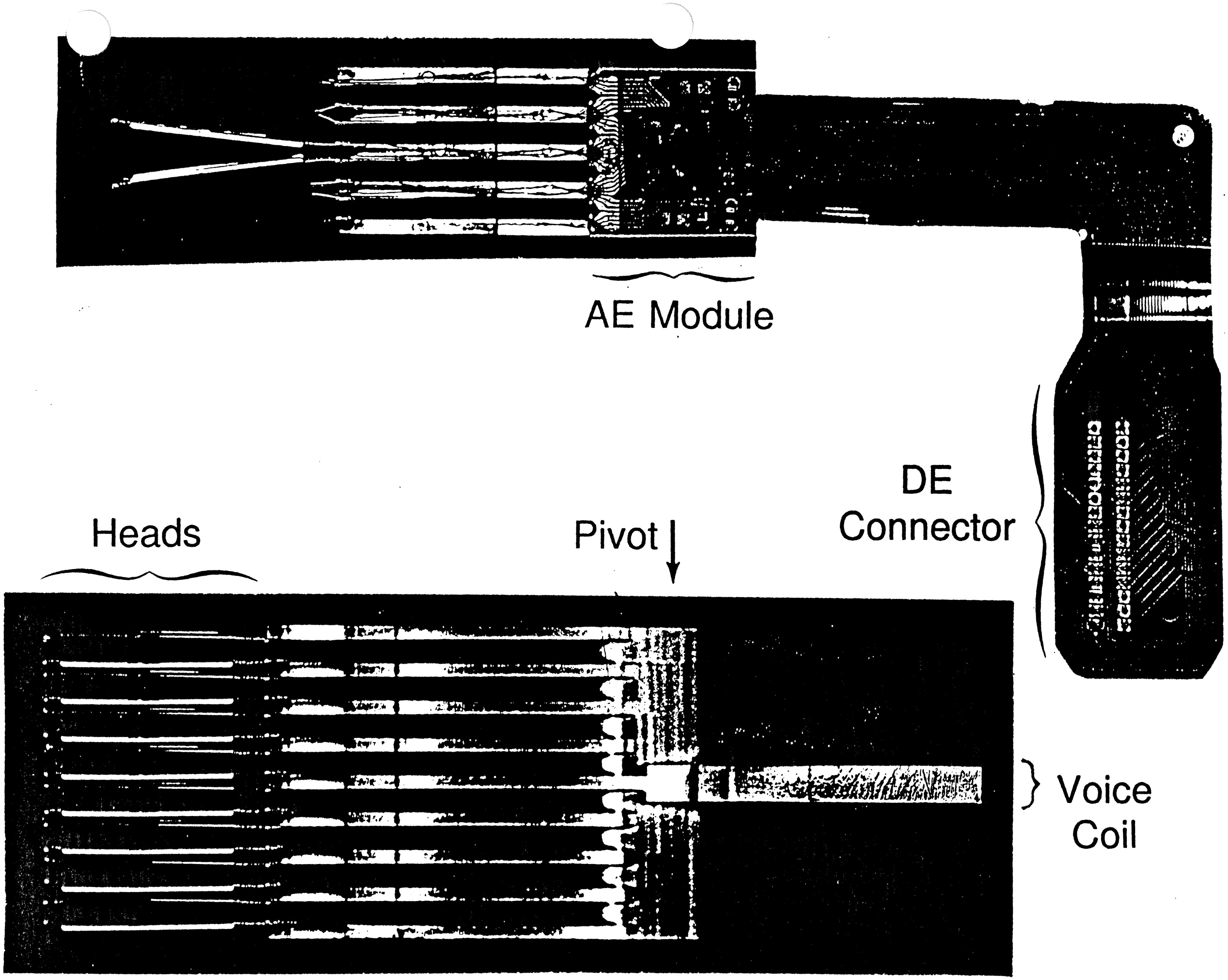
- Pre-amplifier
- Head electronics
- Arm electronics

Port-Dedicated ***Port-Common***



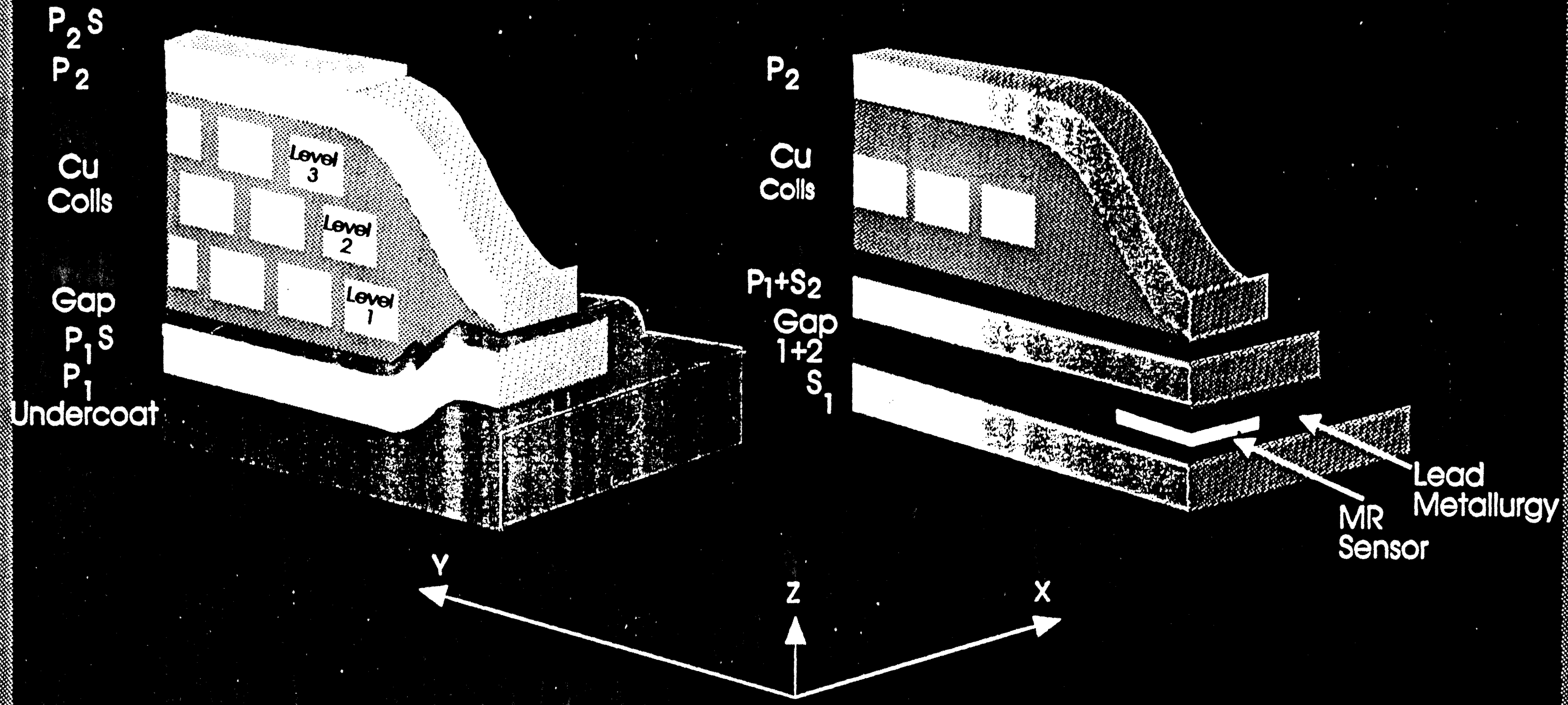


Hard Disk Drive Assembly



2 elec. modules for high stack.

Magnetic Head Design



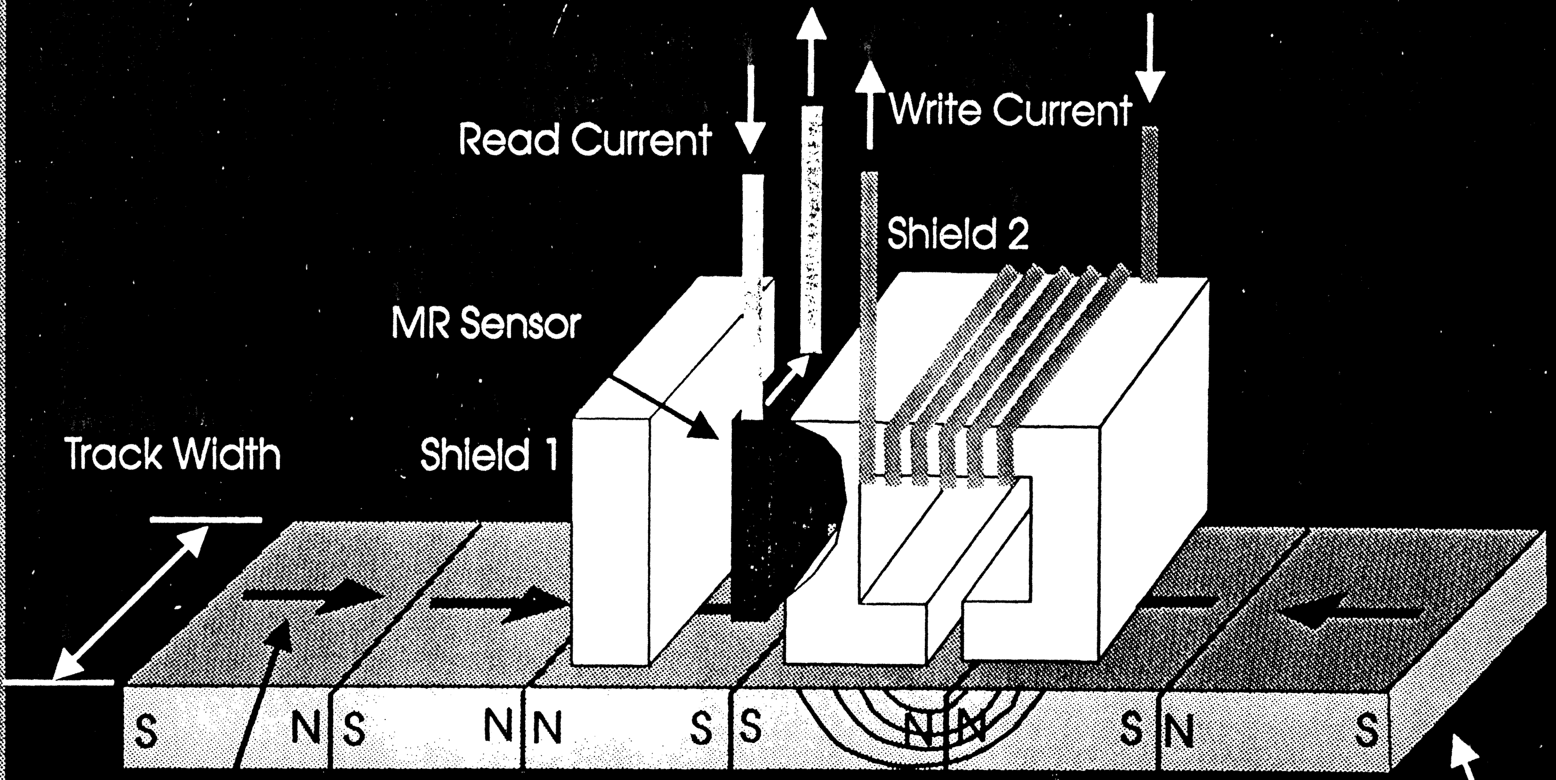
Thin Film Inductive Head Design

Merged MR Head Design

IBM

Ed Grochowski

Magnetic Recording Process



Read Current

Write Current

Shield 2

MR Sensor

Track Width

Shield 1

Magnetoresistive
Read Element

Inductive
Write Element

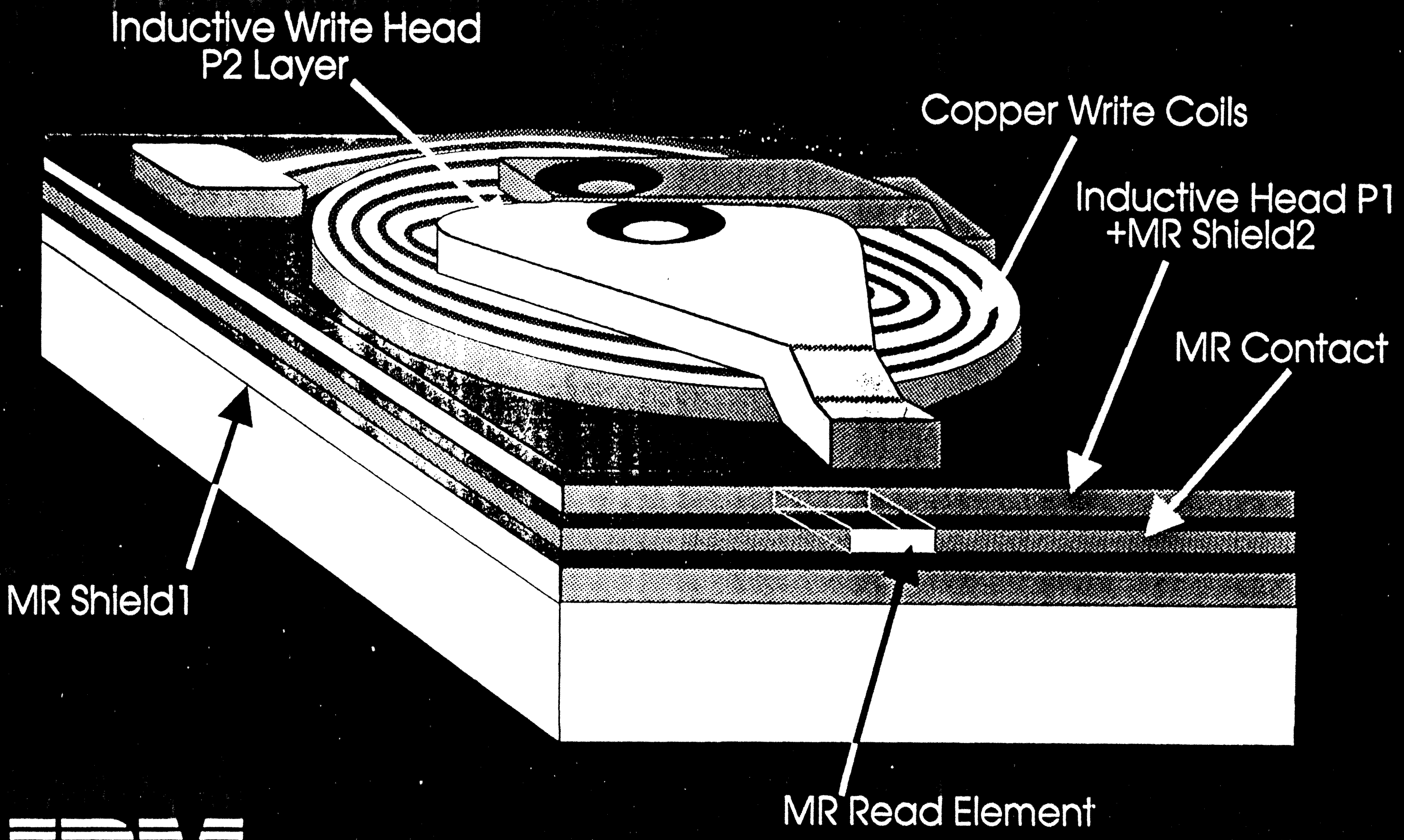
Magnetization

Recording medium

IBM

Ed Grochowski

Merged Magnetoresistive Head



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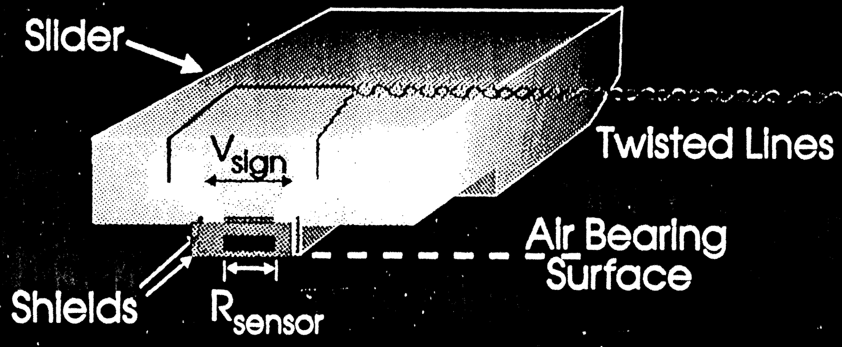
AC coupled amp.

MR Head Basics

$V_{sign} = I_{bias} \times \Delta R_{sensor}$



Slider

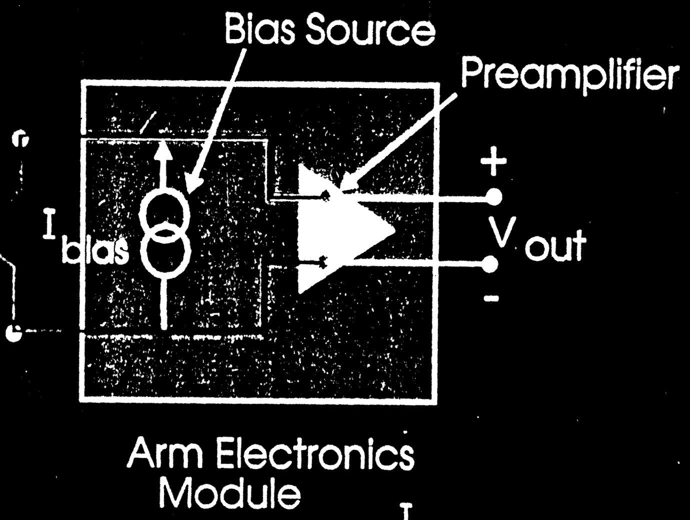
V_{sign}

Twisted Lines

Air Bearing Surface

Shields

R_{sensor}



Bias Source

Preamplifier

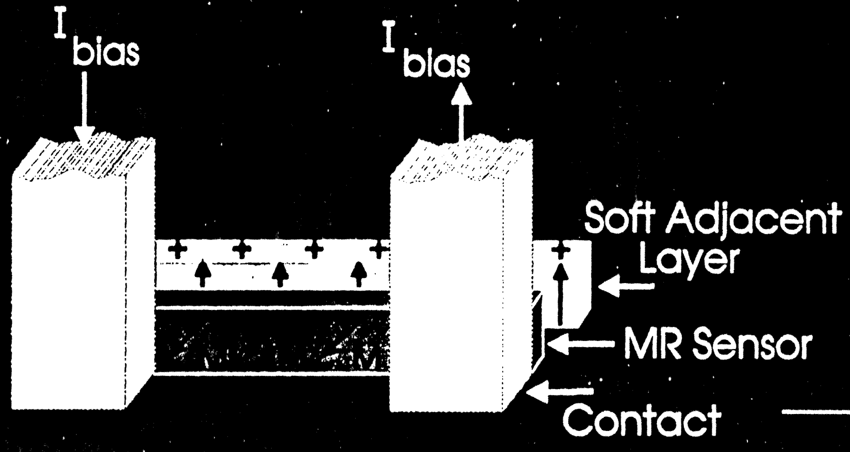
I_{bias}

+

V_{out}

-

Arm Electronics Module



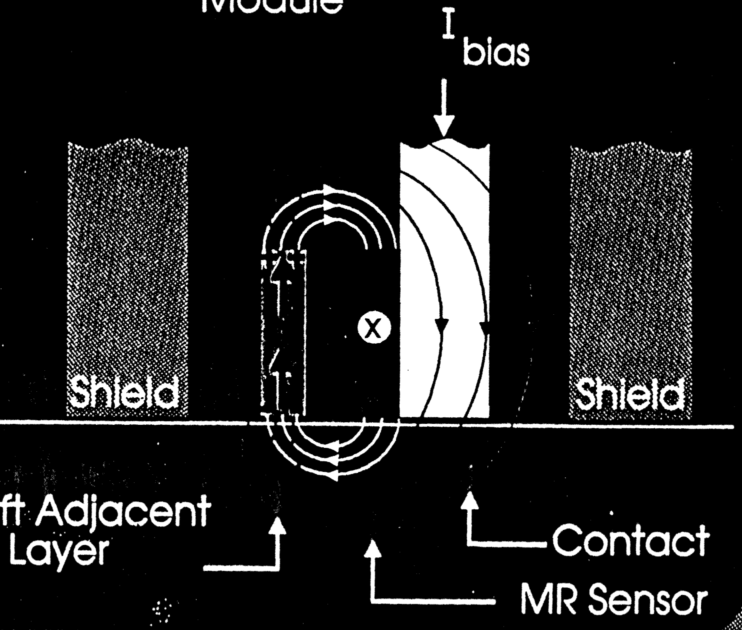
I_{bias}

I_{bias}

Soft Adjacent Layer

MR Sensor

Contact



I_{bias}

Shield

Shield

Soft Adjacent Layer

Contact

MR Sensor

IBM

Ed Grochowski/Klaas Klaassen

SAL biased so like hard magnet $\mu_r = 1$

Noise/Bandwidth Comparison

Comparing an

- Inductive read head
- MR read head

read-out by the same voltage sensing (high input impedance) pre-amplifier, shows that the

- ***Number of turns n***
- ***(Inverse of) the sensor height h***

have equivalent roles in the

- Signal amplitude
- Bandwidth
- Signal-to-noise ratio

Inductor is limit of useful BW.

Noise and Bandwidth

Comparison (Inductive Read Head / MR Read Head

- <u>Inductive Read Head</u>
- <u>MR Read Head</u>

Read out by same voltage sensing preamp.

- Input referred noise voltage V_{an}
- Input capacitance C_t

★ Scale inductive head: turns ratio η

single turn resistance

$$R_h = \eta R_o\,,\ L_h = \eta^2 L_o\,,\ V_h = \eta V_o$$

★ Scale MR head: inverse sensor height ratio η'

$$R_{mr} = \eta' R'_o\,,\ V_{mr} = \eta' V'_o$$

Noise, Bandwidth Cont.

- <u>Inductive Head</u>
  Input circuit bandwidth of *critically damped* head:

$$f_{-3dB} = \frac{1}{2\pi\underbrace{\sqrt{\eta^2 L_o C_t}}_{\tau}} = \frac{1}{2\pi\eta\sqrt{L_o C_t}}$$

(Spot) Signal-to-Noise Ratio ($\Delta f = 1$ Hz)

$$SNR = \frac{V_h^2}{\underbrace{4kTR_h}_{\text{thermal}} + \underbrace{V_{an}^2}_{\text{amp}}}$$

$$SNR = \frac{\eta^2 V_0^2}{4kT\eta R_0 + V_{an}^2}$$

Noise, Bandwidth Cont.

- MR Head

  Input circuit bandwidth:

$$f_{-3dB} = \frac{1}{2\pi \underbrace{R_{mr}C_t}_{\tau}} = \frac{1}{2\pi\eta' R'_o C_t}$$

Spot SNR: $\Delta f = 1\,\mathrm{Hz}$ window

$$SNR = \frac{V_{mr}^2}{4kTR_{mr} + V_{an}^2}$$

all extraneous noise sources e.g. leads.

$$SNR = \frac{\eta'^2 V'^2_o}{4kT\eta' R'_o + V_{an}^2}$$

Noise, Bandwidth Cont.

Hence, the inductive and the MR head have the same scaling factor dependence

Signal: $V = \eta V_o$

Bandwidth: $f_{-3dB} = \dfrac{1}{2\pi\eta\tau_o}$

S/N Ratio $SNR = \dfrac{\eta^2 V_o^2}{4kT\eta R_o + V_{an}^2}$

The role of number of turns n in an inductive head is equivalent to the role of (the inverse of) the sensor height h in an MR head

Some Recording Physics

☐ *Single-Element Inductive Read/Write Heads*

- ***Advantages***
  - Self-generating (need no bias)
  - Simple servoing (single element) (symmetrical track profile)
  - Linear reader
  - Robust (in view of ESD and corrosion)
  - No thermal asperities (when flying low)

- ***Disadvantages***
  - High velocities only (Faraday, $d\Phi/dt$ sensitive)
  - Large N (narrow trackwidths)
  - High inductance (high speed writing requires large electronics supply voltage, dissipation)
  - Limited bandwidth (coil-electronics resonance)

- ***Probably not extendable beyond (12.5 MB/s, 5 μm tracks)***

Inductive Heads

Single-element read/write transducer

- *Scale head turns N*

$V_h = NV_o$

$R_h = NR_o$ Leads: $L = L_l$

$L_h = N^2L_o$

$C_h = NC_o$ Extra, parallel port:

$I_W = MMF/N$ $C = C_e$

- Critically damped head band-end:

$$\omega_o = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{N^3L_oC_o}}$$

- Degrades quickly for increasing *N*
  (needed for decreasing trackwidths)
- Extra burdened by parallel port (C_e)

For higher data rates/narrower tracks an MR head is unavoidable

Some Recording Physics (Cont)

☐ *MR Read/Inductive Write Heads*

Positioning of the two elements:

Side-by-side, piggy back, ***merged***, integrated

- ***Advantages***
  - Large signal/unit trackwidth
  - Velocity independent (flux-sensing)
  - Very large bandwidths possible
  - Separately optimized read and write heads
    - Low *N* write head
    - Write-wide, read-narrow
  - Isolated pulse shape with no undershoot
- ***Disadvantages***
  - Active read element exposed at ABS
    - Thermal asperities
    - Electro-erosion
    - Corrosion
    - Smearing

Smears is
pop corn type
noise.

Some Recording Physics (Cont)

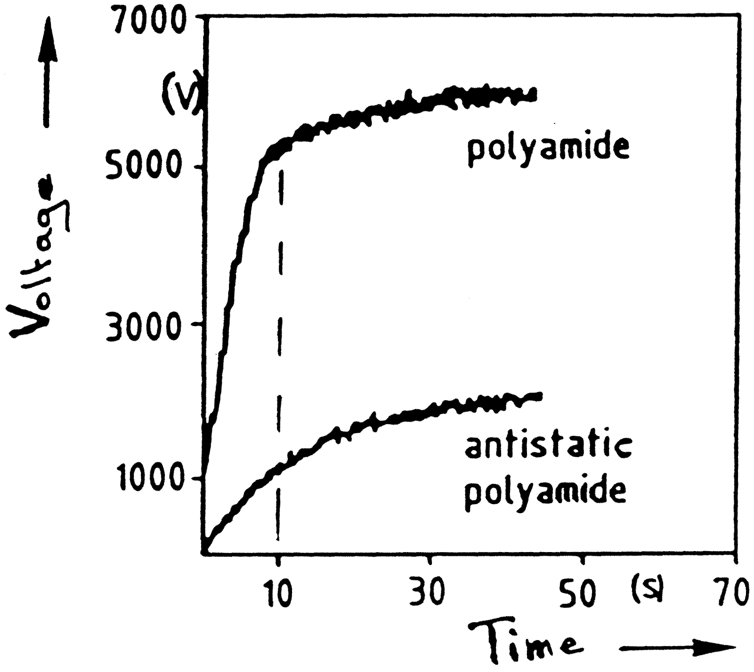
- ESD sensitive

/ electron streams moves atoms in sensor (current density & temp driven)

- Electromigration (sensor temp., current density)
- Interdiffusion (sensor temp.)
- Non-linear read sensor (amplitude asymmetry)
- Needs shields for high resolution
- Asymmetrical track profile
- Write-to-read offset (skewed slider, micro jog)
- Complexity (e.g. lapping)

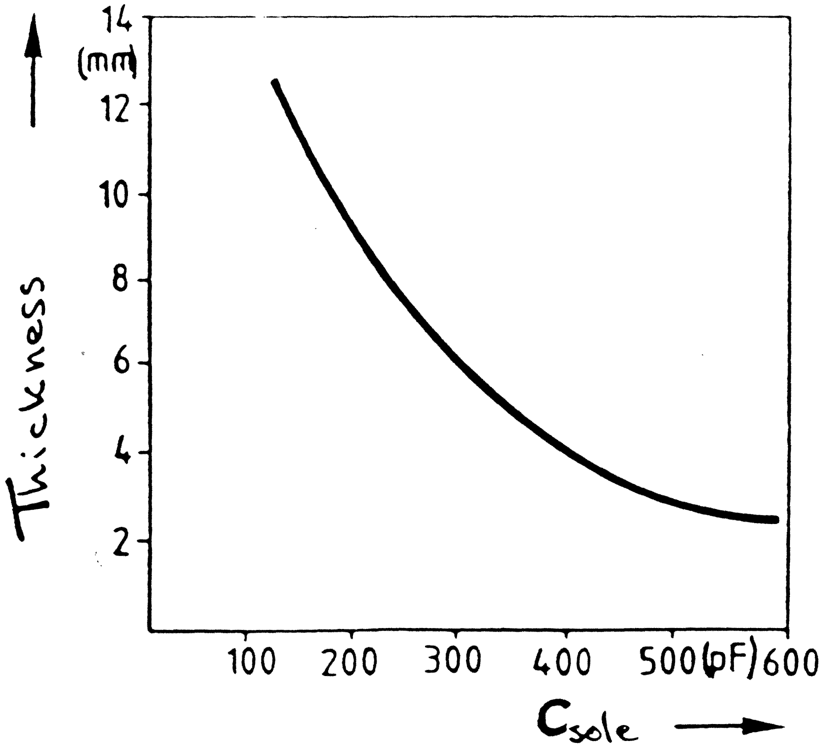
ESD Discharge

Charge Build-Up



e.g. carpet

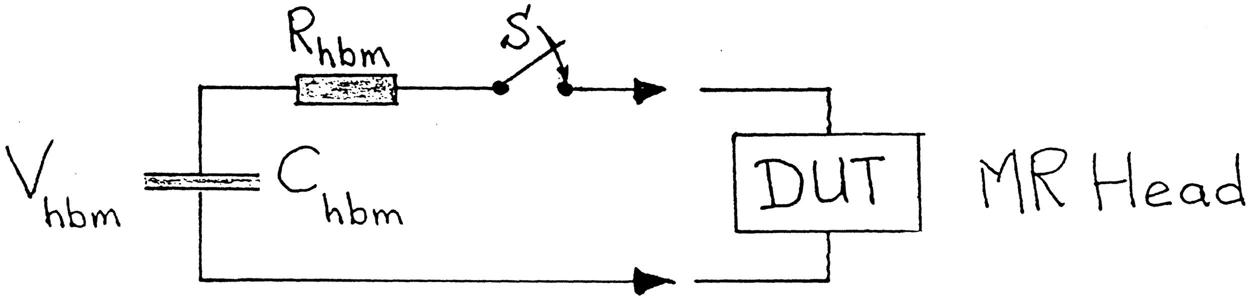
Shoe Sole Capacitance



Electro-Static Discharge (ESD)

- MR sensor failure due to ***electical overstress*** caused by accidental electrostatic discharge (tools, people)

- Simulated by ***Human Body Model***



loose metallic
object greatly
reduces series
R & very high
currents

$$C_{hbm} = 100\text{pF}, \quad R_{hbm} = 1.5\text{k}\Omega \quad (\tau_{hbm} = 150\text{ ns})$$

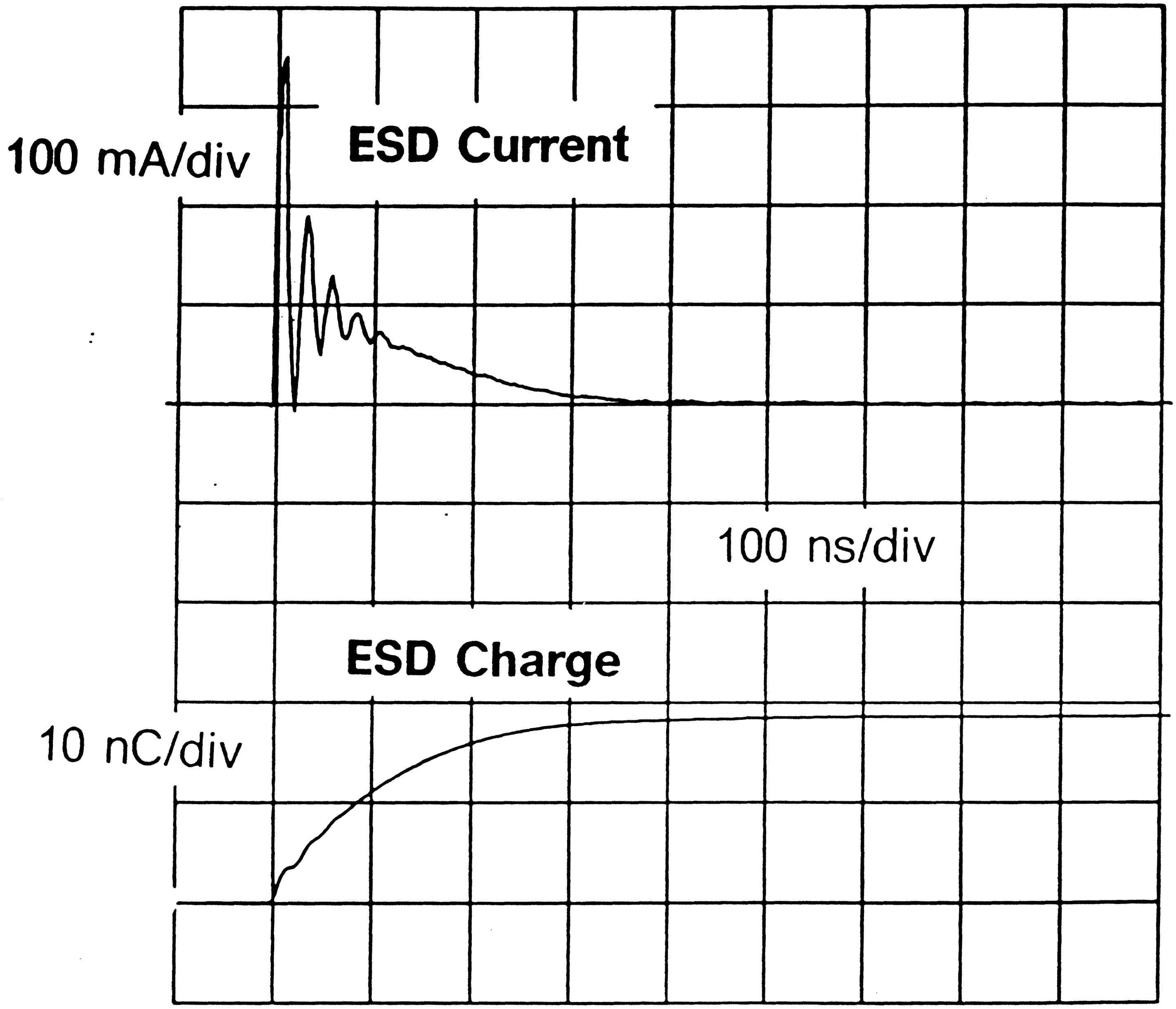
- ***Energy release*** into MR head

$$E_{MR} = R_{MR} I_o^2 \frac{\tau_{hbm}}{2} \qquad (R_{MR} \ll R_{hbm})$$

$$I_o = V_{hbm}/R_{hbm}$$

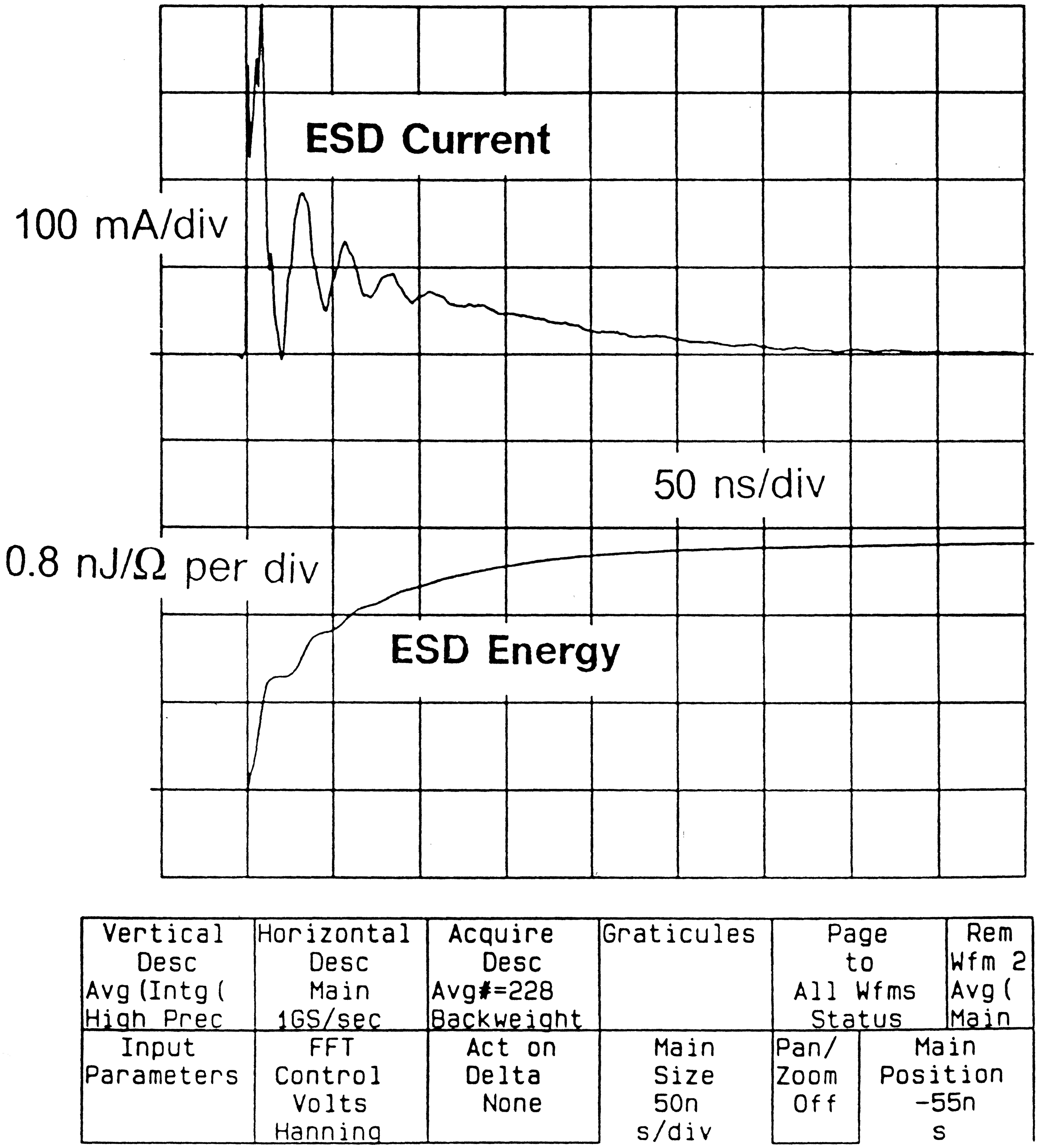
$$E_{MR} = \frac{R_{MR}}{R_{hbm}} E_{hbm}, \qquad E_{hbm} = \frac{1}{2} C_{hbm} V_{hbm}^2$$

ESD Discharge



Vertical Desc Avg(Intg(High Prec	Horizontal Desc Main 500MS/sec	Acquire Desc Avg#=172 Backweight	Graticules	Page to All Wfms Status	Rem Wfm 2 Avg(Main
Input Parameters	FFT Control Volts Hanning	Act on Delta None	Main Size 100n s/div	Pan/ Zoom Off	Main Position -110n s

ESD Discharge



Vertical Desc Avg (Intg (High Prec	Horizontal Desc Main 1GS/sec	Acquire Desc Avg#=228 Backweight	Graticules	Page to All Wfms Status	Rem Wfm 2 Avg (Main
Input Parameters	FFT Control Volts Hanning	Act on Delta None	Main Size 50n s/div	Pan/ Zoom Off	Main Position -55n s

- almost adiabatic damage

Electro-Static Discharge (ESD)

- ***Lethal sensor MR peak voltage***

  Heat flow study:

  $$V_{p,MR} = K_1 R_{MR} + K_2 TW$$

  $K_1 \simeq 33mA, \qquad K_2 \simeq 1.7 \times 10^5\ V/m$

- ***Typical values***

  For $R_{MR} = 30\ \Omega$ head, track width $TW = 7.5\ \mu$m, we expect:

  $V_{p,MR} = 2.28\ V \qquad V_{hbm} = 114\ V$

  $I_{p,MR} = 74.5\ mA \qquad Q_{MR} = 11\ nC$

  $E_{MR} = 13\ nJ \qquad E_{hbm} = 650\ nJ$

- ***Counter Measures***

  ESD protection devices across electronics port similar to those in place to protect the module from ESD damage

CMOS circuits - compatible requirements

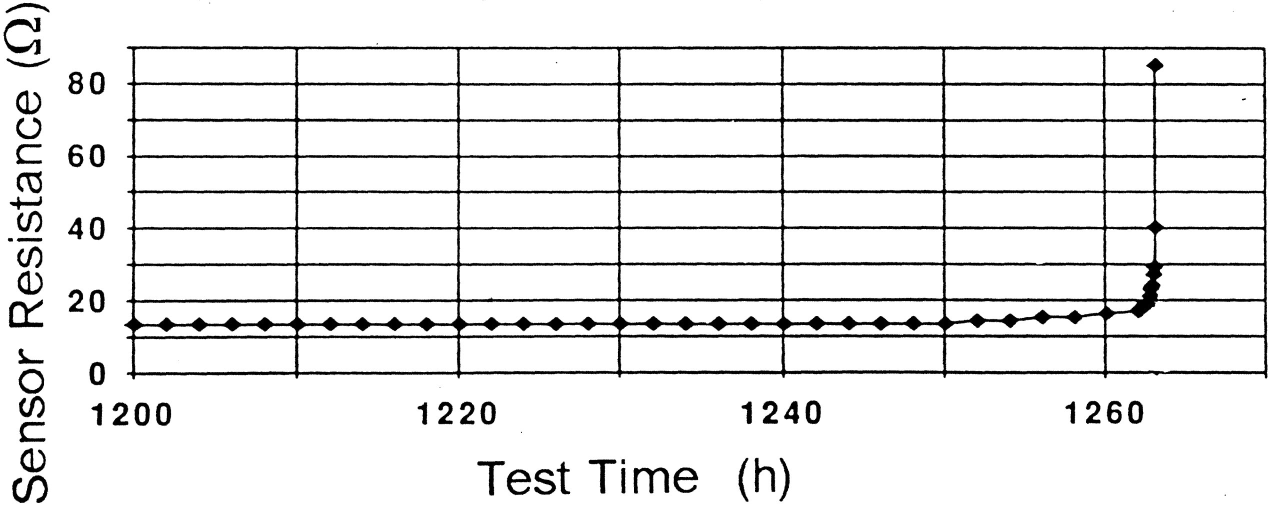
Electromigration

- ***Mean Time To Failure:***

$$MTTF = cJ^{-n} e^{E_a/kT}$$

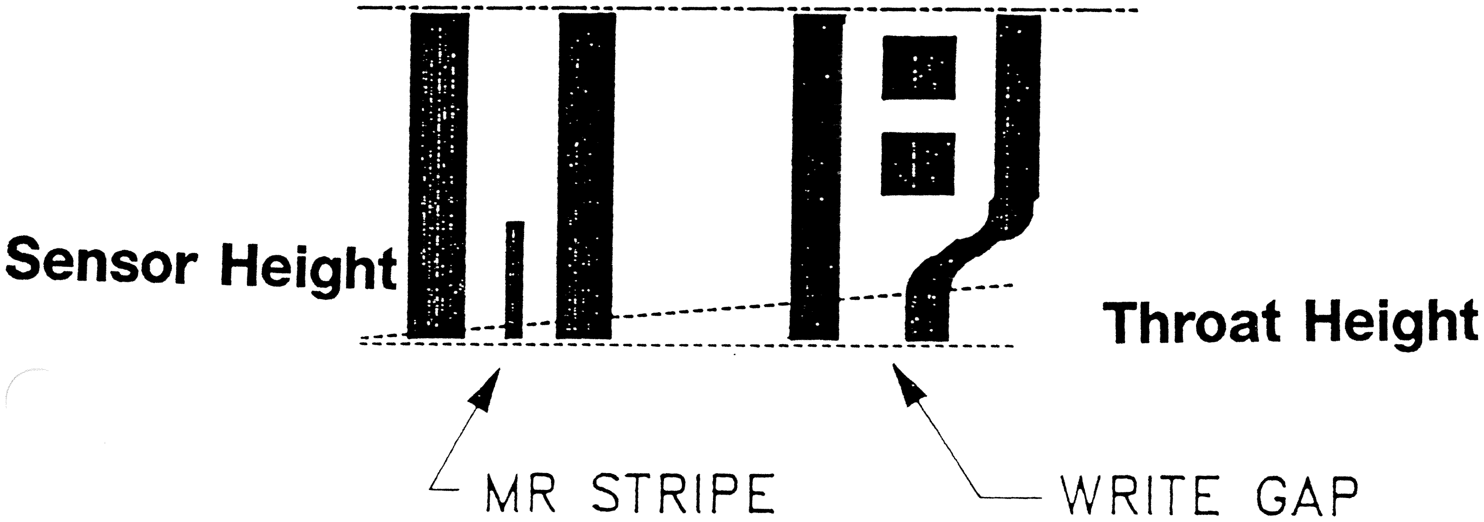
c constant (cross sectional sensor area)
J sensor current density
n experimentally determined exponent
E_a activation energy
k Boltzmann's constant
T absolute temperature

- ***Self-accelerating void/crack formation***



- ***Keep MR bias low enough (T and J), turn off when not needed***

Lapping Issues



Base Line Disturbances

Base line disturbances (ABS exposed MR heads):

- ***Thermal Events***
  - Additive to data signal

  A. Classical ″Thermal Asperity″ (TA)
  - o Fast rising (electronics BW limited)
  - o Compound, fixed exponential decay
  - o Mono-polar (positive)
  - o Heating, hard asperity frictional contact

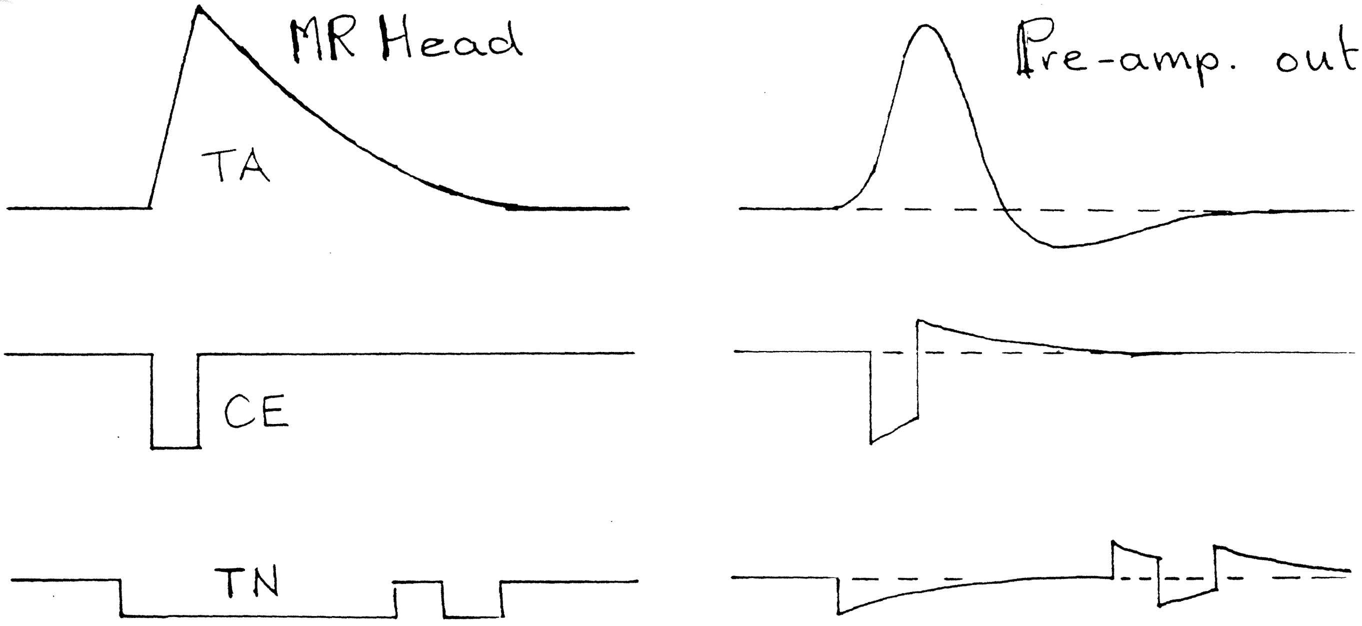
  B. Proximity ″Thermal Interference″
  - o Mono-polar
  - o Cooling by lube and proximity of disk ″summits″
  - o ″Wandering base line″ type of disturbance

- ***Conductive Events (CE)***
  - Mono-polar (negative for SE inputs)
  - Short lasting (contact time)
  - Fast rise/fall times (electronics BW limited)
  - Amplitude can be large
  - No data during event

Base Line Disturbances

- ***Smearing Events***
  - Conductive smears across read gap
  - Intermittent contacts
  - Fast rise/fall time (electronics BW limited)
  - Random signal, "Telegraph Noise" (TN)

N.B: High-pass nature of MR front-end electronics affects observed waveshapes

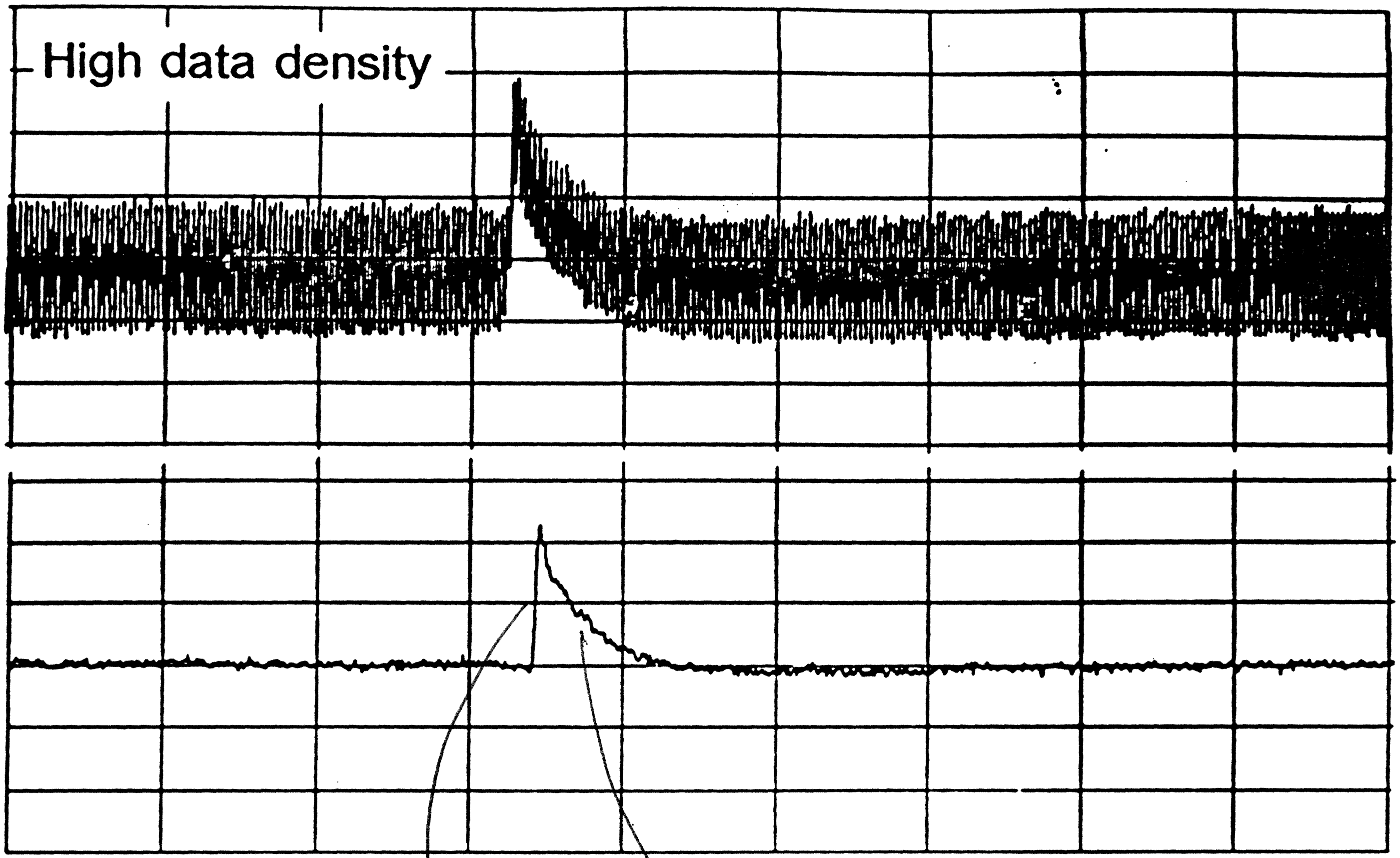


look like thermal asperities (exp. decay)

Base Line Disturbances

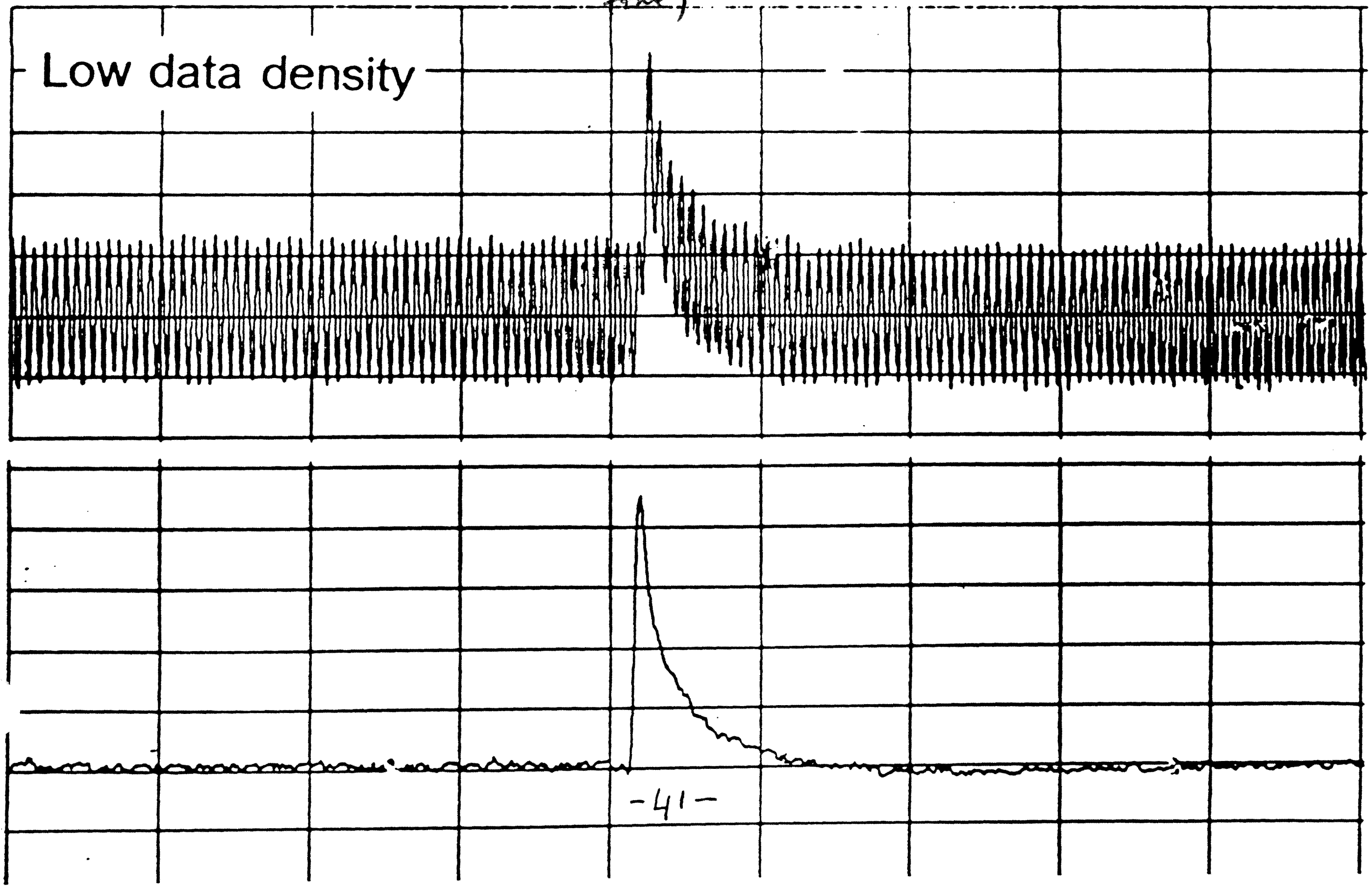
- ***Counter Measures***
  - *Thermal Events*
    Flag and remove TAs
    Restore base line variations
  - *Conductive Events*
    Turn MR bias off (landing/resting/taking off)
    Minimize voltage difference (sensor-disk)
    Limit ground return current (compare: Ground fault interruptor)
  - *Smearing Events*
    Remove conduction path
    Ground shields, apply potential to MR sensor (flying heads only)

"Classical" Thermal Asperity



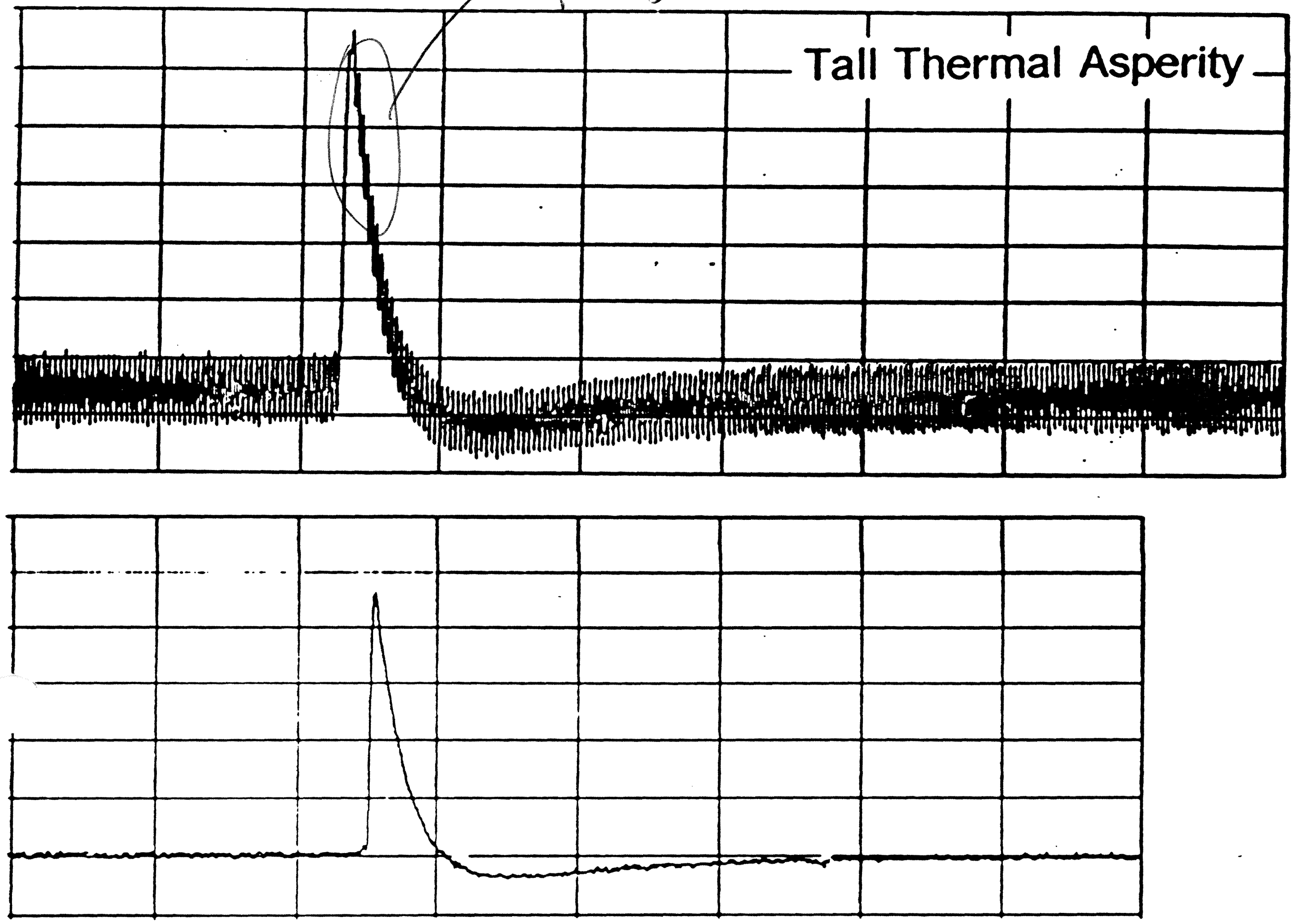
rise time is longest (rise time of amp or contact time)

thermal decay ($\tau = 0.5-1.5 \mu s$)

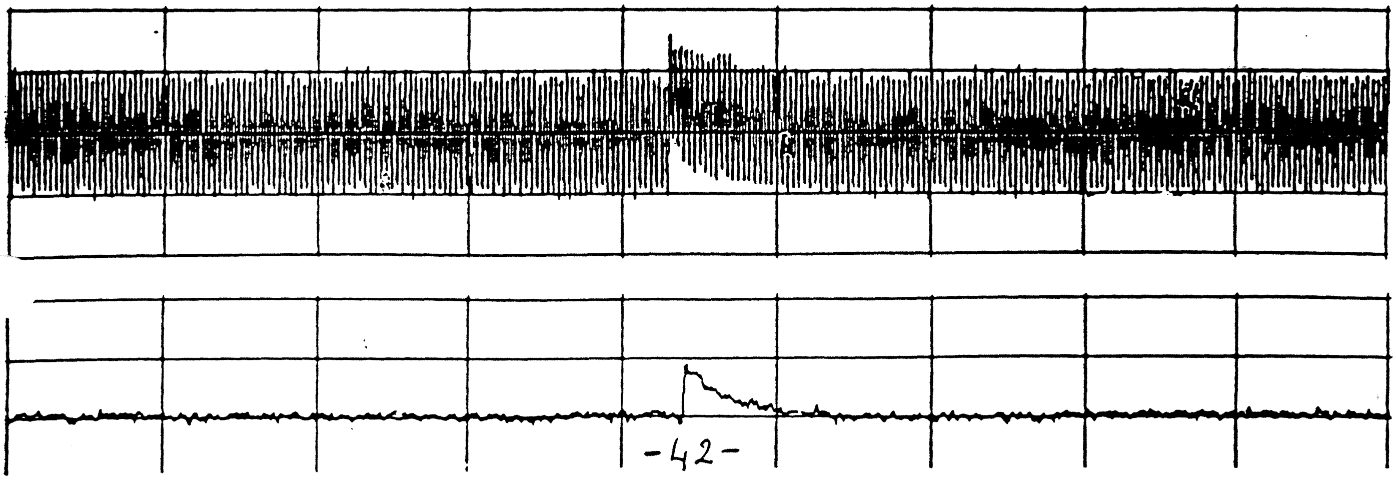


Different Size TAs

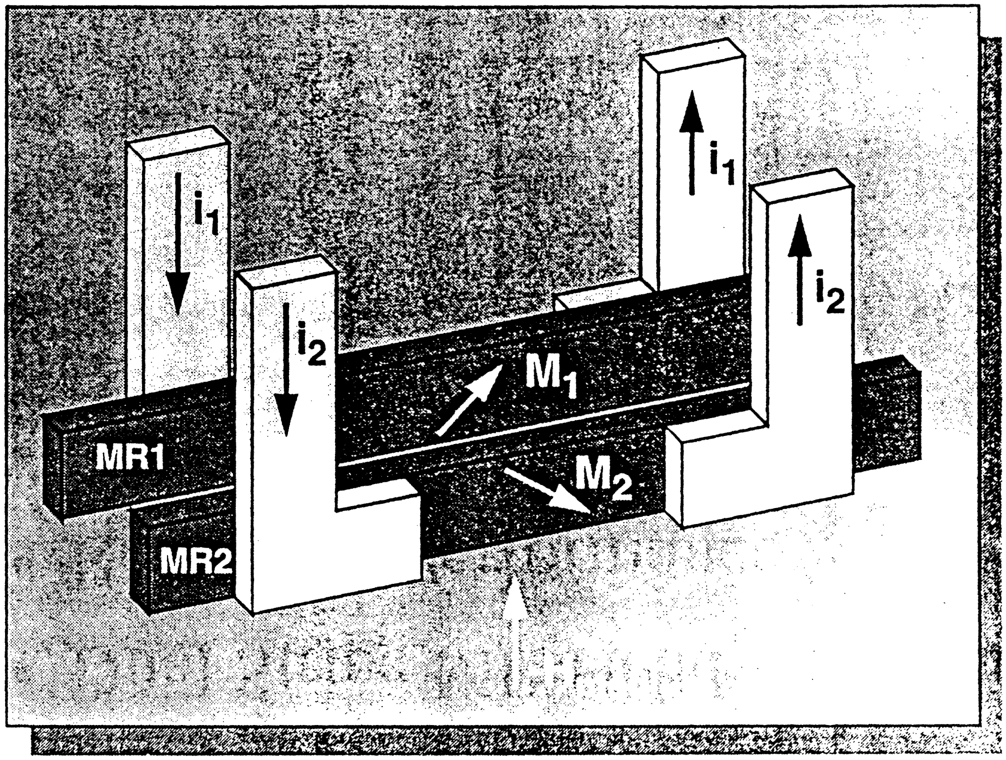
data smaller since spacing loss



Small Thermal Asperity



Dual Stripe MR Head



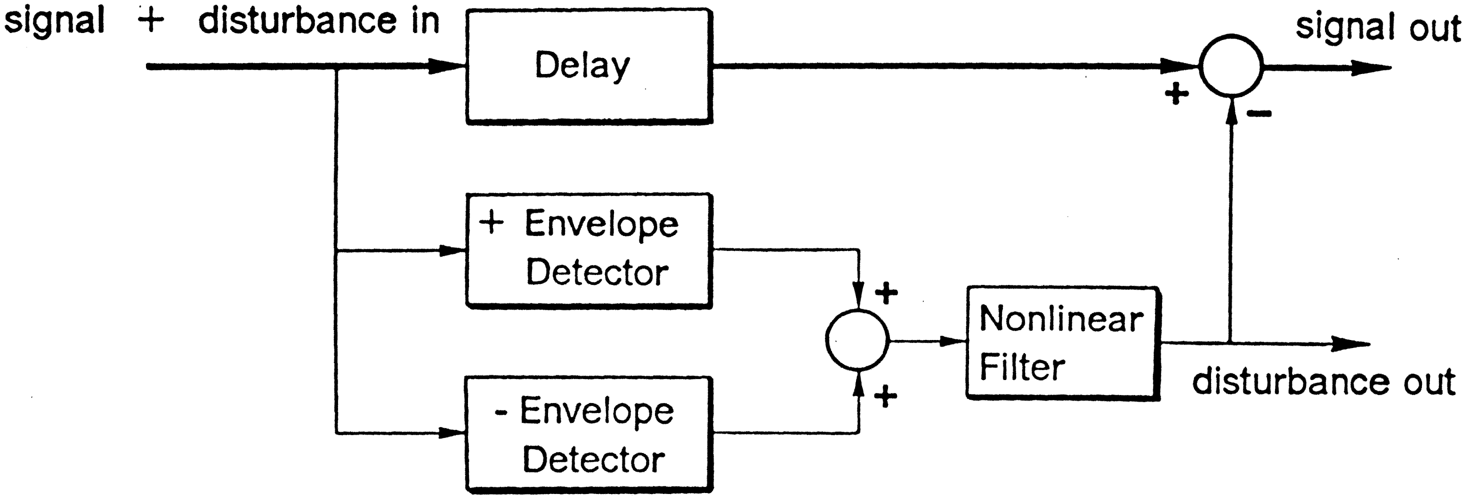
Why Dual Stripe Design?

- Double the signal
  (for same bias current I_B)
- Cancelling of even harmonics
  (on track) — not off-track
- Thermal asperity suppression
  (10% tolerance → 20 dB)
  resistance.
- Symmetrical track profile
  (servo advantage)
- Interference rejection
  (10% tolerance → CMRR = 20 dB)
  resistance

Issues Dual Stripe Design

- Interstripe shorting
- Alignment tolerances
- Needs matched MR sensors
- Needs 3 MR leads
- Temperature rise limited biasing → ½I_B per stripe → same signal — only coolers to external sinks
- Disk flux shared between sensors → smaller signal

Asperity Reduction Circuit (ARC)



signal + disturbance in

Delay

+ Envelope Detector

- Envelope Detector

+

+

Nonlinear Filter

+

−

signal out

disturbance out

In practice drop delay so do correction after asperity begun.

United States Patent [19]

Jove et al.

[11] Patent Number: 4,914,398

[45] Date of Patent: Apr. 3, 1990

[54] METHOD AND CIRCUITRY TO SUPPRESS ADDITIVE DISTURBANCES IN DATA CHANNELS CONTAINING MR SENSORS

[75] Inventors: Stephen A. Jove, Watsonville; Klaas B. Klaassen; Jacobus C. L. van Peppen, both of San Jose, all of Calif.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 226,634

[22] Filed: Aug. 1, 1988

[51] Int. Cl.⁴ H03K 5/00; H04B 1/10

[52] U.S. Cl. 328/167; 328/162; 307/520; 307/555; 307/350; 455/296; 455/303; 333/14

[58] Field of Search 307/350, 358, 359, 555, 307/520; 328/165, 167, 169, 151, 162; 455/296, 303, 304, 305-308, 222, 225; 333/14; 330/109, 149, 151

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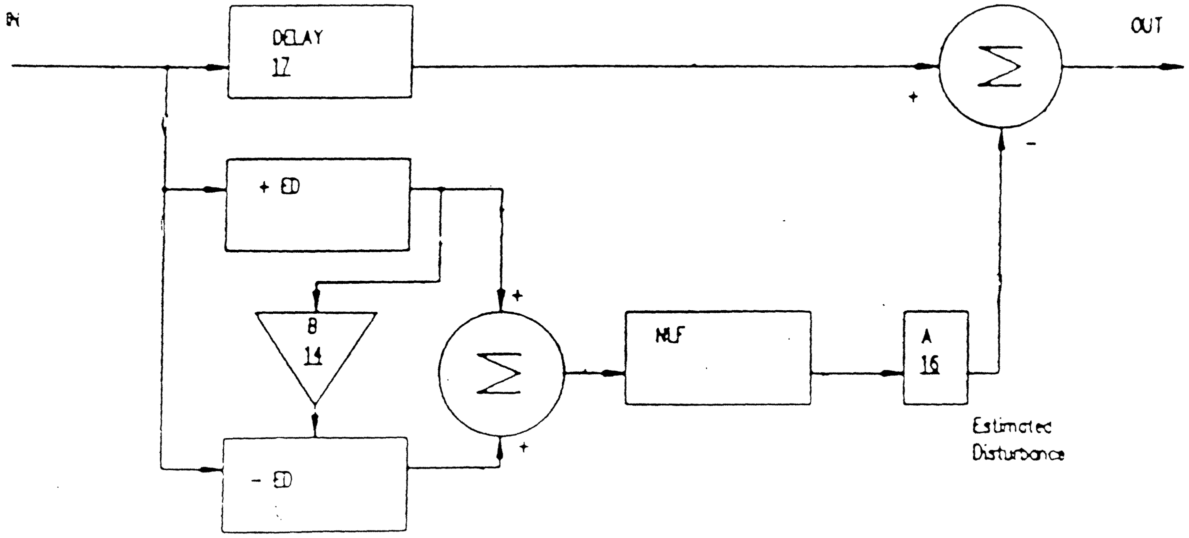
Primary Examiner—Stanley D. Miller
Assistant Examiner—Timothy P. Callahan
Attorney, Agent, or Firm—Henry E. Otto, Jr.

[57] ABSTRACT

A method and circuitry are disclosed for suppressing additive transient disturbances in a data channel; e.g., due to thermal transients caused by an MR transducer contacting moving a storage surface. Positive and negative envelope detectors each have their inputs connected to the channel, and provide respective outputs which are summed and contain an envelope component and a residue component. A buffer interconnects the detectors to allow both detectors to follow rapid positive excursions of the data channel signal. A nonlinear signal-adaptive filter is connected to the summed output to further reduce the residue component. The data channel signal (or preferably the output from a delay means connected to the channel) is summed with the output from the filter. The relative amplitudes of these two outputs is set such that the resulting summed output signal is free of additive disturbances.

11 Claims, 4 Drawing Sheets

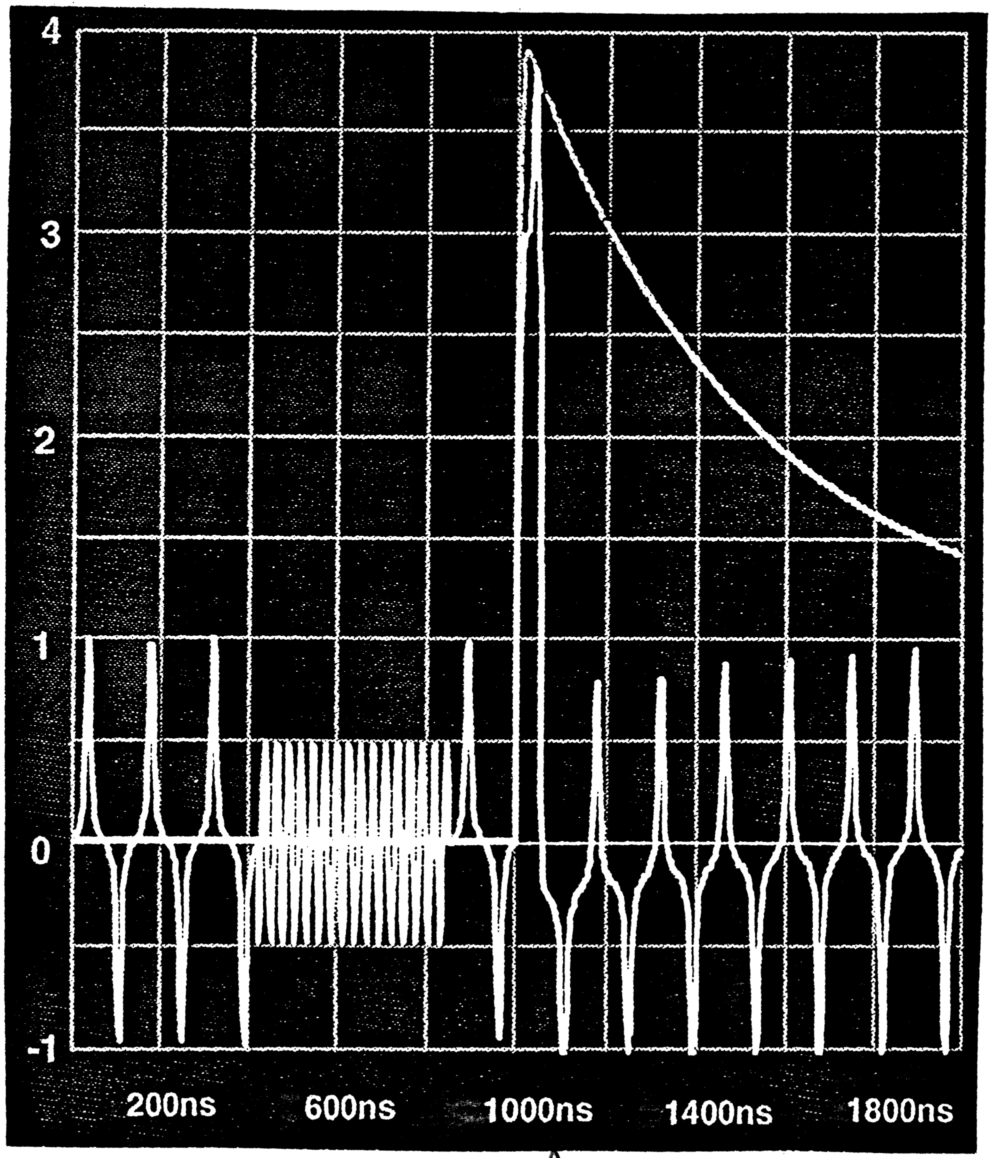


TA Base Line Restoration

Detect base line variation, subtract from signal

Asperity Reduction Circuit (ARC)

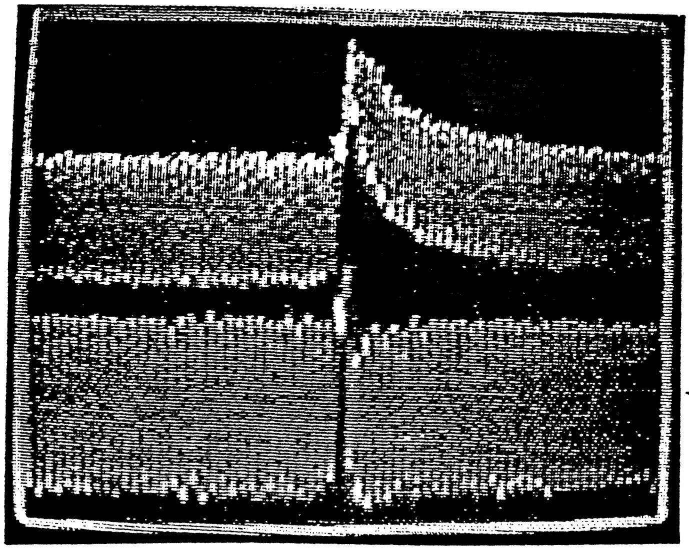
Subtractive restoration also provides restored TA



correction kicks in

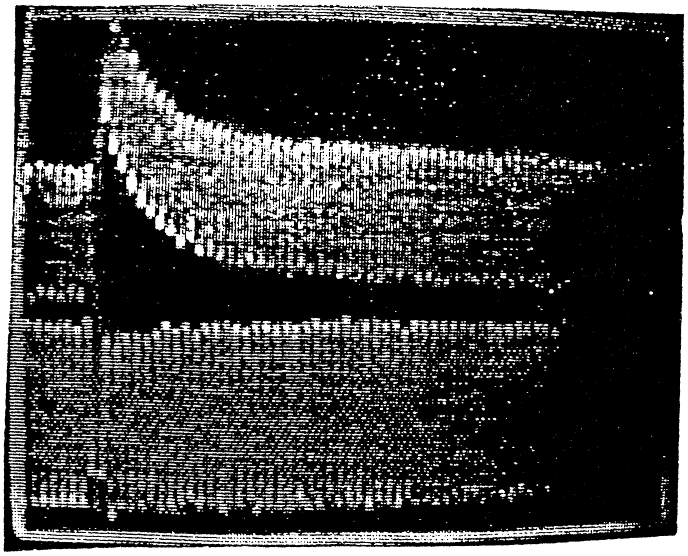
Asperity Reduction Circuit (ARC)

Electronic Thermal Asperity Removal:



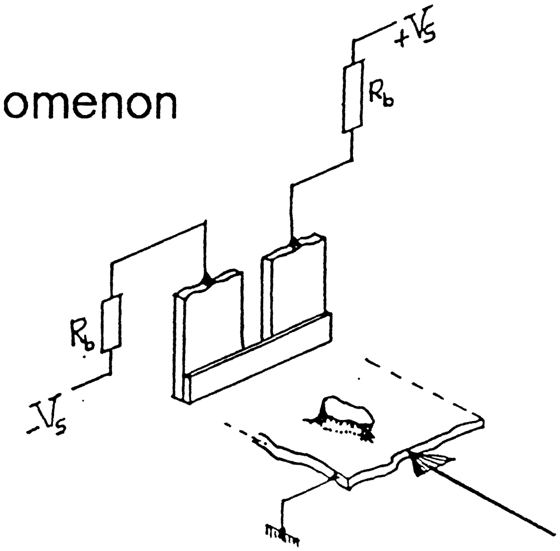
Electronically corrected.
Magnitude 2 times

amplitude loss not corrected (ECC takes care of this)



MR Sensor Edge Erosion

Observed phenomenon



edges of sensor biased different than disk.

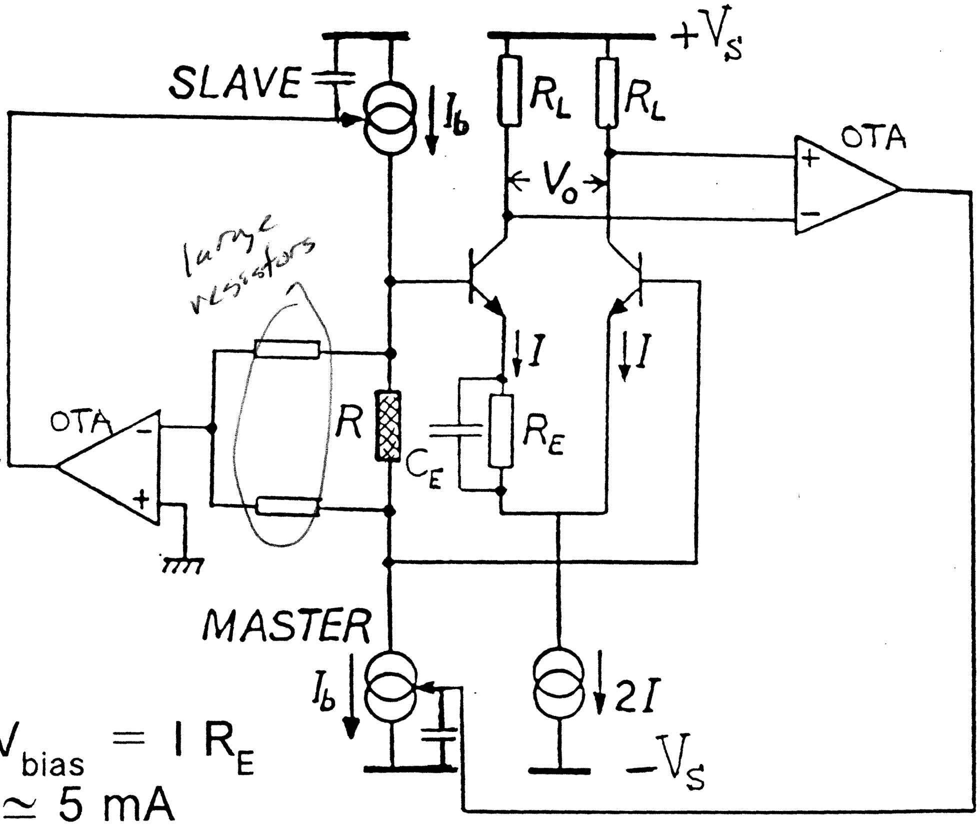
Electro-erosion creates recessed sensor
Loss of sensitivity

Counter measures:

- **Keep disk at potential of sensor**
  (floating, biased Disk Enclosure)
- **Keep MR sensor at ground potential**
  (requires dual power supply)
- **Keep one sensor lead at ground potential**
  (single supply, single-ended amplifier input)
  no CMR
- **Limit ground return currents to safe values**
  (ground fault interruptor analogy)

Sensor Erosion Protection

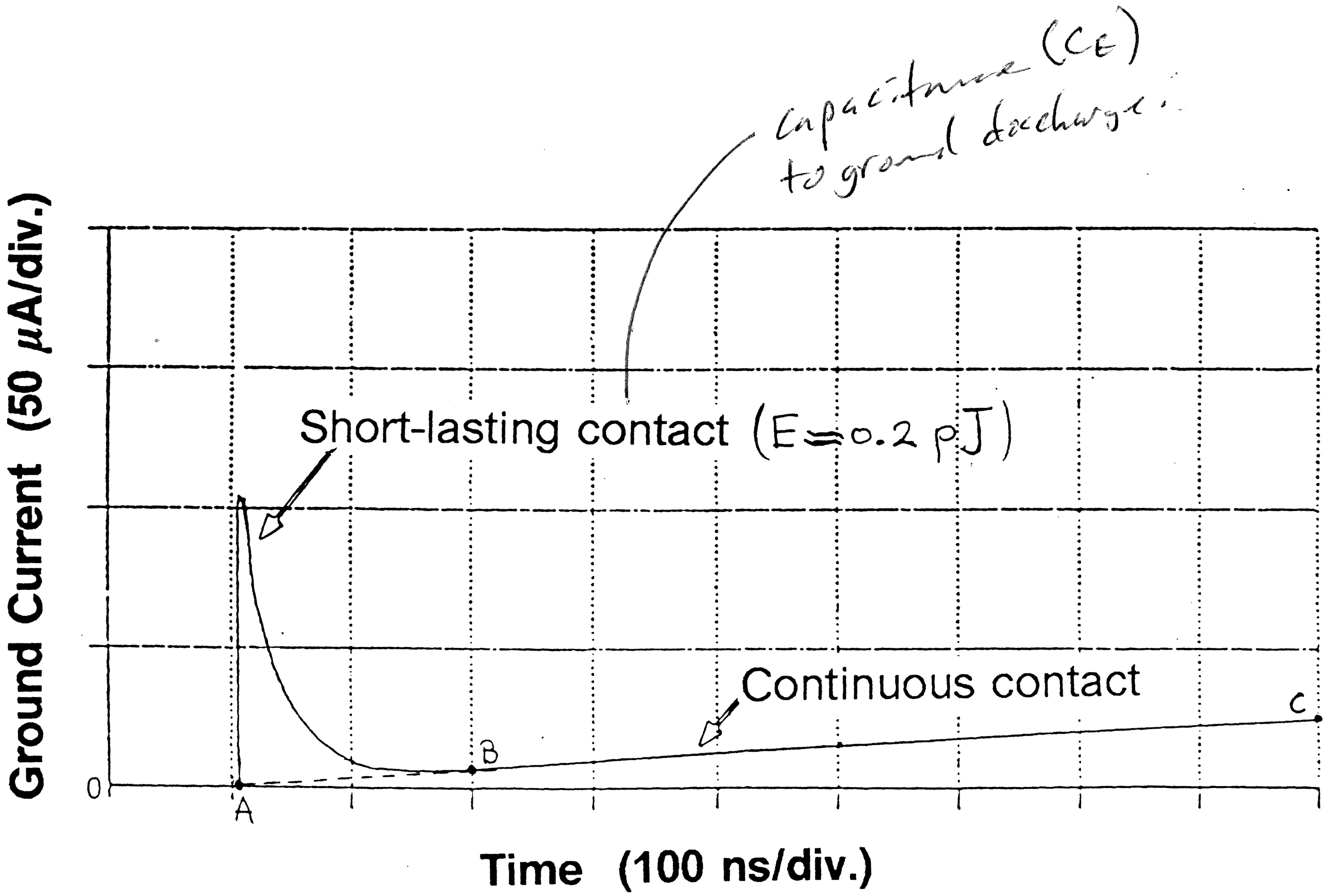
- Module detects relative resistance variation $\Delta R/R$ (Less sensitivity scatter due to tolerances)
- Maintains **center of MR sensor** at ground potential
- Limits peak ground return current to less than 100 μA for short-lasting conductive events



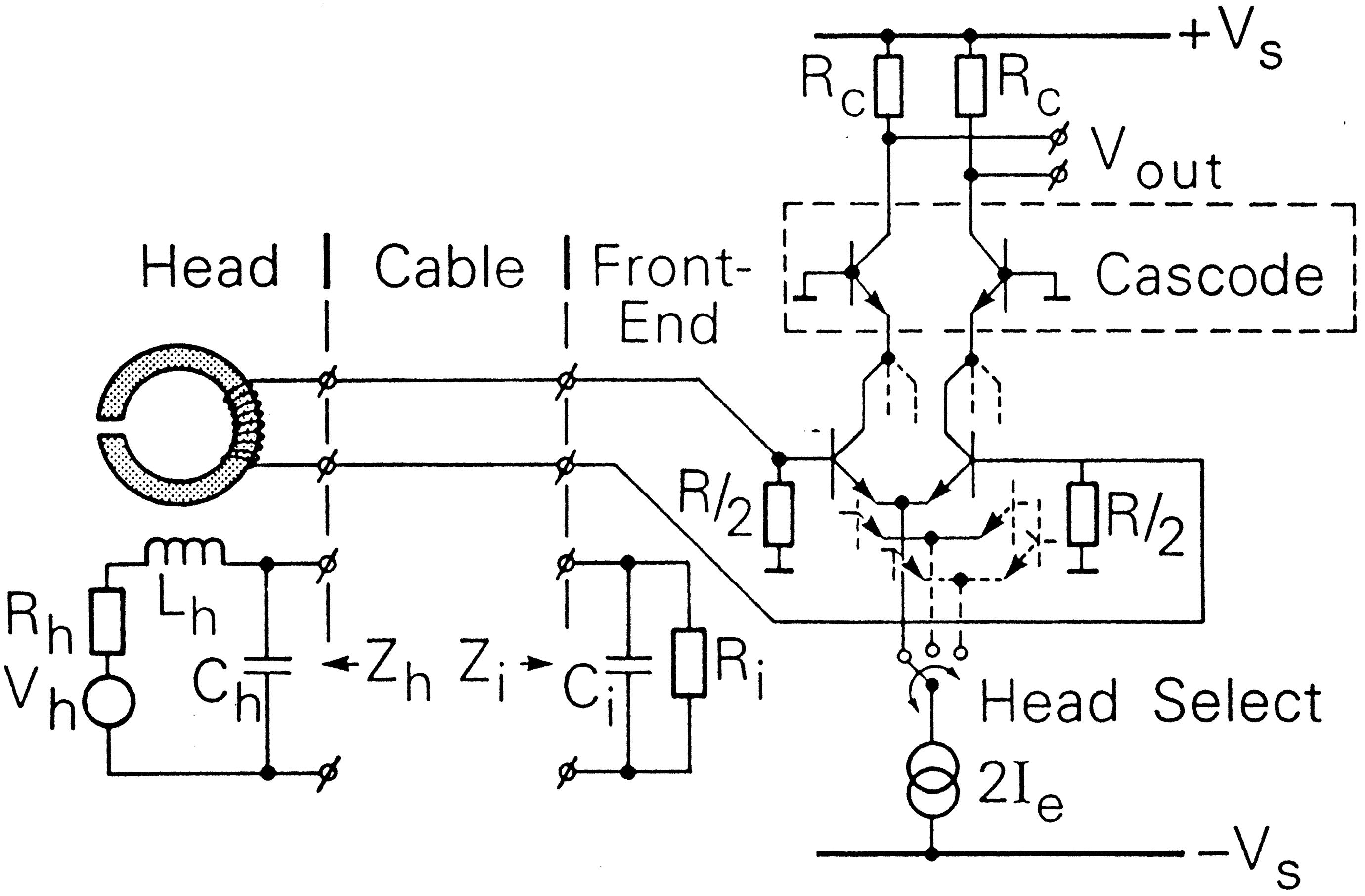
Voltage bias of sensor can't draw current to ground.

Voltage bias $V_{bias} = I R_E$
$I = \text{constant} \simeq 5\ \text{mA}$
Bias current $I_b = V_{bias}/R$
Output $V_o = A V_{bias} \Delta R/R$, gain $A = R_L/r_e$

Conductive Asperity Current

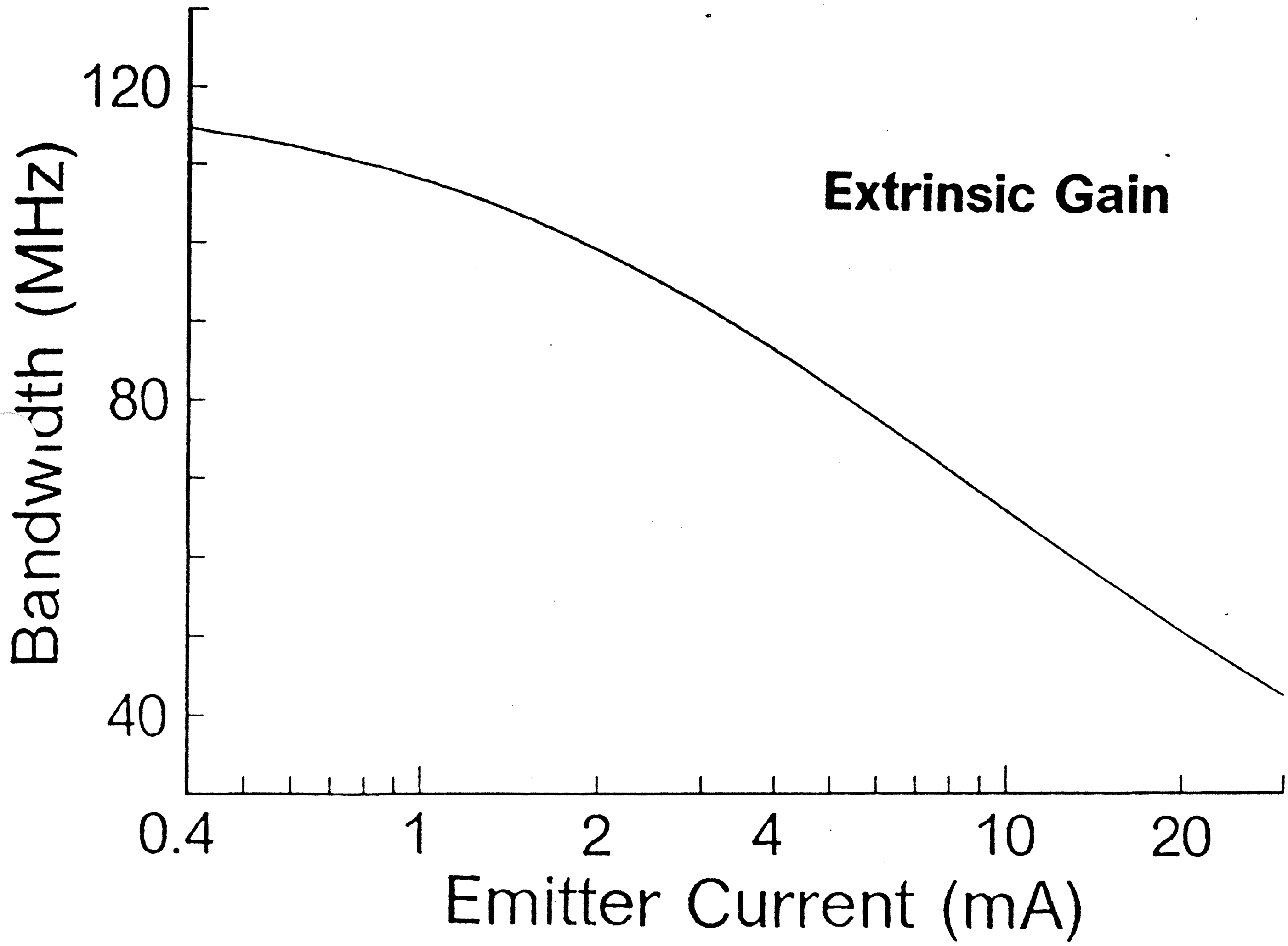


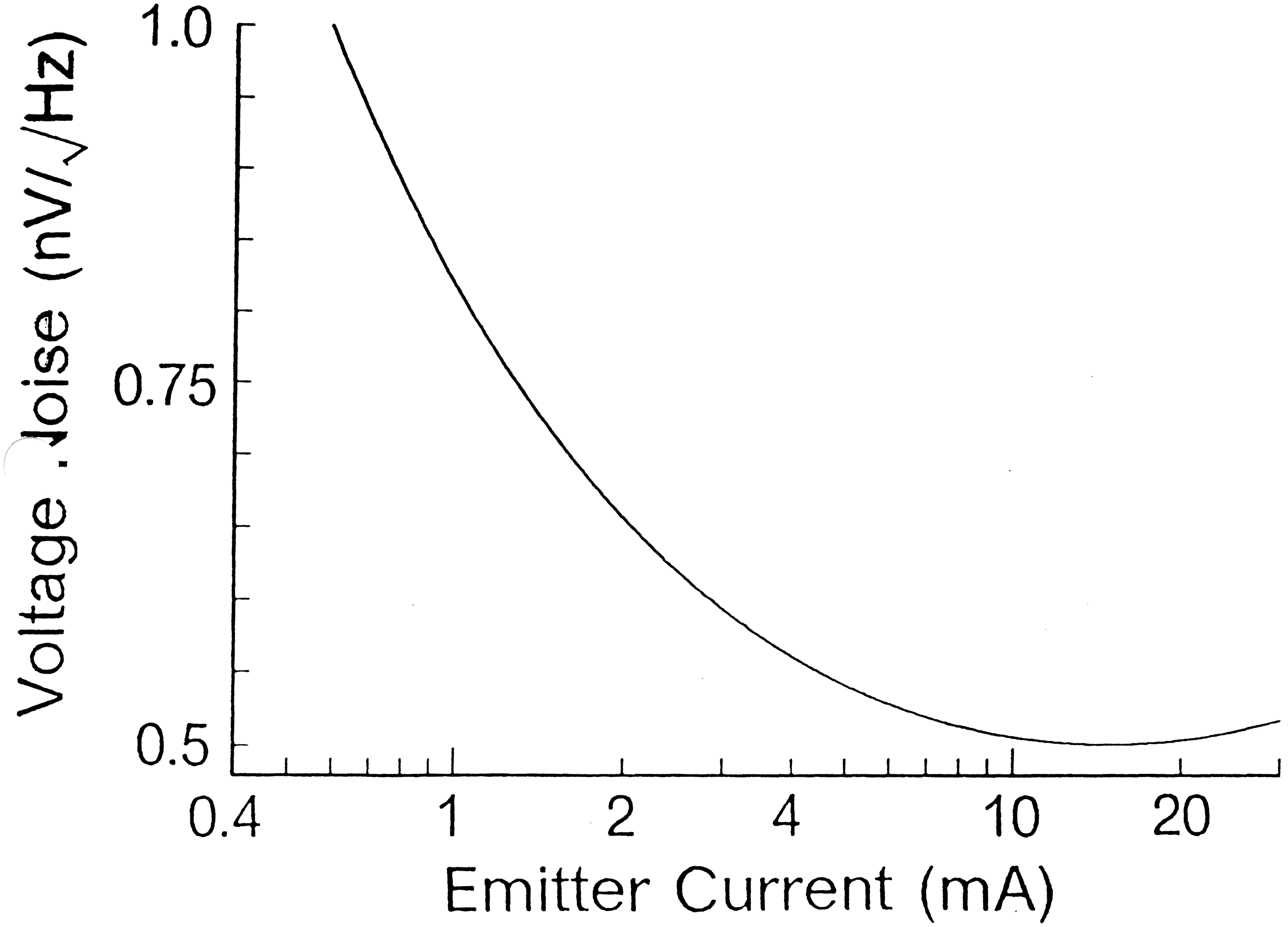
Inductive Front End



extrinsic gain/attenuation before reach electronics

- capacitance loading by amp input



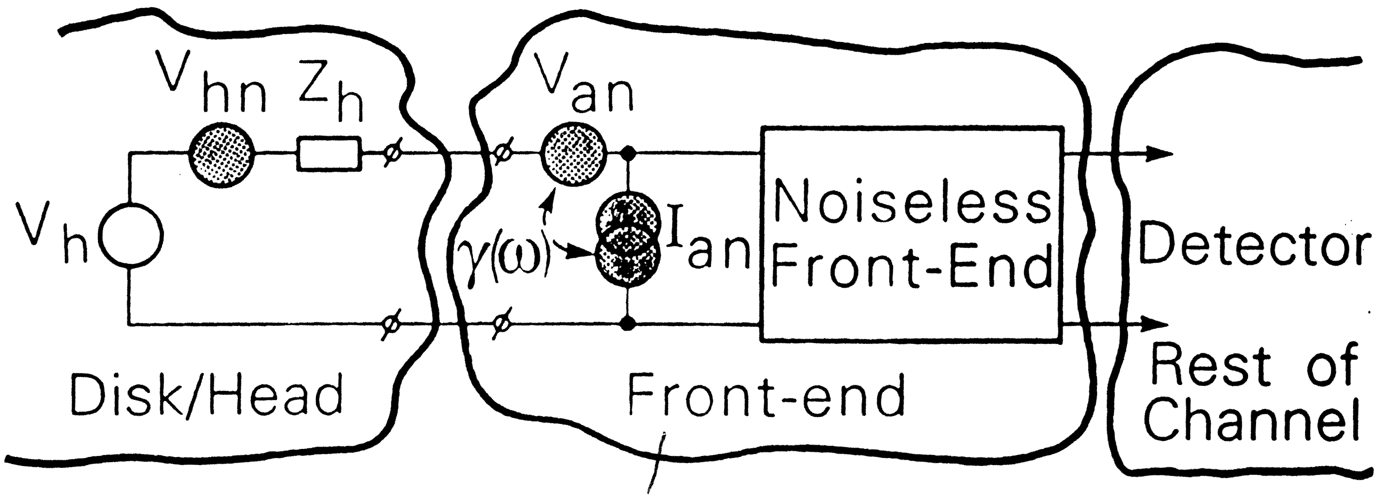


opposes attenuation

Noise Modelling Results

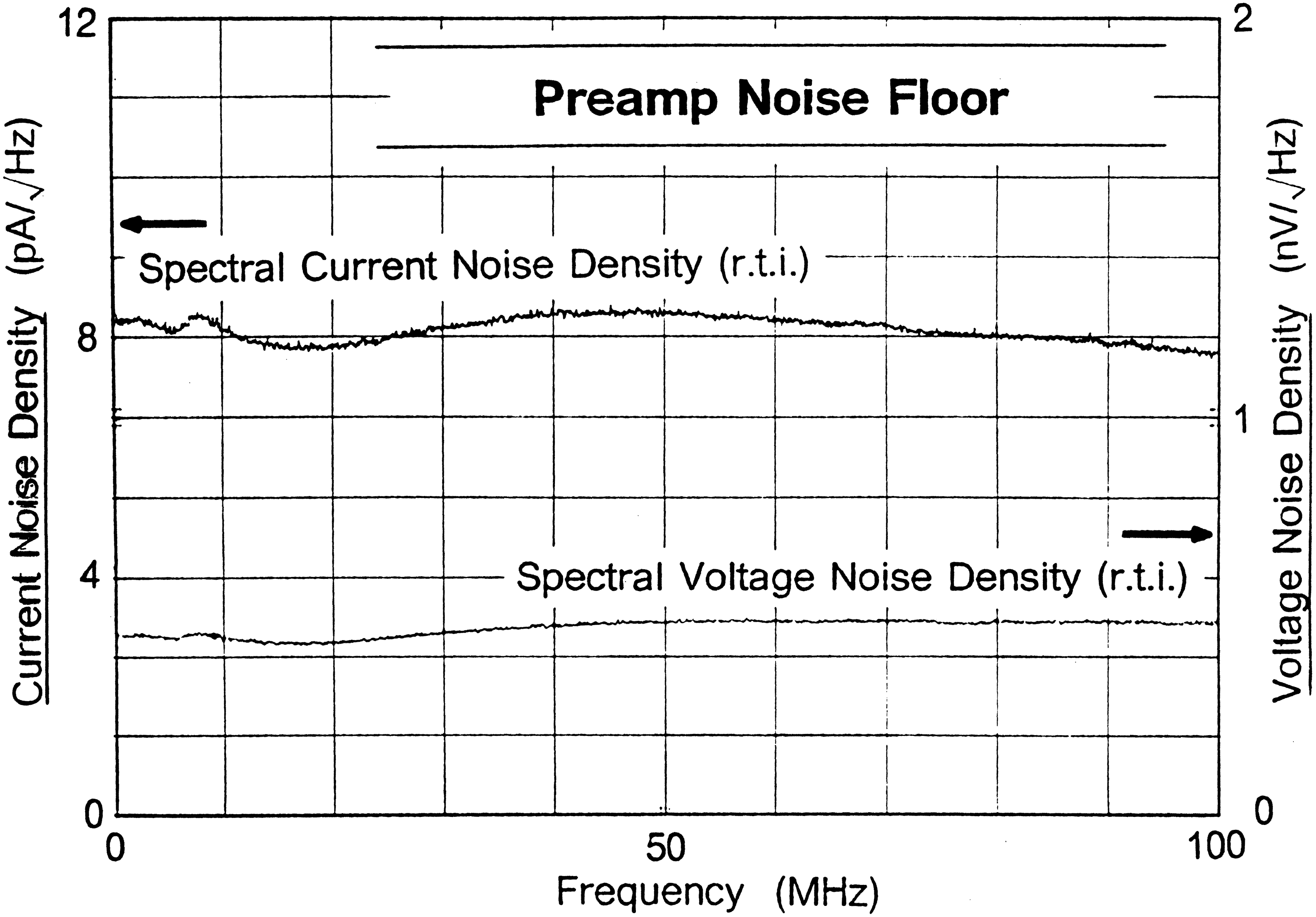
- Noise versus bandwidth dilemma
- Forces compromise value for the input transistor bias current
- For high bandwidth and low noise:

parameter	**Current**	**Performance**
high f_t	(5 GHz)	
high β	(80)	For n = 36
low $r_{bb'}$	(2.5 Ω)	BW = 100 MHz
$\lvert Z_h \rvert << 2R_{damping}$	(2 kΩ)	v_{en} = 0.5 nV/√Hz
low K_l — indl/√turn	(1.25 nH)	at bias current
low K_r — res: single turn	(1 Ω)	2.5 - 5 mA

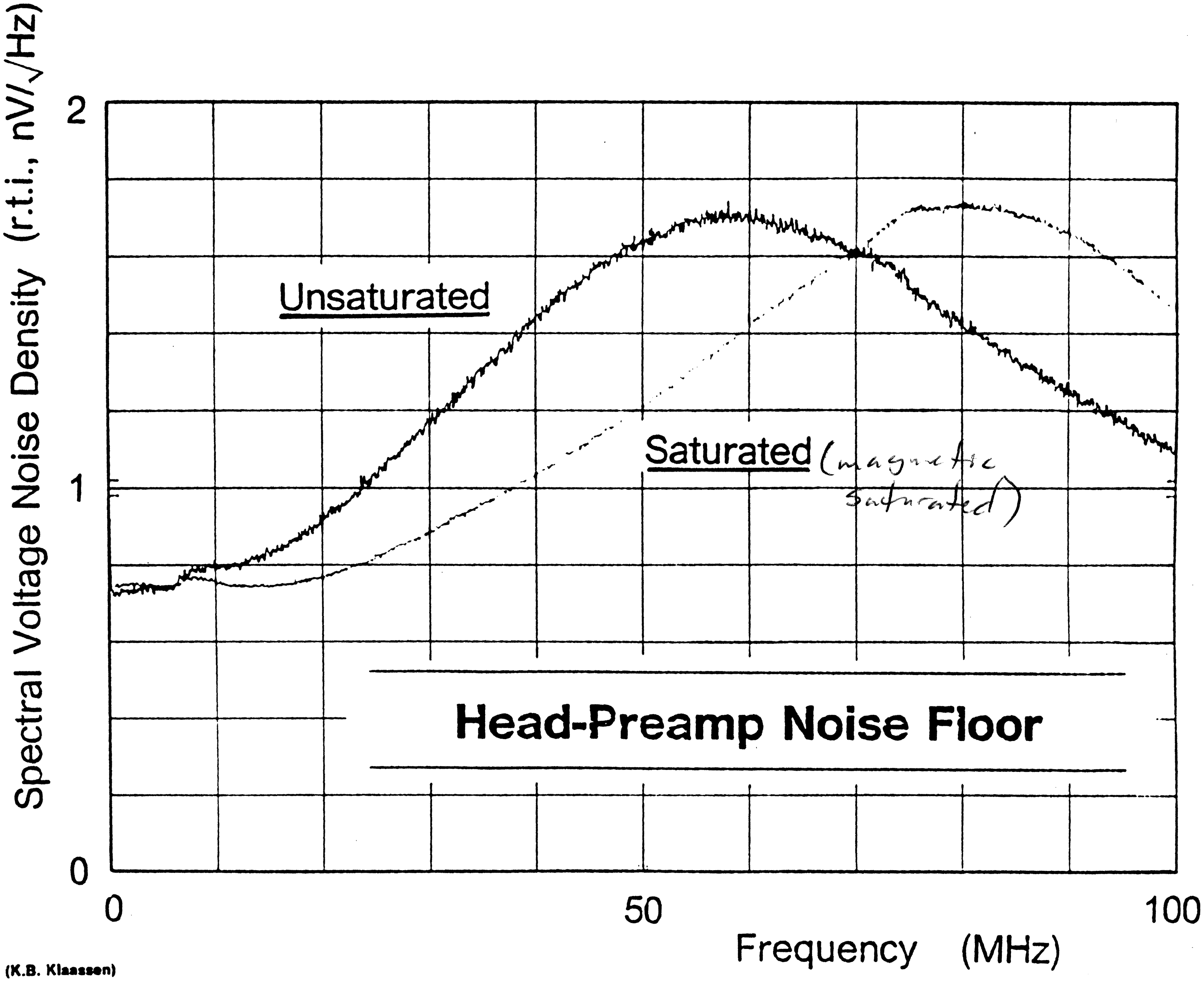


noise source

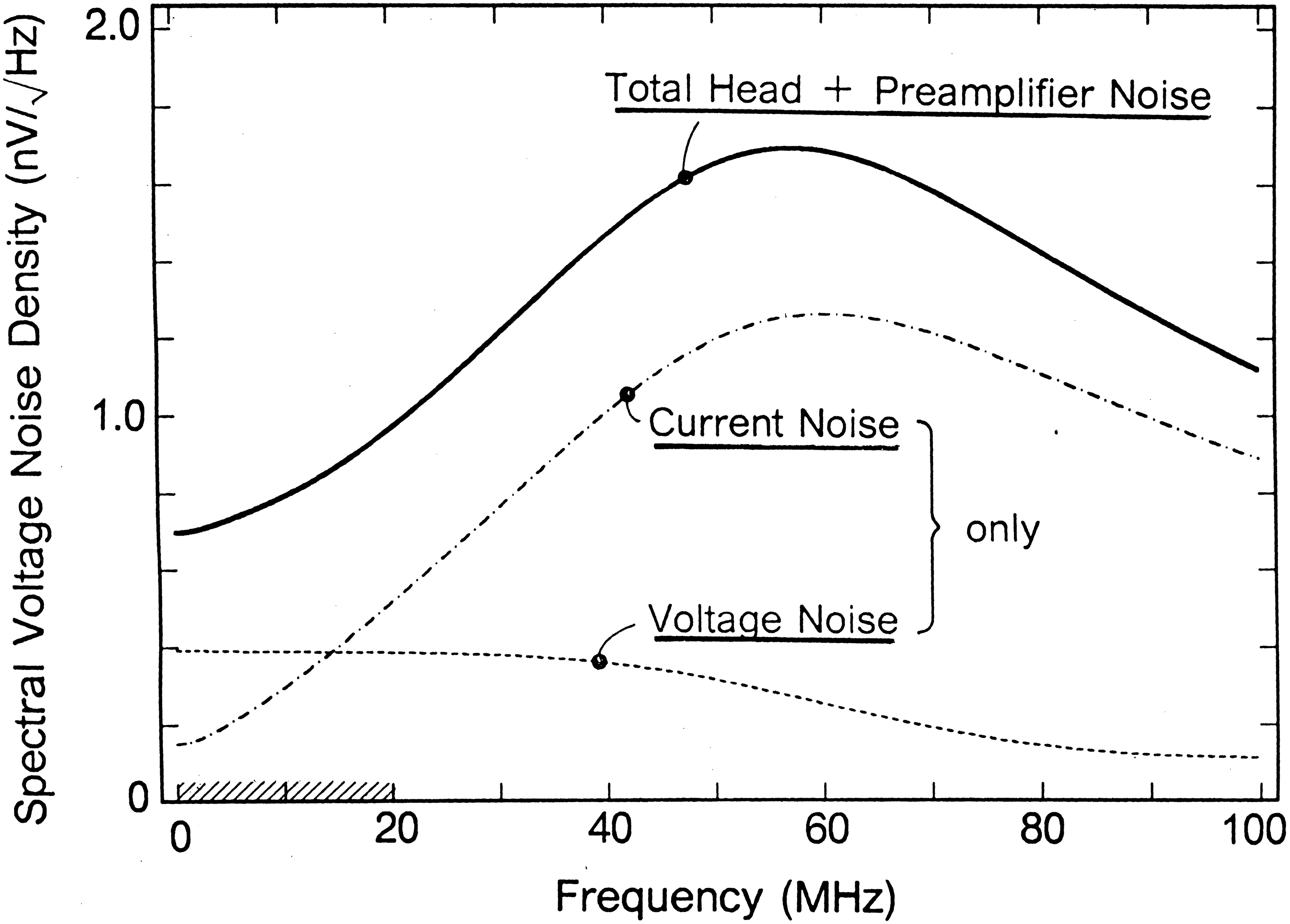
~can be correlated towards band ends



I_n through head impedance gives noise voltage

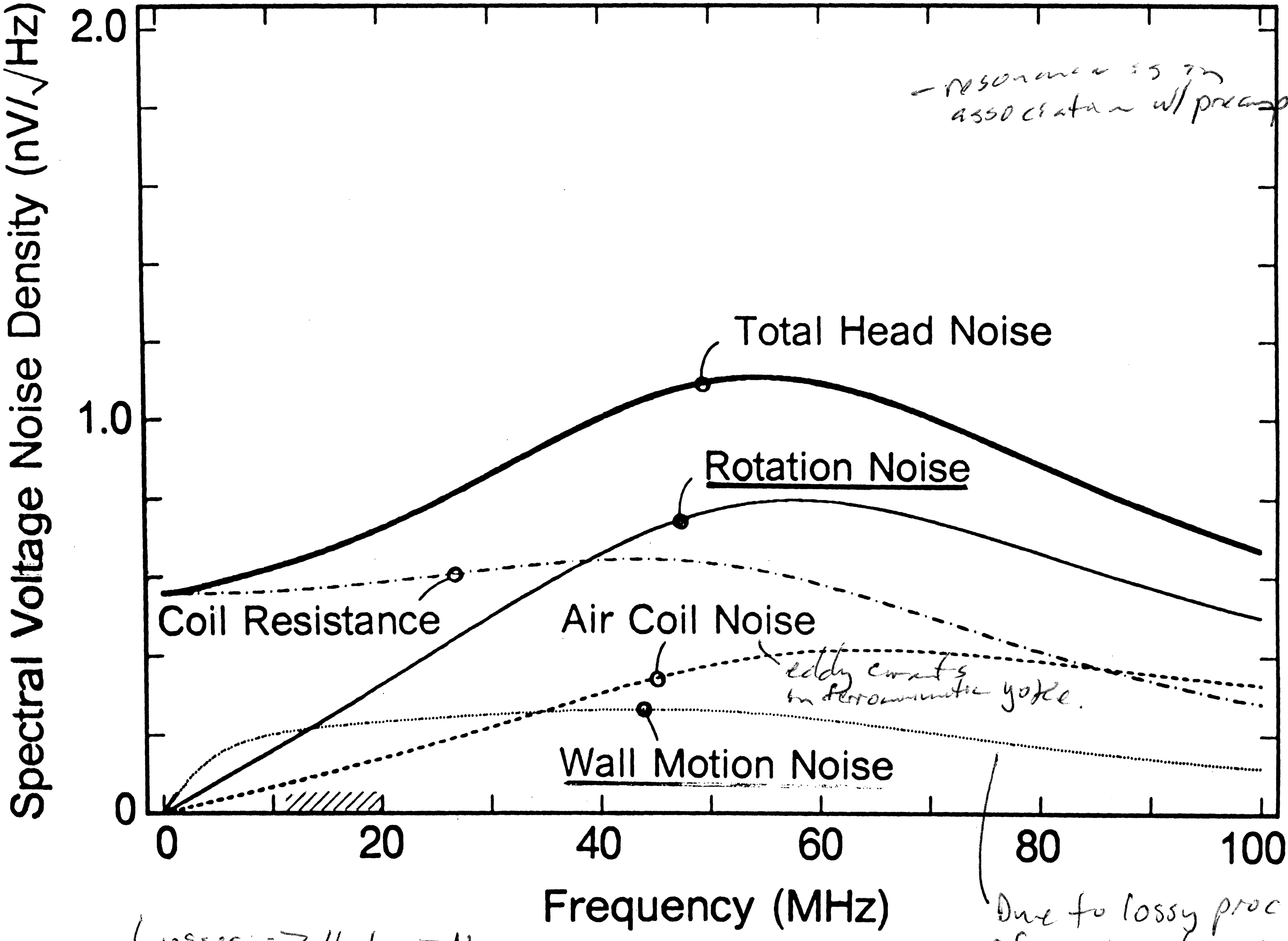


9/91 (K.B. Klaassen)



—When go against resonance current noise dominates

Head Noise



-resonance is in association w/ preamp

eddy currents in ferromagnetic yoke.

Due to lossy process of moving domains

Losses => Heat => Noise

Noise Matching

Often mistaken for ***"Impedance Matching"***

(Transmission lines, reflection free: $Z_i = Z_{TL}$)
(Maximum power transfer: $Z_i = Z_s^{\star}$)
(conjugate load impedance

Define ***"optimal source resistance"***

$$R_{opt} = \frac{V_{an}}{I_{an}}$$

(Just a ratio, non-physical resistance)

- ***Low Electronics Noise Design***
  - Make V_{an} and I_{an} as small as economically feasible (large area, low-noise input devices)
  - Put most effort into reducing largest contributor: $V_{an}, \; I_{an}|Z_h|$ (scale Z_h by changing turns N, scaling limited by write fuction of the head)
  - If $|Z_h| \neq R_{opt}$ further reduction of electronics noise is possible by ***"Noise Matching"***

Noise Matching

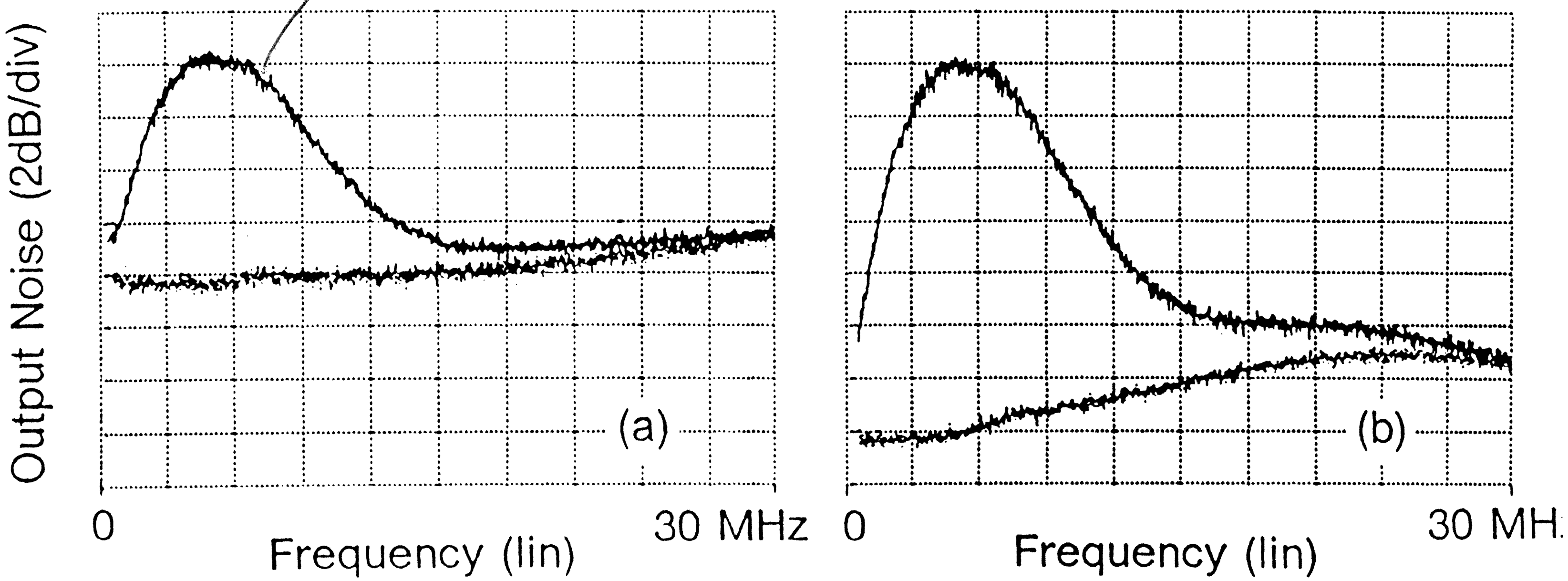
- Insert reactive components (no noise contribution) for noise matching:
  - Transformer $N = \sqrt{R_{opt}/|Z_h|}$
  - Series/parallel reactances (finite band)

- but may get interference

Example: IBM 3380 channel front-end obtains 6 dB Signal-to-Electronics-Noise improvement by noise matching

total w/ disk (DC Erase)

6dB S/N improvement



Transformer $N = 23/4$,

Total noise (top), Head and electronics noise (bottom)

Internal X-former in head design possible

Magnetic Head Instability

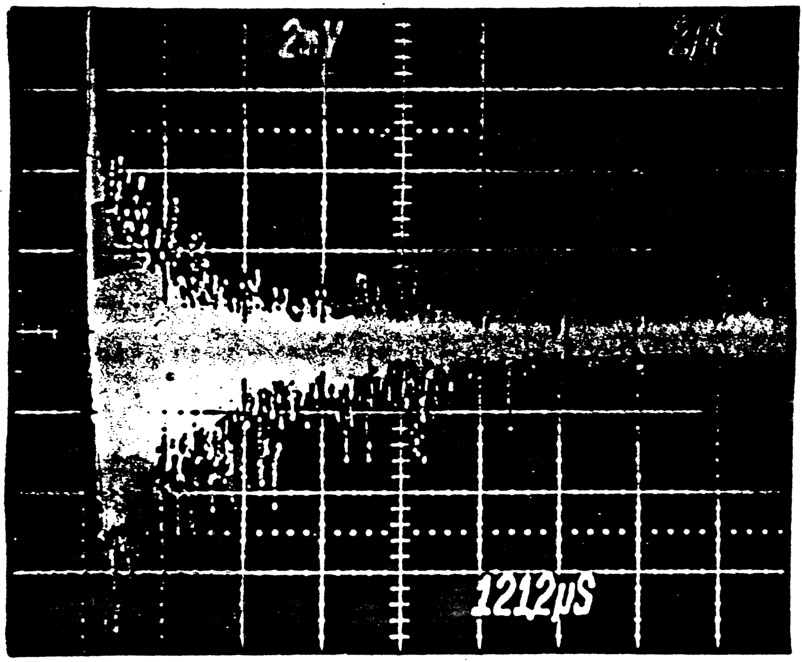
- **Write Instability**

  Definition: Delayed relaxation of head yoke, ***immediately after write***

- **Read Instability**

  Definition: Domain wall instability in head yoke, ***long after last write***

Relaxation after Write

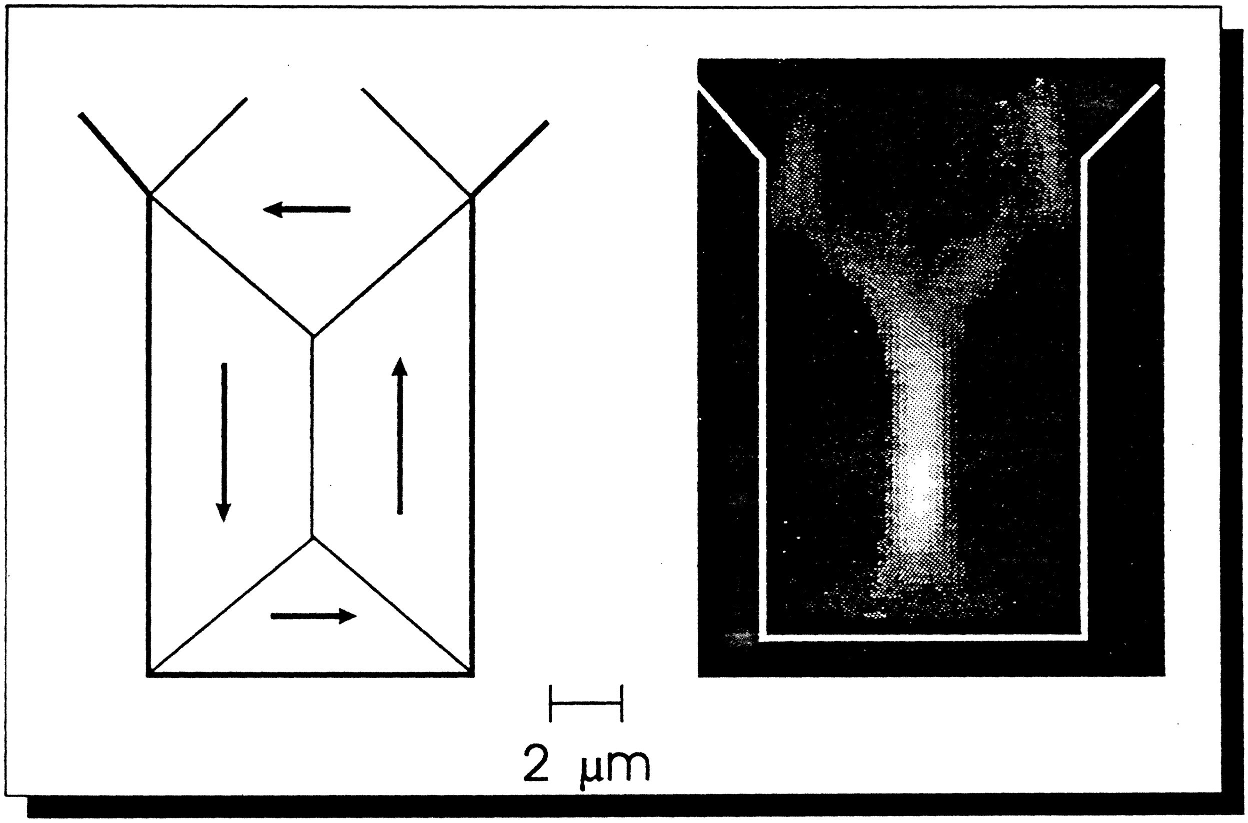


Can cause
Servo problems

I_W = 34 mA

t_o = 1 μs

Domain Images



- vertical domain wall shows biggest domain noise.

klaas.cdr

P.K. 9/9/91

MR Front-Ends

General

Front-end read/write electronics combined in a stand-alone analog integrated circuit

- Bipolar or BiCMOS technology
- Trend BiCMOS because:

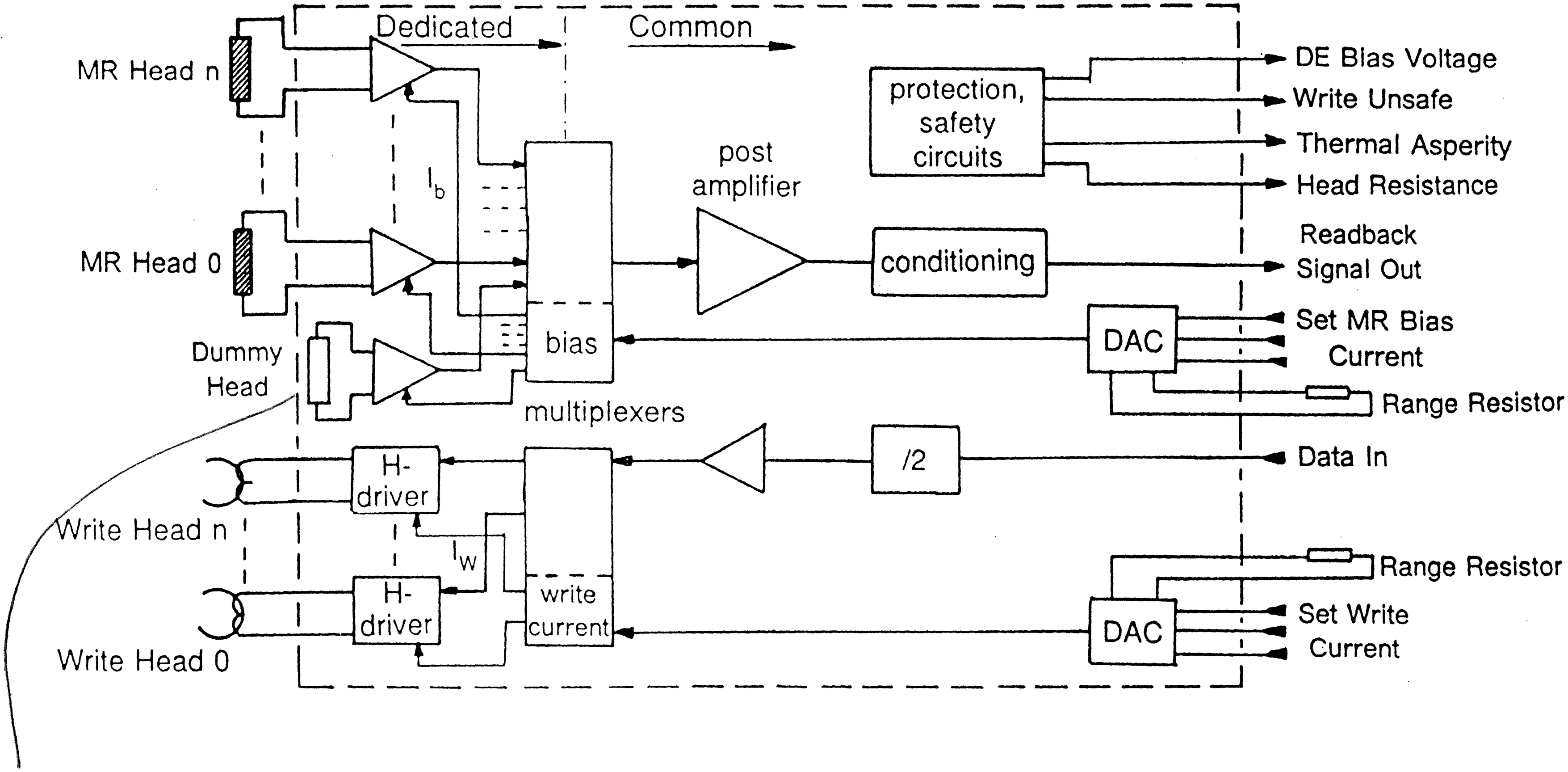
  Bipolar
  - Higher currents
  - larger transconductance
  - higher gain-bandwidth product
  - lower noise (for low source resistance)
  - virtually ideal current switches
  - tolerances can be kept small
  - good V_{be} matching

  CMOS
  - virtually ideal voltage switches
  - allows low-power CMOS logic
  - very good packing density

Location

- Inside disk enclosure
- As close as possible to read/write transducers
  - Read signals small: 150 - 700 μV_{pp}
  - Write signals: require wide-band interconnections
  - Usually on the side of the head actuator arm

MR Front-End Architecture



parking
head so
keep circuit
active

MR Front-Ends

Various Design Considerations

A - MR Head Signal Amplitude

Magnetic transitions in disk cause a magnetic flux impinging on the MR sensor which produces a ΔR_{MR} which increases

1 - Linearly with track width (TW)
2 - Inversly proportional with sensor height (h)
3 - (Approximately) linearly with disk $M_r t$

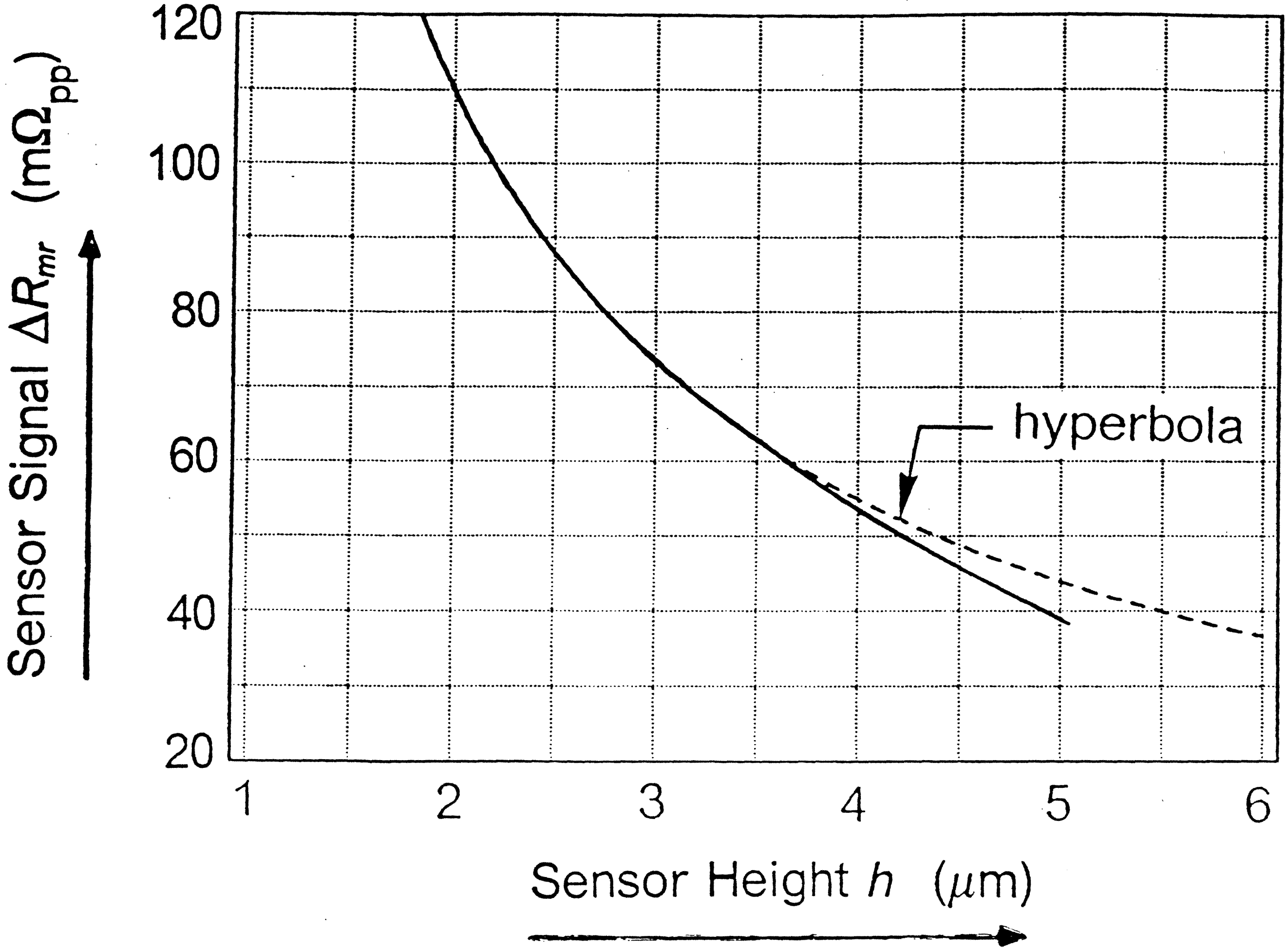
low Mrt <1 memu/c
so don't overdrive circu

Electronically detecting $\Delta R_{MR}/R_{MR}$ instead of ΔR_{MR}, therefore, makes the pre-amplifier output insensitive to variations in ① and ②

N.B: Especially the sensor height (defined by lapping) varies strongly

$\Delta R_{\mathrm{MR}}/R_{\mathrm{MR}}$ *Detection*

provides inherent or self-AGC, relieving the dynamic range requirements of the channel AGC.



$$R_{mr} = \rho \frac{l}{th} = \alpha \frac{1}{h}$$

$$\Delta R_{mr} \simeq \beta \frac{1}{h}$$

Hence,

$$\frac{\Delta R_{mr}}{R_{mr}} \quad \text{independent of } h$$

MR Front-Ends

B - Biasing and Sensing Architectures

— *Four Possible Architectures*
Different forms of providing electrical bias to the MR sensor and sensing the read signals lead to four different front-end electronics architectures

— $\Delta R_{MR}/R_{MR}$ *Detection*
Only those architectures where biasing and sensing have the same physical dimension give $\Delta R_{MR}/R_{MR}$ detection

e, g. current bias & sensing.

— *Sensor Temperature/Current Density*

- o MR sensor output increases with bias
- o Bias limited by electromigration/interdiffusion
- o Maxima for sensor current density and temperature
- o For maximum head output approach these maxima as closely as possible
- o Largest head-to-head variation due to sensor height h
- o Voltage biasing allows sensor current density and temperature rise independent of h
- o Voltage biasing allows biasing closer to the limits

$\uparrow \frac{\Delta R}{R}$ & voltage senseng

MR Front-End Configurations

Biasing	***Sensing***	
	Current $\|Z_{in}\| \ll R_{mr}$	Voltage $\|Z_{in}\| \gg R_{mr}$
Current (I_B)	$\Delta I_s = \frac{\Delta R_{mr}}{R_{mr}} I_B$	$\Delta V_s = \Delta R_{mr} I_B$
Voltage (V_B)	$\Delta I_s = -\frac{\Delta R_{mr}}{R_{mr}^2} V_B$	$\Delta V_s = \frac{\Delta R_{mr}}{R_{mr}} V_B$

overcorrected by $1/R_{mr}$

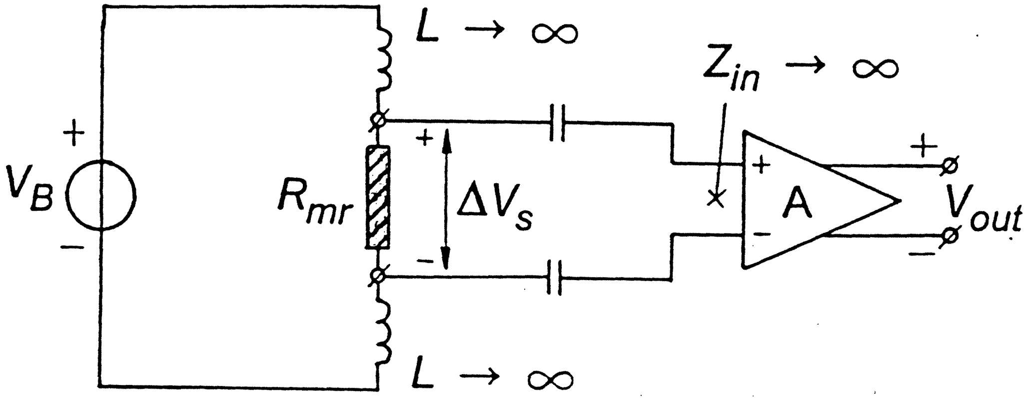
Biasing

"Constant" ≡ independent of R_{mr}

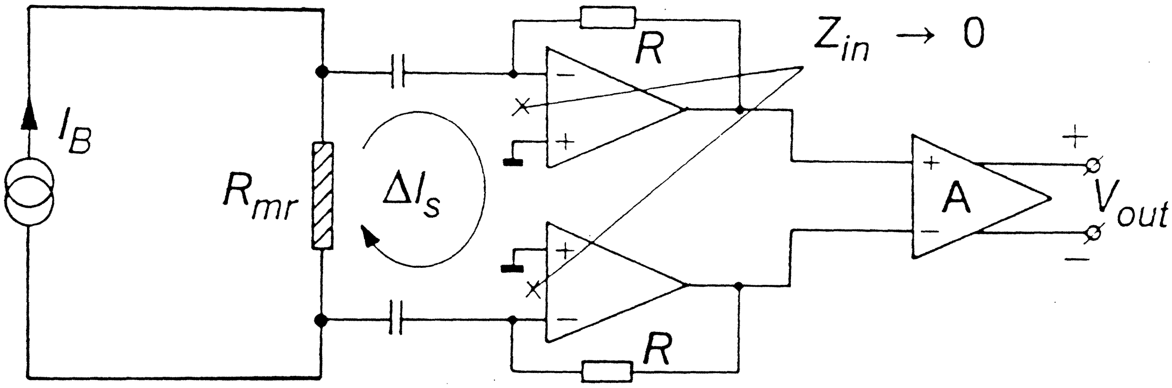
Constant Current (I_B)	Constant Voltage (V_B)
Sensor Current Density:	
$J_c = I_B \frac{1}{t\boxed{h}}$	$J_v = V_B \frac{1}{\rho l}$
Sensor Power Dissipation	
$P_c = I_B^2 R_{mr} = I_B^2 \rho \frac{l}{t\boxed{h}}$	$P_v = V_B^2 \frac{1}{R_{mr}} = V_B^2 \frac{1}{\rho} \frac{t\boxed{h}}{l}$
Sensor Temperature Rise:	
$\Delta T_c = P_c \times R_{thermal}$	$\Delta T_v = P_v \times R_{thermal}$
$\Delta T_c = I_B^2 \frac{\rho l}{th} \times \frac{gK}{2lh}$	$\Delta T_v = V_B^2 \frac{th}{\rho l} \times \frac{gK}{2lh}$
$\Delta T_c = I_B^2 \rho K \frac{g}{2t\boxed{h^2}}$	$\Delta T_v = V_B^2 \frac{K}{\rho} \frac{gt}{2l^2}$

no h dependence
so max. current
density

Paradox Illustration



Biasing	Sensing	Sensitivity Equation
V_B	ΔV_s	$V_{out} = \frac{\Delta R_{mr}}{R_{mr}} V_B A$



Biasing	Sensing	Sensitivity Equation
I_B	ΔI_s	$V_{out} = -\frac{\Delta R_{mr}}{R_{mr}} I_B R A$

MR Front-Ends

— *Differential Output Configuration*

Output signal is differentially coupled to the drive's circuit board.

- o $Z_{out} = Z_{trans.line}$ for bandwidth
- o High Z_{out} when not reading

  Smaller write-read recovery transients

  (AC coupling caps remain charged during sector servoed writing)

  Hardwired multiplex of modules into single port

- draw mre
current & freq,
varies

C - Amplifier Configurations

— *Differential Input Configuration*

Pre-amplifiers with a differential input exhibit high CMRR and PSRR; are more interference robust.

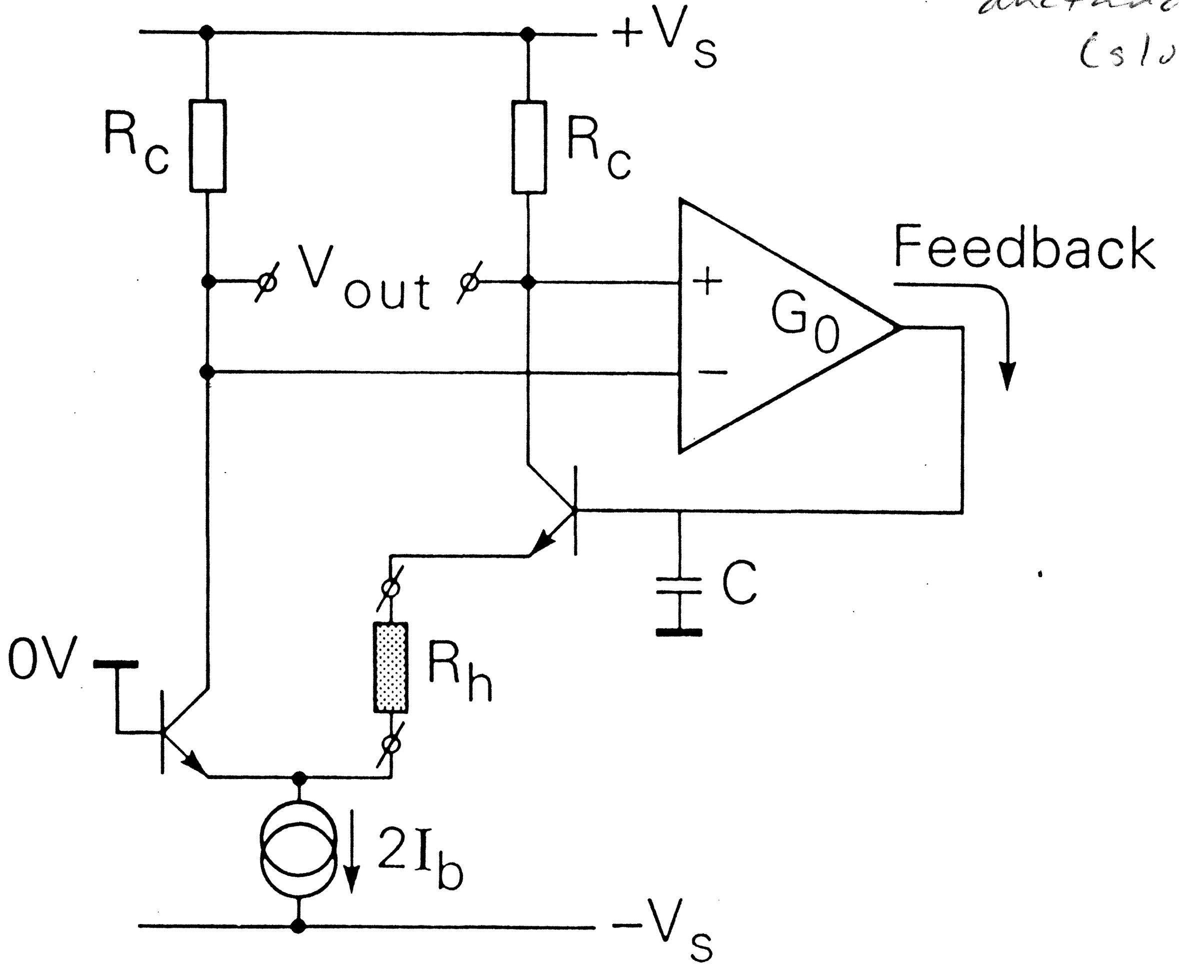
- o MR-to-disk potential must be zero
- o Dual power supply needed
  (DC-to-DC convertor: 80 % power efficiency, needle impulse interference, filter components)
- o Floating Disk Enclosure (Only AC grounded)
  1. Pre-amplifier biases DE at head potential
  2. DE is held at fixed DC potential, pre-amplifier biases heads at this potential.
     Needs fail safe: Customer shorting DE to ground automatically shuts off bias to MR heads

— *Single-Ended Input Configuration*

One input terminal is (virtually) grounded. No CMRR; lower PSRR.

- o Smaller package, common ground
- o Single supply voltage
- o MR head one side grounded

To not cause interference problems the DE must be designed as a *"cage of Faraday"*



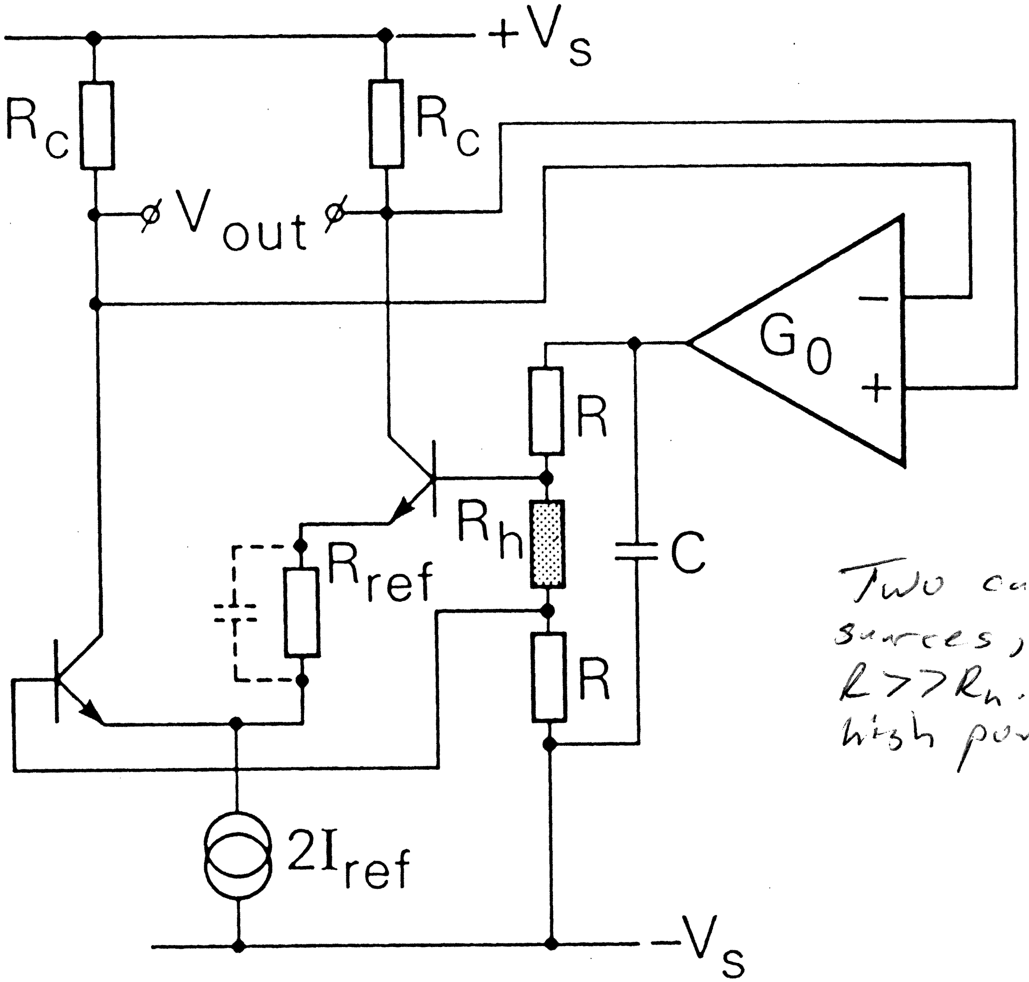
Operational Transconductance Amp.
(slowly varying)

Signal freq's
- short circuit
DC - adjusts

MR Front-Ends

D - Basic Design Examples

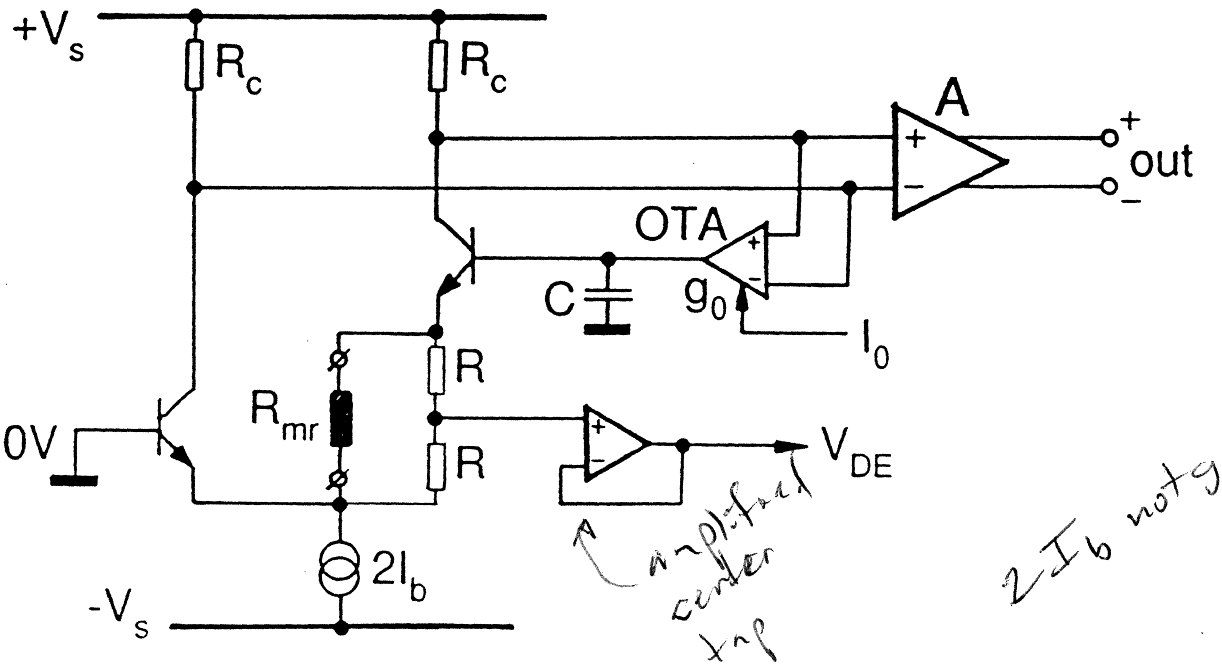
- Differential/Single Ended
- Voltage/Current Biasing
- Voltage/Current Sensing
- Comments



Two current sources, large $R >> R_h$. Needs high power.

Biasing	Sensing	Sensitivity Eqn.
$V_B = I_{ref}R_{ref}$	ΔV_s	$V_{out} = 2\frac{\Delta R_{mr}}{R_{mr}} V_B \frac{R_c}{R_{ref}}$

Dual power-supply approach (Cornell 70d)



amplified center tap

2Ib not good.

Biasing	Sensing	Sensitivity Equation
I_B	ΔI_s	$V_{out} = 2\dfrac{\Delta R_{mr}}{R_{mr}} I_B A R_c$

MR sensor in ll w/input stage bias.

Self bias

Biasing	Sensing	Sensitivity Equation
I_B	ΔI_s	$V_{out} = 2 \frac{\Delta R_{mr}}{R_{mr}} I_B A R_c$

Comments:

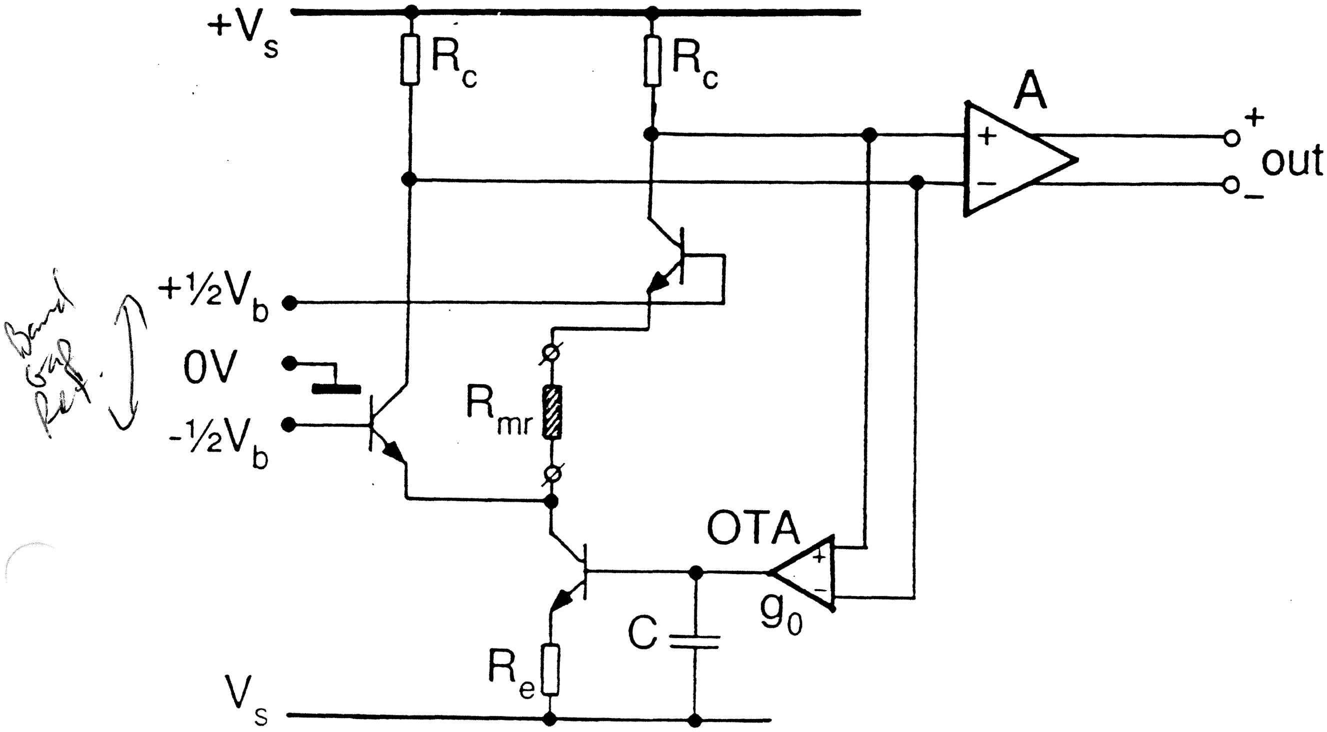
- Differential input
- High CMRR possible
- Lowest possible sensor-disk potential
- Needs dual power supply and $2I_B$
- Low-frequency band end:

$$f_{-3dB} = \frac{1}{2\pi} \frac{2g_o R_c}{C R_{mr}}$$

- Settling time upon head switch:

$$\Delta t = C \frac{\Delta V_B}{I_{OTA,max}}$$

- Fast settle mode (enlarge I_o into OTA)
- f_{-3dB} will move up proportionally

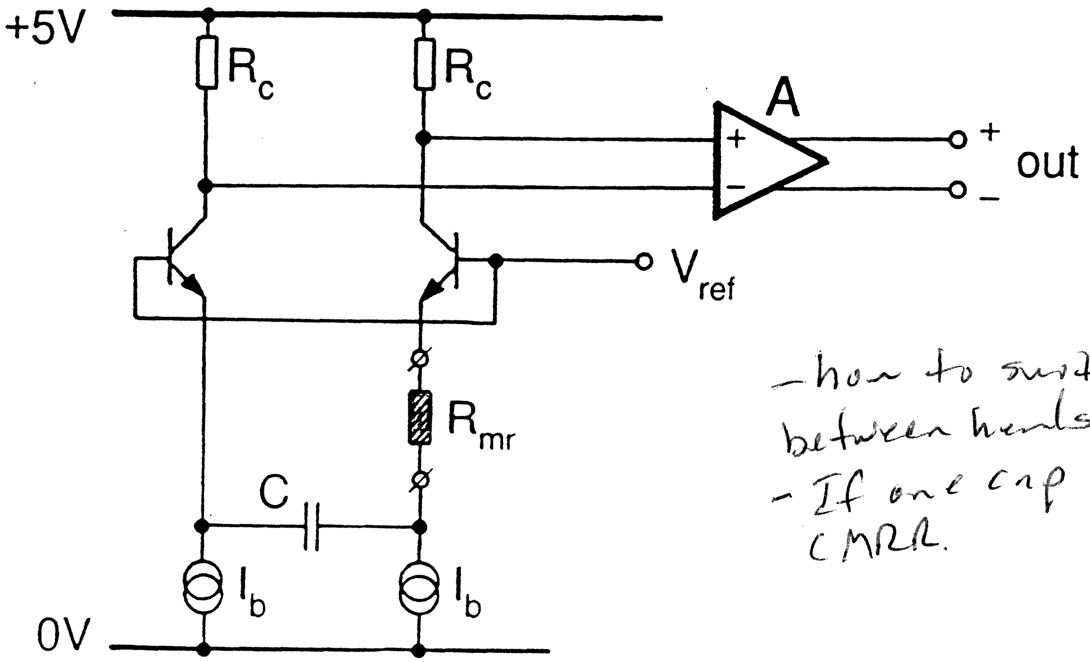


Biasing	Sensing	Sensitivity Equation
V_B	ΔI_s	$V_{out} = 2\frac{\Delta R_{mr}}{R_{mr}^2} R_c A$

Biasing	Sensing	Sensitivity Equation
V_B	ΔI_s	$V_{out} = \frac{\Delta R_{mr}}{R_{mr}^2} 2R_c A$

Comments:

- Dual supply needed
- Differential; high CMRR
- Current drain: $2I_B$
- Output proportional to $\frac{\Delta R_{mr}}{R_{mr}^2}$



- how to switch between heads?
- If one cap lost CMRR.

Biasing	Sensing	Sensitivity Equation
I_B	ΔI_s	$V_{out} = 2 \dfrac{\Delta R_{mr}}{R_{mr}} I_B R_c A$

Biasing	Sensing	Sensitivity Equation
I_B	ΔI_s	$V_{out} = \frac{\Delta R_{mr}}{R_{mr}} I_B 2 R_c A$

Comments:

- AC-coupled version of previous circuit
- Does not need feedback loop
- Current drain: $2I_B$
- Settling time:

$$\Delta t = C \frac{\Delta V_B}{I_B} = C(R_{mr,max} - R_{mr,min})$$

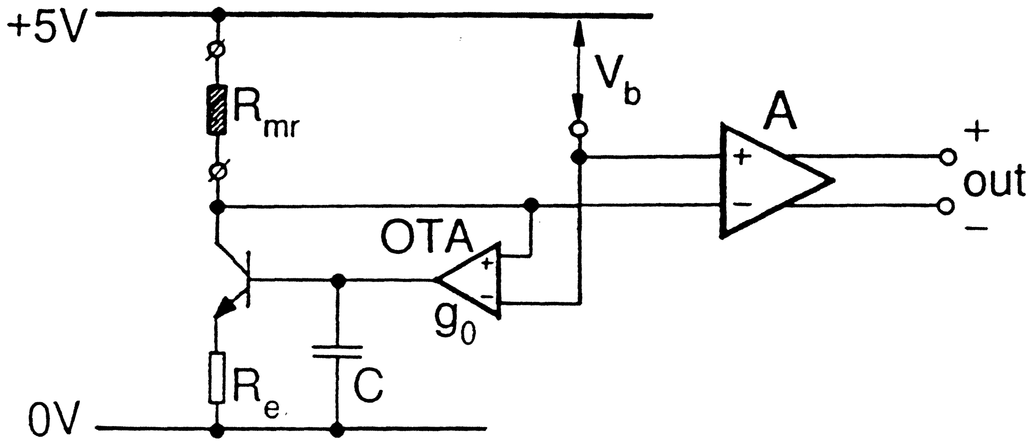
switch between heads

- Low-frequency band end:

$$f_{-3dB} = \frac{1}{2\pi C R_{mr}}$$

Single Ended Supply

Float MR @ + power supply voltage - not good!



Biasing	Sensing	Sensitivity Equation
V_B	ΔV_s	$V_{out} = \frac{\Delta R_{mr}}{R_{mr}} V_B A$

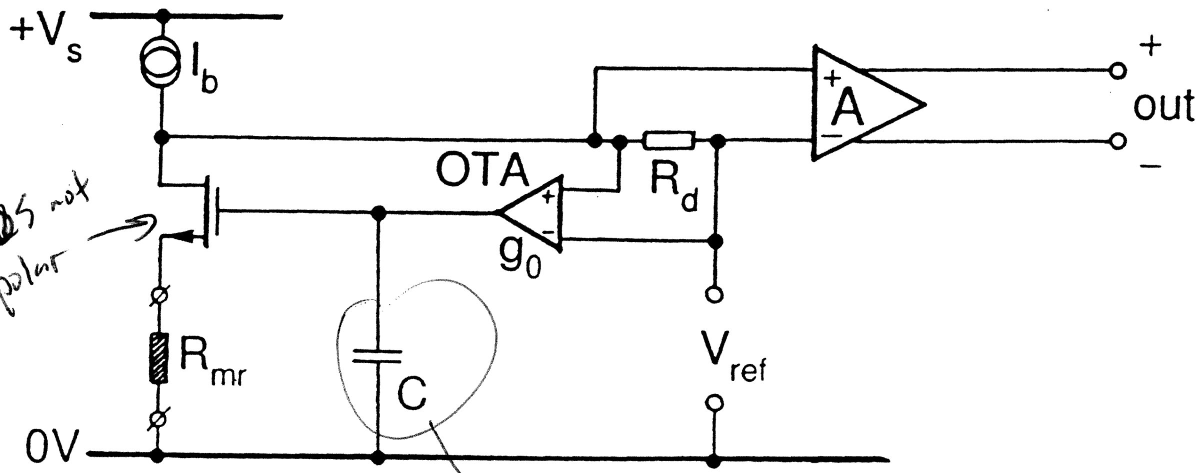
Biasing	Sensing	Sensitivity Equation
V_B	ΔV_s	$V_{out} = \dfrac{\Delta R_{mr}}{R_{mr}} V_B A$

Comments:

- MR sensor at +5V!
  - Conductive asperities
  - Flash-overs
- Bias entire Disk Enclosure at +5V
  - Customer induced shorts
  - Detect/monitor DE potential
- Low-frequency band end:

$$f_{-3dB} = \frac{1}{2\pi} \frac{g_o R_{mr}}{C R_e}$$

one lead of sensor ~~t~~tied to ground.



MOS not bipolar

large so discrete component w/extra parasitics

Biasing	Sensing	Sensitivity Equation
I_B	ΔI_s	$V_{out} = \dfrac{\Delta R_{mr}}{R_{mr}} I_B A R_d$

Biasing	Sensing	Sensitivity Equation
I_B	ΔI_s	$V_{out} = \frac{\Delta R_{mr}}{R_{mr}} I_B A R_d$

Comments:

- Single-ended input
  - No CMRR
  - Sensitive to interference pick up
  - Use Disk Enclosure as Faraday Cage

no clock into disk enclosure, no glitches fed in.

- Low-frequency band end:

$$f_{-3dB} = \frac{1}{2\pi} \frac{g_o R_d}{C R_{mr}}$$

- Dependent on R_{mr}
- Parasitic capacitance of OTA loop and other head input circuits

Parasitic Impedances

MR head is a non-self-generating transducer; it needs an electrical bias to operate

- Bias causes a DC voltage across the head ($R_{MR} \simeq 25\Omega$, $I_{Bias} \simeq 10$ mA $\rightarrow V_{MR} \simeq 250$ mV)
- V_{MR} too large to apply DC-coupled gain
- Need AC coupling/by-pass capacitor in input stage

Parasitic Impedances

The AC coupling/by-pass capacitor is afflicted with parasitics (R_s, L_s) and also the head-to-electronics leads (R_l, L_l, C_l).

These parasitics can:

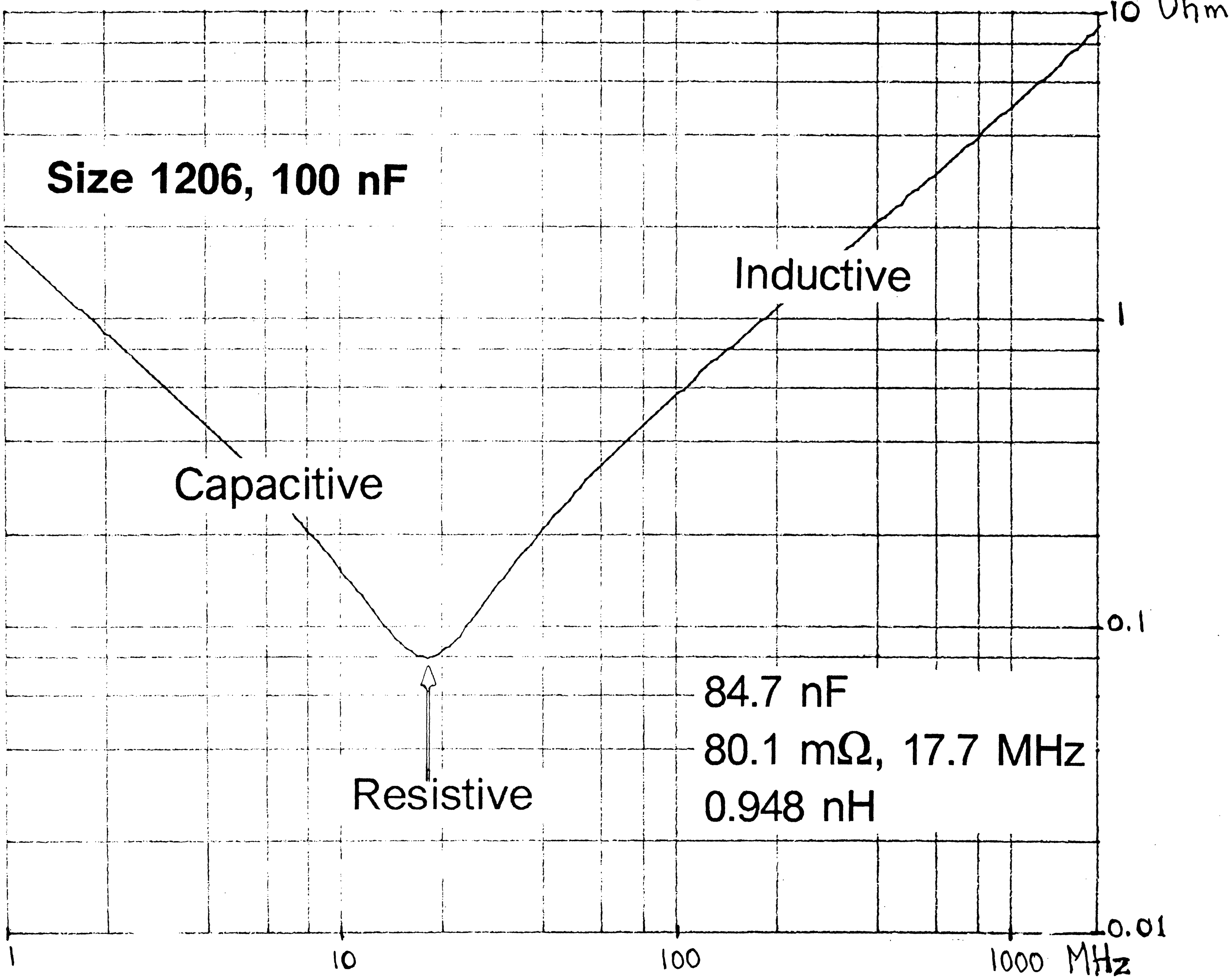
— reduce the available gain and bandwidth

— increase the electronics noise

— endanger the MR bias loop stability

Close proximity, good capacitors with short thick wide leads are required

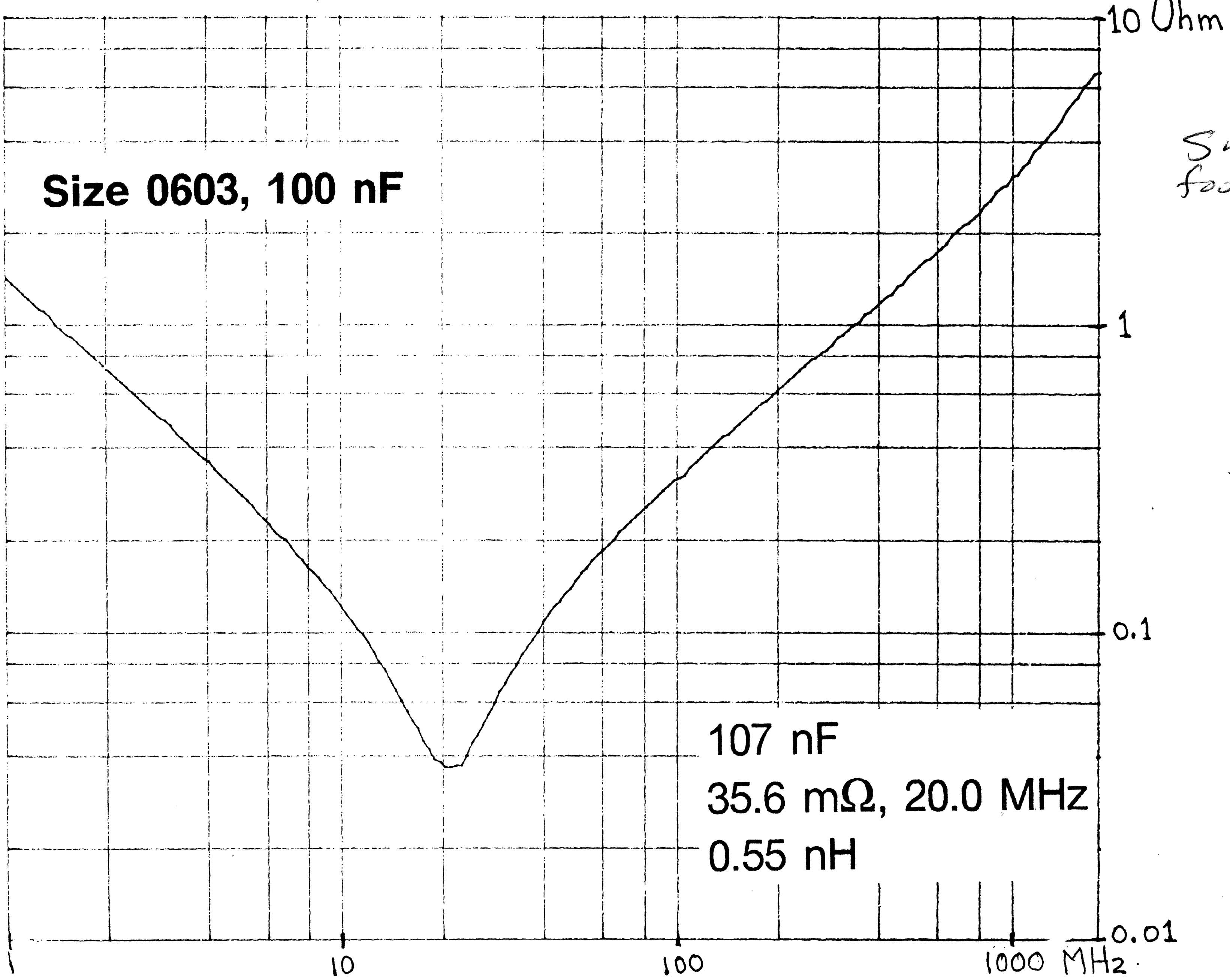
Surface-Mount Capacitors



Size 1206, 100 nF

84.7 nF
80.1 mΩ, 17.7 MHz
0.948 nH

Surface-Mount Capacitors

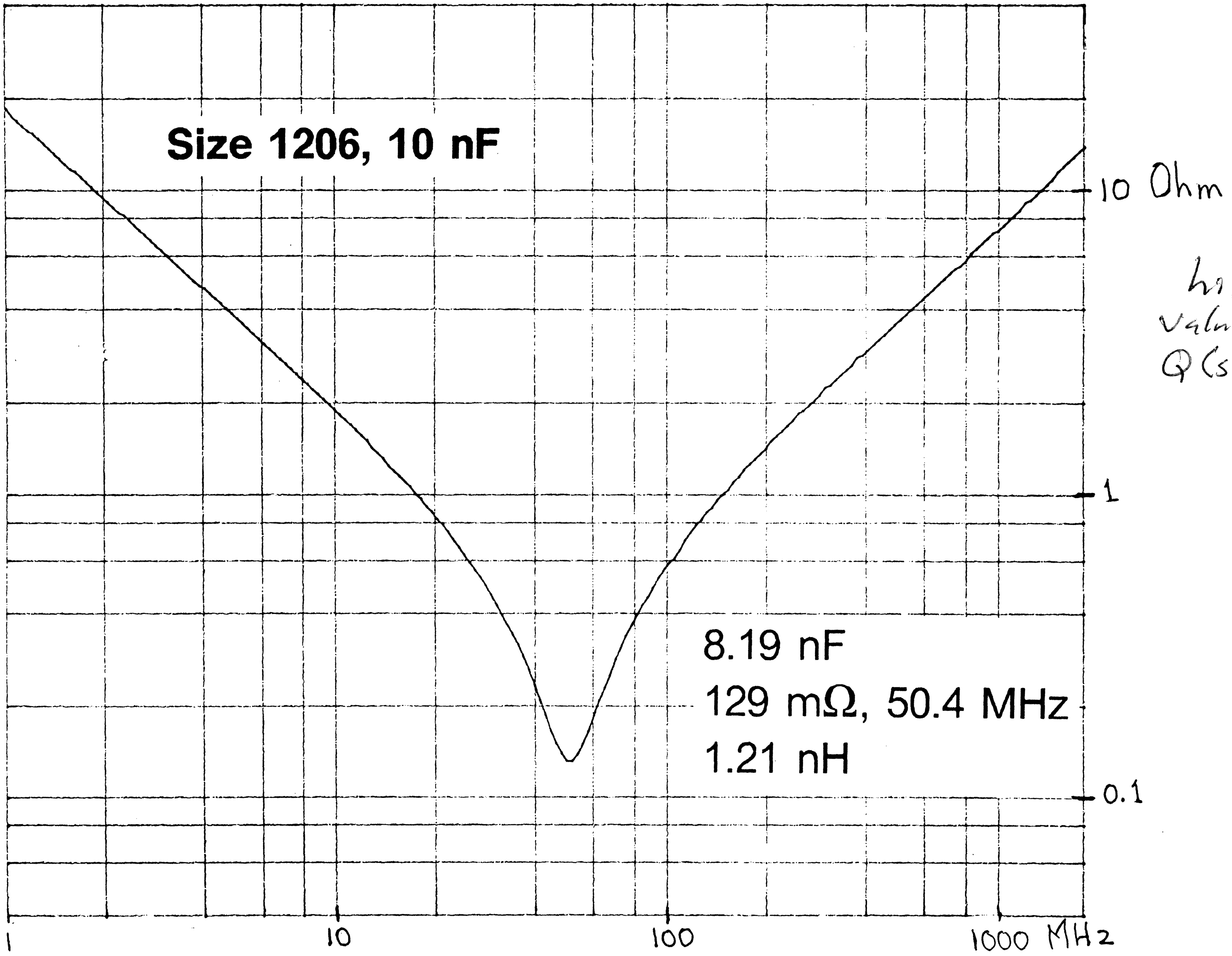


Size 0603, 100 nF

107 nF
35.6 mΩ, 20.0 MHz
0.55 nH

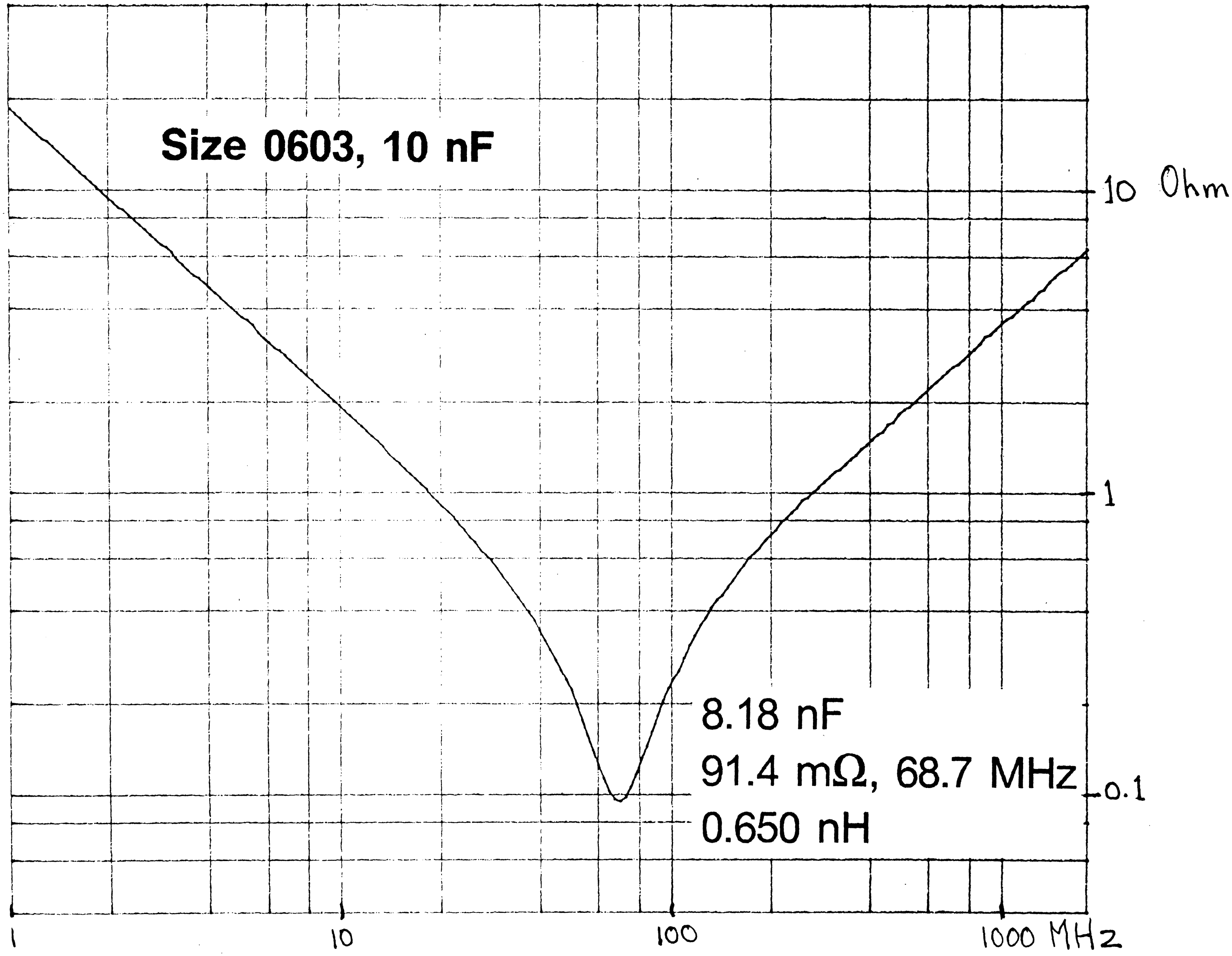
Smaller foot print

Surface-Mount Capacitors

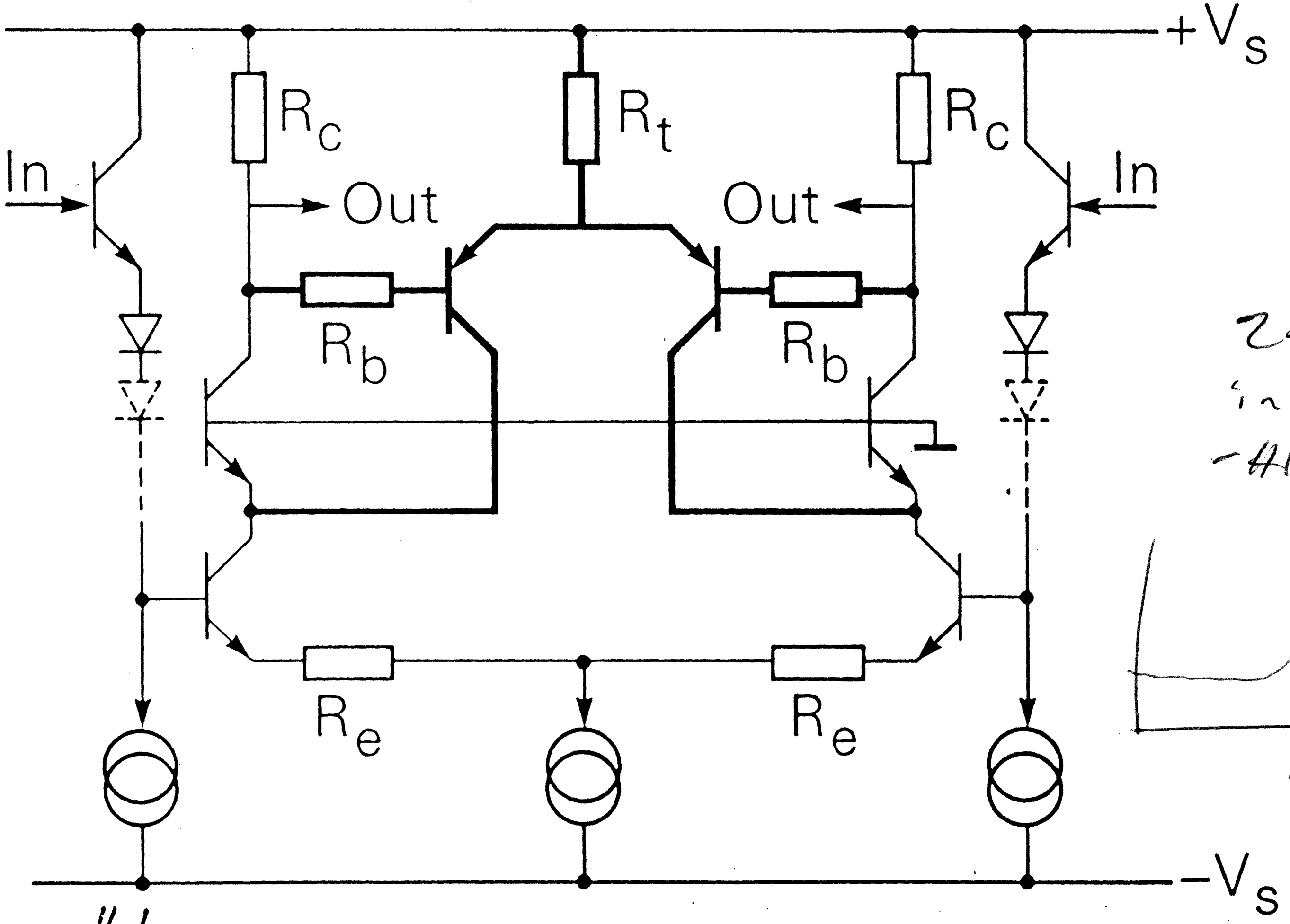


higher values, higher Q (sharper)

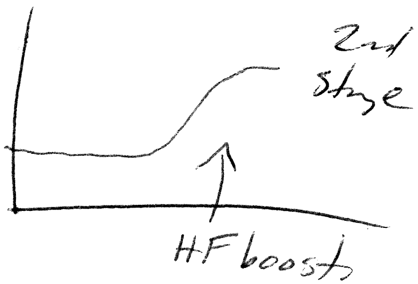
Surface-Mount Capacitors

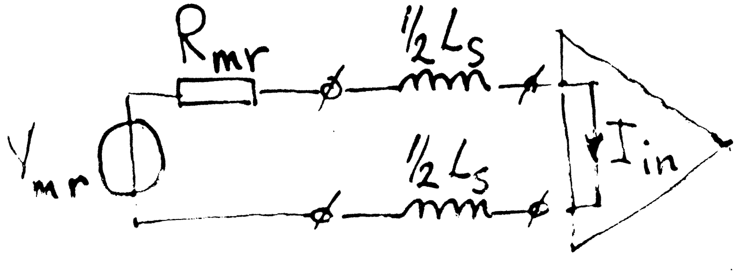


Extrinsic Gain Equalization



2nd stage
in amp.
-HF boost



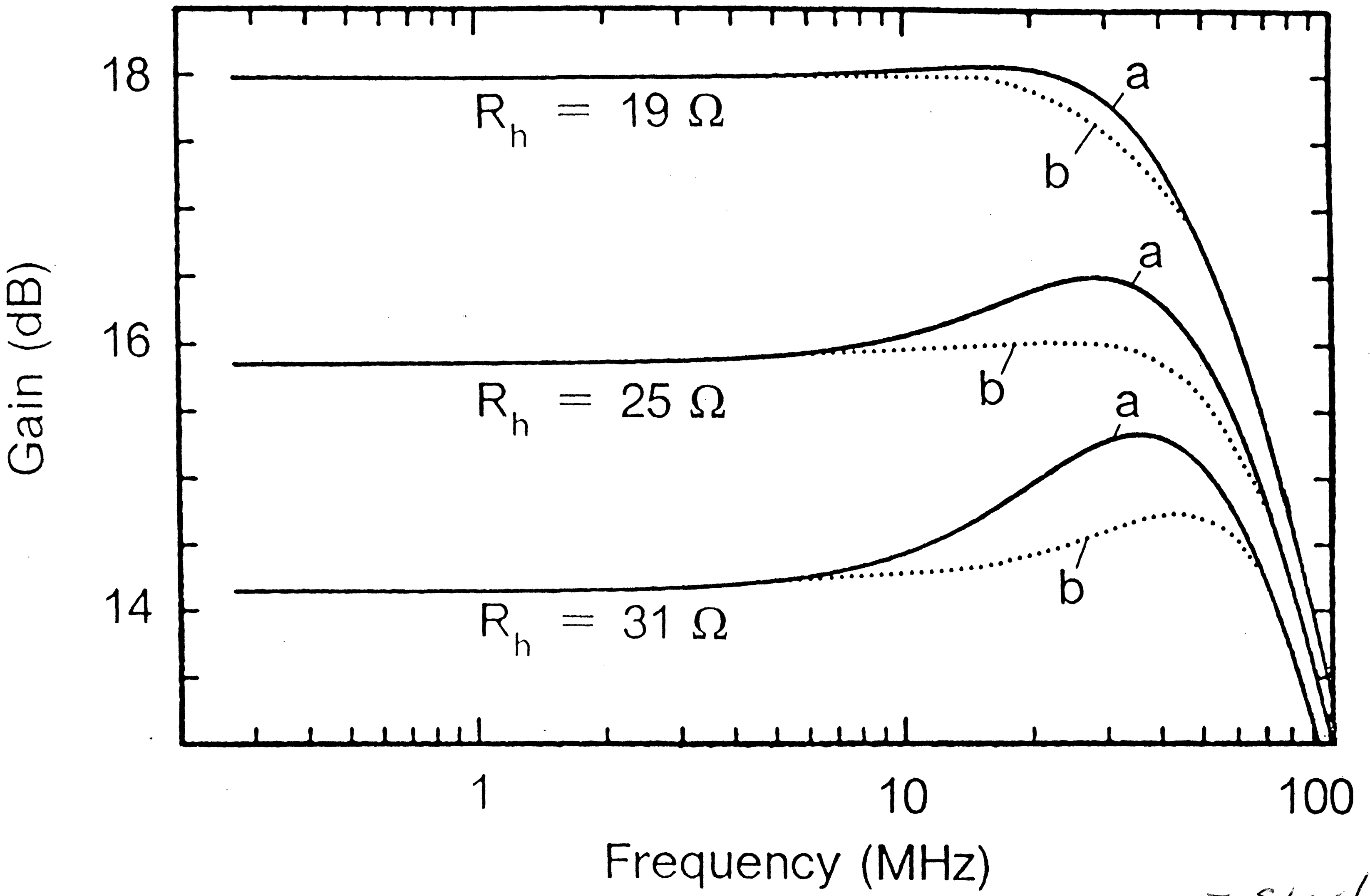


$$\cancel{f_{-3dB} = \frac{L_s}{2\pi R_{mr}}}$$

$$\tau = \frac{L_s}{R_{mr}}$$

$$f_{-3dB} = \frac{1}{2\pi}\,\frac{R_{mr}}{2\pi L_s}$$

equalize for this attenuation - boost.



Gain depends on head resistance.

a - signal from head resistance
b - with equalization

- small contribution to noise, increase in amp @ HF.

Design for Flexibility

Programmable Front-End Electronics

- Same module for different products
- Can be "fine tuned" to individual heads
  - in manufacturing
  - autonomously, when need arises (DRP)

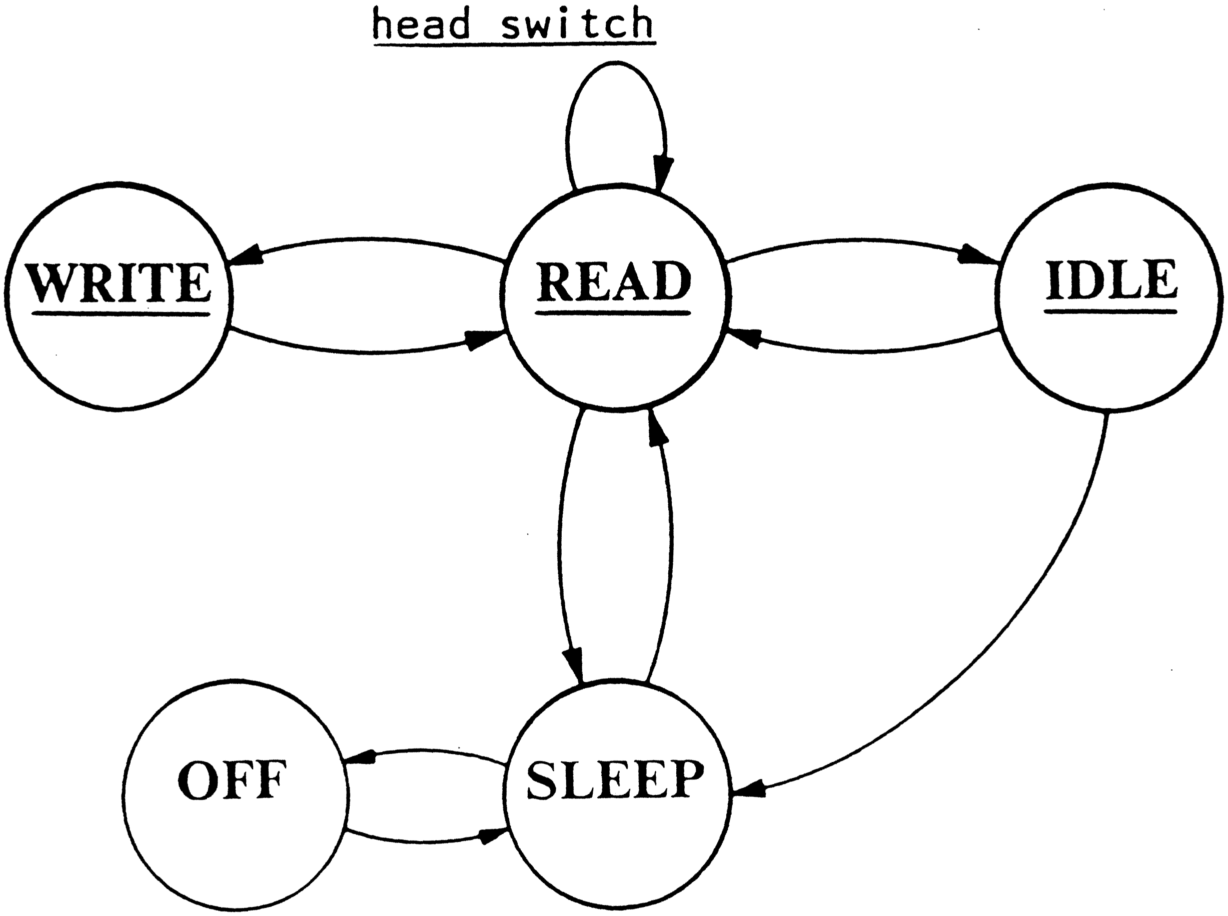
data recovery procedure, beyond ECC, e.g. increase bias.

- Easier to use in development
  (Head parameters not yet known)

Digitally programmable/addressable via serial port

- Individual MR head bias
- Individual head write current
- Write damping
- Pre-equalization (counters lead effects)
- Head select
- Servo bank writing/multi-channel servo writing
- Signal gain
- MR bias off/on/reduced during writing
- Select "modes of awareness" (sleep, idle, etc)

States of "Awareness"



1992

Higher Data Rates, Why?

Data Rate =

$$2\pi \times \frac{RPM}{60} \times \frac{Track}{Radius} \times \frac{Linear}{Density}$$

Storage Industry Trends:

$$\textbf{\textit{Latency}} = \tfrac{1}{2} \times \frac{60}{RPM} \qquad \textbf{\textit{(down)}}$$

$$\frac{\textbf{\textit{Areal}}}{\textbf{\textit{Density}}} = \frac{track}{Density} \times \frac{Linear}{Density} \qquad \textbf{\textit{(up)}}$$

Conclusion:

Data rates are forced up, unless we use smaller disks (capacity loss)

Data Rate - Bandwidth

Higher Data Rates require wider signal path bandwidths.

Toughest Requirement:

- ***Write Path Bandwidth***
  - Well-defined transitions require short write current reversal times.
  - Write bandwidth much larger than read bandwidth
  - Write head/electronics interconnection becomes important
  - Reflections, standing waves, wave shapes

Goal of Study

What limits the data rate in an "industry typical" recording channel front-end?

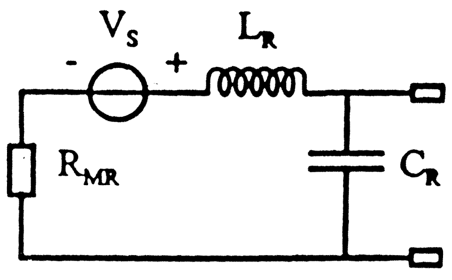
Front-End: {
Transducer
Interconnect
AE Module

"All components in the Signal Path ahead of the channel chip"

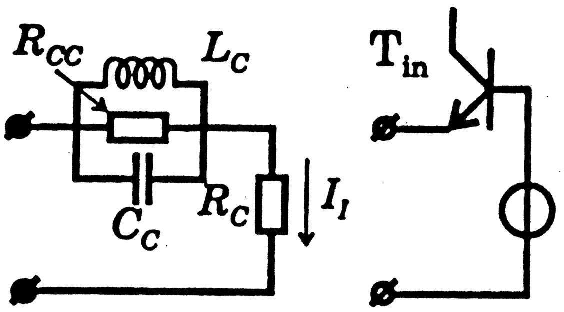
A – Read Signal Path
B – Write Signal Path

**NB: Analysis should be adequate up to 1 GHz ⇒ A detailed component description is needed

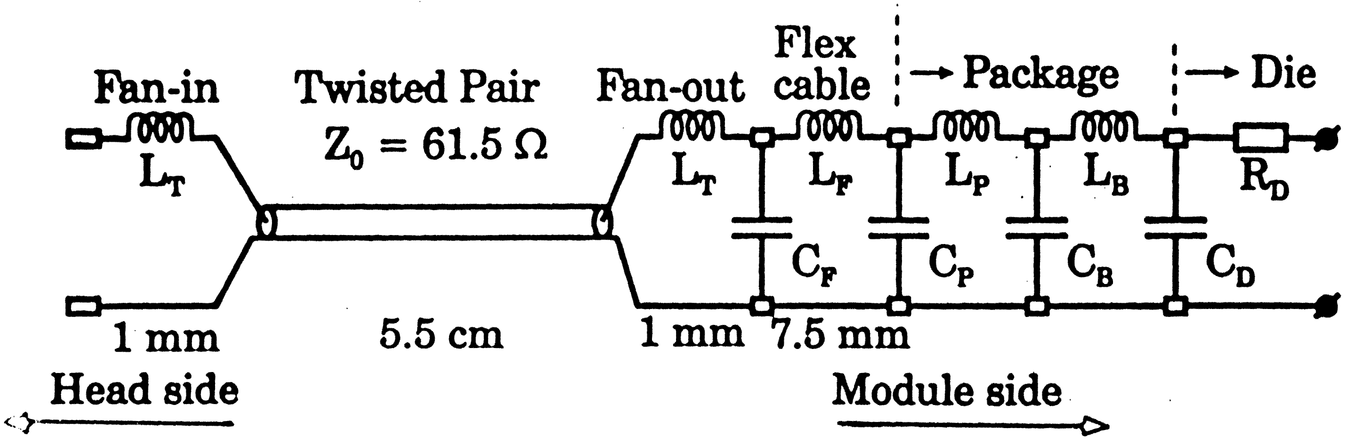
Read Channel Front End

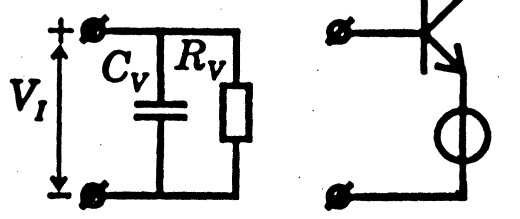


(a) MR head head



(a) Current sensing

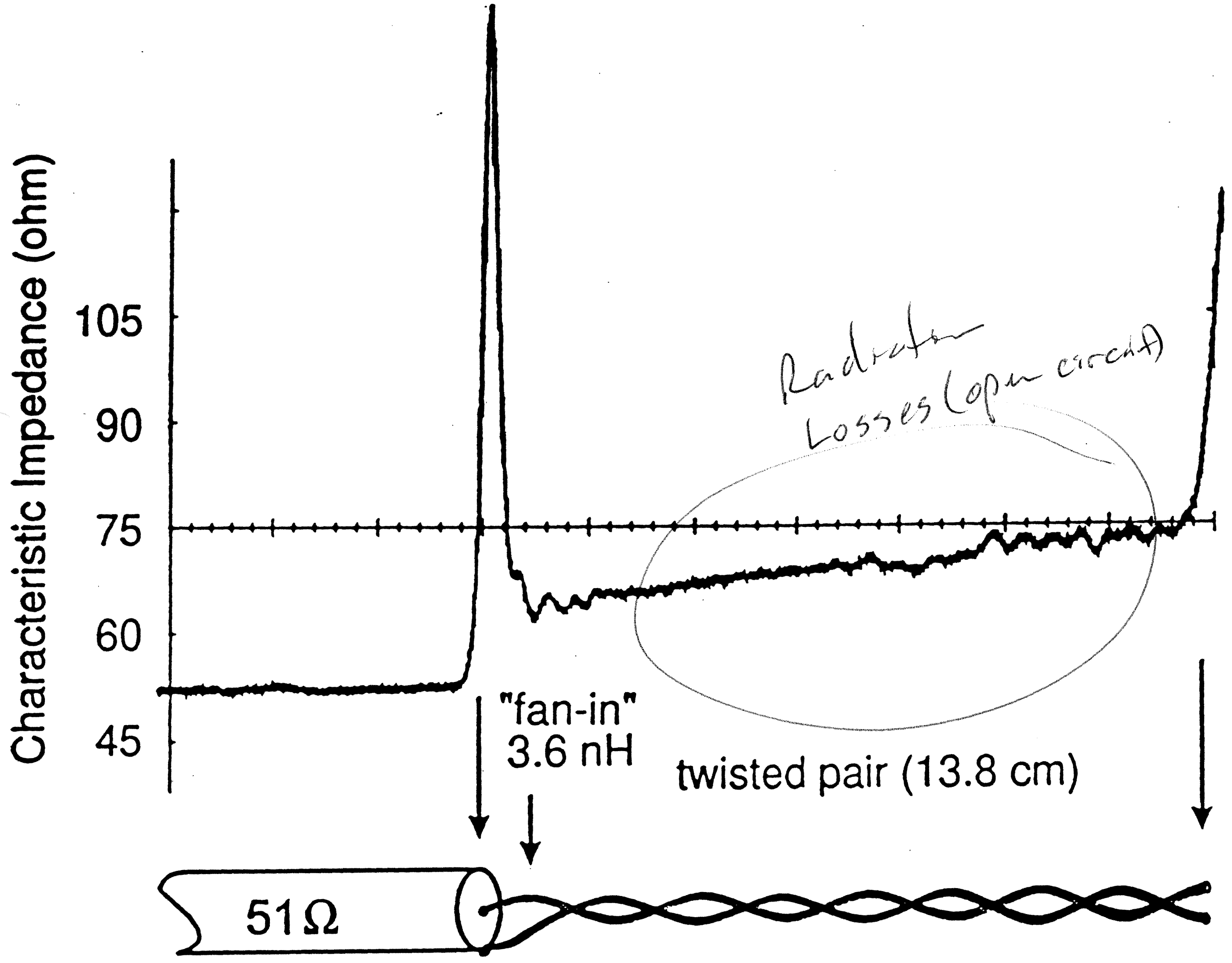




(b) Voltage sensing

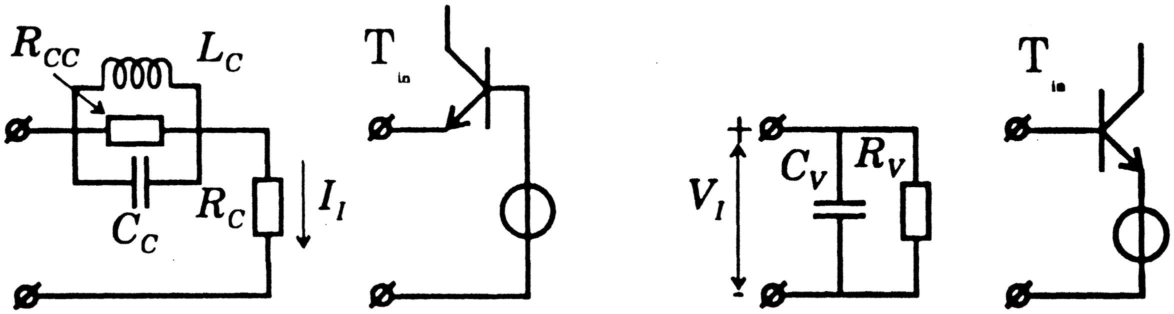
Time Domain Reflectometer

Twisted Pair Characterization



Open line so looks

Pre-amplifier input impedance models



(a) Current sensing

(b) Voltage sensing

Read Channel Parameter Values

- **MR Read Head**

  $15\,\Omega \leq R_{MR} \leq 45\,\Omega$, $L_R = 1$ nH,
  $C_R = 0.5$ pF, $V_S = I_{bias}\,\Delta R_{MR}$

- **Interconnect**

(a) Twisted Pair:

Gold-cladded copper wire, diameter 36 μm
Poly-urethane insulation, thickness 12 μm
One twist per mm, length 55 mm
$Z_0 = 61.5\,\Omega$, $v_p = 209\times10^6$ m/s, $\varepsilon_r = 2.1$, $R_S = 80.6\,\Omega$/m
Fan-in and fan-out 1 mm; $L_T = 3.6$ nH

(b) Flex cable:

Length 7.5 mm, $L_F = 15$ nH, $C_F = 0.75$ pF

(c) Package:

$L_P = 5$ nH, $C_P = 1$ pF
Bonding wire, $C_B = 0.6$ pF, $L_B = 1$ nH
Semiconductor die, $C_D = 0.5$ pF, $R_D = 0.5\,\Omega$

- **Read Pre-Amplifier**

  Single-ended input,NPN transistor area 14000 μm^2,
  $f_t = 3$ GHz, biased at 7 mA

(a) Voltage Sensing: $|Z_{in}| \gg R_{MR}$

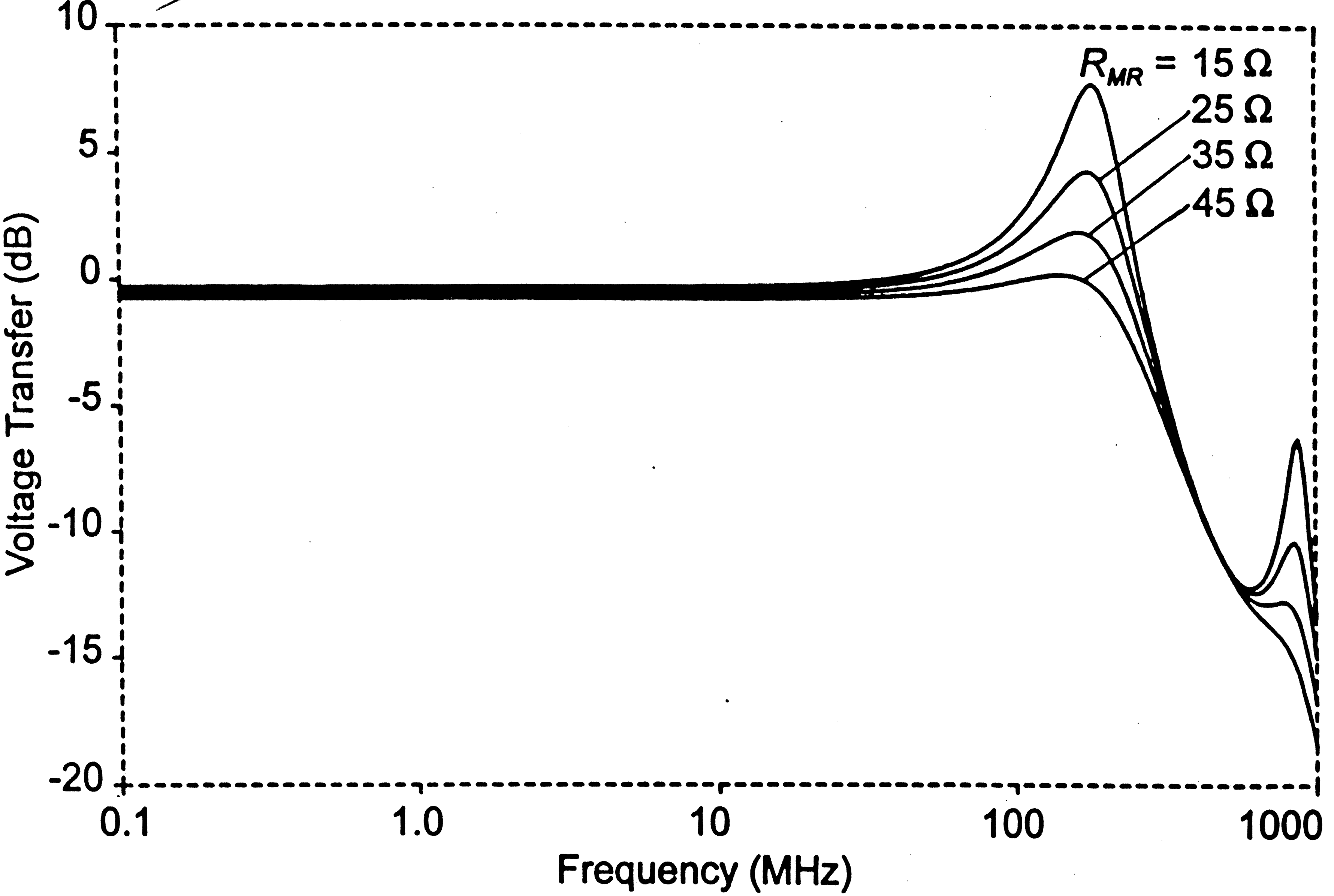
$C_V = 14$ pF, $R_V = 500\,\Omega$

(b) Current Sensing: $|Z_{in}| \ll R_{MR}$

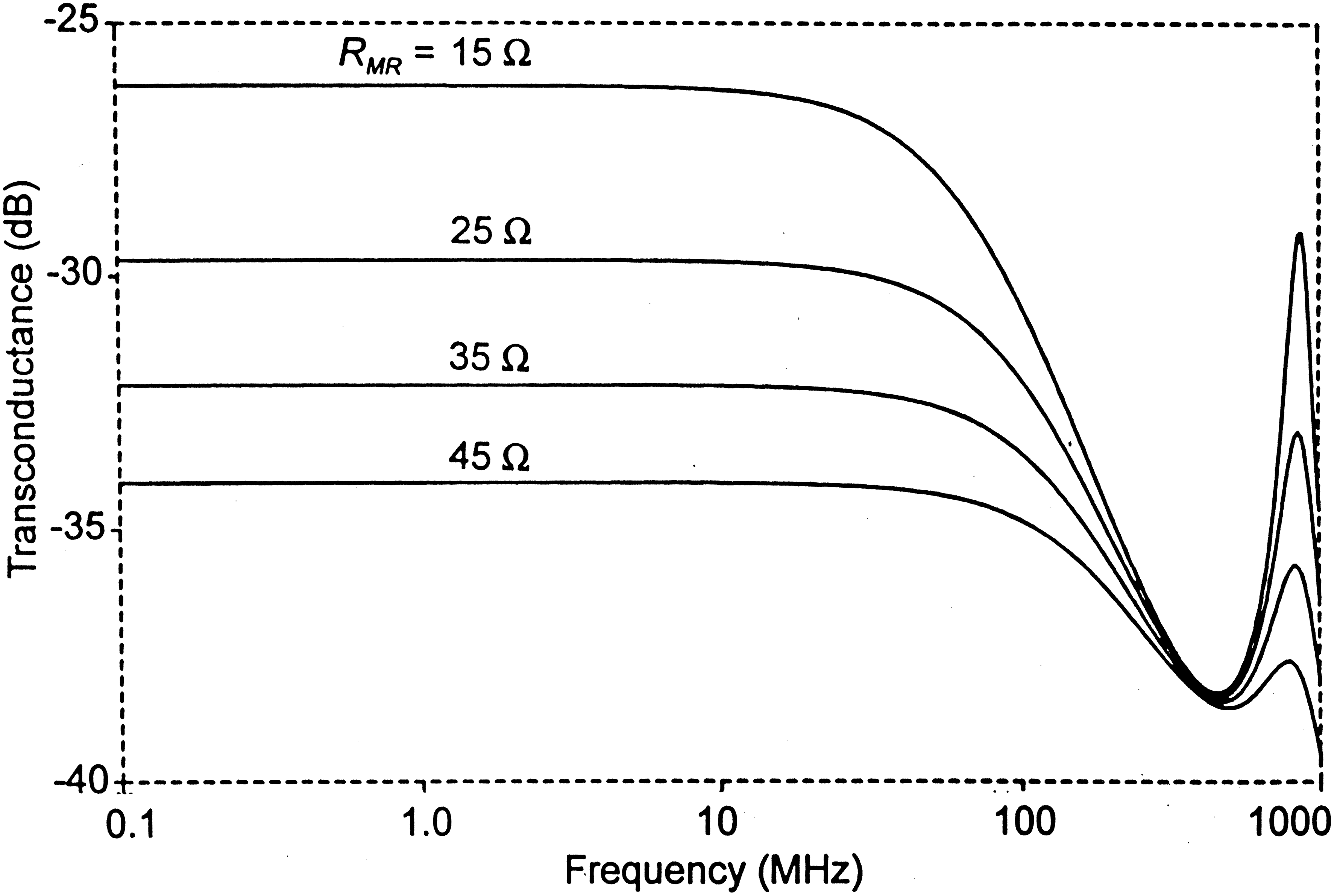
$C_C = 0.85$ pF, $R_{CC} = 3.5\,\Omega$, $L_C = 0.15$ nH, $R_C = 5\Omega$

Voltage Sensing Amp

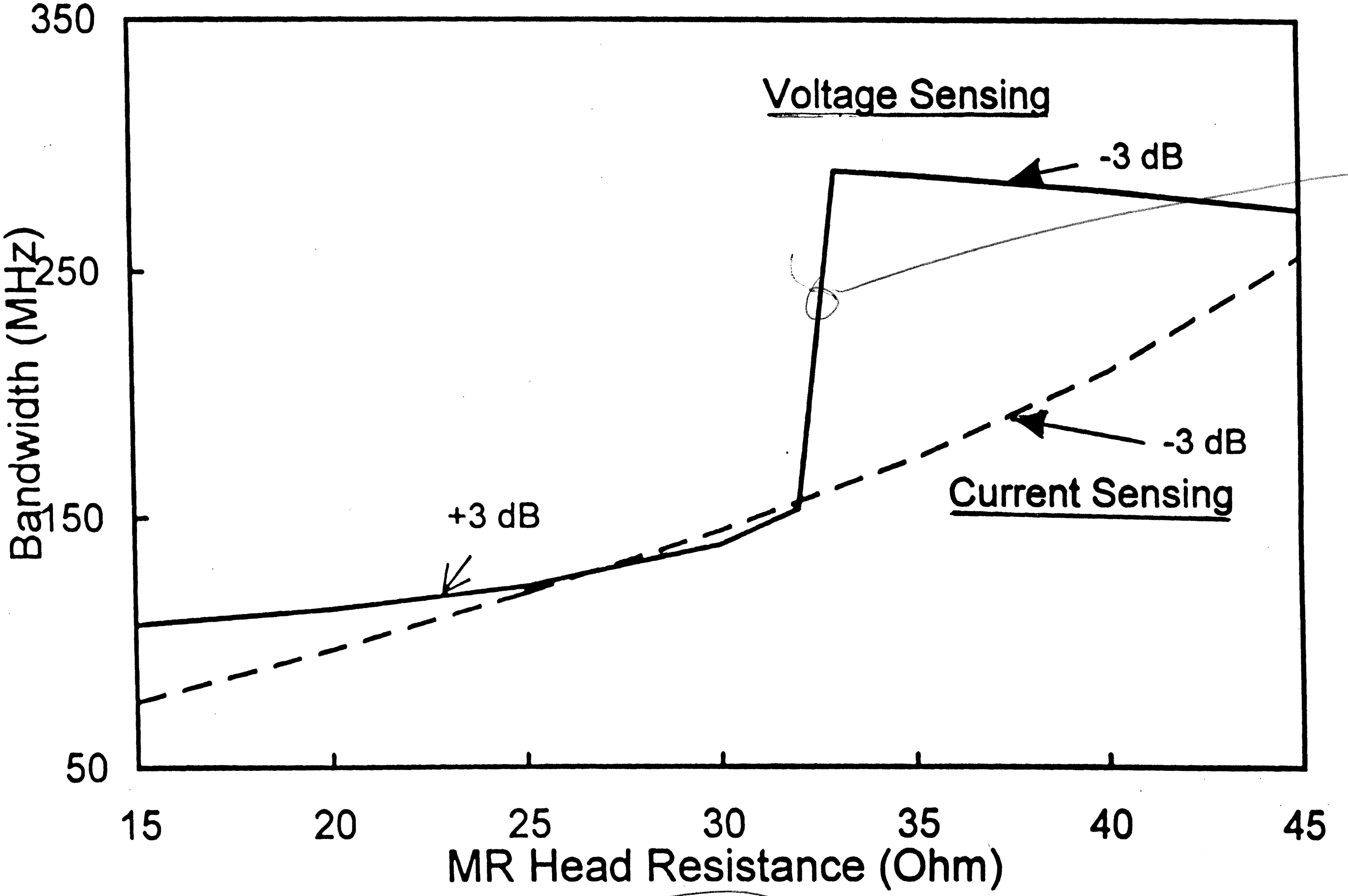
Voltage transfer across MR head to preamp input leads



Current Sensing Amp



Read Bandwidth (full front-end)



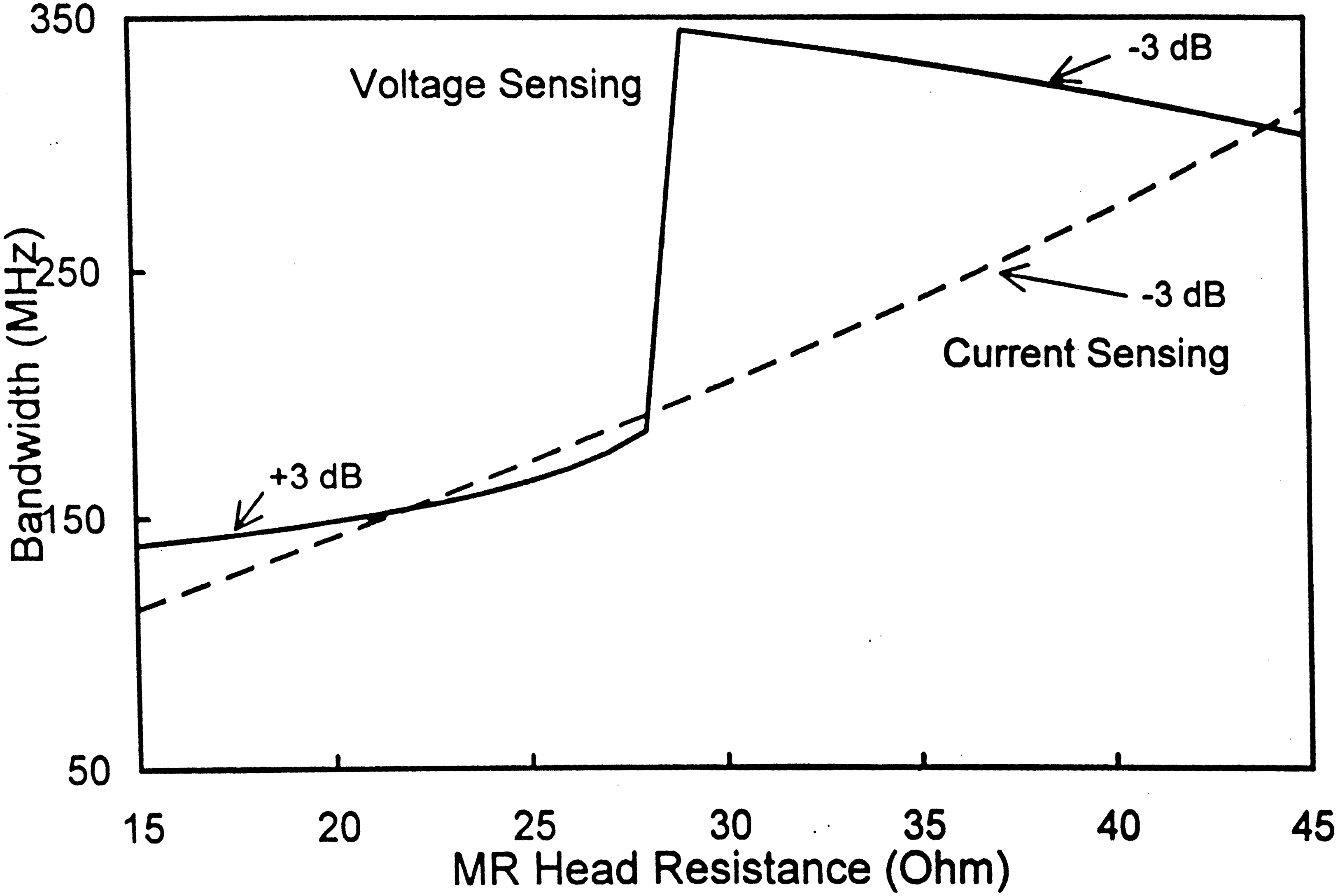
due to shape of Voltage X-fer (switch +3dB to -3dB)

~ same

voltage sensing

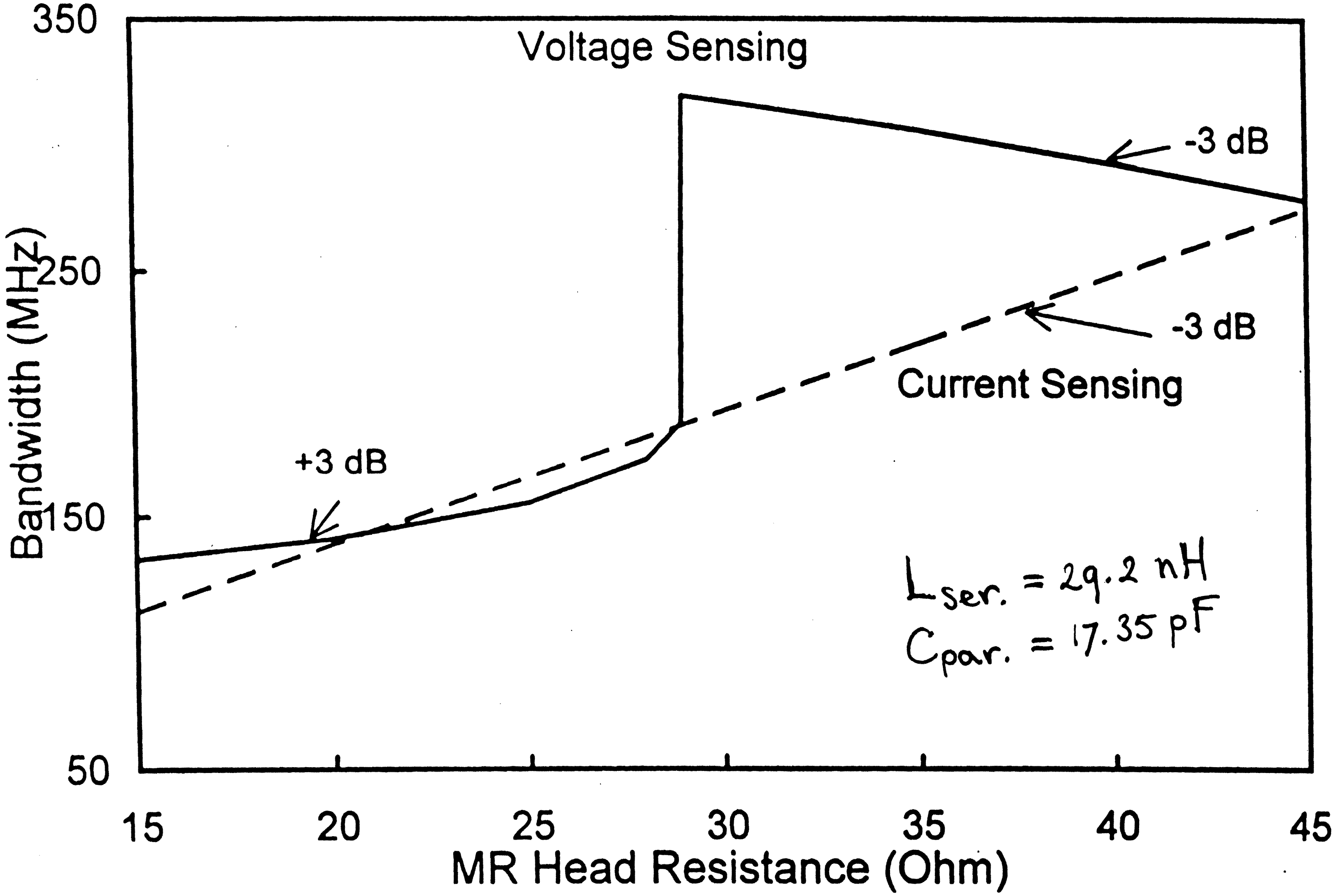
Read Bandwidth (no transmission line)

This is optomistic



Read Bandwidth (lumped approximation)

– a little less optomistic



$L_{ser.} = 29.2$ nH
$C_{par.} = 17.35$ pF

Conclusions

- **Read Path**
  - √ The bandwidth increases with increasing R_{MR}
  - √ Only for higher R_{MR} is voltage sensing better than current sensing (> 33 Ω)
  - √ Current sensing gives a better equalizable frequency response
  - √ Without transmission line the bandwidth is 50 - 75 MHz optimistic
  - √ The minimum bandwidth is 76 MHz (CS) or 108 MHz (VS)

Write Driver Dilemma

★ Limited power supply voltage: $V_s \pm x$ %
(e.g. 5V ± 10%)

★ Active devices in write driver output stage need voltage head room of ΔV when fully on.
(Bipolar devices $\Delta V \simeq 0.9$ V)

- Available peak-to-peak head voltage swing:

$$V_{h,pp} = 2\left\{V_s(1 - \frac{x}{100}) - 2\Delta V\right\}$$

- Also:

$$V_{h,pp} \simeq 2\left\{L\frac{dI}{dt} + IR\right\} = 4\frac{LI_W}{\tau_W} + 2I_W R_h$$

I_W peak-to-base write current
τ_W write current reversal time
R_h head series resistance
L inductance $(L = L_h + L_l)$

- Scaling $L_h = N^2 L_o$, $R_h = NR_o$, $I_W = MMF/N$

Write Driver Dilemma

- $V_{h,pp} = MMF\left\{\dfrac{4L_l}{N\tau_W} + \dfrac{4NL_o}{\tau_W} + 2R_o\right\}$
- Smallest when $N = \sqrt{\dfrac{L_l}{L_o}}$ $\quad (L_h = L_l)$

head ind. = wire parasitic ind.

- Minimum is:

$$V_{h,pp} = MMF\left\{\frac{8\sqrt{L_l L_o}}{\tau_W} + 2R_o\right\}$$

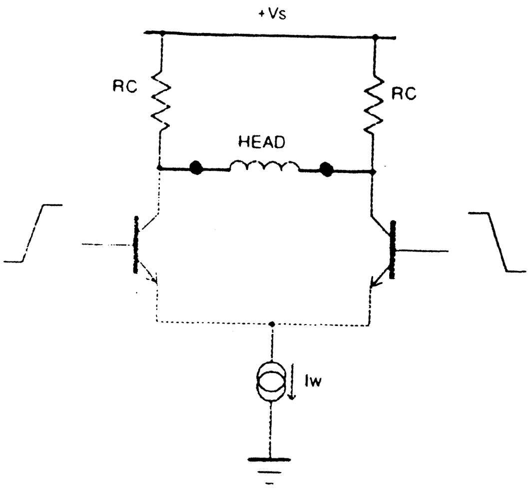
- Therefore MMF, L_l, L_o and R_o are limited to values satisfying:

$$MMF\left\{\frac{4\sqrt{L_l L_o}}{\tau_W} + R_o\right\} \leq V_s\left(1 - \frac{x}{100}\right) - \Delta V$$

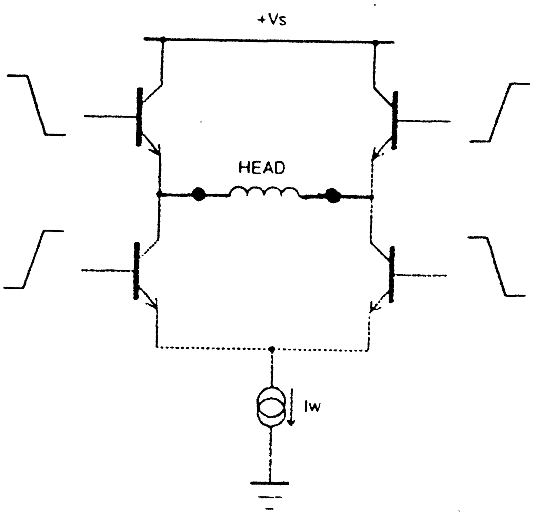
Example: Suppose $L_o = 0.8$ nH, $R_o = 1\ \Omega$, $V_s = 5$V, $x = 10\%$, $\Delta V = 0.9$V, $\tau_W = 5$ ns, $L_l = 60$ nH

- ★ We find $\boldsymbol{V_{h,pp} = 5.4\text{V}}$, $\boldsymbol{I_W = 46\text{mA}}$, $\boldsymbol{N = 9}$, $\boldsymbol{L_h = 65\text{nH}}$
- ★ For a (0,k) run-length limited code with an 8/9 code rate (where τ_W is half the closest transition spacing), we find a maximum data rate of **11.1 MB/s**

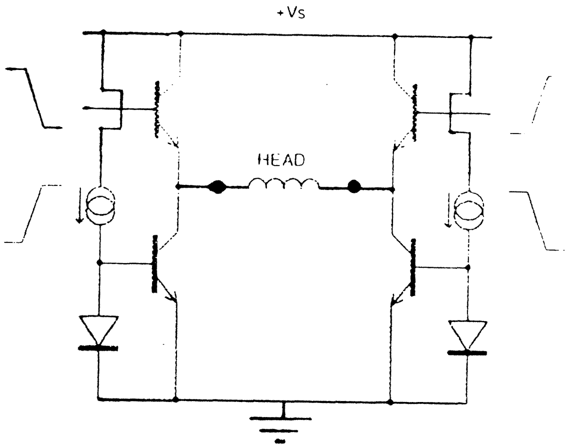
Write Driver Topologies



Power Inefficient
Poor Headroom

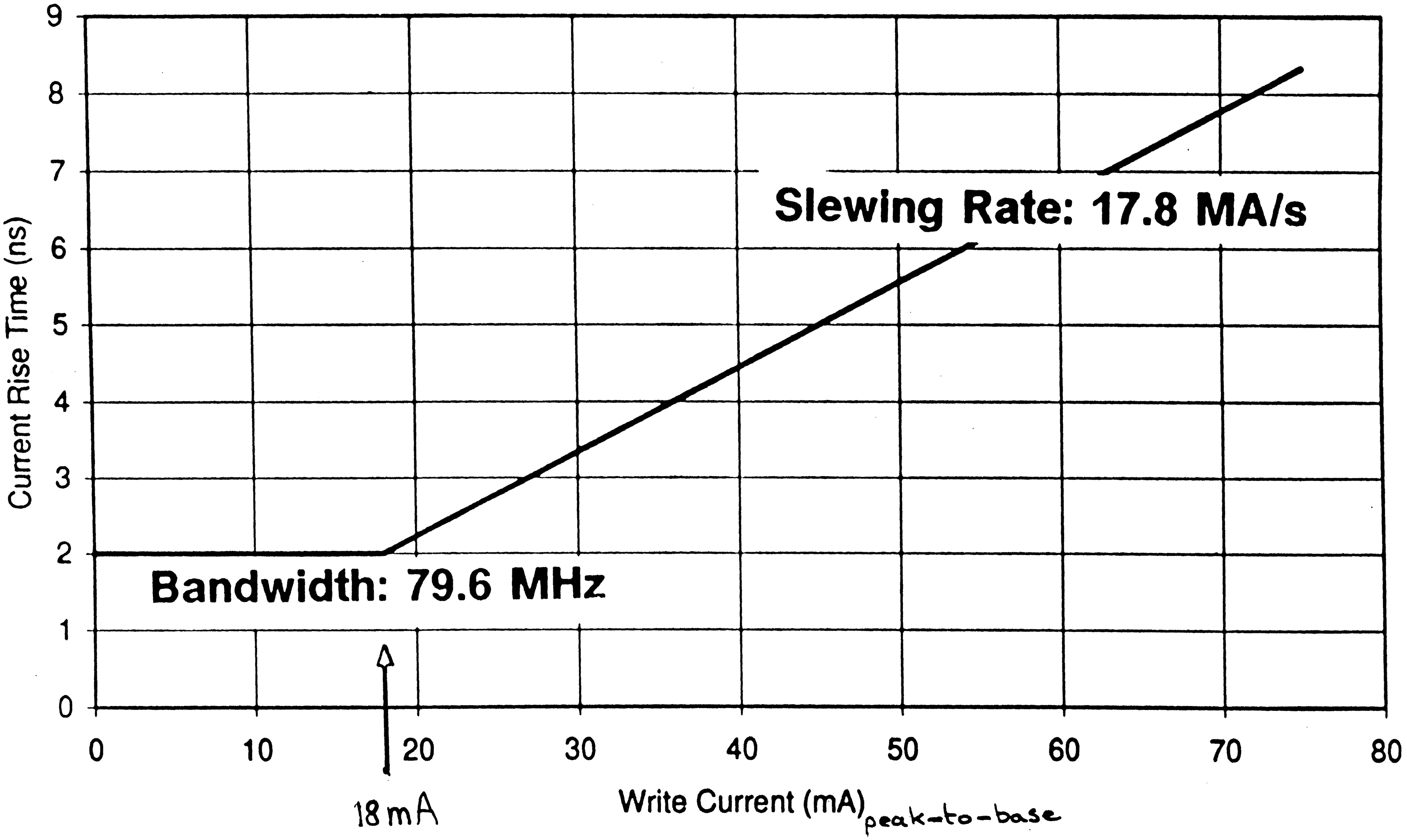


Power Efficient
Poor Headroom

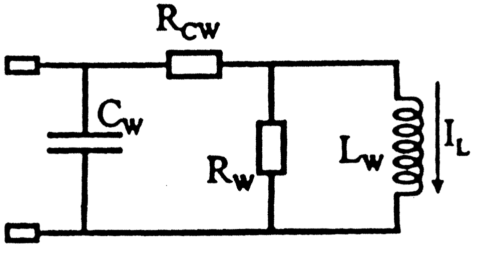


Power Efficient
Good Headroom

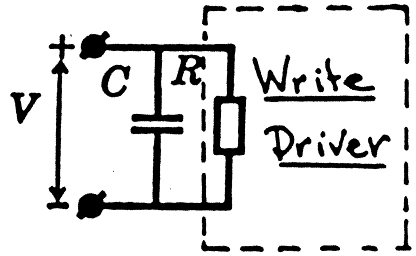
Write Driver Output

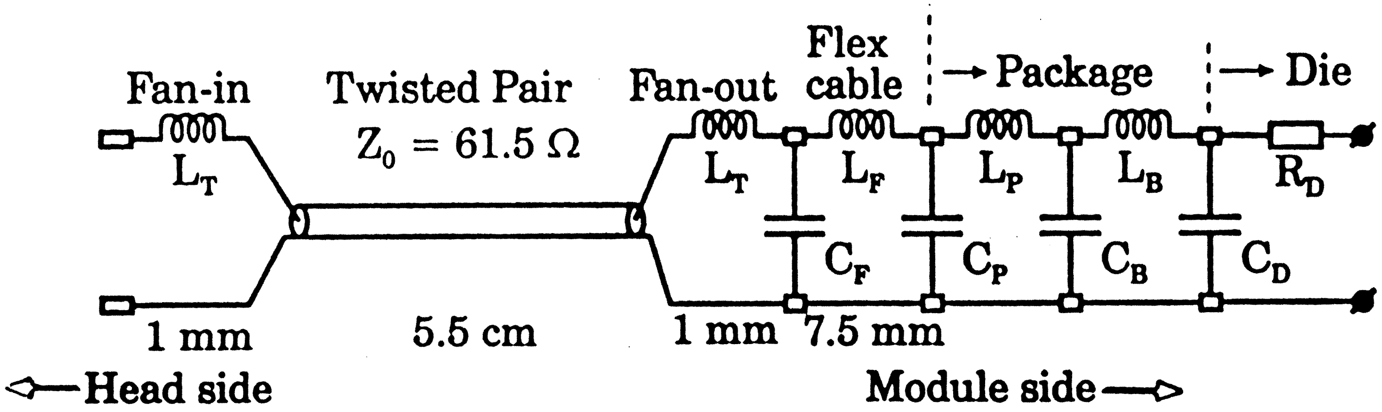


Write Channel Front End

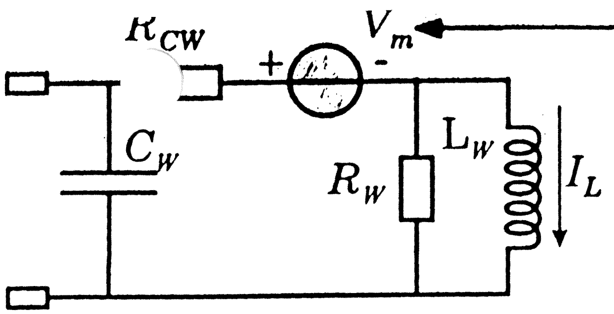


(b) Thin-film write head



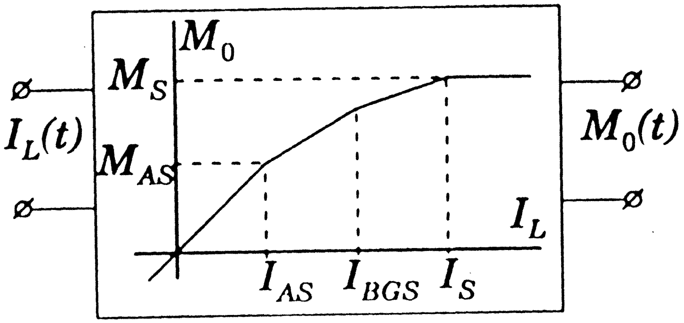


Write Head Model



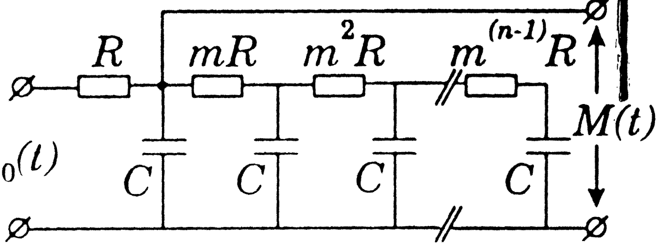
(a) Write Head Coil

$$V_m = \mu_0 NA \frac{dM(t)}{dt}$$



← measured externally

(b) I_L to M_0 Conversion

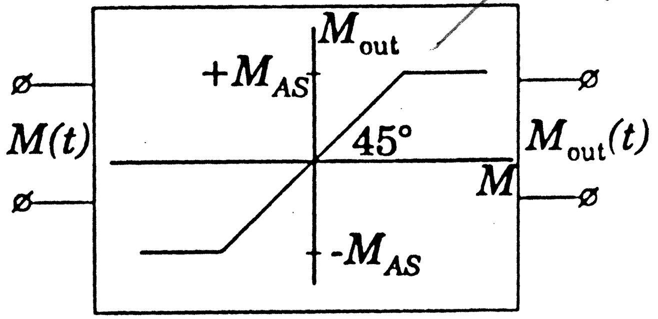


← Low Pass Filter

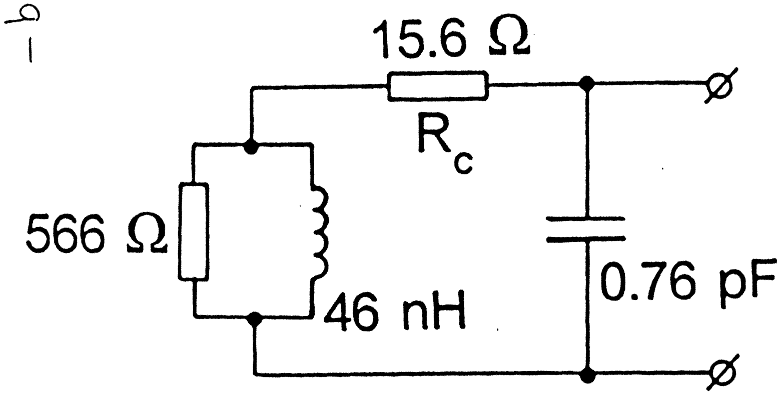
$\tau_1 = RC$ $\tau_n = m^{(n-1)}\tau_1$

(c) Eddy Current Filter

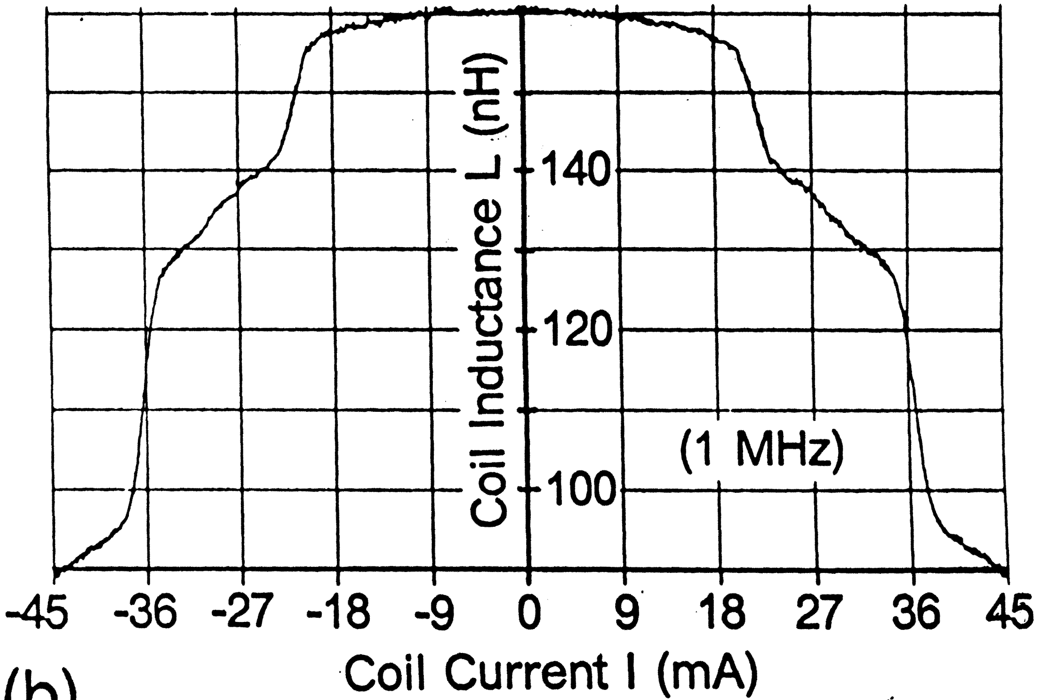
apex saturation



(d) Apex window



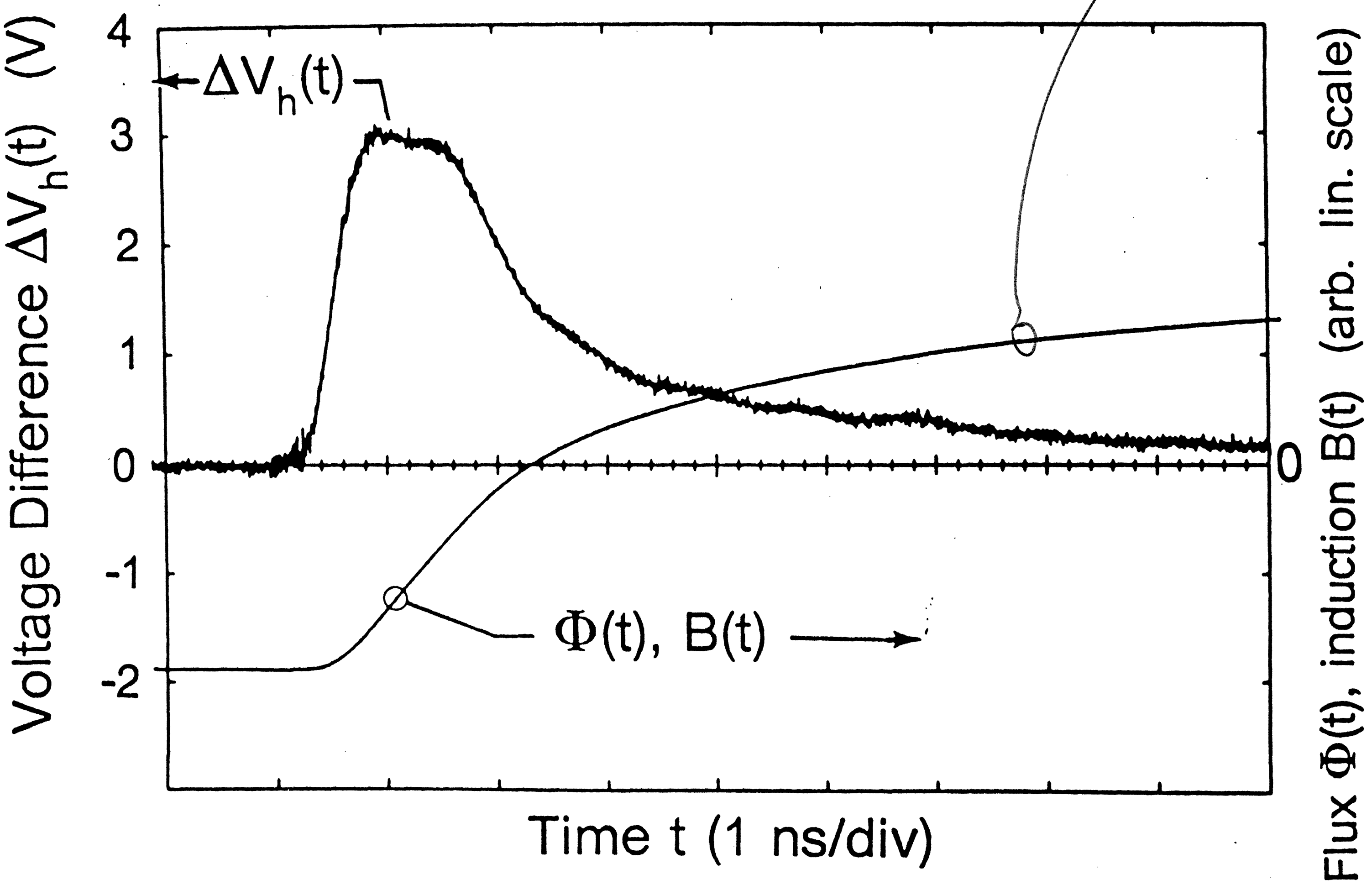
(a)



(b)

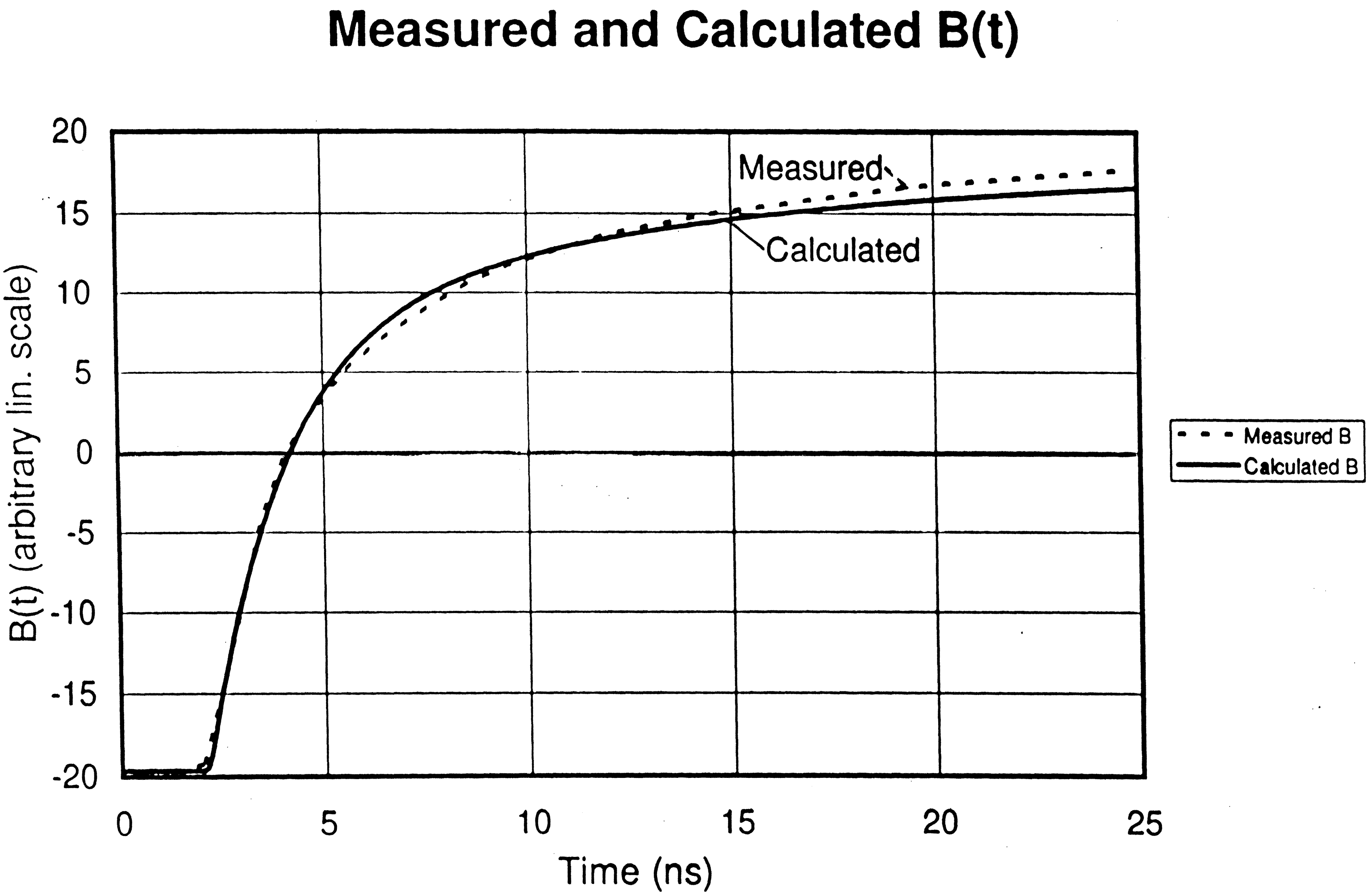
When saturated no Im response.

-model very close to data.



integrate

To generate
M vs I
curve


Measured and Calculated B(t)
Measured
Calculated
B(t) (arbitrary lin. scale)
20
15
10
5
0
-5
-10
-15
-20
0
5
10
15
20
25
Time (ns)
Measured B
Calculated B

Write Channel Parameter Values

- **Write Driver**

  Differential output,NPN trnasistor area 7000 μm^2,
  f_t = 3 GHz, C = 2.5 pF, no damping resistor
  Slewing rate 18 MA/s ($I_W \geq 18$ mA)
  Bandwidth 80 MHz, Rise time 2 ns ($I_W \leq 18$ mA)

- **Inductive Write Head**

(a) Geometry:

15 turn 80/20 NiFe head
P_2W pole tip 4 μm, P_2W yoke = 60 μm
P_2T = 4.7 μm, $P_1W \gg P_2W$, P_1T = 3 μm,
yoke height 130 μm

(b) Saturated Coil Impedances:

$C_W = 0.75$ pF, $R_W = 600\ \Omega$, $R_{CW} = 16\ \Omega$, $L_W = 50$ nH

(c) Induced Voltage:

$$V_m = -N\frac{d\Phi}{dt} = -NA\frac{dB(t)}{dt}$$

N = 15, A = $P_2T \times P_2W$ yoke, NA = 4.3×10^{-9} m^2

(d) Current I_W to Induction B_0 Conversion:

$B_0 = B_{AS} = 0.6$ T at $I_W = 22$ mA
$B_0 = B_{BGS} = 0.85$ T at $I_W = 36.6$ mA
$B_0 = B_S = 1$ T at $I_W = 75$ mA

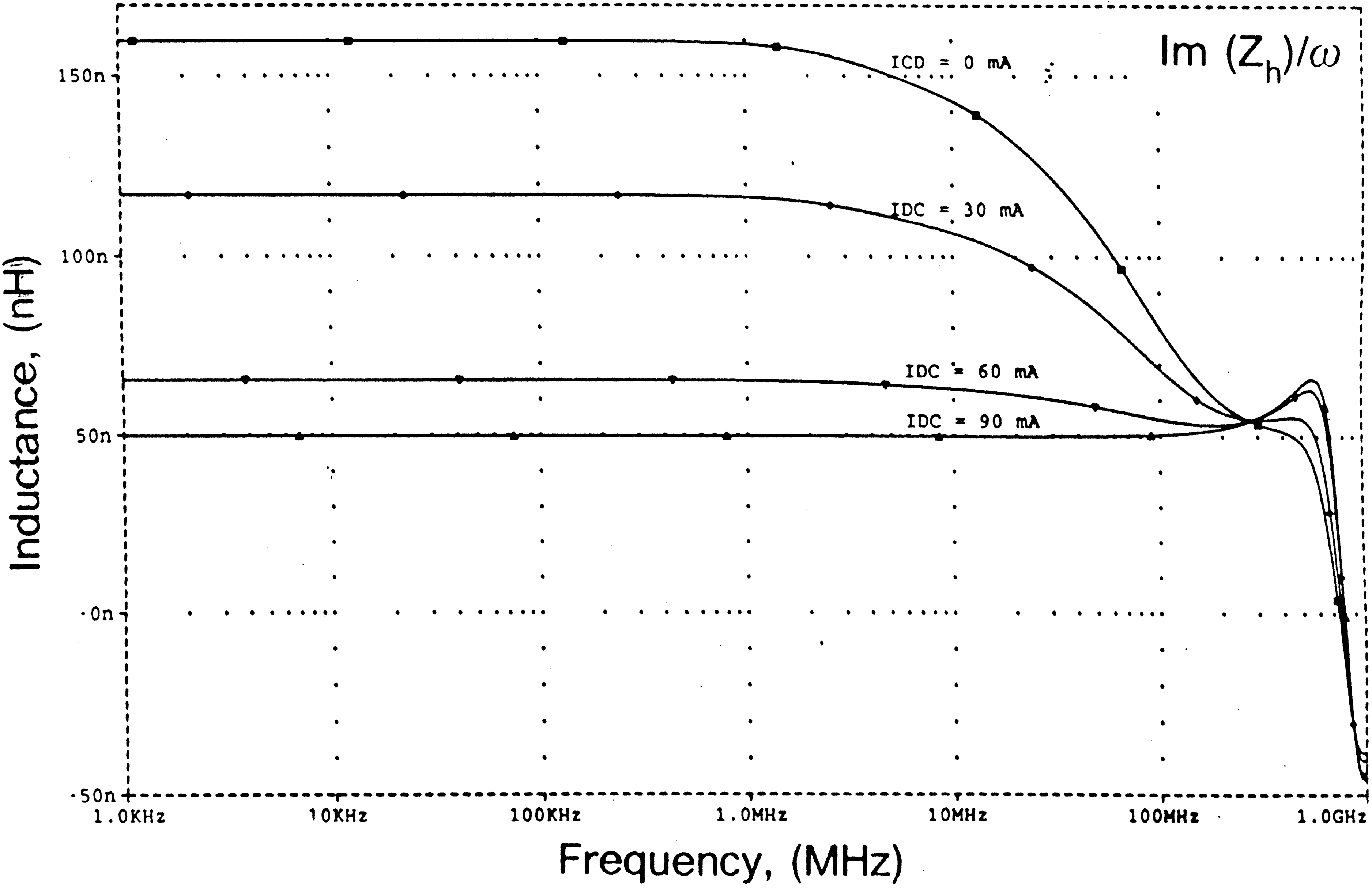
(e) Eddy Current Filtering:

τ_1 = 2.56 ns, m = 3.16, n = 4

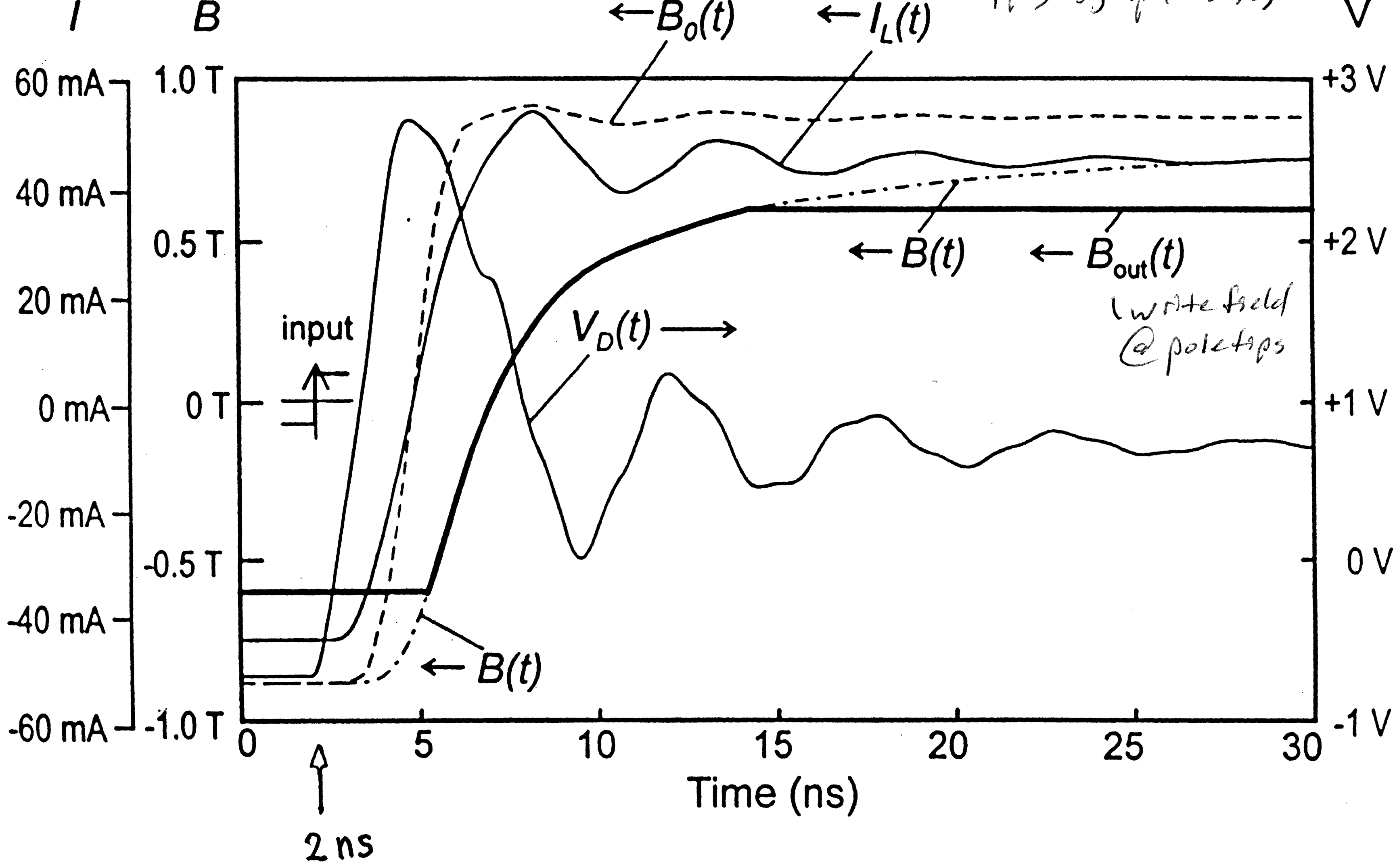
(f) Apex Saturation Window:

$B(t) = B_{out}(t)$ $\quad B \leq B_{AS}$
$B(t) = B_{AS}$ $\quad B > B_{AS}$
$B_{out}(t) \propto H_{write}(t)$

Write Coil Series Inductance



Write Channel Waveforms

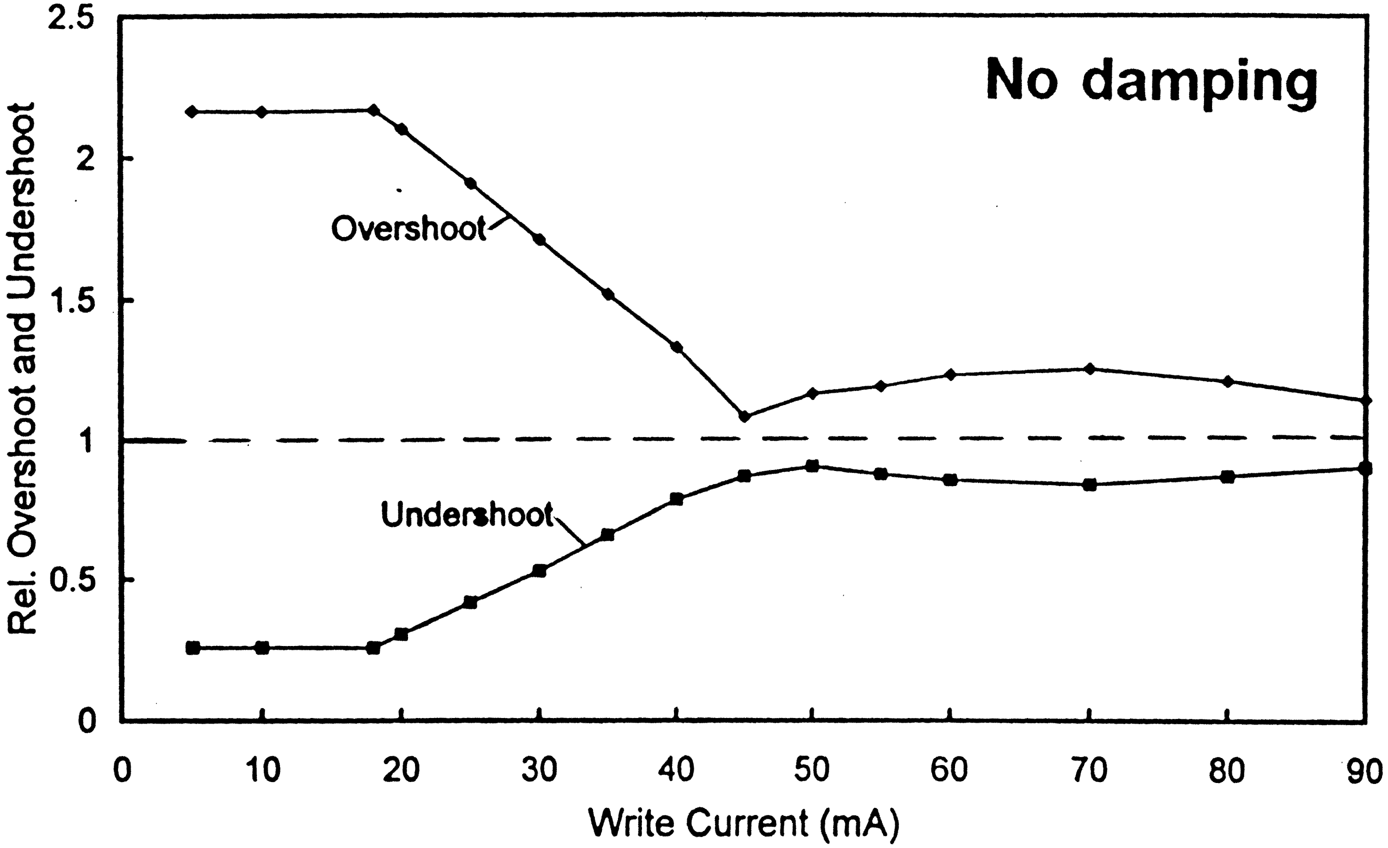


yoke in sat, so little ringing (clipping by apex sat.)

(write field @ poletips

2 ns

(First) Current Over/Undershoot



0-p

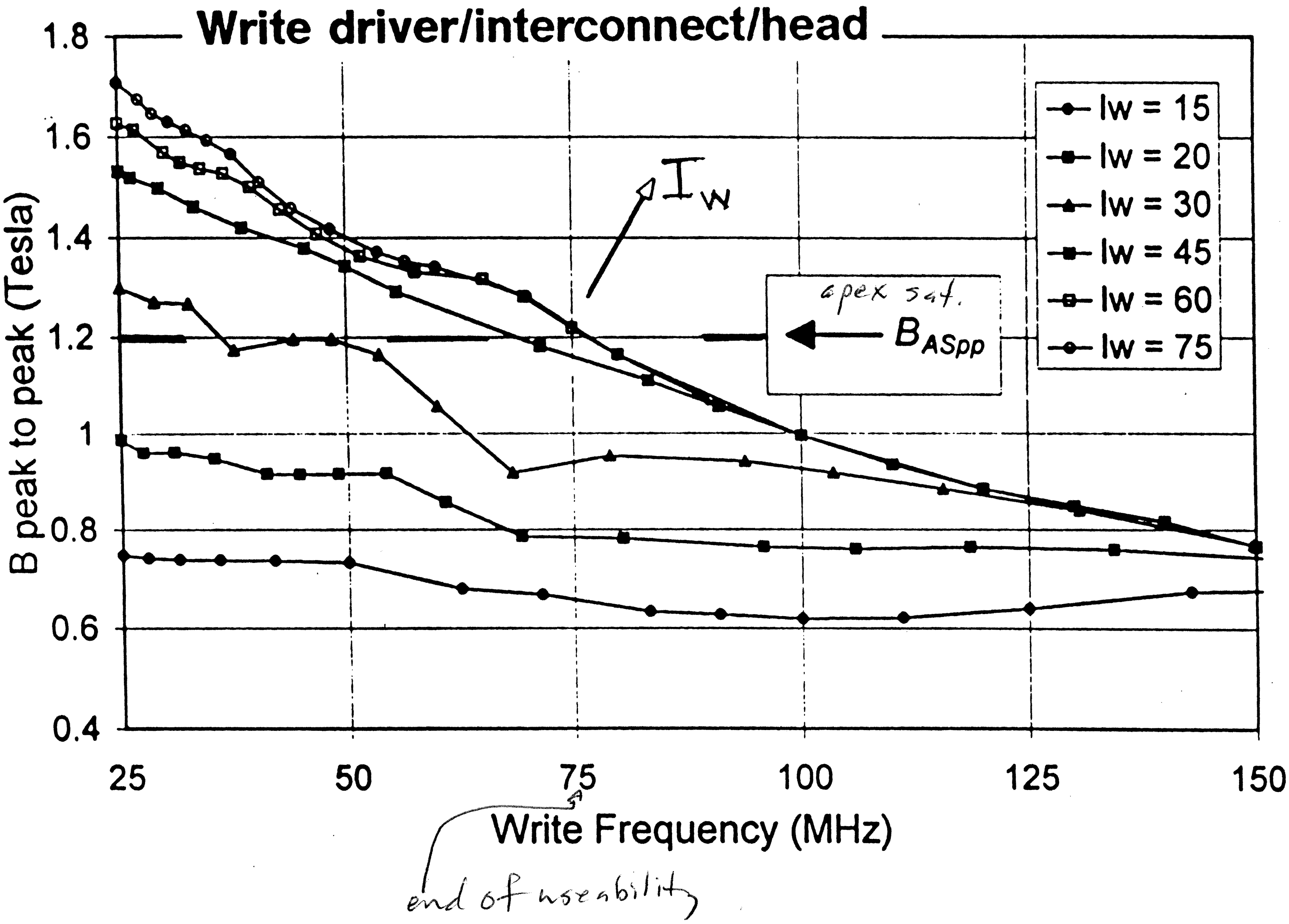
Write Channel Test Signals

- Square wave input
  Induction swing large enough
  Criterion: $B_{pp} > 2\,B_{min}$ (B_{AS})

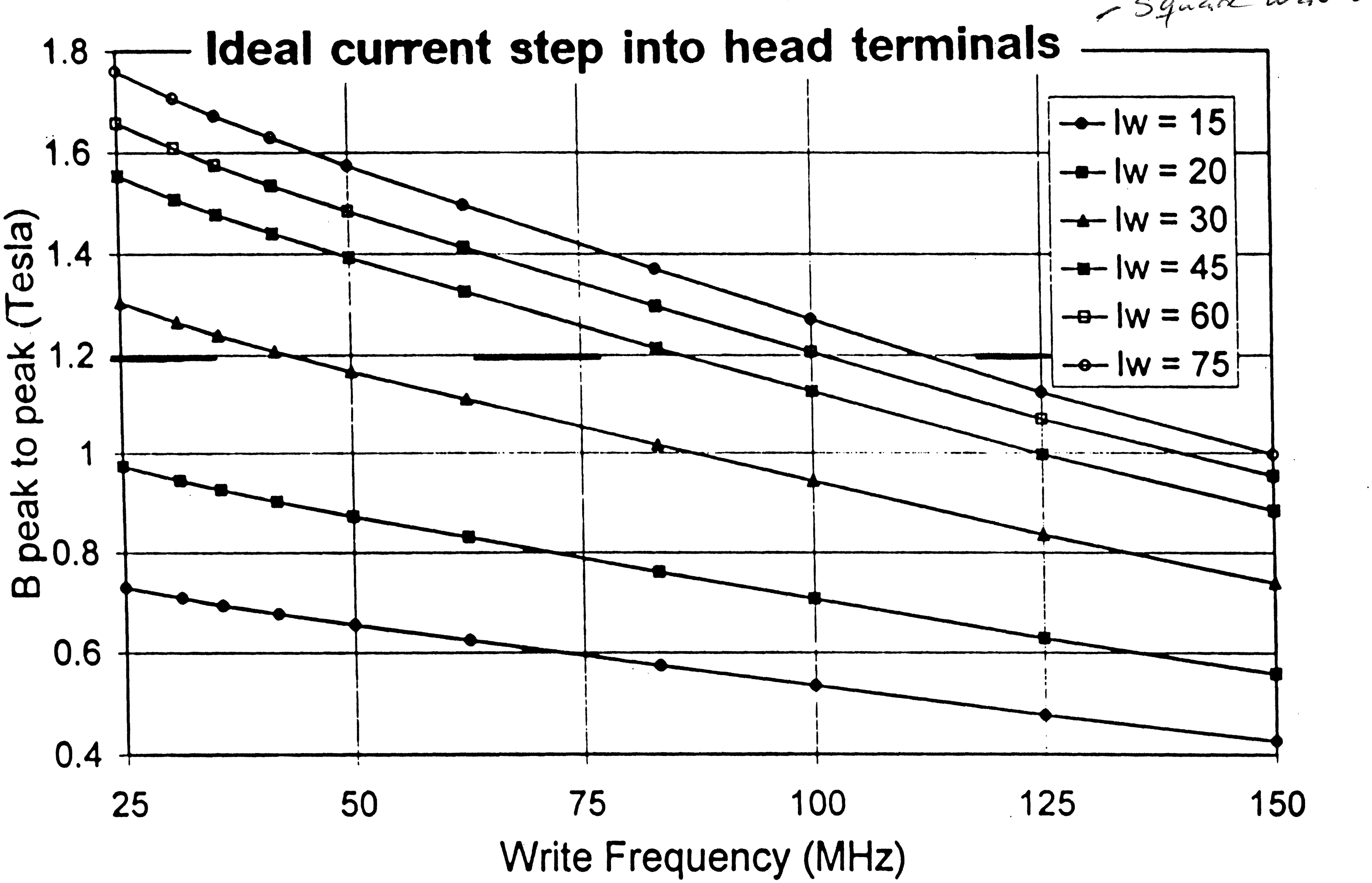
- Isolated transition input
  Reversal time short enough
  Criterion: $\tau_{rev} < \tau_{max}$ $(2\,F_{W_{max}})^{-1}$

- Di-bit input
  Bit shift small enough
  Criterion: $\varepsilon < \varepsilon_{max}$ (15 %)

Peak-to-Peak Yoke Induction Swing

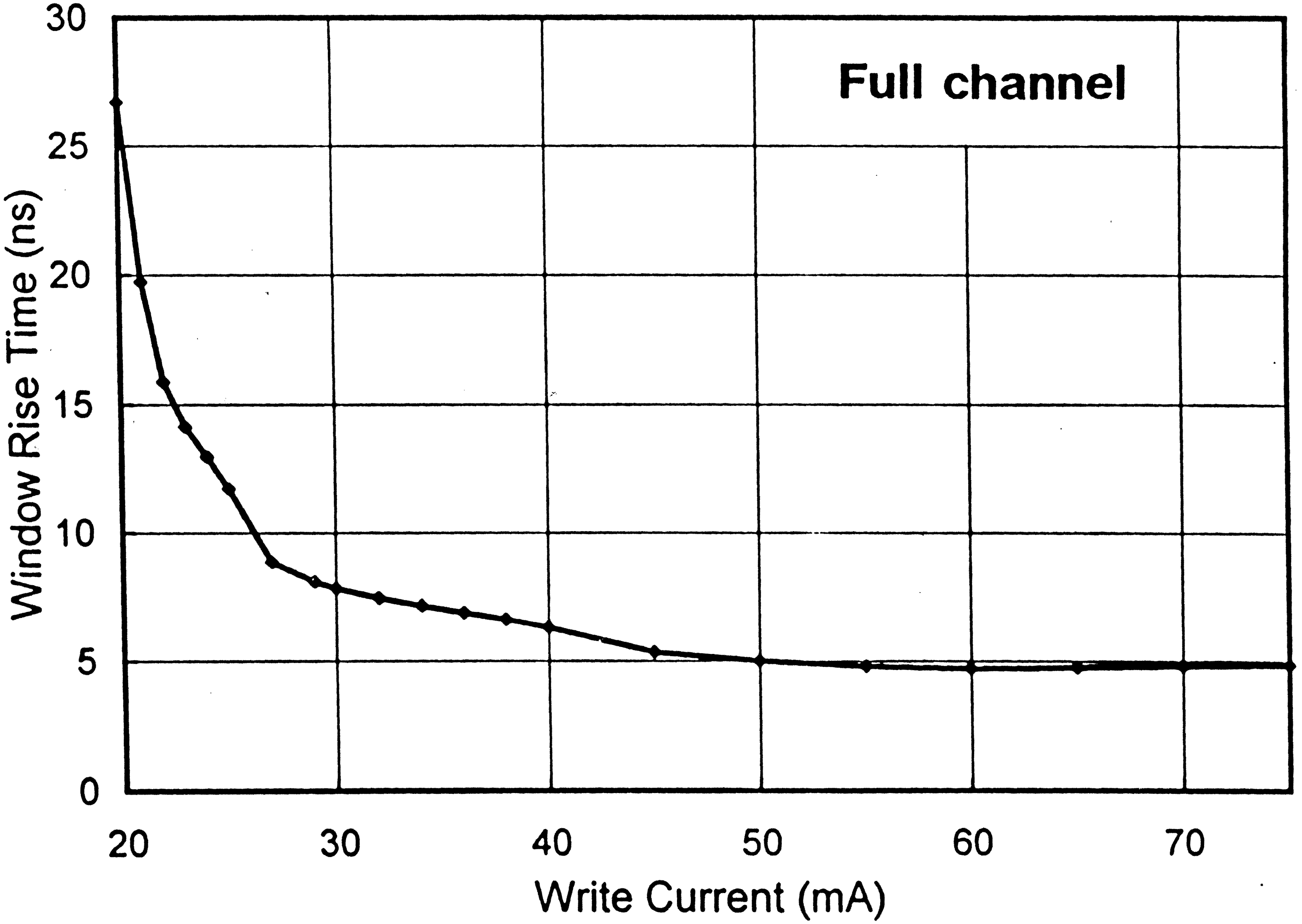


Peak-to-Peak Yoke Induction Swing



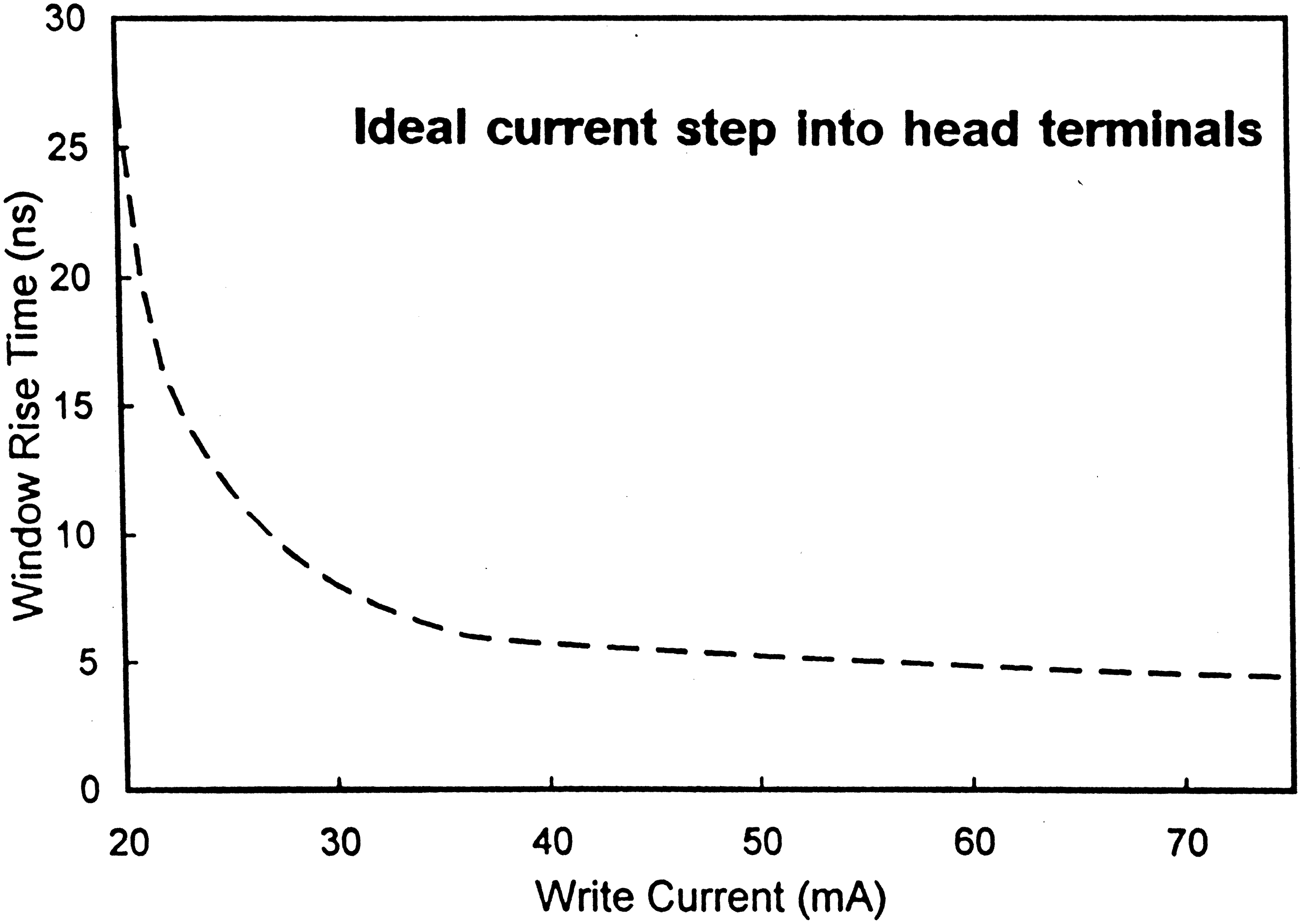
← Square waves

Write Field Reversal Time



apex, sat, limited

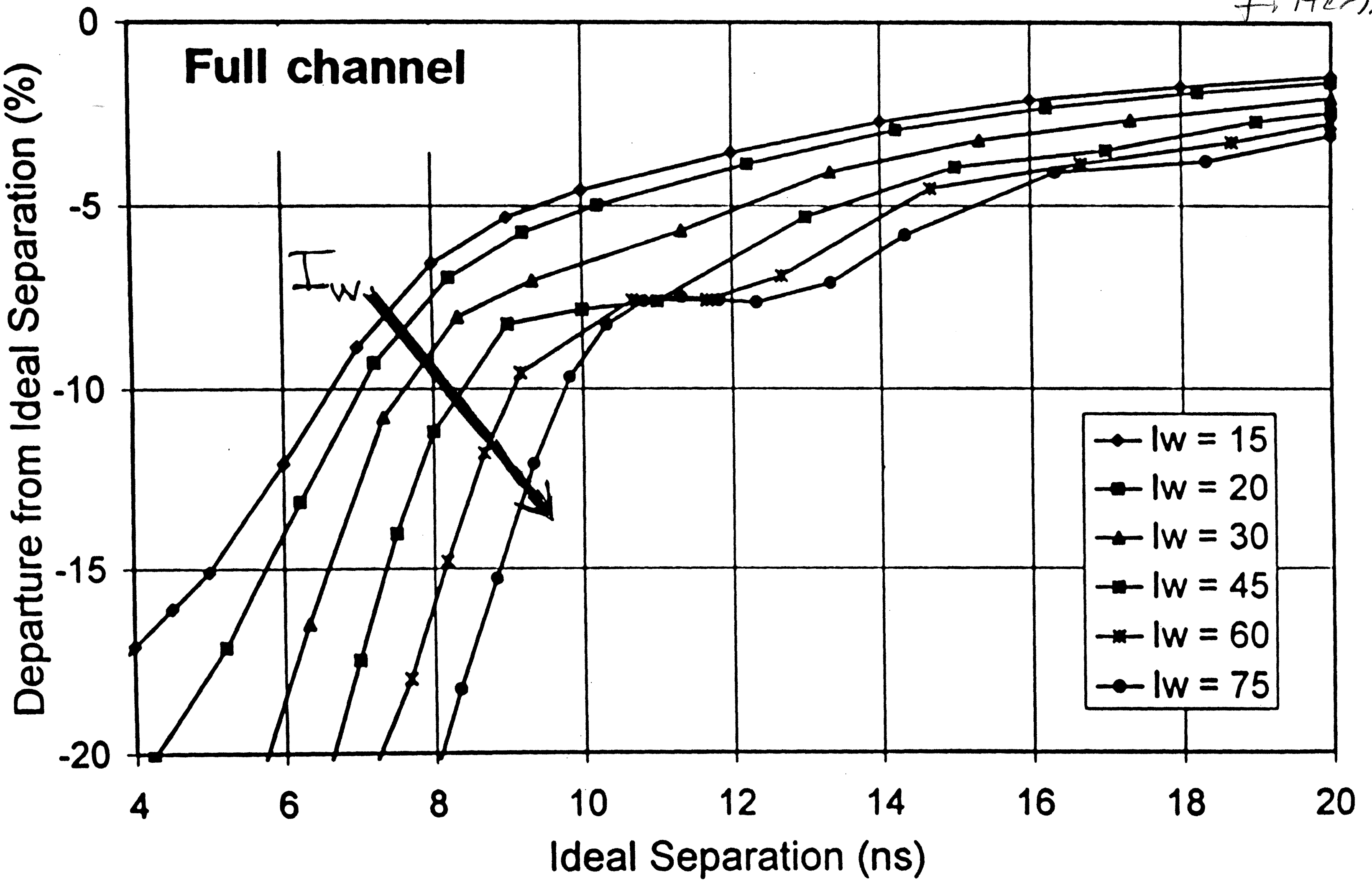
Write Field Reversal Time



– reversal time almost totally head dependent

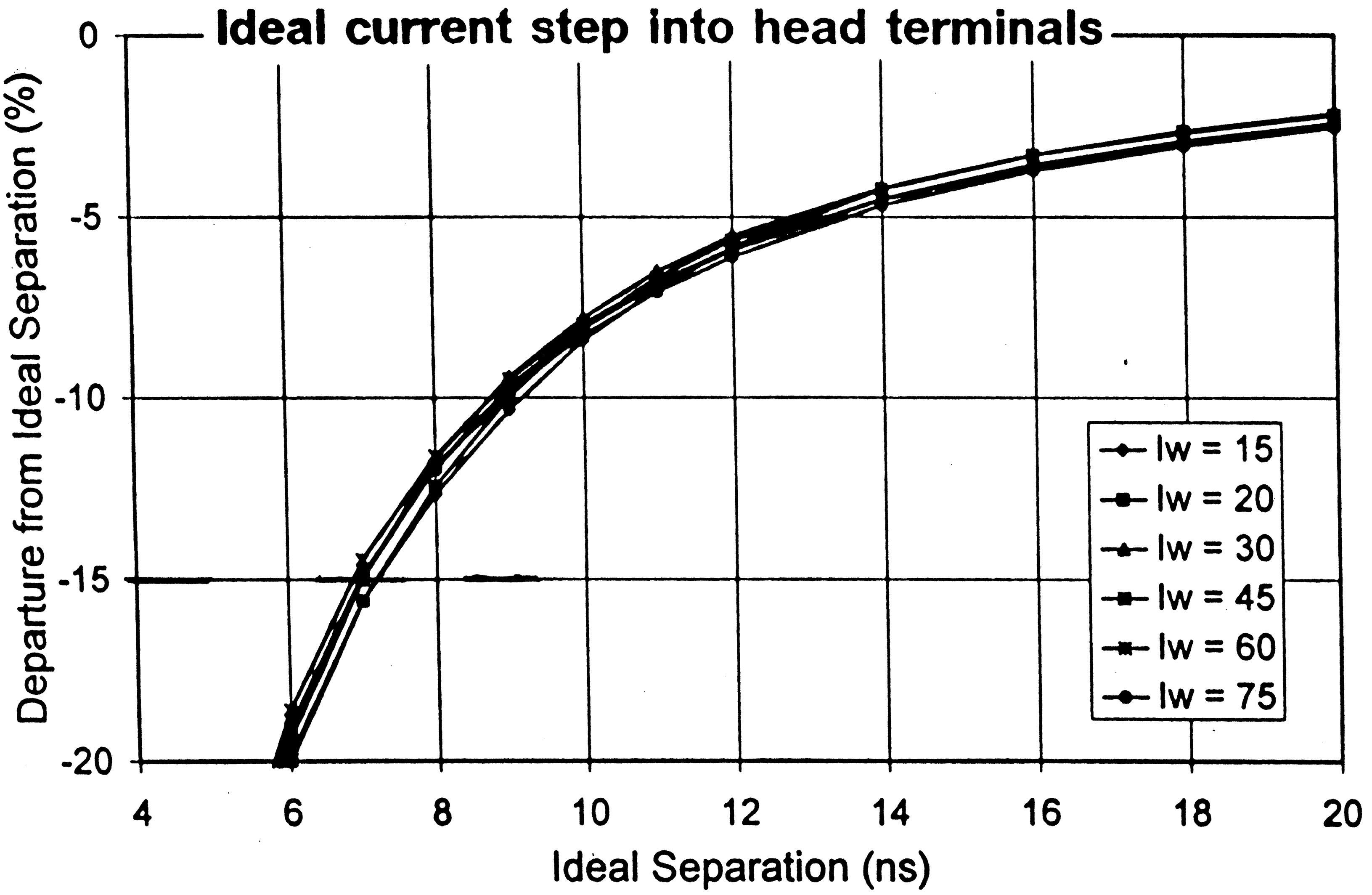
Pulse Compression

diff's due to compensation effects (forms filter).



Pulse Compression

head alone.



Conclusions (Cont.)

- **Write Path**

  Yoke swing $B_{pp} > 2B_{AS}$

  Transition rise time $\tau < 1/(2F_{W,max})$

  Bit shift $\varepsilon < 15\ \%$

  √ ***Full Write Path:***

  Mag. Swing and Bit Shift limited to

  $\Delta T > 7.1$ ns and $F_{W,max} < 70$ MHz

  - N.B: $I_W = 45$ mA, $\tau = 6$ ns

  √ ***Head Only:***

  Mag. Swing and Bit Shift limited to

  $\Delta T > 7.1$ ns and $F_{W,max} < 70$ MHz

  - Now: $I_W = 36$ mA, $\tau = 6.8$ ns

Final Conclusion

Therefore, the maximum data rate for this channel using a (0,k) RLL code with an 8/9 rate is 15.56 MB/s

$$(F_{W,max} = 70\ \text{MHz},\ \ \Delta T = 7.1\ \text{ns})$$

- So severe limitations
on data rate with
current technology

Finally ....

- MR heads require a well-matched disk and electronics, especially for more demanding applications:
  - high data rates
  - narrow trackwidths
  - near contact operation

- Front-end must be designed as a ***system***
  - A collection of individually optimized components makes a sub-optimal front-end
  - Components have limited exchangeability

- Many electronic design options exist
  - Choice depends on application
  - Do not expect "generic" modules that serve everyone's needs

IIST

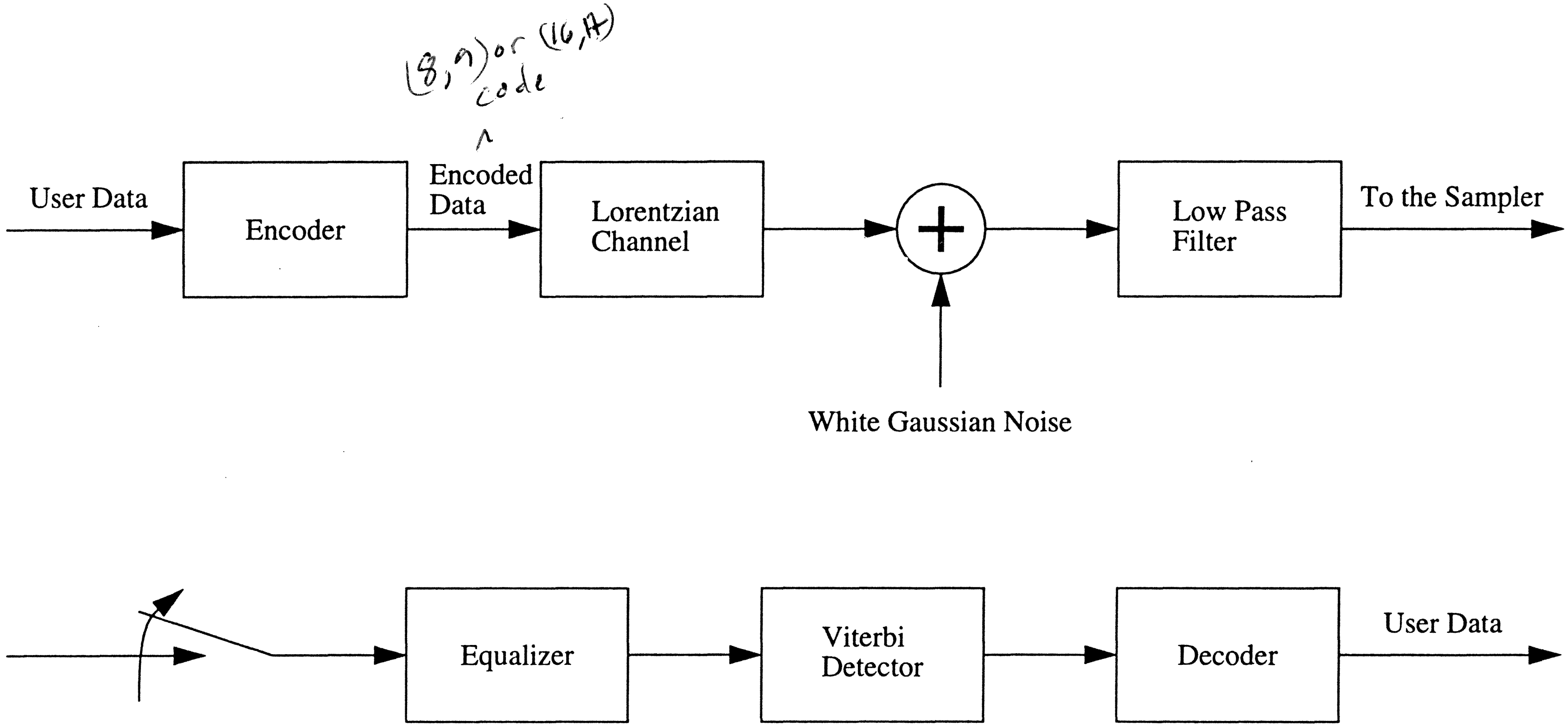
DIGITAL READ/WRITE CHANNELS FOR MAGNETIC RECORDING

Nersi Nazari
GEC Plessey Semiconductors

May 28, 1996

OUTLINE

- Signal detection theory
- Typical digital PRML chip architecture
- Testing digital PRML chips and results
- Trellis coded partial response



Block Diagram of the System

Signal Detection Theory

- Assume a Lorentzian Channel, then for an "isolated" transition the output voltage is

$$h(t) = \frac{1}{1 + \left(\frac{2t}{\mathrm{PW}_{50}}\right)^2},$$

where PW_{50} is the width of the pulse at 50% amplitude.

- If we needed to detect only one isolated transition, use a "matched filter" detector [1],

mirror image of pulse
(symmetric so same)

$$F(t) = h(-t) = h(t) \ .$$

The error probability is given by

$$P_e = \frac{1}{2}Q\left(\sqrt{E_t/\eta_0}\right) \ ,$$

noise floor

where,

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{-u^2/2}\,du \ ,$$

$$E_t = \int_{-\infty}^{\infty} h^2(t)\,dt = \frac{\pi}{4}\ \mathrm{PW}_{50}\ ,$$

is the energy per transition, and η_0 is the amplitude of single sided noise spectral density.

- If we need to detect a “dibit”, two transition T seconds apart, the signal is

$$c(t) = h(t) - h(t-T)\ .$$

Then, the optimum detector is matched to $c(t)$ and is given by

$$F(t) = c(-t) = h(-t) - h(-t-T) \ .$$

The expression for the error probability is exactly the same as single transition, except use [2]

$$E_d = \int_{-\infty}^{\infty} c^2(t)\,dt = \frac{\pi}{2}\ \mathrm{PW}_{50}\,\frac{1}{1+S^2}\ ,$$

use instead of E_t

where $S = \mathrm{PW}_{50}/T$, is the channel normalized density.

- For a "sampled" channel, such as PRML, the signal needs to pass through a low pass filter before sampling, due to sampling the energy per bit is reduced to

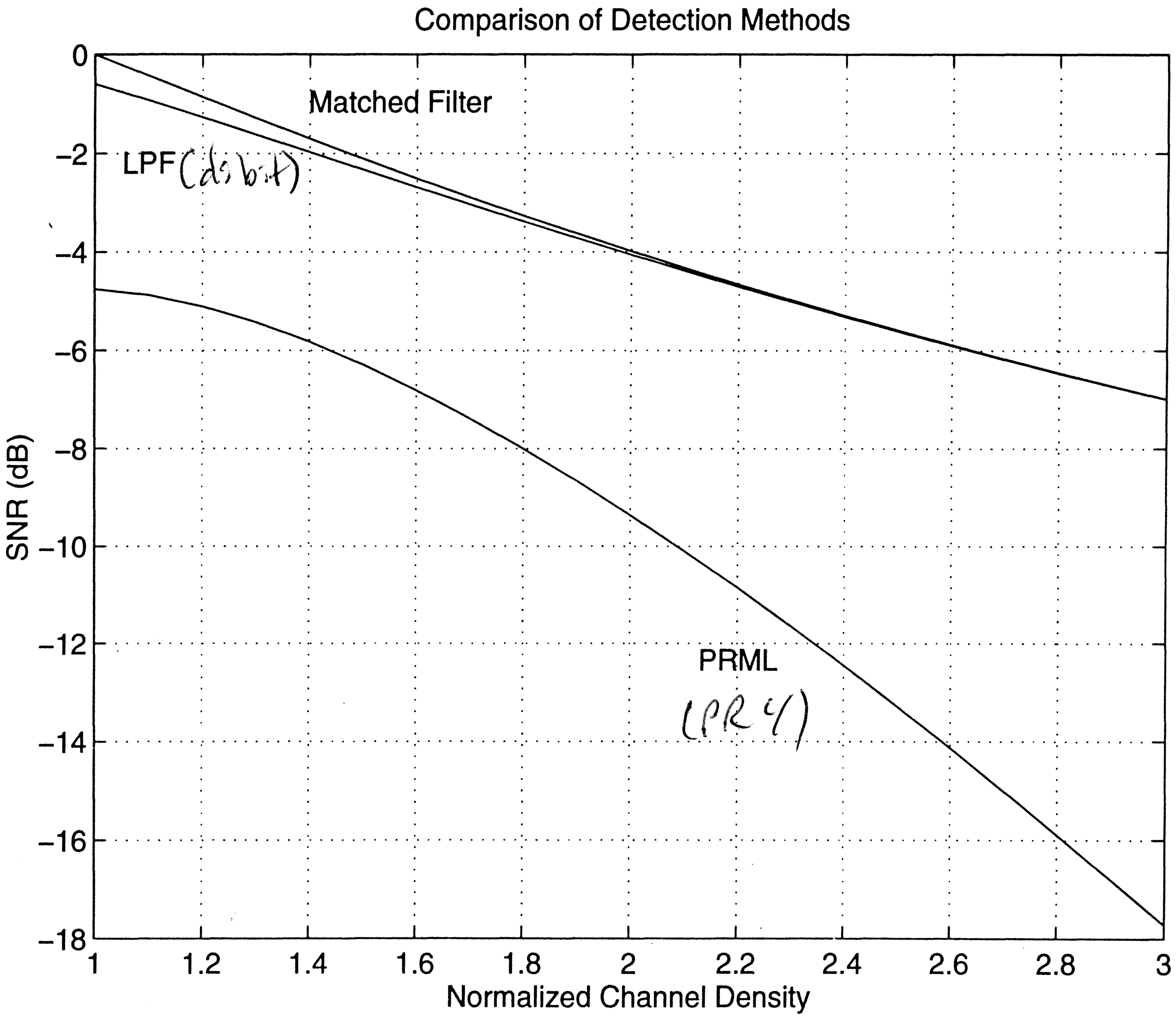
$\frac{1}{2T}$. BW
so no aliasing, before sample.

$$E_l = \int_{-1/2T}^{1/2T} |H(f)|^2 df = E_d [1 - e^{-\pi S}(1 + 2S^2)] \ .$$

- For a PRML channel, signal needs to be equalized to PR4 pulse shape, sequence energy at the Viterbi detector is given by [3]

$$E_v = E_l \frac{(\pi S)^3 (S^2 + 1)}{e^{\pi S} - 1 - 2S^2} \ .$$

Reference [2] shows in detail how the above equation should be modified to account for noise correlation at the Viterbi detector.


Comparison of Detection Methods
Matched Filter
LPF (dibit)
PRML
(PR4)
SNR (dB)
0
-2
-4
-6
-8
-10
-12
-14
-16
-18
1
1.2
1.4
1.6
1.8
2
2.2
2.4
2.6
2.8
3
Normalized Channel Density

Typical Digital PRML Architecture

- PRIV architecture
  - -- Dibit response is equalized to $1 - D^2$
  - -- Odd and even samples can be independently detected
  - -- Channel output has only three values, 0, 1, -1

detect odd/even samples independently

- 8/9 encoding
  - -- Use (0,G/I) codes such as (0,4/4)
  - -- Two transitions can be next to each other
  - -- At least one "1" sample after every G 0's
  - -- At least one "1" sample after every I 0's in odd or even subsequences

high rate
- transitions adjacent to each other

- 7 pole equiripple continuous time filter
    - -- Limits noise bandwidth
    - -- Does most of channel equalization via high frequency boost
    - -- Often also has asymmetric zeros for phase equalization

rise & fall
times different
(as MR heads,
Keeper signals?)

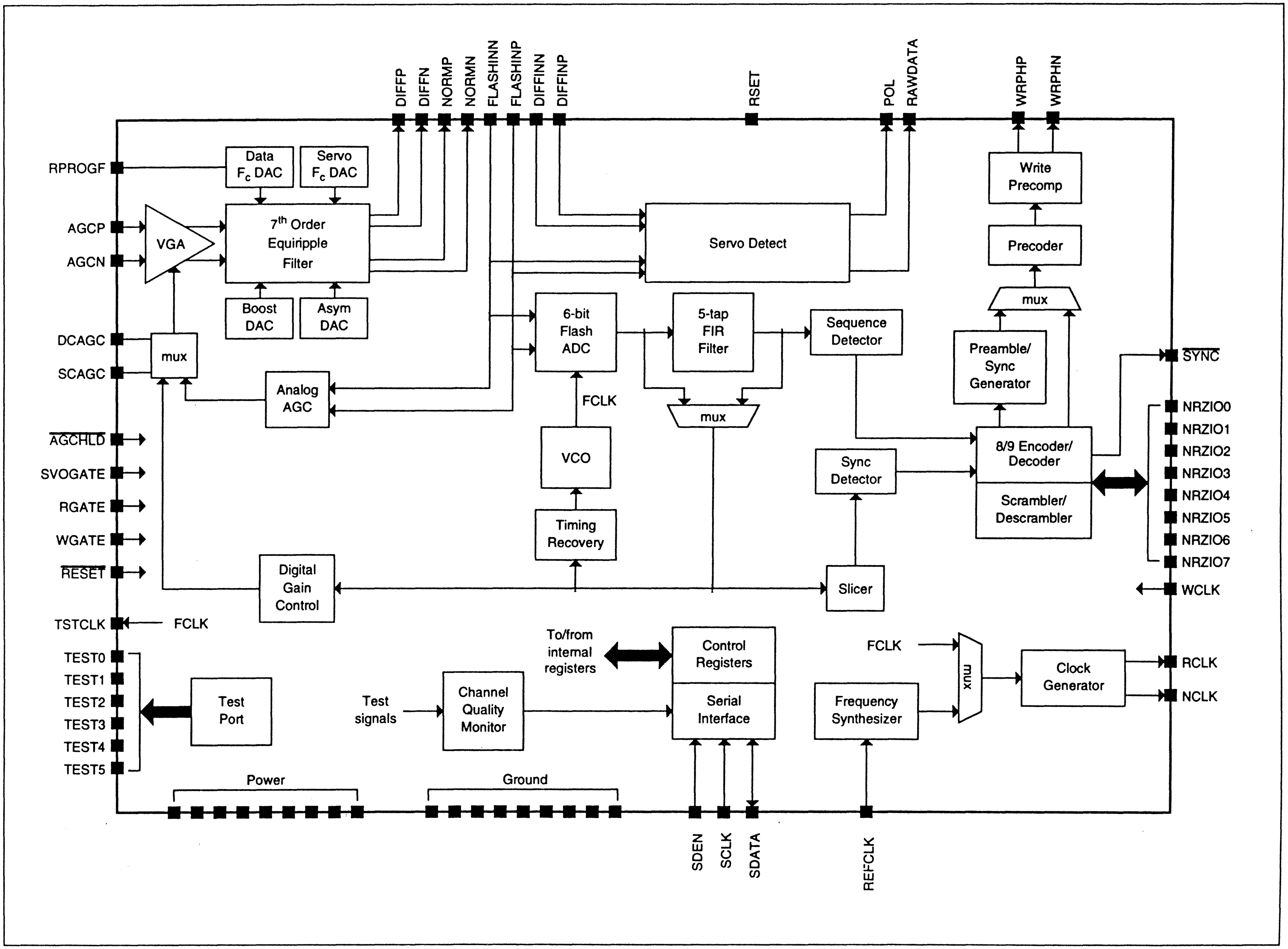
-
    - -- Must be able to quickly change characteristics between data and servo

- 6-bit flash ADC
    - -- Distinguishing block of digital PRML channels
    - -- Besides data recovery, can be used for servo via oversampling

- Variable threshold algorithm (VTA) Viterbi detector
  - -- PRIV signal can be interleaved
  - -- Each interleave can have a trivial Viterbi detector
- 3-7 TAP DIGITAL FILTER
- Write precompensation
  - -- Necessary due to transitions written next to each other
  - -- Write close transitions farther
- Randomizer
  - -- Avoid periodic patterns
  - -- Used for reading "known" patterns

illegal pattern
e.g. all 0's for characterization
of channel.

- Channel quality
  - -- Feedback from the channel for parameter optimization
  - -- Monitor health of the channel
- Digital/analog test port
  - -- Can see into the channel
  - -- Used for testing, engineering development, and manufacturing environment


DIFFP
DIFFN
NORMP
NORMN
FLASHINN
FLASHINP
DIFFINN
DIFFINP
RSET
POL
RAWDATA
WRPHP
WRPHN
RPROGF
AGCP
AGCN
DCAGC
SCAGC
AGCHLD
SVOGATE
RGATE
WGATE
RESET
TSTCLK
FCLK
TEST0
TEST1
TEST2
TEST3
TEST4
TEST5
Data F_c DAC
Servo F_c DAC
VGA
7th Order Equiripple Filter
Boost DAC
Asym DAC
mux
Analog AGC
Servo Detect
6-bit Flash ADC
5-tap FIR Filter
Sequence Detector
FCLK
mux
VCO
Timing Recovery
Digital Gain Control
Slicer
Sync Detector
Write Precomp
Precoder
mux
Preamble/ Sync Generator
8/9 Encoder/ Decoder
Scrambler/ Descrambler
SYNC
NRZIO0
NRZIO1
NRZIO2
NRZIO3
NRZIO4
NRZIO5
NRZIO6
NRZIO7
WCLK
To/from internal registers
Control Registers
Serial Interface
FCLK
mux
Clock Generator
RCLK
NCLK
Frequency Synthesizer
Test Port
Test signals
Channel Quality Monitor
Power
Ground
SDEN
SCLK
SDATA
REFCLK

8/9 (0,4/4) PR4 VS. 2/3 (1,7) E(E)PR4

ADVANTAGES OF 8/9:

- LOWER CHANNEL DATA RATE (33%)
- HIGHER EFFECTIVE SNR (ABOUT 1 dB)
- TRIVIAL VITERBI DETECTOR
- CAN INTERLEAVE MAJOR PORTIONS OF DIGITAL LOGIC
- MORE ROBUST TIMING RECOVERY AND GAIN LOOPS

DISADVANTAGES OF 8/9:

- HIGHER FCI (50%)
    - -- CAN COPE BY OPTIMIZING THE MEDIA
    - -- CAN BE MINIMIZED BY WRITE PRECOMPENSATION
- MORE COMPLICATED ENCODER/DECODER
- IBM PATENT (FOR VENDORS WITHOUT CROSS LICENSING AGREEMENT)

ANALOG VS. DIGITAL PRML

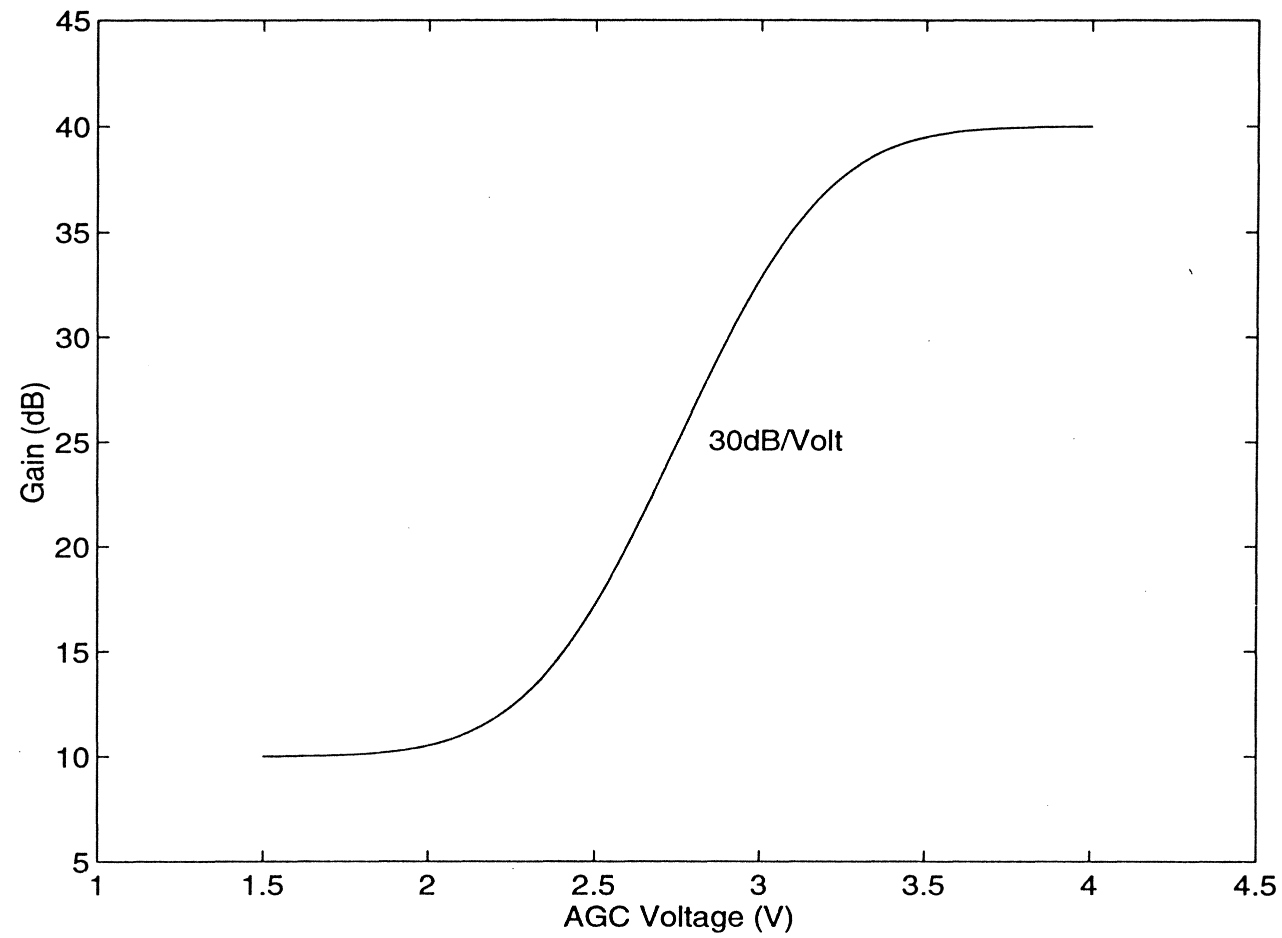
ADVANTAGES OF DIGITAL:

- CHANNEL QUALITY MEASUREMENT
  - -- OPTIMIZATION BY SOFTWARE ON THE BENCH AND IN THE FACTORY
  - -- CHANNEL "HEALTH" MONITORING IN THE FIELD
  - -- ABILITY TO INCORPORATE FLAW SCAN, FLYING HEIGHT MONITOR, ETC.
- EXTENDABLE TO MORE ADVANCED CODING AND DETECTION SCHEMES
- REPEATABILITY/PRECISION
- HIGHER BPI (IBM INTERMAG '93)

DISADVANTAGES OF DIGITAL:

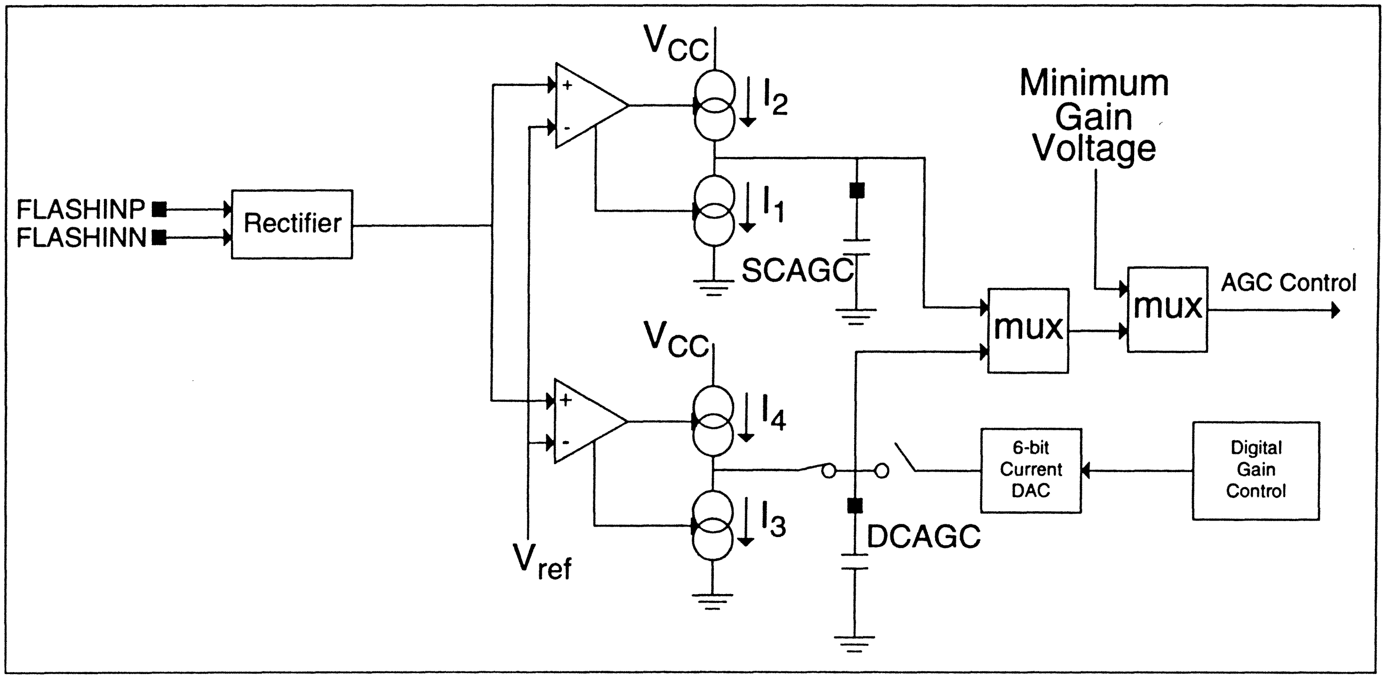
- HIGHER POWER AND LARGER SIZE DUE TO ADC

VGA



45
40
35
30
25
20
15
10
5
Gain (dB)
30dB/Volt
1
1.5
2
2.5
3
3.5
4
4.5
AGC Voltage (V)

GAIN CONTROL



$$G_n = \hat{x}_n(y_n - x_n)\gamma$$

G_n = Gain update at time n

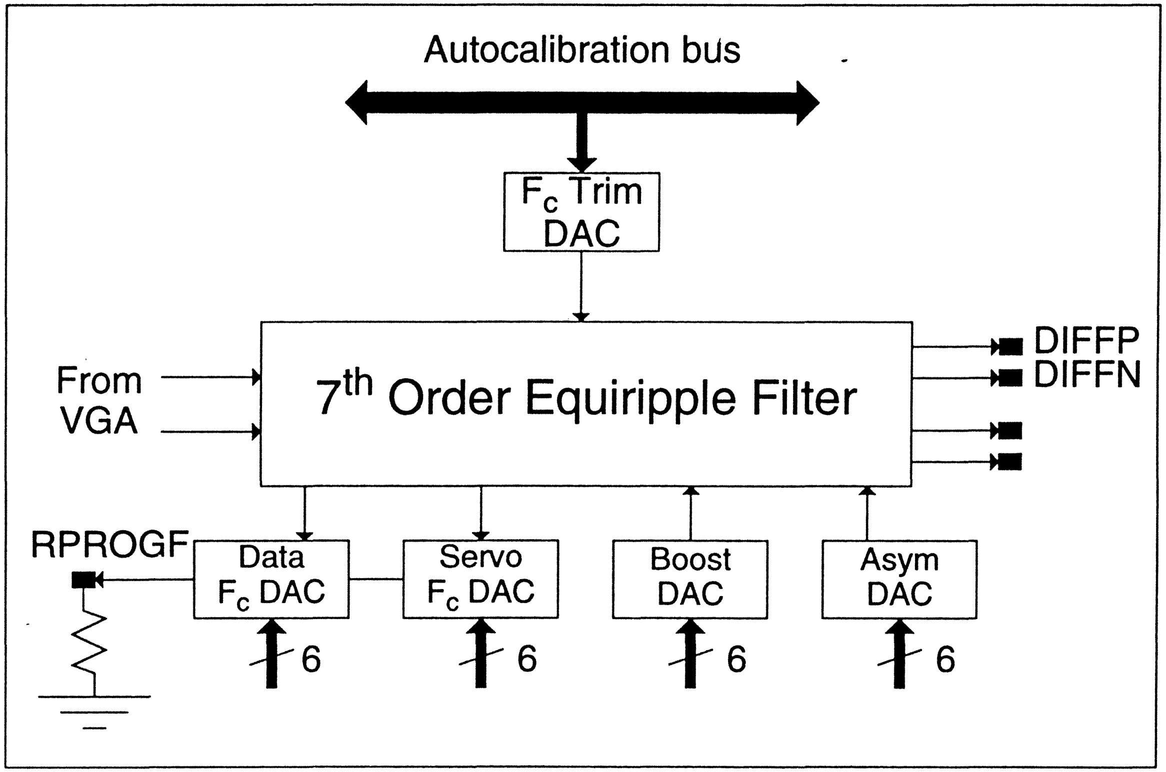
γ = AGC gain factor

y_n = Input value at time n

x_n = Desired value at time n

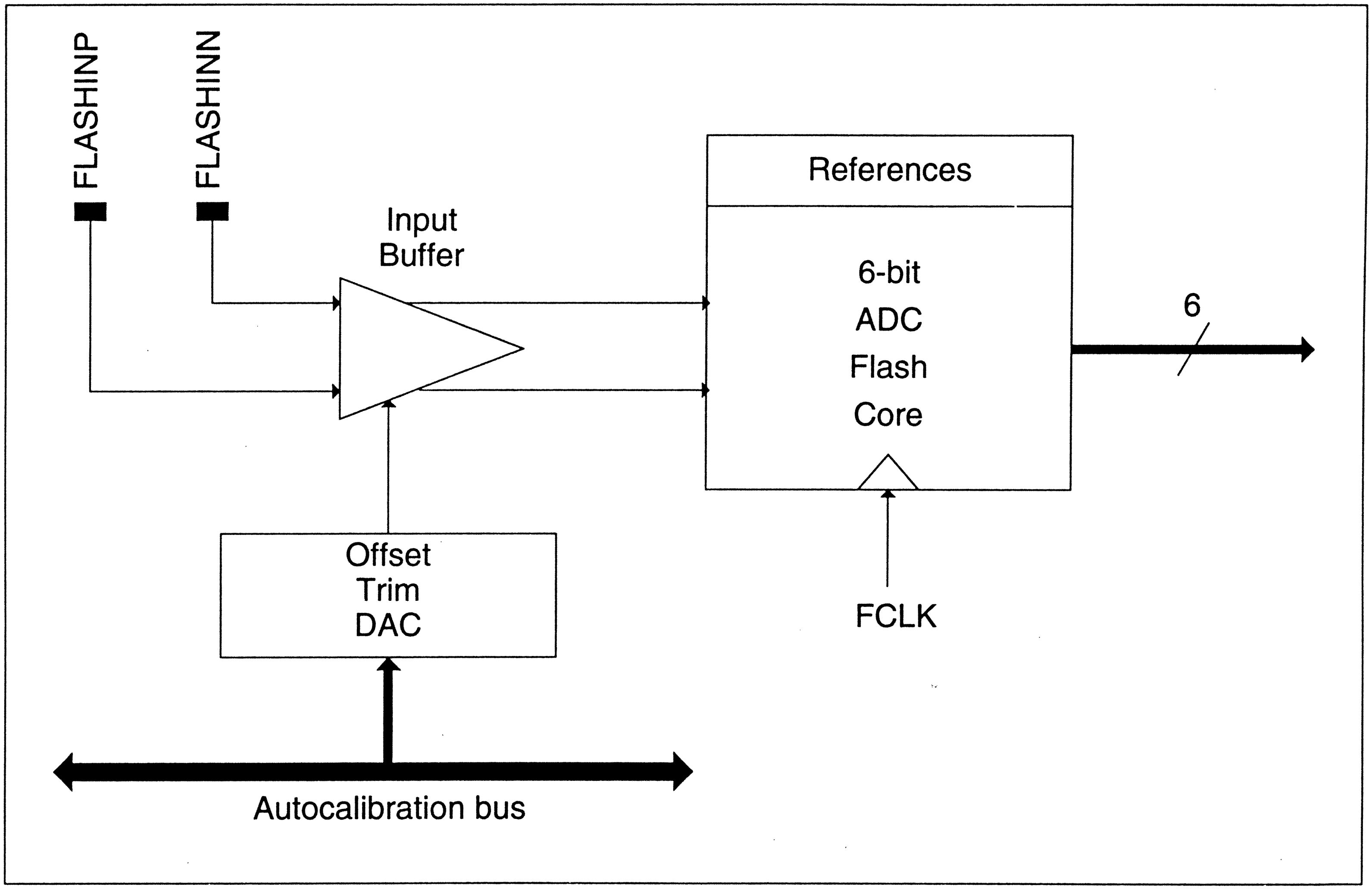
$\hat{x}_n$ = Slicer output at time n

CONTINUOUS TIME FILTER

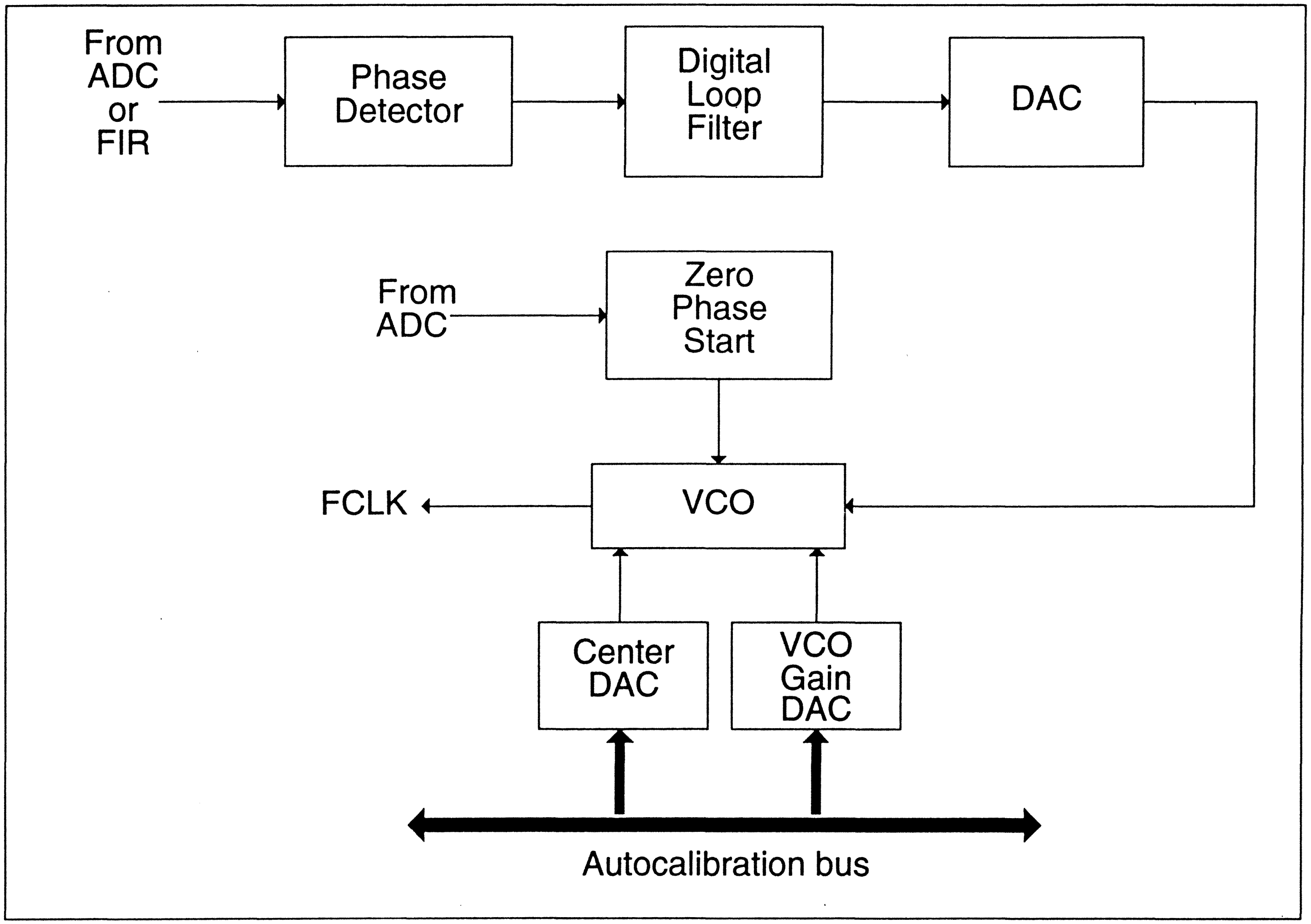


$$\frac{\left(-K_2S^2+K_1S+1\right)18}{S^7+5.23S^6+19.7S^5+45.9S^4+76.5S^3+84.1S^2+57.1S+18}$$

ANALOG-TO-DIGITAL CONVERTER



TIMING RECOVERY


From ADC or FIR

Phase Detector

Digital Loop Filter

DAC

From ADC

Zero Phase Start

FCLK

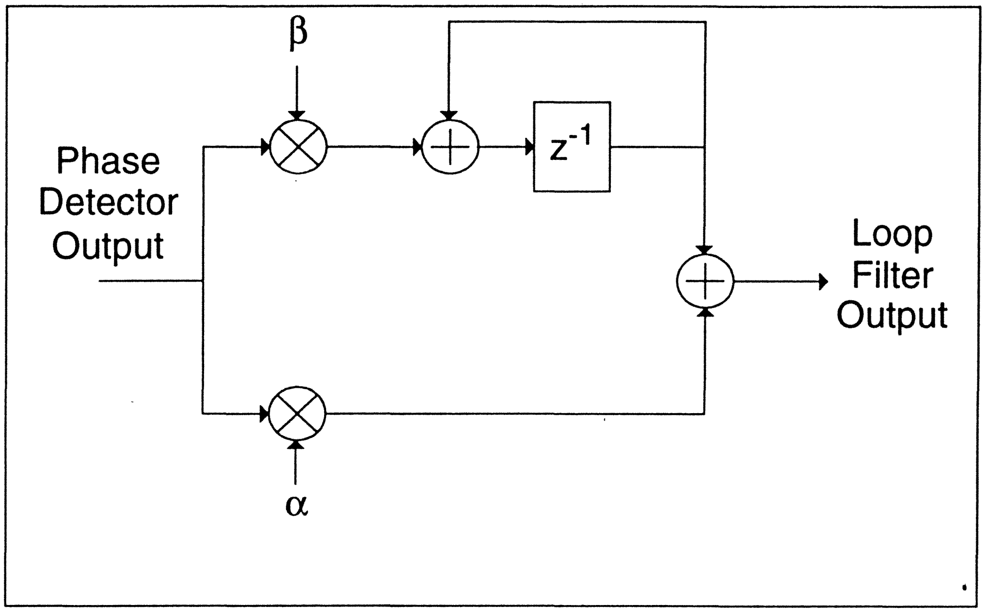
VCO

Center DAC

VCO Gain DAC

Autocalibration bus

TIMING RECOVERY-cont



$$\Delta\tau_n = -y_n x_{n-1} + y_{n-1} x_n$$

$\Delta\tau_n$ = Phase error estimate at time n

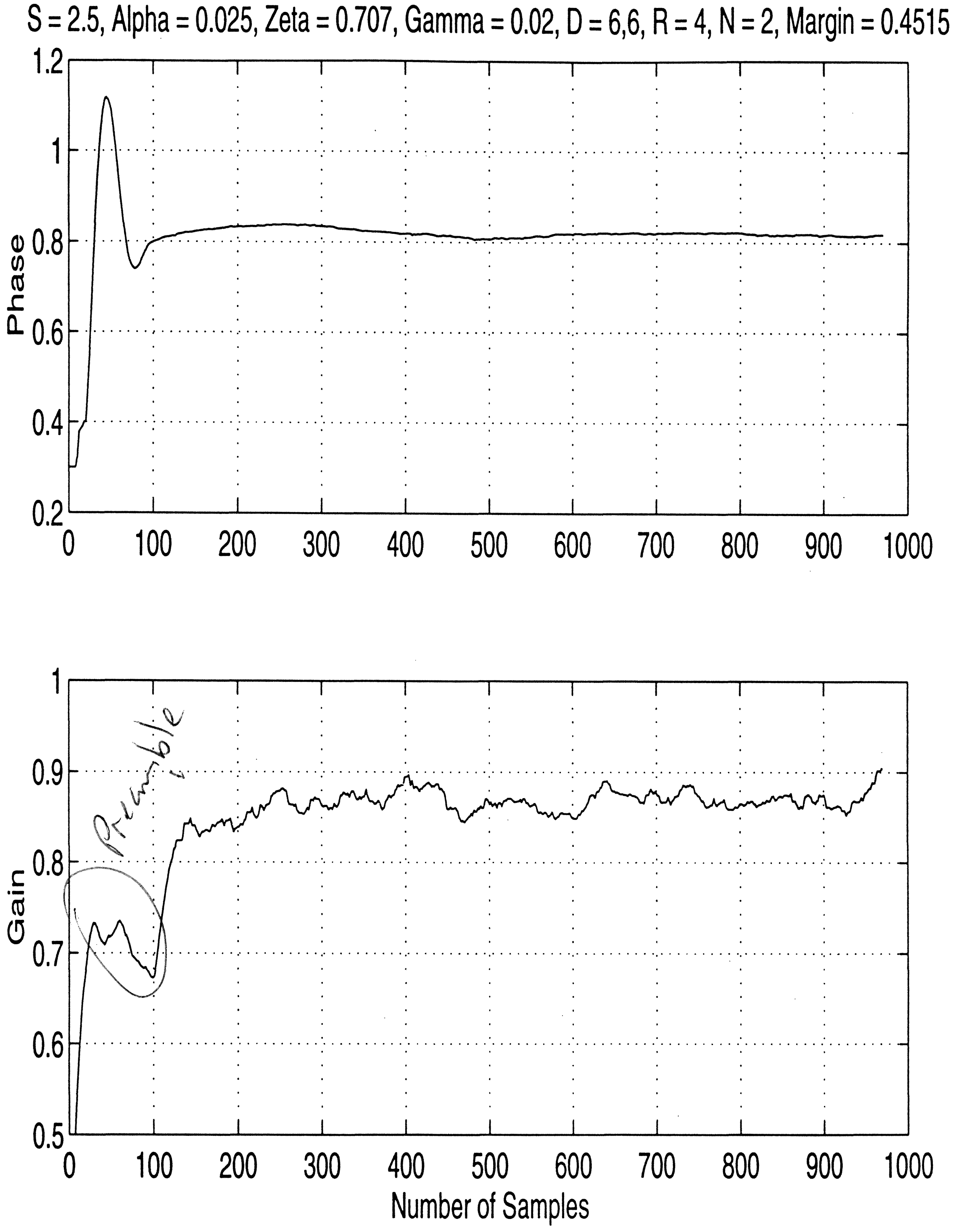
y_n = Input value at time n

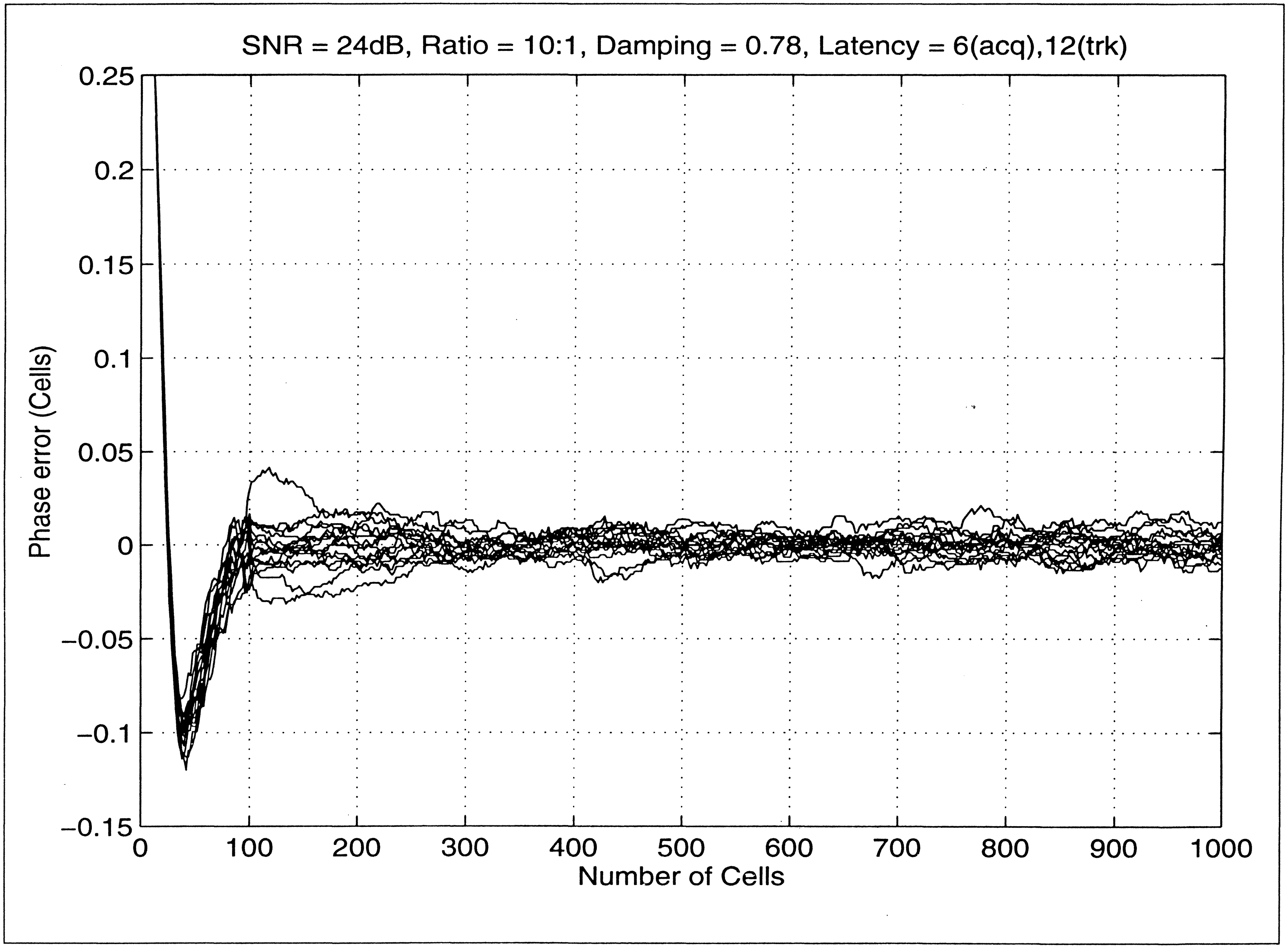
y_{n-1} = Input value at time n-1

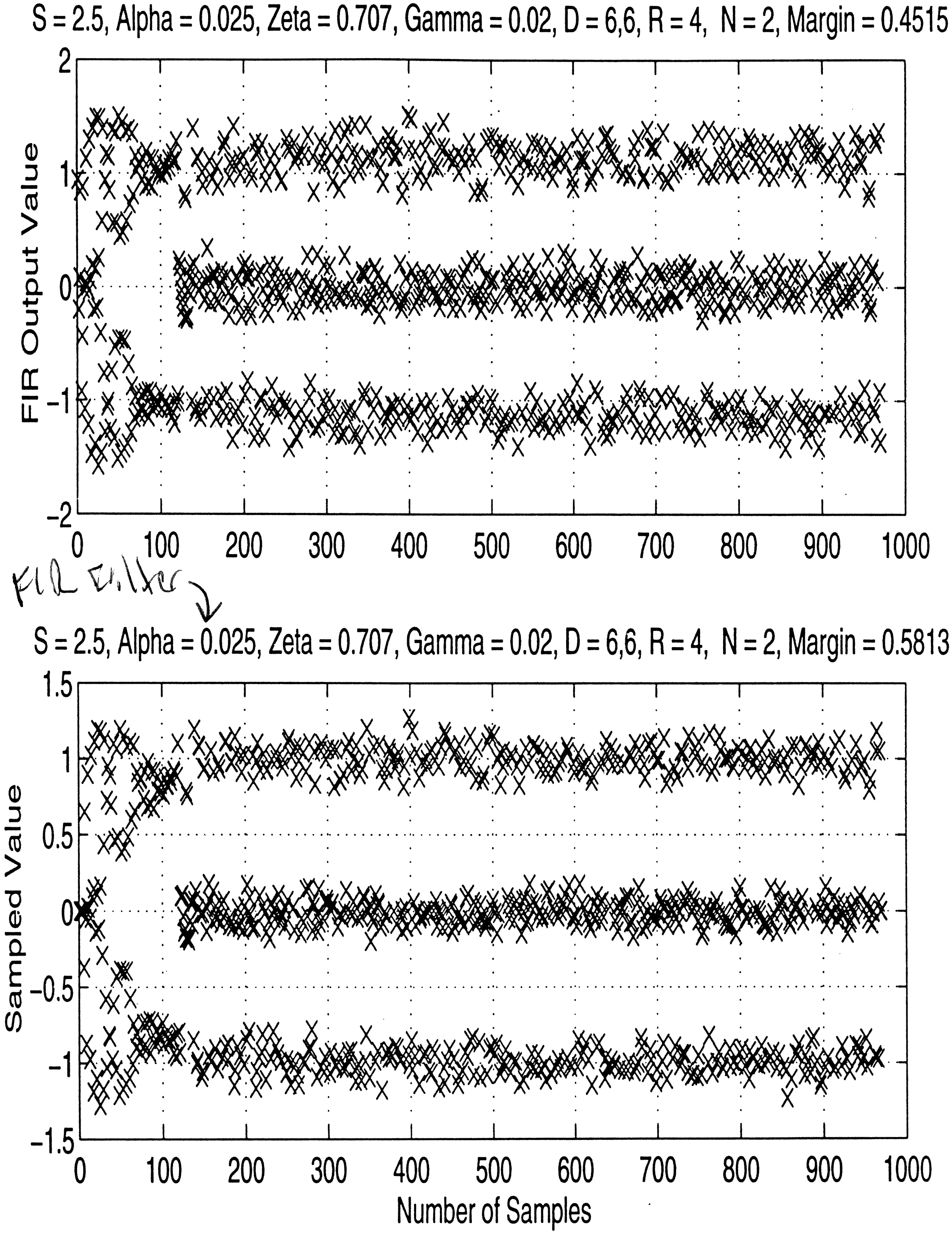
$\hat{x}_n$ = Slicer output for y_n

$\hat{x}_{n-1}$ = Slicer output for y_{n-1}

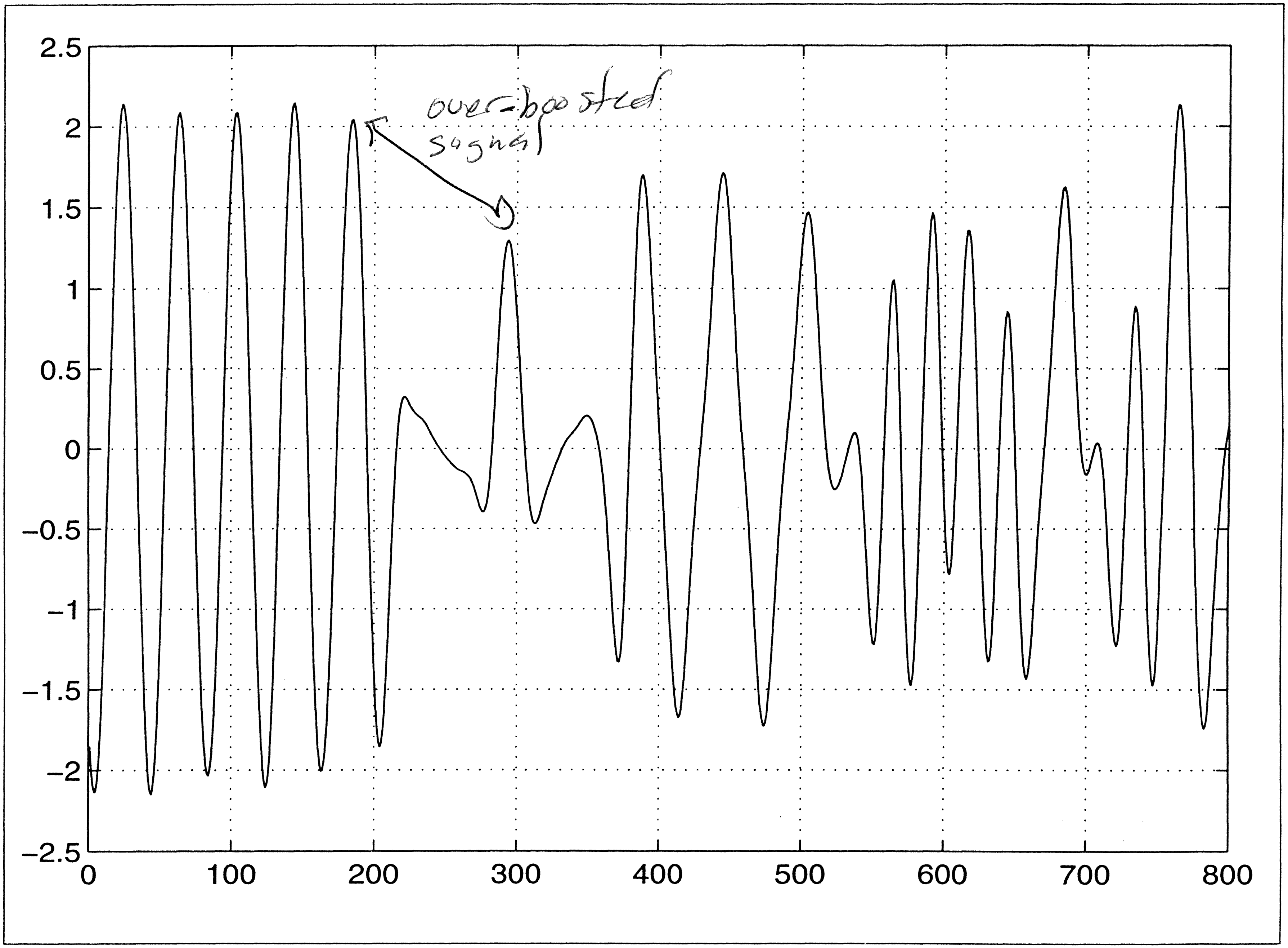
SNR=24dB

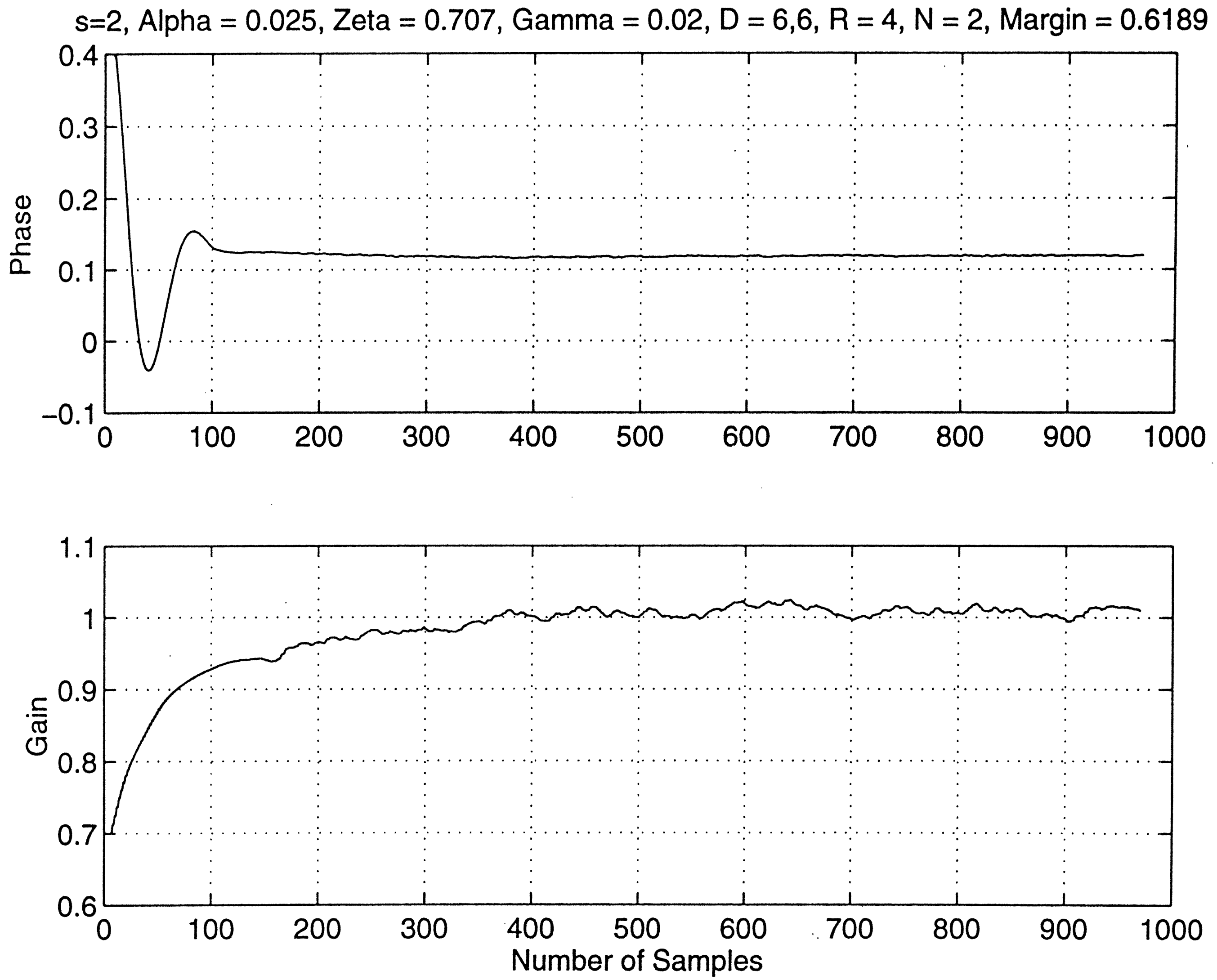

S = 2.5, Alpha = 0.025, Zeta = 0.707, Gamma = 0.02, D = 6,6, R = 4, N = 2, Margin = 0.4515
Phase
1.2
1
0.8
0.6
0.4
0.2
0
100
200
300
400
500
600
700
800
900
1000
Gain
1
0.9
0.8
0.7
0.6
0.5
Preamble
Number of Samples


SNR = 24dB, Ratio = 10:1, Damping = 0.78, Latency = 6(acq),12(trk)
Phase error (Cells)
0.25
0.2
0.15
0.1
0.05
0
−0.05
−0.1
−0.15
0
100
200
300
400
500
600
700
800
900
1000
Number of Cells

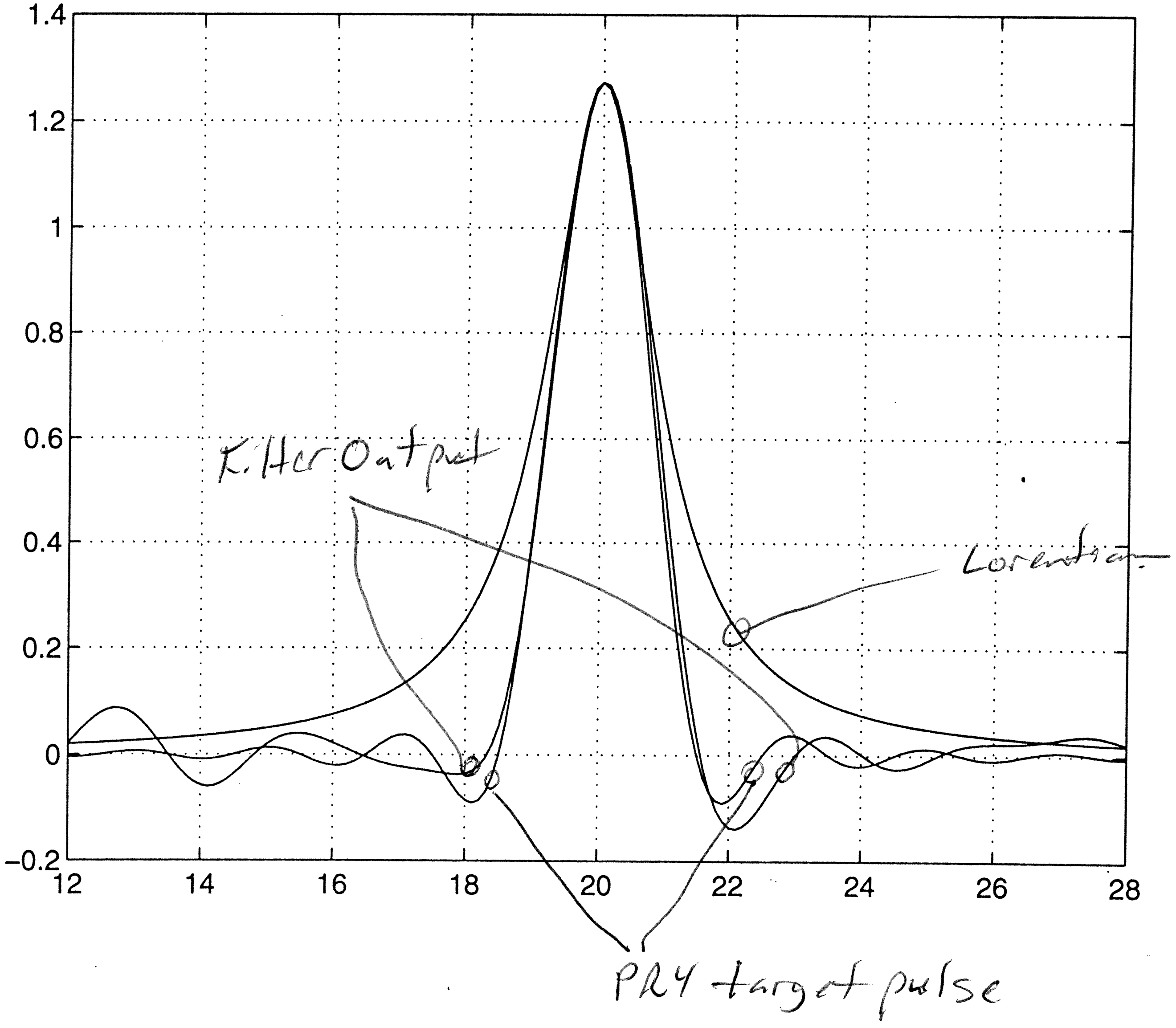

S = 2.5, Alpha = 0.025, Zeta = 0.707, Gamma = 0.02, D = 6,6, R = 4, N = 2, Margin = 0.4515
FIR Output Value
2
1
0
-1
-2
0
100
200
300
400
500
600
700
800
900
1000
S = 2.5, Alpha = 0.025, Zeta = 0.707, Gamma = 0.02, D = 6,6, R = 4, N = 2, Margin = 0.5813
Sampled Value
1.5
1
0.5
0
-0.5
-1
-1.5
0
100
200
300
400
500
600
700
800
900
1000
Number of Samples

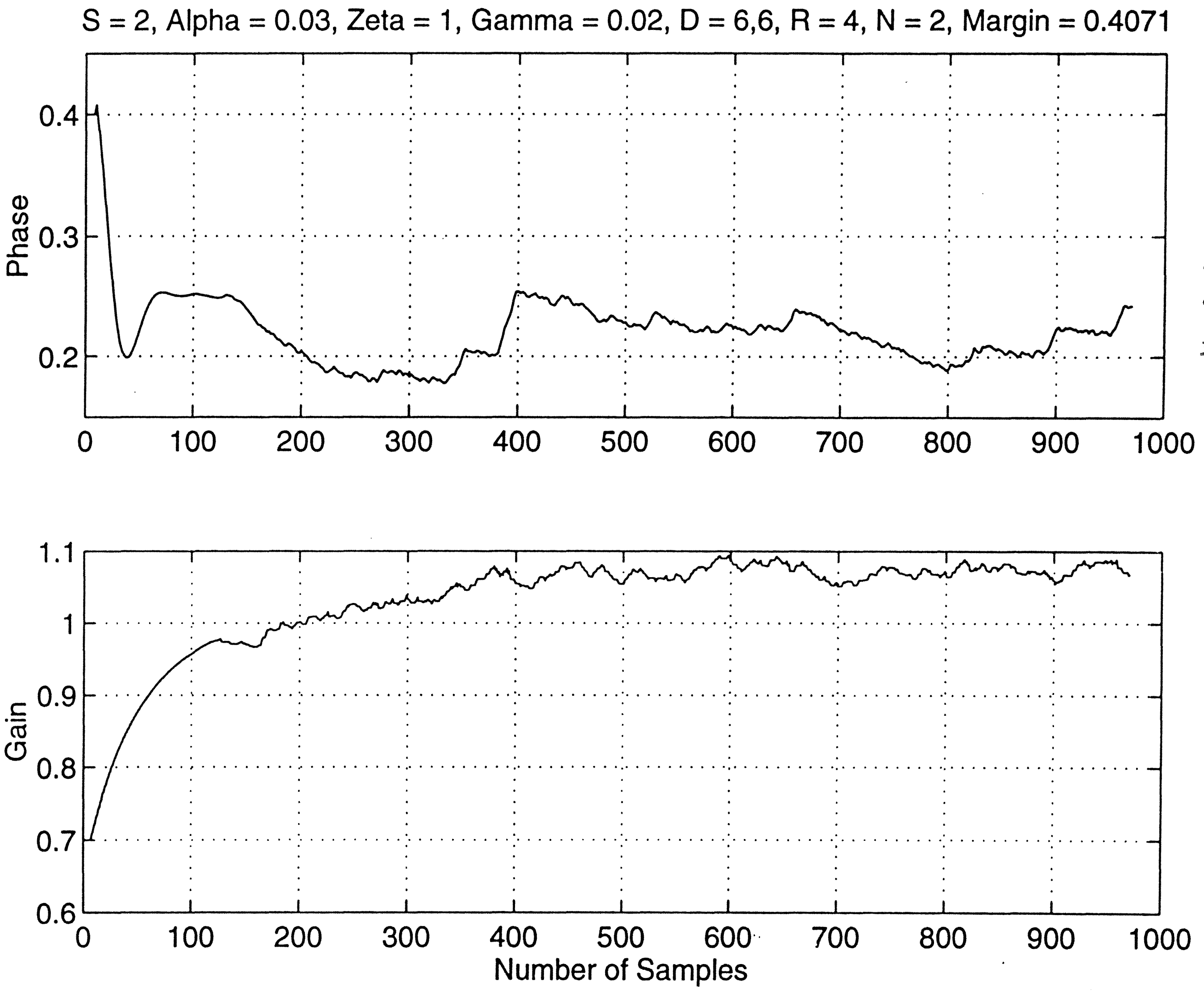
FIR Filter


over-boosted
signal
2.5
2
1.5
1
0.5
0
−0.5
−1
−1.5
−2
−2.5
0
100
200
300
400
500
600
700
800


s=2, Alpha = 0.025, Zeta = 0.707, Gamma = 0.02, D = 6,6, R = 4, N = 2, Margin = 0.6189
Phase
0.4
0.3
0.2
0.1
0
−0.1
0
100
200
300
400
500
600
700
800
900
1000
Gain
1.1
1
0.9
0.8
0.7
0.6
Number of Samples

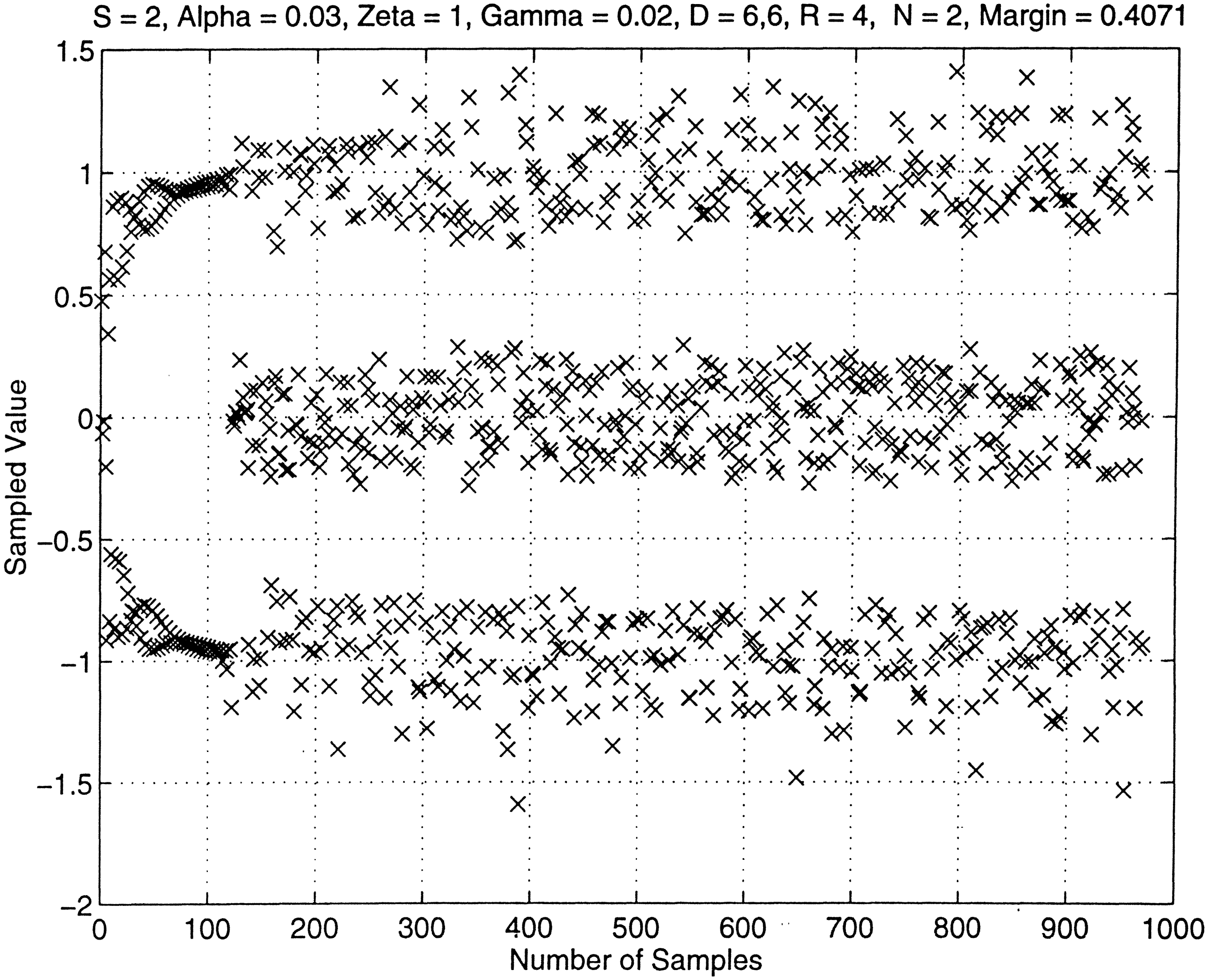
Distorted output



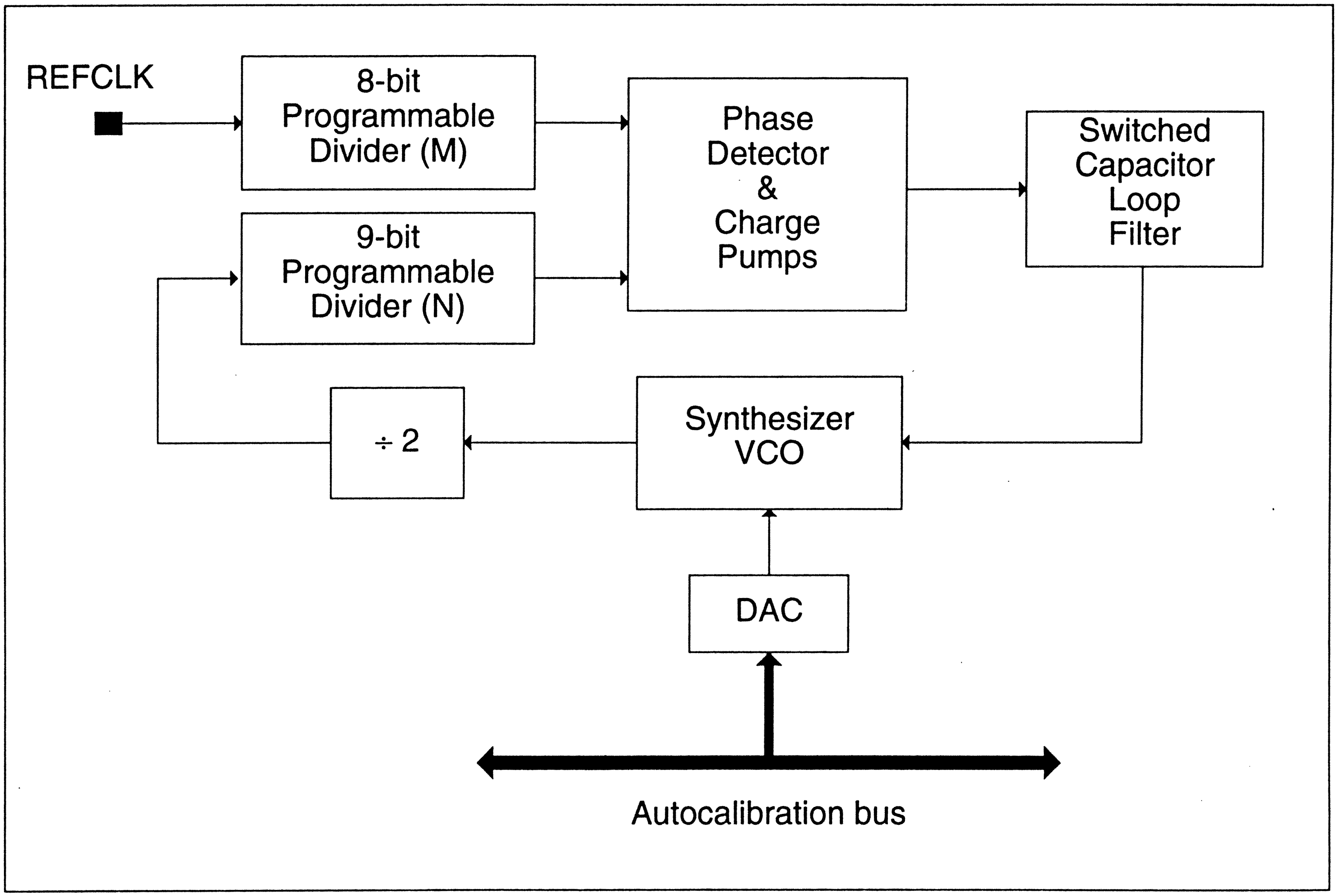


Period
Phenomena
due to phase
~~sy~~asymmetry.

Linear filters important


S = 2, Alpha = 0.03, Zeta = 1, Gamma = 0.02, D = 6,6, R = 4, N = 2, Margin = 0.4071
Sampled Value
1.5
1
0.5
0
−0.5
−1
−1.5
−2
0
100
200
300
400
500
600
700
800
900
1000
Number of Samples

FREQUENCY SYNTHESIZER



REFCLK

8-bit Programmable Divider (M)

9-bit Programmable Divider (N)

Phase Detector & Charge Pumps

Switched Capacitor Loop Filter

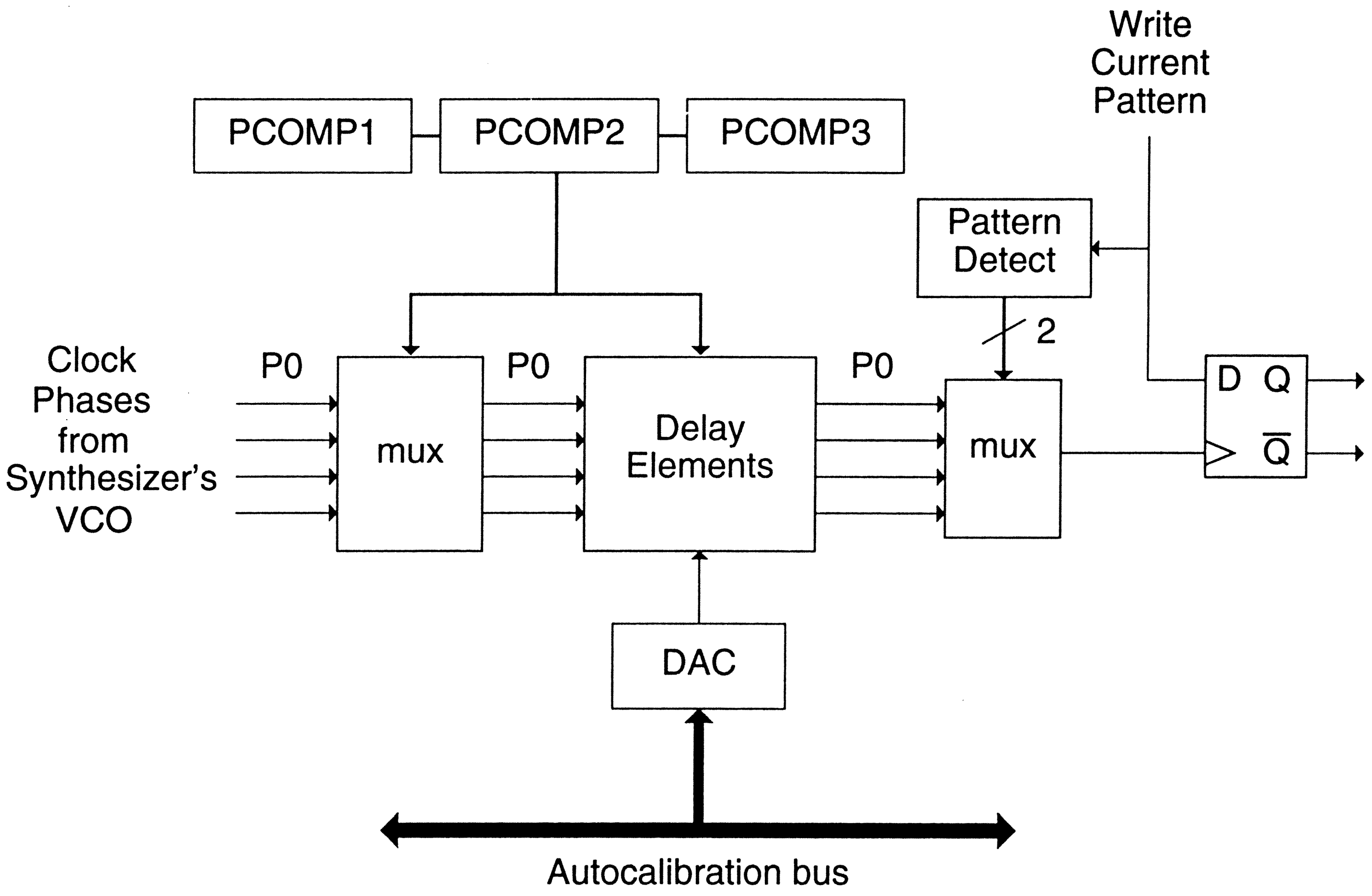
÷ 2

Synthesizer VCO

DAC

Autocalibration bus

WRITE PRECOMPENSATION



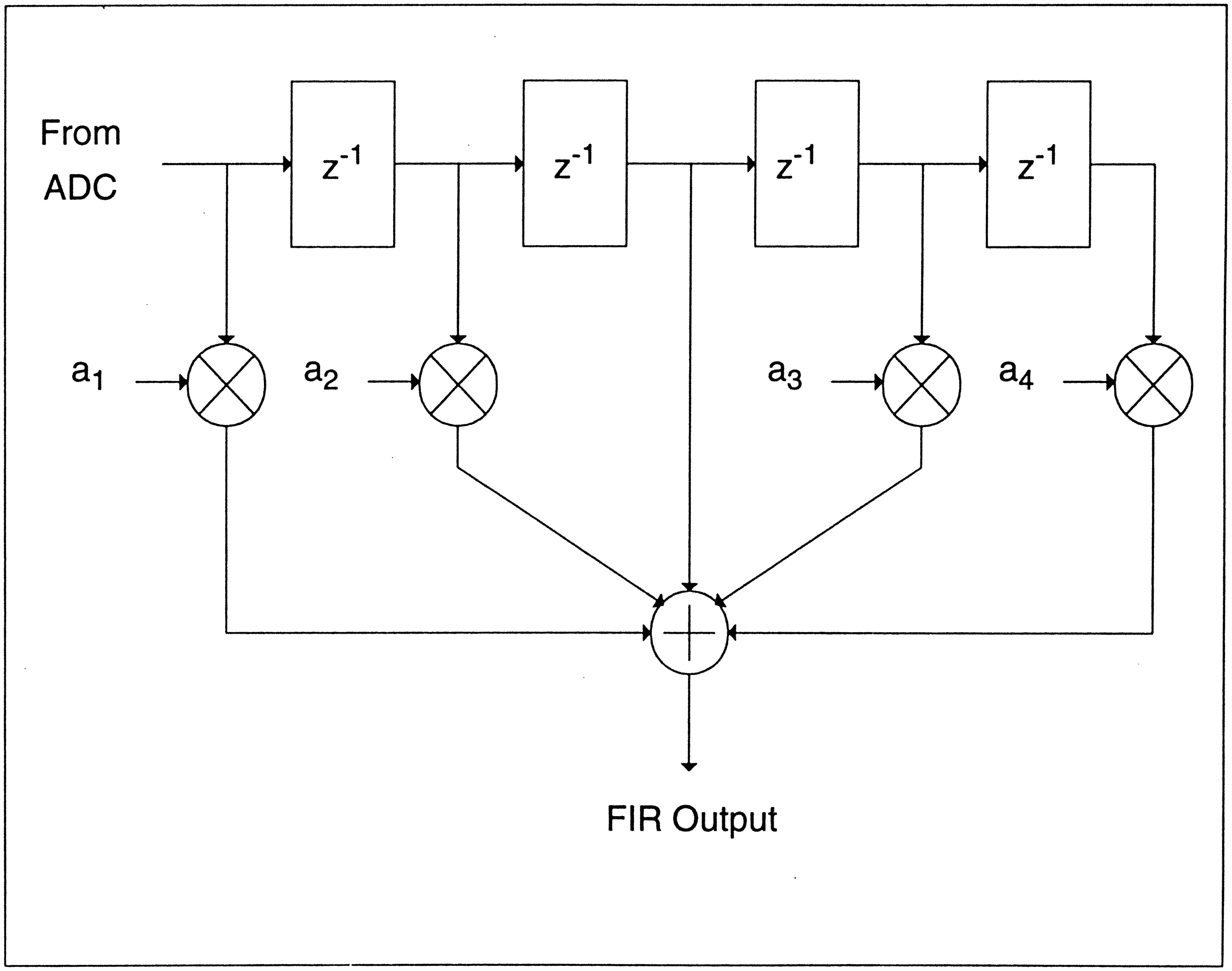
WRITE PRECOMPENSATION-cont

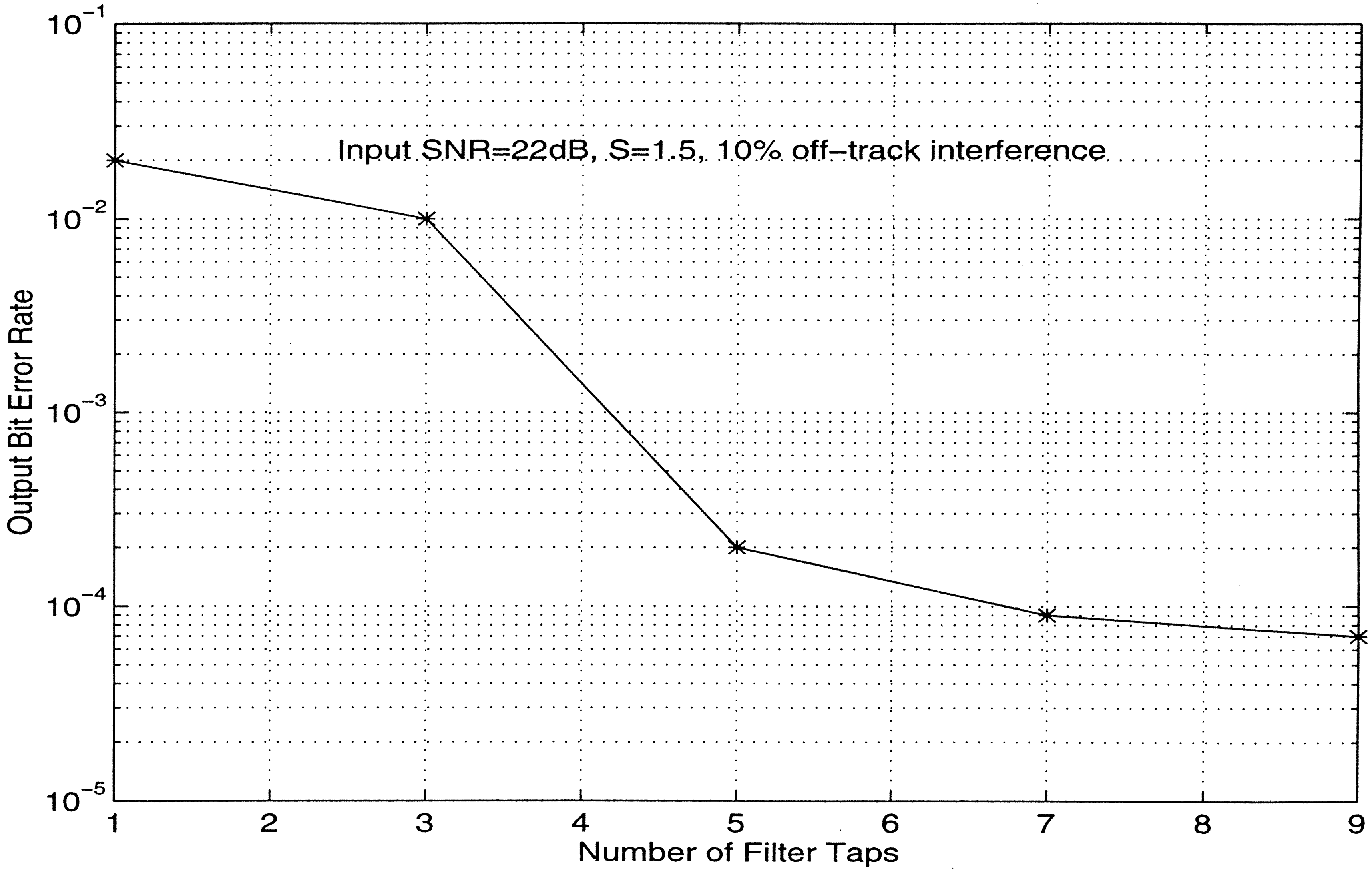
Write Pattern			Write Precomp
t_{-2}	t_{-1}	t_0	
N	N	T	No Precomp
T	N	T	PCOMP1
T	T	T	PCOMP2
N	T	T	PCOMP3

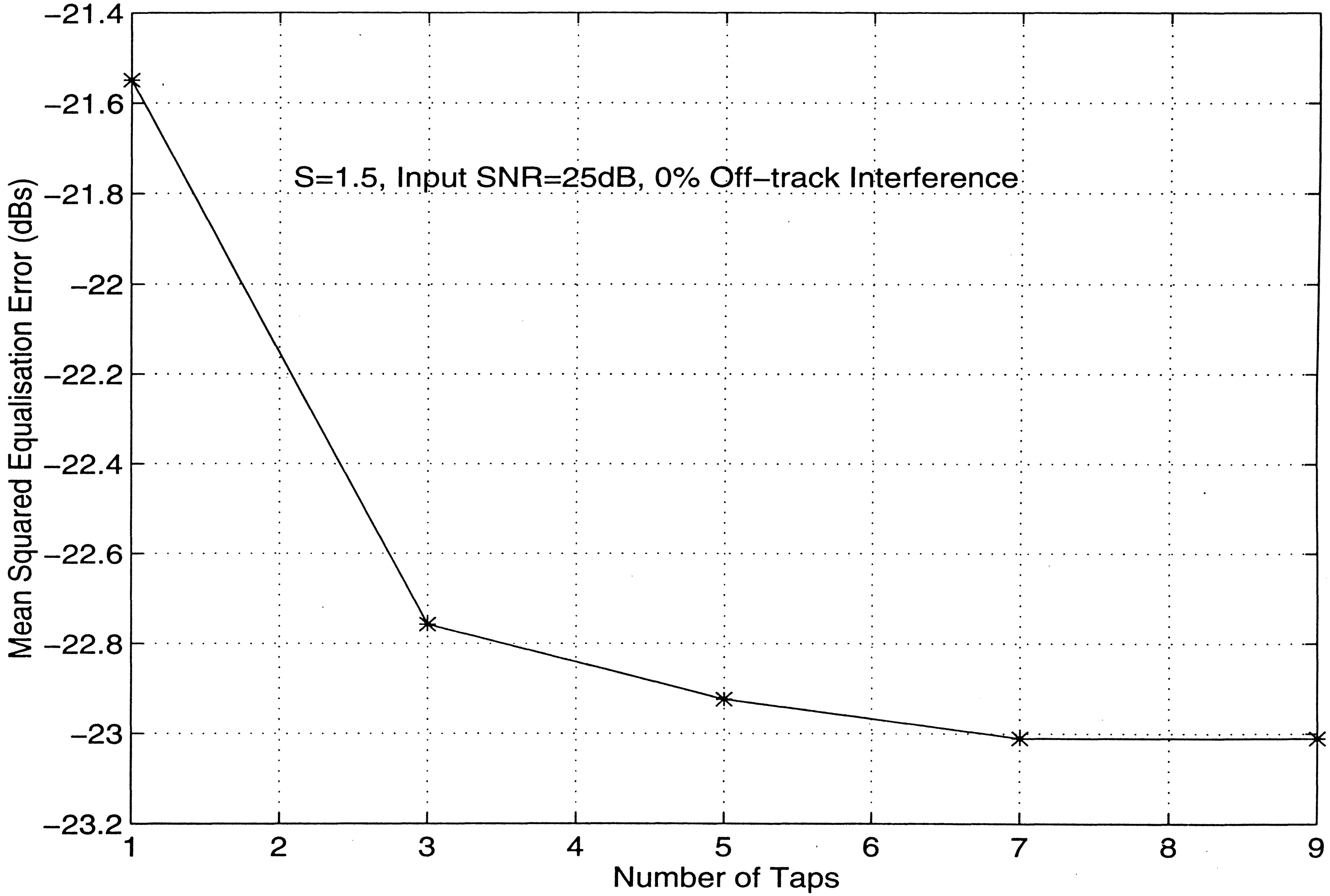
CHANNEL QUALITY/CALIBRATION

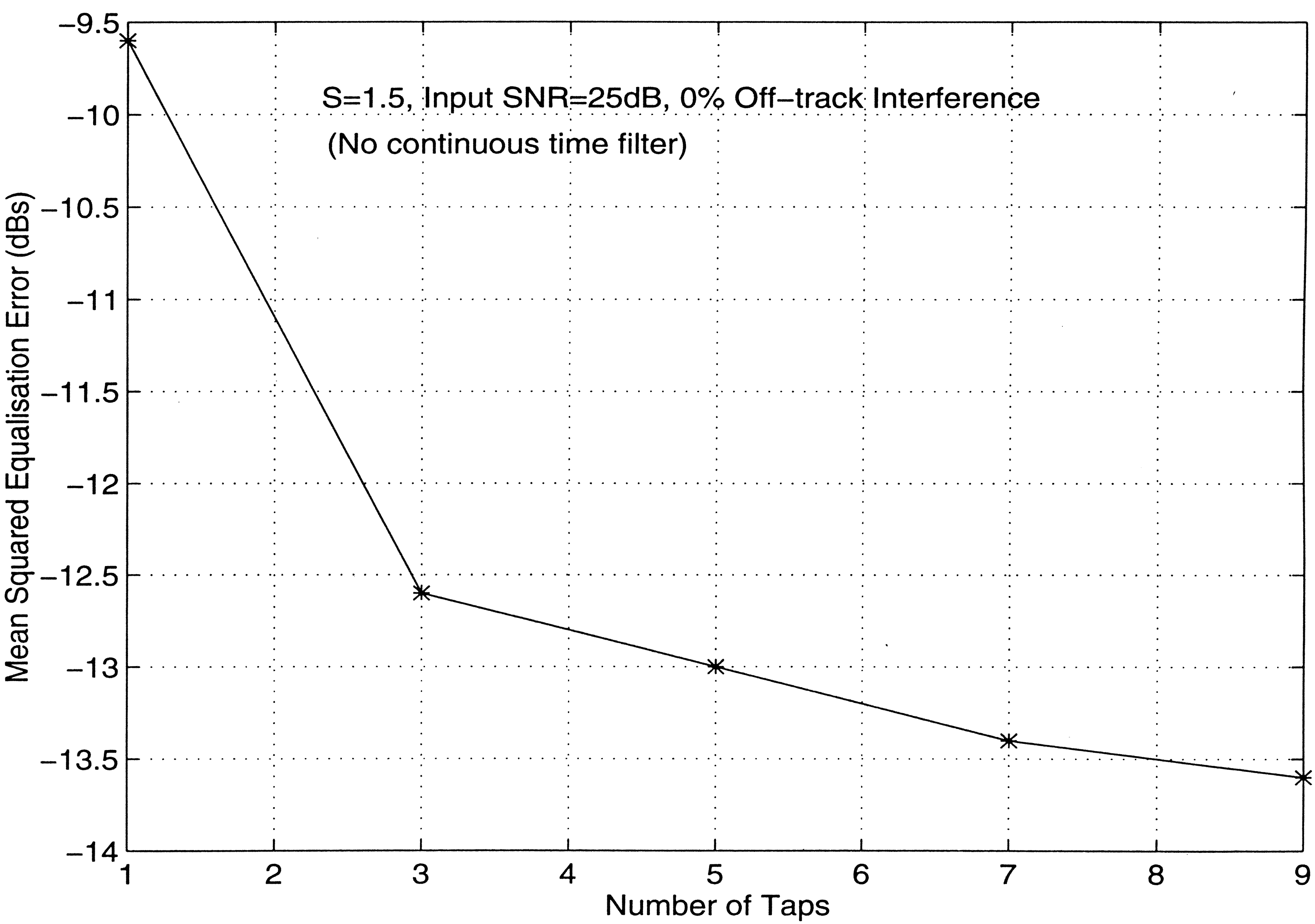
- QUANTITIES:
  - -- NUMBER OF ERRORS
  - -- PHASE DETECTOR OUTPUT
  - -- VCO CONTROL
  - -- AGC CONTROL
  - -- Error in +1 values
  - -- Error in -1 values
  - -- Error in 0 values
  - -- ERROR IN ALL VALUES
- MATHEMATICAL OPERATION ON THE QUANTITIES
  - -- NO OPERATION
  - -- ABSOLUTE VALUE
  - -- SQUARED VALUE
- FEATURE TO REPORT
  - -- MINIMUM
  - -- MAXIMUM
  - -- SUM

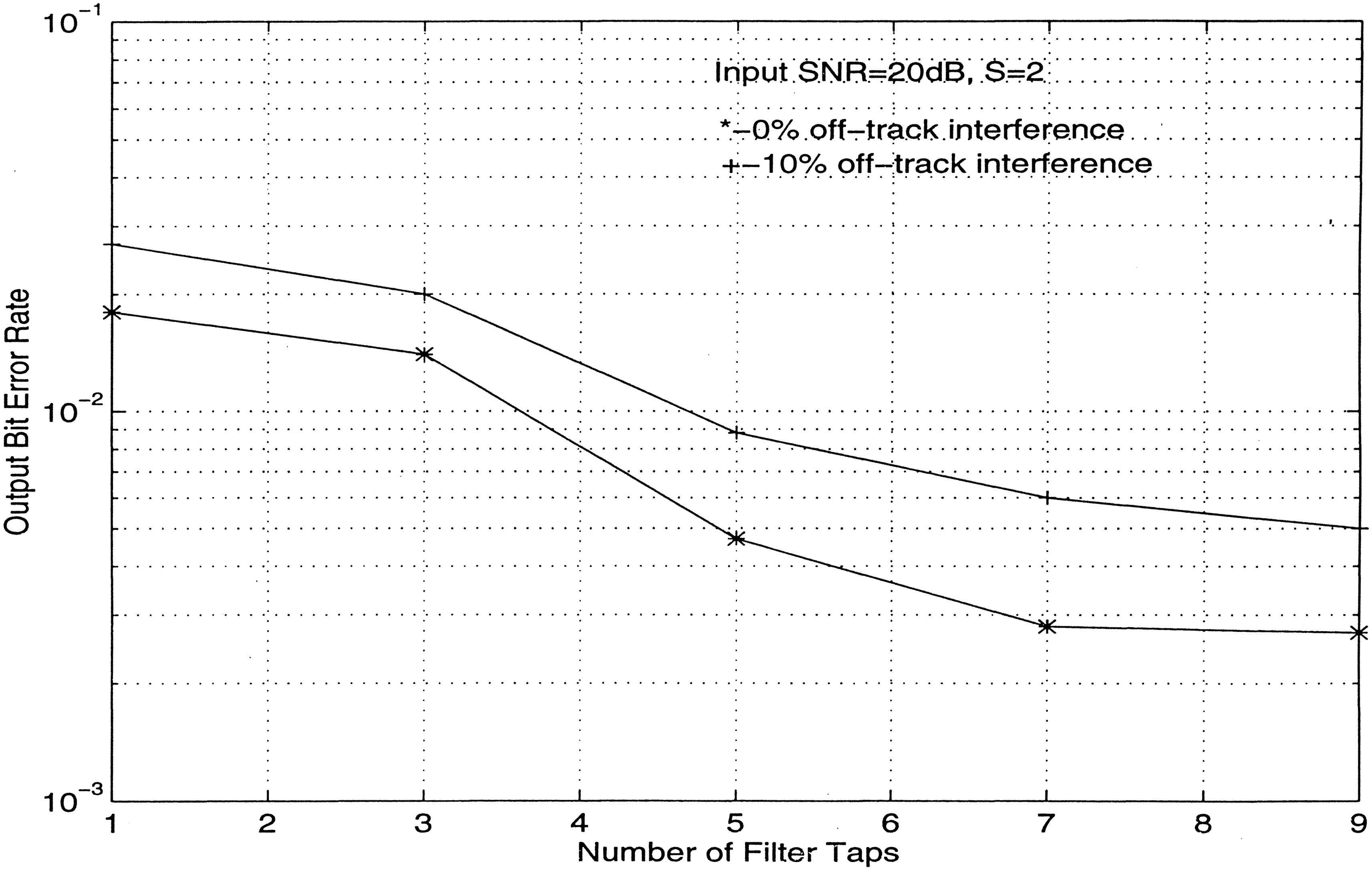
FIR FILTER



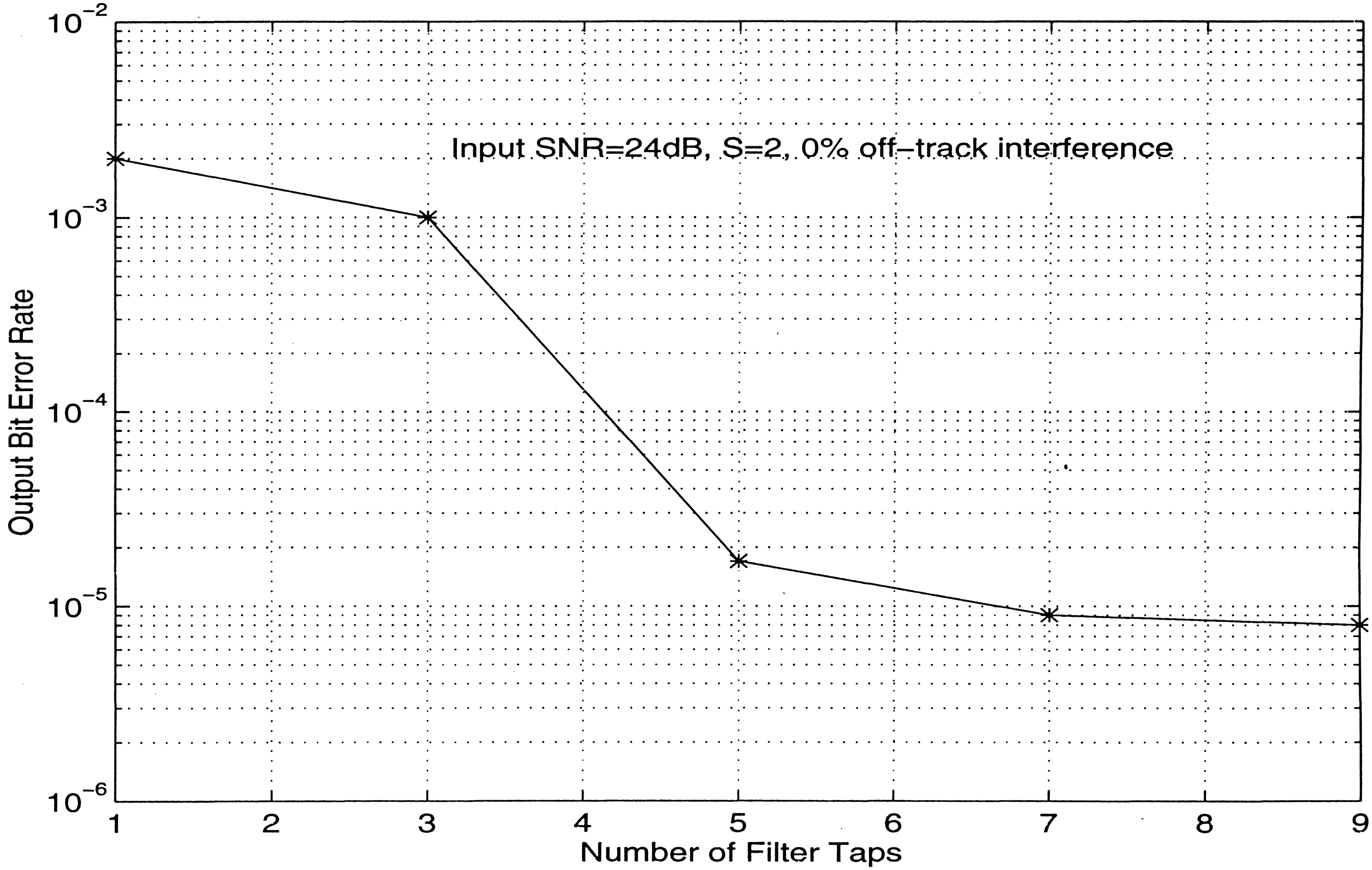

Input SNR=22dB, S=1.5, 10% off-track interference
Output Bit Error Rate
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
1
2
3
4
5
6
7
8
9
Number of Filter Taps

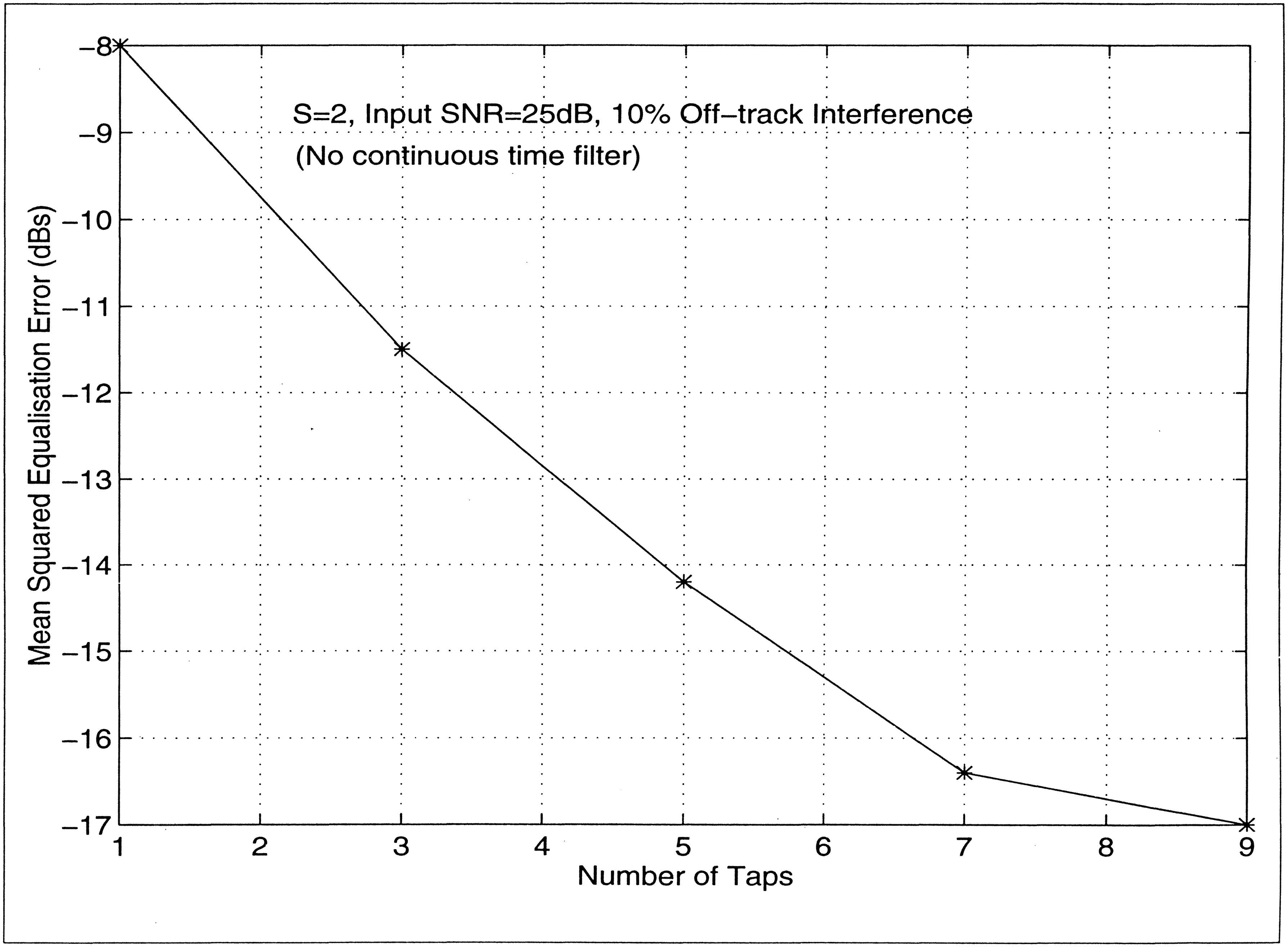

S=1.5, Input SNR=25dB, 0% Off–track Interference
Mean Squared Equalisation Error (dBs)
−21.4
−21.6
−21.8
−22
−22.2
−22.4
−22.6
−22.8
−23
−23.2
1
2
3
4
5
6
7
8
9
Number of Taps

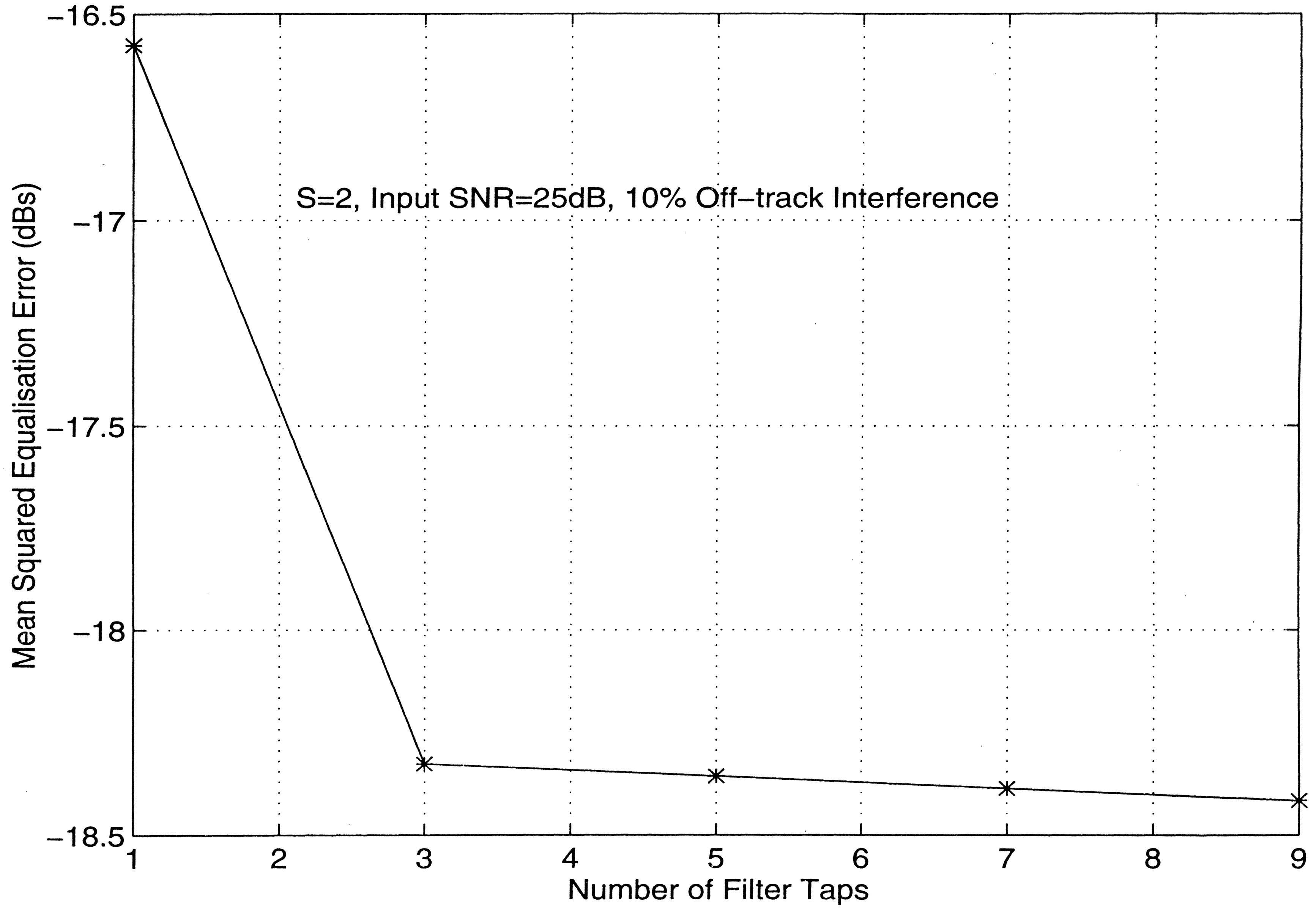

S=1.5, Input SNR=25dB, 0% Off−track Interference
(No continuous time filter)
Mean Squared Equalisation Error (dBs)
Number of Taps
−9.5
−10
−10.5
−11
−11.5
−12
−12.5
−13
−13.5
−14
1
2
3
4
5
6
7
8
9

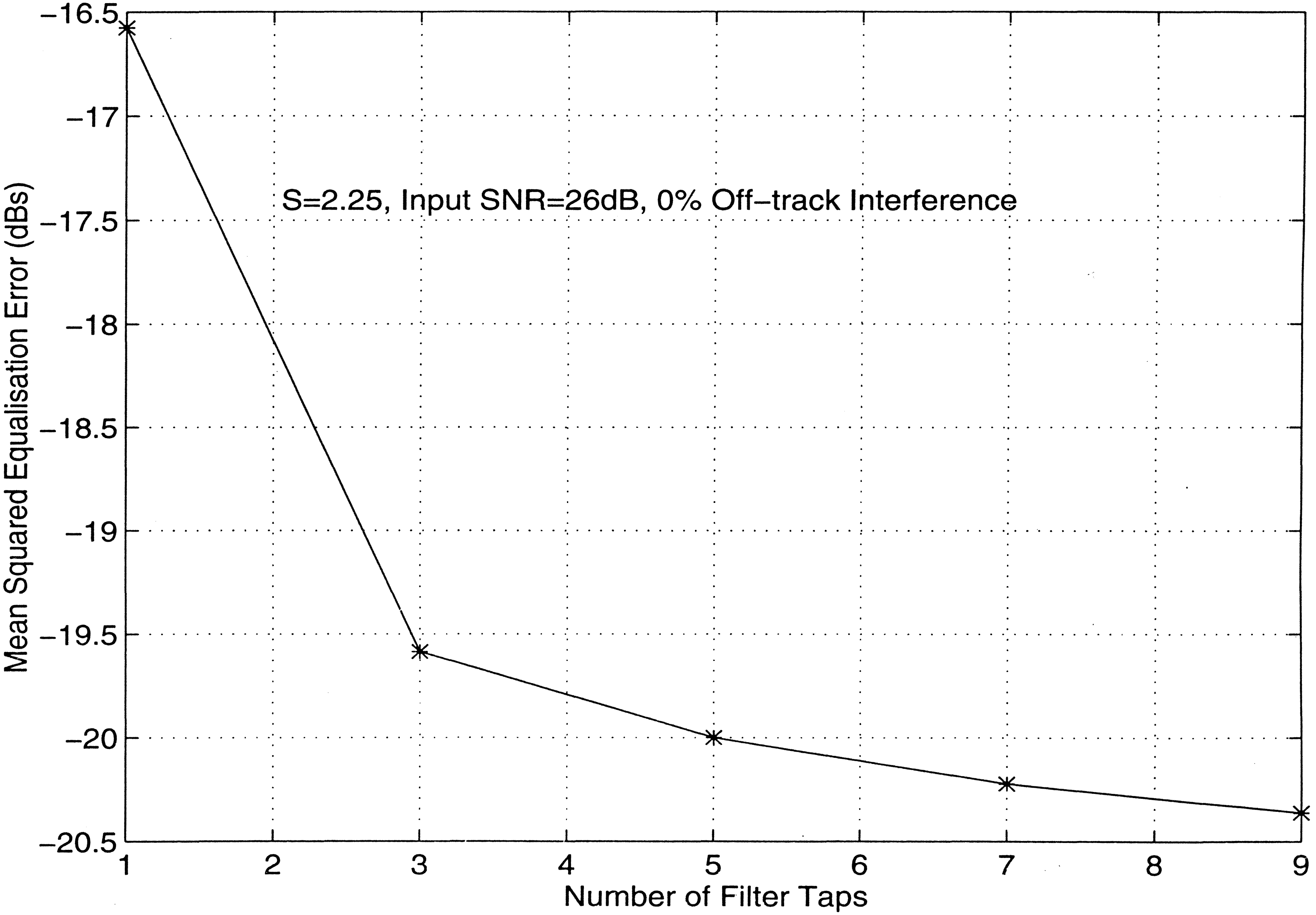


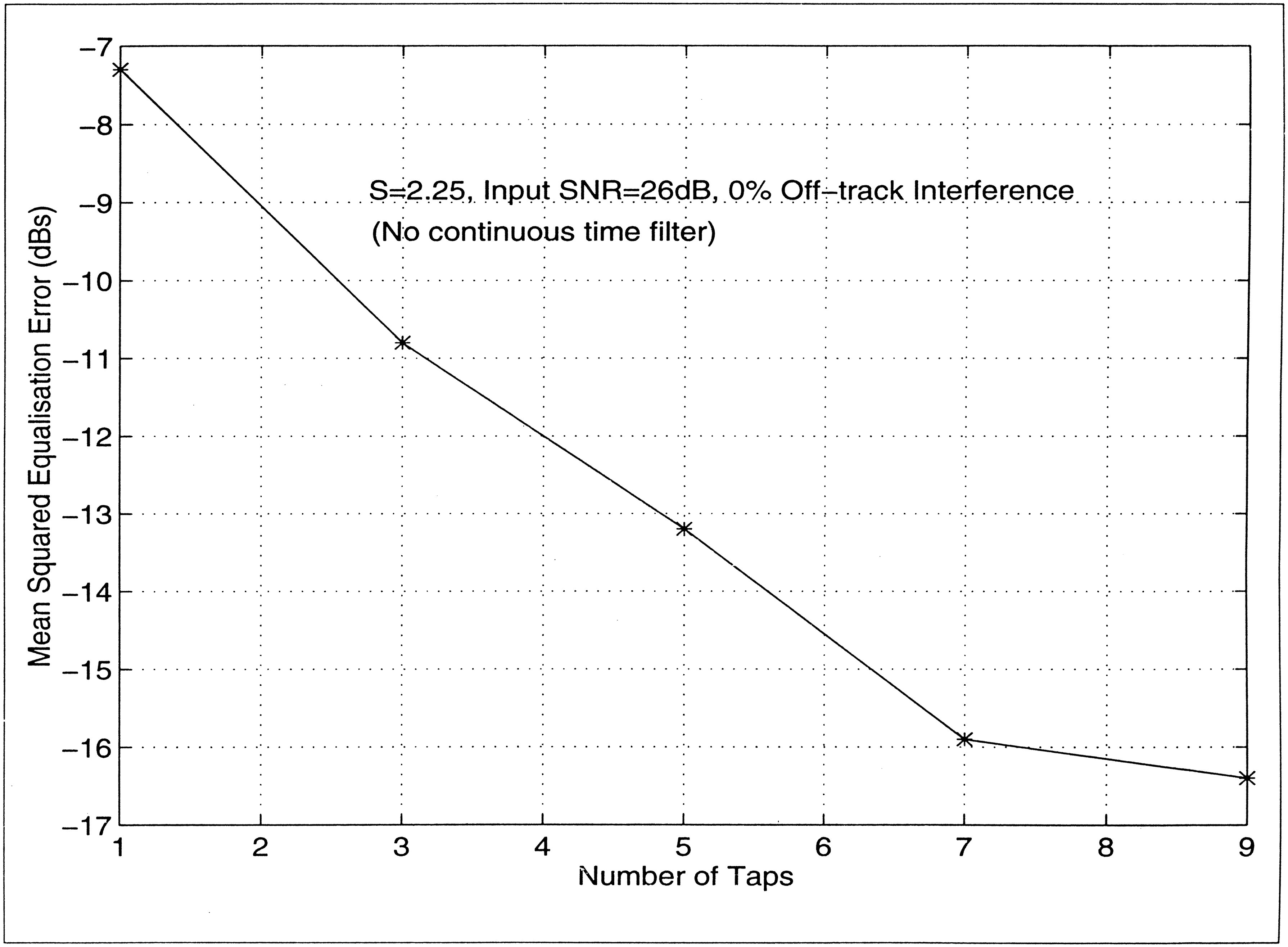
Input SNR=20dB, S=2
*–0% off–track interference
+–10% off–track interference
Output Bit Error Rate
Number of Filter Taps
10^{-1}
10^{-2}
10^{-3}
1
2
3
4
5
6
7
8
9


Input SNR=24dB, S=2, 0% off-track interference
Output Bit Error Rate
Number of Filter Taps
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
1
2
3
4
5
6
7
8
9

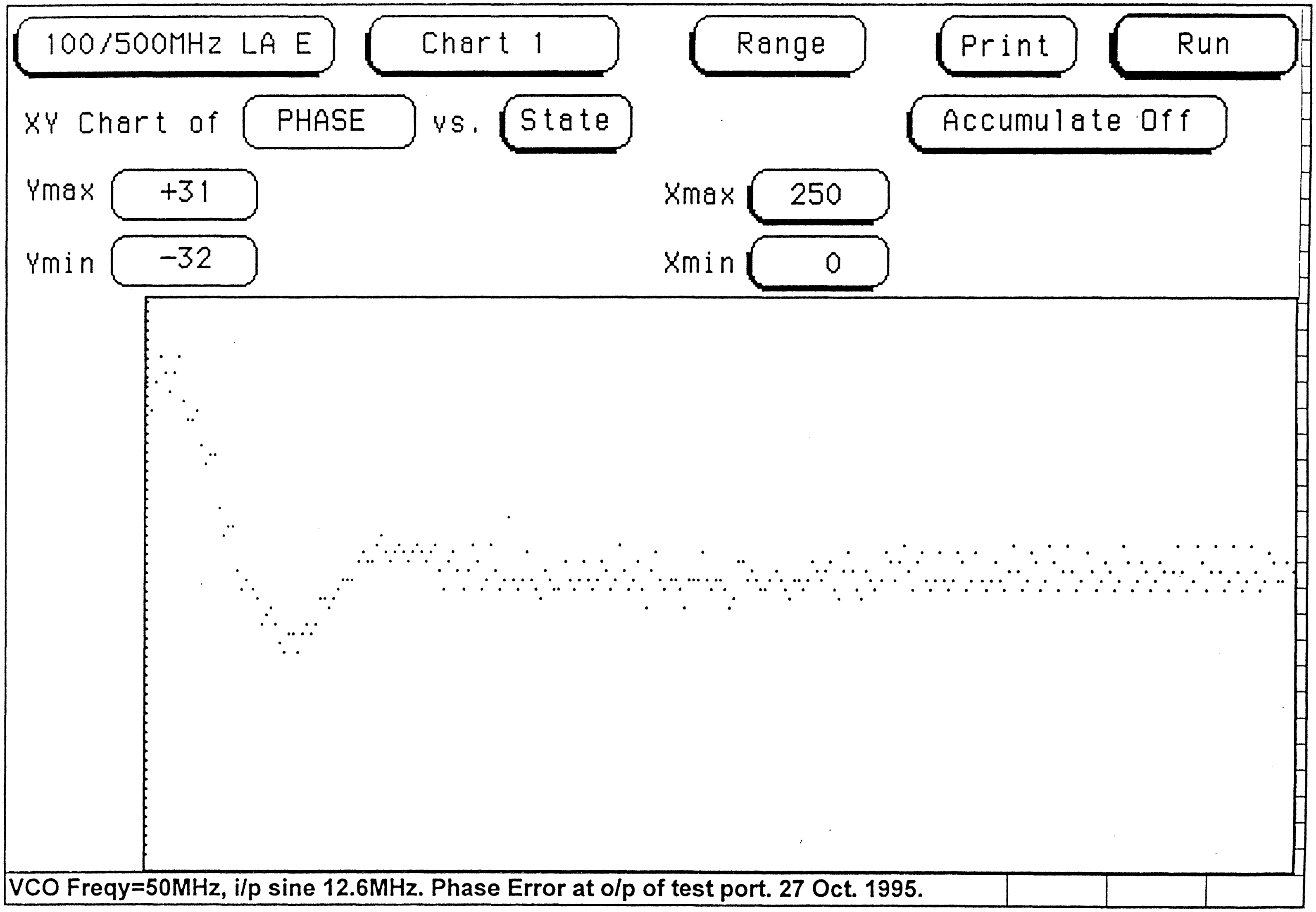

S=2, Input SNR=25dB, 10% Off–track Interference
(No continuous time filter)
Mean Squared Equalisation Error (dBs)
Number of Taps
−8
−9
−10
−11
−12
−13
−14
−15
−16
−17
1
2
3
4
5
6
7
8
9


S=2, Input SNR=25dB, 10% Off–track Interference
Mean Squared Equalisation Error (dBs)
−16.5
−17
−17.5
−18
−18.5
1
2
3
4
5
6
7
8
9
Number of Filter Taps


-16.5
-17
-17.5
-18
-18.5
-19
-19.5
-20
-20.5
1
2
3
4
5
6
7
8
9
Number of Filter Taps
Mean Squared Equalisation Error (dBs)
S=2.25, Input SNR=26dB, 0% Off-track Interference


S=2.25, Input SNR=26dB, 0% Off–track Interference
(No continuous time filter)
Mean Squared Equalisation Error (dBs)
Number of Taps
−7
−8
−9
−10
−11
−12
−13
−14
−15
−16
−17
1
2
3
4
5
6
7
8
9

Phase Error. 27 Oct. 1995



XY Chart of PHASE vs. State

Ymax +31

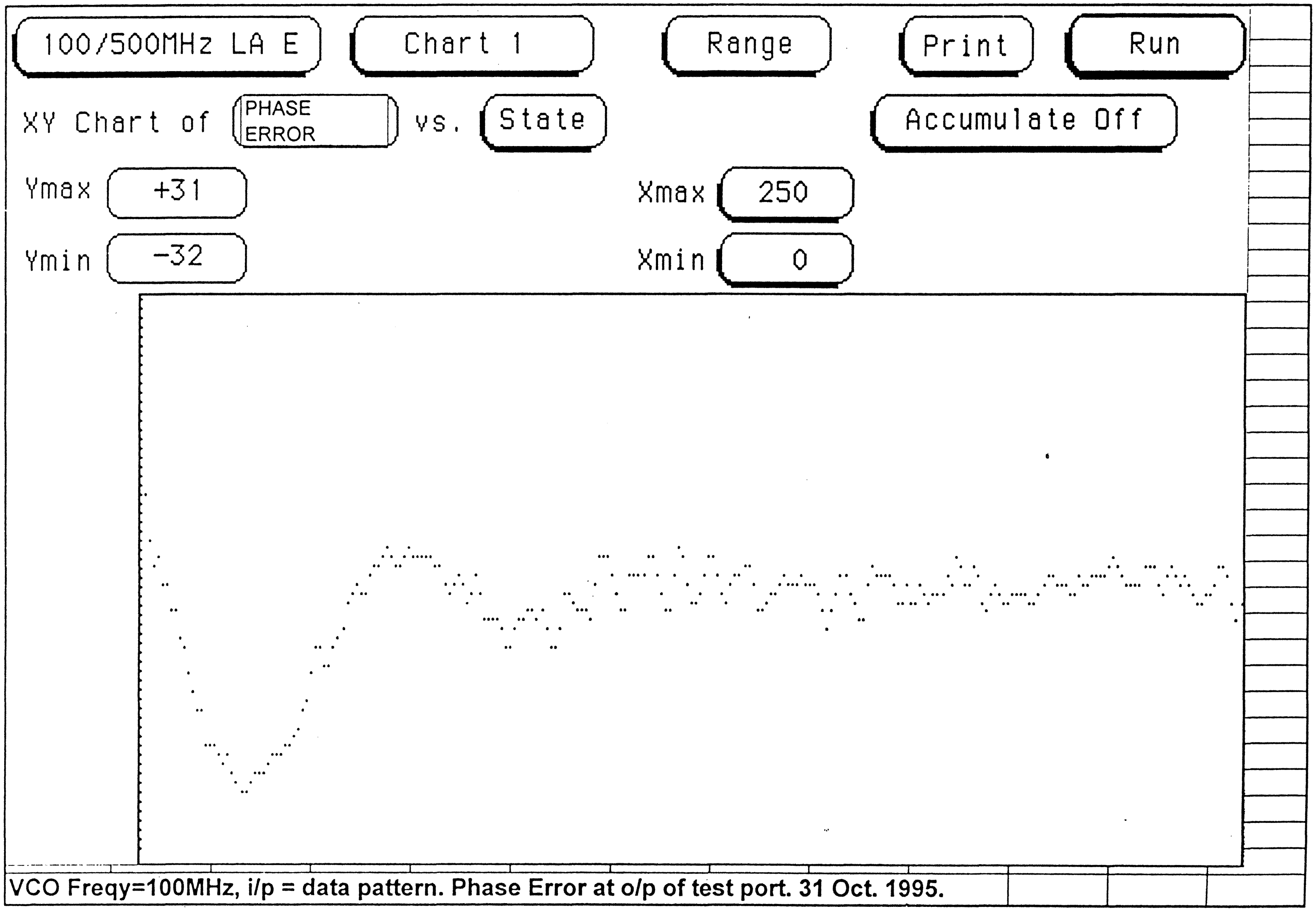
Ymin -32

Xmax 250

Xmin 0

VCO Freqy=50MHz, i/p sine 12.6MHz. Phase Error at o/p of test port. 27 Oct. 1995.

Phase Error



XY Chart of PHASE ERROR vs. State

Ymax +31

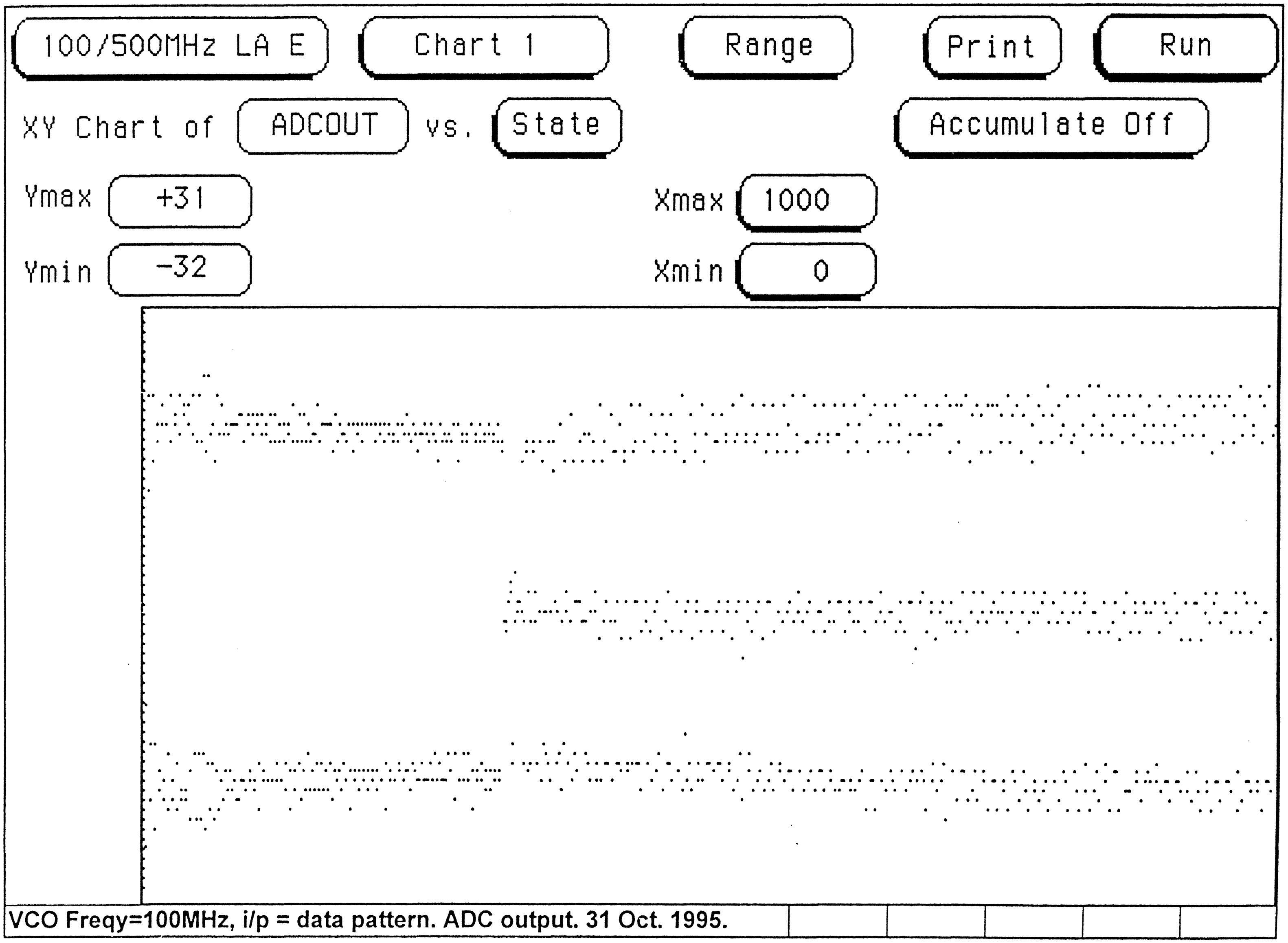
Ymin -32

Xmax 250

Xmin 0

VCO Freqy=100MHz, i/p = data pattern. Phase Error at o/p of test port. 31 Oct. 1995.

ADC(data)



XY Chart of ADCOUT vs. State

Ymax +31

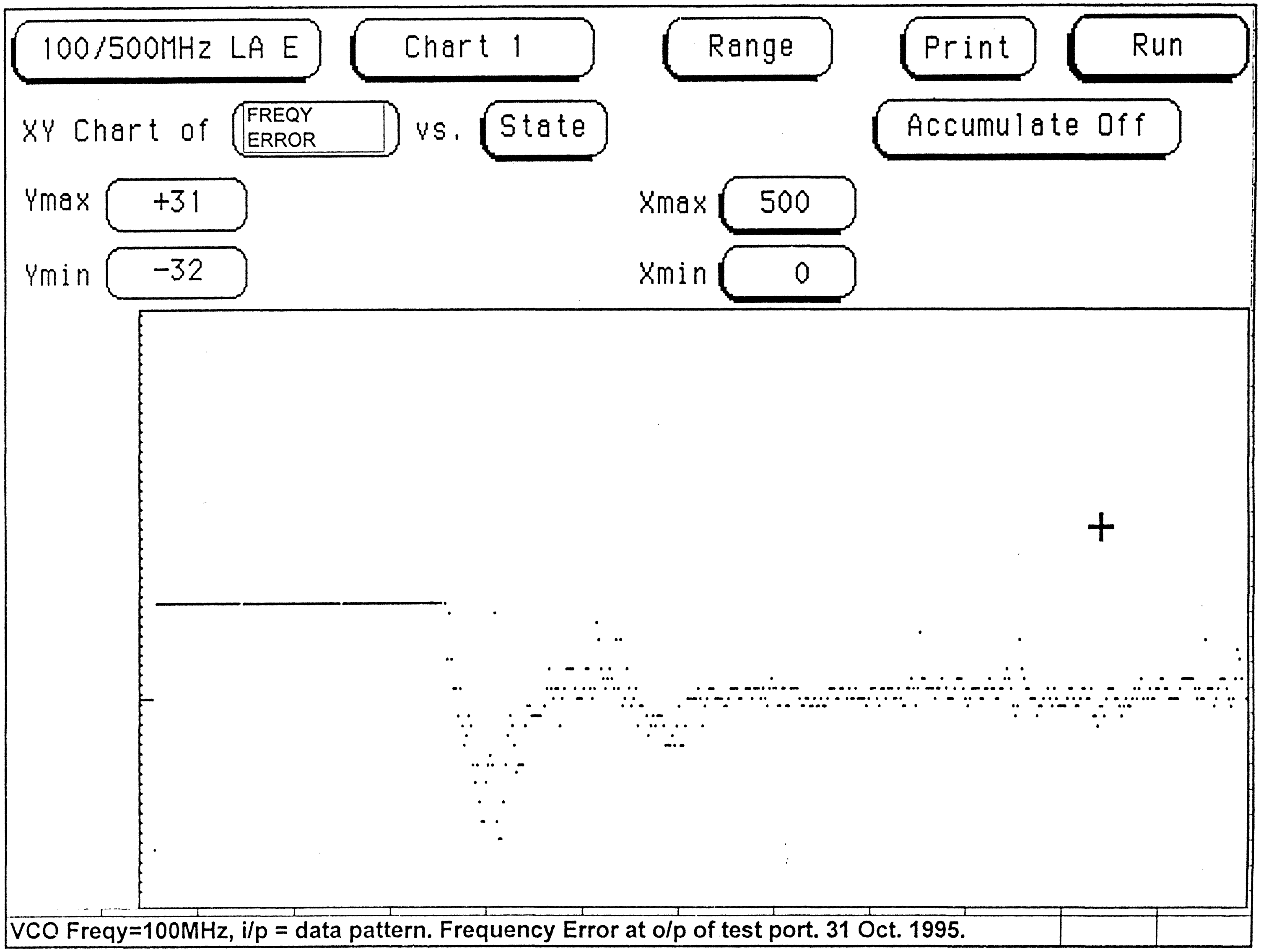
Ymin -32

Xmax 1000

Xmin 0

VCO Freqy=100MHz, i/p = data pattern. ADC output. 31 Oct. 1995.

Frequency Error (Zoom)



XY Chart of FREQY ERROR vs. State

Ymax +31

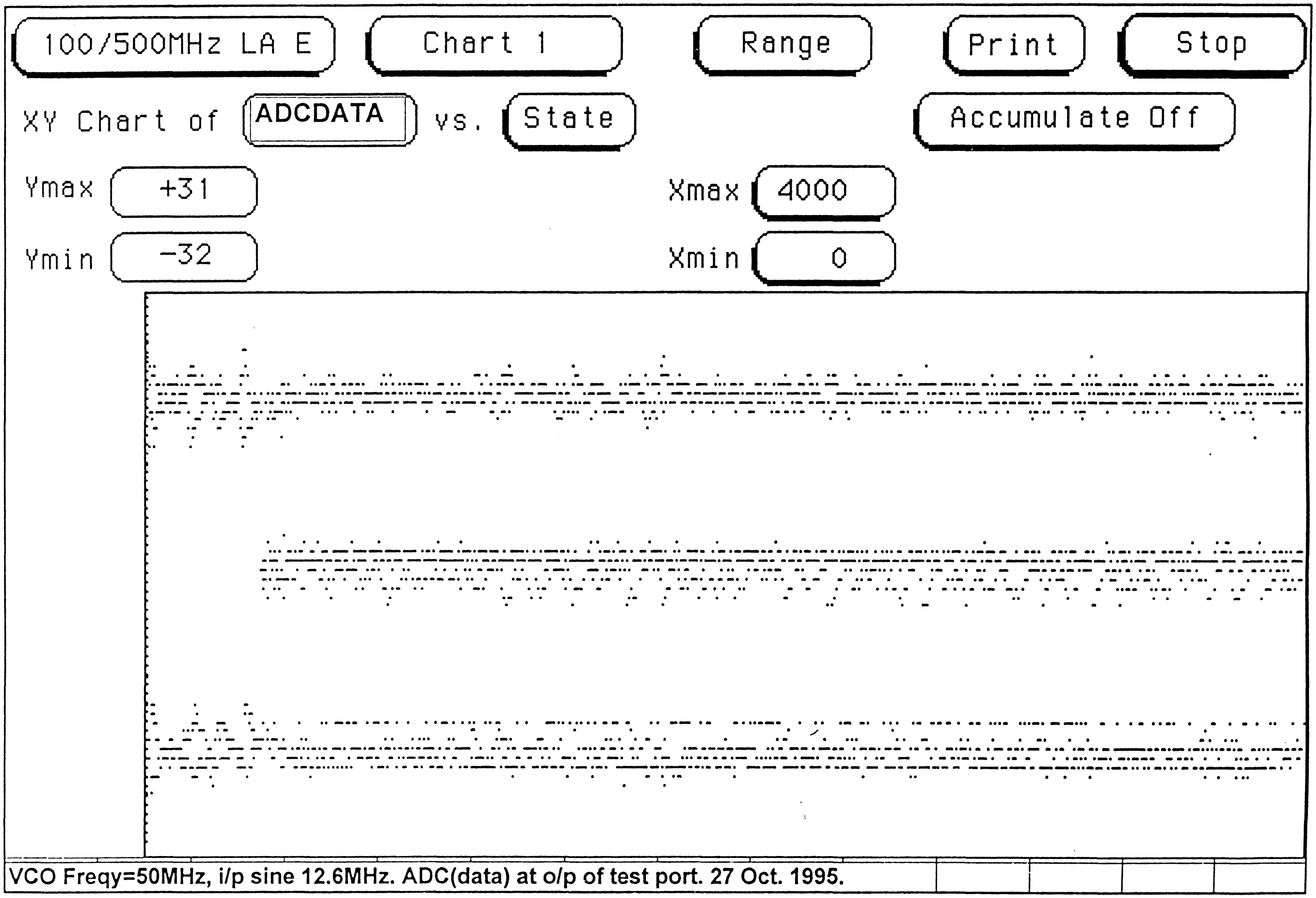
Ymin -32

Xmax 500

Xmin 0

VCO Freqy=100MHz, i/p = data pattern. Frequency Error at o/p of test port. 31 Oct. 1995.

ADC(data)



XY Chart of ADCDATA vs. State

Ymax +31

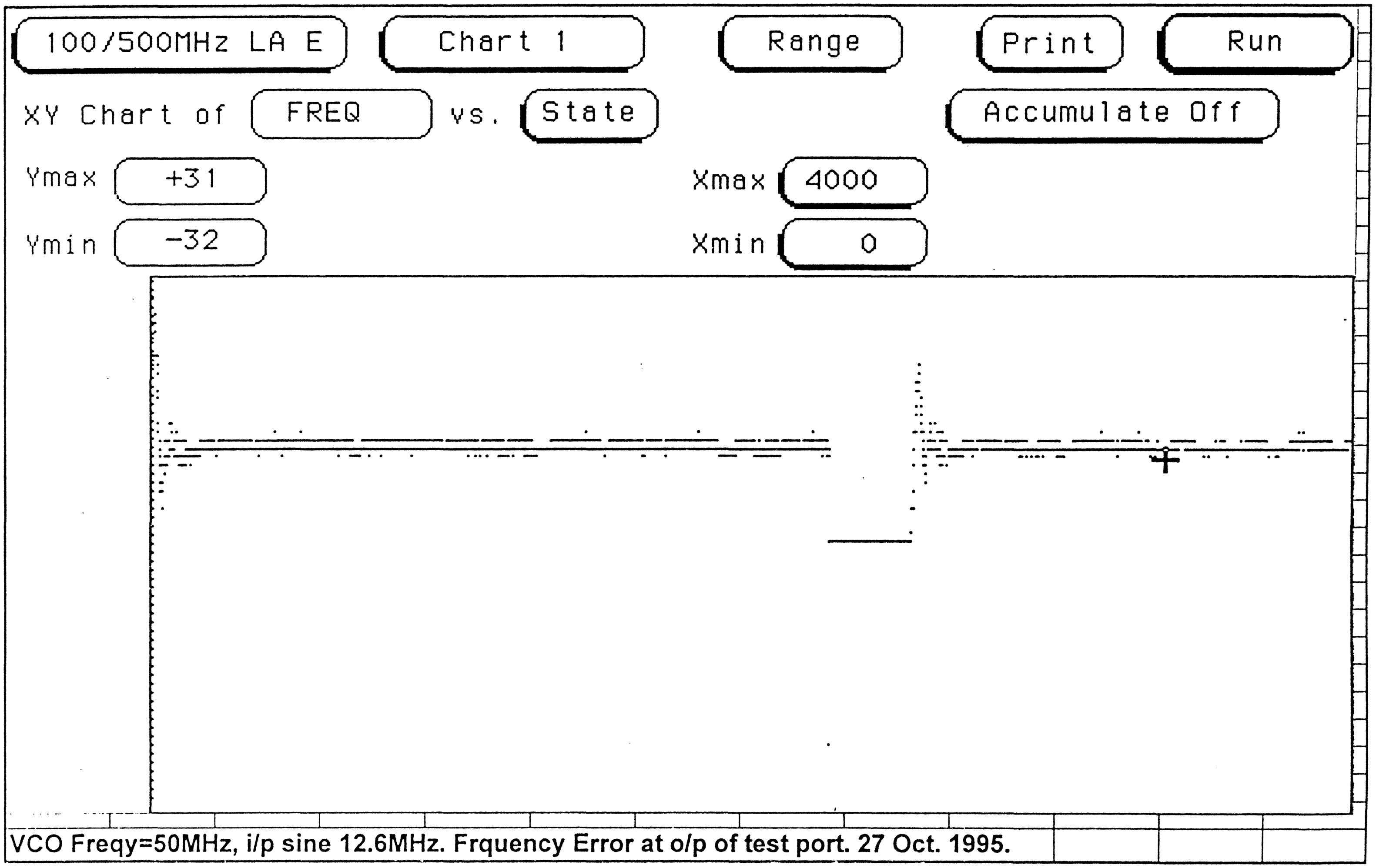
Ymin -32

Xmax 4000

Xmin 0

VCO Freqy=50MHz, i/p sine 12.6MHz. ADC(data) at o/p of test port. 27 Oct. 1995.

Frquency Error. 27 Oct. 1995



XY Chart of FREQ vs. State

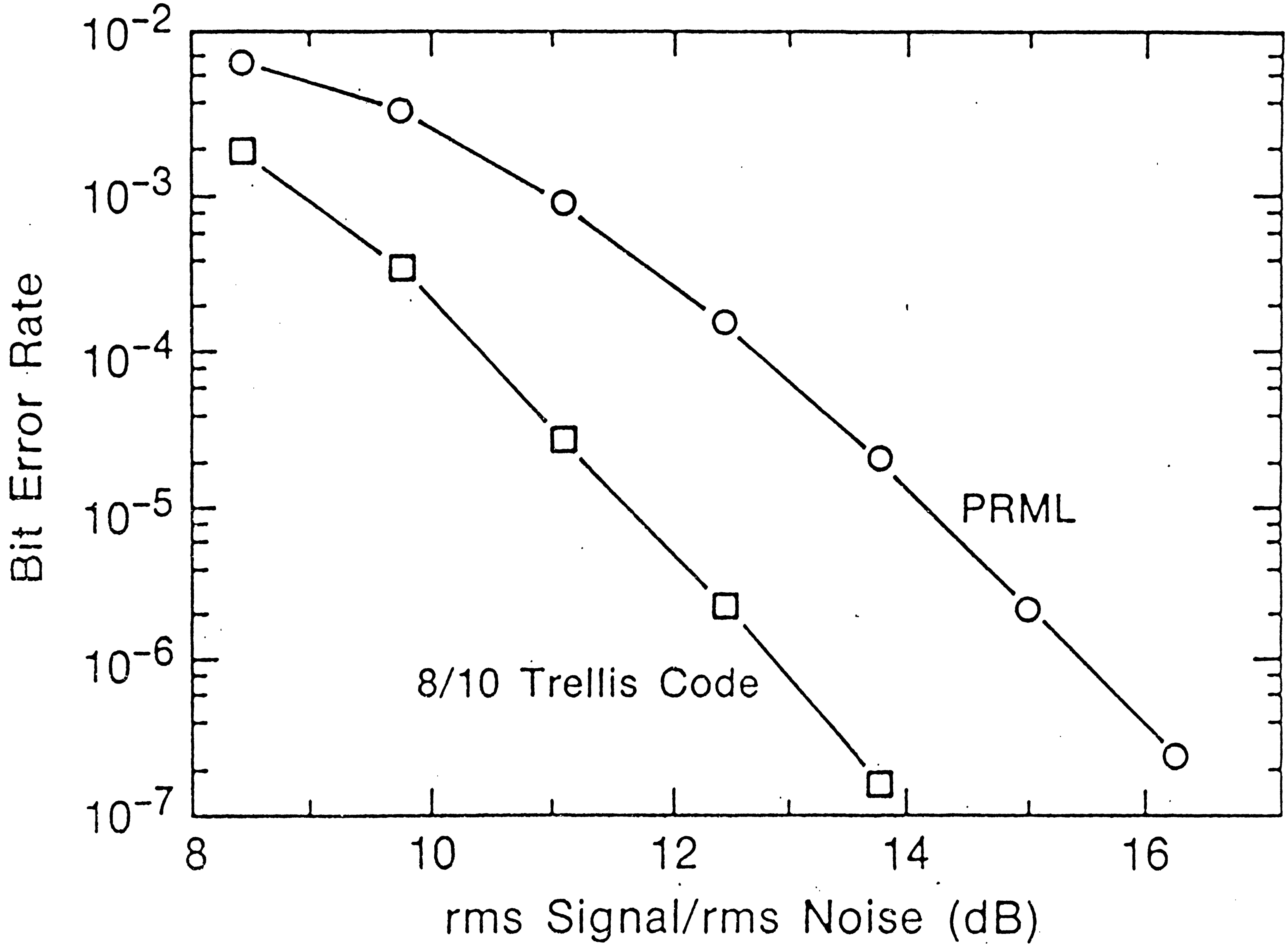
Ymax +31

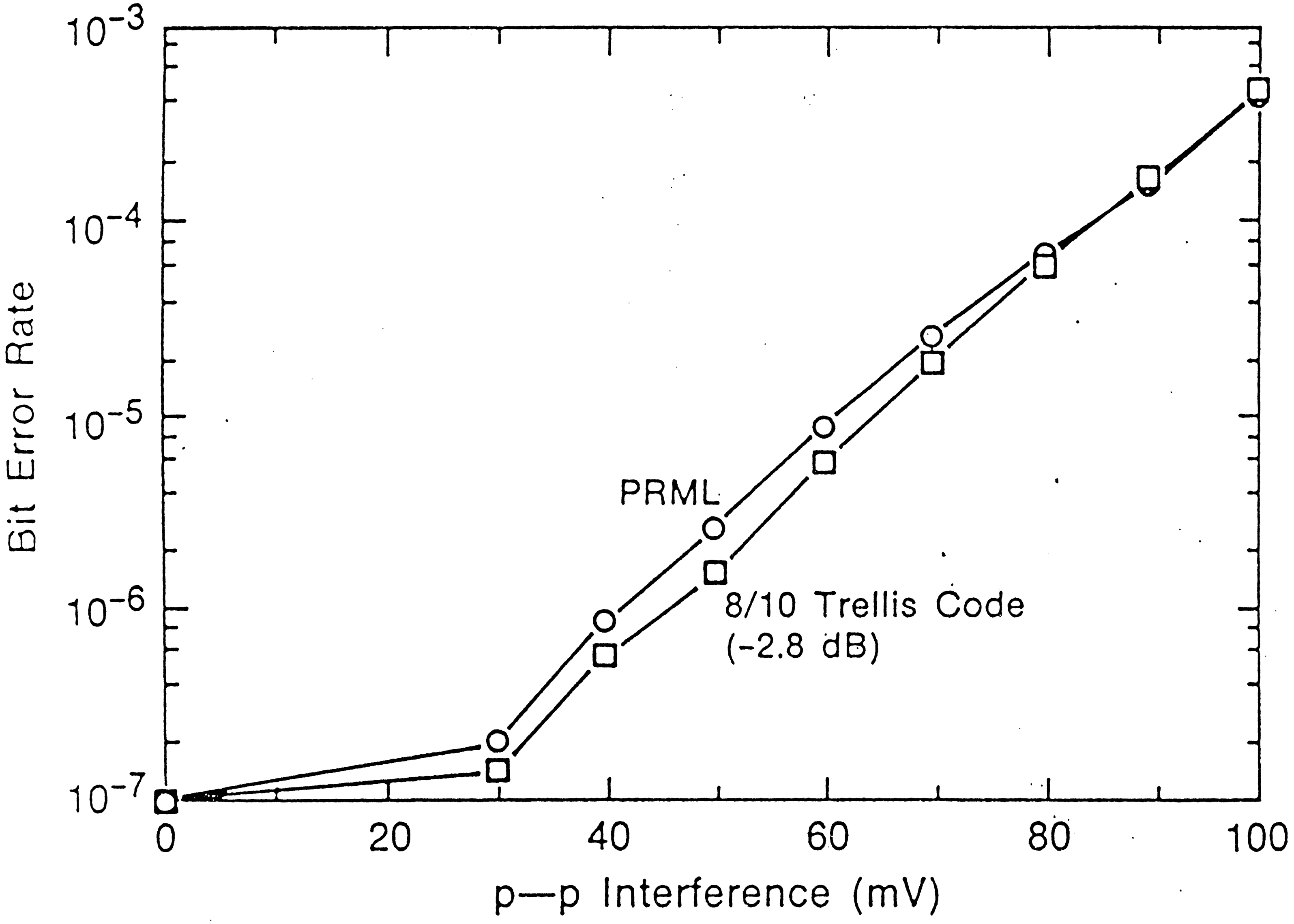
Ymin -32

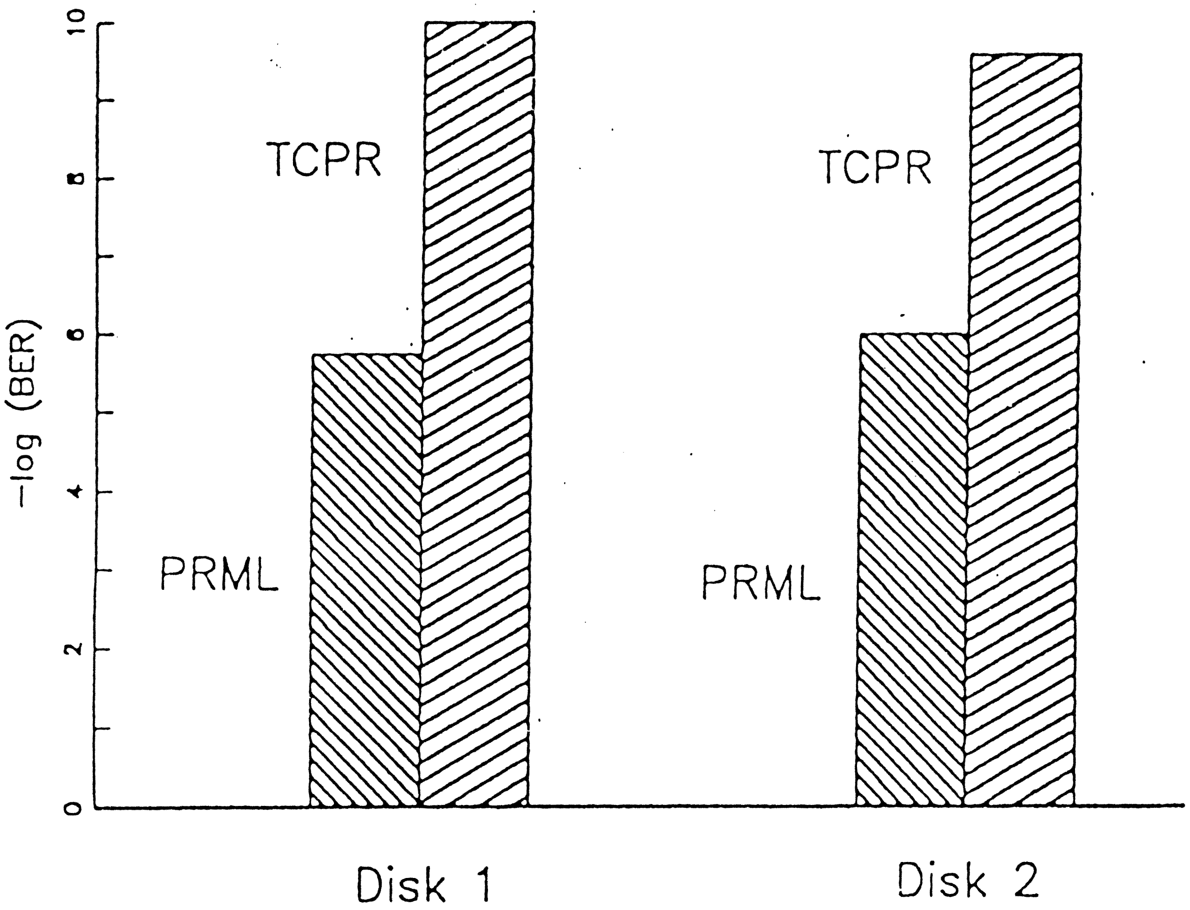
Xmax 4000

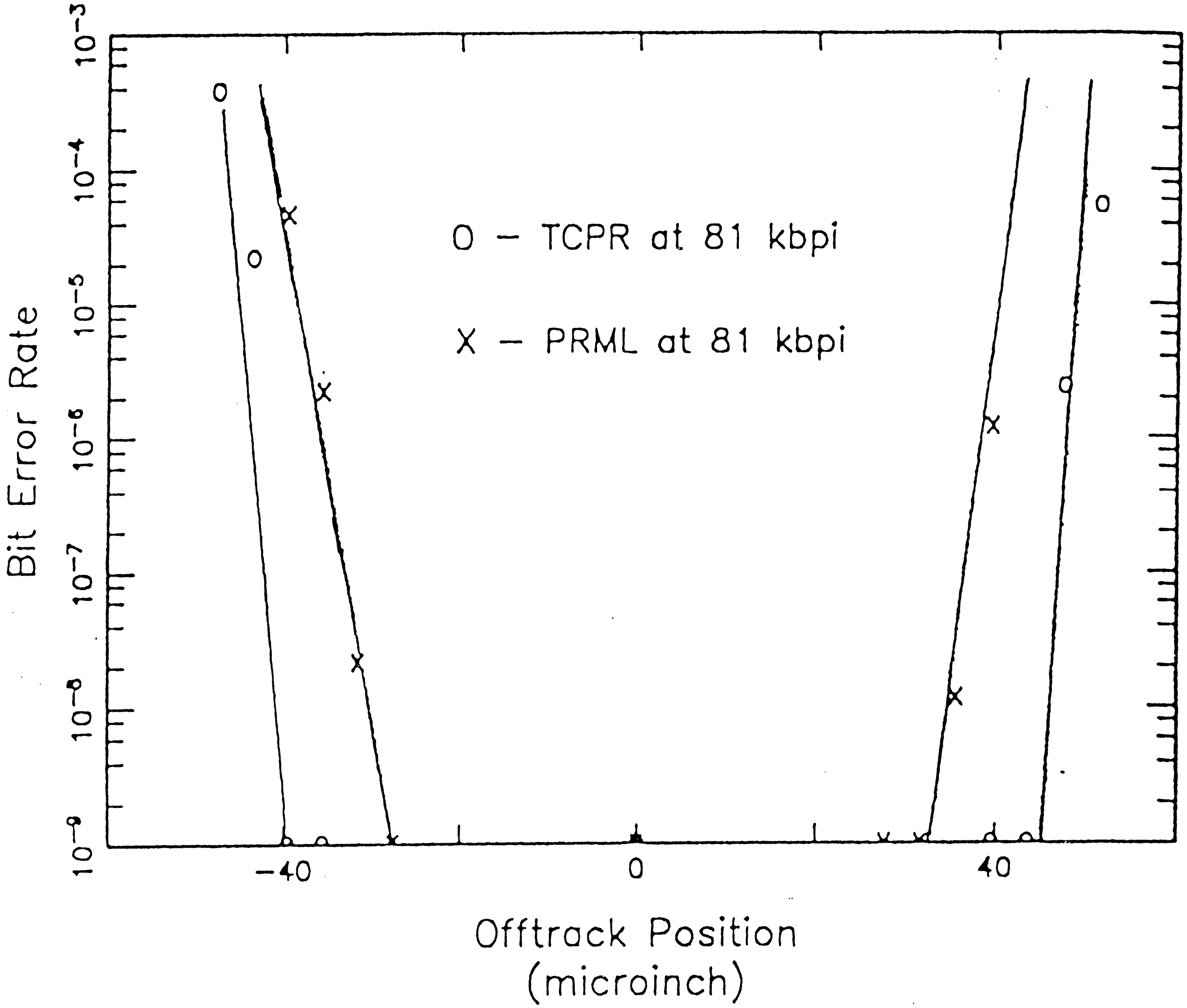
Xmin 0

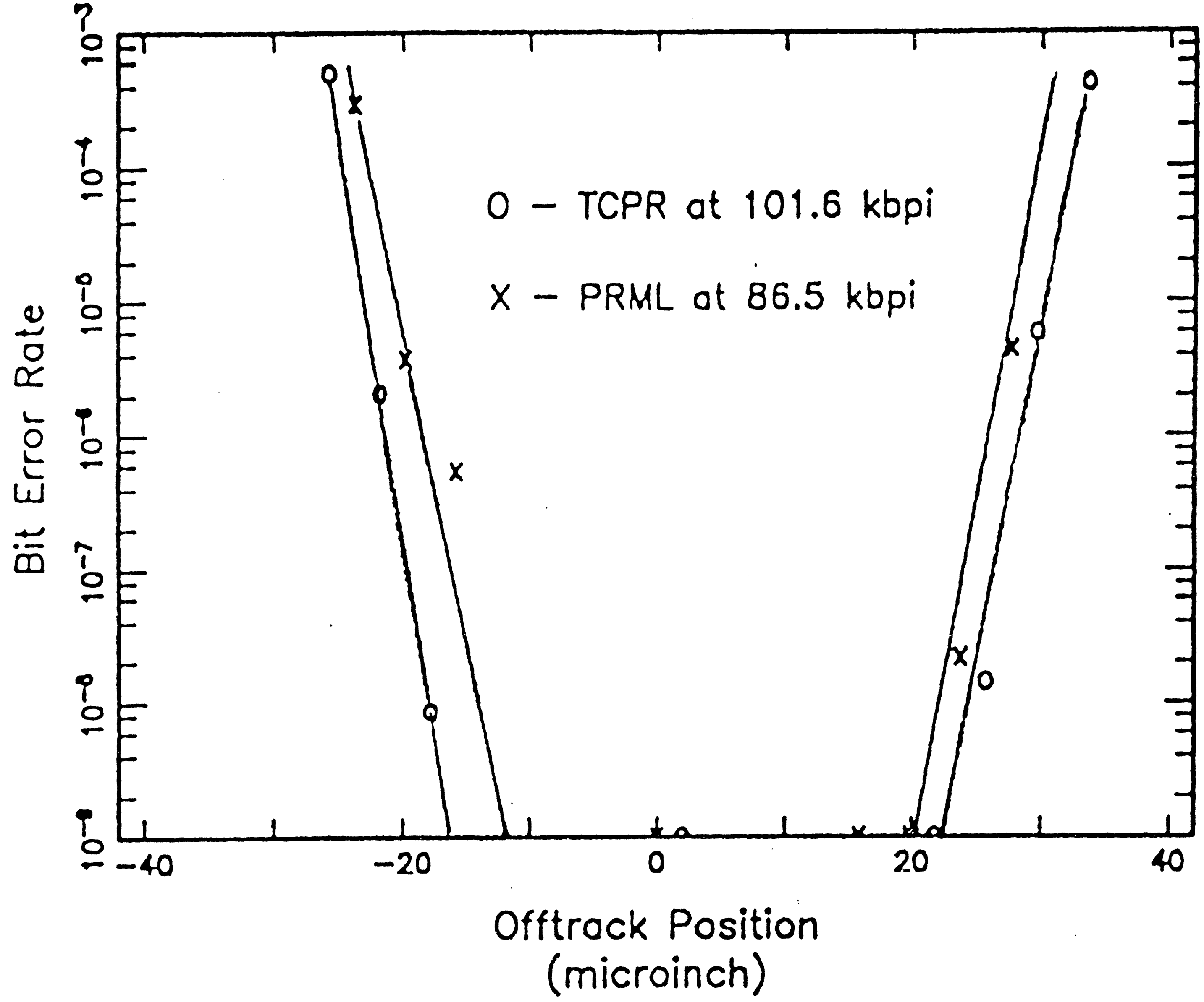
VCO Freqy=50MHz, i/p sine 12.6MHz. Frquency Error at o/p of test port. 27 Oct. 1995.

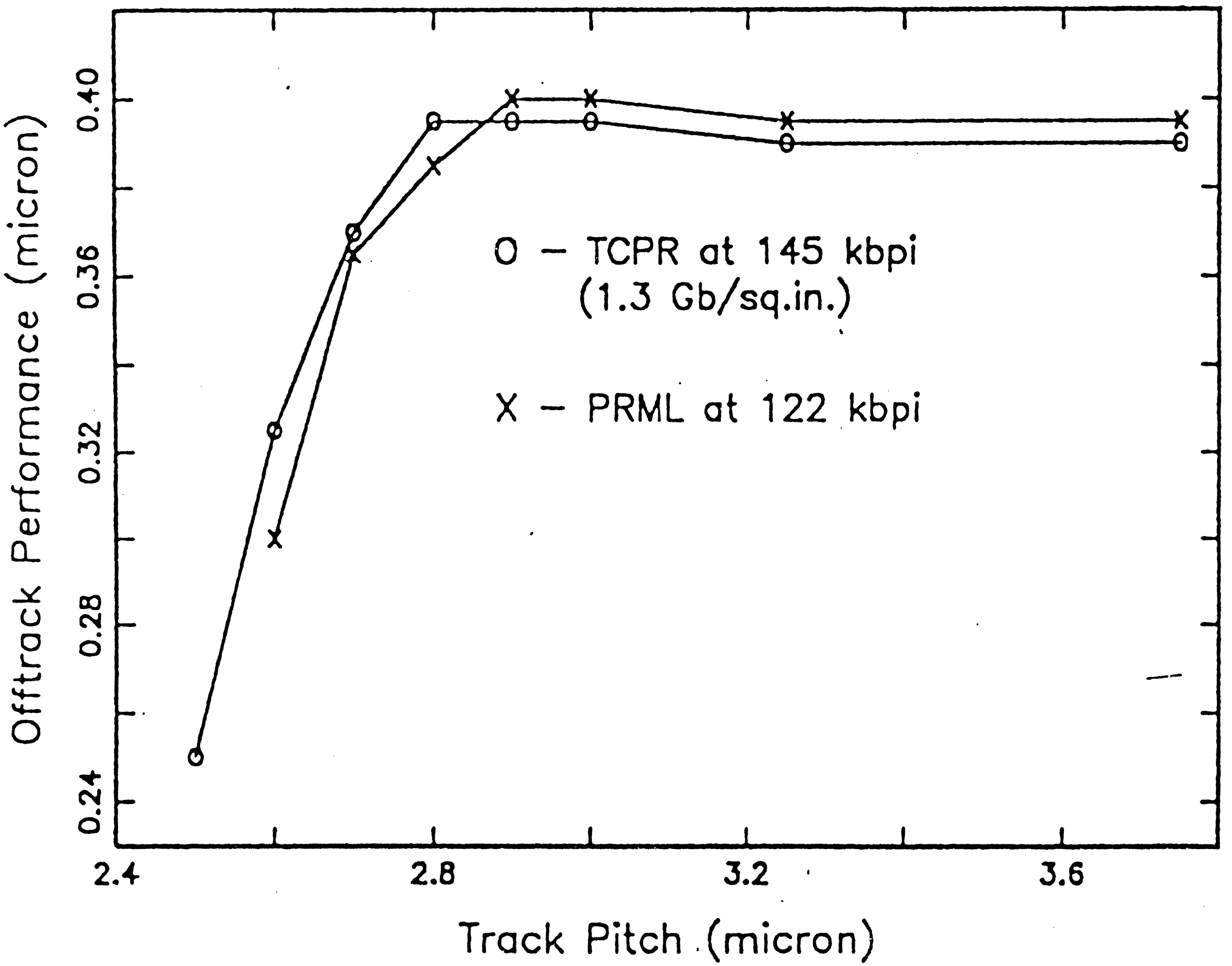

10^-2
10^-3
10^-4
10^-5
10^-6
10^-7
Bit Error Rate
8
10
12
14
16
rms Signal/rms Noise (dB)
PRML
8/10 Trellis Code


10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
Bit Error Rate
PRML
8/10 Trellis Code
(-2.8 dB)
0
20
40
60
80
100
p—p Interference (mV)


10
8
6
4
2
0
−log (BER)
TCPR
PRML
TCPR
PRML
Disk 1
Disk 2


O – TCPR at 81 kbpi
X – PRML at 81 kbpi
Bit Error Rate
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
−40
0
40
Offtrack Position
(microinch)


10^-3
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
Bit Error Rate
O – TCPR at 101.6 kbpi
X – PRML at 86.5 kbpi
-40
-20
0
20
40
Offtrack Position
(microinch)



Offtrack Performance (micron)
0.24
0.28
0.32
0.36
0.40
2.4
2.8
3.2
3.6
Track Pitch (micron)
O – TCPR at 145 kbpi
(1.3 Gb/sq.in.)
X – PRML at 122 kbpi

REFERENCES

[1]. R. E. Ziemer and W. H. Tranter, *Principles of Communications*, Boston: Houghton Mifflin, 1985

[2]. R. Karabed and N. Nazari, "*Analysis of Error Sequences for PRML and EPRML Signaling Performed over Lorentzian Channel*", Submitted to IEEE 1996 Global Telecommunication Conference.

[3]. N. Nazari and C. Varanasi, "*Performance of Recording Channels Employing Partial Response Signaling*", Proceedings of IEEE 1994 Global Telecommunications Conference, pp. 1129-1133.