

**Model 9157 CARD PUNCH  
COUPLER SYSTEM  
TECHNICAL MANUAL**

SDS 900055A

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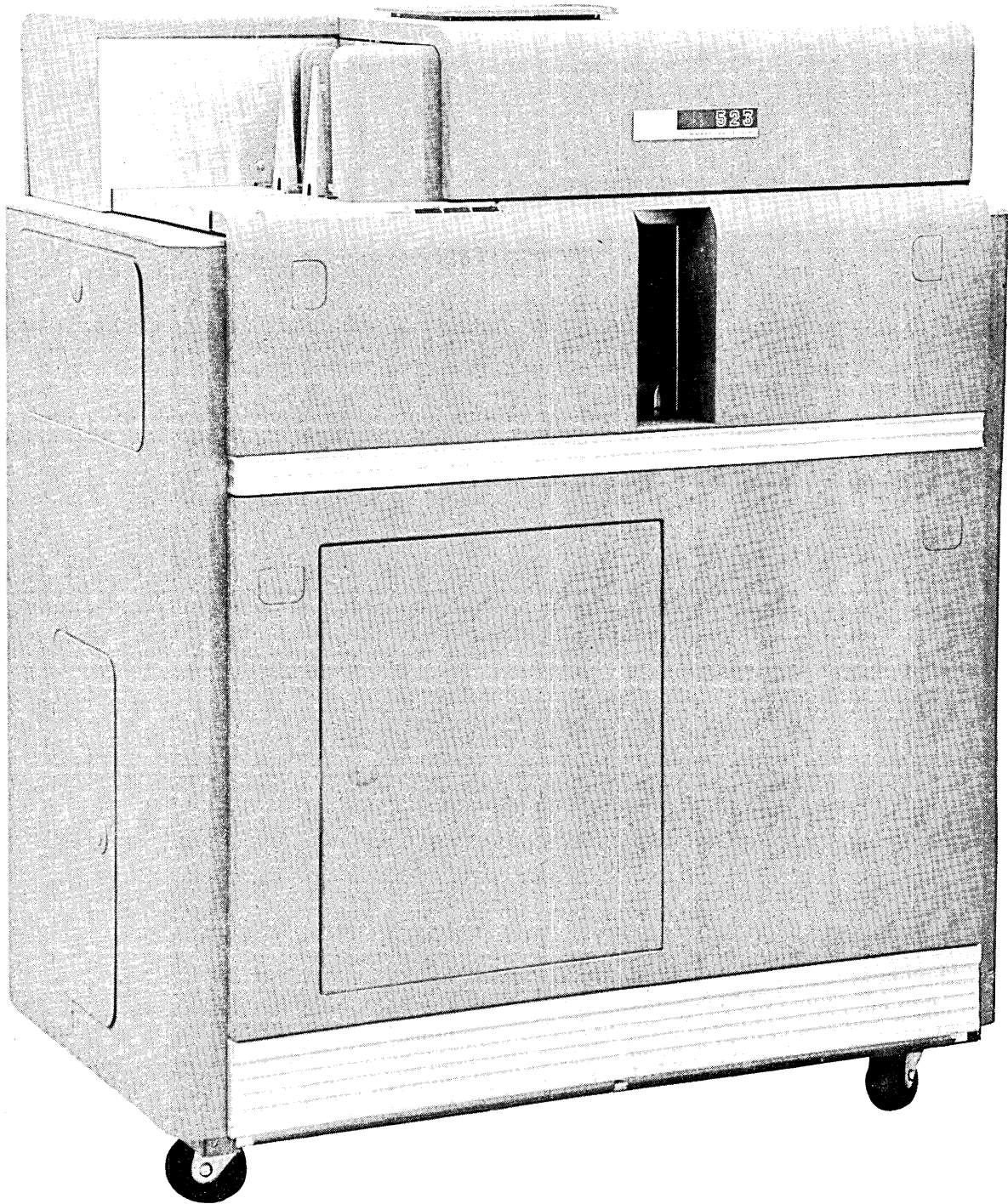
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Card Punch

## PART I. GENERAL DESCRIPTION

### INTRODUCTION

This publication comprises operating and maintenance instructions for the Model 9157/91570 Card Punch Coupler System manufactured by Scientific Data Systems, Incorporated, 1649 Seventeenth Street, Santa Monica, California. Model 9157/91570 is a computer output system which couples a modified IBM 523 Card Punch to SDS Computers. System description and operation are contained in Parts I, II, and III. Modification and adjustment requirements for the IBM 523 Card Punch and maintenance of the system are included in Part IV. Logic diagrams and schematics are contained in Part V to aid with maintenance and testing procedures.

### DESCRIPTION

The system is capable of punching standard 80-column cards at a rate of 100 cards per minute. Hollerith (BCD) and binary punching modes are available and are selected by program control. Card feeding operations are asynchronous, requiring each card cycle to be initiated by the computer program.

The coupler circuits are contained in three rack-mounted, 20-module, swing-out chassis. A 6-foot cable and cable plug module provide connection to the computer AUXILIARY connector. Three cable plug modules with three 25-foot cables connect the coupler to the IBM 523 Card Punch.

Receptacle 45J of the coupler is wired to accommodate a computer AUXILIARY connector for another output coupler device.

### POWER REQUIREMENTS

Power loading on the computer power supplies for operating the card punch coupler system is as follows:

+ 8 volts	1.4 amperes
+25 volts	3.2 amperes
-25 volts	0.6 amperes

The IBM 523 requires 11 amperes from a 110-120 volt, 50 or 60 cycle ac source.

PART II. OPERATING AND PROGRAMMING INSTRUCTIONS

SECTION 2-1. OPERATING INSTRUCTIONS

LOAD AND RUN-IN PROCEDURE

To operate the system, the operator must turn the power on at the power switch on the right-hand side of the IBM 523 Card Punch unit, load the hopper (800 cards maximum), and press the START pushbutton on the control panel. This procedure will initialize the coupler and establish the ready condition for feeding and punching the cards. Card punching can then proceed at a rate of 100 cards per minute under computer program control.

Pressing the STOP pushbutton on the control panel will render the unit not ready and inhibit feeding and punching. Pressing the START pushbutton again will initiate another card cycle, and the unit will be ready once more.

Octal character code designations used for the 9157/91570 Card Punch Coupler are listed in Table 2-1.

STACKER USAGE

Approximately 1,000 cards can be received by the stacker. The first card entering the stacker will not have been processed by the computer and the coupler; also, the last card will not automatically feed through to the stacker. Pressing the START pushbutton again will feed the last card into the stacker.

SECTION 2-2. PROGRAMMING INSTRUCTIONS

ADDRESSING

The computer addresses the punch coupler using operation code  $46_8$  for the first card punch unit and  $47_8$  for unit number two.

Table 2-1. Card Punch Codes

Typewriter Character	Card Holes	Octal Code
∅	0	00
1	1	01
2	2	02
3	3	03
4	4	04
5	5	05
6	6	06
7	7	07
8	8	10
9	9	11
SPACE	8-2	12
#	8-3	13
@	8-4	14
:	8-5	15
>	8-6	16
✓	8-7	17
&	12	20
A	12-1	21
B	12-2	22
C	12-3	23
D	12-4	24
E	12-5	25
F	12-6	26
G	12-7	27
H	12-8	30
I	12-9	31
BACK SPACE	12-0	32
.	12-8-3	33
□	12-8-4	34
[	12-8-5	35
<	12-8-6	36
‡	12-8-7	37

Typewriter Character	Code Holes	Octal Code
-	11	40
J	11-1	41
K	11-2	42
L	11-3	43
M	11-4	44
N	11-5	45
O	11-6	46
P	11-7	47
Q	11-8	50
R	11-9	51
CAR. RET.	11-0	52
S	11-8-3	53
*	11-8-4	54
]	11-8-5	55
;	11-8-6	56
Δ	11-8-7	57
⋈	None	60
/	0-1	61
S	0-2	62
T	0-3	63
U	0-4	64
V	0-5	65
W	0-6	66
X	0-7	67
Y	0-8	70
Z	0-9	71
TAB	0-8-2	72
,	0-8-3	73
%	0-8-4	74
~	0-8-5	75
\	0-8-6	76
##	0-8-7	77

## CORNER-TURNING METHOD

The IBM 523 is a parallel-punching device; that is, it punches one 80-digit row at a time. Punching one card requires that the computer transmit the entire card image twelve times. The coupler then inspects the image each row time and loads an 80-bit buffer register with the appropriate row image.

The row buffer is loaded each row time by connecting the computer buffer to the punch coupler, using an EOM instruction and addressing the punch. Two punching modes are available: Hollerith (BCD), and binary. These modes are controlled by the EOM instruction.

When punching BCD, 80 characters must be transmitted each row time where the first character is punched in card column one. Binary punching requires that 160 characters be transmitted to the punch coupler each row time. The first of the 160 characters is punched in rows 12 through 3 of column one -- the most significant bit of this character appears in row 12. The second character is punched in rows 4 through 9 of column one, with the most significant bit in row 4. Subsequent columns are punched in the same manner with the result that all odd-numbered characters are punched in rows 12 through 3 and all even-numbered characters in rows 4 through 9.

## PROGRAM TESTS

Two punch conditions are available for testing by the computer program using the SKS I/O instruction.

The punch "ready" test is made using the following instruction format:

```
SKS 14046
```

A program skip results if the punch is ready to feed a card. For the punch to be ready to feed, the following conditions must exist:

- a) the hopper is not empty
- b) the stacker is not full
- c) a run-in process has occurred
- d) the chip box is not full
- e) a card jam does not exist
- f) a card cycle is not in process

The punch row buffer is always ready for loading when the punch is ready to feed.

The other program test provides a means of determining the status of the punch row buffer. This instruction format is:

```
SKS 12046
```

and a program skip results if the row buffer is ready for loading.

## CARD FEEDING AND BUFFER LOADING

The punch coupler is set up to communicate with the computer buffer when the following EOM instruction is executed:

```
EOM 0n646
```

where n may be either 2 or 3. When n = 2, the punching mode is BCD, while binary punching occurs when n = 3.

Following the execution of this EOM instruction, the punch coupler proceeds to clock characters from the computer buffer and to load the row buffer until output has been terminated by:

```
EOM 14000
```

and all characters have been transmitted.

A card cycle is initiated when the set-up EOM is executed and the punch is ready.

## TIMING

The IBM 523 Punch operates on a cycle basis. The punch clutch is operated and then the unit will execute one punch cycle. Immediately following the end of that cycle, there is a period during which the clutch may be operated again and provide another punch cycle (Figure 2-1). The continuation of this type of operation results in a punch rate of 100 cards per minute.

If, however, a following punch cycle is not programmed prior to the end of the punch cycle, that following cycle will be lost to the program. The next opportunity to execute a punch cycle, then, would be at the end of this following cycle. If a punch cycle is not called for during the following cycle, the unit will "coast" to a stop at a point where it can accept a signal to punch and will immediately enter a punch cycle when the instruction is received. While the unit is cycling following a punch cycle, it may be instructed to initiate a punch cycle. This information will be held, if necessary, until the appropriate time in the cycle to operate the punch clutch and initiate a punch cycle.

The punch cycle is divided into 14 equal periods of 42.8 milliseconds each. Twelve of these periods are used for row punching, the other two are for card feeding. Of the 42.8 millisecond punch period, approximately 20 milliseconds are required for the actual punching. The remainder of the period, or approximately 23 milliseconds, is available to load the row buffer for the next row.

At the end of a card punch cycle, after row 9 has been punched, there is a 10-millisecond period during which the unit may be instructed to initiate a following punch cycle. This period begins at the time the punch becomes ready.

The punch coupler may be addressed before the row buffer is ready to be loaded, in which case, the coupler will delay clocking characters from the computer until the current information in the buffer has been punched. This procedure may

only be followed for character transmissions other than for the first one which is responsible for initiating the card feed. The punch ready test must always be made prior to executing a feed cycle. The timing diagram in Figure 2-1 illustrates these modes of operation.

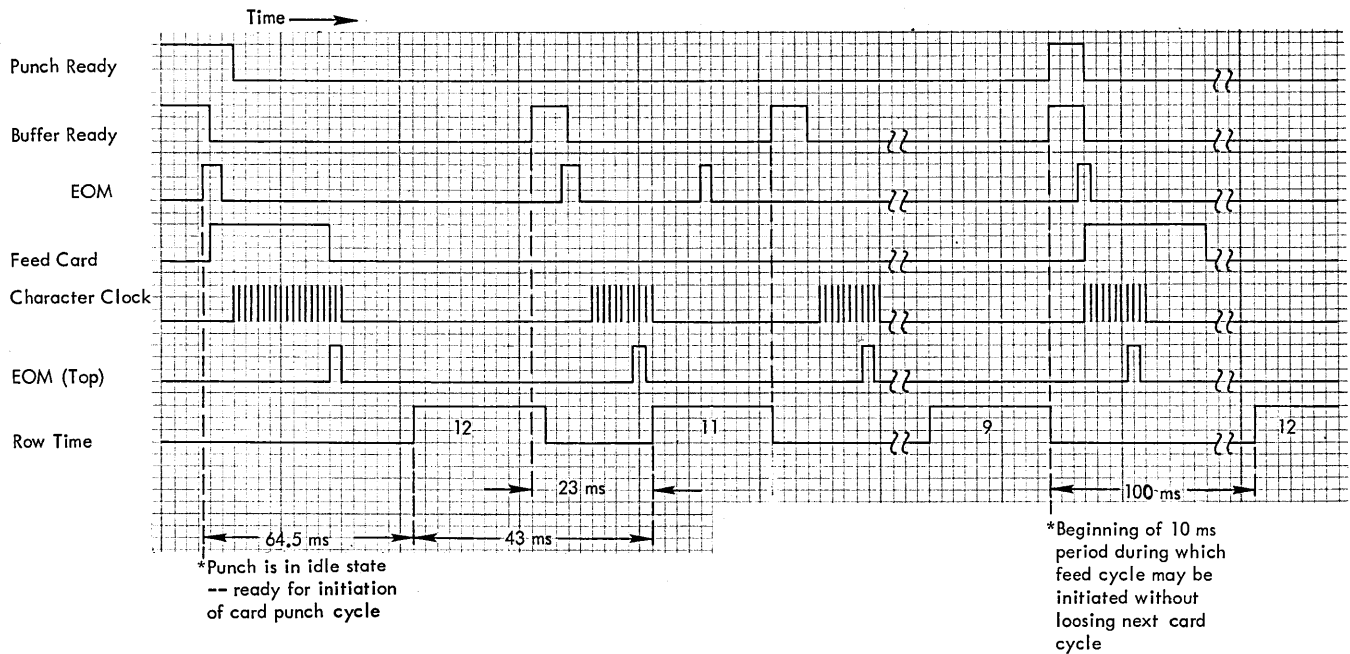


Figure 2-1. Punch Timing Diagram

#### TERMINATING AND ERROR CONDITIONS

The SDS 930 and 9300 Computers provide a mode of operation whereby the computer buffer may continue to address the punch coupler after the row buffer has been loaded (although output has been terminated). This type of operation allows the punch coupler to inform the coupler when it is next ready to accept data for loading of its row buffer. This is accomplished by the punch coupler transmitting an end-of-record (halt) signal when its row buffer is ready and the IORP Extended Mode Channel is employed.

The computer I/O error indicator will be set when the IORP command is used if, after the last card row has been punched, the punch signals that this card has not fed properly. This signal occurs at the same time that end-of-record is given.

#### EXAMPLE OF CARD PUNCH PROGRAM

A typical sample program for punch operation is listed in Table 2-2.



Table 2-2. Sample Program

Program Objective: Punch one card

Location	Instruction	Remarks
200*	LDA 00226	
201	STA 00227	Set row count
202	LDX 00225	
203	SKS 14046	Test bit 12 -- punch ready
204	BRU 00203	
205	EOM 02646	Select Punch
206	2 MIW 00254	
207	SKS 20010	
210*	HLT	Stop on error
211	BRX 00206	
212	EOM 14000	Terminate row output
213	SKS 21000	
214	BRU 00213	
215	SKS 12046	Test bit 13 -- punch buffer ready
216	BRU 00215	
217	MIN 00227	
220*	SKN 00227	Test for 12 rows done
221	BRU 00223	
222	BRU 00202	Continue
223	HLT	Halt when card done
224	BRU 00200	
225	777 77754	Decimal -20
226	777 77764	Decimal -12
227	000 00000	Row count
230*		Start of card image

## PART III. IMPLEMENTATION

### SECTION 3-1. LOGIC DESCRIPTION

Description of the logic circuits in the card punch coupler are presented in sequence by functional circuit groups. Sequence of a typical card punch cycle is illustrated in Figure 3-1, Timing Diagram. Refer to Part V of this manual for a complete list of logic equations and logic diagrams of the circuits described.

#### COUPLER INITIALIZING

Initialization of the coupler during power turn-on is accomplished by a dc reset, Dcr, signal which is obtained using a delay circuit and is present for a few milliseconds after power turn-on. Dcr resets all of the control and counter flip-flops.

- rPb = --- + Dcr
- rSc = --- + Dcr
- rBc = --- + Dcr
- rCt = --- + Dcr
- rRc6 = --- + Dcr
- rRc5 = --- + Dcr
- rRc4 = --- + Dcr
- rRc3 = --- + Dcr

#### PUNCH ADDRESS LOGIC

The punch address is  $46_8$  for the first unit and  $47_8$  for the second unit. This address is decoded from both the computer C Register and the buffer. When decoded from the C Register, the Punch address, Pa, becomes:

$$Pa = \overline{C17} C18 \overline{C19} \overline{C20} C21 C22 \overline{C23}$$

for the first unit connected to the computer W Buffer.

When the punch is addressed from the W Buffer, it is for the purpose of loading the punch buffer; therefore,

$$Lb = W9 \overline{W10} \overline{W11} W12 W13 \overline{W14}$$

#### MODE CONTROL

The punching mode, either BCD or binary, is described by the EOM which connects the computer buffer to the punch coupler. If C14 is true during this EOM, the punching mode is binary; if reset, the mode is BCD. This information is retained in the punch coupler by the Punch binary flip-flop which is controlled as follows:

$$sPb = Pa Buc C14 Q2$$

$$rPb = Pa Buc \overline{C14} \overline{Q2} + \dots$$

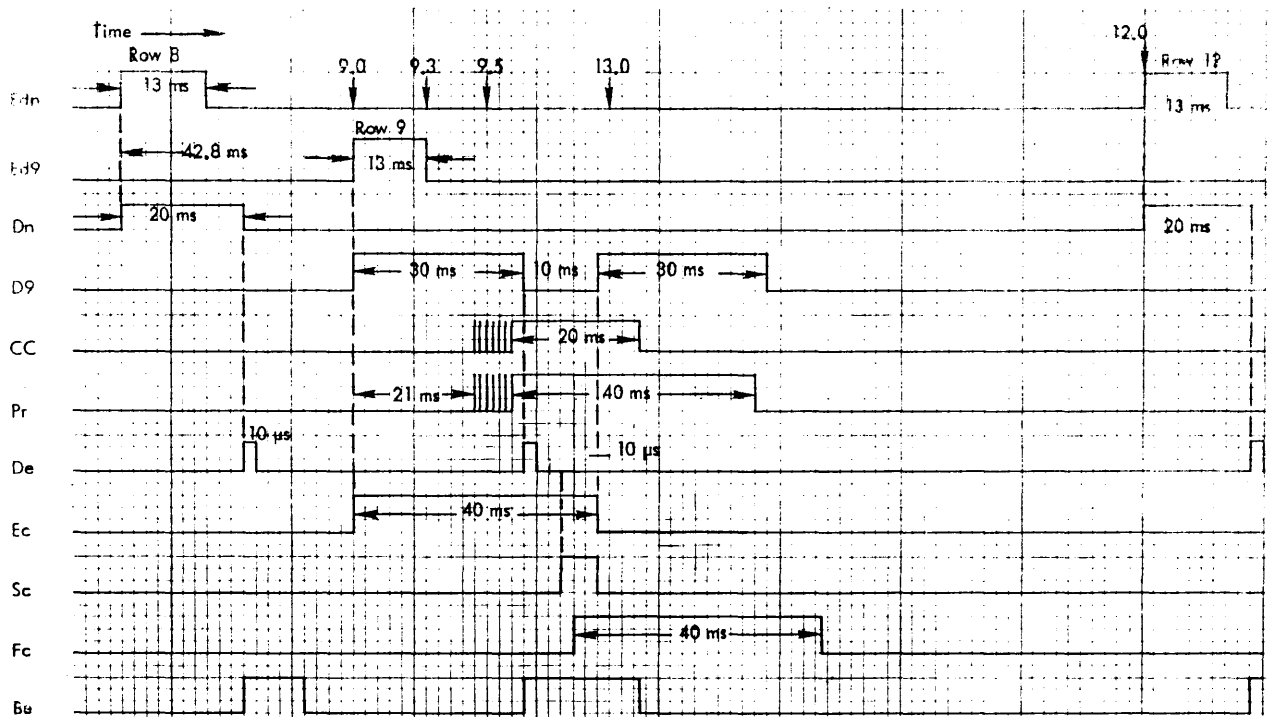


Figure 3-1. Punch Coupler Timing Diagram

## PUNCH TESTS

Two punch conditions are available for testing from the computer. First, the status of the punch row buffer may be determined by using the SKS instruction and bit C13. A program jump will result if the Buffer is empty, Be.

$$\overline{Sio} = \overline{Pa Be C13} + \dots$$

The other test is used to determine if the punch is ready to begin another punch cycle. Bit C12 calls for this test and a program jump results if the punch is ready.

$$\overline{Sio} = \overline{Pa Be \overline{Lb} Sc C12} + \dots$$

The term Sc, Successful cycle, appears here to describe the status of the punch.

The Sc flip-flop is set at the conclusion of each punch cycle if all of the following punch conditions exist:

- a) mechanical interlocks are made
- b) the START key has been operated
- c) the card hopper is not empty
- d) the last card fed properly in the punch station
- e) the last card fed properly into the stacker

Conditions a) through d) are supplied by one signal from the punch, Pr, Punch ready. The last condition is supplied by the punch signal, Cc, Card cycled. Set Sc thus becomes,

$$sSc = Cc Pr \underline{De}$$

where De is a sampling pulse provided by the coupler.

## PUNCH TIMING

The IBM 523 provides twelve timing pulses, one per card row. These pulses are on the order of 13 milliseconds duration and define the time used for punching each row (Figure 3-1). Eleven of these signals are wired in common to provide the coupler with a single pulse, Edn, for card rows 12 through 8. The row 9 pulse, Ed9, is brought out separately and is used in the end-of-cycle timing. (Row 9 is the last row punched.)

Both Edn and Ed9 signals trigger one-shot circuits as follows:

$$\begin{aligned} sDn &= Edn \quad (dc) \\ rDn &= 20 \text{ ms} \end{aligned}$$

and,

$$\begin{aligned} sD9 &= Ed9 \quad (dc) + \dots \\ rD9 &= 30 \text{ ms} \end{aligned}$$

The D9 one-shot is set for 30 ms so that it falls during the time that Pr and Cc are to be sampled (Figure 3-1). The fall of both Dn and D9 trigger a one-shot, De,

$$\begin{aligned} sDe &= Dn + D9 Ec \\ rDe &= 10 \mu s \end{aligned}$$

The D9 one-shot is triggered a second time, at the end of each cycle, for the purpose of establishing a period during which the punch clutch may not be operated. Attempted operation of the clutch during this period results in misfeeds.

The End-of-cycle one-shot supplies the triggering signal for the second operation of D9. Ec is triggered during row 9 time by

$$\begin{aligned} sEc &= Ed9 D9 \quad (dc) \\ rEc &= 40 \text{ ms} \end{aligned}$$

which then triggers D9 again by

$$\begin{aligned} sD9 &= Ec \quad (ac) \\ rD9 &= 30 \text{ ms} \end{aligned}$$

## CARD FEEDING

A Feed card signal is supplied to the punch, once per card cycle. Fc is provided as a result of the punch being addressed for the purpose of loading the row buffer for the first time, which is for row 12.

$$\begin{aligned} sFc &= Buc Pa Sc \overline{D9} Q2 \quad (dc) + \dots \\ rFc &= 40 \text{ ms} \end{aligned}$$

The  $\overline{D9}$  is included here to inhibit feeding during the unreliable period as described previously. The punch may, however, be addressed during this period and the Fc signal will be provided by

$$sFc = \dots + Sc \overline{Be} \overline{D9} Q2 \quad (ac)$$

The term  $\overline{Be}$  here indicates that the row buffer has been loaded with the row 12 punch image. The Be flip-flop is controlled as follows:

$$\begin{aligned} sBe &= De \\ rBe &= \overline{Lb} \overline{W0} \overline{W5} \overline{W6} \end{aligned}$$

Therefore, the Be flip-flop is set after each row has been punched and is then reset once the buffer is again loaded. The term  $\overline{W0} \overline{W5} \overline{W6}$  indicates that the computer buffer output has been terminated and that all characters have been received by the punch coupler.

Since Fc resets the Sc flip-flop,

$$rSc = Fc Q2 + \dots$$

the fact that Sc is set and Be is reset means then that the row buffer has been loaded and the punch has not been instructed to feed a card.

## BUFFER LOADING

When the row buffer is ready to be loaded (Be is set), and the punch is addressed by the computer buffer, then the characters are clocked from the computer, inspected, and the punch image is shifted into the row buffer.

A row counter is employed in the punch coupler which defines the card row that is to be punched next. The state of this counter and the characters presented to the coupler by the computer buffer determine whether a one or a zero is shifted into the row buffer. The row buffer shifts from bit 80 towards bit 1 and, thereby, the image for the previous row is replaced by the image for the next row to be punched.

The row counter consists of four flip-flops, Rc3 through Rc6, and provides the following states:

Row	Rc3	Rc4	Rc5	Rc6	Decoded Term
12	0	1	0	0	Rt4
11	0	1	0	1	Rt5
0	0	1	1	0	Rt6
1	0	1	1	1	Rt7
2	1	0	1	0	Rt2
3	1	0	1	1	Rt3
4	1	1	0	0	Rt4
5	1	1	0	1	Rt5
6	1	1	1	0	Rt6
7	1	1	1	1	Rt7
8	0	0	1	0	Rt2
9	0	0	1	1	Rt3

The counting is controlled by the following logic:

$$\begin{aligned} sRc6 &= \overline{Rc6} \underline{Dn} \\ rRc6 &= Rc6 \underline{Dn} + D9 \underline{Ec} + Dcr \\ sRc5 &= \overline{Rc5} \underline{Rc6} \\ rRc5 &= Rc5 \overline{Rc4} \underline{Rc6} + D9 \underline{Ec} + Dcr \\ sRc4 &= \overline{Rc4} \underline{Rc5} \underline{Rc6} + D9 \underline{Ec} \\ rRc4 &= Rc4 \underline{Rc5} \underline{Rc6} + Dcr \\ sRc3 &= \overline{Rc3} \underline{Rc4} \\ rRc3 &= Rc3 \underline{Rc4} + D9 \underline{Ec} + Dcr \end{aligned}$$

The dc term D9 Ec controls each flip-flop so that during run-in and at the end of each card cycle, the counter is forced to the row 12 configuration.

The counter state and the computer buffer character then determine the sB80 term. For the BCD punching mode, inspection of the character set and counter state leads to the following function:

$$\begin{aligned} sB80 &= [\overline{R1} \underline{R2} \underline{Rt4} \overline{Rc3}] && \text{(Row 12)} \\ &+ R1 \overline{R2} \underline{Rt5} \overline{Rc3} && \text{(Row 11)} \\ &+ (R1 \underline{R2} \overline{R3} \overline{R4} \overline{R5} \overline{R6} + \overline{R1} \underline{R2} \overline{R3} \overline{R4} \overline{R5} \overline{R6} + S_n) \underline{Rt6} \underline{Rc3} && \text{(Row 0)} \\ &+ \overline{R3} \underline{R4} \underline{R5} \underline{R6} \underline{Rt7} \underline{Rc3} && \text{(Row 1)} \\ &+ (R4 \underline{Rc4} + \overline{R4} \underline{Rc4})(R5 \underline{Rc5} + \overline{R5} \underline{Rc5})(R6 \underline{Rc6} + \overline{R6} \underline{Rc6}) \underline{Rc3} \underline{S_n} && \text{(Rows 2-7)} \\ &+ \underline{Rt2} \overline{Rc3} \underline{R3} (\overline{R4} \overline{R5} \underline{R6}) \underline{S_n} && \text{(Row 8)} \\ &+ \underline{Rt3} \overline{Rc3} \underline{R3} (\overline{R4} \overline{R5} \underline{R6}) \overline{Pb} \underline{Sh} && \text{(Row 9)} \\ &+ \dots \end{aligned}$$

where:

$$S_n = (R1 \overline{R2} + \overline{R1} R2) (R3 \overline{R4} R5 \overline{R6})$$

The Sh term is the shifting clock for the entire row buffer and is derived from the term which clocks the computer buffer.

The computer buffer clock is derived from a one-shot which is triggered by,

$$\begin{aligned} sSd &= Lb \underline{Be} \overline{W5} \overline{W6} \underline{Q2} && \text{(ac)} \\ rSd &= 6.8 \mu s \end{aligned}$$

The buffer clock becomes,

$$\overline{Ecw} = \underline{Sd}$$

and the shift clock is then,

$$Sh = Lb \underline{Be} \underline{Ct} \underline{Sd}$$

The Sh signal is gated here by Ct for the purpose of punching in the binary mode.

When the row buffer is being loaded in the binary mode, 160 characters will be transmitted by the computer buffer but only every other character will be inspected for shifting information into the row buffer.

The Ct flip-flop controls this operation by being "toggled" by each character clock.

$$\begin{aligned} sCt &= \overline{Pb} \overline{Ct} \underline{Sd} + D9 \underline{Ec} \\ rCt &= \overline{Pb} \underline{Ct} \underline{Sd} + \overline{Pb} \underline{Rt3} \underline{Dn} \end{aligned}$$

The D9 term is used here to initialize Ct properly during run-in and at the end of each cycle. The reset term Pb Rt3 Dn is required since, beginning with row 4 of the card, it is necessary to shift the row buffer for every other character beginning with the second one.

The setting of B80 in the binary mode is controlled as follows

$$\begin{aligned} sB80 &= [R1 \underline{Rt4} \\ &+ R2 \underline{Rt5} \\ &+ R3 \underline{Rt6} \\ &+ R4 \underline{Rt7} \\ &+ R5 \underline{Rt2} \\ &+ R6 \underline{Rt3}] \overline{Pb} \underline{Sh} \\ &+ \dots \end{aligned}$$

The Punch magnets are enabled by,

$$\begin{aligned} Pm1 &= Md \underline{B1} \\ &| && | \\ &| && | \\ Pm80 &= Md \underline{B80} \end{aligned}$$

where:

$$Md = \overline{Be} (\underline{Edn} + \underline{Ed9})$$

#### TERMINATING AND ERROR CONDITIONS

A mode of operation is available with the 930 and 9300 computer buffers which permits the buffer to continue addressing the punch after the condition of W0 W5 W6 arises. The purpose of this mode is to allow the punch (or any device) to disconnect from the buffer when it is next ready to receive data.

The punch disconnects by transmitting  $\overline{Whs}$  at  $De$  time if  $W0$  is reset,

$$\overline{Whs} = \overline{Lb De W0 W6}$$

An error response is provided after row 9 has been punched if this card does not feed properly.

$$\overline{Wes} = \overline{Lb Ec De Cc} + - - -$$

An additional error response is supplied if the row buffer has not been loaded by punch time.

$$\overline{Wes} = - - + \overline{Lb Be (Dn + Dg Ec)}$$

### SECTION 3-2. INTERFACE SIGNALS

All of the signals transferred between the IBM 523 and the coupler go through the "shoe" type connector provided in the IBM 523 unit.

#### SIGNALS FROM IBM 523 TO SDS 9157/91570 COUPLER

The following signals are outputs from the IBM 523 which are used by the SDS 9157/91570 Coupler:

- a)  $\overline{Pr}$  (Punch Ready)  
This signal is false when the 523 is ready to accept a start signal which will initiate a punch cycle.
- b)  $\overline{Cc}$  (Cycle Complete)  
This signal is false from 9.5 to 13.0 time (see Electrical Time Chart on IBM Wiring Diagram Type 523) of a punch cycle and indicates that the previous card punched was fed through the 523 read station successfully.

- c)  $\overline{Ed9}$  (Row 9 Time)  
This signal is false from 9.0 to 9.3 time and represents the time that row 9 is being punched.

- d)  $\overline{Edn}$  (Row time 12 through 8)  
The 523 generates a signal similar to  $\overline{Ed9}$  for each row time. These signals for rows 12 through 8 are bussed together in the coupler and provide one signal,  $\overline{Edn}$ .

- e) Power  
The power supply in the 523 is used to drive the punch magnets and other relays in the unit. This supply voltage is +45 volts, and is brought out of the coupler along with the common side of the supply.

The chassis ground of the 523 is brought out and is connected to the computer ground.

#### SIGNALS FROM SDS 9157/91570 COUPLER TO IBM 523

The SDS 9157/91570 Coupler sends the following signals to the IBM 523 unit:

- a)  $Pc$  (Punch Clutch)  
This signal operates a relay in the 523 which, in turn, has contacts that complete the circuit to the clutch.
- b)  $Pmn$  (Punch Magnets, 80 lines)  
The 80-punch magnets are driven from the coupler.

PART IV. INSTALLATION AND MAINTENANCE

SECTION 4-1. INSTALLATION OF CARD PUNCH UNIT

POWER SUPPLY POLARITY CHANGE

The IBM 523 Summary Punch must be modified as follows before being connected to the Model 9157/91570 Card Punch Coupler.

The power supply polarity in the IBM 523 must be reversed to enable SDS standard relay drivers to operate the punch magnets and control relays of the IBM 523. Figures 4-1 and 4-2 show the power circuit before and after modification.

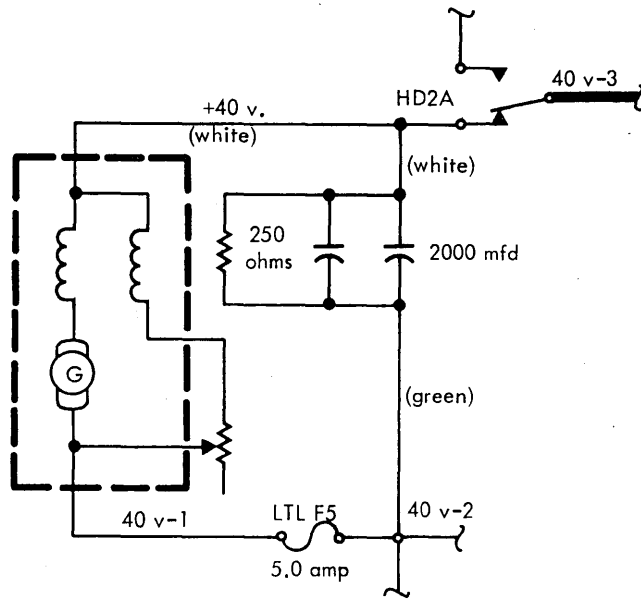


Figure 4-1. IBM 523 Power Supply Wiring Before Modification

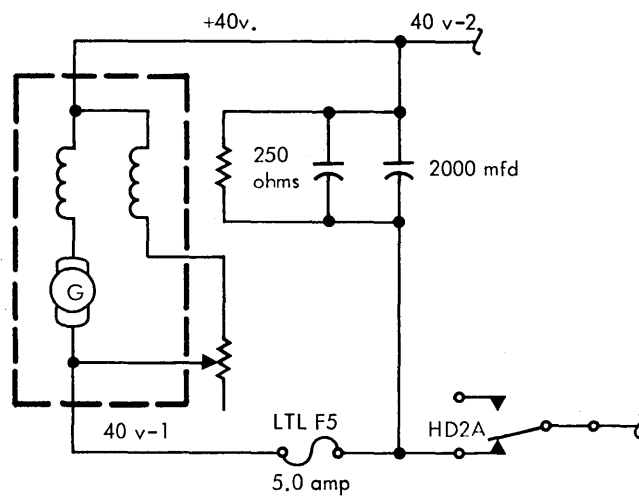


Figure 4-2. IBM 523 Power Supply Wiring After Modification

The following changes are required to reverse power supply polarity:

- a) Disconnect wire at 40v-2 which runs to 2000 mfd filter.
- b) Disconnect wire at 40v-2 which runs to LTL F5 fuse.
- c) Disconnect wire at HD2A which runs to generator.
- d) Disconnect wire at HD2A which runs to 2000 mfd filter.
- e) Connect wires which were disconnected in steps a and b to HD2A.
- f) Connect wires which were disconnected in steps c and d to 40v-2.

#### DISABLE RELAY HD2

The reason for this modification is that the coil of relay No. 11 is wired in parallel with that of HD2, and relay No. 11 must be operated while HD2 must remain inoperative.

Disconnect the wire at the coil of relay HD2. Wrap the end of the wire with insulation tape and tie it back.

#### RELAY NO. 1 WIRING CHANGE

The rectifier in the hold circuit of relay No. 1 must be reversed (reverse connections at rectifier) since the power supply polarity has been reversed.

#### ADJUSTMENT OF CAM P7 CONTACTS

The contacts of cam P7 must be set to make at 9.5 time and to break at 13.0 time. This is a standard IBM modification and is required by the timing control in the coupler.

#### MODE SWITCH SETTING

The toggle switch labeled DETAIL-MASTER must be in the MASTER position.

#### PATCH BOARD CONNECTIONS

Jumper leads must be inserted between the PUNCH MAGNETS and the COUNTER TOTAL EXIT points on the patch board.

#### NOTE

Cut out IBM modification data along dotted line and staple to inside cover of IBM Wiring Diagram Type 523 which is supplied with each IBM 523 Summary Punch Unit.

IMPORTANT

NOTE THE FOLLOWING MODIFICATIONS TO THIS UNIT

1. Power supply polarity is reversed.
2. The coil of the HD2 relay is open-circuited. (The wire to the coil is disconnected at the relay and is tied back and labeled.)
3. Polarity of the rectifier in relay circuit No. 1 has been reversed. (The wire connected to the anode has been interchanged with the wire to the cathode.)
4. Cam P7 is set to make at 9.5 time and to break at 13.0 time.

### SECTION 4-2. MAINTENANCE INSTRUCTIONS

#### PERIODIC SYSTEM TESTING

At regular maintenance intervals, and whenever malfunction is suspected, perform a system test routine to determine the operational status of the card punch system. SDS Catalog No. 034003 Card Punch Test Program, or equivalent, may be used for this purpose.

#### ADJUSTING COUPLER CIRCUITS

Monitor the output signals of the six coupler one-shot circuits in the sequence listed below, and adjust as necessary to obtain the required pulse duration. The START pushbutton on the IBM 523 must be held down and cards must be in the hopper to

perform these adjustment tests. Refer to the Logic Diagrams in PART V for connector and pin numbers of the one-shot outputs.

One-Shot	Pulse Duration
Dn	20 ms
Ec	40 ms
D9	30 ms
De	10 μsec
Fc	40 ms (Ground true side of Be flip-flop)
Sd	6.8 μsec (Ground $\bar{L}b$ )

PART V. REFERENCE DOCUMENTS

SECTION 5-1. LOGIC EQUATIONS FOR  
9157/91570 CARD PUNCH COUPLER

Punch Address - C's

$$Pa = \overline{C17} C18 \overline{C19} \overline{C20} C21 C22 \overline{C23}$$

Punch Address - W's

$$Lb = W9 \overline{W10} \overline{W11} W12 W13 \overline{W14}$$

Punch Binary

$$sPb = Pa Buc C14 \underline{Q2}$$

$$rPb = Pa Buc \overline{C14} \underline{Q2} + Dcr$$

Buffer Empty

$$sBe = \overline{Be} \underline{De}$$

$$rBe = Be Lb W5 \overline{W6} \overline{W0} \underline{Q2} + Dcr$$

Successful Cycle

$$sSc = \overline{Sc} Pr Cc \underline{De}$$

$$rSc = Sc Fc \underline{Q2} + Dcr$$

Column Tally

$$sCt = \overline{Ct} Pb \underline{Sd} + Ec D9$$

$$rCt = Ct Pb \underline{Sd} + Pb Dn Rt3 + Dcr$$

Shift Clock

$$sSd = Lb Be \overline{W5} \overline{W6} \underline{Q2} (ac)$$

$$rSd = 6.8 \mu sec$$

Buffer Clock

$$\textcircled{Ecr} = \overline{Sd}$$

Row Buffer Shift Clock

$$Sh = Lb Be Ct \underline{Sd}$$

Feed Card

$$sFc = Pa Buc Sc \overline{D9} \underline{Q2} (dc) + Sc \overline{Be} \overline{D9} \underline{Q2} (ac)$$

$$rFc = 40 msec$$

Row n Time

$$sDn = Edn (dc)$$

$$rDn = 20 msec$$

Row 9 Time

$$sD9 = Ed9 (dc)$$

$$rD9 = 30 msec$$

End Clock

$$sEc = D9 Ed9 (dc)$$

$$rEc = 40 msec$$

Delay Clock

$$sDe = (\underline{Dn} + \underline{D9} \underline{Ec}) (ac)$$

$$rDe = 10\mu sec$$

Test

$$\textcircled{Sio} = \overline{Pa Be (C13 + C12 Sc \overline{D9})}$$

Row Counter

$$sRc6 = \overline{Rc6} \underline{Dn}$$

$$rRc6 = Rc6 \underline{Dn} + Ec D9 + Dcr$$

$$sRc5 = \overline{Rc5} \underline{Rc6}$$

$$rRc5 = Rc5 \overline{Rc4} \underline{Rc6} + Ec D9 + Dcr$$

$$sRc4 = \overline{Rc4} Rc5 \underline{Rc6} + Ec D9$$

$$rRc4 = Rc4 Rc5 \underline{Rc6} + Dcr$$

$$sRc3 = \overline{Rc3} \underline{Rc4}$$

$$rRc3 = Rc3 \underline{Rc4} + Ec D9 + Dcr$$

Row	<u>Rc3</u>	<u>Rc4</u>	<u>Rc5</u>	<u>Rc6</u>	
12	0	1	0	0	Rt4
11	0	1	0	1	Rt5
0	0	1	1	0	Rt6
1	0	1	1	1	Rt7
2	1	0	1	0	Rt2
3	1	0	1	1	Rt3
4	1	1	0	0	Rt4
5	1	1	0	1	Rt5
6	1	1	1	0	Rt6
7	1	1	1	1	Rt7
8	0	0	1	0	Rt2
9	0	0	1	1	Rt3



Buffer Loading

$$sB80 = \begin{matrix} \textcircled{12} & \{ & \overline{R1} & R2 & Rt4 & Rc3 \\ & & \textcircled{11} & + & R1 & \overline{R2} & Rt5 & \overline{Rc3} \\ & & \textcircled{0} & + & (R1 & R2 & \overline{R3} & \overline{R4} & \overline{R5} & \overline{R6} & + & \overline{R1} & \overline{R2} & \overline{R3} & \overline{R4} & \overline{R5} & \overline{R6} \\ & & & & + & S_n) & Rt6 & \overline{Rc3} \\ & & \textcircled{1} & + & \overline{R3} & \overline{R4} & \overline{R5} & R6 & Rt7 & \overline{Rc3} \\ & & \textcircled{2-7} & + & (R4 & Rc4 & + & \overline{R4} & \overline{Rc4}) & (R5 & Rc5 & + & \overline{R5} & \overline{Rc5}) \\ & & & & (R6 & Rc6 & + & \overline{R6} & \overline{Rc6}) & Rc3 & \overline{S_n} \\ & & \textcircled{8} & + & Rt2 & \overline{Rc3} & R3 & (\overline{R4} & \overline{R5} & \overline{R6}) & \overline{S_n} \\ & & \textcircled{9} & + & Rt3 & \overline{Rc3} & R3 & (\overline{R4} & \overline{R5} & R6) & \overline{Pb} \\ & & \textcircled{12, 4} & + & [ & R1 & Rt4 \\ & & \textcircled{11, 5} & + & R2 & Rt5 \\ & & \textcircled{0, 6} & + & R3 & Rt6 \\ & & \textcircled{1, 7} & + & R4 & Rt7 \\ & & \textcircled{2, 8} & + & R5 & Rt2 \\ & & \textcircled{3, 9} & + & R6 & Rt3 & \overline{Pb} & \overline{S_n} \end{matrix}$$

$$rB80 = \overline{sB80} \overline{Sh}$$

$$sB79 = B80 \overline{Sh}$$

$$rB79 = \overline{B80} \overline{Sh}$$



$$sB1 = B2 \overline{Sh}$$

$$rB1 = \overline{B2} \overline{Sh}$$

$$S_n = (R1 \overline{R2} + \overline{R1} R2) (R3 \overline{R4} R5 \overline{R6})$$

Row Punching

$$Pm1 = Md B1$$

$$Pm80 = Md B80$$

$$Md = \overline{Be} (Edn + Ed9)$$

Halt

$$\textcircled{Whs} = \overline{Lb Be W0 W6}$$

Error

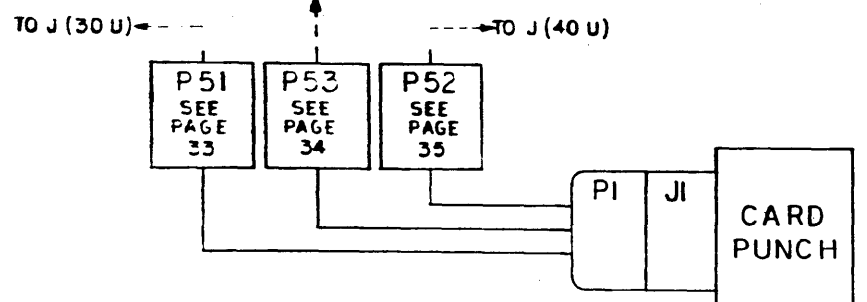
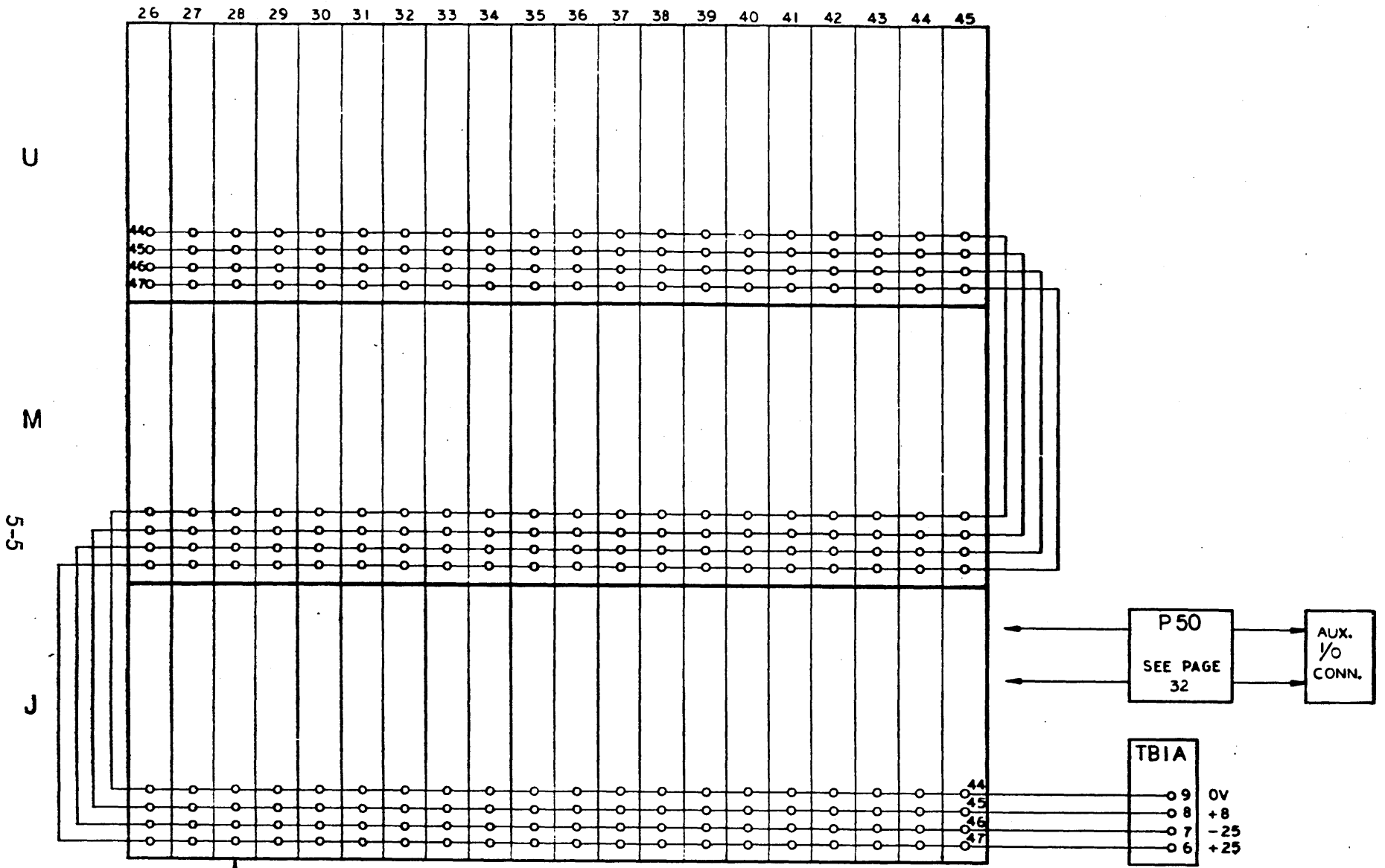
$$\textcircled{Wes} = \overline{Lb Ec Dc Cc} + Lb Be (Du + Dg Ec)$$

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REFERENCE DESIGNATIONS  
 ARE ABBREVIATED.  
 PREFIX THE DESIGNATION  
 WITH UNIT NUMBER  
 OR ASSEMBLY DESIGNATION  
 OR BOTH. (MIL. STD. 16B)

- NOTES:
1. REV LETTERS LISTED INDICATE STATUS OF EACH SHEET OF THIS MULTIPLE SHEET DRAWING.
  2. CHECK INDIVIDUAL SHEETS FOR REVISION LETTER AGAINST THIS SHEET BEFORE USING THIS DRAWING.

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CHASSIS U

CONNECTOR LOCATION

	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
TYPE	RK 53	RK 53	RK 53	RK 53	RK 53	P 52	RK 53	RK 53	RK 53	RK 53	RK 53	RK 53	RK 53	RK 53	RK 53	P 53	RK 53	RK 53	RK 53	RK 53
KEY LOC	8 22	8 22	8 22	8 22	8 22	22 26	8 22	8 22	8 22	6 22	8 22	8 22	8 22	8 22	8 22	18 46	8 22	8 22	8 22	8 22

CHASSIS M

CONNECTOR LOCATION

	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
TYPE	FH 15	FH 15	FH 15	FH 15	FH 15	RK 53	FH 15	FH 15	FH 15	FH 15	FH 15	FH 15	FH 15	FH 15	FH 15	RK 53	FH 15	FH 15	FH 15	FH 15
KEY LOC	8 30	8 30	8 30	8 30	8 30	8 22	8 30	8 30	8 30	6 30	8 30	8 30	8 30	8 30	8 30	8 30	8 30	8 30	8 30	8 30

CHASSIS J

CONNECTOR LOCATION

	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
TYPE	AUX	FH 17	FH 17	GK 51	GK 51	FH 15	IK 51	BH 10	GK 51	IH 11	Ox 13	GK 51	GK 52	IK 51	IK 51	FH 15	IC 12	P 53	Ox 13	RK 53
KEY LOC	6 26	2 32	2 32	2 22	2 22	8 30	2 8	2 42	2 22	2 16	2 46	2 22	2 20	2 8	2 8	8 30	10 34	22 28	2 46	8 22

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CHART, MODULE LOCATION  
CARD PUNCH COUPLER

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MODULE LIST

ITEM	DESCRIPTION	MODEL	QTY
1	RELAY DRIVER	RK53	21
2	AND OR BUFFER	BH10	1
3	COUNTER FF	FH15	20
4	UNIVERSAL FF	FH17	2
5	DIODE GATE 1	GK51	4
6	DIODE GATE 2	GK52	1
7	OR GATE INVERTER	IH11	1
8	AND INVERTER	IC12	1
9	INVERTER AMPLIFIER	IK51	3
10	MULTIVIBRATOR	CX13	2

REPLACEMENT PARTS LIST

ITEM	DESCRIPTION	DESIGNATION	QTY	SUPPLIER CODE (SEE INDEX)
1	RESISTOR, 820Ω ±2%	(P53) R1 THRU R3	3	16, 17
2	RESISTOR, 470Ω ±2%	(P50) R1 THRU R31	31	16, 17
3	RESISTOR, 8.2KΩ ±2%	(P50) R32 THRU R35 (P53) R4 THRU R7	8	16, 17
4	RESISTOR, 33KΩ ±2%	(P53) R8	1	16, 17
5	INDUCTOR, 220μh ±5%	(P50) L1 THRU L31	31	42, 90, 91
6	CAPACITOR, MYLAR .001μf ±10%	(P53) C2	1	26, 27, 74
7	CAPACITOR, TANTALUM 15μf ±10%	(P53) C1	1	22, 23, 76
8	DIODE, SILICON SWITCHING IN907A IN914A IN3063 IN3065	(P50) CR1 THRU CR4 (P53) CR1	5	4, 13 4, 12, 13, 14 4, 6 4
9	CONNECTOR, SOLDER TAIL 47 CONTACT #7008-47	J(26M) THRU J(45M) J(26U) THRU J(45U) J(26J) THRU J(45J)	60	82
10	RESISTOR, 27KΩ ±2%	(P53) R11	1	16, 17
11	RESISTOR, 10Ω ±2%	(P53) R9, R10	2	16, 17
12	CAPACITOR, MYLAR .01μf ±10%	(P53) C3, C4	2	26, 27, 74
13	DIODE, SILICON SWITCHING IN3183	(P53) CR3	1	2, 6, 30, 68

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SIGNAL	PAGE	SIGNAL	PAGE	SIGNAL	PAGE
B1 → B8	24	D9	12	Fa	7
B9 → B16	23	$\overline{D9 Ec}$	12	Fa Buc	7
B17 → B24	22	$\overline{D9 Ec^*}$	12	Fb	7
B25 → B32	21	$\overline{D9 Sc}$	12	Fb*	9
B33 → B40	20	Dcr	8	$\overline{Fb}$	7
B41 → B48	19	De	12	$\overline{Fb^*}$	9
B49 → B56	18	Dn	12	Fc	12
B57 → B64	17	(Dn + D9 Ec)	12	Fm1 → Fm8	31
B65 → B72	16			Fm9 → Fm20	30
B73 → B80	15			Fm21 → Fm32	29
Be	7			Fm33 → Fm44	28
$\overline{Be}$	7			Fm45 → Fm56	27
Buc	7	Ec	12	Fm57 → Fm68	26
Buc*	7	$\overline{Ecw}$	12	Fm69 → Fm80	25
		$\overline{Ed9}$	13	Fr	13
		$\overline{Ed9}$	13	$\overline{Fr}$	13
		$\overline{Edn}$	13		
		$\overline{Edn}$	13		
C12	12				
C13	12				
C14	7			Q2	7
C14*	7			Q2*	7
$\overline{C14}$	7	Fc	12		
$\overline{C17}$	7				
C18	7				
C19	7				
C20	7			R1	11
C21	7	Lb	7	R1 Lb	11
C22	7	Lb*	11	( $\overline{R1} + \overline{Lb}$ )	11
C23	7	Lb Buc	7	R2	11
Cc	13	$\overline{Lb}$	7	R2 Lb	11
$\overline{Cc}$	13			( $\overline{R2} + \overline{Lb}$ )	11
( $\overline{Cc} + \overline{Ec}$ )	12			R3	11
Ct	8			R3 Lb	11
$\overline{Ct}$	8			( $\overline{R3} + \overline{Lb}$ )	11
		$\overline{Md}$	14	R4	11
		Md0 → Md2	14		

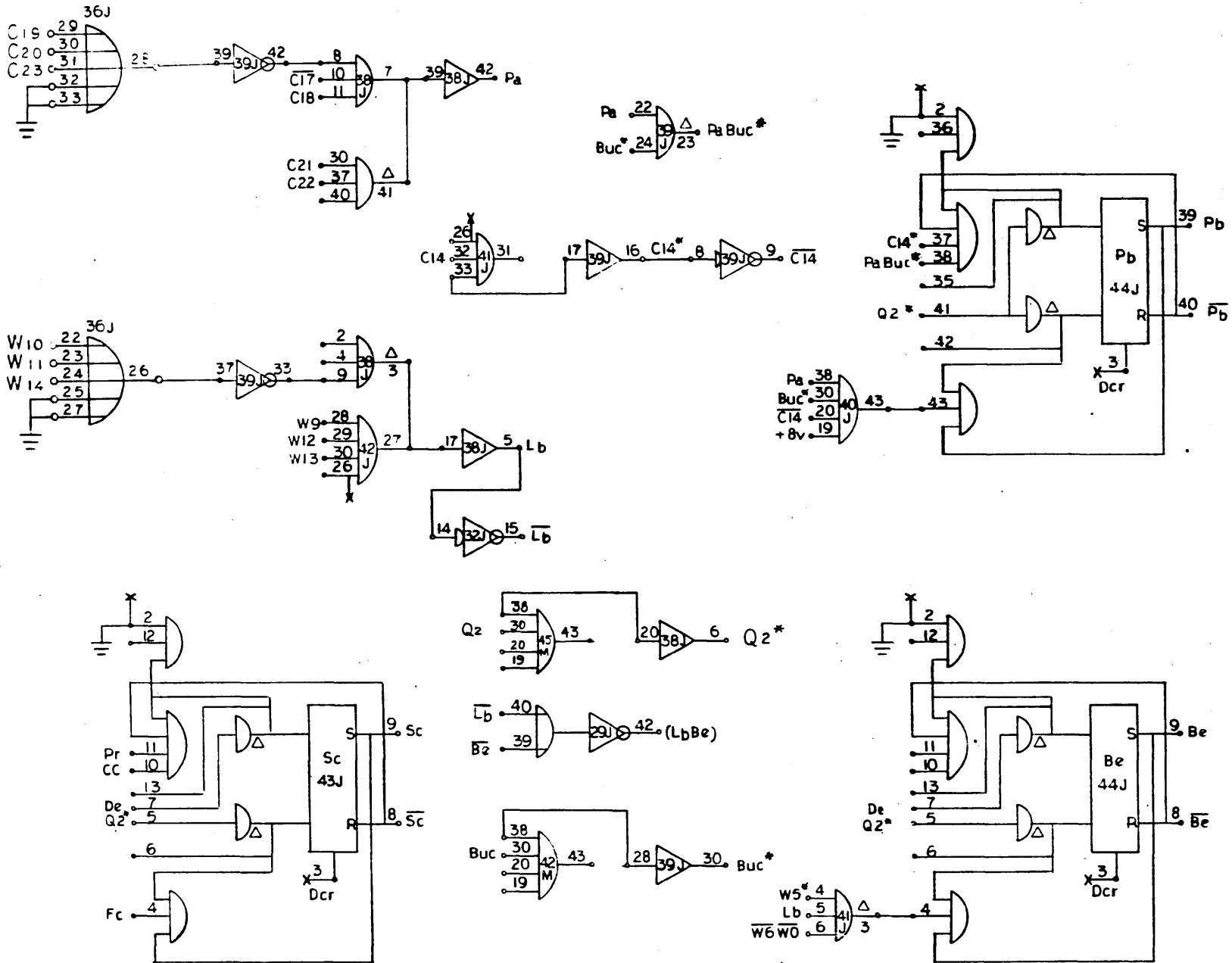
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SIGNAL PAGE SIGNAL PAGE

R4 Lb	11	W0	12
(R4 + Lb)	11	W5	12
R5	11	W5*	12
R5 Lb	11	W5 W6 Lb	14
(R5 + Lb)	11	W6	12
R6	11	W6*	12
R6 Lb	11	W6 W0	12
(R6 + Lb)	11	W9 → W14	7
(R4 R5 R6) S <sub>1</sub>	9	Wes	12
Ra	11	Whe	12
Rc3	8		
Rc3	8		
Rc3*	8		
Rc4	8		
Rc4*	8		
Rc4	8		
Rc4*	8		
Rc5	8		
Rc5*	8		
Rc5	8		
Rc6	8		
Rc6*	8		
Rc6	8		
Rc6*	8		
Ra	9		
Ra	9		
[Rt2] → [Rt7]	9		
aB80	10		
R	7		
R	7		
Sb0 → Sb5	14		
Sb0	12		
W	9		

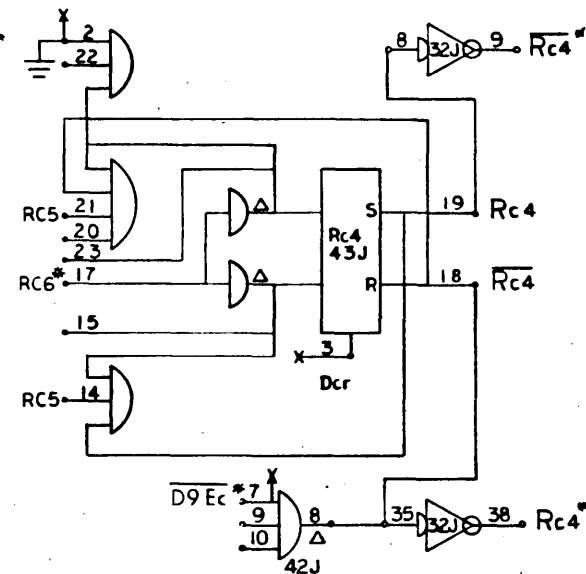
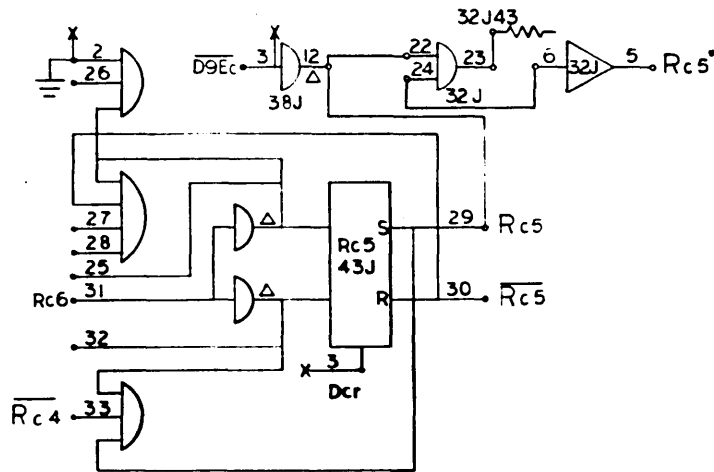
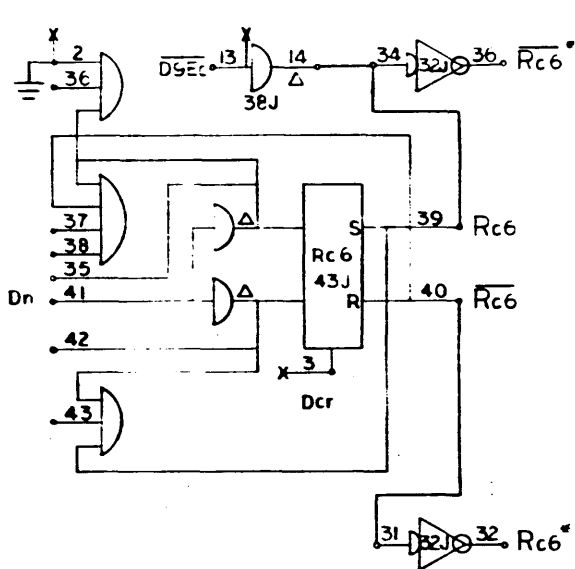
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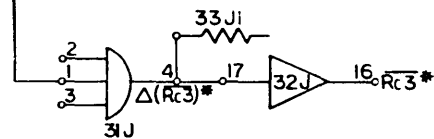
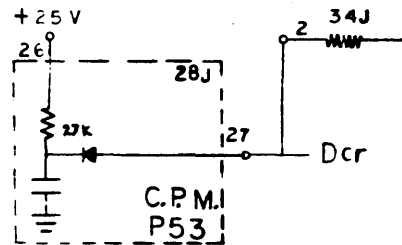
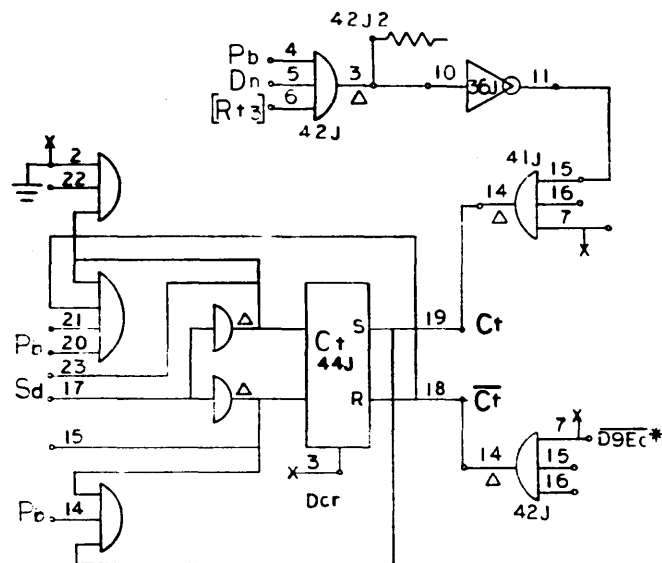
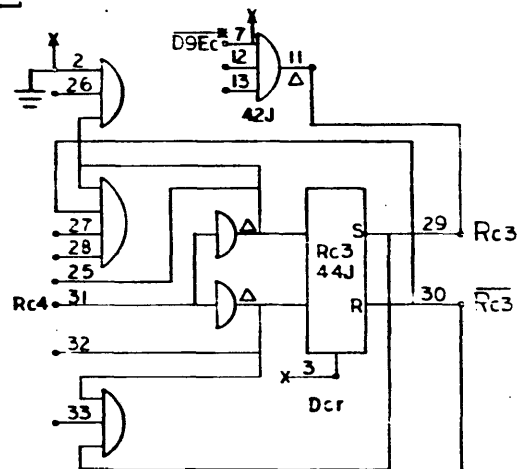


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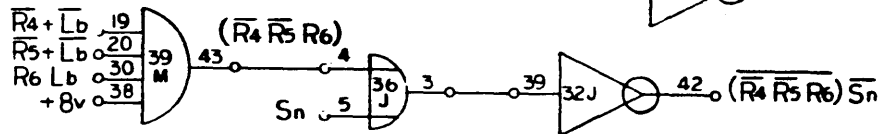
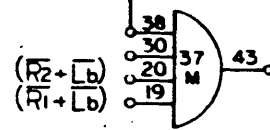
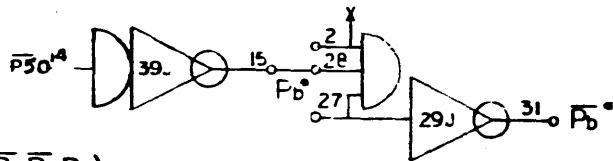
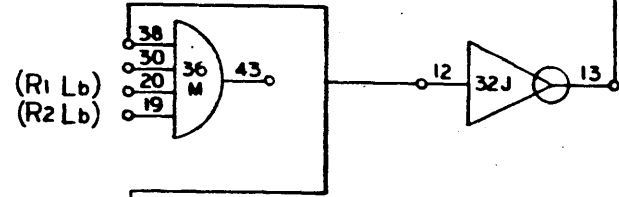
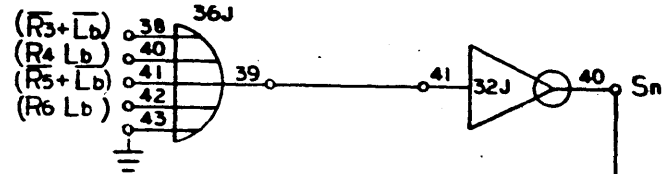
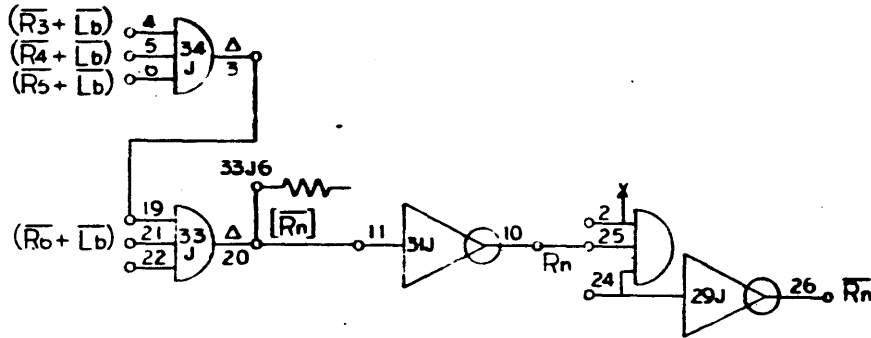
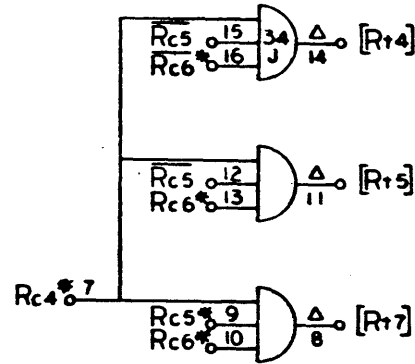
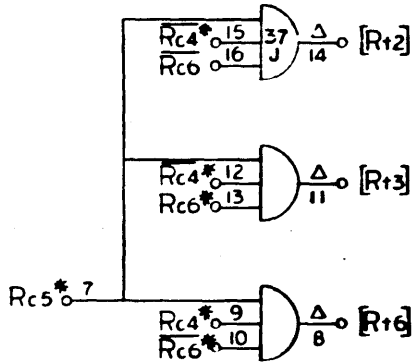
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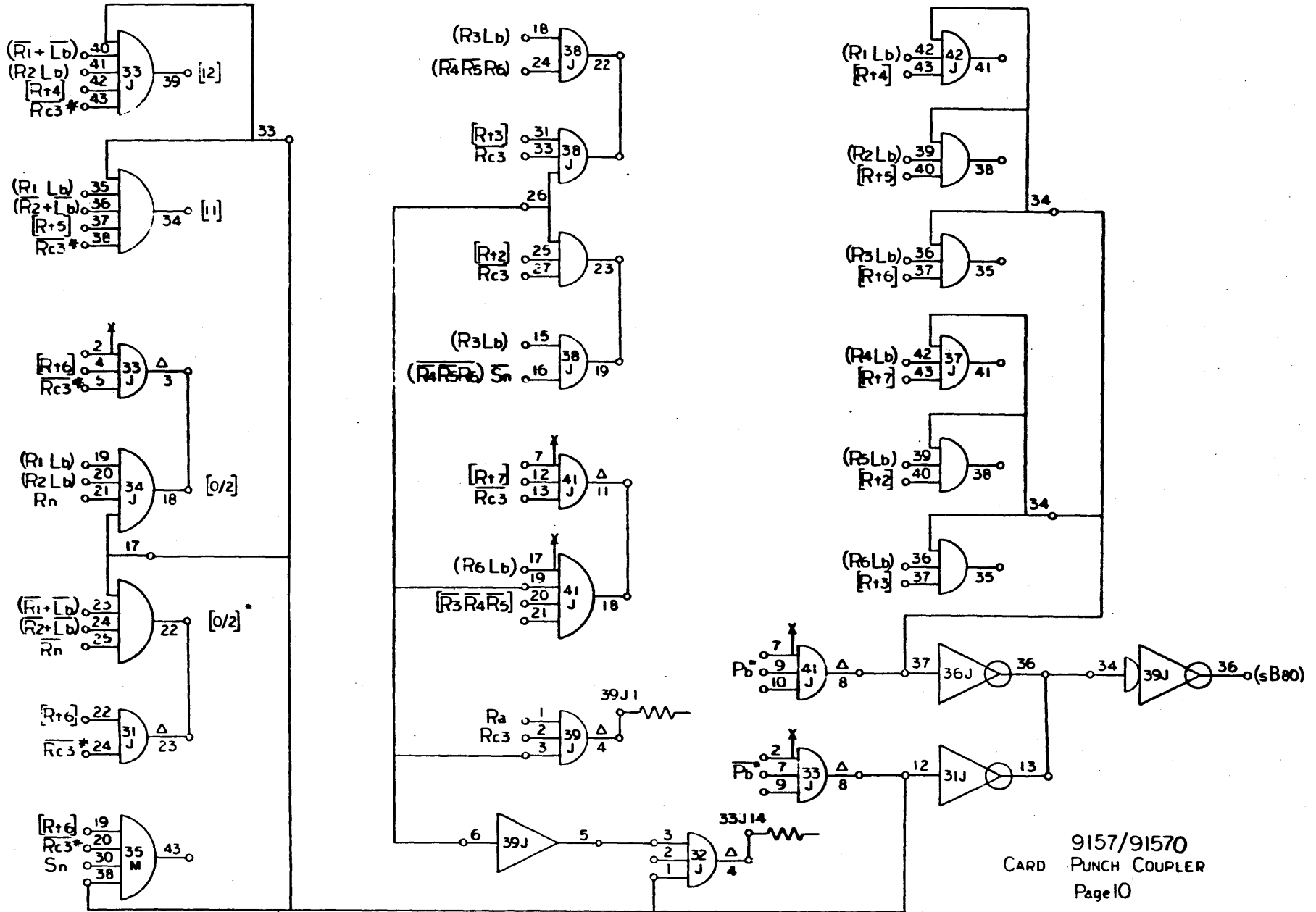
Row	RC3	RC4	RC5	RC6	
12	0	1	0	0	Rt4
11	0	1	0	1	Rt5
0	0	1	1	0	Rt6
1	0	1	1	1	Rt7
2	1	0	1	0	Rt2
3	1	0	1	1	Rt3
4	1	1	0	0	Rt4
5	1	1	0	1	Rt5
6	1	1	1	0	Rt6
7	1	1	1	1	Pt7
8	0	0	1	0	Rt2
9	0	0	1	1	Rt3

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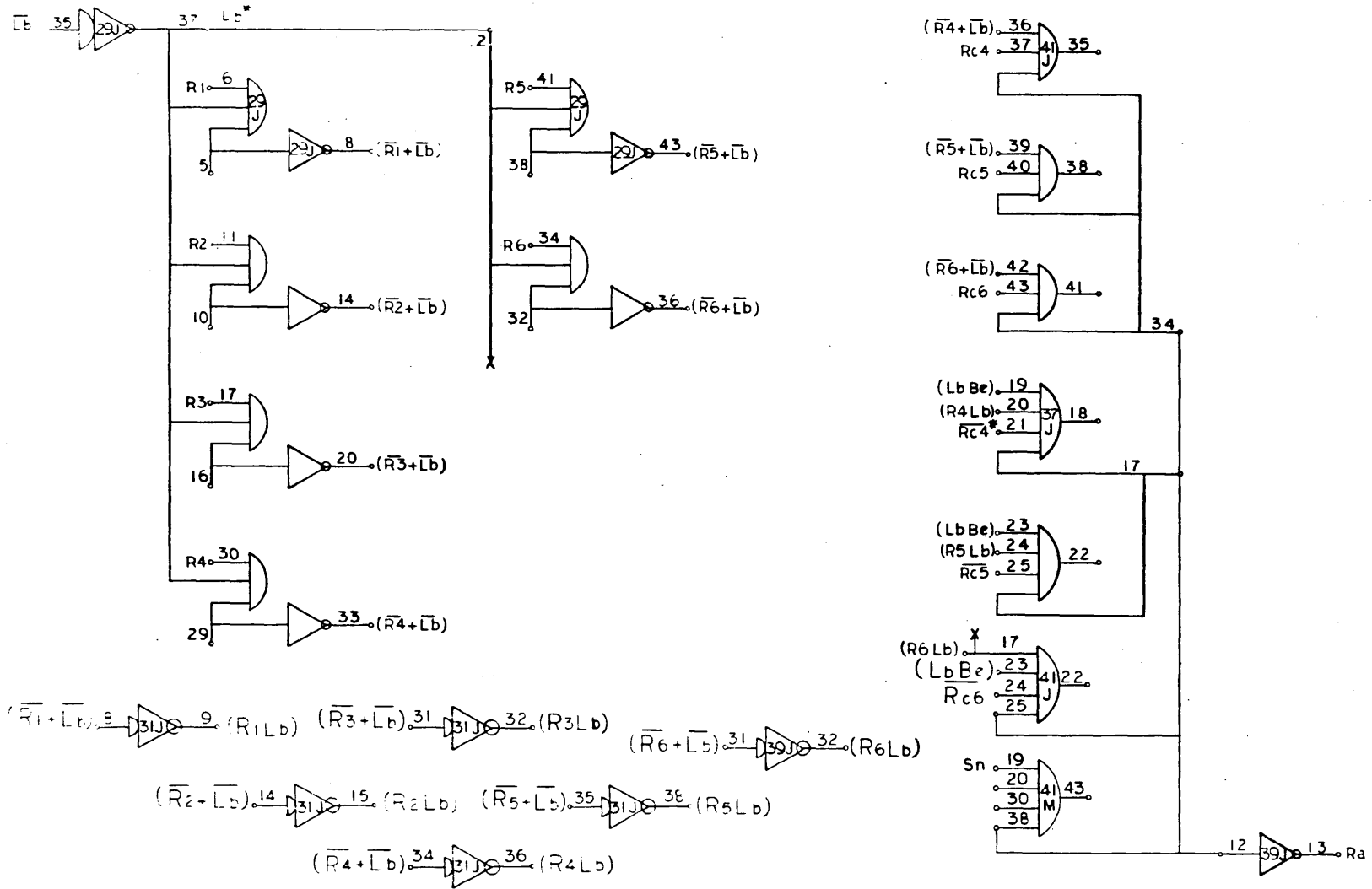
5-13



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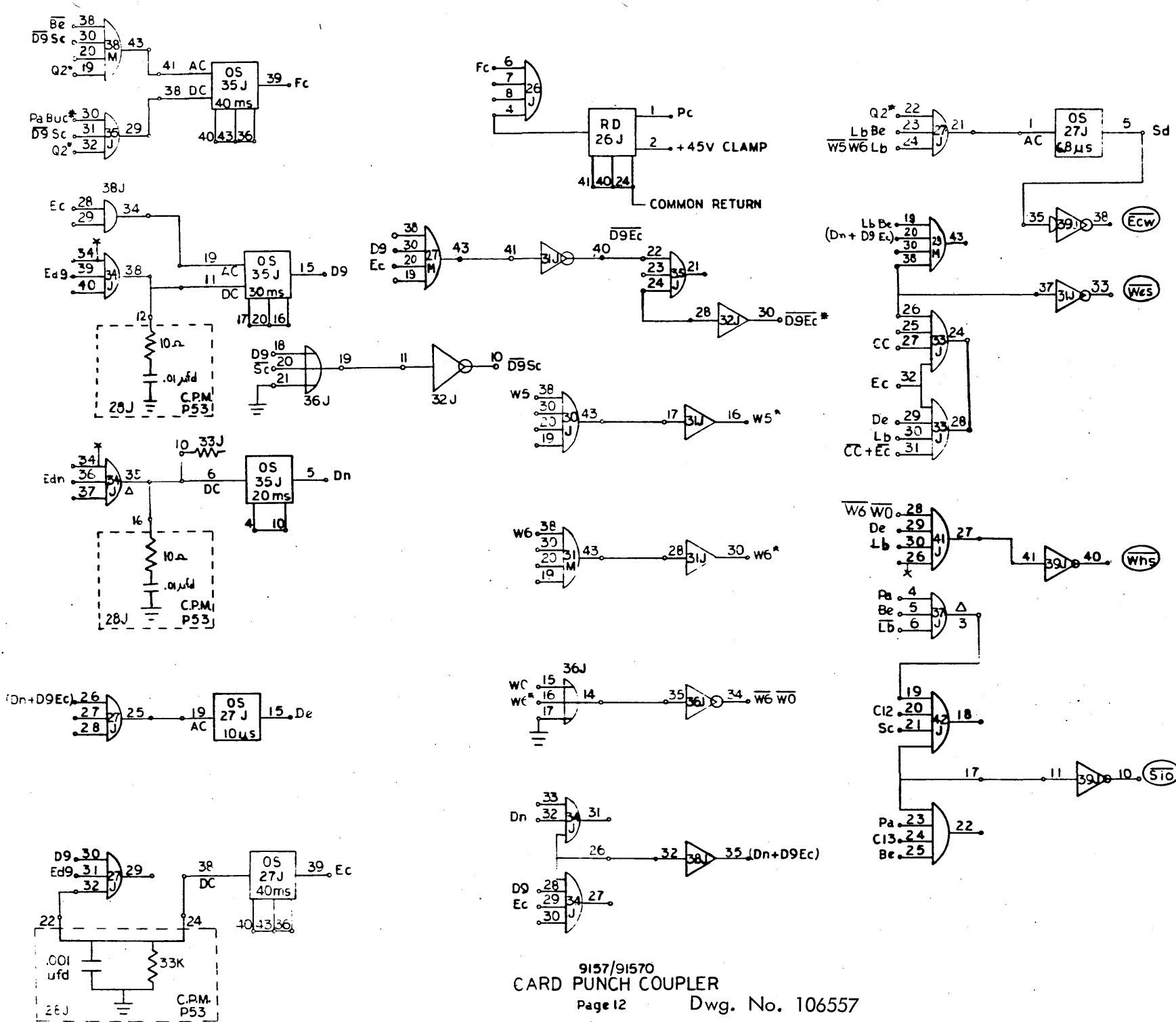
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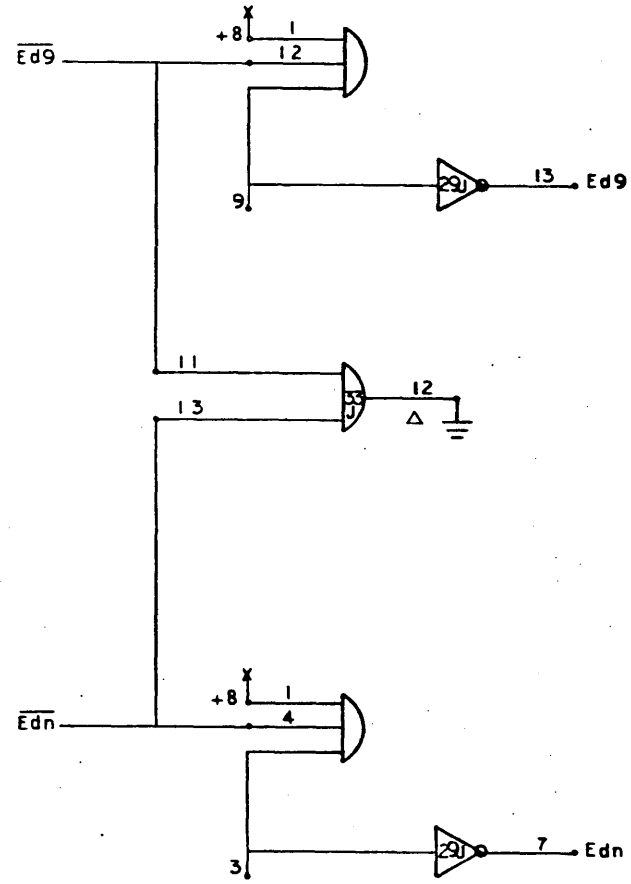
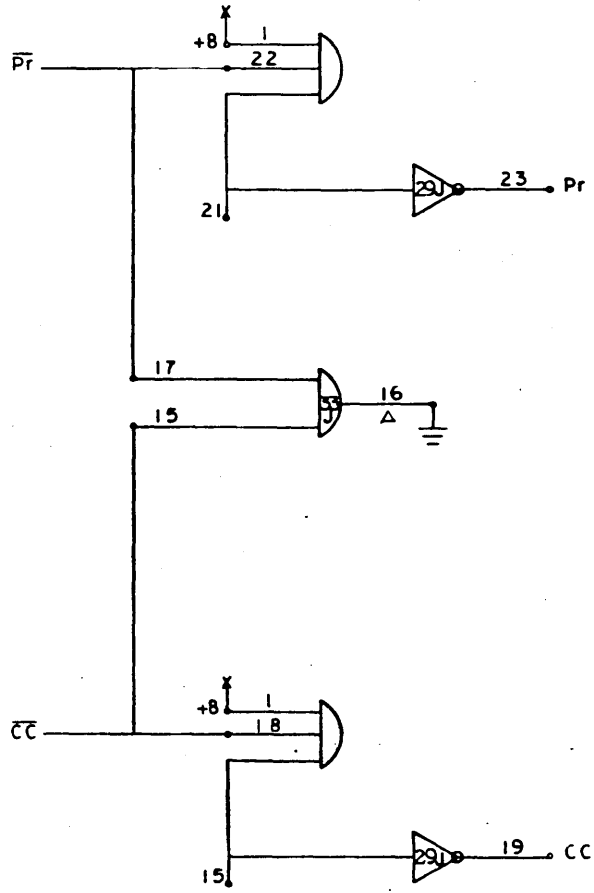
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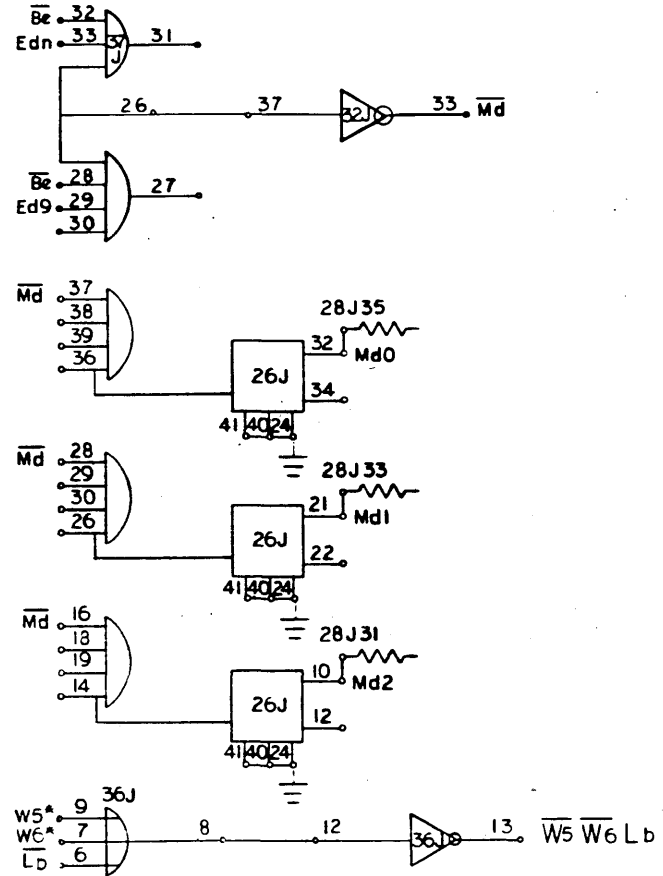
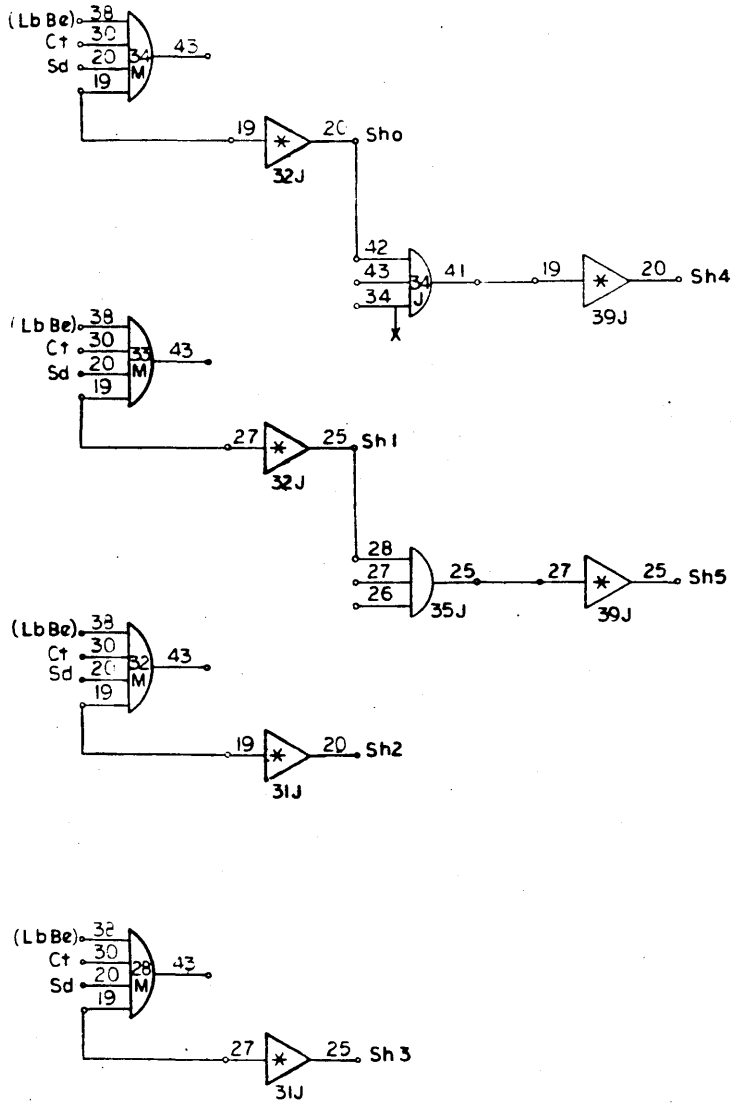


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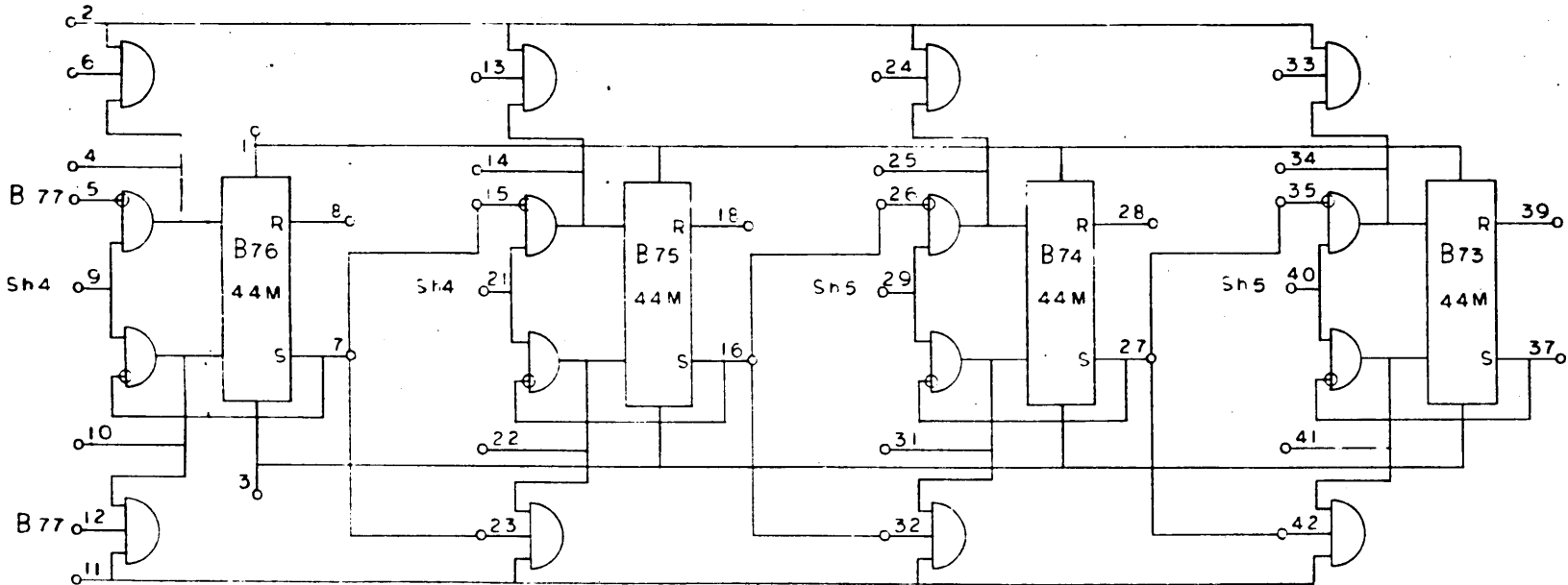
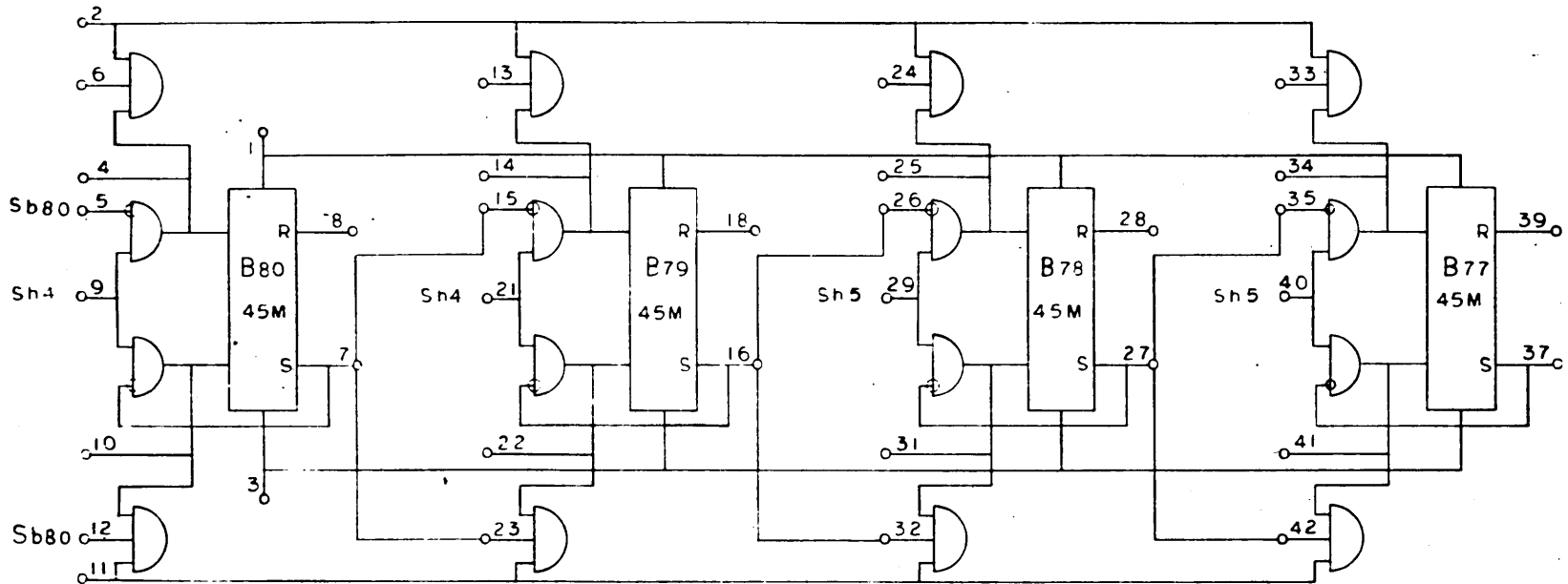


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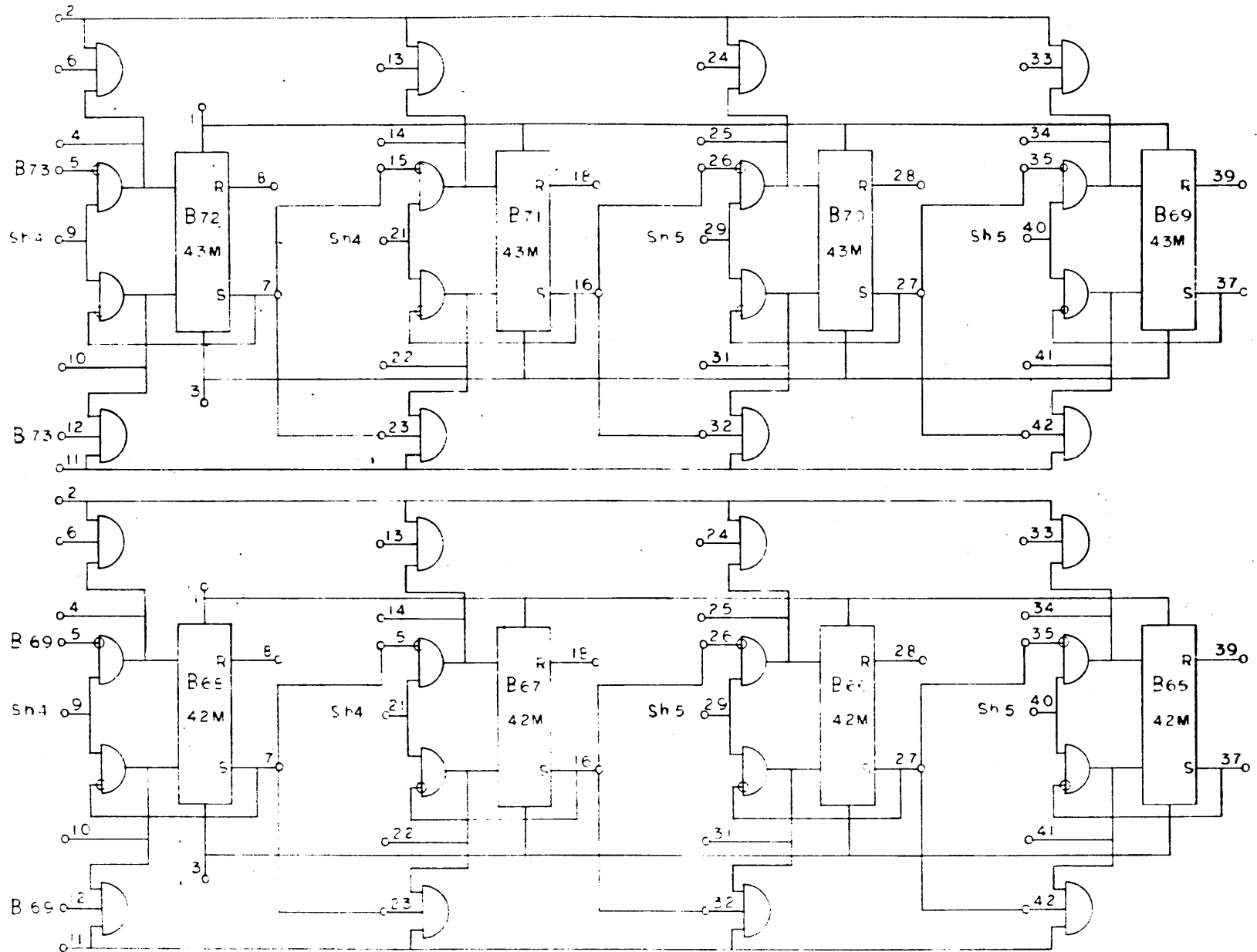


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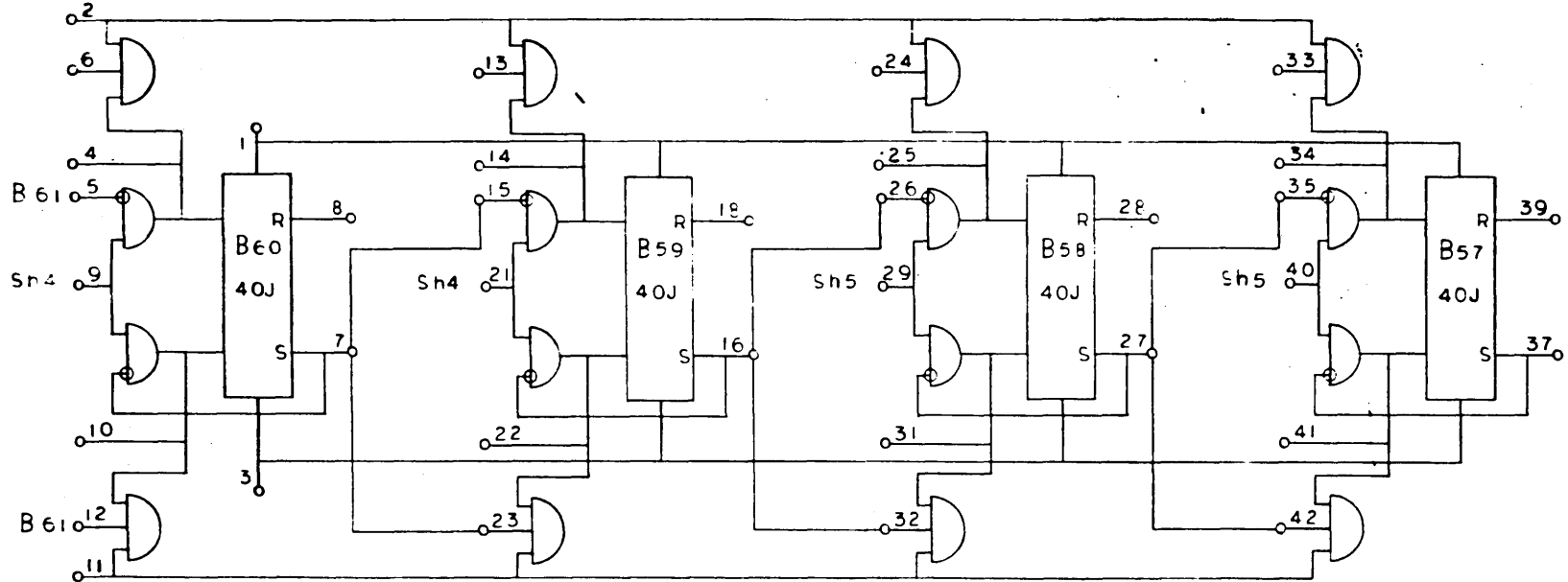
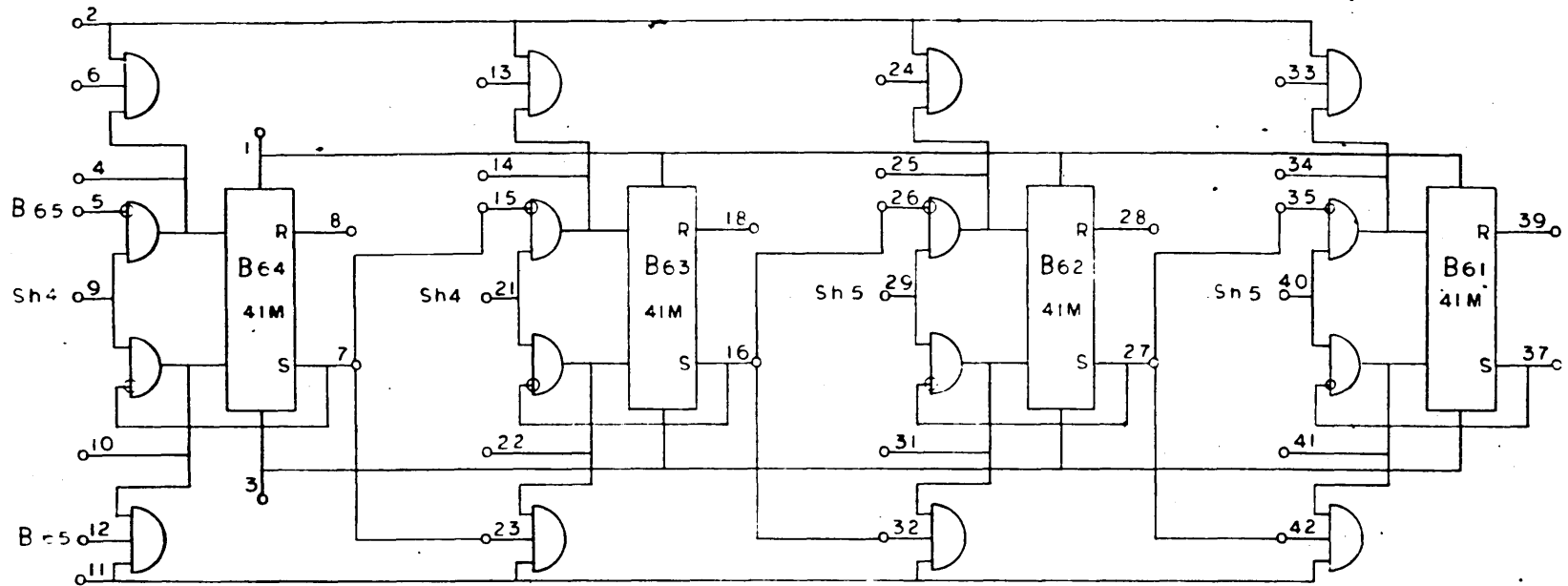




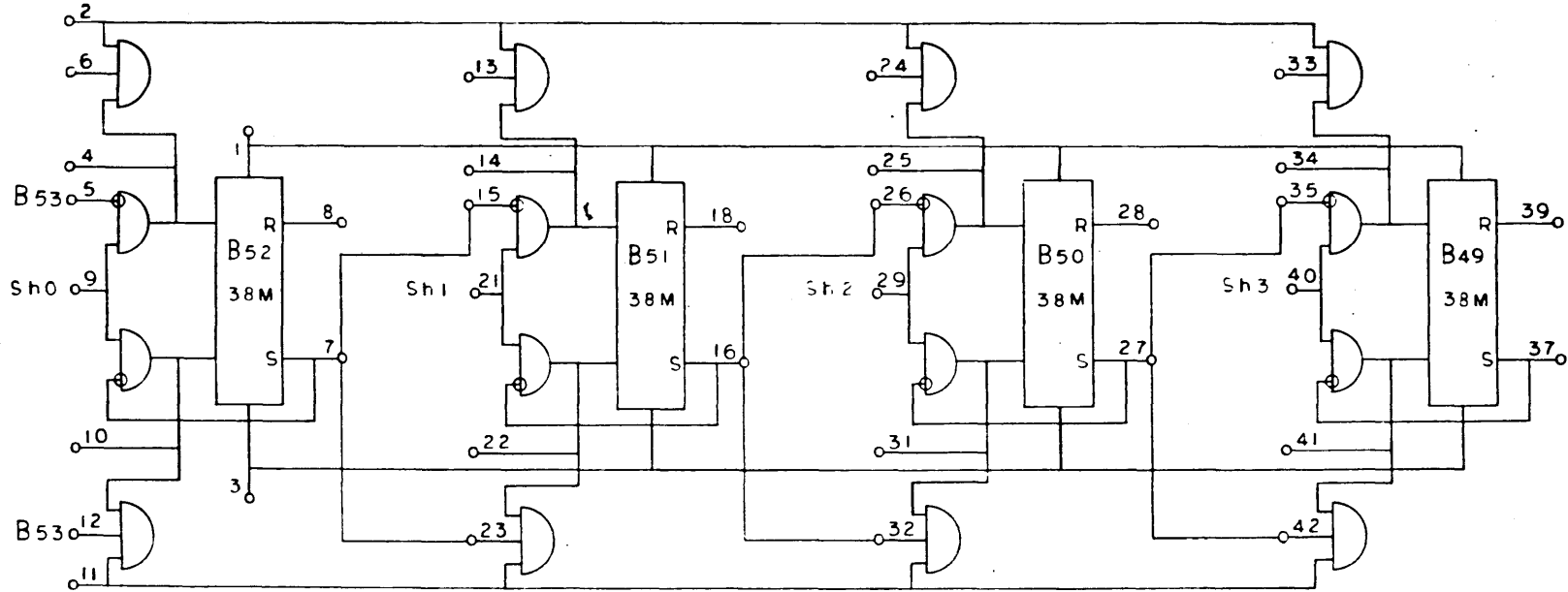
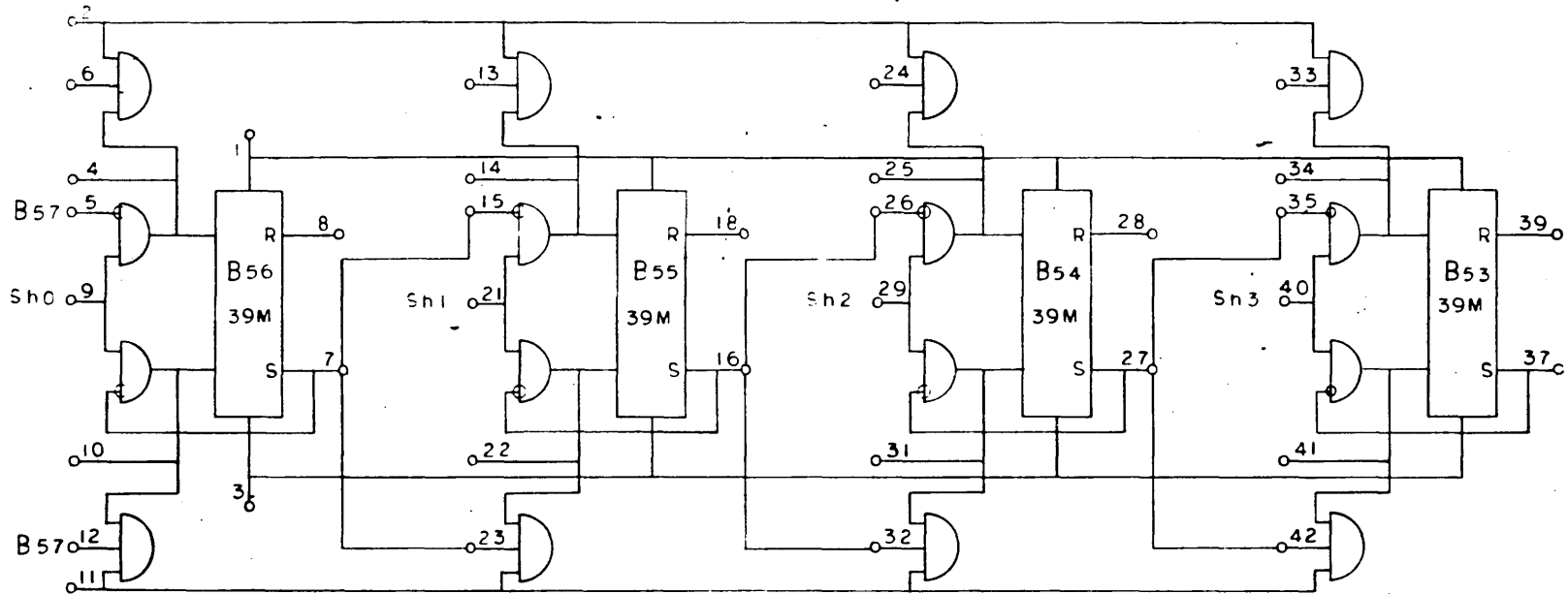
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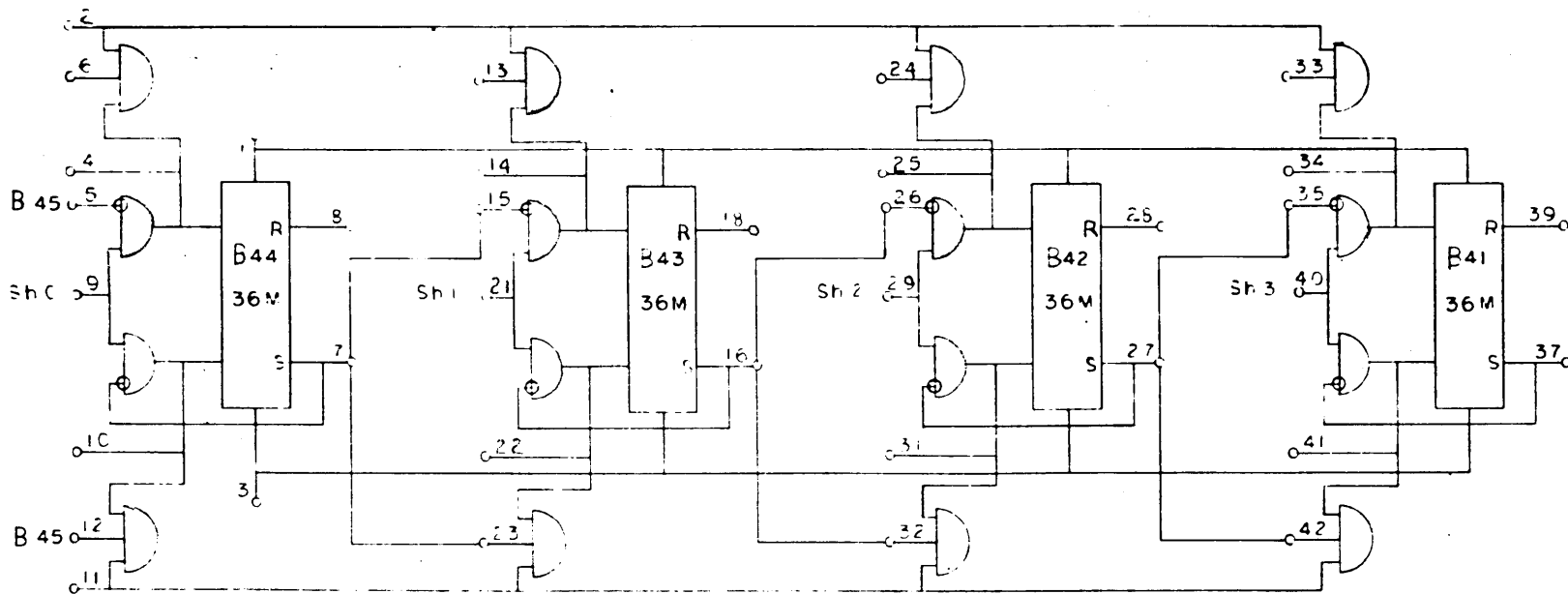
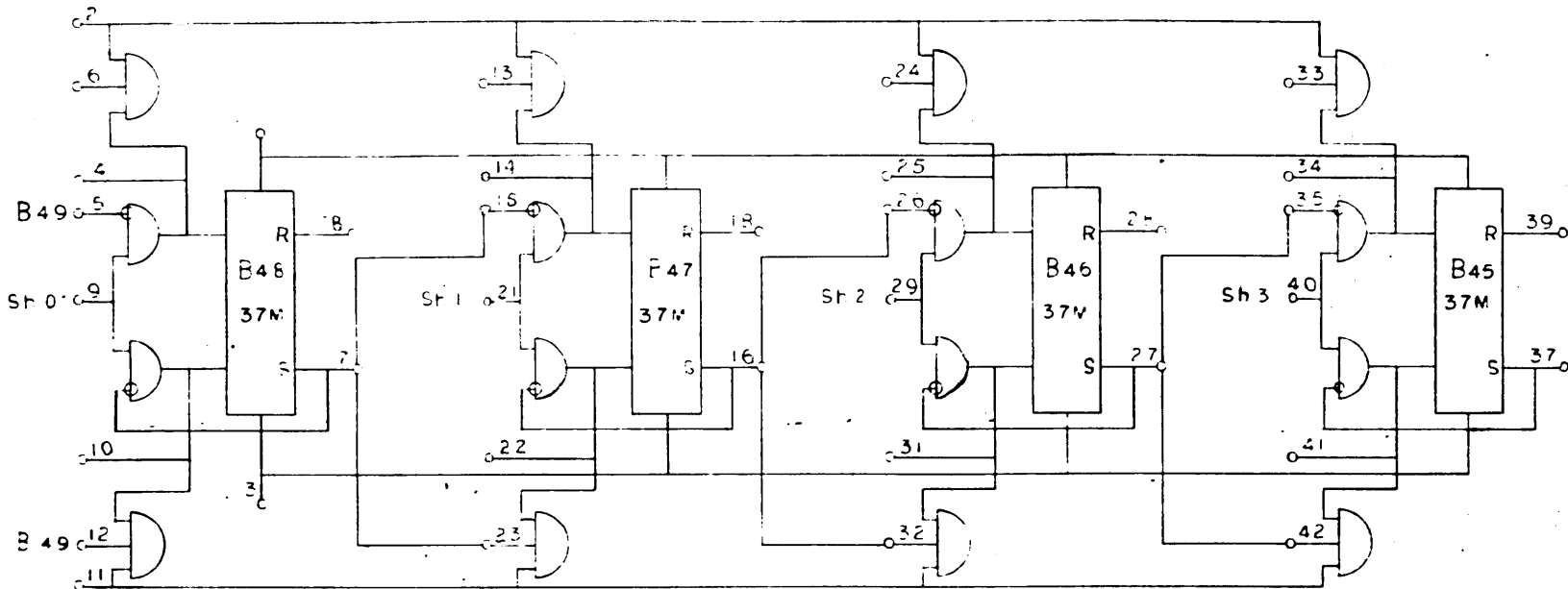


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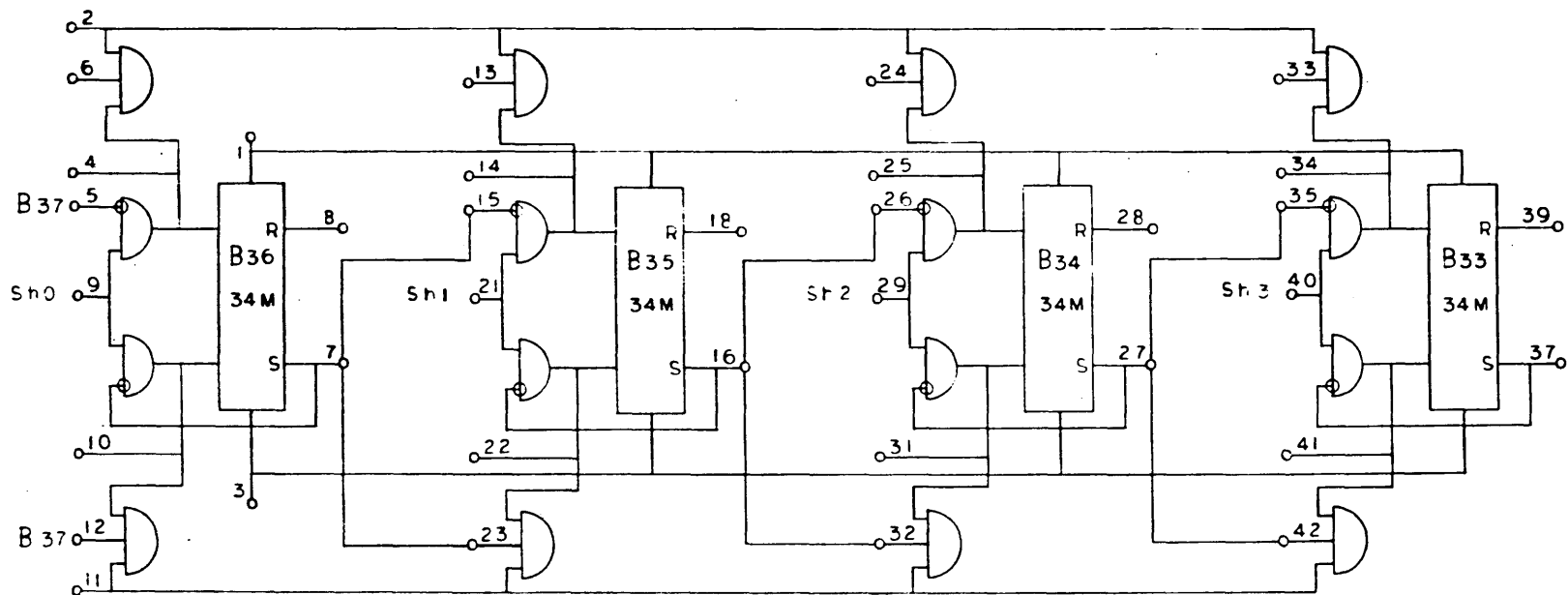
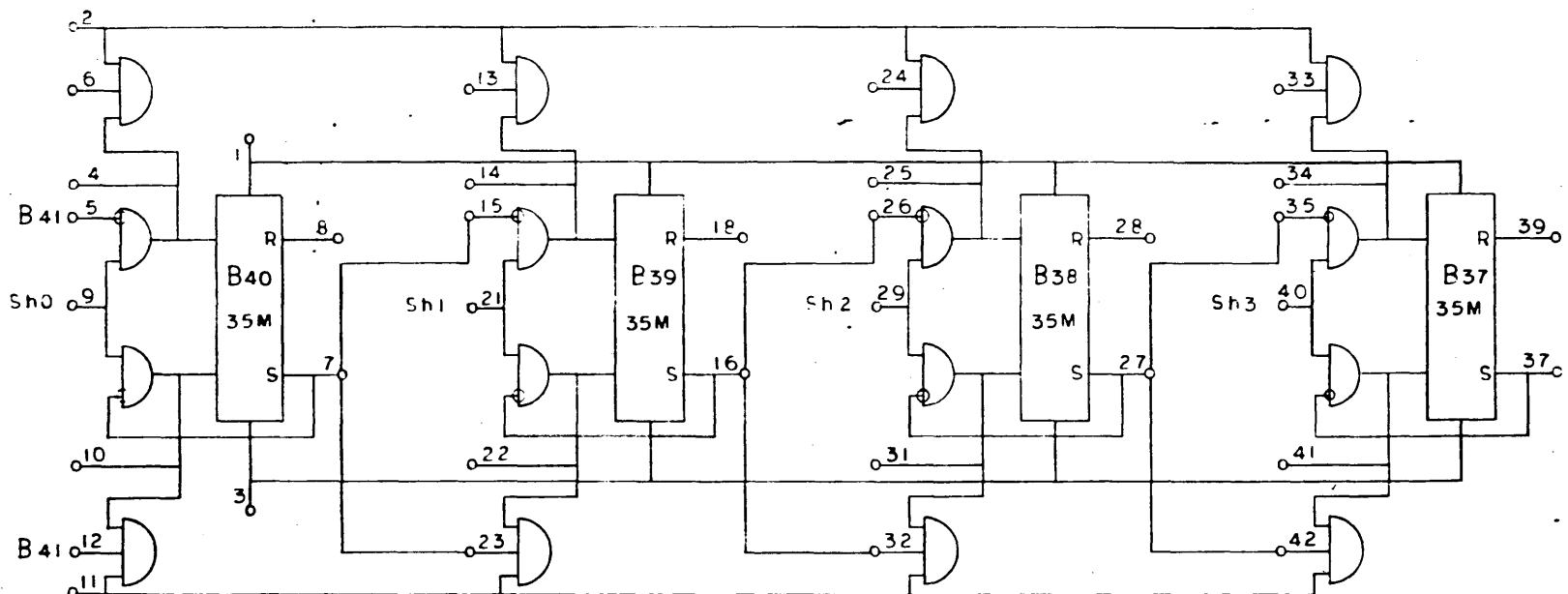
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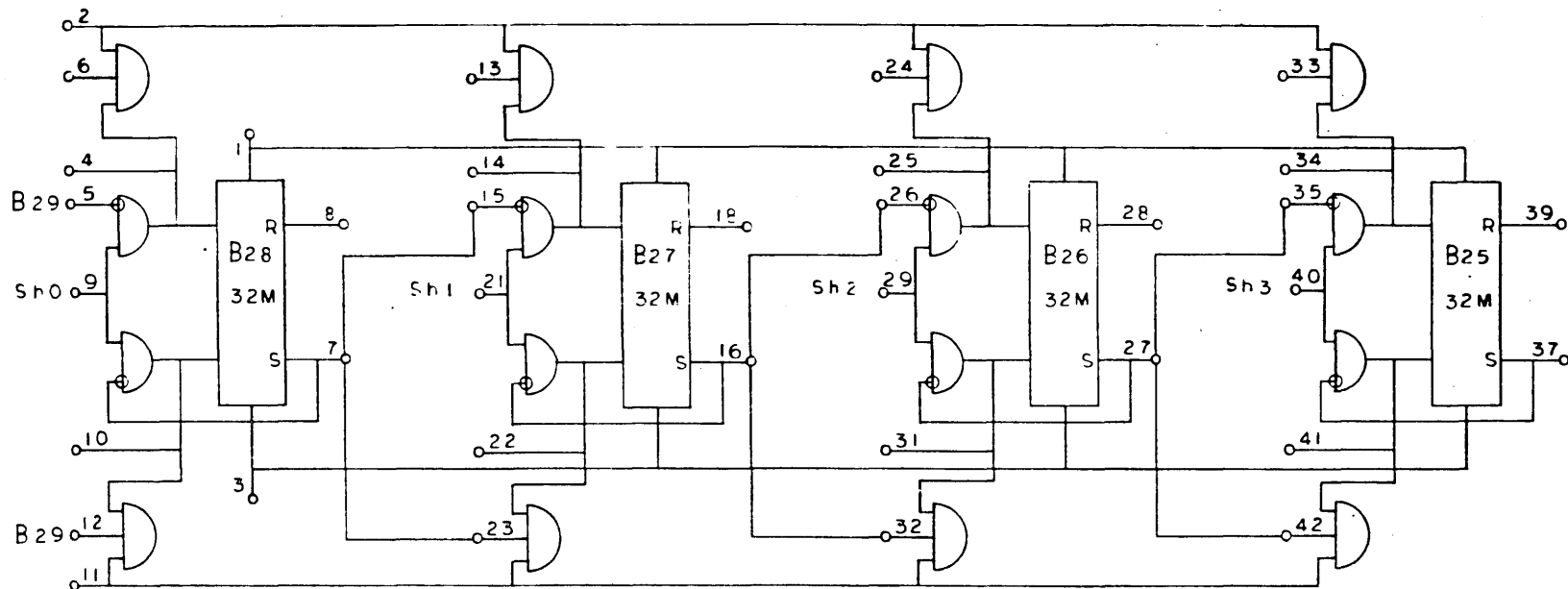
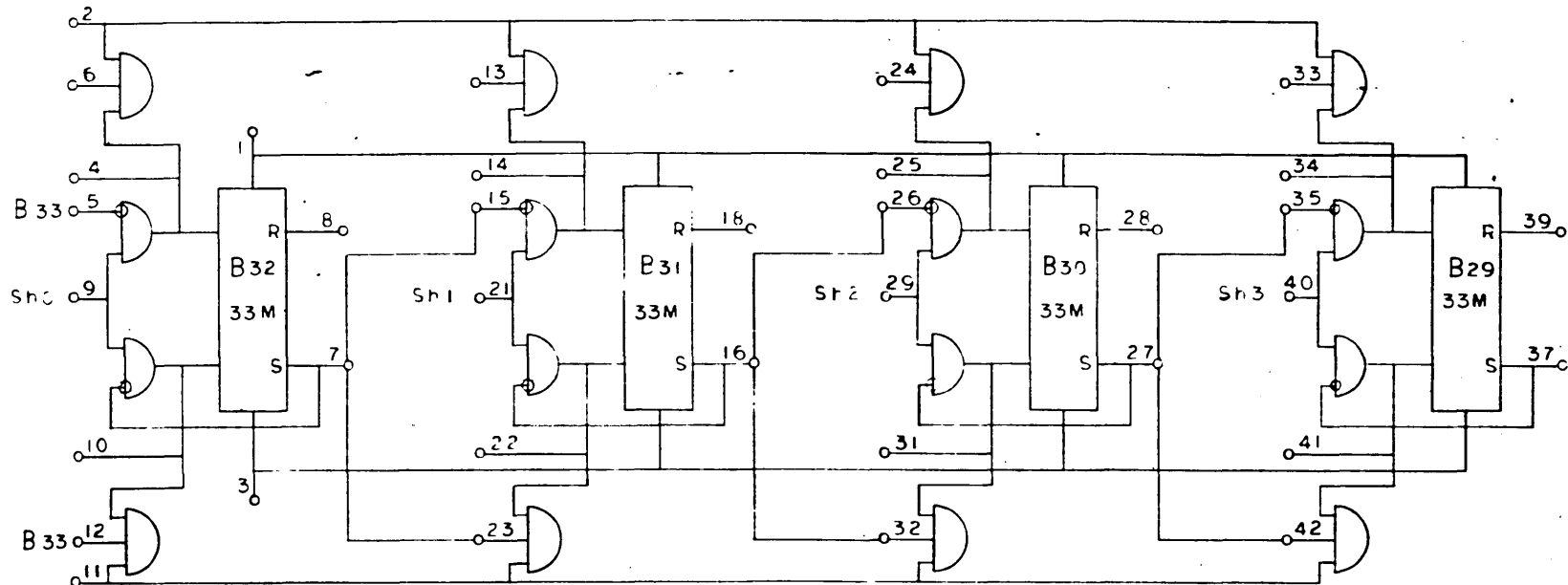




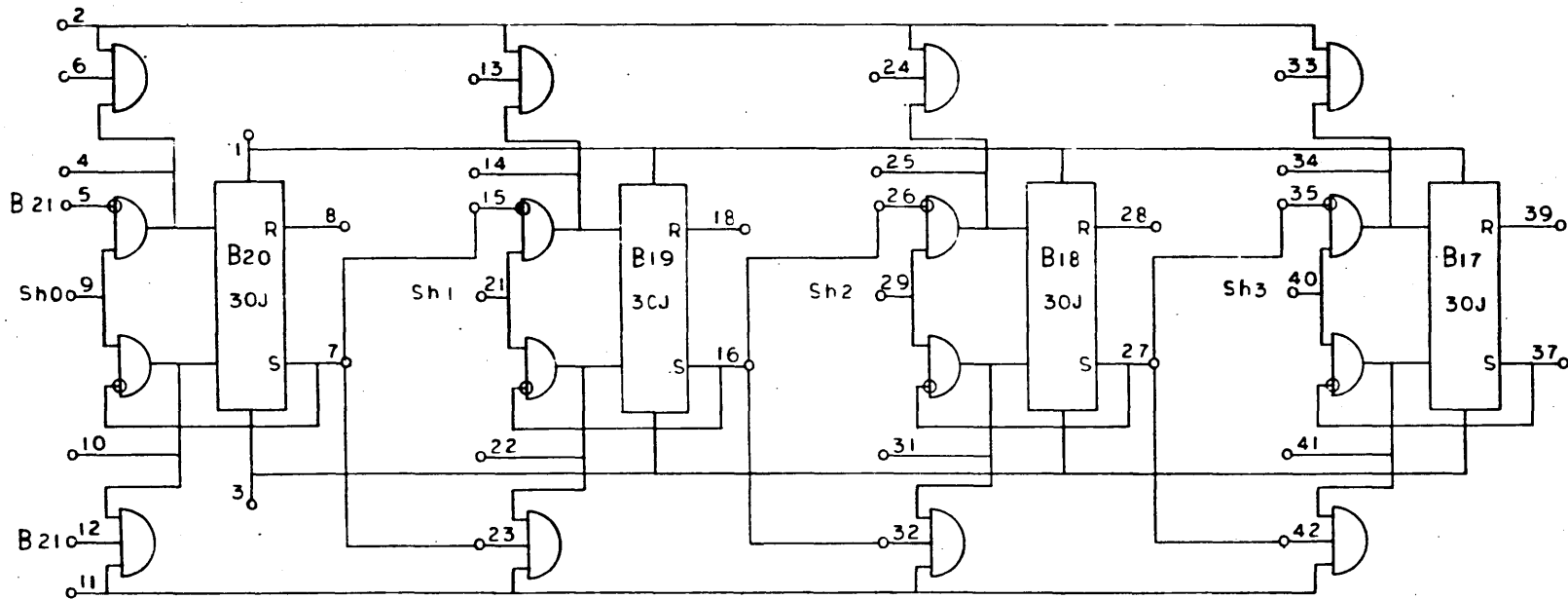
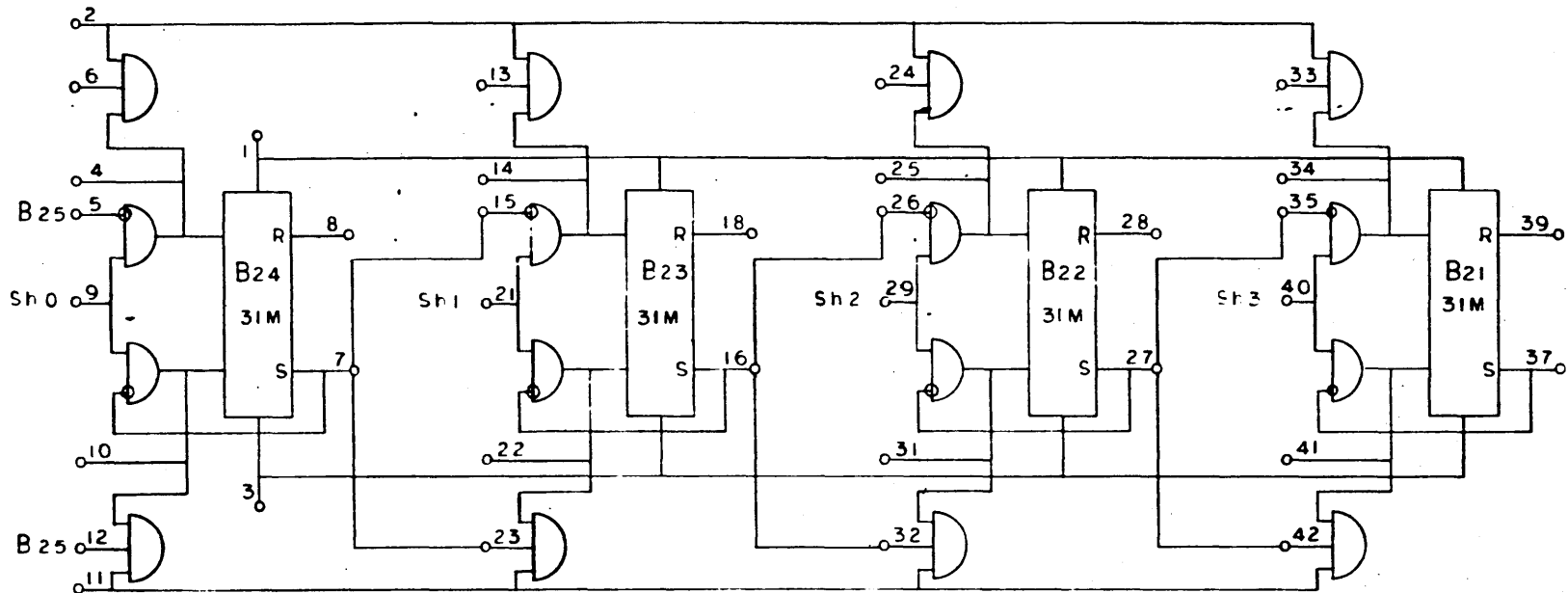
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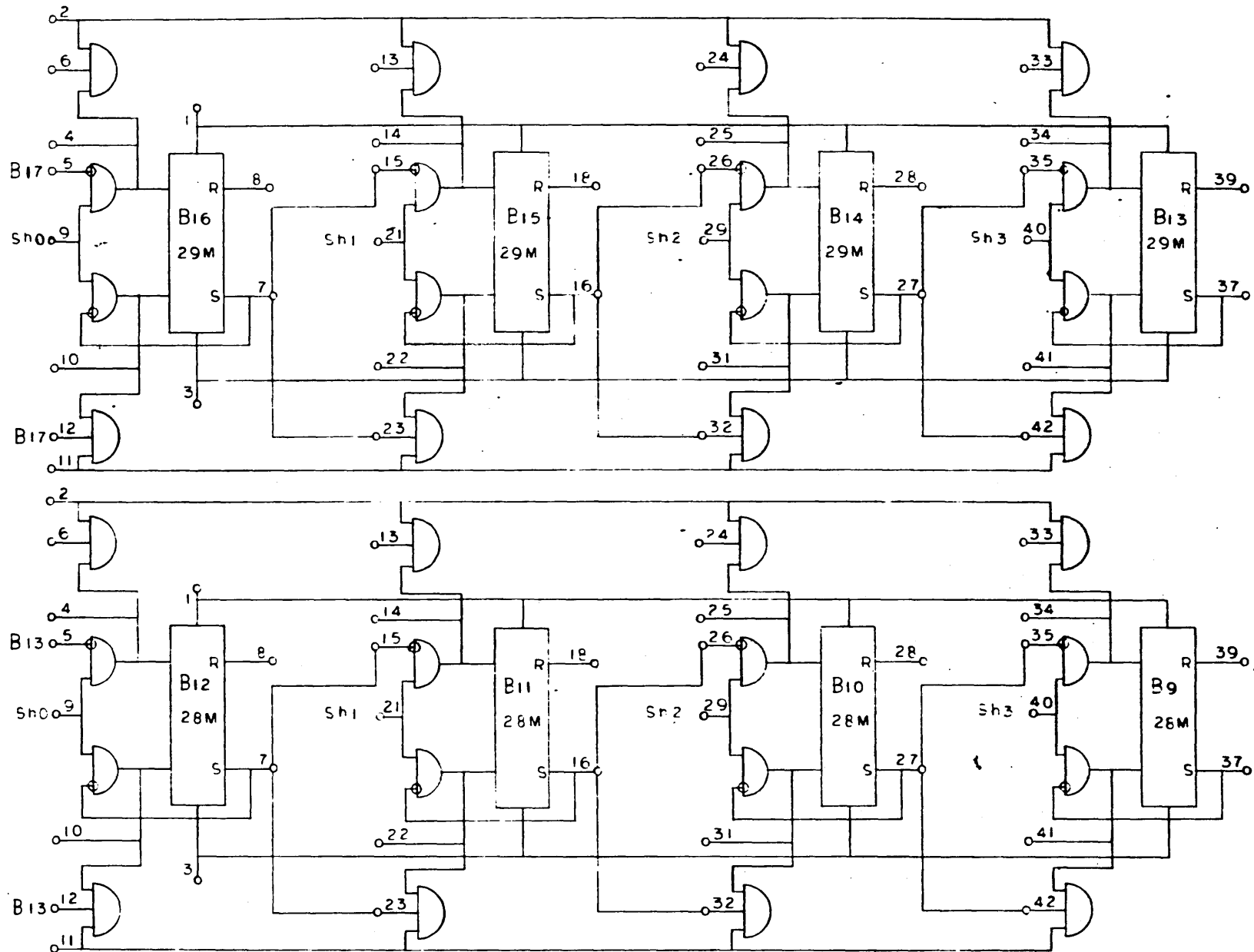


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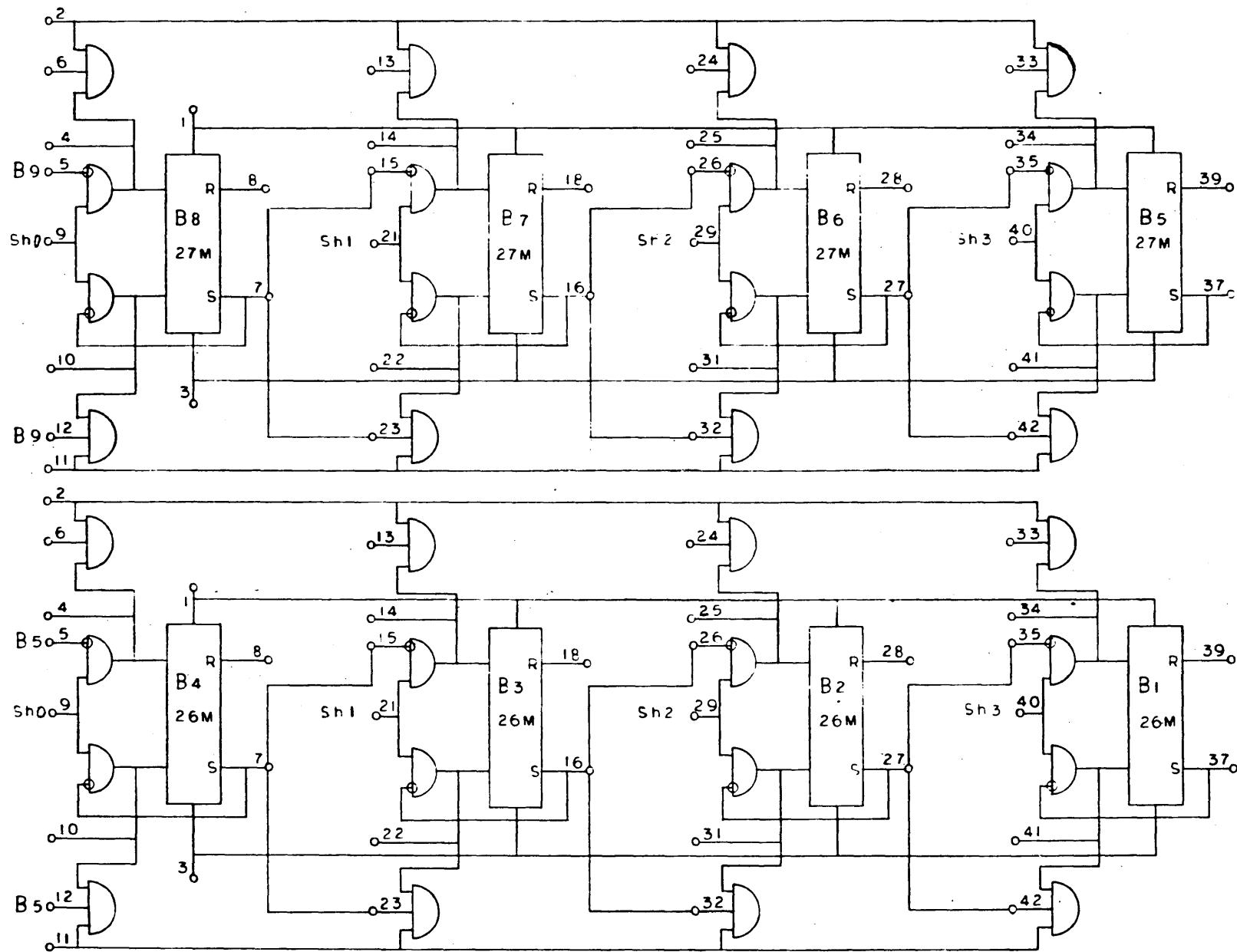
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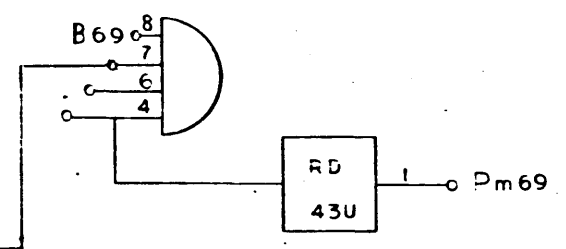
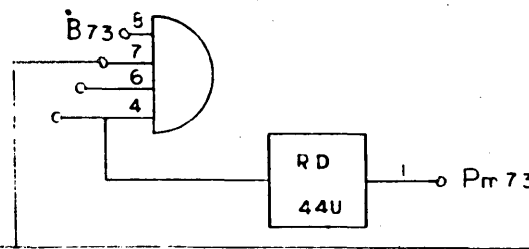
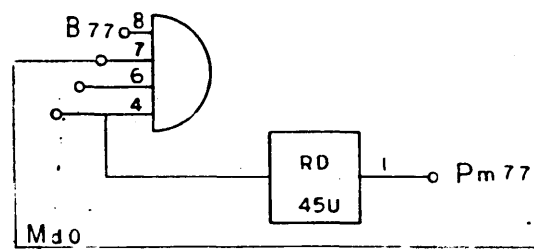
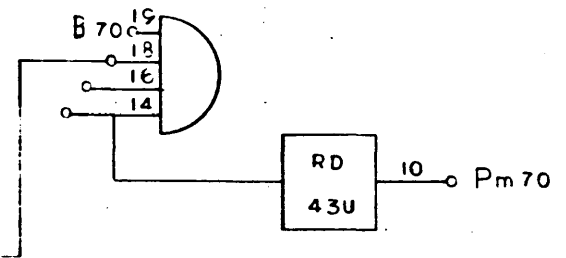
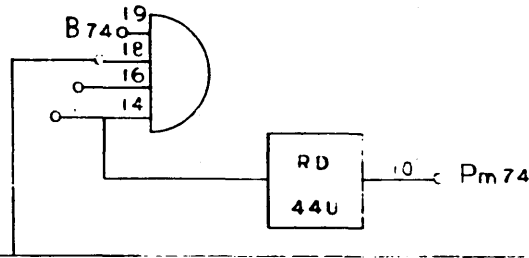
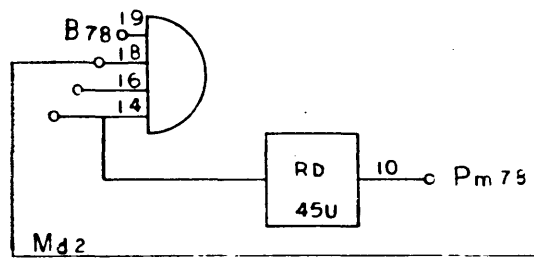
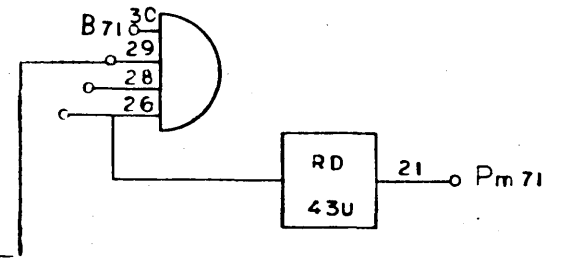
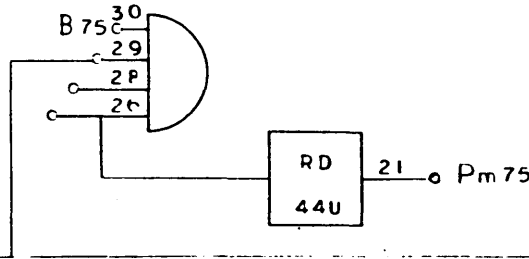
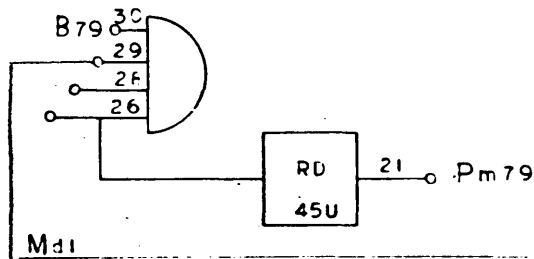
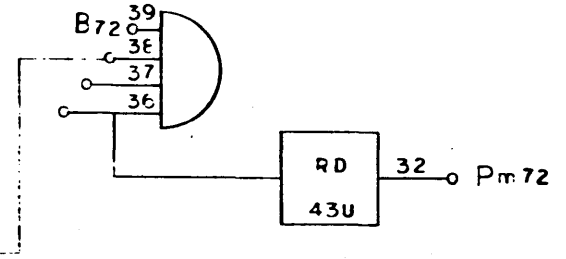
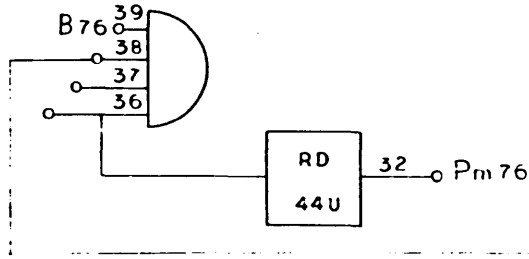
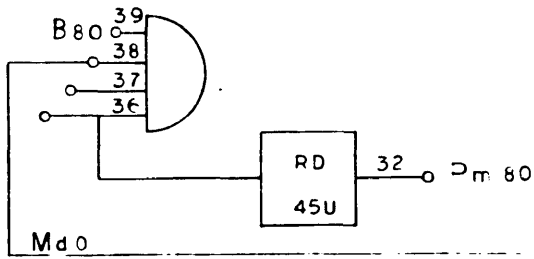
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5-27

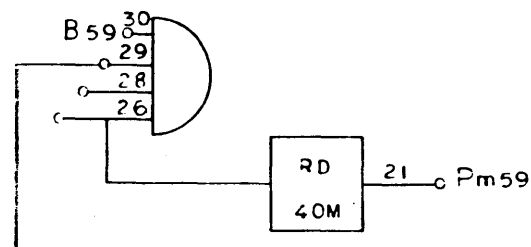
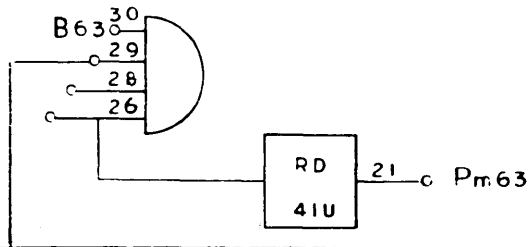
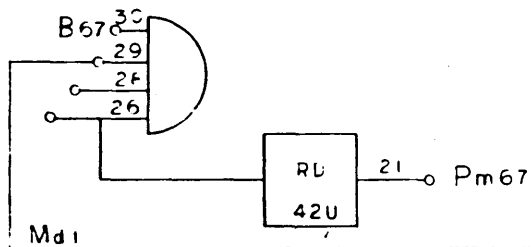
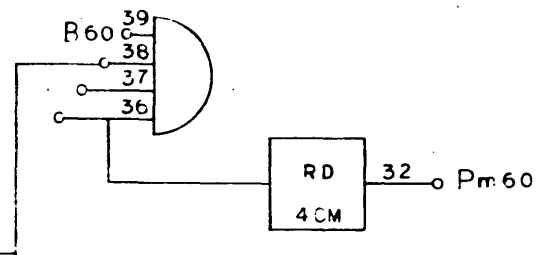
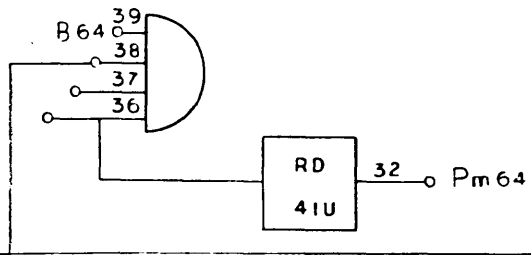
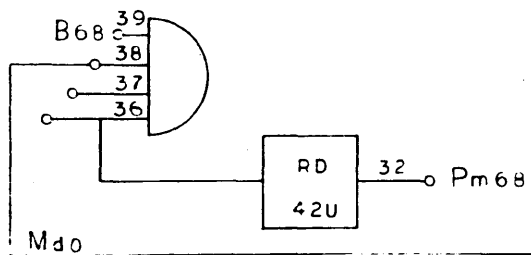




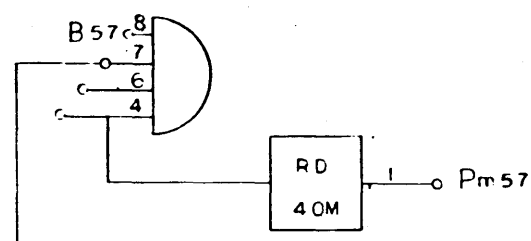
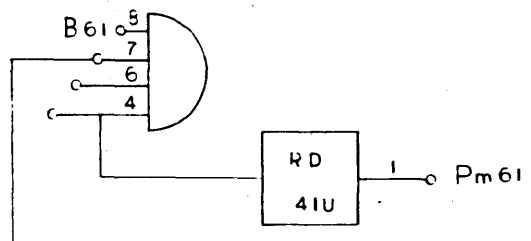
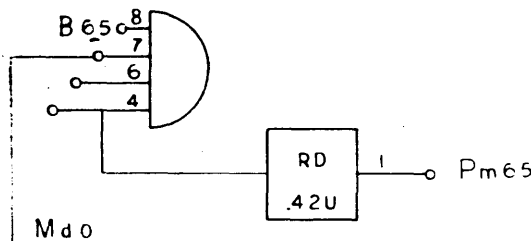
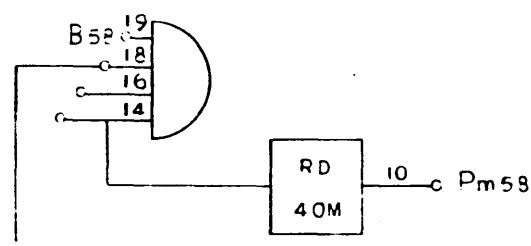
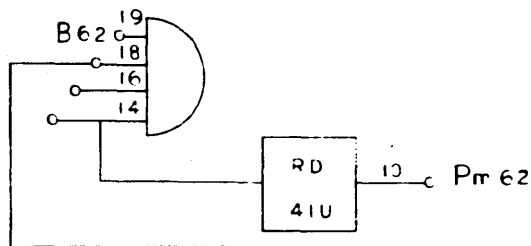
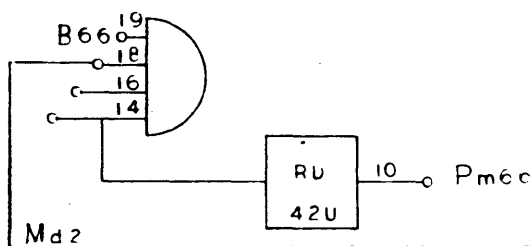
Common Return o—o Pin 40, 41, 24, of 45U, 44U, 43U.

Clamp Voltage o—o Pin 34, 22, 12, 2, of 45U, 44U, 43U.

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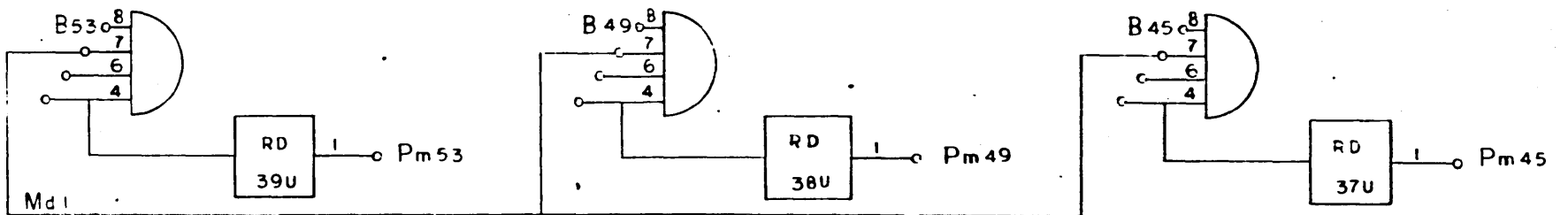
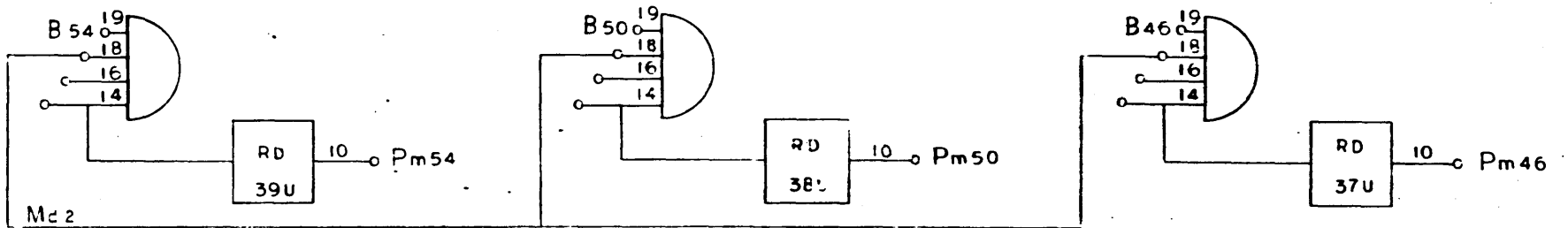
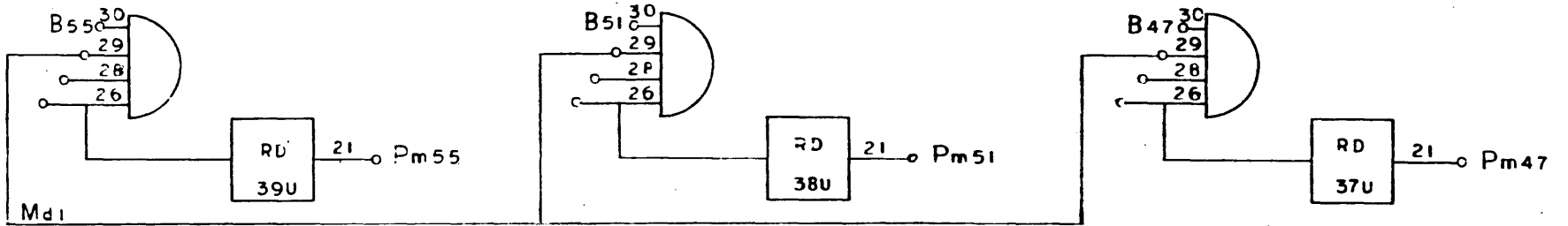
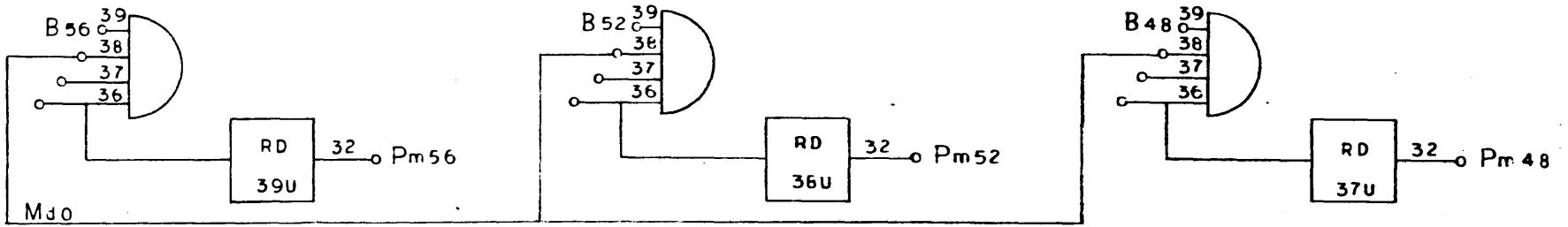


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Common Return  $\circ$   $\rightarrow$  Pin 40, 41, 24 of 42U, 41U, 45M.

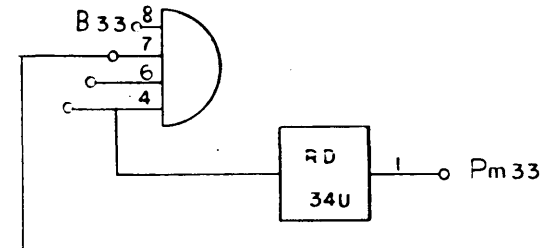
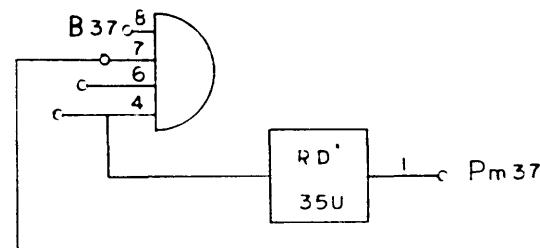
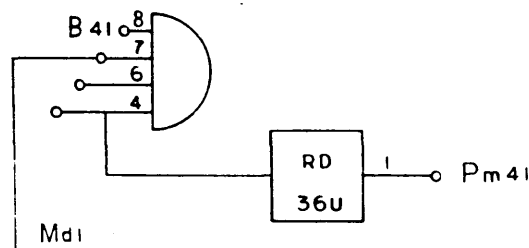
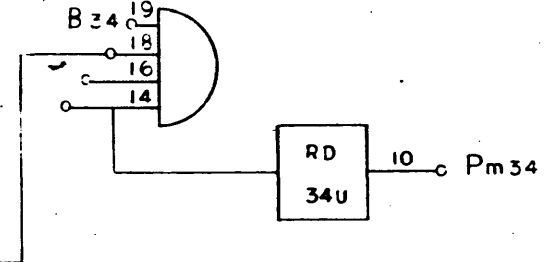
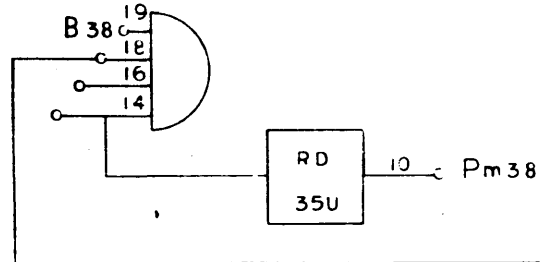
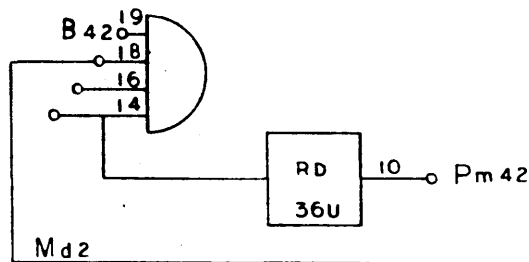
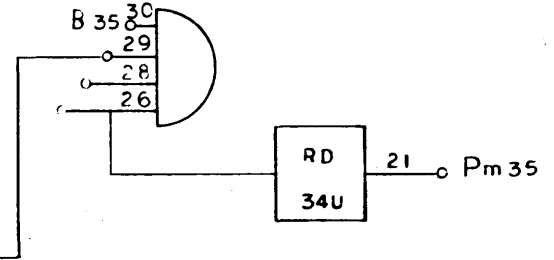
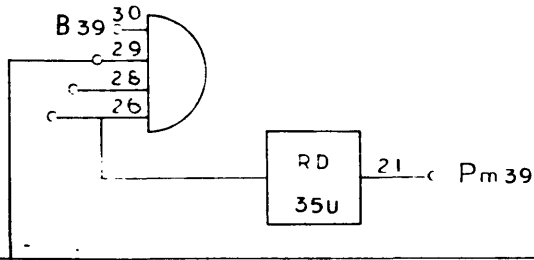
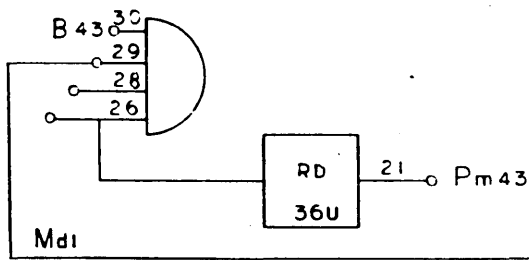
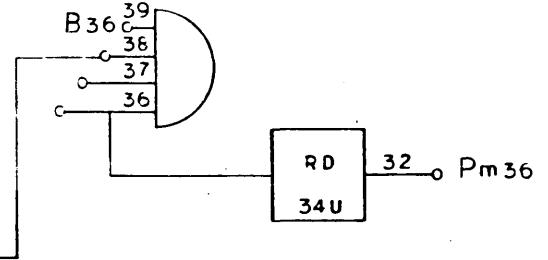
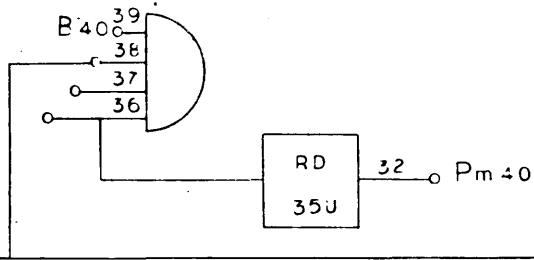
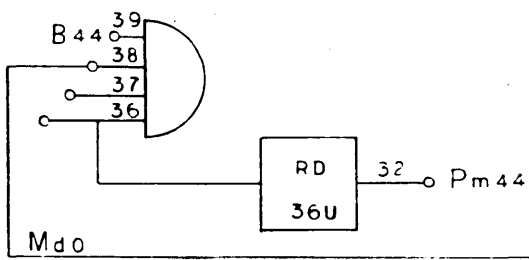
Clamp Voltage  $\circ$   $\rightarrow$  Pin 34, 22, 12, 2, of 42U, 41U, 40M.



Common Return ○ — ○ Pin 40, 41, 24, of 39U, 38U, 37U.

Clamp Voltage ○ — ○ Pin 34, 22, 12, 2, of 39U, 38U, 37U.

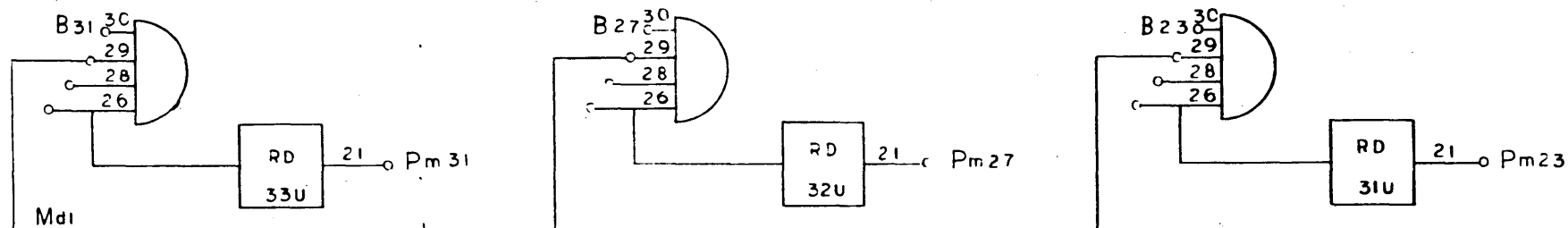
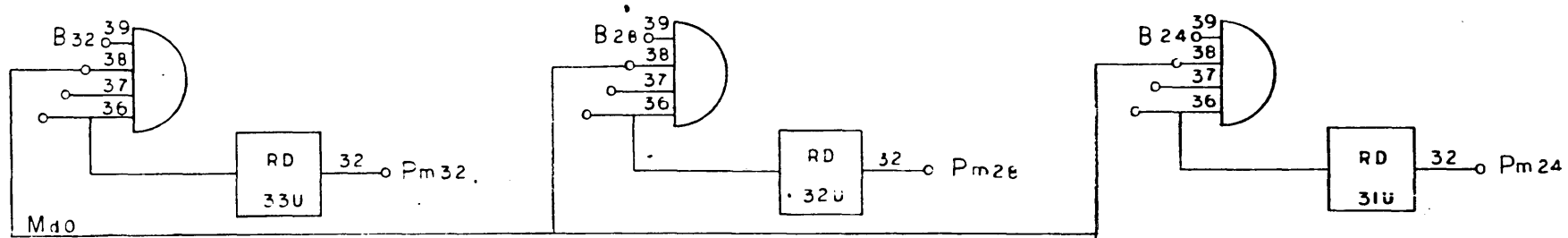
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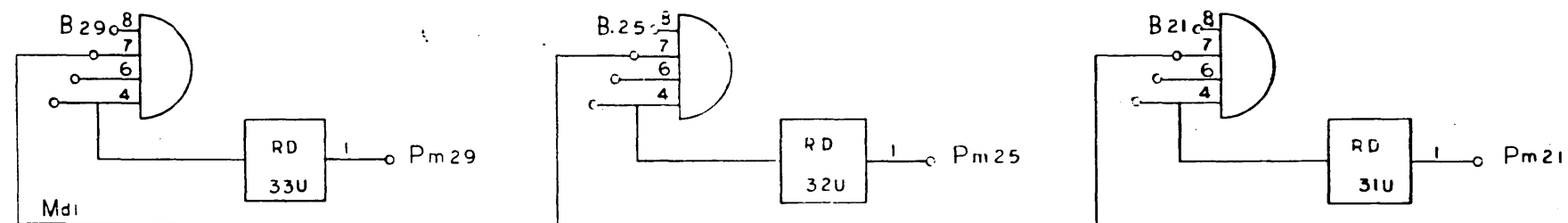
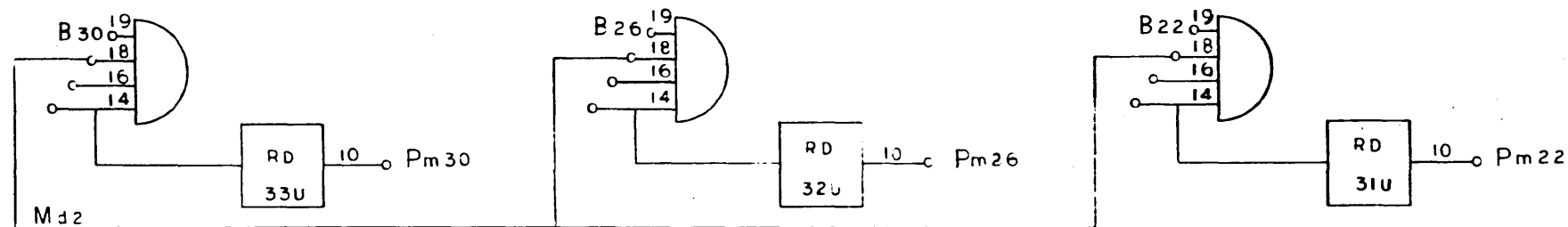
Common Return — Pin 40, 41, 24, of 36U, 35U, 34U.

Clamp Voltage — Pin 34, 22, 12, 2, of 36U, 35U, 34U.

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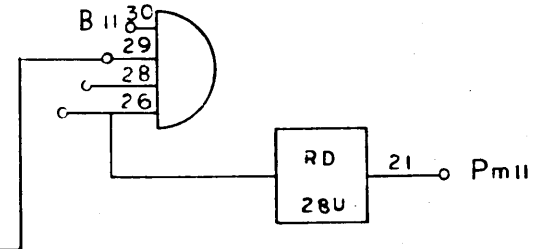
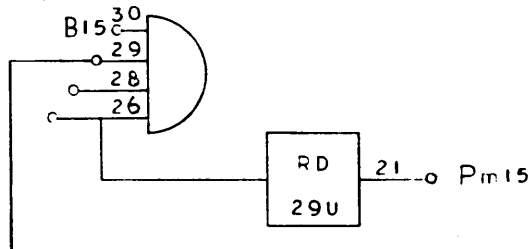
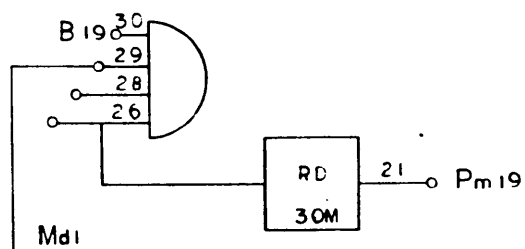
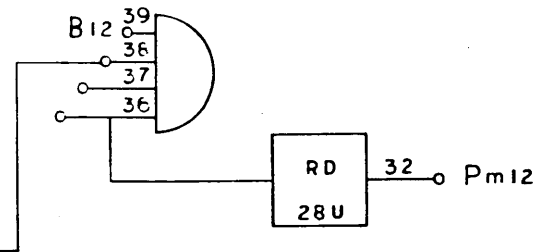
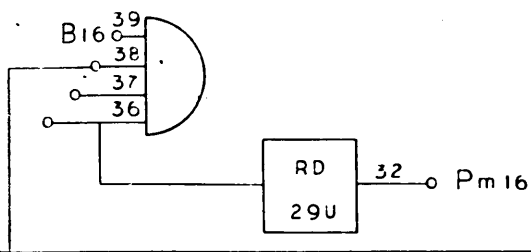
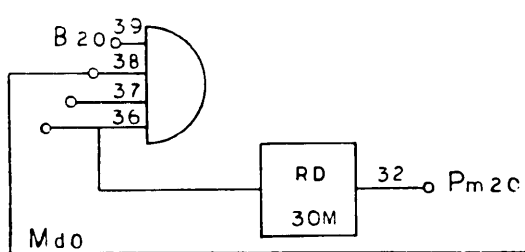


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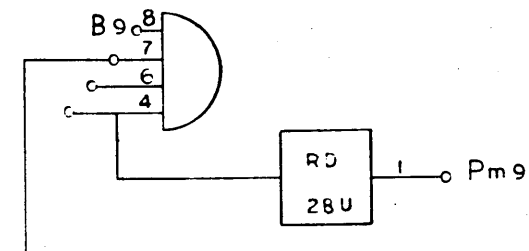
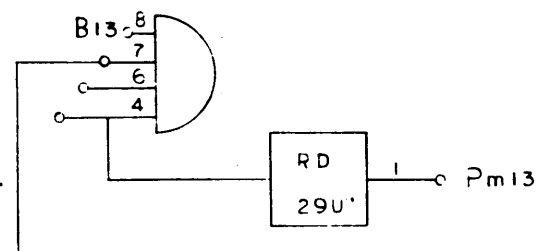
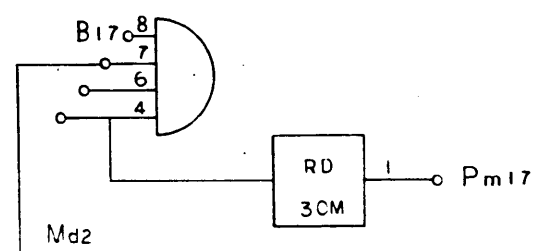
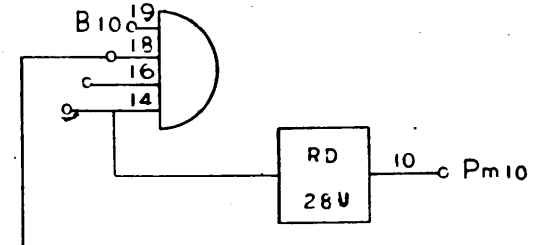
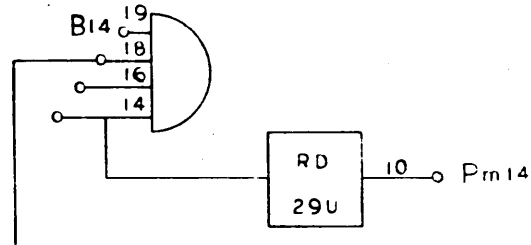
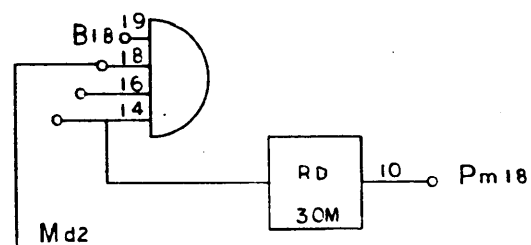


Common Return — Pin 40, 41, 24, of 33U, 32U, 31U.

Clamp Voltage — Pin 34, 22, 12, 2, of 33U, 32U, 31U.



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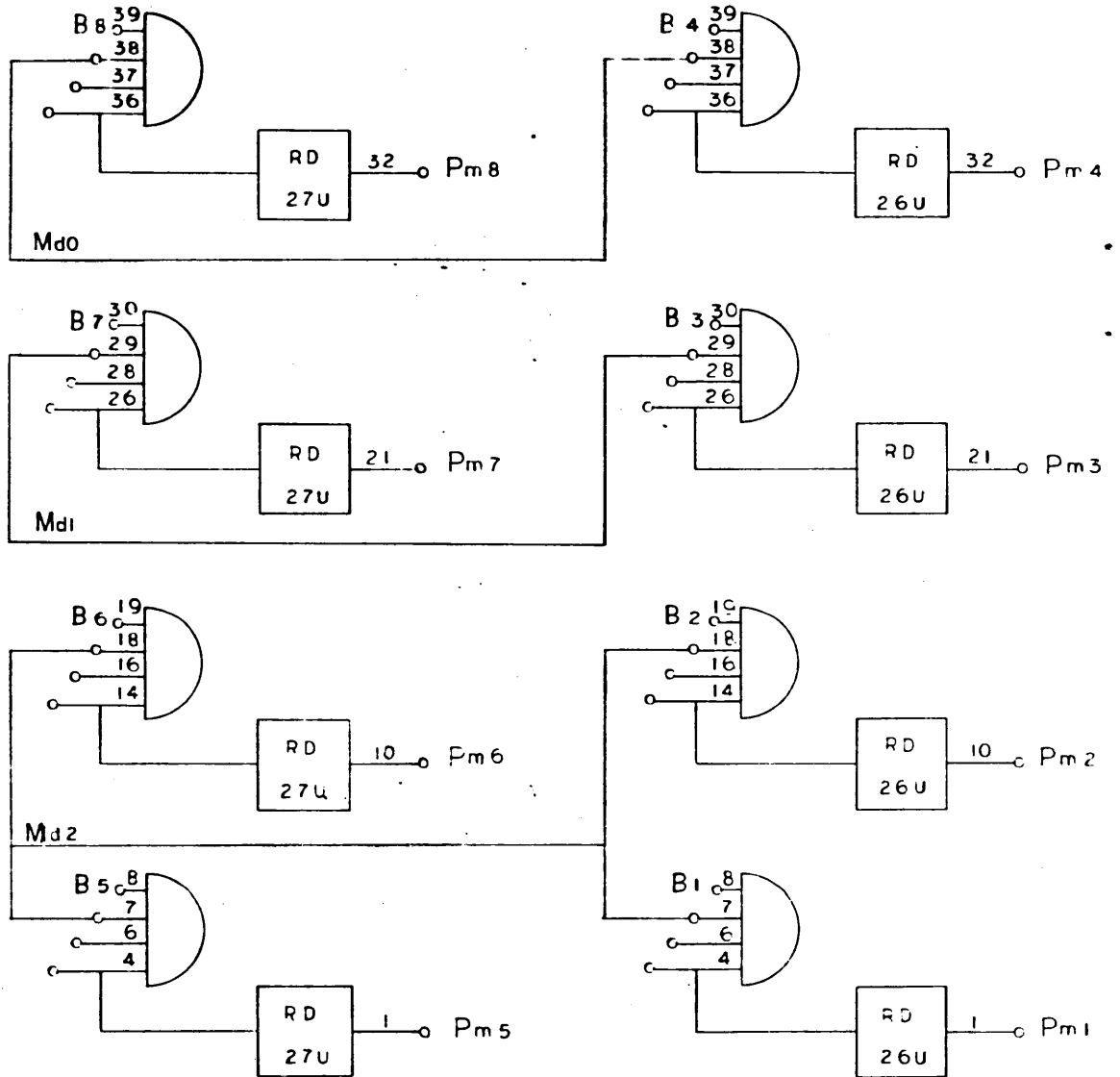


Common Return — Pin 40, 41, 24, of 30M, 29U, 28U.

Clamp Voltage — Pin 34, 22, 12, 2, of 30M, 29U, 28U.

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Common Return  $\circ$ — $\circ$  Pin 40, 41, 24 of 27U, 26U.

Clamp Voltage  $\circ$ — $\circ$  Pin 34, 22, 12, 2, of 27U, 26U.

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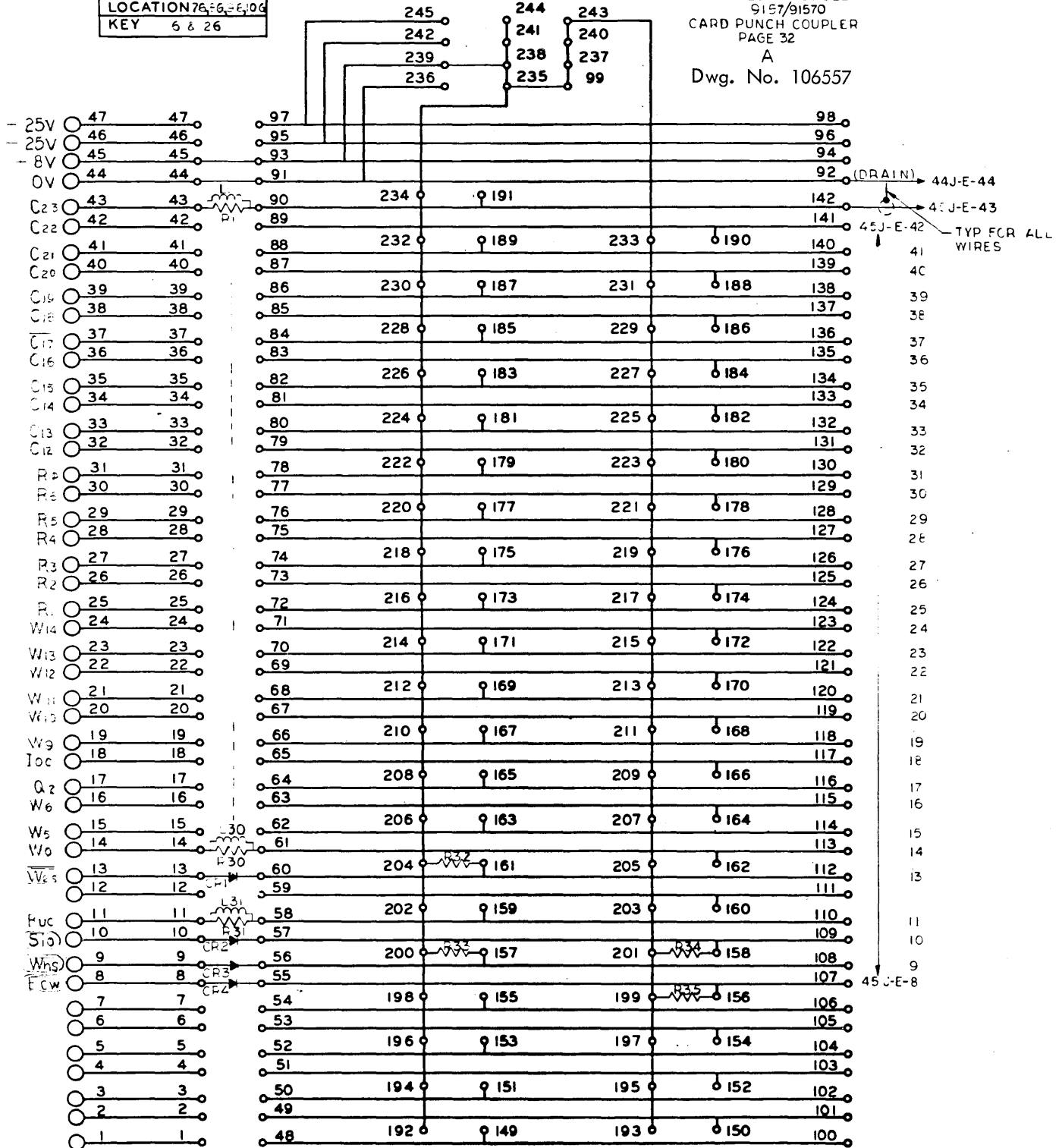
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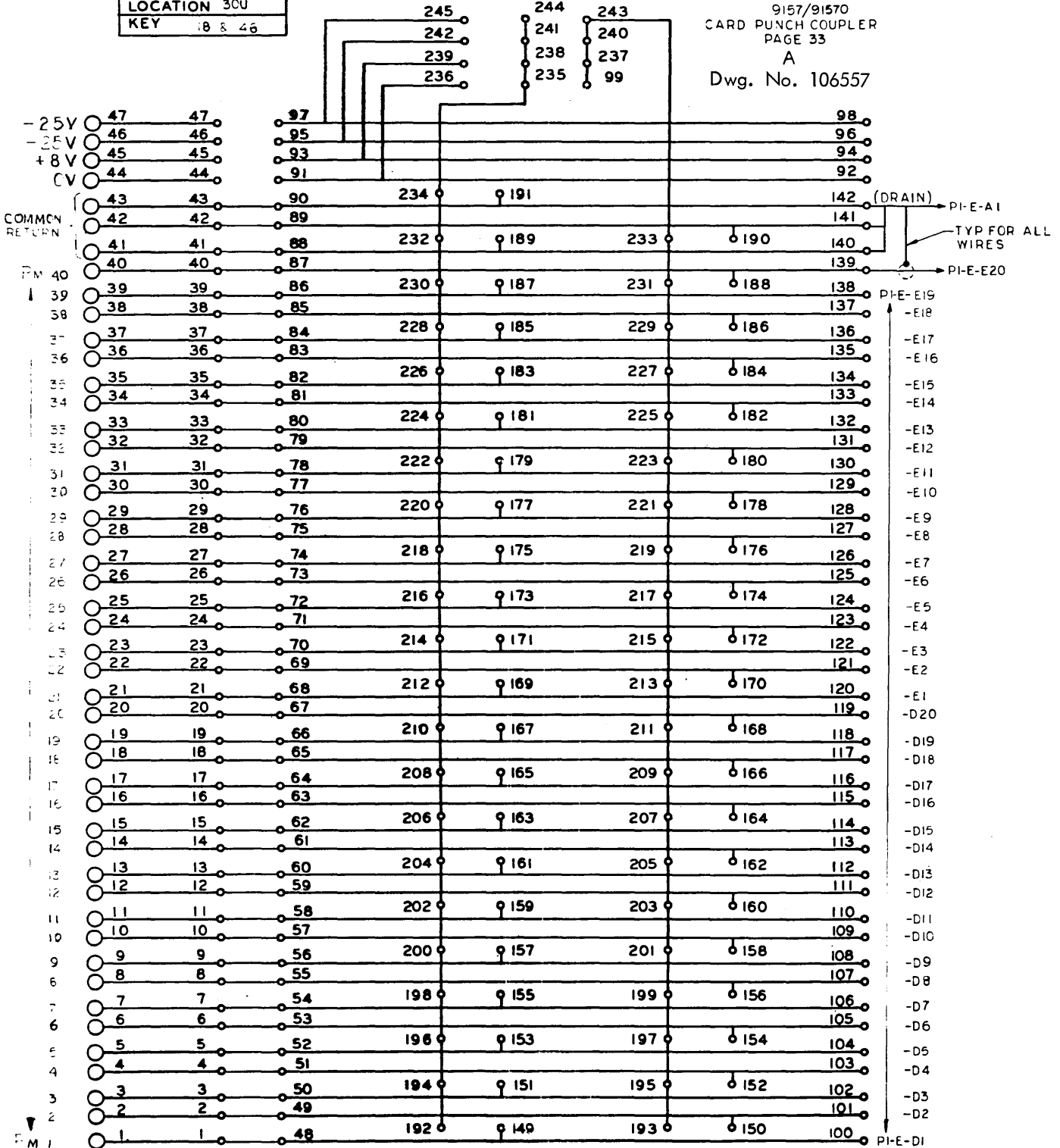
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LOCATION	76, 6, 6, 6, 0, 6
KEY	6 & 26

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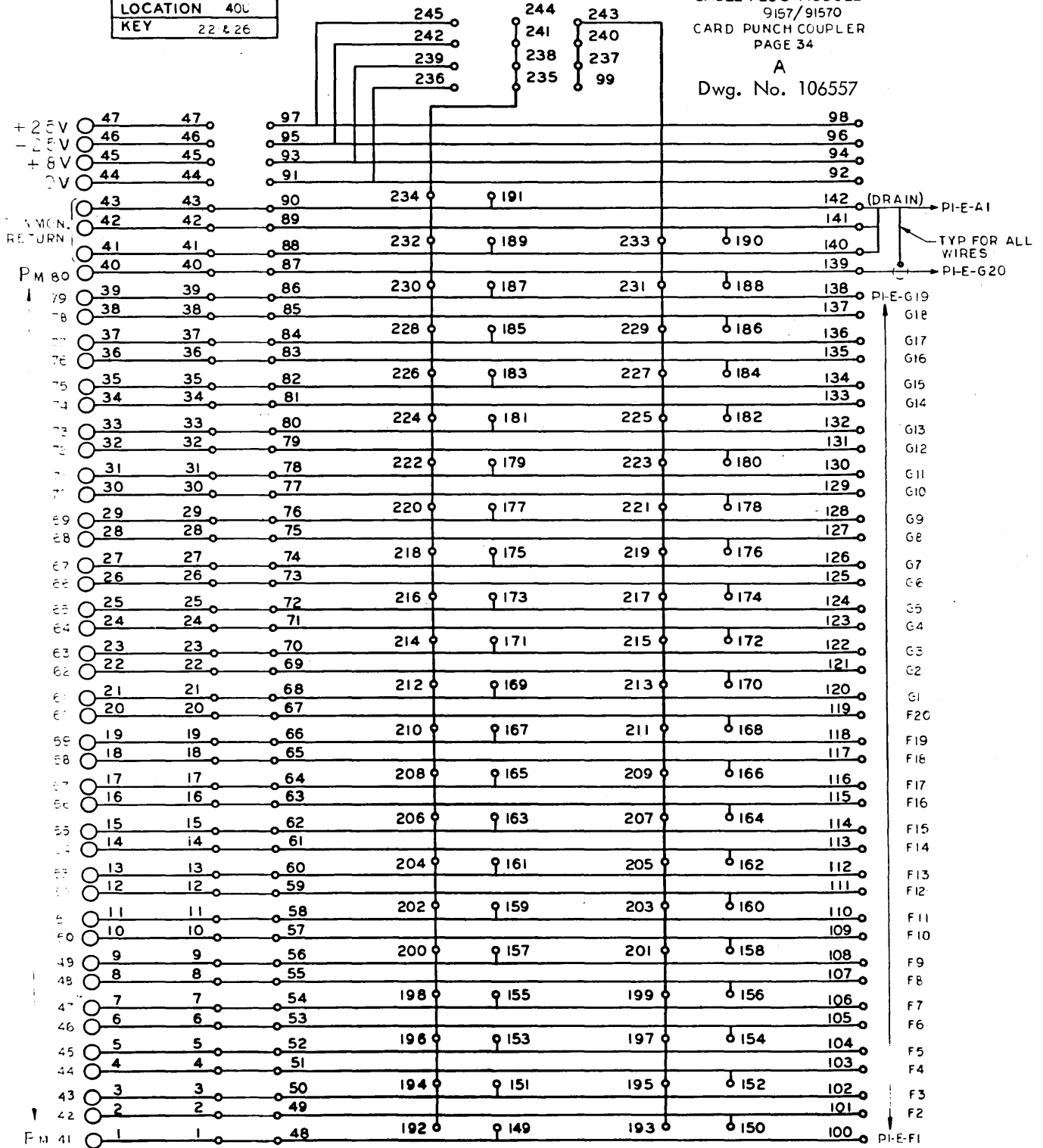
DESIGNATION	P51
LOCATION	30U
KEY	18 & 46

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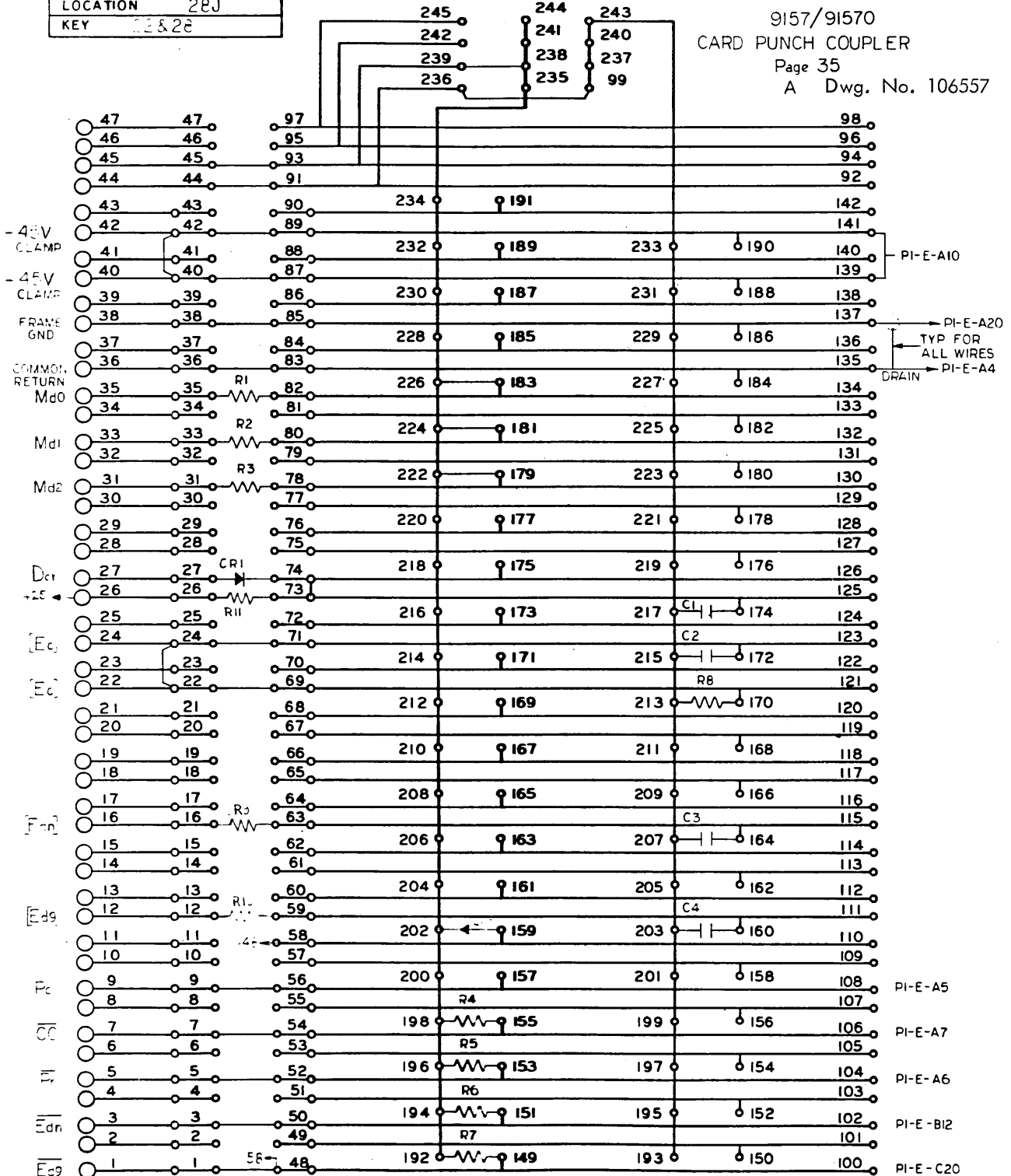
DESIGNATION	P52
LOCATION	40L
KEY	22 & 26

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DESIGNATION	P53
LOCATION	28J
KEY	22&2e

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LOC 26M		LOC 27M		LOC 28M		LOC 29M		LOC 30M		LOC 31M		LOC 32M		LOC 33M		LOC 34M		LOC 35M		LOC 36M		LOC 37M		LOC 38M			
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LOC 39M		LOC 40M		LOC 41M		LOC 42M		LOC 43M		LOC 44M		LOC 45M		LOC	LOC	LOC	LOC	LOC	LOC	LOC	LOC
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47		47		47		47		47		47		47		47		47		47	

RK53 P52 RK53 RK53 RK53 RK53 RK53



5-43

LOC 39J		LOC 40J		LOC 41J		LOC 42J		LOC 43J		LOC 44J		LOC 45J		LOC	LOC	LOC	LOC	LOC	LOC				
PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE		
1	10	1		1		1		1		1		1		1		1		1		1		1	
2		2		2		2	E	2	7,8	2	7,8	2		2		2		2		2		2	
3		3		3	7	3		3	7,8	3	7,8	3		3		3		3		3		3	
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47		47		47		47		47		47		47		47		47		47		47		47	

ROW  
J

IK51 FH15 GK51 GK51 FH17 FH17

9157/91570  
CARD PUNCH COUPLER

Page 40 Dwg. No. 106557

A

Loc 26J		Loc 27J		Loc 28J		Loc 29J		Loc 30J		Loc 31J		Loc 32J		Loc 33J		Loc 34J		Loc 35J		Loc 36J		Loc 37J		Loc 38J			
PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE
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47		47		47		47		47		47		47		47		47		47		47		47		47			

ROW  
J

5-44

RK53 OX13 P53 IC12 FHI5 IK5I IK5I GK52 GK5I OX13 IHI GK5I BH10

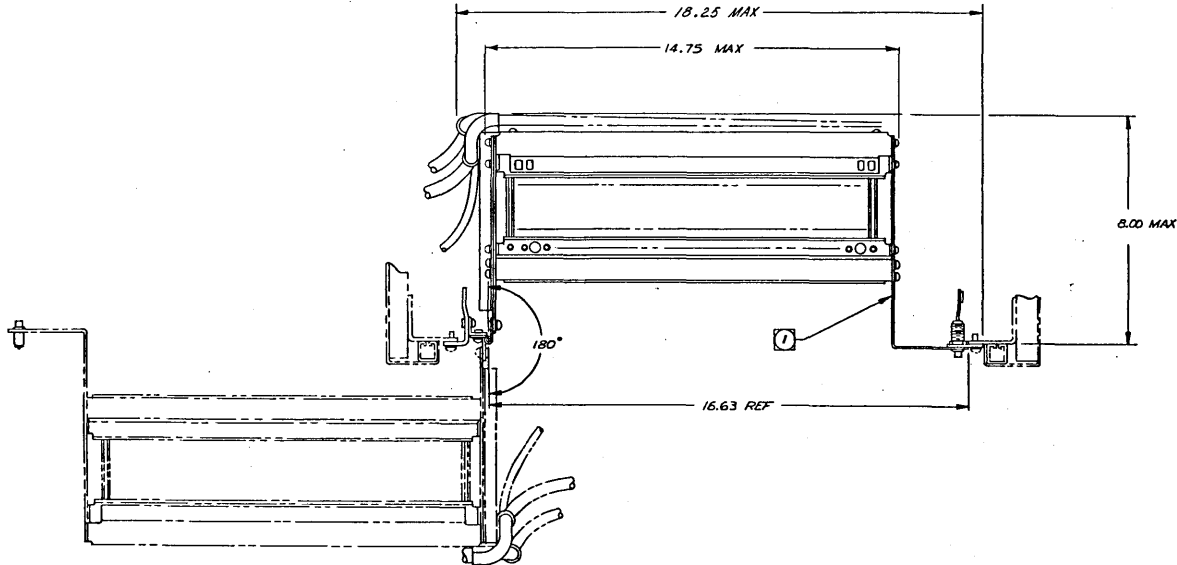
SECTION 5-3. ENGINEERING DRAWINGS AND MODULE LOCATION CHARTS

REV		DESCRIPTION		REVISIONS		106538		A	
NO.	DATE	BY	APPROVED	CHK	DATE	APP	DATE	CHK	DATE
A									

5. MODIFICATIONS TO IBM 523 SUMMARY PUNCH (REF SDS SPEC. 103240)
- REVERSE POWER SUPPLY POLARITY AS INDICATED IN SDS MANUAL 900055.
  - OPEN-CIRCUIT THE COIL OF THE HD2 RELAY (DISCONNECT THE WIRE TO THE COIL AT THE RELAY, TIE BACK, & LABEL).
  - REVERSE POLARITY OF THE RECTIFIER IN NO.1 RELAY CIRCUIT (INTERCHANGE WIRE CONNECTED TO THE ANODE WITH THE WIRE TO THE CATHODE).
  - SET CAM PT TO MAKE AT 9.5 TIME & BREAK AT 13.0 TIME.
  - IF IC1 IS SUPPLIED, DISCONNECT COIL (TIE BACK & LABEL)

NOTES: UNLESS OTHERWISE SPECIFIED

- MATERIAL: CHASSIS - STEEL, CAD PLATED, CLEAR CHROMATE DIPPED.  
HARDWARE - STEEL, CAD PLATED.
- INSTALL IN LOCATION J (38 P) OF ASSOCIATED 951/91510 CARD PDR COUPLER OR AUX. INPUT/OUTPUT CONNECTOR OF ASSOCIATED COMPUTER. CABLE IS 6 FT LONG.
- POWER CABLE ENDS ARE TAGGED AS TO DESTINATION IN ASSOCIATED COMPUTER.
- CHASSIS LETTER DESIGNATIONS ARE U, M, & J.

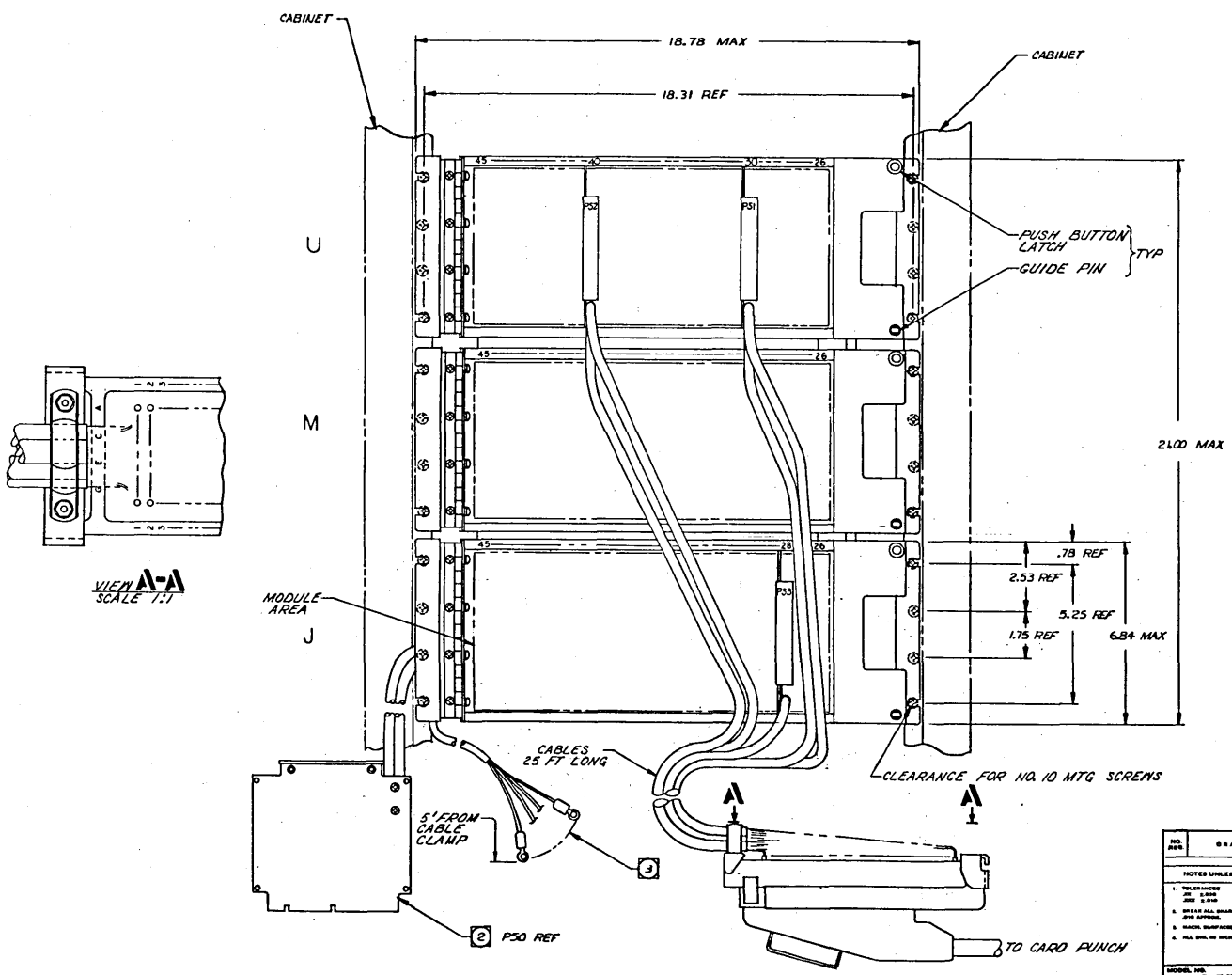


NO. REV	DRAWING NO.	DESCRIPTION	REFERENCE DESIGNATION	ITEM NO.
MATERIAL LIST				
NOTED UNLESS SPECIFIED		DRAWN <i>BRILMAN</i> 2-28-64	<b>SDS</b> SCIENTIFIC DATA SYSTEMS 1115 FIFTEENTH STREET SANTA MONICA CALIFORNIA	
1. DIMENSIONS AS SHOWN	APPROVED BY	CHECK <i>3/1/64</i> 3/5/64	TITLE <b>INSTALLATION DWG, CARD PUNCH COUPLER</b>	
2. HOLE ALL SURFACE	DATE	APPR. <i>J. Brant</i> 3/1/64		
3. BACK SURFACE				
4. ALL DIM. TO CENTER				
MODEL NO.	9157/91570	SIZE	DWG NO.	A
TEXT ASSY.		D	106538	
SCALE 1:2		DO NOT SCALE DRAWING		SHEET 1 OF 2

106538 | A

REV.		DESCRIPTION	CHK	DATE	APPROVED
		SEE SHEET ONE			

1-6538 A



VIEW A-A  
SCALE 1:1

DWG. NO.	DRAWING NO.	DESCRIPTION	REFERENCE DESIGNATION	ITEM NO.
		MATERIAL LIST		
NOTES UNLESS SPECIFIED		DRAWN: BRILMAN 2-26-64	SDS SCIENTIFIC DATA SYSTEMS	
1. TOLERANCES UNLESS SPECIFIED		CHECK: P. J. BROWN 6/5/64	1545 FIFTEENTH STREET SANTA MONICA CALIFORNIA	
2. DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED		APPR: J. BROWN 6/9/64	TITLE	
3. BREAK ALL SHARP CORNERS AND EDGES			INSTALLATION DWG.,	
4. HATCH SURFACES			CARD PUNCH COUPLER	
5. ALL DIM. IN INCHES				
MODEL NO.	9157/31570	REV.	DWG. NO.	A
NEXT ASSY.		D	106538	
SCALE			DO NOT SCALE DRAWING SHEET 2 OF 2	

106538 | A

SDS  
 CARD PUNCH  
 COUPLER  
 MODEL NO 9157  
 SER NO.

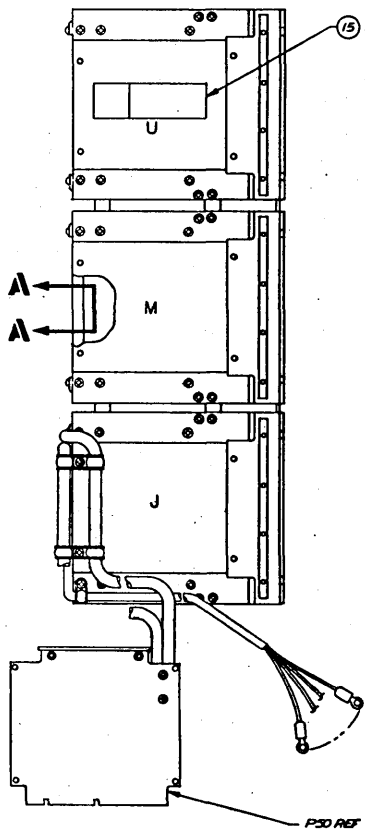
DETAIL **B**  
 SCALE 1/1

**B**

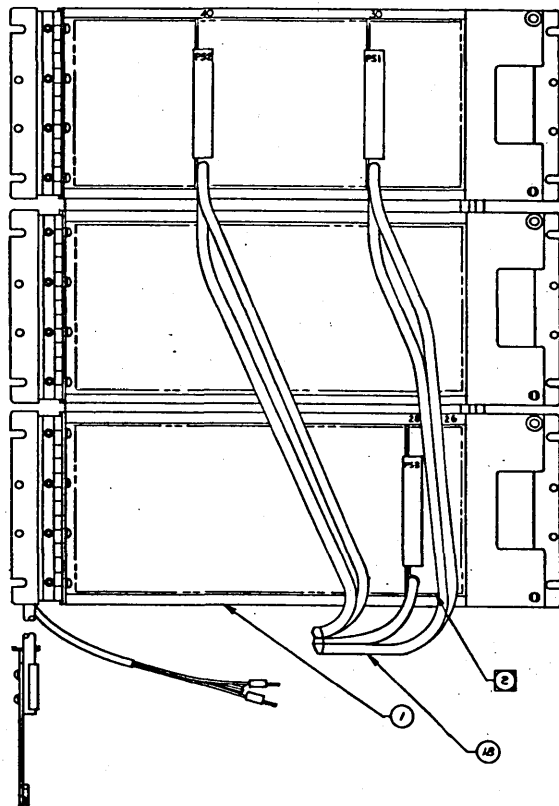
NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE MATERIAL LIST 104758 SHEET 2.
2. FOR LOCATION OF MODULES & POLARIZING PLUS (ITEM 13) SEE 106545
3. MARK TITLE, MODEL NO. & SERIAL NO. JE HIGH AS SHOWN; COLOR-BLACK.
4. REF LOGIC DIAGRAM NO. 106557
5. REF INSTALLATION DWG NO. 106538

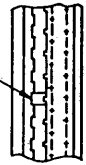
REVISIONS				104758	A
REV.	DESCRIPTION	CHK.	DATE	APPROVED	
A	RELEASED TO MFG		7/1/68		



**B** SEE DETAIL **B**



**B** 120 RES



SECTION **A-A**  
 SCALE 1/1

DWG. NO.	DRAWING NO.	DESCRIPTION	REFERENCE DESIGNATION	DATE
		MATERIAL LIST		
NOTES UNLESS SPECIFIED		DRAWN: BRILMAN 2-29-68	SDS OPERATING DATA SYSTEMS	
1. UNLESS OTHERWISE SPECIFIED	CHECK: [Signature]	DATE: 3-13-68	242 LUTHERAN STREET SANTA MONICA, CALIFORNIA	
2. DIMENSIONS UNLESS OTHERWISE SPECIFIED	APPR: [Signature]		TITLE: ASSEMBLY, CARD PUNCH COUPLER	
3. DIMENSIONS UNLESS OTHERWISE SPECIFIED			REV. NO. D	104758 A
4. DIMENSIONS UNLESS OTHERWISE SPECIFIED				
5. DIMENSIONS UNLESS OTHERWISE SPECIFIED				
MODEL NO. 9157				
SHEET NO.			SCALE 1/1	NO NOT SCALE DRAWING
				SHEET 1 OF 2


REV	A	MATERIAL LIST			ML	DWG. NO.	REV						
DWG. NO.		ASSY. CARD PUNCH COUPLER				MOD #	104758	A					
ML		104758			SDS SCIENTIFIC DATA SYSTEMS			9157			DATE 2/27 SHEET 2 OF 2		
ITEM	DWG. TITLE	DWG. NO.	NO. REQ.	REMARKS OR CRT. DESIG.									
1	Assy, Coupler Chassis	106543	1										
2													
3	Assy, P. W. And Or Buffer	100164	1	BH10 see DL100402									
4	Assy, P. W. Universal F.F.	101534	2	FH17	101535								
5	Assy, P. W. Diode Gate 1	100246	4	GK51	100424								
6	Assy, P. W. Diode Gate 2	100267	1	GK52	100425								
7	Assy, P. W. Or Gate Inverter	100319	1	IH11	100321								
8	Assy, P. W. And Inverter	101540	1	IC12	101541								
9	Assy, P. W. Inverter Ampl.	100388	3	IK51	100434								
10	Assy, P. W. <sup>One-Shot</sup> Multivibrator	103932	2	OX13	103933								
11	Assy, P. W. Relay Driver	100905	21	RK53	100906								
12	Assy, P. W. Counter F.F.	101026	20	FH15 see DL 101027									
13	Pin, Polarizing	100282	120										
14	Chart, Module Location	106545	x	ref									
15	Nameplate, Blank	101109	1										
16	Diagram, Logic	106557	x	ref									
17	Installation Dwg	106538	x	ref									
18	Assy, Cable Plug Mod.	106540	1										

REVISIONS				
REV.	DESCRIPTION	CHK	DATE	APPROVED
A	Released to Mfg	<i>CD</i>	3/19/64	<i>[Signature]</i>

106545 A

NO. REQ.	DRAWING NO.	DESCRIPTION	REFERENCE DESIGNATION	ITEM NO.
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MATERIAL LIST

NOTES UNLESS SPECIFIED  1. TOLERANCES .XX ±.030      ANGULAR ±½° .XXX ±.010  2. BREAK ALL SHARP EDGES .010 APPROX.  3. MACH. SURFACES <b>J</b>  4. ALL DIM. IN INCHES	DRAWN <i>D. TELL</i> 2/28/64	 <p>SDS SCIENTIFIC DATA SYSTEMS SANTA MONICA, CALIFORNIA</p>	TITLE  CHART, MODULE LOCATION, CARD PUNCH COUPLER
	CHECK <i>[Signature]</i> 3-12-64		
	APPR. <i>[Signature]</i> 3/25/64		
MODEL NO.  9157	SIZE  <b>A</b>	DWG. NO.  106545	CHANGE LETTER  A
NEXT ASSY.  104758	SCALE	DO NOT SCALE DRAWING	SHEET 1 of 4



**CONNECTOR LOCATION**

	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Type																									
Key Loc.																									

**CONNECTOR LOCATION**

	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26
Type	RK 53	RK 53	RK 53	RK 53	RK 53	P 52	RK 53	RK 53	RK 53	RK 53	RK 53	RK 53	RK 53	RK 53	RK 53	P 51	RK 53	RK 53	RK 53	RK 53
Key Loc.	8 22	8 22	8 22	8 22	8 22	22 26	8 22	8 22	8 22	8 22	8 22	8 22	8 22	8 22	8 22	18 46	8 22	8 22	8 22	8 22

**LET.**

<b>CHASSIS</b>	<b>U</b>
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Note Location 1 - 25 on Fixed Chassis  
 26 - 45 on Swing out Chassis

<b>TITLE</b>	<b>CHART, MODULE LOCATION CARD PUNCH COUPLER</b>		<b>SCIENTIFIC DATA SYSTEM</b>	
			106545	A
			SHEET 2	OF 4

**SECTION 5-4. MODULE DATA SHEETS AND SUPPLIERS CODE INDEX**

# AND:OR Buffer Amplifier

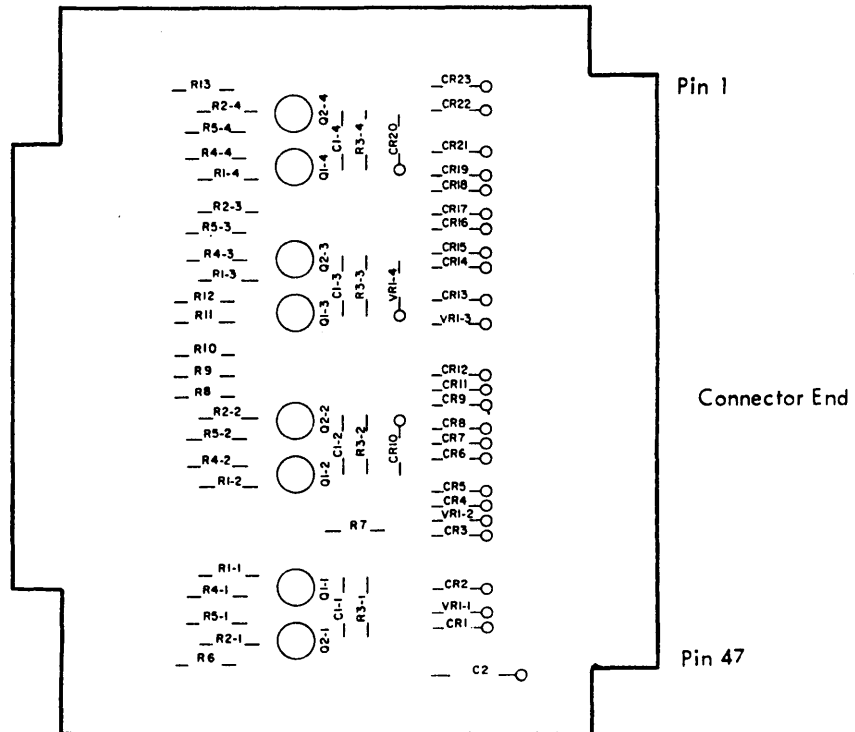
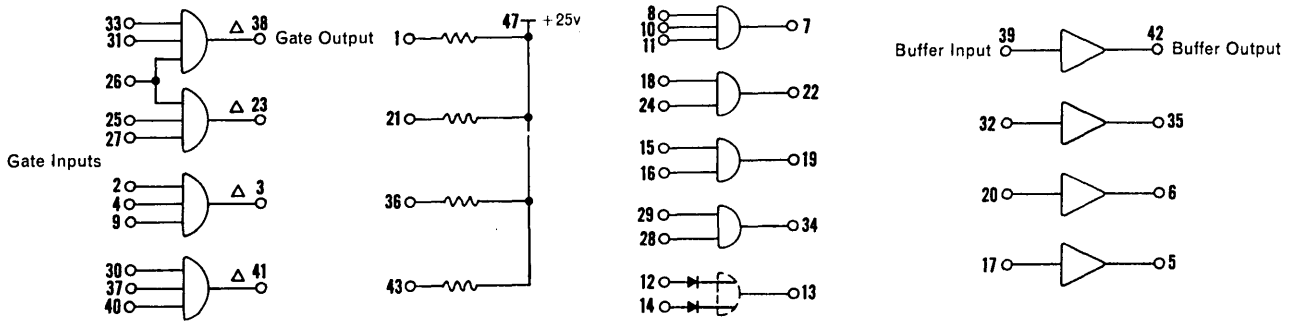
BH10

Assy. No. 100164

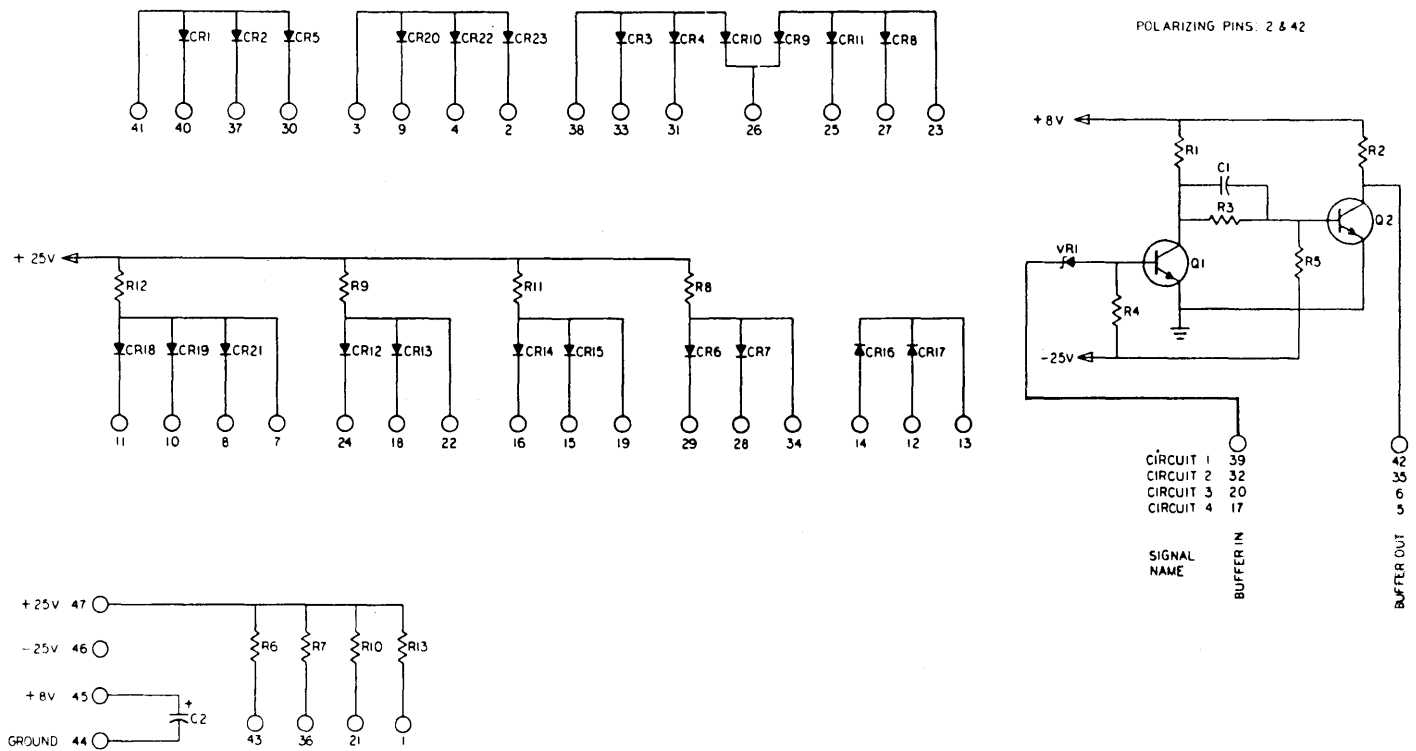
This module contains four complete diode AND gates, four diode  $\Delta$  AND gates which can be used for expansion gates, or as independent gates by adding one of the gate resistors, one gated input OR gate, plus four buffer amplifiers. AND:OR gates can be constructed by wiring one input pin of an AND gate to one input pin of another to form an OR gate output. The buffer circuits may be used to amplify AND:OR and AND gate outputs when implementing cascaded logic, or where a large fan-out is needed.

**Maximum Operating Frequency**

Fan-In	1 Mc
Gate Input	10 terms
Output	2 loads
Output Delay	20 loads
+25 Volt Supply	100 ns
+ 8 Volt Supply	49 ma
-25 Volt Supply	63 ma
Module Dissipation	15 ma
	2.2 watts



# Model BH10 Schematic



## Model BH10 Parts List

Item	Description	Designator	Qty.	Supplier Code (See Index)
1	Transistor	2N834	Q1,2	1,5,7,9,5
2	Diode	1N746	VR1	2,12,13,14
3	Diode	1N914A	CR1 through CR23	4,12,13,14
4	Capacitor, Mica	68pf ± 5%	C1	19,20,21
5	Capacitor, Tantalum	4.7µf ± 20%, 50v	C2	23,77
6	Resistor	560 ohms ± 2%	R1,3	16,17
7	Resistor	820 ohms ± 2%	R2	16,17
8	Resistor	3.9 k ohms ± 2%	R6 through R13	16,17
9	Resistor	10 k ohms ± 2%	R4	16,17
10	Resistor	18 k ohms ± 2%	R5	16,17

NOTE: Unless otherwise noted, 1/2-watt resistors may be used. To maintain specified performance, use replacement types designated in SDS Suppliers Code Index.

# Universal Flip-Flop

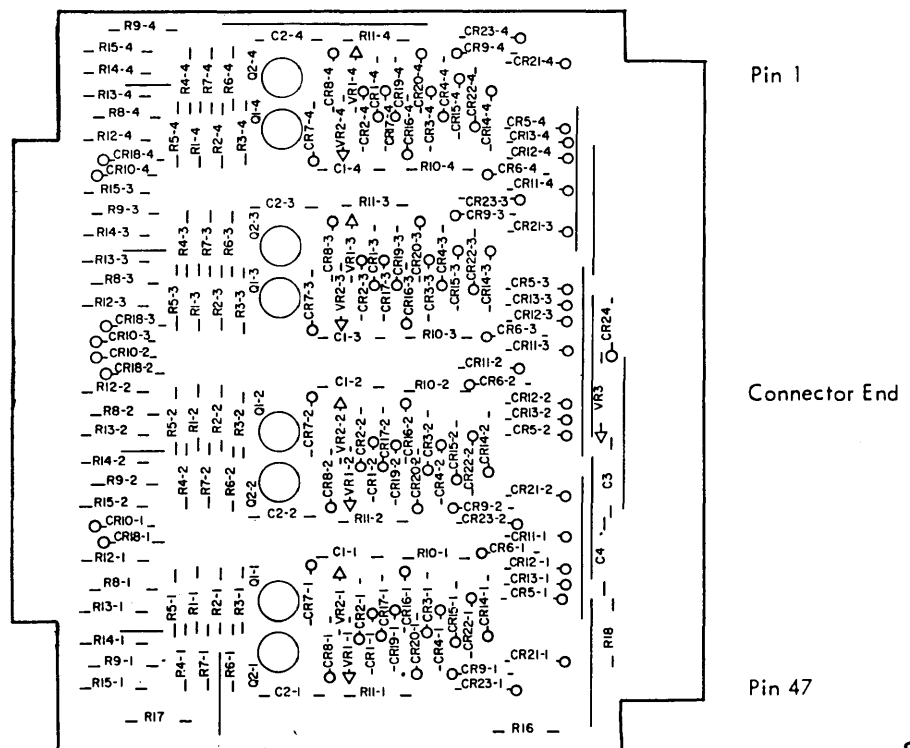
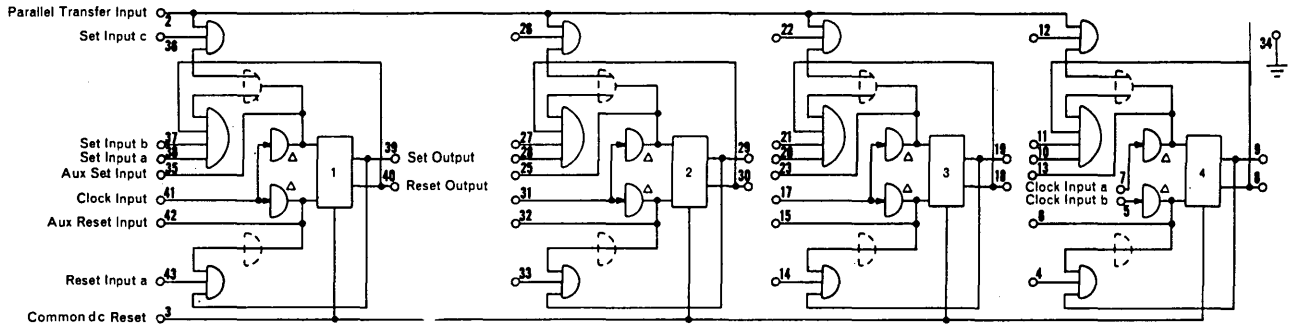
Assy. No. 101534

FH17

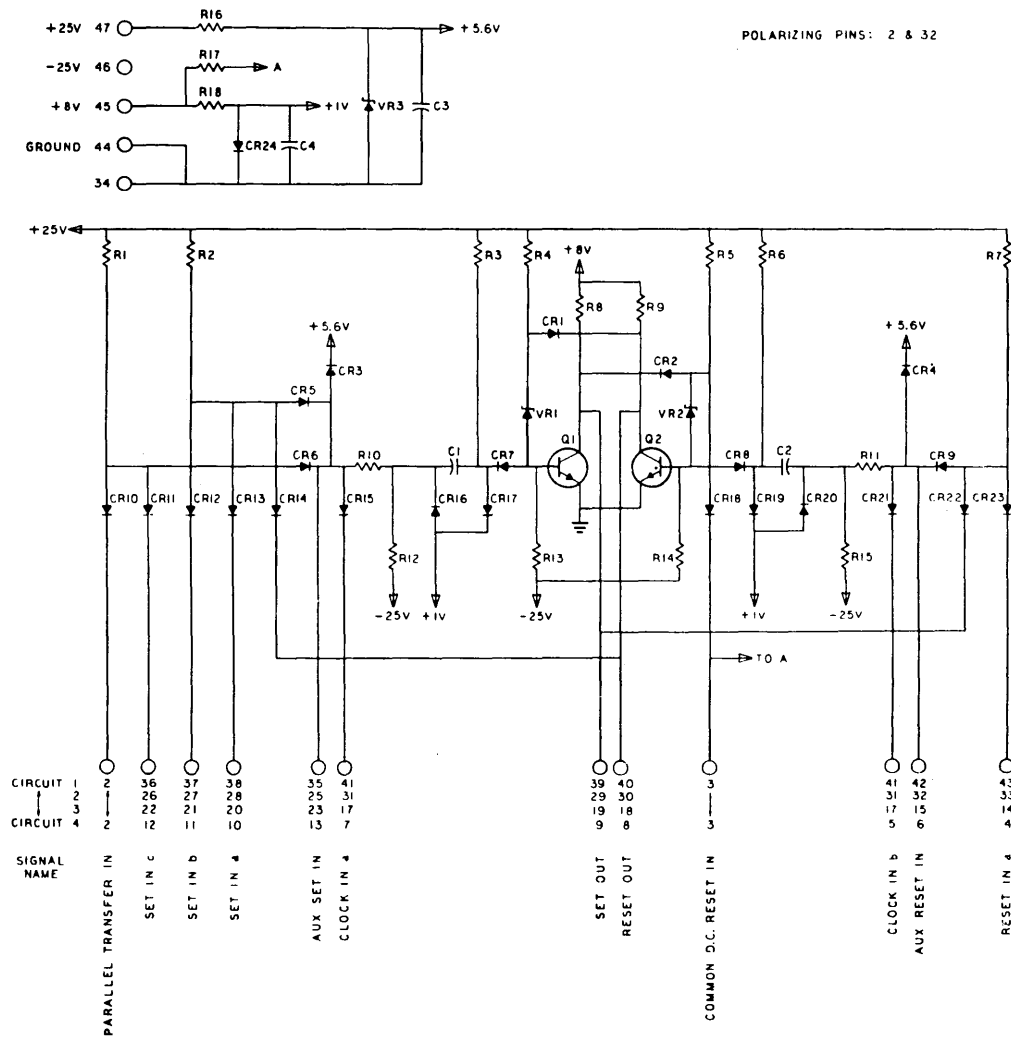
This module contains four independent flip-flop circuits with input gating that permits a wide range of applications. For a binary counter, the Set Output of each flip-flop is connected to the Clock Input of the next, causing it to toggle. A decade counter (8, 4, 2, 1) is similar, but requires a connection from Reset Output 4 to Set Input 2a, and instead of Set Output 3, Set Output 1 drives Clock Input 4b. The Parallel Transfer Input allows presetting of the flip-flops, and is connected to ground if not used. Clock termination circuits are wired on the module, as are the comprehensive noise level control circuits.

True signals have no effect on the dc inputs which respond only when false (0-volt) signals are applied.

Maximum Operating Frequency	1 Mc
Fan-In (Each aux. input)	10 terms
Set, Reset Inputs	2 loads
Clock Input	3 loads
Common dc Reset Input	6 loads
Parallel Transfer Input	8 loads
Set Output	10 loads
Reset Output	10 loads
Output Delay (Typical)	100 ns
+25 Volt Supply	140 ma
+ 8 Volt Supply	54 ma
-25 Volt Supply	3 ma
Module Dissipation	4.1 watts



# Model FH17 Schematic



## Model FH17 Parts List

Item	Description	Designator	Qty.	Supplier Code (See Index)
1	Transistor	2N834	Q1,2	8 1,5,7,95
2	Diode	1N914A	CR1 through CR24	93 4,12,13,14
3	Diode	1N746	VR1,2	8 2,12,13,14
4	Diode	1N3827 1N1765	VR3	1 2 6
5	Capacitor, Mica	330pf ± 5%	C1,2	8 19,20,21
6	Capacitor, Mylar	0.01µf ± 10%	C3,4	2 74,27,26
7	Resistor	120 ohms ± 2%	R10,11	8 16,17
8	Resistor	470 ohms ± 2%	R8,9,18	9 16,17
9	Resistor	3.9 k ohms ± 2%	R1,2,7	12 16,17
10	Resistor	4.7 k ohms ± 2%	R16	1 16,17
11	Resistor	47 k ohms ± 2%	R17	1 16,17
12	Resistor	100 k ohms ± 2%	R13,14	8 16,17
13	Resistor	470 k ohms ± 2%	R12,15	8 16,17
14	Resistor	5.6 k ohms ± 2%	R4,5	8 16,17
15	Resistor	10 k ohms ± 2%	R3,6	8 16,17

### NOTE

Unless otherwise noted, 1/2-watt resistors may be used. To maintain specified performance, use replacement types designated in SDS Suppliers Code Index.

# Diode Gate No. 1

Assy. No. 100246

# GK51

Input

Gate Input

Loading

2 unit loads

Power Drain

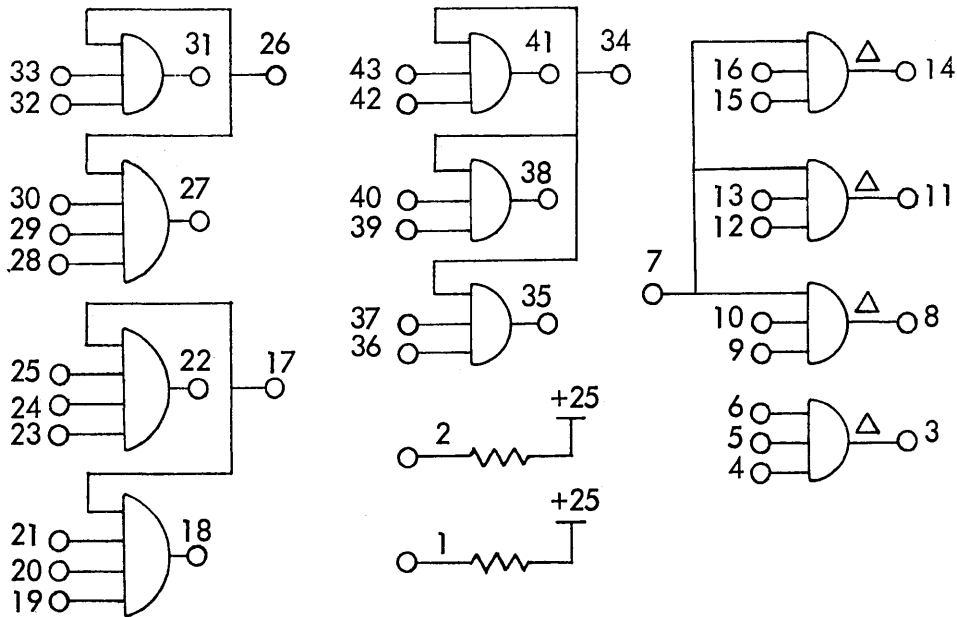
+25 Volt Supply 55 ma

Operating Frequency

to 4 Mc

Module Dissipation

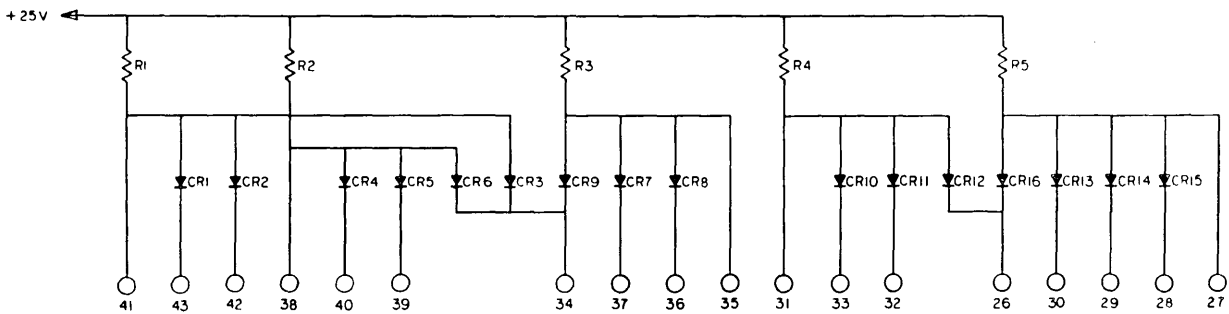
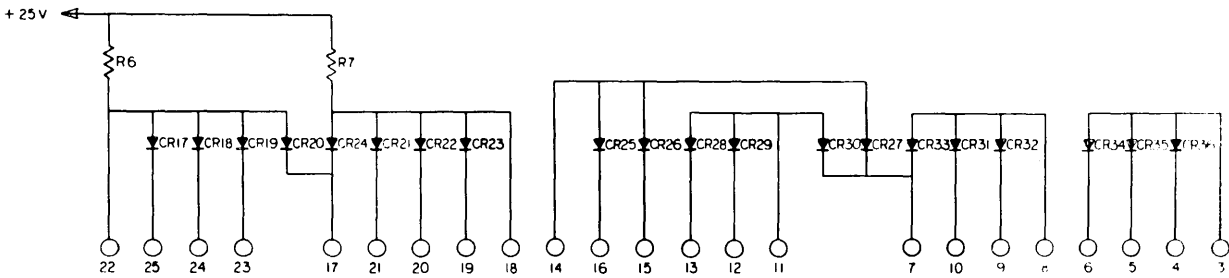
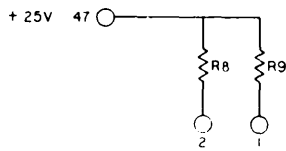
1.4 watts



# Module GK 51 Parts List

Item	Description	Designator	Qty	Supplier Code (See Index)
1	Diode, 1N907A 1N914A 1N3063 1N3065	CR1 thru CR36	36	4, 13 4, 12, 13, 14 4, 6 4
2	Resistor, $\pm 2\%$ , 1/2 watt, 3.9 k ohms	R1 thru R9	9	16, 17

POLARIZING PINS: 2 & 22





# Diode Gate No. 2

Assy. No. 100267

# GK52

Input

Gate Input

Loading

2 unit loads

Power Drain

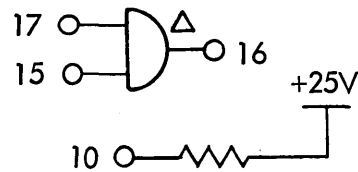
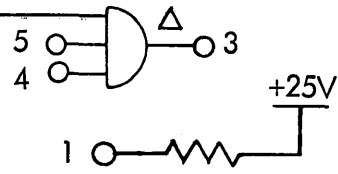
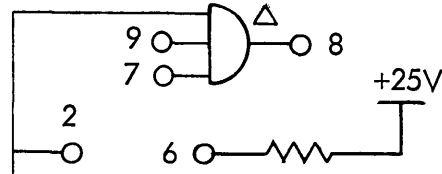
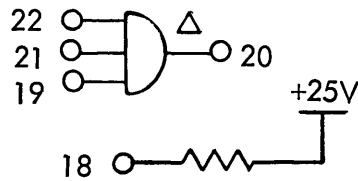
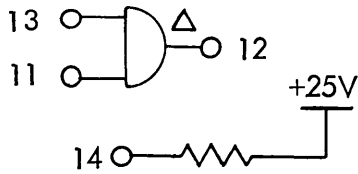
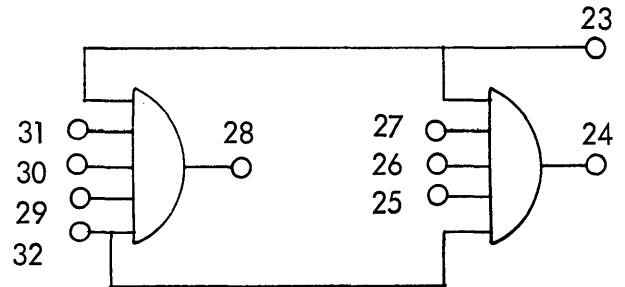
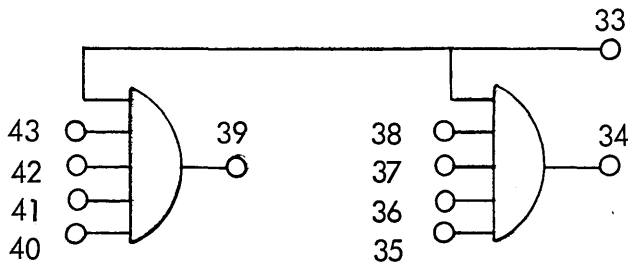
+25 Volt Supply 55 ma

Operating Frequency

to 4 Mc

Module Dissipation

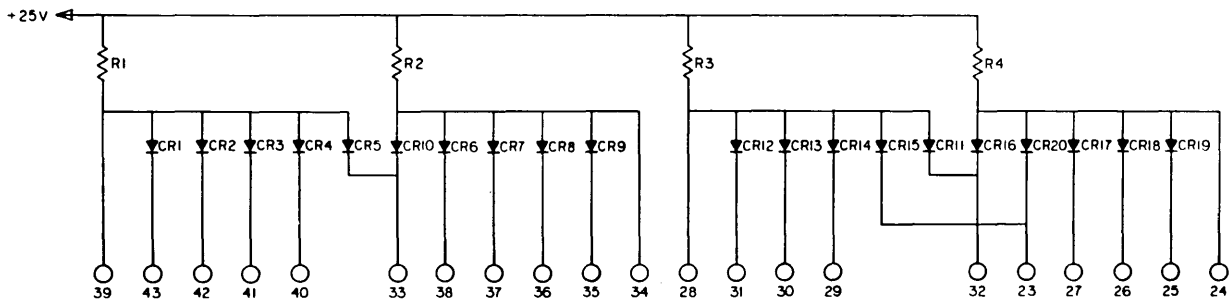
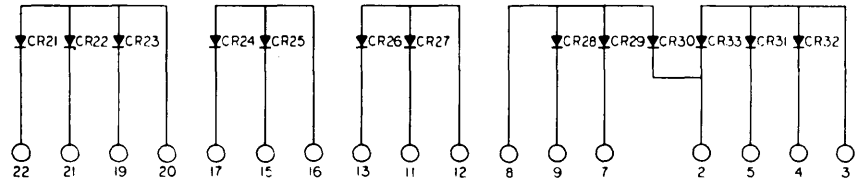
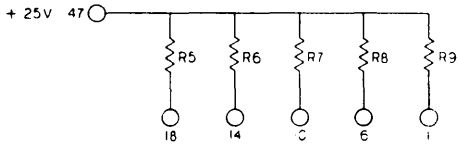
1.4 watts



Module GK 52 Parts List

Item	Description	Designator	Qty	Supplier Code (See Index)
1	Diode, 1N907A 1N914A 1N3063 1N3065	CR1 thru CR33	33	4, 13 4, 12, 13, 14 4, 6 4
2	Resistor, $\pm 2\%$ , 1/2 watt, 3.9 k ohms	R1 thru R9	9	16, 17

POLARIZING PINS: 2 & 20



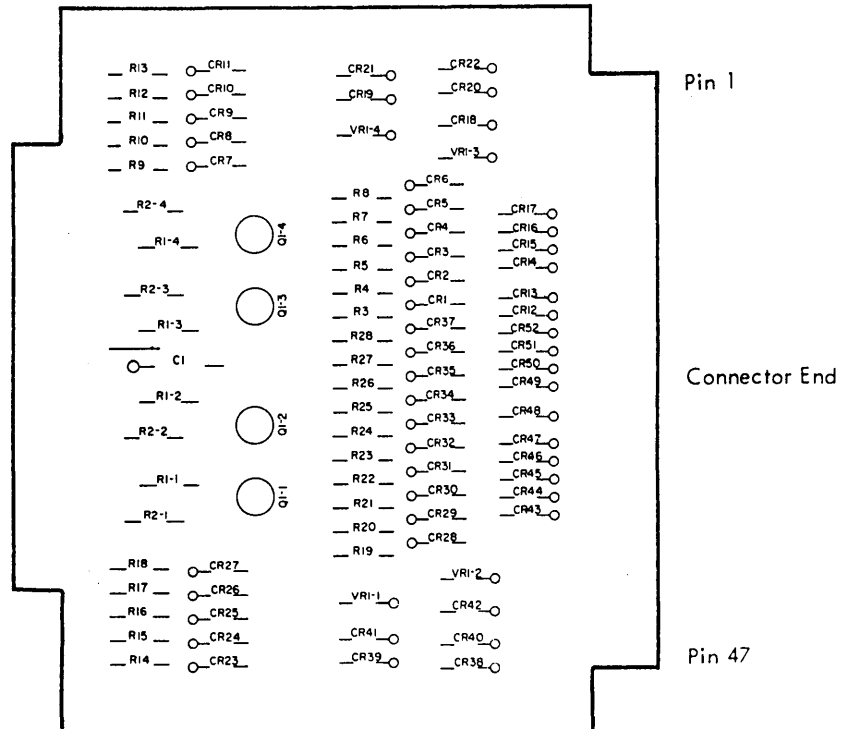
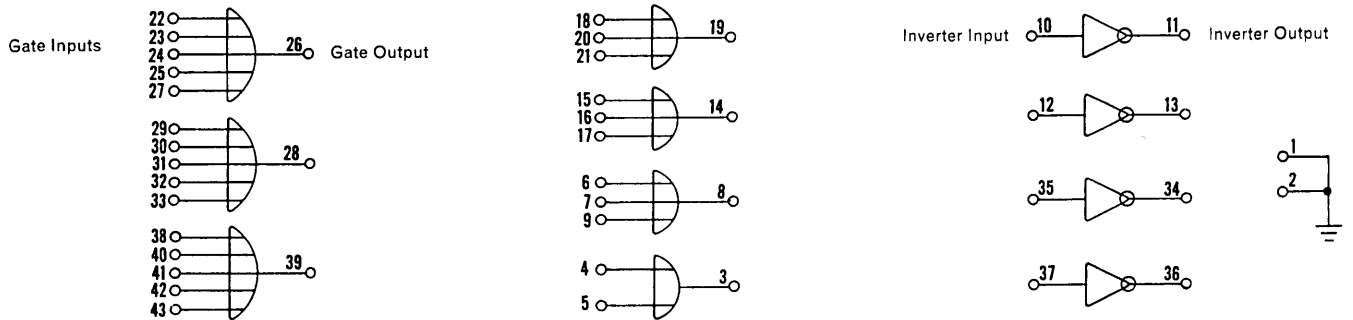
# OR Gate/Inverter (NOR)

IH11

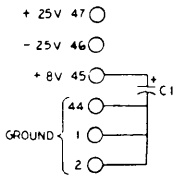
Assy. No. 100319

This module contains three 5-term OR gates, three 3-term OR gates, one 2-term OR gate, and four inverter circuits. Since each of the diode gate circuits is a complete OR structure, it may be freely used with the inverters to implement NOR logic. Two pins are available to ground unused OR gate inputs. Unused inverter circuits may be used in conjunction with Gate Expander or Flip-Flop modules.

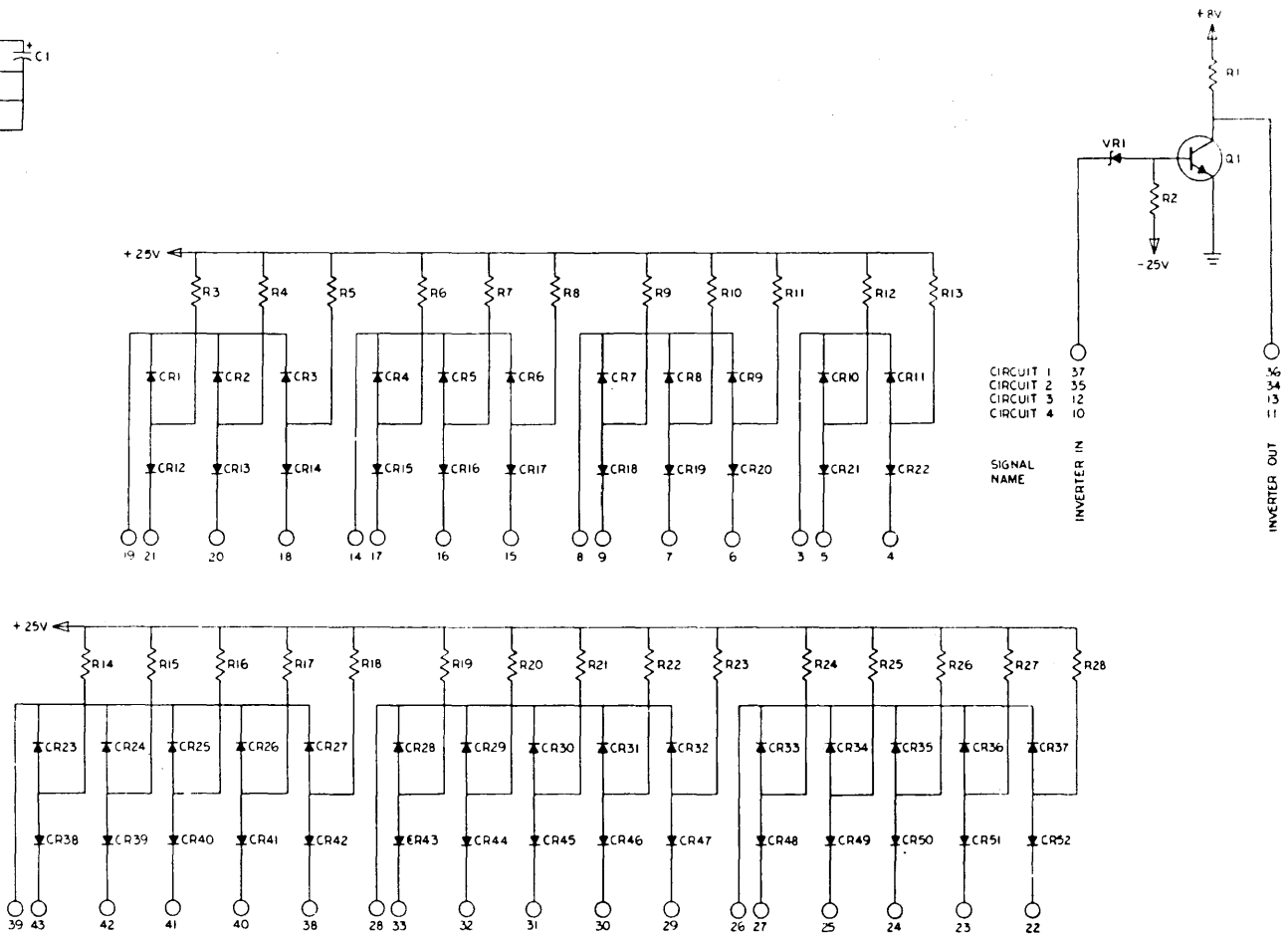
Maximum Operating Frequency	1 Mc
Fan-In	10 terms
Gate Input	2 loads
Output	12 loads
Output Delay (Typical)	60 ns
+25 Volt Supply	150 ma
+8 Volt Supply	38 ma
-25 Volt Supply	5 ma
Module Dissipation	3.6 watts



# Model IH11 Schematic



POLARIZING PINS 2 & 16



## Model IH11 Parts List

Item	Description	Designator	Qty.	Supplier Code (See Index)
1	Transistor	2N834	Q1	4, 5, 7, 95
2	Diode	1N746	VR1	2, 12, 13, 14
3	Diode	1N914A	CR1 through CR52	4, 12, 13, 14
4	Capacitor, Tantalum	4.7 $\mu$ f $\pm$ 20%, 50v	C1	23, 77
5	Resistor	820 ohms $\pm$ 2%	R1	16, 17
6	Resistor	3.9k ohms $\pm$ 2%	R23 through R28	16, 17
7	Resistor	18k ohms $\pm$ 2%	R2	16, 17

NOTE: Unless otherwise noted, 1/2-watt resistors may be used. To maintain specified performance, use replacement types designated in SDS Suppliers Code Index.

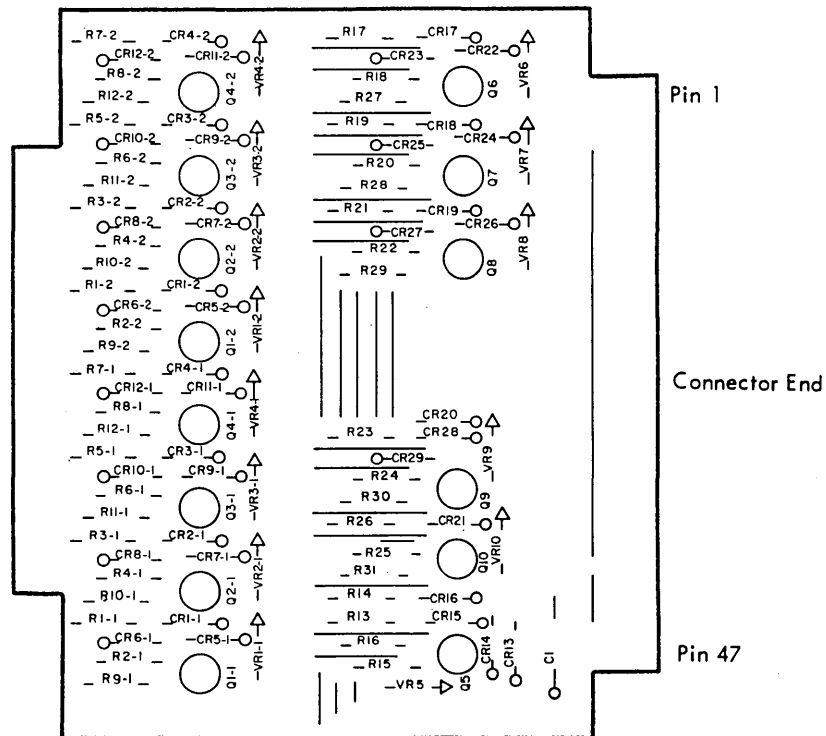
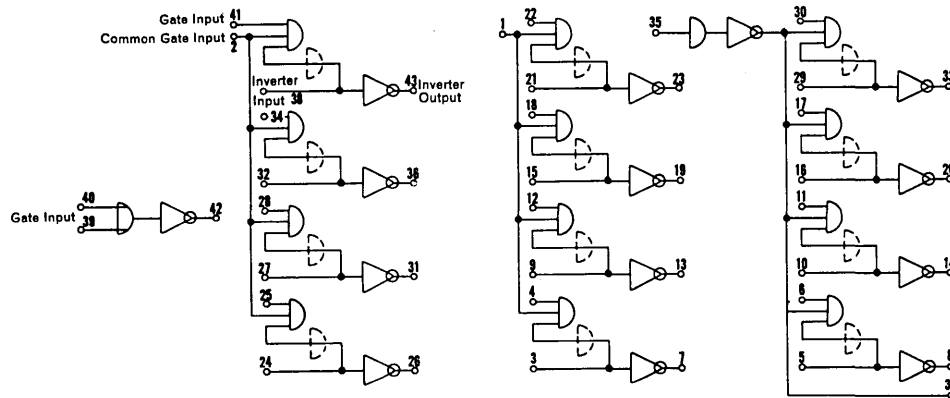
# AND Gate/Inverter

Assy. No. 101540

# IC12

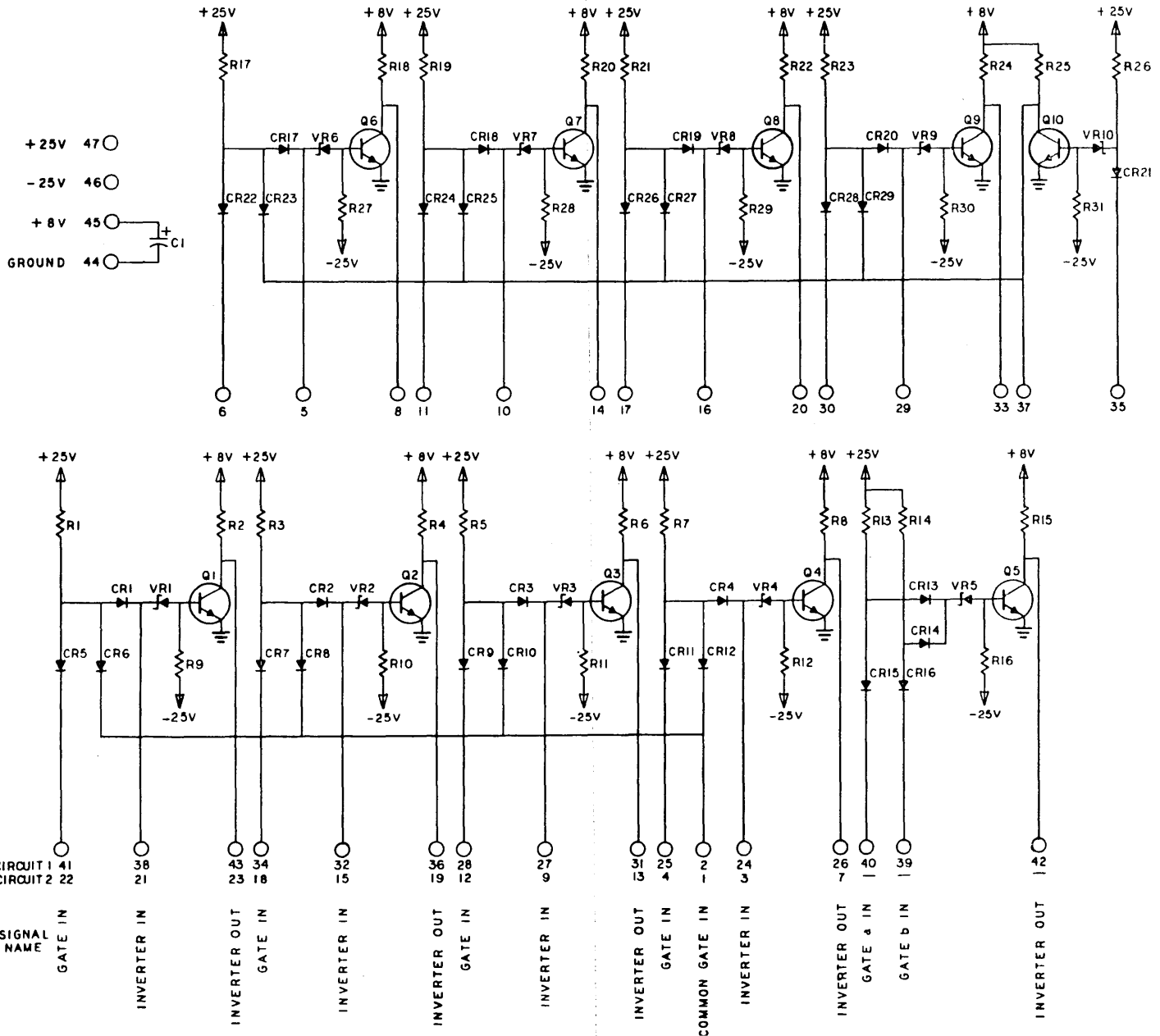
This module contains fourteen inverter circuits, each with a gated input. The gating may be expanded by wiring additional terms to the Inverter Input from a suitable Gate Expander module. These inverter circuits have a greater output capability than the other inverter circuits of the series. Inverter circuits may be used for NAND and NOR constructions or for improving the fan-out of flip-flops. The input gating is prewired to facilitate applications requiring decoding or selection operations, particularly when the inverter output is used to control flip-flop "repeater" type inputs. The input gate loads on the IC12 module are larger than normal loads. However the inverters operate satisfactorily at reduced output capability with standard gate inputs.

Max. Operating Freq.	300 kc
Fan-In (Inverter Input)	10 terms
Gate Input	2 loads
Common Gate Input	8 loads
Output	24 loads
Output (With External 300 kc Gate Input)	9 loads
Output Delay (Typical)	600 ns
+25 Volt Supply	96 ma
+8 Volt Supply	51 ma
-25 Volt Supply	9 ma
Module Dissipation	3.1 watts



Model IC12 Schematic

POLARIZING PINS: 10 & 34



Model IC12 Parts List

Item	Description	Designator	Qty.	Supplier Code (See Index)
1	Transistor 2N2538 2N2476 2N2848	Q1 through Q10	14	1 7 3
2	Diode 1N746	VR1 through VR10	14	2, 12, 13, 14
3	Diode 1N914A	CR1 through CR29	41	4, 12, 13, 14
4	Capacitor, Tantalum 4.7 $\mu$ f $\pm$ 20%, 50v	C1	1	23, 77
5	Resistor 3.9 k ohms $\pm$ 2%	R1, 3, 5, 7, 13, 14, 17 19, 21, 23, 26	15	16, 17
6	Resistor 2.2 k ohms $\pm$ 2%	R2, 4, 6, 8, 15, 18, 20 22, 24, 25	14	16, 17
7	Resistor 39 k ohms $\pm$ 2%	R9, 10, 11, 12, 16, 27 28, 29, 30, 31	14	16, 17

NOTE: Unless otherwise noted, 1/2-watt resistors may be used. To maintain specified performance, use replacement types designated in SDS Suppliers Code Index.

# Inverter Amplifier

Assy. No. 100388

# IK51

Fan In

Inverter Input 10 terms  
Standard or High Power Buffer Input 10 terms

Input

Inverter Input 2 loads  
Standard or High Power Buffer Input 2 loads

Output

Inverter Output 12 loads, 200 pf  
Standard Buffer A or B 20 loads, 200 pf  
High Power Buffer A or B 60 loads, 400 pf

Operating Frequency

4.0 Mc, Maximum

Power Drain

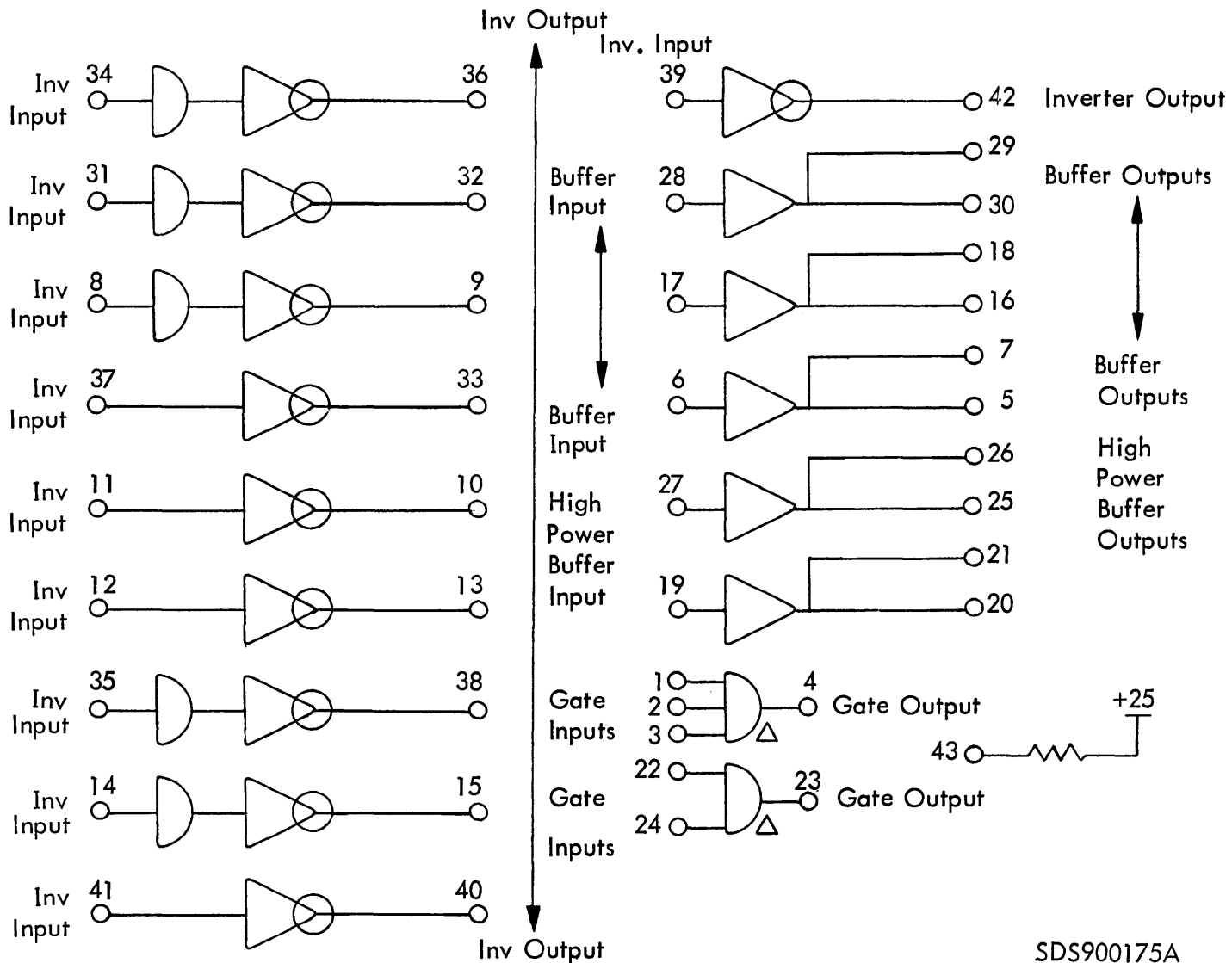
+45 Volt Supply 35 ma  
+ 8 Volt Supply 165 ma  
-25 Volt Supply 25 ma

Module Dissipation

2.8 watts

Delay (typical)

20 nsec  
45 nsec  
64 nsec



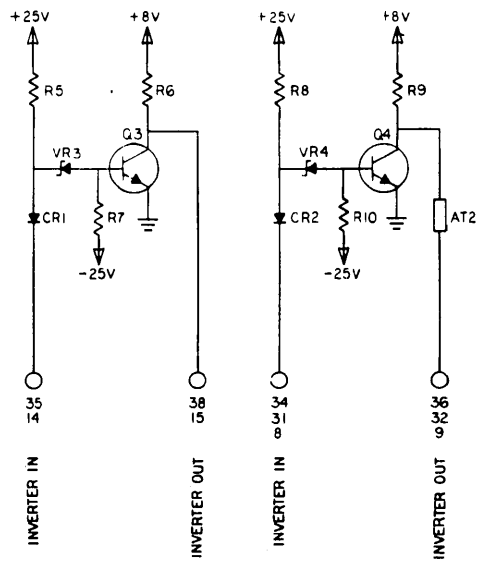
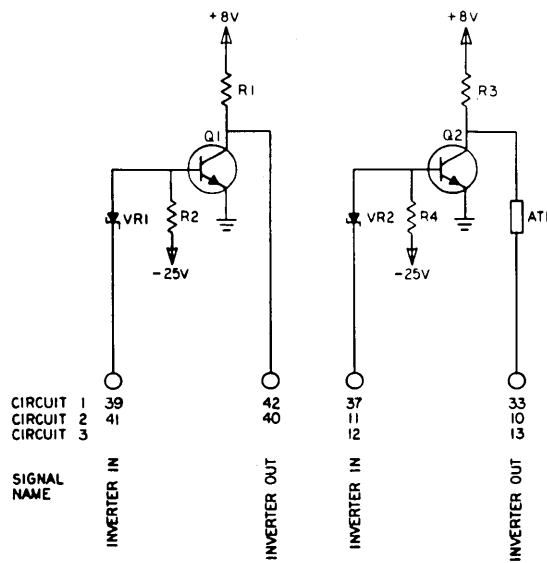
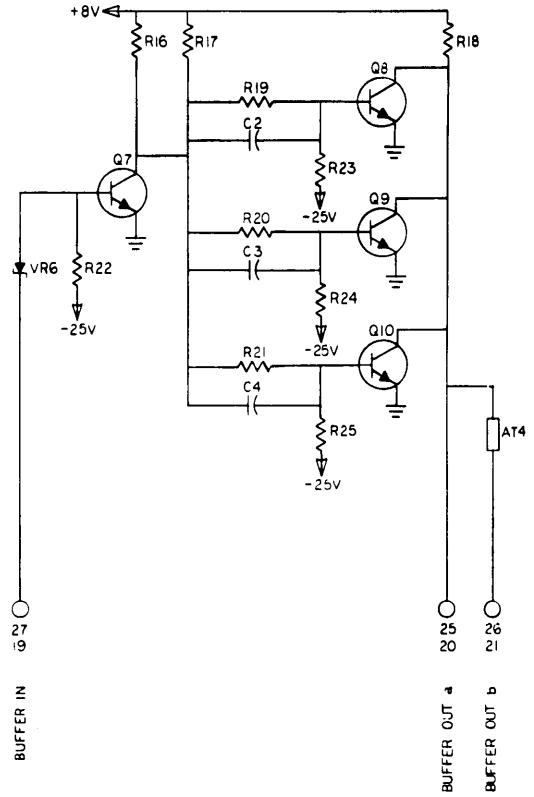
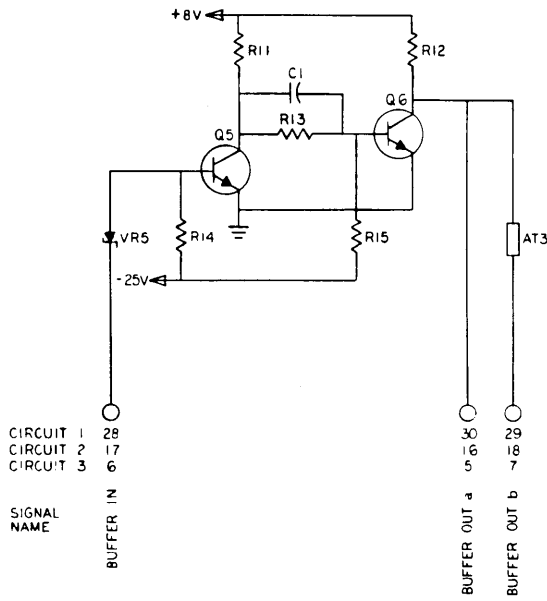
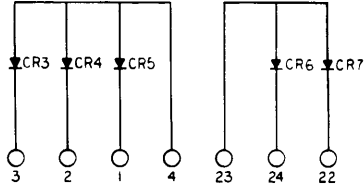
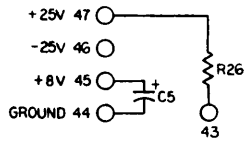
Module IK 51 Parts List

Item	Description	Designator	Qty.	Supplier Code (See Index)
1	Transistor 2N2369 2N2501	Q1 through Q10	24	3 1
2	Diode 1N746	VR1 through VR6	15	2, 13, 14, 32
3	Diode 1N907A 1N914A 1N3063 1N3065	CR1 through CR7	10	4, 13 4, 12, 13, 14 4, 6 4
4	Capacitor, Silver Mica, $\pm 5\%$ , 68pf	C1, 2, 3, 4	9	19, 20, 21
5	Capacitor, Tantalum, $\pm 5\%$ , 4.7 $\mu$ f	C5	1	22, 23, 77
6	Resistor, $\pm 2\%$ , 1/2 watt, 560 ohms	R11, 13, 16, 17, 19, 20, 21	16	16, 17
7	Resistor, $\pm 2\%$ , 1/2 watt, 820 ohms	R1, 3, 6, 9, 12	13	16, 17
8	Resistor, $\pm 2\%$ , 1/2 watt, 3.9 k ohms	R5, 8, 26	6	16, 17
9	Resistor, $\pm 2\%$ , 1/2 watt, 10 k ohms	R14	3	16, 17
10	Resistor, $\pm 2\%$ , 1/2 watt, 15 k ohms	R22	2	16, 17
11	Resistor, $\pm 2\%$ , 1/2 watt, 18 k ohms	R2, 4, 7, 10, 15	13	16, 17
12	Resistor, $\pm 2\%$ , 1/2 watt, 27 k ohms	R23, 24, 25	6	16, 17
13	Assy, Resistive Term. 3 ea. 56-590-65/3B	AT1 through AT4	11	72
14	Resistor, $\pm 2\%$ , 1/2 watt, 470 ohms	R18	2	16, 17



# Module IK51 Schematic

POLARIZING PINS: 2 & 8



# One-Shot Multivibrator

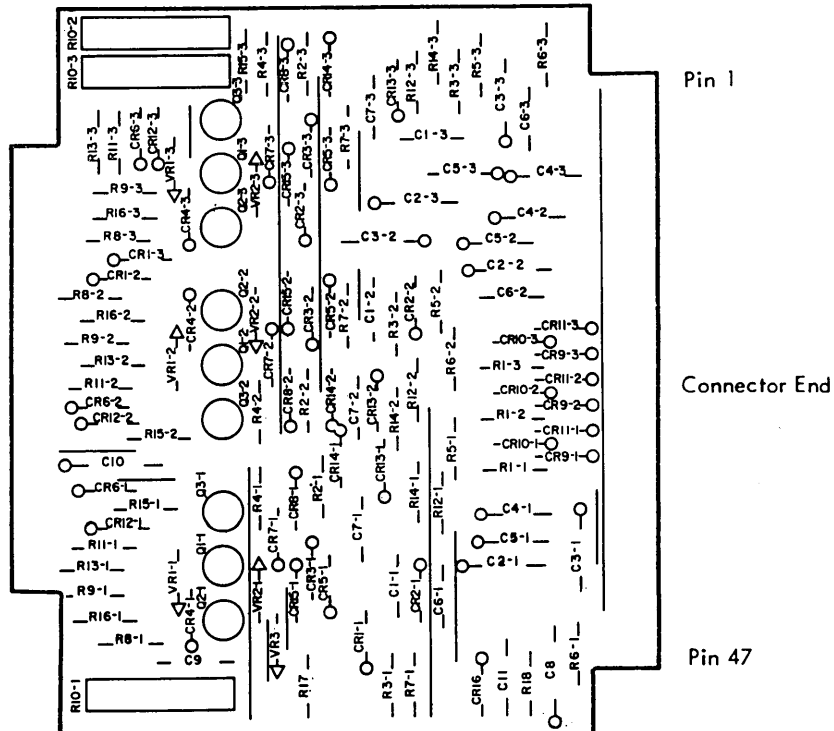
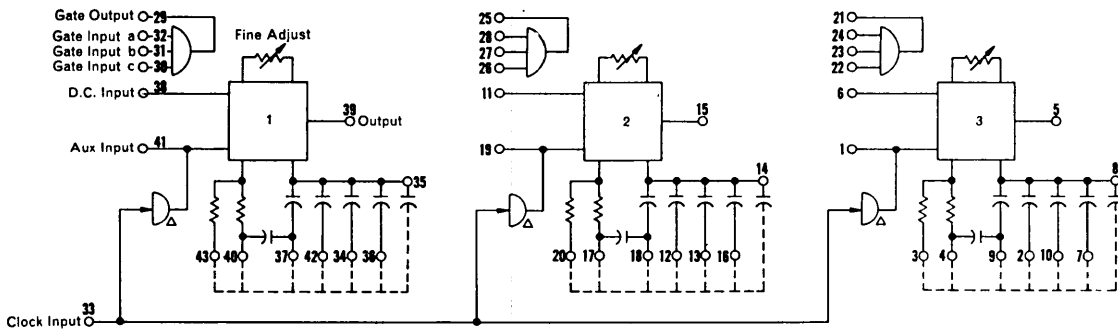
OX13

Assy. No. 103932

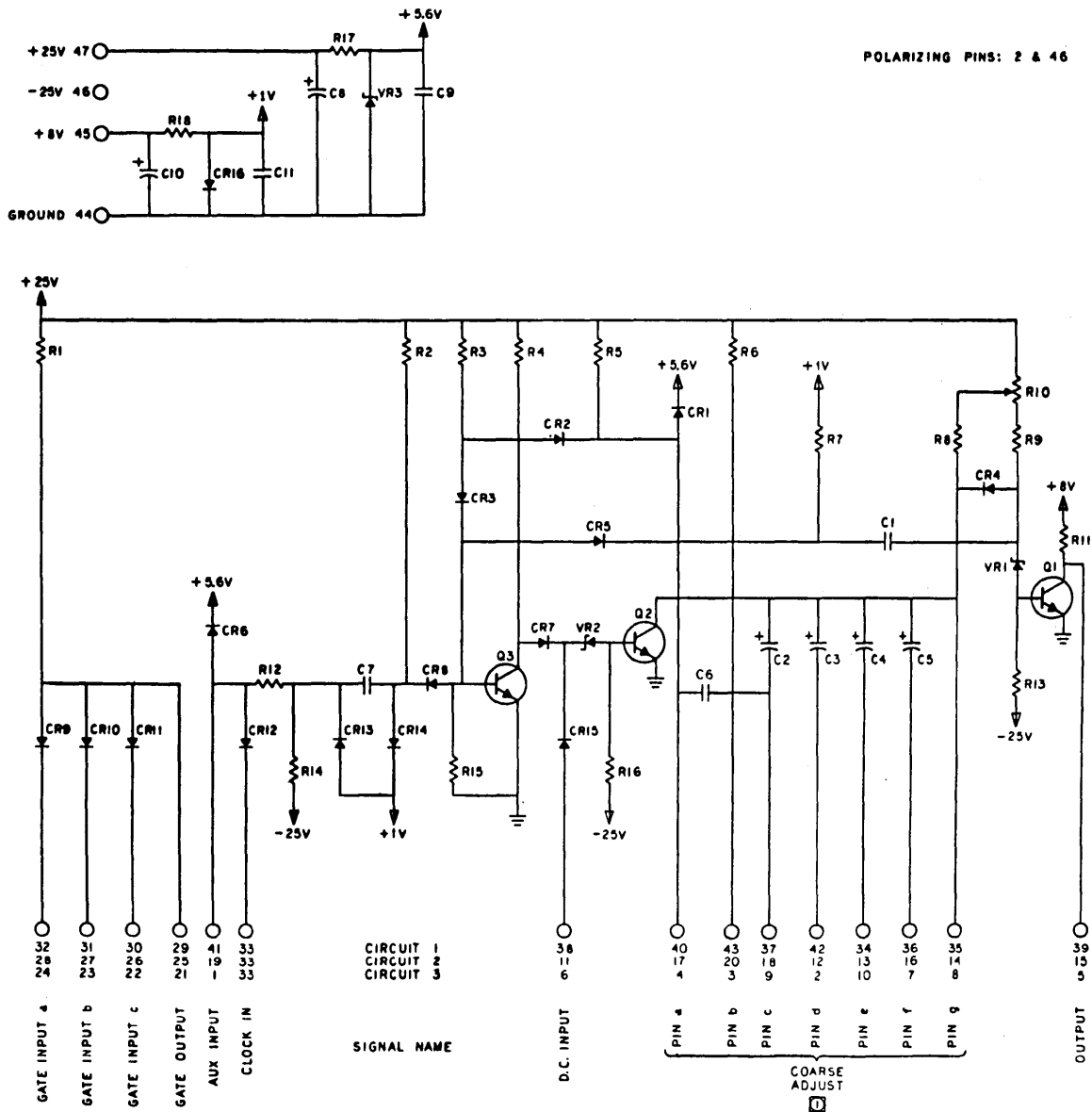
The module contains three identical one-shot circuits. Each circuit has a single output which is normally low, and becomes high for a defined period following the application of an input. The period can be adjusted. Both ac and dc input connections are provided, which must be driven by a standard AND gate (also provided on the module). When using the dc input, triggering occurs when the gate is enabled for at least 100 ns. For the ac input, triggering occurs when the gate is disabled (inhibited), following a period of the gate being enabled for at least 0.5 microseconds.

At duty cycles exceeding 40%, the nominal output pulse width is reduced by a small amount from the theoretical value. With 20% pulse width reduction, duty cycles up to 75% are permissible.

Gate Input	2 loads
Output	20 loads
Output pulse width (with capacitors on module)	2 μs to 200 ms
Maximum pulse width (with 47 μf 35 v capacitor)	10 seconds
Continuous adjustment	4:1 (Typical)
Temperature sensitivity of pulse width:	
Below 20 μs	0.2% per °C. (Typical)
Above 20 μs	0.3% per °C. (Typical)
+25 Volt Supply	48 ma
+8 Volt Supply	31 ma
-25 Volt Supply	4 ma
Module Dissipation	1.6 watts



# Model OX13 Schematic



**NOTES:**  
 1 THE TABLE BELOW GIVES COARSE ADJUST PIN CONNECTIONS FOR TEN DIFFERENT DELAY RANGES. FINE ADJUST IS ACCOMPLISHED BY VARYING R10.

DELAY RANGE	COARSE ADJUST PIN CONNECTIONS					
	a	b	c	d	e	f
2 μSEC-6.7 μSEC	X	X				
6.7 μSEC-20 μSEC	X	X	X			
20 μSEC-67 μSEC	X	X	X	X		
67 μSEC-200 μSEC	X	X	X	X	X	
200 μSEC-670 μSEC	X	X	X	X	X	X
670 μSEC-2 MSEC	X	X	X	X	X	X
2 MSEC-6.7 MSEC	X	X	X	X	X	X
6.7 MSEC-20 MSEC	X	X	X	X	X	X
20 MSEC-67 MSEC	X	X	X	X	X	X
67 MSEC-200 MSEC	X	X	X	X	X	X

**EXAMPLE:**  
 TO OBTAIN 300 μSEC DELAY, JUMPER COARSE ADJUST PINS a, b AND d, AND VARY R10 FOR FINE ADJUSTMENT.

BY ADDING A CAPACITOR C, EXTERNALLY, FURTHER DELAY RANGES CAN BE OBTAINED AS FOLLOWS:  
 a) JUMPER PIN a TO b AND CONNECT CAPACITOR BETWEEN PINS a AND g; THE DELAY RANGE THEN IS  $20 \times C$  TO  $67 \times C$  MILLISECONDS. (C IS IN MICROFARADS.)  
 b) CONNECT CAPACITOR BETWEEN PINS a AND g; THE DELAY RANGE IS  $67 \times C$  TO  $200 \times C$  MILLISECONDS. (C IS IN MICROFARADS.)

Model OX13 Parts List

Item	Description	Designator	Qty.	Supplier Code (See Index)
1	Transistor 2N2369 2N2501 2N2710	Q1,2	6	3, 11 1 95
2	Transistor 2N930 2N2483	Q3	3	3, 11 3
3	Diode 1N746	VR1,2	6	2, 12, 13, 14
4	Diode 1N914A	CR1 through CR16	46	4, 12, 13, 14
5	Diode 1N752	VR3	1	2, 12, 13, 14
6	Capacitor, Mica 100 pf $\pm$ 5%	C6	3	19, 20, 21
7	Capacitor, Mica 220 pf $\pm$ 5%	C1	3	19, 20, 21
8	Capacitor, Mica 510 pf $\pm$ 5%	C7	3	19, 20, 21
9	Capacitor, Mylar 1000 pf $\pm$ 10%	C2	3	74, 27
10	Capacitor, Mylar 0.01 $\mu$ f $\pm$ 10%	C3, 9, 11	5	74, 27, 26
11	Capacitor, Tantalum 0.1 $\mu$ f $\pm$ 20%, 50v	C4	3	23, 77
12	Capacitor, Tantalum 1.0 $\mu$ f $\pm$ 20%, 50v	C5	3	23, 77
13	Capacitor, Tantalum 4.7 $\mu$ f $\pm$ 20%, 50v	C8, 10	2	23, 77
14	Potentiometer 2 k ohms $\pm$ 10%	R10	3	35, 44
15	Resistor 270 ohms $\pm$ 2%	R12	3	16, 17
16	Resistor 470 ohms $\pm$ 2%	R9, 18	4	16, 17
17	Resistor 820 ohms $\pm$ 2%	R11	3	16, 17
18	Resistor 1.0k ohms $\pm$ 2%	R7	3	16, 17
19	Resistor 3.9k ohms $\pm$ 2%	R1, 8	6	16, 17
20	Resistor 4.7k ohms $\pm$ 2%	R17	1	16, 17
21	Resistor 15k ohms $\pm$ 2%	R2, 4	6	16, 17
22	Resistor 47k ohms $\pm$ 2%	R13, 16	6	16, 17
23	Resistor 100k ohms $\pm$ 2%	R15	3	16, 17
24	Resistor 220k ohms $\pm$ 2%	R6	3	16, 17
25	Resistor 470k ohms $\pm$ 2%	R3, 14	6	16, 17
26	Resistor 4.7 megohms $\pm$ 2%	R5	3	16, 17

NOTE: Unless otherwise noted, 1/2-watt resistors may be used. To maintain specified performance, use replacement types designated in SDS Suppliers Code Index.

# Relay Driver

Assy. No. 100905

# RK53

Input

Input a, b, c  
Auxiliary Input

Loading

2 loads  
2 loads

Operating Frequency

to 2 Kc

Output

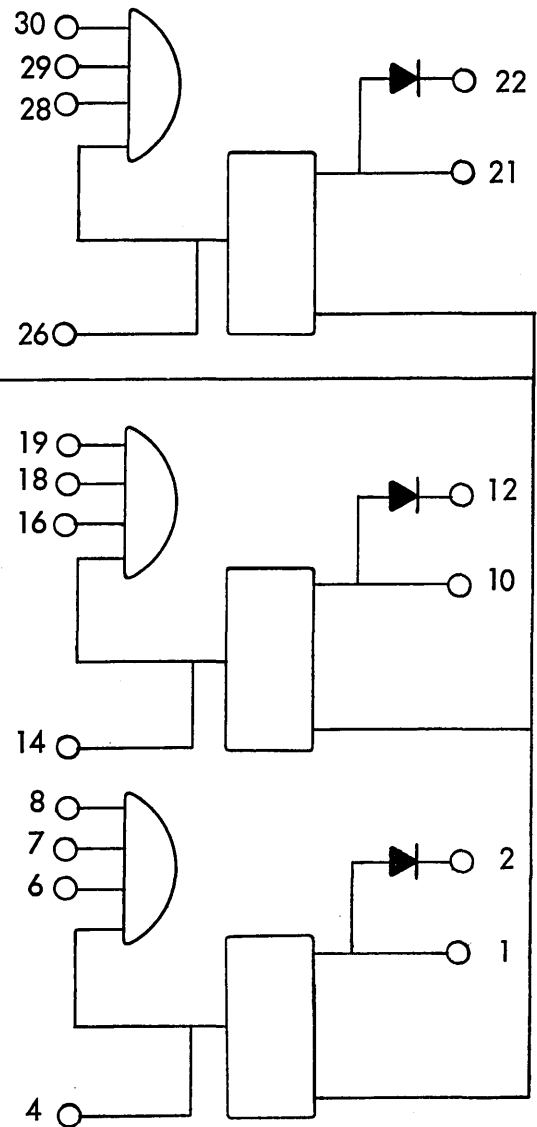
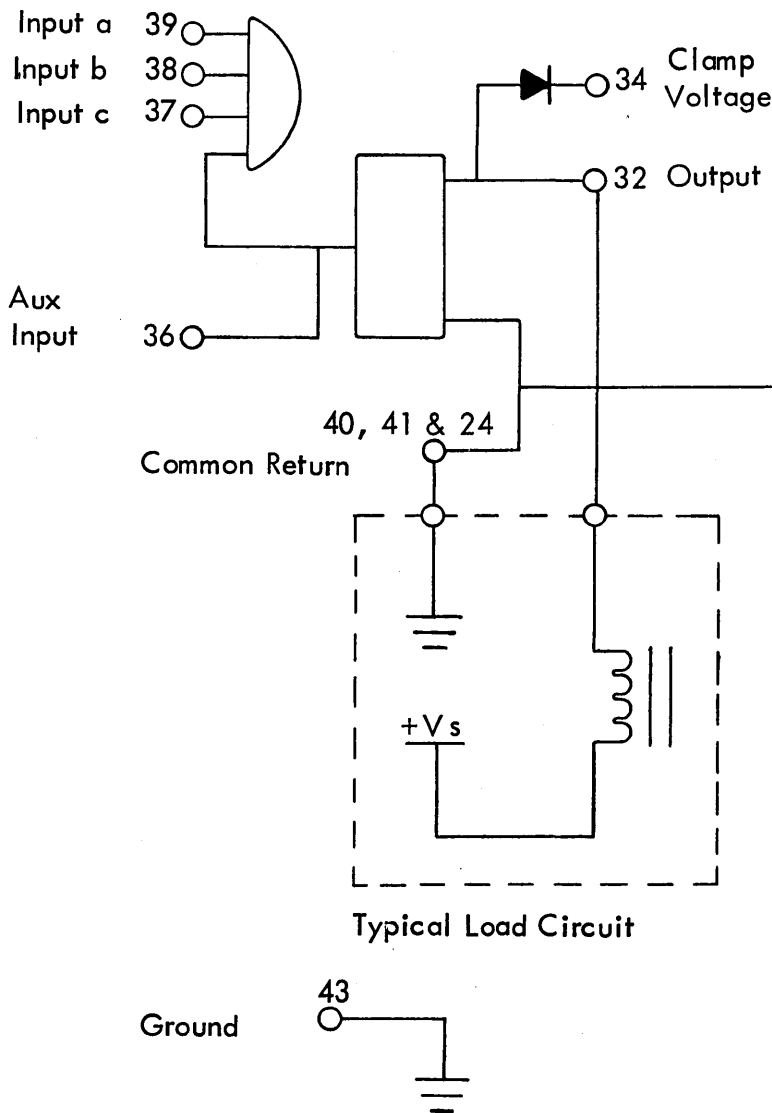
Current 350 ma (max)  
Clamp Voltage +60 volts (max)  
Relay Voltage +60 volts (max)  
Drop across Output Transistor + 2 volts (max)  
Switching Time 60  $\mu$ sec (typical)

Power Drain

+25 Volt Supply 28 ma  
+ 8 Volt Supply 0 ma  
(worst case) 600 ma  
-25 Volt Supply 22 ma

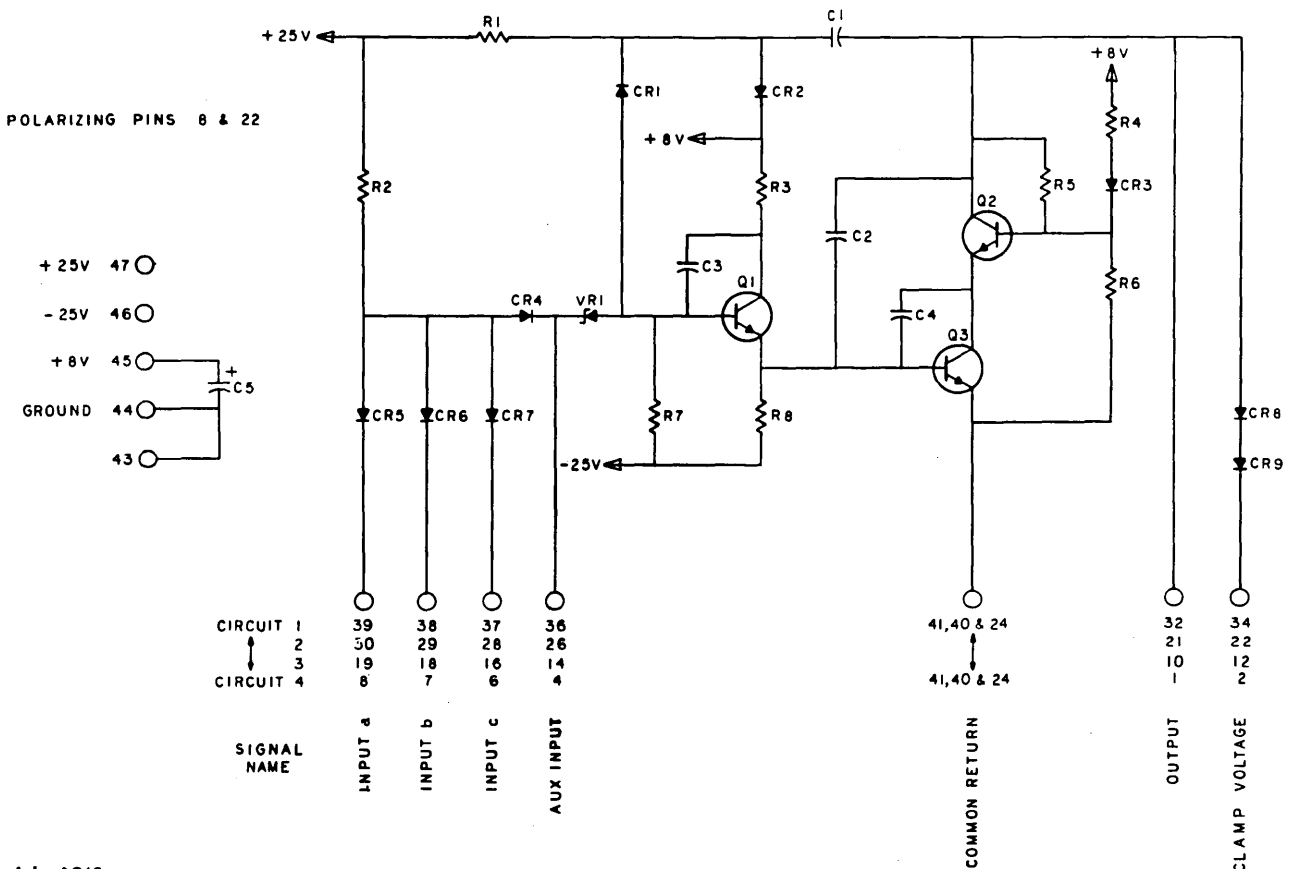
Module Dissipation

4.8 watts (typical)



# Module RK 53 Parts List

Item	Description	Designator	Qty	Supplier Code (See Index)
1	Transistor, 2N2219 2N2404	Q1,2,3	12	1 29
2	Diode, Zener 1N746	VR1	4	2, 13, 14, 32
3	Diode, 1N907A 1N914A 1N3063 1N3065	CR1,4,5,6,7,8,9	28	4, 13 4, 12, 13, 14 4, 6 4
4	Diode 1N921	CR2,3	8	13, 15, 28
5	Capacitor, Mylar, $\pm 5\%$ , 3300 pf	C1,4	8	26, 27, 74
6	Capacitor, Mylar, $\pm 5\%$ , 4700 pf	C2,3	8	26, 27, 74
7	Capacitor, Tantalum, $\pm 5\%$ , 4.7 $\mu$ f	C5	8	22, 23, 77
8	Resistor, Metal Film, 1 watt, $\pm 1\%$ , 100 ohms	R3	4	36, 38, 73
9	Resistor, Metal Film, 1 watt, $\pm 1\%$ , 68 ohms	R4	4	36, 38, 73
10	Resistor, 1/2 watt, $\pm 2\%$ , 3.9 k ohms	R2	4	16, 17
11	Resistor, 1/2 watt, $\pm 2\%$ , 4.7 k ohms	R8	4	16, 17
12	Resistor, 1/2 watt, $\pm 2\%$ , 22 k ohms	R5,6	8	16, 17
13	Resistor, 1/2 watt, $\pm 2\%$ , 47 k ohms	R1,7	8	16, 17



# Counter Flip-Flop

Assy. No. 101026

**FH15**

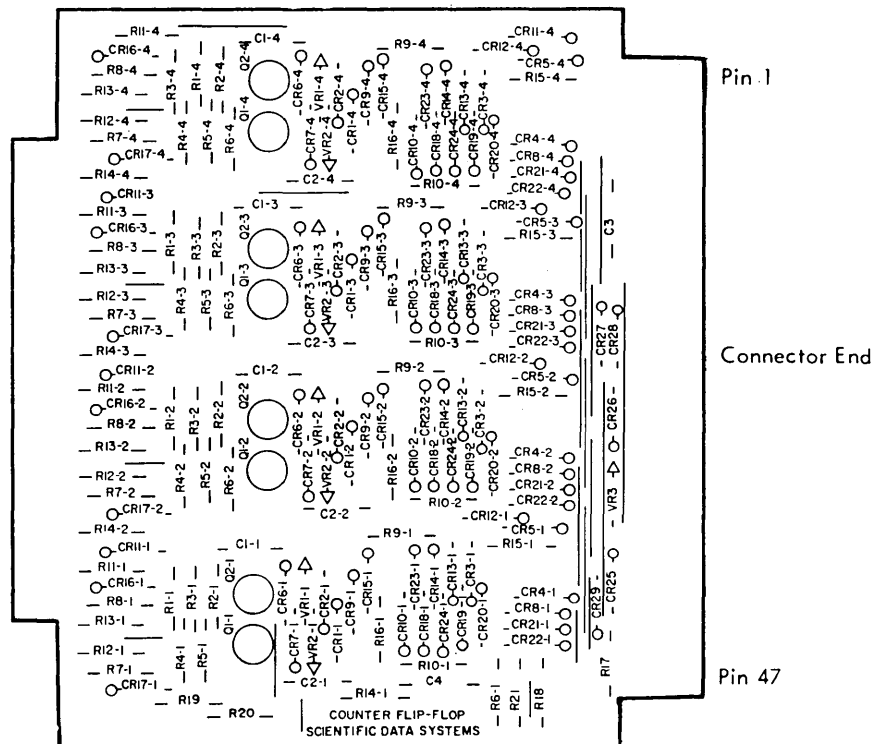
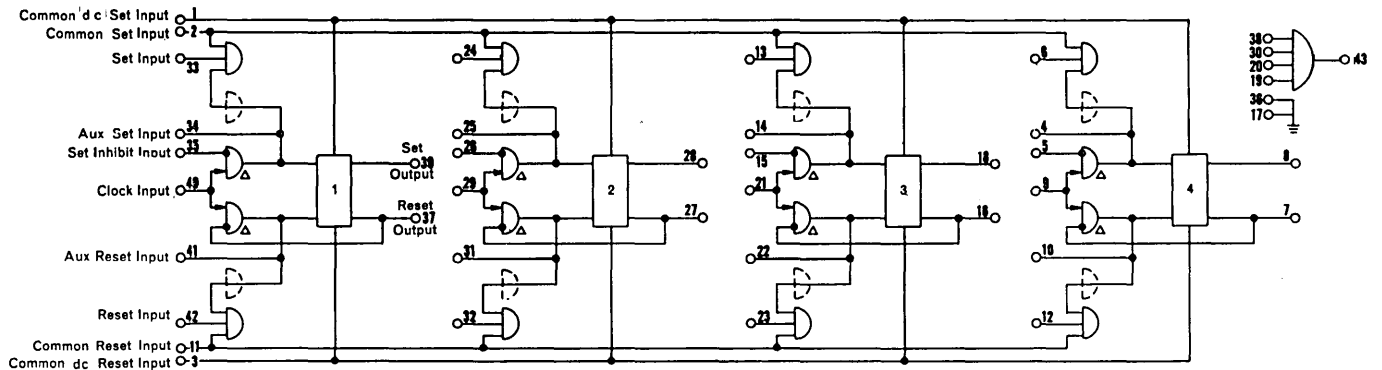
This module contains four flip-flop circuits which are independent except for the Common Set and Reset Input lines. The input gating on the card provides for constructing binary or decimal unlocked counters, and shift registers.

Either clocked or unclocked operation of the flip-flops is satisfactory. Clock termination circuits are prewired on the module, as are the comprehensive noise level control circuits.

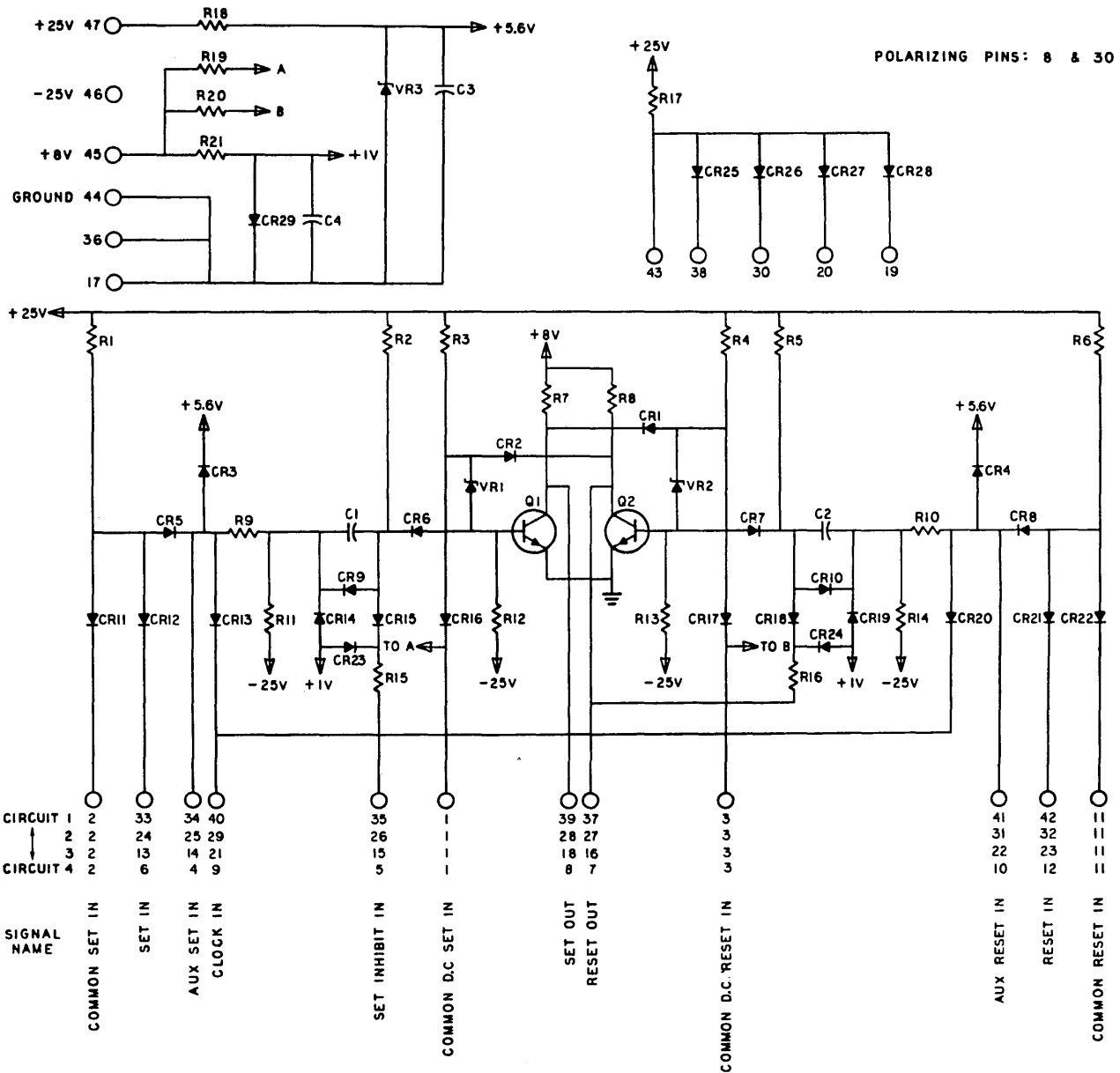
The Counter Flip-flop may be used in a unique "repeater" manner which enables it to follow the true and false changes of a single input logic signal connected to the Set Inhibit Input and the Reset Input. This flip-flop may be used in gated RS, JK, Delay, or Trigger configurations. Other applications include the mechanization of large, unusually efficient clocked counters.

True signals have no effect on the dc inputs which respond only when false (0-volt) signals are applied.

Maximum Operating Frequency	1 Mc
Fan-In (Each aux. input)	10 terms
Set, Reset Inputs	2 loads
Clock Input	4 loads
Common dc Set, Reset Inputs	6 loads
Common Set, Reset Inputs	8 loads
Set Inhibit Input	4 loads
Set Output	12 loads
Reset Output	8 loads
Output Delay (Typical)	100 ns
+25 Volt Supply	93 ma
+8 Volt Supply	54 ma
-25 Volt Supply	3 ma
Module Dissipation	2.9 watts



### Model FH15 Schematic



### Model FH15 Parts List

Item	Description	Designator	Qty.	Supplier Code (See Index)
1	Transistor	2N834	Q1,2	8 1,5,7,95
2	Diode	1N914A	CR1 through CR29	101 4,12,13,14
3	Diode	1N746	VR1,2	8 2,12,13,14
4	Diode	1N752	VR3	1 2,12,13,14
5	Capacitor, Mica	330pf ± 5%	C1,2	8 19,20,21
6	Capacitor, Mylar	0.01µf ± 10%	C3,4	2 74,27,26
7	Resistor	120 ohms ± 2%	R9,10,15,16	16 16,17
8	Resistor	470 ohms ± 2%	R21,7,8	9 16,17
9	Resistor	3.9 k ohms ± 2%	R1,6,17	9 16,17
10	Resistor	4.7 k ohms ± 2%	R18	1 16,17
11	Resistor	5.6 k ohms ± 2%	R3,4	8 16,17
12	Resistor	10 k ohms ± 2%	R2,5	8 16,17
13	Resistor	47 k ohms ± 2%	R19,20	2 16,17
14	Resistor	100 k ohms ± 2%	R12,13	8 16,17
15	Resistor	470 k ohms ± 2%	R11,14	8 16,17

NOTE: Unless otherwise noted, 1/2-watt resistors may be used. To maintain specified performance, use replacement types designated in SDS Suppliers Code Index.



Code No.	Name	Address	Part Number
1	Motorola Semiconductor	5005 E. McDowell Road, Phoenix, Arizona	Silicon Transistors
2	Motorola Semiconductor	5005 E. McDowell Road, Phoenix, Arizona	Silicon Diodes
3	Fairchild Semiconductor	545 Whisman Road, Mountain View, Calif.	Silicon Transistors
4	Fairchild Semiconductor	4300 Redwood Parkway, San Rafael, Calif.	Silicon Diodes
5	General Electric Company	Semiconductor Products Dept., Syracuse, N.Y.	Silicon Transistors
6	General Electric Company	Semiconductor Products Dept., Syracuse, N.Y.	Silicon Diodes
7	RCA Semiconductor Division	Somerville, New Jersey	Silicon Transistors
8	Silicon Transistor Corporation	150 Glen Cove Road, Carle Place, L.I., N.Y.	Silicon Transistors
9	Silicon Transistor Corporation	150 Glen Cove Road, Carle Place, L.I., N.Y.	Silicon Diodes
10	Hughes, Semiconductor Division	500 Superior Avenue, Newport Beach, Calif.	Silicon Transistors
11	Texas Instruments, Inc.	P.O. Box 5012, Dallas 22, Texas	Silicon Transistors
12	Texas Instruments, Inc.	P.O. Box 5012, Dallas 22, Texas	Silicon Diodes
13	Pacific Semiconductors, Inc.	12955 Chadron Avenue, Hawthorne, Calif.	Silicon Diodes

SUPPLIERS CODE INDEX

Code No.	Name	Address	Part Number
14	Continental Device Corporation	12515 Chadron Avenue, Hawthorne, Calif.	Silicon Diodes
15	Sperry Semiconductor Division	Norwalk, Connecticut	Silicon Diodes
16	Corning Electronic Components	550 High Street, Bradford, Pennsylvania	C 20 Series
17	Welwyn International, Inc.	3355 Edgecliff Terrace, Cleveland 11, Ohio	F 20 Series
18	Texas Instruments, Inc.	P.O. Box 5012, Dallas 22, Texas	CD 1/4R Series
19	Arco Electronics, Inc.	Community Drive, Great Neck, N. Y.	CM 15 B Series
20	Sangamo Electric Company	1207 N. 11th Street, Springfield, Illinois	CM 15 B Series
21	Micamold Elect. Mfg. Corp.	65 Gouverneur Street, Newark 4, N. J.	CM 15 B Series
22	Kemet Company	11901 Madison Avenue, Cleveland 1, Ohio	J-Series
23	Sprague Electric Company	481 Marshall Street, North Adams, Mass.	150 D Series
24	U.S. Semiconductor Products, Inc.	3540 W. Osborn Road, Phoenix, Arizona	TSK Series
25	General Electric Company	Capacitor Department, Hudson Falls, N. Y.	Lectrofilm- B Series
26	Sprague Electric Company	481 Marshall Street, North Adams, Mass.	158P Series
27	Sprague Electric Company	481 Marshall Street, North Adams, Mass.	192 P Series
28	Rheem Semiconductor Corp.	350 Ellis Street, Mountain View, Calif.	Silicon Diodes
29	National Semiconductor Corp.	P.O. Box 443, Danbury, Connecticut	Silicon Transistors
30	General Instrument Corp.	65 Gouverneur Street, Newark, N. J.	Silicon Transistors

SUPPLIERS CODE INDEX

Code No.	Name	Address	Part Number
31	Sylvania Electric Products, Inc.	100 Sylvan Road, Woburn, Mass.	Silicon Transistors
32	Western Semiconductors	2200 S. Fairview Street, Santa Ana, Calif.	Silicon Diodes
33	Computer Diode Corp.	250 Garibaldi Avenue, Lodi, N. J.	Silicon Diodes
34	Tungsol Electric, Inc.	1 Summer Avenue, Newark, N. J.	Silicon Diodes
35	Bourns, Inc.	6135 Magnolia Avenue, Riverside, Calif.	Potentiometers
36	International Resistance Co.	401 N. Broad Street, Philadelphia, Pa.	CEC/T0 Type, MEC/T0 Type
37	General Resistance, Inc.	430 Southern Blvd., New York, N. Y.	Precision Resistors 16S32A8 Series
38	Sprague Electric Co.	481 Marshall St. North Adams, Mass.	420E/FC5 Type
39	Technitrol Engineering Co.	1952 E. Allegheny Ave., Philadelphia, Pa.	H Series
40	Technitrol Engineering Co.	1952 E. Allegheny Ave., Philadelphia, Pa.	G Series
41	Delevan Electronics Corp.	77 Olean Road, East Aurora, N. Y.	220-XX/R Series
42	Delevan Electronics Corp.	77 Olean Road, East Aurora, N. Y.	1537 Series 2500 Series
43	Delco Radio Division, G.M.	700 E. Firmin Street, Kokomo, Indiana	Silicon Diodes
44	Atohm Electronics	7648 San Fernando Road, Sun Valley, Calif.	Potentiometers 124 Series
45	Dale Electronics Inc.	1370 28th Avenue, Columbus, Nebraska	Power Resistors
46	Tepro Electric Corporation	5 St. Paul Street, Rochester, N. Y.	Power Resistors
47	Sage Electronics Corporation	Country Club Road, E. Rochester, N. Y.	Power Resistors

SUPPLIERS CODE INDEX

Code No.	Name	Address	Part Number
48	Littelfuse, Inc.	1865 Miner Street, Des Plaines, Illinois	Fuses
49	Bussman Manufacturing Co.	University @ Jefferson, St. Louis, Missouri	Fuses
50	Sola Electric Company	1717 Busse Road, Elk Grove, Illinois	CVN Transformers
51	Cinch-Jones Division	1026 S. Homan Avenue, Chicago, Illinois	#142 Terminal Block
52	Cinch-Jones Division	1026 S. Homan Avenue, Chicago, Illinois	#300 Series Connector
53	Ohmite Manufacturing Co.	3635 Howard Street, Skokie, Illinois	#VT2 Transformer
54	Cutler-Hammer Inc.	321 N. 12th Street, Milwaukee, Wisc.	7360 K7
55	Centralab	900A E. Keefe Avenue, Milwaukee, Wisc.	PA 2005
56	Eldema Corporation	1805 Belcroft Avenue, El Monte, Calif.	36-3ACB-2H
57	Sprague Electric Co.	481 Marshall Street, N. Adams, Mass.	Capacitors 36D Series
58	General Electric Co.	Capacitor Department, Imo, South Carolina	Capacitors 43F 3000 Series
59	Sangamo Electric Company	1207 N. 11th Street, Springfield, Illinois	Capacitors DCM Series
60	Cinch-Jones Division	1026 S. Homan Avenue, Chicago, Illinois	#141 Terminal Block
61	Cutler-Hammer Inc.	321 N. 12th Street, Milwaukee, Wisc.	8363-K8
62	Amelco, Inc.	341 Moffet Blvd. Mountain View, Calif.	Silicon Transistors
63	Transitron Electronic Corp.	168-182 Albion St. Wakefield, Mass.	Silicon Diodes

SUPPLIERS CODE INDEX

Code No.	Name	Address	Part Number
64	Hughes, Semiconductor Division	500 Superior Ave., Newport Beach, Calif.	Silicon Diodes
65	General Instrument Corp.	65 Gouverneur St. Newark 4, N. J.	Silicon Diodes
66	American Semiconductor Corporation	3940 N. Kilpatrick, Chicago, Illinois	Silicon Diodes
67	Hoffman Electronics Corp. Semiconductor Division	Box 471, 1001 N Arden El Monte, Calif.	Silicon Diodes
68	Delta Semiconductors, Inc.	835 Production Pl. Newport Beach, Calif.	Silicon Diodes
69	Pulse Engineering, Inc.	Santa Clara, Calif.	Transformers
70	Nytronics, Inc.	550 Springfield Ave. Berkeley Heights, NJ.	S, M and L Series
71	Alladin Electronics Inc.	Nashville 10, Tenn.	Transformers
72	Ferroxcube Corp. of America	Saugerties, N. Y.	Ferrite Components
73	Electra Mfg. Co., Electronics, Division	4051 Broadway Kansas City, Mo.	MFS 1/2 T0 Series
74	General Electric Co.	Capacitor Dept. Hudson Falls, N. Y.	61F-AA Series
75	U. S. Semiconductor Products, Inc.	3540 W. Osborn Rd. Phoenix, Arizona	TSK6 Series
76	U. S. Semiconductor Products, Inc.	3540 W. Osborn Rd. Phoenix, Arizona	TSK20 Series
77	U. S. Semiconductor Products, Inc.	3540 W. Osborn Rd. Phoenix, Arizona	TSK50 Series
78	Ohmite Mfg. Co.	3635 Howard St. Skokie, Illinois	Relays
79	Allied Control Co., Inc.	2 E. End Ave. New York, N. Y.	Relays
80	Sprague Electric Co.	481 Marshall St. No. Adams, Mass.	90P Series
81	Sangamo Electric Co.	1207 No. 11th St. Springfield, Ill.	5010 Series

SUPPLIERS CODE INDEX

Code No.	Name	Address	Part Number
82	Elco Corporation	M St. below Erie Ave. Philadelphia, Pa.	Connectors
83	Chicago Miniature Lamp Works	1510 N. Ogden Ave. Chicago, Ill.	Lamps
84	General Electric Co.	Miniature Lamp Dept. Nela Park Cleveland 12, Ohio	Lamps
85	Tung-Sol Electric Co.	370 Orange Street Newark 7, N. J.	Lamps
86	Automatic Electric Sales Corp.	North Lake, Ill.	Relays
87	U. S. Semiconductor Products, Inc.	3540 W. Osborn Rd. Phoenix, Ariz.	TSK35 Series
88	Sage Electronics Corp.	Country Club Rd. E. Rochester, N. Y.	3550M Series
89	Dale Electronics Corp.	1370 28th Ave. Columbus, Neb.	RH-50 Series
90	J. W. Miller Co.	5917 S. Main Street Los Angeles, Calif.	9310/9210/9220 Series
91	Stanwyck Winding Co.	137 Walsh Ave. Newburgh, N. Y.	20000/40000/60000 Series
92	Int. Resistance Corp.	401 N. Broad St. Phila., Pa.	MEF/TO Series
93	Electra Mfg.	4051 Broadway Kansas City, Mo.	MFS 1/ TO Series
94	Sprague Electric	481 Marshall St. North Adams, Mass.	421E/FC5 Series
95	Philco Corp. Lansdale, Pa.	Lansdale, Pa.	Semiconductors
96	Amperex Electronic Corp.	Hicksville, Long Island, N. Y.	Semiconductors & Indicators
97	Siliconix, Inc.	1140 W. Evelyn Ave. Sunnyvale, Calif.	Semiconductors
98	Continental Conn. Corp.	Woodside 77, N. Y.	Connectors

SUPPLIERS CODE INDEX

Code No.	Name	Address	Part Number
99	Sprague Electric Co.	481 Marshall St. No. Adams, Mass.	261E Series
100	Ohmite Mfg. Co.	3635 Howard St. Skokie, Illinois	2TA-51FS Series
101	Royal Electric Corp.	Pawtucket, Rhode Island	Plugs and ac cords
102	Harvey Hubbell, Inc.	Bridgeport, Conn.	Connectors
103	The Wiremold Co.	Hartford 10, Conn.	ac Wiremolds
104	Dialight Corp.	60 Stewart Ave. Brooklyn, N. Y.	Lamps
105	Heinemann Electric Co.	120 Brunswick Pike Trenton, N. J.	Circuit Breakers
106	Arrow-Hart & Hegeman Electric Co.	103 Hawthorne St. Hartford, Conn.	Switches
107	Allen-Bradley Co.	136 W. Greenfield Ave. Milwaukee, Wisc.	Contactors
108	General Electric Co.	West Lynn, Mass.	Meters
109	Nytronics, Inc.	550 Springfield Ave. Berkeley Heights, N. J.	WEE Series Inductors
110	Winchester Electronics Inc.	Norwalk, Conn.	Connectors
111	Amp, Inc.	Harrisburg, Pa.	Connectors
112	Grayhill, Inc.	P.O. Box 373 561 Hillgrave Ave. La Grange, Ill.	Switches
113	Controls Co.	9555 Soreng Ave. Schiller Park, Ill.	Switches
114	Amphenol Borg Electronics	1830 S. 54 Ave. Chicago, Ill.	Connectors
115	International Resistance Co.	401 N. Broad St. Philadelphia, Pa.	MEA Series
116	International Resistance Co.	401 N. Broad St. Philadelphia, Pa.	MEF Series

SUPPLIERS CODE INDEX

Code No.	Name	Address	Part Number
117	Electra Mfg. Co. Electronics Division	4051 Broadway Kansas City, Mo.	MF 1/8 Series
118	Electra Mfg. Co. Electronics Division	4051 Broadway Kansas City, Mo.	MF1 Series
119	Texas Instruments, Inc.	P.O. Box 5012 Dallas 22, Texas	Sensistor
120	Thermalloy Co.	4417 No. Central Expressway Dallas 5, Texas	Heat Sinks
121	Astro Dynamics, Inc.	Second Avenue Northwest Industrial Pk Burlington, Mass.	Heat Sinks
122	Tor Mfg. Co.	1533 E. Walnut St. Pasadena, California	Heat Sinks
123	Wakefield Eng. Inc.	9 Broadway Wakefield, Mass.	Heat Sinks
124	Bourns, Inc.	6135 Magnolia Ave. Riverside, California	3250L Series
125	International Resistance Co.	401 N. Broad St. Philadelphia, Pa.	201-00 Series
126	General Resistance Inc.	430 Southern Blvd. New York, N.Y.	10S30A6 Series
127	Erie Resistor Corp.	644 W. 12th Street Erie, Pa.	503 Series
128	Centralab	900A E. Keefe Ave. Milwaukee, Wisc.	833 Series
129	General Resistance Inc.	430 Southern Blvd. New York, N.Y.	8S24A4 Series
130	C.P.Clare & Co.	3101 Pratt Blvd. Chicago, Ill.	
131	The Adams & Westlake Co.	N. Michigan St. Elkhart, Indiana	



SUPPLIERS CODE INDEX

Code No.	Name	Address	Part Number
132			
133			
134	Cannon Electric Co.	3208 Humbolt St. Los Angeles 31, Calif.	Connectors
135	Indiana General	Keasbey, New Jersey	Toroids
136	Sprague	481 Marshall Street North Adams, Mass.	
137	Electro Cube	805 Fairview Ave. So. Pasadena, Calif.	
138	Monitor Products Inc.	Pasadena, California	Crystals
139	Rotron Mfg. Co.	Woodstock, N. Y.	Blowers
140	Digitran Co.	Pasadena, California	511 Series
141	Minneapolis Honeywell	2747 4th Ave. South Minneapolis 8, Minn.	Silicon Transformers
142	Babcock Relay, Inc.	1645 Babcock Ave. Costa Mesa, Calif.	BW Series Relay
143	Simco Company	19th & Walnut St. Lansdale, Penn.	Bar-Static & Power Supply
144	IMC Magnetic Corp.	570 Main St. Westburg, N. Y.	Fans
145	Malco Mfg., Co.	4025 Westlake St. Chicago, Ill.	Terminals
146	Drake, Mfg. Co.	4626 No. Olcott Ave. Chicago, Ill.	HR 119 Neon Lamp