CARTRIDGE DISK CONTROLLER
MODEL 7250A01
ASSEMBLY NO. 202624

903059A
Price: $38.00

FIELD ENGINEERING
MAINTENANCE MANUAL

CARTRIDGE DISK CONTROLLER MODEL 7250A01

ASSEMBLY NO. 202624

Specifications, equipment descriptions, and procedures contained herein are subject to change without notice.

February 1974

Prepared by
Service Education, Western Operations

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701 So. Aviation Blvd., El Segundo, Calif. 90245, 213 679-4511

PREFACE

The purpose of a Field Engineering Maintenance Manual (FEMM) is to provide, under one cover, Development Engineering-produced documentation which is relevant to the maintenance of Xerox Computer equipment.

ENGINEERING SUPPORT INDEX (ESI)

The Engineering Support Index is a table of contents indicating the drawings contained in this manual and reflects the revision level of each individual drawing to the Top Assembly drawing.

UPDATING

When Engineering Orders (EO) to Top Assemblies are released, documentation is updated and distributed to appropriate installations by Xerox Computer Field Engineering through the method of Field Modification Kits (FMK's). If Xerox is responsible for maintaining the affected equipment, the EO and the documentation Update Package is sent to the appropriate customer Service District office. The Customer Engineer is then responsible for prompt EO installation and manual updating. If the Xerox customer is responsible for equipment maintenance, a notification of the EO and the documentation Update Package is sent to the customer address that the customer has provided.

The Update Package typically includes a revised title page, revised Engineering Support Index page, and all pages that have been revised.

CHANGES

Changes to a FEMM drawing can only be brought about by the submission of a Drawing Change Request (DCR). To effect a drawing change, field personnel must submit a Technical Action Request (TAR). A DCR may then be submitted by Maintenance Engineering after the TAR is reviewed. Customers who wish to notify Xerox of any discrepancies within the FEMM may submit their comments on the Reader Survey sheet in the back of the manual and forward it to Xerox Computer Field Engineering Publications.

ENGINEERING SUPPORT INDEX

MODEL 7250A01 TOP ASSEMBLY 202624 LEVEL A

NAME CARTRIDGE DISK CONTROLLER

ENGINEERING SUPPORT INDEX (Cont.)

MODEL 7250A01 TOP ASSEMBLY 202624 LEVEL A

NAME CARTRIDGE DISK CONTROLLER

RELATED PUBLICATIONS

The following Xerox publications contain information not included within this manual. These publications must be available as part of Site Documentation in order for the user of this manual to learn, install, operate, and maintain the equipment.

Publication Title	Document No.
Cartridge Disk Reference Manual	903024
Cartridge Disk Drive Maintenance Manual Modes 7251/7252	903042
Sigma 2/3 Diagnostic Program Monitor Manual	901650
Sigma 2/3 Comprehensive RAD Diagnostic Manual	901721
Sigma 5/7 Diagnostic Program Monitor Manual	901649
Sigma 5/7 Comprehensive RAD Diagnostic Manual	901678

SECTION I

THEORY OF OPERATIONS

Revisions				204262	A
LAL	Rev.	Description	Chk	Date	Approved
X	A	MANUFACTURING RELEASE, NO E.O.	[illegible]	1-30-74	[illegible] 1-30-74

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Model No. First Use	Finish	Code Ident.	Size	Dwg. No.	Change Letter
7250		18338	A	204262	A
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INTRODUCTION

1-1 PURPOSE

This document provides a theory of operation for 7250 Cartridge Disk Controller (with Multiple Drive Selection Unit) for use by Xerox customer engineers and customer personnel responsible for installation, operation, and maintenance of the cartridge disk system. The material is intended for use in conjunction with the block, functional, and logic diagrams, as well as schematics, phase sequence charts, flow diagrams, and timing diagrams contained in the Engineering Technical Information, section III of the Field Engineering Maintenance Manual.

1-2 SCOPE

This document describes the operation of the controller and the multiple drive selection unit. It is divided into three major parts, as follows:

a. Equipment physical description, section 2 . O
b. General functional description, section 3 . O
c. Detailed functional description, section 4 . O

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SECTION 2.0

EQUIPMENT PHYSICAL DESCRIPTION

2-1 GENERAL

A cross-sectional view of the 7250 Cartridge Disk Controller equipment cabinet (figure 2-1) shows the locations of the controller and the multiple drive selection unit. The controller is a three-chassis logic unit, mounted in a swing frame assembly. Mounted on the swing frame assembly is a maintenance panel, which contains switches, lamps, and a test point that allows the controller to be operated offline from the system.

The multiple drive selection unit is a one-chassis logic unit mounted in a swing frame assembly beneath the power distribution panel at the front of the cabinet. Switches and lamps for the selection unit are located on two modules in the logic chassis.

2-2 CONTROLS AND INDICATORS

2-3 SUBCONTROLLER SWITCHES

Switches are located on three modules in the subcontroller and perform the following functions:

a. On-Line/Off-line Switch — This switch is located on the LT94 module in position 23c. The storage unit is off-line when the switch is down. With the switch down, the storage unit is under control of the MAINT/MONITOR switch on the maintenance panel.

b. Test Mode Switch — This switch is located on the LT95 module in position 22c and controls the subcontroller test module. The subcontroller is in the test mode with the switch down, and in the normal mode with the switch up.

c. Address Switches — These switches are located on the LT26 module in position 24c and are used to define the address of the controller in the computer system. Figure 2-2 illustrates the LT26 module and gives the relationship between the switches and the device address.

2-4 MAINTENANCE PANEL

The maintenance panel, mounted on the swing frame, provides a means of exercising a Cartridge Disk Drive file in an off-line mode, and of monitoring the operation of the Cartridge Disk Drive either while online or offline. The maintenance panel is intended for use by service personnel only, and is not required for normal operation of the Cartridge Disk Drive. The following controls and indicators are provided (see figure 2-3).

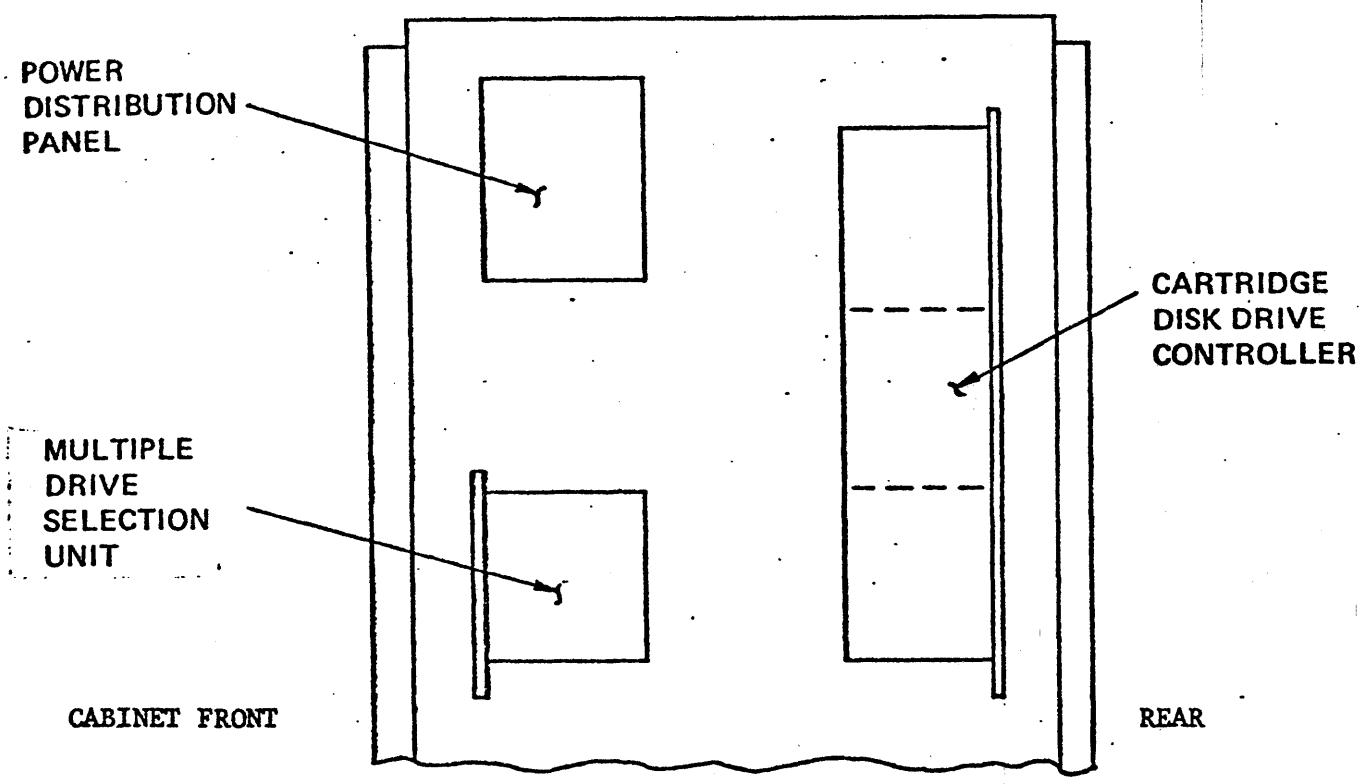

Figure 2-1. Cross Sectional View of Controller Cabinet

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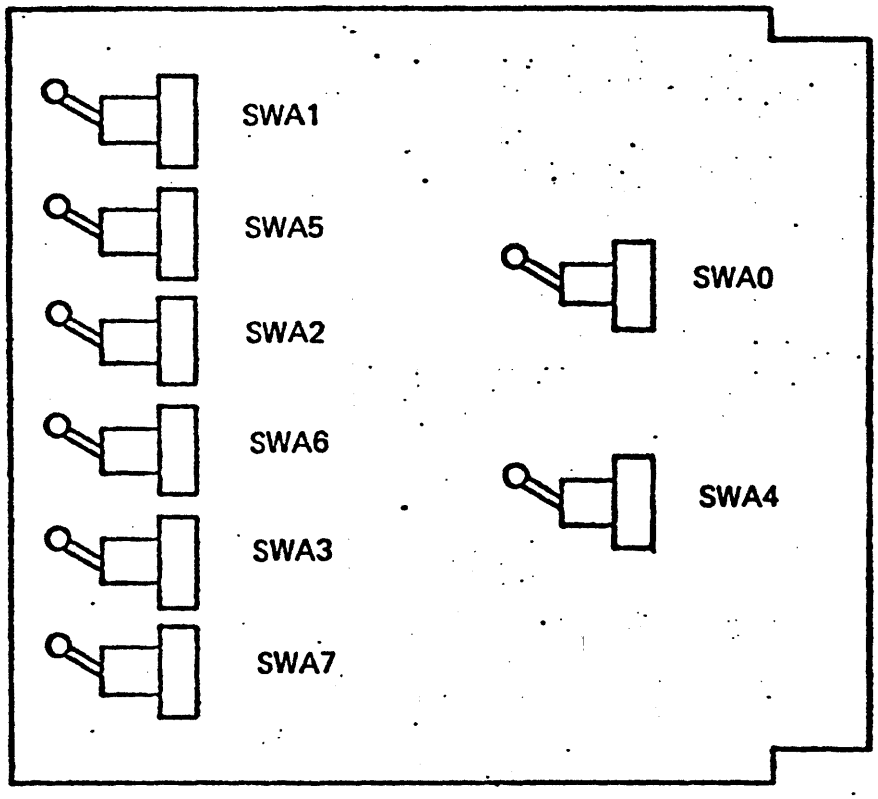

Figure 2-2. Address Switches – 24C (Controller)

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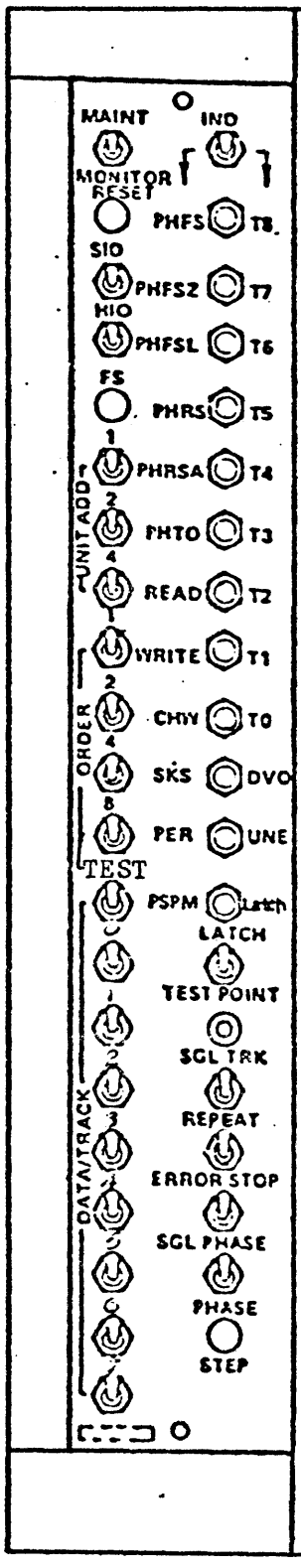

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Figure 2-3. Maintenance Panel

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a. MAINT/MONITOR Switch – Master Maintenance/Monitor Switch. In MAINT position, the maintenance panel provides signals necessary to record and read from the storage unit. In MONITOR position, the 12 indicators provide a means of monitoring IOP/controller operations. In MAINT position, controller will report not operational in response to a TDV instruction.

b. RESET Pushbutton – Provides a master reset signal to the controller.

c. SIO Switch – Function indicator.

d. HIO Switch – Function indicator.

e. FS Pushbutton – Function strobe signal. FS is used in conjunction with the SIO or HIO switch to initiate controller action.

f. UNIT ADD Switches – Unit address switches. Three switches used to select one of the eight storage units.

g. ORDER Switches – Switches which select the order to be executed. Write, Read, Checkwrite, Seek, Sense, or Testmode.

h. DATA/TRACK Switches – Eight switches which simulate eight bits of data or, during a Seek operation, select the track address desired.

i. IND Switch – Selects one of two sets of functions to be displayed on the indicators.

j. SGL TRK Switch – Provides a method for inhibiting the track register from incrementing, thus allowing any one track to be exercised. In the OFF position, the track register will continuously increment from track 0 to the highest track available.

k. REPEAT Switch – Allows continuous operation on one or all tracks as defined by the single track switch. In the off position, only one operation will be completed.

l. ERROR STOP Switch – The error stop switch halts the operation currently being executed upon receipt of a transmission error (parity error, checkwrite error, or sync pattern missed). The failing track is displayed and the sector counter is incremented by one from the failing sector.

m. SGL PHASE Switch – Used in conjunction with the phase step pushbutton to progress through an operation one phase at a time.

n. PHASE STEP Pushbutton – Single-phase clock. Describable under single-phase switch.

Indicators

IND (left)	Lamp	IND (right)
PHFS	1	TRACK 8
PHFSZ	2	TRACK 7
PHFSL	3	TRACK 6
PHRS	4	TRACK 5
PHRSA	5	TRACK 4
PHTO	6	TRACK 3
READ	7	TRACK 2
WRITE	8	TRACK 1
CHW (Checkwrite)	9	TRACK 0
SKS (Seek or Sense)	10	DVO (Device Operational)
PER (Parity Error)	11	UNE (Unusual End)
PSPM (Preamble Sync Pattern Missed)	12	LATCH

2-5 SELECTION UNIT

Indicators and switches for the selection unit are mounted on two modules located at 01A and 02A. These modules are shown in figures 2-4 and 2-5, respectively.

Indicators:

UNIT 1 - Unit 1 is being addressed or has had an error.

UNIT 2 - Unit 2 is being addressed or has had an error.

UNIT 3 - Unit 3 is being addressed or has had an error.

UNIT 4 - Unit 4 is being addressed or has had an error.

CARTRIDGE - Cartridge disk is being addressed; an even-numbered device address received from controller.

FIXED - Fixed disk is being addressed; an odd-numbered device address received from controller.

UPPER HEAD - Upper read/write head is being addressed; an even-numbered track address received from controller.

SELECTED FILE READY - Address is ready and has been selected.

SELECTED FILE READY S/R/W - The selected file is ready to perform a seek, read, or write operation.

LOGICAL ADDRESS INTERLOCK ERROR - Track address greater than 407 was received by the disk drive.

SEEK INCOMPLETE ERROR - Seek operation was not completed by the disk drive.

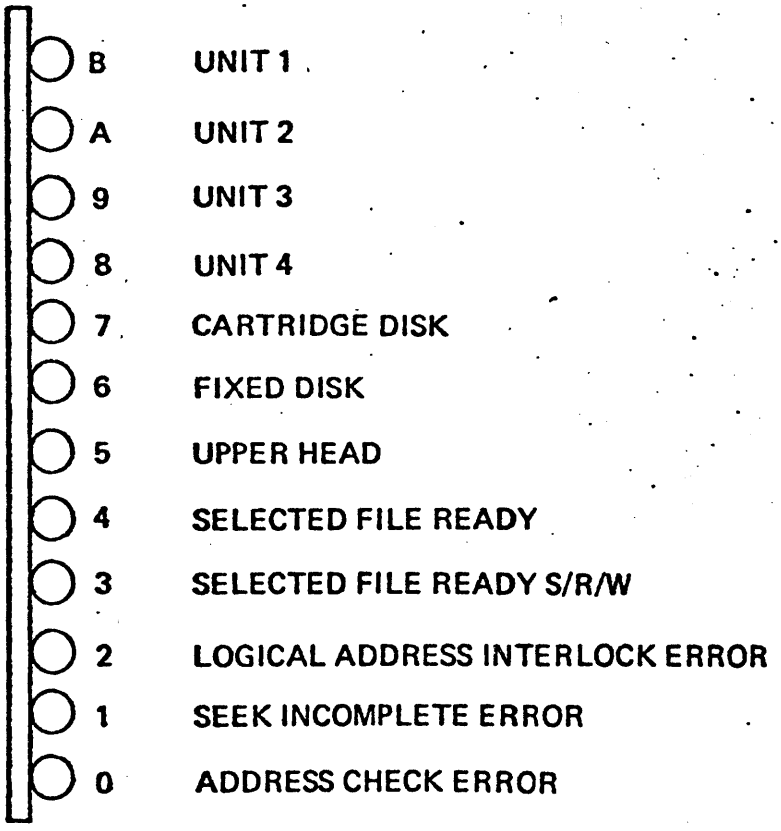

Figure 2-4. Indicator Lamp Card-01A (MDSU)

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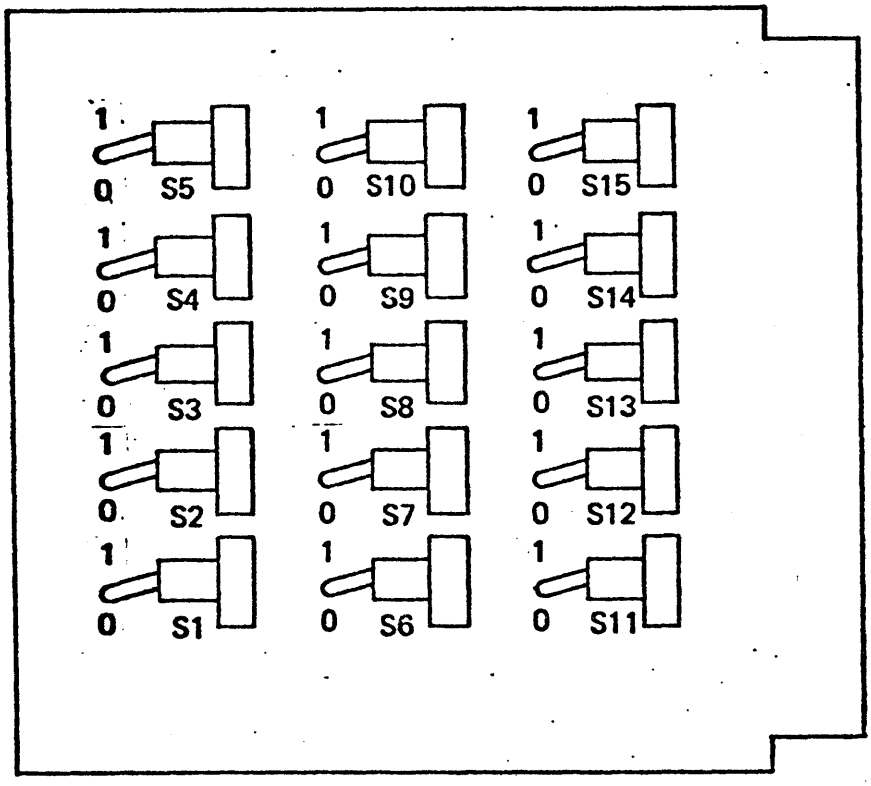

Figure 2-5. Switch Card-02A (MDSU)

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ADDRESS CHECK ERROR - Cylinder address read from the disk drive did not compare with that contained in track register TRK2 through TRK9.

Switches:

1 - VERIFY switch placed in the one position to verify the cylinder address read from the disk file.

2 - INITIALIZE switch placed in the one position to write cylinder addresses and sector marks on the disk. Normal operation and address verification requires this switch be in the zero position

3 - MANUAL RESET switch placed in the one position to reset the error and unit error flip-flops and extinguish the indicator lamps

4 - Address switch for Unit 1 cartridge disk

5 - Address switch for Unit 1 fixed disk

6 - Address switch for Unit 2 cartridge disk

7 - Address switch for Unit 2 fixed disk

8 - Address switch for Unit 3 cartridge disk

9 - Address switch for Unit 3 fixed disk

10 - Address switch for Unit 4 cartridge disk

11 - Address switch for Unit 4 fixed disk

2-6 POWER REQUIREMENTS

Power required by the cartridge disk storage system is 120 Vac ±10%, 60 Hz ±1%, single-phase power, 3-wire, 30A service. System power is supplied to the power distribution panel above the selection unit at the front of the controller cabinet. Power is distributed from here to the PT20 power supply within the controller cabinet and to the individual power supplies within each disk drive cabinet. These power supplies provide the drives with +24 Vdc, -24 Vdc, +5 Vdc.

SECTION 3.0

GENERAL FUNCTIONAL DESCRIPTION

3-1 GENERAL

The Cartridge Disk Controller Model 7250, establishes communication between the Input/Output Processor (IOP) and the cartridge disk storage unit. The controller receives data from the IOP on a parallel basis and may be one byte, two bytes, or four bytes. The data is then converted to bit serial format for transfer to a storage unit. Conversely, data is received from the storage unit on a bit serial basis and the controller converts it to a byte or bytes for parallel transfer to the IOP.

The controller is connected to the disk drives through the multiple drive selection unit which converts Cartridge Disk Drive control information to disk drive information. In addition, the selection unit generates the RESTORE command for the disk drives.

The Cartridge Disk Drive Controller and Multiple Drive Selection Unit may control up to four cartridge disk drives, models 7251 and 7252 (see figure 3-1). Terms frequently used within the text are defined in table 3-1.

3-2 I/O COMMUNICATION

The controller is capable of operating on a 1-byte, 2-byte, or 4-byte IOP interface depending on the option installed and incorporates the extended subcontroller in its design. To accomplish communication with the IOP and storage unit, the controller has four operating states: order-out, data-out, data-in, and order-in. These operating states are named as viewed from the IOP. The controller also has a ready or standby condition during which it is not communicating with the IOP. Thus, order-out implies that an order is being sent out of the IOP to the controller.

The order-out state is the state in which an order is transferred from the IOP to the controller. The order received may be a Read, Write, Checkwrite, Seek, Sense, or Test.

The data-out state is the state in which data is transferred from the IOP to the controller. Data-out orders are Write, Checkwrite, Seek and Test.

The data-in state is the state in which data is transferred from the controller to the IOP. Data-in orders are Read and Sense.

The order-in state is the state in which the controller reports errors or other terminal conditions to the IOP.

The normal quiescent state of the controller is the order-out state and the normal quiescent phase is PHFS. Thus, when power is first applied to the controller, it is in this state and phase.

After an order-out is completed and a new order is in the controller order register, the controller advances to a data-in or data-out state as determined by the order. Upon completion of the data transfer, the controller advances to the order-in state to report status of the last operation. After the status has been reported, the controller returns to the ready state.

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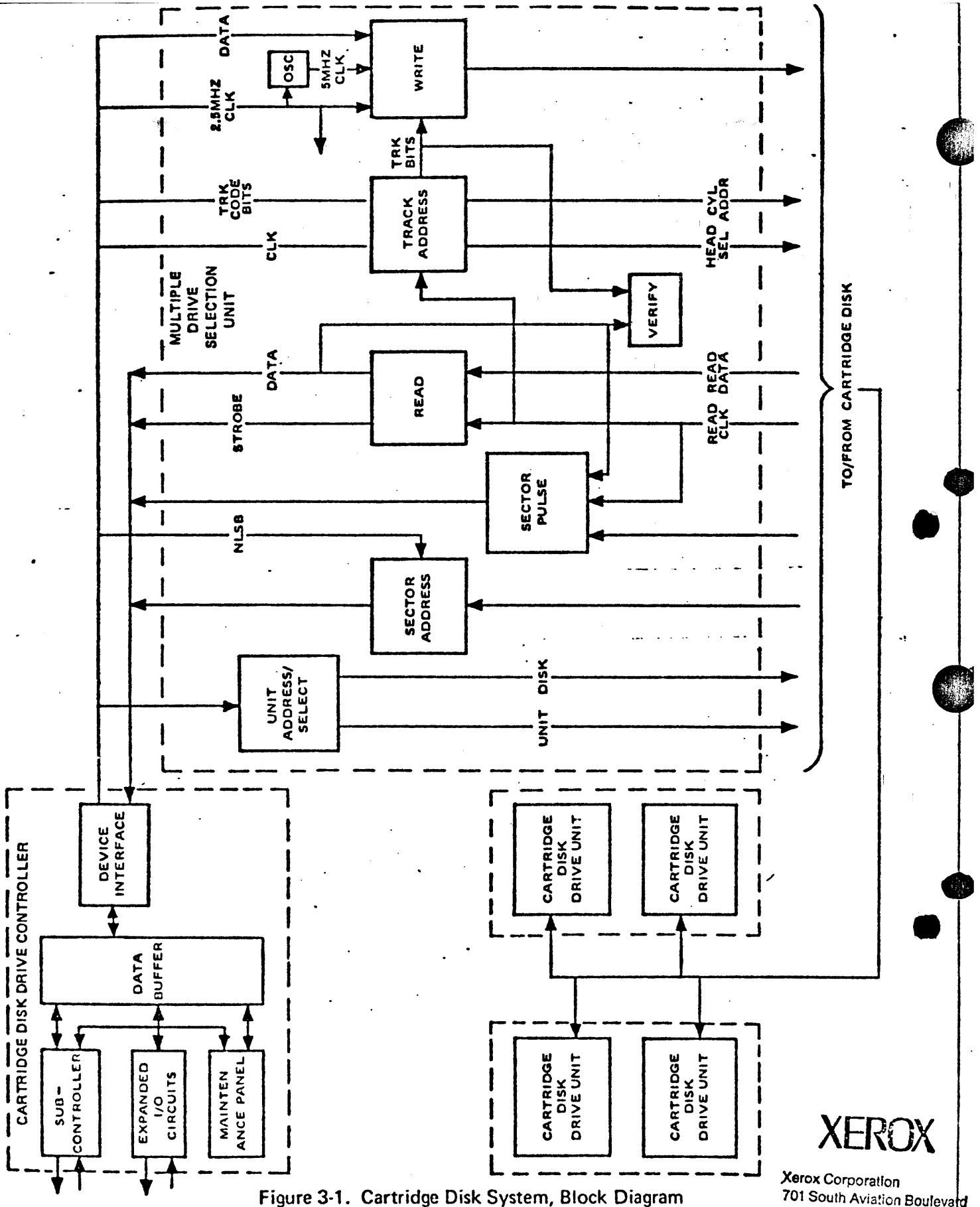

Figure 3-1. Cartridge Disk System, Block Diagram

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3-3 DATA TRANSFER AND STORAGE

Data transfers with the IOP are controlled by the IOP timing while data transfers with the storage unit are controlled by the storage unit timing. To efficiently handle the difference in the timing, the controller provides temporary storage for up to 16 bytes of data. The storage is provided by a 16-byte buffer referred to as the Fast Access Memory (FAM).

Data is stored on the disk surface (figure 3-2) in groups of data and each group is stored in a specific location (see figure 3-2). Each location has a unique address and is identified by its storage unit address, track address, and sector address (rotational position of the recording surface). The track address includes the cylinder address (head position) and the head selection (upper or lower surface). The units, tracks and sectors are organized in the system as follows:

Storage Unit	Model 7251	Model 7252
Storage units per system	1 to 4	1 to 4
Disks per storage unit	1 Cartridge	1 Cartridge and 1 Fixed
Tracks per disk	408	408
Sectors per track	16	16
Bytes per sector	360	360
Bits per byte	8	8
Bytes per storage unit	2.3 million	4.6 million

Each group of data is preceded by four bytes of synchronizing preamble and followed by one byte of parity. Each sector is separated from the next by a gap of 356.4 microseconds. Within this gap, one byte of cylinder address is written when the disk pack is initialized. This address is used to verify cylinder address after each seek operation. The total gap time allows command chaining to be performed between reading or writing each data group.

Table 3-1. Glossary of File Terms

Term	Definition
B counter (Byte counter)	Flip-flops B00 through B12 and POST. Counts bits and bytes during execution of a read order, write order, or checkwrite order.
CA, CB, CC and CD registers (C-register)	Input registers which are driven by the data lines from the IOP. The CA register is part of the 16-byte buffer. The CB, CC and CD registers are part of the extended interface.
Condition code	A two-bit code transmitted from the controller which indicates to the IOP the status of the file.

Table 3-1. Glossary of File Terms (Cont.)

Term	Definition
Data-in service cycle	A service cycle during which data bytes are transferred from the controller to the IOP.
Data-out service cycle	A service cycle during which data bytes are transferred from the IOP to the controller.
D-register	Flip-flops D00 through D07. Used during execution of a write order or a checkwrite order to transform the data format from parallel to serial. Used during execution of a read order to transform the data format from serial to parallel.
DA, DB, DC, and DD registers	Output registers which drive the data lines to the IOP. The DA register is part of the subcontroller. The DB, DC, and DD registers are part of the extended interface.
End Data signal	Signal /ED/. May be generated by either the IOP or the Cartridge Disk Drive controller. Causes an end to data transfer for the current service cycle.
End Service signal	Signal /ES/. Generated only by the IOP. Causes an end to the service cycle.
Extended Interface	A standard set of modules which form part of the controller and increase the data path width from one to two or four-byte parallel transfers.
FAM read cycle	A cycle of operation of the fast access memory (FAM) circuits, during which a byte is transferred from the addressed location in the FAM module to the K-register, or to the CB, CC, or DC registers for a wide interface operation.
FAM write cycle	A cycle of operation of the fast access memory (FAM) circuits, during which a byte is transferred from the J-register to the addressed location in the FAM module.
Function indicator	A signal that indicates the type of function (AIO, ASC, HIO, TIO, TDV, or SIO).
Function Response signals	Signals /FR0/ through /FR7/. Signals transmitted to the IOP in response to a function strobe (FS) and a function indicator signal (AIO, ASC, SIO, TDV, TIO, or HIO).

Table 3-1. Glossary of File Terms (Cont.)

Term	Definition
Function Strobe	Signal /FS/. Generated by the IOP to indicate that a response is required of a controller.
IOP byte signals	Signals /DA0/ through /DA7/, /DB0/ through /DB7/, /DC0/ through /DC7/, and /DD0/ through /DD7/. Transfer data between the controller and the IOP. Signals /DA0/ through /DA7/ are also used for exchange of orders, address, and status.
J-register	Buffered latches J00 through J07. Accepts data from the C-register or D-register for transfer to the FAM module, T-register and S-register.
K-register	Buffered latches K00 through K07. Accepts data from the FAM module for transfer to the DA register or D-register. During execution of a sense order, accepts data from the S-register and the T-register for transfer to the DA register.
Order code	An eight bit code indicating the type of order to be executed by the controller (read, write, checkwrite, seek, sense, or test).
Order-in service cycle	A service cycle during which status information is transmitted from the controller to the IOP.
Order-out service cycle	A service cycle during which an order code is accepted from the IOP.
Order register	Buffered latches ORD0 through ORD7. Stores the order code (seek, sense, read, write, checkwrite, or test) during execution of an order.
Phase control circuits	Flip-flops PHFS, PHFSZ, PHFSL, PHSRV and PHTO, and associated circuits. Establish phase of controller and respond to subcontroller outputs and internal timing and control signals.
P-register	Flip-flops P00 through P07. Used to generate checksum during execution of a read order, write order, or checkwrite order and to generate test data in testmode 2.
Request Strobe Acknowledge signal	Signal /RSA/. Generated by the IOP to indicate that a data exchange has taken place in response to an /RS/ signal.
Request Strobe signal	Signal /RS/. Generated within the controller to request a data transfer between the IOP and the controller.

Table 3-1. Glossary of File Terms (Cont.)

Term	Definition
R:K-counter	Flip-flops R:K0 through R:K4. Indicates the number of active bytes in the FAM module during execution of a read order, write order, or checkwrite order.
R:L-register	Buffered latches R:L0 through R:L3. Addresses the FAM module.
R:LR counter	Flip-flops R:LR0 through R:LR3. Tracks the read addresses for the FAM module. The count is transferred to the R:L-register to address the FAM module for a write cycle.
R:LW counter	Flip-flops R:LW0 through R:LW3. Tracks the write addresses for the FAM module. The count is transferred to the R:L-register to address the FAM module for a read cycle.
Sector address	A four-bit code which addresses one of the 16 sectors of each track.
Service Call signal	Signal /SC/. Generated by the controller when service is required for data transfer.
Service connect	A state of the controller in which data transfers between the IOP and the controller are enabled. SERVICON is set.
Service cycle code	A two-bit code indicating the type of service cycle requested by the controller.
S-register (counter)	Flip-flops SEC0 through SEC3. Stores sector address.
Subcontroller	A standard set of modules which form part of every device controller and which monitor and respond to IOP signals.
Terminal order	An optional byte of control information from the IOP appended to a service cycle, which indicates count done, interrupt, channel end, unusual end, or command chaining.
Track address	An 11-bit code which addresses one of 408 tracks on the surfaces of the disk cartridge. (Only nine of the 11 bits are used.)
T-register (counter)	Flip-flops TRK0VF through TRK8. Stores track address.
Unit address	A three-bit code which addresses one of the eight (maximum) storage units in a file.

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Table 3-1. Glossary of File Terms (Cont.)

Term	Definition
U-register	Flip-flops U0 through U2. Stores the address of the storage unit.
Wide interface	The extended interface option.
16-byte buffer	A standard set of modules which form part of the controller and provides buffer storage capability. The CA register, the FAM module, the J-register and K-register, and associated control counters and registers are part of the buffer.

3-4 CONTROLLER

The controller for the storage unit is only one of several device controllers exchanging data with the computer memory through the IOP. Two techniques are used to limit communication with the IOP to only one controller at any time. For some IOP commands, only one controller is addressed, and only the addressed controller can respond. For other IOP commands, a priority chain established by cable routing limits response to the highest priority controller awaiting that command. The subcontroller portion of the controller (figure 3-1) monitors signals from the IOP and determines if and how the controller responds to commands. The subcontroller responds to all control signals, either by passing the signals to other controllers associated with the computer installation or by returning signals to the IOP. The subcontroller controls exchange of data on the eight-bit data path. The expanded interface circuits provide up to 24 additional data lines when a 16-bit or 32-bit data path is used. When the storage unit is operating off-line, signals are received from the maintenance panel through the maintenance panel interface. Commands from the IOP cause phase control circuits of the controller to cycle through a definite sequence of phases. During each phase of the sequence, the phase control circuits respond to IOP signals, selection unit signals, and internally generated signals to determine when to go from one phase to another. During this sequence of phases, data is transferred between the selection unit and the IOP through the data buffer, the selection unit interface, and the subcontroller and expanded interface circuits.

3-5 IOP INTERFACE

The response of the subcontroller to IOP commands is summarized in figure 3-3. The five commands associated with CPU instructions are as follows:

Mnemonic	Function
AIO	Acknowledge input/output interrupt
HIO	Halt input/output operation
TDV	Test device
TIO	Test input/output
SIO	Start input/output

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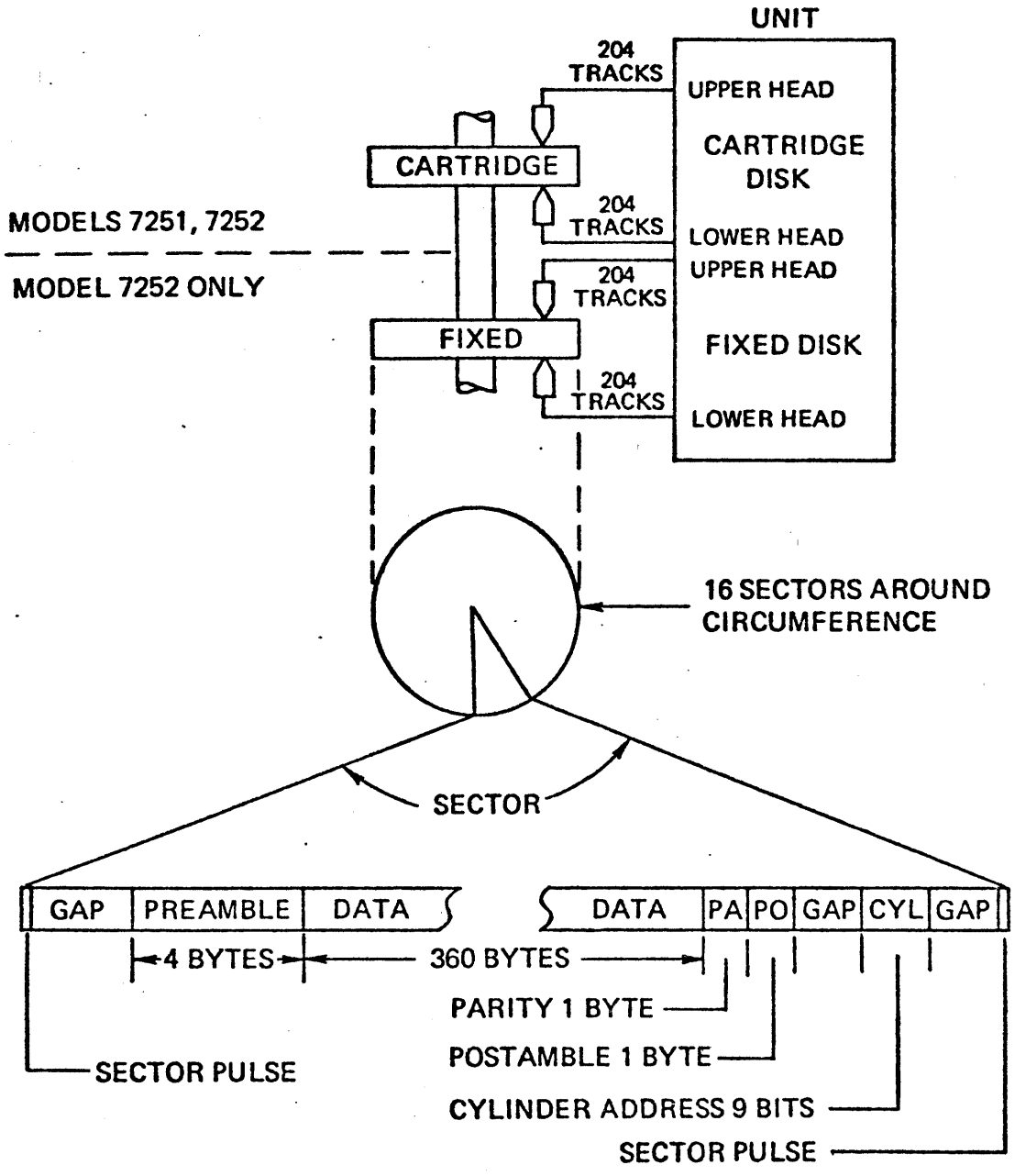

Figure 3-2. Cartridge Disk File, Data Organization

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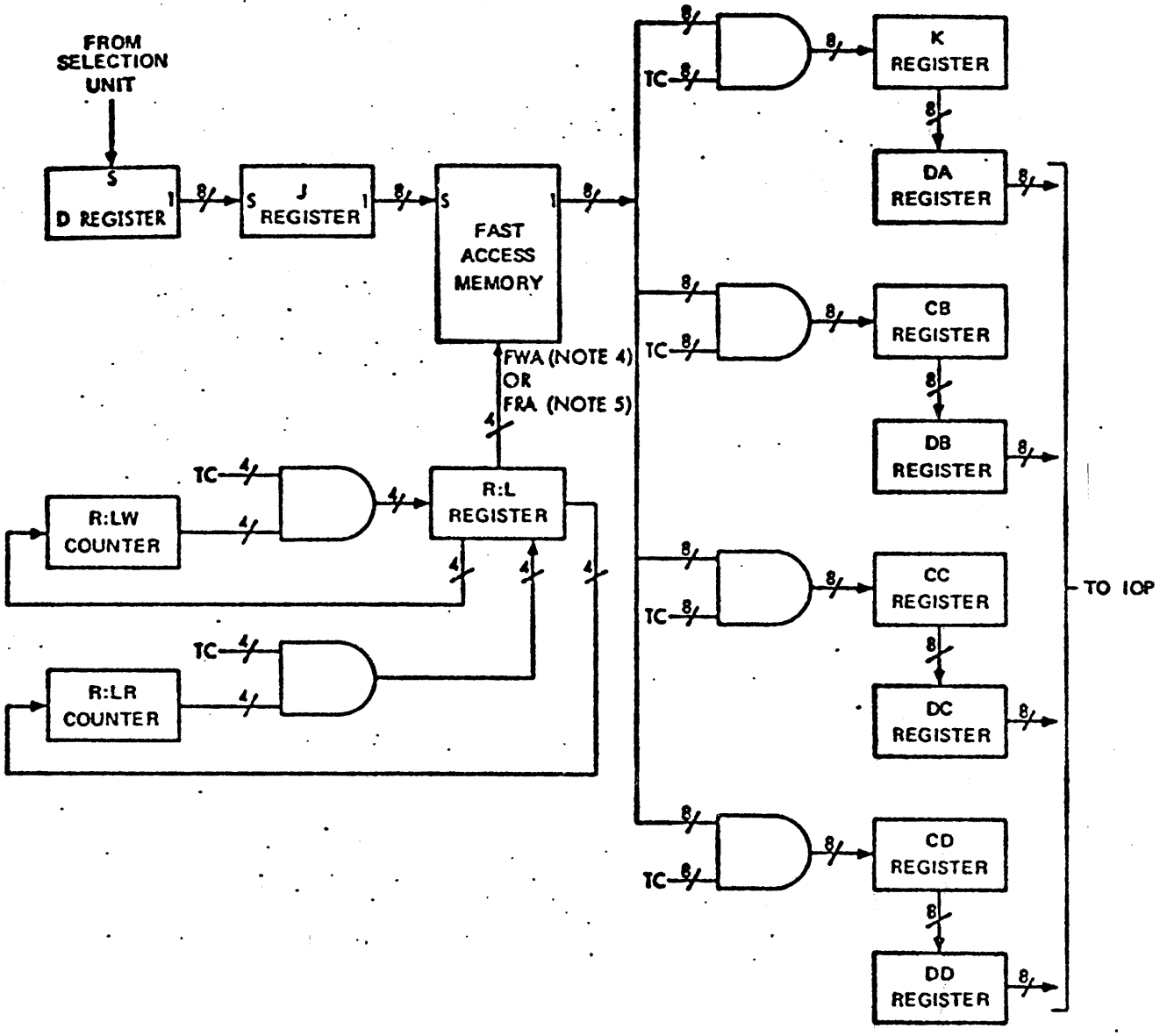

NOTES:

1. IOP DATA PATH MAY BE 8, 16, OR 32 BITS WIDE
2. R:LW COUNTER, R:LR COUNTER AND R:L REGISTER CONTROL
   ACCESS TO 16 REGISTERS IN FAST ACCESS MEMORY MODULE
3. INDICATED TIMING CONTROL SIGNALS (TC) ARE NOT IDENTICAL
4. FWA IS 4-BIT FAST MEMORY WRITE ADDRESS
5. FRA IS 4-BIT FAST MEMORY READ ADDRESS

Figure 3-3. Read Order Data Path, Block Diagram

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3-5 (cont'd)

The acknowledge service call (ASC) command is generated by the IOP in response to a service call from the subcontroller.

3-6 AIO Command

The AIO command, which is generated by the IOP when an interrupt is detected, is not addressed to any device or device controller. Only the highest priority device controller with an interrupt pending can respond to the AIO command. Any device controller that does not have an interrupt pending passes signals to the next device controller in the priority sequence. If the controller in the storage file is the highest priority device controller with an interrupt pending, it responds to the AIO command by transmitting its address and the contents of its device address register (U-register) to the IOP and by transmitting signals that indicate the cause of the interrupt. When an AIO command is accepted, the interrupt condition is cleared.

3-7 HIO Command

The HIO command, which is addressed to a specific device controller, halts an input/output operation and returns the function response signals and condition code signals to the IOP. These signals indicate the status of the controller to the IOP and to the CPU.

3-8 TDV Command

The TDV command, which is addressed to a specific device controller and device, returns function response signals and condition code signals to the IOP. These signals indicate any errors that occur during an input/output operation and the nature of the errors.

3-9 TIO Command

The TIO command, which is addressed to a specific device controller, returns function response signals and condition code signals to the IOP. These signals indicate the status of the controller to the IOP and to the CPU. The TIO command performs a function similar to that of the HIO command without causing a halt.

3-10 SIO Command

The SIO command, which is addressed to a specific device controller, returns function response signals and condition code signals to the IOP. These signals indicate the status of the controller to the IOP and to the CPU. In addition, the SIO command starts an input/output operation if the storage file is ready. The first response is to request an order-out service cycle from the IOP. During this service cycle, a code for one of seven orders (seek, sense, read I, read II, write, checkwrite, or test) is stored in the order register of the controller. A sequence of ASC commands in response to service calls from the controller then causes the order to be executed.

3-11 INTERNAL OPERATIONS

In response to an AIO, HIO, TIO, TDV, or SIO command from the IOP, the controller gathers data available in registers and flip-flops of the controller, or from signals available at the selection unit interface, and transmits the data to the IOP as function response signals or condition code signals. If an SIO command is accepted, the I/O operation that results depends upon the order received during the order-out service cycle. For each order, the IOP responds to a sequence of service calls from the controller by generating ASC commands. Each service call is identified by a two-bit code as requesting one of the four types of service cycles listed in table 3-2.

Regardless of the order received, a specific number of bytes are exchanged as the phase control circuits of the subcontroller cycle through a definite sequence of phases. If a seek order is stored, subsequent data-out service calls cause two bytes of data to be stored in controller registers. If a sense order is stored, subsequent data-in service calls cause three bytes of data to be transmitted to the IOP. If a write order is stored, subsequent data-out service calls cause data bytes in memory to be stored in the disk file of the addressed storage unit. If a read order is stored, subsequent data-in service calls cause data from the disk file of the addressed storage unit to be stored in memory. If a checkwrite order is stored, data accepted from memory is compared with data read from the disk file of the addressed storage unit.

Table 3-2. Service Cycle Operations

Service Cycle	Operation
Order-out	Control information is transmitted from the IOP to the controller. First service cycle of any input/output operation.
Order-in	Status information is transmitted from the controller to the IOP. Last service cycle of any input/output operation.
Data-out	Data is transmitted from the computer memory through the IOP to a disk file. Four bytes of data are transmitted during each service cycle; therefore, a rapid sequence of service cycles is required during execution of a write order or a checkwrite order. For a seek order, one data-out service cycle (transferring two bytes) is required.
Data-in	Data is transmitted from a disk file through the IOP to the computer memory. Four bytes of data are transmitted during each service cycle; therefore, a rapid sequence of service cycles is required during execution of a read order. For a sense order, one data-in service cycle is required.

3-12 Read

During a read order (figure 3-3), data is read from the storage unit and transferred to the IOP. When Read/Write Possible gets reset at byte 10 time, the clock (RWCK) is switched from the internal oscillator to the data strobe clock received from the storage unit. Data is read from the storage unit and shifted into the data register. When the data register contains eight bits of data, as indicated by BIT7RWE, the data is transferred in parallel to the J-register. This causes JFULL to be set and a FAM write cycle is started to store the data in FAM.

When four bytes of data are stored in FAM, SCR is set and a service call (CSL) is sent to the IOP. On a 1-byte interface, data is transferred from FAM to the K-register to the data output register (DA) to the IOP. For the 4-byte interface, data byte 1 is transferred from FAM to the K-register, data byte 2 from FAM to the CB register, data byte 3 from FAM to the CC register, and data byte 4 from FAM to the CD register. When the fourth byte is transferred to the CD register, ALLBYTES is generated and KFULL is set. The I/O delay line is started for PHRS and a request strobe (RS:D) is sent to the IOP. Sending RS:D allows the four bytes of data to be strobed into the output data registers; K to DA, CB to DB, CC to DC, and CD to DC. When request strobe acknowledge (RSA:R) is received, KFULL is reset, the registers are cleared, and data may be transferred from FAM again.

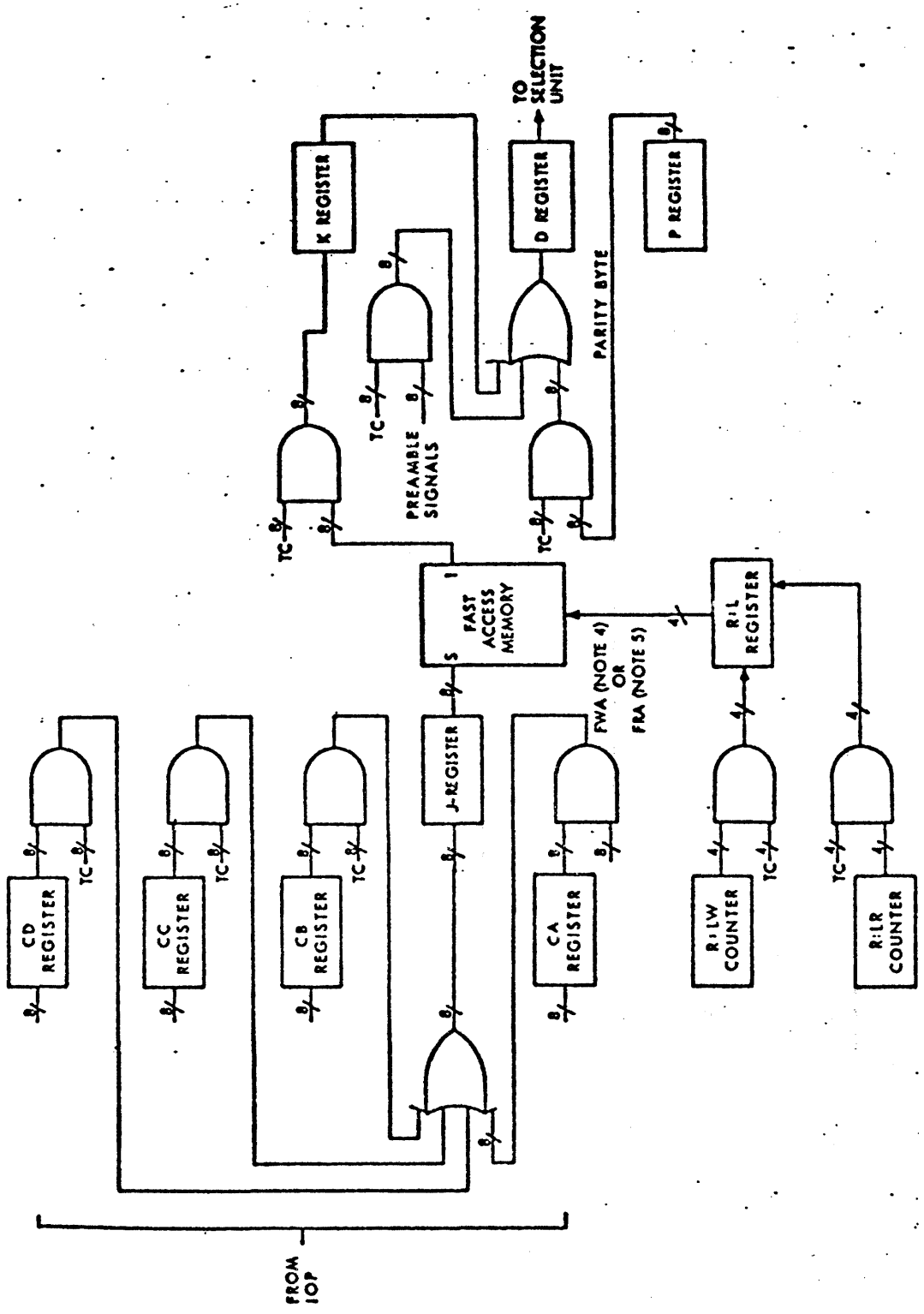
During a read operation, parity is formed on the data read from the storage unit. On the 360th byte, the POST state is entered and the parity formed during the read operation is compared with the parity actually written on the disk. If the parity bytes do not compare, the parity error flip-flop (PER) is set.

For read order X'12', parity errors are not reported until the IOP has signaled count done and the controller has entered the order-in state.

3-13 Write or Checkwrite

For a write or checkwrite operation (figure 3-4), data is received from the IOP and stored in the input CA register. If the 4-byte interface is installed, data will also be stored in the CB, CC, and CD registers. Data is transferred from the CA register directly into the J-register. For a checkwrite operation, the inverted side of the CA register is transferred. Data in the extension registers first goes through byte alignment logic and checkwrite inversion logic and then to the J-register. Byte present marker bits (BPB, BPC, and BPD) are set to indicate which byte is to be transferred. The marker bits strobe the data through the byte alignment logic C(BCD)0 through 7, through the checkwrite inversion logic C(BCD)0 through 7C, and into the J-register. When the first byte is stored in J-register, JFULL is set and the FAM delay line is started for a FAM write cycle. This in turn stores the data into FAM and resets JFULL after all the bytes have been stored.

When data is stored in FAM, one byte is removed and stored in the K-register. This byte remains there until the preamble has been written on the disk. At this time, the bit and byte counter are set to 664 and the contents of the K-register are transferred to the data register (D00 through D07). When the K-register data is transferred, KFULL is reset, the K-register is cleared (KXO), and another byte is transferred from FAM to the K-register.



NOTES:

1. IOP DATA PATH MAY BE 8, 16, OR 32 BITS WIDE
2. R:LW COUNTER, R:LR COUNTER AND R:L REGISTER CONTROL ACCESS TO 16 REGISTERS IN FAST ACCESS MEMORY MODULE
3. INDICATED TIMING CONTROL (TC) SIGNALS ARE NOT IDENTICAL
4. FWA IS 4-BIT FAST MEMORY WRITE ADDRESS
5. FRA IS 4-BIT FAST MEMORY READ ADDRESS

Figure 3-4. Write Order or Checkwrite Order Data Path, Block Diagram

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3-13 (cont'd)

Data is shifted out of the data register and sent to the storage unit. As the data is shifted from the data register, a parity byte is generated for each sector. On the 360th byte, the parity byte is transferred to the data register and sent to the storage unit.

The data path for a write and checkwrite operation is the same up to the output of the data register. For a write operation, the data from D07 is shifted to the storage unit. For a checkwrite operation, D07 is compared with the data returned from the storage unit. The data for a checkwrite operation was inverted by the checkwrite inversion logic before it was stored in FAM. Therefore, any comparison of data between DAR and D07 during a checkwrite operation is an error. If an error is detected, the CER flip-flop is set and transmission error is reported during the order-in cycle.

3-14 Seek

The seek order (Figure 3-5) causes the controller to expect two bytes of data from the IOP specifying the track and sector addresses. If the byte count is other than two, the controller signals incorrect length during the order in.

When the seek order is received from the IOP, the sector (SEC) and track (TRK) address registers are set to zero. During the data-out cycle, the seek data is transferred to the J-register. The FAM delay line is started and data from the J-register is transferred to the track and sector address registers as controlled by the seek/sense byte counter (S00 and S01). If the seek data indicates a nonexistent address, the controller terminates the sequence with an unusual end and the sector unavailable (SUN) status bit for the TDV is set. The seek data format and illegal addresses are shown below.

SEEK DATA FORMAT

	Byte 1								Byte 2							
DA	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
				TRACK									SECTOR			

Illegal Addresses: any address containing a 1 in bits 0, or 1, or 2 of byte 1

The track address is transmitted to the disk drive through the selection unit, following reception of a sector mark at any time the controller is busy, except during the data transfer of a seek order.

3-15 Sense

The sense order (figure 3-6) causes the controller to send three bytes of data to the IOP. The first two bytes contain the contents of the track and sector address registers and one bit defining the state of the write protect switch defined by that address. The third byte contains the current angular position of the addressed storage unit. Response to the sense order is held up until immediately following a sector pulse to prevent incorrect reporting of the current angular position. The sense data format is shown below.

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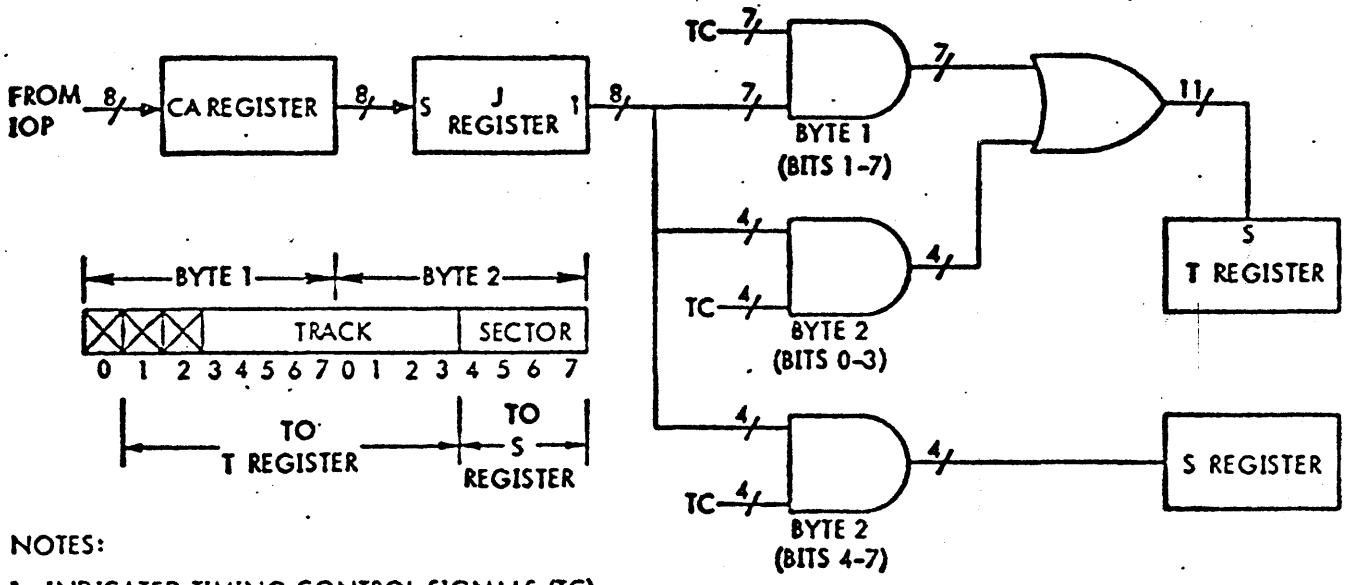

NOTES:

1. INDICATED TIMING CONTROL SIGNALS (TC) ARE NOT IDENTICAL
2. IF BITS 0-2 OF BYTE 1 ARE ONES, TRACK DOES NOT EXIST

Figure 3-5. Seek Order Data Path, Block Diagram

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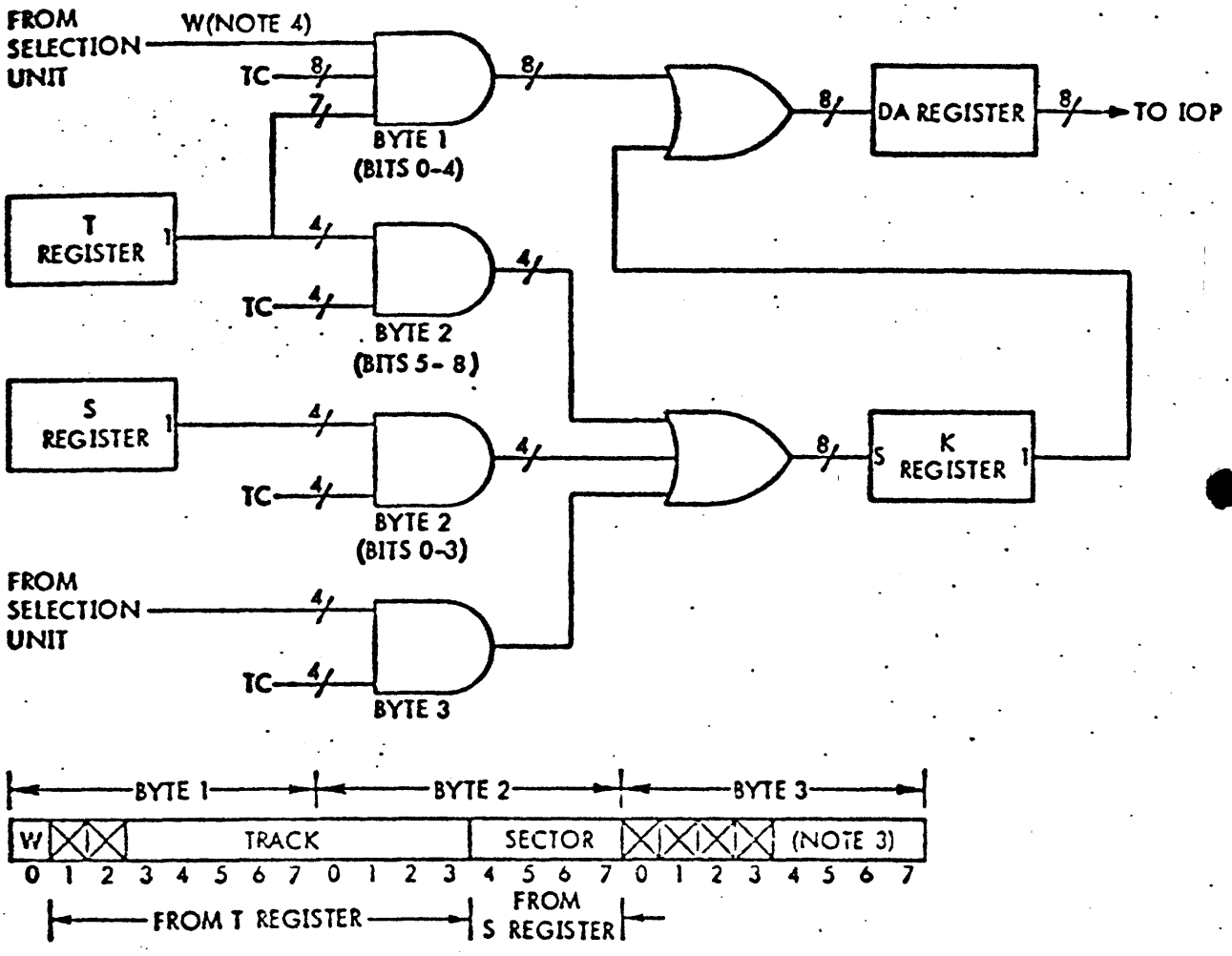

NOTES:

1. INDICATED TIMING CONTROL SIGNALS (TC) ARE NOT IDENTICAL
2. SELECTION UNIT PROVIDES 4 BITS, WHICH INDICATE CURRENT SECTOR AT READ/WRITE HEADS
3. SELECTION UNIT PROVIDES W BIT, WHICH INDICATES IF TRACK IS WRITE-PROTECTED (W = 1 IF WRITE-PROTECTED)

Figure 3-6. Sense Order Data Path, Block Diagram

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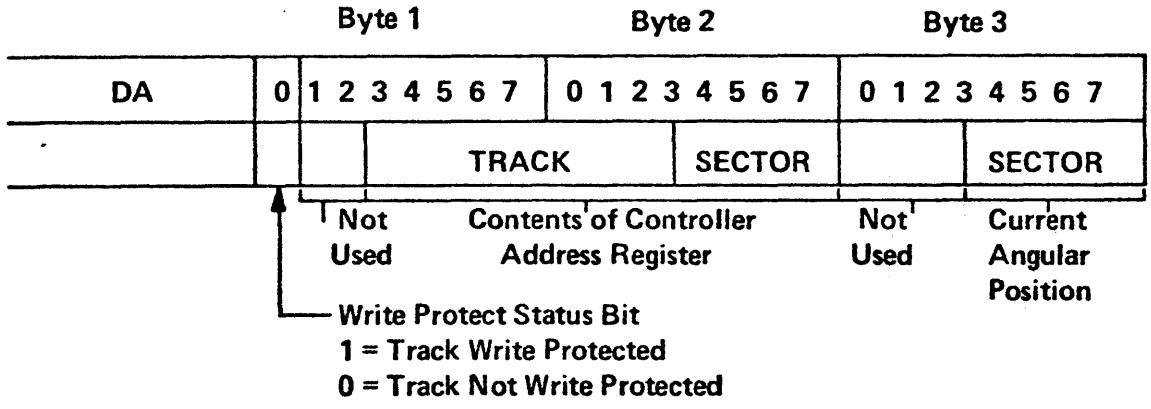
SENSE DATA FORMAT



3-16 Test

When test order X'13' is received by the controller during the order-out operation, one byte of data is requested on the following data-out operation. The data byte is decoded to determine the test mode and the TDV status response. After terminating the data-out operation, the order received in the following order-out operation is modified as determined by the testmode.

When testmode 1 is selected by data bit 7, data is transferred to or from FAM. Data is transferred to FAM on a write operation and from FAM on a read operation. During a write operation, service calls are made until the FAM contains 16 bytes as indicated by R:KO. R:SWRITE, which starts the FAM timing, is enabled by TM1; however, R:SREAD is inhibited during a write operation. The opposite is true for a read operation.

For a read operation, R:KO is preset to indicate there are 16 bytes of data in FAM. Service calls are made as in a normal read operation whenever the K-register is full.

Sector timing is inhibited at DXT time and data is not transferred to the storage unit.

When testmode 2 is selected, more of the logic is added to the test circuitry. During a testmode 2 write operation, data is transferred completely through the controller to the storage unit interface. Transfers to the storage unit are inhibited by the term NTESTING. Parity is formed as during a normal write operation. The parity clock is inhibited from the time parity is transferred to the data register (DXP) until another operation is started (PRE). At that time the parity register stores the parity byte that was generated. This allows the diagnostic program to check the contents of the parity register via testmode TDV. For a testmode 2 read or checkwrite operation, the parity register is used as a storage unit data simulator. For both operations, the preamble and preamble sync pattern are transferred to the parity register. The preamble is shifted through P07 and is fed into the normal data from disk path. The controller then recognizes the preamble sync pattern (PSPR) and performs the normal read or checkwrite operations. After the sync pattern is transferred, actual data is simulated by transferring the contents of the bit and byte counter into the parity register. This checks not only the read and checkwrite logic but also the bit and byte counter.

3-16 (cont'd)

If the modifier bit (MB) is also set during a testmode 2 read order, the parity error flip-flop (PER) is set and the error reporting logic of the controller is checked.

When the testmode selection is made, the TDV status response can also be selected. The status reponse is determined by latches TDVST1, TDVST2, and TDVST3. If none of the latches are set, the TDV status returned will be the normal controller status.

TDVST1 — Selects the output of the parity register

TDVST2 — Selects write enable as would be sent to the storage unit (WRTRWE), a signal indicating only the single interface is installed (NDX2+4), and track register bits 0 through 4

TDVST3 — Selects track register bits 5 through 8 and the sector register

Testmode and TDV status resets are accomplished by either transferring a byte of 0's from the IOP on the test order data byte or by a manual reset.

3-17 MULTIPLE DRIVE SELECTION UNIT

The multiple drive selection unit interfaces between the controller and the cartridge disk drives. It converts Cartridge Disk Drive control information into disk drive control information. The selection unit has five major functions:

a. Selects disk drive, converting device address into unit address and cartridge or fixed disk selection

b. Initiates the seek operation and verifies the seek

c. Encodes data for the disk drive

d. Decodes data from the disk drive

e. Initializes the disk cartridge for use

3-18 DISK DRIVE SELECTION

The three-bit device address from the controller is capable of selecting up to eight different drives. The three bits are further decoded within the selection unit to select one of four disk drive units and one of two disks within the selected unit. Only Model 7252 has two disks, a cartridge disk and a fixed disk. Model 7251 has only the cartridge disk.

The two most significant bits of the device address from the controller select the unit. The least significant bit will be true to select the fixed disk within the Model 7252 disk drive.

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Address switches (see paragraph 2-5) are provided for each disk within each disk drive. This permits disabling the decoding for drives or disks which are not present in the system.

Outputs from the selection unit to the devices are select lines NSELECT1 through NSELECT4 and DISKSEL. Only one of the NSELECTx lines may be low at one time. DISKSEL will be low to select the cartridge disk and high to select the fixed disk.

3-19 SEEK OPERATION

After the sector pulse has been received when the controller is busy (except during data-out of the seek order), a nine-bit track address is shifted out serially to a nine-bit register in the selection unit (TRK2 through TRK9 and HDSEL). The eight most significant bits of the track address are used as a cylinder address. The LSB is used to select the read/write head. When the LSB is a zero (even-numbered track addresses), the upper head is selected. When the LSB is a one, the lower head is selected.

The eight-bit cylinder address in TRK2 through TRK9 is sent to the selected device immediately after it has been shifted in from the controller. If this new address is different from the previous one, the disk drive initiates a seek operation to the new address.

At the conclusion of the seek operation, the selection unit will verify the seek address from the cylinder address recorded in the sector gap. Two checks are made in succession and if one (or both) is satisfactory, further operation may be performed. If both checks are not satisfactory, a RESTORE operation is initiated by the selection unit, and the ADDRESS CHECK ERROR indicator is lighted along with the unit number indicator.

The RESTORE operation will also be initated if the NSEEKING line is driven low by the disk unit, indicating that excessive current is required to move the carriage.

3-20 DATA ENCODING

Serial data is received from the controller at a 2.5 MHz rate. This provides a 400-nanosecond bit, or cell, time. The 2.5 MHz clock from the controller is doubled to 5.0 MHz within the selection unit to provide 200-nanosecond clock and data pulses to the disk drive. The data encoding method is double frequency.

The encoded data from the selection unit includes clock bits and data bits. Clock bits will occur continuously every 400 nanoseconds for as long as writing is enabled. A data one will inject a 100-nanosecond bit between two clock bits in the data stream.

3-21 DATA DECODING

The selected device provides the selection unit with both a read clock and a read data line. Pulse width on these lines is nominally 100 nanoseconds. The read data clocks occur every 400 nanoseconds and the read data pulses, indicating data ones, will occur between clock pulses.

The selection unit will provide the controller with data bits 400 nanoseconds wide and read data strobes of 120 nanoseconds every bit time.

3-22 DISK INITIALIZING

A disk cartridge is initialized by writing the cylinder address and an electrical sector mark in every sector of every track address on the pack. This can be done only with the INITIALIZE switch in the one position. Initializing may be done under program control, as described in the 725X Cartridge Disk Storage System Reference Manual, Publication Number 903024, or from the maintenance panel, as described in drawing 203328, Specification, Test and Acceptance, 7250 Controller.

During initialization, the mechanical sector marks from the device are used to generate sector marks for the selection unit and the controller. Controller sector timing starts at the trailing edge of the sector mark. When the controller write enable signal WEN goes low, at the end of the data record, zeros will begin to be written on the disk and a psuedo-sector counter in the selection unit starts counting. Sixty-four byte times after the fall of WEN, the eight-bit cylinder address is written following one synchronization bit.

Eight byte times after the following mechanical sector mark, the electrical sector mark is written. This electrical sector mark consists of four bytes of all data ones.

Writing of cylinder address and sector marks on this surface continues until a new track address appears in the controller. This will select the other head and cylinder addresses and sector marks will be written onto the other disk surface. The next new track address will select the other head and cause a seek to the next cylinder. Writing continues in this manner until the complete cartridge has been initialized.

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SECTION 4.0

DETAILED FUNCTIONAL DESCRIPTION

4-1 SCOPE AND ORGANIZATION

This section describes the operation of all circuits in the controller and selection unit, and is supported by the functional block diagrams, logic diagrams, flow charts, timing diagrams and logic equations. Individual circuits related to the transfer of data through the file are described in sequence from circuits functionally close to the IOP interface to circuits functionally close to the storage units. Cross references relate the circuit being described to circuits that provide inputs and accept outputs.

4-2 SUBCONTROLLER

The device controller (DC) includes a subcontroller which provides the following circuits:

a. Relay logic and switches for placing the DC on-line or off-line

b. Logic elements to determine priority of the DC

c. Cable drivers and cable receivers to connect the eight-bit data path interface

d. Switches for establishing the address of a DC and for providing a means of comparing the DC address generated by the IOP with the address of the DC

e. A latch that, when set, indicates the device is connected for service through the DC.

Not all possible functions of the subcontroller are used in the DC. Subcontroller functions used by this controller are described in paragraphs 4-3 through 4-25.

The subcontroller consists of the following modules incorporated in the controller to interface with the IOP:

Location	Type	Location	Type
C21	FT79	C28	AT57
C22	LT95	C29	LT 89
C23	LT94	C30	AT60
C24	LT26		
C26	AT83	C31	DT26
C27	LT90	C32	AT56

4-3 Function Strobe and Function Indicators

The subcontroller can respond to a function strobe signal /FS/ accompanied by one of the following function indicator signals:

Function Indicator	Function
/AIO/	Acknowledge interrupt call
/ASC/	Acknowledge service call
/HIO/	Halt input/output
/SIO/	Start input/output
/TDV/	Test device
/TIO/	Test input/output

The HIO, SIO, TDV, and TIO functions are always addressed to a specific DC, and only the subcontroller associated with the addressed DC can respond. The AIO and ASC functions are not addressed to a specific DC, and each subcontroller associated with an IOP receives the function strobe and function indicator in a priority sequence established by cable connections. If a subcontroller in a DC does not respond, the AIO or ASC function indicator enables the subcontroller of the next DC in the priority sequence to respond. If the subcontroller does respond, it acknowledges the function strobe and generates function response signals, condition code signals, and other signals related to the function.

The HIO, SIO, TDV, and TIO function indicator signals are generated when the CPU processes an instruction. The AIO function indicator signal is generated in response to an interrupt call by a DC.

The ASC function indicator signal is generated in response to a service call by a DC.

4-4 IOP Data Line Signals

The IOP data line signals consist of DA0:R through DA7:R which may contain an address status, terminal order information, or orders.

Signals DA0:R through DA3:R are compared with the settings of the switches on the LT26 switch comparator module to generate device controller addressed signal DCA.

Table 4-1. Information in Function Response Signals for TIO, HIO, or SIO Command

INFORMATION	FUNCTION RESPONSE SIGNALS							
	FR0D	FR1D	FR2D	FR3D	FR4D	FR5D	FR6D	FR7D
Interrupt pending	1	X	X	X	X	X	X	0
Device automatic	X	X	X	1	X	X	X	0
Unusual end	X	X	X	X	1	X	X	0
Device ready	X	0	0	X	X	X	X	0
Device busy	X	1	1	X	X	X	X	0
Disk storage unit not operational	X	0	1	X	X	X	X	0
Controller ready	X	X	X	X	X	0	0	0
Controller busy	X	X	X	X	X	1	1	0

Note

An X under a signal indicates that the signal is not related to that information.

If any pair of corresponding bits of the DAn:R inputs and the SWA inputs (where n represents any integer from 0 to 3) are different, signal DCA is false; therefore, signal DCA is true when the IOP data line code is identical to the address code set in the switches, indicating that the device controller is addressed.

Signals DA5:R through DA7:R contain the device address code and control signals SU0D through SU2D.

For terminal orders, signals DA0:R through DA3:R indicate interrupt, count done, command chaining, or IOP halt, as described in detail in paragraph 4-22.

4-5 Priority Signals

Signals /HPI/, /HPS/, /AVI/, and /AVO/ control priority when the controller is on-line. The IOP generates an /AVI/ signal that is always true. This signal goes to the highest priority device controller at all times. When the IOP generates a true function strobe signal (FS), each DC, beginning with the highest priority DC, responds to the /AVI/ signal in priority sequence. If a DC does not generate a function strobe acknowledge signal, the DC passes the /AVI/ signal on to the next DC in sequence in the form of a true /AVO/ signal.

4-5 (cont'd)

In the controller, a true /AVO/ signal is generated in one of three ways:

a. When an AIO is received with no interrupt pending

b. When an ASC is received with no service call pending

c. When a TDV, TIO, HIO, or SIO is received without an address recognition occurring in the subcontroller

4-6 Subcontroller Response

When the subcontroller does not generate a true /AVO/ signal, it generates a true function strobe acknowledge (FSL) signal, regardless of the type of function.

After generating the function strobe acknowledge signal, the subcontroller generates additional signals that depend on the function being performed. The signals include the function response signals, condition code signals, service cycle identification signals, and request strobe signals. These signals are used by the IOP to determine the type of response required. Paragraphs 4-7 through 4-12 group these signals for each type of function indicator.

4-7 TDV Function Indicator

For a TDV function, the function response signals /FR0/, /FR2/, /FR3/, and /FR4/ contain information while the other function response signals are always false.

/FR0/	is true if a rate error is detected (RER)
/FR2/	is true if the sector is unavailable (SUN)
/FR3/	is true for a write protect violation (WPV)
/FR4/	is true if the preamble sync pattern was missed

The conditions for which flip-flops RER, SUN and WPV are set are described in paragraphs 4-54, 4-55, and 4-61.

Condition code signals (/DOR/, /IOR/) will be true under the following conditions:

DOR when the device and controller are operational

IOR when the controller is not in a test condition

4-8 TIO Function Indicator

For a TIO function, the function response signals will contain information as listed in table 4-1.

The condition code signals (DOR, IOR) will be true under the following conditions:

DOR when the device is operational (OPER)

IOR when the device and controller are READY

4-9 HIO Function Indicator

For an HIO function, the function response signals will contain the information as listed in table 4-1.

The condition code signals will be true under the following conditions:

DOR when the device is operational (OPER)

IOR when the device is not busy (NDVBUSY)

4-10 SIO Function Indicator

For an SIO function, the function response signals will contain the information as listed in table 4-1.

The condition code signals will be true under the following conditions:

DOR when the device is operational (OPER)

IOR when the device and controller are READY

The possible condition codes and their meanings are:

DOR	IOR	Meaning
0	0	Device not operational
1	0	Interrupt pending, device busy, or controller busy
1	1	SIO accepted

4-11 AIO Function Indicator

For an AIO function, the controller places its address on the function response lines /FR0/ through /FR3/. The unit address stored in the unit register (U0 through U2) is placed on function response lines /FR5/ through /FR7/. Function response line /FR4/ will be false.

The condition code (DOR, IOR) is (1,1) only for the subcontroller having the highest priority and a pending interrupt.

A condition code (DOR, IOR) of (1,0) indicates a fault condition (UNE set) in the controller responding to the AIO command.

In addition to function response signals and condition code signals, status signals are generated and transmitted through signals /DA0/, /DA2/, and /DA3/.

DA0	rate error (RER)
DA2	sector unavailable (SUN)
DA3	write protect violate (WPV)

4-12 ASC Function Indicator

The ASC function indicator is an IOP response to a service call from the controller and can occur only after an SIO command has been accepted, causing service call latch CSL to be set by NDATA NIN. This will cause the service call signal /SC/ to be raised.

Service calls are a part of the execution of the seek order, sense order, write order, read order, and checkwrite order. For an ASC function, the function response signals contain the same information as for the AIO function (paragraph 4-11).

The ASC function indicator will cause the subcontroller to enter the service phase (PHSRV) and thus cause the service connect latch (SERVICON) to be set.

While the controller is connected for service, the (DOR, IOR) signals generate one of four service cycle identification codes controlled by the states of flip-flops DATA and IN.

The possible service cycle identification codes are:

(DATA/IN)		(DOR, IOR)		Service Cycle
0	0	1	1	Order-out
0	1	1	0	Order-in
1	0	0	1	Data-out
1	1	0	0	Data-in

While the service connect latch (SERVICON) is set, request strobes (/RS/) may be sent to the IOP as determined by the phase control circuits.

4-13 Phase Control Circuits

The phase control circuits control the response of the controller to IOP commands (AIO, HIO, TIO, TDV, or SIO). In response to IOP commands, the phase flip-flops cycle through a sequence of three phases (PHFS, PHFSZ and PHFSL), during which the function response signals and condition code signals are returned to the IOP. In response to an accepted SIO command, the controller requests an order-out service cycle and executes the order received. For a seek order, write order, test order, or checkwrite order, execution of the order involves one or more data-out service cycles followed by an order-in service cycle. For a sense order or a read order, execution of the order involves one or more data-in service cycles followed by an order-in service cycle. During each service cycle, the phase flip-flops cycle through two phases (PHFS and PHSRV) reporting subphases PHRS and PHRSA as required to transfer data. The phase control circuits control the timing of the phases, identify the service cycle, and provide signals for use by other circuits of the controller.

4-14 I/O Phase Delay Line

Clock signals for the subcontroller are generated by a 200-nanosecond delay line on the DT26 module. The line is driven by a buffered latch which is normally in the set state (NT000).

When the delay line is not in use and no pulse is present, the NTCYCLE latch will be reset. Resetting NT000 will cause a pulse to be propagated down the delay line. At the T100 tap, the pulse sets NTCYCLE and NT000. This will limit the pulse to approximately 120 nanoseconds.

The PHCLK buffer is set by T100. The output is tied to NT200 so that when the pulse arrives at this latter tap clock term PHCLK is quickly cut off. The trailing edge of PHCLK is the clock for the DATA, IN, and DCBUSY flip-flops as well as the subcontroller phase flip-flops.

NTCYCLE will be held set until the pulse has disappeared completely from the delay line. While this latch is set, NT000 cannot be reset to start another timing pulse through the delay line.

A clock pulse normally traverses the full 200-nanosecond length of the delay line. To speed up the data-in and data-out cycles, the signal NTSTOP prevents the line from running past the 100-nanosecond tap during subphase PHRSA. This decreases the time from receiving a request strobe acknowledge (RSA) until the time that the next request strobe (RS) may be raised. Note that the TSTOP latch is not effective during the last PHRSA of an input operation when end service (ES) is true. This allows the subcontroller to generate PHCLK without returning to PHRS to do so.

Timing is shown in figure 4-1.

4-15 Phase Flip-Flops

Phase flip-flops PHFS, PHFSZ, PHFSL, PHSRV, and PHTO, and phase latches PHRS and PHRSA, which control inputs to the I/O phase delay line, cycle through a sequence of phases determined by the commands and orders received from the IOP. All phase flip-flops are clocked by PHCLK, which goes true at T100 and goes false at T200.

A reset signal received from the computer through the IOP, or a reset signal from the maintenance panel, will generate the term RESETMANL. This will reset all phase flip-flops except PHFS, which will be set. This is the initial condition and the idle phase for the subcontroller.

Table 4-2 identifies the phase flip-flops and latches.

4-16 Response to I/O Instructions

The sequence of phases in response to an IOP command (TDV, TIO, SIO, HIO, or AIO) is independent of the function indicator. A function indicator and its associated function strobe (FS) will start the I/O phase delay line when an addressed TDV, TIO, SIO, or HIO command is received or when an AIO is received and the controller has an interrupt pending. The signal which starts the delay line is TTSHAIOC.

Operational flip-flop OPER is immediately reset by PHFS and clock NT000.

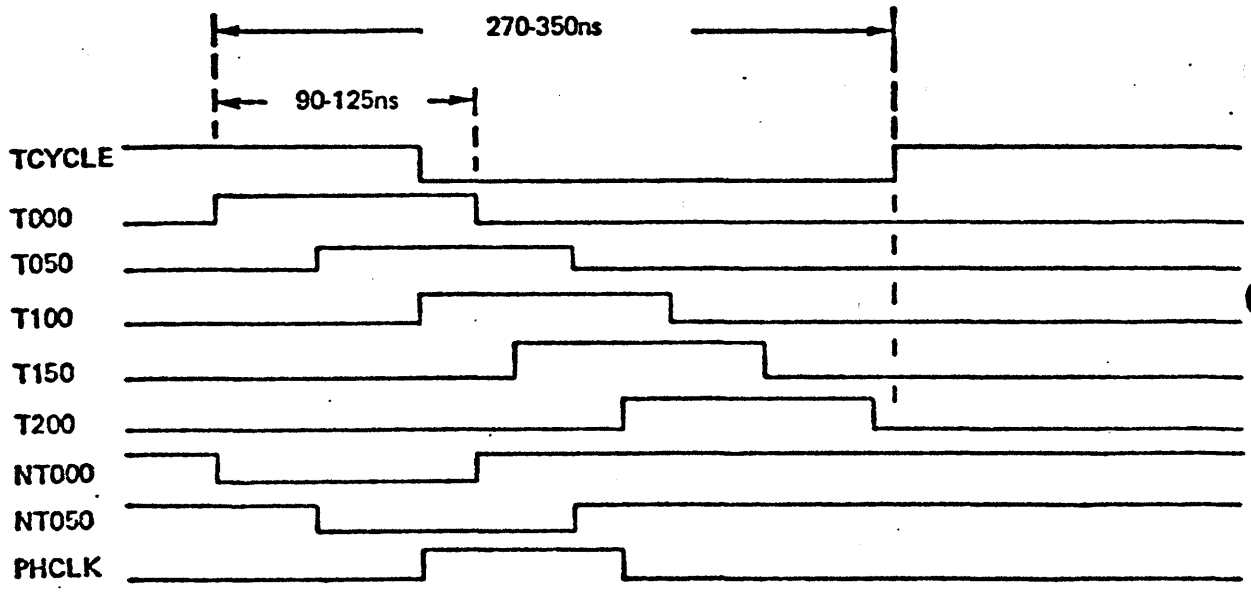

Figure 4-1. Subcontroller Timing Generator

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Table 4-2. Subcontroller Phases

PHASE	IMPLEMENTATION	PURPOSE
PHFS	Flip-flop	(a) Service calls or interrupt calls are raised in PHFS. (b) Function strobe is detected while in PHFS. (c) Subcontroller is in PHFS when idle.
PHFSZ	Flip-flop	A time delay between PHFS and PHFSL.
PHFSL	Flip-flop	The phase in which the function strobe acknowledge signal, /FSL/, is sent to the IOP for the five I/O instructions: SIO, TIO, TDV, HIO, and AIO.
PHSRV	Flip-flop	The phase during which the subcontroller is connected for service with the IOP. PHSRV is divided in subphases by latches PHRS and PHRSA.
PHRS	Buffered latch	The subphase of PHSRV during which a request strobe, /RS/, may be sent to the IOP.
PHRSA	Buffered latch	The subphase of PHSRV during which the subcontroller waits for the request strobe acknowledge, /RSA/, from the IOP (except for terminal orders).
PHTO	Flip-flop	The terminal order phase PHTO is entered from PHSRV after a request strobe has been raised for a terminal order.

Transfer from phase PHFS to phase FSZ occurs at T200 and the delay line is started again by PHFSZ when NTCYCLE resets.

The operational flip-flop OPER samples the device test signal DVTR and is clocked by NT000.

At T200, PHFSZ is reset and PHFSL is set. While in phase PHFSL, function response signals, condition code signals, and device controller addresses are transmitted to the IOP as described in paragraphs 4-7 through 4-12. The acknowledge signal, /FSL/, is raised and the subcontroller waits in PHFSL until the IOP drops /FS/.

If an SIO function is being executed, the device controller busy flip-flop, DCBUSY, is set at the end of PHFSL and a service call is made to the IOP for an order-out. Both these actions occur only if the controller is operational, is not already busy, and does not have an interrupt pending.

An HIO function resets the DCBUSY flip-flop and clears the unusual end and interrupt call latches.

4-16 (cont'd)
The I/O phase delay line is started in phase PHFSL when the function strobe signal, /FS/, goes false. At T200, PHFSL is reset and PHFS is set.

4-17 ASC Function

The sequence of events comprising an ASC function normally includes:

a. A service call, /SC/, raised by the controller

b. The acknowledge service call, /ASC/, and function strobe, /FS/, raised by the IOP

c. The subcontroller advancing from PHFS to PHSRV and setting the service connect flip-flop, SERVICON

The phase sequence for ASC is initiated when a service call is made by the subcontroller for the purpose of doing an order-out, order-in, data-out, or data-in operation. The service call latch, CSL, is set and the /SC/ line to the IOP is raised.

The IOP responds by raising /ASC/ and /FS/. The I/O phase delay line is started by ASCB and the subcontroller advances from PHFS to PHFSZ. The delay line is restarted in PHFSZ and the subcontroller advances to PHSRV. During PHSRV the function strobe acknowledge signal, /FSL/, is raised. When the IOP drops the function strobe, the service connect latch, SERVICON, is set. This in turn causes the PHRS latch to be set and the service call latch, CSL, to be reset.

After making a service call and being connected for service, the subcontroller may execute any of four types of service cycles. The type of service required is specified by two flip-flops, DATA and IN, in the subcontroller. These flip-flops drive the /DOR/ and /IOR/ lines as described in paragraph 4-12.

While in the service phase, PHSRV, request strobes may be issued to the IOP. One request strobe is generated each time the I/O phase delay line is started during subphase PHRS (unless end service latch ES is set).

The order-out and order-in cycles consist of the transfer of a single byte of data, plus possibly a terminal order byte (see paragraph 4-22). The data-out and data-in cycles consist of one or more data byte transfers and, again, the sequence may conclude with a terminal order.

Service cycles are terminated when the subcontroller, the controller, or the IOP causes end data, ED, to be set. If ES is also set during the order or data transfer, no terminal order is necessary and the subcontroller returns to PHFS without going through PHTO.

4-18 Order-Out

An order-out is one of the four basic types of service cycles performed by the subcontroller. Its purpose is to transfer an order from the IOP to the device controller. The order-out occurs following an SIO function or as the result of a command chain.

After an SIO has been successfully completed (DCBUSY is set), the subcontroller goes to the order-out state and makes a service call. The sequence proceeds as shown in figure 4-2 with little intervention from

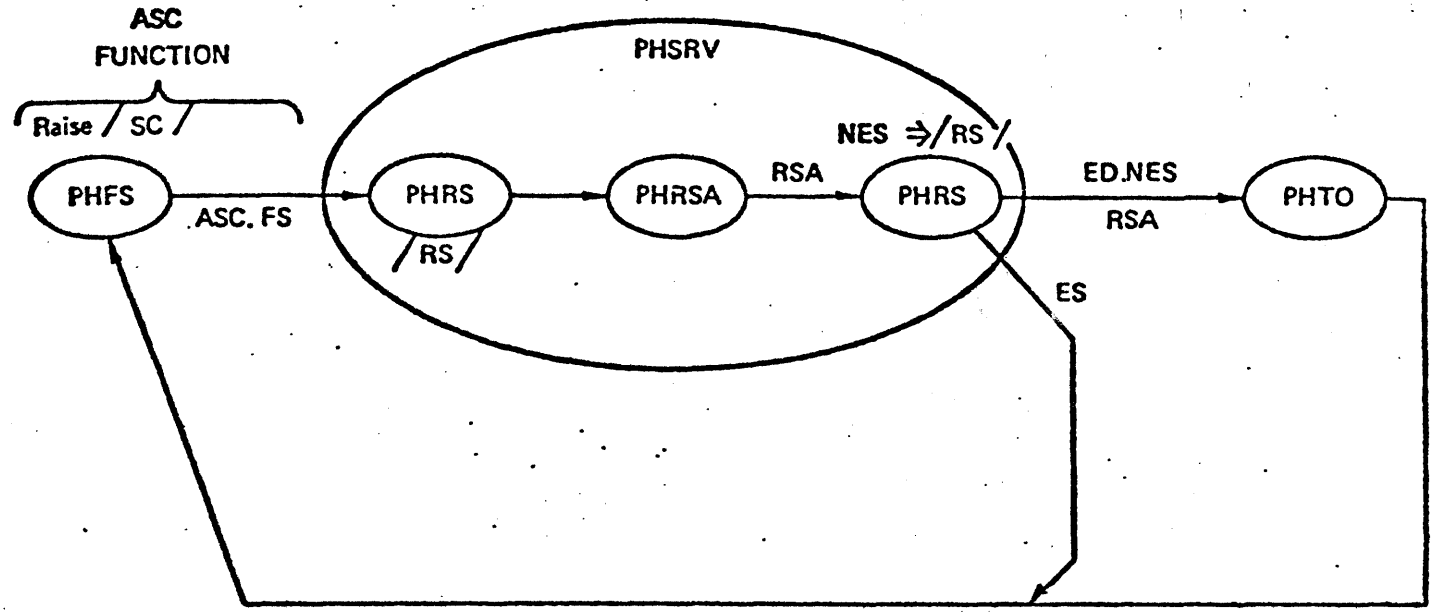

Figure 4-2. Order-Out Phase Sequence

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the controller, except to start the timing delay line during phase PHRS. The controller accomplishes this through signal TSTART (PHRS).

Starting the delay line for PHRS causes a request strobe to be sent to the IOP and allows the subcontroller to advance to PHRSA. When the request strobe acknowledge signal is received, the accompanying order is stored in the order register. It remains there until it is replaced by another order during the next order-out.

A terminal order (see paragraph 4-22) may or may not be required after the order is obtained. If /ES/ is not received when the IOP acknowledges the request strobe for the order, a terminal order is necessary. In this case the controller must again start the timing delay line with TSTART (PHRS). If /ES/ is received with the order, a terminal order is not necessary and the subcontroller returns to PHFS.

4-19 Order-In

An order-in is one of the four basic types of service cycles performed by the subcontroller. It allows the subcontroller to report error or other terminal conditions (such as channel end) to the IOP. An order-in occurs as a result of setting the unusual end latch, UNE, or the finished flip-flop, FINISH. The subcontroller terminates any data operations taking place by signaling /ED/ to the IOP, and then makes a service call by raising CSL/M(OI).

The phase sequence for the order-in is shown in figure 4-3. It begins with the service connection being made by the ASC function.

As with the other types of service cycles, a terminal order may or may not be required afterwards. Again, this is under control of the IOP which indicates the requirement by raising /ED/ and holding /ES/ false during the request strobe acknowledgement. The controller must, in all cases, provide the line starting signal, TSTART (PHRS), during phase PHRS.

4-20 Data-Out

Data-out is one of the four basic types of service cycles performed by the subcontroller. It provides the means for an output device to obtain the data from the IOP. The data-out state may follow an order-out or a prior data-out cycle. After an order-out, it is up to the controller to decode the order, check its validity and, if output (ORD7), enter the data-out state.

Data-out proceeds as shown in figure 4-4. It begins when the controller raises CSL/M(DATA) to make a service call. The ASC operation then results in the service connection with PHSRV and SERVICON being set. The subcontroller remains in PHSRV where it can cycle between subphases PHRS and PHRSA, transferring data bytes until the end data latch, ED, is set. ED may be set either by the controller or by /ED/ from the IOP.

The data-out sequence is concluded with a terminal order if the IOP raises /ED/ but not /ES/ when acknowledging a request strobe. The controller must provide the delay line starting signal for each PHRS whether a request strobe is being raised for data or the terminal order.

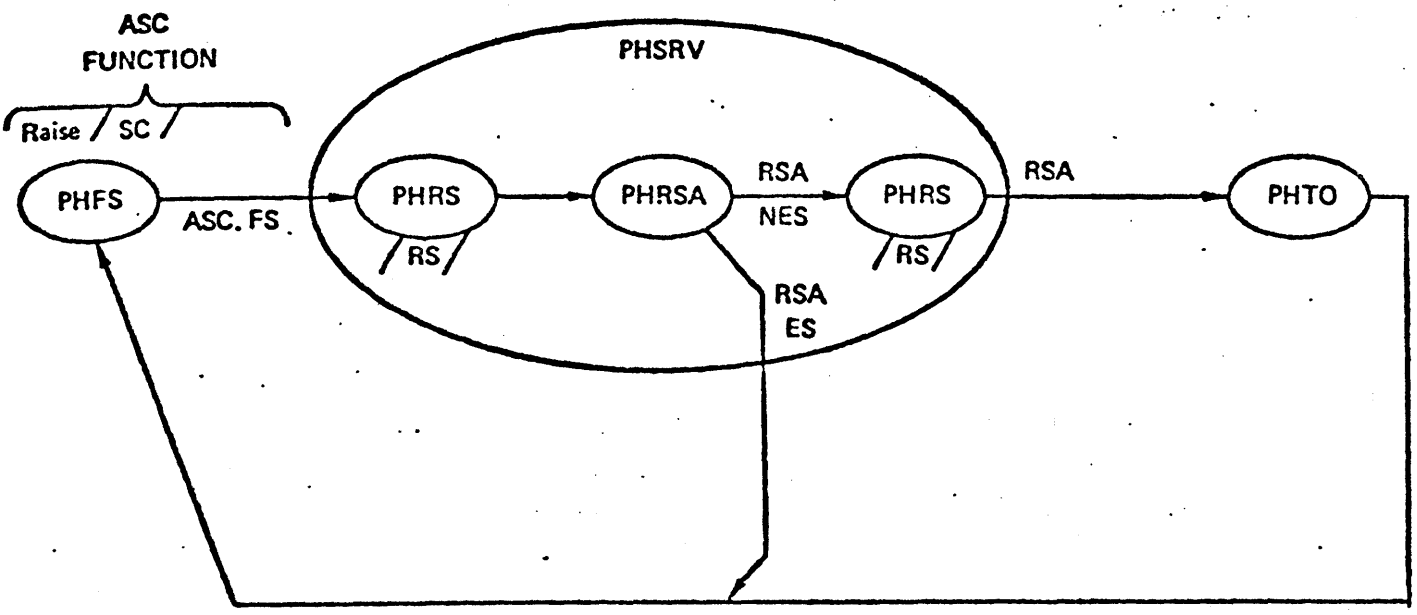

Figure 4-3. Order-In Phase Sequence

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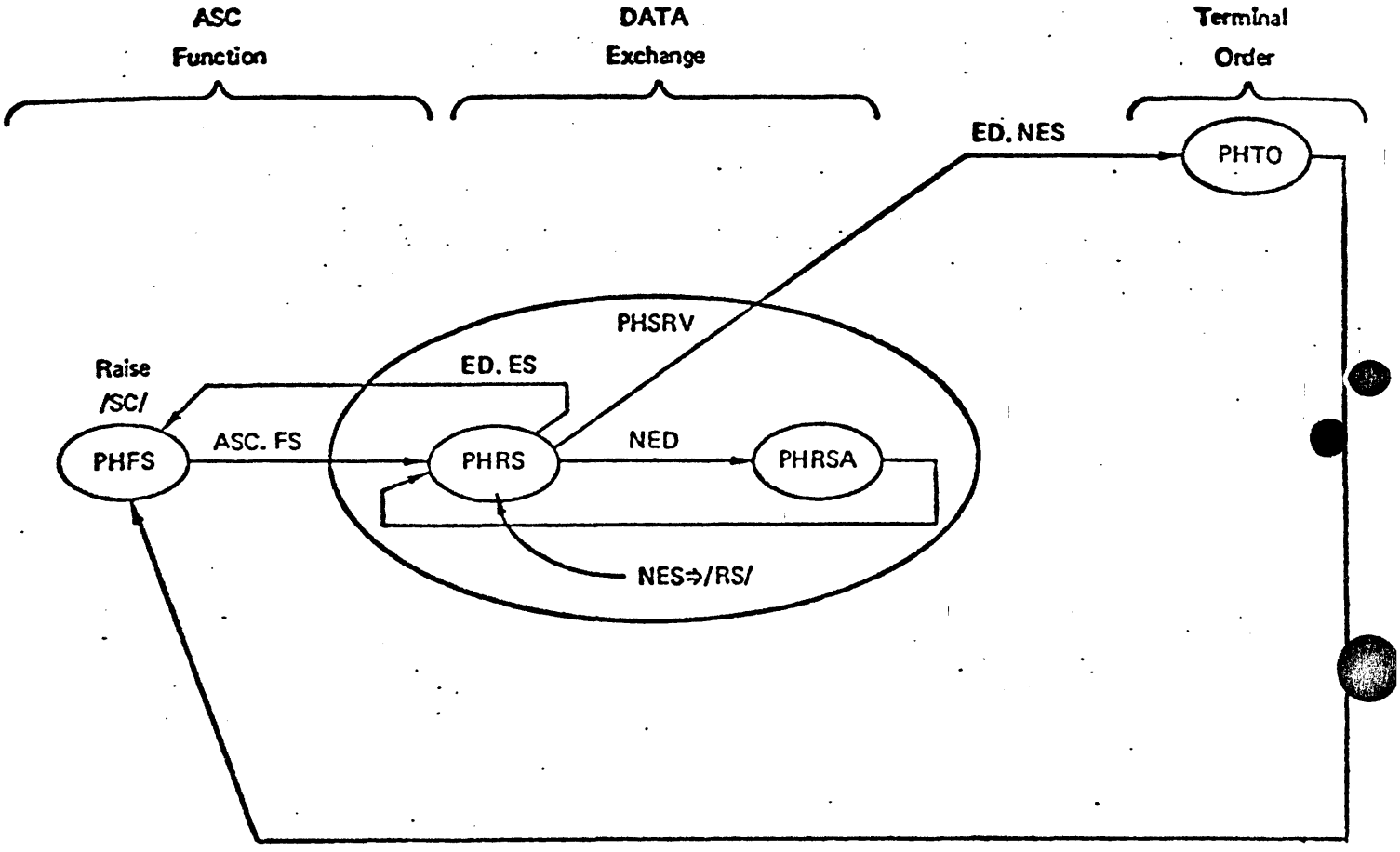

Figure 4-4. Data-Out Phase Sequence

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4-21 Data-In

Data-in is another of the four basic types of service cycles performed by the subcontroller. It provides the means for the controller to transfer data to the IOP. The data-in cycle may follow an order-out or a previous data cycle. Following an order-out, the controller must decode the order, check its validity and, if input (ORD7 false), enter the data-in state.

Data-in proceeds as shown in figure 4-5. It begins when the controller raises CSL/M(DATA) to make a service call. The resultant ASC operation then makes the service connection by setting SERVICON and advancing the subcontroller to phase PHSRV. The subcontroller remains in PHSRV where it can cycle between subphases PHRS and PHRSA, transferring data to the IOP, until the end data latch, ED, is set. End data may be set either by the controller or the IOP.

The data-in sequence is concluded with a terminal order if the IOP raises /ED/ but not /ES/ when acknowledging a request strobe. The controller must start the subcontroller's delay line for PHRS for each request strobe whether it is for a data byte or the terminal order.

4-22 Terminal Order

A terminal order is an operation which may take place at the end of any of the four service cycles described in paragraphs 4-18 through 4-21. Its purpose is to convey flag bits or control information from the IOP to the subcontroller, and it consists of a transfer of one byte on the data lines.

Four terminal order bits have been assigned specific meanings as follows:

Bit 0 Interrupt ____ CIL
Bit 1 Count Done ____ CDN
Bit 2 Command Chain ____ CCH
Bit 3 IOP Halt ____ UNE

During the terminal order, the subcontroller stores these bits into four buffered latches, CIL, CDN, CCH, and UNE, respectively.

It is always the IOP that specifies whether or not a terminal order is to be issued. It does so by acknowledging a request strobe while holding /ES/ low and /ED/ high. When this situation is detected, the subcontroller produces one more request strobe then goes to the terminal order phase, PHTO, to await the request strobe acknowledge from the IOP. After obtaining the order and storing the four bits as stated above, the subcontroller returns to PHFS where further action may be taken according to the state of those bits.

4-23 Command Chaining

Command chaining is specified by bit 2 in the terminal order concluding an order-in service cycle. At this time, CCH is set if bit 2 is true.

If command chaining is not specified in that terminal order, the device controller busy flip-flop, DCBUSY, is reset as the subcontroller returns from phase PHTO to PHFS. If command chaining is specified, DCBUSY remains set and the subcontroller goes to the order-out state and makes a service call, just as it does following a successful SIO.

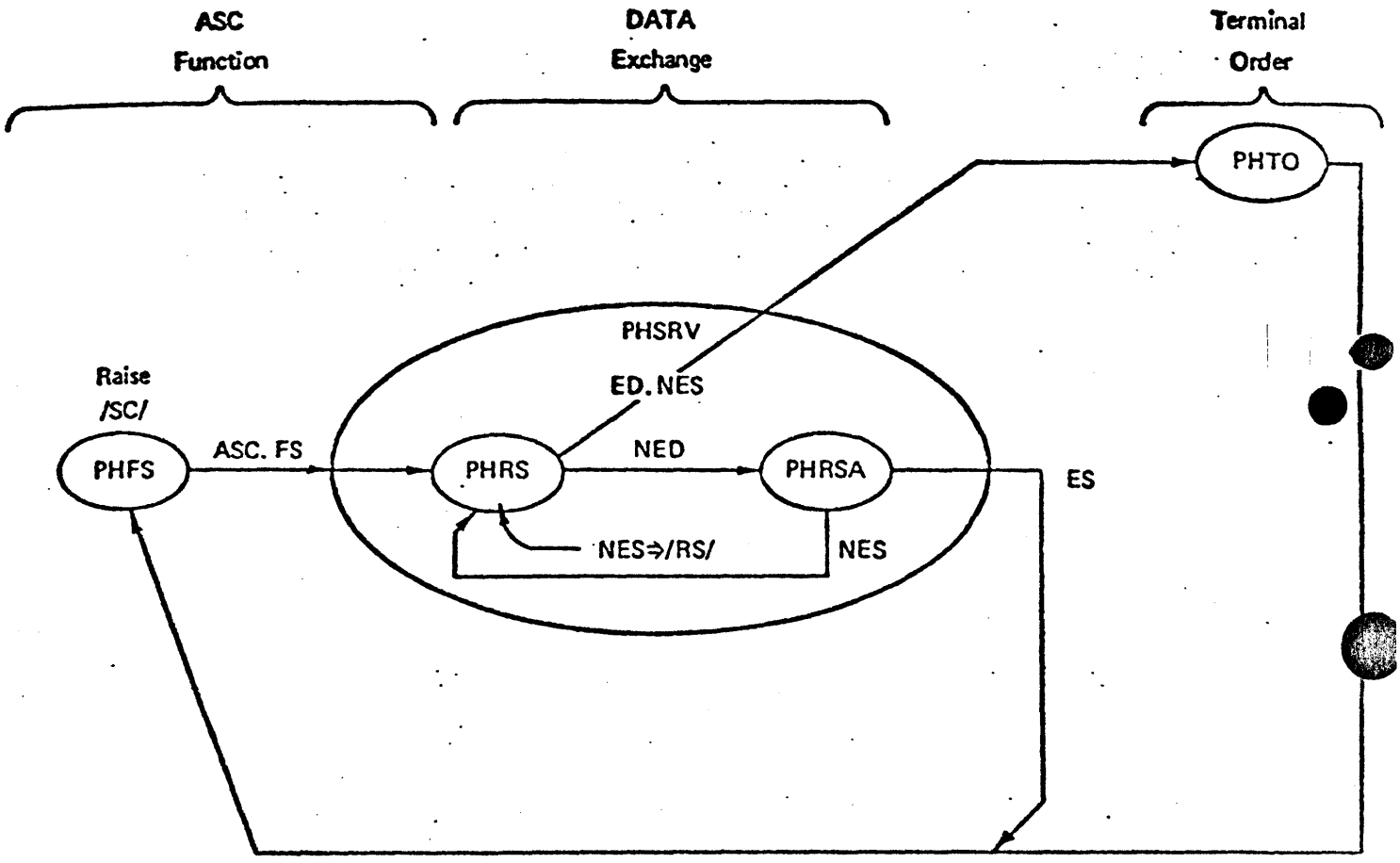

Figure 4-5. Data-In Phase Sequence

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4-24 Testmode

The subcontroller may be switched to the testmode by placing a toggle switch on the LT95 module in the down position. The testmode allows testing of the phasing, the data register, the order register, some control terms, and much of the IOP without using the device itself.

When operating in the testmode, the normal control signals which transfer information to the data register for data-in or order-in are disabled. Replacing them is another signal which gates the subcontroller's order register into the data register. Thus, a data-in or order-in cycle causes the order received in an order-out to be returned to the IOP on the data lines.

4-25 Order Register

The order register is an 8-bit register which receives the order during an order-out. The order will be received from the IOP over the /DA0/ through /DA7/ lines or from the maintenance panel switches.

Orders are transferred into the register from the IOP by signal ORDXDA and from the maintenance panel by signal ORDXMAINT. One or the other of these signals will be enabled by the condition of latch MAINT-1 controlled by the MAINT/MONITOR switch on the maintenance panel. The selected gating term will be true during PHRSA of the order-out and while PHRSAT000W is true.

The order register is cleared by signal ORDXO, which is true during PHRSA of an order-out. This term is approximately 50 nanoseconds shorter than ORDXDA or ORDXMAINT, thus clearing the register just prior to loading it with a new order.

The order is held in the register until the next order-out. Order decoding is done by the controller. Decoding is enabled by signal ORDENABLE, provided by the subcontroller. This term will be true only during data service cycles when the subcontroller is not in the testmode (as described in paragraph 4-24).

Order decoding is accomplished by the controller and uses data bits DA3, DA5, DA6, and DA7. The presence of any other data bit true will cause the unusual end (UNE) flip-flop to be set (as described in paragraph 4-61). Decoding of the orders is as follows:

BIT 3	5	6	7	ORDER
0	0	0	1	Write
*	0	1	0	Read
0	0	1	1	Seek
0	1	0	0	Sense
0	1	0	1	Checkwrite
1	0	1	1	Test

*Bit 3 is true for a read 12 order. It is used in the parity reporting logic to enable setting TER at the end of the failing sector instead of after all data has been transferred in a multisector read operation.

4-25 (cont'd)
The decoded orders are further combined to generate control terms within the controller.

SKS	=	Seek or sense order
RCHW	=	Read or checkwrite order
WCHW	=	Write or checkwrite order
WRCH	=	Write, read, or checkwrite order

Any bit configuration of bits 3, 5, 6, and 7 (other than as indicated above) will cause the signal ILO to be true. This illegal order signal will cause UNE to be set (as described in paragraph 4-62).

4-26 EXTENDED INTERFACE

The controller contains the extended interface option which is a basic set of logic added to expand the controller/IOP data path to either two or four bytes. The conversion from a 4-byte data path to a 2-byte data path consists of removing four modules and one cable.

The extended interface contains the following circuits:

a. Three input data registers and three output data registers
b. Byte alignment logic
c. Interface control circuits
d. Cable receivers and drivers to connect the 4-byte data path interface

The option consists of the following modules incorporated in the controller to interface with the IOP:

Location	Type	Description
20B	IT11	Interface Control logic
21B	FT10	WIDEINTER and byte presence flip-flops
22B	BT10	C-register control logic
23B	FT26	Byte accumulator (byte alignment) C(BCD)
24B	FT80	CB register
25B	FT80	CC register
26B	FT80	CD register
27B	FT81	DB:D-register
28B	FT81	DC:D-register
29B	AT60	Cable receiver/driver
30B	FT81	DD:D-register
31B	AT60	Cable receiver/driver
32B	BT11	Miscellaneous control buffer

4-26 (cont'd)
Not part of the extended interface option, but included in the controller for use with the option are the logic modules at locations listed below:

22A	LT71	C(BCD) inverters
23A	LT96	CD register parity check logic
24A	LT96	CB and CC register parity check logic

During data transfers between the IOP and controller, the data path width may be extended to two or four bytes. The registers which receive data are the CA, CB, CC, and CD registers. Registers which transmit data are the DA, DB, DC, and DD registers. The CA register is part of the 16-byte buffer, while the DA register is part of the extended subcontroller. All the other registers are part of the extended interface option.

The controller's buffer storage area, 16-byte buffer or FAM, can process only one byte at a time. Provision is made in the wide interface to handle the bytes sequentially and to signal when all bytes have been transferred to their proper destination.

4-27 Interface Width Control

Three signals from the IOP will control the operation of the extended interface:

a. EDX2 will enable the interface for the 2-byte wide data path.
b. EDX4 will enable the interface for the 4-byte wide data path.
c. IER will interrupt the extended data path and return it to the 1-byte width.

When the IOP holds /IER/ low, the wide interface may be enabled. The sector end flip-flop, SECEND, will be set only during the last seven bytes of a sector of a data-in operation. With this flip-flop reset and IER low, the WIDEINTR/1 flip-flop will be set with end service, ES, of a data service cycle (except for a seek or sense order).

The setting of WIDEINTR/1 enables the set input of WIDEINTR/2, which will be set by T000 during the first PHRS of the data service cycle. These two flip-flops control the start of the byte presence indicator cycle (described in paragraph 4-28).

The setting of WIDEINTR/1 will also enable the raising of either the /DX2/ or /DX4/ line by the controller. This indicates to the IOP that the controller is in the directed data path width.

4-28 Byte Presence Indicators

The byte presence indicators, BPB, BPC and BPD, comprise a ring counter started by the WIDEINTR flip-flops and ended with the resetting of BPD. The BPB flip-flop will be set at the start of a data-out service cycle after the byte from the CA register has been transferred to indicate that there is a data byte present in the CB register. The next clock will clear BPB and set BPC (if on the 4-byte data path) to indicate there is a data byte in the CC register. The next clock will clear BPC and set BPD, indicating there is a data byte in the CD register. The setting of each flip-flop, in turn, will direct the data from each register through the byte alignment logic into the FAM.

4-28 (cont'd)

During a data-in service cycle, BPB is set when a byte has been transferred to the K-register. This will direct the next byte to the CB register. BPC will direct the next byte to the CC register and BPD will direct the next to the CD register.

Note that the clock for the byte presence indicators is derived from the FAM read or write timing. This synchronizes the transfer of data in and out of the FAM to the timing of the FAM, which is independent of the IOP interface timing and the device interface timing. FAM timing is described in paragraph 4-38.

4-29 Maintenance Provisions

When the controller is placed in the maintenance mode from the maintenance panel, data for the four C-registers on a data-out operation will come from the DATA/TRACK switches on the panel. The controller will be placed in the 4-byte data path by the MAINT switch.

4-30 Parity Check

The /PC/ line is raised to indicate that parity may be checked on the ensuing data transfer. The IOP may raise the line for data-out or order-out operations while the controller raises it for data-in operations. The controller will not raise the /PC/ line during seek or sense operations.

During a data-out operation each C-register has its own parity check circuit whose output (CAPAR, CBPAR, CCPAR, or CDPAR) will be true if the associated one byte contains even parity. Each output is gated with its byte presence indicator (CAPAR is gated with T100) to produce a clock (if /PC/ is true) for the PARCNTR flip-flop. The clock may also be produced if even parity is detected in the order received from the IOP.

The PARCNTR flip-flop is set through its mark input at the time that either the order register or CA register is cleared, just prior to receiving a new data byte (ORDX0 or CAX0). Thereafter, as each byte is checked for parity, when even parity is detected the flip-flop is clocked. An odd number of even parity detects will leave the flip-flop reset. An even number of even parity bytes will leave the flip-flop set.

The reset output, NPARCNTR, is exclusive OR gated with WIDEINTR/2 and this result is exclusive OR gated with the parity bit from the IOP, received over the /DAP/ line to set the PAR(IOP) flip-flop.

If even parity is detected for the complete parallel data transfer, the parity transmission error latch, PTE, will be set. This, in turn, will cause the unusual end flip-flop, UNE, to be set and the data operation terminated (see paragraph 4-19).

During a data-in operation, as each byte is read from the FAM, it is checked for even parity by the R-register parity circuit. If odd parity is detected, NPARR is high and the PARD flip-flop will be clocked. An even number of bytes with odd parity will leave PARD set. An odd number of bytes with odd parity will leave PARD reset. PARD will cause PARD:D to be set and drive the /DAP/ line to the IOP high. It will be driven at the same time that the /PC/ line is driven to indicate to the IOP that the data may be checked for parity.

4-31 16-BYTE BUFFER

The 16-byte buffer is a basic set of logic which provides a standard modular sub-group for the purpose of standardization of device controllers. The buffer supplies storage for 16 bytes of data in a FAM module. It also contains the FAM input and output registers, timing, and control circuits.

The buffer consists of the following modules incorporated in the controller:

Location	Type	Description
12B	FT81	K-register
13B	FT25	Fast access memory (FAM)
14B	FT79	J-register
15B	FT66	R:L R:WRITE R:READ
16B	FT75	R:LW R:LR counters
17B	XT10	Terminators
18B	HT15	Delay line sensors
19B	DT14	Delay line
10C	BT22	JFULL inputs, JXO
11C	FT66	KFULL JFULL
12C	BT11	J- and K-registers, LW, LR controls
13C	IT11	R:SREAD and R:SWRITE inputs
14C	AT75	Priority determination logic
15C	FT75	R:K counter
17C	LT18	R:K decodes
18C	BT11	R:K decodes and control
19C	FT81	CA register

The buffer is an integral part of the controller and provides the temporary storage capability necessary to interface between the different data transfer rates of the IOP and the device. A byte which is to be stored in the FAM can be transmitted from the IOP or the maintenance panel during a data-out. This byte is first stored in the CA register, then is transferred to the J-register for the subsequent write operation. As the data enters the J-register, JFULL is set to indicate the presence of data. JFULL is reset upon writing into FAM. During execution of a read order, the data is transferred from the data shift D-register. The utilization of JFULL is the same.

During a FAM read operation, the byte from the FAM is stored in the K-register prior to its transmission to the DA register during execution of a read order or to the D-register during execution of a write or

checkwrite order. KFULL is set upon reading data from the FAM and is reset when the data is transferred to the DA or the D-register.

The particular address location within the FAM is specified by a 4-bit address register (R:L0—R:L3) which accepts addresses from the R:LW counter during a write operation and from the R:LR counter during a read operation. The number of bytes within the memory are tracked by the R:K counter. As each byte is written into memory, the R:K counter is incremented; as each byte is read from memory, the R:K counter is decremented. Therefore, the state of the R:K counter indicates the number of bytes still remaining in the memory. This is decoded by logic.

The various timing pulses necessary to properly sequence the events are generated by a delay line. The logic to start a read or write cycle, as well as the logic required to determine priority between a read and a write operation, is contained in the start-up logic.

The above description of operation is a general overview and is for a single byte of data. Paragraphs 4-32 through 4-40 and figure 4-6 provide a more detailed description of operation.

4-32 C-Register

The C-register includes the CA, CB, CC, and CD registers. These registers receive the data transmitted from the IOP over the /DA/, /DB/, /DC/, and /DD/ lines. Data is strobed into all registers at the same time by CAX(IOP). Note that the individual terms for the extension registers (CB, CC and CD) are CAX(IOP) one logic level later.

The strobe will be true when the controller is not in the maintenance mode of operation, during a data-out, and PHRSAT000W is true. Similarly, data from the maintenance panel switches will be strobed in when the controller is in the maintenance mode. The other timing inputs are the same.

The register is cleared by CAX0 (CBX0, CCX0 and CDX0) which will be true during PHRSA and T000. Since PHRSAT000W is 50 nanoseconds longer than T000, the existing data at the fall of T000 will be latched into the C-register.

The outputs of the CA register are transmitted to the J-register (see paragraph 4-33). The outputs from the CB, CC, and CD registers are channeled through the byte alignment logic, which is controlled by the byte presence indicators (see paragraph 4-28). During a checkwrite operation, NCA00 through NCA07 is transferred to the J-register and the outputs from CB, CC, and CD are complemented by exclusive OR gates following the byte alignment logic.

Data received from the IOP or the maintenance panel switches is routed to the FAM through the J-register.

During a data-in operation, the CB, CC, and CD registers receive data directly from the FAM (R00-R07). Bytes are strobed into each register under the control of the byte presence indicators (paragraph 4-28). When all registers, including the K-register of the buffer are full, data is transferred to the DA, DB, DC and DD registers for transmission to the IOP.

4-33 J-Register

The J-register is the input register to the FAM module and has four sets of input gates:

a. The outputs of the CA register (CA00-CA07) are strobed into the J-register by JXCA during a data-out.

b. The inverted outputs of the CA register are strobed into the J-register by JXNCA during a checkwrite (data-out).

c. The outputs of the CB, CC, and CD registers are strobed into the J-register by JXC(BCD) during a data-out.

d. The outputs of the D-register (DAR, D00-D06) are strobed into the J-register by JXD during a read.

Just prior to data being strobed into the register, it is cleared by JX0.

As data is strobed into the J-register, the JFULL latch is set. Two things should be noted about the JFULL latch:

a. JFULL is not set during the first PHRS following PHFS. Data is strobed into the C-register during PHRSA, which is after the first PHRS. Therefore, no meaningful data is in the C-register during the first PHRS.

b. The JFULL and JFULL/DLYD latches are implemented upside-down. This is necessary to ensure that JFULL will be reset at R:T110. Since the M-input overrides the E-input, this condition is satisfied. If, for example, JFULL remained set beyond R:T300, it is possible that an additional write cycle may be initiated.

JFULL will be reset whenever an order-out operation is being performed, or at R:T110 of a memory write cycle, during a data-in service cycle, or after all bytes have been transferred during any other service cycle (NDATAIN).

Since JFULL is reset early in a write cycle, JFULL/DLYD is provided. This inverted latch is set when JFULL sets, but it will not reset until after JFULL is reset and the write cycle is completed (R:T300). NJFULL/DLYD indicates that the J-register is not in use and the write cycle has been completed.

During a seek order operation, the contents of the J-register containing the track and sector addresses will be transmitted to the track (T) and sector (S) counters by terms LSB1 and LSB2 (described in paragraphs 4-50 and 4-51).

4-34 K-Register

The K-register is the output register from the FAM. It receives inputs directly from the 16-byte memory, or from the track and sector counters during a sense operation. The transfer from memory into the

K-register will occur at R:T200 of a read cycle. This transfer term will be inhibited during a data-in operation when any of the byte presence indicators is set (N(DATAIN·BP)). This inhibit is used to hold a data byte in the K-register as data bytes are transferred into the CB, CC, and CD registers for subsequent transmittal to the IOP.

After the last data byte has been read from the FAM and stored in its destination register (K for the 1-byte data path, CB for the 2-byte data path, and CD for the 4-byte data path), the KFULL latch will be set. KFULL is set at R:T220 of the last memory read cycle. At R:T300 of the same cycle, KFULL will cause KFULL/DLYD to be set.

When data is transferred from the K-register to the D-register or to the DA register (along with CB, CC, and CD to the DB, DC, and DD registers), the KFULL latch will be reset. This will reset the KFULL/DLYD latch and set KX0ENABLE. An order-out service cycle will also reset KFULL.

When KX0ENABLE is true, the next memory read cycle will clear the K-register just prior to a new data byte being transferred in from the FAM.

4-35 Fast Access Memory (FAM)

The FT25 FAM module provides storage for 128 bits arranged as sixteen 8-bit bytes. Data is written in o read out eight bits at a time. Read-out is nondescriptive and is identified as R00 through R07.

Data is written into any of the 16 locations on the trailing edge of the clock, R:T180, by addressing the location and holding R:CLKEN true. Addressing is provided by R:L0 through R:L3. The signal R:CKLEN will be true during a memory write cycle when the NR:CLKEN/1 latch is reset. This latch will be reset by an order-out and can only be set at the end of a FAM cycle (R:T300) when the FAM is full (R:K0) during testmode 1 (TM1).

A complete description of the FT25 may be found by referring to the description of the FT40 in the Xerox T-Series IC Circuit Logic Modules (Publication No. 64-51-03). The FT40 is the same as the FT25 with the exception of pin assignments.

4-36 Buffer Address Register and Counters

Two 4-bit counters supply the address for the buffer write and read cycles. One is used to track write operations (R:LW0 through R:LW3) and the other is used to track read operations (R:LR0 through R:LR3). The counters are energized only while the BUFFER/EN latch is set. The BUFFER/EN latch i set only during data service cycles (DATA) and is reset by an SIO (CLEAR-1) or during an order-in service cycle (ORDIN·PHSRV). (See figure 4-6).

The two address counters are cleared by R:LX0 during an order-out and PHRSAT000W. The term (R:LX0) provides a clock to the counters while the counter set inputs are held false, thereby resetting all counter stages. The counters are incremented during read or write operations by the falling edge of R:LRCLK or R:LWCLK, respectively. Both clocks use R:T060/1 which falls immediately after R:T130 of a read or write cycle.

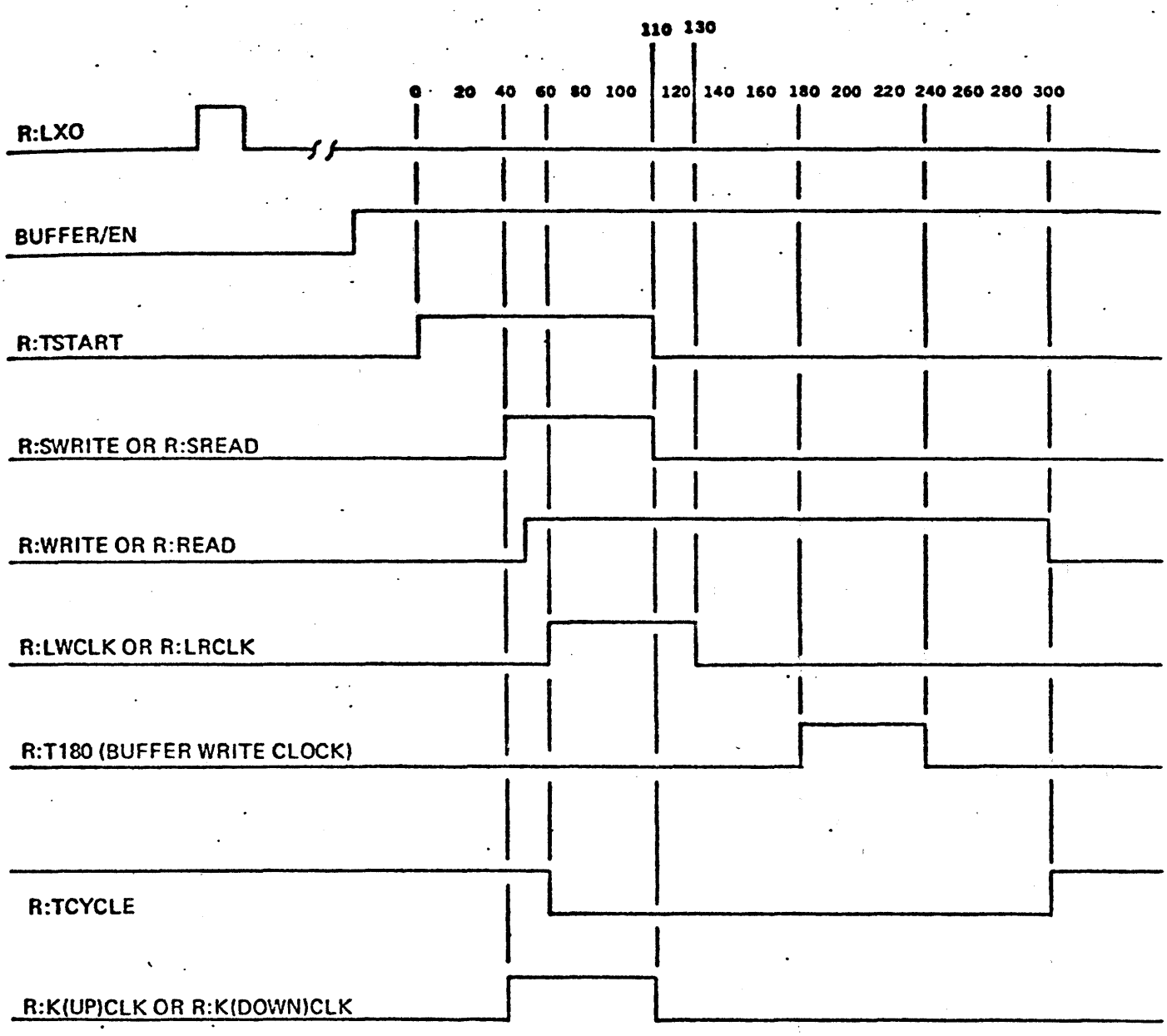

Figure 4-6. Buffer Timing Diagram

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4-36 (cont'd)

The counter outputs are gated to the buffer address register (R:L0 through R:L3), via R:SWRITE or R:SREAD, depending on which operation is being performed. This group of latches is always forced to the zero state during R:TCYCLE, which is true to indicate that the buffer logic is not in use. The NR:TCYCLE latch is set by R:T060 and reset by R:T300. The latch is held reset by NDCBUSY when the controller is not busy.

The buffer address register (R:L0 through R:L3) selects the byte location within the FAM module.

4-37 Buffer Byte Counter

As a byte is written into or read out of the buffer, the byte counter (R:K0 through R:K4) is incremented by R:K(UP)CLK or decremented by R:K(DOWN)CLK, respectively. (See figure 4-6).

Since the buffer can store a maximum of 16 bytes, when the most significant bit of the counter (R:K0) is set, the buffer is full. Note that during an order-out sequence for a data-in operation in testmode 1, a separate input is provided to set R:K0, thus signifying that the buffer is full. This is necessary to ensure that at least 16 bytes of data will be transmitted to the IOP in the subsequent data-in operation. NORD7 is true to indicate that the order requires a data-in operation.

The byte counter is cleared at the same time as the two address counters R:K(LOAD)CLK=ORDOUT·PHRSAT000W. This load clock will clock all stages of the counter to zero while the set inputs are held false. R:K0 may be set at this time for testmode 1 data-in as described in the preceeding paragraph.

The least significant bit of the counter is clocked by R:T060/1. The outputs of this stage, R:K4 and NR:K4, are used to generate incremental and decremental clocks R:K(UP)CLK and R:K(DOWN)CLK. These two clocks are used by the succeeding stages. Since NR:T110 is used in the up and down clocks, the four most significant stages will be clocked 110 nanoseconds after the timing is started. R:K4 will be clocked approximately 20 nanoseconds later. This is necessary to ensure that R:K4 is held static until the falling edge of NR:T110 has had time to propagate.

The byte counter is incremented once for each write cycle and decremented once for each read cycle. When the counter has decremented to the state of all zero's, this signifies that the buffer is empty. As noted earlier, when R:K0 is set, this signifies that the buffer is full.

4-38 Buffer Timing and Control

The buffer timing and control circuits include the buffer start-up logic (rejection gates), delay line, and the R:READ and R:WRITE latches.

The timing signals to control the various sequences in the buffer are generated by the DT14 delay line module in combination with the HT15 sensor module. Figure 4-7 shows the timing outputs from the generator. Note that outputs R:T060/1, R:T110, R:T180, and R:T200 use inverting sensors from downstream in the delay line to ensure a more predictable trailing edge. This is because the pulse in the delay line may be from 82 to 133 nanoseconds in duration.

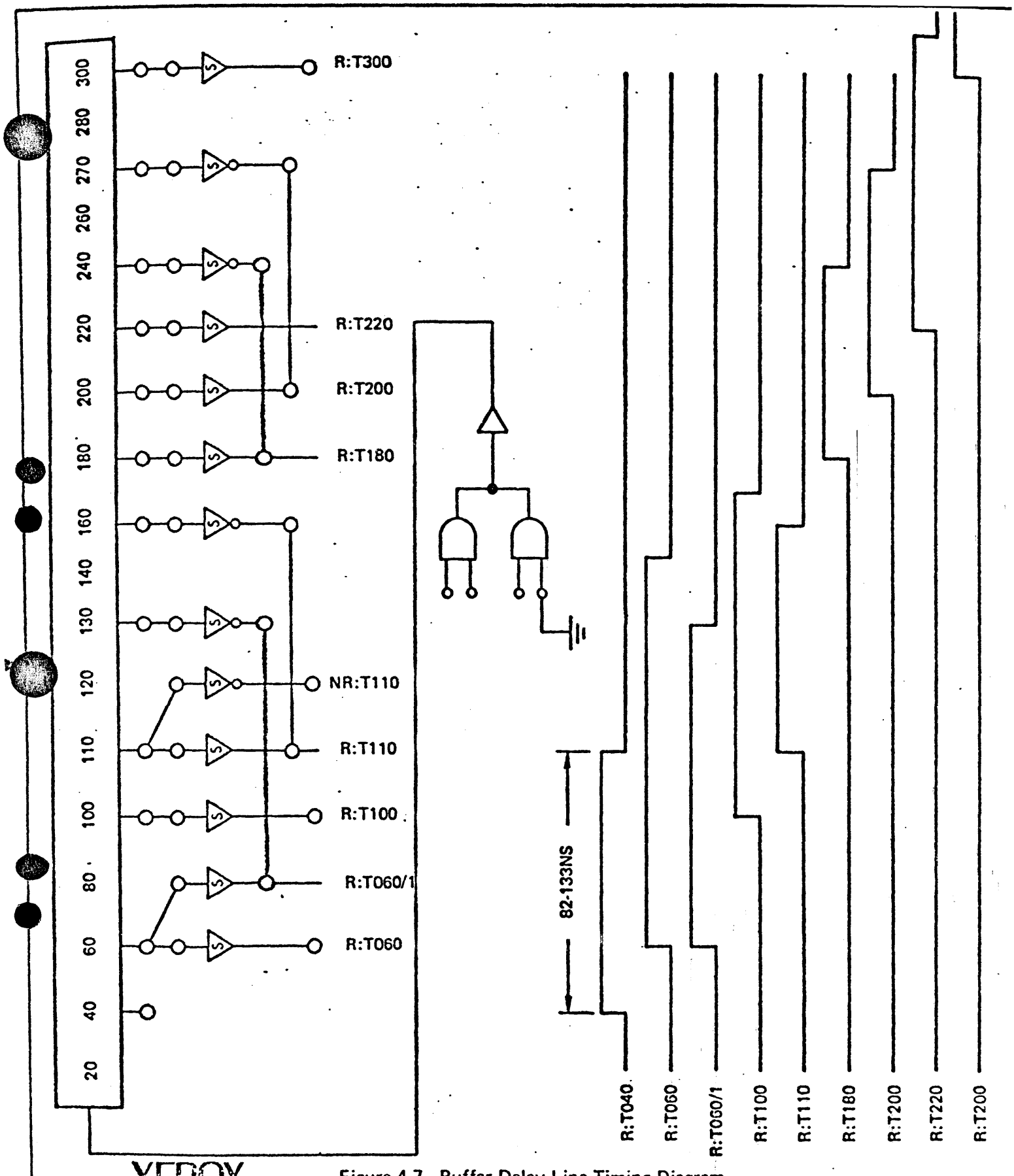

Figure 4-7. Buffer Delay Line Timing Diagram

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4-38 (cont'd)

The pulse will be started in the delay line when R:TSTART goes true. One of the conditions necessary to start the delay line is that R:TCYCLE be true. This condition indicates that the buffer logic is at rest.

The NR:TCYCLE latch will be set at R:T060, thereby limiting the length of the propagated pulse to 82-133 nanoseconds, depending on transition times in the circuit. The latch will be reset at R:T300. Since the pulse at the R:T300 output may be 133 nanoseconds long, the buffer could be idled unnecessarily long. For this reason, the NR:TCYCLE latch is implemented upside down to use the set-override feature to permit setting the latch at R:T060.

Signal R:TSTART is generated by the buffer cycle start-up logic. This is contained on an AT75 module and includes input gating and two special rejection gates, R:SWRITE and R:SREAD. These gates operate like latches with one exception, the erase input overrides the mark inputs. Also, each rejection gate has multiple set and reset outputs. Set outputs from each gate are wired together to provide R:TSTART, which will be true if either rejection gate is set.

If both rejection gates are set at the same time, R:SWRITE will take priority. This is accomplished by wiring a reset output from R:SWRITE directly to the set output of R:SREAD, thereby disabling the R:SREAD output. This will not affect R:TSTART.

Note that the set outputs of both rejection gates are gated with R:T040/D to set the R:WRITE and R:READ latches. These latches are used to control transfer terms in the controller during buffer write and read cycles. (See figure 4-6.)

When R:TSTART goes true, the M-inputs to the priority logic are inhibited by a fast (10-nanosecond propagation maximum) inverter whose output is NR:TSTART. The rejection gates will be reset at R:T110. Note that, with the erase override feature, the rejection gates will be enabled only when the BUFFER/EN latch is set.

4-39 R:SWRITE

There are two conditions in which R:SWRITE is initiated: normal mode of operation, and testmode 1. In either case, (JFULL·R:TCYCLE) must be true indicating that there is data in the J register and no other buffer operation is in progress. In testmode 1 (TM1), when ORD7 is true, data is being transmitted from the IOP to the controller. In this mode of operation, the absence of NR:K0 in the term for the M-input indicates that any number of write cycles may be initiated. However, after 16 bytes have been stored, R:K0 goes true, and the write clock to the FAM will be inhibited by R:CLKEN/1. Therefore, although further bytes may be accepted by the controller, no more will be written into memory.

In the normal mode of operation, a buffer write cycle may be initiated when the J-register is full and the buffer electronics is not in use (as noted in paragraph 4-38). Also, the buffer must not be full, as indicated by N:RK0, and (M/R:SWRITE) must be true. This last term will be true under one of the following conditions:

a. A read order is in progress, indicated by NORD7.
b. The buffer is empty and data must be written into it, indicated by R:EMPTY.
c. The K-register is full; therefore a FAM read cycle is not necessary.

4-39 (cont'd)

A read order will give the J-register priority because data from the device must be transferred as soon as it is available. Transfers to the IOP can be held up.

4-40 R:SREAD

The condition in which R:SREAD is initiated requires that no buffer operation is in progress (R:TCYCLE), the K-register is empty of data (NKFULL), there is still data in the FAM (N:REMPTY), and the term (M/R:SREAD) must be true.

The purpose of (M/S:READ) is to inhibit the start of a read cycle under the following conditions:

a. During any of the read orders (NORD7) if there is data in the J-register (JFULL), and the buffer is not full (NR:K0)

b. During a write, checkwrite, or seek operation while in testmode 1 (TM1·ORD7)

c. During a data-in service cycle using the wide interface when the end data (ED) latch is set

Note that a read cycle will take precedence over a write cycle when a write or checkwrite operation is in progress. This is because data must be in the K-register and ready for use by the device at the instant the device requires it. Transfers from the IOP may be held up.

4-41 Service Call Logic

The service call logic is used to drive the service call line, /SC/, to the IOP and initiate one of four types of service cycles (as described in paragraphs 4-17 through 4-21). The logic includes the CSL latch (part of the subcontroller) and the service call request (SCR) latch.

The CSL latch can only be set when the controller is busy. This will remove NDCBUSY from the reset input and provide one of the terms necessary to set the latch. Also, the subcontroller must be in its idle phase (PHFS), the subcontroller timing must be idle (TCYCLE), the controller must be in the maintenance or on-line mode (MAINT+INC), and the term CSL/M1 must be true.

CSL/M1 will be true when a service call is to be made. There are four inputs, any of which may raise the signal:

a. For an order-out service call (NDATA·NIN). This will occur after the controller becomes busy following the SIO sequence.

b. For an order-in service call (FINISH+UNE). This will occur after a data transfer is completed, either normally or with an unusual end.

c. For a test order-in (TEST·NDATA). During a subcontroller test mode, when either CDN or UNE is set, the DATA flip-flop will be reset and the next service cycle will be an order-in.

d. For a data service cycle, the term CSL/M(DATA) will be raised. Count done and unusual end must be false (NUNE·NCDN).

4-41 (cont'd)

The term CSL/M(DATA) will be true for any of eight different conditions:

a. SCR is set and a data-out operation is in progress.

b. A data-out operation is in progress, the J-register is empty, there are no bytes in the C-register extension, and there are less than 12 bytes in the FAM.

c. SCR is set and a read order is in progress.

d. A read order is in progress, the K-register is full, and the data record is completed, as indicated by POST being set. This empties the FAM at the end of a data record.

e. The subcontroller is in the test mode of operation (see paragraph 4-24). Continuous service calls will be generated until the subcontroller is advanced to the order-in state.

f. The controller is executing a test order.

g. A seek order is being executed and all the seek bytes have not been transferred from the IOP.

h. A sense order is being executed and a sector pulse has been received. (Indicated by NTSE.) This ensures angular position is correct.

The SCR flip-flop is used by the controller to request a service call during read, write, and checkwrite orders. During a data-out operation, the controller will try to keep the FAM as full as possible. During a data-in operation, the controller will try to keep the FAM as empty as possible.

During execution of a read order, the set input will be true when FSL:D is low and one of the following conditions is true:

a. There are eight or more bytes stored in the FAM.

b. There are four to seven or twelve to sixteen bytes stored in the FAM and the controller is in phase PHFS.

c. The controller is in testmode 1, in phase PHFS, and there are eight to eleven or less than four bytes stored in the FAM.

During execution of a write or checkwrite order, the set input to SCR will be true when FSL:D is low and there are less than eight bytes stored in the FAM.

The reset input to SCR will be true when the function strobe acknowledge (FSL) is returned to the IOP and one of the following conditions is true:

a. The CDN latch has been set (by either the IOP or controller).

4-41 (cont'd)

b. There are eight or more bytes stored in the FAM or data is not being transferred to the device during execution of a write or checkwrite order.

c. There are less than eight bytes stored in the FAM during execution of a read order.

4-42 Interrupt Call Logic

The interrupt call line, /IC/, to the IOP is driven by the CIL buffer latch in the subcontroller. This latch is set when an interrupt is pending and has not been acknowledged by the IOP. The CIL latch is set if data bit 0 (DA0:R) is received true during a terminal order. There is no provision for a controller-generated interrupt.

4-43 Data Operations End

Data operations between the IOP and controller may be concluded by resetting the NED latch in the subcontroller (see paragraphs 4-20 and 4-21). The controller may reset this latch by resetting the NED:D latch, which will also drive the end data, /ED/, line to the IOP. Any of seven possible conditions will reset the NED:D latch:

a. The DATA flip-flop (paragraph 4-12) is reset. This will cause end data to be signaled for the 1-byte order-in data transfer.

b. The last sense byte is being transferred.

c. The last seek byte is being transferred.

d. The FAM is empty during a read order and the last byte is being transferred.

e. The controller is in the maintenance mode; the controller is not requesting a service call; and the operation in progress is not a seek or sense.

f. The UNE latch or FINISH flip-flop has been set, indicating an end of the data operation.

The FINISH flip-flop will normally be set at the end of a seek, sense, write, and checkwrite operation. During a write or checkwrite, when CDN is set by the IOP, FINISH may be set when the 16-byte buffer is empty, as indicated by R:EMPTY·NKFULL/DLYD·NJFULL/DLYD. The flip-flop may also be set when the test order data byte has been requested.

The unusual end latch, UNE, may be set by the IOP during a terminal order (paragraph 4-22) or by the controller (paragraph 4-62).

4-44 DEVICE INTERFACE CONTROL LOGIC

The device interface control circuits are used to transfer data between the 16-byte buffer and the device at a rate determined by the device capabilities. The logic also provides the necessary control signals to the

device and receives status information. The control logic includes a clock circuit, bit and byte counter, track and sector registers, data shift register, and parity register. Paragraphs 4-45 through 4-64 describe the device interface control logic circuits in greater detail.

4-45 Interface Clock Logic

The interface clock will provide one of two clocks, depending on the operation:

a. A 2.5 MHz clock

b. A clock derived from the read data, DSR, received from the device for a read operation

The internal clock is generated by a 5.0 MHz oscillator having an output signal designated CLK5MH. This signal is divided in two by a flip-flop whose output signal of 2.5 MHz is designated CLK.

When the device type (TYPOR-NTYP1R) returned from the selected unit is decoded, NEXT is true and CLK is gated with CLK5MH to provide a 2.5 MHz clock.

When the data strobe is enabled during a read operation, the setting of DSE will gate the data strobe received from the device, DSR. At the same time, internal clock gate will be disabled.

There are four separate driver outputs for the clock designated RWCK-1 through RWCK-4. The 2.5 MHz clock is transmitted ungated to the selection unit over line /CLK/.

4-46 Seek/Sense Byte Counter

The seek/sense byte counter is used to track the number of bytes during execution of seek and sense orders and to provide timed gates for the operations. The counter consists of flip-flops S00 and S01.

During an order-out service cycle, the flip-flops will be set as the order is transferred from the IOP into the order register. As data bytes are transferred during execution of a seek or sense order, the counter is decremented. Decoded counter outputs SBY1 through SBY4 are provided to generate the gating terms for a particular operation.

SBY1 through SBY3 are used to gate the three sense order bytes into the K-register. SBY2 and SBY3 are used to generate transfer terms LSB1 and LSB2 which gate the two seek order bytes into the T-register and S-register (as described in paragraphs 4-50 and 4-51).

4-47 Bit and Byte Counter

The bit and byte counter (B-counter) is a 14-stage counter (B00 through B12, and POST) which performs the following functions:

a. Counts bits transmitted to or received from the addressed storage unit. Transfers are in serial format.

b. Controls data transfers within the controller so that 8-bit bytes are transferred between registers.

c. Controls writing of the 4-byte preamble (including sync pattern) during execution of a write order.

d. Enables search for the 4-bit synchronization pattern during execution of a read or checkwrite order.

e. Identifies the postamble during execution of read, write, or checkwrite order.

Bits are counted by B10 through B12; bytes are counted by B00 through B09; and the postamble is identified when the most significant bit, POST, is set.

At the beginning of each intersector gap, flip-flops TSE, RWP, RWE, PRE, and BCE are in the reset state. Flip-flop SECPD is in the set state. When a sector pulse or index pulse is detected, SECP goes true and clears flip-flops B00 through B05. The trailing edge of SECP clocks SECPD to the reset state.

(Refer to sheet 59 of drawing 180118 for the following sector timing.) The next read/write clock will set TSE, which generates DXT and BX0. BX0 resets flip-flops B06 through B12, whose set inputs are false (NBX0), on the next clock (RWCK-1). At the same time RWP is set, which sets SECPD through its M-input.

Track shift enable (TSE) allows the track address (TRK0-8) to be loaded into the data register and shifted out serially to the storage unit. TSE is reset by the 11th clock pulse after the fall of the sector pulse (9th clock pulse after TSE is set).

As the track address is transferred into the data shift register, read/write possible flip-flop RWP is set. RWP will be reset at byte 10 time (B06·B08). With RWP set, PRE is set at byte 9 time and reset at the end of the preamble. PRE is reset by BX0 which will occur when the sync pattern has been detected during a read or checkwrite operation, or when the sync byte has been written during a write operation.

Five bit times after PRE is set, RWE may be set, enabling read/write operations. RWE will not be reset until after the second byte time of the postamble.

Following writing or detecting the sync pattern, BX0 is used to preset the bit and byte counter for tracking the data record. With NEXT true the counter will be preset to 664 (decimal) for a read and to 665 for a write or checkwrite operation. The term BX1MED is used to preset the counter for the medium speed device.

When the byte counter reaches 1023 (decimal), the data record is complete. The next clock will reset B00 through B12 and set POST. During the postamble the parity byte is written (during a write) or checked (during a read or checkwrite).

The resetting of RWE at the end of byte two of the postamble concludes the data operation and indicates the end of the sector.

4-48 D-Register

The data register (D00 through D07) converts the parallel data of the IOP to serial data format for the storage unit. Inputs to the data register are the track register (DXT), the alternate 10 pattern of the

preamble (DXPRE), the preamble sync pattern 0011 (PSBWEN), the data from the K-register (DXK), and the parity from the parity register (DXP). These data inputs are then shifted right; the outputs coming from D07 are sent to the storage unit.

For a read operation, the data from the storage unit is clocked into flip-flop DAR with the data strobe generated from the read data. The output of DAR is then shifted into the data register. When seven bits of data are in the D-register and one bit in DAR, a parallel transfer is made from DAR-D06 and DAR to the J-register for storage in the FAM.

During a data operation, the first transfer into the D-register is made from the track register with the DXT term. This enables the eight least significant bits of the track address to be transferred from TRK1 through TRK8, to be stored in D00 through D07. The bit in D07 will immediately be placed on the /TRK/ line to the device. The data shift right enable, DSHR, goes true and the next clock pulse will shift the data one place to the right. At the same time, the most significant bit of the track address is transferred from TRK0 to D00. As each new bit enters D07, it is transferred over /TRK/ to the storage unit. Right shifting continues until the complete track address has been transmitted and TSE is reset.

At byte 9, bit zero time, PRE is set (see figure 4-8). At bit four time, RWE is set and either REND or WEND is raised, indicating to the device that a read or write operation is to be performed. With the setting of RWE, gate timing term BIT7RWE will be true every bit seven time until RWE is reset. This timing term is used to generate the DXPRE, DXK, DXP, and JXD transfer terms to gate data into or out of the data register.

a. Write. During a write operation, DXPRE will cause the following data pattern to be set into D00-D07: 01010101. Since D07 drives the data line to the device, the pattern transmitted to the storage unit is 10101010. This pattern is repeated two more times. When the fourth DXPRE occurs, the input to D02 is made true and the input to D01 made false. This will cause the synchronization pattern to be set into the register. The last preamble byte pattern to the device will be 10101100, the last four bits being the sync pattern.

   As the last bit of the sync pattern is being transmitted to the storage unit, the term DXK goes true and, on the next clock, the first data byte is transferred from the K-register to the D-register. At each bit seven time during the data record, a new byte is strobed into the D-register from the K-register and shifted out to the device.

   At bit seven time of byte 1024 (byte 0 of POST), the term DXP goes true and, on the next clock, the contents of the parity (P) register are transferred into the D-register and shifted out to the device.

b. Read. During a read operation, as soon as RWE is set and REND sent to the storage unit, data from the device will be strobed into DAR by the read data strobe. From DAR, the data will be shifted right to D00 and through the data register. During the preamble, the search is made for the sync pattern. Detection of the sync pattern will cause signal PSPR to go true.

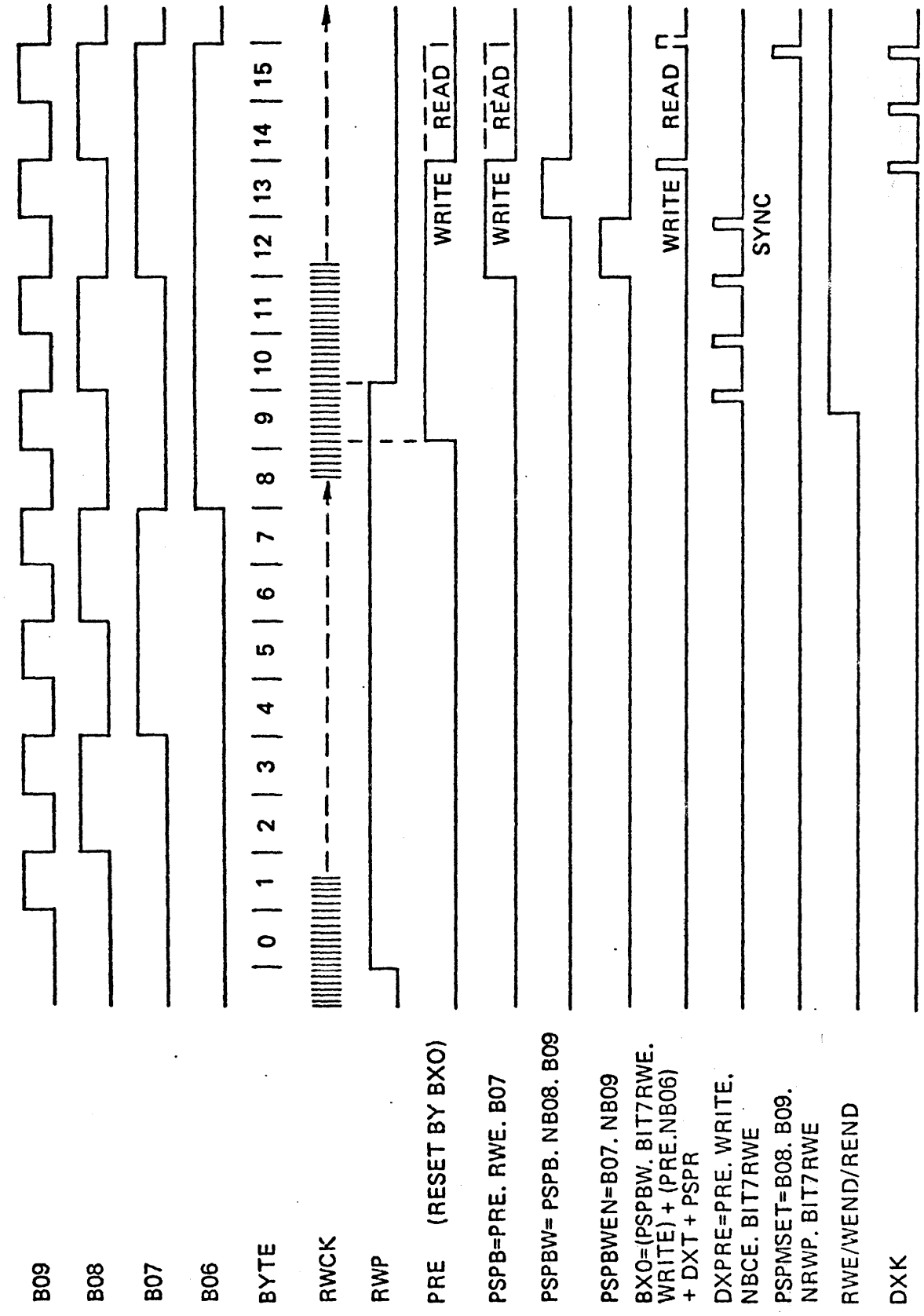

Figure 4-8. Preamble Timing

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CONTROLLER

Xerox Corporation
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204262 A

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1586(3-73)

PSPR will generate BXO and cause the B-counter to be set to 664. The setting of the B-counter starts the data record.

As data is read from the storage unit, it is strobed into DAR then right shifted through the D-register. At each bit seven time (BIT7RWE) the data in DAR through D06 will be transferred to the J-register for storage in the FAM. The last JXD transfer will occur at bit seven time of byte 1023. The data parity byte will not be transferred to the FAM.

c. Checkwrite. The execution of a checkwrite order will operate similar to the read order until the time the sync pattern is detected. When PSPR goes true, transfer term DXK is raised and a data byte is transferred from the K-register to the D-register. For the remainder of the data record, bytes will be transferred from the K-register to the D-register every BIT7RWE until the end of the record.

As the data is right shifted in the data register, ND07 is OR gated exclusively with DAR, the data read from the storage unit. The data for a checkwrite operation was inverted by the checkwrite inversion logic before it was stored in the FAM. Therefore, any comparison of data between DAR and D07 during a checkwrite operation is an error. If an error is detected, the CER flip-flop is set and transmission error is reported during the order-in cycle (see paragraphs 4-56 and 4-60).

4-49 Parity Register

The parity register, or P-register, operates in conjunction with the data register. Parity is generated for all data transferred between the D-register and the storage unit during the execution of read or write orders. Parity is generated bit-by-bit so that each bit position in the parity byte contains the parity bit for the corresponding bit position in all data bytes.

When a write order is being executed, the P-register is preset to all ones by PX1, which is true while preamble state flip-flop PRE is set. As the data bits are shifted out of D07 to the storage unit, they are also OR gated exclusively with the output of P07. The result is strobed into P00 as the contents of the P-register are shifted to the right. As each data bit is transferred to the device, parity is generated for the bit position.

With the setting of POST, further data transfers are halted and, at the next BIT7RWE time, the contents of the P-register are transferred to the D-register and shifted out to the storage unit.

When a read order is being executed, the P-register is preset to all ones. As the data is read from the storage unit into DAR, the output of DAR is OR gated exclusively with P07 and the result strobed into P00. The contents of the P-register are shifted to the right and the next data bit is OR gated exclusively with P07 to generate the next parity bit. This continues with all data bytes until the setting of POST signals the end of the data record. At this time, the parity generated during the read operation should be the same as that recorded during the write operation.

The parity byte is read from the storage unit into DAR. The output of DAR is OR gated exclusively with P07. Any difference between the read generated parity byte and the parity byte from the device will cause parity error flip-flop PER to be set.

4-49 (cont'd)

During a checkwrite operation, parity generation or checking do not occur. During testmode 2 read or checkwrite, the preamble sync pattern is loaded into the parity register and shifted through, appearing as data to the controller at P07. After the controller recognizes the sync pattern, the contents of the B-counter are transferred through PXB into the P-register. This is then shifted out to the controller to simulate data from the storage unit.

4-50 Sector Register/Counter

The S-register, which consists of flip-flops SEC0 through SEC3, stores the address of the sector at which a read, write, or checkwrite operation will begin. During the execution of a seek order, the S-register is first cleared by E-input term, TSRST. This will be true as the first seek byte is being transferred from the IOP to the controller. The S-register will be loaded under control of the seek/sense byte counter (see paragraph 4-46). The transfer term is LSB2 and the data enters the flip-flops through the M-inputs.

The S-register is connected as a ripple counter in the three least significant bits. The most significant bit flip-flop is gated and clocked. The clock term for ripple counter and the MSB flip-flop is NRWE. With the setting of RWE at the beginning of a new sector, the sector counter is incremented. When the count reaches 15, the counter recycles to zero.

Note that RWE cannot be set unless SECOMP is true. SECOMP will be true when the sector address returned from the device over the /AN0/ through /AN3/ lines is the same as the address contained in the register. This ensures that the addressed sector is now under the read/write head. The setting of RWE increments the S-register in preparation for the next sector.

The complement of the least significant bit of the sector address (NSEC3) is continuously transmitted to the selection unit. The signal is sent out over the /IDS/ line, and is returned to the controller during seek and seek verification operations to prevent a sector compare (SECOMP) signal from being generated.

4-51 Track Register/Counter

The T-register, which consists of flip-flops TRK0 through TRK8, and TRKOVF, stores the address of the track from which data will be read or onto which data will be written. During the execution of a seek order, the T-register is first cleared by the E-input term, TSRST. This will be true as the first seek byte is being transferred from the IOP to the controller. The T-register will be loaded under control of the seek/sense byte counter (see paragraph 4-46). The four least significant track bits will be transferred by LSB2. The remainder of the track address bits will be transferred by LSB1. Note that TRKOVF will be set if any of the three most significant bits of the first seek byte contains a one, indicating an out-of-limits track address.

The T-register is connected as a ripple counter and will be incremented each time the sector register cycles back to zero. If the track address is incremented out of limits, TRKOVF will be set.

The track overflow flip-flop (TRKOVF), when set, indicates that the track register contains an address greater than the last available track. TRKOVF will set sector unavailable (SUN) and cause the controller to terminate with an unusual end (UNE). For storage units with a file capacity of less than 512 tracks, the track register is decoded at the input to SUN to guard against incorrect addressing.

4-51 (cont'd)

During maintenance panel operations in the REPEAT mode, the track register is inhibited against incrementing beyond the highest available track. For single-track (SGLTRK) operations, the clock to the track register is held high, causing the track register to remain at the desired address. A MANUAL RESET will clear the track register.

4-52 Storage Unit Address Register

The U-register, which consists of flip-flops U0 through U2, stores the address of the storage unit to be used for input/output operations. Inputs from the storage unit address drivers are clocked into the register during PHFSL of an SIO, TIO, or TDV when the controller is not busy (NDCBUSY). The clock will occur 110 nanoseconds after the subcontroller timing has been started in PHFSL.

The storage unit address drivers receive data from the maintenance panel or the IOP data lines. When the controller is not in the maintenance mode, /DA5/ through /DA7/ are gated to the register and strobed in as described above. The address is also latched into the address drivers during PHFSL and the outputs from the drivers drive lines /ID0/ through /ID3/ to the storage unit. When the address contained in the storage unit address register is the same as that in the storage unit address drivers, the device selected term (DVSEL) goes true. When the controller becomes busy (DCBUSY), the device selected term generates DVBUSY.

4-53 Error Circuits

The error circuits of the controller consist of flip-flops, buffered latches, and associated logic elements. These flip-flops, latches, and the signals controlled by them provide information to the IOP concerning error conditions that occur during execution of orders or as a result of power failure or programming errors. Error signals are provided during order-in service cycles of an input/output operation. Program response to these error conditions may cause data to be provided by execution of additional commands (TDV, AIO, TIO, HIO, or SIO). Error logic circuits are described in paragraphs 4-54 through 4-63.

4-54 Sector Unavailable Logic

Sector unavailable flip-flop SUN may be set in the preamble time interval during which PRE is set and RWE is reset. This interval precedes the incrementing of the sector and track addresses (see paragraph 4-31). Therefore, SUN is set if a sector address stored in the S-register or a track address stored in the T-register represents an address which does not exist in the storage unit. The capacity of the storage unit is indicated by the type. Type identification is returned from the selected device over the /TYP0/ and /TYP1/ lines.

During execution of a seek order, if the most significant bit of the new track address stored in the T-register (TRKOVF) is true, SUN is set through its M-input during the terminal order of the data service cycle. SUN will also be set when the disk drive indicates an address out of limits (LOGADDRINT) or when a RESTORE has been generated by the selection unit.

Track overflow (TRKOVF) may also be true when the track address is incremented out of limits during successive read or write operations. This will cause SUN to be set during the next preamble time interval (during which PRE is set and RWE is reset), or during a terminal order of a data service cycle for a sense order.

4-54 (cont'd)

Once SUN is set, it can be reset only by signal CLEAR.

4-55 Rate Error Logic

During execution of a write order or a checkwrite order, data from the IOP must be provided in time for a transfer from the K-register to the D-register at the rate determined by read/write clock RWCK. During execution of a read order, data must be accepted by the IOP before the FAM is filled, so additional data can be stored in the FAM at the rate established by read/write clock PWCK. Rate error flip-flop RER is set if either kind of rate error is detected.

During execution of a read order, data is transferred from the D-register to the J-register at BIT7RWE. If the J-register is still full (JFULL/DLYD) at BIT6RWE and the IOP has not signaled count done (CDN), the rate error flip-flop is set through its M-input.

During execution of a write order or a checkwrite order, a rate error is detected if the K-register does not have data available for transfer (NKFULL) to the D-register during:

a. Preamble sync pattern time (PSPB+PSPR)
b. Bit seven time of the data record (NPRE·NPOST·BIT7RWE)

Once RER is set, it can be reset only by signal CLEAR.

4-56 Checkwrite Error Logic

Checkwrite error flip-flop CER may be set through its M-input if a sector pulse or index pulse is received when RWE is set. This condition would occur if data strobes were missing during execution of a read order or checkwrite order. In this case, the B-counter value would be incorrect.

CER is set during execution of a checkwrite order if the data bits read from the storage file through flip-flop DAR do not match the data bits in the D-register read from D07 (as described in paragraph 4-48).

Once CER is set, it can be reset only by signal CLEAR.

4-57 Parity Error Logic

Parity error flip-flop PER can be set only during execution of a read order, and then only while the parity byte is being read from the addressed storage unit. The parity byte read from the device is strobed into DAR where it is compared with the parity byte generated during the read operation (as described in paragraph 4-49). If these two parity bytes do not compare, PER is set.

Once PER is set, it can be reset only by signal CLEAR.

4-58 Parity Transmission Error Logic

Parity transmission error latch (PTE) is set when an error is detected by the parity circuits (as described in paragraph 4-30). The data lines from the IOP are monitored during all order-out and data-out

transfers. Only when operating on the extended interface, and the IOP does not drive the /PC/ line, will parity checking not occur.

Once PTE is set, it can be reset only by signal CLEAR.

4-59 Preamble Sync Pattern Missed Logic

During execution of a read order or checkwrite order, a search is conducted for the preamble sync pattern (as described in paragraph 4-48). If the preamble sync pattern is not detected, flip-flop PSPM is set. The search for the sync pattern will normally terminate with a count of 14 in the B-counter. When the pattern is detected, the counter is reset (as described in paragraph 4-47). Should the sync pattern be missed, the counter will increment to 15 and at BIT7RWE the PSPM flip-flop will be set.

Once set, PSPM can be reset only by signal CLEAR.

4-60 Transmission Error Logic

The transmission error logic will raise signal TER when any of the following conditions exist:

a. Rate error detected (RER)

b. Checkwrite error detected (CER)

c. Parity error detected during execution of a READI order. Reported during order-in (PER)

d. Parity error detected during READI and the buffer is empty

e. Parity error detected in data received from the IOP (PER)

f. Preamble sync pattern missed (PSPM)

4-61 Write Protect Violate Logic

During execution of a write order, when PRE is set and the addressed device is holding the /TRP/ line true (indicating it is write protected), the WPV flip-flop will be set.

Once WPV is set, it can be reset only by signal CLEAR.

4-62 Unusual End Logic

When an unusual end condition is detected by the controller, it raises signal UNE/M1 when the subcontroller returns to phase PHFS and an order is being decoded (ORDENABLE). The raising of this signal will cause unusual end latch UNE to be set. Setting UNE will terminate operations (as described in paragraph 4-43).

4-62 (cont'd)

The conditions which will raise UNE/M1 are:

a. Illegal order decoded (ILO) (see paragraph 4-25)
b. Illegal bit used in the order (ORD0, ORD1, ORD2, ORD4)
c. Device not operational (NDVO:R)
d. Power failure (PWRMON from the device)
e. Sector unavailable (SUN)
f. Transmission error (TER)
g. Write protect violation (WPV)

Once UNE is set, it can be reset only by signal CLEAR.

4-63 Incorrect Length Logic

Incorrect length flip-flop (INL) is set for any of three conditions:

a. The number of data bytes transferred during execution of a read order, write order, or checkwrite order is not an integral multiple of 360 (for the medium speed device) or 1024 (for the extended performance device).

b. The number of bytes transferred during a seek order is not 2.

c. The number of bytes transferred during a sense order is not 3.

Although none of these conditions is necessarily an error, the information that INL was set may be required by a program. Therefore, while UNE will not be set, a signal is returned to the IOP over the /DA1/ line during an order-in service cycle.

Count done flip-flop (CDN), which should be set after all data bytes have been transferred following execution of any order, controls signals related to setting flip-flop INL. During execution of a seek order or a sense order, INL is set during the order-in service cycle if CDN is not set or if the seek/sense byte counter has not decremented to zero for a sense or to one for a seek.

During execution of a read order, INL is set if count done is received from the IOP while there is still data in the buffer, as indicated by KFULL or NR:EMPTY.

During execution of a write order or a checkwrite order, INL is set if count done is received from the IOP, the buffer is empty (R:EMPTY·NKFULL/DLYD), and data is to be transferred from the J-register to the D-register, as indicated by BIT7RWE·NPOST.

Flip-flop INL is reset during an order-out service cycle or by the signal CLEAR.

4-64 Device Interface Signals

Signals exchanged between the controller and any storage unit use a set of transmission lines common to all storage units. These are described briefly below:

/AN0/ – /AN3/	Sector address (angular position) data from the device. Compare with address in S-register to enable setting RWE.
/CLK/	2.5 MHz clock to selection unit: CONCLK (2.5).
/DA1/	Data signal from storage unit. Clocked into DAR flip-flop.
/DAM/	Manchester encoded data to the storage units. Used by medium speed devices only.
/DAT/	Data output to the storage unit from D07.
/DS/	Data strobe from selected device. Generates RWCK during read operations.
/DVO/	Selected device operational signal from storage unit.
/DVT/	Device test signal from storage unit.
/ID0/ – /ID2/	Device address signals from controller to storage units.
/NSEC3/	Least significant bit of sector address to selection unit: NSEC3.
/NSUNSET/	Used to set SUN.
/PWRMON/	Not used.
/REN/	Not used.
/SC1/	Track and sector shift clock to storage unit.
/SC2/	Not used.
/SLN/	Select now line to storage units.
/SP/	Sector pulse from storage unit.
/SUN/	Used by MDSU to reset ERRORSENSE.
/TRK/	Track address to storage unit from D07. Data shifted into storage unit by /SC1/.

/TRP/ Track protect signal from storage unit. Used in check to write protect violation.

/TYP0/, /TYP1/ Storage unit type identification. Used to select internal clock rate and to check for unavailable sector and track addresses.

/WEN/ Write enable signal to storage unit.

4-65 OFF-LINE OPERATION

The maintenance panel incorporated in the controller can be used either to monitor operation of the controller or to simulate IOP inputs to the controller. In either case, the maintenance panel is connected to the controller by the positioning of the on-line switch in the subcontroller and the MAINT/MONITOR switch on the maintenance panel. When the maintenance panel is used to monitor operation of the controller, indicators on the maintenance panel read selected signals of the controller during on-line operation. When the maintenance panel is used to simulate IOP inputs, no storage unit attached to the controller is accessible to the IOP.

4-66 ON-LINE/OFF-LINE CONTROL

The controller will be connected to, and disconnected from, the IOP in a transient free manner by sequencing the connect/disconnect circuit. This circuit is controlled by the term PT18S from switch S1 on the LT94 module in location 23C. This switch will provide a ground (from the cabinet power distribution panel) when in the up position (on-line), and an open when in the down position (off-line).

a. Connect. When a ground is provided by switch S1 (PT18S low), the relay driver on the AT83 module in location 26C supplies a ground path for the relays on the module.

1. Approximately 4.5 milliseconds after the ground is applied, term NINI will be grounded.

2. Approximately 0.5 milliseconds later, the term INI will go high and the short circuit between /AVI/ and /AVO/ will be removed.

3. Approximately 120 microseconds later the term INC will go high and NINC will go low. When terms INI and INC have reached the true state, the controller is connected to the IOP interface and the cable driver lines to the IOP will become active.

b. Disconnect. When signal PT18S becomes open, the ground for the relays on the AT83 module is removed.

1. Approximately 1.6 milliseconds after the ground is removed, INC is grounded and NINC goes true. All service calls will be inhibited to the IOP.

2. Approximately 4.2 milliseconds after INC is grounded, the term INI is grounded and /AVI/ will be short-circuited to /AVO/. The timing can vary as much as 250 microseconds.

3. Approximately 0.5 milliseconds after INI is grounded, NINI goes true.

When INI is grounded, the subcontroller is considered disconnected from the IOP by the fact that the cable drivers to the IOP have been inhibited. The /AVI/ input is short-circuited to /AVO/ so that the subcontroller is still physically connected to the priority cable without interferring with its operation.

4-67 MAINTENANCE PANEL OPERATIONS

The maintenance panel will be connected to the controller when the on-line switch (paragraph 4-66) is placed in the down position and the MAINT/MONITOR switch is in the MAINT position.

The maintenance panel can be used to monitor on-line operations when the MAINT/MONITOR switch is placed in the MONITOR position with the controller connected to the IOP (as described in paragraph 4-66). Placing the switch in the MAINT position with the controller on-line will not affect the operations. The MAINT position will be effective only when the controller is disconnected from the IOP (as described in paragraph 4-66).

Paragraph 2-4 describes the various switches, pushbuttons, and indicators on the maintenance panel. The SIO/HIO switch is used to select an SIO or HIO simulation of the IOP. The FS pushbutton will simulate the function strobe from the IOP.

The gating structure of the order register in the subcontroller allows for the insertion of an order from the maintenance panel during an order-out service cycle. The PHASESTEP flip-flop in the subcontroller may be clocked by a pulse generated from the maintenance panel STEP switch to allow single stepping through the subcontroller phases.

A complete description of the maintenance panel operation is contained in section II of the Field Engineering Maintenance Manual.

4-68 MULTIPLE DRIVE SELECTION UNIT (MDSU)

In the following description of operation of the multiple drive selection unit, reference will be made (by sheet number) to the logic diagrams, drawing 203329, for that unit. Interface lines between the selection unit and the device are normally high. They are driven low for a desired signal transfer.

4-69 UNIT SELECTION (Sheet 2)

Three device address bits are received from the controller over lines /ID0/ through /ID2/. The three identification bits and their complements are used to decode eight specific addresses, DEV1C through DEV4C and DEV1F through DEV4F. These addresses identify each of the four cartridge disk drives and the particular disk within each drive.

4-69 (cont'd)

The eight identification signals are sent to the address select switches where each may be selected or rejected as required by the system configuration. Note that only one of the signals may be true at any time.

The outputs from the address switches become set inputs to the select flip-flops. The least significant device address bit, ID2R, is used to set the DISKSEL flip-flop. All the select flip-flops are clocked by SLNR, which is driven low by the controller during an SIO operation indicating "select now".

One of the SELECTx flip-flops will be set to select one of four cartridge disk drives. When DISKSEL is set, the fixed disk within the drive is selected (possible only with the model 7252 cartridge disk drive).

Note that all even-numbered device addresses from the controller will select the cartridge disk. All odd-numbered device addresses from the controller will select the fixed disk. In effect, the LSB of the device address selects the disk while the two most significant bits select the drive.

The unit selection, drive and disk, will be displayed on the indicator module, 01A (see paragraph 4-78). The select flip-flops are erased during a power-up by the term NINITRST, which is true for approximately 50 microseconds.

4-70 TRACK ADDRESSING (Sheet 3)

A nine-bit track address is transmitted serially from the controller to the selection unit during the first nine bit times of a sector. (See timing chart sheet 59, drawing 204492, logic diagram, Cartridge Disk Drive Controller.) The track address is received on the /TRK/ line and is clocked into the shift register, TRK2 through TRK9 and HDSEL, by the clock SC1R.

The LSB of the received track address will be in HDSEL and is used to select the upper or lower surface read/write head. When HDSEL is false, the upper head is selected; when true, the lower head is selected. Even-numbered track addresses will select the upper head and odd-numbered track addresses will select the lower head.

The eight most significant bits of the track address will be transferred in parallel to the selected drive to become the cylinder address. The transfer is made by the term NSTROBE supplied to the disk drive. The head select term is not strobed into the disk drive but is held constant to continuously select the head.

The track register and the head select flip-flop will be reset by a RESTORE order (see paragraph 4-74).

Note that in the input gating to the track register and the head select flip-flop, the term STROBECLK must be true in order to transfer in the track address from the controller. This term will be true for six microseconds after the trailing edge of the sector pulse. This is ample time to shift in the nine bits (3.6 microseconds). The other input, TRKOUT-1, is used during seek verification as described in paragraph 4-77.

The clock term SC1R has three sources, each operational at a different time:

a. The line receiver for SC1 from the controller will be used during the transfer of the track address from the controller.

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4-70 (cont'd)

b. The read clock from the disk drive, RDCLK, will be used while RDPREP is true during cylinder reading.

c. The write data clock from the selection unit write circuits, GWRCLK, will be used while WRPREP is true during initialization of a pack.

The quiescent condition of SC1R is true; therefore, the register will be clocked on the leading edge of any clock pulse when the SC1R line is driven false. Note that the signal NCLKNINE is also normally true, and is driven during WRPREP or RDPREP, when the cylinder address is being written on or read from the disk.

4-71 SECTOR MARK (Sheet 4)

Two sector marks from the disk drive are used to generate the sector mark to initiate an operation within the controller and selection unit. The mechanical sector mark is used only during pack initialization. The electrical sector mark is used for every other operation.

The mechanical sector mark is received over the /NSECTORREC/ line. This line supplies one 40-microsecond, 0 volt pulse for each of the sector slots as they pass by the transducer.

The electrical sector mark, written on the data track during pack initialization, is a series of 64 data ones (four bytes), starting 25.6 microseconds after the trailing edge of the mechanical sector mark.

The sector mark is a 2.5-microsecond pulse (SECTOR) from a one-shot, triggered when SECTORTRIG is driven false. When the pack is being initialized, INITNC is true; when NSECTORREC goes true at the trailing edge of the mechanical sector pulse, SECTORTRIG is driven false. In normal operation, INITNC is false and INITNO is true and the mechanical sector mark will not trigger the one-shot.

In normal operation, SECTOR will be triggered when flip-flop SECTORRECFF is reset. The flip-flop is marked by the mechanical sector mark if the disk drive is ready to seek, read, or write, as indicated by NREADYSRW being low. The flip-flop is erased by SECTORRECE, which will be true when four consecutive data ones have been read from the disk pack.

The four-stage shift register, SP1 through SP4, is reset by the term which marked the sector recognition flip-flop, SECTORRECFF. Four consecutive data ones will load the register and generate the erase term for the flip-flop. This should occur 27.2 microseconds after the mechanical sector mark. SECTOR is 2.5 microseconds in duration. Therefore, controller sector timing, which begins with the trailing edge of the sector mark, will begin 29.7 microseconds after the trailing edge of the mechanical sector mark.

Note that the sector mark delivered to the controller, SPD, will be disabled by NLOCKOUTB1 being false. This condition will occur during pack initialization when WRCYL is true (see paragraph 4-76) or during a seek and cylinder verification operation when LOCKOUTB1 is true (see paragraph 4-77).

With the fall of SECTOR, the SECDLYD one-shot is triggered. This signal is used to generate STROBECLK which must remain true for the duration of the track address transfer from the controller

4-71 (cont'd)

to the selection unit as described in paragraph 4-70. When the 6-microsecond SECDLYD pulse falls, STROBE is triggered. The 1.5-microsecond pulse is used to strobe the track address into the disk drive and to reset the header error flip-flops (see paragraph 4-74).

The three one-shots in the sector mark circuit are individually adjustable and should be set to the specified duration in order to maintain the critical timing relationships. This is especially true of SECDLYD.

4-72 READ DECODING (Sheet 6)

The read decoding timing diagram (figure 4-9) shows the complete decoding operation of the selection unit. Received from the disk drive are the signals NREADCLOCK and NREADDATA. These signals are inverted to provide RDCLK and DATADETM. Pulses on these two lines are nominally 100 nanoseconds in width. The clock pulses occur every 400 nanoseconds, marking the bit, or cell, time. Data ones are pulses within cells.

The presence of a data one will mark the DATADET flip-flop. Two hundred nanoseconds later RDCLK will reset DATADET and mark DATAR. The set time for DATADET is 200 nanoseconds while DATAR will be set for a full bit time, 400 nanoseconds. Consecutive ones will leave DATAR set.

The clock received from the disk is nominally 100 nanoseconds in width, but the tolerance is 50 nanoseconds. To provide a more stable pulse width, the read clock triggers a one-shot whose output is 120 nanoseconds. This one-shot is adjustable and must be set to the specified time.

4-73 WRITE ENCODING (Sheet 6)

The write circuits will be enabled only at the time that either the write enable signal WEN is being received from the controller, or when the write cylinder flip-flop WRCYL is set during pack initialization. When the write circuits are enabled, NWRGATE will be low to the disk drives. At all other times, NREADGATE will be low.

Data to be written will be write data from the controller (DAT), cylinder address (TRKOUT1), or the electrical sector mark (ONEWRT). The data encoding timing diagram (figure 4-10) shows the complete encoding operation of the selection unit. Data to be written, ORDAT, will be clocked into the data flip-flop DATFF.

The 2.5 MHz controller clock is used to transfer data into DATFF. The clock is also used to synchronize the 5.0 MHz oscillator on the AT41 module in location 21A. Note the phase relationship of the 5.0 MHz clock and the 2.5 MHz clock: the trailing edge of the 5.0 MHz clock occurs at the same time as the leading or trailing edge of the 2.5 MHz clock.

The two clocks are gated together to generate GWRCLK, a continuous stream of 100-nanosecond pulses spaced 400 nanoseconds apart. The output of DATAFF will gate CLK(5.0) pulses to generate DATAW. Two clocks will be gated for each data one, one of these pulses being coincident with GWRCLK. The combined clock and data signal WDCLK will be transmitted to the disk drive over the NWDCLK line.

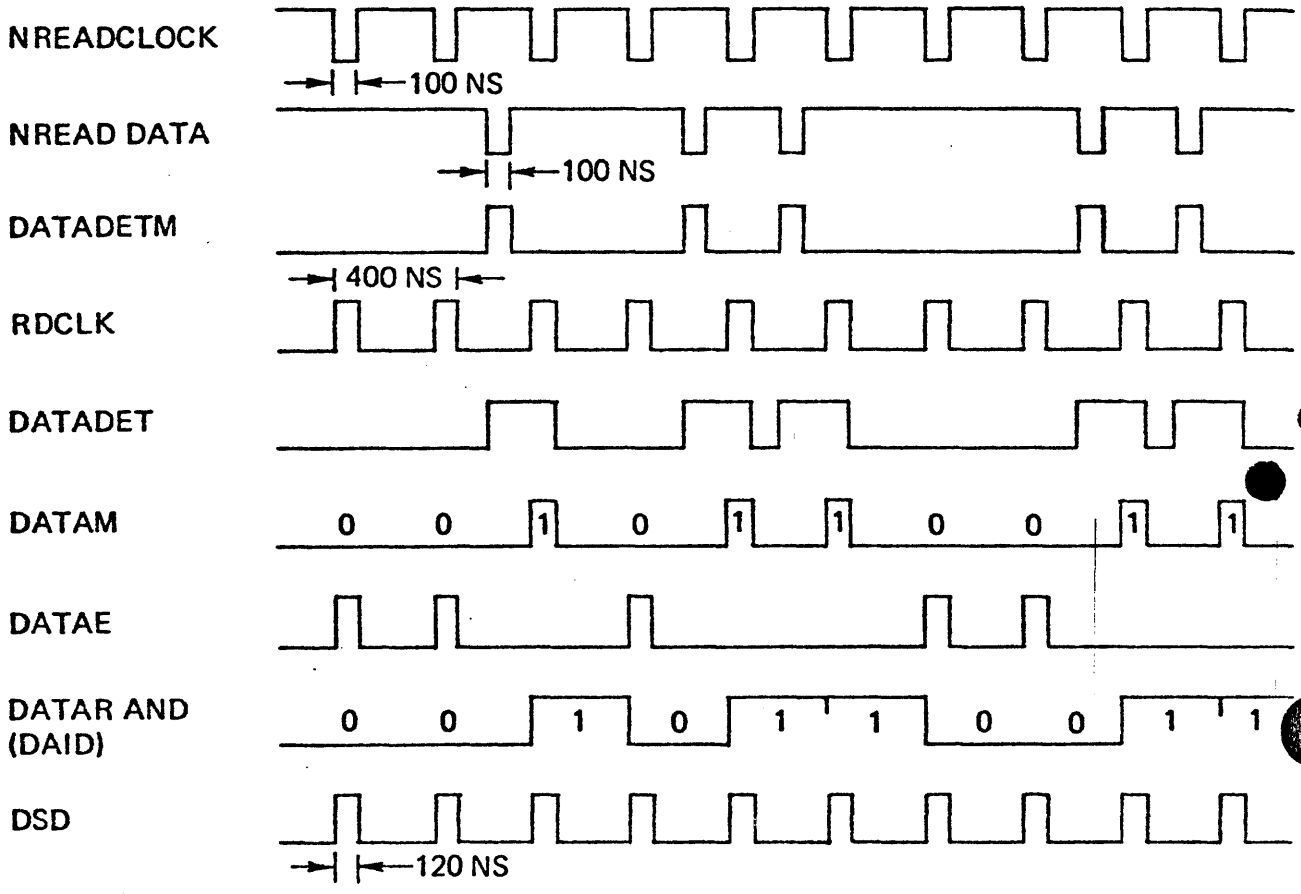

Figure 4-9. Read Timing

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Xerox Corporation
701 South Aviation Boulevard
El Segundo, California 9024[illegible]

Title

THEORY OF OPERATION
CARTRIDGE DISK
CONTROLLER

Xerox Corporation
El Segundo, California

XEROX

204262 A

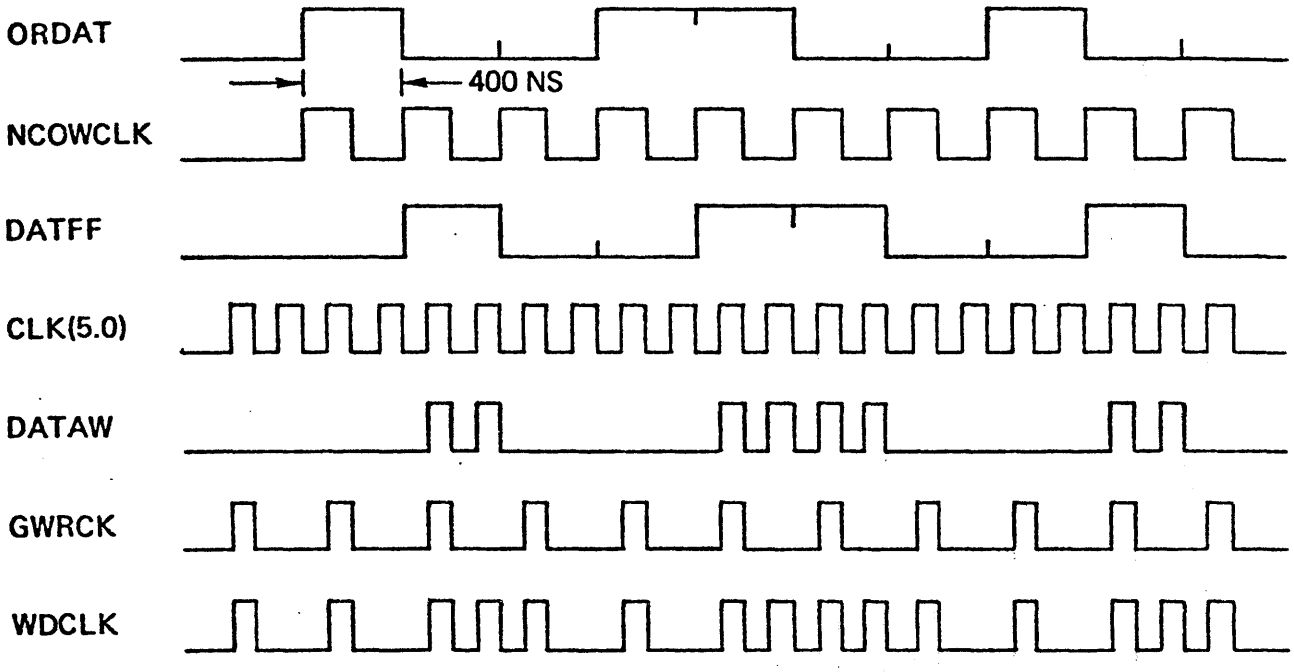

Figure 4-10. Write Timing

XEROX

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701 South Aviation Boulevard
El Segundo, California 90245

Title
THEORY OF OPERATION
CARTRIDGE DISK
CONTROLLER

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El Segundo, California

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4-74 SEEK OPERATION (Sheets 2, 3, and 4)

Each time the controller receives a sector mark (when the controller is busy, except during data out of the seek order), it will transfer the track address into the track register of the selection unit. This address will be strobed into the selected disk drive shortly after it is received by the selection unit. When the new address is the same as the old address, no seek occurs. When the new address is not the same as the old address, the disk drive will perform a seek operation.

When the disk drive performs a seek, signal NREADYSRW goes high. This marks the flip-flop LOCKOUT which in turn marks SELLOCK (see sheet 4). SELLOCK is used to generate LOCKOUTB1 (sheet 2) which drives NLOCKOUTB1 false. This disables the gating of the sector address, received from the disk drive, to the controller. The complement of the LSB of sector address in the controller is enabled back to the controller. This prevents a sector compare in the controller for sector 0000. NLOCKOUTB1 also prevents sector pulses from being transferred to the controller.

When the seek had been completed and the disk drive is ready for another seek, read, or write operation, NREADYSRW goes low, removing the mark to LOCKOUT and enabling LOCKOUTENB. The next sector mark will clock LOCKOUT reset (see figure 4-11).

SELLOCK and NLOCKOUT will mark the verification flip-flop VERIFYFF (sheet 3). VERIFYFF enables the set input to HDRER1 and also generates LOCKOUTB1. While VERIFYFF is set, a comparison is made between the cylinder address in TRK2 through TRK9 with the address recorded on the disk. This will occur when RDPREP is set, as described in paragraph 4-77.

As the cylinder address is read from the disk, the address in the selection unit is shifted through TRK9 and TRKOUT. TRKOUT provides the additional delay to match the sync bit read from the disk. The two addresses are exclusive OR gated to generate ORERR should the data not match. An error will cause the flip-flop HDRER1 to be set. TRKOUT1 is also shifted back into the track register to save the address.

The next sector mark will clock SELLOCK reset. This removes the mark input term to VERIFYFF but that flip-flop remains set. The strobe which follows the sector mark will erase HDRER1 if it had been set. Resetting HDRER1 will clock HDRERHOLD, saving the result of the first cylinder address check. Another comparison is made between the address in the selection unit and the address from the disk.

If the second check is in error, HDRER1 will be set. If the two successive checks did not compare RESTHDR is generated and RESTORE is marked. A restore order is sent to the disk drive over NRESTORE. The disk drive will raise NREADYSRW and the cylinder address will be checked when NREADYSRW returns to a low. RESTORE clears the track address register (sheet 3) so that the stored address will match that received from the disk drive.

If either of the two address comparisons is satisfactory, RESTORE will not be marked and the following sector mark will erase VERIFYFF. With VERIFYFF reset, LOCKOUTB1 will be false and the sector address from the disk drive and sector pulses are enabled to the controller. Note that sector pulses to the controller are inhibited during the seek operation and for the first two sectors following the completion of the seek.

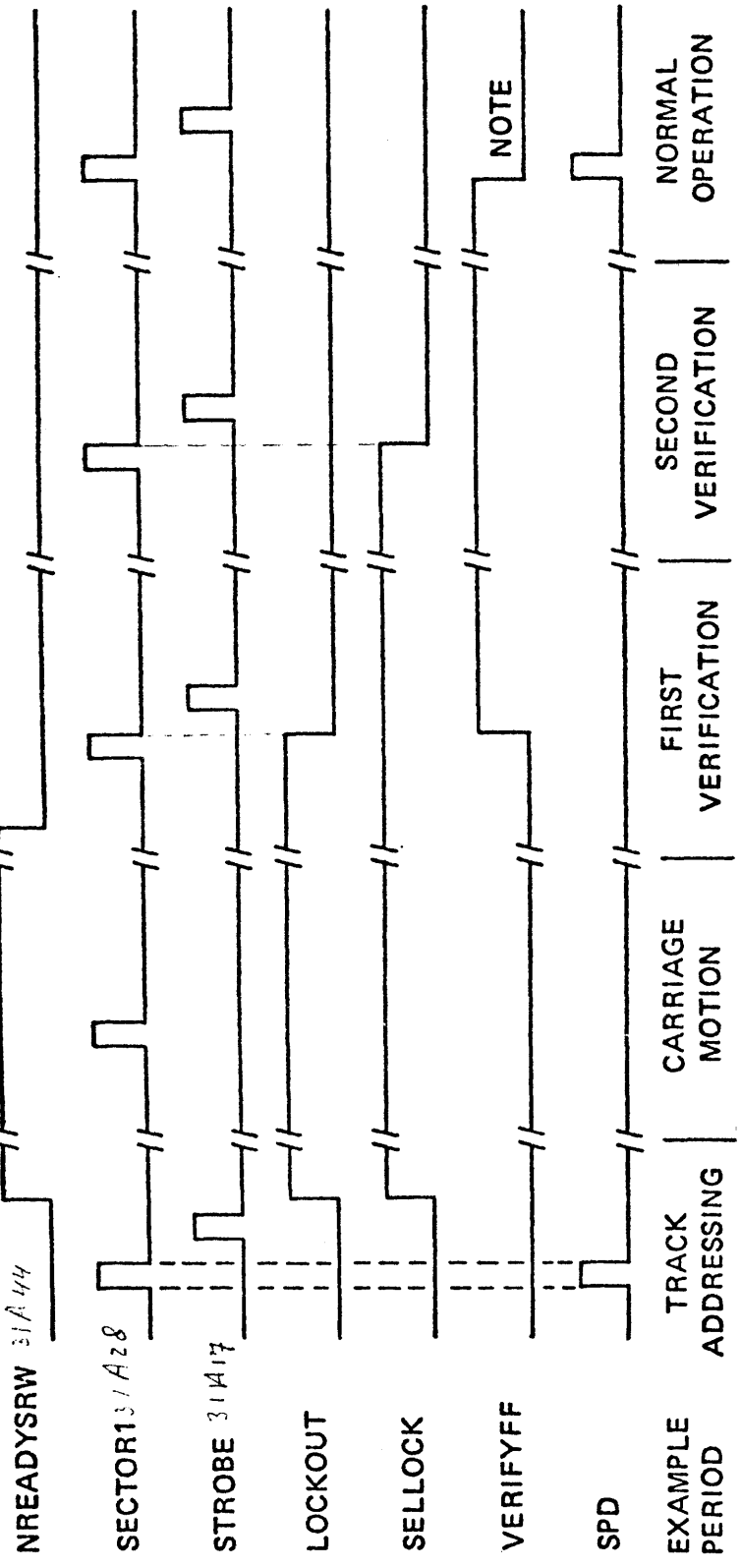

Figure 4-11. Cylinder Verification Timing

XEROX

Xerox Corporation
701 South Aviation Boulevard
El Segundo, California 90245

Title
THEORY OF OPERATION
CARTRIDGE DISK
CONTROLLER

Xerox Corporation
El Segundo, California

XEROX

204262 | A

4-74 (cont'd)
Figure 4-11 shows the timing relationships for a seek and cylinder verification. The chart is divided into six example periods.

4-75 PSEUDO-SECTOR COUNTER (Sheet 5)

The pseudo-sector counter is a twelve-bit ripple counter which counts bit times (400-nanosecond increments). The counter is reset and held to zero during a device select (NSLN is true), a seek operation (LOCKOUT), a write operation (WENR), and a sector mark (SECTOR1). The counter is used during disk cartridge initialization to locate the cylinder address in the intersector gap and the electrical sector mark behind the mechanical sector mark. It is used during seek verification to locate the cylinder address.

Associated with the pseudo-sector counter is a four-stage counter used to count nine pulses. This counter is clocked by NCLKNINE, gated read or write clocks (see paragraph 4-70).

The two counters work together to locate the cylinder address for writing or reading. The pseudo-sector counter enables either WRPREP or RDPREP which in turn enable NCLKNINE. Nine clock pulses are counted and WRPREP or RDPREP is reset.

4-76 WRITE CYLINDER ADDRESS

During pack initialization, the INITIALIZE switch is in the one position. This places a true into the set input of WRCYL (sheet 6). Following the sector mark, the controller transfers a track address into the track register (see paragraph 4-70). A normal controller data write operation takes place with the controller holding WENR high until the end of the data record. When WENR goes false, WRCYL is clocked to the set state. This enables the write data clock GWRCLK. Removing WENR also permits the pseudo-sector counter to count.

The gate T200 is enabled 204.8 microseconds after the counter starts. The next clock pulse will clock WRPREP set. This enables CLKNINE (sheet 3) resulting in clock pulses for the nine counter and generating SC1R for the track register and TRKOUT. The track address is shifted out of the track register through TR9 and TRKOUT. Note that TRKOUT1 is enabled at the same time as the clock, and that TRKOUT1 is returned to the track register, thereby saving the contents of the track register.

TRKOUT1 is one of the three inputs that generate ORDAT for the write circuits and the address is written onto the disk pack as cylinder address. Note that TRKOUT was marked by STROBECLK. The first bit written will always be a one, followed by eight bits of address from the track register. This leading one is used by RDPREP, as described in paragraph 4-77.

After the cylinder address had been transferred, the nine counter generates NINE which erases WRPREP. This inhibits any further clocks to the track register and to the nine counter. A count of nine will remain in the counter until the next sector mark, holding WRPREP and TRKOUT erased.

The sector mark following the cylinder address write operation will reset the pseudo-sector counter and the nine counter. It will also clock ONEWRTS set (SECTORREC·WRCYL). When FF0128 sets, 25.6 microseconds after the sector mark, ONEWRT is set (sheet 6). ONEWRT provides a constant data

one into the write circuits (ORDAT). A series of data ones will be written until ONEWRT is erased by FF0064, 12.8 microseconds after FF0128. Four bytes of data ones at the start of a sector is the electrical sector mark.

At time 409.6 following the mechanical sector mark, FF2048 is set and WRCYL will be erased. This enables the next sector pulse to be sent to the controller. The sector counter within the controller was incremented when WENR was raised and now contains the next sector address. When a sector compare occurs, a write operation begins and WENR is raised. When WENR drops at the end of the data record, another cylinder address and sector mark writing operation begins.

Sixteen revolutions of the disk pack are required to write cylinder addresses and electrical sector marks in every sector of one track address. When the track address is incremented, the other read/write head is selected. Every other incremented track address will result in a seek operation. In order to prevent erroneously setting the header error flip-flops and thereby generating a restore order, the VERIFY switch must be in the zero (down) position. This prevents setting RDPREP as described in paragraph 4-77.

4-77 READ CYLINDER ADDRESS (Sheet 5)

Except during pack initialization, the read cylinder address circuits will be enabled by the VERIFY switch being in the one position. This input will set RDPREPENA when the pseudo-sector count reaches T1350. This will occur 1356.8 microseconds after the counter is enabled following its reset by SECTOR1. The read "window" will be opened before the cylinder address appears under the read head. This allows for any variation in the write or read timing.

With RDPREPENA set and providing a gating term for RDPREPCLK, the first data one of the cylinder address (DATAR) will cause RDPREP to be set. RDPREP enables the clocks to the track register, TRKOUT, and the nine counter. When the cylinder address has been read and compared with TRKOUT as described in paragraph 4-74, RDPREPENA and RDPREP are erased.

4-78 STATUS AND ERROR CIRCUITS

Three status signals are returned to the controller from the selection unit. They are:

a. /DVT/, indicating that the device addressed is in the system, as determined by address switch position (sheet 2)

b. /DVO/, indicating that the file is ready, a device select has been made, and both INITIALIZE and VERIFY switches are not on at the same time (sheet 7)

c. /TRP/, indicating that a write protect violation has occured (sheet 7)

d. /NSUNSET/, low to indicate that a track address out of limits was received, or a RESTORE was generated by a cylinder address verification error (sheet 7)

Three error flip-flops (sheet 7) will store error conditions for display on the indicator module, AO1:

a. LOGADRINTERR, set when the disk drive indicates that track address out of limits was received

4-78 (cont'd)

b. SEEKINCERR, set when the disk drive indicates that a seek has not been completed for any reason

c. ADCKERR, set by the selection unit when the address in the track register does not compare with that read from the device

If any of the error flip-flops is set, one of four unit error flip-flops will be set by the addressed unit select line. The set error flip-flop will also disable the unit select lines to the indicators. Therefore, if an error occurs, the indicator lamps will indicate what error has occurred and in what disk drive unit. Any change in unit address will not alter the readout on the indicator module.

Error condition indications can be cleared only by resetting both the error flip-flop and the unit error flip-flop. This can be done with manual RESET switch, module AO2, or with a power-up reset (sheet 2).

4-79 SECTOR FORMAT AND TIMING (Figure 4-12)

The sector format is divided into three significant sections:

a. Data file, as determined by the controller

b. Cylinder address

c. Electrical sector pulse

The sector format as determined by the controller contains the following parts with byte count and time shown:

a.	Gap for track address transfer and sector compare	10 bytes	32.0 μs
b.	Preamble	4 bytes	12.8 μs
c.	Data record	360 bytes	1152.0 μs
d.	Parity byte	1 byte	3.2 μs
e.	Postamble	1 byte	3.2 μs
		376 bytes	1203.2 μs

Between the fall of the sector pulse and the start of sector timing, one bit time (see note) is used by the controller to reset the byte counter and transfer the track address to the data shift register. This additional 400 nanoseconds brings the total time to 1203.6 microseconds for the complete record, from the fall of the sector mark to the end of the write or read enable (WEND or REND).

NOTE

The time from the trailing edge of the sector pulse until BXO will vary from one to two bit times. Two clock pulses are required to set TSE and then reset the counter. For this discussion, one bit time is used.

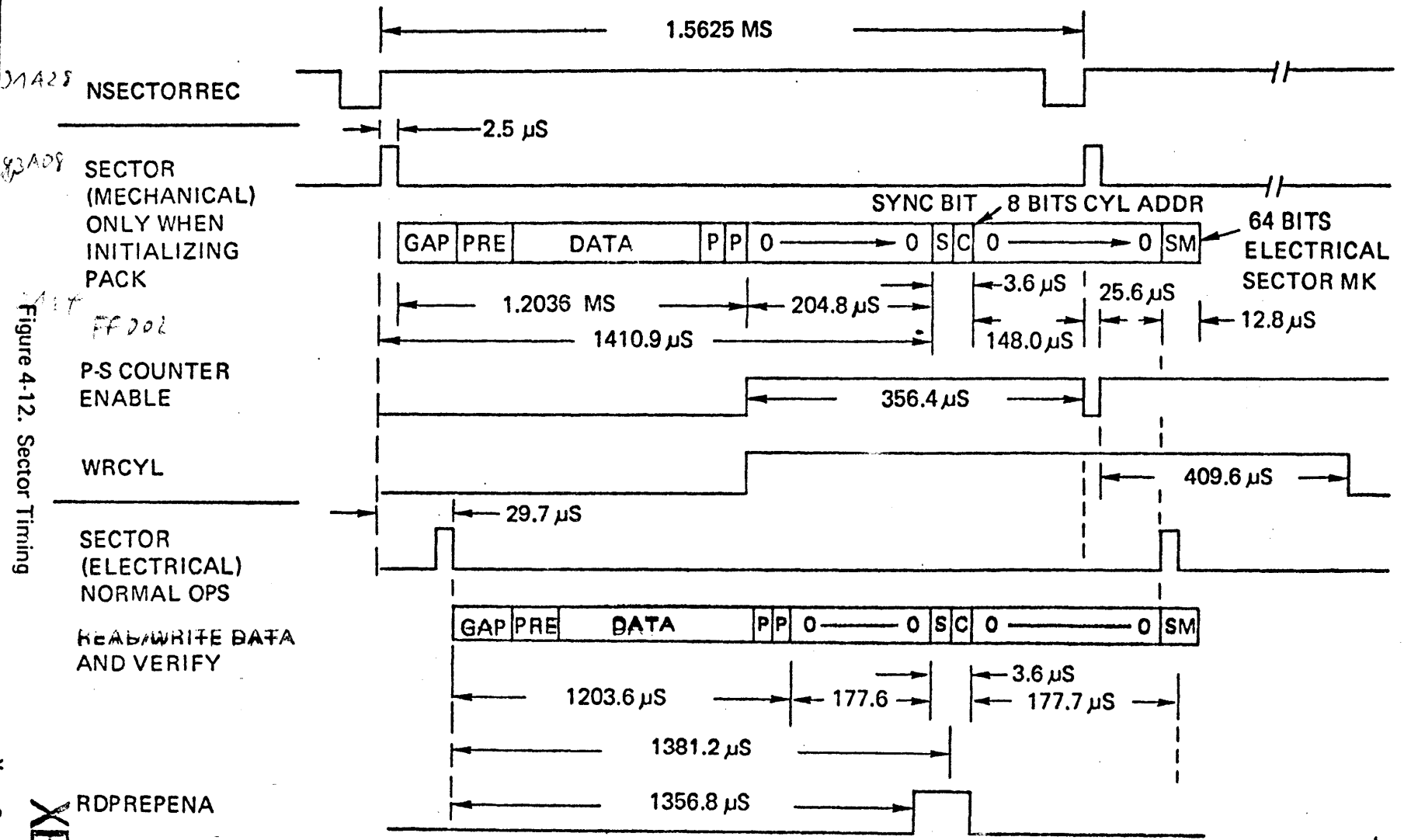

Figure 4-12. Sector Timing

Title
THEORY OF OPERATION
CARTRIDGE DISK
CONTROLLER

Xerox Corporation
El Segundo, California

204262

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Sheet 89 of 90

4-79 (cont'd)

At 2400 rpm each revolution of the disk takes 25 milliseconds. Each of the 16 sectors takes 1.5625 milliseconds. The sector pulse sent to the controller and used by the selection unit is 2.5 microseconds in duration. The sector pulse and data file will require 1206.1 μs of the sector time. This leaves a gap of 356.4 μs in which the cylinder address is positioned.

When the pack is being initialized, the mechanical sector mark is used to start the timing. NSECTORREC will be low for 40 μs. At the trailing edge, SECTOR is triggered to produce the 2.5 μs sector. At the trailing edge of SECTOR (SPD to the controller), the controller timing starts. The write enable signal drops 1203.2 μs later.

When WENR drops, the selection unit pseudo-sector counter is enabled. At time 204.8, the cylinder address is enabled and written onto the disk. This places the cylinder address 1410.9 μs into the sector, following the trailing edge of the mechanical sector mark.

With the nine-bit cylinder address using 3.6 μs, the gap following the address will be 148.0 μs to the trailing edge of the next mechanical sector mark, or 150.5 μs to the trailing edge of the next sector pulse. While the sector pulse is present, the pseudo-sector counter is reset and held at zero. Therefore, the counter did not reach time 409.6 to reset WRCYL.

Following the sector pulse, the counter is enabled and the electrical sector pulse is written 25.6 μs later. The 64 bits of the sector mark require 12.8 μs. When the counter reaches time 409.6, WRCYL is erased and the operation proceeds as described in paragraph 4-14.

During normal operation, the electrical sector mark is used. The sector mark begins 25.6 μs after the mechanical sector mark. Four bits are required to trigger SECTOR, this taking 1.6 μs. Therefore, the trailing edge of the electrical sector pulse will occur 29.7 μs after the trailing edge of the mechanical sector mark. This effectively places the cylinder address 1381.2 μs after the electrical sector mark. This is sufficient time to write data into or read data from the sector. The cylinder address read window is opened at time 1356.8, and the address read when the first data one sets RDPREP as described in paragraph 4-77.

The gap from the data file to cylinder address is 177.6 μs and from the cylinder address to sector mark, 177.7 μs, when the electrical sector mark is being used.

SECTION II

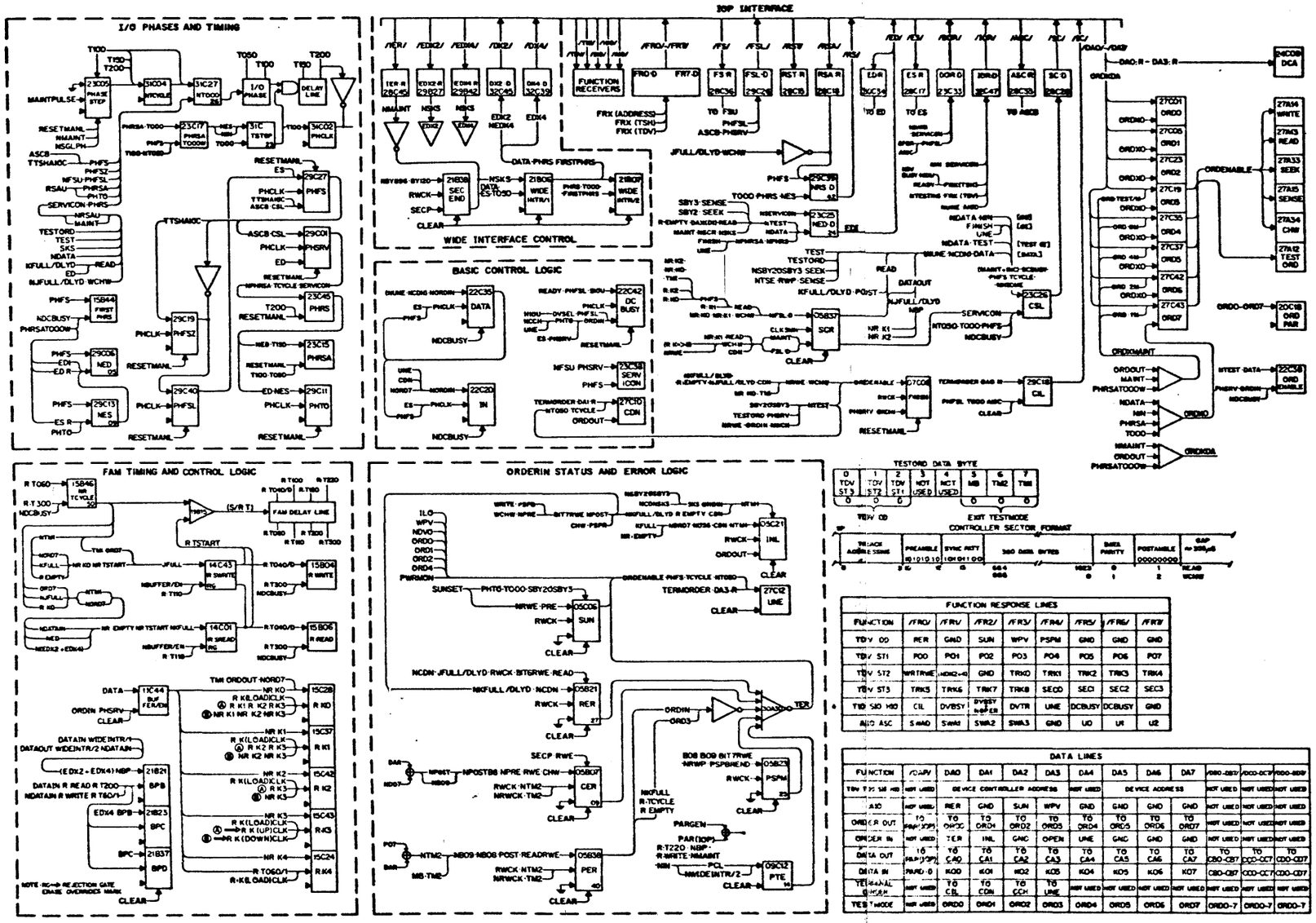
FIELD MAINTENANCE PROCEDURES

SECTION III

ENGINEERING TECHNICAL INFORMATION

REVISIONS					204260	A
LTR	REV.	DESCRIPTION	CHK	DATE	APPROVED	
	A	MANUFACTURING RELEASE - NO E.O.		11-7-73		

7250A01 CARTRIDGE DISK CONTROLLER



FUNCTION	/FRO/	/FRV/	/FR2/	/FR3/	/FR4/	/FRS/	/FR6/	/FR8/
TDV OD	RER	GND	SUN	WPV	PSPM	GND	GND	GND
TDV ST1	POO	PO1	PO2	PO3	PO4	PO5	PO6	PO7
TDV ST2	WRTRWE	INDX2+4	GND	TRK0	TRK1	TRK2	TRK3	TRK4
TDV ST3	TRK5	TRK6	TRK7	TRK8	SECO	SEC1	SEC2	SEC3
TDV SID HID	CIL	DVBSY	DVBSY buffer	DVTR	UNE	DCBUSY	DCBUSY	GND
AID ASC	S WA0	S WA1	S WA2	S WA3	GND	UO	U1	U2

FUNCTION	/OARV	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7	/DBO-DB7	/DCO-DC7	/DDO-DD7
TDV ST3 SID HID	NOT USED	DEVICE CONTROLLER ADDRESS				NOT USED	DEVICE ADDRESS			NOT USED	NOT USED	NOT USED
AID	NOT USED	RER	GND	SUN	WPV	GND	GND	GND	GND	NOT USED	NOT USED	NOT USED
ORDER OUT	TO ORDIN	TO ORDO	TO ORD1	TO ORD2	TO ORD3	TO ORD4	TO ORD5	TO ORD6	TO ORD7	NOT USED	NOT USED	NOT USED
ORDER IN	NOT USED	TER	INL	GNC	OPEN	UNE	GAC	GND	GND	NOT USED	NOT USED	NOT USED
DATA OUT	TO DRIVER	TO CA0	TO CA1	TO CA2	TO CA3	TO CA4	TO CA5	TO CA6	TO CA7	TO CB0-CB7	TO CC0-CC7	TO CD0-CD7
DATA IN	PAUSE-0	KO0	KO1	KO2	KO3	KO4	KO5	KO6	KO7	CB0-CB7	CC0-CC7	CD0-CD7
TESTMODE CHAIN	NOT USED	TO CIL	TO CDN	TO CCH	TO UNE	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
TESTMODE	NOT USED	ORD0	ORD1	ORD2	ORD3	ORD4	ORD5	ORD6	ORD7	ORDO-7	ORDO-7	ORDO-7

DIST CODE 409

MATERIAL LIST

NOTES UNLESS SPECIFIED
1. TOLERANCES .XX ±.08 DIMENSIONED ANGLES ±1/2° .XXX ±.010
2. BREAK ALL SHARP EDGES .015 APPROX.
3. FINISH SURFACES
4. ALL DIM. IN INCHES
5. ALL TRUE POSITION TOLERANCES APPLY AT MMC

DRAWN	S. NAKESS	11-5-73
CHECK		11-7-73
APPR.		11-12-73

MATERIAL
FINISH
MODEL NO. FIRST USE 7250
NEXT ASSY. FIRST USE 202624

XEROX

TITLE
CARTRIDGE DISK
FUNCTIONAL DIAGRAM

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204260	A
SCALE NONE	DO NOT SCALE DRAWING	SHEET 1 OF 3	

REVISIONS					204260 A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHEET NO. 1			

7250A01 CARTRIDGE DISK CONTROL_____ER

REV-G 11/29/72

FROM IOP

TO IOP

DEVICE INTERFACE

NOT USED

BYTES

BITS

SEEK SENSE BYTE CTR USAGE			
S00	S01	DECODE	TRANSFERS
1	1	SBY1	SENSE BYTE 1
1	0	SBY2	SENSE BYTE 2 LSB1
0	1	SBY3	SENSE BYTE 3 LSB2
0	0	SBY4	

SERO - RUP 2.5 μs

SERO - PRE 30 μs

DIST CODE

MATERIAL LIST

NOTES UNLESS SPECIFIED

1. TOLERANCES .XX ±.03 DIMENSIONED ANGLES ±1/2° .XXX ±.010 .X ±.06
2. BREAK ALL SHARP EDGES .010 APPROX.
3. RACK SURFACES
4. ALL DIM. IN INCHES
5. ALL TRUE POSITION TOLERANCES APPLY AT MMC

DRAWN

CHECK

APPR.

MATERIAL

FINISH

MODEL NO. FIRST USE SEE SHEET 1

NEXT ASSY. FIRST USE SEE SHEET 1

XEROX

TITLE

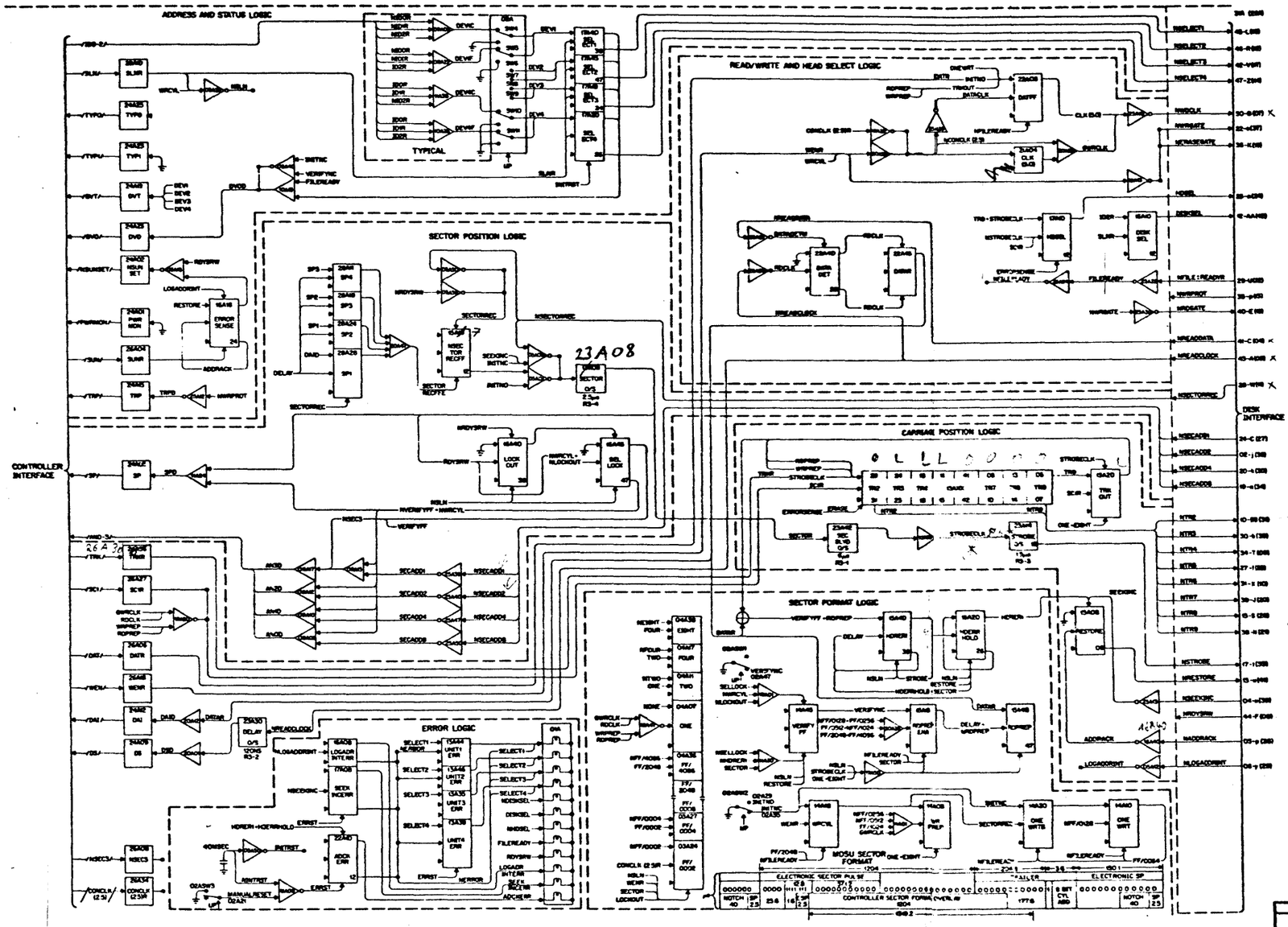
CARTRIDGE DISK FUNCTIONAL DIAGRAM

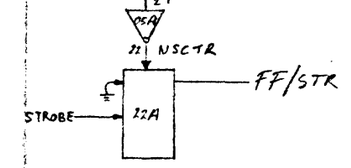
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204260	A

SCALE NONE | DO NOT SCALE DRAWING | SHEET 2 OF 3

REVISIONS					204260 A
LTR.	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHEET NO. 1			

7250A01 MULTIPLE DRIVE SELECTION UNIT





DIST CODE

MATERIAL LIST

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3. MACH. SURFACES √
4. ALL DIM. IN INCHES
5. ALL TRUE POSITION TOLERANCES APPLY AT MMC

DRAWN
CHECK
APPR.
MATERIAL
FINISH

MODEL NO. FIRST USE SEE SHEET 1
NEXT ASSY. FIRST USE SEE SHEET 1

XEROX

TITLE

CARTRIDGE DISK FUNCTIONAL DIAGRAM

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204260	A
SCALE NONE	DO NOT SCALE DRAWING	SHEET 3 OF 3	

NOTES:

1. REV. LETTERS LISTED INDICATE STATUS OF EACH SHEET OF THIS MULTIPLE SHEET DRAWING.
2. CHECK INDIVIDUAL SHEETS FOR REVISION LETTER AGAINST THIS SHEET BEFORE USING THIS DRAWING.

REVISION INDEX

PAGE	CHG	PAGE	CHG	PAGE	CHG	PAGE	CHG	PAGE	CHG	PAGE	CHG	PAGE	CHG
1	A	16	A	31	A	46	A	61	A				
2	A	17	A	32	A	47	A						
3	A	18	A	33	A	48	A						
4	A	19	A	34	A	49	A						
5	A	20	A	35	A	50	A						
6	A	21	A	36	A	51	A						
7	A	22	A	37	A	52	A						
8	A	23	A	38	A	53	A						
9	A	24	A	39	A	54	A						
10	A	25	A	40	A	55	A						
11	A	26	A	41	A	56	A						
12	A	27	A	42	A	57	A						
13	A	28	A	43	A	58	A						
14	A	29	A	44	A	59	A						
15	A	30	A	45	A	60	A						

REVISIONS					
LAL	REV	DESCRIPTION	CHK	DATE	APP'D
X	A	RELEASED TO MFG. NO E.O.	JM	1-31-77	

204492 A

XEROX

Xerox Corporation
701 South Aviation Boulevard
El Segundo California 90245

MATERIAL LIST

	DRAWN	1-15-74
NOTES UNLESS SPECIFIED	CHECK	1-21-74
7	APPR.	1-31-74
	MATERIAL	

MODEL NO.	FINISH
PRINT USE 7250	
NEXT ASSY.	
PRINT USE 202624	

TITLE
SDS SCIENTIFIC DATA SYSTEMS
SANTA MONICA, CALIFORNIA

DIAGRAM, LOGIC — CARTRIDE DISK CONTROLLER

SCALE	SIZE	DWG. NO.	REV.
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DO NOT SCALE DRAWING		SHEET 1 OF 61	

DIST CODE 409

204492 A

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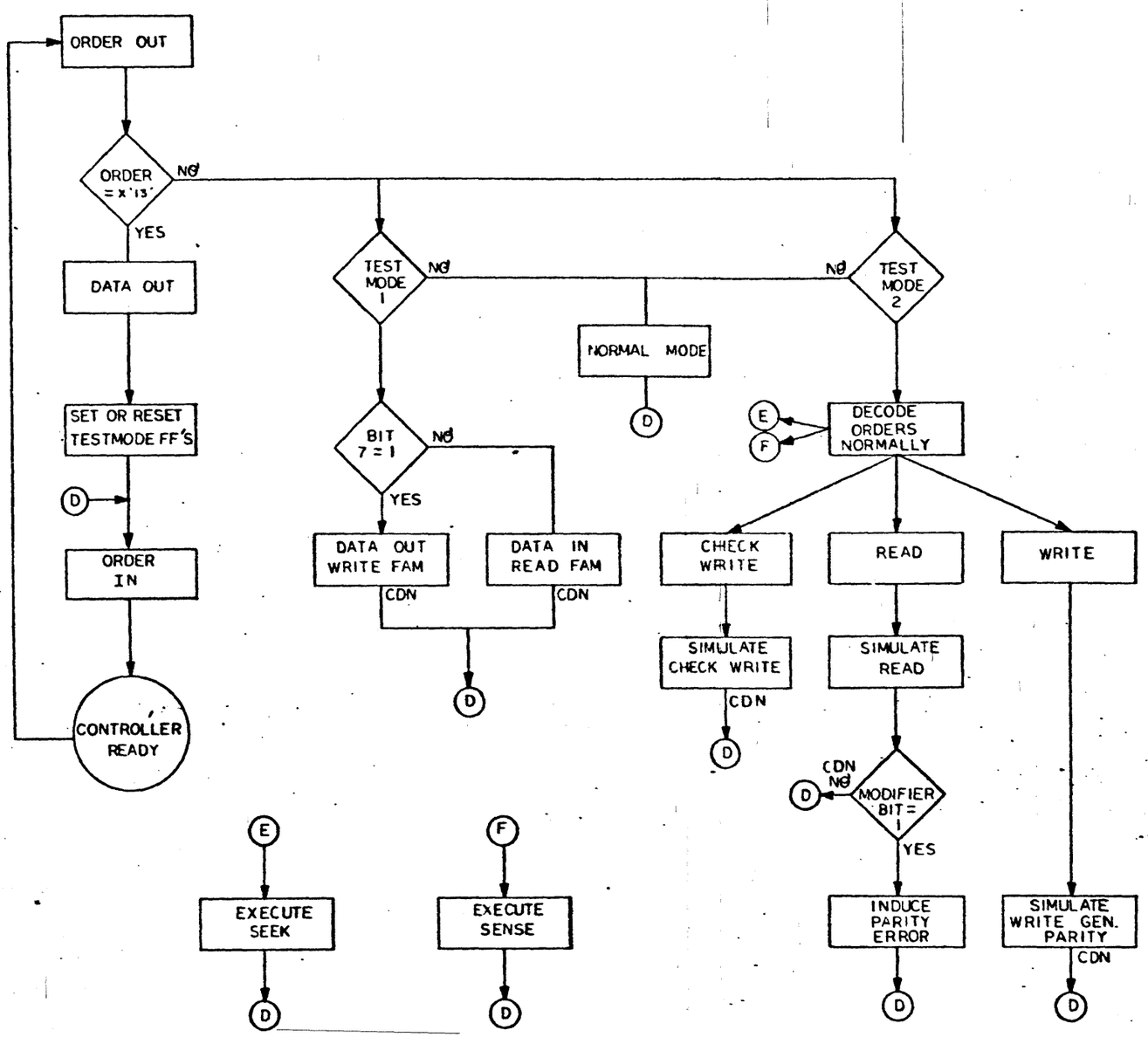

7250

TESTMODE (DIAGNOSTIC)

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE
DIAGRAM, LOGIC—
CARTRIDGE DISK
CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 2 OF 61

204492 A

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LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
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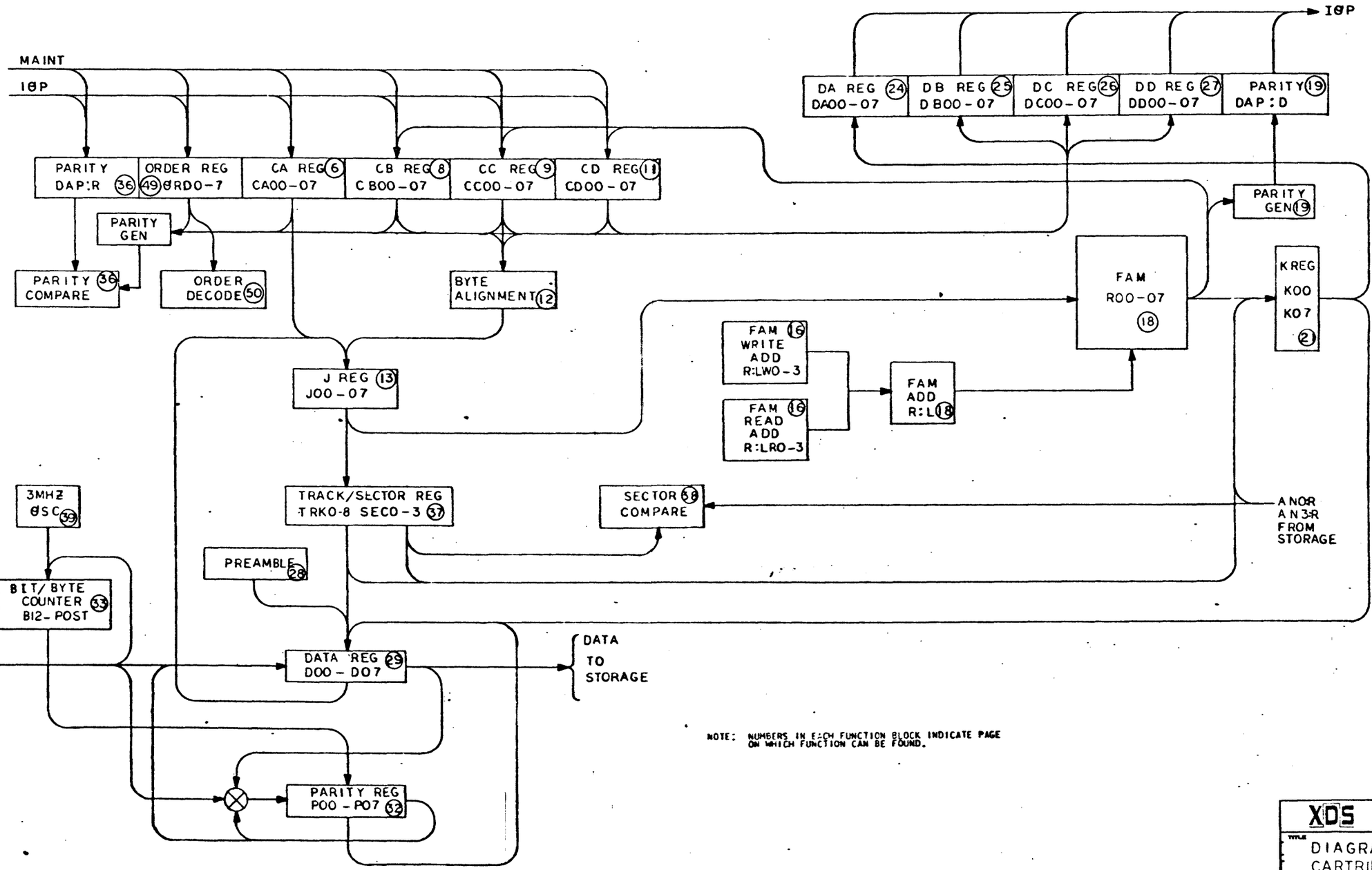

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XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

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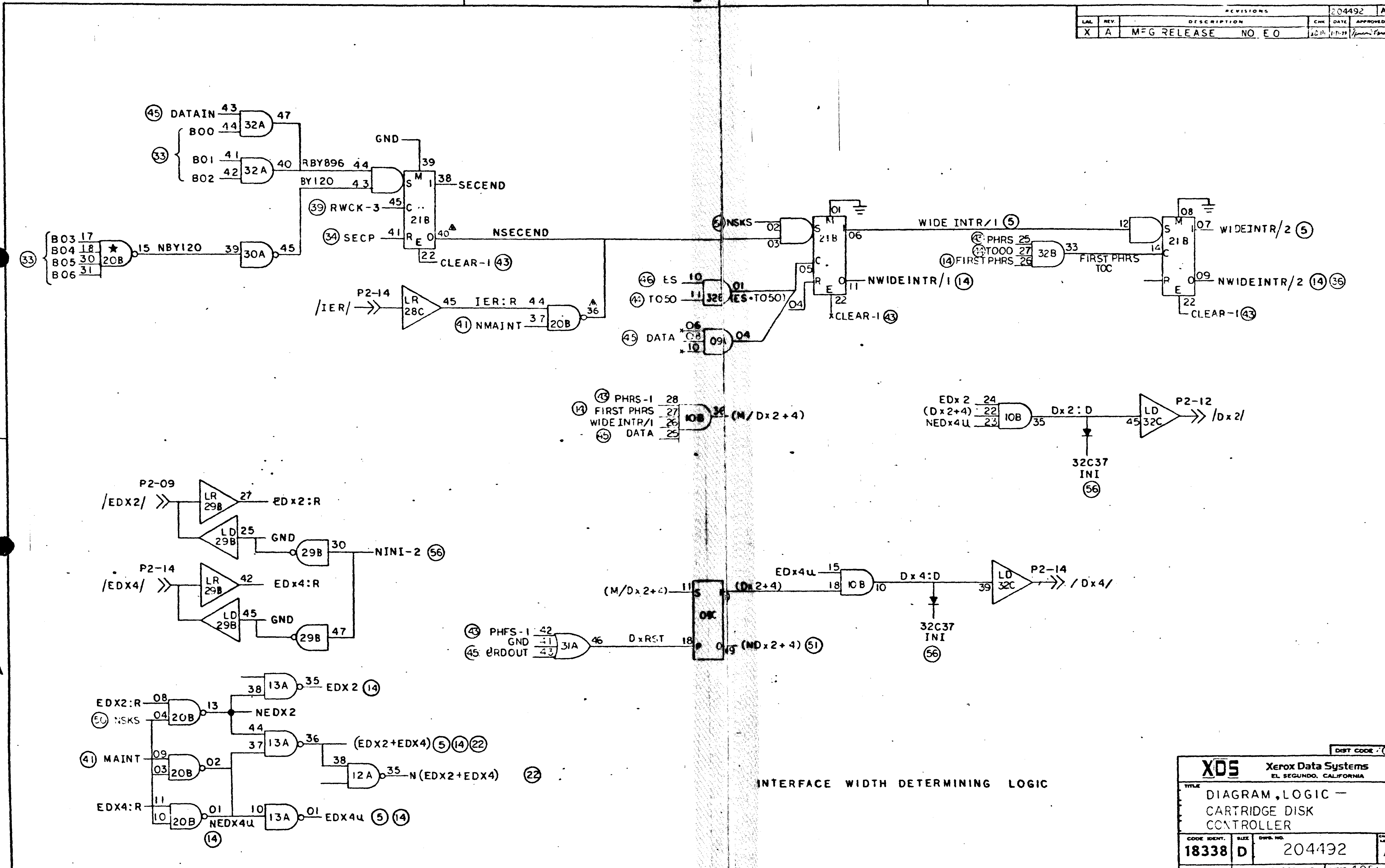
SCALE — DO NOT SCALE DRAWING SHEET 3

L Hunter 4-10-70



INTERFACE WIDTH DETERMINING LOGIC

LTR	REV	DESCRIPTION	CHK	DATE	APPROVED
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204492 A

Xerox Data Systems, El Segundo, California

DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

DO NOT SCALE DRAWING — SHEET 4 OF 64

DIST CODE 09

REVISIONS				204492 A
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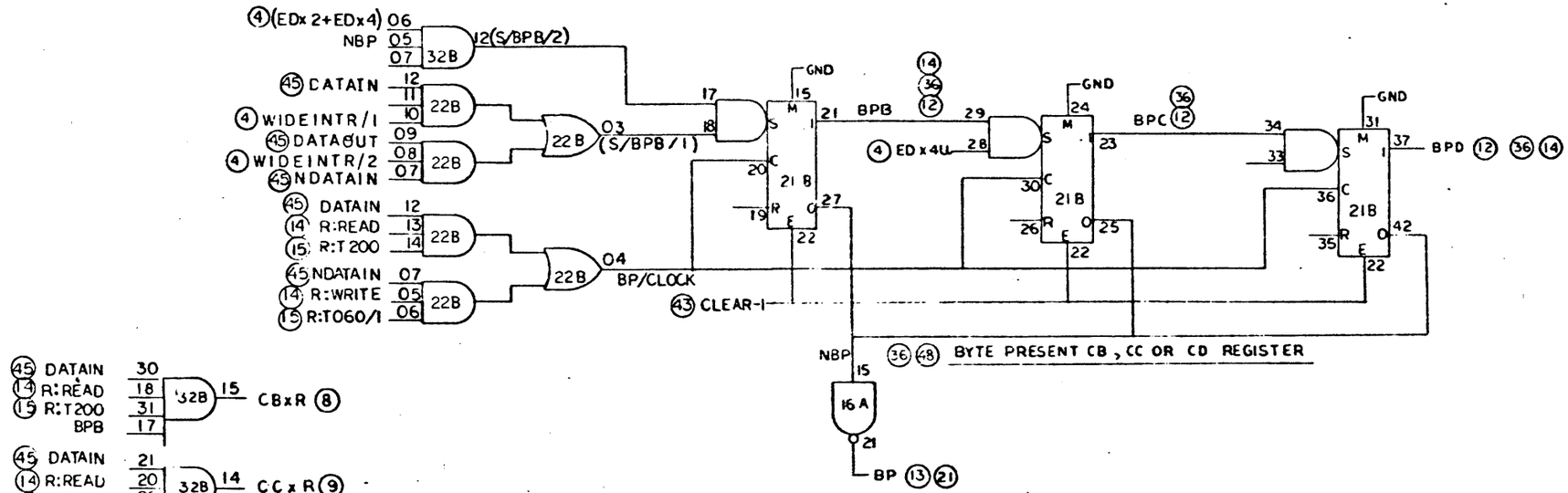

DIST CODE 409

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TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.
18338	D	204492

SCALE — DO NOT SCALE DRAWING SHEET 5

204492 A

9-16-70

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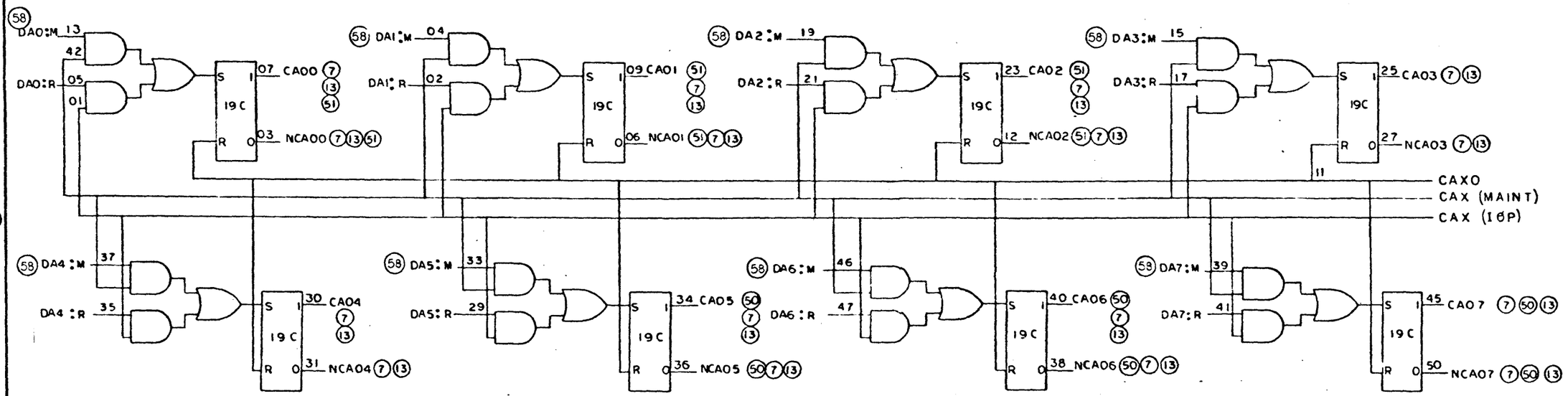
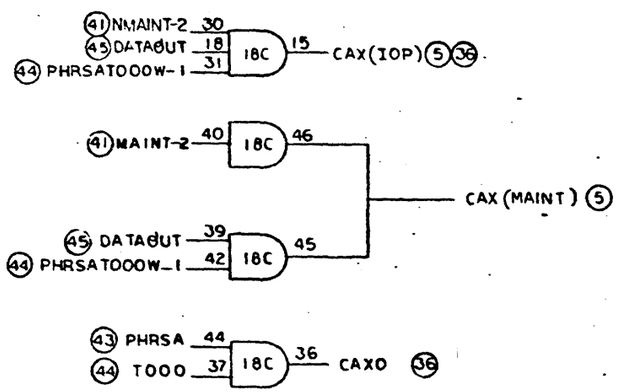
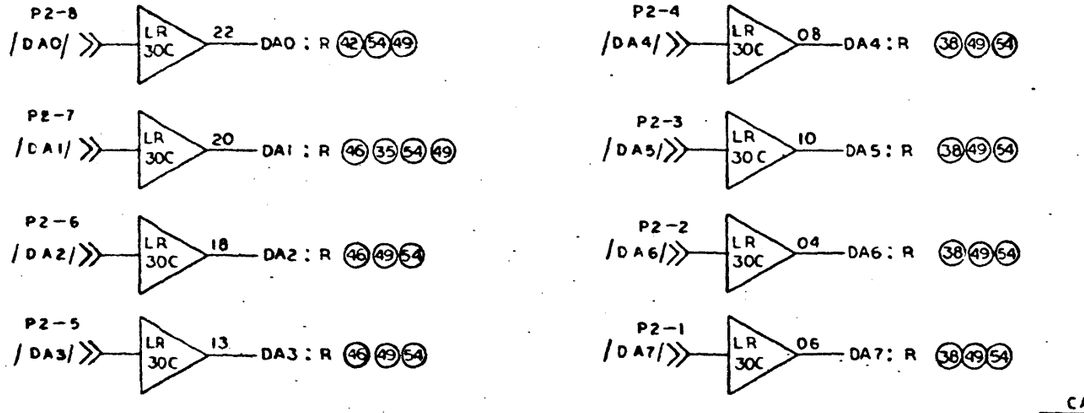






CAREG & CONTROL

204492 A

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

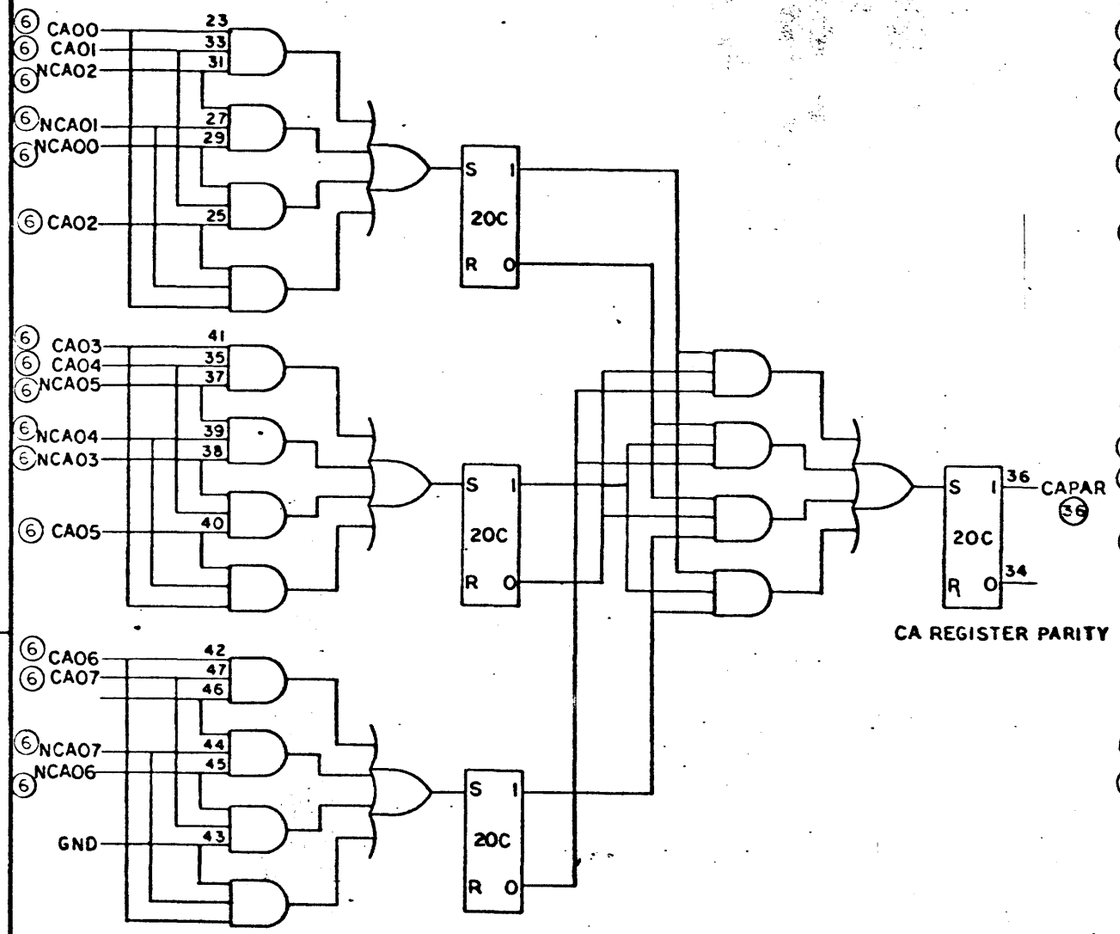
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

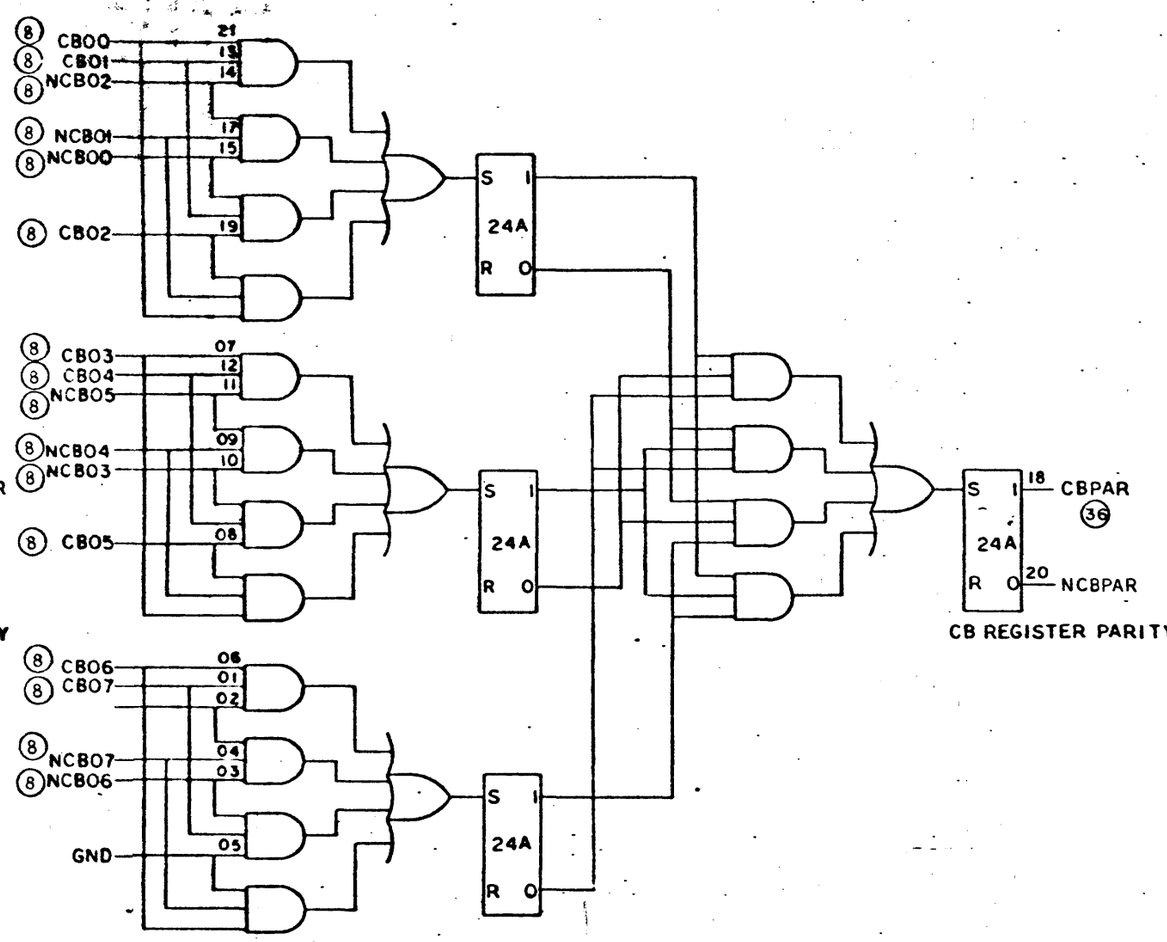
SCALE — DO NOT SCALE DRAWING SHEET 60F 67

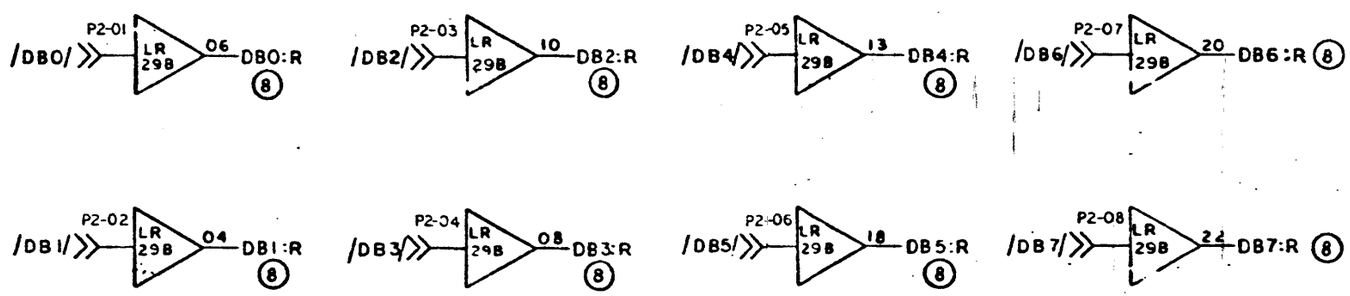
4-20-70

REVISIONS					204492 A
LTR	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			

NOTES:
1. SIGNALS CA00-CA07 AND NCA00-NCA07 ARE GENERATED ON SHT 6.
2. SIGNALS CB00-CB07 AND NCB00-NCB07 ARE GENERATED ON SHT 8.







DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

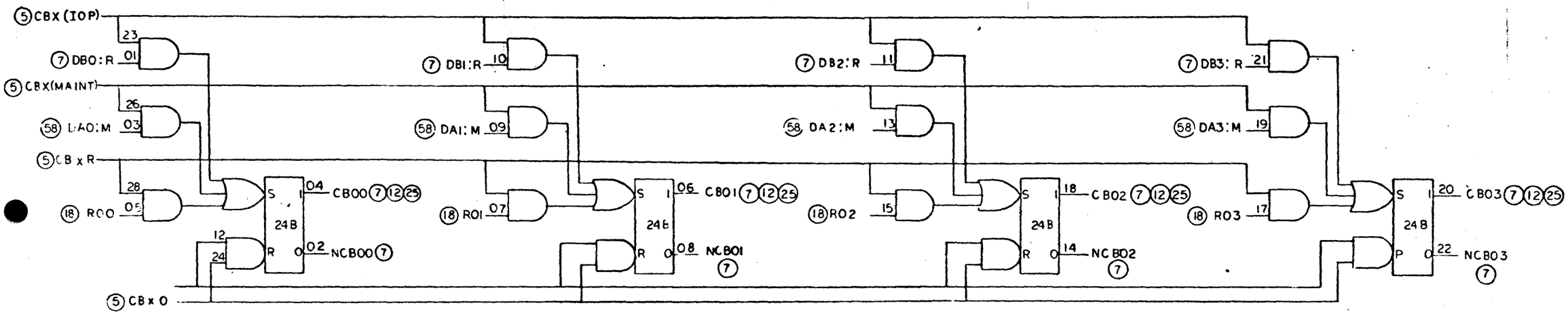
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

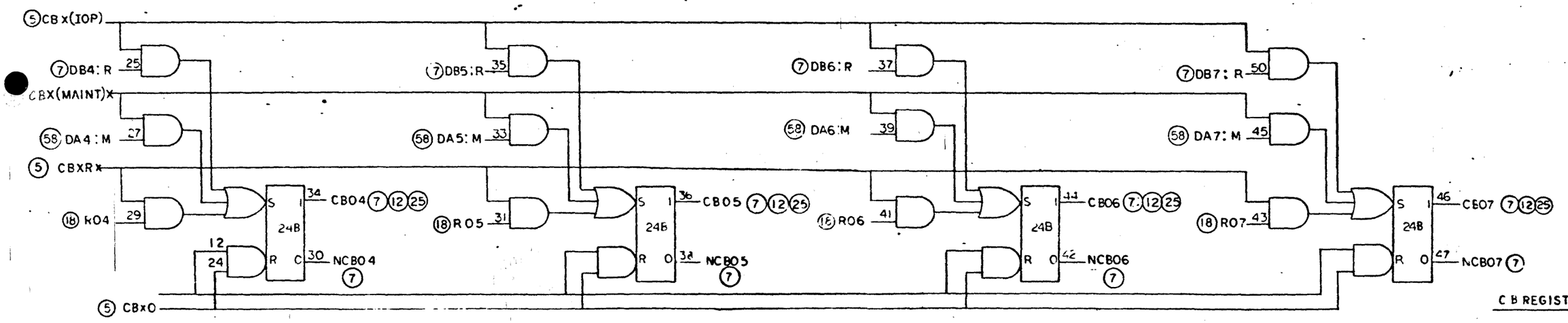
SCALE — | DO NOT SCALE DRAWING | SHEET 7 OF 61

L. Hunter 5-21-73

204492 A

REVISIONS					204492 A
LTR	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			





C B REGISTER

DIST CODE 409

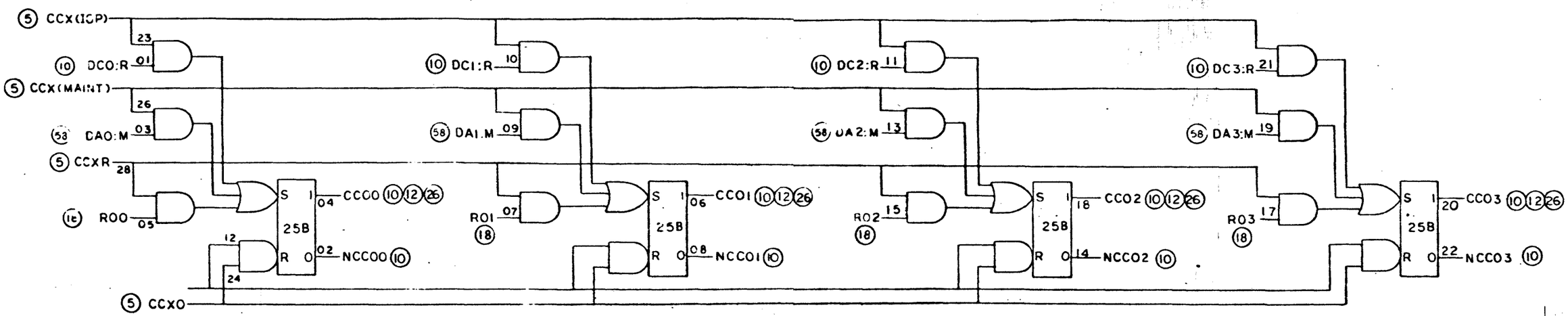
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

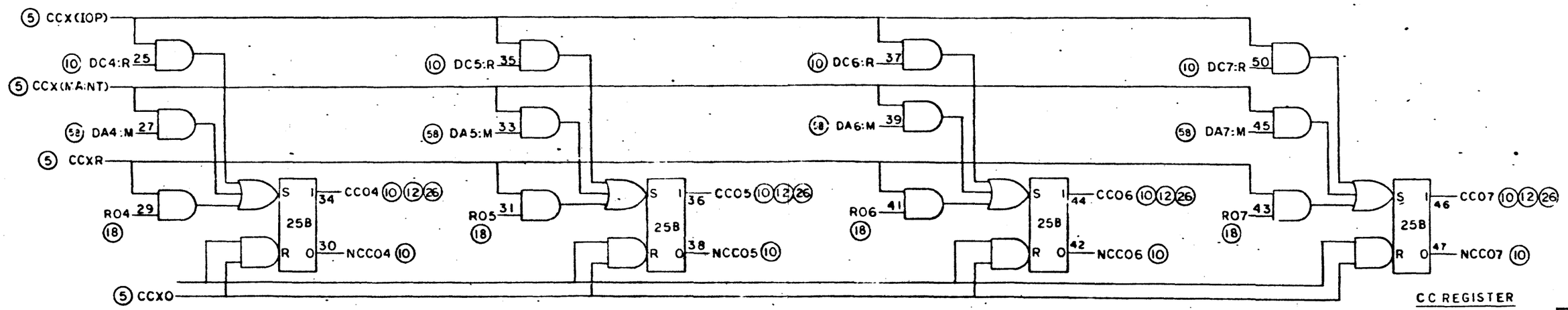
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A
SCALE	DO NOT SCALE DRAWING		SHEET 8 OF 61

204492 A

REVISIONS				204492 A
LAL	REV.	DESCRIPTION	CHK	DATE / APPROVED
X	A	MFG RELEASE NO E.O.		





CC REGISTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTIDGE DISK CONTROLLER

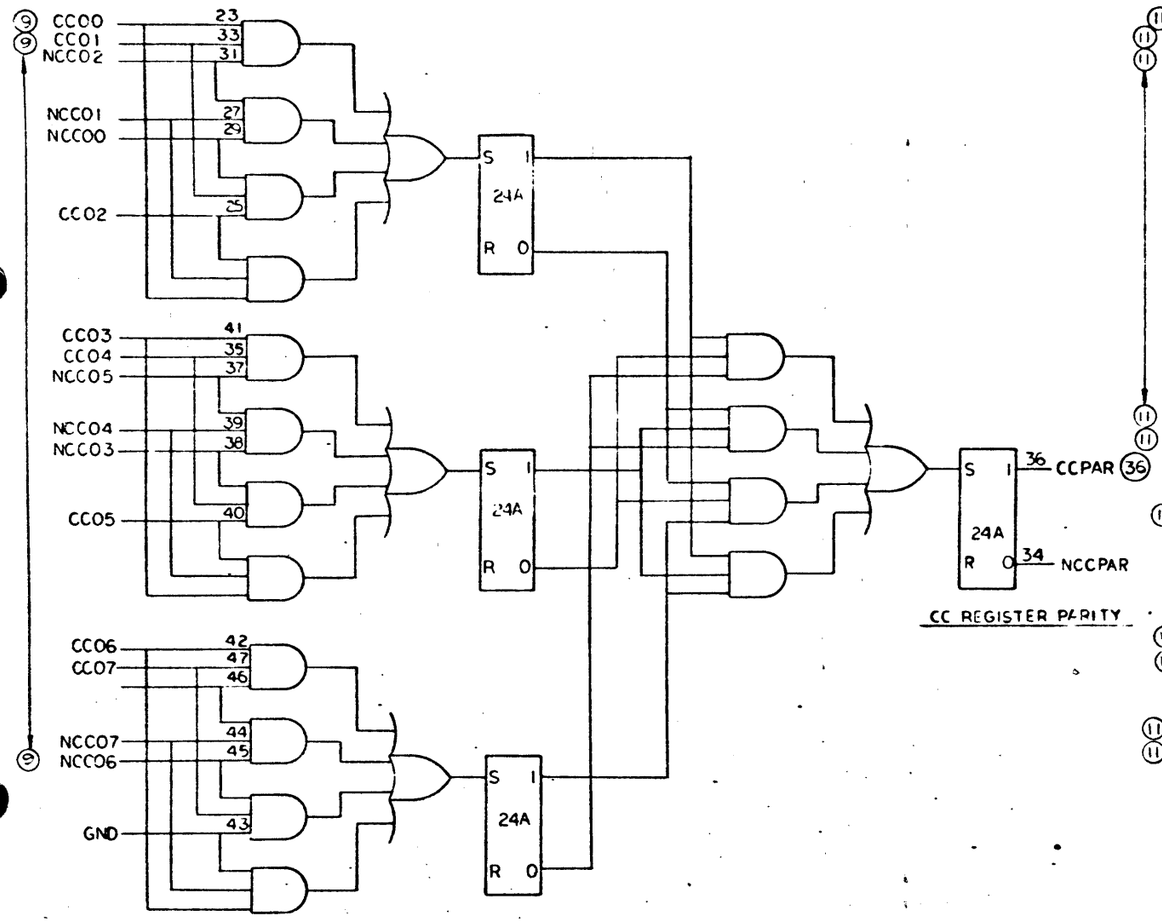
CODE IDENT.	SIZE	DWG. NO.	REVISION LETTER
18338	D	204492	A

SCALE —— DO NOT SCALE DRAWING SHEET 9 OF 61

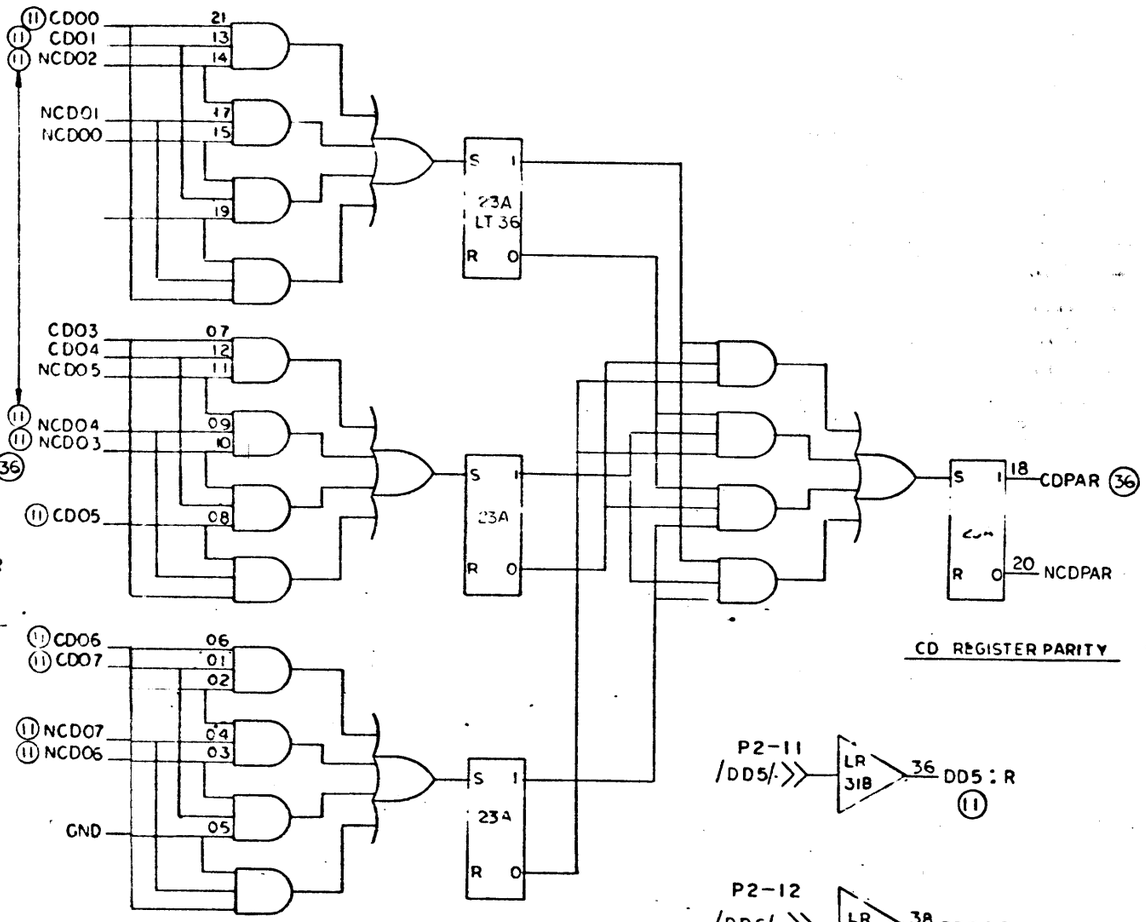
204492 A

REVISIONS					204492 A
LAL	REV	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			

NOTES:
1. SIGNALS CC00-CC07 AND NCC00-NCC07 ARE GENERATED ON SHT 9.
2. SIGNALS CD00-CD07 AND NCD00-NCD07 ARE GENERATED ON SHT 11.



CC REGISTER PARITY



CD REGISTER PARITY

P2-10 /DC0/ → LR 298 → 34 DC0 : R (9)
P2-11 /DC1/ → LR 298 → 36 DC1 : R (9)
P2-12 /DC2/ → LR 298 → 38 DC2 : R (9)
P2-13 /DC3/ → LR 298 → 40 DC3 : R (9)
P2-1 /DC4/ → LR 311 → 06 DC4 : R (9)
P2-2 /DC5/ → LR 318 → 04 DC5 : R (9)
P2-3 /DC6/ → LR 318 → 10 DC6 : R (9)
P2-4 /DC7/ → LR 318 → 08 DC7 : R (9)

P2-11 /DD5/ → LR 318 → 36 DD5 : R (11)
P2-12 /DD6/ → LR 318 → 38 DD6 : R (11)
P2-13 /DD7/ → LR 318 → 40 DD7 : R (11)
P2-6 /DD0/ → LR 318 → 18 DD0 : R (11)
P2-8 /DD2/ → LR 318 → 22 DD2 : R (11)
P2-7 /DD1/ → LR 318 → 20 DD1 : R (11)
P2-9 /DD3/ → LR 318 → 27 DD3 : R (11)
P2-10 /DD4/ → LR 318 → 34 DD4 : R (11)

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM LOGIC — CARTRIDGE DISK CONTROLLER

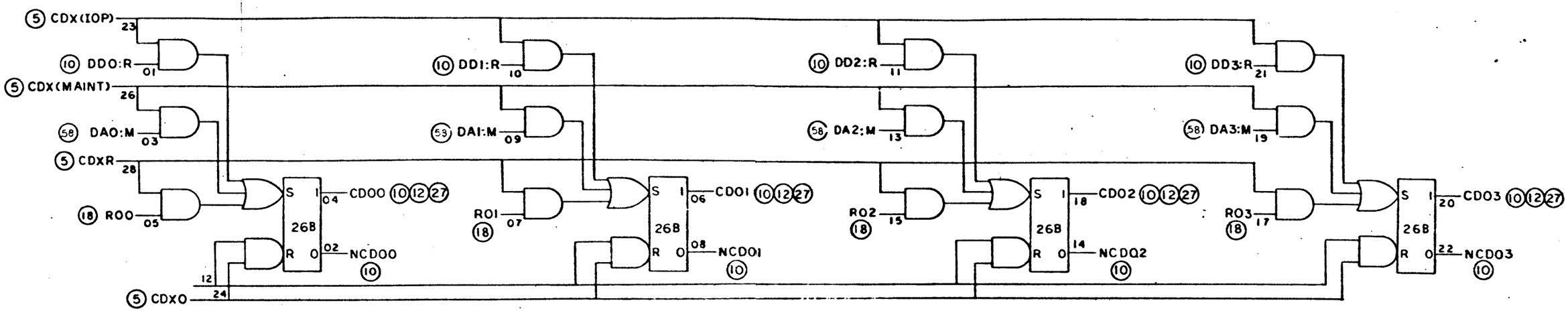
CODE IDENT.	SIZE	DWG	CHANGE LETTER
18338	D	204492	A

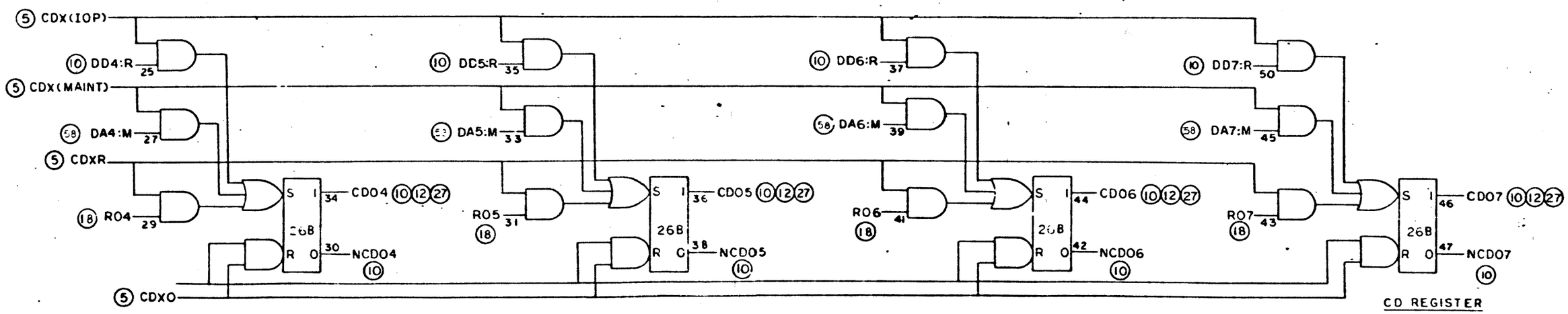
SCALE — DO NOT SCALE DRAWING SHEET 100F61

204492 A

L Hunter 6-24-70

REVISIONS					204492	A
LTR.	REV.	DESCRIPTION	CHK	DATE	APPROVED	
X	A	MFG RELEASE NO E.O.				





CD REGISTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

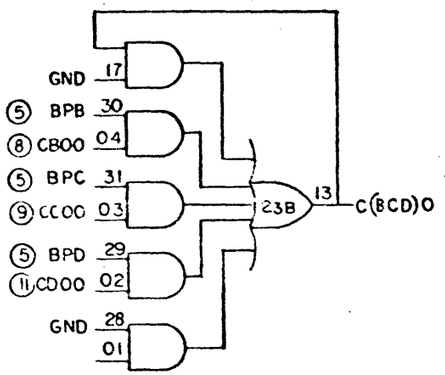
CODE IDENT.	SIZE	DWG. NO.	CONTROL LETTER
18338	D	204492	A

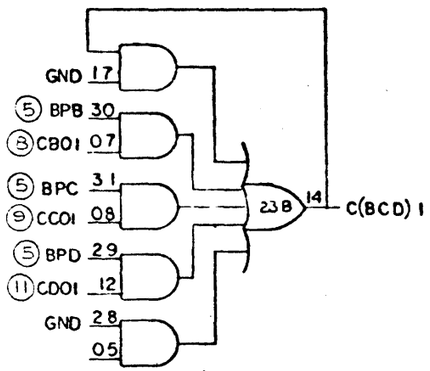
SCALE —— DO NOT SCALE DRAWING SHEET 11 OF 60

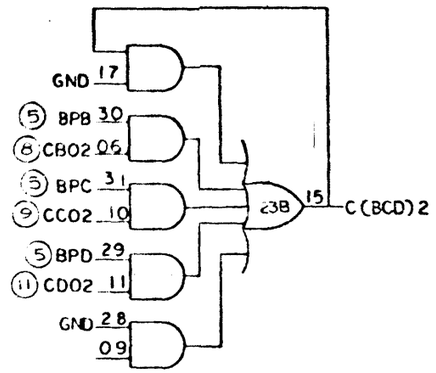
204492 A

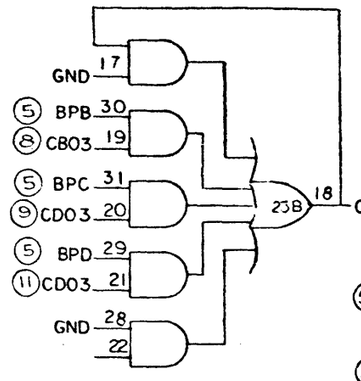
REVISIONS				204492 A
LAL	REV	DESCRIPTION	CHK	DATE / APPROVED
X	A	MFG RELEASE NO E.O.		

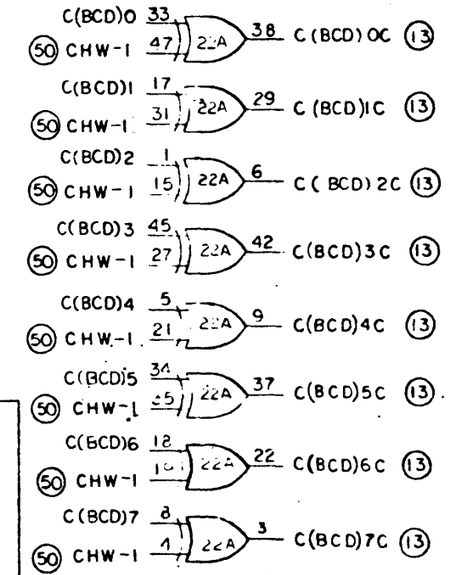
NOTES:
1 SIGNALS CB00-CB07 ARE GENERATED ON SHT 8
2 SIGNALS CC00-CC07 ARE GENERATED ON SHT 9
3 SIGNALS CD00-CD07 ARE GENERATED ON SHT 11



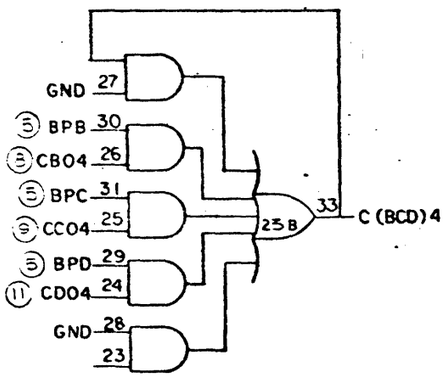


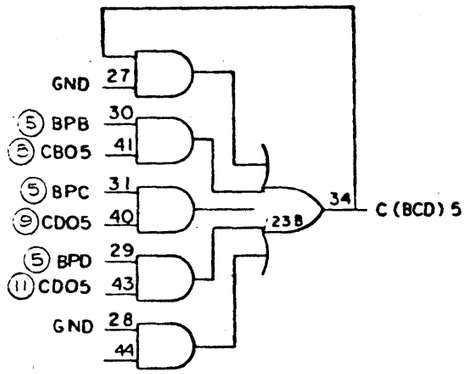


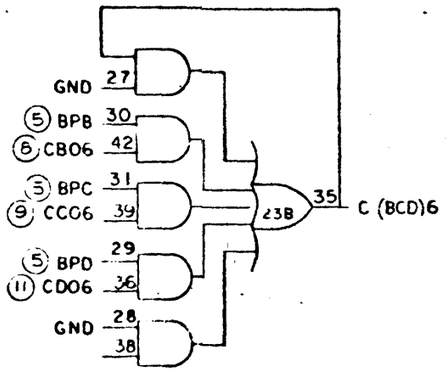


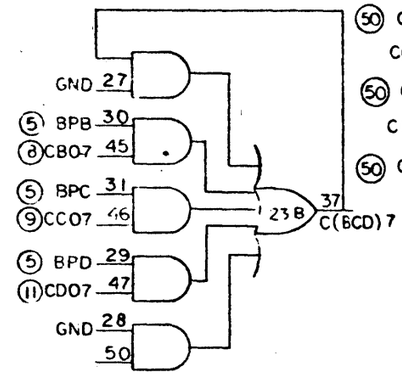


DATA INVERSION FOR CHECKWRITE









BYTE ALIGNMENT

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 12 OF 61

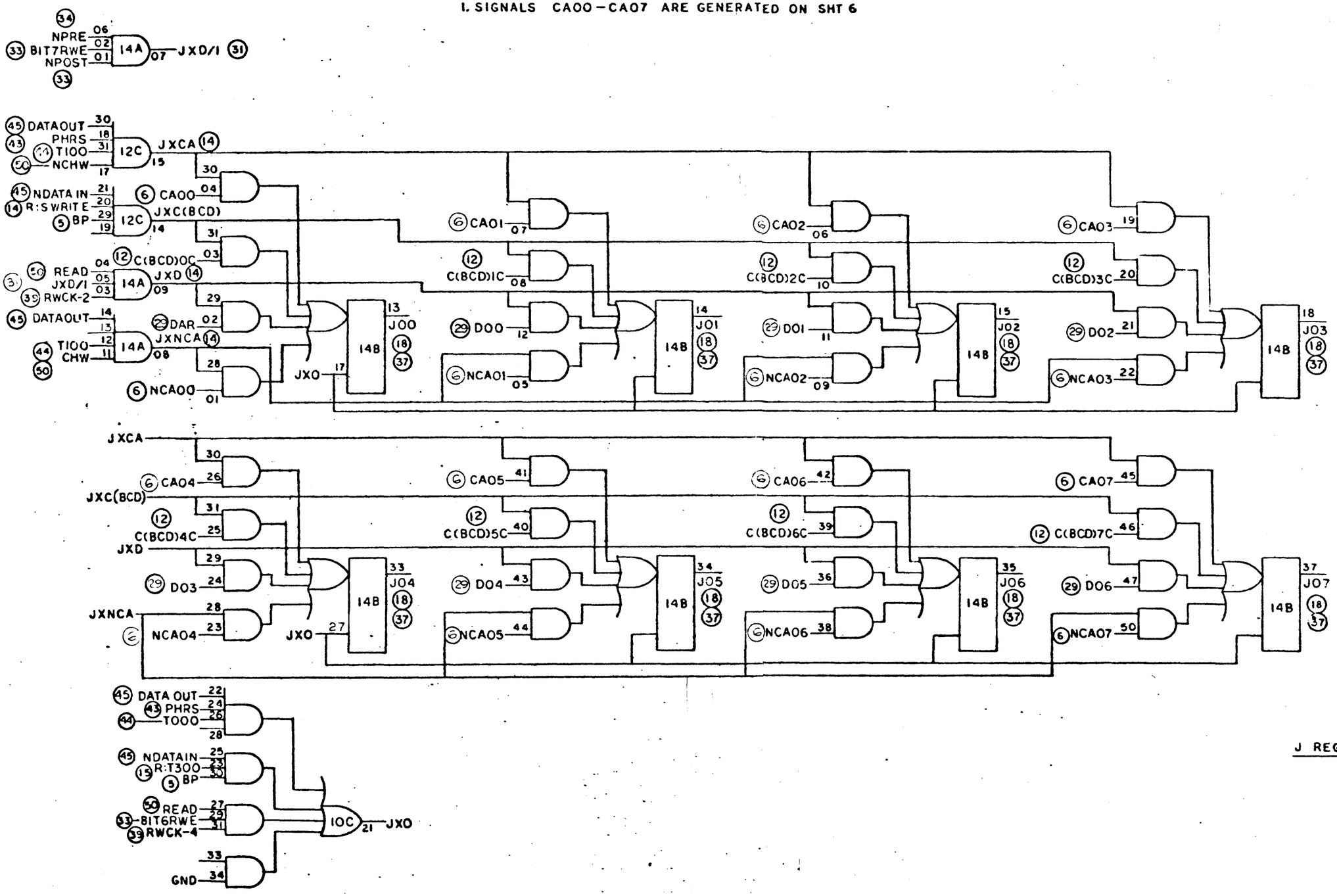
L Hunter 8-27-70

204492 A

REVISIONS					204492	A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED	
X	A	MFG RELEASE NO E.O.				

NOTES

1. SIGNALS CA00 – CA07 ARE GENERATED ON SHT 6



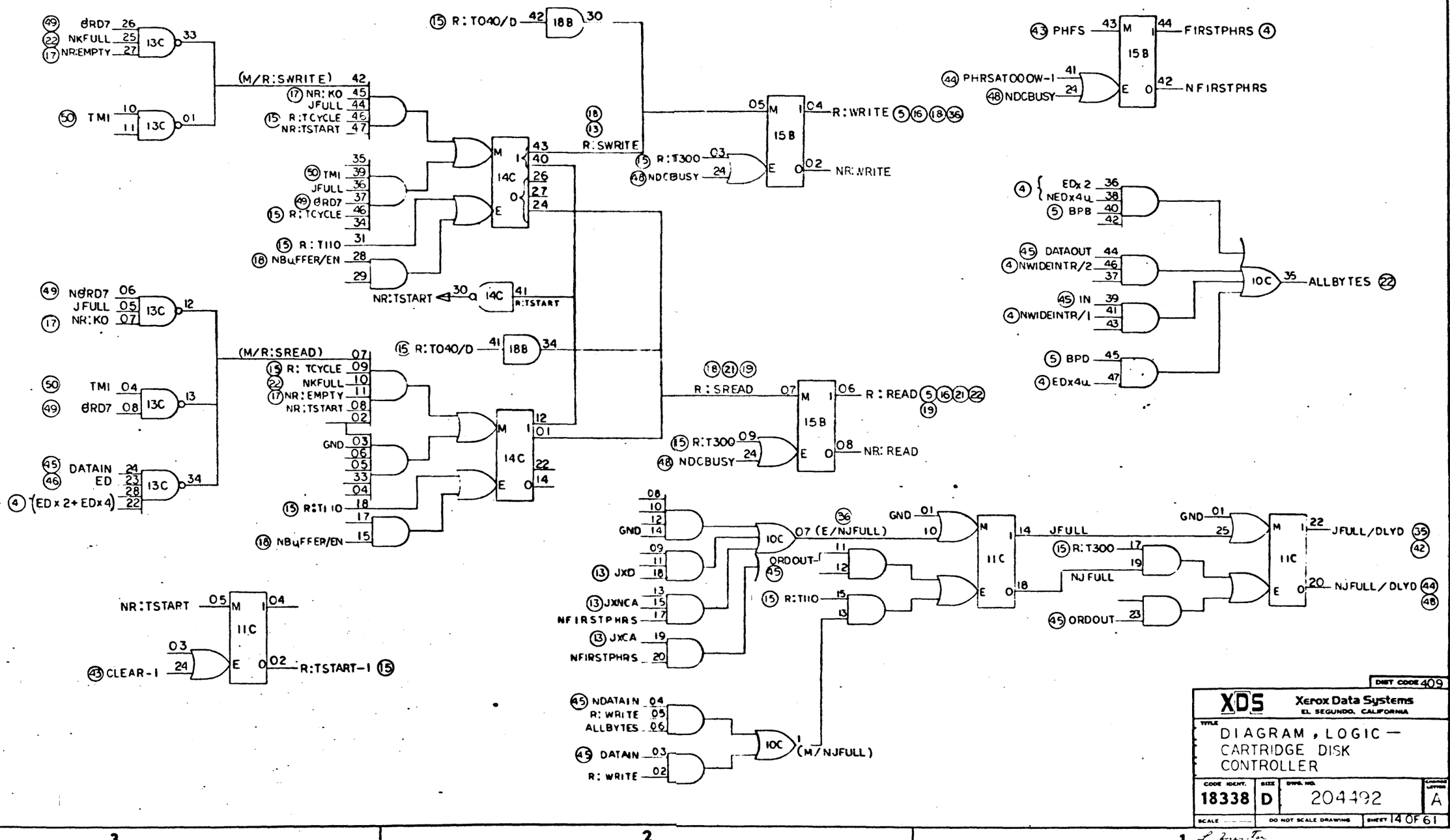
J REGISTER

DIST CODE 409			
XDS Xerox Data Systems, EL SEGUNDO, CALIFORNIA			
TITLE: DIAGRAM, LOGIC – CARTRIDGE DISK CONTROLLER			
CODE IDENT. 18338	SIZE D	DWG. NO. 204492	CHANGE LTR A
SCALE —	DO NOT SCALE DRAWING	SHEET 13 OF 61	

204492 A

L. Hunter 4-29-13

REVISIONS					204492 A
LAL	REV	DESCRIPTION	CHG	DATE	APPROVED
X	A	MFG RELEASE NO E.O			



DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE
DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	REVISION LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 14 OF 61

204492 A

REVISIONS				204492 A
LAL	REV.	DESCRIPTION	CHK	APPROVED
X	A	MFG RELEASE NO E.O.		

(48) NDCBUSY — 24
R:T300 — 47
E, C — 50 — R:TCYCLE (14) (18) (35)
158
R:T060 — 45 — M, I — 46 — NR:TCYCLE

(14) R:TSTART-1 — 06
R:TCYCLE — 08
19B
GND
46X

DELAY LINE — TIME IN NSEC

20 40 60 80 100 110 19B 130 160 180 200 220 240 270 300

47 31 38 26 23 18 17 25 19 20 07 11

R:T040/D — (14) R:T040/D — 47
R:T060/D — 24
R:T100/D — 43
R:T110/D — 25 20
R:T130/D — 40
R:T160/D — 46
R:T180/D — 27
R:T200/D — 22
R:T220/D — 45
R:T240/D — 44
R:T270/D — 21
R:T300/D — 23

SENSORS IN 18B →

29 04 26 05 18 01 03 06 17 28 02 19 07

R:T060 — (34)
R:T060/1 — (5) (16) (17)
R:T100 —
R:T110 — (14)
NR:T110 — (18)
R:T180 — (18)
R:T200 — (5) (21)
R:T220 — (5) (22) (6) (19)
R:T300 — (13) (14) (18) (22)

20 40 60 80 100 120 140 160 180 200 220 240 260 280 300

R:T040
R:T060
T060/1
R:T100
R:T110
R:T180
R:T200
R:T220
R:T300

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

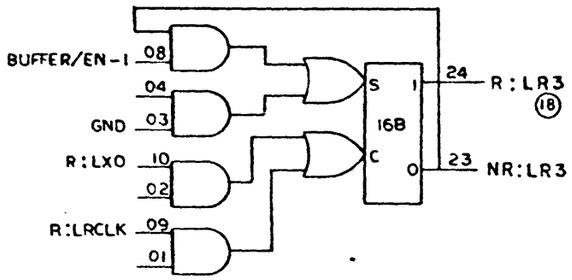
CODE IDENT.	SIZE	DWG. NO.	CONFIG LEVEL
18338	D	204492	A

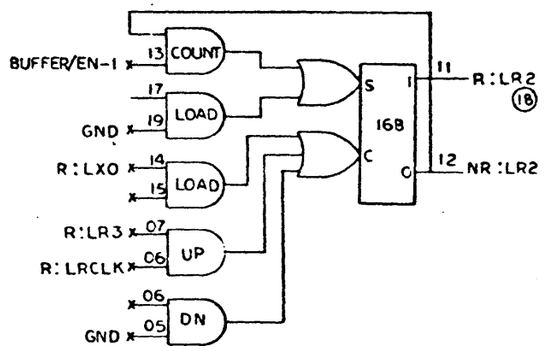
SCALE — DO NOT SCALE DRAWING SHEET 150F 61

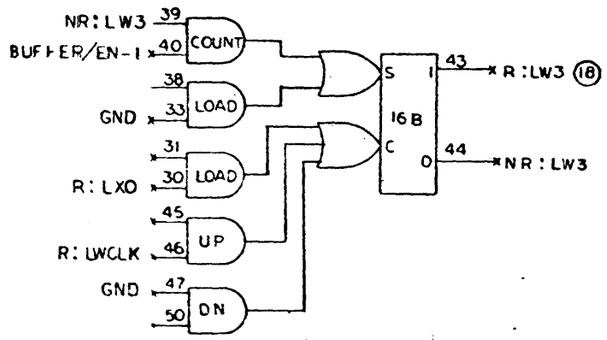
204492 A

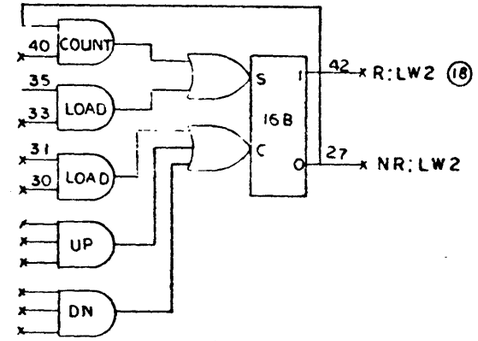
3 2 1

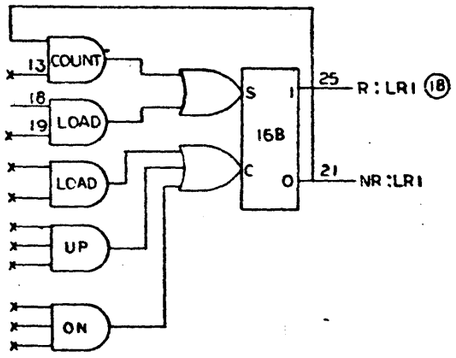
REVISIONS					204492 A
LTR	REV	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			

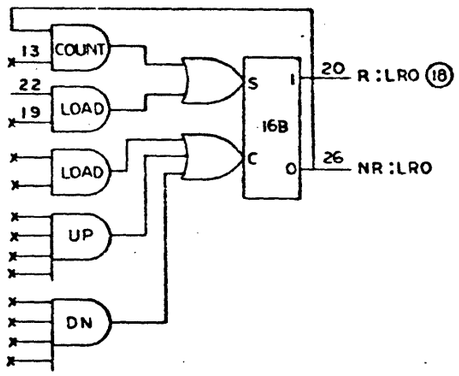


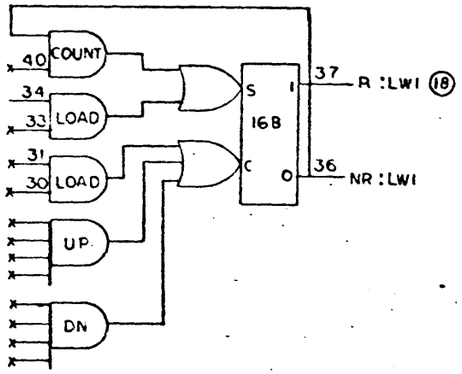


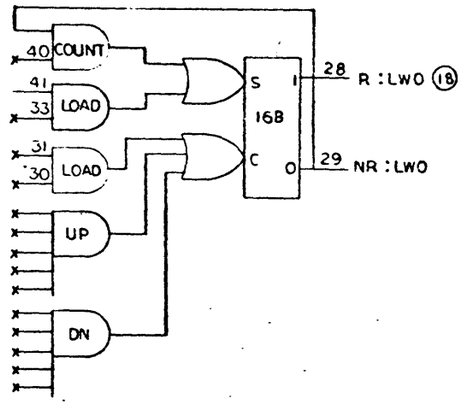












(18) BUFFER/EN 10, 11 — 12C — 01 BUFFER/EN-1

(14) R:WRITE 03
(15) R:T060/1 09 — 12C — 02 R:LWCLK

(45) ORDOUT 40
(44) PHRSATOOOW-1 41 — 12C — 46 R:LXO

(14) R:READ 39
(15) R:T060/1 42 — 12C — 45 R:LRCLK

FAM READ/WRITE ADDRESS

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

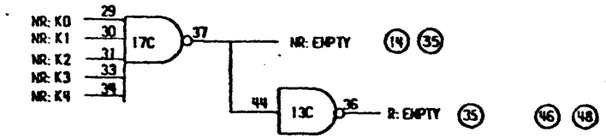
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

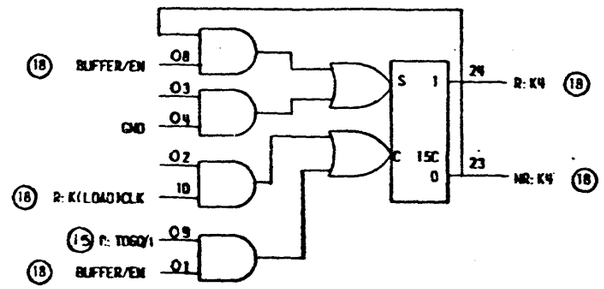
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

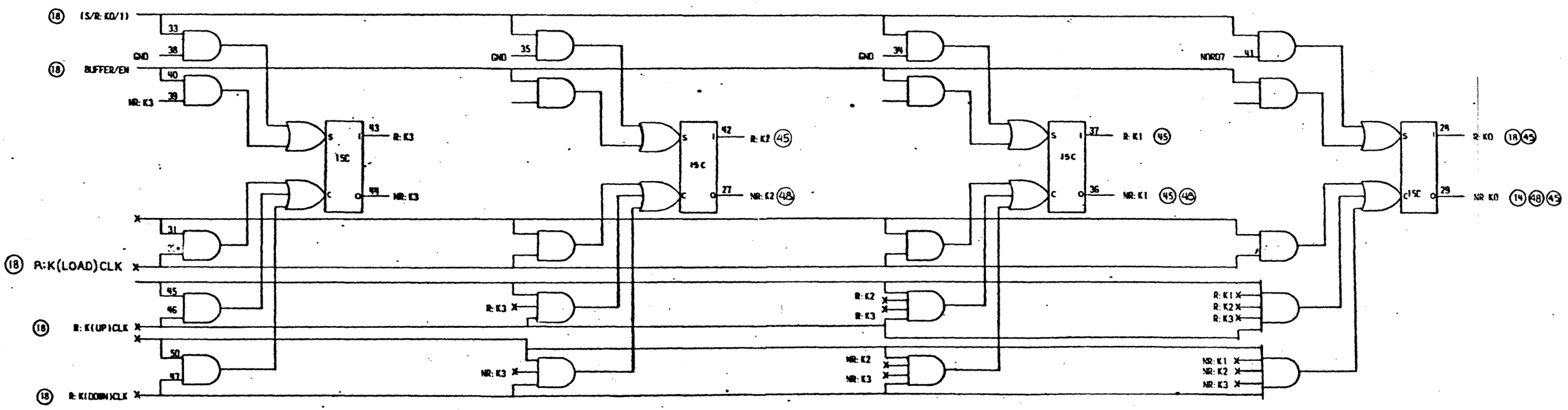
SCALE — DO NOT SCALE DRAWING SHEET 16 OF 61

204492 A

REVISIONS					204492 A
LAL	REV.	DESCRIPTION	CHG	DATE	APPROVED
X	A	MFG RELEASE NO E.O.		2-11-79	







FAN DIFFERANCE COUNTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

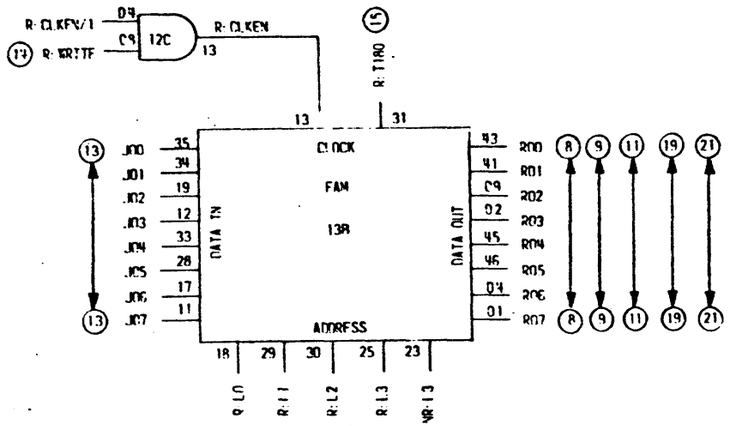
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

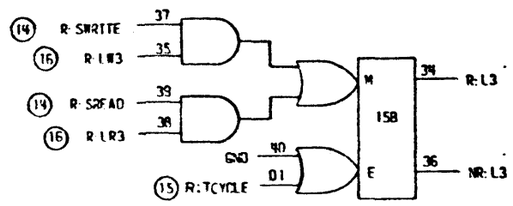
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

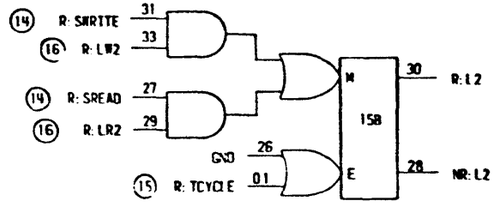
SCALE — DO NOT SCALE DRAWING SHEET 17 OF 61

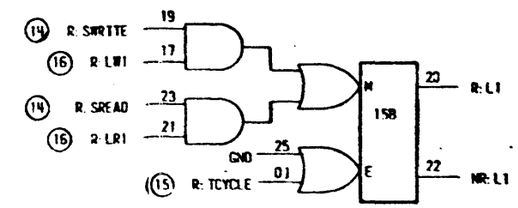
204492 A

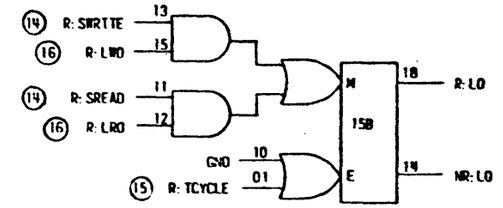
REVISIONS				
LTR	REV	DESCRIPTION	CHG	DATE / APPROVED
X	A	MFG RELEASE NO E.O.		

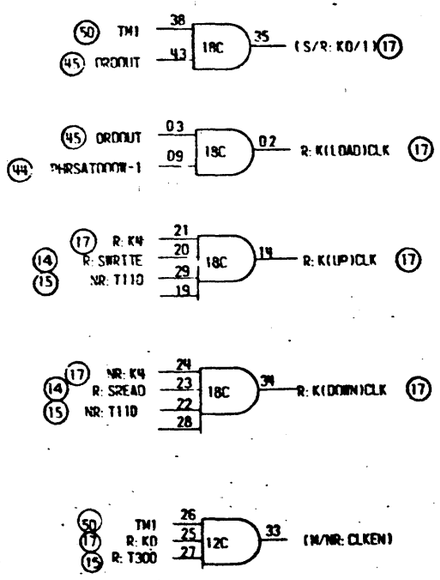


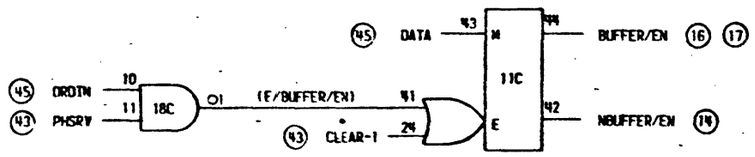


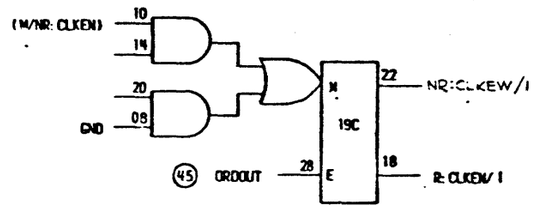


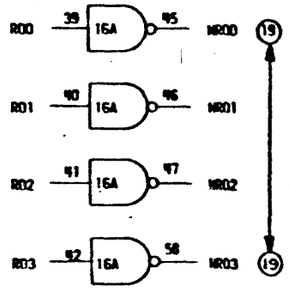


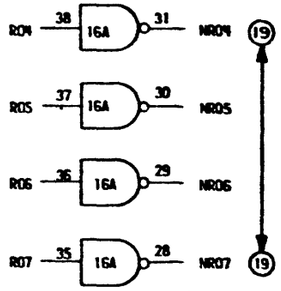












FAM

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	REV. LTR
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 18 OF 61

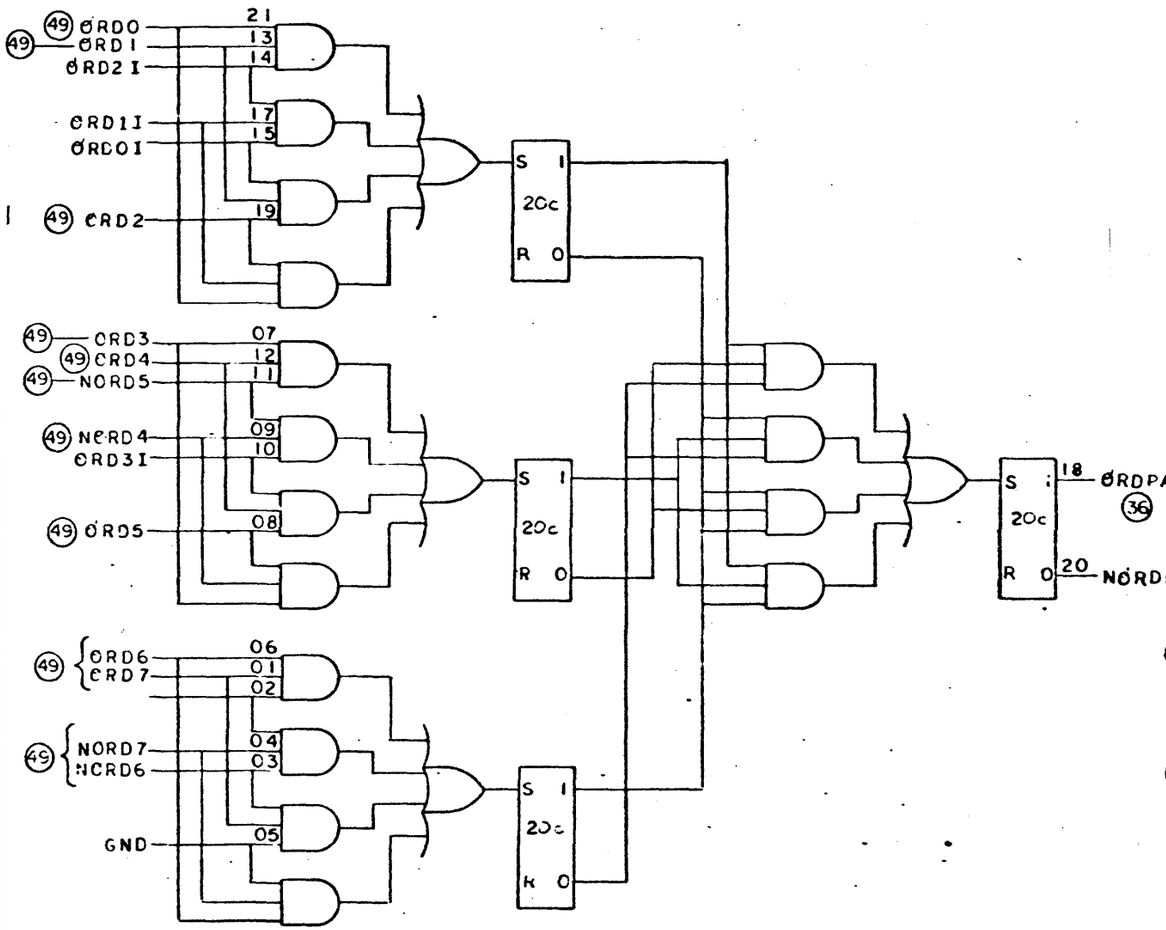
204492 A

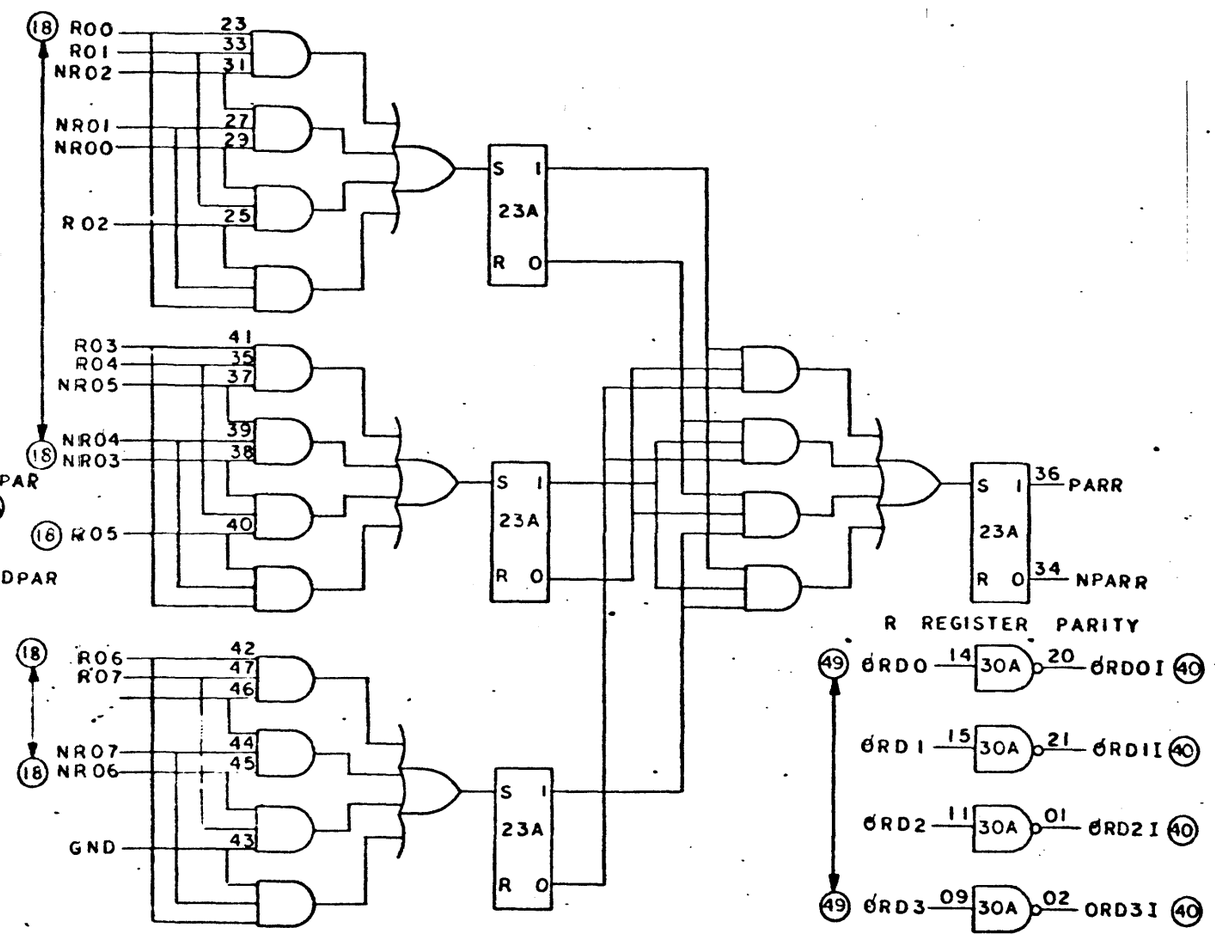
B

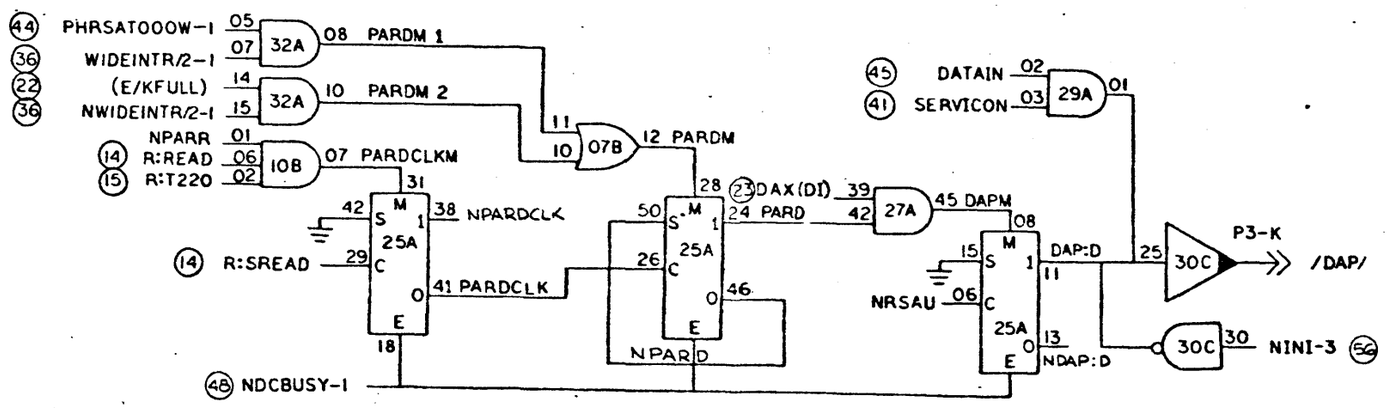
A

3 2 1

REVISIONS					204492	A
LTR	REV.	DESCRIPTION	CHK	DATE	APPROVED	
X	A	MFG RELEASE NO E.O.	LWH	1-3-72		







DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DRWG. NO.	CHANGE
18338	D	204492	A

SCALE — | DO NOT SCALE DRAWING | SHEET 19 OF 61

L Hunt 9-22-70

204492 A

REVISIONS				204492	A
LTR	REV	DESCRIPTION	DATE	APPROVED	
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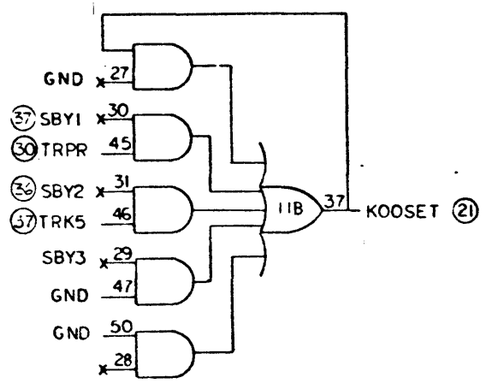
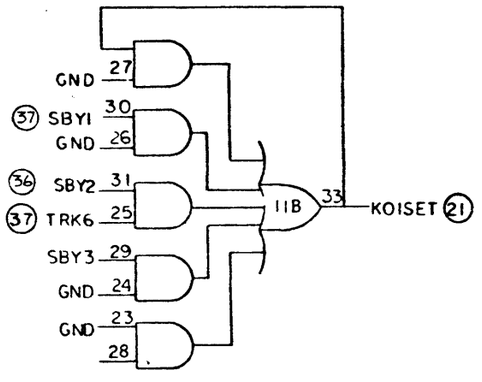
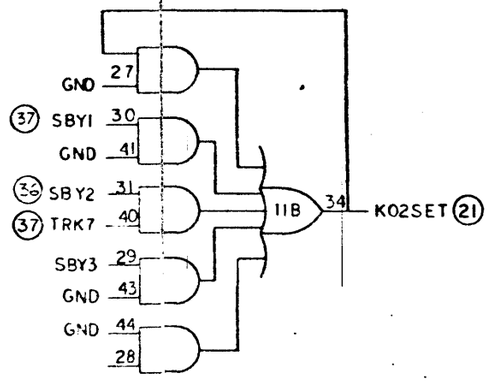
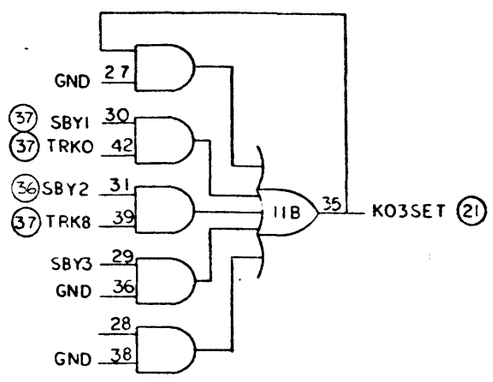
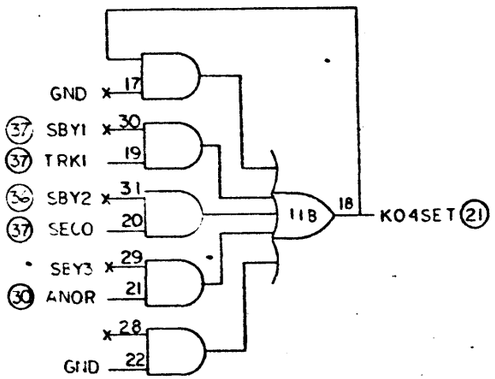
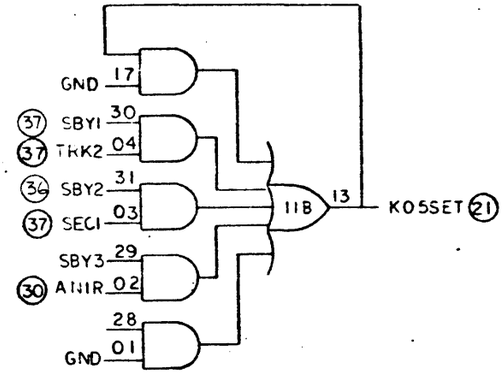


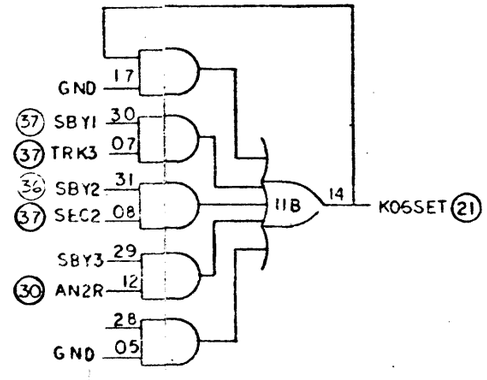


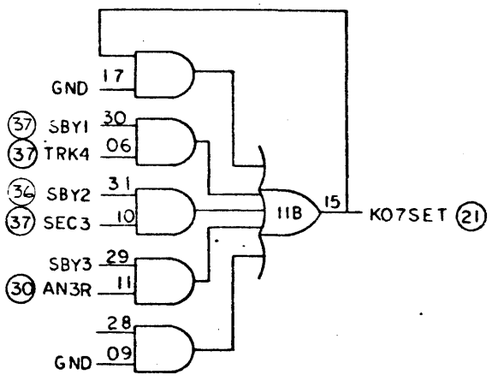


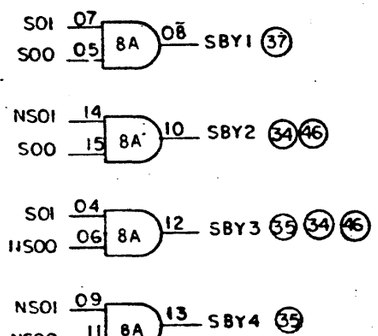


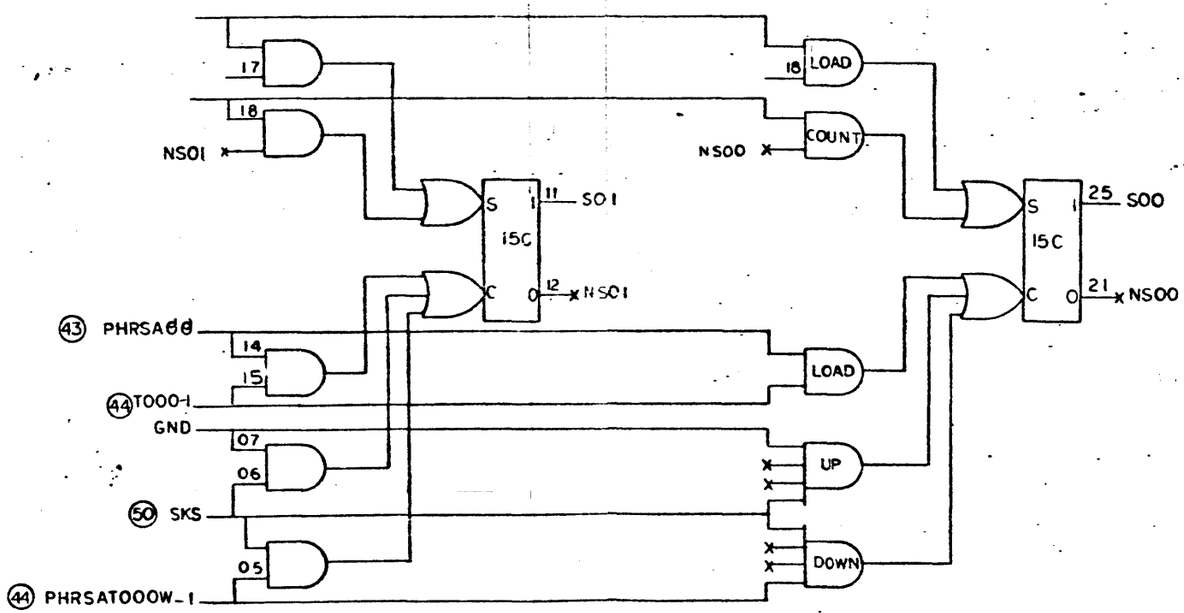












SEEK OR SENSE BYTE COUNTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

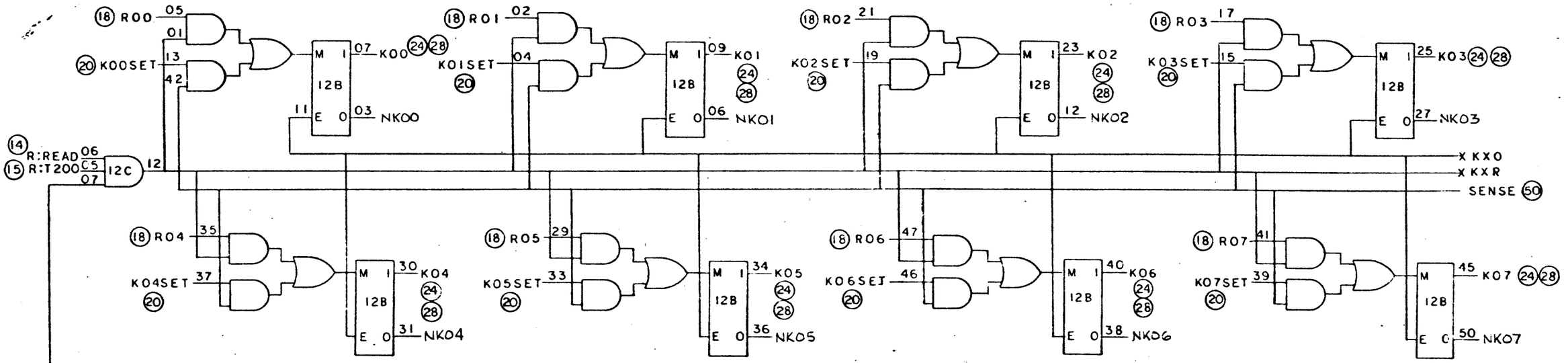
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

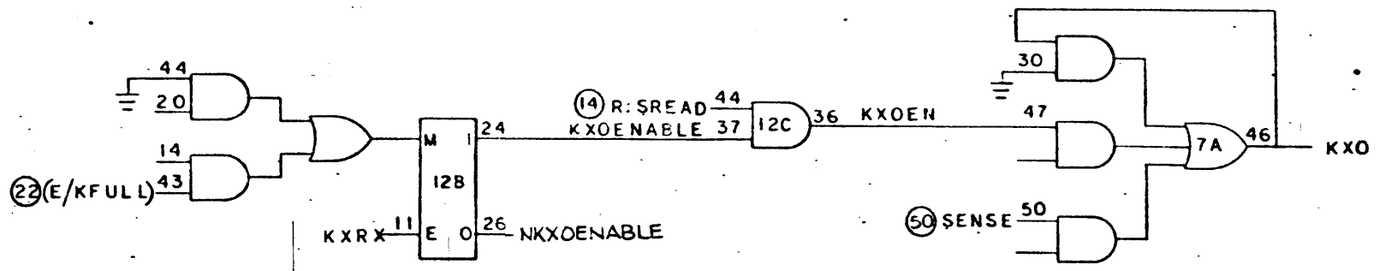
SCALE — DO NOT SCALE DRAWING SHEET 20 OF 61

L. Hunter 4-28-70

204492 A

REVISIONS					204492 A
LAL	REV	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O		1-9-71	



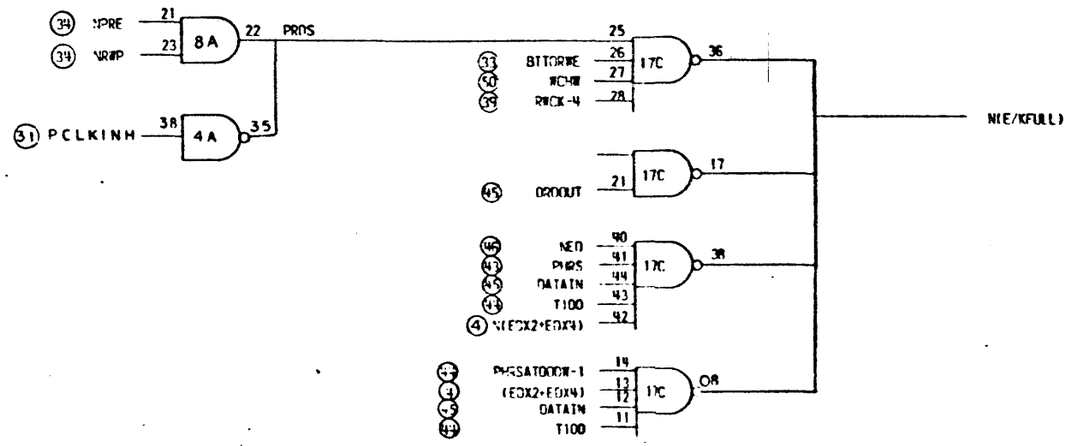


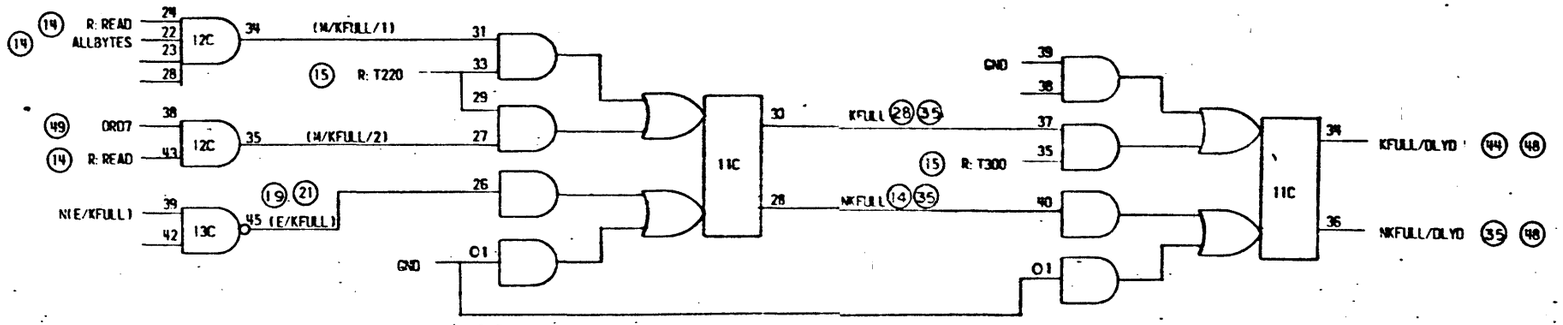
K REGISTER

DIST CODE 409			
XDS Xerox Data Systems EL SEGUNDO, CALIFORNIA			
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER			
CODE IDENT. 18338	SIZE D	DWG. NO. 204492.	CHANGE LETTER A
SCALE —	DO NOT SCALE DRAWING	SHEET 21 OF 61	

204492A

REVISIONS					204492 A
LTR	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			





DIST CODE 409

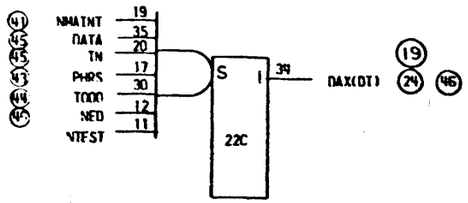
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

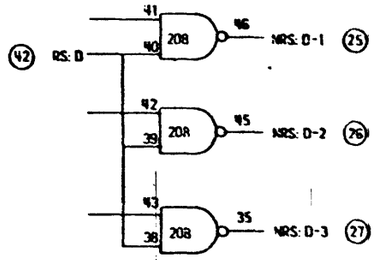
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

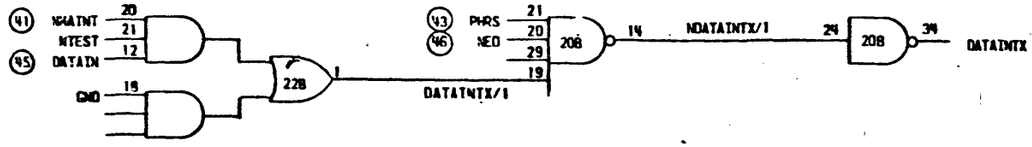
CODE IDENT.	SIZE	DWG. NO.	REVISION LETTER
18338	D	204492	A

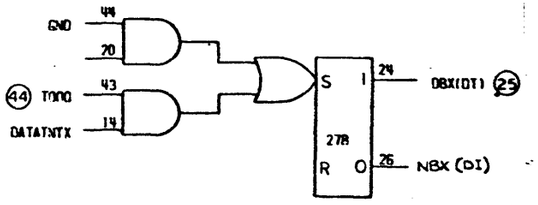
SCALE — DO NOT SCALE DRAWING SHEET 220F 61

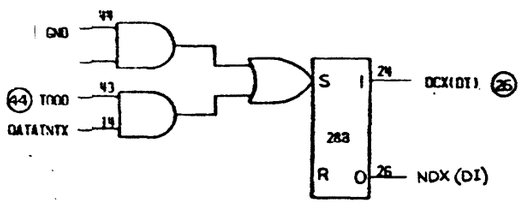
REVISIONS					204492	A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED	
X	A	MFG RELEASE NO E.O.				

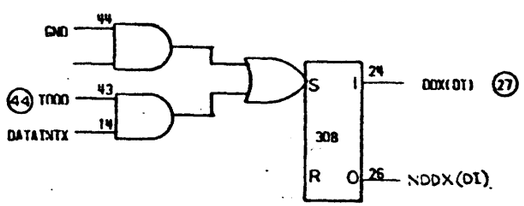


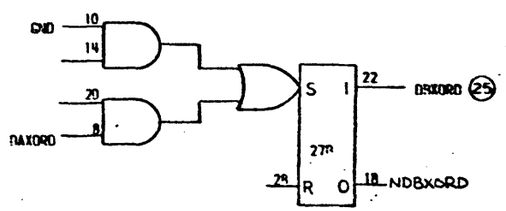


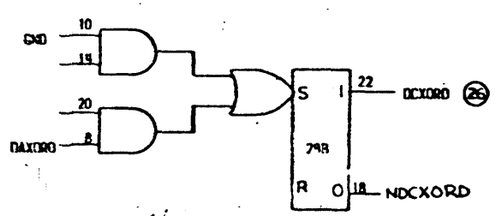


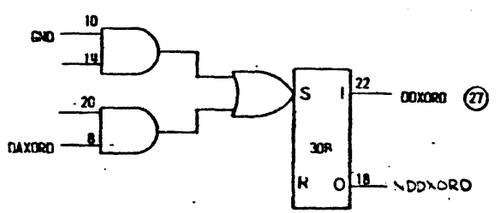


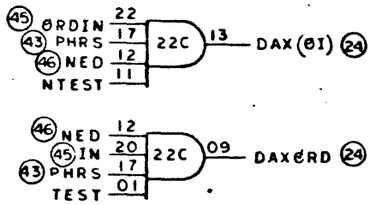




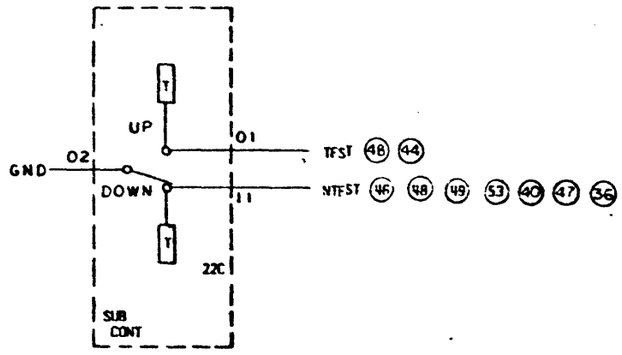








D REGISTER CONTROL



DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

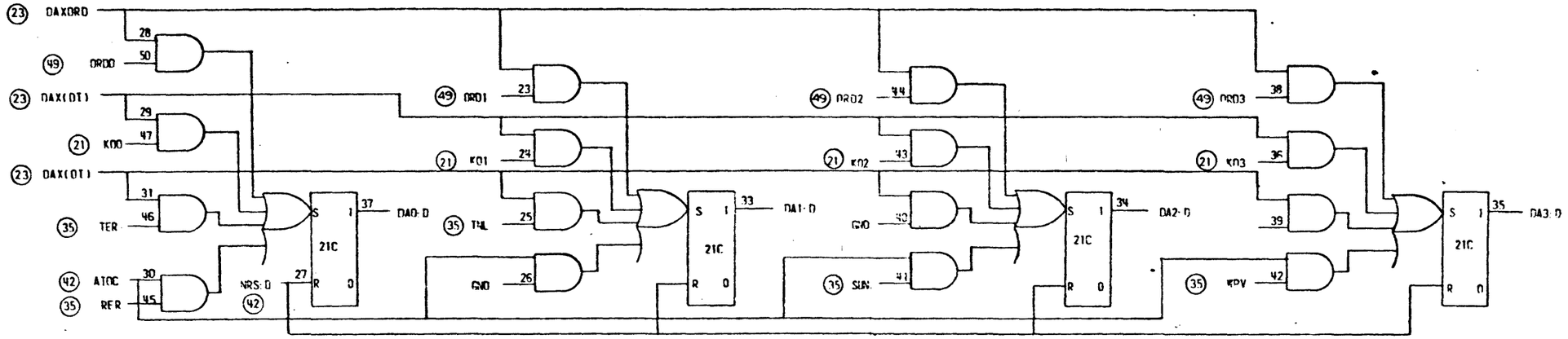
TITLE
DIAGRAM, LOGIC —
CARTRIDGE DISK
CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	REVISION LETTER
18338	D	204492	A
SCALE ——	DO NOT SCALE DRAWING	SHEET 230F61	

L. Hunter

204492 A

REVISIONS				204492 A
LAL	REV	DESCRIPTION	DATE	APPROVED
X	A	MFG RELEASE NO E.O.	3/31/71	



DA REGISTER

DIST CODE 429

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE
DIAGRAM LOGIC
CARTRIDGE DISK
CONTROLLER

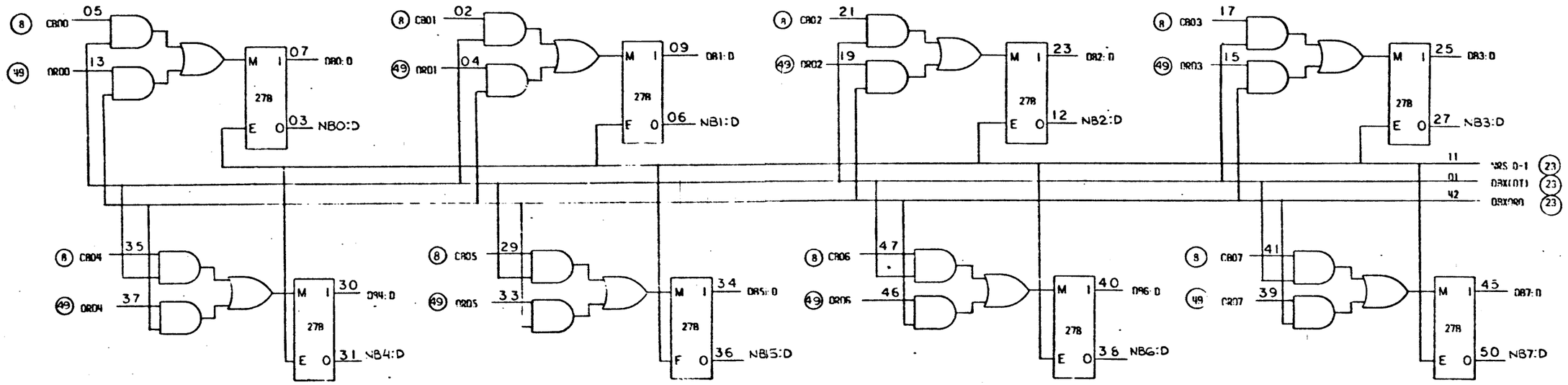
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

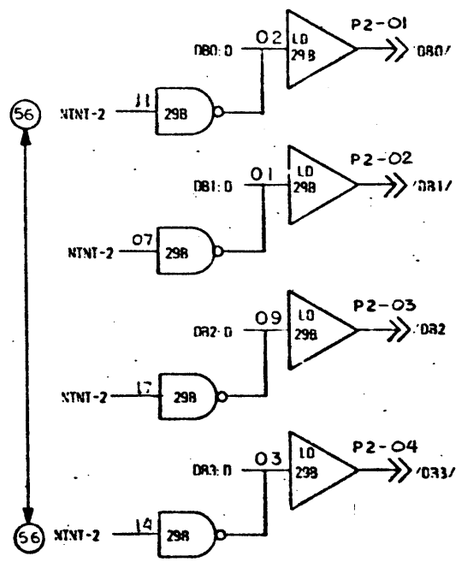
SCALE —— DO NOT SCALE DRAWING SHEET 240F61

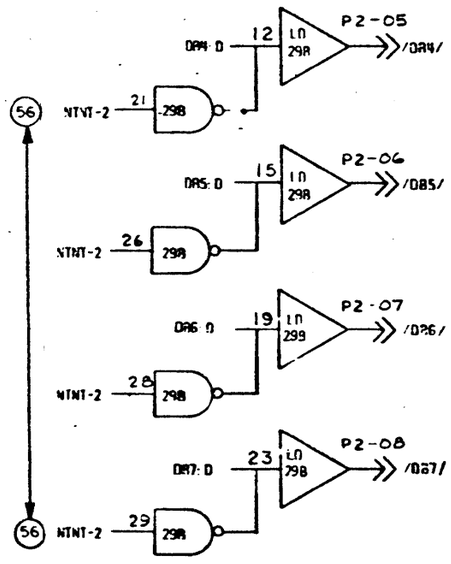
204492 A

L Hunter

REVISIONS					204492 A
LTR.	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.	[illegible]	[illegible]	[illegible]







DB REGISTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

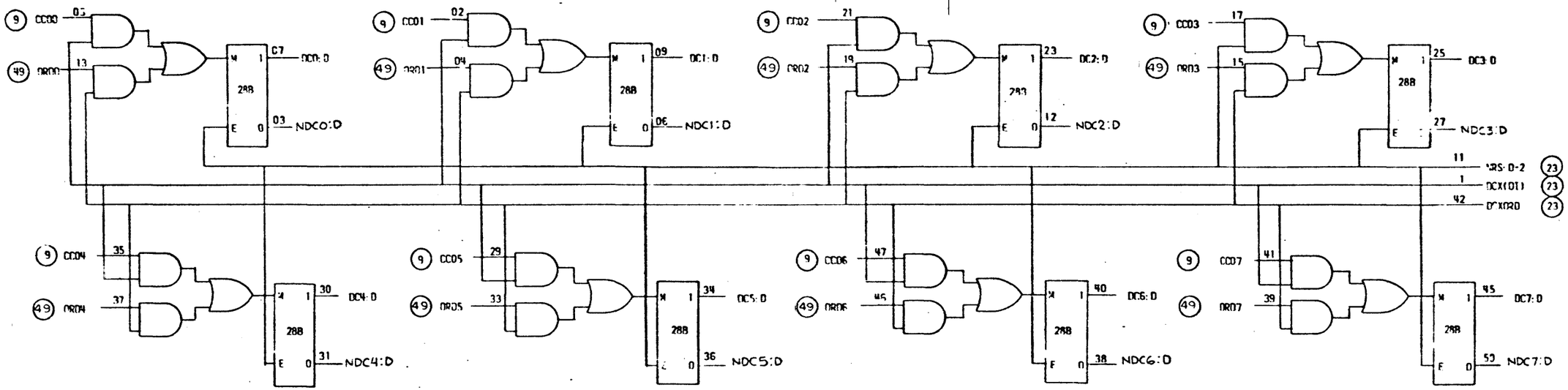
TITLE
DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

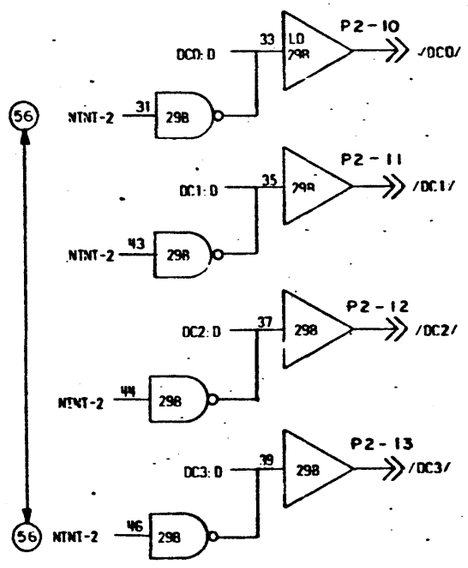
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A
SCALE ——	DO NOT SCALE DRAWING		SHEET 25 OF 61

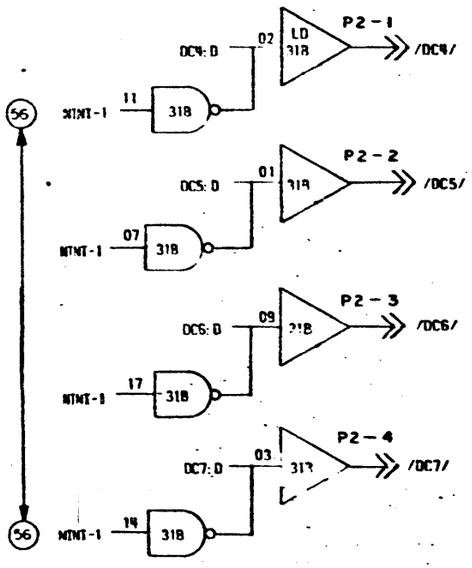
204492 A

L. Hunter

REVISIONS					204492 A
LAL	REV	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO EO			







DC REGISTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

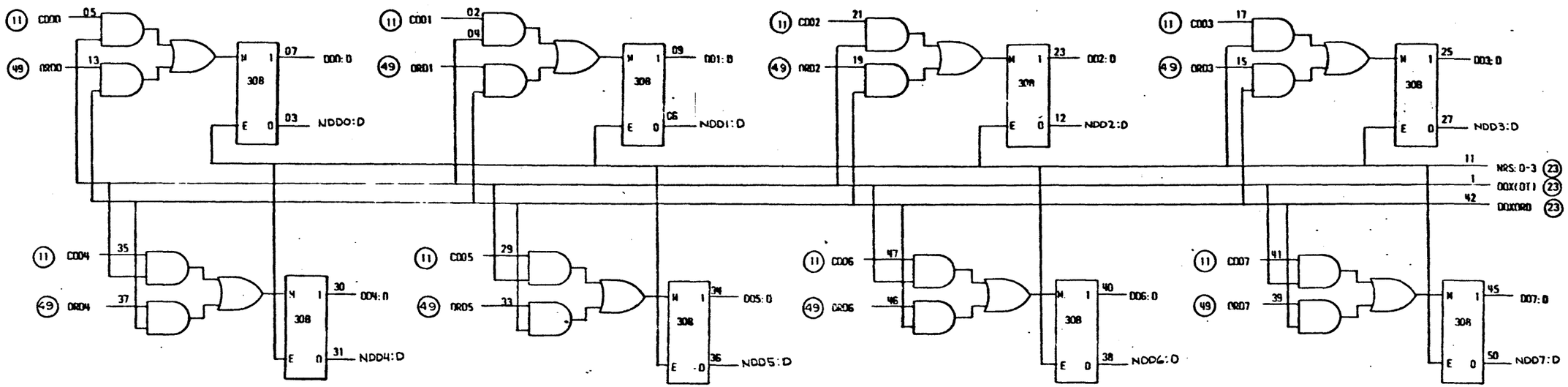
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

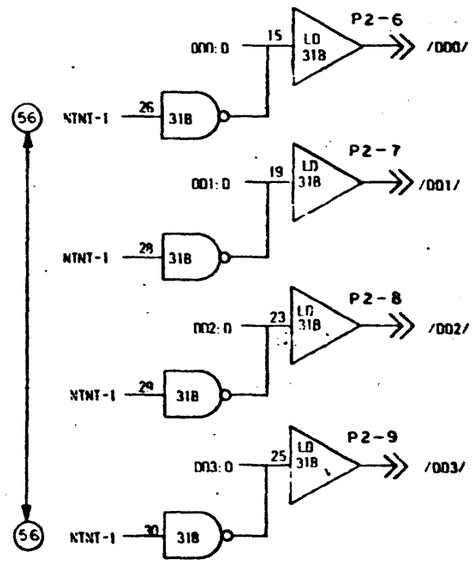
CODE IDENT.	SIZE	DWG. NO.	REV. LETTER
18338	D	204492	A

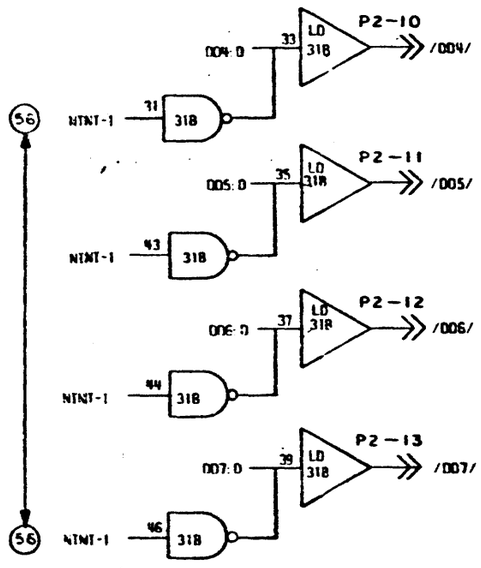
SCALE — DO NOT SCALE DRAWING SHEET 26 OF 61

204492 A

REVISIONS					204492 A
LTR.	REV.	DESCRIPTION	CHK.	DATE	APPROVED
X	A	MFG RELEASE NO EO .	J.S.M.	1-31-74	







DD REGISTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

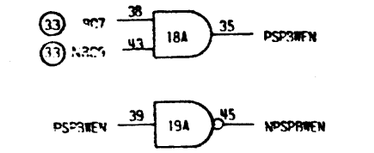
CODE IDENT.	SIZE	DRWG. NO.	CHANGE LETTER
18338	D	204492	A

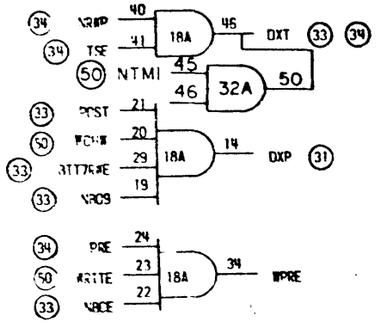
SCALE — | DO NOT SCALE DRAWING | SHEET 27 OF 61

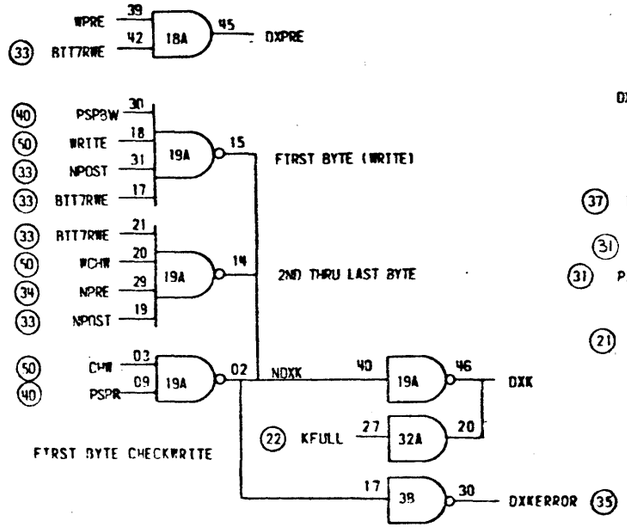
204492 A

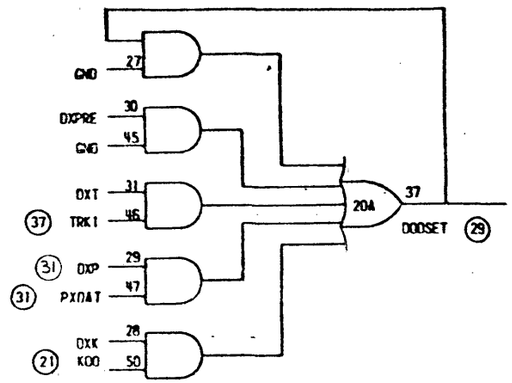
L. Hunter

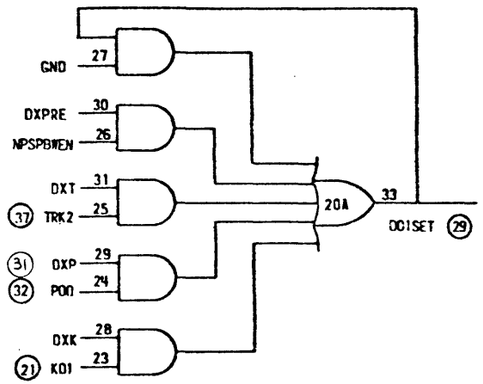
REVISIONS				204492	A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO EO			

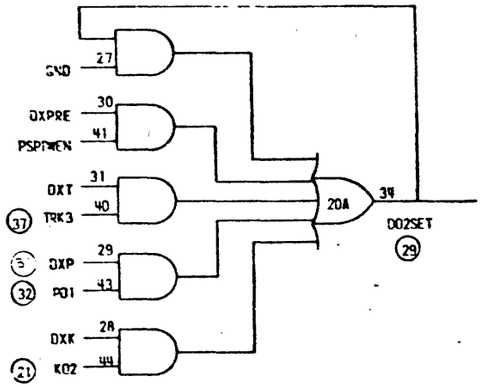


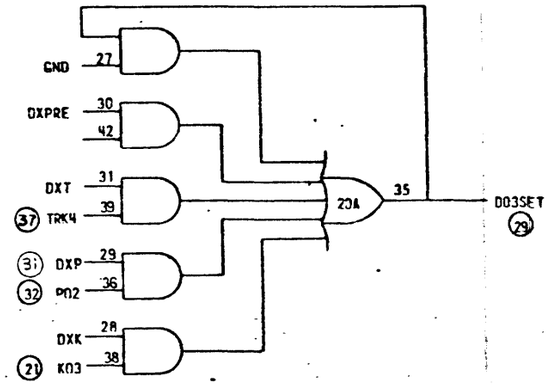


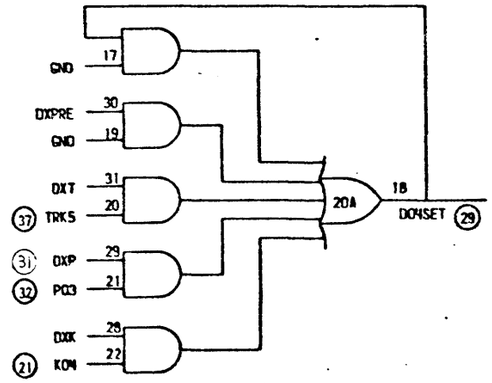


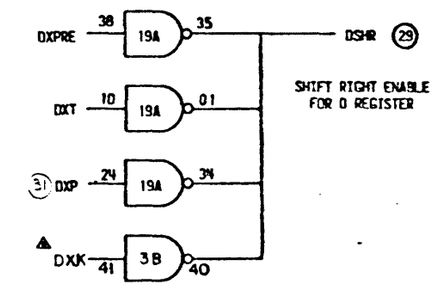


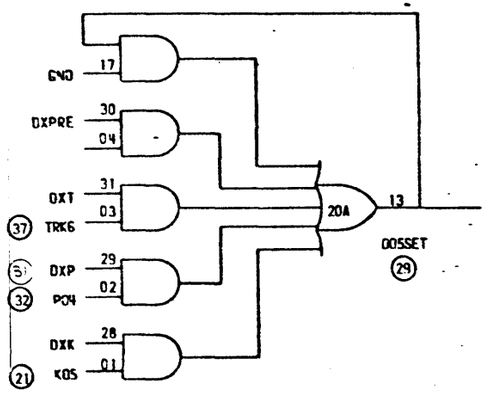


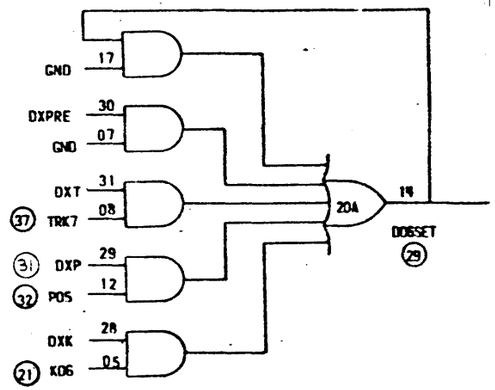


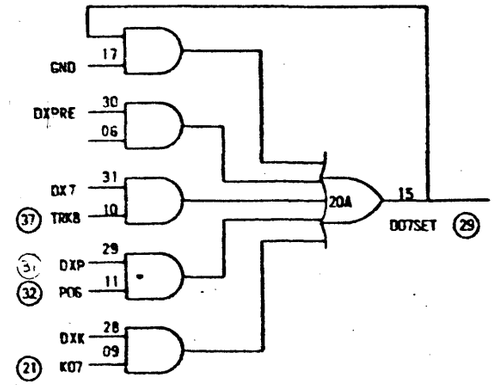


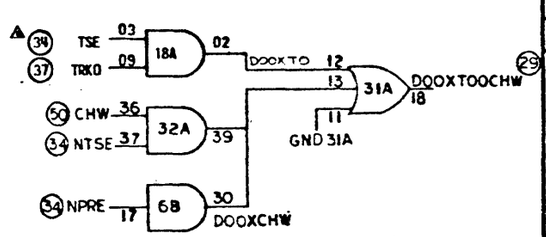












DIST CODE 409

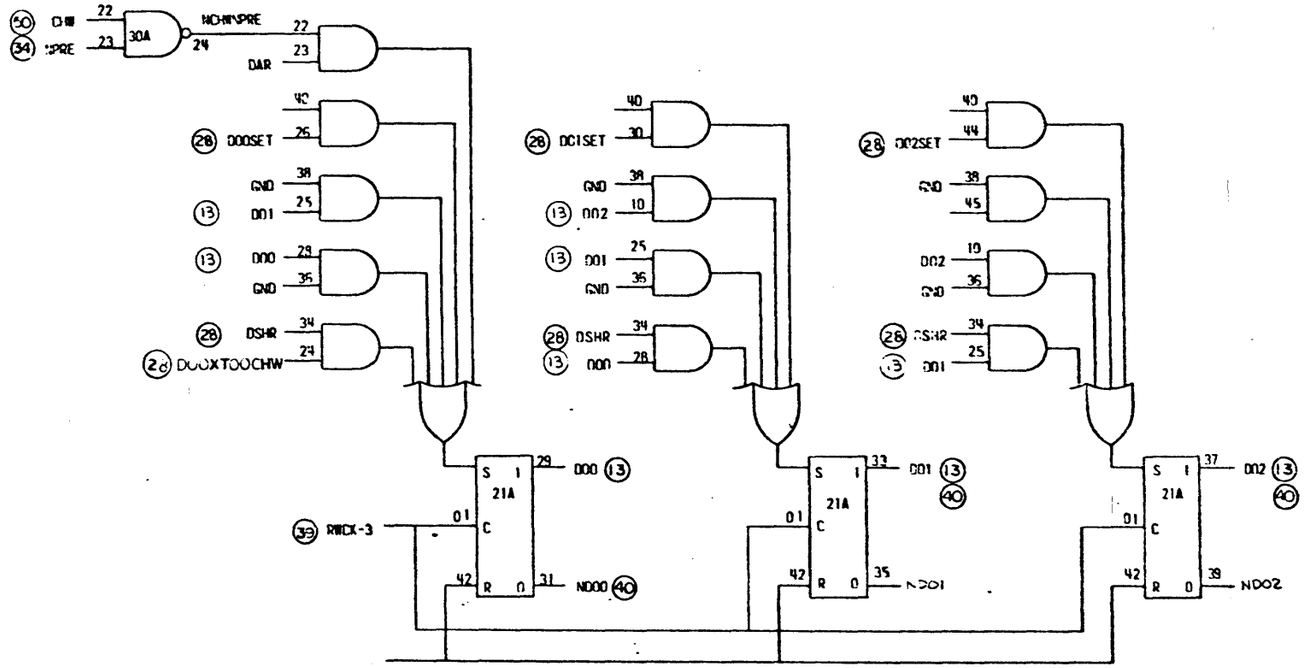
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

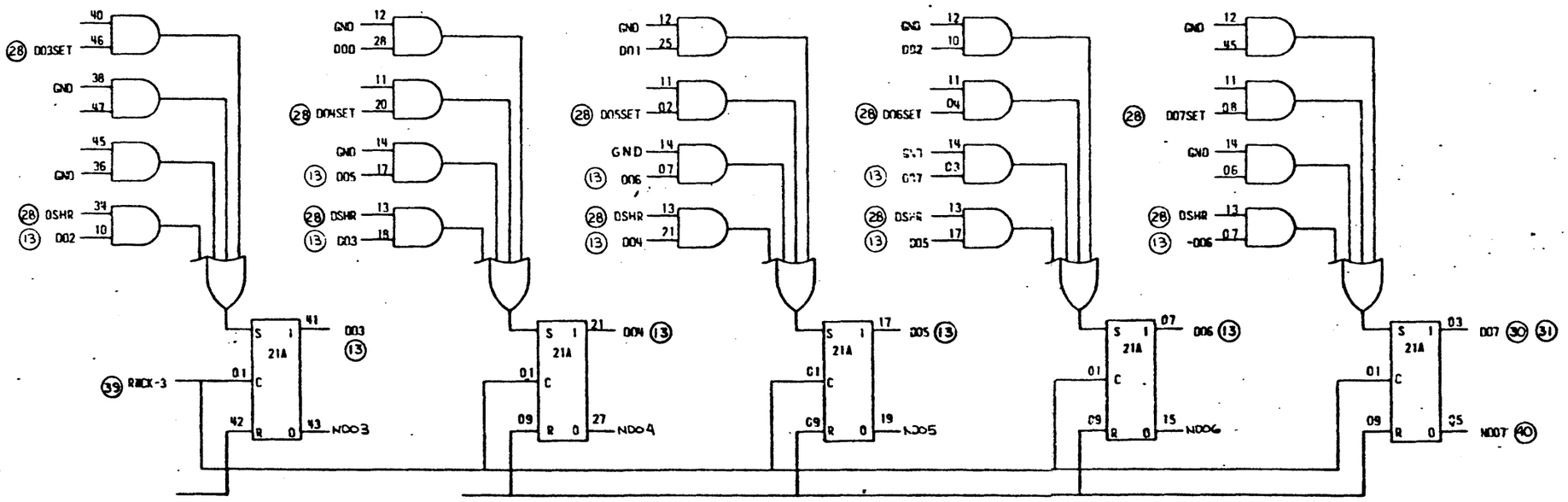
TITLE
DIAGRAM, LOGIC
CARTRIDGE DISK
CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A
SCALE ——	DO NOT SCALE DRAWING	SHEET 28 OF 61	

204492 A

REVISIONS				201492	A
LAL	REV	DESCRIPTION		DATE	APPROVED
X	A	MFG RELEASE, NO E O			





DATA REGISTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

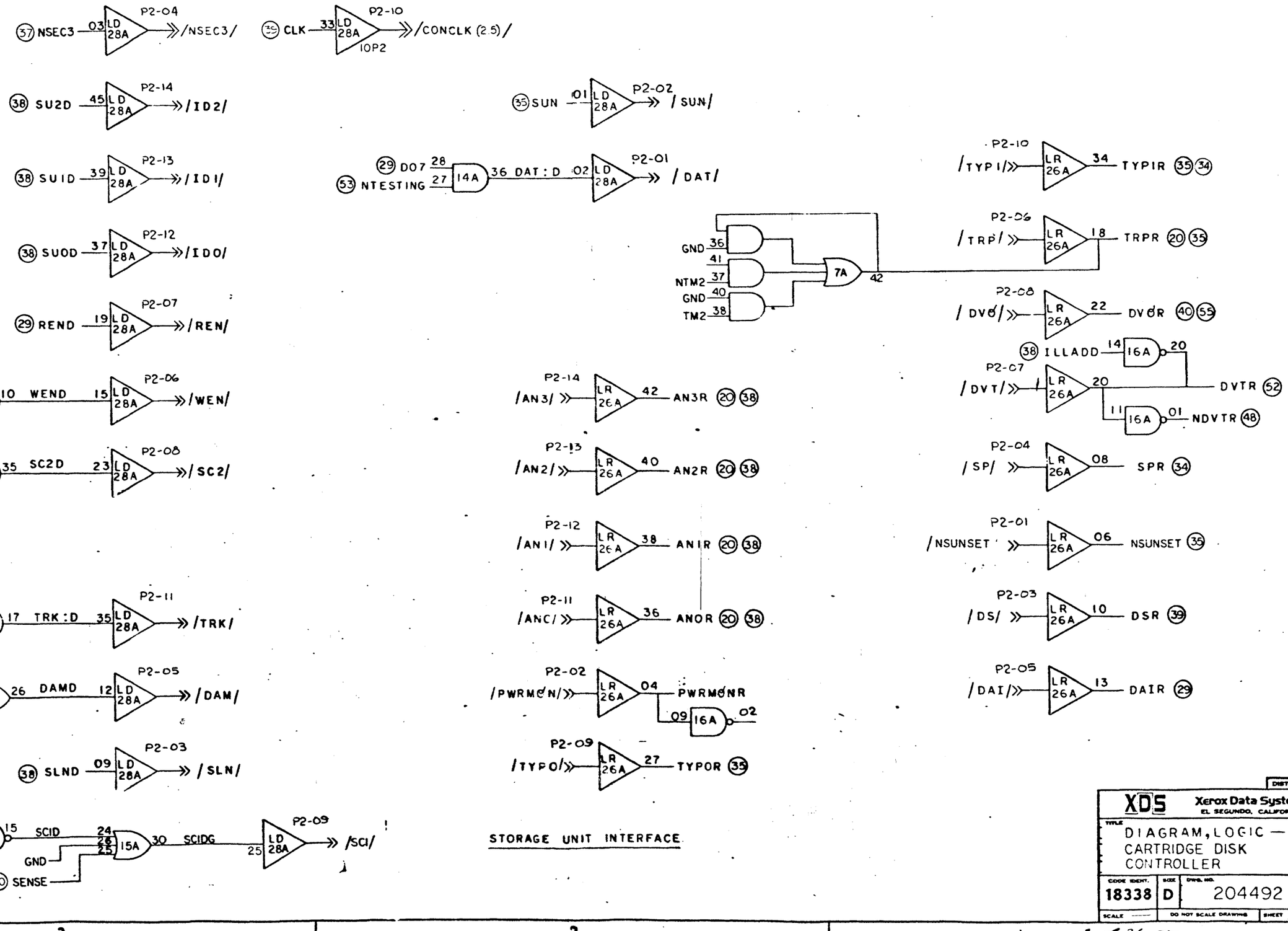
TITLE
DIAGRAM, LOGIC
CARTRIDGE DISK
CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A
SCALE —	DO NOT SCALE DRAWING	SHEET 29 OF 61	

204492 A

REVISIONS					
LAL	REV.	DESCRIPTION	CHG	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			

204492 A



STORAGE UNIT INTERFACE

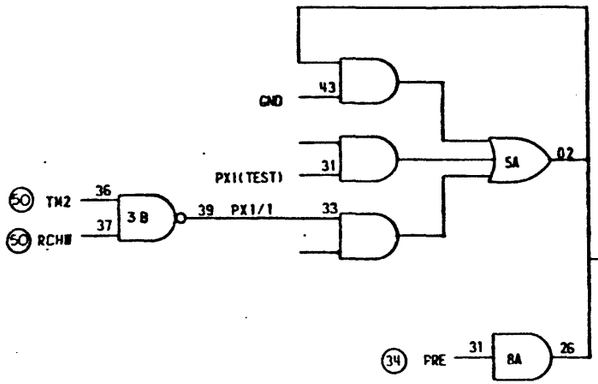
DIST CODE 409

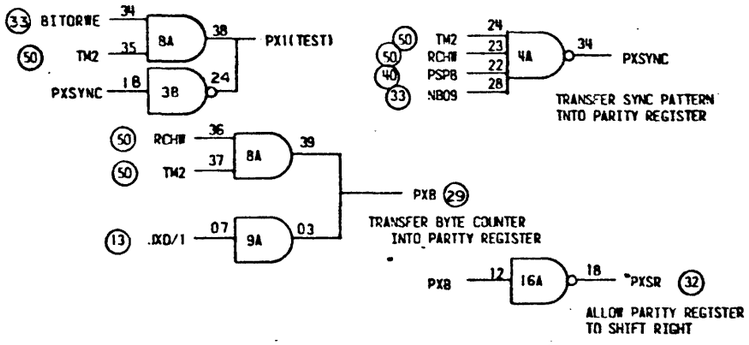
XDS Xerox Data Systems EL SEGUNDO, CALIFORNIA

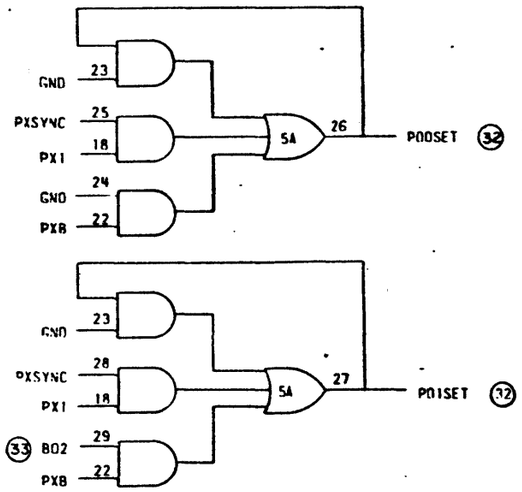
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

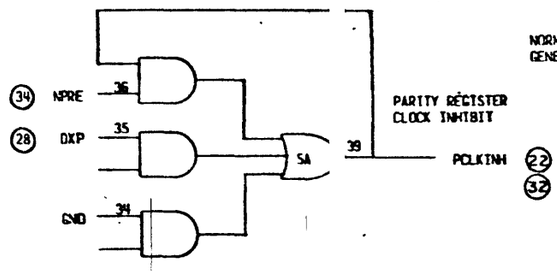
CODE IDENT.	SIZE	DWG. NO.	CONTENT LET. NO.
18338	D	204492	A
SCALE —	DO NOT SCALE DRAWING	SHEET 30 OF 61	

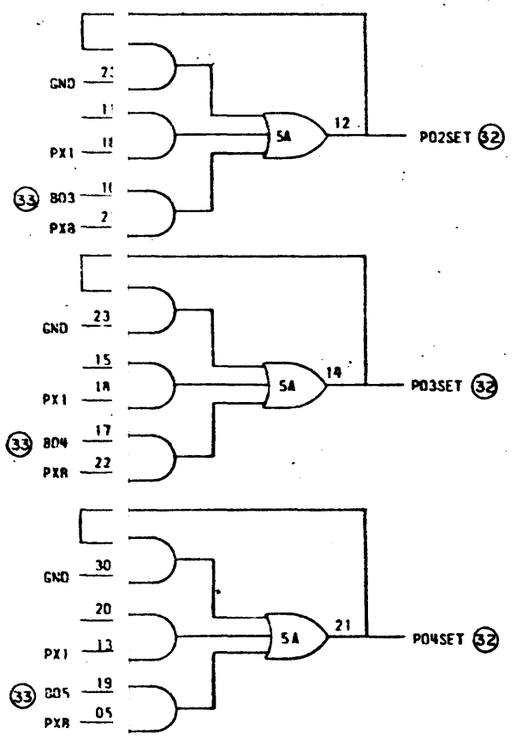
REVISIONS					204492	A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED	
X	A	MFG RELEASE NO E.O.				

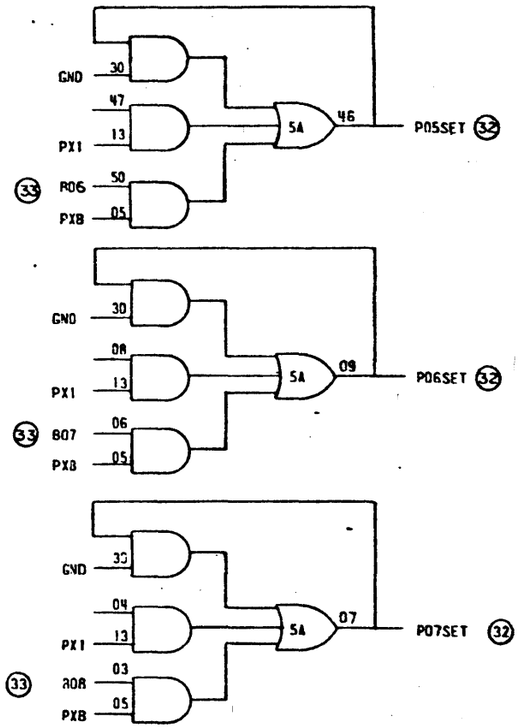












DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

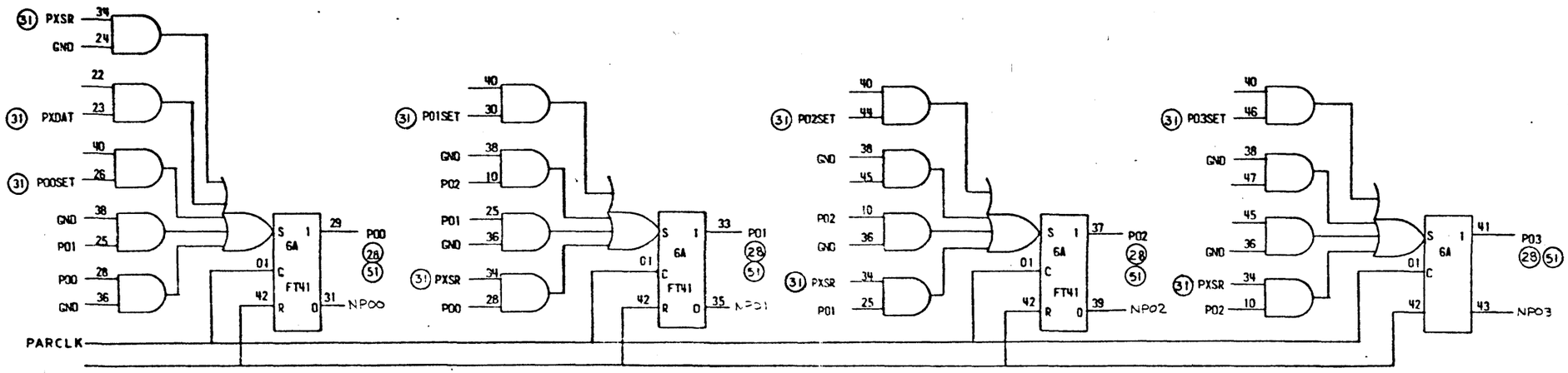
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

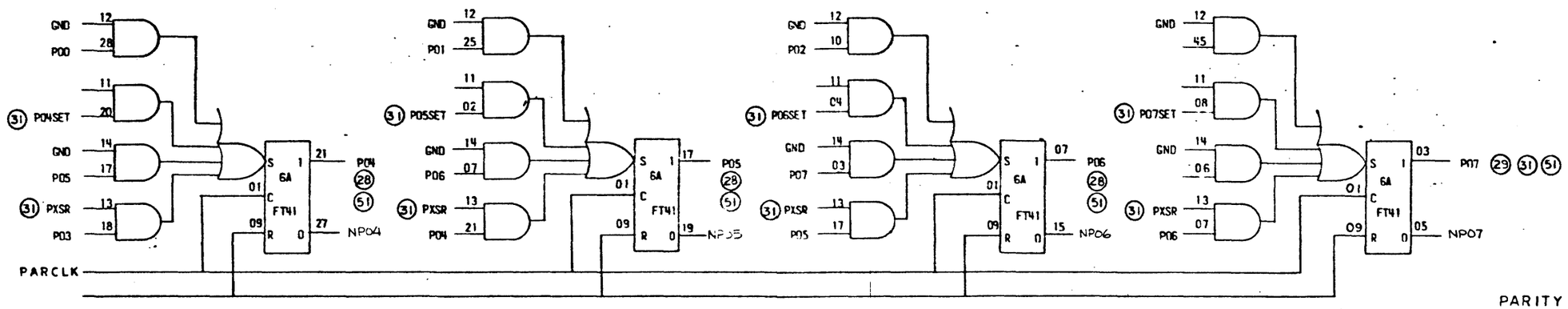
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 31 OF 61

204492 A1

REVISIONS				204492	A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.	[illegible]	[illegible]	[illegible]





PARITY REGISTER

DIST CODE 439

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

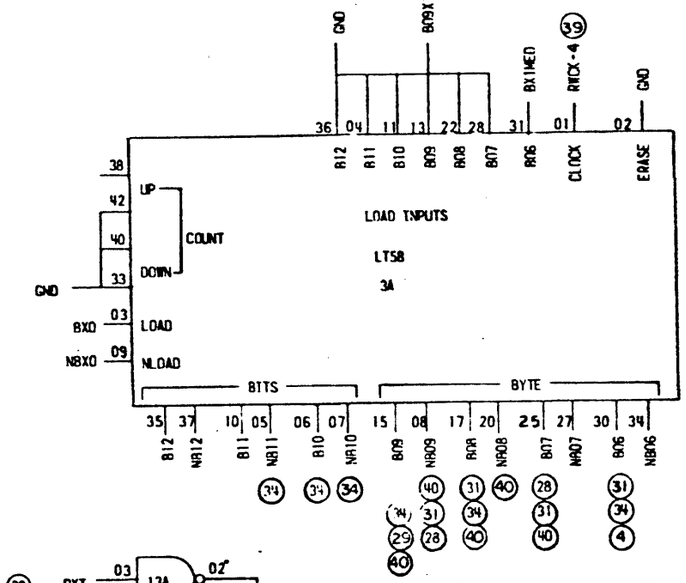
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

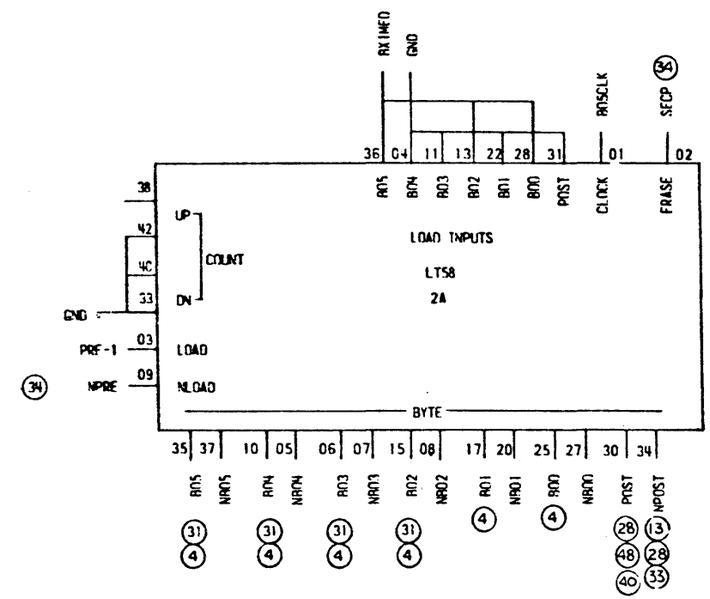
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

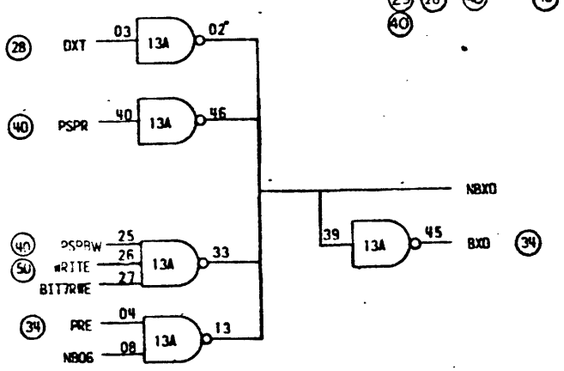
SCALE —— DO NOT SCALE DRAWING SHEET 32 OF 61

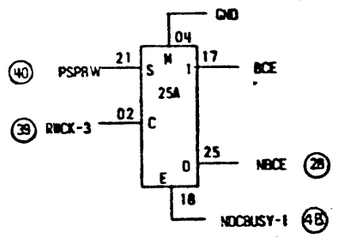
204492 A

REVISIONS				204492 A
LTR	REV.	DESCRIPTION	CHK	DATE
X	A	MFG RELEASE NO E C	JEW	1-31-79

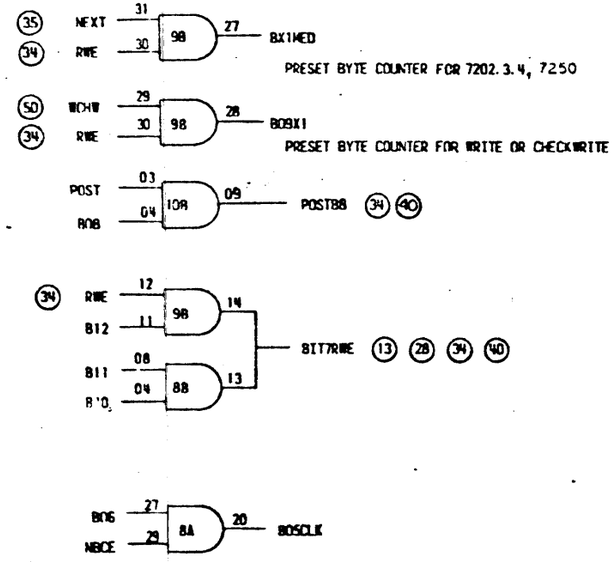


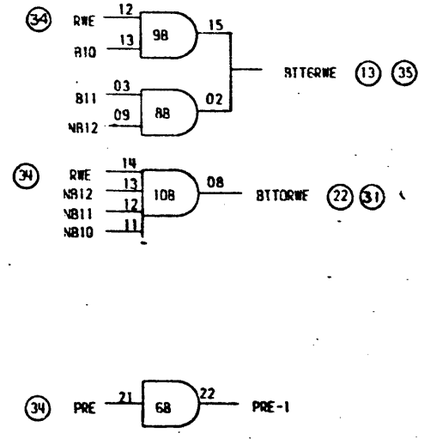






BYTE COUNTER ENABLE





BIT/BYTE COUNTER

DIST CODE 409

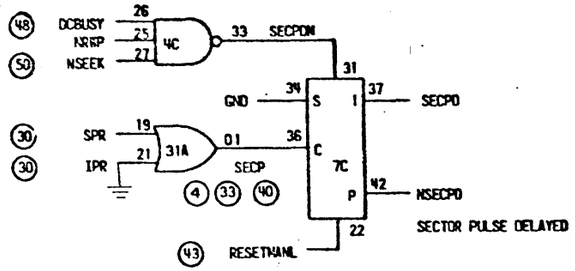
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

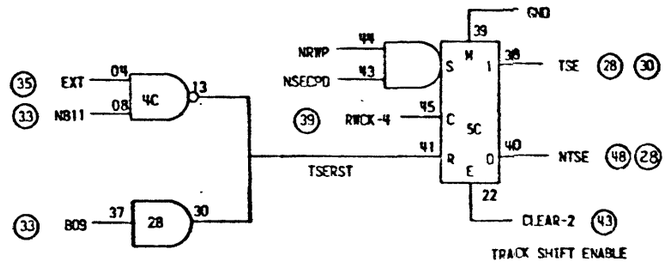
TITLE
DIAGRAM, LOGIC—
CARTRIDGE DISK
CONTROLLER

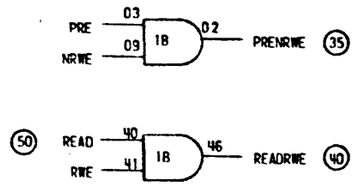
CODE IDENT.	SIZE	DWG. NO.	CHANGE LTR
18338	D	204492	A
SCALE —	DO NOT SCALE DRAWING	SHEET 330F61	

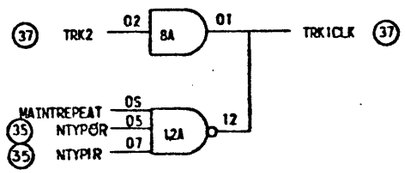
L. Hunter

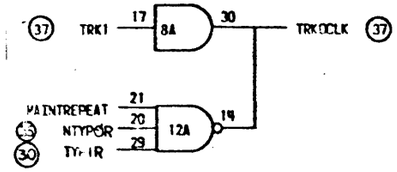
REVISIONS						D 2492 A
LTR	REV	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			

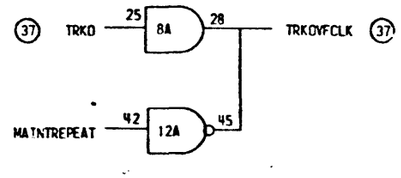


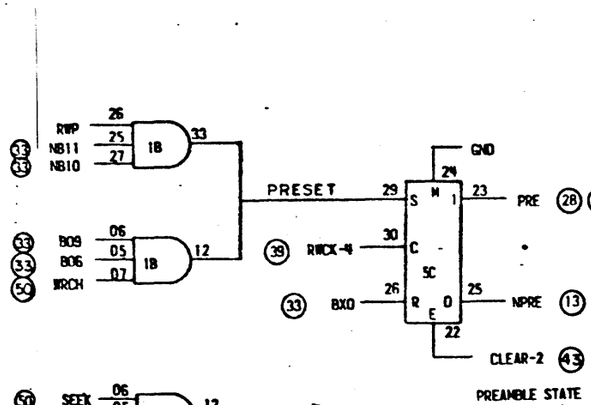


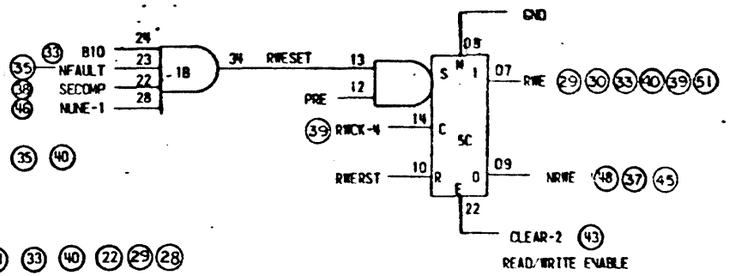


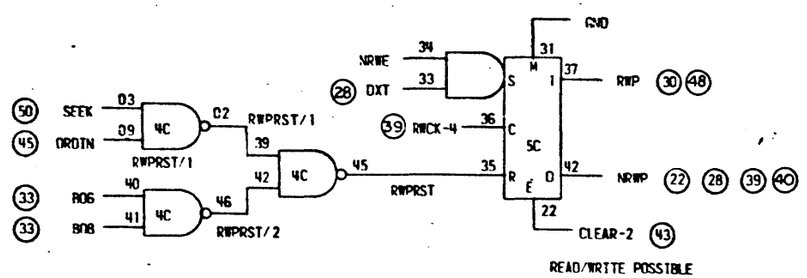


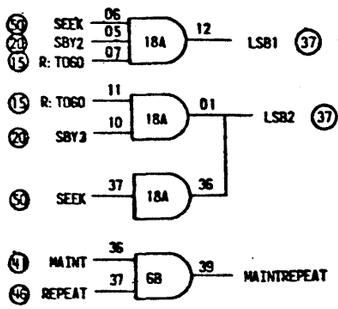


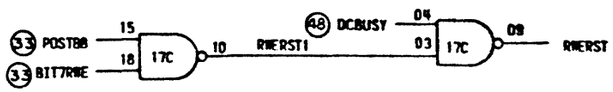












DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

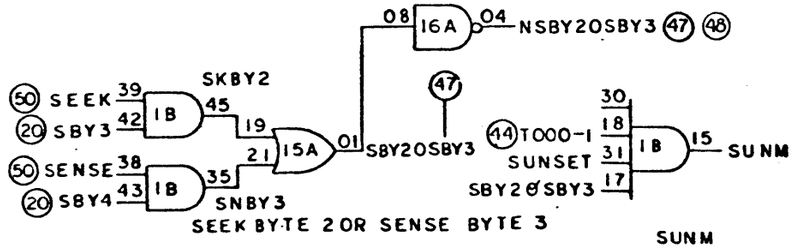
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

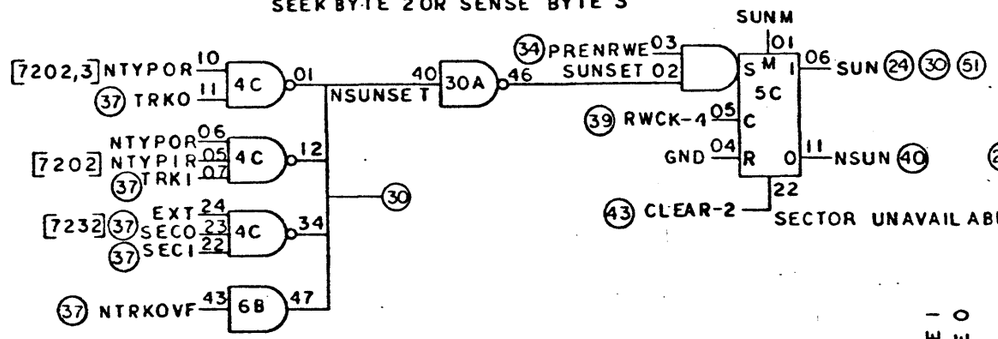
SCALE — DO NOT SCALE DRAWING SHEET 340F61

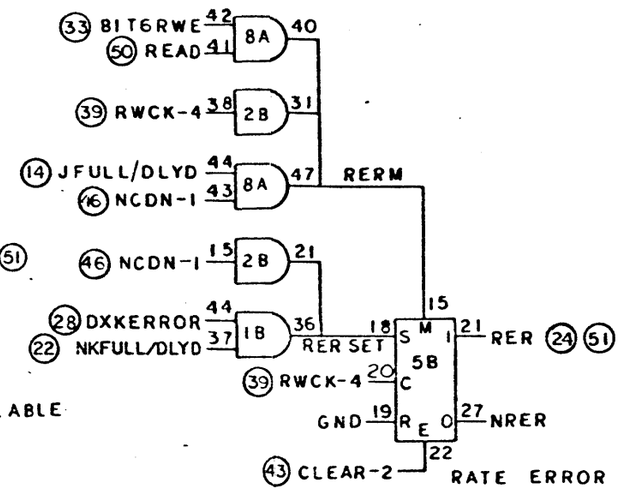
204492 A

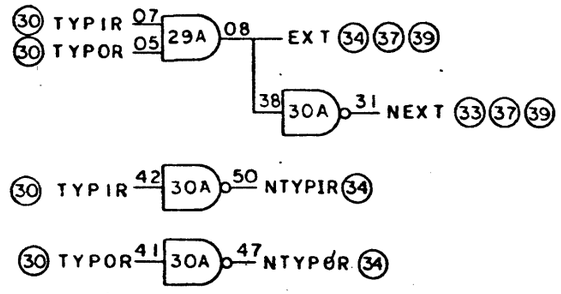
L. Hunter

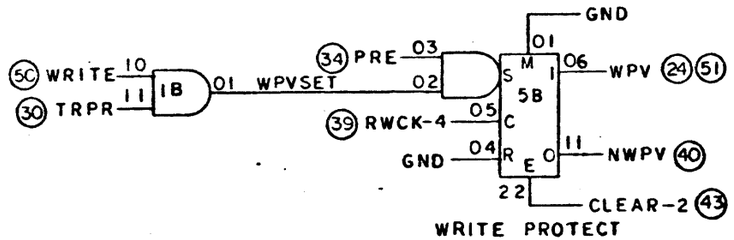
REVISIONS					204492 A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO. E.O.			



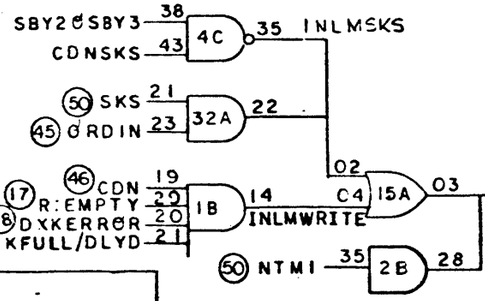


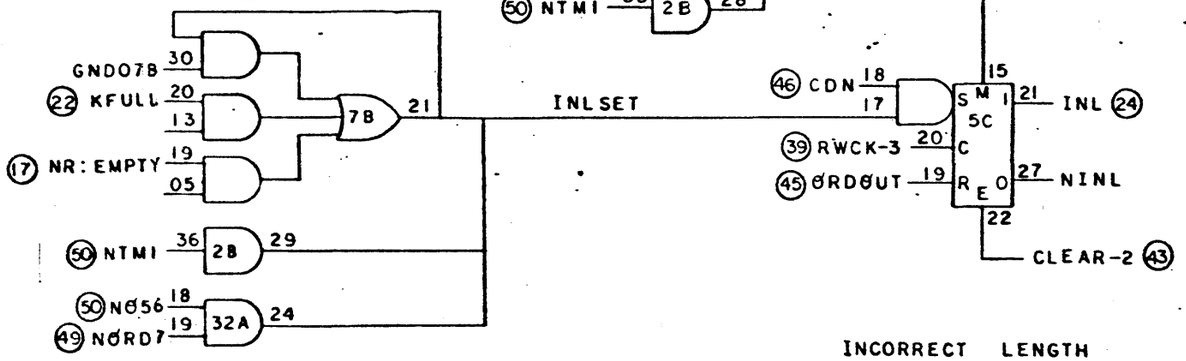


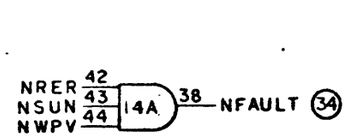


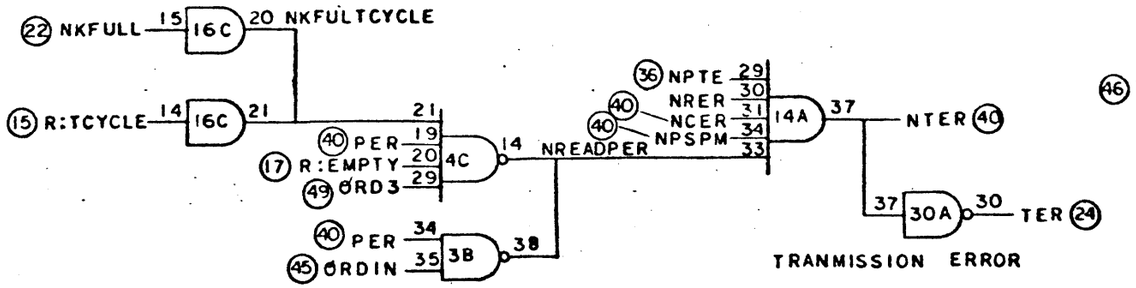


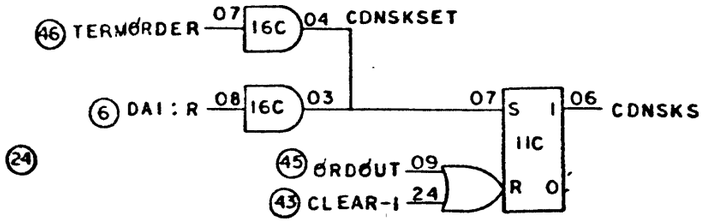
TYPE 1	TYPE 0	
0	0	7202
1	0	7203
0	1	7250,
1	1	7232











DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CONTROL LETTER
18338	D	204492	A

SCALE — | DO NOT SCALE DRAWING | SHEET 35 OF 51

204492 A

REVISIONS					204492 A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			

(7) CBPAR 14, 15 — (5) BPB 15 — 29A — 10 PCC1B

(10) CCPAR 04, 06 — (5) BPC 06 — 29A — 12 PCC1C

(10) CDPAR 09, 11 — (5) BPD 11 — 29A — 13 PCC1D

05, 06, 07 — 15A — 15 — PCC1

PCL 27, 29 — 29A — 20

(14) R:WRITE 23, (15) R:T200 21 — 29A — 22

PCLSET 35 — M 1 — 38 PCL

9C

ØRDØCAXO 36 — E 0 — 39 NPCL

PARITY CHECK LATCH

P2-9 /DAP/ — P3-K — LR 30C — 27 DAP:R 45 — S M 1 25A — 27 PAR (IØP)

GND 34

ØRDØCAXPAR 30 — C

E 0 — 44 NPAR (IØP)

18 — NDCBUSY-1 (48)

PARITY FROM IØP

(4) NWIDEINTR/2 45 — 1 — 46 NWIDEINTR/2-1 (19)

11C

CLEAR-1 24, 47 — 0 — 50 WIDEINTR/2-1 (19)

(14) (E/NJFULL) 18, (7) CAPAR 19 — 29A — 24

NPCL 44, WIDEINTR/2-1 37 — 19A — 36

PCC2 09, PCC3 10, PCC1 08 — 15A — 17 PARCNTRCLK — 01 C

(43) PHRSA 31, (45) ØRDOUT 33 — 29A — 26

(19) ØRDPAR 34, (44) PHCLK 35 — 29A — 38

PCL 25 — 29A — 28

ØRDØCAXO — 03 — 22 — S M 1 25A — 23 PARCNTR

E 0 — 20 NPARCNTR

18 — NDCBUSY (48)

PARITY COUNTER FOR INTERFACE PARITY DURING "OUT"

07, 10 — 22A — 26 PARGEN

C8 — PAR(IØP) 04 — 17A — 03

(5) NBP 36, (15) R:T 220 37 — 29A — 39

(14) R:WRITE 41, (45) NIN 42 — 29A — 40

(41) NMAINT 20 — 10B — 17

NPCL 24, WIDEINTR/2-1 23 — 13A — 34

PTESET 13 — M 1 — 12 PTE

9C

CLEAR-1 17 — E 0 — 14 NPTE (35)

PARITY TRANSMISSION ERROR

(45) ØRDOUT 45, (41) NMAINT 46 — 29A — 50 ØRDXPAR

GND 13, 11, 12 — 15A — 18 ØRDØCAXPAR

(6) CAX(IOP) 12

(43) PHRSA 17 — 29A — 30

GND 14, (49) ØRDXO 22, (6) CAXO 23 — 15A — 20 ØRDØCAXO

ØRDØCAXPAR 27, PC:R 29 — 68 — 20 PCLSET

36 — 27A — 37, 44 NED (46)

P2-11 /PC/ — LR 30C — 36 PC:R

03 — 02B — 05, 06, 07 NTEST (23)

P3M — LD 30C — 35 PC:D

13 — 18C — 04 DATAIN (45), 08 RS:D

(56) NINI-3 — 43 — 30C

18 — 16C — 12 NSKS (50)

PARITY COMPARE

DIST CODE 409

XDS Xerox Data Systems EL SEGUNDO, CALIFORNIA

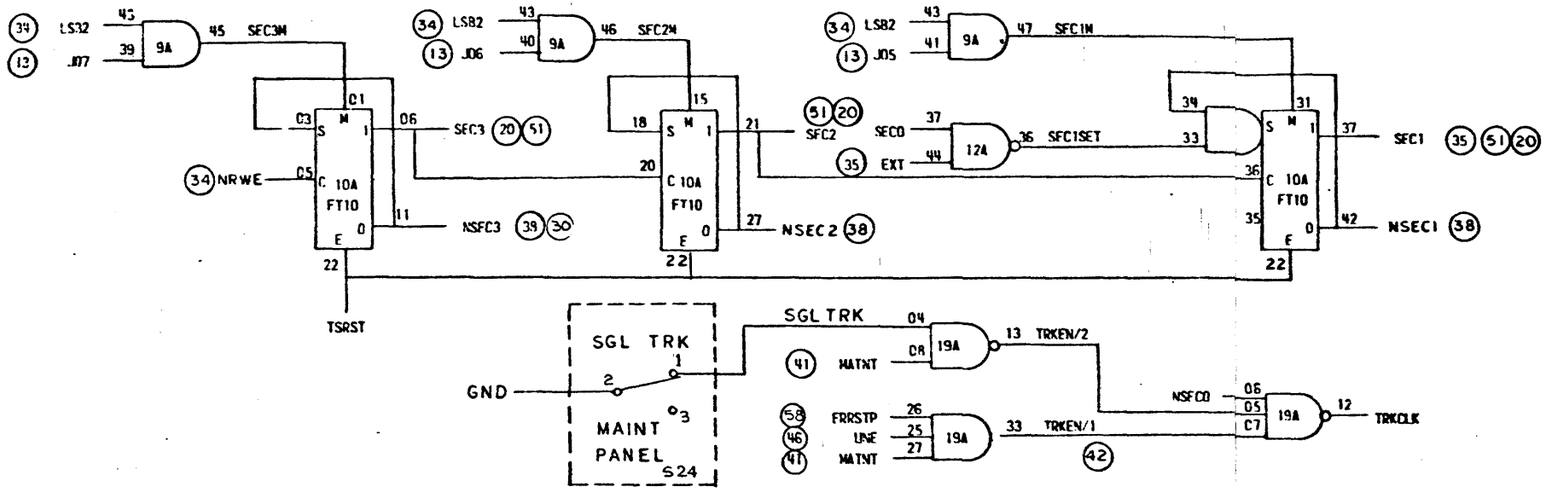
TITLE: DIAGRAM, LOGIC— CARTRIDGE DISK CONTROLLER

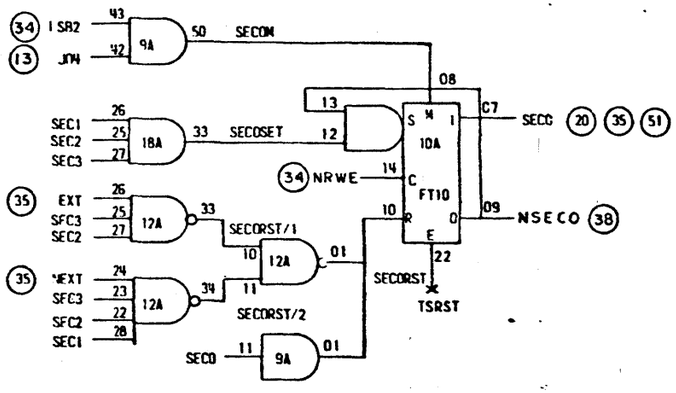
CODE IDENT.	SIZE	DWG. NO.	LATEST LETTER
18338	D	204492	A

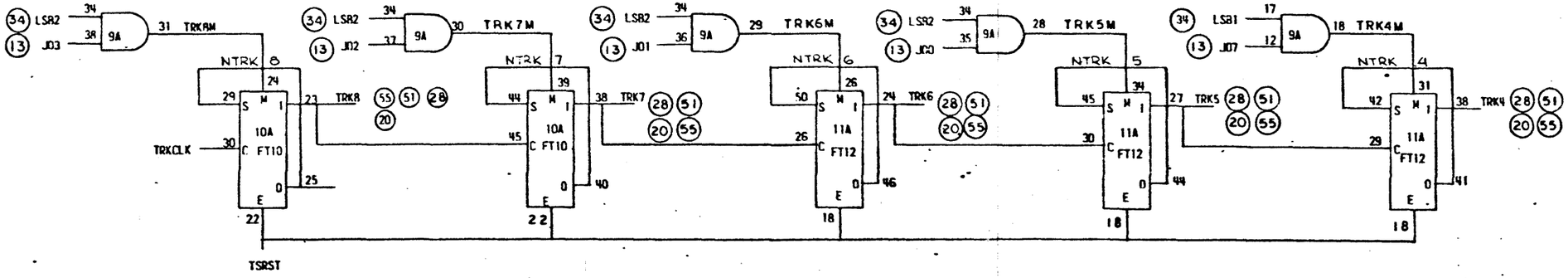
SCALE — DO NOT SCALE DRAWING SHEET 36 OF 61

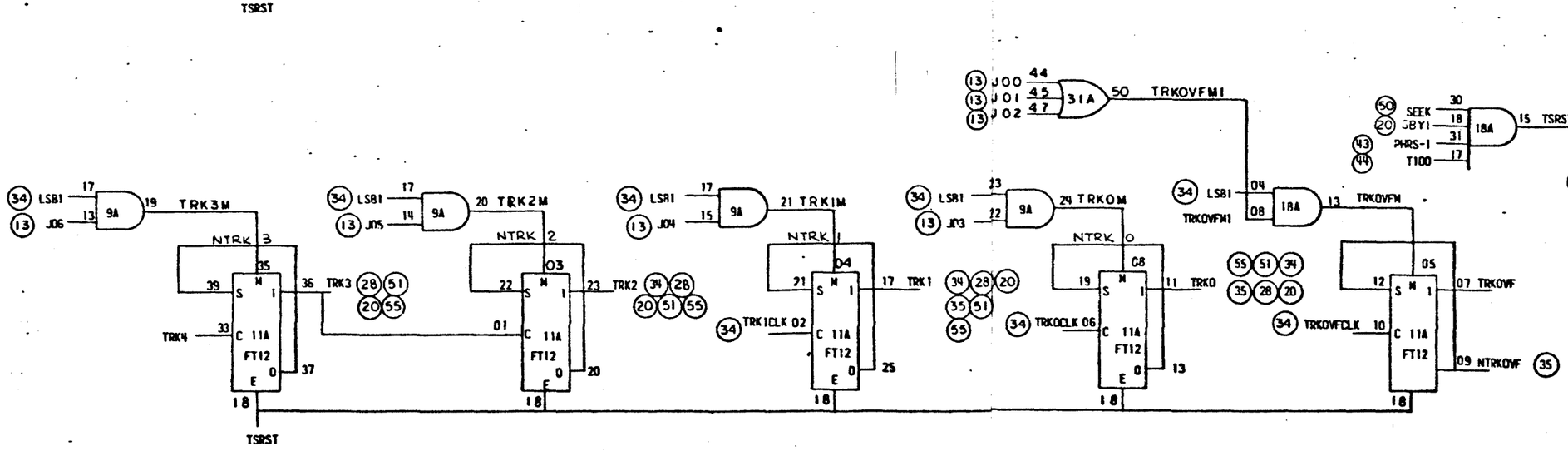
204492 A

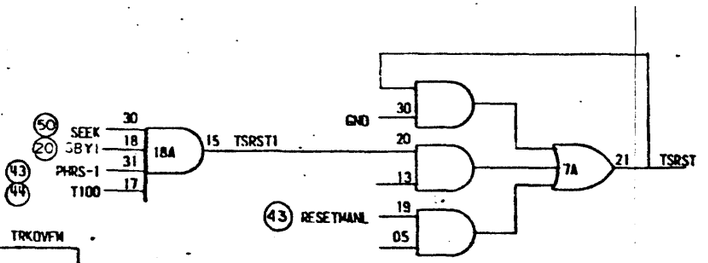
REVISIONS				204492 A
LAL	REV.	DESCRIPTION	DATE	APPROVED
X	A	MFG RELEASE NO E.O		











TRACK SECTOR REGISTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

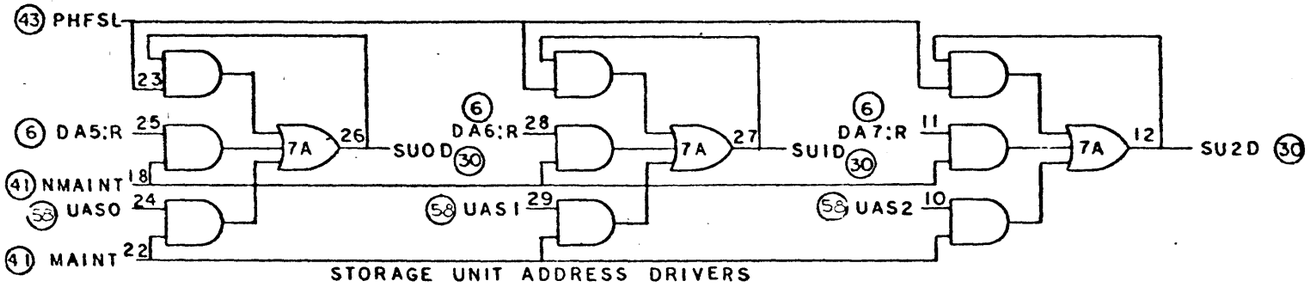
CODE IDENT.	SIZE	DWG. NO.	REVISION LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 370F 61

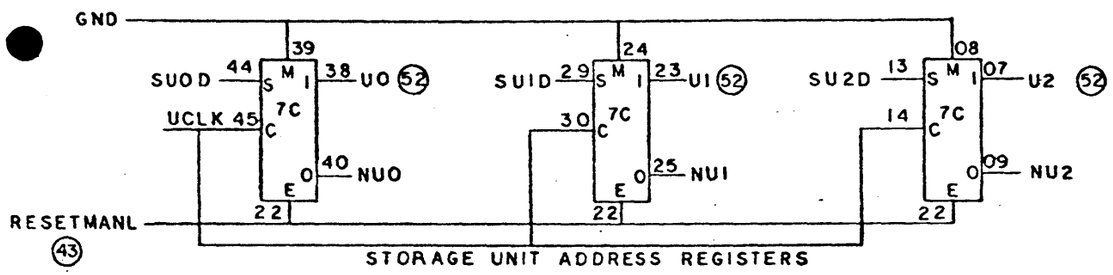
204492 A

L. Hunter

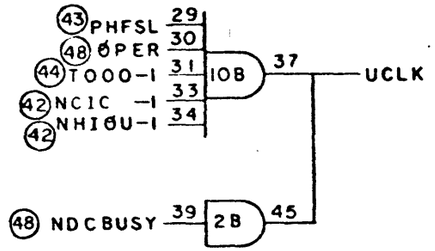
REVISIONS				204492 A
LAL	REV.	DESCRIPTION	DATE	APPROVED
X	A	MFG RELEASE NO E.O.		

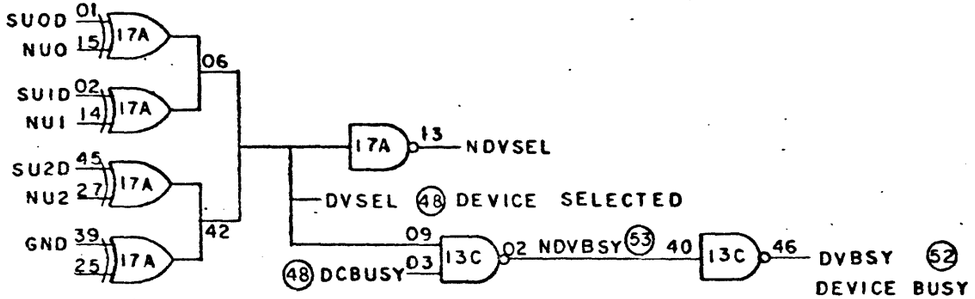


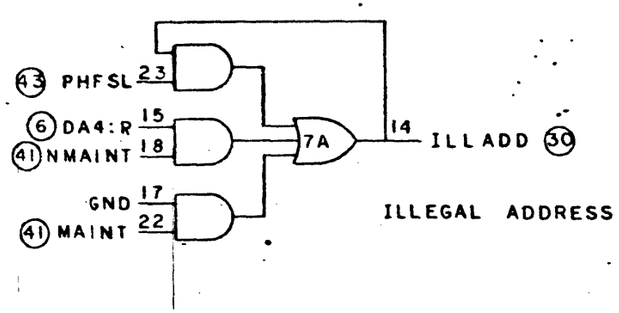
STORAGE UNIT ADDRESS DRIVERS

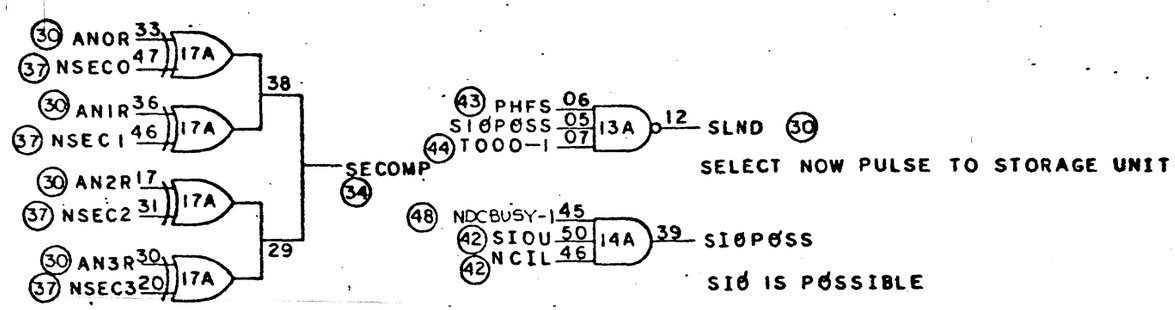


STORAGE UNIT ADDRESS REGISTERS









SECTOR COMPARESON

DIST CODE 409

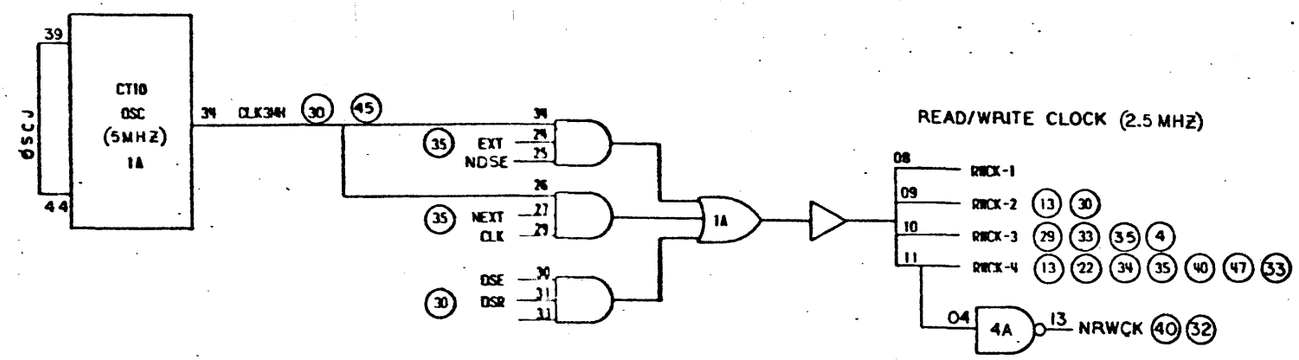
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

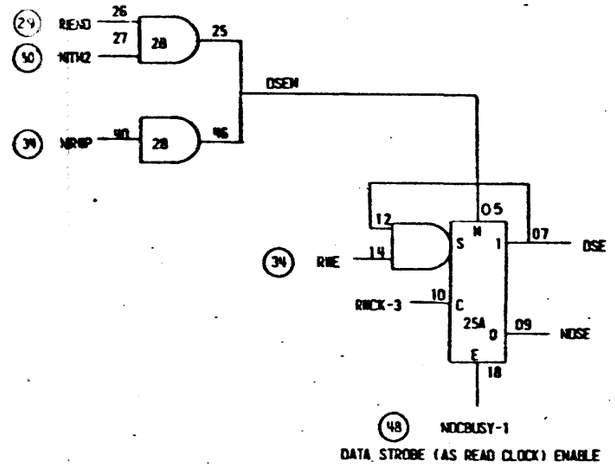
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

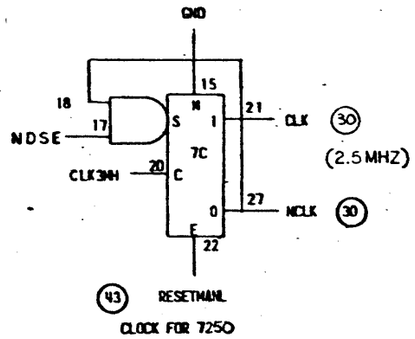
CODE IDENT.	SIZE	DWG. NO.	REVISION
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 380F61

REVISIONS				204492	A
LAL	REV.	DESCRIPTION	CHK.	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			







DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

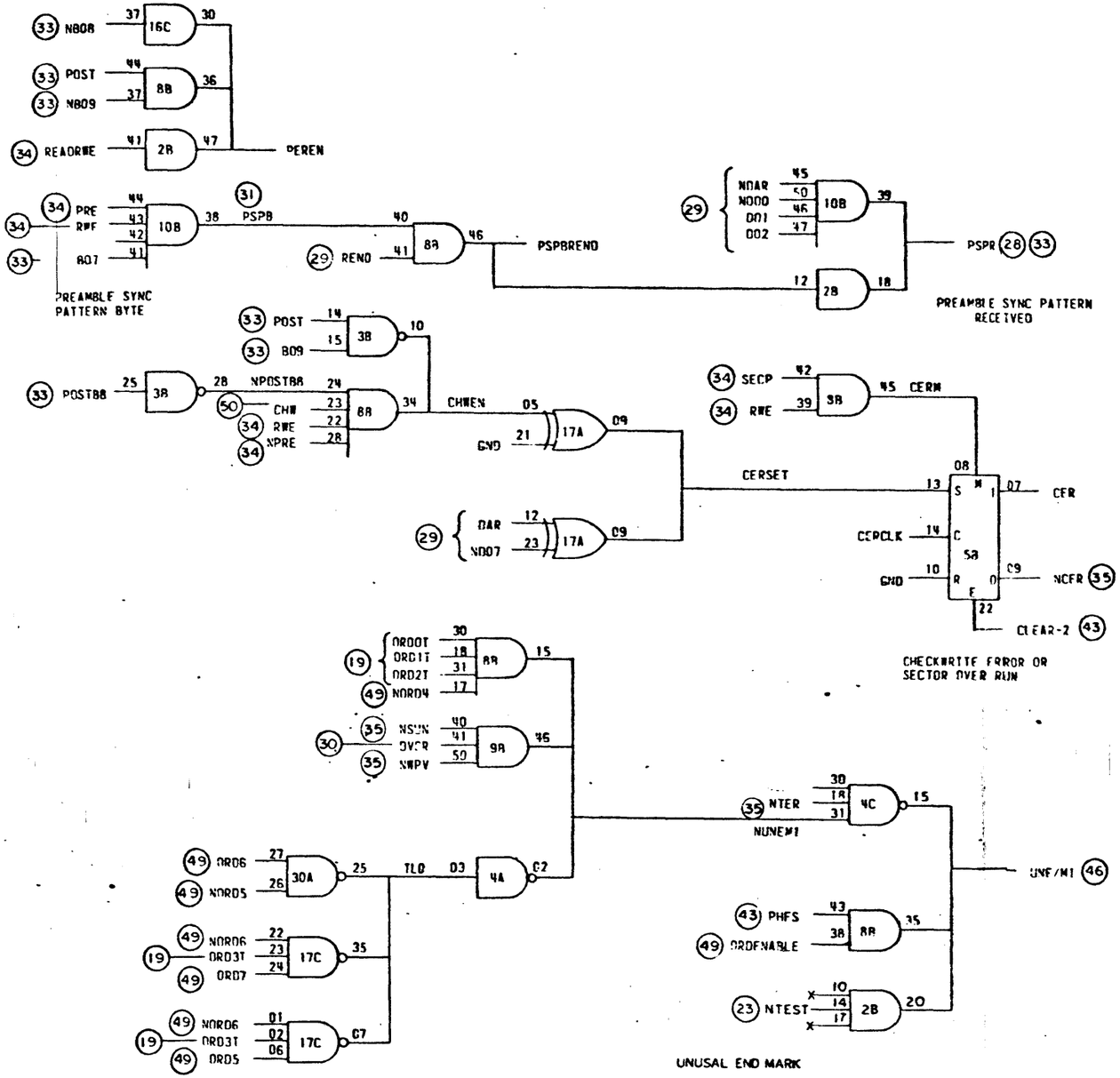
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 39 OF 61

L. Hunter

204492 A

REVISION			204492	A
LAL	REV	DESCRIPTION		
X	A	MFG RELEASE, NO E.O.		

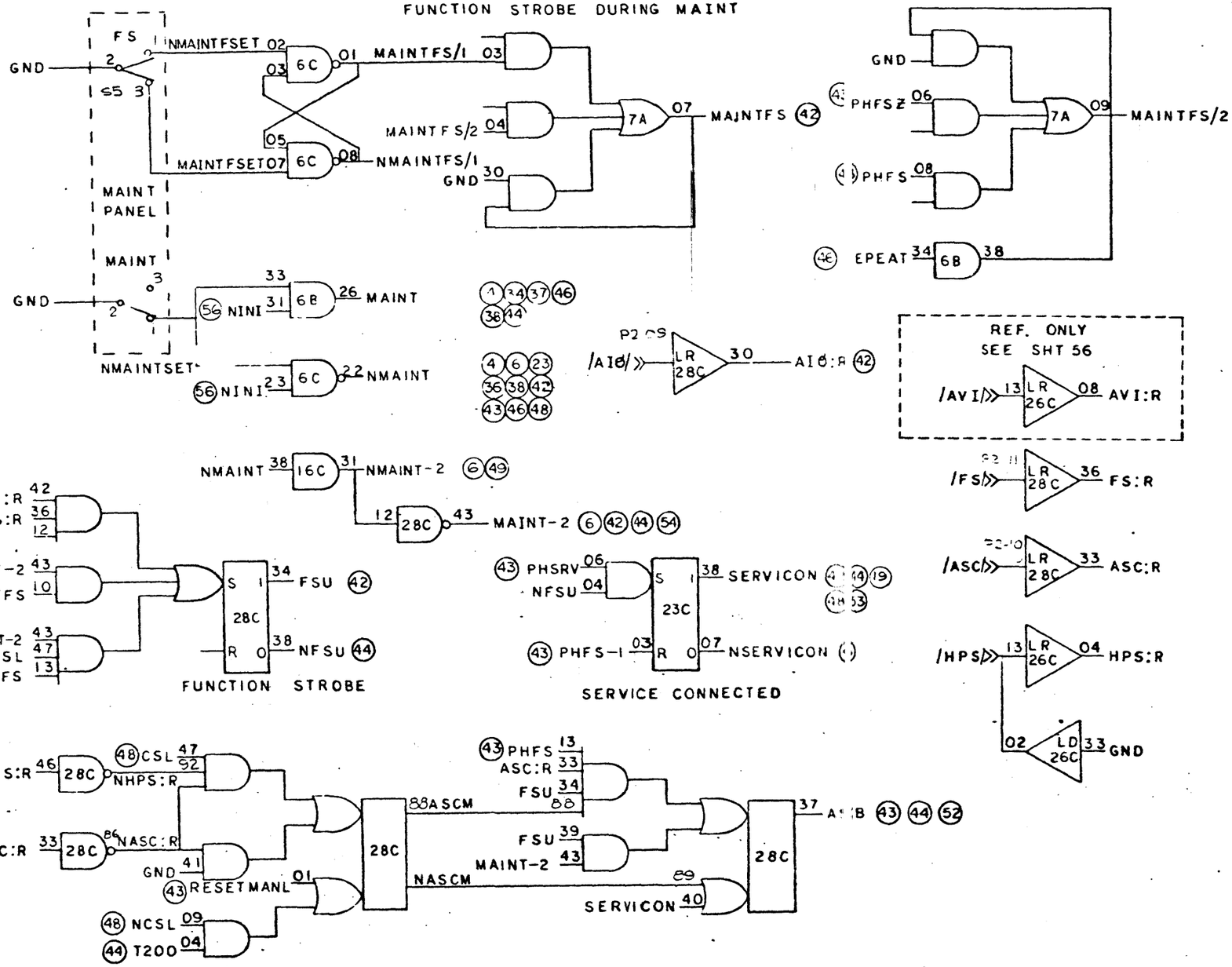


DIST CODE 403				
XDS Xerox Data Systems EL SEGUNDO, CALIFORNIA				
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER				
CODE IDENT. 18338	SIZE D	DWG. NO. 204492		REV A
SCALE —	DO NOT SCALE DRAWING	SHEET 40 OF 61		

204492 A

REVISIONS				20-JAN-92	A
LAL	REV	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O	AM		

FUNCTION STROBE DURING MAINT



DIST CODE 409

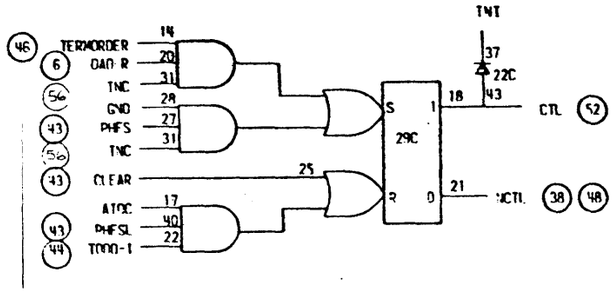
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

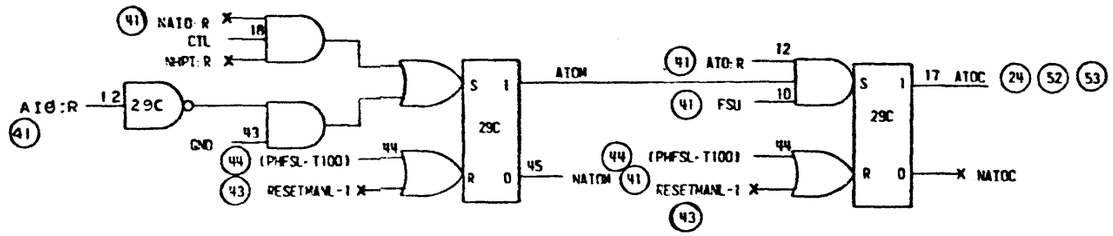
TITLE
DIAGRAM, LOGIC
CARTRIDGE DISK
CONTROLLER

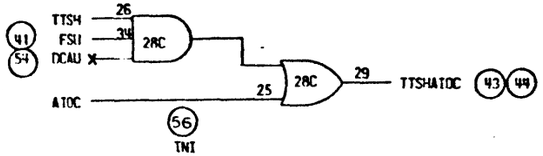
CODE IDENT.	SIZE	DWG. NO.	REV.
18338	D	204492	A

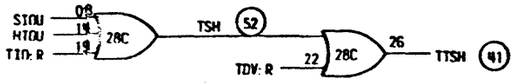
SCALE — DO NOT SCALE DRAWING SHEET 41 OF 61

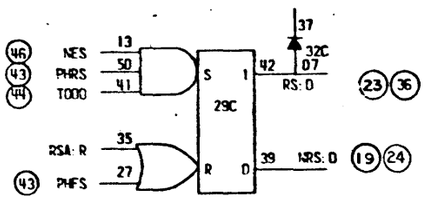
REVISIONS			204492	A
LAL	REV.	DESCRIPTION	DATE	APPROVED
X	A	MFG RELEASE NO E.O		

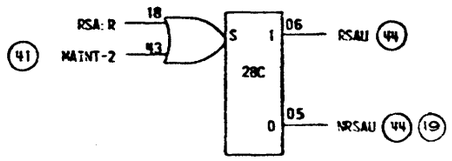


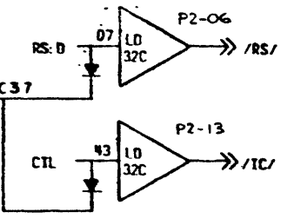


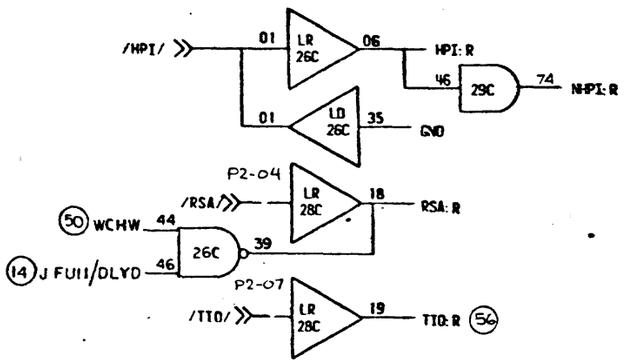


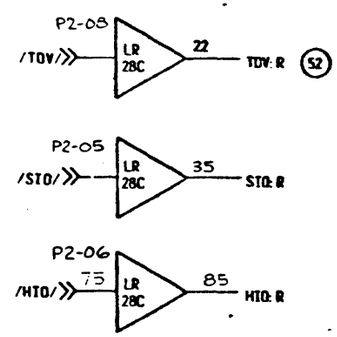


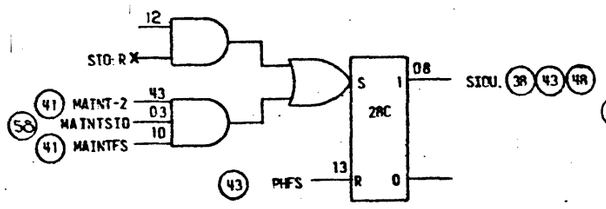


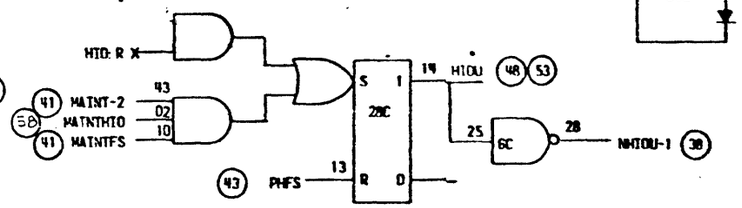


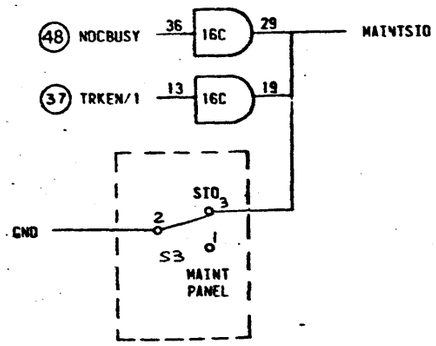












DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

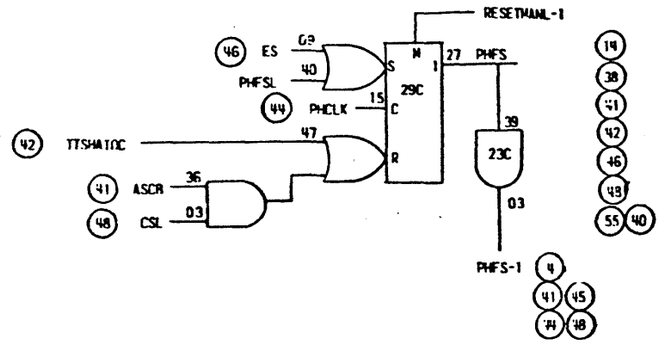
CODE IDENT.	SIZE	DWG. NO.	CONTROL LETTER
18338	D	204492	A

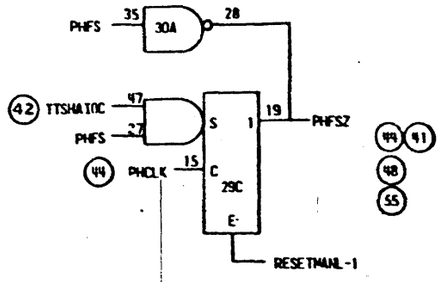
SCALE — DO NOT SCALE DRAWING SHEET 420F61

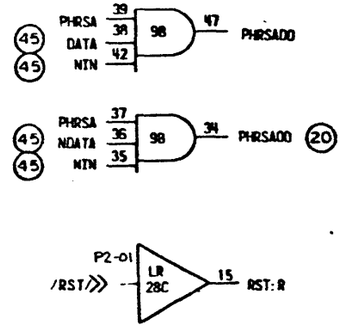
204492 A

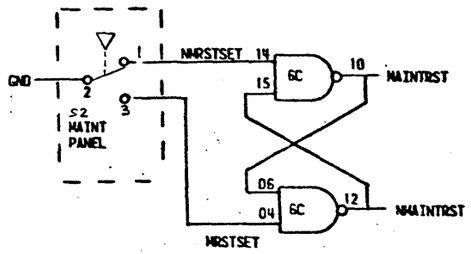
L. Hunter

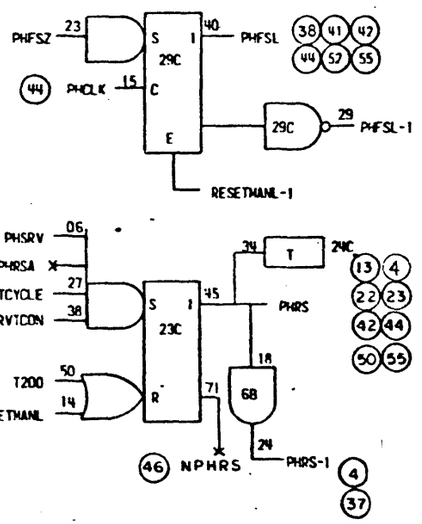
REVISIONS				204492 A
LAL	REV.	DESCRIPTION	CHK	DATE / APPROVED
X	A	MFG RELEASE NO E.O.		

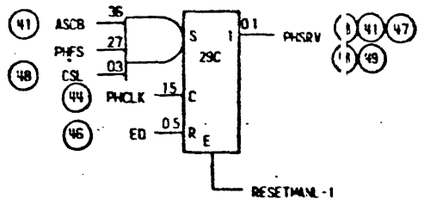


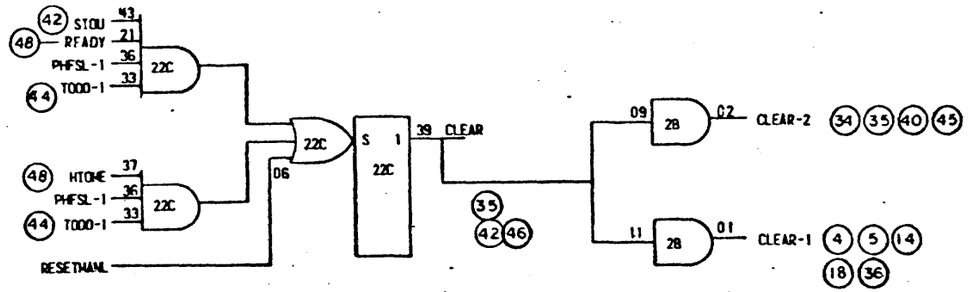


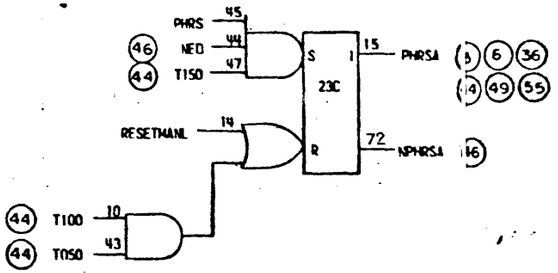


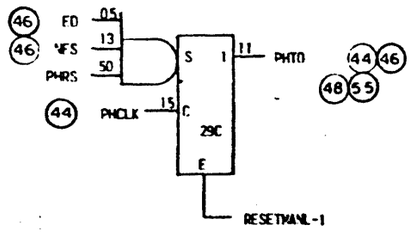


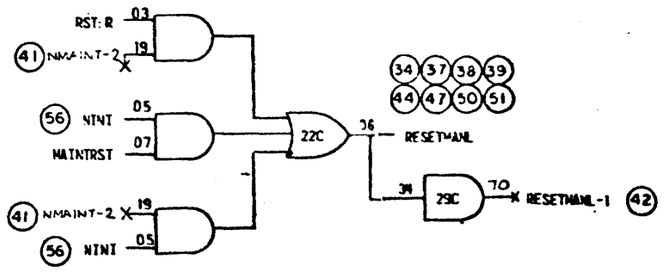












DEPT CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC - CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 43 OF 61

204492 A

REVISIONS			04492	A
LTR	REV	DESCRIPTION		
X	A	MFG RELEASE NO E.O.		

GND078 X 30 7B
(50) TESTØRD 47 13 X 7B
(23) TEST 50 5 X 7B
7B 46 TSTART 1/1

(50) TSTART1/1 24
SKS 25
(45) NDATA 26
31A 30 TSTART 1

(22) KFULL/DLYD 29
GND 27
(46) ED 28
31A 35 TSTART (READ)

(50) READ 40
27A 46

TSTART (READ) 33
TSTART 1 31
TSTART (WCHW) 37
31A 34 TSTART (PHRS)

(50) WCHW 03
(13) NJFULL/DLYD 09
27A 02 TSTART (WCHW)

(43) PHRSA 15
T000 34
S 1
23C
R
17 PHRSAT000W (46) (49)

11 16C 1 PHRSAT000W-1 (6) (14) (16) (18) (19) (20) (22)

T1C0 10
NT050 30
(43) PHFS-1 03

(46) NES 30
PHRSAT000W 29
31C
(45) NIN 28
31C
S
31C
R
T000 26
23 NTSTØP

(43) PHFS-1 40
(41) ASCB 39
31C

(43) PHFS-1 40
(42) TTSHAIØC 41
31C

(43) PHFSZ 33
31C

(43) PHFSL 42
(41) NFSU 43
31C

(43) PHTØ 31
(42) RSAU 45
31C

(43) PHRSA 44
(42) RSAU 45
31C

(43) PHRS 38
(42) NRSAU 34
(41) SERVICON 36
TSTART (PHRS) 35
31C

(41) (43) PHRS 38
MAINT-2 37
(41) SERVICON 36
TSTART (PHRS) 35
31C

31C

T100 25
NTCYCLE 04
S 1
31C
R 0
27 NT000

T
T000 26
(4) (5) (6) (13) (23) (42) (48) (49)

31C Δ50 NS
T
NT050 46
T050 47
24C13

31C Δ50 NS
T
T100 22
(13) (22) (37) (36) (43) (50)

24C14

31C Δ50 NS

T 24C18
T150 24
(43)

31C Δ50 NS
T 24C20
20 T200 (41) (43)
01

NTSTOP 23
T100 22
S 1
31C
R
02 PHCLK (36) (43) (45) (48)

T100 10
(43) PHFSL-1 11
S
23C
R
08 (PHFSL-T100) (42)

T100 10
GND
S M 1
23C
MAINTPULSE 09
C
E
05 PHASE STEP

(41) MAINT 43
SGLPH 44
6C 47 NMAINTSGLPH 12
(43) RESETMANL 14
23C

T100 22
T150 24
T200 20
21
S 1
31C
R 0
04 NTCYCLE
12 TCYCLE (43) (46) (48)
24C30
T

PHASE STEP
GND
2 3
S28
2 of 3
S27
SGL PHASE MAINT PANEL
NMPULSET 09
11 6C 13 MAINTPULSE
MULT
SET 27 6C 29 20 NMAINTPULSE
NSGLPH
46 6C 50 SGLPH

T 24C40
T000 30
S 1
22C
R 0
33 T000-1 (35) (38) (42) (43) (46)
NT000-1 (48)

DIST CODE 409

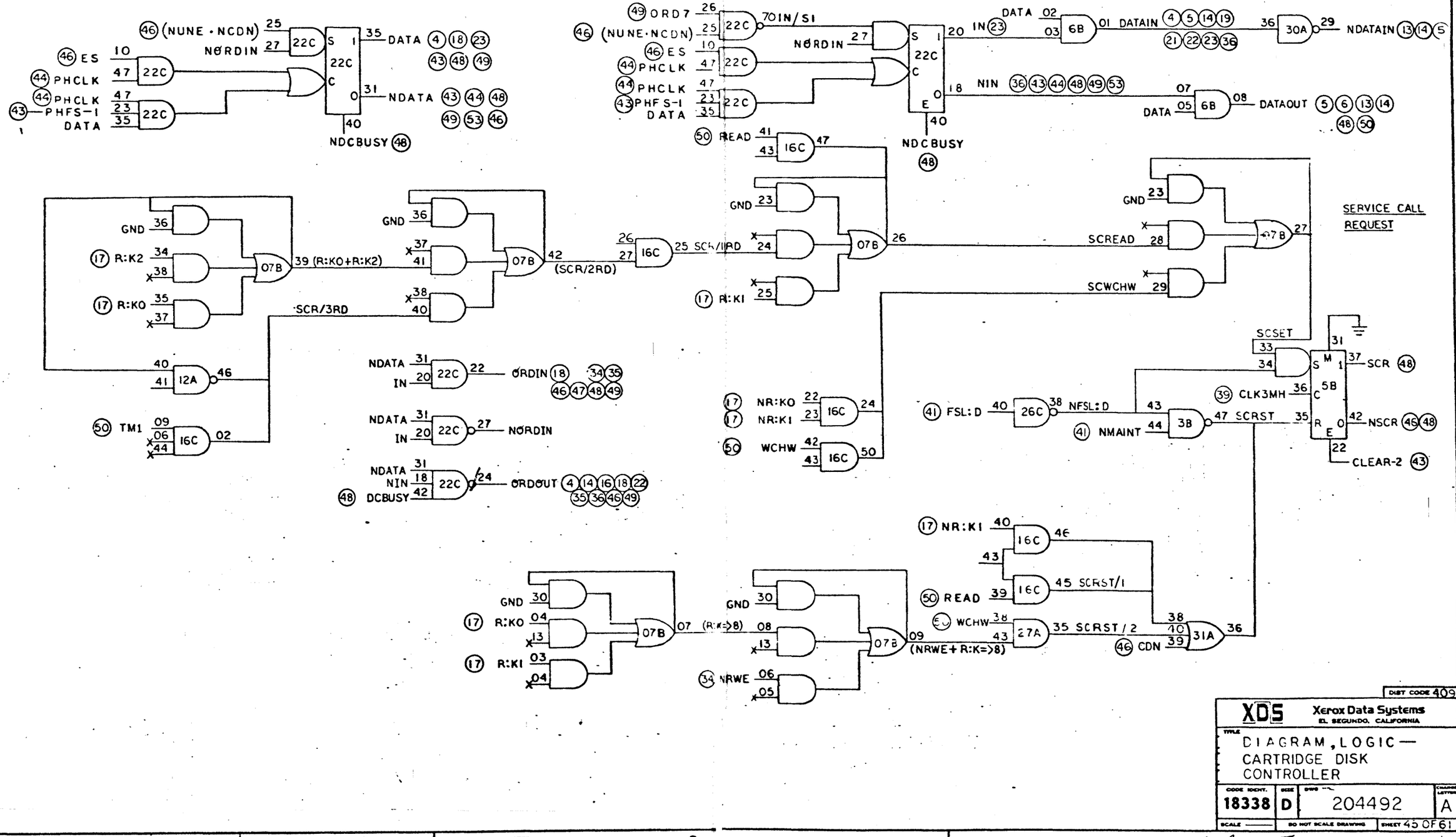
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A
SCALE	DO NOT SCALE DRAWING	SHEET 440F 61	

204492 A

REVISIONS					204492 A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.			



DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

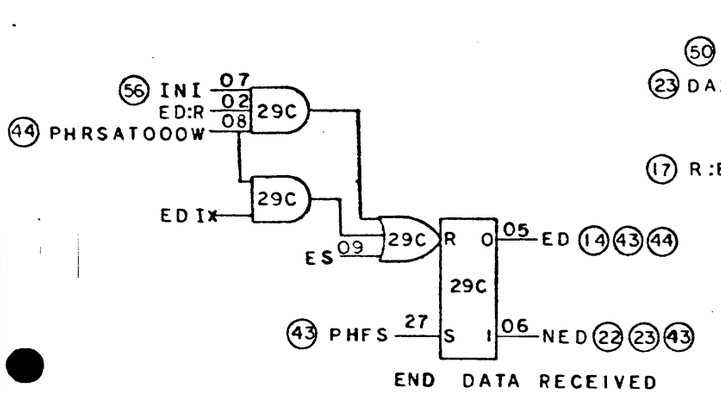
TITLE
DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

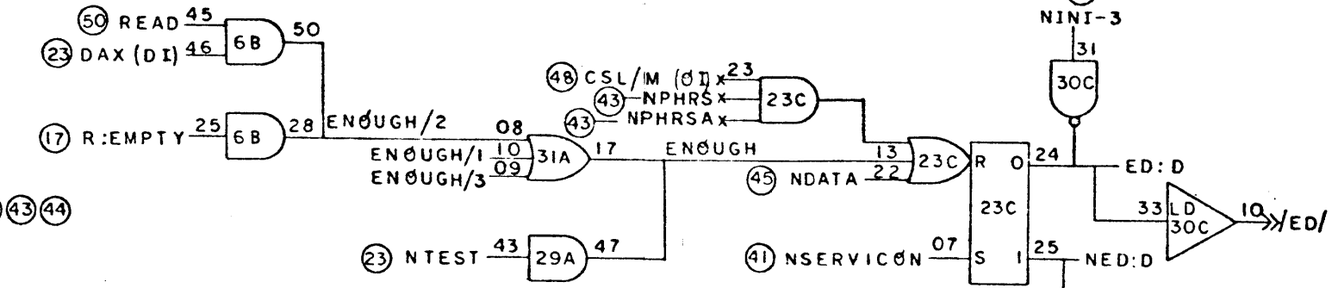
CODE IDENT.	SIZE	DWG —	CHANGE LETTER
18338	D	204492	A

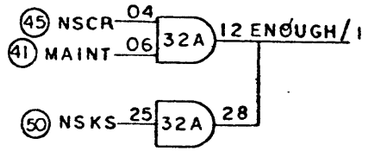
SCALE — DO NOT SCALE DRAWING SHEET 45 OF 61

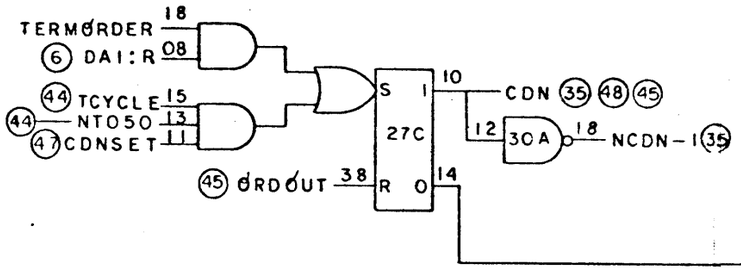
204492 A

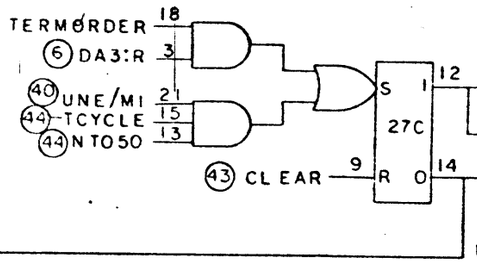
REVISIONS			204492	A
LTR	REV.	DESCRIPTION		
V	A	MFG RELEASE NO E.O		

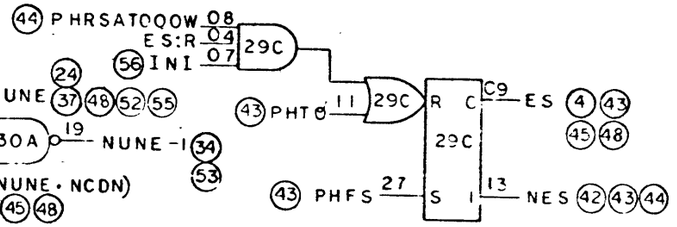


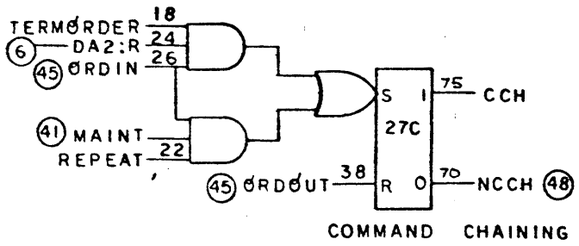


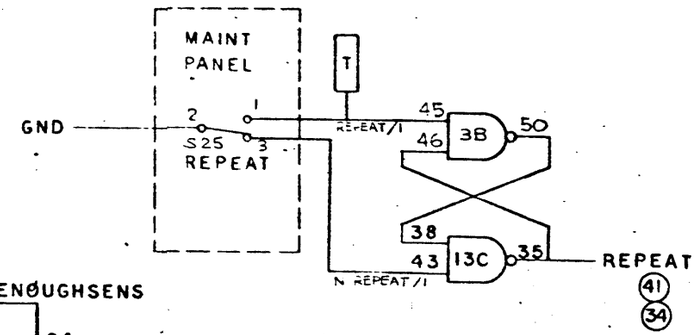


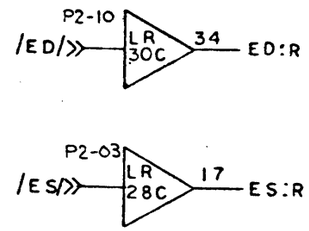


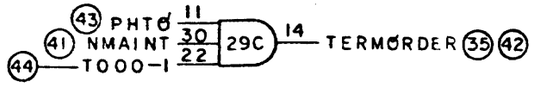


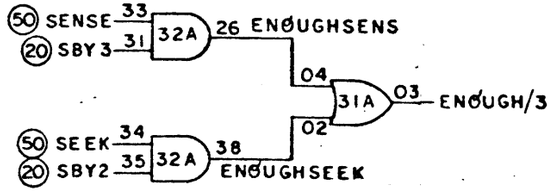












DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

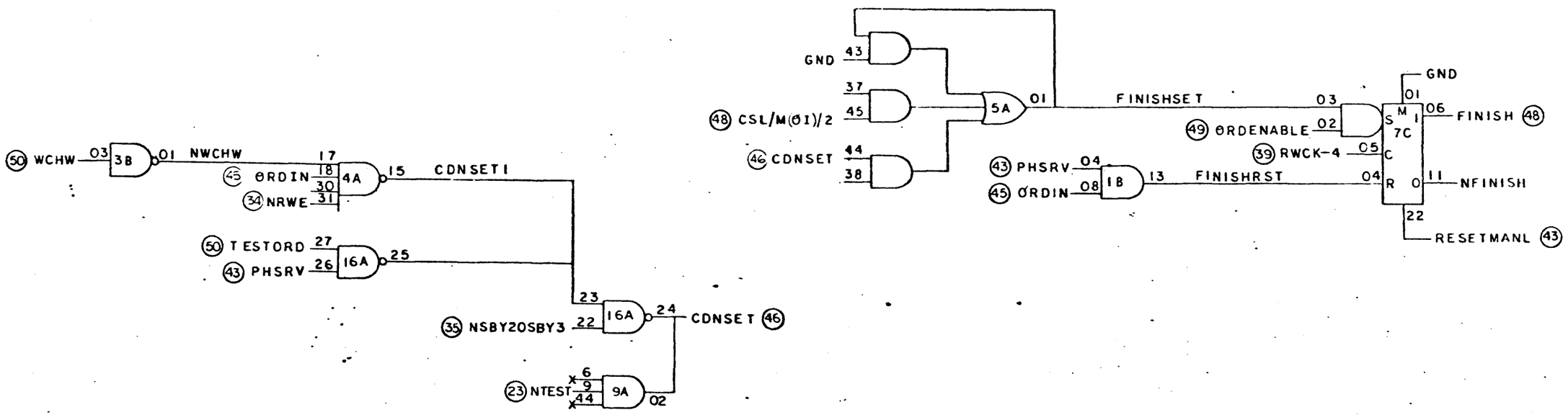
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 46 OF 61

204492 A

REVISIONS				204492	A
LTR	REV	DESCRIPTION		APPD	
X	A	MFG RELEASE NO E.C.			



DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE
DIAGRAM, LOGIC —
CARTRIDGE DISK
CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	REVISION LETTER
18338	D	204492	A

SCALE —— DO NOT SCALE DRAWING SHEET 470F61

L. Hunter

204492 A

REVISIONS				204492 A
LTR	REV	DESCRIPTION	DATE	APPROVED
X		MFS RELEASE NOTE	1-31-74	

(30) NDVTR 18 — 19 (23) NTEST — 6C — 24 OPER/S1

(43) PHFSZ 09 — 14 OPER/S1 — 22C — S 1 — 15 OPER — (38) (53)
(44) NTOOO-1X — C
(43) PHFS-1 — 23 — R — E — 06 RESETMANL (43)

(46) CDN 30 — 18 (22) NKFULL DLYD — 31 (17) R EMPTY — 17 (14) NJFULL DLYD — 13C — 15 CSL/M(OI)/1
CSL/M(OI)/1 — 31 — 6C — 26
CSL M(OI)/T — 33
(50) TM1 27 — 29 (17) NR KO — 39 — 20
(34) NRWF 17 — 23 — 19
(50) WCHR 35 — 16C — 28
26 — CSL/M(OI)/2 (47)

(42) NDCBUSY 40 — 2B (42) NCTL — 15 — 22C — 21 READY (43) (53)
(46) NCCH X — 12 (46) UNF — 27C — 39 DCBUSY/R1
READY — 21 — (42) STOU 43 — 36 (43) PHFSL-1 — S 1 — 22C — C — R 0 — E — 42 DCBUSY (52) (45) (34)
(44) PHCLK — 47
39 DCBUSY/R1 — 46 — (43) PHTO 45 — 22 (45) ORDTY
(43) PHSRV 41 — 10 (46) FS
(38) DVSEL 23 — 22 (42) STOU — 28 — 24 — (43) PHFSL-1 36 — 37 (43) HTOME
06 RESETMANL (43)
40 NDCBUSY (36) (38) (29) (42) (45) (49) (14) (15)
22C — 29 NDCBUSY-1 (33) (36) (38) (19)

23 — 21 — 38 — NHIOME 02 — 03 — 32A — 01 NHIODCBUSY
22 DCBUSY

(45) NTN 21 — 22 (45) NDATA — 23C
(23) TEST 46 — 23C
23C — 70CSL/M1
(46) CSL/M(DATA) 37 — 41 (NUSE- NCCH) — 42 (45) DATA — 23C — 23
(46) UNE 05 — 06 GND — 07 (47) FINISH — 31A — 15 CSL/M(OI) (46)

(MAINT INC) 40 — 28 — 23C — S 1 — 23C — R 0 — 26 CSL — 29 NCSL (41)
(43) (41) — 43 (41)
(43) PHFS 39 — 27 (44) TCYCLE
(41) SERVICON 38 — 36 (45) NSCR — 23C
(43) PHFS 39 — 30 (44) NTOSO — 34 (44) TOOO — 23C
LOW PRIORITY SERVICE CALL
NDCBUSY-1 35

(56) TNT — 30C46
47 — 28C — 28 — 39 SC B
(56) NTNT-3 — 46 — I 30C — 39 — LD 30C — P2-13 — /SC/
SC R — 40 — LR 30C

(45) SCR 45 — 46 (50) READ — 50 — 17C — 39
(33) POST 21 — 20 (50) READ — 29 — 13C — 14
(22) KFULL/DLYD (SCAT11+SCR) 34
GND 43 — 44 — X 37 — 7B — 01 — 6C — 38
(45) SCR 45 — X 36
(45) DATAOUT — 35
(34) NTSF 45 — 46 (34) RWD — 8A — 50 NTSERWP — 36 — 6C — 39
(50) SENSE — 37
(23) TEST 41 — 6C — 40
(50) SEEK 05 — 07 (35) NSRY2OSRY3 — 3B — 08
(50) TESTORD 04 — 06 — 3B — 12
SCAT 11 NBP
GND 23
(17) NR:K1 15 — X 18
(17) NR:K2 17 — X 22
7B — 14 — SCAT 11 — 44 (5) NBP 43 — 45 — 9B — 33
(14) NJFULYDLYD

NCSL/M(DATA) — 40 — 4A — 46 CSL/M(DATA)

(41) NMAINT 44 — 37 (56) NTNC — 4C — 36 (MAINT INC)

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

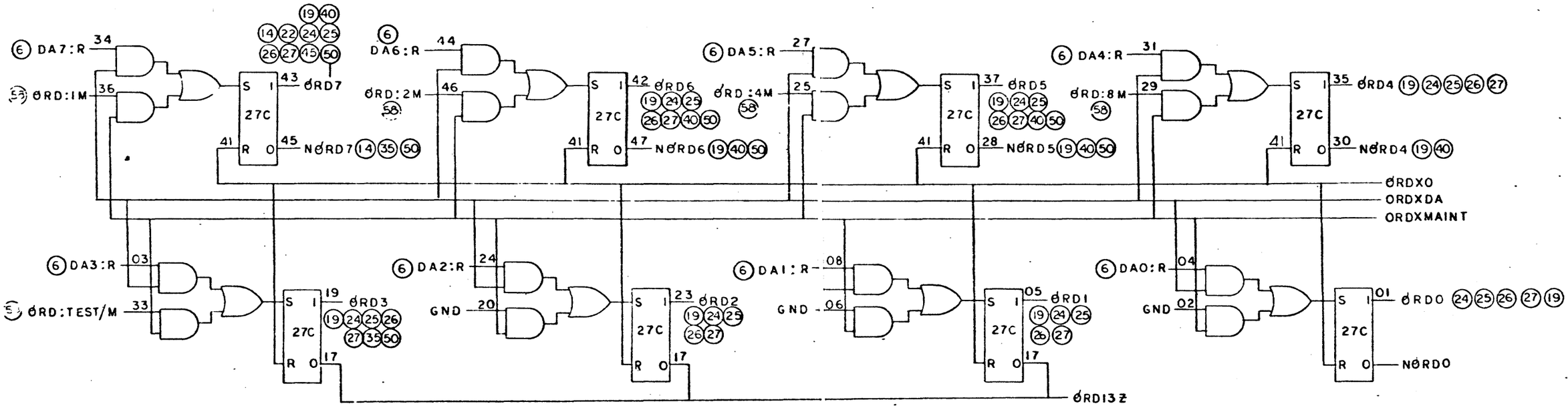
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A
SCALE —	DO NOT SCALE DRAWING	SHEET 48 OF 61	

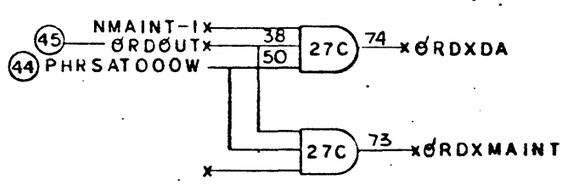
204492 A

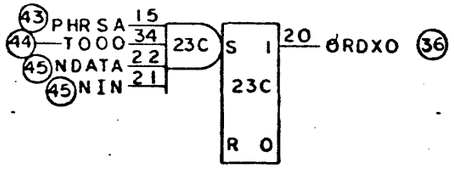
B A

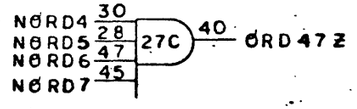
L Hunter

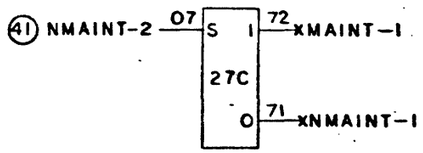
REVISIONS				204492	A
LAL	REV.	DESCRIPTION	CHK.	DATE	APPROVED
X	A	MFG RELEASE NO E.O		1-27-71	

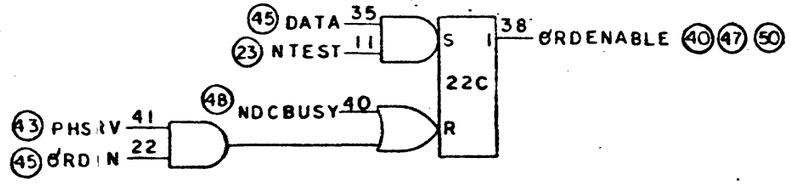












ØRDER REGISTER

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

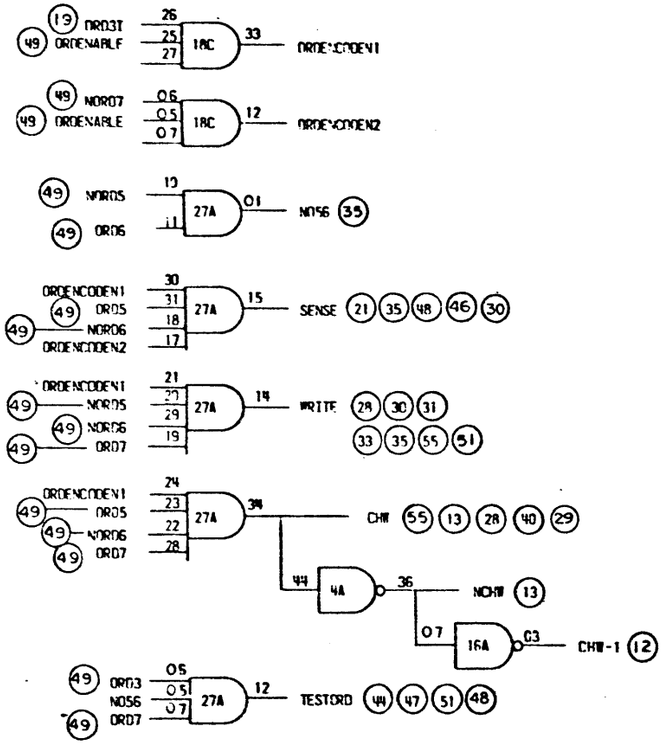
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

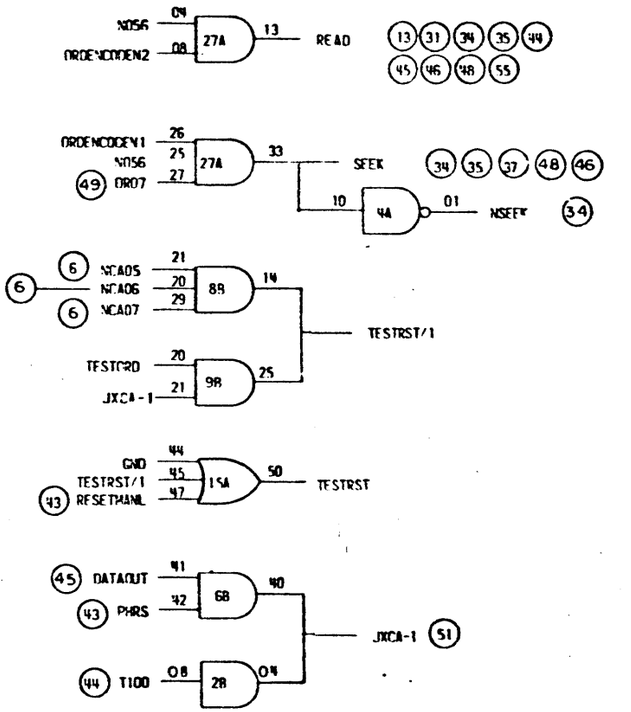
SCALE — DO NOT SCALE DRAWING SHEET 49 OF 61

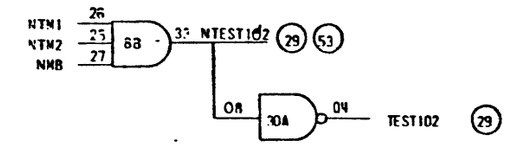
204492 A

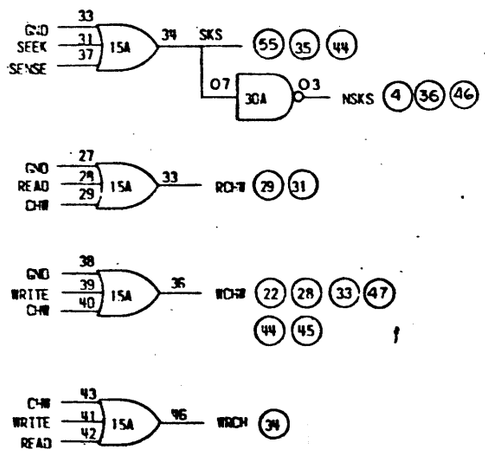
L. Hunt

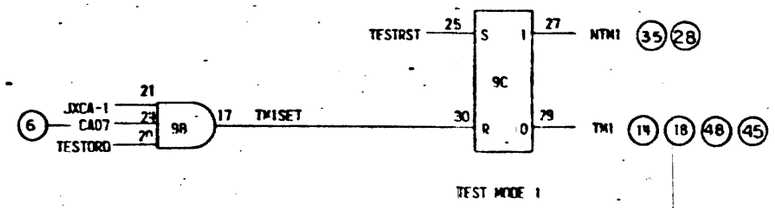
REVISIONS					20 : : 2	A
LAL	REV.	DESCRIPTION	CHG.	DATE	APPROVED	
X	A	MFG RELEASE NO E.O.				



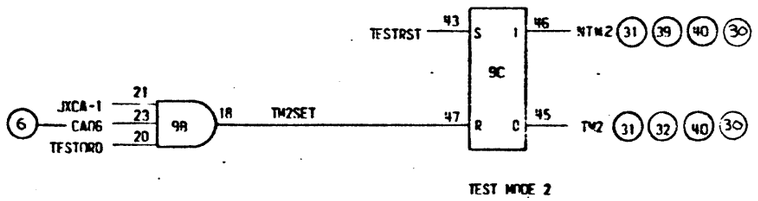




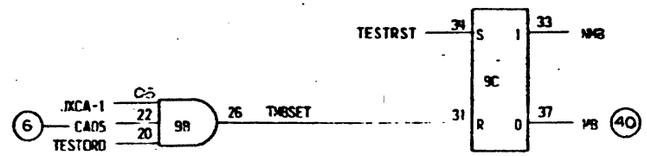




TEST MODE 1



TEST MODE 2



TEST MODE MODIFIER BIT

ORDER DECODE

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	REV. LETTER
18338	D	204492	A

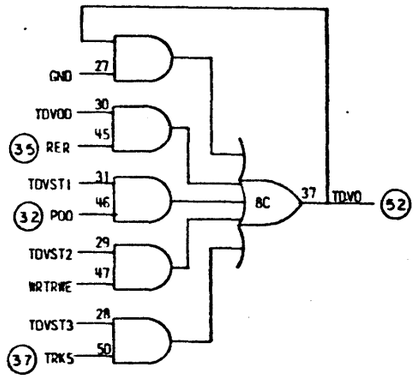
SCALE — DO NOT SCALE DRAWING SHEET 500F61

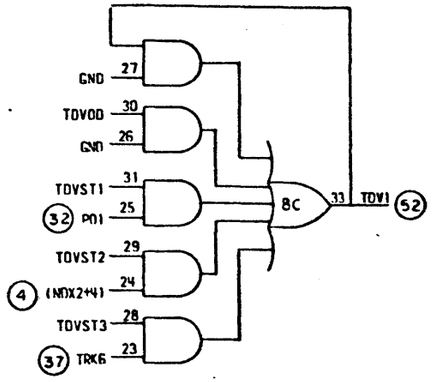
204492 A1 A

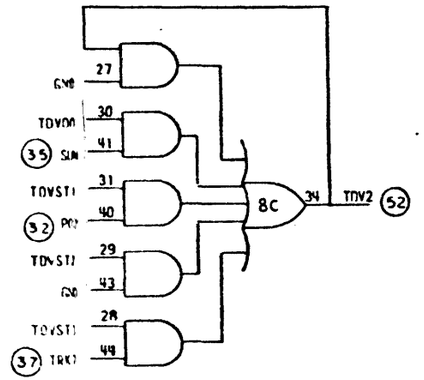
B

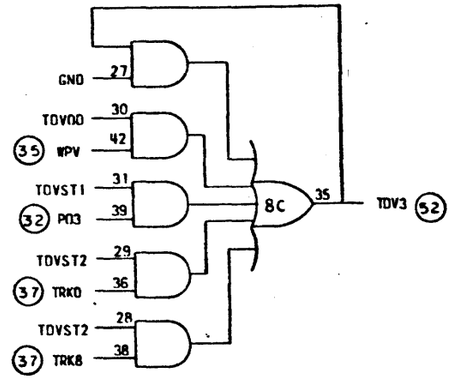
L. Hunter

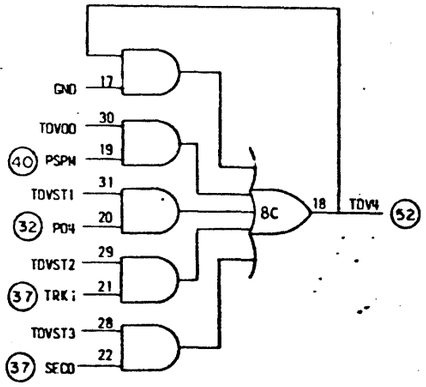
REVISIONS				204492	A
LTR	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.C.			

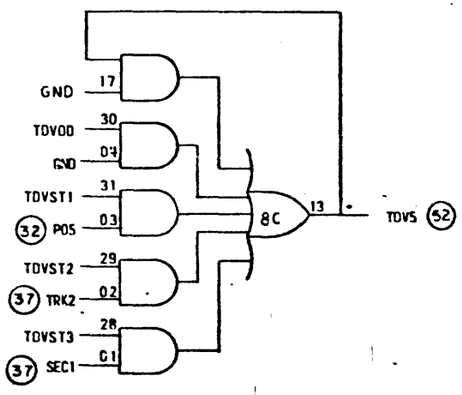


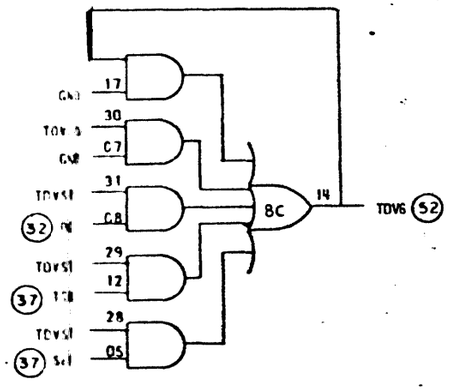


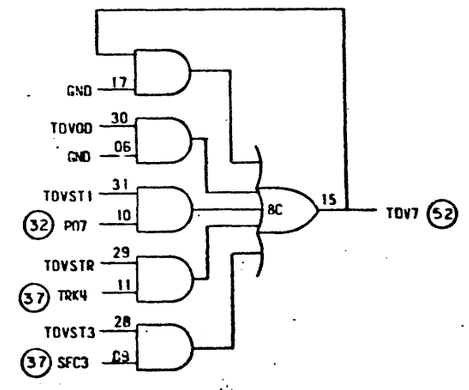


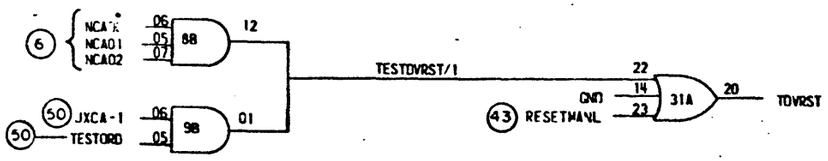


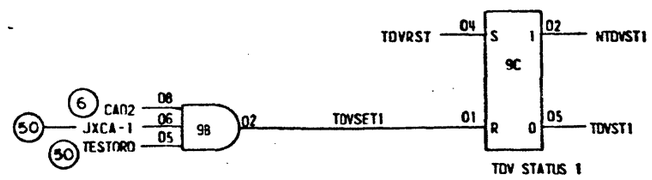


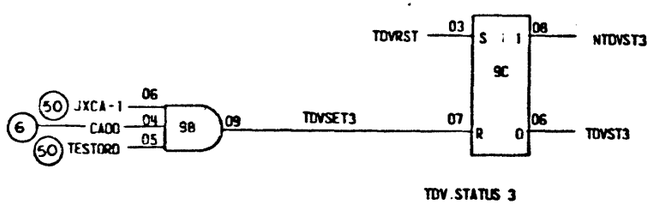


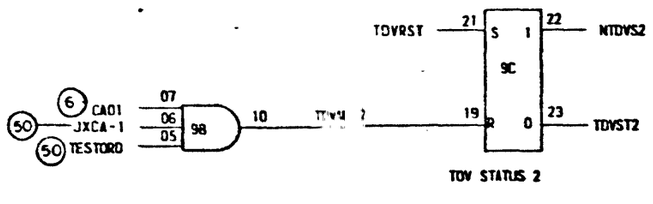


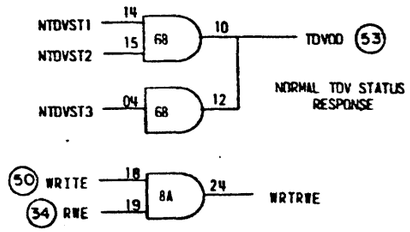












DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 5 OF 61

L. Hunter

REVISIONS				204492 A
LTR	REV	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O			

(41) ASCB 36
(42) AI0C 17
29C 24 FRX (ADDRESS)

(42) TSH
(43) PHFSL
28C 23 FRX (TSH) (53)
24
(42) TDV:R 22
28C 20 FRX (TDV) (53)

FRX (TSH) 09
FRX (TDV) 34
FRX (ADDRESS) 11
32C11
32C34
32C09
32C37 INI (56)

(42) CIL 44
(51) TDVO 40
(54) SWAO 42
(38) DVBSY 38
(51) TDVI 46
(54) SWAI 36
(53) N(OPER+BSY) 33
(51) TDV2 25
(54) SWA2 35
(30) DVTR 23
(51) TDV3 31
(54) SWA3 27
32C
91 FR0:D LD 32C P2-8 />/FR0/
90 FR1:D LD 32C P2-7 />/FR1/
89 FR2:D LD 32C P2-6 />/FR2/
88 FR3:D LD 32C P2-5 />/FR3/

(46) UNE 21
(51) TDV4 15
GND 20
(48) DCBUSY 14
(51) TDV5 22
(38) U0 13
(48) DCBUSY 02
(51) TDV6 08
(73) U1 3
GND 10
(51) TDV7 01
(38) U2 12
32C
87 FR4:D LD 32C P2-4 />/FR4/
86 FR5:D LD 32C P2-3 />/FR5/
85 FR6:D LD 32C P2-2 />/FR6/
84 FR7:D LD 32C P2-1 />/FR7/
32C04 INI (56)

FUNCTION RESPONSE LINES

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

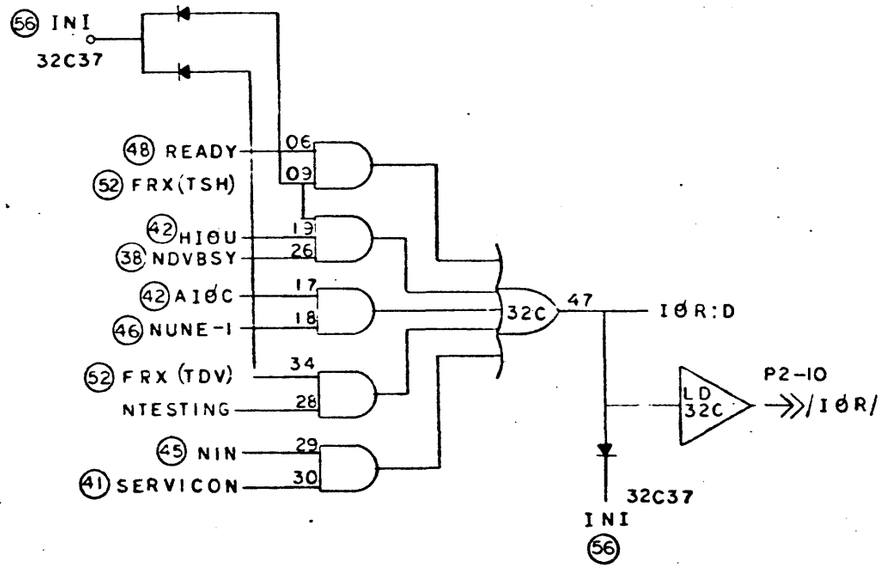
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

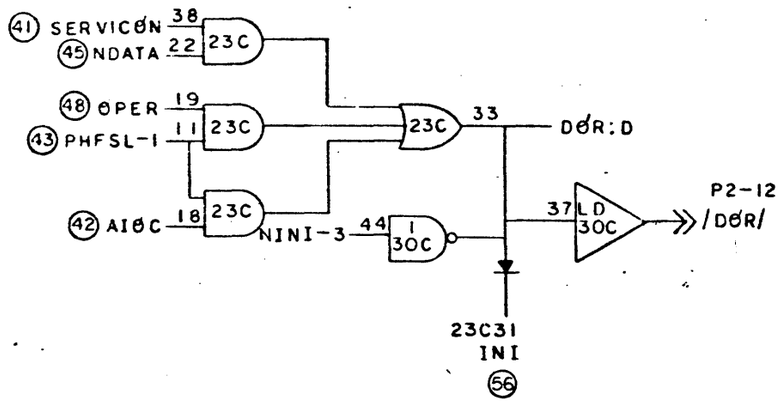
CODE IDENT.	SIZE	DWG. NO	CHANGE LETTER
18338	D	204492	A

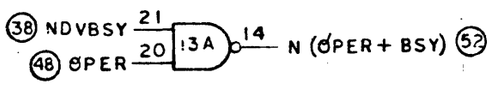
SCALE — DO NOT SCALE DRAWING SHEET 520F61

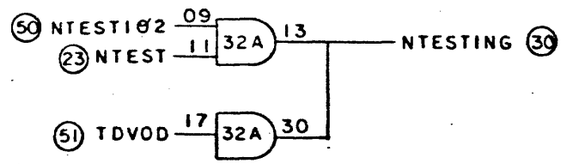
L Hunter

REVISIONS				204492 A
LAL	REV.	DESCRIPTION	CHK	DATE / APPROVED
X	A	MFG RELEASE NO E.O.		









204492 A

A

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG.	CHANGE LETTER
18338	D	204492	A

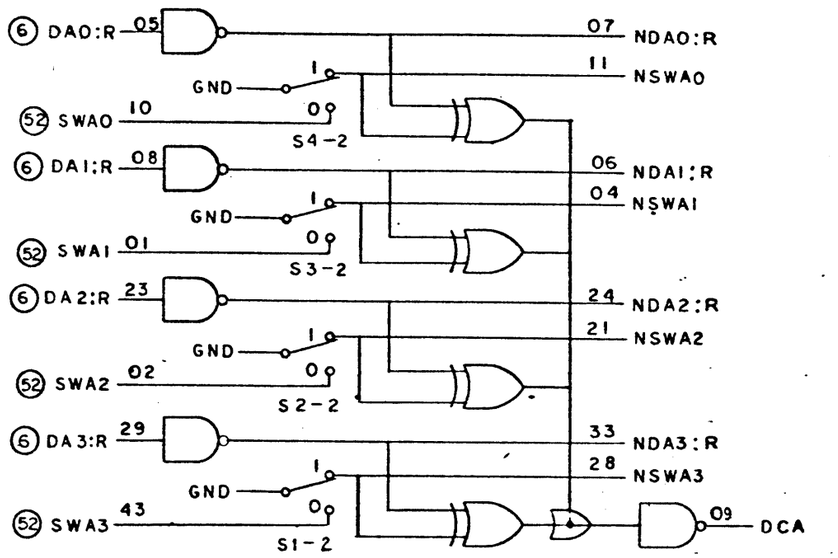
SCALE —— DO NOT SCALE DRAWING SHEET 530F 61

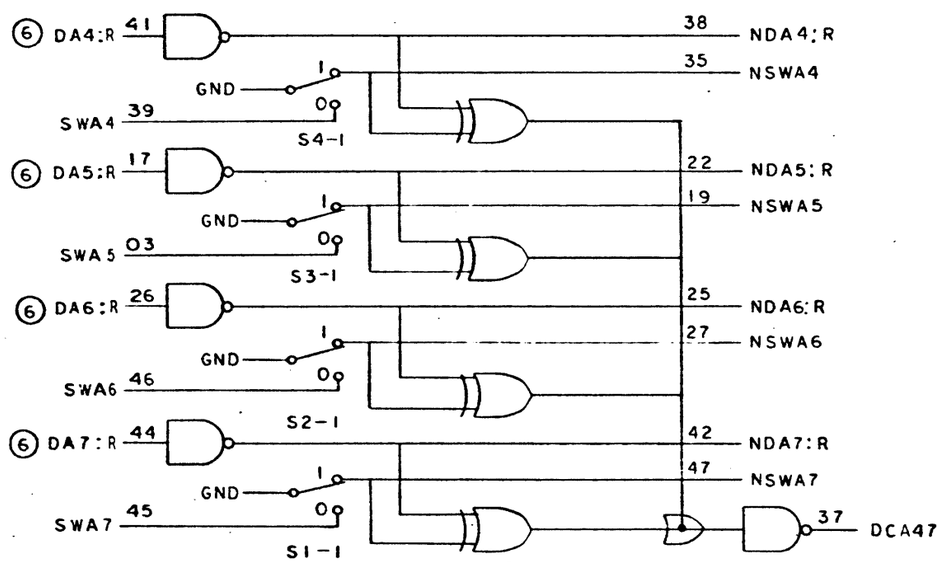
L. Hunter

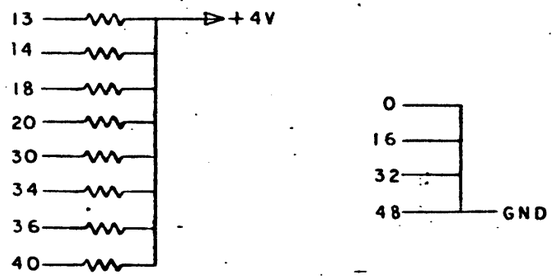
REVISIONS				204492 A
LTR	REV	DESCRIPTION		APPROVED
X	A	MFG RELEASE		

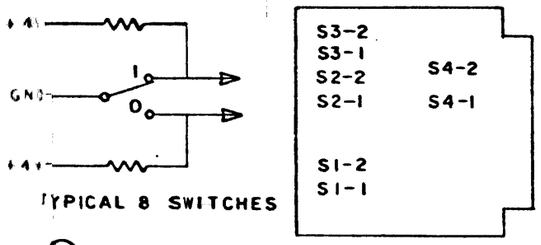
NOTE: SWITCHES SHOWN IN ON POSITION
BAT HANDLES UP

MODULE LOCATION 24C





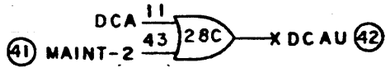


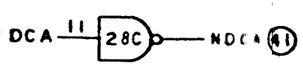


TYPICAL 8 SWITCHES

+4V ← 49

+8V ← 51





DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	REV LETTER
18338	D	204492	A

SCALE — | DO NOT SCALE DRAWING | SHEET 540F61

204492 A

L Hunton

REVISIONS				204492	A
LAL	REV.	DESCRIPTION	CHK	DATE	APPD
X	A	MFG RELEASE NO E.O			

GND
O2C32

IND1
GND 23
(43) PHFS 25
(58) INDUP 18
(37) TRK8 24
(58) INDN 22
3C
26 44
QT14
06 2C
D
R 14
46
INDI:D (58)

IND2
(43) PHFSZ 28
(37) TRK7 29
3C
27 43
06 2C
D
P 13
47
IND2:D (58)

IND3
(43) PHFSL 11
(37) TRK6 10
3C
12 39
06 2C
D
N 12
31
IND3:D (58)

IND4
(43) PHRS 15
(37) TRK5 17
3C
14 38
06 2C
D
M 11
36
IND4:D (58)

IND5
GND 30
(43) PHRSA 20
(58) INDUP 13
(37) TRK4 19
(58) INDN 05
3C
2C
D
L 10
29
IND5:D (58)

IND6
(43) PHTØ 47
(37) TRK3 50
3C
2C
D
K 9
28
IND6:D (58)

IND7
(50) READ 08
(37) TRK2 06
3C
2C
D
H 8
19
IND7:D (58)

IND8
(50) WRITE 04
(37) TRK1 03
3C
2C
D
G 7
18
IND8:D (58)

IND9
GND 43
(50) CHW 31
(58) INDUP 37
(37) TRKO 33
(58) INDN 38
3C
02 12
06 2C
D
B 2
14
IND9:D (58)

INDIO
(50) SKS 45
(50) DVØR 44
3C
01 10
06 2C
D
D 4
17
INDIO:D (58)

IND11
GND 36
(40) PER 35
(46) UNE 34
3C
39 05
06 2C
D
E 5
3
INDII:D (58)

IND12
(40) FSPM 41
TPIL 40
3C
42 04
06 2C
D
A 1
2
INDI2:D (58)

TPI 09
LATCH 11
6B
13 TPILSET
44
S 1
9C
R 40
41 TPIL
NLATCH

IND RET.
30 INDR
3
C

TEST
POINT
LATCH
S23
MAINT PANEL
TPI
NLATCH (58)
LATCH (58)
GND

DIST CODE 409
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA
TITLE
DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A
SCALE —	DO NOT SCALE DRAWING	SHEET 5 OF 61	

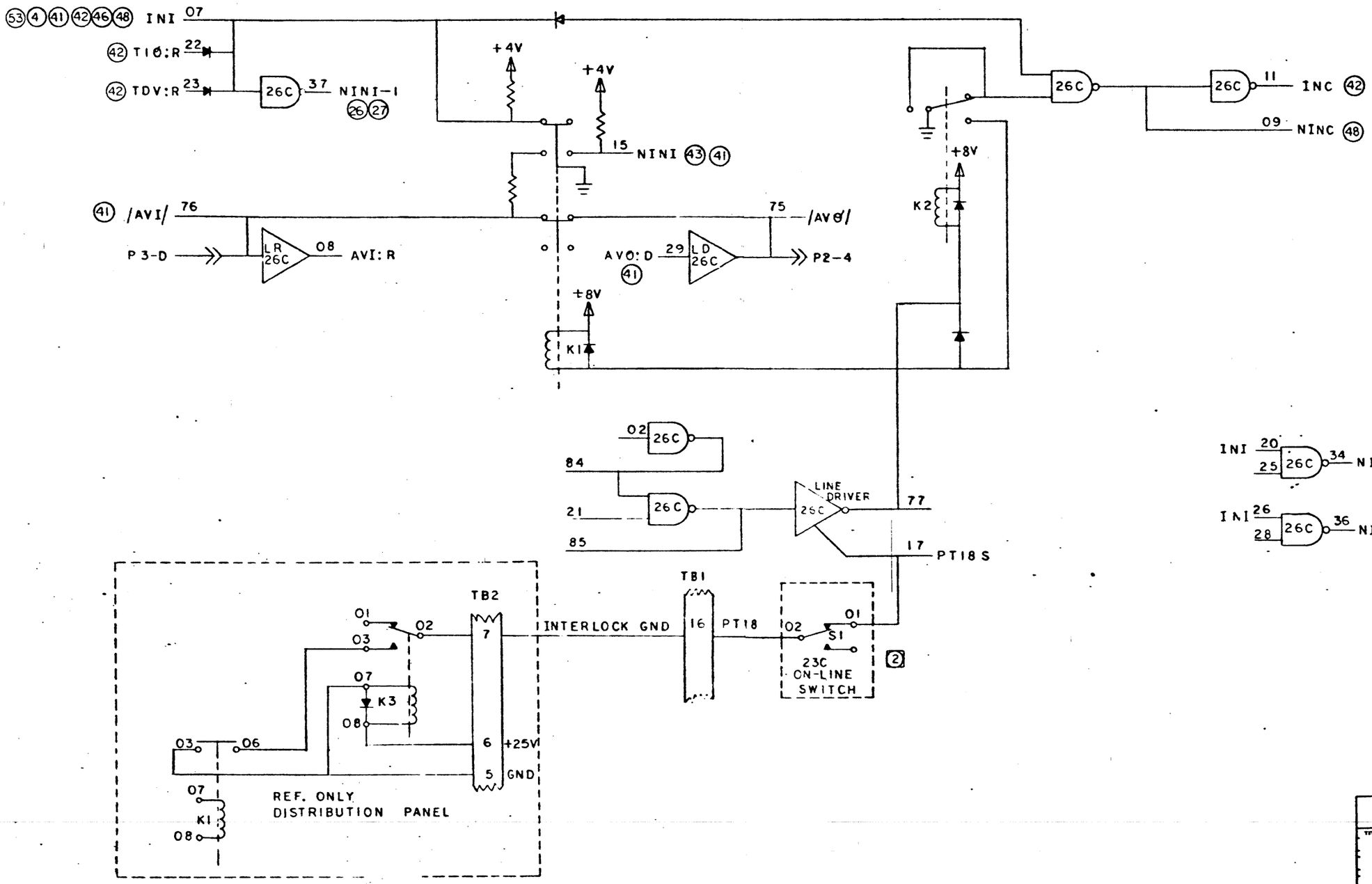
204492 A

L. Hunter

REVISIONS				204492 A
LTR	REV	DESCRIPTION		
X	A	MFG RELEASE NO E O		

NOTES: UNLESS OTHERWISE SPECIFIED

1. RELAYS ARE SHOWN IN THE OFF-LINE POSITION.
2. SWITCH IS SHOWN IN THE ON-LINE (1) POSITION.



DIST CODE 409

XDS Xerox Data Systems EL SEGUNDO, CALIFORNIA

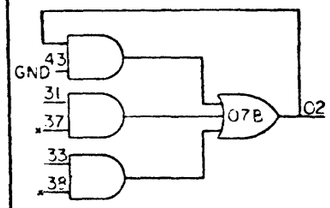
TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

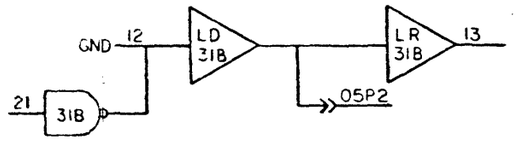
CODE IDENT.	SIZE	DWG. NO	CONTROL LETTER
18338	D	204492	A

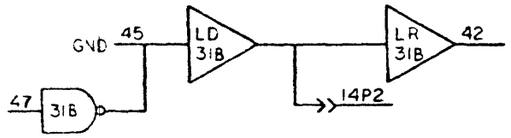
SCALE — DO NOT SCALE DRAWING SHEET 56 OF 61

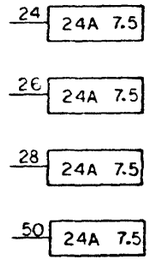
204492 A

REVISIONS				204492 A
LAL	REV	DESCRIPTION	DATE	APPROVED
X	A	MFG RELEASE NO E.O.		

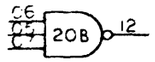




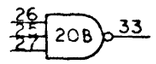




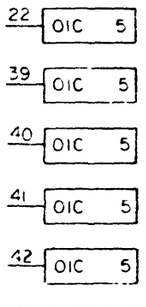
4 BYTE INTERFACE

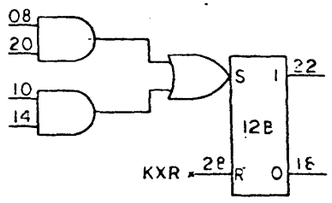


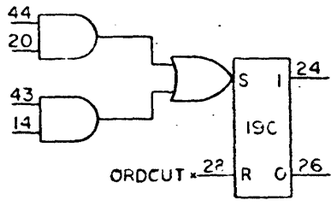
2 BYTE INTERFACE

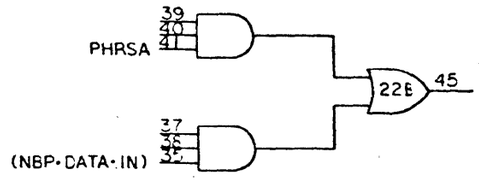


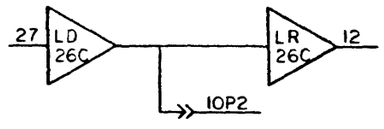
TERMINATORS

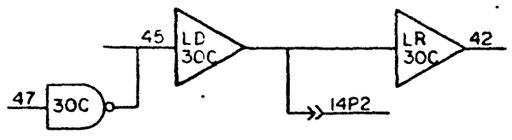












204492A

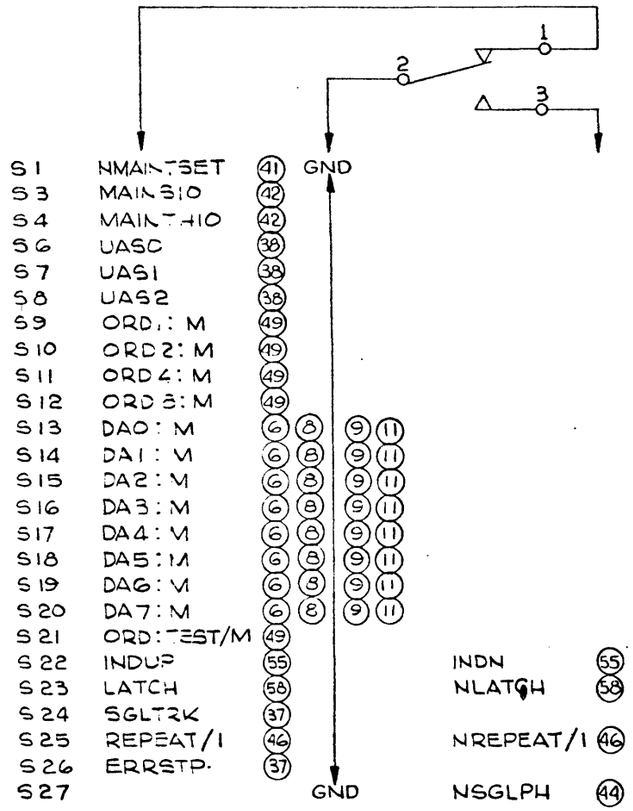
DIST CODE 409

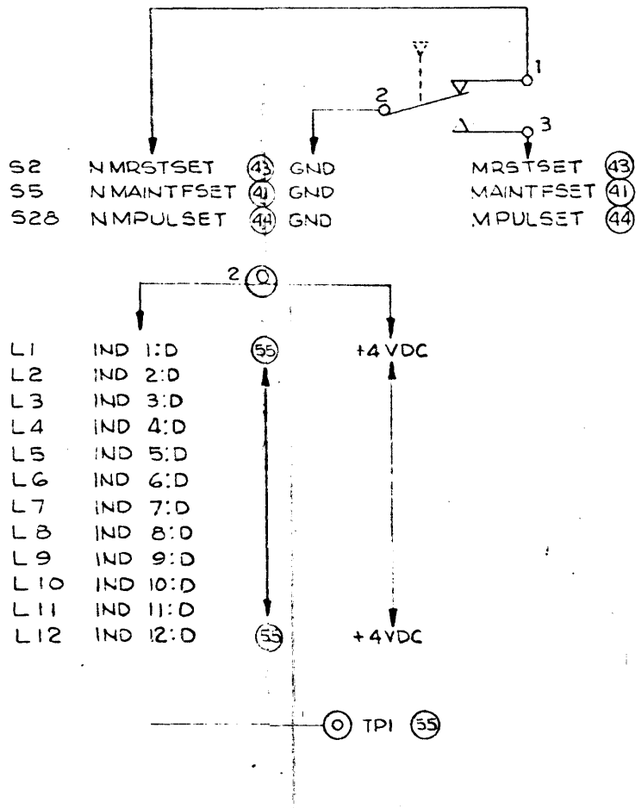
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LTR
18338	D	204492	A
SCALE —	DO NOT SCALE DRAWING	SHEET 57 OF 61	

REVISIONS					204492 A
LAL	REV	DESCRIPTION	CHN	DATE	APPROVED
A	-	MFG REL: NO EC			





204492 A

DIST CODE 403

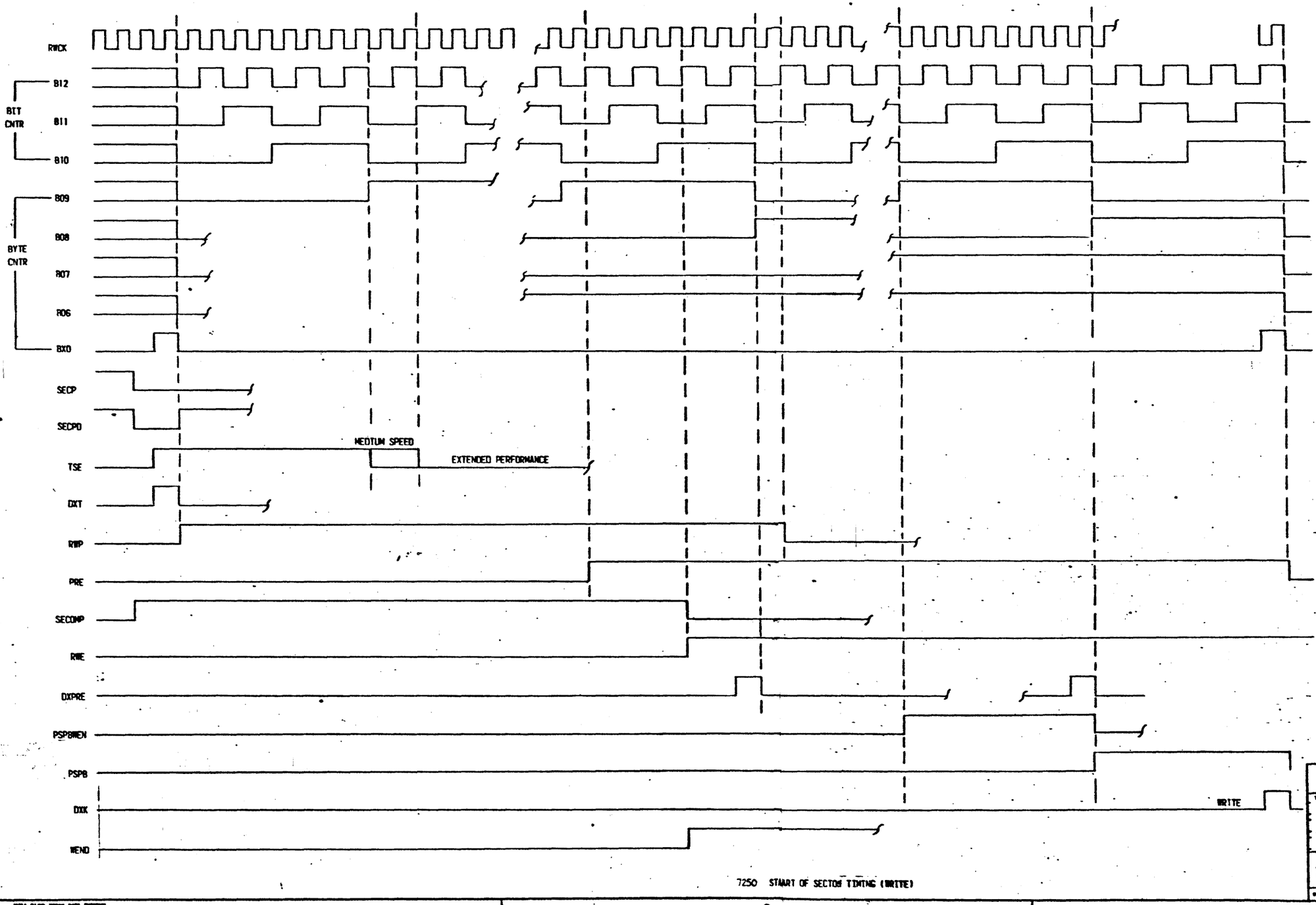
XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM LOGIC - CARTRIDGE DISK CONTROLLER -

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 58 OF 61

REVISIONS					204492 A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE NO E.O.	Sm	1-11-71	



7250 START OF SECTOR TIMING (WRITE)

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

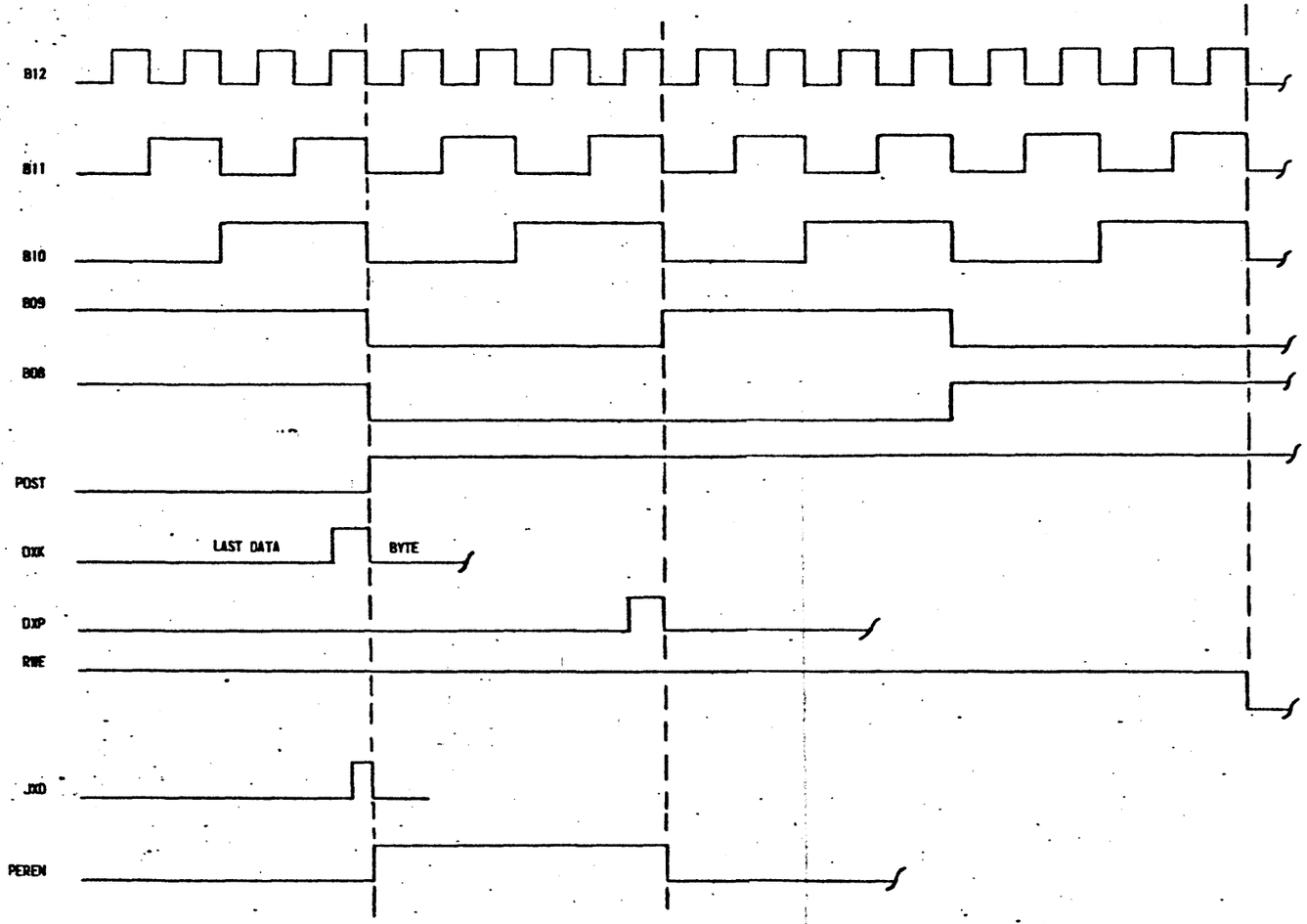
CODE IDENT.	SIZE	DWG. NO.	REVISION LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 59 OF 61

204492 A

L. Hunter

REVISIONS					204492	A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED	
X	A	MFG RELEASE - NO E.O.				



7250 END OF SECTOR

DIST CODE 409

XDS Xerox Data Systems
EL SEGUNDO, CALIFORNIA

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	DRAWING LETTER
18338	D	204492	A

SCALE — DO NOT SCALE DRAWING SHEET 60 OF 61

204492 A

L. Hunter

REVISIONS					204492	A
LTR.	REV.	DESCRIPTION	CHK	DATE	APPROVED	
		SEE SH 1				

SIGNAL GLOSSARY

DIST CODE 409

XEROX

TITLE: DIAGRAM, LOGIC — CARTRIDGE DISK CONTROLLER

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204492	A

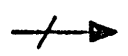
SCALE —— DO NOT SCALE DRAWING SHEET 61 OF 61

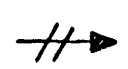
NOTES: SYMBOLOGY IS AS FOLLOWS

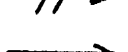
$\vee$ = OR FUNCTION

$\wedge$ = AND "

 = DC SET

 = CLOCKED ON TRAILING EDGE OF CLOCK

 = " " LEADING " " "

 = THEN

(THIS DOCUMENT CONTAINS 11 PAGES

X	A	MFG REL - NO E.O.	MK	12-70	[illegible]
LAL	REV.	DESCRIPTION	CHK	DATE	APP

REVISIONS 456

DIST CODE

MATERIAL LIST

NOTES UNLESS SPECIFIED

1 TOLERANCES
.XX ± .005 DIMENSIONED ANGLES ± 1/2°
.XXX ± .010
2 BREAK ALL SHARP EDGES .010 APPROX
3 MACH SURFACES 7
4 ALL DIM IN INCHES
5 ALL TRUE POSITION TOLERANCES APPLY AT MMC

MODEL NO 7231
FIRST USE
NEXT ASSY
FIRST USE

DRAWN I.L. 12-1
CHECK [illegible] 12-3
APPR [illegible] 12-3
MATERIAL

FINISH

XDS Xerox Data Systems

TITLE
CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

S A F DO NOT SCALE DRAWING SHEET 1

PHASE SEQUENCE CHART

OPERATION: SIO, TIO, TDV, HIO

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
		SIO ∨ HIO ∨ TIO ∨ TDV = TTSH 28C26 (TTSH ∧ FSU ∧ DCAU) ∨ AIOC = TTSHAIOC 28C29	
PHFS	START DELAY LINE	TTSHAIOC	
TOOO 31C26	⫽→ SLND 13A12	SIO ∧ NCIL ∧ NDCBUSY	Select pulse to Storage Unit
	0 ⫽→ OPER 22C15		
	0 → CSL 23C26	NCSL/M1 ∨ NDCBUSY	
PHCLK	0 /→ PHFS	TTSHAIOC	
	1 /→ PHFSZ	TTSHAIOC ∧ PHFS	
PHFSZ	START DELAY LINE	PHFSZ	
TOOO	1 ⫽→ OPER 22C15	DVTR	Device tested is operational (from storage unit)
PHCLK	0 /→ PHFSZ		
	1 /→ PHFSL		
PHFSL	Status → FRO-7	TSH ∨ TDV	
	1 → IOR 32C47	TSH ∧ READY ∧ TDV ∧ NTESTING	$\overline{CC2}$
	1 → DOR :D 30C37	OPER	$\overline{CC1}$
	send FSL:D	PHFSL	
	DA5:R ∨ UAS0 → SU0D DA6:R ∨ UAS1 → SU1D DA7:R ∨ UAS2 → SU2D	IOP ∨ MAINT	Storage unit address
	DA4:R → ILLADD		
	START DELAY LINE	NFSU	
TOOO	SU0D /→ U0 SU1D /→ U1 SU2D /→ U2	OPER ∧ NAIOC ∧ NDCBUSY ∧ NHIO	Storage unit address is stored
	1 ⫽→ CLEAR	HIOU ∨ SIOU ∧ READY	
	0 → BPB BPC BPD WIDEINTR/1 WIDEINTR/2 BUFFER/EN TSE PRE RWE RWP SUN RER INL WPV PTE PER PSPM CER CIL SCR UNE	CLEAR	
	1 → R:TSTART 14C41	CLEAR 22C39	

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

SCALE | DO NOT SCALE DRAWING | SHEET 2

PHASE SEQUENCE CHART

OPERATION: SIO, TIO, TDV, HIO

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
PHCLK	0 → / → PHFSL		
	1 → / → PHFS		
	1 → / → DCBUSY 22C42	28C08 22C21 SIOU ∧ READY	
	0 → / → DCBUSY	HIOM	
	0 → FIRSTPHRS	NDCBUSY	
	R:WRITE		
	R:READ		
	ORDENABLE		
	BCE		
	DAR		
	PARCNTR		
	PAR(IOP)		
	DSE		
	DATA		
	0 IN		
	1 → R:TCYCLE 15B50		

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

SCALE | DO NOT SCALE DRAWING | SHEET 3

PHASE SEQUENCE CHART

OPERATION: ORDEROUT

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
ORDOUT	22 C 24		
PHFS	0 → RS:D 32 C07		
	SERVICON		
	HIOU		
	SIOU		
	ED		
	ES		
	PHRSATOOOW		
	DX2		
	0 → DX4		
	CSL/M1	NDATA ∧ NIN	
	1 → FSU 28C34	FS:R	
	1 → ASCB 28C37	ASC:R ∧ ASCM ∧ FSU	
	START DELAY LINE	ASCB	
PHCLK 31C02	0 ⇢ PHFS	ASCB ∧ CSL	
	1 ⇢ PHSRV 29C01	ASCB ∧ CSL	
PHSRV	send FSL:D		delay line is not started in PHSRV
	1 → SERVICON	NFSU	
	1 → PHRS	TCYCLE ∧ NPHRSA ∧ SERVICON	
PHRS	TSTART (PHRS)	NDATA	
T000	1 → RS:D	NES	
T150	1 → PHRSA	NED	
T200	0 → PHRS		
PHRSA	START DELAY LINE	RSAU	
	0 → RS:D	RSAU	
T000	1 → ORDXO		clear order register
	1 PHRSATOOOW		
	1 TSTOP	PHRSATOOOW ∧ NIN	
	1 ORDXDA	PHRSATOOOW	
	0 FIRSTPHRS	PHRSATOOOW	
	1 → R:K(LOAD)CLK	PHRSATOOOW	
	ORDXPAR	PHRSATOOOW	check parity on order
	1 → ED	PHRSATOOOW ∧ EDI	
	1 → ES	PHRSATOOOW ∧ ES:R	
T100	0 → PHRSA		
	1 → PHRS	NPHRSA	

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

SCALE | DO NOT SCALE DRAWING | SHEET 4

PHASE SEQUENCE CHART

OPERATION: ORDER OUT

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
PHCLK	→ PARCNTR	ORDPAR ∧ PCL	Clock Parity Counter
	1 → DATA	ES ∧ (UNE . NCDN)	
	1 → IN	ES ∧ NORD7	
	0 → IN 22C20	ES ∧ ORD7	
	1 → ED	ES	
	1 → PHFS	ES	
PHRS	TSTART(PHRS)	NDATA	
T000	1 → RS:D	NES 29C13	
T200	0 → PHRS		
PHCLK	1 → PHTO	ED 29C05	
	0 → PHSRV	ED	
PHTO	1 → ES 29C09		
	0 → RS:D	RSAU	
	START DELAY LINE	RSAU	
T000	TERMORDER	NMAINT	
	1 → CDN 27C10	TERMORDER ∧ DA1:R	Count Done
	1 → CCH	TERMORDER ∧ DA2:R	Command Chaining
	1 → UNE 27C12	TERMORDER ∧ DA3:R	IOP HALT
	1 → CIL 29C18	TERMORDER ∧ DA0:R	Interrupt
T050	1 → WIDEINTR/1	ES ∧ WIDEN ∧ NSECEND	
PHCLK	1 → PHFS	ES	
	0 → PHTO		
PHFS	0 → RS:D		
	SERVICON		
	HIOU		
	SIOU		
	ED		
	ES		
	PHRSAT000W		
	DX2		
	0 → DX4		
	CSL/M1	SEEK ∧ NSBY20SBY3 ∨	
		TESTORD ∨ SCR	
	1 → FSU	FS:R	
	1 → ASCB	ASC:R ∧ FSU ∧ ASCM	
	1 → UNE	ORDENABLE ∧ UNE/M1	
	START DELAY LINE	ASCB	
PHCLK	0 → PHFS	ASCB ∧ CSL	
	1 → PHSRV 29C01	ASCB ∧ CSL	

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	REVISED LETTER
18338	B	183293	A

SCALE | DO NOT SCALE DRAWING | SHEET 5

PHASE SEQUENCE CHART

OPERATION: DATAOUT

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
PHSRV 06808 DATAOUT	send FSL:D	ASCB	delay line is not started in PHSRV
	1 ⟶ SERVICON 23C38	NFSU	
	1 ⟶ PHRS 23C45	TCYCLE ∧ NPHRSA ∧ SERVICON	
PHRS	1 ⟶ (DX2-4) 2 09C10	FIRSTPHRS ∧ DATA ∧ WIDEINTR/1	wide interface
	TSTART (PHRS)	TESTORD ∨ SKS ∨ WCHW ∧	
		NJFULL/DLYD	
T000	1 ⟶/ WIDEINTR/2	FIRSTPHRS ∧ WIDEINTR/1	
	JX0	DATAOUT	clear J register
	1 ⟶ RS:D	NES	
T100	JXCA	DATAOUT ∧ NCHW	transfer CA to J
	JXNCA	DATA ∧ CHW	transfer false side of CA to J (Checkwrite)
	1 ⟶ JFULL 11C14	JXCA ∨ JXNCA ∧ NFIRSTPHRS	
	1 ⟶ R:SWRITE	JFULL ∧ (M/R:SWRITE) ∧ NR:K0 ∧	Start FAM write cycle
		R:TCYCLE ∧ NR:TSTART	
		FAM TIMING	
		SBY2 ∧ R:T060 = LSB1	Load seek Byte 1 into track register
		SBY3 ∧ R:T060 = LSB2	Load seek Byte 2 into track & sector register.
		R:T110 ⟹ 0 ⟶ JFULL	
	0 ⟶ SEC3 - TRK0VF	FIRSTPHRS 15344	Clear sector and track registers for seek on first time PHRS is entered.
	0 ⟶ TM1, TM2, MB, TDVST1, TDVST2, TDVST3	JXCA ∧ TESTORD	Clear test mode F.F. if test order
	CA00-07 ⟶ TM1, TM2, MB, TDVST1, TDVST2, TDVST3	JXCA-1	select test mode F.F. if test order.
T150	1 ⟶ PHRSA	NED	
PHCLK	1 ⟶/ PHTO	NES ∧ ED	terminal order required
	1 ⟶/ PHFS	ES	no terminal order required
T200	0 ⟶ PHRS		
PHRSA	0 ⟶ RS:D	RSAU	
	START DELAY LINE	RSAU	
T000	CAX0 = CBX0, CCX0, CDX0		Clear input registers
	1 ⟶ PHRSAT000W		

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

SCALE | DO NOT SCALE DRAWING | SHEET 6

PHASE SEQUENCE CHART

OPERATION: DATAOUT

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
PHRSA	PHRSATOOOW CONTINUED		
	1 ⟶ TSTO? N 21C23	PHRSATOOOW ∧ (NES ∧ NIN)	
	1 ⟶ ES 2 9C09	PHRSATOOOW ∧ ES:R	
	CAX(IOP)	PHRSATOOOW ∧ NMAINT	transfer data lines into CA reg
	CAX(MAINT)	PHRSATOOOW ∧ MAINT	transfer data switch settings into CA (Maintenance Panel)
	0 ⟶ FIRSTPHRS	PHRSATOOOW	
T100	0 ⟶ PHRSA		
	1 ⟶ PHRS	NPHRSA	repeat PHRS
PHTO	1 ⟶ ES		
	1 ⟶ ED 2 9C65	ES	
	0 ⟶ RS:D	RSAU	RS:D was raised in PHRS
	START DELAY LINE	RSAU	
	1 ⟶ SUN	SBY2OSBY3 ∧ SUNSET	set sector unavailable if conditions exist
	TERMORDER	NMAINT	terminal order sets flags as in Order Out PHTO sequence.
T050	1 ⟶/ WIDEINTR/1	ES ∧ WIDEN ∧ NSECEND	set up wide interface operations
PHCLK	1 ⟶/ PHFS	ES	
	0 PHTO		
	0 DATA 22 C35	UNE V CDN ∧ ES	
	1 ⟶/ IN 22C20	UNE V CDN ∧ ES	

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

SCALE | DO NOT SCALE DRAWING | SHEET 7

PHASE SEQUENCE CHART

OPERATION: DATAIN

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
DATAIN 06801 PHFS	0 ⟶ RS:D		
	SERVICON		
	HIOU		
	SIOU		
	ED		
	ES		
	PHRSATOOOW		
	DX2		
	0 ⟶ DX4		
	CSL/M1	READ ∧ KFULL/DLYD ∧ CSL/DATA/M1 ∨ SENSE ∧ NTSERWP	
	1 ⟶ FSU	FS:R	
	1 ⟶ ASCB	ASC:R ∧ FSU ∧ ASCM	
	1 ⟶ UNE	ORDENABLE ∧ UNE/M1	
	START DELAY LINE	ASCB	
PHCLK	0 ⟶/ PHFS	ASCB ∧ CSL	
	1 ⟶/ PHSRV	ASCB ∧ CSL	
PHSRV	send FSL:D	ASCB	delay line is not started in PHSRV
	1 ⟶ SERVICON	NFSU	
	1 ⟶ PHRS	TCYCLE ∧ NPHRSA ∧ SERVICON	
PHRS	1 ⟶ (DX2+4)	FIRSTPHRS ∧ DATA ∧ WIDEINTR/1	
	DATAINTX	NMAINT ∧ NTEST ∧ NED	
	DAXORD	IN ∧ NTEST ∧ NED	
	TSTART (PHRS)	SKS ∨ READ ∧ (ED ∨ KFULL/DLYD)	
T000	1 ⟶/ WIDEINTR/2	FIRSTPHRS ∧ WIDEINTR/1	
	DAX(DI)	NMAINT ∧ NED ∧ NTEST	data transfer to data lines
	DBX(DI),DCX(DI),DDX(DI)	DATAINTX	data transfer to data lines
	1 ⟶ RS:D	NES	
T100	0 ⟶ KFULL	NED ∧ N(EDX2+EDX4)	erase KFULL for 1 byte interface

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

SCALE | DO NOT SCALE DRAWING | SHEET 8

PHASE SEQUENCE CHART

OPERATION: DATAIN

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
PHRS CONTINUED			
T150	1 → PHRSA	NED	
PHCLK	1 → PHTO	ED	
	0 → PHSRV	ED	
T200	0 → PHRS		
PHRSA	START DELAY LINE	RSAU	
	0 → RS:D	RSAU	
T000	CAXO, CBXO, CCXO, CDXO		clear output registers
	1 → PHRSAT000W		
	1 TSTOP	PHRSAT000W ∧ NES	
	1 ES	PHRSAT000W ∧ ES:R	
	0 → FIRSTPHRS		
T100	E/KFULL	PHRSAT000W ∧ (EDX2+EDX4)	erase KFULL for wide interface
	0 → PHRSA		
	1 → PHRS	NPHRSA	
PHTO	1 → ES		
	1 → ED	ES	
	0 → RS:D	RSAU	
	START DELAY LINE	RSAU	
T000	TERMORDER	NMAINT	terminal order sets flags as in Order Out PHTO sequence
T050	1 → WIDEINTR/1	ES ∧ WIDEN ∧ NSECEND	
PHCLK	1 → PHFS	ES	
	0 PHTO		
	0 DATA	UNE ∨ CDN ∧ ES	
	1 → IN	UNE ∨ CDN ∧ ES	

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

SCALE | DO NOT SCALE DRAWING | SHEET 9

IN 06801
PHASE SEQUENCE CHART

OPERATION: ORDER IN

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
0221N 22022	CSL/M1	UNE ∨ FINISH	
	1 ⟶ ED:D	CSL/M(OI)	
PHFS	1 ⟶ CSL	CSL/M1 ∧ DCBUSY ∧ TCYCLE	CSL = SC:D SERVICE CALL
	FSU	FS:R	
	1 ⟶ ASCB	ASC:R ∧ ASCM ∧ FSU	
	START DELAY LINE	ASCB	
PHCLK	0 ⟶/ PHFS		
	1 ⟶/ PHSRV	ASCB ∧ PHFS ∧ CSL	
PHSRV	1 ⟶ PHRS	TCYCLE ∧ NPHRSA ∧ SERVICON	delay line is not started in PHSRV
	0 ⟶ BUFFER/EN		
	0 ⟶ ORDENABLE		
	send FSL:D	ASCB ∧ PHSRV	
PHRS	DAX(OI)	NED ∧ NTEST	
	status ⟶ $DA_{0:D-7:D}$	DAX(OI)	
	TSTART(PHRS)	NDATA	
T000	1 ⟶ RS:D	NES	SERVICE REQUEST
T150	1 ⟶ PHRSA	NED	
T200	0 ⟶ PHRS		
PHRSA	START DELAY LINE	RSAU	
	0 ⟶ RS:D	RSAU	
T000	1 ⟶ PHRSAT000W		
	1 ⟶ ED	PHRSAT000W ∧ (ED:R ∨ EDI)	End Data
	1 ⟶ ES	PHRSAT000W ∧ ES:R	End Service
T100	0 ⟶ PHRSA		
	1 ⟶ PHRS	NPHRSA ∧ NES	
PHCLK	1 ⟶/ PHFS	ES	
	0 ⟶/ PHSRV	ED	
PHRS	TSTART(PHRS)	NDATA	
T000	1 ⟶/ RS:D	NES	

NOTES:

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

18338	B	183293	A

DO NOT SCALE DRAWING SHEET 10

1825 (9/70) XEROX DATA SYSTEMS

PHASE SEQUENCE CHART

OPERATION: ORDER IN

TIME	FUNCTION PERFORMED	SIGNALS INVOLVED	COMMENTS
PHRS CONTINUED			
PHCLK	1 ⟋→ PHTO	ED	
T200	0 → PHRS		
PHTO	1 → ES		
	0 → RS:D	RSAU	
	START DELAY LINE	RSAU	
TOOO	TERMORDER	NMAINT	Terminal order sets flags as in order out PHTO sequence.
T050	1 ⟋→ WIDEINTR/1	ES ∧ WIDEN ∧ NSECEND	next operation will be on wide interface (if installed)
PHCLK	1 ⟋→ PHFS	ES	
	0 PHTO		
	0 DATA	ORDIN ∧ ES	
	0 IN	ORDIN ∧ ES	
	0 ⟋→ DCBUSY	ORDIN ∧ (UNE ∨ NCCH)	see PHFSL TOOO of SIO for action of NDCBUSY

NOTES:

LAST SHEET

XDS Xerox Data Systems

TITLE: CHART, PHASE SEQUENCE

CODE IDENT	SIZE	DWG NO	CHANGE LETTER
18338	B	183293	A

SCALE: DO NOT SCALE DRAWING SHEET 11

CHASSIS	MODULE LOCATION																													
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	BT31	BT27	IT13	BT31	AT12	BT11	AT10	FT12	LT96 (2)	LT96	LT71	FT41	FT26	IT11	BT11	LT71	IT13	BT27	BT18	IT11	IT11	FT12	FT10	BT13	BT31	FT27	FT41	FT27	IT11	LT58	LT58	CT10
B	BT11 (2) (1)	AT60 (J6) (2)	FT81 (2)	AT60 (J5) (2) (1)	FT81 (2)	FT81 (2) (1)	FT80 (2)	FT80 (2)	FT80 (2) (1)	FT26 (2) (1)	ST10 (2) (1)	FT10 (2) (1)	IT11 (2) (1)	DT14	HT15	XT10	FT75	FT66	FT79	FT25	FT81	FT26	BT18	BT15	BT11	FT27	BT31	FT10	XT10	IT31	BT13	BT11
C	AI56 (J1)	DT26	AI60 (J2)	LT89	AT57 (J3)	LT90	AT83 (J4)		LT26	LT94	LT95	FT79	LT96	FT81	BT1	IT18	BT13	FT75	AT75	IT11	BT11	FT66	BT22	FT57	FT26	FT10	IT31	FT10	IT11	FT27	QT14	XT10

NOTES:

(1) Install for 2 byte Interface.

(2) Install for 4 byte Interface.

401
423

X	A	MANUFACTURING RELEASE, NO E.O.			
LAL	REV	FMK 10742 DESCRIPTION	CHK	DATE	APP
		REVISIONS 401, 423			

DIST CODE

DRAWN	D.K.	9-10-73	XDS Xerox Data Systems EL SEGUNDO CALIFORNIA
CHECK			
APPR	S.A.M.	VI-21-73	TITLE: ASSY., MODULE KIT AND LOCATION CHART, CONTROLLER
MATERIAL			
MODEL NO / PART NO	—		
DRAWING NO / PART NO	203183		CODE IDENT 18338 · SIZE B · DWG NO 204493 · REV A
			SCALE — · DO NOT SCALE DRAWING · SHEET 1 OF 3

XEROX
Xerox Corporation
701 South Aviation Boulevard
El Segundo, California 90245

Xerox Corporation
701 South Aviation Boulevard
El Segundo, California 90245
213 679-4511

XEROX

401
423

Material List

ML	Drawing No. 204493	Rev. A

Drawing Title

ASSY., MODULE KIT AND LOCATION CHART, CONTROLLER

Model No. ———

Date 9-10-73

Sheet 2 of 3

Rev. A

Drawing No. 204493

ML

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
1				
2	Assy, P.W., Cable Receiver	123018	1	(AT10)
3	Assy, P.W., Cable Driver	124629	1	(AT12)
4	Assy, P.W., Cable Driver	148773	1	(AT56)
5	Assy, P.W., Cable Receiver	148841	1	(AT57)
6	Assy, P.W., Cable Driver/Receiver	149472	1	(AT60)
7	Assy, P.W., Priority Logic	153853	1	(AT75)
8	Assy, P.W., Cable Driver/Receiver	159313	1	(AT83)
9				
10	Assy, P.W., Band Gate	116029	6	(BT11)
11	Assy P.W., Buffered Matrix	116407	3	(BT13)
12	Assy, P.W., Gated Buffer No. 1	117389	1	(BT15)
13	Assy, P.W., Band Gate	126613	2	(BT18)
14	Assy, P.W., Fast Buffer	127393	1	(BT22)
15	Assy, P.W.,OR Gate	137867	2	(BT27)
16	Assy, P.W., Buffered And Gate	145085	4	(BT31)
17	Assy, P.W., Clock Oscillator	123491	1	(CT10)
18	Assy, P.W., Delay Line	127319	1	(DT14)
19	Assy, P.W., Timing Generator	149056	1	(DT26)
20	Crystal, Quartz (5,000.00 KHz)	128131-027	1	INSTALL IN ITEM #17
21	Assy, P.W., Basic Flip-Flop	116380	4	(FT10)
22	Assy, P.W., Gated Flip-Flop	117028	2	(FT12)
23	Assy, P.W., Fast Access Memory	126743	1	(FT25)
24	Assy, P.W., Buffered Latch No. 3	126856	3	(FT26)
25	Assy, P.W., Buffered Latch No. 2	126986	4	(FT27)
26	Assy, P.W., Register Flip-Flop	133251	2	(FT41)
27	Assy, P.W., RF Flip-Flop	145101	1	(FT57)
28	Assy, P.W. Buffered Latch	148711	2	(FT66)
29	Assy, P.W., Up-Down Counter	153576	2	(FT75)
30	Assy, P.W., Buffered Latch	156459	2	(FT79)
31	Assy, P.W., Buffered Latch	156477	2	(FT81)
32				
33	Assy, P.W., Delay Line Sensors	127391	1	(HT15)

MODULE LOCATION

CHASSIS	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A		(1)	ZT91		FT56		AT10	IT31	AT12	OT18	FT43	AT41	BT31	BT27	IT31	FT43	FT43	FT43	FT43	FT56	BT27	BT31	BT31	BT31	BT31	BT27	BT27	IT31	FT12	FT12	ST14	QT17

NOTES:

(1) ASSY,RIBBON CABLE 203810 (INCLUDES P.W BOARD ZT92).

LAL	REV	DESCRIPTION	CHK	DATE	APP
	B	ZT92, ADDED NOTE 1		6/3/73	
X	A	SEE DCR 102483; CHAS."A",LOC.31 WAS: MFG. RELEASE, NO E.O.		3-23-73	

REVISIONS

DIST CODE 423

DRAWN T.O. 3-23-73
CHECK
APPR

XDS Xerox Data Systems EL SEGUNDO CALIFORNIA

TITLE: CHART, MODULE LOCATION MULTIPLE DRIVE SELECTION UNIT

MATERIAL

FINISH

NEXT ASSY 203126

CODE IDENT 18338 | SIZE B | DWG NO 203146 | REV B

SCALE | DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				203329 A
LAL	REV.	DESCRIPTION	CHK	DATE / APPROVED
X	A	MFG RELEASE, NO E.O.		10-5-73

REVISION INDEX							
PAGE	CHG	PAGE	CHG	PAGE	CHG	PAGE	CHG
1	A	5	A				
2	A	6	A				
3	A	7	A				
4	A	8	A				

NOTES: UNLESS OTHERWISE SPECIFIED.

1. REVISION LETTERS LISTED INDICATE STATUS OF EACH SHEET OF THIS MULTIPLE SHEET DRAWING
2. CHECK INDIVIDUAL SHEETS FOR REVISION LETTER AGAINST THIS SHEET BEFORE USING THIS DRAWING.

CHASSIS	MODULE LOCATION																														
	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A		ZT92	ZT92		FT56		AT10	IT31	AT12	OT18	FT43	AT41	BT31	BT27	IT31	FT43	FT43	FT43	FT43	FT56	BT27	BT31	BT31	BT31	BT31	BT27	BT27	IT31	FT12	FT12	ST14	QT17

NOTES UNLESS SPECIFIED	DRAWN		
1. TOLERANCES .XX ±.05 DIMENSIONED ANGLES .XXX ±.010 ±1/2°	CHECK		10-5-73
2. BREAK ALL SHARP EDGES .010 APPROX.	APPR.		10-5-73
3. MATL SURFACES 63	MATERIAL		
4. ALL DIM IN INCHES			
5. ALL TRUE POSITION TOLS APPLY AT MMC			
MODEL NO. FIRST USE 7250	FINISH		
NEXT ASSY. FIRST USE 203126			

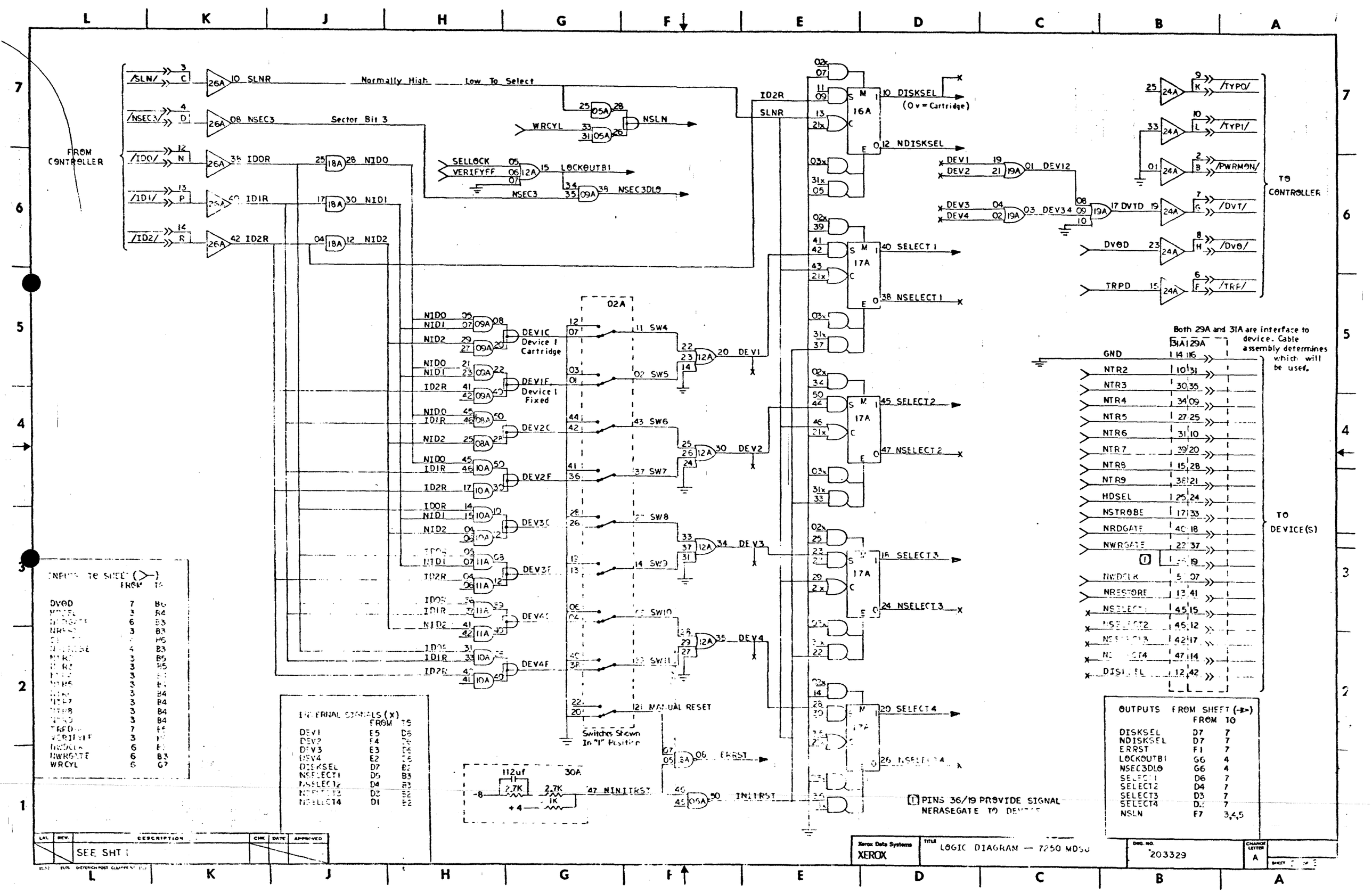
DIST CODE 109

XEROX

TITLE: DIAGRAM, LOGIC — MULTIPLE DRIVE SELECTION UNIT

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	203329	A

SCALE NONE | DO NOT SCALE DRAWING | SHEET 1 OF 8



INPUTS TO SHEET (<)

	FROM	TO
DVT0D	7	B6
NTR2	3	B4
NRDGATE	6	B3
NRESTORE	3	B3
NTR5	3	B5
NTR6	3	B5
NTR7	3	B4
NTR8	3	B4
NTR9	3	B4
TRPD	7	E5
WRITEFF	3	H5
NWDCLK	6	F3
NWRGATE	6	B3
WRCYL	6	G7

INTERNAL SIGNALS (X)

	FROM	TO
DEV1	E5	D6
DEV2	E4	D5
DEV3	E3	D4
DEV4	E2	D3
DISKSEL	D7	B2
NSELECT1	D5	B3
NSELECT2	D4	B3
NSELECT3	D3	B2
NSELECT4	D1	B2

OUTPUTS FROM SHEET (>)

	FROM	TO
DISKSEL	D7	7
NDISKSEL	D7	7
ERRST	F1	7
LOCKOUTBI	G6	4
NSEC3DL0	G6	4
SELECT1	D6	7
SELECT2	D4	7
SELECT3	D3	7
SELECT4	D2	7
NSLN	F7	3,4,5

LAST REV.	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHT 1			

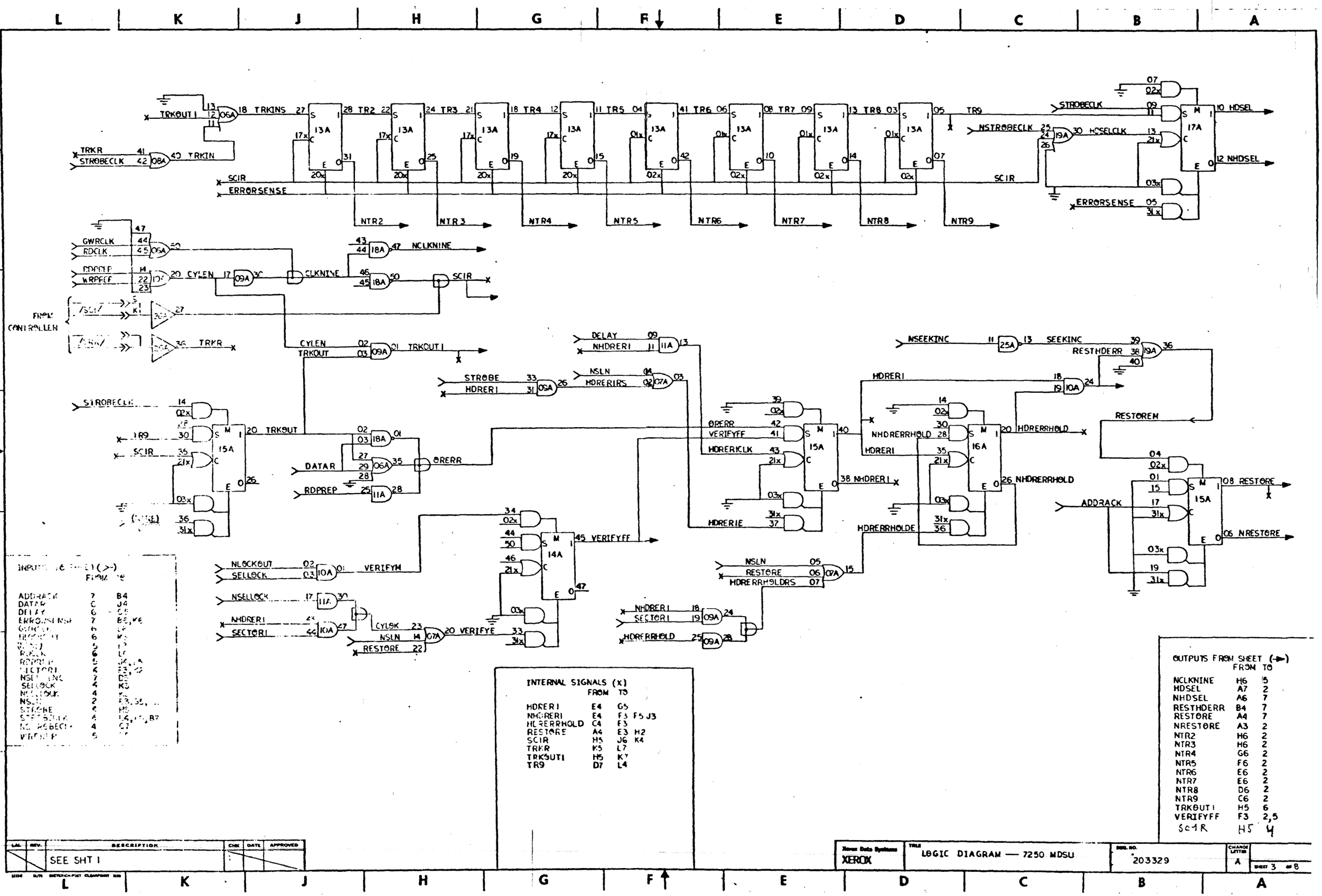
Xerox Data Systems XEROX

TITLE LOGIC DIAGRAM — 7250 MDSC

DWG. NO. 203329

CHANGE LETTER A

SHEET 2 OF 3



INPUTS FROM SHEET (<-)

	FROM	TO
ADDRACK	7	B4
DATAR	6	J4
DELAY	6	C5
ERRORSENSE	7	B5, K6
GWRCLK	6	L2
HDRERIRS	6	K3
NCLKNINE	5	L3
RDCLK	6	L5
RDPREP	5	J4, L4
SECTOR1	5	E3, J2
NSELLOCK	4	D5
SELLOCK	4	K2
NLOCKOUT	4	K3
NSLN	2	E3, J5, ...
STROBE	4	H5
STROBECLK	4	L4, L5, B7
NSTROBECLK	4	G7
WRPREP	5	L5

INTERNAL SIGNALS (X)

	FROM	TO
HDRER1	E4	G5
NHDRER1	E4	F3 F5 J3
HDRERRHOLD	C4	F3
RESTORE	A4	E3 H2
SCIR	H5	J6 K4
TRKR	K5	L7
TRKOUT1	H5	K7
TR9	D7	L4

OUTPUTS FROM SHEET (->)

	FROM	TO
NCLKNINE	H6	5
HDSEL	A7	2
NHDSEL	A6	7
RESTHDERR	B4	7
RESTORE	A4	7
NRESTORE	A3	2
NTR2	H6	2
NTR3	H6	2
NTR4	G6	2
NTR5	F6	2
NTR6	E6	2
NTR7	E6	2
NTR8	D6	2
NTR9	C6	2
TRKOUT1	H5	6
VERIFYFF	F3	2,5
SCIR	H5	4

LTR	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHT 1			

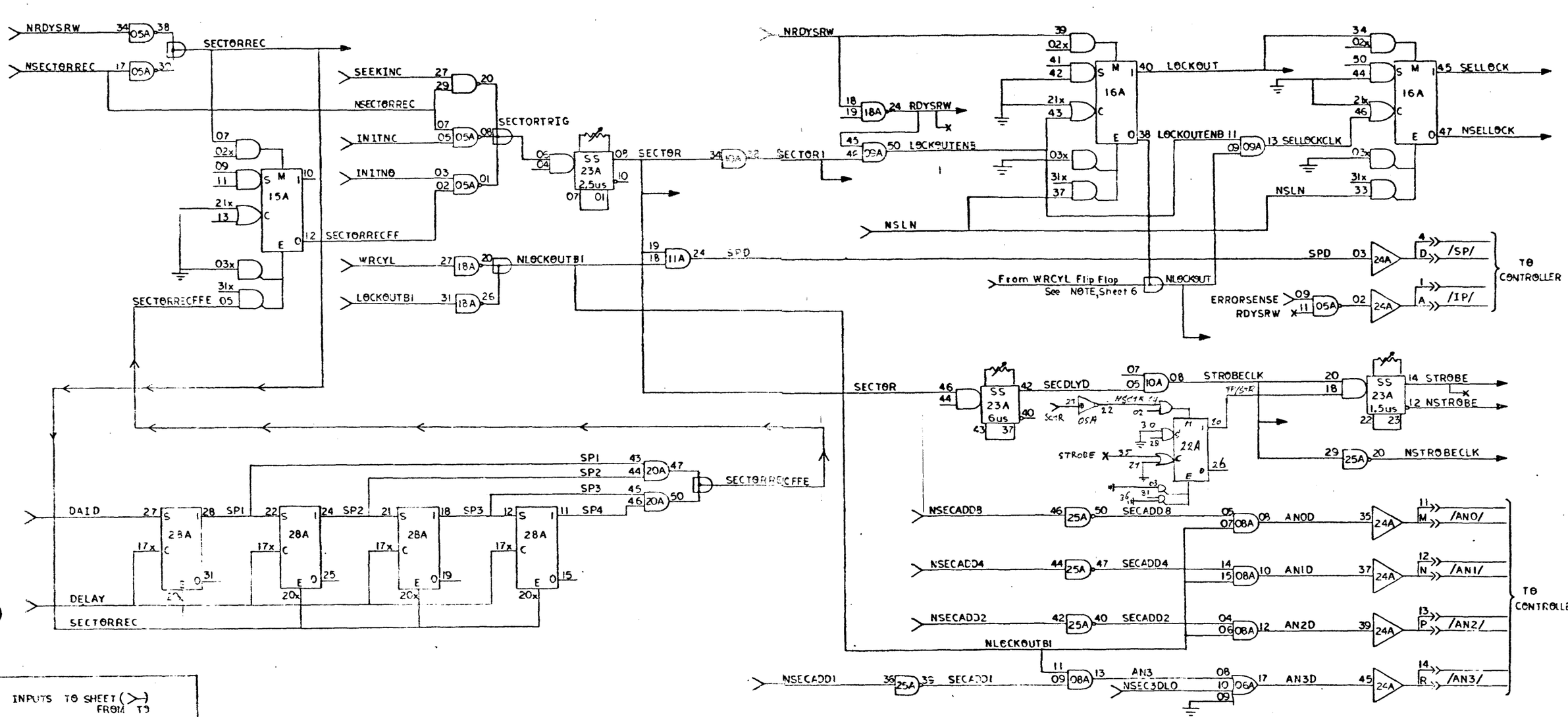
Xerox Data Systems XEROX

TITLE: LOGIC DIAGRAM — 7250 MDSU

DWG. NO. 203329

CHANGE LETTER A

SHEET 3 OF 8



INPUTS TO SHEET (→)

	FROM	TO
DAID	6	L4
DELAY	6	L3
ERRORSENSE	6	C5
INITNC	6	J6
INITNO	6	J6
LOCKOUTBI	2	J5
NRDYSRW	7	F7, L7
NSEC3DLO	2	F2
NSECADDI	7	F2
NSECADD2	7	E3
NSECADD4	7	E3
NSECADD8	7	E4
NSECTORREC	7	L7
SEEKINC	3	H7
NSLN	2	E6
WRCYL	6	J5
SCHR	4	D4

INTERNAL SIGNALS (X)

	FROM	TO
RDYSRW	E6	C5
STROBE	44	D4

OUTPUTS FROM SHEET (→)

	FROM	TO
LOCKOUT	C7	5
NLOCKOUT	C5	3
RDYSRW	E6	7
SECTOR	G6	5
SECTORI	F6	3,5
SECTORREC	J7	6
SELLOCK	A7	2,3
NSELLOCK	A6	3
STROBE	A5	3
NSTROBE	A4	2
STROBECLK	C4	3,5
NSTROBECLK	A4	3

LAC	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHT 1			

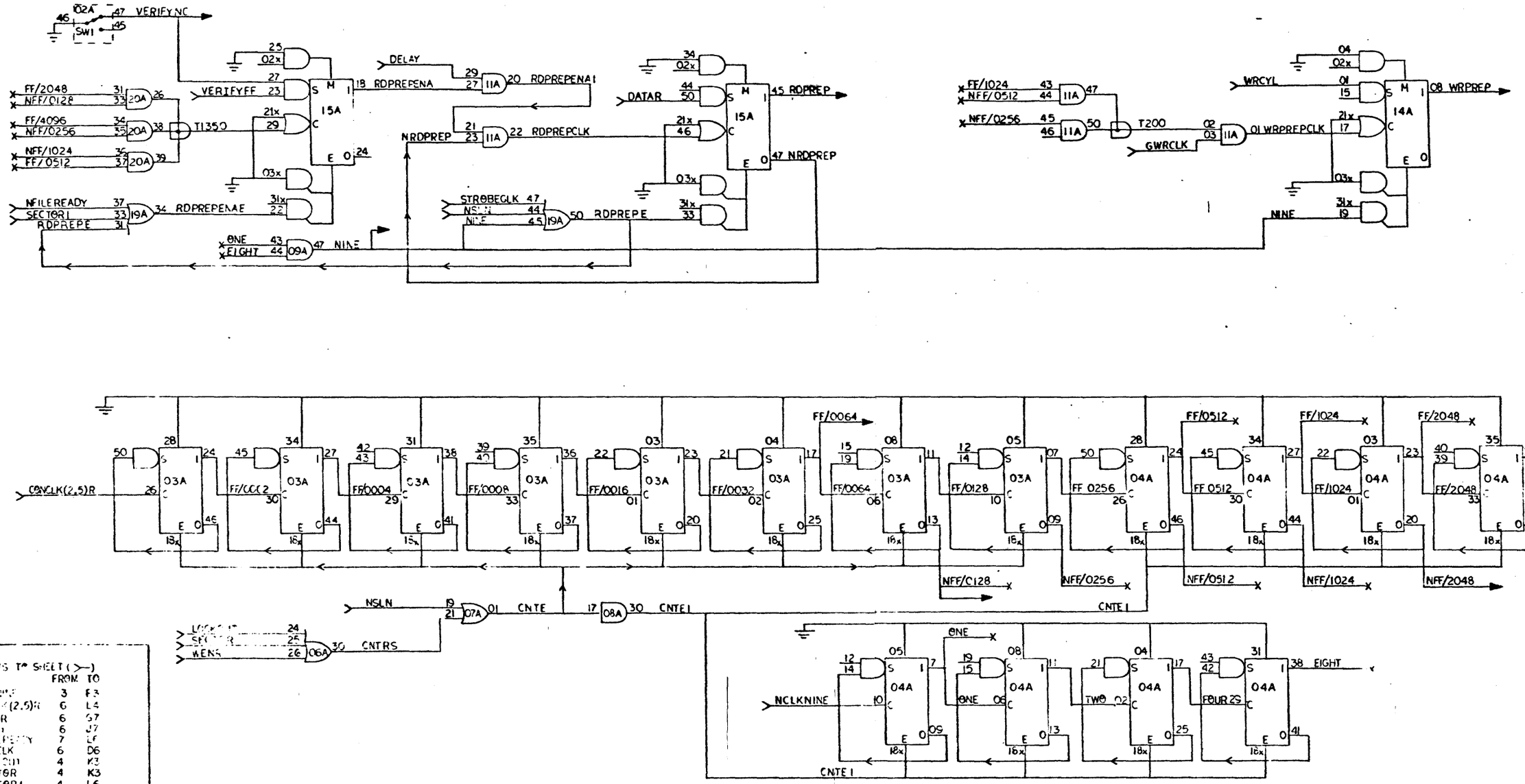
Xerox Data Systems XEROX

TITLE: LOGIC DIAGRAM — 7250

DWG. NO. 203329

CHANGE LETTER: A

SHEET 4 OF 8



INPUTS TO SHEET (←)

	FROM	TO
NCLKNINE	3	F3
CONCLK(2,5)R	6	L4
CONCLK	6	G7
CONCLK1	6	J7
NFILEREADY	7	L6
GWRCLK	6	D6
LOCK(2:0)	4	K3
SECTOR	4	K3
SECTOR1	4	L6
NSLN	2	J3,H6
STROBECLK	4	H6
VERIFYFF	3	K7
WENR	6	K3
WRCYL	6	C7

INTERNAL SIGNALS (X)

	FROM	TO
EIGHT	C3	K6
NFF/C128	E4	L7
NFF/0256	D4	E7, L6
FF/0512	C5	L6
NFF/0512	C4	E7
FF/1024	B5	E6
NFF/1024	B4	L6
FF/2048	B5	L7
FF/4096	A4	L6
ONE	E3	K5

OUTPUTS FROM SHEET (→)

	FROM	TO
FF/0064	F4	6
NFF/0128	E4	6
NFF/2048	B4	6
(NINE)	J6	3
RDPREP	F7	3
VERIFYNC	K7	7
WRPREP	B7	3

CAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHT 1			

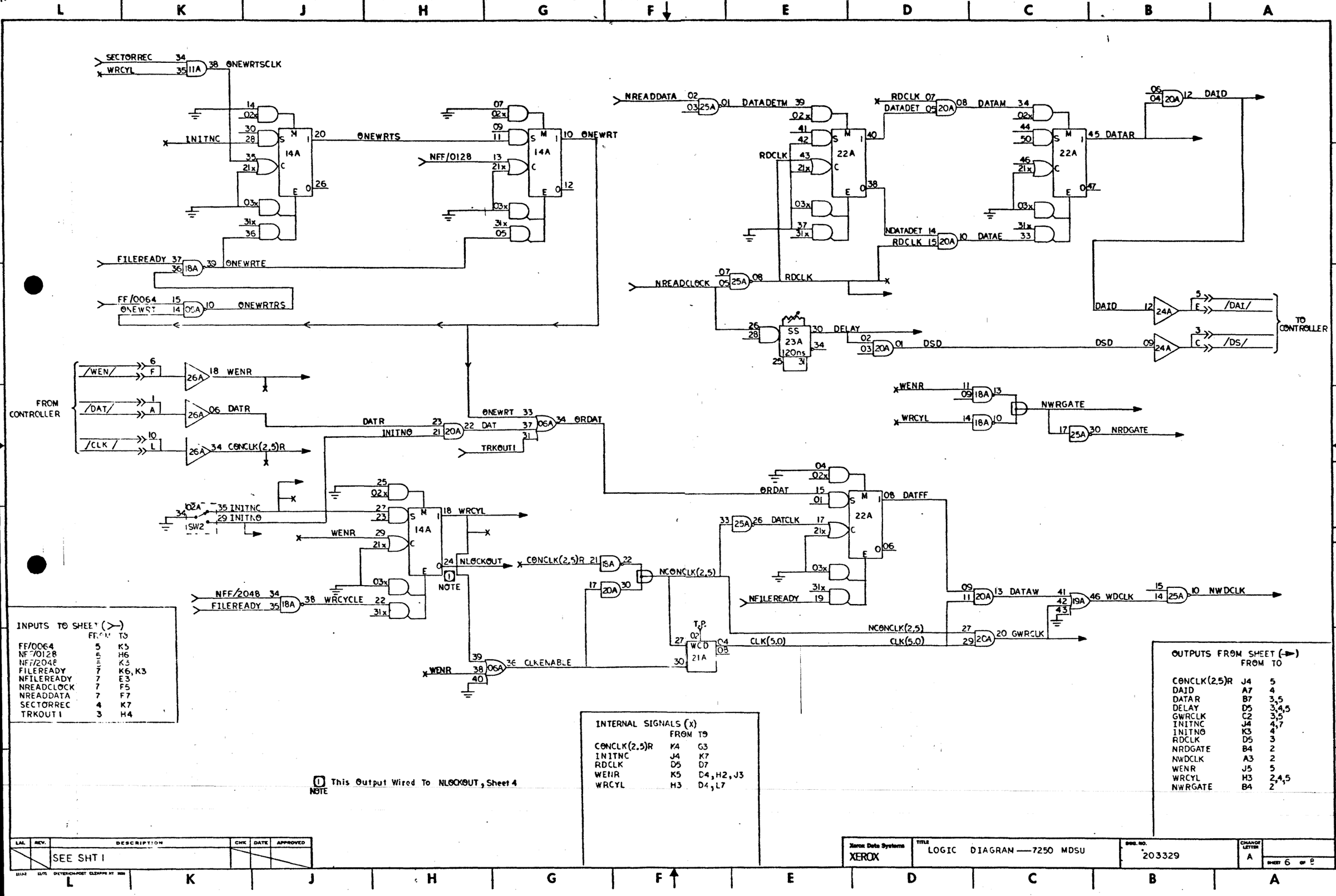
Xerox Data Systems XEROX

TITLE: LOGIC DIAGRAM — 7250 MDSU

DWG. NO. 203329

CHANGE LETTER: A

SHEET 5 OF 8



INPUTS TO SHEET (>)

	FROM	TO
FF/0064	5	K5
NFF/0128	5	H6
NFF/2048	5	K3
FILEREADY	7	K6, K3
NFILEREADY	7	E3
NREADCLOCK	7	F5
NREADDATA	7	F7
SECTORREC	4	K7
TRKOUT1	3	H4

INTERNAL SIGNALS (x)

	FROM	TO
CΘNCLK(2,5)R	K4	G3
INITNC	J4	K7
RDCLK	D5	D7
WENR	K5	D4, H2, J3
WRCYL	H3	D4, L7

OUTPUTS FROM SHEET (->)

	FROM	TO
CΘNCLK(2,5)R	J4	5
DAID	A7	4
DATAR	B7	3,5
DELAY	D5	3,4,5
GWRCLK	C2	3,5
INITNC	J4	4,7
INITNΘ	K5	4
RDCLK	D5	3
NRDGATE	B4	2
NWDCLK	A3	2
WENR	J5	5
WRCYL	H3	2,4,5
NWRGATE	B4	2

(1) NOTE This Output Wired To NLOCKOUT, Sheet 4

LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHT 1			

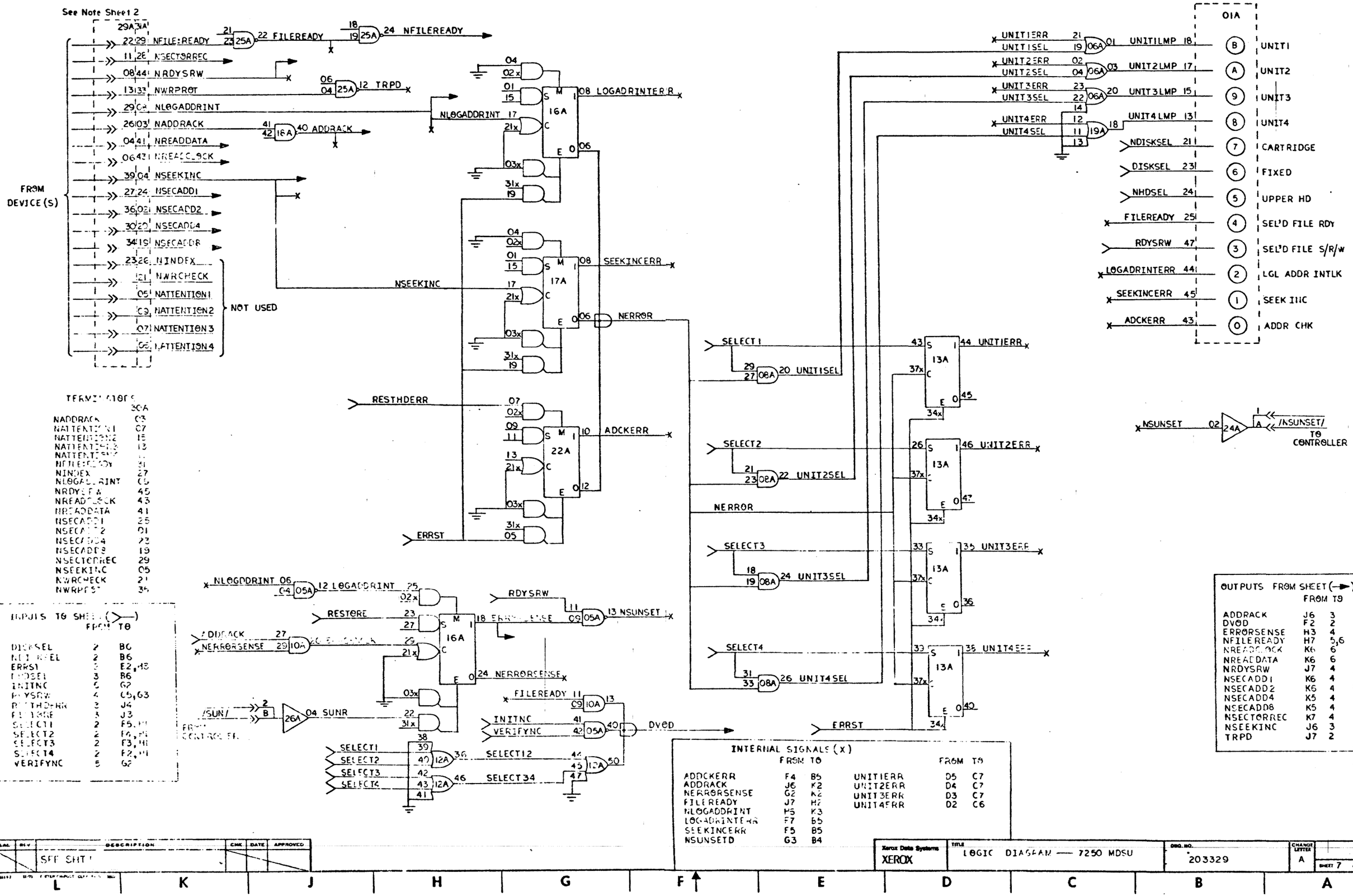
Xerox Data Systems XEROX

TITLE LOGIC DIAGRAM — 7250 MDSU

DWG. NO. 203329

CHANGE LETTER A

SHEET 6 OF 9


See Note Sheet 2
FROM DEVICE(S)
NFILEREADY
NSECTORREC
NRDYSRW
NWRPROT
NLOGADDRINT
NADDRACK
NREADDATA
NREADCLOCK
NSEEKINC
NSECADD1
NSECADD2
NSECADD4
NSECADD8
NINDEX
NWRCHECK
NATTENTION1
NATTENTION2
NATTENTION3
NATTENTION4
NOT USED
25A
FILEREADY
NFILEREADY
TRPD
16A
ADDRACK
NLOGADDRINT
LOGADRINTERR
17A
SEEKINCERR
NERROR
RESTHDERR
22A
ADCKERR
ERRST
TERMINATORS
INPUTS TO SHEET (→) FROM T8
DISKSEL 2 B6
NHDSEL 2 B6
ERRST 3 E2,H3
FMDSEL 3 B6
INITNC 5 G2
RDYSRW 4 C5,G3
RESTHDERR 3 J4
RESTORE 3 J3
SELECT1 2 F5,H1
SELECT2 2 F4,H1
SELECT3 2 F3,H1
SELECT4 2 F2,H1
VERIFYNC 5 G2
NLOGDDRINT 06
12 LOGADDRINT
RESTORE
ADDRACK
NERRORSENSE
10A
24 NERRORSENSE
RDYSRW
13 NSUNSET
/SUN/
26A
04 SUNR
FROM CONTROLLER
FILEREADY 11
10A
INITNC
VERIFYNC
05A
DVOD
SELECT1
SELECT2
SELECT3
SELECT4
12A
SELECT12
SELECT34
SELECT1
08A
20 UNIT1SEL
SELECT2
22 UNIT2SEL
NERROR
SELECT3
24 UNIT3SEL
SELECT4
26 UNIT4SEL
13A
UNIT1ERR
UNIT2ERR
UNIT3ERR
UNIT4ERR
01A
UNIT1LMP
UNIT2LMP
UNIT3LMP
UNIT4LMP
NDISKSEL
DISKSEL
NHDSEL
FILEREADY
RDYSRW
LOGADRINTERR
SEEKINCERR
ADCKERR
B UNIT1
A UNIT2
9 UNIT3
8 UNIT4
7 CARTRIDGE
6 FIXED
5 UPPER HD
4 SEL'D FILE RDY
3 SEL'D FILE S/R/W
2 LGL ADDR INTLK
1 SEEK IIIC
0 ADDR CHK
NSUNSET
24A
/NSUNSET/ TO CONTROLLER
INTERNAL SIGNALS (X)
FROM T8
ADDCKERR F4 B5
ADDRACK J6 K2
NERRORSENSE G2 K2
FILEREADY J7 H2
NLOGADDRINT H5 K3
LOGADRINTERR F7 B5
SEEKINCERR F5 B5
NSUNSETD G3 B4
UNIT1ERR D5 C7
UNIT2ERR D4 C7
UNIT3ERR D3 C7
UNIT4ERR D2 C6
OUTPUTS FROM SHEET (→)
FROM T8
ADDRACK J6 3
DVOD F2 2
ERRORSENSE H3 4
NFILEREADY H7 5,6
NREADCLOCK K6 6
NREADDATA K6 6
NRDYSRW J7 4
NSECADD1 K6 4
NSECADD2 K6 4
NSECADD4 K5 4
NSECADD8 K5 4
NSECTORREC K7 4
NSEEKINC J6 3
TRPD J7 2
DESCRIPTION
SEE SHT 1
Xerox Data Systems
XEROX
TITLE LOGIC DIAGRAM — 7250 MDSU
DRG. NO. 203329
CHANGE LETTER A
SHEET 7 OF 9

IOP — CONTROLLER			
	32C		
SIGNAL NAME	CABLE PIN	CIRCUIT	CONNECTOR
/FR7/	1 A	D	8
/FR6/	2 B	D	8
/FR5/	3 C	D	8
/FR4/	4 D	D	8
/FR3/	5 E	D	8
/FR2/	6 F	D	8
/FR1/	7 G	D	8
/FR0/	8 H	D	8
/FR5/	9 K	D	8
/DB8/	10 L	D	8
/DB9/	11 M	D	8
/DX3/	12 N	D	8
/DC/	13 P	D	8
/DX4/	14 R	D	8
	30C		
SIGNAL NAME	CABLE PIN	CIRCUIT	CONNECTOR
/DA7/	1 A	R D	6 2
/DA6/	2 B	R D	4 1
/DA5/	3 C	R D	10 9
/DA4/	4 D	R D	8 3
/DA3/	5 E	R D	13 12
/DA2/	6 F	R D	18 15
/DA1/	7 G	R D	20 19
/DA0/	8 H	R D	22 23
/DAP/	9 K	R D	27 25
/ED/	10 L	R D	34 33
/PC/	11 M	R D	36 35
/DBR/	12 N	R D	38 37
/SC/	13 P	D	40 39
	14 R	R D	45 42

IOP — CONTROLLER			
	28C		
SIGNAL NAME	CABLE PIN	CIRCUIT	CONNECTOR
/RST/	1 A	R	15
/CLI/	2 B	R	7
/ES/	3 C	R	17
/RSA/	4 D	R	18
/SI0/	5 E	R	8
/HI0/	6 F	R	8
/TI0/	7 G	R	19
/TDV/	8 H	R	22
/AI0/	9 K	R	30
/ASC/	10 L	R	33
/FS/	11 M	R	36
/SID/	12 N	R	35
/WADR/	13 P	R	44
/IER/	14 R	R	45
	26C		
SIGNAL NAME	CABLE PIN	CIRCUIT	CONNECTOR
/HPI/	1 A	R D	6 35
/HPS/	2 B	R D	4 33
/FAST/	3 C	R D	10 31
/AVI/ /AV0/	4 D	R D	8 29

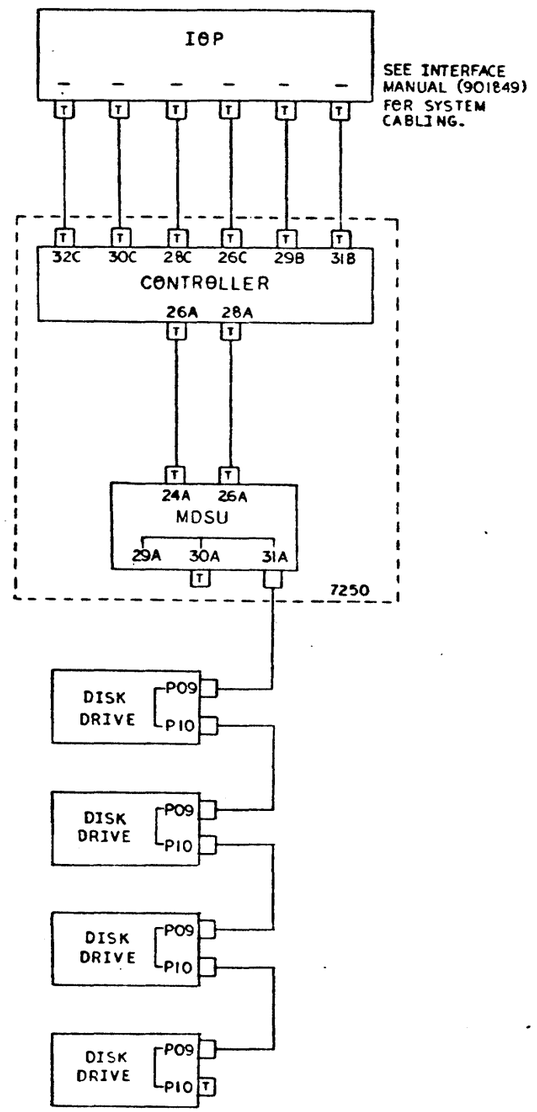
IOP — CONTROLLER			
	29B		
SIGNAL NAME	CABLE PIN	CIRCUIT	CONNECTOR
/DB0/	1 A	R D	6 2
/DB1/	2 B	R D	4 1
/DB2/	3 C	R D	10 9
/DB3/	4 D	R D	8 3
/DB4/	5 E	R D	13 12
/DB5/	6 F	R D	18 15
/DB6/	7 G	R D	20 19
/DB7/	8 H	R D	22 23
/EDX2/	9 K	R D	27 25
/DC0/	10 L	R D	34 33
/DC1/	11 M	R D	36 35
/DC2/	12 N	R D	38 37
/DC3/	13 P	R D	40 39
/EDX4/	14 R	R D	45 42
	31B		
SIGNAL NAME	CABLE PIN	CIRCUIT	CONNECTOR
/DC4/	1 A	R D	6 2
/DC5/	2 B	R D	4 1
/DC6/	3 C	R D	10 9
/DC7/	4 D	R D	8 3
	5 E	R D	13 12
/DD0/	6 F	R D	18 15
/DD1/	7 G	R D	20 19
/DD2/	8 H	R D	22 23
/DD3/	9 K	R D	27 25
/DD4/	10 L	R D	34 33
/DD5/	11 M	R D	36 35
/DD6/	12 N	R D	38 37
/DD7/	13 P	R D	40 39
	14 R	R D	45 42

CONTROLLER — MDSU					
26A				24A	
CONNECTOR	CIRCUIT	CABLE PIN	SIGNAL NAME	CABLE PIN	CIRCUIT	CONNECTOR
6	R	1 A	/NSUNSET/	1 A	D	2
4	R	2 B	/POWERMON/	2 B	D	1
10	R	3 C	/DS/	3 C	D	9
8	R	4 D	/SP/	4 D	D	3
13	R	5 E	/DAI/	5 E	D	12
18	R	6 F	/TRP/	6 F	D	15
20	R	7 G	/DV1/	7 G	D	19
22	R	8 H	/DV0/	8 H	D	23
27	R	9 K	/TYP0/	9 K	D	25
34	R	10 L	/TYP1/	10 L	D	33
36	R	11 M	/AN0/	11 M	D	35
38	R	12 N	/AN1/	12 N	D	37
40	R	13 P	/AN2/	13 P	D	39
42	R	14 R	/AN3/	14 R	D	45
28A				26A		
CONNECTOR	CIRCUIT	CABLE PIN	SIGNAL NAME	CABLE PIN	CIRCUIT	CONNECTOR
2	D	1 A	/DAT/	1 A	R	6
1	D	2 B	/SUN/	2 B	R	4
9	D	3 C	/SLN/	3 C	R	10
3	D	4 D	/NSEC3/	4 D	R	8
12	D	5 E		5 E	R	13
15	D	6 F	/WEN/	6 F	R	18
19	D	7 G		7 G	R	20
23	D	8 H		8 H	R	22
25	D	9 K	/SC1/	9 K	R	27
33	D	10 L	/CONCLK(2.5)/	10 L	R	34
35	D	11 M	/TRK/	11 M	R	36
37	D	12 N	/ID0/	12 N	R	38
39	D	13 P	/ID1/	13 P	R	40
45	D	14 R	/ID2/	14 R	R	42

MDSU — DISK DRIVE				
29A	31A			P09 OR P10
CONNECTOR/CABLE PIN	CONNECTOR/CABLE PIN	OUTPUT/INPUT	SIGNAL NAME	CABLE PIN
31	10	0	NTR2	BB
35	30		NTR3	b
9	34		NTR4	T
25	27		NTR5	f
10	31		NTR6	X
20	39		NTR7	J
28	15		NTR8	s
21	38		NTR9	N
24	25		HDSEL	a
33	17		NSTROBE	t
15	45		NSELECT1	L
12	46		NSELECT2	R
17	42		NSELECT3	V
14	47		NSELECT4	Z
42	12		DISKSEL	AA
41	13		NRESTORE	w
7	50		NWDCLK	B
18	40		NRDGATE	E
37	22		NWRGATE	e
19	36		NERASEGATE [1]	K
16	14		GND	
22	29		NFILE:READY	U
11	28		NSECTORREC	W
8	44		NRDYSRW	F
13	33		NWRPROT	P
29	8		NLOGADDRINT	y
26	3		NADDRACK	p
4	41		NREADDATA	C
6	43		NREADCLOCK	A
39	4		NSEEKINC	u
27	24		NSECADD1	c
36	2		NSECADD2	j
30	20		NSECADD4	k
34	19		NSECADD8	n
23	26		NINDEX	Y
	5		NATTENTION1	CC
	9		NATTENTION2	DD
	7		NATTENTION3	EE
	6		NATTENTION4	FF
	21		NWRCHECK	h

[1] NERASEGATE IS WIRED TO AND GENERATED BY NWRGATE (See Sheet 2)

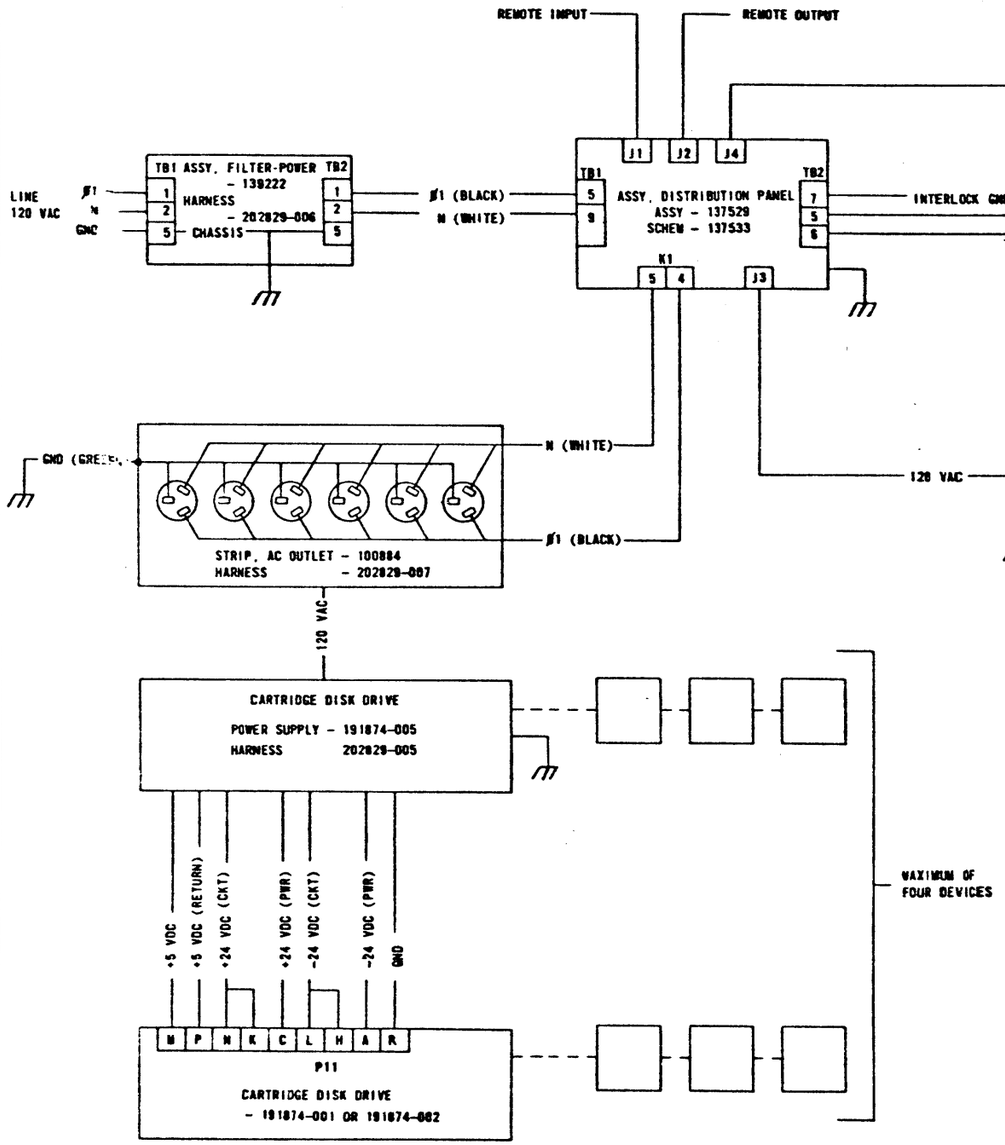
TYPICAL SYSTEM CABLING



LAI	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHT 1			

Xerox Data Systems XEROX | TITLE LOGIC DIAGRAM — MDSU | DWG. NO. 203329 | CHANGE LETTER A | SHEET 8 OF 8

REVISIONS				204349 B
LAL	REV.	DESCRIPTION	CHK	DATE / APPROVED
	–	ENGRG RELEASE		
X	B	REVISED & REDRAWN, MFG RELEASE, NO E.O.		



DIST CODE 409

NOTES UNLESS SPECIFIED
1. TOLERANCES .XX ±.05 .XXX ±.010 DIMENSIONED ANGLES ±1/2°
2. BREAK ALL SHARP EDGES .005 APPROX.
3. FINISH SURFACES ✓
4. ALL DIM. IN INCHES
5. ALL TRUE POSITION TOLERANCES APPLY AT MMC

DRAWN	[illegible]	7-31-73
CHECK	[illegible]	8-3-73
APPR.	[illegible]	8-3-73
MATERIAL		
FINISH		
MODEL NO. FIRST USE	———	
NEXT ASSY. FIRST USE	202624	

XEROX

TITLE: DIAGRAM, POWER CABLING, CARTRIDGE DISK SUBSYSTEM

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	204349	B

SCALE NONE | DO NOT SCALE DRAWING | SHEET 1 OF 1

204349 B

REVISIONS				137533 F
LAL	REV	DESCRIPTION	CHK	DATE / APPROVED
	A	ENGRG RELEASE		
	B	REVISED AND REDRAWN		
	C	ADDED J8		
X	D	MFG RELEASE NO E.O.		
X	E	SEE REV E.O 137535E ADDED REVS. B & C, ZONE 3A ADDED R2 & C1		
X	F	SEE REV E.O 137527L; ADDED R1 & RC2. FMK = 7202-03/10, 7203-03/09, 7204-02/09, 7212-01/09, 7232-01/10.		

NOTES:

1. FOR REPLACEMENT PARTS LIST SEE SHEET 2, 'A' SIZE.

TB1

$\phi 1$ 4
$\phi 2$ 5
6
$\phi 3$ 7
8
N 9
N 10
G 11
G 12

TO DISC MOTORS

E1

TB2

7 INT

6 +25V

5 GRD

REMOTE

S1

LOCAL

RC1

RC2

R1

K4

K1

K3

CR1

K5

J1 X
W
120V, 50/60 HZ REMOTE ON-OFF INPUT

J2 X
W
120V, 50/60 HZ REMOTE ON-OFF OUTPUT

TB1

POWER MONITOR A CT B 1 2 3

T1

C1

F1

TB2

R2

J3 X W TO PT 20 POWER SUPPLY

J4 X W 120V, 50/60 HZ OUTPUT FANS

J5 X W 120V, 50/60 HZ OUTPUT FANS

J6 X W 120V, 50/60 HZ OUTPUT FANS

J7 X W 120V, 50/60 HZ OUTPUT FANS

E2

J8 W X 120V 50/60HZ OUTPUT FANS

413
DIST CODE

MATERIAL LIST

NOTES UNLESS SPECIFIED

DRAWN [illegible] 2/12/67
CHECK [illegible] 2/27/67
APPR. [illegible] 2.27.67

MATERIAL

FINISH

MODEL NO. FIRST USE 7212

NEXT ASSY. FIRST USE 137529

SDS SCIENTIFIC DATA SYSTEMS SANTA MONICA, CALIFORNIA

TITLE SCHEMATIC DIAGRAM. DISTRIBUTION PANEL

SIZE D DWG NO 137533 REVISION LETTER F

DO NOT SCALE DRAWING SHEET 1 OF 3

137533 F1

MODEL NO 7212

REPLACEMENT PARTS LIST

137533-F

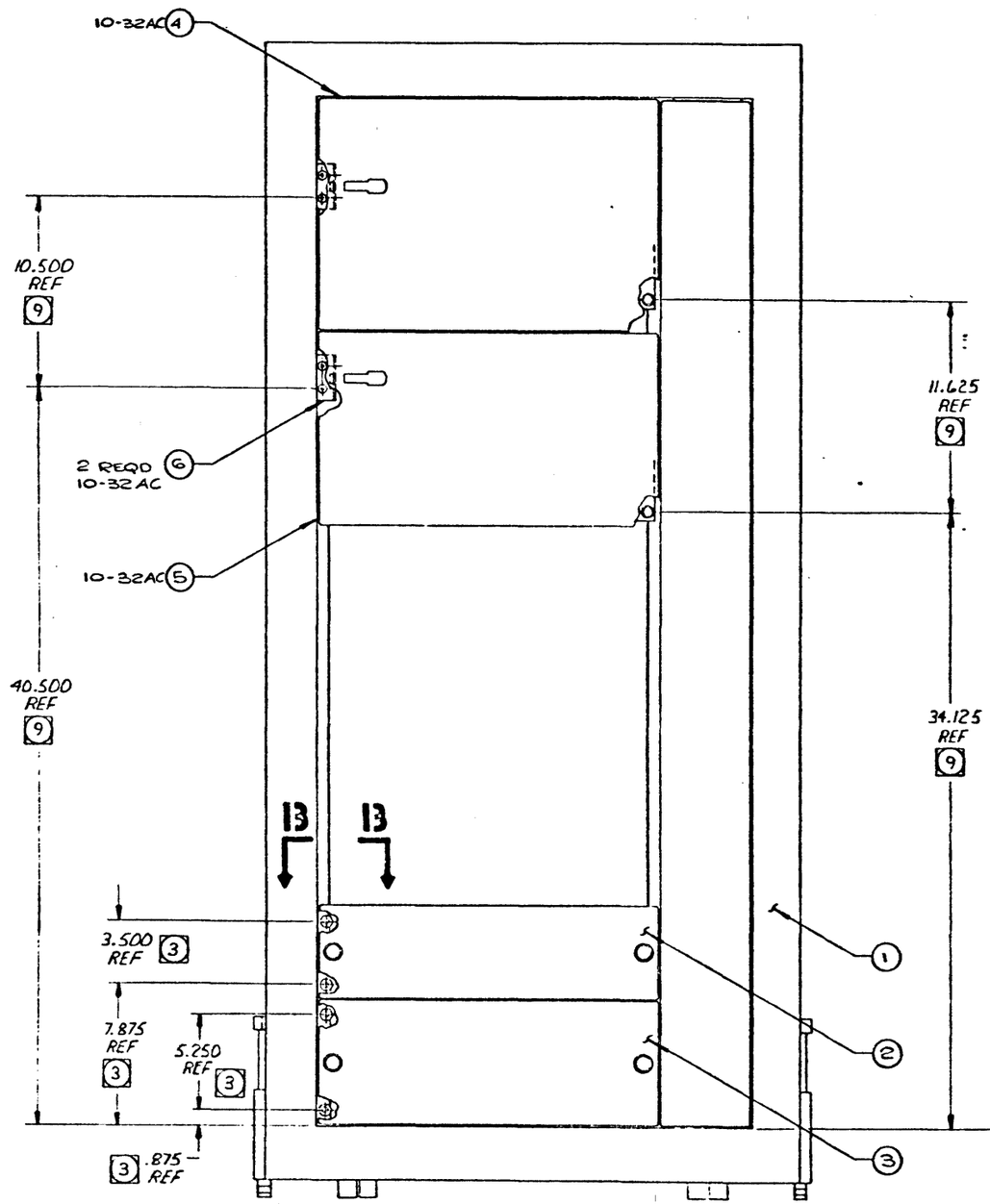
ITEM	DESCRIPTION	DESIGNATORS	QTY	SUPPLIER AND PART NO.		ZIP
1	Diode, 7E Silicon Rectifier, SDS 113 200V, 750 MA	CR1	1	Motorola Texas Int. Rect. Corp.	1N4003 1N4003 1N2069A	85002 75222 90245
2	Fuse, S 250 V .250 Amp 3AG	F1	1	Littelfuse Bussman	312000 Series AGC, MTH, GLH	60016 63107
3	Contactor, 3 Pole St. 30A, 600 VAC	K1	1	Westinghouse General Electric Arrow-Hart Rowan Controller	A201K1BA CR161CC222 CRA-130-U 120 VAC XB2601	15009 61701 06106 21157
4	Relay DN DPDT, 5A 24 VDC Coil	K3	1	Guardian Elec. Guardian Elec. Line Electric Potter-Brumfield	905-2C-24 VDC 645-2C-24 VDC MW2D-24 VDC GA11D-24 VDC	60607 60607 07050 47570
5	Relay, DR DPDT, 10A 115 VACOIL	K4	1	Eagle Signal Life Instrument Phillips-Advance Potter-Brumfield Guardian Electric SDS	25AA-A1115 RA0-3102 GH-1155 KA3310 1200 Series 130132	52802 02030 60431 47570 60607
6	Relay, AG, SPST Thermal Delay 115 VAC	K5	1	Arrow-Hart Bryant General Electric Hubbell Pass and Seymour	FS2 FS2 FS2 FS2 FS2	06106 06605 06050 06602 13209
7	Resistor, DU, Fixed Film, 10-1M 2 PCT	R1	1	Corning Electra Int. Res. Co.	C-32 MF7C CES, L-32	16701 67301 52602

TITLE
ASSY,
DISTRIBUTION PANEL

SDS

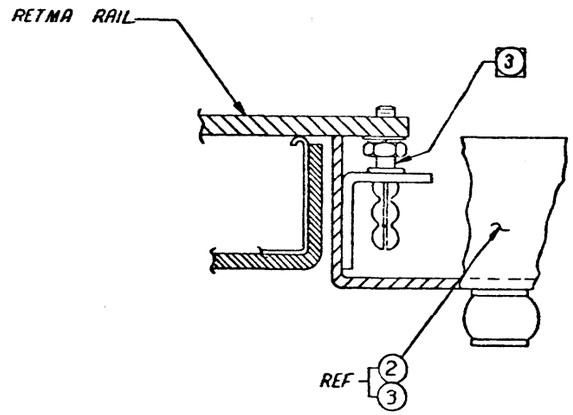
137533 F

REVISIONS				202624 A
LTR	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE, NO. C.O.		5-17-73	



FRONT

DETAIL C (SEE SH 2)
SCALE: NONE



SECTION 13-13
8 LOCATIONS
SCALE: NONE

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR IDENTIFICATION AND SERIALIZATION MARK CHARACTERS .12 HIGH, COLOR: BLACK PER XEROX SPEC 101624 & 100198, APPROX AS SHOWN.
2. FOR MATERIAL LIST SEE SHEET 3 & 4.
3. INSTALL STUDS AND RELATED HARDWARE (SUPPLIED LOOSE WITH PANEL ASSY XEROX NO. 203116, 203117) IN RETMA RAIL AT DIMENSIONS INDICATED (REF SECTION B-B).
4. HARDWARE CALLOUTS PER XEROX SPEC 155984.
5. MANUFACTURING WILL SELECT CLAMP SIZE AND LOCATION. CABLE OR CABLE BUNDLE SHALL BE SECURED SUFFICIENTLY TIGHT TO PREVENT CHAFING AND/OR PROVIDE STRAIN RELIEF. SPIRAL TUBING AND/OR NYLON GROMMET SHALL BE APPLIED WHEREVER NECESSARY TO PREVENT CHAFING AND WEAR DAMAGE.
6. BOND IN PLACE PER XEROX APPLICATION SPEC 182246, USING XEROX ADHESIVE NO. 182245-001.
7. ADHERE LABEL (ITEM 20) IN APPROX LOCATION SHOWN.
8. MOUNT DISTRIBUTION PANEL ASSY (ITEM 7), WITH SWITCH 'S1' IN POSITION SHOWN.
9. MOUNT DOOR ASSY (ITEM 4 & 5) AND DOOR BRACKET (ITEM 6) AT DIMENSIONS INDICATED.
10. HARDWARE CONFIGURATION IDENTICAL BOTH SIDES OF POWER SUPPLY (ITEM 12).
11. PLUG 'P1' OF PT20 POWER SUPPLY (ITEM 12) INTO 'J3' OF DIST. PANEL ASSY (ITEM 7).
12. PLUG FAN CABLE PLUG OF RAD CONTROLLER (PART OF ITEM 8) INTO 'J4' OF DIST. PANEL ASSY (ITEM 7).

MATERIAL LIST

NOTES UNLESS SPECIFIED
1. TOLERANCES .XX ±.03 .XXX ±.010 ANGULAR ±1/2°
2. BREAK ALL SHARP EDGES .005 APPROX. √
3. FINISH SURFACES
4. ALL DIM. IN INCHES
5. ALL TRUE POSITION TOLERANCES APPLY AT MMC

DRAWN		3-13-73
CHECK	Adne	5-17-73
APPR.	Tedesco	5-30-73

MATERIAL

FINISH

MODEL NO. 7250
FIRST USE

NEXT ASSY.
FIRST USE

DIST CODE 401

XEROX 5531

TITLE
ASSY, CARTRIDGE
DISK SUBSYSTEM

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	202624	A

SCALE 1/4 | DO NOT SCALE DRAWING | SHEET 1 OF 4

202624 A

MODEL NO 7212

REPLACEMENT PARTS LIST

ITEM	DESCRIPTION	DESIGNATORS	QTY	SUPPLIER AND PART NO.		ZIP
8	Capacitor, Fixed Polystyrene 1000 pf ± 5% 500V	C1	1	Amperex Corning Electra Int Res. Co. Nucleonic Prod Dale Welwyn	1-2-21 C-20 to 470K MF20C (51 OHM -470K) RG20, MDA, MCA RBX-003 DC 1/8 510K 4.7M F-20	11802 16701 67301 52602 90023 68601 44091
9	Resistor, Carbon 200 ½W ± 5%	R2	1	Nucleonic Prod XDS Siemens-Halske	Typett -0- B31010D∅E	90023 90404 10601
10	Suppressor Network Resistor - Capacitor	RC1, RC2	2 2	Teletype Corp.	178535	60078

TITLE

ASSY,
DISTRIBUTION PANEL

SDS

137533 F

MODEL NO 7212

REPLACEMENT PARTS LIST

137533-F

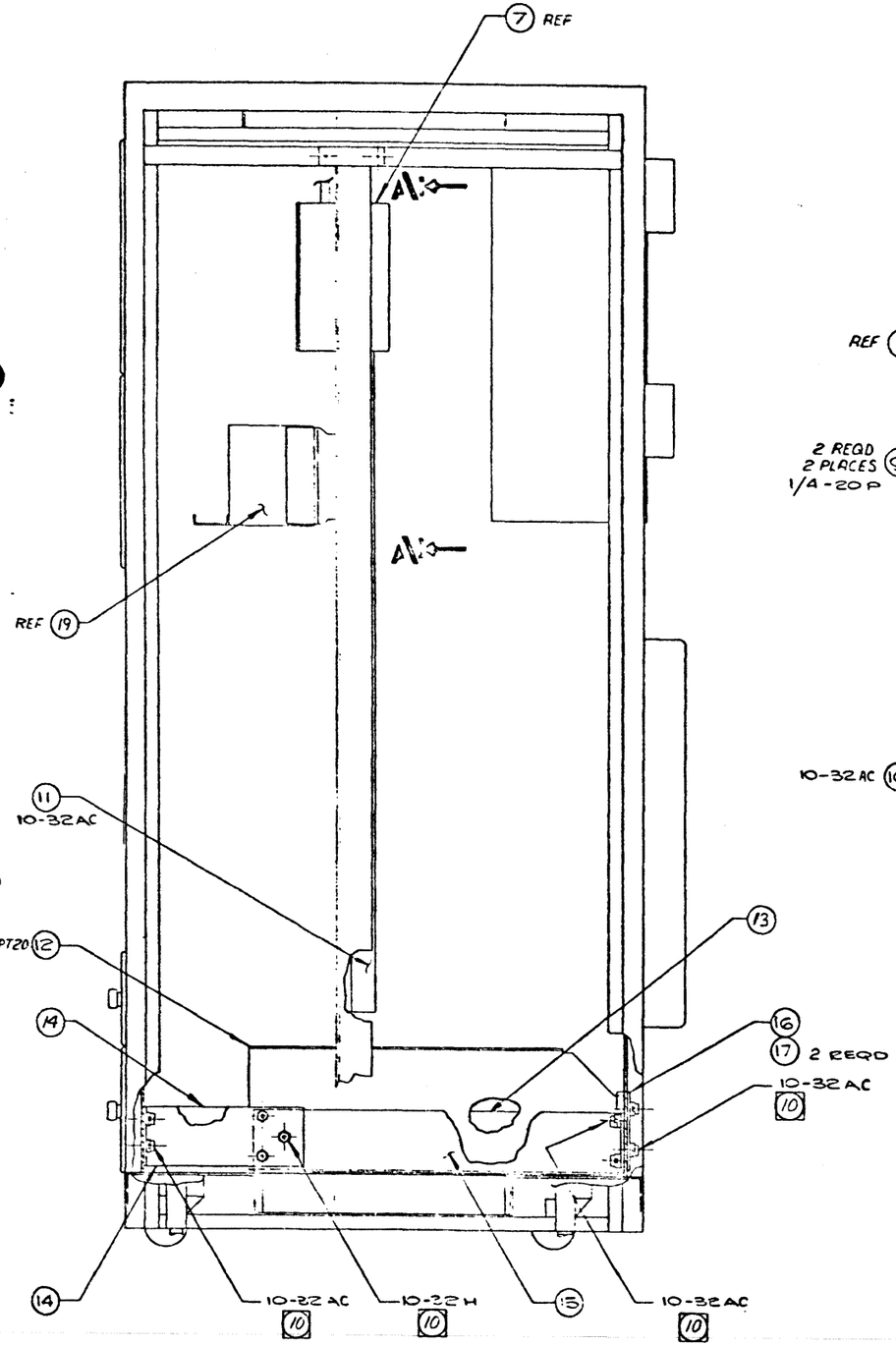
ITEM	DESCRIPTION	DESIGNATORS	QTY	SUPPLIER AND PART NO.		ZIP
1	Diode, 7E Silicon Rectifier, SDS 113 200V, 750 MA	CR1	1	Motorola Texas Int. Rect. Corp.	1N4003 1N4003 1N2069A	85002 75222 90245
2	Fuse, S 250 V .250 Amp 3AG	F1	1	Littelfuse Bussman	312000 Series AGC, MTH, GLH	60016 63107
3	Contactor, 3 Pole St. 30A, 600 VAC	K1	1	Westinghouse General Electric Arrow-Hart Rowan Controller	A201K1BA CR161CC222 CRA-130-U 120 VAC XB2601	15009 61701 06106 21157
4	Relay DN DPDT, 5A 24 VDC Coil	K3	1	Guardian Elec. Guardian Elec. Line Electric Potter-Brumfield	905-2C-24 VDC 645-2C-24 VDC MW2D-24 VDC GA11D-24 VDC	60607 60607 07050 47570
5	Relay, DR DPDT, 10A 115 VACOIL	K4	1	Eagle Signal Life Instrument Phillips-Advance Potter-Brumfield Guardian Electric SDS	25AA-A1115 RA0-3102 GH-1155 KA3310 1200 Series 130132	52802 02030 60431 47570 60607
6	Relay, AG, SPST Thermal Delay 115 VAC	K5	1	Arrow-Hart Bryant General Electric Hubbell Pass and Seymour	FS2 FS2 FS2 FS2 FS2	06106 06605 06058 06602 13209
7	Resistor, DU, Fixed Film, 10-1M 2 PCT	R1	1	Corning Electra Int. Res. Co.	C-32 MF7C CES, L-32	16701 67301 52602

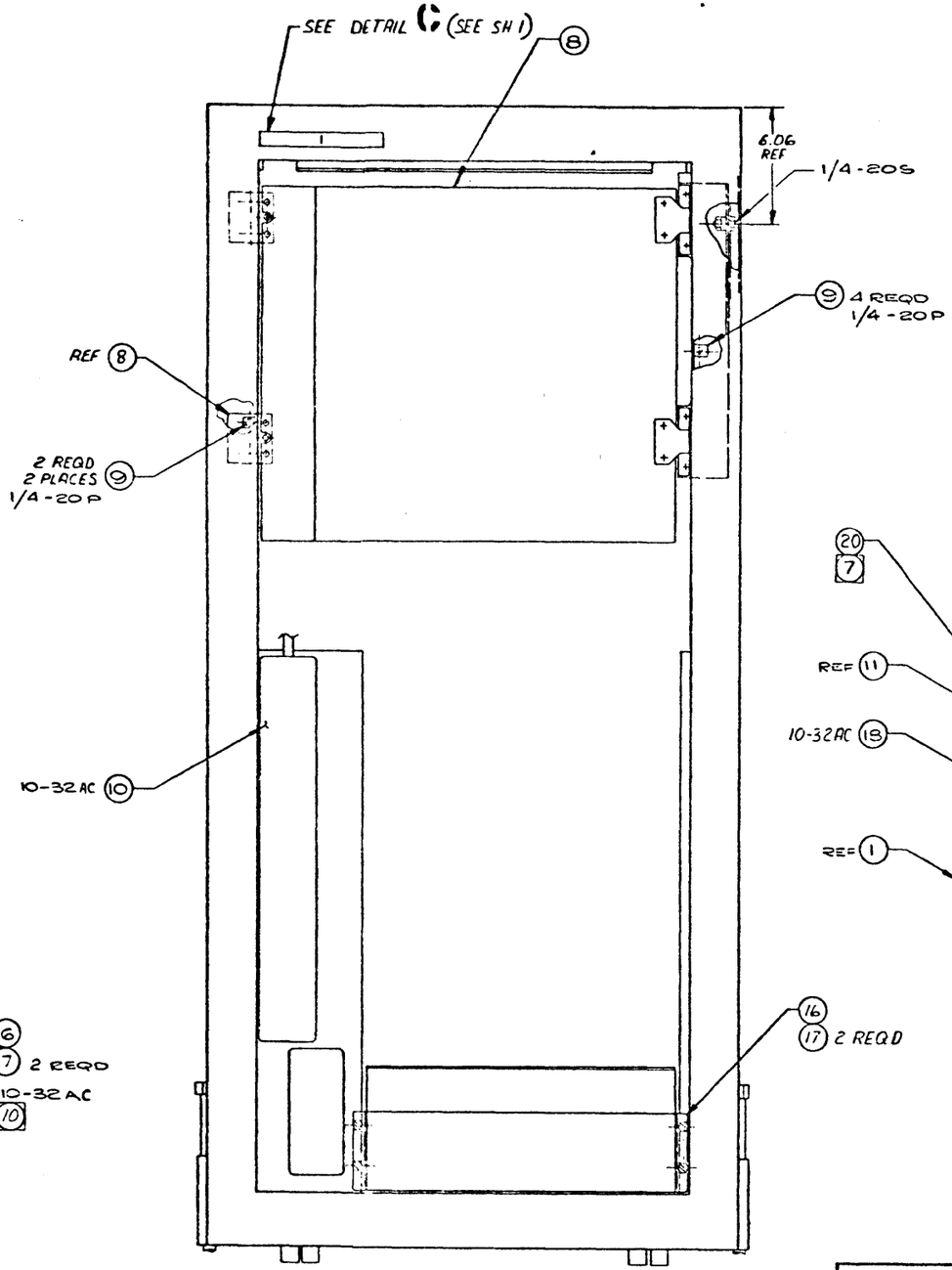
TITLE
ASSY,
DISTRIBUTION PANEL

505

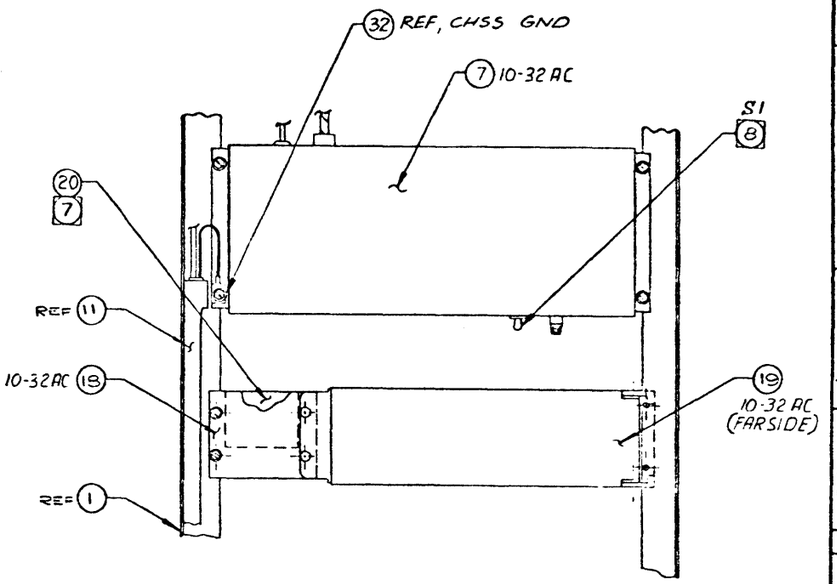
137533 F

REVISIONS				202624 A
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
		SEE SHT 1			





REAR



VIEW A-A

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX ±.05 .XXX ±.010 DIMENSIONED ANGLES ±1/2°	DRAWN	TO	5-13-73
2. BREAK ALL SHARP EDGES .010 APPROX.	CHECK	[illegible]	5-17-73
3. MACH. SURFACES	APPR.	[illegible]	5-23-73
4. ALL DIM. IN INCHES	MATERIAL		
5. ALL TRUE POSITION TOLERANCES APPLY AT MMC	FINISH		

MATERIAL LIST

DIST CODE AC

XEROX

TITLE: ASSY, CARTRIDGE DISK SUBSYSTEM

MODEL NO. FIRST USE	CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
7250	18338	D	202624	A
NEXT ASSY. FIRST USE	SCALE —	DO NOT SCALE DRAWING	SHEET 1 OF 4	

701 South Aviation Boulevard
El Segundo, California 90245

XEROX

401

Material List

ML | Drawing No. 202624 | Rev.

Rev.	Drawing Title	Model No.	Date	Sheet
A	ASSEMBLY, CARTRIDGE DISK SUBSYSTEM	———	3-13-73	4 Of 4

Drawing No. 202624 ML

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
27	Assembly, Harness, Cartridge Disk Subsyst.	202829-001A	1	
28	Assembly, Harness, Cartridge Disk Subsyst.	202829-002A	1	
29				
30				
31	Assembly, Harness, Cartridge Disk Subsyst.	202829-006A	1	
32	Assembly, Harness, Cartridge Disk Subsyst.	202829-007 A	1	
33				
34	Application & Installation Information, Cartridge Disk Subsystem	203777	REF	
35	Specification, Product Design	203521	REF	
36	Procedure, Test & Calibration	203328	REF	
37	List, Pin, Cartridge Disk Subsystem	201822A	REF	
38	Equations, Logic	201823A	REF	
39	Diagram, Logic	203329	REF	
40				
41				
42				
43				
44				
45				
46				
47				
48				
49				
50				
51				
52				

701 South Aviation Boulevard
El Segundo, California 90245

XERO)

401

Material List

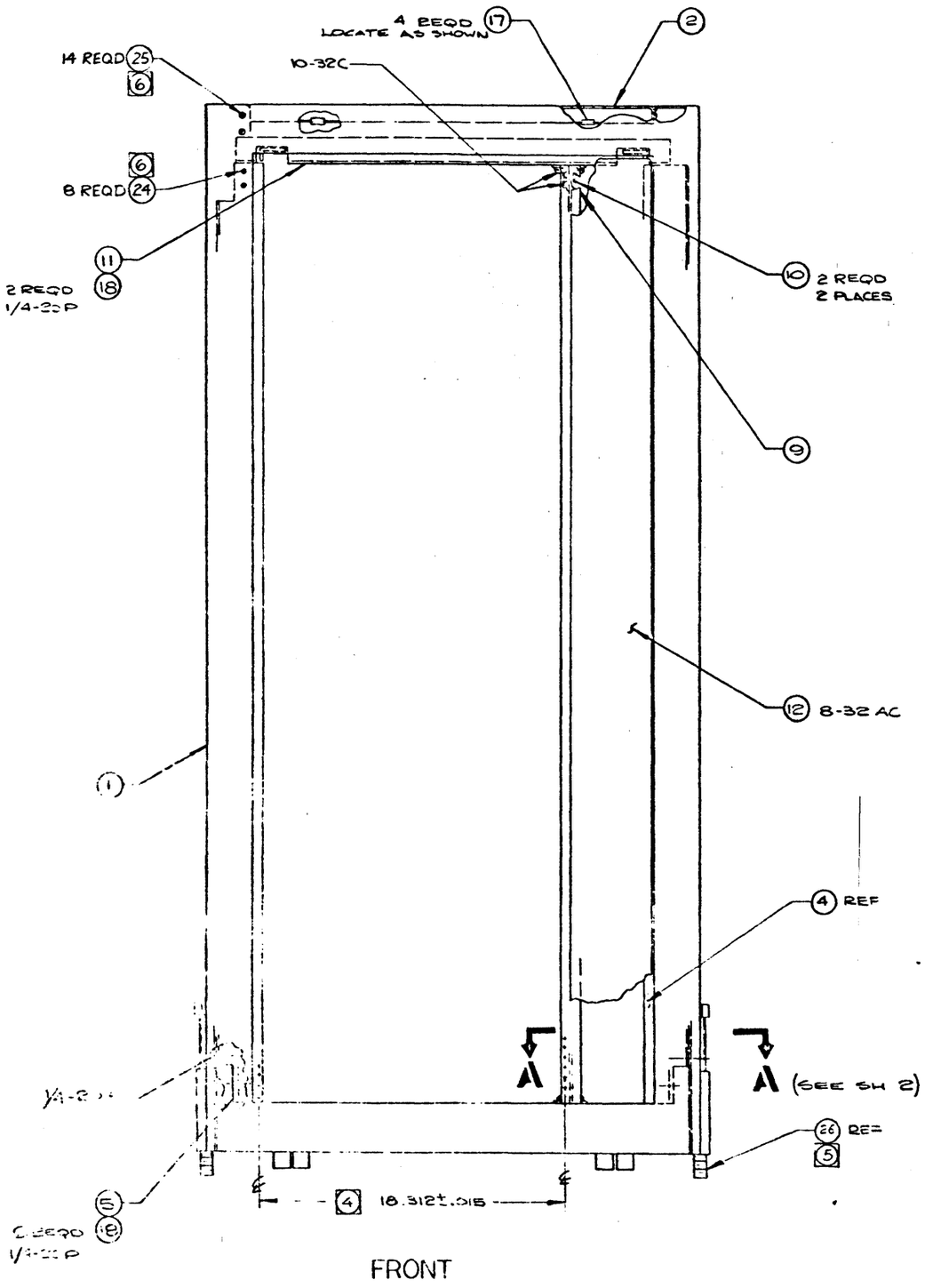
ML	Drawing No. 202624	Rev. A

Drawing Title	Model No.	Date	Sheet
ASSEMBLY, CARTRIDGE DISK SUBSYSTEM	———	3-13 73	3 Of 4

Rev. A

ML Drawing No. 202624

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
1	Assembly, Cabinet - CART Disk Subsystem	202626	1	
2	Assembly, Panel, Push-On	203116	1	
3	Assembly, Panel, Push-On	203117	1	
4	Assembly, Door - Hinged	203121	1	
5	Assembly, Door - Hinged	203119	1	
6	Bracket, Front Door, L.R.	165308	2	
7	Assembly, Distribution Panel	137529	1	
8	Assembly, Controller Kit	203183	1	
9	Nut, Unistrut	124631-005	8	
10	Assembly, Filter - Power	139222	1	
11	Strip, A.C. - Outlet	100884	1	
12	Assembly, PERIPH. Power Supply	154895	1	PT20
13	Angle, Power Supply Support	101059-002	1	
14	Angle, Power Supply Mounting, PT20	147447	2	
15	Angle, Power Supply Support	101059-001	1	
16	Angle, Power Supply Support	139212	2	
17	Screw, 100° Flat Head, Self-Locking	182830-405	4	
18	Angle, Chassis Latch	203142	1	
19	ASSY, Multiple Drive Selection Unit	203126	1	
20	Label, Switches and Lamps	203806	1	
21	Strip, Marker	135171	1	
22	Strap, Cable Tie	158555	A/R	5
23	Anchor, Cable Tie	124856	A/R	5
24	Tubing, Spiral	101625	A/R	5
25	Grommet, Nylon	100840	A/R	5 6
26	Clamp, Cable - Nylon	100657	A/R	5



NOTES: UNLESS OTHERWISE SPECIFIED

1. IDENTIFY ASSY PER XEROX SPEC 100198.
2. FOR MATERIAL LIST SEE SHEET 3.
3. HARDWARE CALLOUTS PER XEROX SPEC 155984.
4. INSTALL TEE (ITEM 9) TO DIMENSION SHOWN.
5. ASSY, SHIPPING HARDWARE KIT (ITEM 26) TO BE SUPPLIED LOOSE.
6. INSTALL IN FRONT FACE OF CABINET ONLY.

REVISIONS					202626 B
LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
X	A	MFG RELEASE, NO E.O.	[illegible]	5-3-73	[illegible]
	B	SEE DCR 100369: SH 1, ZONE 2G ITEM (25) REF WAS: ITEM (25) REF; SH 2, ZONE 2G ITEM (18) WAS: ITEM (8).	[illegible]	10/17/72	[illegible]

DIST CODE 4C1

MATERIAL LIST

NOTES UNLESS SPECIFIED			
1. TOLERANCES .XX ±.02 DIMENSIONED ANGLES ±1/2° .XXX ±.010	DRAWN	TO	3-[illegible]-72
2. BREAK ALL SHARP EDGES .010 APPROX	CHECK	[illegible]	5-2-72
3. BLACK SURFACES	APPR.	[illegible]	5-30-72
4. ALL DIM. IN INCHES	MATERIAL		
5. ALL TRUE POSITION TOLERANCES APPLY AT M/C	FINISH		
MODEL NO. FIRST USE			
NEXT ASSY. FIRST USE 202624			

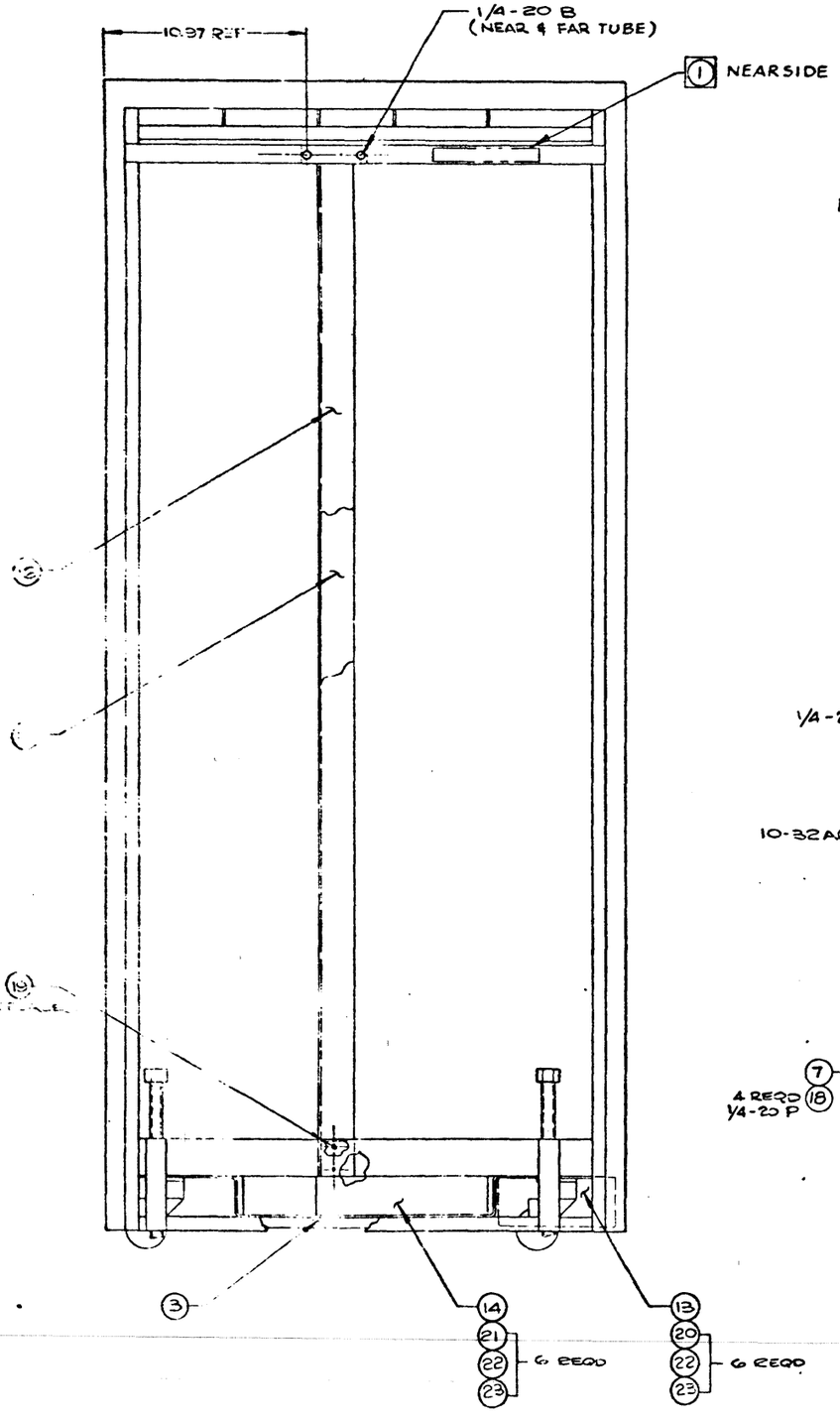
XEROX

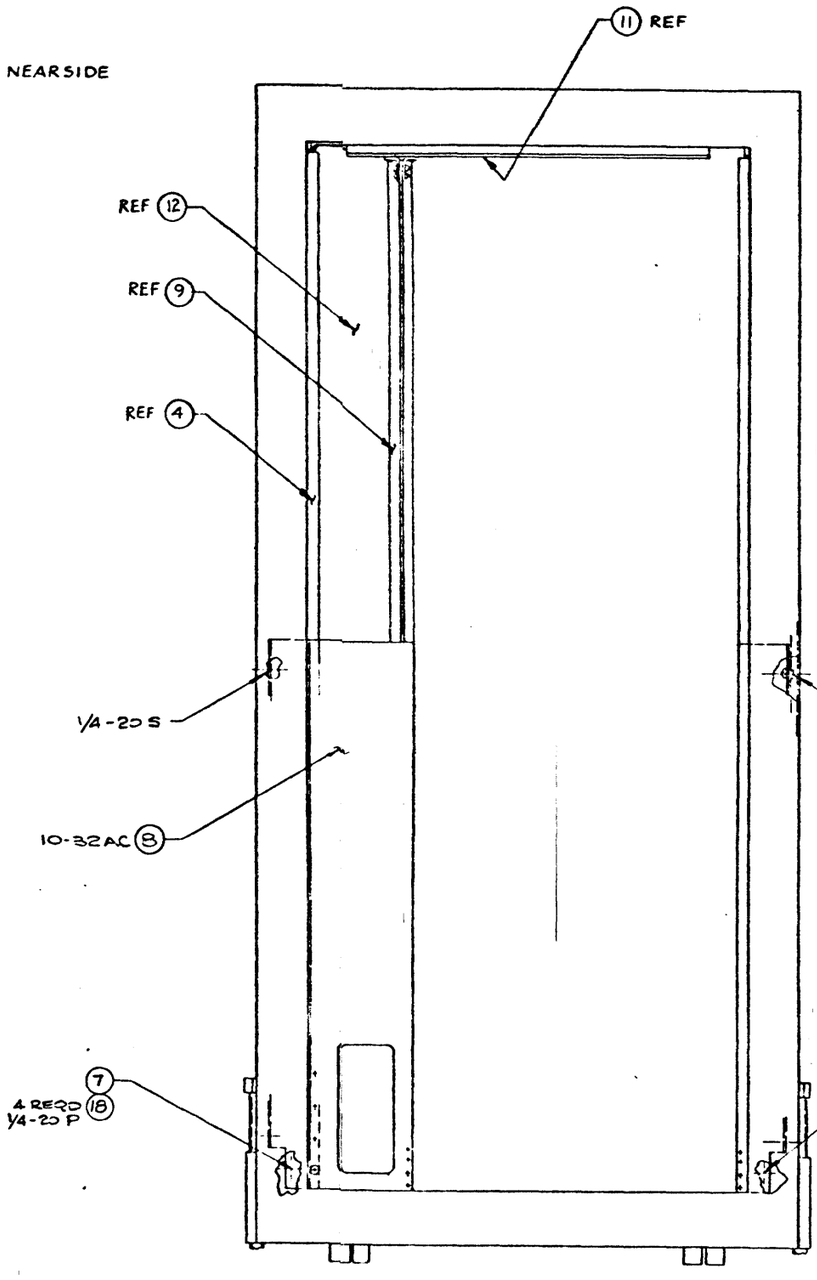
TITLE
ASSY, CABINET — CARTRIDGE DISK SUBSYSTEM

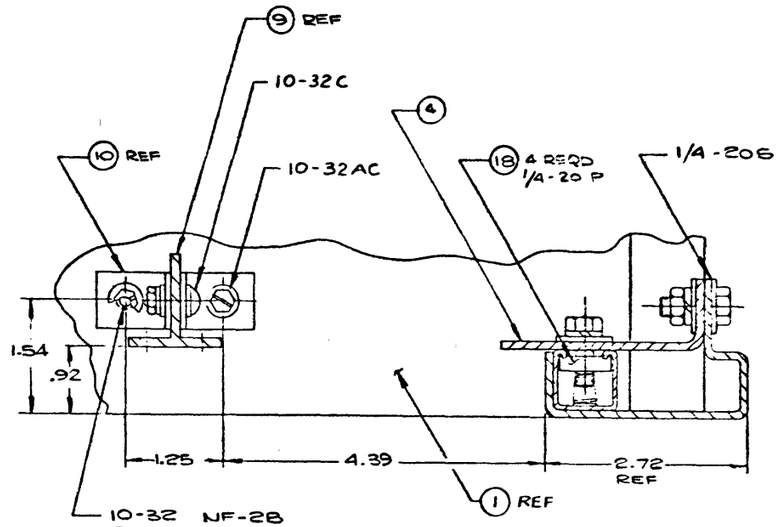
CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	202626	B

SCALE 1/4 FULL | DO NOT SCALE DRAWING | SHEET 1 OF 3

REVISIONS					202626	B
LTR.	REV.	DESCRIPTION	CHK	DATE	APPROVED	
		SEE SHT 1				







SECTION A-A (SEE SH 1)
FILLER PANEL (ITEM 12) OMITTED FOR CLARITY
SCALE: 1/1

REAR

MATERIAL LIST

DIST CODE 42

NOTES UNLESS SPECIFIED
1. TOLERANCES
.XX ±.01 .XXX ±.005 DIMENSIONED ANGLES ±1/2°
2. BREAK ALL SHARP EDGES .010 APPROX.
3. MACH. SURFACES √
4. ALL DIM. IN INCHES
5. ALL TRUE POSITION TOLERANCES APPLY AT MMC

MODEL NO. FIRST USE ——
NEXT ASSY. FIRST USE 202624

DRAWN	T.O.	5-2-73
CHECK	Wiese	5-2-73
APPR.	Tedotte	5-30-73

MATERIAL
FINISH

XEROX

TITLE
ASSY, CABINET-CARTRIDGE DISK SUBSYSTEM

CODE IDENT.	SIZE	DWG. NO.	CHANGE LETTER
18338	D	202626	B

SCALE —— DO NOT SCALE DRAWING SHEET 1 OF 2

701 South Aviation Boulevard
El Segundo, California 90245

XEROX

401

Material List

ML | Drawing No. 202626 | Rev. B

Rev. B | Drawing Title: ASSEMBLY, CABINET - CARTRIDGE DISK SUBSYSTEM | Model No. —— — | Date 3-5-73 | Sheet 3 Of 3

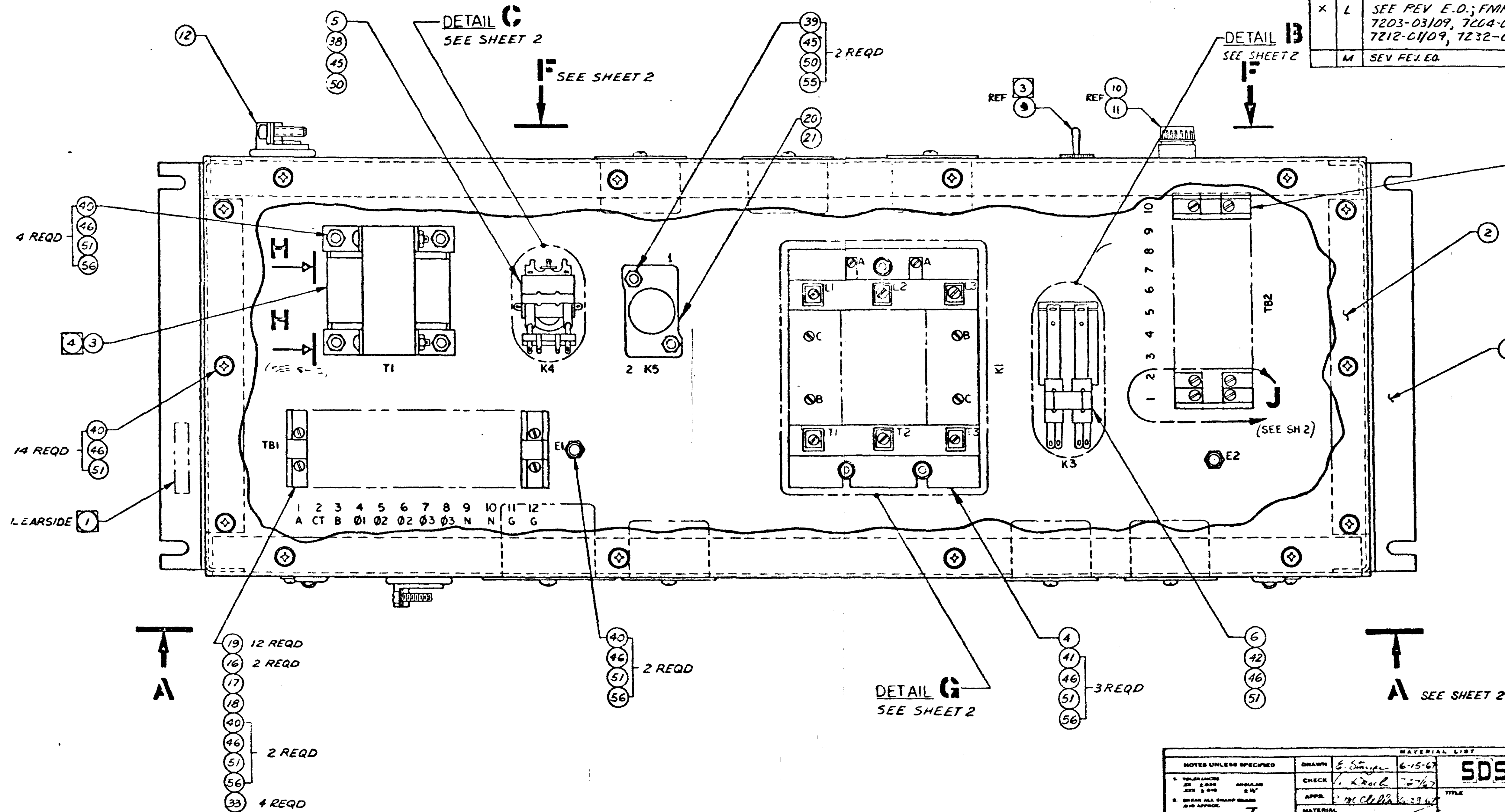
Drawing No. 202626 ML

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
1	Cabinet, Basic Structure	180656	1	
2	Cap, Cabinet Top	117424	1	
3	Plate, Counter Balance	133155	1	
4	Angle, Mounting	131201	1	
5	Angle, Mounting (Retma Pattern)	117422	1	
6	Angle, Mounting, Rear	203112-001	1	
7	Angle Mounting, Rear	203112-002	1	
8	Plate, Mounting	203111	1	
9	Tee, Mounting	131313	1	
10	Angle, Support	131200	4	
11	Channel, Support	203114	1	
12	Panel, Filler, Cabinet	203747	1	
13	Plate, Counter Balance	132645	1	
14	Plate, Counter Balance	132646	1	
15	Bracket, Mounting - Center	203140-001	1	
16	Bracket, Mounting - Center	203140-002	1	
17	Clip, Speed, "U" Type	129565-002	4	
18	Nut, Unistrut	124631-005	20	
19	Screw, SEMS	187672-J05	4	
20	Screw, Cap, Steel, HEX Head	101441-104	6	
21	Screw, Cap, Steel, HEX Head	101441-107	6	
22	Washer, Flat	100018-600	12	
23	Washer, Lock, Spring	100023-600	12	
24	Screw, Nylon	203889-303	8	(6)
25	Screw, Nylon	203889-404	14	(6)
26	ASSY, Kit - Shipping Hardware	203886	1	(5)

NOTES: UNLESS OTHERWISE SPECIFIED

1. IDENTIFY ASSY PER XDS SPEC 100198.
2. FOR MATERIAL LIST SEE SHEETS 3 & 4.
3. MOUNT S1 WITH TERMINALS 3 & 6 TOWARD J5 AND TERMINALS 1 & 4 TOWARD F1.
4. MOUNT T1 WITH TERMINALS 1 THRU 6 TOWARD K4.
5. INSULATE LEADS OF ITEMS 22, 23, 35 & 36 USING ITEM 29 PRIOR TO ASSEMBLY.
6. SILVER SCREW IS ALWAYS "W", BRASS SCREW ALWAYS "X".

LAL	REV.	DESCRIPTION	CHK	DATE	APPROVED
		REVISIONS 137529 M			
X	E	SEE REV. E.O. SH. 1 ADDED: ITEM (12) SH.2 ITEM (12) WAS. 2 REQ'D; ADDED: ITEM (28).(VIEW A-A) & M/L RELEASED TO MFG ON REV. D	CB	[illegible]	[illegible]
X	F	SEE REV E.O. [illegible] ADDED ITEMS [illegible] ADDED DETAIL [illegible] REV'D NOTE 5	[illegible]	[illegible]	[illegible]
	G	SEE DCP No 42808, ITEM 30 REV LTR WAS E	[illegible]	[illegible]	[illegible]
	H	SEE REV E.O.; REV'D DETAIL "E" & ADDED NOTE 6	[illegible]	[illegible]	[illegible]
	J	SEE REV E.O.; NOTE 1 ON F.D. WAS FARSIDE SHT 1 ZONE 3A; REVISED VIEW F-F.	[illegible]	[illegible] 70	T. Bailey 6-11-70
	K	SEE REV E.O.	[illegible]	[illegible]	[illegible]
X	L	SEE REV E.O.; FMK# 7202-03/10, 7203-03/09, 7204-02/07, 7212-01/09, 7232-01/10.	CB	3/1/[illegible]	[illegible]
	M	SEV REV. E.O.	CB	12/3/71	J.N. [illegible]



XDS Xerox Data Systems Formerly Scientific Data Systems

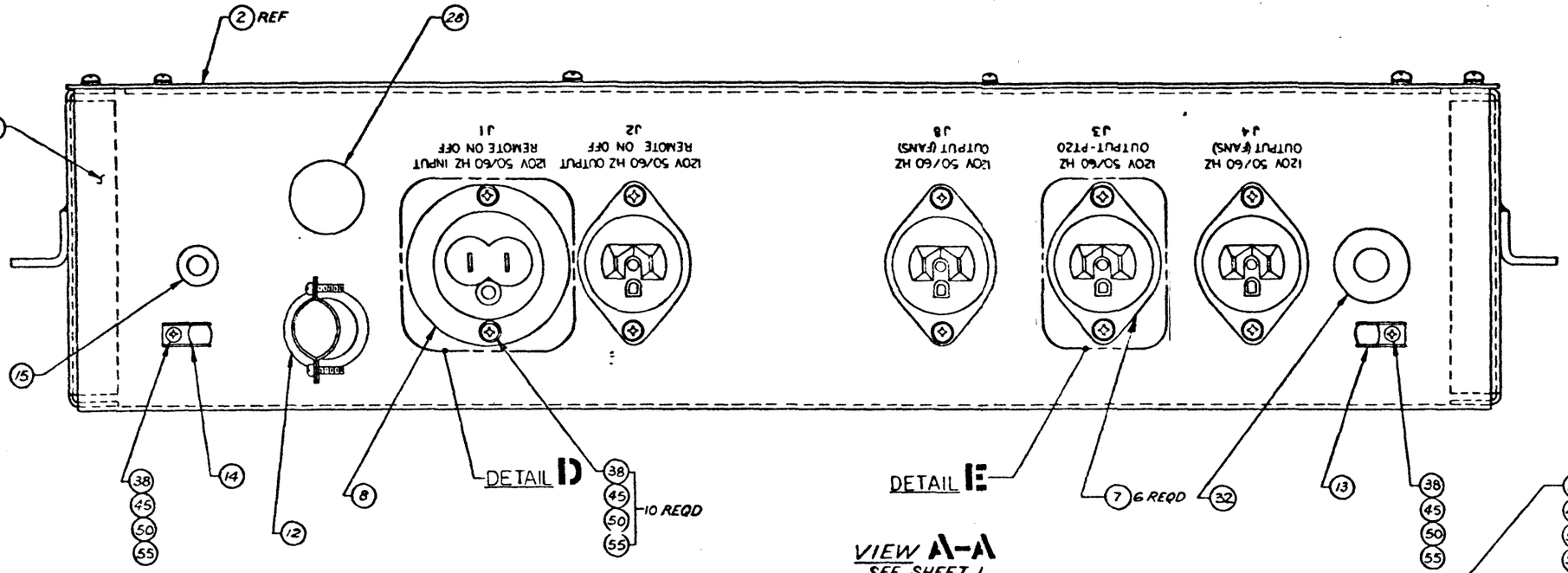
DIST CODE 401

MATERIAL LIST

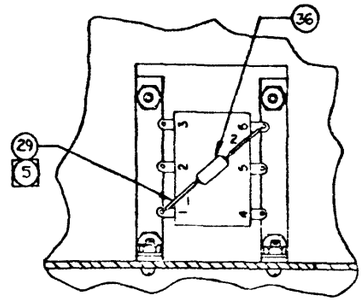
NOTES UNLESS SPECIFIED				
1. TOLERANCES .XX ±.030 .XXX ±.010 ANGULAR ±1/2°	DRAWN	E. [illegible]	6-15-67	SDS SCIENTIFIC DATA SYSTEMS SANTA MONICA, CALIFORNIA
2. BREAK ALL SHARP EDGES .010 APPROX.	CHECK	[illegible]	[illegible]	TITLE ASSEMBLY, DISTRIBUTION PANEL
3. MACH. SURFACES	APPR.	[illegible]	6-23-67	
4. ALL DIM. IN INCHES	MATERIAL			
MODEL NO. FIRST USE 7212	FINISH			SIZE D · DWG. NO. 137529 · CHANGE LETTER M
NEXT ASSY. FIRST USE 137528				SCALE — · DO NOT SCALE DRAWING · SHEET 1 of 4

137529 M

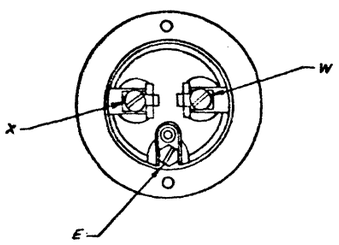
REVISIONS				137529 M
REV.	DESCRIPTION	CHK	DATE	APPROVED
	SEE SHEET ONE			



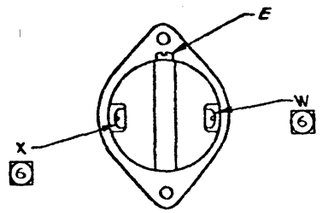
VIEW A-A
SEE SHEET 1



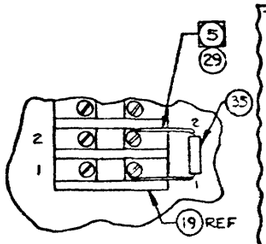
DETAIL H-H
SEE SHEET 1



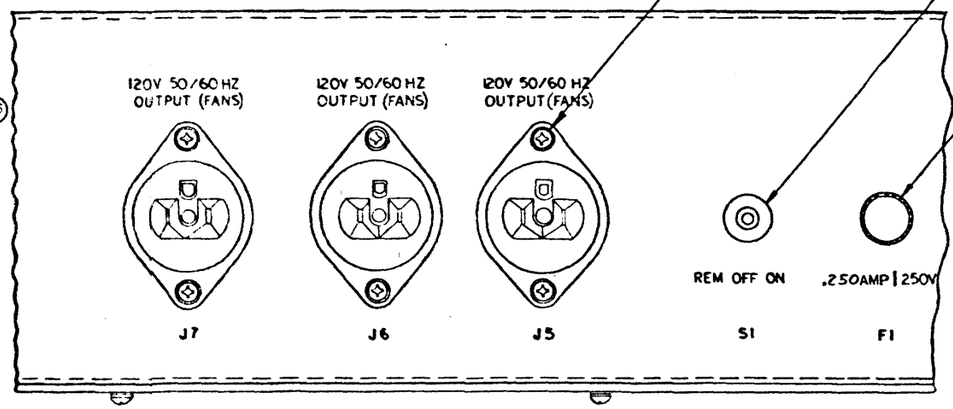
DETAIL D
J1
(REAR VIEW)



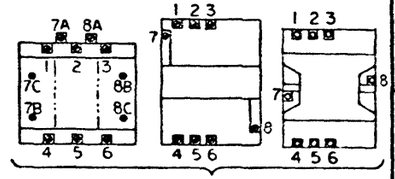
DETAIL E
J2,J3,J4,J5,J6,J7
(REAR VIEW)



DETAIL J
SEE SHEET 1

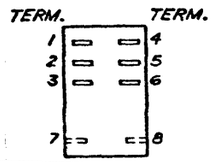


VIEW F-F
SEE SHEET 1

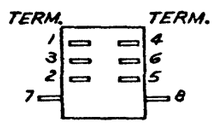


SELECT APPLICABLE
CONFIGURATION FROM THOSE
SHOWN

DETAIL G
SCALE: NONE
SEE SHEET 1



DETAIL B
K3
SEE SHEET 1



DETAIL C
K4
SEE SHEET 1

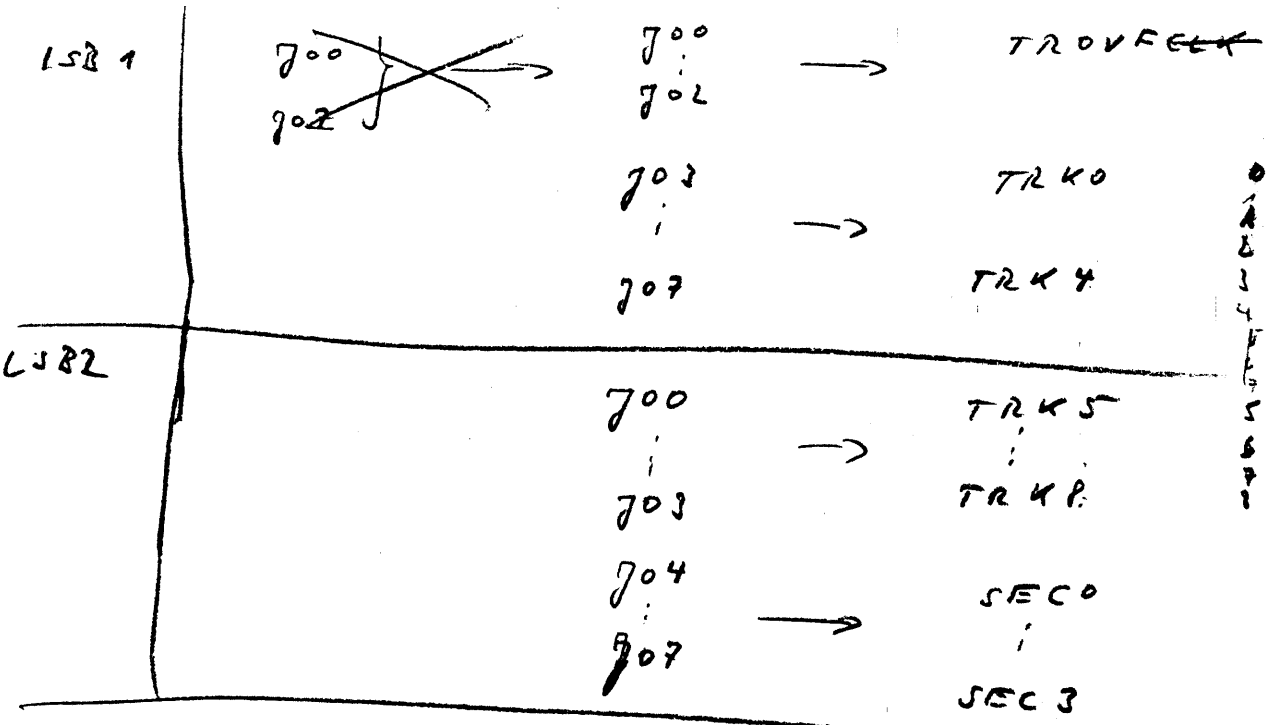
XDS Xerox Data Systems Formerly Scientific Data Systems

DIST CODE 401

MATERIAL LIST				
NOTES UNLESS SPECIFIED	DRAWN	L. Stringer	6-15-67	SDS SCIENTIFIC DATA SYSTEMS SANTA MONICA, CALIFORNIA
1. TOLERANCES .XX ±.010 .XXX ±.005 ANGULAR ±1°	CHECK	A. Bates	7/27/67	
2. BREAK ALL SHARP EDGES .010 APPROX.	APPR.	E. M. Clark	6-28-67	TITLE ASSEMBLY, DISTRIBUTION PANEL
3. FINISH SURFACES 7	MATERIAL			
4. ALL DIM. IN INCHES	FINISH			
MODEL NO. FIRST USE 7212				SIZE D DWG. NO. 137529 CHANGE LETTER M
NEXT ASSY. FIRST USE 137528				SCALE 1:1 DO NOT SCALE DRAWING SHEET 2 of 4

137529 M

3 2 1


LSB 1
700
702
700
702
TROVFELK
703
707
TRK0
TRK4
LSB2
700
703
704
707
TRK5
TRKP
SEC0
SEC3
DATA SW
TR/SEC
0 10 20 30 40 50 60 70
0 1
0
10
20
30
40
50
60
70
80
90
A0
B0
C0
D0
E0
F0
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110
120
130
140
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181
191
1A1
1B1
1C1
1D1
1E1
1F1
198 höchste Adresse