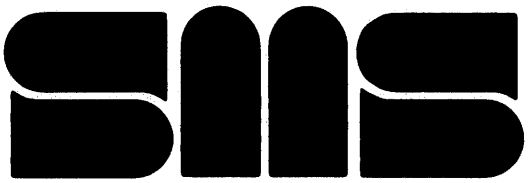

OMTI 5050
PROGRAMMABLE DATA SEQUENCER
REFERENCE MANUAL
JUNE 20th, 1986

Scientific Micro Systems, Inc.

OMTI 5050
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PUBLICATION NUMBER: **3001222**

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PROGRAMMABLE DATA SEQUENCER

REFERENCE MANUAL

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TABLE OF CONTENTS

SECTION 1

INTRODUCTION

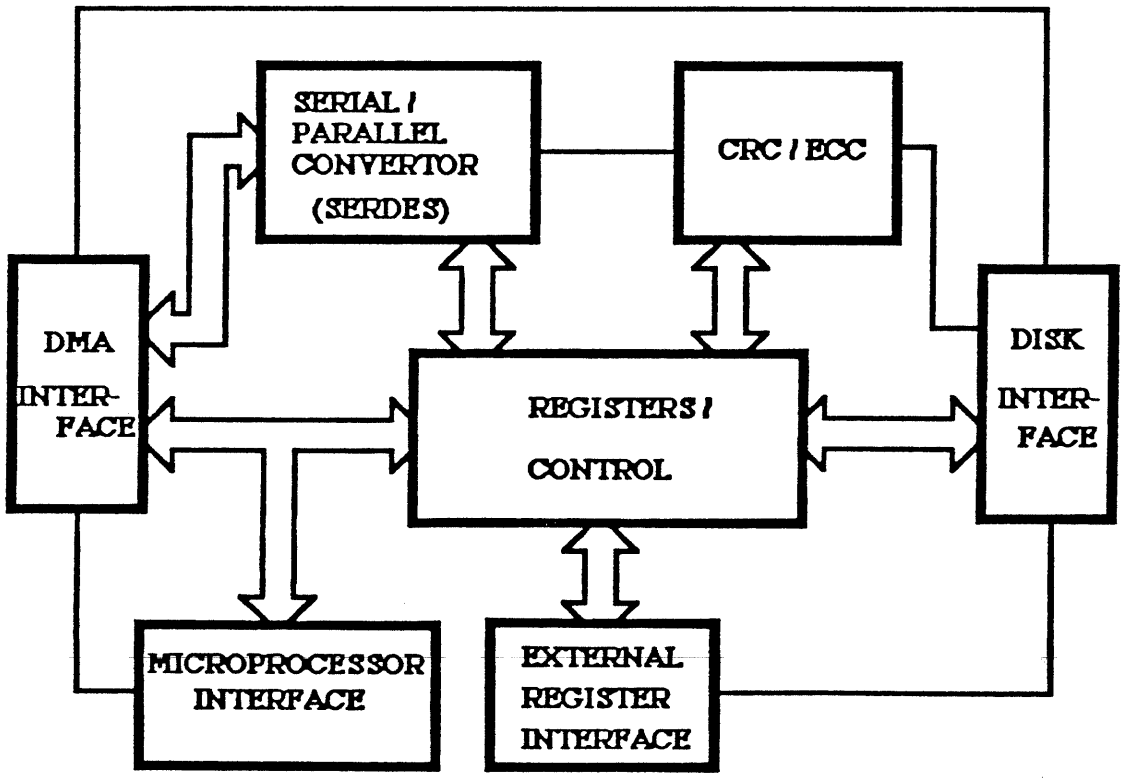
1.1 DESCRIPTION

The OMTI 5050 Programmable Data Sequencer is an application specific CMOS/VLSI integrated circuit mounted in a 68-pin plastic leaded chip carrier. The OMTI 5050 manages the flow of block-level information between serial disk interfaces and a host or buffer memory in advanced Winchester disk controller designs.

A dual-bus structure is used so the disk data transfers and the micro-processor can be operating at the same time without impacting the disk transfer rate or the performance of the micro-processor.

The OMTI 5050 is designed to be used with the OMTI 5060 Direct Memory Access Controller (DMAC), a RAM buffer, a byte oriented micro-processor, and appropriate drivers and receivers. The Data Sequencer can also be used with the OMTI 5070 MFM/Encode/Decode/VCO chip or the OMTI 5027 2-7/Encode/Decode/VCO chip to provide all the functions needed to interface to disk drives using MFM or 2-7 encoded data.

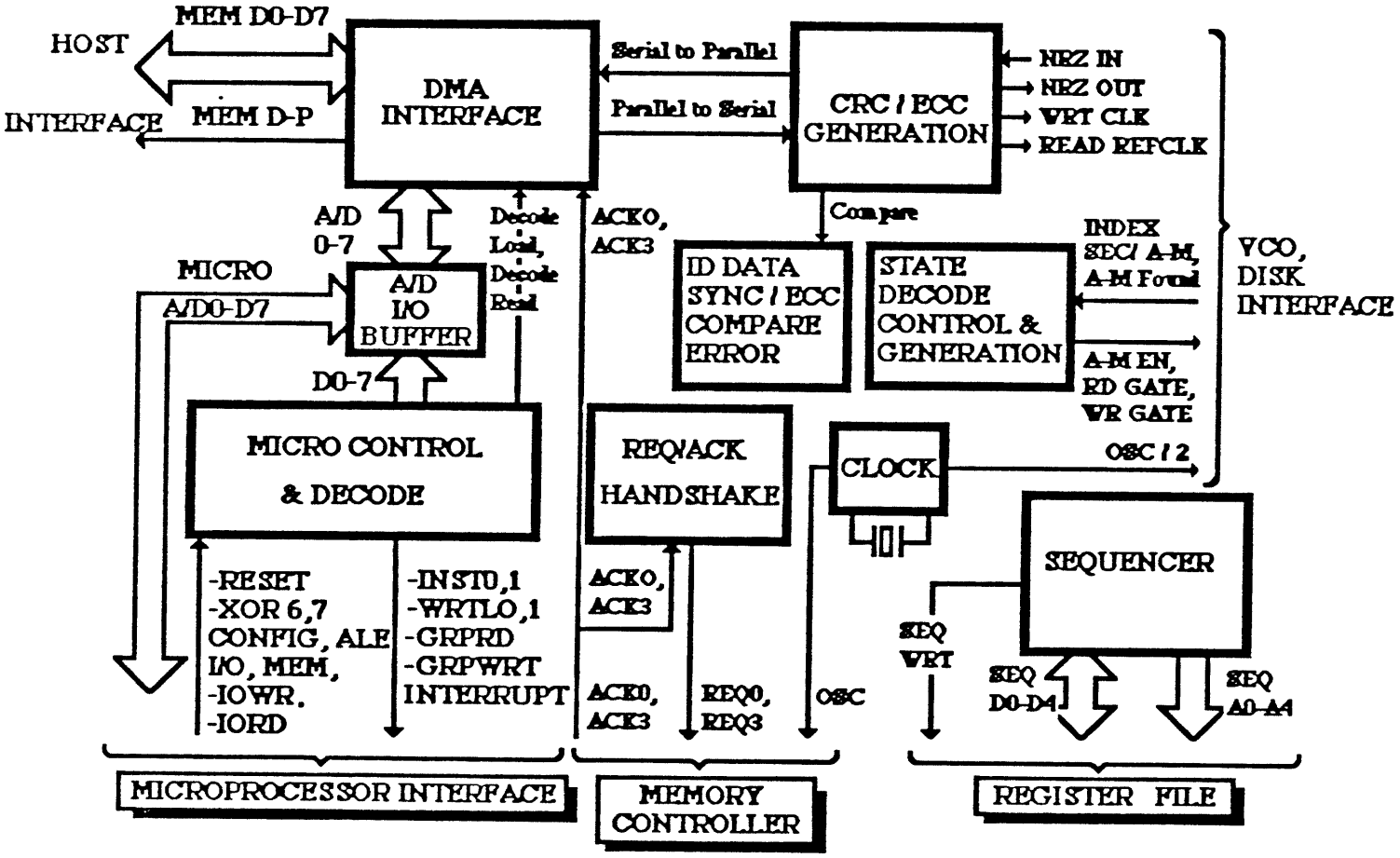
The Data Sequencer provides the bit-serial data management, format control, error detection, and serialization/de-serialization functions normally associated with data controllers. The chip is designed to be used directly with NRZ interfaces such as ESDI. (Enhanced Standard Drive Interface) When used with the OMTI 5070 or OMTI 5027 chips, it provides all the control lines required for MFM or 2-7 interfaces such as ST-506 or ST-412 and ST-238 drives.



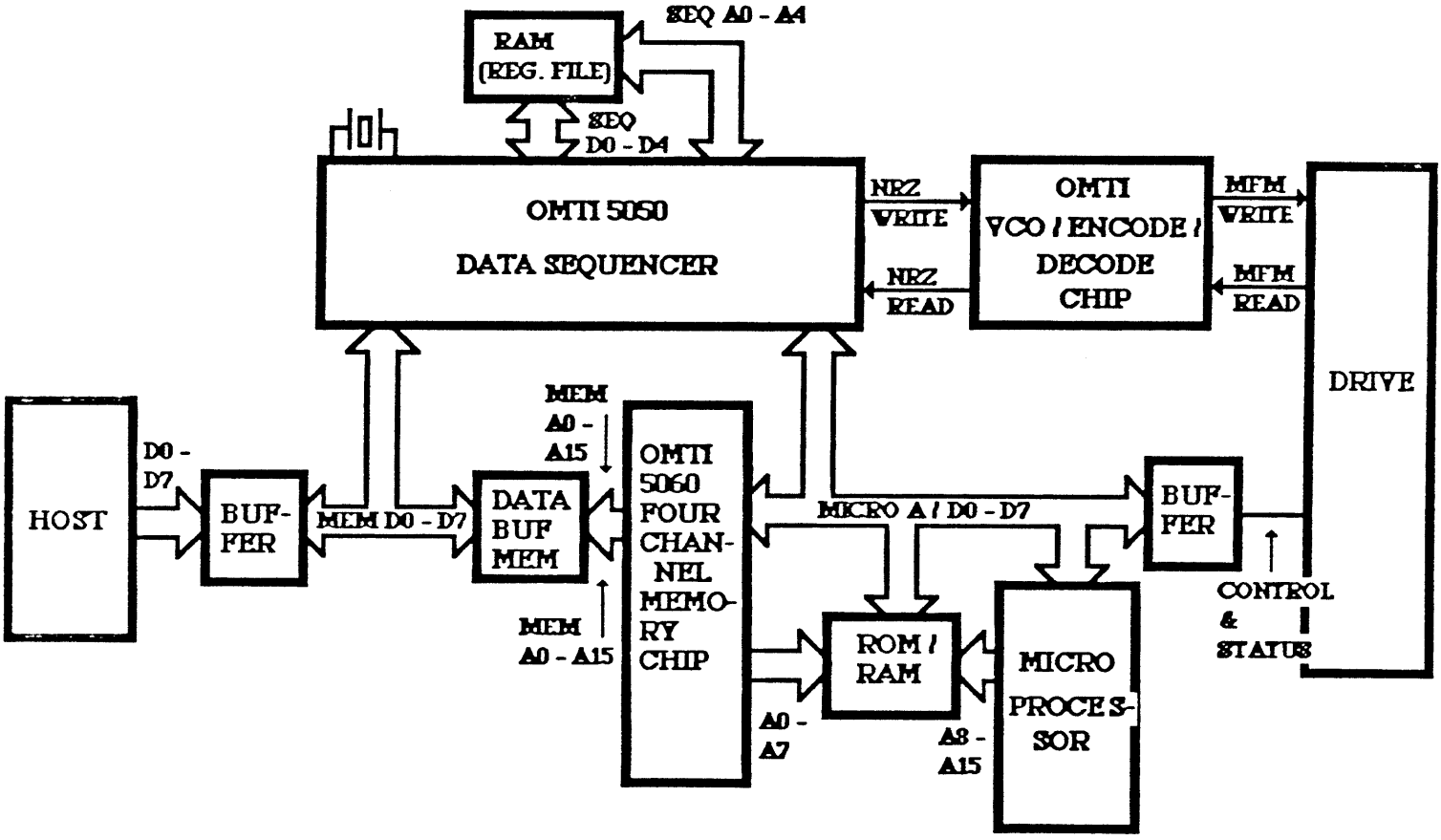
CONCEPTUAL BLOCK DIAGRAM

1.2 FEATURES

* High Performance Dual-Bus Architecture.
* High-level Instruction Set including :
  - Individual Sector Formatting.
  - Track Formatting.
  - Read ID.
  - Read/Write Long.
  - Read Syndrome.
  - Verify (with data in buffer).
  - Check Data ECC.
  - Check Track Format
* 10 MHz bit rate--up to 10 Mbit/sec Drive Data Transfer Rate.
* Programmable Disk Format.
  - Programmable Sector Size up to 65,536 bytes/sector.
  - Programmable ID Data and Size.
  - Programmable Gap Sizes and Fill Characters.
  - User-definable Header Flag Byte or Nibble.
  - Up to 64-bit Programmable (ECC) Polynomial and ID CRC or ECC.
* Hard or Soft Sector Modes.
* NRZ Serial Disk Interface.
* Direct Interface to ESDI Type Drives.
* Multi-sector Transfer capability with Automatic Sector Increment.
* Programmable Automatic ID Retries.
* Surface-mount Plastic 68-pin Leaded Chip Carrier Package.
* Low Power Consumption.
* Strobe Logic to access External Registers on the Micro Bus.
* Logic to Transfer Data between the Micro Bus and Buffer Memory.



FUNCTIONAL BLOCK DIAGRAM



TYPICAL SYSTEM CONFIGURATION

1.3 D. C. INFORMATION

1.3.1 Absolute Maximum Ratings:

* Voltages on all pins with respect to GND range from -0.3 V to +7.0 V.

* Ambient operating temperature is 0 degrees C. to +70 degrees C.

* Storage temperature ranges from -65 degrees C. to +150 degrees C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

1.3.2 Standard Test Conditions :

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows.

* +4.50 V < VCC < +5.50 V

* GND = 0 V

* 0 degrees C. < TA < +70 degrees C.

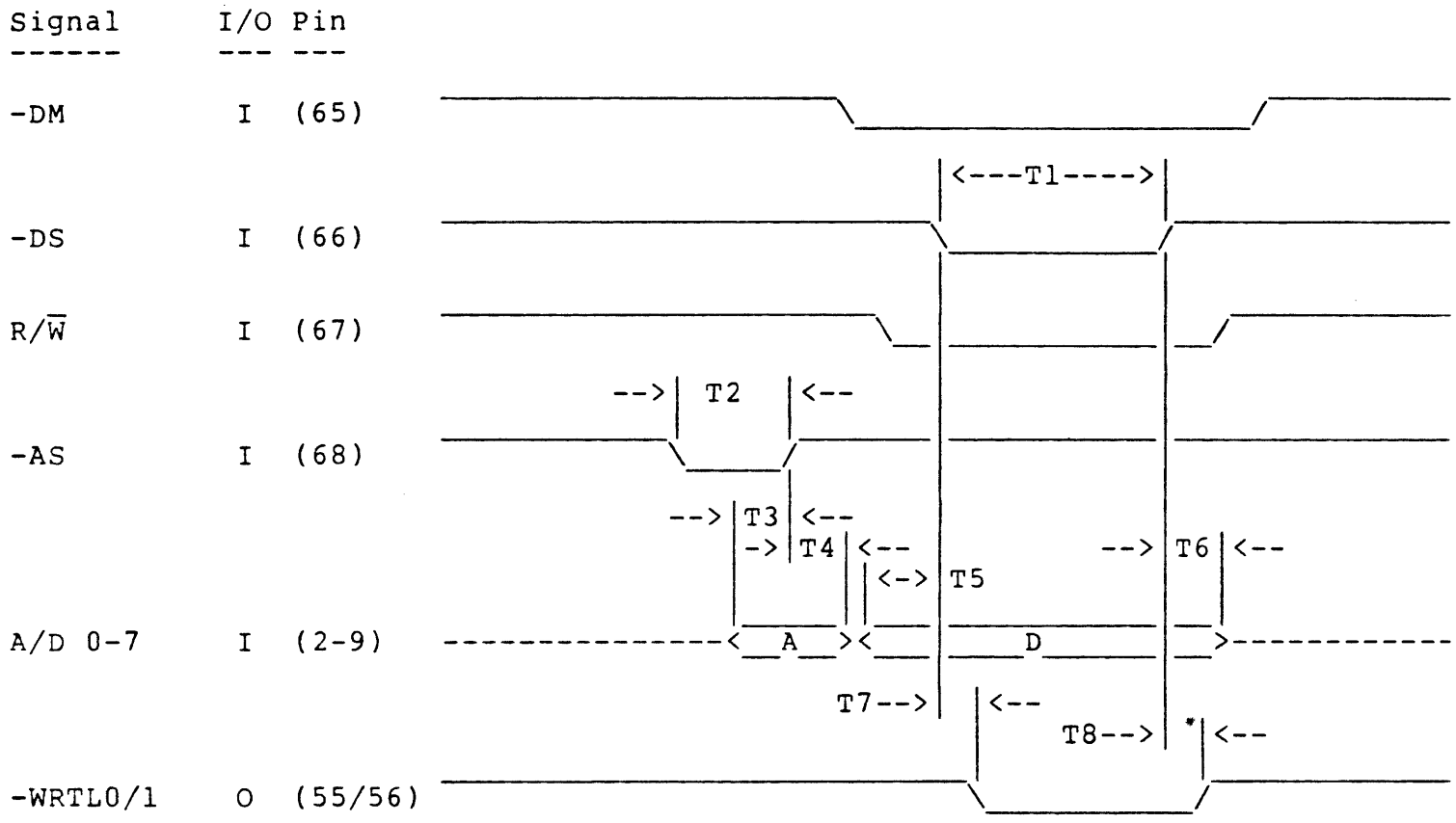
1.3.3 D. C. Characteristics :

Parameter	Min	Max	Unit	Condition	Notes
Input High Voltage	2	VCC	V		
Input Low Voltage	-0.3	0.8	V		
Output High Voltage	2.4	VCC	V		
Output Low Voltage		0.4	V		
Output Low Current	4.0		mA		
Output High Current	-4.0		mA		
Input Leakage	-30	10	uA		
Output Leakage		10	uA		
VCC Supply Current		50	mA		

1.4 A.C. CHARACTERISTICS

The two relevant timing diagrams and A.C. characteristics for interfacing the 5050 Data Sequencer are given below. (For more information about these chips, the reader is referred to :
- Zilog's Z8681/82 ROMless Z8 Microcomputer Product Specification
- or Intel's 8051 Single Chip 8-Bit N-Channel Microprocessor Data Sheet.

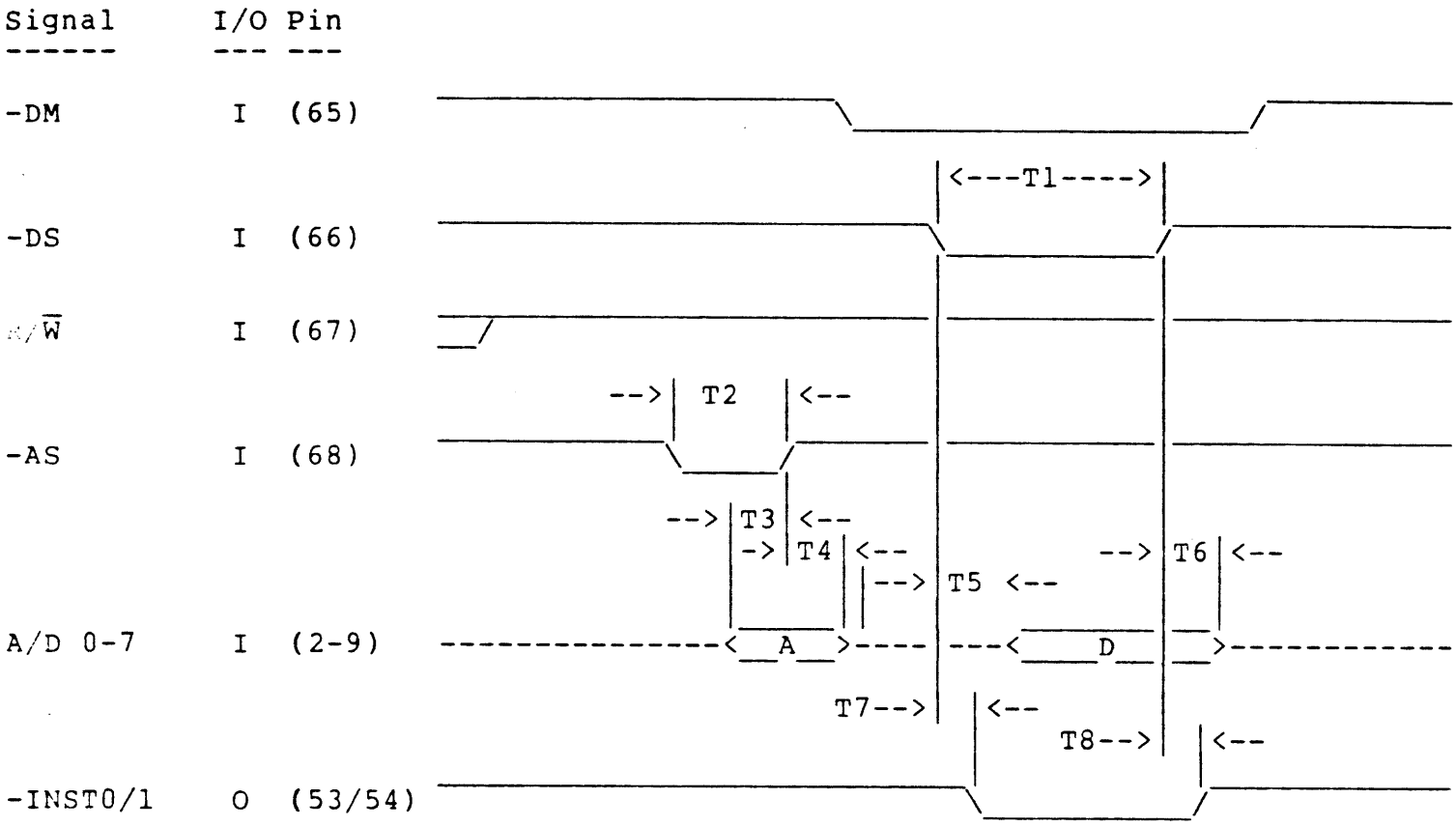
1.4.1 WRITE Operation , Z8 Configuration (Configuration = 1)



VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	-DS Low Pulse Width	100			ns
T2	-AS Low Pulse Width	50			ns
T3	Address Setup to -AS Low to High	25			ns
T4	Address Hold after -AS Low to High	25			ns
T5	Data Setup to -DS High to Low	25			ns
T6	Data Hold After -DS Low to High	25			ns
T7	-DS High to Low to -WRLT0/1 High to Low		25		ns
T8	-DS Low to High to -WRLT0/1 Low to High		25		ns

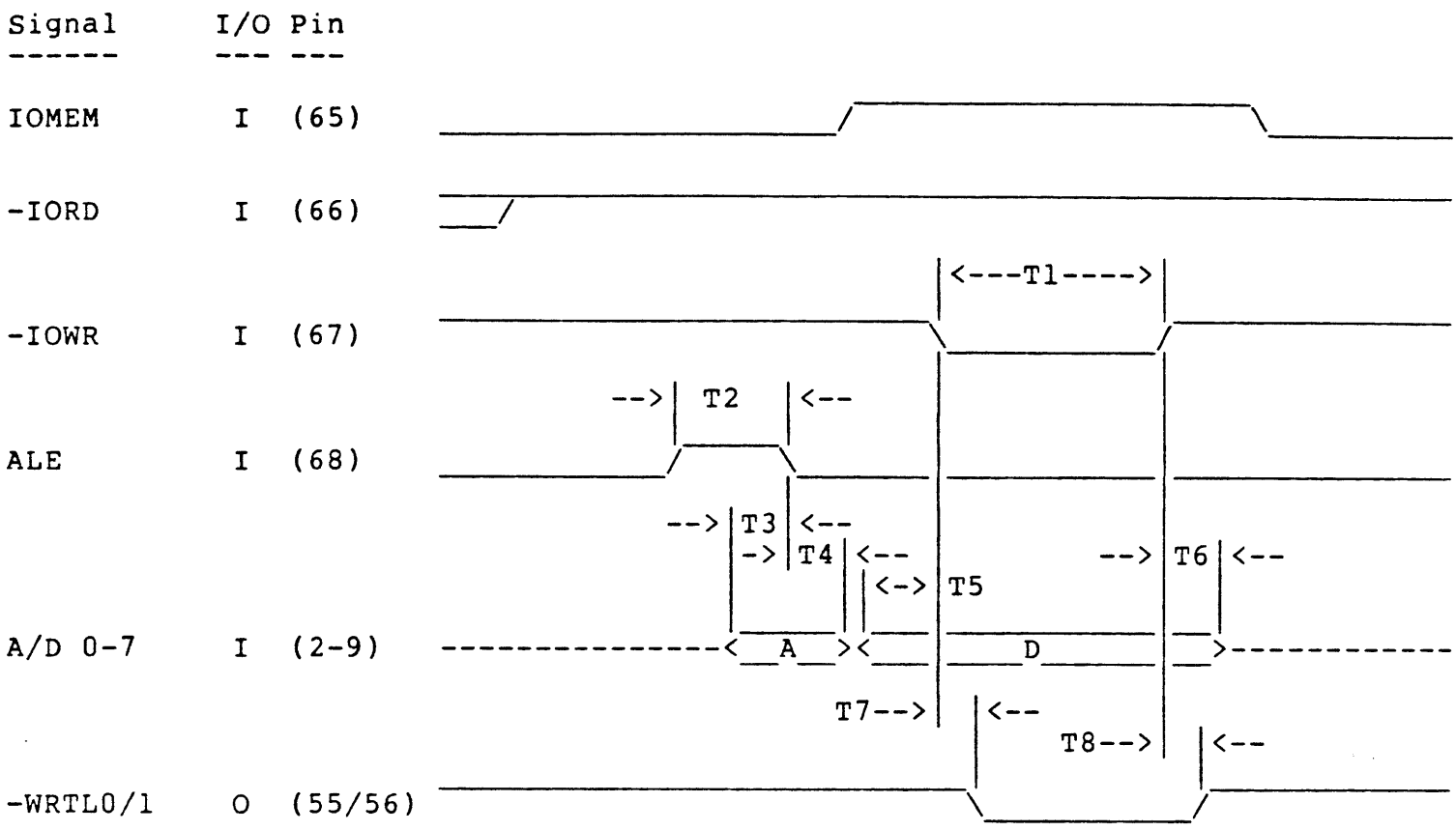
1.4.2 READ Operation, Z8 Configuration (Configuration = 1)



VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	-DS Low Pulse Width	100			ns
T2	-AS Low Pulse Width	50			ns
T3	Address Setup to -AS Low to High	25			ns
T4	Address Hold after -AS Low to High	25			ns
T5	Data Valid from -DS High to Low			50	ns
T6	Data Float After -DS Low to High		35		ns
T7	-DS High to Low to -INST0/1 High to Low		25		ns
T8	-DS Low to High to -INST0/1 Low to High		25		ns

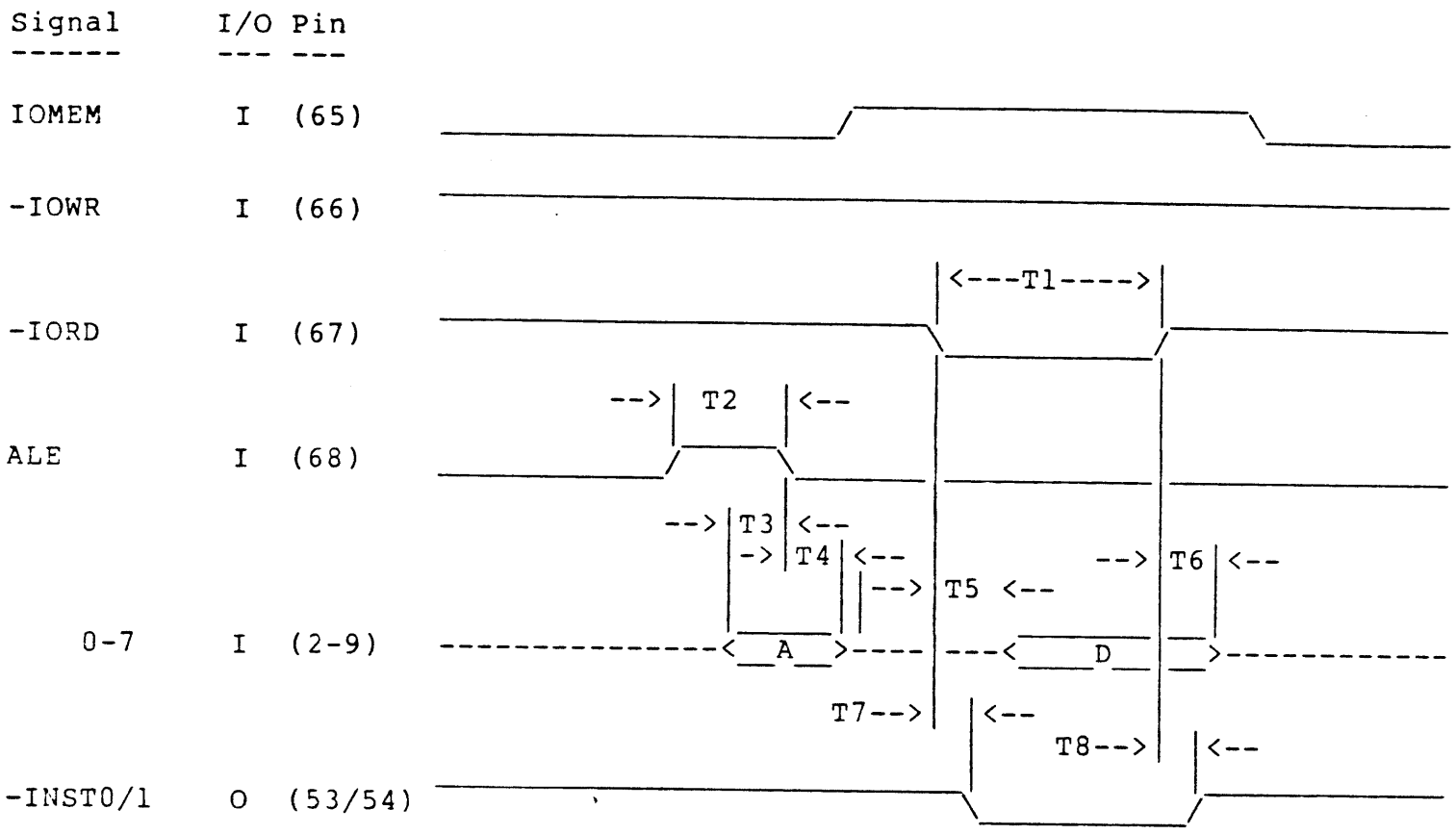
1.4.3 WRITE Operation , 8051 Configuration (Configuration = 0)



VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	-IOWR Low Pulse Width	100			ns
T2	ALE High Pulse Width	50			ns
T3	Address Setup to ALE High to Low	25			ns
T4	Address Hold after ALE High to Low	25			ns
T5	Data Setup to -IOWR High to Low	25			ns
T6	Data Hold After -IOWR Low to High	25			ns
T7	-IOWR High to Low to -WRLT0/1 High to Low		25		ns
T8	-IOWR Low to High to -WRLT0/1 Low to High		25		ns

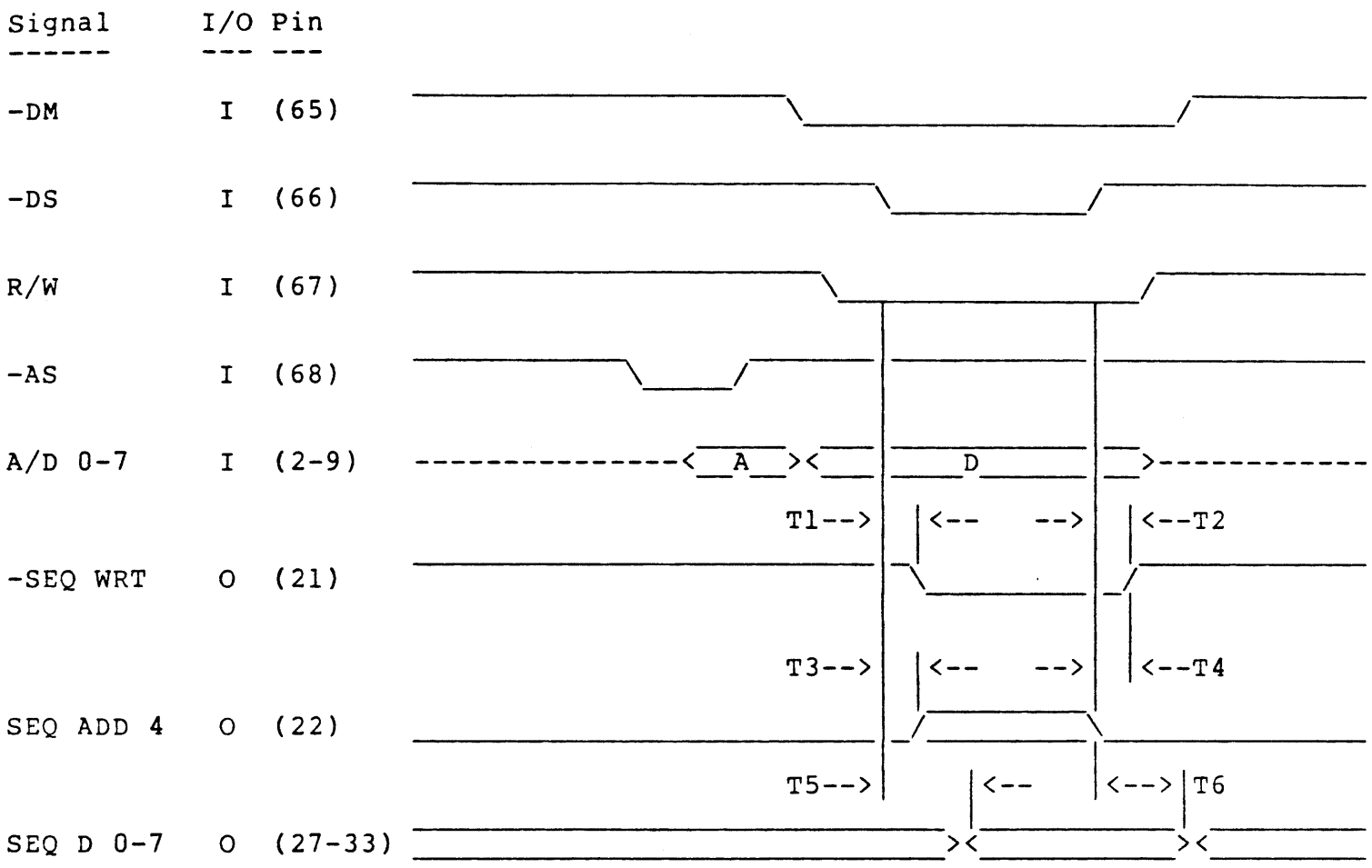
1.4.4 READ Operation, 8051 Configuration (Configuration = 0)



VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	-IORD Low Pulse Width	100			ns
T2	ALE High Pulse Width	50			ns
T3	Address Setup to ALE High to Low	25			ns
T4	Address Hold after ALE High to Low	25			ns
T5	Data Valid from -IORD High to Low			50	ns
T6	Data Float After -IORD Low to High		35		ns
T7	-IORD High to Low to -INST0/1 High to Low		25		ns
T8	-IORD Low to High to -INST0/1 Low to High		25		ns

1.4.5 SEQUENCER REGISTER LOAD Operation

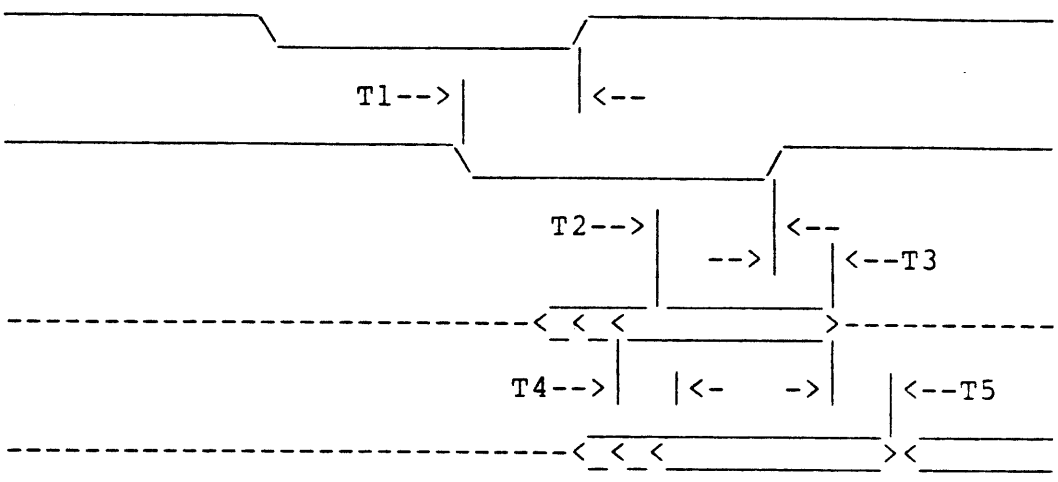


VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	-DS High to Low to -SEQ WRT High to Low		40		ns
T2	-DS Low to High to -SEQ WRT Low to High		40		ns
T3	-DS High to Low to SEQ A 4 Address Valid		40		ns
T4	-DS Low to High to SEQ A 4 Address Invalid		40		ns
T5	-DS High to Low to SEQ D 0-7 data Valid		35		ns
T6	-DS Low to High to SEQ D 0-7 Data Invalid		35		ns

1.4.6 DMA REQUEST / ACKNOWLEDGE HANDSHAKE

Signal	I/O	Pin
-REQ 0/3	O	(44/46)
-ACK 0/3	I	(45/47)
MEM D 0-7	I	(36-43)
MEM D P	O	(63)

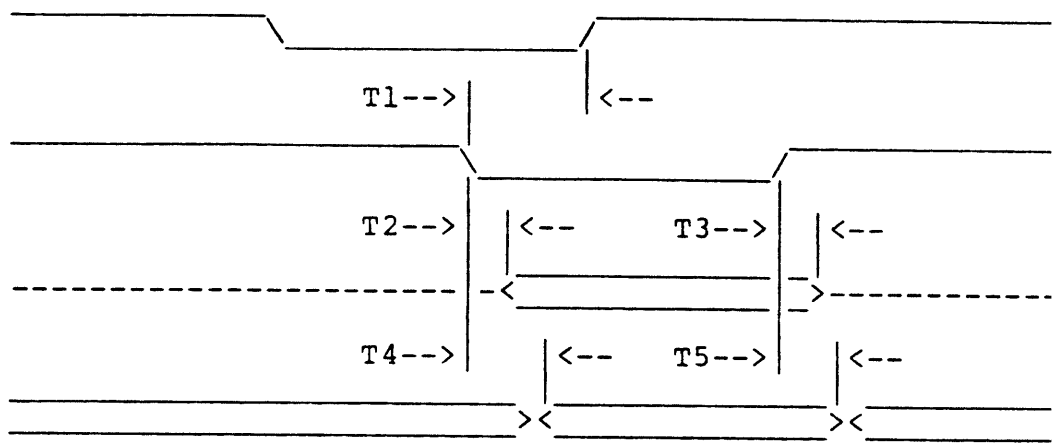


VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	-ACK High to Low to -REQ Low to High	45		ns	
T2	MEM D 0-7 Setup to -ACK Low to High	15			ns
T3	MEM D 0-7 Hold from -ACK Low to High	10			ns
T4	MEM D 0-7 Valid to MEM D P Valid		40		ns
T5	MEM D 0-7 Invalid to MEM D P Invalid		10		ns

1.4.7 DISK / MPU TO DMA MEMORY

Signal	I/O	Pin
-REQ 0/3	O	(44/46)
-ACK 0/3	I	(45/47)
MEM D 0-7	O	(36-43)
MEM D P	O	(63)



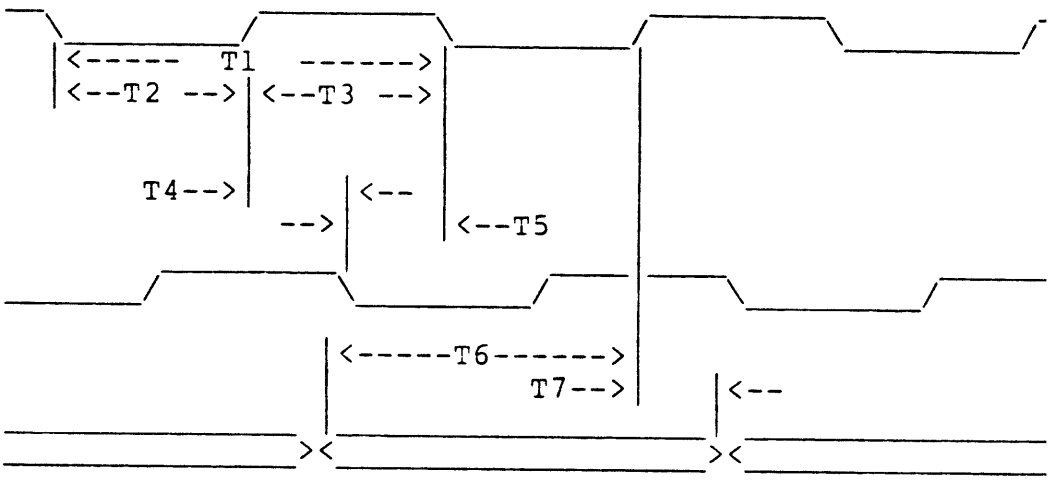
VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	-ACK High to Low to -REQ Low to High		45		ns
T2	-ACK High to Low to MEM D 0-7 Valid		15		ns
T3	-ACK Low to High to MEM D 0-7 Invalid		10		ns
T4	MEM D 0-7 Valid to MEM D P Valid		40		ns
T5	MEM D 0-7 Invalid to MEM D P Invalid		10		ns

1.4.8 DISK INTERFACE SIGNALS

1.4.8.1 READ DATA SIGNALS

Signal	I/O	Pin
RD REF CLK	I	(19)
WRT CLK	O	(15)
NRZ IN	I	(17)

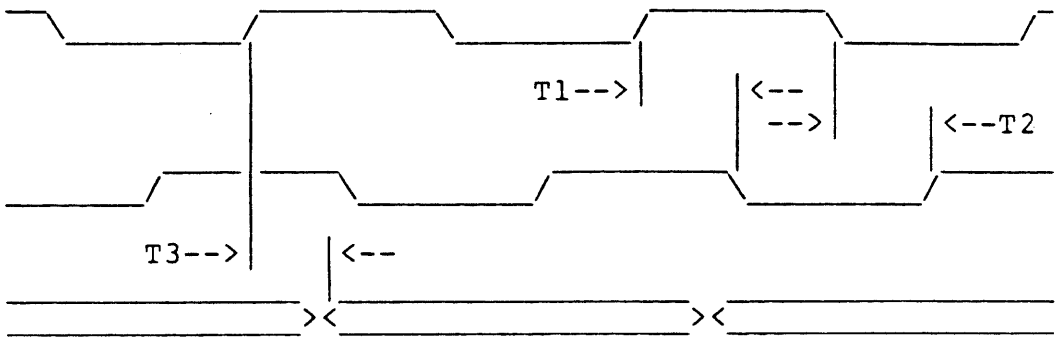


VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	RD REF CLK Period	100			ns
T2	RD REF CLK Low Width	50			ns
T3	RD REF CLK High Width	50			ns
T4	RD REF CLK High to WRT CLK Low Delay		45		ns
T5	RD REF CLK Low to WRT CLK High Delay		45		ns
T6	NRZ IN Data Setup to RD REF CLK	20			ns
T7	NRZ IN Data Hold from RD REF CLK	10			ns

1.4.8.2 WRITE DATA SIGNALS

Signal	I/O	Pin
RD REF CLK	I	(19)
WRT CLK	O	(15)
NRZ OUT	O	(16)



VCC = 5.0V, TA = 25oC

Symbol	Item	min	typ	max	unit
T1	RD REF CLK High to WRT CLK Low Delay		45		ns
T2	RD REF CLK Low to WRT CLK High Delay		45		ns
T3	RD REF CLK Low to High to NRZ OUT Delay		50		ns

Multiplication factors to convert from nominal environment:

Process	+1 std. deviation	1.35
	-1 std. deviation	0.65
Voltage	4.75V	1.06
	5.25V	0.95
Temperature	0oC	0.93
	70oC	1.15

SECTION 2

2.1 INTRODUCTION

The OMTI 5050's basic function is to manage the translation of a serial bit stream from a high-speed Winchester disk into parallel bytes of data that are transferred to a buffer or host memory. The transfer across the memory bus is handled by a DMA Controller, such as the OMTI 5060B DMAC chip.

The OMTI 5050 is very versatile and can be initialized to match the unique hardware requirements of different disk drives. It is initialized by writing :

- the **24 internal Transfer Control registers**
- and **32 external State Control registers.**

The micro-processor can read **12 Transfer Control Status registers** at any time, even while a transfer is in progress, to determine the status of the Data Sequencer.

The State Control registers reside in the State Control ROM or RAM. If in a RAM, they are initialized by the local micro-processor.

The Data Sequencer also has logic to transfer data from the micro-processor bus to the DMA bus, under micro-processor control, strobe logic to address external registers and an input for a crystal oscillator with a OSC and OSC/2 output.

The OMTI 5050 is designed to be used with the OMTI 5060 DMA Controller, a RAM buffer and a byte-oriented micro-processor. The chip has a configuration input line to match its micro-processor interface timing to Z8 or 8051-type micro-processors.

2.2 INTERFACES

2.2.1 Micro-Processor Interface

The micro-processor interface contains logic to allow the local micro-processor to directly read or write the Transfer Control registers. The micro-processor bus is an 8-bit address/data bus. The control line timing can be set up for Z8- or 8051-type micro-processors. (Refer to the Timing diagrams and Pin Descriptions for details.)

The Data Sequencer has logic to allow the micro-processor to read or write the buffer memory and to read or write the external State Control registers through the micro-processor interface. The Data Sequencer also has logic to handle transfers from a peripheral on the micro-processor bus to the buffer memory under micro-processor control. The buffer memory to micro-processor bus transfers use channel 3 of the DMAC.

2.2.2 DMA Interface

The DMA interface is used to transfer bytes of data between the Data Sequencer and buffer memory. The transfers are under the control of the DMA controller chip. Channel 0 is used for transfers between the buffer and the disk, and channel 3 is used for transfers between the micro-processor bus and the buffer memory.

2.2.3 State Control Register Interface

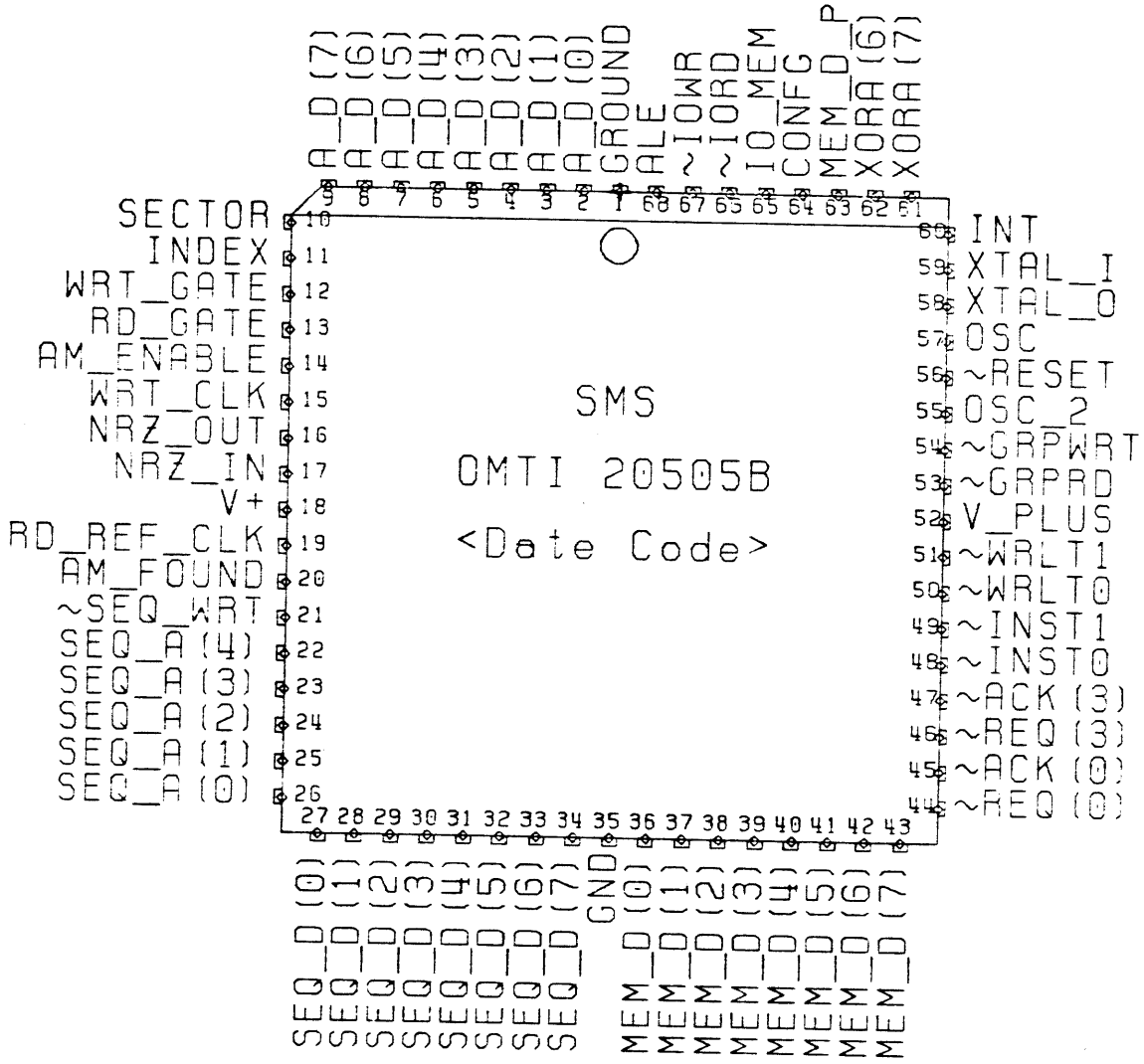
The state control interface is used for writing and reading the State Control parameters.

2.2.4 Serial Disk Interface

The disk interface logic contains the control and status lines for the disk itself, including the serial data stream.

2.2.5 Clock

The Data Sequencer provides two clock outputs, OSC and OSC/2 that can be used by other circuits. The clock frequency is determined by an external crystal or clock source. The frequency of the oscillator is know function of the NRZ data rate.


SECTOR 10
INDEX 11
WRT_GATE 12
RD_GATE 13
AM_ENABLE 14
WRT_CLK 15
NRZ_OUT 16
NRZ_IN 17
V+ 18
RD_REF_CLK 19
AM_FOUND 20
~SEQ_WRT 21
SEQ_A(4) 22
SEQ_A(3) 23
SEQ_A(2) 24
SEQ_A(1) 25
SEQ_A(0) 26
9 8 7 6 5 4 3 2 1 68 67 65 65 64 63 62 61
AD(7) AD(6) AD(5) AD(4) AD(3) AD(2) AD(1) AD(0) GROUND ALE ~IOWR ~IORD IO_MEM CONFG MEM_DP XORA(6) XORA(7)
INT 60
XTAL_I 59
XTAL_O 58
OSC 57
~RESET 56
OSC_2 55
~GRPWRT 54
~GRPRD 53
V_PLUS 52
~WRLT1 51
~WRLT0 50
~INST1 49
~INST0 48
~ACK(3) 47
~REQ(3) 46
~ACK(0) 45
~REQ(0) 44
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
SEQD(0) SEQD(1) SEQD(2) SEQD(3) SEQD(4) SEQD(5) SEQD(6) SEQD(7) GND MEMD(0) MEMD(1) MEMD(2) MEMD(3) MEMD(4) MEMD(5) MEMD(6) MEMD(7)
SMS
OMTI 20505B
<Date Code>

2.3 PIN DESCRIPTIONS

Symbol	Type	Pin #	Name and Function
-ACK0 -ACK3	I	45 47	**DMA Memory Acknowledge. (Active Low.)** This input strobe is used to enable data from the sequencer in a write buffer memory operation, or to save data in the sequencer in a read buffer memory operation.
A/D0- A/D7	I/O	2-9	**Address/Data Bus. (Active High,3-state.)** These multiplexed lines interface with the low-order eight bits of the micro-processor's Address/Data bus. Addresses are latched into the address buffer on the falling edge of ALE. If the address is within the range of the internal chip select, data is either written into or read from the Data Sequencer registers, depending on whether -IOWR or -IORD is active.
ALE(8051 Mode) -AS(Z8 mode)	I	68	**Address Latch Enable. (Active High.)** **Address Strobe (Active Low.)** When in the 8051 mode, the falling edge of the signal is used to latch the address on the micro-processor bus (A/D-0-A/D7) into the internal address buffer. When in the Z8 mode, the rising edge is used to latch the address.
A-M ENABLE	O	14	**Address Mark Enable. (Active High.)** If ESDI mode is selected, this output is active at state 1 strobe time. This function is for writing the Address Mark to the disk. If ESDI mode is not selected, A-M ENABLE is active for state 3 and 9, and can be used for external encoding of the drop clock byte.
A-M FOUND	I	20	**Address Mark found. (Active High.)** This signal, an output from the VCO/Encode/Decode chip, and is used by the Data Sequencer for MFM or 2,7 byte synchronization. If internal synchronization is configured, this input should be grounded.
CONFIG	I	64	**Configuration. (Active High.)** This input signal is internally pulled-up and is used to select the micro-processor strobe inputs. When this line is grounded, the chip is configured for an 8051 type processor; when it is left open, the chip is configured for a Z8-type processor.
-GRPRD	O	53	**Group Read Strobe. (Active Low.)** This output is strobed whenever the micro-processor reads addresses RA3C, RA3D, RA3E or RA3F. It can be used to enable status onto the micro-processor bus (A/D0-7). This output can be used as an external peripheral chip select like an Intel 8255 PIO or 8273 FDC.

Symbol	Type	Pin #	Name and Function
-GRPWRT	O	54	**Group Write Strobe. (Active Low.)** This output is strobed whenever the micro-processor does a write to addresses WA3C, WA3D, WA3E or WA3F. It can be used to latch information from the micro-processor bus (A/D0-7) into an external register. This output can be used as an external peripheral chip select like an Intel 8255 PIO or 8273 FDC.
INDEX	I	11	**Index. (Active High.)** This signal from the disk is pulsed each revolution. The Data Sequencer uses the rising edge of this signal during formatting for synchronizing and for timing out commands.
-INST0 -INST1	O O	48 49	**In Status 0-1. (Active Low.)** These output strobes are internally decoded I/O read strobes (enabled by reading from RR38 or RR39, respectively), used by the micro-processor to read device status from an external tri-data buffer chip to the A/D bus.
INTERRUPT	O	60	**Interrupt. (Programmable.)** If enabled, this signal is asserted when the Busy status bit goes from 1 to 0 (Command complete). This output is deasserted when the micro-processor reads the Status register.
IO/-MEM (8051 mode) -DM(Z8 mode)	I	65	**I/O/-Memory (I/O Active High.)** **-Data Memory (Active Low.)** This signal is used for active high chip enable. When in 8051 mode, this line is connected to the 8051's IO/MEM line; in Z8 mode, this line is an active low chip enable.
-IORD(8051 mode)	I	66	**I/O Read. (Active Low.)** This input, when low, enables the information from the register selected by the previously latched address onto the micro-processor bus (A/D0-7).
-DS(Z8 mode)			**Data Strobe. (Active Low.)** This input, when low, provides the timing for data movement to or from selected registers and the micro-processor bus (A/D0-7).

Symbol	Type	Pin #	Name and Function
-IOWR (8051 mode) R/-W (Z8 mode)	I	67	**I/O Write. (Active Low.)** When this input is low, it gates information from the microprocessor bus (A/D0-7) into the register selected by the previously latched address. **Read/Write. (Active High.)** This signal determines the direction of the data transfer. When low, data is written from the micro-processor bus (A/D0-7) to the Data Sequencer. It is high when not doing writes.
MEM D0- MEM D7	I/O	36- 43	**I/O Memory Data. (Active High.)** This 8-bit bidirectional bus is used to transfer data to and from the DMA buffer memory. The MEM D (0-7) lines are driven by the 5050B when -ACK0 or -ACK3 are low, and the data direction is to the memory device.
MEM D-P	O	63	**Memory Data Parity. (Active High.)** This output line is a fall-through odd parity of the memory data bus. It allows parity checking to be performed on transfers to or from DMA buffer memory.
NRZ IN	I	17	**NRZ Data In. (Active High.)** This serial data input line is the NRZ read data from the : - OMTI 5070 Encode/Decode/VCO chip - or the OMTI 5027 2-7 Encode/Decode/VCO chip - or ESDI-type disk drive.
NRZ OUT	O	16	**NRZ Data Out. (Active High.)** When WRT GATE is active, this serial data output line transmits the serial data to the - OMTI 5070 Encode/Decode/VCO chip - or the OMTI 5027 2-7 Encode/Decode/VCO chip - or ESDI-type disk drive.
OSC	O	57	**Oscillator. (Active High.)** This is a TTL output and is at the XTAL frequency.
OSC/2	O	55	**Oscillator 2. (Active High.)** This signal is a free running clock at one-half the XTAL frequency.

Symbol	Type	Pin #	Name and Function
RD GATE	O	13	**Read Gate. (Active High.)** This output line is active during read commands. The OMTI 5070 or 5027 VCO/Encode/Decode chip must provide AM FOUND when the sequencer is in external sync mode.
RD/REFCLK	I	19	**Read/Reference Clock. (Active High.)** This input signal has two alternative functions. When RD GATE is true, this signal provides the read clock and is used to sample NRZ-IN. When WRT GATE is true, it is used to generate NRZ-OUT. A clock must always be present at this input.
-REQ0 -REQ3	O O	44 46	**DMA Request. (Active Low.)** These output lines are used by the sequencer to request the DMA controller to transfer data to or from the buffer memory. Channel 0 is used for disk data transfers. Channel 3 is used for transfers between the buffer memory and the micro-processor bus.
-RESET	I	56	**Reset. (Active Low.)** When active, this input signal resets RD GATE or WRITE GATE and puts the chip in a not-Busy mode.
SECTOR/ A-M FOUND	I	10	**Sec/A-M Found/Sync. (Active High.)** This line can be configured as either : - the Sector line in a hard-sectored drive, - or as the Address-Mark-Found input from an ESDI-type drive.
SEQ A0- SEQ A4	O	26- 22	**Sequencer Address. (Active High.)** The address lines SEQ A0-A3 select the sequencer's state (0 - 15); SEQ A4 selects the state's Count or Value field (Count = 1, Value = 0).
SEQ D0- SEQ D7	I/O	27- 34	**Sequencer Data. (Active High.)** The sequencer uses this 8-bit bidirectional data bus to access the external State Control register file.
-SEQ WRT	O	21	**Sequencer Write. (Active Low.)** This signal is active when the micro-processor is downloading the sequencer's external State Control register file (enabled by writing WA2E or WA2F).

Symbol	Type	Pin #	Name and Function
-WRTL0 -WRTL1	O O	50 51	**Write Latch 0-1. (Active Low.)** These outputs are internally decoded write strobes (enabled by writing to WA38 or WA39, respectively), used by the micro-processor to write device control information to an external register from the A/D0-7 bus.
WRT CLK	O	15	**Write Clock. (Active High.)** This signal is the NRZ Write Clock at the RD/REFCLK rate.
WRT GATE	O	12	**Write Gate. (Active High.)** This signal is asserted during disk write operations.
-XOR 6 -XOR 7	I I	62 61	**Exclusive OR Address. (Active Low.)** These internally pulled up signals are used for internal chip select. They control the polarity of the corresponding address lines. If another group chip select is required, the appropriate line must be grounded.
XTAL0- XTAL1	I/O	59- 58	**Crystal 0-1. (Active High.)** The XTAL lines may be connected to an external crystal oscillator to provide the OSC and OSC/2 outputs. If an external clock source is available, a clock input can be connected to the XTAL0 input, with the XTAL1 line left open. If a crystal is used, it must be a fundamental parallel resonant type, between the range of one to 20 Mhz.
VCC	I	52 18	**VCC. +5 V.**
GND	I	35 1	**Ground.**

2.4 REGISTERS

Registers on the OMTI 5050 Data Sequencer are of two types:

- **Transfer Control registers,** which are used to initiate and control data transfers and return status information. The Transfer Control registers are directly accessible by the micro-processor.

- **State Control registers,** which reside in the State Control ROM or RAM and hold the counts and values which define the format on the disk. The State Control parameters are used by the state sequencer for command execution. The external State Control registers are accessible through the Transfer Control registers.

TRANSFER CONTROL REGISTERS

WRITE REGISTERS	
Write	Functions
WR20	Command Register
WR21	Sequencer Loop Count
WR22	Index Time-Out
WR23	Sub-Block Count
WR24	Cylinder (High Byte)
WR25	Cylinder (Low Byte)
WR26	Head
WR27	Sector Number
WR28	Micro to Memory
WR29	Sequencer Start/Re-Start
WR2A	Sequencer Loop State
WR2B	Bit Ring Start Count
WR2C	ECC Control
WR2D	Configuration Control
WR2E	External Count Register
WR2F	External Value Register
WR30	Polynomial 63-56
WR31	Polynomial 55-48
WR32	Polynomial 47-40
WR33	Polynomial 39-32
WR34	Polynomial 31-24
WR35	Polynomial 23-16
WR36	Polynomial 15-8
WR37	Polynomial 7-0
WA38	Write Strobe 0
WA39	Write Strobe 1
WA3A	Reserved
WA3B	Reserved
WA3C	External Group Strobe
WA3D	External Group Strobe
WA3E	External Group Strobe
WA3F	External Group Strobe

READ REGISTERS	
Read	Functions
RR20	Status
RR21	Extended Status
RR22	Retry Count/State Address
RR23	Flag Byte
RR24	Cylinder (High Byte)
RR25	Cylinder (Low Byte)
RR26	Head/Flag
RR27	Sector Number
RR28	Memory to Micro
RR29	Loop Count
RR2A	Not Used
RR2B	Not Used
RR2C	Not Used
RR2D	Not Used
RR2E	External Count Register
RR2F	External Value Register
RR30	Not Used
RR31	Not Used
RR32	Not Used
RR33	Not Used
RR34	Not Used
RR35	Not Used
RR36	Not Used
RR37	Not Used
RA38	Read Strobe 0
RA39	Read Strobe 1
RA3A	Reserved
RA3B	Micro to Peripheral Transfer
RA3C	External Group Strobe
RA3D	External Group Strobe
RA3E	External Group Strobe
RA3F	External Group Strobe/ Peripheral to Micro Transfer

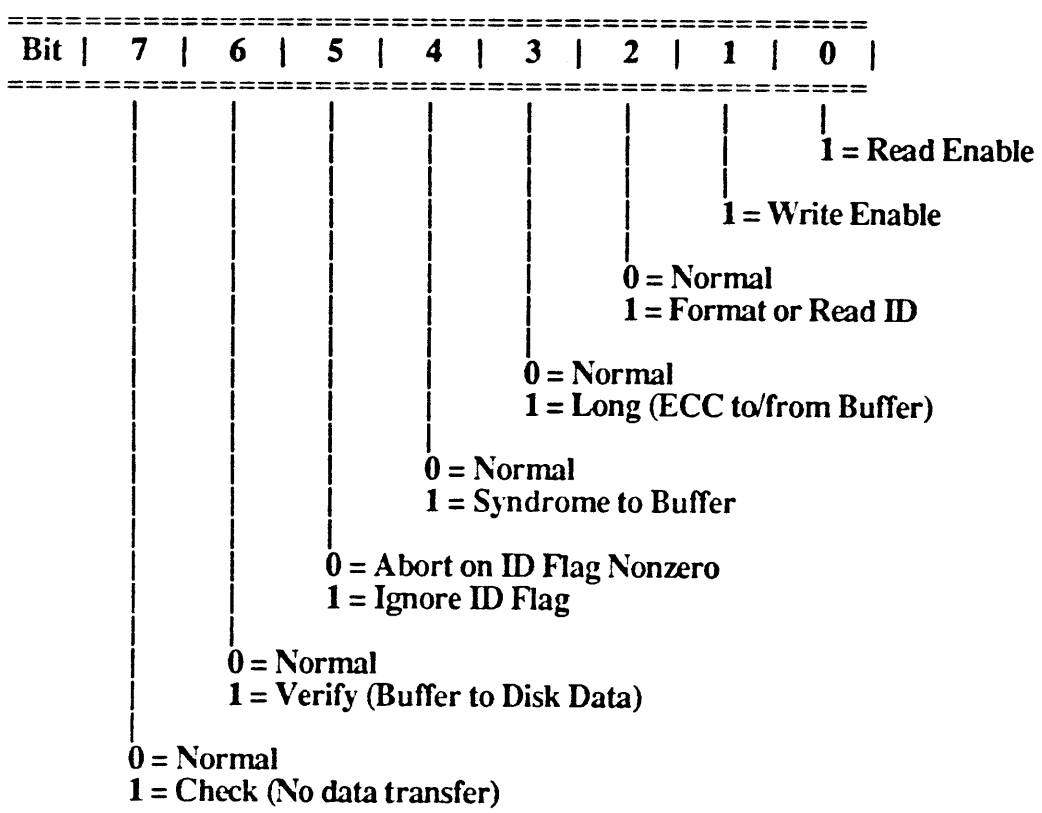
OMTI 5050 ADDRESS MAP

A/D7	A/D6	A/D5	A/D4	A/D3	A/D2	A/D1	A/D0	WRITE	READ
-XOR7	-XOR6	1	0	0	0	0	0	WR20	RR20
-XOR7	-XOR6	1	0	0	0	0	1	WR21	RR21
-XOR7	-XOR6	1	0	0	0	1	0	WR22	RR22
-XOR7	-XOR6	1	0	0	0	1	1	WR23	RR23
-XOR7	-XOR6	1	0	0	1	0	0	WR24	RR24
-XOR7	-XOR6	1	0	0	1	0	1	WR25	RR25
-XOR7	-XOR6	1	0	0	1	1	0	WR26	RR26
-XOR7	-XOR6	1	0	0	1	1	1	WR27	RR27
-XOR7	-XOR6	1	0	1	0	0	0	WR28	RR28
-XOR7	-XOR6	1	0	1	0	0	1	WR29	RR29
-XOR7	-XOR6	1	0	1	0	1	0	WR2A	NOT USED
-XOR7	-XOR6	1	0	1	0	1	1	WR2B	NOT USED
-XOR7	-XOR6	1	0	1	1	0	0	WR2C	NOT USED
-XOR7	-XOR6	1	0	1	1	0	1	WR2D	NOT USED
-XOR7	-XOR6	1	0	1	1	1	0	WR2E	RR2E
-XOR7	-XOR6	1	0	1	1	1	1	WR2F	RR2F
-XOR7	-XOR6	1	1	0	0	0	0	WR30	NOT USED
-XOR7	-XOR6	1	1	0	0	0	1	WR31	NOT USED
-XOR7	-XOR6	1	1	0	0	1	0	WR32	NOT USED
-XOR7	-XOR6	1	1	0	0	1	1	WR33	NOT USED
-XOR7	-XOR6	1	1	0	1	0	0	WR34	NOT USED
-XOR7	-XOR6	1	1	0	1	0	1	WR35	NOT USED
-XOR7	-XOR6	1	1	0	1	1	0	WR36	NOT USED
-XOR7	-XOR6	1	1	0	1	1	1	WR37	NOT USED
-XOR7	-XOR6	1	1	1	0	0	0	WA38	RA38
-XOR7	-XOR6	1	1	1	0	0	1	WA39	RA39
-XOR7	-XOR6	1	1	1	0	1	0	Reserved	Reserved
-XOR7	-XOR6	1	1	1	0	1	1	Reserved	RA3B
-XOR7	-XOR6	1	1	1	1	X	X	WA3C	RA3C
-XOR7	-XOR6	1	1	1	1	X	X	WA3D	RA3D
-XOR7	-XOR6	1	1	1	1	X	X	WA3E	RA3E
-XOR7	-XOR6	1	1	1	1	X	X	WA3F	RA3F

A/D7 through A/D0 are the micro-processor address/data lines.
-XOR7 and -XOR6 are internal chip selects (Active Low.)
Selection occurs when A/D7 = A/D6 = 0. The XOR signals are internally pulled up and should be grounded to invert the select.
X = Don't care.
WR = Write Register. **RR = Read Register.**
WA = Write Address. **RA = Read Address.**

2.4.1 WRITE REGISTERS

2.4.1.1 WRITE REGISTER 20_H : COMMAND



A write to the Command register initiates a command. The command is defined by the bit combination in this register and the other Data Transfer registers.

BIT 0:
When bit 0 is set (1), the operation is a read type command. Data is transferred from the disk to the buffer memory.

BIT 1
When bit 1 is set (1), the operation is a write type command. Data is transferred from the buffer memory to the disk.

Bits 0 and 1 should not be set (1) at the same time.

The remaining bits 2-7 are Command type modifiers, and depending on a read or write type command have different meanings.

BIT 2
When bit 2 is set (1) and the operation is a read, only ID fields will be read to the buffer.

If the operation is a write and bit 2 is set (1), the command is a Format function.

BIT 3
When bit 3 is set (1), both the data and ECC check bits will be written or read to/from the buffer.

BIT 4
When bit 4 is set (1) and the operation is a Read Long, both the data and the syndrome (the result of the ECC check) is written to the buffer.

BIT 5
When bit 5 is cleared (0), this allows processor intervention on all flag conditions. Reads or writes to a sector with a nonzero flag byte or nibble will cause the command to abort and the FLAG BYTE/NIBBLE NONZERO bit of the Extended Status register to be set. After having determined the cause of the error, the micro-processor may choose to read or write the sector anyway, in which case it sets the IGNORE FLAG/FORMAT SECTOR bit and re-issues the command.

When set (1) on read and write commands, the flag byte/nibble will be ignored.

When set (1) on Format commands, the command is a Format Sector command and keys on the SECTOR line instead of the INDEX line. For this function the sequencer must be in HARD SECTORED MODE.

BIT 6
When bit 6 is set (1) on a read command, a byte by byte compare is accomplished by reading data from the buffer and comparing it with data from the disk.

BIT 7
When bit 7 is set (1) on a read command, it permits data fields to be read and checked for ECC errors without transferring the data to the buffer.

2.4.1.2 WRITE REGISTER 21_H: SEQUENCER LOOP COUNT

Bit	7	6	5	4	3	2	1	0
Byte	Number of Sectors (N = N)							

This register specifies the number of sectors to be read or written, or in the case of a Format command, the number of sectors on the disk. (Actually, the value in this register specifies the number of times the loop in the predefined state sequence for the particular command is executed). This value is decremented for each sector handled by the command. An internal register contains the initial value of this register, so that for repeated commands involving the same number of sectors, the register will be automatically reloaded with the proper value.

Once a command has been issued the real time contents of this register can be read by reading the Sequencer Loop Count register (RR29).

2.4.1.3 WRITE REGISTER 22_H: INDEX TIME-OUT

Bit	7	6	5	4	3	2	1	0
Byte				Number of Revolutions before time-out				

This register specifies the number of disk revolutions (as measured by the number of Index pulses) before a command is aborted. Legal values are 2 thru 15. This feature allows the sequencer to do automatic retries when it cannot find the ID. This register gets re-initialized after every successful transfer for multi-block commands. When a command is aborted because of Index Time-out, the Extended Status INDEX TIME-OUT status bit will be set. A holding register holds the value so this register only has to be loaded when a change is required.

2.4.1.4 WRITE REGISTER 23_H: SUB-BLOCK COUNT

Bit	7	6	5	4	3	2	1	0
Byte				Number of Sub-blocks per Sector				

The Sub-Block Count is used to determine the number of data bytes per sector.
The sector size = (Sub-Block Count + 1)*Data Field Count.
The Data Field Count is from the State Controller registers.

EXAMPLES:

Sector Size (Bytes	Sub-Block Count	Data Count
128	7_H	10_H
256	1_H	10_H
512	$1F_H$	10_H
1,024	$3F_H$	10_H
2,048	$7F_H$	10_H
65,536	FF_H	00_H (00=256)

This register should be loaded at initialization and any time a different sector size is being used.

2.4.1.5 WRITE REGISTERS 24 thru 27_H: ID REGISTERS

These four registers are compared to the first four bytes of the ID field read from the disk to determine if the desired sector has been found. Before any command, except FORMAT and CHECK TRACK FORMAT, these registers should be loaded with the first four bytes of the desired ID.

WRITE REGISTER 24 (High Byte) & 25 (Low Byte): CYLINDER (ID BYTES 0&1)

HIGH BYTE

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H							

LOW BYTE

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H							

These above two registers specify the first two bytes of the ID field. The allowed values are 0000 through $FFFF_H$.

WRITE REGISTER 26_H: HEAD (ID Byte 2)

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H or X0 - XF_H							

This byte specifies the third byte of the ID field. If the HEAD/FLAG Byte is selected (Bit 2, WR2D) only the low nibble of this byte is compared. Valid values are 00 thru $0F_H$. When the FLAG BYTE is selected, the valid values are 00 thru FF_H.

WRITE REGISTER 27_H: SECTOR NUMBER

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H							

This register specifies the fourth byte of the ID, normally used as the sector number to be read or written. It is a counter register that is auto-incremented at the end of a valid data field operation. This feature allows sequential operations on one track without having to reload the ID write registers.

2.4.1.6 WRITE REGISTER 28_H: MICRO TO MEMORY

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H							

This register is used to transfer data from the micro-processor bus to the buffer memory.

The micro-processor can write to the buffer memory through this register, and data is latched in this register during transfers from a peripheral on the micro-processor bus to the buffer memory. (Refer to RR3F for details of the peripheral to buffer transfer.)

When the micro-processor writes to WR28, the data is latched into WR28. The Data Sequencer then generates a request to DMA channel 3 to transfer the data from WR28 to the buffer memory location addressed by the DMA at ACK3 time.

The micro-processor should set up channel 3 of the DMA before initially writing to WR28. Subsequent writes to a contiguous block of data do not require re-initialization.

If the DMA does not respond to the channel 3 request, the Micro-Memory Over/Under Run and the Extended Status Nonzero bits in the Status and Extended Status registers will be set.

2.4.1.7 WRITE REGISTER 29_H: SEQUENCER START/RE-START

Bit	7	6	5	4	3	2	1	0
Byte	RE-Start State OX - FX				Start State X0 - XF_H			

During the execution of a command;
- bits 0-3 specify the state number at which the sequencer will begin execution;
- bits 4-7 specify the state number from which the sequence will be re-started after the state number specified in WR2A has been reached.

This value depends on the command and the particular disk configuration. The normal values are 33_H for all commands except Format, which is 21_H.

This register is also used to address the external State Control registers. Valid address values are 00 thr $0F_H$. Refer to the Sequencer State Flow Charts for details.

2.4.1.8 WRITE REGISTER $2A_H$: SEQUENCER LOOP STATE

Bit	7	6	5	4	3	2	1	0
Byte	Loop State XO - XF_H							

This register determines the state number, when the State Controller is looping, at which a jump to the RE-START state is performed. This value depends on the command and the particular disk configuration. Refer to the Sequencer State flow charts for details.

2.4.1.9 WRITE REGISTER $2B_H$: BIT RING CONTROL

Bit	7	6	5	4	3	2	1	0
Byte	03_H							

This register allows the user to specify the bit-level timing relationship between sync detect and byte clock. This register should be initialized with a 03_H.

2.4.1.10 WRITE REGISTER $2C_H$: ECC CONTROL

Bit	7	6	5	4	3	2	1	0

0 = ECC Clear on Init
1 = ECC Preset on Init

- Control XOR Gates -

0 = DATA to ECC
1 = -DATA to ECC

0 = ECC Feedback
1 =-ECC Feedback

0 = ECC Data Out
1 = ECC Data Out

0 = ECC Check Data
1 = -ECC Check Data

0 = MICRO Xfer Disabled
1 = MICRO Xfer Enabled

0 = ID Check = ECC
1 = ID Check = CRC

0 = Disable DATA Sync Timeout
1 = Enable DATA Sync Timeout

The ECC CONTROL register allows format and media compatibility with a variety of peripheral chips and various error correction formats.

BIT 0:
Bit 0 determines whether or not initialization of the ECC shift register string is cleared (to all zeros) or preset (to all ones.)

BIT 1 Through 4:
Bits 1-4 control XOR gates, which determine the polarity of the data at various stages in the ECC check logic. The following figure illustrates these gates in relation to the relevant ECC circuits.

BIT 5
Bit 5, when set (1), enables the transfer of data between a peripheral on the micro-processor bus and the buffer memory. Refer to Read registers RR3B and RR3F for details.

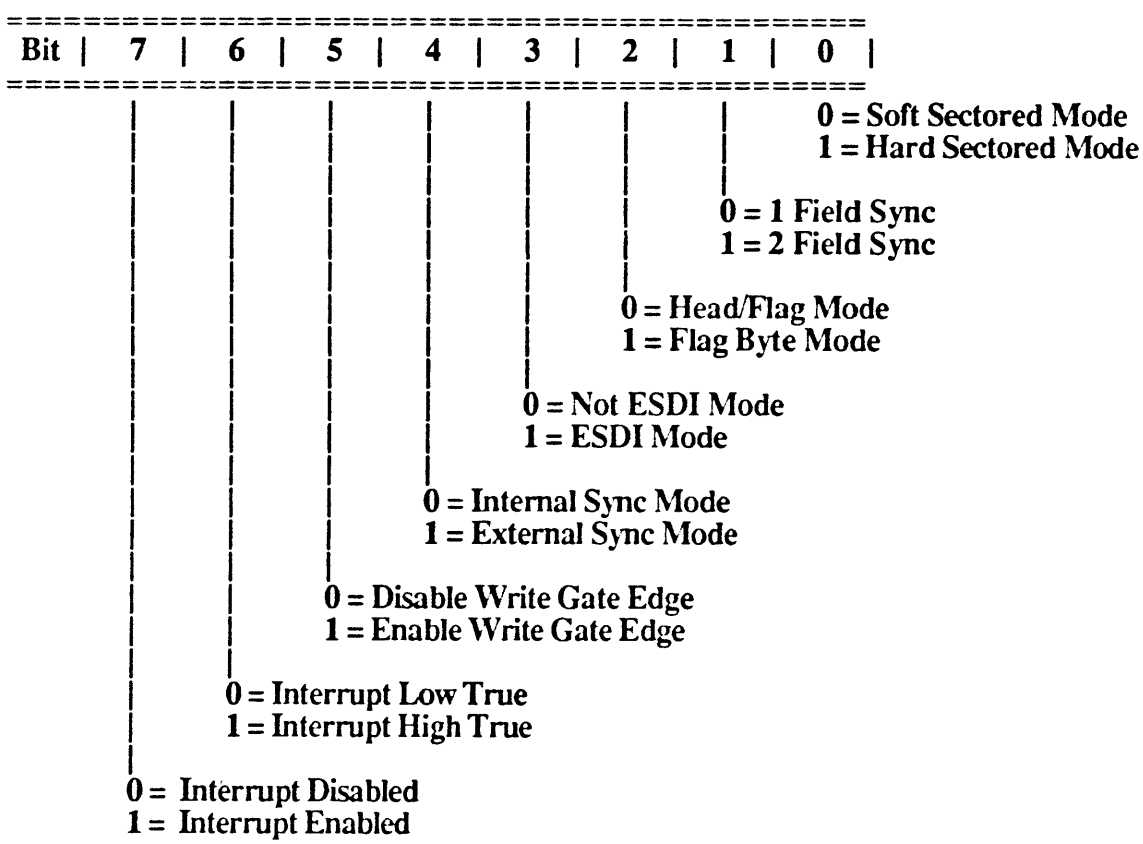
BIT 6
Bit 6 is used to choose which type of error detection code is used for the ID Field.

When bit 6 is cleared (0), the code used is the CCITT CRC-16 polynomial.

When bit 6 is set (1), the data ECC polynomial from registers WR30 through WR37 is used. Be sure to allocate the proper count in the State Control Register that will match the ID correction byte count implemented.

BIT 7
When bit 7 is set and an ID field has been properly read, failure to find the data field sync after 512 bit times will result in a Data Field Sync Time-Out Error bit set in the Extended Status register.

2.4.1.11 WRITE REGISTER $2D_H$: CONFIGURATION CONTROL



BIT 0
Bit 0 selects between the Hard Sectored and Soft sector disk drive environments. This bit is only used during a Format Track Command. In the Hard sectored mode the SECTOR line is used to re-synchronize the sequencer at State 15 and thereby determine the sector boundaries.

BIT 1
Bit 1 selects between the 1 byte sync and 2 byte sync formats. The 1 byte sync is normally used by ESDI drive interfaces and the 2 byte sync (SYNC BYTE, MARKER BYTE) is used by the ST506/412 type drives.

BIT 2
Bit 2 selects between HEAD/FLAG OR FLAG BYTE modes. The Data Sequencer allows the ID field to contain a flag nibble or a byte of information that can be used to alert the firmware of a flag condition with that sector exists, thereby stopping a command if the Ignore Flag Condition bit is not set.

If bit 2 is cleared (0), the flag information is contained in bits 4-7 of byte 2 (Flag/Head) of the ID field.

If bit 2 is set (1), the flag information is the 5th byte of the ID field. This bit also determines which read register contains the flag bits that are read from the disk. If the flag nibble is selected, the Head/Flag byte (RR26) contains the flag information;and if the flag byte is chosen, the Flag Byte register (RR23) will contain the flag information.

BIT 3
Bit 3 selects between an ESDI and a non-ESDI interface.

If the ESDI mode is cleared (0), the Sequencer is in ST-412 mode, and asserts READ GATE as soon as any Non-Format command is issued. This mode must be used to interface to the OMTI 5070 MFM and 5027 2,7 RLL Encode/Decode chips (or OMTI SDMs devices).

If bit 3 is set (1), ESDI mode is configured, and the sequencer assumes the ESDI Search Address / Address Mark Found mode of handshake.

BIT 4
Bit 4 selects between internal sync detect (used for ESDI type interfaces) and external sync detect (used when the sequencer is configured with the OMTI 5070 and OMTI 5027 Encode/Decode/VCO chip.)

If bit 4 is cleared (0), the sequencer performs the BIT to BYTE synchronization by performing a bit to bit compare with the serial data in shift register and the sync field state value.

If bit 4 is set (1), the sequencer keys off of the AM-FOUND line to perform BIT to BYTE synchronization.

BIT 5
Bit 5, when set disables the write gate for two bit times after the ID postamble field only on a Format Track command, thereby providing an edge of write gate for every PLO sync field as required by some ESDI-type drives.

BIT 6
Bit 6 selects between interrupt active low or high.

If bit 6 is cleared (0), and the interrupt is enabled (bit 7), an interrupt will be active LOW.

If bit 6 is set (1), and the interrupt is enabled (bit 7), an interrupt will be active HIGH.

BIT 7
Bit 7 enables or disables interrupts. If enabled, an interrupt is generated by any condition that caused the sequencer to change from a BUSY to NOT BUSY status. The interrupt is cleared by reading the Status Register (RR20).

2.4.1.12 WRITE REGISTER $2E_H$: EXTERNAL COUNT REGISTER

Bit	7	6	5	4	3	2	1	0
Byte	$00 - FF_H$							

This register is used in conjunction with WR29, to store the COUNT in the External State Control Register indexed by the State number loaded in WR29.

2.4.1.13 WRITE REGISTER $2F_H$: EXTERNAL VALUE REGISTER

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H							

This register is used in conjunction with WR29, to store the VALUE in the External State Control Register indexed by the State number loaded in WR29.

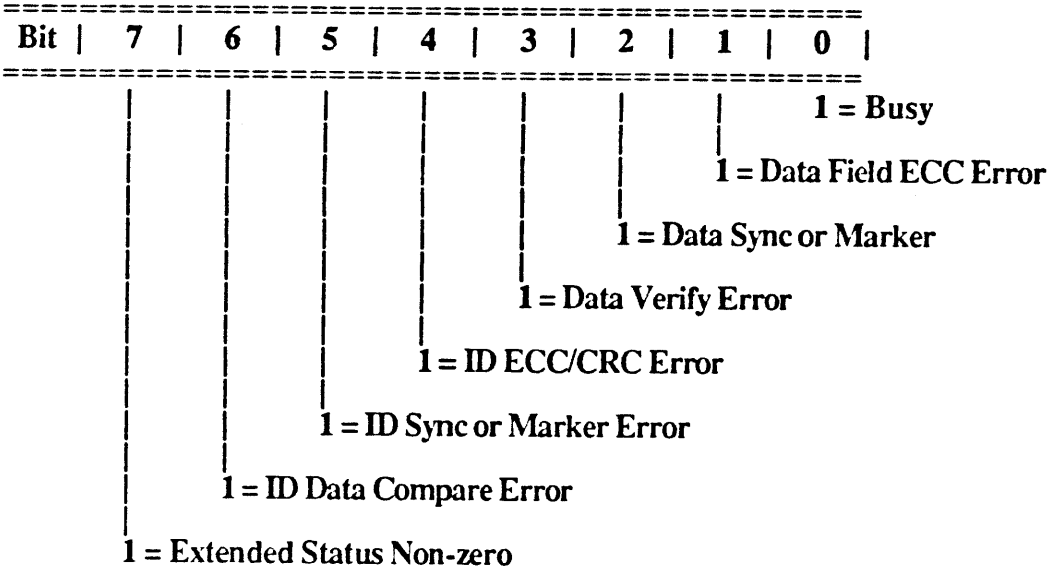
2.4.1.14 WRITE REGISTER $30\text{-}37_H$: POLYNOMIAL GENERATOR

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H							

With these eight registers, the sequencer can be configured to have any polynomial between 8 and 64 bits in length (modulo 8 bits). The value to load in these registers are a function of the polynomial desired, with the 80_H bit of WR30 being the most significant bit in the polynomial and setting every bit that corresponds to a term for that polynomial. Any polynomial less than 64 bits in length, must have all unused byte cleared, not to effect the desired redundancy bytes. It is very important to configure the ID ECC and DATA Field ECC State count in the External State Control Register File to correspond with the polynomial loaded in these eight registers.

2.4.2 READ REGISTERS

2.4.2.1 READ REGISTER 20_H: STATUS



The status register holds sequencer status information and is read at the completion of every command to determine whether execution was successful. During command execution, this register may be polled by the micro-processor in order to determine the bit-significant status on a sector-by-sector real time basis. For example, when a time-out has occurred, the micro-processor can determine whether or not an ID was read successfully (though the ID did not compare), or whether no ID's were successfully read, in which case the disk is improperly formatted or incompatible with the controller.

BIT 0
Bit 0 is set (1), when a command is in progress.

Bit 0 is cleared (0), when the sequencer is in a quiescent state.

BIT 1
Bit 1 is set during read operations when the sequencer detects an ECC error in the data field.

BIT 2
Bit 2 is set when, in external sync mode, the Address Mark is detected (A-M FOUND is true) but the byte value does not compare with the sync or marker byte in the External State Control Register File.

BIT 3
Bit 3 is set when an error is detected during the Read Verify (byte by byte compare) command.

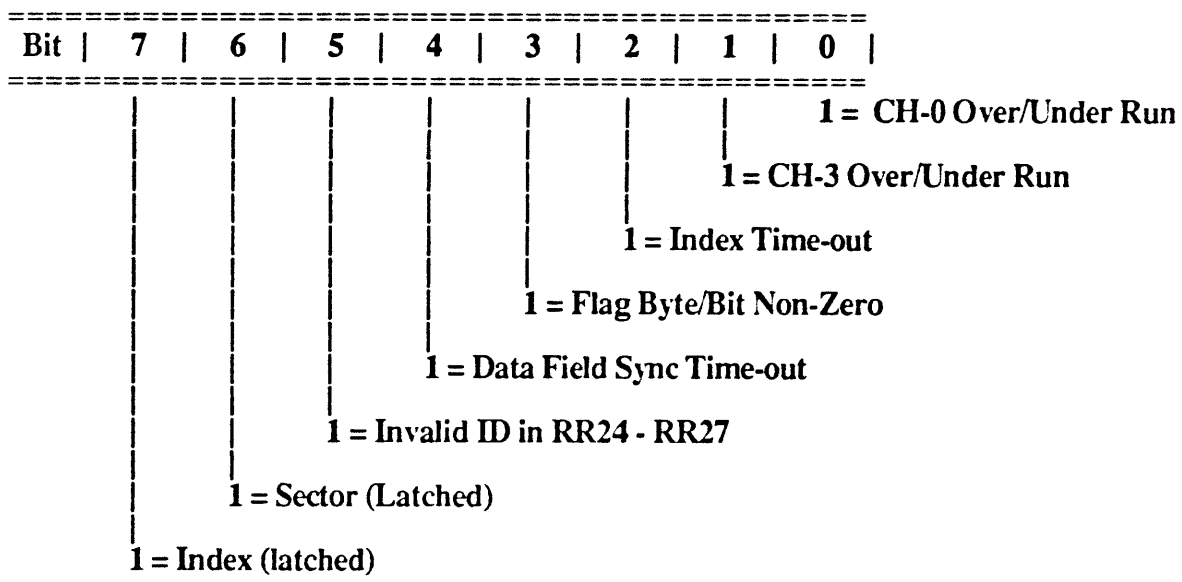
BIT 4
Bit 4 is set if an ECC or CRC error is detected in the ID field.

BIT 5
Bit 5 is set during execution of read/write operations if the sector/s ID sync and ID address mark cannot be found. The number of disk revolutions which may occur before this bit is set is determined by the value in WR22.

BIT 6
Bit 6 is set when the sequencer detects that the four-byte ID data field does not correspond to the contents of WR24-27.

BIT 7
Bit 7 is set when any bit in the Extended Status register RR21 is set.

2.4.2.2 READ REGISTER 21_H: EXTENDED STATUS



The Extended Status register contains additional sequencer status information about command execution.

BIT 0
Bit 0 is set when the DMA channel zero does not respond within one byte time with acknowledge (ACK0) to the Data Sequencer's request (REQ0) for a DMA data transfer.

BIT 1
Bit 1 is set when the DMA channel three does not respond after the micro-processor reads or writes RR28 or WR28.

BIT 2
Bit 2 is set after the sequencer has tried to search for an ID in which ID Sync, ID Compare and ID ECC/CRC have not all been true a sector for the programmed number of retries loaded into WR22.

BIT 3
Bit 3 is set on a read command after the sequencer has found the proper ID but has not found the Data Sync Byte within 512 bit times (if enabled by setting Bit 5 of WR2D to a 1).

BIT 4
Bit 4 is set on a read or write command if the sequencer finds the proper ID but a Flag Condition exists.

BIT 5
Bit 5 is initially set by any command to the sequencer but is cleared after the sequencer has processed any valid ID and RR23-RR27 have a valid ID stored. If after an index time-out this bit is set, RR23-RR27 have the last valid ID processed available.

BIT 6
Bit 6 is a means for the micro-processor to poll for a sector pulse from the disk. This bit is latched so a very narrow pulse can still be captured.

BIT 7
Bit 7 is a means for the micro-processor to poll for an index pulse from the disk. This bit is latched so a very narrow pulse can still be captured.

List of Status bits initialized by issuing a non abort command:

STATUS REGISTER

BIT	NAME	BIT VALUE
0	Busy	1
1	Data ECC Error	0
2	Data Sync + Marker Not Found	0
3	Data Verify Error	0
4	ID ECC/CRC Error	1
5	ID Sync + Marker Not Found	1
6	ID Compare Error	1
7	Extended Status Non-Zero	X

EXTENDED STATUS REGISTER BIT

0	Disk Data Over/Under-run	X
1	Micro Memory Over/Under-run	X
2	Index time-out	0
3	Flag Bit / Byte Non-Zero	X
4	Data Field Sync Time-out	0
5	Invalid ID	1
6	Sector	X
7	Index	X

2.4.2.3 READ REGISTER 22_H: RETRY COUNT /STATE ADDRESS

Bit	7	6	5	4	3	2	1	0
Byte	OX-F = Sequencer State				XO-XF = Retry Count			

Bits 0-3 of this status register contain the actual number of disk revolutions counted on a sector by sector basis to find a valid desired sector on a read or write command.

Bits 4-7 represent the real-time value for the internal state machine of the sequencer. This information is useful for synchronizing the program to the sequencer. It is necessary to debounce this information since the state of the sequencer is changing asynchronously to the microprocessor.

2.4.2.4 READ REGISTER 23_H: FLAG BYTE (Header Byte 5)

Bit	7	6	5	4	3	2	1	0
Byte	$00 - FF_H$ = Flag Byte							

This register contains the fifth byte of header information read from the disk in a real time mode. If the format of the disk does not have five bytes of ID data, this register will not contain any valid information. If the sequencer is configured in the Flag Byte Mode and the Flag Byte Non-Zero Extended Status Bit is set, this register will contain the flag information.

2.4.2.5 READ REGISTER 24 (High Byte) & 25 (Low Byte): CYLINDER (ID BYTES 0&1)

HIGH BYTE

Bit	7	6	5	4	3	2	1	0
Byte	$00 - FF_H$							

LOW BYTE

Bit	7	6	5	4	3	2	1	0
Byte	$00 - FF_H$							

These four registers are the real time updated value of the current ID information from the disk. They are updated on every ID that have valid ID Sync but are not required to have valid ID CRC/ECC. Of the four registers, RR24 represents the first byte of ID information while the RR27 register contains the fourth byte of ID information. If the sequencer is configured in Flag Bit Mode, the high nibble of RR26 contains the flag information.

2.4.2.6 READ REGISTER 26_H: HEAD (ID Byte 2)

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H or X0 - XF_H							

2.4.2.7 READ REGISTER 27_H: SECTOR NUMBER

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H							

2.4.2.8 READ REGISTER 28_H: MEMORY TO MICRO

Bit	7	6	5	4	3	2	1	0
Byte	00 - FF_H							

This register is used to transfer data from the buffer memory to the micro-processor bus.

The micro-processor can read the buffer memory through this register and data is latched in RR28 during transfers from the buffer memory to a peripheral on the memory data bus. (Refer to RR3F for details of the buffer to peripheral transfer.)

When the micro-processor reads RR28, the data in the register is transferred to the micro-processor. The Data Sequencer then does a channel 3 DMA request to get ready for the next micro-processor read.

Channel 3 of the DMA should be initialized before starting a buffer read sequence. It is required to configure the DMA channel 3 control register to be in a read memory /write peripheral mode.

NOTE: It is necessary for the micro-processor to do a read of this register and discard the information the first time after initializing the DMA controller when reading data from the buffer memory. This function is required to set the first channel 3 DMA request and is considered a PRE-FETCH.

If the DMA does not respond to the channel 3 request, the Micro-Memory Over/Under Run and the Extended Status Nonzero bits in the Extended Status and Status registers will be set.

TRANSFERS BETWEEN A PERIPHERAL ON THE MICRO-PROCESSOR BUS AND MEMORY.

The Data Sequencer has the capability to transfer data from a peripheral chip that is on the micro-processor A/D bus to or from buffer memory. To transfer data from the peripheral chip to buffer memory , the micro-processor reads address $3F_H$. To transfer data from buffer memory to the peripheral chip, the micro-processor read address $3B_H$. This operation is enabled by setting the XFER ENABLE bit (bit 5) in the ECC Control register (WR2C). Channel 3 of the DMA is used and should be initialized before starting the transfer.

When the micro-processor does a read from address $3F_H$, the Data Sequencer generates a read strobe on pin 53 (-GRPRD), enabling the data to be latched into the Micro to Memory register (WR28). The rising edge of the strobe causes a DMA cycle, using REQ3 and ACK3 to write the contents of WR28 into the buffer memory.

When the micro-processor reads address $3B_H$, the Data Sequencer generates a write strobe on pin 52 (-GRPWRT), enabling data to be written to the peripheral from the Memory to Micro register (RR28). On the trailing edge of the strobe, a DMA cycle is initiated, using REQ3 and ACK3, to read the next buffer memory location into RR28, in order to prepare for the next transfer.

It is necessary to pre-fetch the first byte from the buffer memory before doing the transfer to the peripheral. The micro-processor does this by setting up the DMA channel 3 control register then reading the Memory to Micro register (RR28). The Data Sequencer does a DMA cycle, using REQ3 and ACK3, to transfer the data from the buffer memory to the Memory to Micro register (RR28). This pre-fetches the data that will be written to the peripheral on the next transfer.

2.4.2.9 READ REGISTER 29_H: SEQUENCER LOOP COUNT

Bit	7	6	5	4	3	2	1	0
Byte	$00 - FF_H$							

This register contains the real time value of the sequencer loop counter. This value is decremented every time the sequencer is incremented from the Loop End State to the Restart State. This information is valuable in a multi-sector command for the micro-processor to synchronize to the sequencer. It is necessary to debounce this information since the state of the sequencer is changing asynchronously to the micro-processor.

2.4.2.10 READ REGISTER $2E_H$: EXTERNAL COUNT REGISTER

Bit	7	6	5	4	3	2	1	0
Byte	$00 - FF_H$							

This register is used in conjunction with WR29, to read the COUNT in the External State Control Register indexed by the State number loaded in WR29.

2.4.2.11 READ REGISTER $2F_H$: EXTERNAL VALUE REGISTER

Bit	7	6	5	4	3	2	1	0
Byte	$00 - FF_H$							

This register is used in conjunction with WR29, to read the VALUE in the External State Control Register indexed by the State number loaded in WR29.

2.4 STATE CONTROL REGISTERS

The State Control registers contain the parameters that specify the size and content of the various fields of the disk format. These registers are external to the chip and may be located in any type of external memory (e.g. RAM, ROM, EPROM). The device access time must be less than two bit times of the NRZ Data Rate. (See the A. C. Timing Characteristics for details.)

If the State Control Register is implemented in a RAM type of memory device, the micro-processor must initialize them before reading, writing, or formatting the disk.

To write to the State Control Registers, the micro-processor writes the State Address (0 to FH) to the Sequencer Start/Re-Start Register (WR29). This State Address value is then an index into the State Control Register. The parameters for that State are then transferred to the State Control RAM by writing the count to the External Count Register (WR2E) and the value to the External Value Register (WR2F).

To read the State Control Registers, the micro-processor writes the State Address (0 to FH) to the Sequencer Start/Re-Start Register (WR29). The parameters are then read from the State Control Register by reading the External Count register (RR2E) for the count and the External Value register (RR2F) for the value.

2.4.4. STROBE LOGIC

In addition to the above registers, there are addresses in the chip address space that can be read/written by the micro-processor to read or write an external register.

WRITE ADDRESSES WA38 through WA3F:

Address	38_H	:External	Out	Strobe 0:	Asserts	-WRTL0	(Pin 50)
Address	39_H	:External	Out	Strobe 1:	Asserts	-WRTL1	(Pin 51)
Address	$3C_H$	:External	Out	Group Strobe:	Asserts	-GRPWRT	(Pin 52)
Address	$3D_H$	:External	Out	Group Strobe:	Asserts	-GRPWRT	(Pin 52)
Address	$3E_H$	:External	Out	Group Strobe:	Asserts	-GRPWRT	(Pin 52)
Address	$3F_H$	:External	Out	Group Strobe:	Asserts	-GRPWRT	(Pin 52)

READ ADDRESSES RA38 through RA3F:

Address	38_H	:External	In	Strobe 0:	Asserts	-INST0	(Pin 48)
Address	39_H	:External	In	Strobe 1:	Asserts	-INST1	(Pin 49)
Address	$3C_H$	:External	In	Group Strobe:	Asserts	-GRPRD	(Pin 53)
Address	$3D_H$	:External	In	Group Strobe :	Asserts	-GRPRD	(Pin 53)
Address	$3E_H$	:External	In	Group Strobe:	Asserts	-GRPRD	(Pin 53)
Address	$3F_H$	:External	In	Group Strobe:	Asserts	-GRPRD	(Pin 53)

2.4.5 LIST OF OMTI 5050 COMMANDS

Commands are issued to the Data Sequencer by initializing all necessary parameters, then writing the command to the Command register (WR20).

HEX	BITs 7654 3210	COMMANDs
00	0000 0000	ABORT
01	0000 0001	NORMAL READ
02	0000 0010	NORMAL WRITE
05	0000 0101	READ ID
06	0000 0110	FORMAT TRACK
09	0000 1001	READ LONG
0A	0000 1010	WRITE LONG
0E	0000 1110	FORMAT TRACK LONG
19	0001 1001	READ SYNDROME LONG
1D	0001 1101	READ ID SYNDROME LONG
21	0010 0001	READ-IGNORE FLAG
22	0010 0010	WRITE-IGNORE FLAG
26	0010 0110	FORMAT SECTOR
29	0010 1001	READ LONG-IGNORE FLAG
2A	0010 1010	WRITE LONG-IGNORE FLAG
39	0011 1001	READ SYNDROME-IGNORE FLAG
41	0100 0001	VERIFY
49	0100 1001	VERIFY LONG
59	0101 1001	VERIFY SYNDROME LONG
61	0110 0001	VERIFY-IGNORE FLAG
69	0110 1001	VERIFY LONG-IGNORE FLAG
79	0111 1001	VERIFY SYNDROME LONG-IGNORE FLAG
81	1000 0001	CHECK DATA ECC

85	**1000 0101**	**CHECK TRACK FORMAT**
A1	**1010 0001**	**CHECK DATA ECC-IGNORE FLAG**

There are other combinations of bits that can be written to the Command register, but the results may not defined.

2.4.5.1 COMMAND DESCRIPTION

ABORT **00_H**

Issuing an ABORT to the Command register when the Data Sequencer is busy will abort the executing command. The status goes from Busy to Not-Busy. If enabled, the INTERRUPT will set.

NORMAL READ **01_H:**

The Read command is used to transfer a block(s) of data from the disk to the buffer.

NORMAL WRITE **02_H:**

The WRITE command is used to transfer block(s) of data from the buffer memory to the disk.

READ ID **05_H:**

The READ ID command is used for transferring ID sequencially from the disk to the buffer memory.

FORMAT TRACK **06_H:**

The FORMAT command is used to format one track on the disk. After the command is issued, the Data Sequencer waits for the next INDEX pulse. On the rising edge of INDEX, the Data Sequencer turns on WRT GATE; and it stays on until the loop counter has counted through zero. If (as in a normal FORMAT TRACK command) the LOOPEND State equals an $0F_H$, WRT GATE is turned off on the next rising edge of INDEX, and an INTERRUPT is set (if enabled). If the Enable Write Gate Edge bit is set (Bit 5, WR2D), WRT GATE is disabled for 2 bit times preceding each data field preamble. This feature is an option for some ESDI type formats.

The size of each field of each sector on the track is determined by the counts in the State Controller Register. Except for the ID Data field, the ID ECC/CRC field and the Data ECC field, the values for all other fields are determined by the values in the State Controller Registers. The ID data field bytes are read by the Data Sequencer from the buffer memory using DMA channel zero. It is the firmware responsibility to configure DMA channel 0 to the correct mode and point to a location in buffer memory where a contiguous table of physically sequential ID data field is located.

The ID ECC/CRC and the data ECC fields values are generated by the Data Sequencer based on the contents of the ECC control and polynomial registers. The sequence loop count (WR21) defines the number of sectors on a track (the number of State Controller loops.)

INITIALIZATION

Before issuing the FORMAT command, the micro-processor should write the number of sectors on the track to the Sequencer Loop Count Register. The Index Timeout register should be loaded with a number greater than 1.

The Sub-Block Count is used to define the number of data bytes per sector.

The sector size = (Sub-Block Count +1)*Data Field Count.

The Sub Block Count is from (WR23) and the Data Field Count is from the State Controller memory.

The Sequencer Start/Re-Start register should be loaded with 21_H and the Sequence Loop State register should be loaded with $0F_H$.

The ID Data field bytes are read by the Data Sequencer from the buffer memory using DMA channel zero. It is the firmwares responsibility to configure DMA channel 0 to the correct mode and point to a location in buffer memory where a contiguous table of physically sequential ID data field is located.

FORMAT SECTOR

The FORMAT SECTOR command can be used on Hard Sectored disks to format one or more sectors. After the command is issued, the Data Sequencer will start the format on the next SECTOR or INDEX pulse and format for the number of sectors specified in the Sequencer Loop Count register.

It is the responsibility of the micro-processor to issue the command during the sector just before the sector to be formatted. The micro-processor can count the sectors since Index by polling the Extended Status register Index and Sector bits. This command allows the controller to easily map out bad sectors even after the disk has been formatted and used.

PARAMETER INITIALIZATION BEFORE ISSUING COMMANDS

The ID Write Registers should be set to the desired disk location if this has not already been done. Note: The sector register gets incremented after each error free block is transferred so it is not necessary to re-initialize it for sequential block transfers.

The Sub-Block Count only needs to be re-initialized if the block size changes.

The Sequencer Start/Re-Start and Sequencer Loop State registers should be initialized to 33_H and 0EH respectively, and do not need to be changed except when doing FORMAT. Do not forget to change back after configuring for these commands.

Status after READ LONG commands -- ECC invalid bit = 1.

INITIALIZATION

After a RESET, the chip goes not-busy, the read gate (RD GATE) and write gate (WRT GATE) signals are reset and the Disk Data Over/Under Run and Micro-memory Over/Under Run bits (Bits 0 and 1, RR21) in the Extended Status are cleared.

It is the responsibility of the micro-processor firmware to initialize all other parameters after a power-up. This includes all of the Transfer Control registers and the external State Control registers if they are in RAM.

ID Search

In Non-ESDI mode, after a Read/Write type command is issued to the Sequencer, RD GATE is asserted. Three bit times after A-M FOUND signal goes active, the Data Sequencer then compares the Sync byte followed by the Marker byte. Then the Sequencer reads the ID Data which is latched into the ID read registers (RR24 thru RR27), and compared with the contents of the ID write registers (WR24 thru WR27).

If they compare, the ID DATA NO COMPARE bit in the Status register is cleared. If the ID compared, the flag byte/nibble is checked. If the flag byte/nibble is nonzero, the command is aborted with the FLAG BYTE/NIBBLE NONZERO bit in the Extended Status register set (1).

The ID ECC/CRC is read and checked. If good, the ID ECC Error bit in the Status register is cleared.

If there were any ID type Errors (ID Sync, ID Compare or ID ECC/CRC), the Data Sequencer will automatically de-assert RD Gate and loop back to the Start State to retry the desired sector ID. The Sequencer searches until it finds the valid ID or for the number of revolutions specified in the Index Time-Out register.

Data Transfer

If the ID Sync, ID compared, the flag byte/nibble was zero and the ID ECC/CRC was good, RD Gate is de-asserted and re-asserted to read the data field.

When in the External Sync Detect mode (Bit 4, WR2D), after the Address Mark is detected (A-M FOUND activated) the value of the Data Sync byte then the Data Marker byte is compared to the value in the State Control memory. If they do not compare, the command is aborted with the Data Sync + Marker Not Found bit in the Status register set.

If A-M Found is not detected within 512 bit times after RD GATE is activated, the command is aborted with the Data Field Sync Time-Out bit in the Extended Status register set.

After the A-M Found is detected and the Data Sync and Data Marker Bytes are valid, the Sequencer then uses REQ0 and ACK0 to request the DMA to transfer the data to the buffer memory.

If, during the data transfer, the DMA does not respond within one byte time to the Data Sequencer request (REQ0); the Disk Data Over/Under run bit set in the Extended Status register.

When the command is complete or aborted, the status will go Not Busy; and if enabled, the interrupt will set.

APPENDIX A

INITIALIZATION OF THE REGISTER FILE

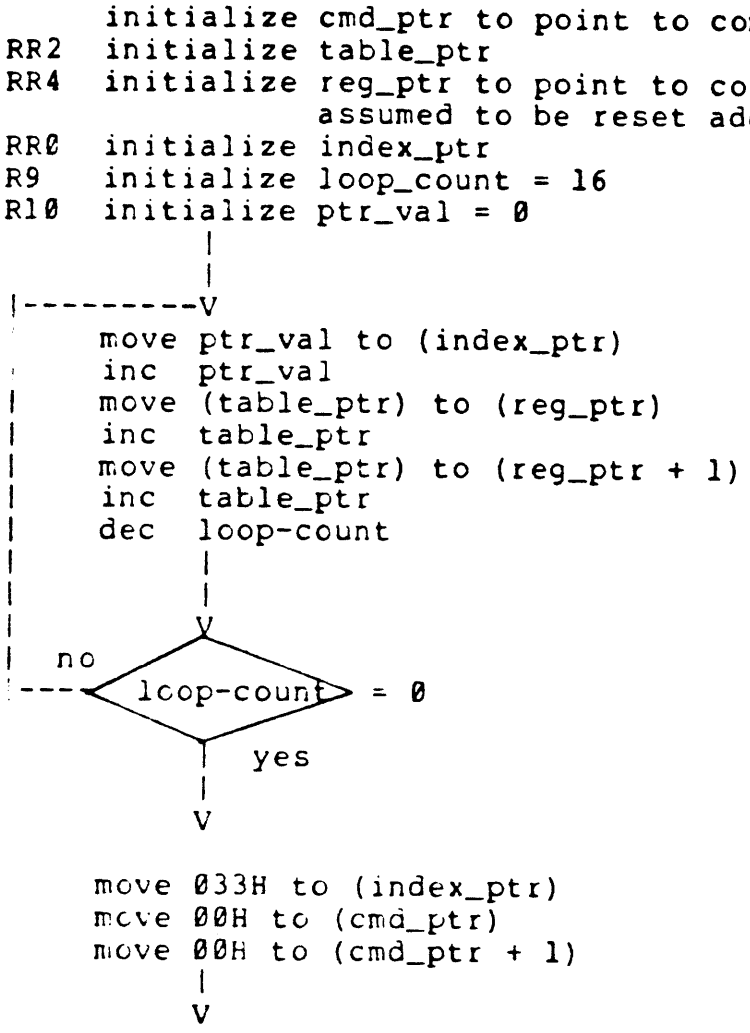
In order to initialize the Format Parameter Register File, a table is first set up, typically in ROM, containing the values to be written into the file. Each Define Byte directive specifies the contents of a Count or Value register. An example table for a soft-sectored format is as follows:

```
SEQTBL:
        DB    001H          ;; State 0 Count
        DB    000H          ;; State 0 Value
        DB    00BH          ;; Post Index Byte Count
        DB    04EH          ;; Post Index Data Value
        DB    00CH          ;; ID Preamble Byte Count
        DB    000H          ;; ID Preamble Data Value
        DB    001H          ;; ID Sync Byte Count
        DB    0A1H          ;; ID Sync Byte Value
        DB    001H          ;; ID Marker Byte Count
        DB    0FEH          ;; ID Marker Byte Value
        DB    004H          ;; ID Data Field Byte Count
        DB    000H          ;; ID Data Field Value (No Care)
        DB    004H          ;; ID ECC Field Count
        DB    000H          ;; ID ECC Field Value (No Care)
        DB    002H          ;; ID Postamble Byte Count
        DB    000H          ;; ID Postamble Data Value
        DB    00CH          ;; Data Field Preamble Byte Count
        DB    000H          ;; Data Field Preamble Value
        DB    001H          ;; Data Sync Byte Count
        DB    0A1H          ;; Data Sync Byte Value
        DB    001H          ;; Data Marker Byte Count
        DB    0F8H          ;; Data Marker Byte Value
        DB    004H          ;; Data Field Byte Count
        DB    0E5H          ;; Data Field Format Value
        DB    004H          ;; Data Field ECC Byte Count
        DB    000H          ;; Data Field ECC Value (No Care)
        DB    002H          ;; Data Field Postamble Byte Count
        DB    000H          ;; Data Field Postamble Data Value
        DB    00EH          ;; Inter-Sector Gap Byte Count
        DB    04EH          ;; Inter-Sector Gap Data Value
        DB    001H          ;; Pre-Index Gap Count (Wait for Index)
        DB    04EH          ;; Pre-Index Gap Value
TBLEND: EQU   $             ;; End of Table
```

Data in the table is then used by a download program to initialize the Register File. The following is an example of such a program in Z8 assembly language.

```
LOADSRF:  LD    R2,#SEQTBL > 8       ;; POINT TO TABLE HIGH
          LD    R3,#SEQTBL&0FFH      ;; POINT TO TABLE LOW
          LD    R1,.LRSTST           ;; INDEX POINTER
          LD    R4,#80H              ;; INIT HIGH BYTE OF RR4
          LD    R5,.LSEQCNT          ;; COUNT REGISTER
          LD    R9,#16               ;; LOOP COUNT
          LD    R10,#0               ;; POINTER VALUE
LOADSRF1: LDE   @RR0,R10             ;; OUTPUT INDEX VALUE
          LDC   R14,@RR2             ;; GET COUNT FROM TABLE
          LDE   @RR4,R14             ;; OUTPUT COUNT TO REGISTER FILE
          INCW  RR2                  ;; BUMP TABLE POINTER
          INC   R5                   ;; VALUE REGISTER
          LDC   R14,@RR2             ;; GET VALUE FROM TABLE
          LDE   @RR4,R14             ;; OUTPUT VALUE TO REGISTER FILE
          INCW  RR2                  ;; BUMP TABLE POINTER
          DEC   R5                   ;; COUNT REGISTER
          INC   R10                  ;; NEXT INDEX VALUE
          DJNZ  R9,LOADSRF1          ;; DO 16 TIMES
          LD    R14,#033H            ;; RESTART/START STATE
          LDE   @RR0,R14             ;; REPLACE VALUE TO SEQUENCER
          CLR   R14                  ;; CLEAR A
          LD    R1,.LSEQCMD          ;; POINT TO COMMAND
          LDE   @RR0,R14             ;; NOP COMMAND TO SEQUENCER
          INC   R1                   ;; POINT TO EXTENDED STATUS
          LDE   R14,@RR0             ;; READ EXTENDED STATUS (CLEAR STATUS)
          RET
```

A flowchart for this program is given below. Symbols enclosed in parenthesis represent the contents pointed to by the symbol.



The initialization process is summarized in Figure A-1. A register pair is selected by writing a register index number (ptr_val) into WR9. The first value in the table, which in this case is the ESDI Sector Gap Count Register, is written into WR14, thereby selecting the Count register. Using the same index value (WR9 = 0), the value parameter (the second entry in the table) is written into WR15, thereby selecting the Value register. WR9 is then incremented, and the operation is repeated for the remaining values to be transferred.

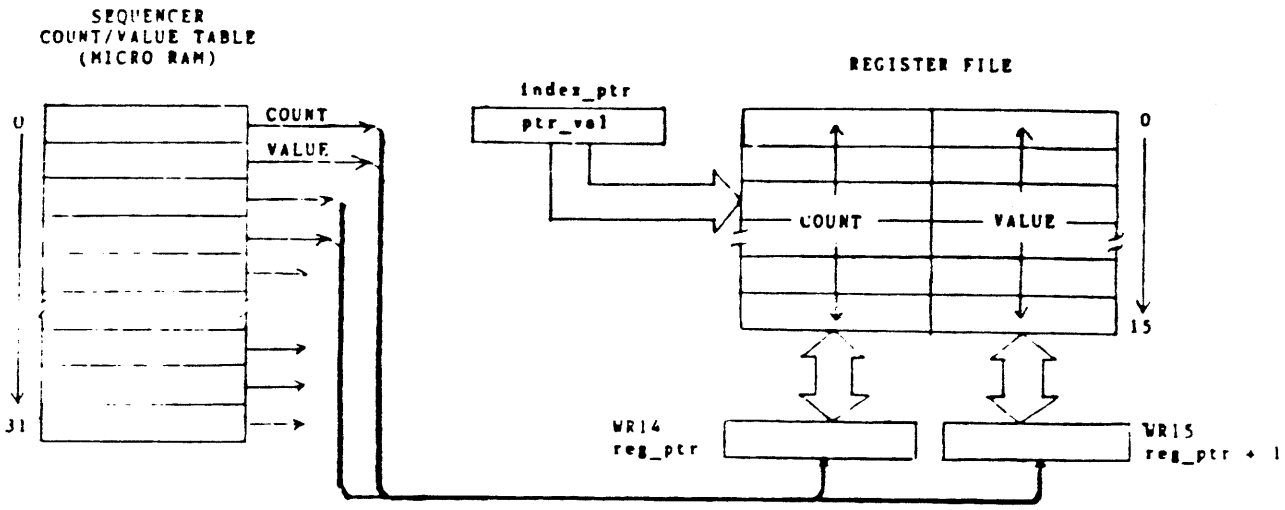


Figure A-1. Initializing the Register File

APPENDIX B

SEQUENCER STATE FLOW CHART (SOFT-SECTORED)

FORMAT COMMAND

State	Mode	Function	Count	Value
0		----		
1	START	POST INDEX GAP	SEQ-CNT	SEQ-VAL
2	RESTART	ID PREAMBLE	SEQ-CNT	SEQ-VAL
3		ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	MEMORY
6		ID ECC	SEQ-CNT	ECC GENERATOR
7		ID POSTAMBLE	SEQ-CNT	SEQ-VAL
8		DATA PREAMBLE	SEQ-CNT	SEQ-VAL
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	SEQ-VAL
12		DATA ECC	SEQ-CNT	ECC GENERATOR
13		DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
14	LOOP	INTER SECTOR GAP	SEQ-CNT	SEQ-VAL
15	HOLD	PRE-INDEX GAP (HOLD)	INDEX	SEQ-VAL
16		DONE		

READ COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	SEQ-VAL
6		ID ECC	SEQ-CNT	SEQ-VAL
7		ID POSTAMBLE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA TO MEMORY
12		DATA ECC	SEQ-CNT	SEQ-VAL
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

READ LONG COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		SKIP STATE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA TO MEMORY
12		DATA ECC	SEQ-CNT	ECC TO MEMORY
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

READ SYNDROME COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		SKIP STATE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA TO MEMORY
12		DATA ECC	SEQ-CNT	SYND TO MEMORY
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

READ VERIFY COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		SKIP STATE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA FROM MEMORY
12		DATA ECC	SEQ-CNT	ECC CHECK
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

READ VERIFY LONG COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		SKIP STATE	1	
8		SKIP STATE	1	
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA FROM MEMORY
12		DATA ECC	SEQ-CNT	DATA FROM MEMORY
13		SKIP STATE	1	
14	LOOP	SKIP STATE	1	
15		----		
16		----		

WRITE COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		ID POSTAMBLE	SEQ-CNT	
8		DATA PREAMBLE	SEQ-CNT	SEQ-VAL
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA FROM MEMORY
12		DATA ECC	SEQ-CNT	ECC CHECK
13		DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
14	LOOP	SKIP STATE	1	
15		----		
16		----		

WRITE LONG COMMAND

State	Mode	Function	Count	Value
0		----		
1		----		
2		----		
3	ST/RESTRT	ID SYNC BYTE	SEQ-CNT	SEQ-VAL
4		ID MARKER BYTE	SEQ-CNT	SEQ-VAL
5		ID DATA FIELD	SEQ-CNT	HEADER REGISTER
6		ID ECC	SEQ-CNT	ECC CHECK
7		ID POSTAMBLE	SEQ-CNT	
8		DATA PREAMBLE	SEQ-CNT	SEQ-VAL
9		DATA SYNC BYTE	SEQ-CNT	SEQ-VAL
10		DATA MARKER BYTE	SEQ-CNT	SEQ-VAL
11		DATA FIELD	CNT*BLK	DATA FROM MEMORY
12		DATA ECC	SEQ-CNT	DATA FROM MEMORY
13		DATA POSTAMBLE	SEQ-CNT	SEQ-VAL
14	LOOP	SKIP STATE	1	
15		----		
16		----		