**PUBLICATION NO. Tbd**

# DATA SEPARATOR CHIP

## ENCODER/DECODER/VCO

## NRZ/MFM

## SPECIFICATIONS

Preliminary

**Model :**

## OMTI5070

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# OMTI PFM 5070 VCO/ENCODE/DECODE CHIP
# PRODUCT SPECIFICATION
# (PART #20507)

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# CHAPTER 1

# GENERAL DESCRIPTION

## 1.1 INTRODUCTION

The OMTI PFM 5070 VCO/Encode/Decode chip provides all of the necessary functions needed to convert disk drives with MFM serial data interfaces (i.e., ST506/412, SA1000) to NRZ data and clock. It contains an internal voltage controlled oscillator, phase-locked loop, encode/decode logic, Address Mark generation and detection, and all the circuitry required for write precompensation.

The PFM 5070 is capable of operation at data rates up to 10 megabits per second by proper selection of the external frequency and loop gain components. The need for delay lines is eliminated by selecting write precompensation values with a constant current controlled RC network.

## 1.2 5070 VCO/ENCODE/DECODE CHIP CAPABILITIES

* Data rate control to 10 megabits per second
* No external logic required
* Internal VCO and phase-locked loop
* MFM to NRZ and NRZ to MFM conversion
* Internal address mark detection and generation circuitry
* Externally controlled write precompensation
* Internal early, on time, and late timing
* Control for external filter/varactor
* 24-pin plastic package

## 1.3 FUNCTIONAL OVERVIEW

Figure 1 illustrates the internal block diagram of the PFM 5070 VCO/Encode Decode chip. Each logic block is discussed in the following sections.

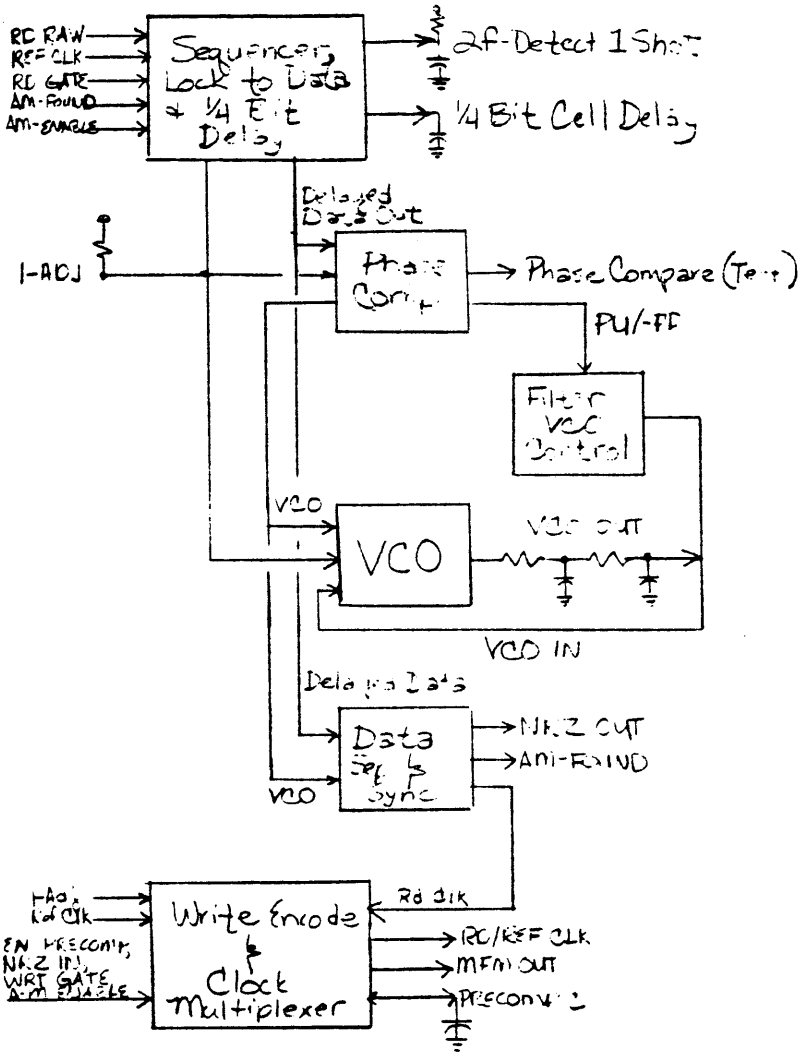


**Figure 1. Internal Block Diagram**

### 1.3.1 Sequencer, Lock to Data and 1/4-Bit Delay

This block delays the raw data from the disk by 1/4-bit cell time in preparation for use by the Phase Comparator. It also provides the A-M FOUND signal to the Data Sequencer, which allows it to lock on the data. Figure 2 contains a flow chart describing the Search Sync mode and AM Detect operations performed by this block.

### 1.3.2 Phase Comparator

The Phase Comparator compares the phase and frequency of the incoming signal with the VCO frequency, and generates an error voltage that is related to the phase and frequency difference between the two signals. The PU/-PD (Pump-Up/Pump-Down) signal communicates the result of the comparison to the VCO via the Filter VCO Control.

### 1.3.3 Filter VCO Control

The Filter VCO Control attenuates the high-frequency error components of the PU/-PD and inputs the corrected signal to the VCO (via the VCO IN line).

### 1.3.4 VCO

The Voltage Controlled Oscillator is a voltage to frequency converter used to provide a clock which is at the same frequency and phase as the raw data. The clock's frequency is determined by the PU/-PD signal.

### 1.3.5 Data Separator and Synchronization

The Data Separator and Synchronization block generates the NRZ output from the delayed data and the clock generated by the VCO.

### 1.3.6 Write Encode and Clock Multiplexer

This block converts NRZ data (from the Data Sequencer) into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal can then be used to record information on the disk. When AM-ENABLE is active, a clock pulse will be deleted in the outgoing MFM stream in order to record Address Marks on the disk. In addition, precompensation signals are generated, when needed, for use in recording inner tracks.

SEQUENCE AFTER RD GATE TRUE EDGE:

1. Wait for 8 read raw pulses at high frequency; if not, retriggerable 1-shot will time-out and restart sequence.
2. Set lock to data: disable VCO for 2 read raw pulses and start VCO in phase with read raw.
3. Wait for 24 more read raw pulses at high frequency; if not, retriggerable 1-shot will time-out and restart sequence.
4. Set Search Address Mark and output VCO/2 to RD/REF clock. Wait for a "1" or 96 more read raw pulses. If no "1", restart sequence.
5. If "1" is detected, Adress Mark Found and lock up or 12 raw read pulses and restart sequence.

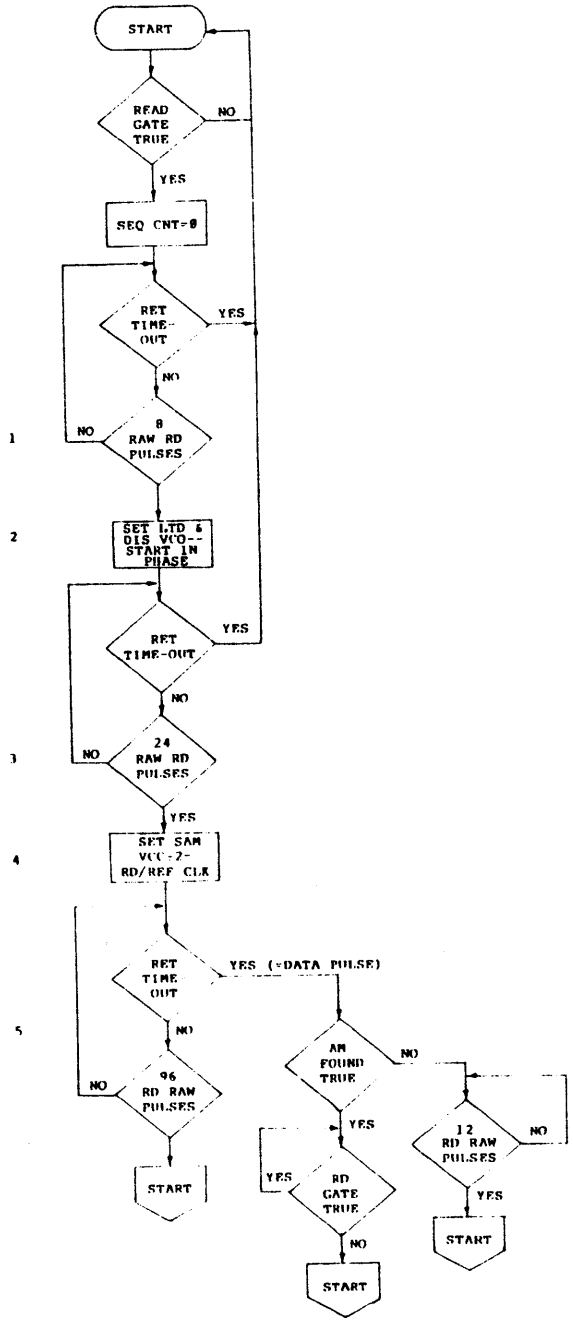


**Figure 2. Flow Chart of Search Sync Mode**

## 1.4 SYSTEM CONFIGURATION

Illustrated below is a typical system configuration, incorporating the VCO/Encode/Decode chip, the 5050 Data Sequencer, and the 5060 Memory Controller. Figure 4 shows all the external RC circuitry for a standard 5 MHz interface.

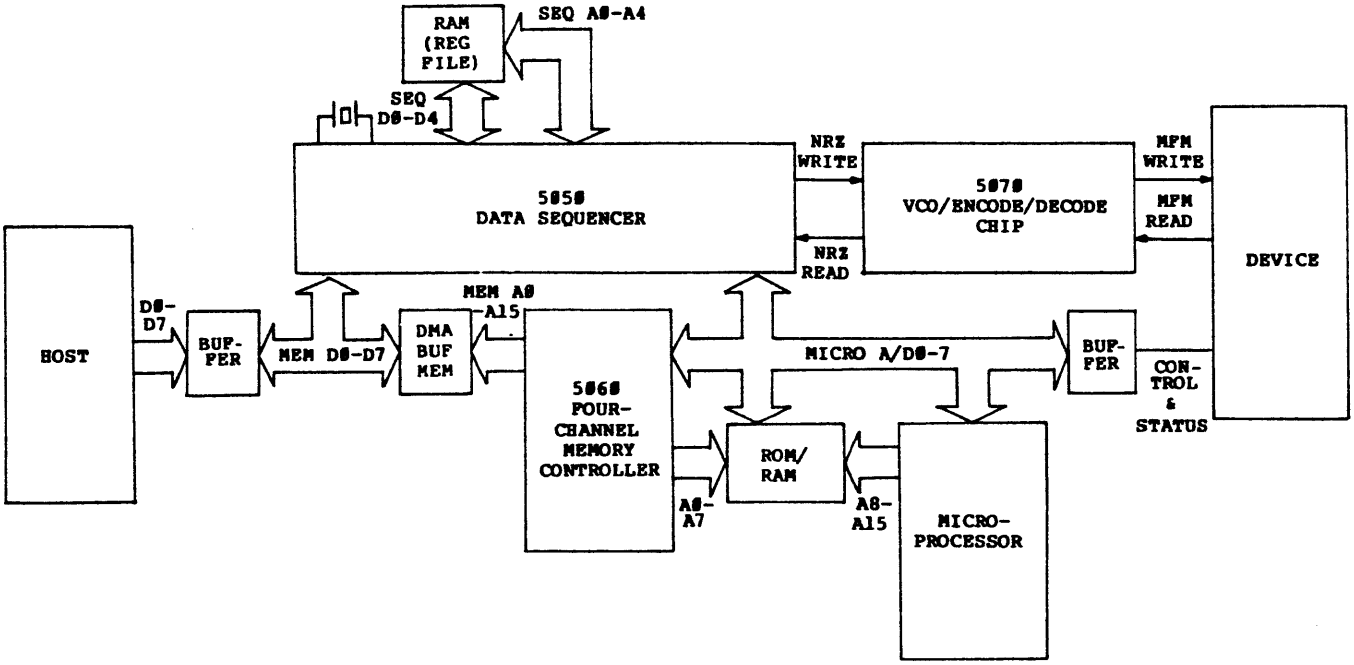


**Figure 3. Typical System Configuration**

### 1.4.1 Disk Interface

The disk interface consists of the MFM OUT line containing MFM-encoded data written to the disk, and the RD RAW line containing the MFM-encoded data to be translated to NRZ and input to the Data Sequencer.

### 1.4.2 Data Sequencer Interface

Three pairs of lines connect the 5070 with the 5050 Data Sequencer. These lines serve to transmit NRZ serial data between the two chips, enable the encoding and decoding of Address Marks, and provide various clock pulses to coordinate the data transfer.

### 1.4.3 Microprocessor Interface

The ENPRECOMP signal from the microprocessor enables precompensation for write operations on inner disk tracks.

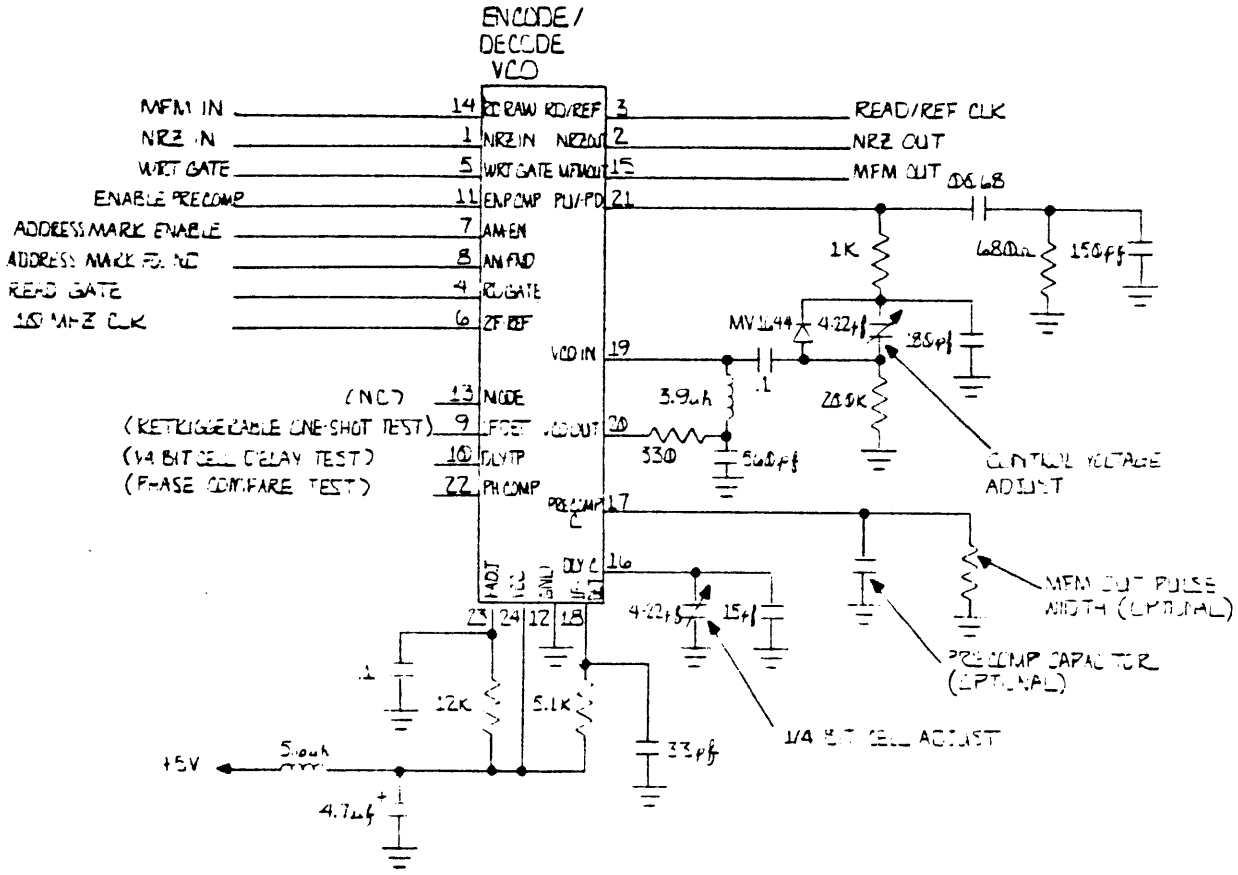


**Figure 4. VCO Encode/Decode External RC Circuitry**

# CHAPTER 2

# INTERFACING

## 2.1 SIGNAL DESCRIPTIONS

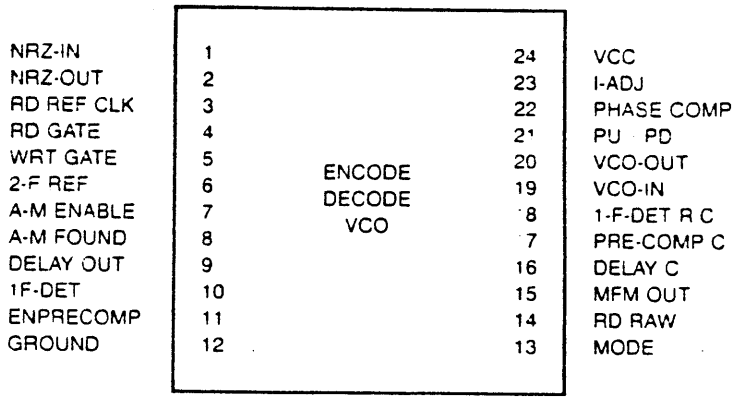


**Figure 5. Pin Assignments**

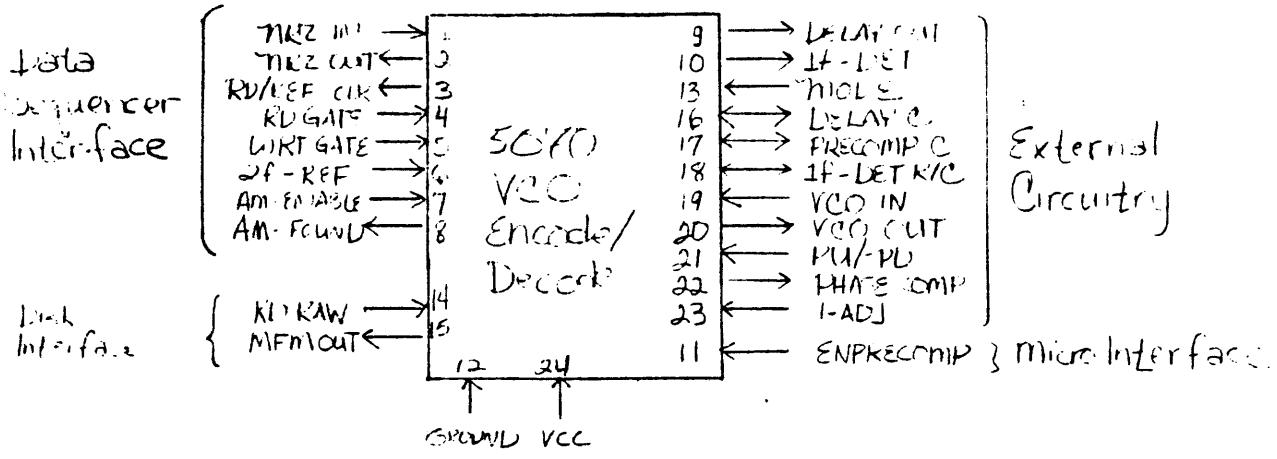


**Figure 6. Pin Functions**

**Table 1. Pin Descriptions**

| Symbol | Type | Pin # | Name and Function |
|---|---|---|---|
| 1-F DET | O | 10 | 1-f Detect. (Active High.) This test output is used to calibrate the retriggerable One-Shot RC used for the Preamble detect circuit. |
| 1-F DET RC | I/O | 18 | 1-f Detect Connect RC. (Active High.) This I/O line is connected to the junction point between a resistor to VCC and a capacitor to GND. This circuit is used for the retriggerable One-Shot that detects the 1-f used for VCO sync in the Preamble. |
| 2-F REF | I | 6 | 2-f Reference Clock. (Active High.) When RD GATE is false, this signal is divided by 2 and output on the RD/REF clock line. |
| A-M ENABLE | I | 7 | Address Mark Enable. (Active High.) When both this signal and WRT GATE are active, A-M ENABLE encodes an Address Mark (a special byte with a missing clock pulse). When A-M ENABLE is true and RD GATE is active, the Data Sequencer is locked from resyncing, thus placing the sequencer in external sync detect mode. |
| A-M FOUND | O | 8 | Address Mark Found. (Active High.) This output line goes High after RD GATE goes High and the missing clock pattern of the Address Mark is detected. The Data Sequencer uses this signal for byte synchronization during Read operations. |
| DELAY C | I/O | 16 | Delay Cell. (Active High.) This I/O pin is connected to a variable capacitor used to generate the 1/4-bit cell delay. |
| DELAY OUT | O | 9 | Delay Output. (Active High.) This test output is used to calibrate the One-Shot RC used for the 1/4-bit cell delay circuit. |
| ENPRECOMP | I | 11 | Enable Precompensation. (Active High.) When active, this signal enables precompensation for disk write operations on inner tracks. When this signal is inactive, write precompensation is disabled. |

**Table 1. Pin Descriptions, continued**

| Symbol | Type | Pin # | Name and Function |
|---|---|---|---|
| I-ADJ | I | 23 | Input Adjust. (Active High.) This input provides the current reference for all constant current controlled elements of the chip, i.e. phase comparator, PU/-PD signal, 1/4 bit cell delay, and write precompensation circuitry. An external fixed resistor from 5 V connected to this pin determines the constant current value. |
| MFM OUT | O | 15 | MFM Write Data. (Active High.) This signal is the MFM-encoded data output when WR GATE is active. |
| MODE | I | 13 | Mode Enable. (Active High.) When Low, this signal enables the VCO lock sequencer to lock to data after 1 clock of 2-f, and also sets Search Address Mode after 8, rather than 32, clock cycles. |
| NRZ IN | I | 1 | NRZ Serial Input. (Active High.) This serial data input line is the output from the Data Sequencer. This input must be at the data rate of the read/reference clock. |
| NRZ OUT | O | 2 | NRZ Serial Output. (Active High.) This signal is the serial output to the Data Sequencer. This signal must be at the data rate of the read/reference clock. |
| PHASE COMP | O | 22 | Phase Compare. (Active High.) This output is used for calibration of the 1/4-bit cell delay. |
| PRECOMP C | I/O | 17 | Precomp Capacitor. (Active High.) This I/O line is connected to an external capacitor used to generate the write precompensation delay time when precompensation is enabled. |
| PU/-PD | I | 21 | Filter Source/-Sink. (Filter Source active High; -Sink active Low; 3-state.) This 3-state output will be enabled High when the phase comparator requires a VCO increase in frequency, and will be enabled Low when the phase comparator requires a VCO decrease in frequency. The active High or Low current source/sink is proportional to the I-ADJ signal. |

**Table 1. Pin Descriptions, continued**

| Symbol | Type | Pin # | Name and Function |
|---|---|---|---|
| RD GATE | I | 4 | Read Gate. (Active High.) The transition of this signal from Low to High configures the chip in Search Sync mode (see Figure 4). During the Search for Address Mark phase of the Search Sync mode (VCO is locked), this signal selects the VCO clock/2 to be present at the RD/REFCLK line. |
| RD RAW | I | 14 | Read Raw Data. (Active High.) This input is the raw data containing both clock and data pulses output from the disk drive. |
| RD/REFCLK | O | 3 | Read/Reference Clock. (Active High.) This multiplexed output is used by the Data Sequencer for both read and write clock. The 2-f reference clock/2 will be present at this line when RD GATE is false. When RD GATE is true during the Search for Address Mark phase (VCO is locked), the VCO clock/2 will be present at this line. |
| VCO IN | I | 19 | VCO Input. (Active High.) This signal is the output of the VCO controlled by the charge-pump delay of the VCO output. |
| VCO OUT | O | 20 | VCO Output. (Active High.) This signal is used for the VCO source with the delay controlled by the charge-pump, and feed-back in the VCO input. |
| WRT GATE | I | 5 | Write Gate. (Active High.) When active, this signal enables encoding of NRZ serial data to MFM encoded data. |
| VCC | I | 24 | VCC. +5 V. |
| GND | I | 12 | Ground. |

## 2.2 TIMING

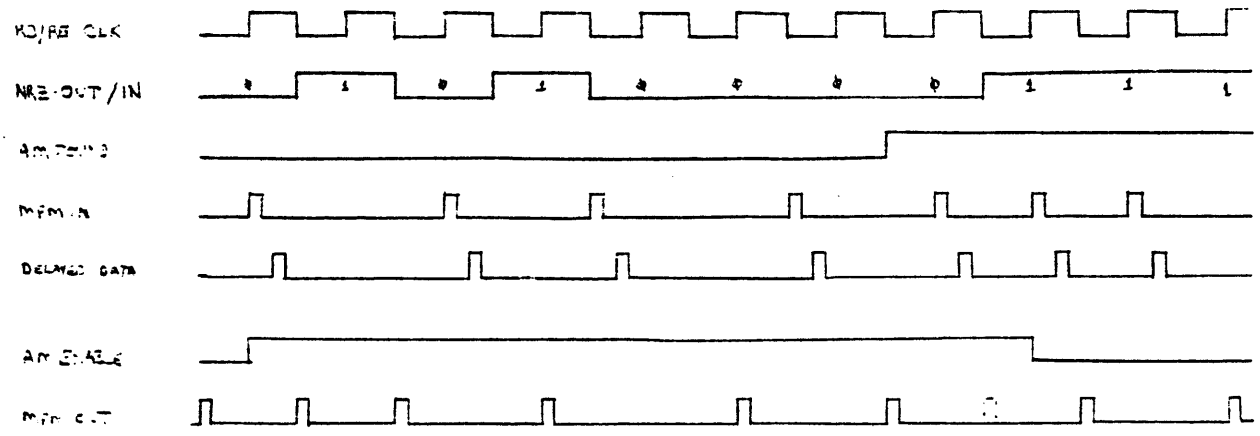

**Figure 7. VCO/Encode/Decode Timing**

## 2.3 D.C. INFORMATION

### 2.3.1 Absolute Maximum Ratings

- Voltages on all pins with respect to GND range from -Ø.3 V to +7.Ø V.
- Ambient operating temperature is Ø°C to +7Ø°C.
- Storage temperature ranges from -65°C to +15Ø°C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

### 2.3.2 Standard Test Conditions

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

- +4.75 V < VCC < +5.25 V
- GND = Ø V
- Ø°C < TA < +7Ø°C

### 2.3.3 D.C. Characteristics

| Parameter | Min | Max | Unit | Condition | Notes |
|---|---|---|---|---|---|
| Input High Voltage | 2 | VCC | V | | |
| Input Low Voltage | -Ø.3 | Ø.8 | V | | |
| Output High Voltage | 2 | VCC | V | | |
| Output Low Voltage | | Ø.4 | V | | |
| Input Leakage | -3Ø | 1Ø | uA | | |
| Output Leakage | | 1Ø | uA | | |
| VCC Supply Current | | 5Ø | mA | | |

## 2.4 PACKAGE DIMENSIONS

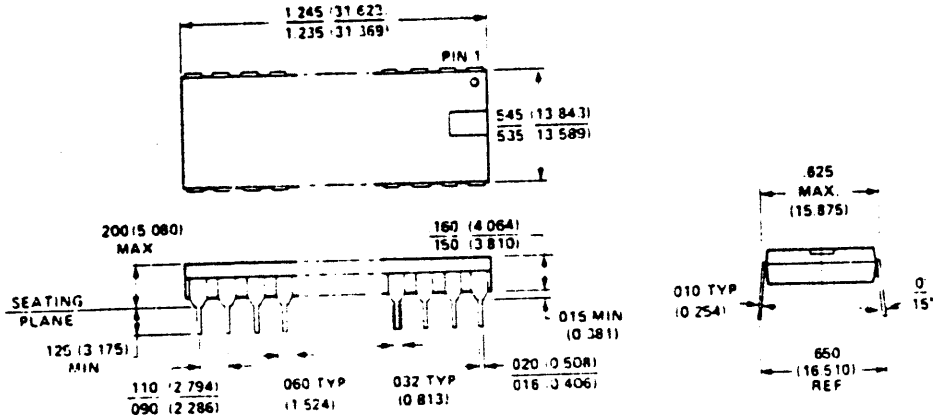


Figure 8. Package Dimensions